96711900

CONTROL DATA CORPORATION

CDC® TAPE CASSETTE CONTROLLER

FA104-A

GENERAL DESCRIPTION
OPERATION
INSTALLATION
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE REFERENCE/MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released.
(10/76)	
B	Manual revised; includes Engineering Change Order 14823, improving check-out capabilities and correcting
(6/77)	documentation.
C	Manual revised to incorporate field print package FA104-A; when this revision package is incorporated the completed
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or use Comment Sheet in the back this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
FA104-A	01	ECO 14559 ECO 14436 ECO 14342	
	02	ECO 14559	
	03	ECO 14823	

LIST OF EFFECTIVE PAGES

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PREFACE

This manual provides programming reference and maintenance information relative to the CONTROL DATA® Tape Cassette Controller. The tape cassette controller provides communication between the FA104-A cassette and a CYBER 18 processor.

The manual is intended to serve programmers and customer engineers who require detailed machine-level information about the tape cassette controller. Detailed information regarding system-level programming and maintenance is provided in system reference/maintenance manuals.

Additional information may be found in the following publications:

Publication	Publication Number
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
Basic Micro-Programmable Processor Hardware Maintenance Manual	39451400
CYBER 18 Computer Systems Central Processor Field Repair Guide	60475001
CYBER 18 Computer Systems Overview Manual	60475000
Micro-Programmable Computer Family Hardware Reference Manual	88973400
Tape Cassette Subsystem Hardware Maintenance Manual	60475060
CYBER 18 Equipment Cabinets Hardware Reference/Maintenance Manual	96768280

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FIGURES

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This manual contains hardware maintenance and programming reference information relative to the peripheral I/O controller for cassette-to-central processing unit communication. The hardware information is provided to help maintenance personnel understand the functional operation of the cassette controller. The programming information provides reference data to help programming personnel understand the controller's operational characteristics. This controller has been designed to meet the European Computer Manufacturers Association (ECMA-34) standard for data interchange on a 3.81 millimeter magnetic tape cassette.

PHYSICAL AND FUNCTIONAL DESCRIPTION

PHYSICAL DESCRIPTION

The cassette controller (figure 1-1) is a four-layer printed circuit board that measures 11 by 14 inches. The board contains capacitors, resistors, and integrated circuits to produce the logic functions required to control two tape transports and provide a communication link between a CYBER 18 processor and a magnetic tape cassette. The controller is installed in one of the processor's I/O peripheral controller slots (A/Q or A/Q-DMA) and is accessed via the associated equipment designation.

FUNCTIONAL DESCRIPTION

The cassette controller is capable of interfacing with one or two tape transports and receives address, data, and discrete signals from the central processing unit (CPU) via the I/O-TTY controller. The controller may be status- or interrupt-driven at the macro level, and data transfer may also take place in the automatic data transfer mode at the micro level. Figure 1-2 is a functional block diagram of the operation of the cassette controller.

Data Transfer

Data transfer of read information from a tape cassette or write information to a tape cassette is via the A/Q channel of the central processing unit. The A/Q channel operations result in a series of actions by the controller and/or tape transport.

Write

When the cassette is inserted into the selected transport, the lid is closed, and the automatic rewind feature is enabled, the following sequence occurs. If side B is active, the side B status is provided to the CPU. The tape rewinds to the transparent leader, stops, and winds forward until the beginning-of-tape (BOT) hole is sensed (figure 1-3). Tape motion stops, beginning-of-tape status occurs, and the READY indicator on the operators panel illuminates. When a function command directing a write motion is issued, forward tape motion begins to bring the tape up to speed. After the tape reaches the proper data transfer speed, the data or tape mark is recorded in serial format for one record. A record format consists of an inter-record gap (IRG), preamble, data, cyclic redundancy check (CRC), postamble, another inter-record gap; a tape mark record does not contain data (figure 1-4). Record data is transcribed on the tape in Manchester code (phase transition) format (figure 4-10).

Read

To read a record, the controller senses the phase transitions appearing on the tape and converts them to ASCII codes. The detected phase transitions are processed to extract only the character data; the preamble, cyclic redundancy check, and postamble are discarded within the controller logic. The character data transitions are converted to ASCII codes (D00 through D07 data bits) and are coupled by lines RD01 through RD08 to the I/O-TTY controller. The I/O-TTY controller transfers the character data and status function data to the central processing unit via the three-state bus. Controller, tape, and transport status is coupled to the I/O-TTY controller via lines RD01 through RD16 (refer to Status Functions in section 2).

Automatic Data Transfer

The controller performs automatic data transfer (ADT) operation whenever the ADT mode is designated. The requested operation (write or read) occurs as described under write and read control of the micro and macro interrupts. In this case, the A/Q channel then provides/accepts a character. This intermittent operation sequence continues until the terminate signal is received to inhibit the interrupts and thereby terminate the sequence.

Deadstart

When the controller is inserted into a micro processor peripheral I/O slot that is connected for deadstart operation, prerecorded cassettes can be read into the CPU via the asynchronous serial data path to the breakpoint controller at a rate of 9600 baud. The deadstart read operation occurs as described for a read operation, but instead of being transferred via the RD lines to the I/O-TTY controller, the data is transferred from the deadstart output register to the breakpoint controller.

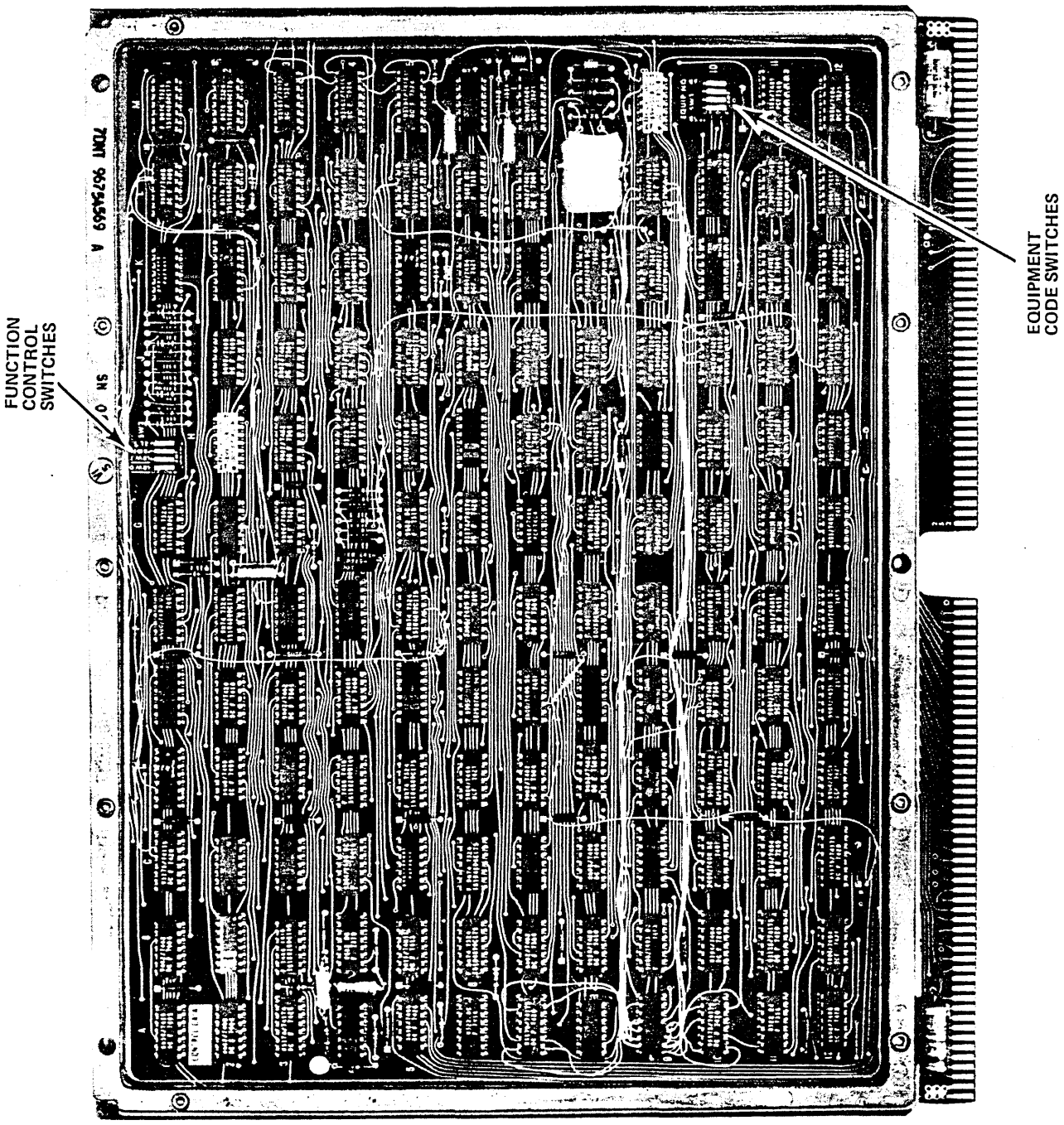

Figure 1-1. Tape Cassette Controller

Echo

Echo mode places the data path in loopback and tests the controller without operation of the transport. Operation starts as in a write operation and terminates as in a read operation. This loopback operation continues until the CPU stops sending data. Echo mode is reset when a clear controller is received.

REFERENCE DATA

POWER REQUIREMENTS

Controller:	+4.75 to 5.25 volts at 2.4 amperes
Transport: (each)	+4.8 to 5.2 volts at 1.6 ampere

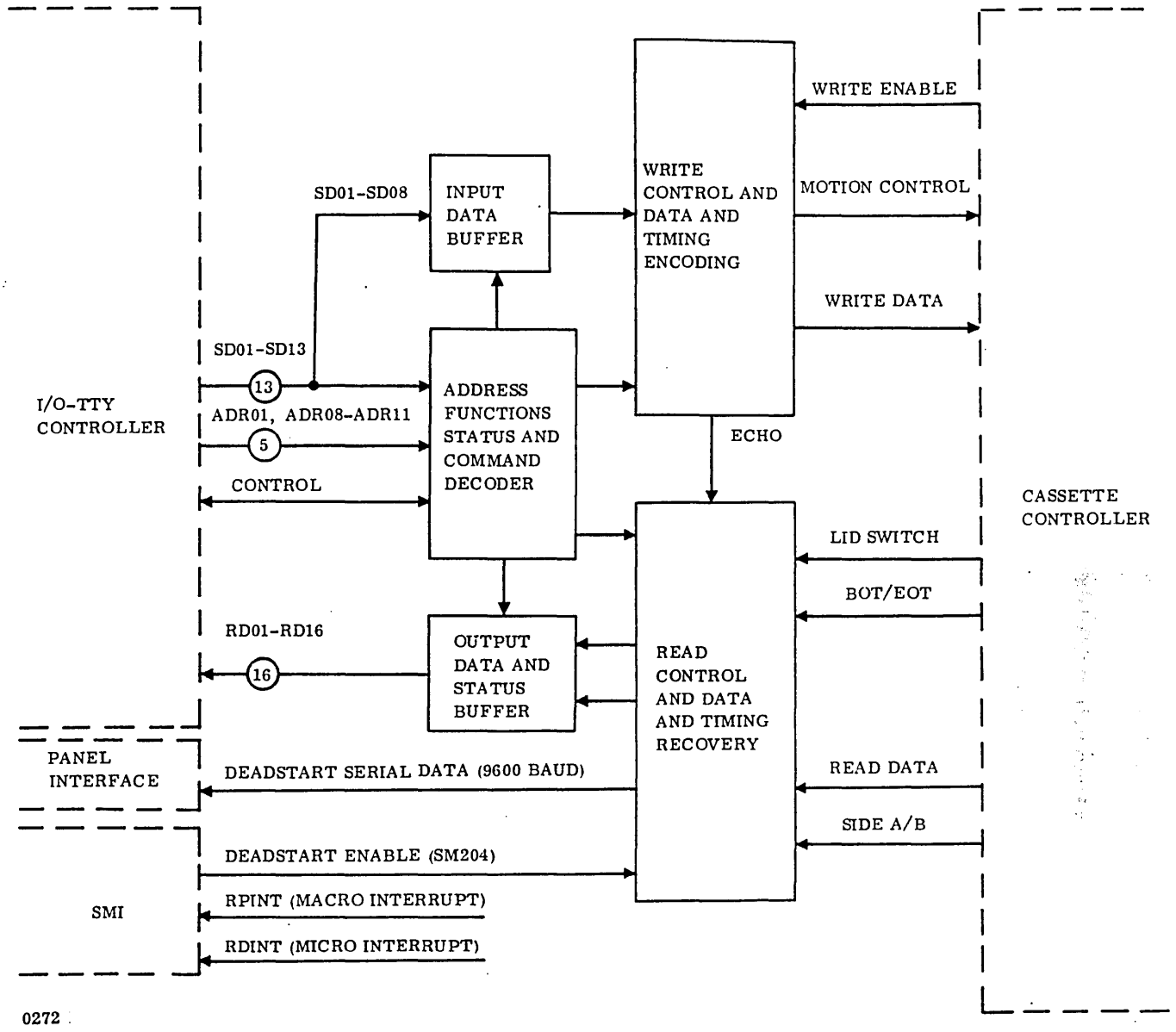

Figure 1-2. Tape Cassette Controller Functional Block Diagram

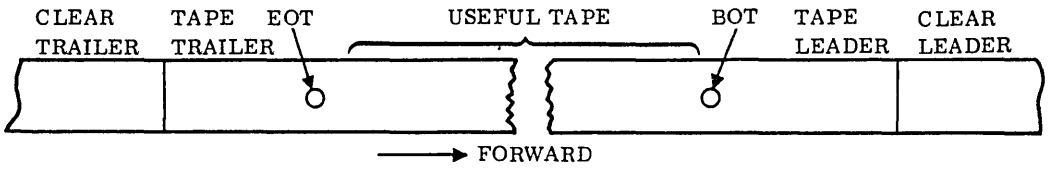

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Figure 1-3. Tape Structure

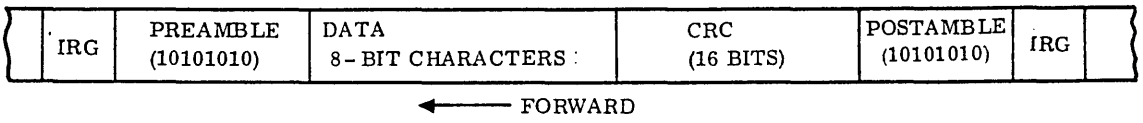

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Figure 1-4. Record Format

+11.2 to 12.48 volts at 1.7 amperes

1.25 amperes peak

-11.2 to 12.48 volts at 0.1 amperes

TRANSFER CHARACTERISTICS

Transfer format:

Write data – Parallel (8-bit characters) from CPU to controller
Serial (Manchester code†) from controller to tape

Read data – Serial (Manchester code†) from tape to controller
Parallel (8-bit characters) from controller to CPU

Deadstart:

Read data – Serial (Manchester code†) from tape to controller
Serial (ASCII code) from controller to breakpoint controller

Transfer rate:

Read or write: – 750 characters per second (character equals eight bits)

Deadstart – 9600 baud from controller to breakpoint controller

†Manchester code is a phase transition, nonreturn-to-zero format.

TAPE CHARACTERISTICS

Industry standards: ECMA34/ANSI x 3B1-638 (Phillips-type digital cassette tape)

Inter-record gap:

Start – 240 milliseconds (nominal)
Equals 0.75 in. (1.9 cm) tape length

Stop – 76 milliseconds (nominal)
Equals 0.55 in. (1.4 cm) tape length

Tape speed:

Start – 1.65 in. (4.2 cm) per second

Operational – 7.5 in. (19.1 cm) per second

Fast – 50 in. (127 cm) per second

Slow – 7.5 in. (19.1 cm) per second

ENVIRONMENT

Operating:

- Controller

  Temperature – 32° to 122° F (0° to 50° C)

  Altitude – Sea level to 10,000 ft. (3100 m)

  Humidity – 10 to 90 percent relative humidity at 104° F (40° C) (noncondensing)

- Transport

  Temperature – 50° to 113° F (10° to 45° C)

  Altitude – Sea level to 10,000 ft. (3100 m)

  Humidity – 20 to 80 percent relative humidity at 104° F (40° C) (noncondensing)

This section contains functional descriptions of internal and external controls, external indicators, and programming reference material (word-bit definitions) for the tape cassette controller. External controls and indicators are optional items applicable to the system configuration. Internal controls refer to the switches installed on the controller. The internal switches are used primarily for maintenance purposes. When the internal switches are changed from the initial installation setting for checkout purposes, they must be reset to their original positions before the controller is released for system operation. If a replacement cassette controller is installed in a system, these switches must be set in the same positions they were in on the removed controller.

CONTROLS AND INDICATORS

CASSETTE CONTROLLER

Equipment Code

The equipment code (figure 2-1) is a four-segment dual inline package (DIP) switch (SW1; location M10, figure 1-1) and is used to set the equipment code (E field) address of the controller. This setting is applicable only to the system in which the controller is presently installed. The switch is set when the controller is installed and is not normally changed as long as the controller remains in the system.

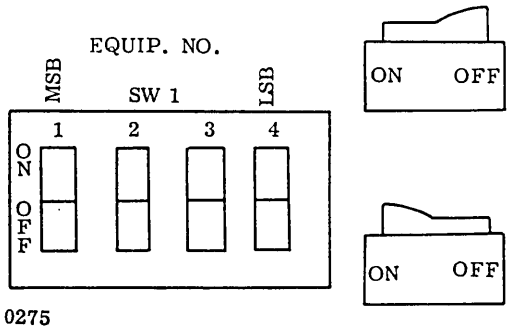


Figure 2-1. Equipment Code Selector Switch (SW1)

A four-segment DIP switch (SW2, location H1, figure 1-1) is used to establish the following modes of operation (figure 2-2 and table 2-1).

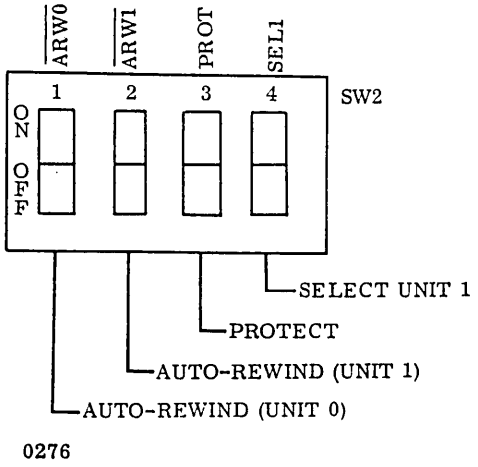


Figure 2-2. Control Functions Selector Switch (SW2)

Automatic Rewind (A-Rwnd) Enable

The unit 0 and unit 1 switches are segments 1 and 2 of DIP switch SW2. When a switch is ON, the auto-rewind feature for unit 0 or 1 is operational. When one of the switches is OFF, the auto-rewind feature for units 0 or 1 is not operational.

NOTE

The controller function commands are always operational and are independent of these switch settings.

The unit 0 switch enables/disables the auto-rewind feature for unit 0. This switch facilitates edit operations in systems with only one transport and permits sequential loads of diagnostic overlays (for example, for systems containing more than one deadstart device).

The unit 1 switch enables/disables the auto-rewind feature for unit 1. Thus, in a two-transport system, it is possible to have the auto-rewind feature operative on only one of the units, if auto-rewind is desired. Auto-rewind on unit 1 is not usable unless the unit 1 over-ride switch is enabled.

TABLE 2-1. CONTROL FUNCTIONS (SW2)

Position	Segment 1	Segment 2	Segment 3	Segment 4
ON	Auto-rewind enabled (unit 0)	Auto-rewind enabled (unit 1)	Selects protected mode	Selects unit 1
OFF	Auto-rewind inhibited (unit 0)	Auto-rewind inhibited (unit 1)	Selects unprotected mode	Normal unit selection occurs

Protect Switch

The protect switch (table 2-1) is segment 3 of DIP switch SW2.

When the switch is off, the controller ignores the program protect line state from the CPU and accepts all I/O instructions such as function, status, and data transfer commands (when unprotected, the controller never rejects a function, status, or data transfer command because of the program protect condition).

When the switch is on, the controller monitors the program protect line from the CPU. The controller's response to the I/O instruction is then determined by the state of the program protect line as follows.

- If the program protect line indicates that the I/O instruction is unprotected, then the controller generates a reject for each function and data transfer command. Note, however, that a status command is never rejected because of the program protect condition (or any other condition).
- If the program protect line indicates that the I/O instruction is protected, then a reply response is enabled for all commands (function, status, and data transfers). Note that the controller does not actually return a reply until all other conditions indicate that a reply is permissible.

Select Unit 1 Switch

The select unit 1 switch is segment 4 of DIP switch SW2.

When the switch is on, all of the normal unit select controls are ignored and unit 1 is connected to the controller. Unit 0 can never be connected to the controller when the select unit 1 switch is on.

When the switch is off, all normal unit select controls (master clear, clear controller, and unit select function commands) are in effect; they determine which unit is connected to the controller.

NOTE

Normally this switch is never on. It is furnished to aid in loading prerecorded deadstart routines from unit 1. In a two-transport system, unit 0 would always be used to load deadstart routines unless the transport is not in service, when deadstart routines can be easily loaded from unit 1 by setting this switch to on and master clearing the processor. However, as soon as unit 0 is once again available, this switch should be set to off and the processor master cleared.

CASSETTE TRANSPORT

Lid Switch

The lid switch senses whether the protective lid on tl transport is open. This signal is part of the interlock sign that is sent back to the transport; therefore, when the lid open, the interlock signal causes the transport to go n ready. Conversely, when the protective lid is closed (tl cassette is loaded and +5 volts is available at the transport the transport is ready. This signal is also used in tl selected controller to automatically initiate the rewi sequence whenever the lid is closed and the auto-rewi enable switch is on.

Side A/B Switch

The side A/B switch senses whether the cassette is load with the side A or side B track positioned under tl read/write head. This signal is used in the controller as status bit.

Write Enable Switch

The write enable switch senses the presence or absence the cassette write plug for whichever track is position under the read/write head. This signal is used in tl controller to cause illegal motion commands to reject and part of the write select signal that is sent back to tl transport. When the write plug is missing, the write enab signal causes the write select signal to inhibit the write he at the transport.

EXTERNAL CONTROLS AND INDICATORS

Deadstart Switch

The deadstart switch on the operators panel is connected via DS-SWNC and DS-SWNO. When this switch is activated, it sets the deadstart signal (SM204), which is then sent to the cassette controller and to any other controller wired on the deadstart bus. If the controller is ready, this action may initiate the deadstart operation (see Deadstart in section 4 for operation).

D/S ACTIVE Indicator

The D/S ACTIVE indicator† on the operators panel displays the status of the deadstart signal (SM204).

READY Indicator

The READY indicator† on the operators panel displays the following information to the operator:

- The selected unit is ready.
- No CRC/format errors have been detected.
- The rewind sequence is not active.

UNIT 0 SELECT Indicator

In a two-transport system, the UNIT 0 SELECT indicator† on the operators panel illuminates whenever unit 0 is selected. This indicator is not used in a system with only one transport.

UNIT 1 SELECT Indicator

In a two-transport system, the UNIT 1 SELECT indicator† on the operators panel illuminates whenever unit 1 is selected.

External Auto-Rewind

Provision for an external auto-rewind is included on the controller. If pin 34 on the backplane connector is grounded via a logical low (0.4 volts or lower) an auto-rewind cycle on the selected unit takes place. The signal must be of short duration – 10 microseconds or less.

The controller provides this capability. The presence of these indicators is dependent upon the installation.

PROGRAMMING INFORMATION

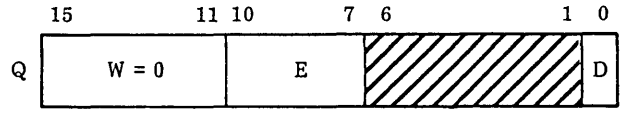
This tape cassette controller employs the CDC convention of address, control, and status functions of the CPU A/Q registers. Actual designations of the A/Q register counterparts within the controller are SD for A-register bits and ADR for Q-register bits. The send line (SD01 through SD13) and read line (RD01 through RD16) bits represent the A00 through A15 bits of the control and status function words. The ADR01 and ADR08 through ADR11 bits represent the Q00 and Q07 through Q10 bits of the address words.

CASSETTE CONTROLLER INPUT/OUTPUT BIT DESCRIPTIONS

Addressing

The equipment address is defined by the E field of the CPU A register (Q10 through Q07). This address is specified by selecting the positions on the four-segment switch, SW1, located on the controller card. The W field of the Q register (Q15 through Q11) must be zero.

The D field of Q, Q register bit 0, is combined with the computer's I/O instructions to specify an operation:



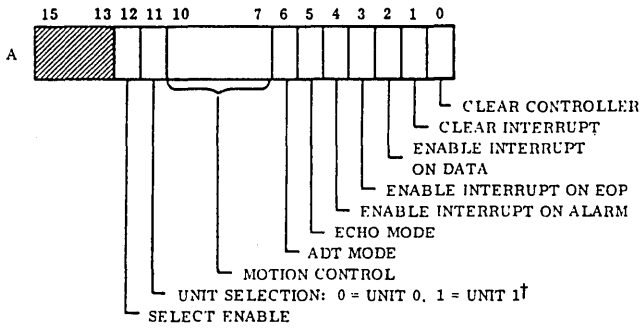
	Computer Instruction	
D Field (Q00)	Output from A (OUT)	Input to A (INP)
0	Write data transfer	Read data transfer
1	control function	status

A-REGISTER CONTROL FUNCTIONS

When Q register bit 0 equals 1 and is accompanied by both an equipment address and an A-register instruction, the control function specified by the bits of the instruction are performed. The control functions are shown in figure 2-3.

Clear Controller

If set, A-register bit 0 functions as a momentary master clear and clears all interrupt conditions (A-register status bits A03 through A06, A08, A09, and A14), all interrupt enables (set with A-register function bits A02 through A04), and the interrupt responses (macro and micro interrupt lines, RPINT, and RDINT) between the controller and CPU interrupt hardware. In addition, this command clears motion requests, tape mark status, ADT mode, and echo mode.



†A MANUAL SWITCH ON THE CONTROLLER CARD CAN OVERRIDE THIS FUNCTION BIT AND FORCE UNIT 1 TO ALWAYS BE SELECTED.

Figure 2-3. CPU Control Function Bit Assignments Relative to the Cassette Controller

A function code in which A-register bit 0 and any of bits A01 through A11 are set first clears all previous functions and then honors the function conditions indicated by bits A01 through A11. In other words, director functions may be stacked. Whenever stacked functions are issued, it is possible to have a mixed response to the function command; reply and reject conditions can exist simultaneously. When this happens, the response is always a reject. Whenever a reject is the response to an output function command, the function command is not honored; whenever the response to the director function is a reject, the clear controller command will not be honored.

NOTE

If status bit A05 is set due to a not ready condition, the alarm status bit and related interrupt, if re-enabled, is not cleared with this command.

Clear Interrupt

If set, bit 1 clears the interrupt responses between the cassette controller and the CPU by clearing all interrupt enables. However, the command does not clear the interrupt conditions, which are still available as status bits (A03 through A06, A08, A09, and A14).

If an interrupt enable (function bits A02, A03, and/or A04) is coded along with a clear interrupt, that selection is honored but any previous selections are cleared.

This command is not honored when a reject occurs.

Enable Interrupt on Data

If set, bit 2 enables an interrupt whenever the controller has data available (read) or requests data (write). Data interrupts are normally cleared by accepting or providing the data. They may also be cleared by master clear, clear controller, or clear interrupt commands. If A-register bit 2 equals 0, the data interrupt enable is unchanged.

In ADT mode, the interrupt response, resulting from a data interrupt condition, between the controller and the CPU is a micro interrupt (RDINT line). In non-ADT mode, the interrupt response is a macro interrupt (RPINT line).

Enable Interrupt on End-of-Operation

If set, bit 3 enables an interrupt when the controller has completed a motion command. The interrupt occurs when the controller becomes not busy. End-of-operation interrupts are normally cleared when a new motion command is received. They may also be cleared by master clear, clear controller, or clear interrupt commands. If A-register bit 3 equals 0, the end-of-operation interrupt enable is unchanged. A unit select operation also generates an end-of-operation. When selecting ADT mode, end-of-operation interrupts must be enabled or a reject occurs.

Enable Interrupt on Alarm

If set, bit 4 enables an interrupt when an alarm condition occurs. When enabled, the alarm interrupt is generated by any of the following conditions:

- End-of-tape (status bit A09=1)
- Transport not ready (status bit A00=0)
- Overflow (lost data during read) (status bit A06=1)
- Underflow (lost data during write) (status bit A06=1)
- CRC error (status bit A08=1)
- Format error (status bit A08=1)
- Runaway (no status)

Alarm interrupts normally are cleared when a new motion command is received. If the alarm is due to an end-of-tape condition, a reverse motion command (search tape mark (reverse), backspace, or rewind) is required to clear the interrupt. If the alarm is due to a transport not ready condition, no motion commands can be issued. Alarm interrupts may also be cleared by master clear, clear controller, or clear interrupt commands. If A-register bit 4 equals 0, alarm interrupt enable is unchanged.

Echo Mode

If set, bit 5 causes the controller to internally loopback the data path. Data normally sent to the cassette becomes data from the cassette. In this way, the integrity of the controller write and read logic can be tested independently of the transport.

When the command is given, the regular write data sequence is initiated except that no tape motion occurs since the transport is forced to a not ready condition. If tape motion commands are included in the same function word as the echo mode command, they are ignored by the controller, and

the controller goes into the echo mode of operation. Since ADT mode and echo mode operations are incompatible, commands in which both modes are selected cause a reject and neither mode is selected. Echo mode cannot be selected while the controller is busy.

As in a normal write operation, an immediate data request and the related interrupt, if enabled, is generated with the echo mode command, and the controller goes busy. Approximately five character-times after the transport start-up delay times out, the data that was output earlier to the controller has completed looping back and becomes available to the CPU.

In echo mode, the difference between data request and data available (status bit 3 and related interrupts when enabled) is determined by noting whether data available status bit 14 is also set.

As in a normal write data operation, the record continues until a data underrun condition is reached; the controller then initiates the normal shutdown sequence (write CRC and postamble). The controller continues to operate in echo mode until all data, CRCs, and postamble fields have been looped back and all data that was output has been made available to the CPU. Approximately four character-times after the last data was output, the last data available appears. Within one character-time after the last data available sets, the read logic detects the end-of-record. Approximately 76 milliseconds later, the controller goes not busy and the end-of-operation status and the related interrupt, if enabled, occurs. Each mode is cleared by a master clear or a clear controller command.

ADT Mode

If set, bit 6 directs the controller to operate in auto-data transfer mode. To operate in ADT mode, the end-of-operation interrupt must be enabled (A-register bit 2 equals 1) in conjunction with either a read motion or a write motion command or the function is rejected.

ADT mode cannot be selected (or deselected) with this command while the controller is busy.

ADT mode operation is normally cleared by completing the operation. When the CPU generates STERM during the last data transfer, the controller is taken out of ADT mode and no further data interrupts occur.

If the controller is performing an ADT read operation when STERM occurs, the tape continues to move and data from the tape continues to be processed by the controller, but no further micro (data) interrupts are generated. No further data is input to the CPU. Once the end-of-record is reached, all normal error checks are performed and an end-of-operation interrupt is generated.

If the controller is performing an ADT write operation when STERM occurs, no further micro (data) interrupts are generated. No further data is output from the CPU and a data under-run condition develops; the controller goes into a normal shutdown sequence (write CRC and postamble) and an end-of-operation interrupt is generated.

ADT mode is also cleared by a master clear or a clear controller command.

A-REGISTER MOTION CONTROL BITS

Table 2-2 illustrates motion control bit designations.

TABLE 2-2. MOTION CONTROL BIT DESIGNATIONS

Bits				Function†
10	9	8	7	
1	0	0	0	Search tape mark (reverse)
1	0	0	1	Search tape mark (forward)
1	0	1	0	Write tape mark
1	0	1	1	Write one record
1	1	0	0	Backspace one record (or tape mark)
1	1	0	1	Rewind
1	1	1	0	Erase
1	1	1	1	Read one record

†Bits A07, A08, A09, and A10 control tape transport motion. The motion control commands can only be accepted when the tape transport is ready and the controller is in the not busy state.

Search Tape Mark (Reverse)

When bits 10 through 7 are set to 1000, the controller reads the tape, at 7.5 inches per second, in the reverse direction. When a tape mark is found, the tape transport stops. No data is transferred to the computer. If this command is issued and no tape marks are encountered before beginning-of-tape/ end-of-tape is encountered, the tape stops at the load point with the beginning-of-tape status bit set. This command cannot be used in the region of tape between the end-of-tape hold and clear trailer.

After tape motion ceases, the controller goes not busy and the end-of-operation interrupt, if requested, occurs.

Search Tape Mark (Forward)

Bits 10 through 7 set to 1001 direct the controller to read the tape in forward motion. When a tape mark record is found, the tape transport stops and no data is transferred to the computer.

After tape motion ceases at the end of the inter-record gap, the controller goes busy. The end-of-operation interrupt, if requested, occurs at this time.

Search tape mark (forward or reverse) is also cleared via a master reset or a clear controller command or if a tape runaway condition occurs.

Write Tape Mark

Bits 10 through 7 set to 1010 initiate the write tape mark operation. For this motion command, the computer does not go to data transfer mode (Q00=0), but handles all activities automatically without external influence. The sequence of events as the tape moves forward is:

Inter-record gap
Preamble
Cyclic redundancy check, all zeroes
Postamble
Inter-record gap

After tape motion ceases at the end of the inter-record gap, the controller goes BUSY. The end-of-operation interrupt, if requested, occurs at this time.

The write tape mark command is one of the illegal motion commands detected by the reply/reject logic. If write is disabled at the cassette (i.e., the write plug has been removed) when this command is issued, the write tape mark command is not honored and the controller responds with a reject to the CPU.

Write One Rec

If bits 10 through 7 a et to 1011, the write motion is initiated. The processor goes into transfer mode so that the data can be converted from eight bits parallel to serial form and be properly recorded on the tape (Manchester code) with preamble, data, cyclic redundancy check, and postamble.

Prior to writing the preamble, timing is established by a data request (and interrupt if enabled) issued by the controller. On request, one byte (eight bits) at a time is provided at the cassette controller's input buffer and the data request (interrupt) is reset so that the next byte can be requested at the proper time (figure 2-4).

Transfer continues until the next data character is unavailable from the A/Q channel when needed (i.e., under-run). This initiates shutdown (cyclic redundancy check, postamble, and inter-record gap). The sequence of recording one block (record) is as follows:

- The inter-record gap is defined as a dc polarity or blank area recorded on the tape before and after a given record. No clock or data transitions occur in the gap. Start delay is nominally 240 milleseconds; tape motion is nominally 0.75 inches (1.9 centimeters) per second.
- The preamble, 10101010, is eight bits (one character) in length and immediately precedes data in each block. The least significant bit (zero) is written first.
- Data is in eight-bit characters and may be of any length from one to 256. The least significant bit is written first.
- The cyclic redundancy check is the last two characters in the data portion of a data block. The 16-bit cyclic redundancy check is written in each data block immediately preceding the postamble. It is generated by the polynomial of $x^{16} + x^{15} + x^2 + 1$.
- Immediately following the cyclic redundancy check, th postamble 10101010 is written. The least significant bi is written first.
- The parameters are the same as for the initial inter record gap above. Stop delay is nominally 36.2 milleseconds; tape motion is nominally 0.34 inches/0.8 centimeters. After tape motion ceases at the end o the inter-record gap, the controller goes not busy. Th end-of-operations interrupt, if requested, occurs at thi time.

Following receipt of the tape motion command and prior t the preamble, the transport comes up to speed and write the leader inter-record gap in approximately 240 milli seconds. If, during this time, the first data character ha not been received from the A/Q channel, a tape mark i written. This accidental generation of a tape mark i accompanied by an alarm condition, plus a macro interrup if the alarm interrupts are enabled due to the underflo (during WRITE) status bit (A-register bit 6 equals 1) being set.

This command is also an illegal motion command if it i issued when write is disabled.

Backspace

If bits 10 through 7 are set to 1100, the tape moves backward (reverse) one record, either data or tape mark.

After tape motion ceases at the end of inter-record gap, the controller goes not busy. The end-of-operation interrupt, if requested, occurs at this time.

Note that if this command is issued and beginning-of-tape/end-of-tape is encountered during the backspace operation, the rewind sequence is initiated and the tape stops at the load point with the beginning-of-tape status set. This implies that the backspace command cannot be used in the region of tape between the end-of-tape hole and the clear trailer.

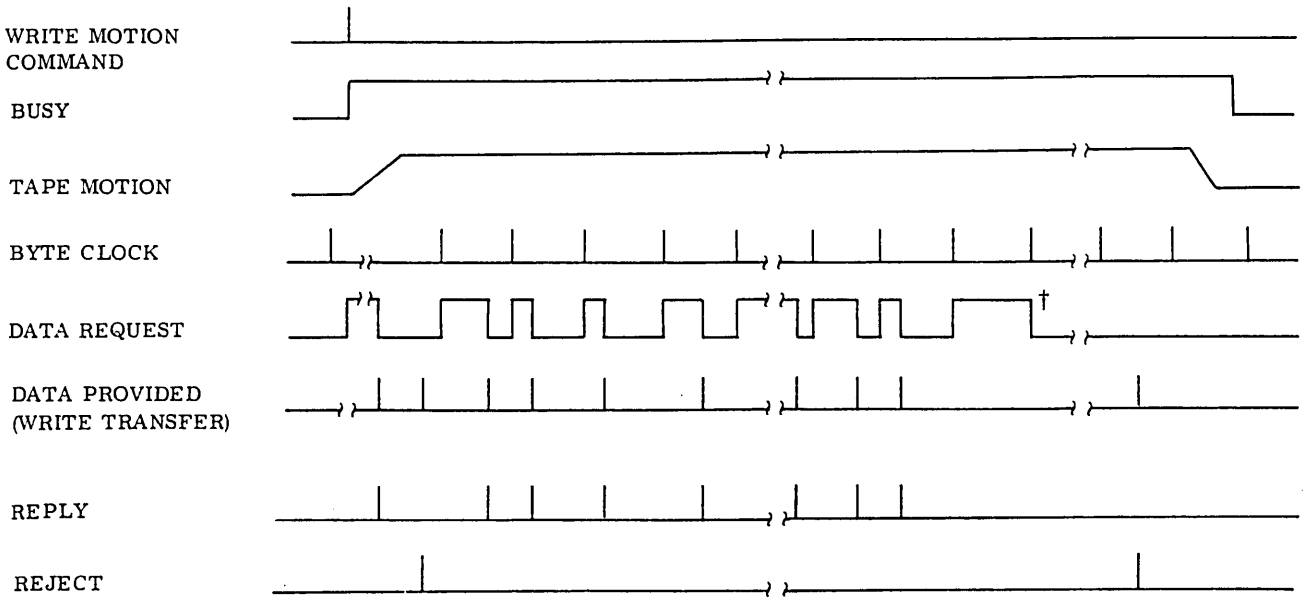
Rewind

If bits 10 through 7 are set to 1101, the tape rewinds to the beginning-of-tape position. The beginning-of-tape status bit is then on.

Cassette data tape consists of approximately 380 feet of 0.15-inch wide oxide-coated magnetic recording tape attached at each end to a 20-inch transparent plastic leader. A tiny hole is located approximately 18 inches in from each leader, designating beginning-of-tape or end-of-tape. Only one light sensor is available, and the distinction between the front transparent leader, the beginning-of-tape hole, the end-of-tape hole, and the ending transparent leader (trailer) must be determined using logical sequences and timing.

The tape rewind operations are as follows:

- If light is sensed the tape moves in the reverse direction at slow speed (7.5 inches per second) for three seconds.



† DATA UNDER-RUN DETECTED — START OF SHUTDOWN SEQUENCE

0277

Figure 2-4. Typical Write Timing Diagram

If light is still present, the sensor must be on the front transparent leader. The transport is then stopped for 80 milliseconds and moved forward at 7.5 inches per second until light is not sensed and then sensed again. This is the beginning-of-tape position, and all motion ceases slightly beyond the beginning-of-tape point. The beginning-of-tape status bit is not on.

- If light is not sensed after three seconds, the transport moves to fast rewind (50 inches per second) and continues at high speed until the front transparent leader is sensed. (Timing logic permits the controller to ignore the end-of-tape and beginning-of-tape holes as they pass by. The transport stops, changes direction to forward, and slowly advances to the beginning-of-tape as above.

After tape motion ceases, the controller goes not busy. The end-of-operation interrupt, if requested, occurs at this time.

Note that this sequence can also be initiated by any of three other means:

- Auto-rewind.
- BOT/EOT is encountered during search tape mark (reverse) or backspace commands.
- External circuitry can reposition the tape to beginning-of-tape through external rewind in order to fully implement the automatic initialization of the system.

Erase

If bits 10 through 7 are set to 1110, the tape moves forward and is erased for approximately 3 to 4 inches (8 to 10 centimeters). The resultant tape appears as a long inter-record gap.

This command is also an illegal motion command if it is issued when write is disabled.

After tape motion ceases, the controller goes not busy. The end-of-operation interrupt, if requested, occurs at this time.

Read One Record

If bits 10 through 7 are set to 1111, read motion in the forward direction is initiated; data records cannot be read in the reverse direction (figure 2-5).

After receiving this command, the transport initiates forward motion and begins reading the tape contents. The sequence on the tape of one record (block) is:

- Inter-record gap – A blank interval on the tape during which no signals are received
- Preamble – An eight-bit (one character) sequence consisting of 10101010 (zero read first). It is used to define the beginning of the record and to synchronize bit clock timing.

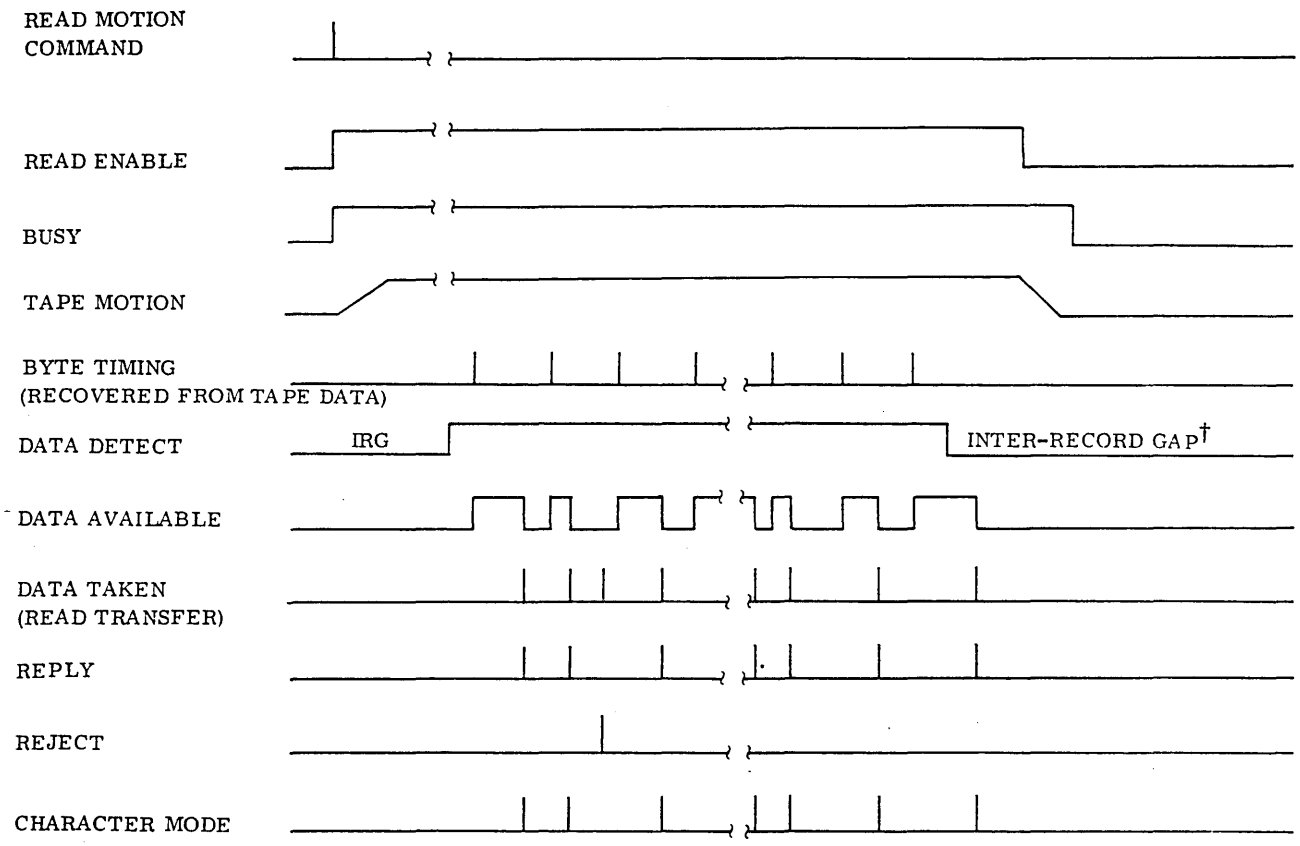


Figure 2-5. Typical Read Timing Diagram

- Data – Data occurs in eight-bit characters and may be of any length from one to 256.
- Cyclic redundancy check – The last two characters of the data area are the cyclic redundancy check characters; they immediately precede the postamble.
- Postamble – An eight-bit (one-character) sequence consisting of 10101010 (zero read first). It is used in conjunction with the trailer inter-record gap to define the end of record.
- Inter-record gap – A blank interval on this tape during which no signals are received. Upon entering this area, the loss of the clock signal is noted, designating the characters in the three holding registers as the postamble and cyclic redundancy check.

After tape motion ceases at the end of the inter-record gap, the controller goes busy. The end-of-operation interrupt, if requested, occurs at this time.

Motion/No Motion

If set, bit 10 enables/disables the decoding of A-regist function bits 7 through 9 as motion commands. When th bit is set, bits 7 through 9 specify one of the eight moti commands, and when it is clear, function bits 7 through have no meaning.

Unit 0/1 Selection

If set, bit 11 specifies which transport is connected to th controller. The select is executed only if bit 12 equals (unit select enable):

Bit 11 equals 0 – Select unit 0.

Bit 11 equals 1 – Select unit 1.

Only one transport is selected at a time, and no simultaneous or overlapping operations are permitted, including rewind and auto-rewind. The following conditions cause a reject of any function during a unit select.

- Unit select if the controller/transport is busy
- Unit select and motion command in the same function

The controller goes busy for 40 milliseconds following a legal unit select, permitting sufficient time for mechanical head loading of the selected transport. Issuing a unit select clears the end-of-operation and any other residual status as defined for issuing a motion control. After the 40 millisecond timeout, the end-of-operation status is set and, if enabled, an end-of-operation interrupt occurs. A clear controller does not affect the selected unit. The following also control the selection of the transport:

- Manual select unit 1 switch, if enabled, forces unit select to unit 1.
- System master clear forces unit select to unit 0 (overridden by the select unit 1 switch).

Unit Select Enable

If set bit 12 enables the unit 0/1 select feature discussed above.

- If bit 12 equals 1, the unit specified in Unit 0/1 Selection above is selected.
- If bit 12 equals 0, no unit select occurs regardless of the state of bit 11.

STATUS FUNCTION

The status function is shown in figure 2-6. When Q-register bit 0 equals 1 and is accompanied by both an equipment number (address) and an input to A instruction, the cassette controller status is transferred to the A register. The controller always replies to the processor status request. The status responses are described below.

Ready

If set, bit 0 indicates that the tape transport is operational (+5 volts are applied, the cassette is loaded, and the lid is closed). These conditions must exist before the transport can move the tape in either direction. If this bit is not on, operator intervention is usually required. In echo mode this bit is off and an alarm is present while the test is in progress (when a transport is attached to the controller).

Busy

If set, bit 1 indicates that the tape transport is busy during any motion cycle. The controller can accept motion commands only in the not busy condition. Nonmotion (no operation) commands or status requests are honored at all times. This bit clears automatically when the specified tape operation has been completed and all tape motion has ceased.

Write Enabled

If set, bit 2 indicates the presence or absence of the write plug at the cassette transport:

- Bit 2 is equal to 1 and the plug is present – Write operations are permitted.
- Bit 2 is equal to 0 and the plug is missing – Write operations are not permitted.

When bit 2 is equal to 0 (file is protected), the write one record, write tape mark, and erase motion commands are not honored and a reject is generated. All other motion commands are not affected by this bit. When bit 2 equals 1, all motion commands function normally.

Data (Available/Request)

If set, bit 3 indicates that the controller has data available from a read or is requesting data for a write either from a true read or write operation or from an echo mode operation. If data interrupts are enabled, setting this status causes an interrupt. Normally this status is reset and the interrupt cleared when data is taken or provided by the computer. It is also cleared by master clear and the clear controller command. The clear interrupt command does not clear this status bit.

NOTE

This bit remains set at the end of an ADT read operation whenever a short read occurs (the entire record is not read). Therefore, this bit is also cleared when a new motion command is received.

End-of-Operation

If set, bit 4 indicates that the cassette controller has completed a tape motion cycle and all tape motion has ceased. If the end-of-operation interrupt is enabled, setting this status causes an interrupt that is normally cleared when a new motion command is received. It is also cleared by the master clear and the clear controller command; it is not cleared by the clear interrupt command. Note that during tape runaway situations when the tape reads over random bit patterns or fully erased tape searching for legitimate records, this bit sets when tape motion ceases. This does not mean the tape motion command that led to the tape runaway has completed the cycle normally.

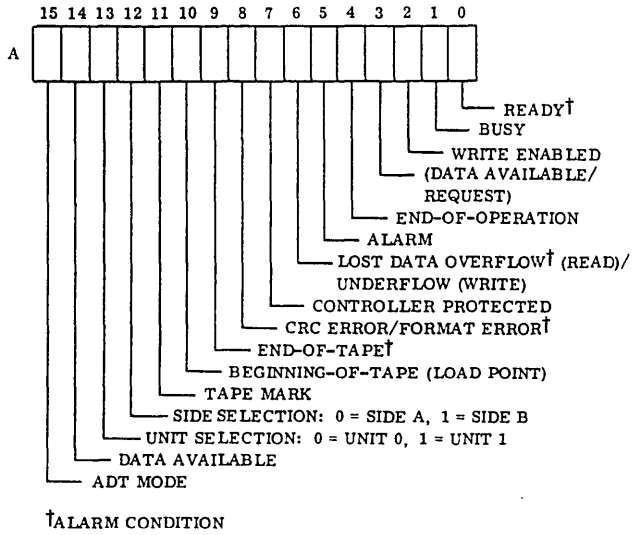


Figure 2-6. CPU Status Function Bit Assignments Relative to the Cassette Controller

Alarm

If set, bit 5 indicates that one or more of the alarm conditions is active. The alarm conditions are not ready, lost data (overflow during read/underflow during write), cyclic redundancy check error, format error, and/or end-of-tape. If alarm interrupts have been enabled, setting this bit causes an interrupt. It is cleared when the conditions causing the alarm have been cleared.

Note that this bit is set when the controller is in echo mode when a transport is attached to the controller.

During tape runaway, this bit also sets if the runaway timer expires. However, there are no other status bits to indicate the cause for the alarm. In this instance, the bit is cleared when a new motion command is received or by a master clear or clear controller command.

Lost Data (Overflow During Read/Underflow During Write)

Overflow (during read) results only if a read transfer occurs after the overflow has occurred.

If set, bit 6 indicates that a data character was available to the processor as part of a read operation but was not accepted prior to the succeeding character being available, resulting in part of the data block being lost. If alarm interrupts are enabled, setting this bit causes an interrupt. It is set whenever the succeeding character becomes available with no empty buffer storage. The succeeding character overwrites the lost character in the holding register. It is normally cleared when a new motion command is received; it is also cleared by master clear a clear controller command. It is not cleared by the cl interrupt command.

Note that, during the ADT mode of operation, this bit is if the entire record is not read.

If set, bit 6 (underflow during write) can also indicate tha data underflow condition developed during one of t following write operations:

- A/Q mode – When a data word was not furnished by t processor (data under-run), the record terminati (shutdown) sequence was initiated, and a write da command from the processor occurs during t shutdown sequence.
- ADT mode – When the record termination (shutdow sequence was initiated but STERM did not occur due a lack of a data word (data under-run).
- When a tape mark is accidentally written by starting write a record but no data is output within 1 milliseconds.

PROTECTED

If set, bit 7 indicates that the program protect switch is the protected position. Refer to Protect Switch above for description of protected versus nonprotected operation.

Cyclic Redundancy Check Error/Format Error

If set, bit 8 indicates that either a cyclic redundancy che error has occurred during a data read operation or during t read-after-write portion of a write operation or that format error has occurred during a data read operation. alarm interrupts are enabled, setting this bit causes interrupt. This bit is set to indicate a format err whenever the preamble is missing or incomplete, causing data record to be lost or the read data to be unreliable.

This bit is also set if the postamble is missing or incomple when an inter-record gap is detected. A format error can b defined in terms of the following conditions:

- A format error occurs if, after issuing a read moti command or during the read-after-write portion of write motion command, the first eight consecutive bi detected after passing from a gap (no clock transition to a data (clock transitions present) portion of the tap are not deciphered as a legitimate preamble code.
- An error occurs if a legitimate preamble is detected the beginning of a record but a legitimate postamble not read as the last eight bits from the tape once th end of record inter-record gap is detected.

Note that these error conditions can be detected during deadstart operations and that if this status bit is set at the end of any record (inter-record gap) during deadstart operations, it aborts the deadstart loading process.

This bit is cleared when a new motion command is received. It is also cleared by a master clear and the clear controller command. It is not cleared by the clear interrupt command.

End-of-Tape

If set, bit 9 indicates that the end-of-tape warning hole was sensed during a forward motion command (write motion, read motion, write tape mark, search tape mark, or erase). Like the beginning-of-tape hole, the end-of-tape hole is located between the two recording tracks; therefore, sensing the end-of-tape in no way invalidates the operation currently underway. The end-of-tape is located approximately 16 inches (41 centimeters) from the beginning of the clear trailer. Tape density, exclusive of gaps, is 100 characters per inch/39 characters per centimeter. End-of-tape is set as soon as the hole is sensed by the transport photo-electronics. If alarm interrupts are enabled, setting this status bit causes an interrupt. It is cleared whenever a reverse direction command (search tape mark (reverse), backspace, or rewind) is received. It is also cleared by master clear and the clear controller command. It is not cleared by the clear interrupt command. Note that search tape mark (reverse) and backspace commands should not be used when this bit is set. End-of-tape clears whenever a unit select operation is executed. Also note that if this bit sets, it terminates any deadstart read operation that is in progress. Thus, no deadstart routines can be written in the region of tape between the end-of-tape hole and clear trailer, since the deadstart routine would not fully load in the deadstart mode.

Beginning-of-Tape (Load Point)

If set, bit 10 indicates that the transport is currently located at the beginning-of-tape point. As noted under Rewind above, this fact is logically derived, since the transport light detector circuitry is unable to distinguish between the beginning-of-tape hold, the end-of-tape hold, and the transparent leader and trailer.

Bit 10 is set when the tape reaches (or is loaded) beginning-of-tape in any legal way. This includes:

- Auto-rewind (normally initiated whenever the lid on the selected unit is opened and then closed during a tape loading sequence)
- Backspace one record
- Search tape mark (reverse)
- Rewind

After rewinding to the transparent leader, the transport runs forward until light is sensed again; this is the beginning-of-tape hole. The transport is then commanded to stop. Depending upon the dynamic stopping characteristics of the transport, the tape stops at the beginning-of-tape hole or a short distance thereafter. In either case, this bit is set. It is cleared whenever a forward motion command moves the tape off the beginning-of-tape or whenever the alternate unit is successfully selected. It is cleared via a manual CPU master reset but not by a clear controller command.

Tape Mark

If set, bit 11 indicates that a tape mark has been detected either as part of a read operation, read-after-write portion of a write operation, or search tape mark command. Tape mark is defined as a tape block (record) consisting of a preamble, no data, a cyclic redundancy check (all zeroes), and a postamble. Tape mark status is cleared upon receipt of any new motion command and by a master clear and the clear controller command.

Side B

The cassette has two sides, A and B. If set, bit 12 indicates which track of the cassette tape is in position under the read/write head. A sensor in the transport itself detects the presence/absence of an offset slot in the cassette and is used to define sides A and B of the cassette. This bit is set whenever a cassette is loaded in the transport with side B visible, indicating the second track is positioned under the read/write head.

This bit is clear whenever a cassette is loaded in the transport with side A visible.

Unit 1

If set, bit 13 indicates which transport, unit 0 or unit 1, is logically connected to the controller at any given time. The controller can only service one transport at a time.

The unit numbers 0 or 1 are assigned to a particular transport by using a unique cable assembly.

This bit is defined as follows:

- Bit 13 equals 0 – Unit 0 is logically connected to the controller
- Bit 13 equals 1 – Unit 1 is logically connected to the controller

Note that is the UNIT 1 SELECT indicator/switch on the operators panel is on, unit 1 is always connected to the controller, and unit 0 is never connected to the controller.

Normally this bit is set or cleared by using function bit A11. It is also cleared by master clear except when the UNIT 1 SELECT indicator/switch in on. When the UNIT 1 SELECT indicator/switch is off, all normal controls on this bit are in effect.

Data Available

If set, bit 14 indicates that the controller has data available from a read operation or from echo mode operation. If data interrupts are enabled, setting this status causes an interrupt. This status is reset and the interrupt cleared when data is taken by the computer. It is also cleared by master clear and the clear controller command. It is not cleared by the clear interrupt command. Note that this bit remains set at the end of an ADT read operation whenever a short read occurs (the entire record is not read). Therefore, this bit is also cleared when a new motion command is received.

NOTE

This status bit is provided in addition to bit 3 in order to resolve interpretation of the data interrupts issued during echo mode operations.

Auto-Data Transfer Mode

This bit indicates that the controller is operating in the Al mode. It is set whenever a function code is received which function bit A06 is set. It is normally clear whenever a terminate signal (STERM) is received from t processor during the normal termination of an ADT oper tion. A master clear and a clear controller command al clear this bit. When this bit is set, the data available data request condition generates a micro interrupt that processed by the processor emulator at the micro level.

Procedures for the installation of the tape cassette controller are provided in the CYBER 18 Computer Systems with MOS Memory Installation Manual. Refer to that manual for detailed instructions on initial system installation or on adding new equipment to the system.

This section contains the external and internal interface diagrams and tables. The diagrams depict the source and termination of all the write and read and control signals that enter and leave the tape cassette controller, and the tables contain definitions of the signals. Detailed descriptions of the internal controller functions are illustrated by block diagrams. The diagrams represent groups of logic that perform definite functions. Numbers in the upper right corner of the blocks indicate the logic diagram sheet that contains the functional logic group.

EXTERNAL INTERFACE

Figure 4-1 indicates the source and termination points of data and control signals applicable to the tape cassette controller. Table 4-1 tabulates these signals in alphabetical sequence and provides the functional description of each. The field print package logic diagrams contain diagonal (/) and asterisk (*) symbols to indicate the active low (not) condition of a signal. The diagonal is used to designate the low condition of CPU external read and write signals. The asterisk is used to designate the low condition of internal signals and tape transport interface signals. For example, CPU signals are designated ADR08/ through ADR11/, SD01/ through SD13/, READ-SSTB/, etc., while internal and tape transport interface signals are designated READ*, WRITE*, TRDY*, FAST/ LOW*, etc.

OVERALL FUNCTIONAL DESCRIPTION

The tape cassette controller (figure 4-2) contains all the logic for the program control of data to and from the CPU via the I/O-TTY controller, to and from the tape cassette, from the tape cassette to the breakpoint controller, and for control of the transport. All function and status requests are initiated by the computer. The controller interfaces with one or two tape cassette transports† and has the following capabilities:

- It is capable of reading and writing industry standard cassette (ECMA-34/ ANSI x 3B1-638) via the A/Q channel of the processor with a transfer rate of 750 characters per second (a character consists of eight bits).
- It is capable of reading prerecorded cassette tape for deadstart and program loading into the processor via the serial asynchronous interface at the 9600 baud rate. The character transfer rate is 750 characters per second.

INTERFACE

A/Q Interface

The cassette controller interfaces to the internal, TTL-level, A/Q channel of the CPU. The controller may be status- or interrupt-driven at the macro level, and data transfers may also take place in the auto-data transfer mode at the micro level. Data from the controller to the CPU is eight bits wide, control function command words are 13 bits wide, and status words are 16 bits wide.

Deadstart Interface

Only the read function is performed in the deadstart mode of operation. The data is ASCII, asynchronous binary serial bit by bit at the 9600 baud rate. The maximum character is composed of one start bit, seven binary bits (data), one parity bit, and at least one stop bit. The deadstart signal (SM204) is a direct current level controlled within the CPU. The serial data signal conditioning is open collector TTL.

Transport Interface

The signal transfer between the controller and each transport is achieved via cable (maximum length, 10 feet) that connects to the backplane directly behind the controller card and to the transport.

DATA TRANSFER

To read information from or write information onto a tape cassette using A/Q channel operation, an orderly dialogue occurs on the channel that results in a series of actions by the controller and/or transport.

Write

When the cassette is inserted into the selected transport and the lid is closed, the ready status (and the side B status, if that side is in the active position) occurs, and a rewind sequence is automatically initiated, assuming that the auto-rewind feature has not been disabled by pressing the associated unit 0 or unit 1 disable switch segment (ARW0 and/or ARW1, respectively) on the controller.

†Two transports (units 0 and 1) can be sequentially served by the controller. Parallel or simultaneous operations are not possible (i.e., one transport is always idle or in a standby state).

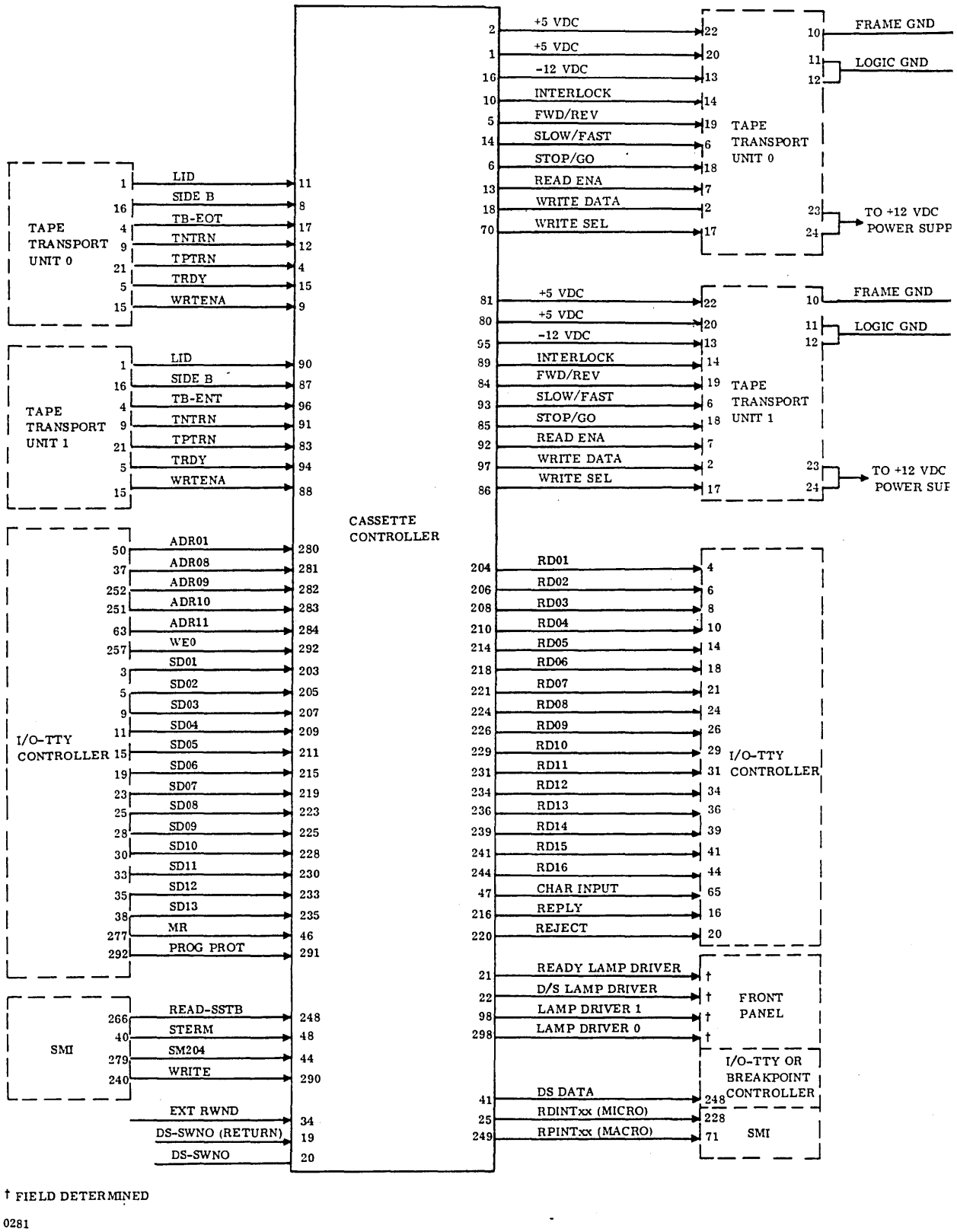


Figure 4-1. External Data and Control Signals

TABLE 4-1. EXTERNAL SIGNAL INTERFACE

Signal	Function
ADR01, ADR08 through ADR11	ADR address bits to the peripheral controller. During an I/O operation these bits are transferred from the O register via the I/O-TTY controller to the cassette controller. ADR01 (Q register bit 0) specifies director operation and ADR08 through ADR11 (Q register bits 7 through 10) specify the equipment code.
BOT/EOT	Indicates when transport detects light at beginning-of-tape or end-of-tape
CHARINPUT	Indicates that the controller's input to the CPU is contained in the eight least significant bits of the A register (the eight most significant bits of the A register are not altered).
DSDATA	Serial asynchronous interface (deadstart data line) for panel mode input at 9600 baud
D/S LAMP	This line displays the status of SM204 during deadstart loading procedures.
DS-SWNO	When the DEADSTART switch is on the operators panel, this line connects to the normally open contact of the DEADSTART switch.
DS-SWNO (return)	Deadstart signal return
EXT. RWND	Permits external circuits to reposition tape to beginning-of-tape for fully automated initialization procedures
FWD/REV	Controls direction of tape motion
INTERLOCK	Used to enable the transport ready signal
LID	Indicates position of protective cover (open/closed)
MR	Clears the peripheral controller (master clear)
PROG PROT	Indicates that this I/O operation was initiated by an I/O instruction whose program protect bit is set.
RDINT	Micro (ADT or data) interrupt line
RD01 through RD16	RD data bits from the cassette controller. In a CPU input operation, these bits are transferred from the controller to the CPU A register via the I/O-TTY controller.
READ	Initiates an input transfer of one word from the controller to the CPU A register via the RD lines.
READY	Indicates transport status (tape does not move when transport is not ready)
READY LAMP	This line drives the READY indicator LED located on the operators panel.
REJECT	Indicates controller response to a CPU read or write when the operation cannot be performed. The REJECT drops after the READ or WRITE drops.
REPLY	Indicates controller acceptance of a CPU READ or WRITE. The REPLY drops after the READ or WRITE drops.
RPINT	Macro (program) interrupt line
SD01 through SD13	A register data bits to the cassette controller. In a CPU output operation, these bits are transferred from the I/O-TTY controller to the cassette controller. SD01 is the least significant bit.
SIDE A/B	Indicates which side of the cassette is active when loaded
SM204	Signals the controller when to start and stop sending deadstart data to the panel interface (DEADSTART indicator)
SLOW/FAST*	Controls tape speed (7.5 IPS/ 50 IPS)
STOP/GO	Controls tape motion

TABLE 4-1. EXTERNAL SIGNAL INTERFACE (Continued)

Signal	Function
STERM	Indicates that this is the last data transfer of an ADT buffer operation (Terminate)
TNTRN	One of two read data lines; indicates when a negative transition has been detected by the read head
TPTRN	One of two read data lines; indicates when a positive transition has been detected by the read head
WE0	Indicates that bits 11 through 15 in the Q register address are all zero (W=0)
WRITE	Initiates an output transfer of one word from the A register to the cassette controller via the SD lines.
WRITE SEL	Enables the write head
WRT ENA	Indicates presence or absence of the write plug in the tape cassette
UNIT 0 LAMP	In a two transport system, this line drives the UNIT 0 SELECT LED whenever unit 0 is selected.
UNIT 1 LAMP	This line drives the UNIT 1 SELECT LED whenever unit 1 is selected.

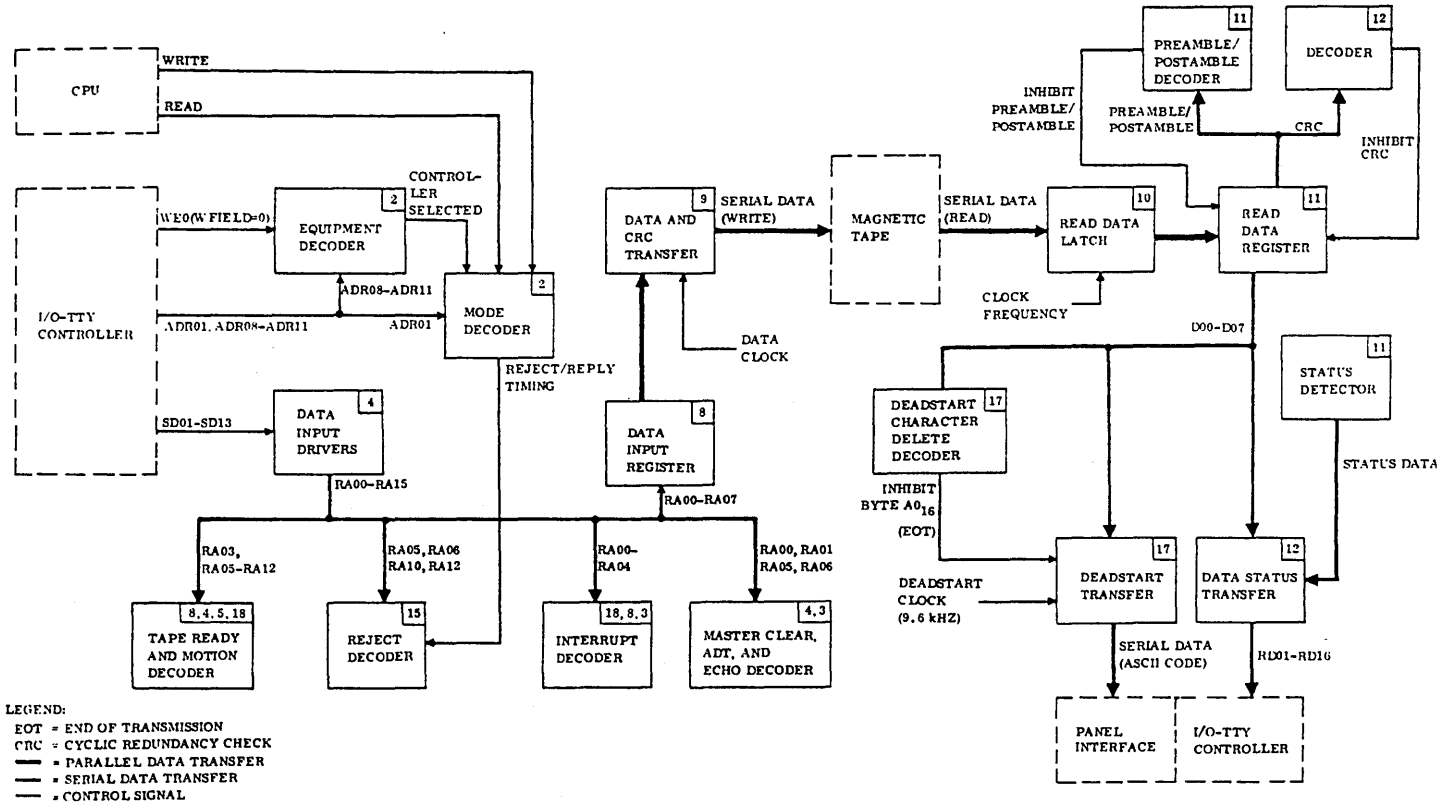


Figure 4-2. Cassette Controller Data Signal Flow

The tape rewinds to the transparent leader, stops, and winds forward until the beginning-of-tape hole is sensed. Tape motion ceases, beginning-of-tape status occurs, and the READY indicator on the operators panel illuminates.

A function command is issued directing initiation of write motion, typically with data request and end-of-operation interrupts requested. Forward tape motion begins (7.5 inches/ 19 centimeters per second); at the end of a 50-millisecond interval, the tape is up to speed. The tape moves approximately 1.6 inches/4 centimeters. Since the transport write data line is held steady, an inter-record gap is written on the tape.

Start delay is used only by the write logic and is defined as the total elapsed time from the decoding of any write motion command until the first bit of the preamble is written onto the tape. This delay includes 50 milliseconds for the transport ramp start plus an additional 190 milliseconds (approximately) for writing the leader inter-record gap that precedes the record or tape mark that follows.

Stop delay for the write logic is common to the read logic and is defined as the total elapsed time from the end of the write sequence, or from the time end-of-record is detected during read operations, until the stop command is issued to the transport. This delay for a read is specified at 36.25 ± 3.15 milliseconds. For a write, this delay is approximately 20 milliseconds longer than for a read. An additional delay of approximately 40 milliseconds is used after the stop command is issued to the transport before the controller goes not busy and issues an end-of-operation.

After receiving the write motion command, the data request status bit is set, accompanied by a macro interrupt, if requested. If the tape cassette is in ADT mode, a micro (data) interrupt also occurs.

As soon as the character is obtained and stored in the output holding register, the data request and corresponding interrupt drop.

At the conclusion of the inter-record gap interval, the preamble (10101010) is moved into the output shift register. Starting with the least significant bit of zero, the bits are sent one at a time through the bi-phase encoding logic where bit clock transitions are added and onto the transport write data line.

Following the issuance of the preamble, the first data character is moved from the output holding register to the output shift register and sent out, the least significant bit first, as described above. The data is also sent through the cyclic redundancy checksum generator for accumulation.

Transferring the character from the output holding register to the output shift register empties the holding register. The data request status is set again, accompanied by a macro interrupt if requested. If the cassette is in ADT mode, a micro (data) interrupt also occurs. This action occurs during the data portion of a write operation each time the output holding register becomes empty.

As soon as a character is obtained and stored in the output holding register, the data request and corresponding interrupt drop. When the output holding register is empty at the time its contents should be moved into the output shift register, the controller declares that an under-run exists. A data under-run indicates the end of the data portion of a block. During ADT operation, the receipt of a terminate signal defines the end of the data transfer, micro (data) interrupts are disabled, and an under-run condition develops that initiates shutdown as in normal A/Q operation.

At this point, the accumulated CRC becomes the source for the phase-encoding logic for the next 16 bits. Following this, the eight-bit postamble is shifted out. At this point the bi-phase encoding logic is turned off (i.e., the write data line is held steady at a logical 1).

Tape motion continues for a fixed delay time, and the transport is then commanded to stop. During these two intervals, inter-record gap is written. The delay time inserts a sufficiently long interval to ensure that the proper length inter-record gap is written, consistent with the transport stop dynamics. End-of-operation status is then set, and the unit becomes not busy.

Read

The read operation is enabled when a cassette is inserted, the lid is closed, and the rewind sequence is completed to ensure the tape is resting at the beginning-of-tape. When the tape is already operational, the read head must be resting on an inter-record gap. Data can only be read when the tape is moving in the forward direction at slow speed.

After the beginning-of-tape point has been reached as indicated by the status bit and the side B status has been checked to determine whether the cassette has been loaded correctly, a function command is issued directing initiation of read motion (typically with data available and end-of-operation interrupts requested). Forward tape motion begins at 7.5 inches per second/19 centimeters per second. The tape comes up to speed, and approximately 70 milliseconds after the tape is at proper speed, positive and negative data transitions begin arriving from the transport read data lines.

These positive and negative data lines are merged into a single composite read data line. The two data lines also are used to synchronize a phase lock loop oscillator to the recovered read data streams. This oscillator is used for clocking all of the read data registers (shift, buffer, cyclic redundancy check, etc.).

Information passes through the more than 24 input shift register bits (three characters). This shift register delay is needed for cyclic redundancy check and postamble detection. Character synchronization is obtained from the eight bits of the preamble.

When the preamble has filled the last eight bits of the input shift register, it is discarded. As the next character (first data character) reaches the last eight bits of the input shift register, it is parallel-loaded into the input holding register. When the input holding register is filled, the data available status (and the interrupt if requested) is set. If the cassette is in ADT mode, a micro (data) interrupt also occurs. This signals the processor to input a character. Meanwhile, data continues to shift through the input shift register under control of the recovered read data bit clock. The data available status (and the interrupts if requested) clears whenever the input holding register is empty.

As each character reaches the end of the input shift register, it is moved into the holding register where it remains until emptied by the CPU. If the input holding register is not empty at the time that the next character is moved to the input holding register, an over-run condition is signalled, and the corresponding status bit (and alarm interrupt if requested) is set.

This action of shifting data and filling and emptying the holding register continues until a lack of transitions is detected, indicating that the ending inter-record gap has been reached. Only after this inter-record gap is sensed can the three preceding characters be identified as the CRC and postamble (rather than data). The CRC logic is located on the second shift register so that at the next character boundary, the data and CRC have been checked. A test for all zeroes is made in the cyclic redundancy check; sensing any nonzero condition sets the cyclic redundancy check error status and alarm interrupt if requested. No more data available status signals or interrupts are set, since the CRC and postamble are discarded.

As soon as the cyclic redundancy check has been checked and the end-of-record (inter-record gap) has been detected, the transport is halted and the end-of-operation status and interrupts, if requested, are set.

The same cyclic redundancy check sequence described above occurs during the read-after-write phase of any write data operation (the timing is identical). During any search tape mark (forward or reverse), backspace, or read command, if the tape reads over random (undefined) bit patterns or fully erased tape searching for legitimate records (tape runaway), it either stops in the first blank area of tape that occurs after detecting eight or more data transitions or it stops after approximately 5.5 seconds (41 inches) of tape have elapsed since the command was issued, whichever occurs first.

Self-Test (Echo)

Echo mode places the data path in loopback and tests the controller in lieu of the transport. Operation starts as in a write operation and terminates as in a read operation.

Data interrupts occur for both data request and data available under the same conditions as described individually under Read and Write above.

Because of the inherent time delays through the controller, several data request interrupts are received prior to the first data available interrupt. After that, they occur interlaced until the CPU stops sending data. The remaining data available interrupts are then received. Since the program cannot distinguish between the data request and data available conditions using the signal data request/ available, a separate status bit is provided for data available.

Echo mode is reset via a clear controller command. Any motion commands that are included in the output function to select echo mode are ignored.

Auto-Data Transfer

The controller performs an auto-data transfer (ADT) operation whenever the ADT mode bit is set in accordance with the ADT mode conditions. Depending on whether write or read motion has been requested, data write or r operations occur as previously described except for occurrence of micro interrupts. A/Q channel operat trigger data request/ available macro (program) interru if enabled, during ADT operations. The data requ available signal simultaneously triggers a micro (d interrupt in addition to the macro (program) interrupt. A/Q channel then provides/ accepts a character. sequence continues until a termination signal (STERM received. Receipt of this signal inhibits generation of further data interrupts (macro or micro) for the remain of the block.

Since data request/ available interrupts are no longer be generated, data no longer is provided/ accepted by the channel and the block terminates normally. As soon as t motion ceases, an end-of-operation macro interrupt generated with the end-of-operation status set. Note t during an ADT read operation, the alarm status (and ma interrupt, if enabled) occurs if the entire record has been read.

Deadstart

When plugged into an I/O slot that is wired for deadst operations, prerecorded cassettes can be read into processor via the 9600 bits-per-second asynchronous se panel interface. Only one device can be ready to be deadstart device though many controllers could be attac to the same signals. With power applied and a casse mounted in the tape transport, ready is obtained by clos the lid. Conversely, the transport is made not ready opening the lid or by removing the cassette.

Tape positioning is controlled by the auto-rewind or exter rewind features. If the auto-rewind feature is enabled the operators panel, then the tape is automatically pc tioned to the beginning-of-tape (load point) when cassette is loaded and the lid of the transport is closed. the auto-rewind feature is disabled, no tape position occurs during the deadstart procedure. If the exter rewind signal is generated, the tape is automatic positioned to beginning-of-tape (load point). Automatic t positioning can only occur on unit 1 if the UNIT 1 SELE switch is enabled/set.

The READY indicator on the operators panel turns on wl the cassette is ready for the operator to initiate deadstart operation.

Operation begins when the DEADSTART switch (connec to SWNC and SWNO) is pressed. This action causes processor to set the deadstart signal, SM204, which contr the entire deadstart operation.

While the deadstart signal is active, the D/S ACTI indicator on the operators panel is also on.

As soon as the deadstart signal becomes true, the control initiates a read motion command and the operations begin described above for read operations. As soon as d characters become available from the third shift regist they are parallel-transferred to a 10-bit shift register which start and stop bits are appended and the regis serial output is shifted out at a 9600 bits-per-second rate the panel interface. Except for the byte $A0_{16}$, all bytes transmitted as written on the cassette tape. No parity generated. The byte $A0_{16}$ is not transmitted.

Operations continue through one or more records until the deadstart signal (SM204) drops. At that time, any data remaining in the current record is transferred via the ASCII data line, and the transport comes to an orderly stop in the inter-record gap after the current record.

If any errors are detected by the controller, the transfer terminates normally and the appropriate status is set as in any other read operation.

When the controller has detected a cyclic redundancy check or format error during deadstart operations, note that the READY indicator goes out and the D/S ACTIVE indicator remains on after the tape has ceased all motion. Also note that deadstart routines cannot be written in the region of tape between the end-of-tape hole and the clear trailer. If an error occurs, the deadstart operation must be repeated.

During any deadstart operation, controller status is reported as ready and busy.

Reject Conditions

The following is a summary of all the conditions that can cause the controller to generate an external reject.

- Protect violation
- Illegal echo command – Trying to select echo mode while the controller is busy. Any other function commands issued after the controller is in echo mode (to clear and re-enable interrupts, for example) must not include A register function bit 5, or a reject occurs.
- Illegal auto-data transfer command – Trying to issue an ADT command without a read or write motion command and without the end-of-operation interrupt enabled
- Mode conflict – Echo and ADT modes simultaneously selected
- Motion command when controller is busy
- Motion command when unit is not ready
- Illegal motion command – Attempting a write tape mark, write, or erase motion command when write is not enabled when the file is protected
- Illegal unit selection command – Attempting to select the opposite unit while the controller is busy
- Write data transfer without a data request
- Read data transfer without a data available
- Motion command and unit select in same function

CONTROLLER AND MODE SELECTION

Selection of the cassette controller (figure 4-3) is deciphered by the equipment decoder, M11, in accordance with the setting of the equipment number switch, M10. When the controller is installed, these four-segment DIP switches are set to the equipment number to designate the controller's selection address. This address, peculiar to each system, is determined at the time of installation and should not be changed unless intended. When the WE0 signal (W field equals zero) is active (low) and the address lines' (ADR08/ through ADR11/) bit configuration matches the equipment number switch settings, the cassette controller is selected (controller-selected ADR goes active high). This controller select enables the reply/reject timing generator (A/Q clock) and the mode decoder to initiate the handshake (reply and reject) cycle and mode selection (read data transfer, write data transfer, control function, or status). Refer to table 4-2 for mode selection conditions.

TABLE 4-2. MODE SELECTION

ADR01	Read	Write	Protect	ADR	Selection
High	Low	High	High	High	Read Data Transfer
Low	Low	High	High	High	Status
High	High	Low	Low	High	Write Data Transfer
Low	High	Low	High	High	Control Function

The protect detector assures protection of the CPU programs. Otherwise, protect switch H1 can be set to off (high) to select the unprotected condition. When H1 is off, the controller ignores the state of the program protect signal from the CPU and accepts all input/output instructions. An unprotected controller never rejects a function, status, or data transfer due to the program protect signal state. When program protection is required, the protect switch must be set to on (low) to enable the reply response (function, status, and data transfer) for protected instructions.

REPLY/REJECT SELECTION

The reply/reject selection function (figure 4-4) decodes the controller mode selection and response conditions to provide a reject or reply signal to the CPU. The reply or reject response must occur during a time span of a minimum of 200 nanoseconds to a maximum of 10.0 microseconds after the read or write signal goes active (high). This is accomplished in a handshake sequence:

1. The CPU read or write signal is high.
2. If data is transferred, the reply line immediately goes high.
3. If data is not transferred sometime during the 10.0 microsecond period, the reject line goes high.

Either condition 2 or 3 causes the write line to drop, which then causes the respective reply or reject signal to drop. If for any reason the controller does not respond, the CPU drops the request a maximum of 13.0 microseconds after the read or write request signal went high. The reply/reject timing generator produces the RRF1, $\overline{\text{RRF1}}$, RRF2, RRF3, and $\overline{\text{RRF3}}$ timing signals (figure 4-5).

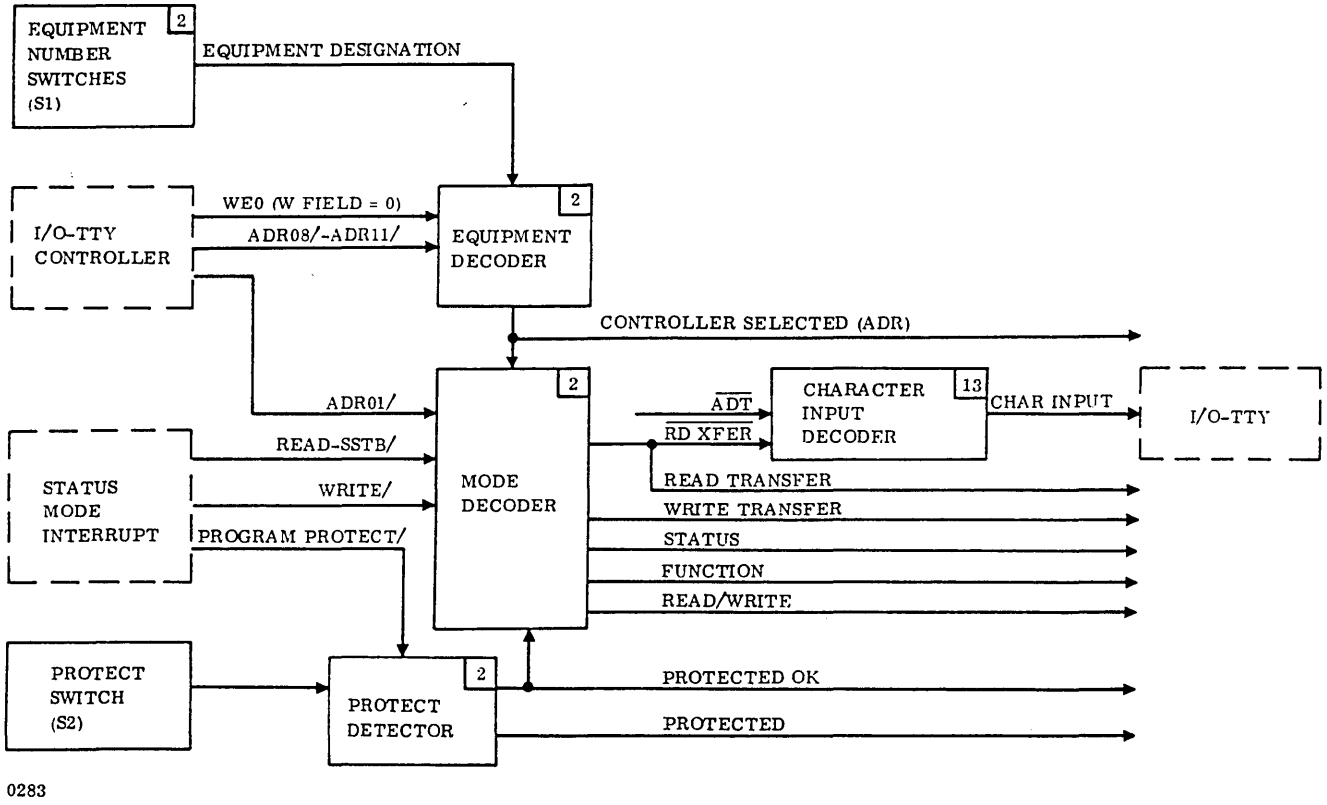


Figure 4-3. Controller and Mode Selection

The reply or reject response is produced during the RRF3 time of the reply/reject timing generator. These timing signals are produced by the four-bit shift register, H11, which is enabled by the selected controller signal being high. The time periods are generated by the oscillator frequency (1.536 MHz) signal applied to the clock input. All time periods are terminated when the read or write drops. These RRF signals time the clear interrupts, no operation and clear function, reject decoding, data input strobe, data/status selection, and reject decoder. If any of the reject conditions listed in table 4-3 exist, the reject decoder (D9, E9, and F9) produces a reject/reply (high) signal. This signal sets the reject flip-flop E5 and applies a high to the reject AND gate G12. When time RRF3 goes high, the reject signal at the backplane terminal goes active (low). This also applies the reject controller signal to the clear interrupt, data/status selector, and data input strobe to produce a master clearing of internal controller logic, initiate a clear interrupt (RPINT) for the CPU, and inhibit the output of data from the read output buffer register, respectively.

CLEAR AND ECHO SELECTION

The clear and echo selection function (figure 4-6) detects the control function word data bit (RA00 and RA01) conditions to enable the clear interrupt (RPINT), clear controller (master clear), no-operation function, clear function, and echo operation. When word bit RA00 is high (resulting in the selection of the clear controller function), the master clear signals are activated. The clear controller signal at AND gate D10 is produced when the RRF1 and RRF2 states, at the time the function has been designated, are both low at AND gate K11, and the reject controller signal is inactive (high) at AND gate E4. The master clear logic generates the MC and MR signals that are applied to the internal controller functions. Master clear can also be activated by the I/O-TTY controller applying a low signal to backplane terminal 46.

When word bit RA01 is high (resulting in the selection of the clear interrupt function), the clear interrupt signal is generated. This causes the data interrupt enable flip-flop (C-9) to be reset via the data interrupt enable OR gate (C8).

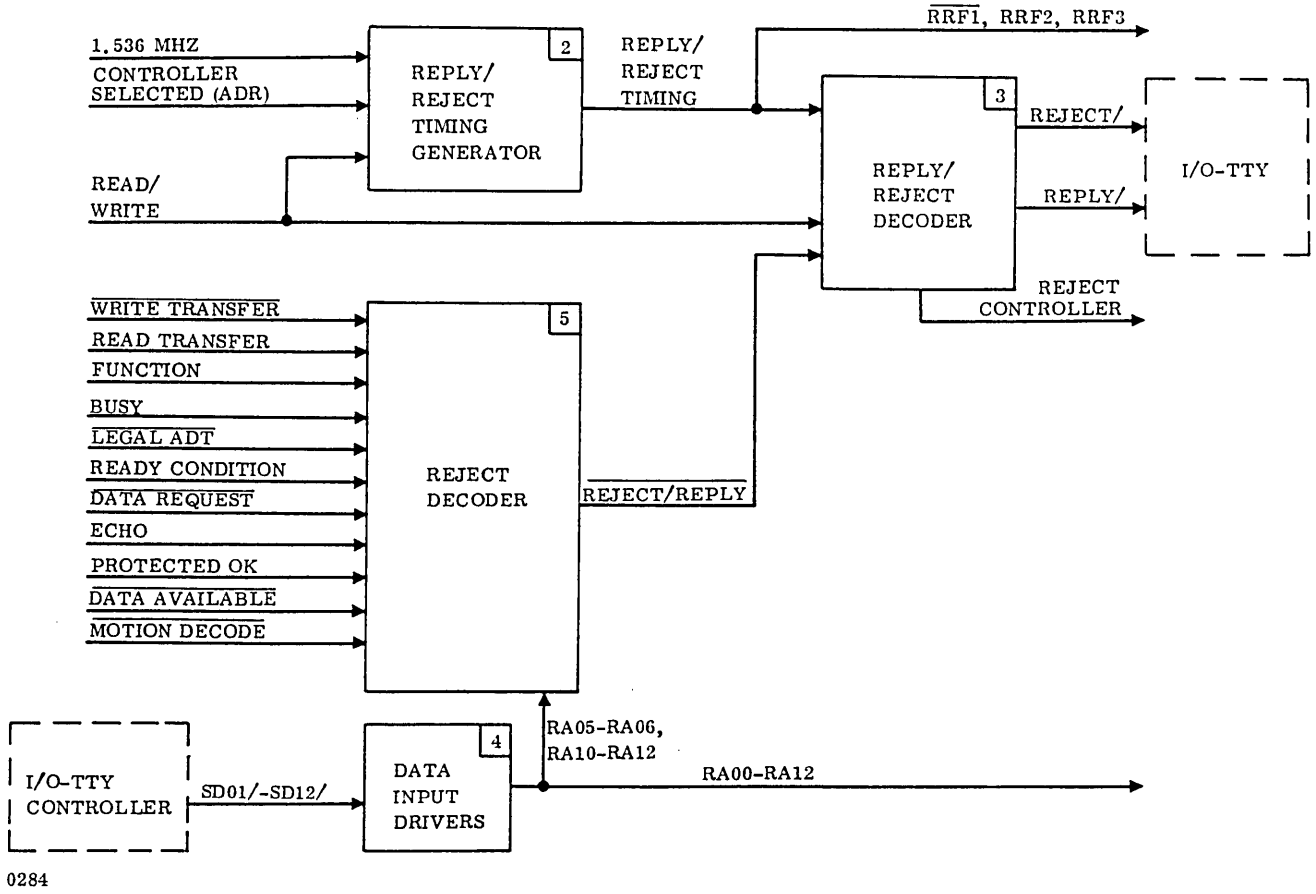


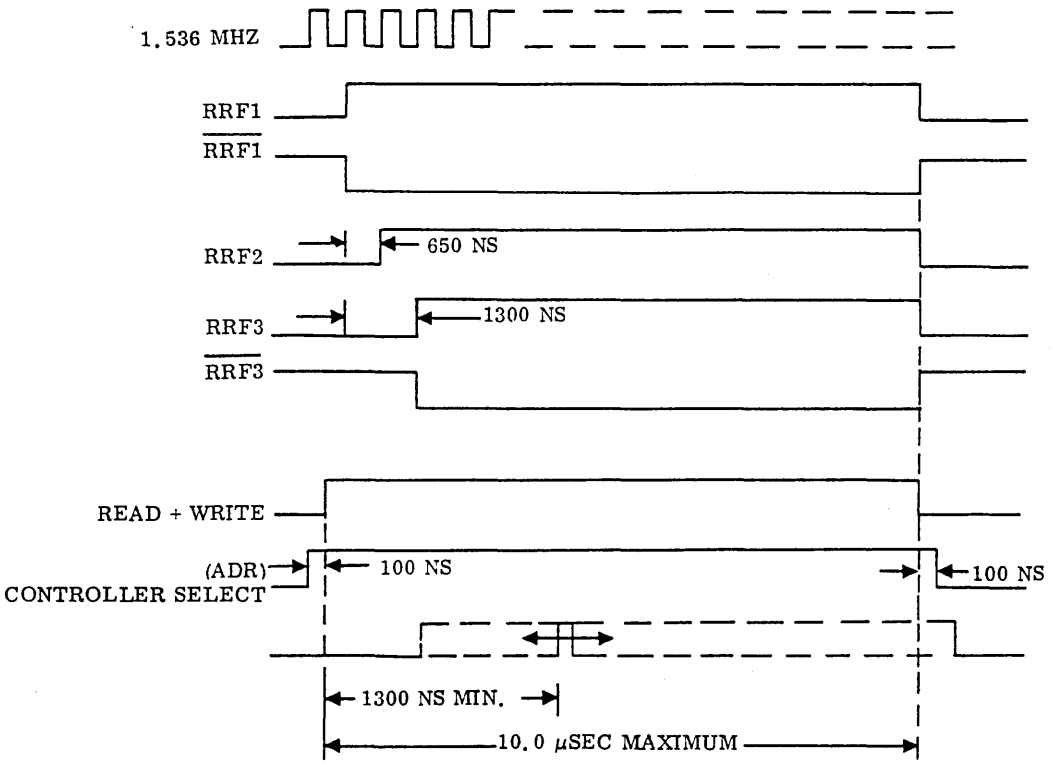
Figure 4-4. Reject/Reply Selection

When a function has been selected and a reject condition exists indicating that all conditions necessary to provide the selected function are not active, the no-operation function or clear function is produced. The no-operation function signal is produced when RRF3 is low (AND gate E10), and the clear function is produced when RRF3 is low and the busy signal is also low at AND gate E8. The no-operation function inhibits the interrupt enable functions selected by word bits RA02 through RA04 at interrupt enable gate C10 and the unit select enable (RA12) at AND gate E4. The clear function enables the echo function and inhibits motion detector no. 2 AND gate B8.

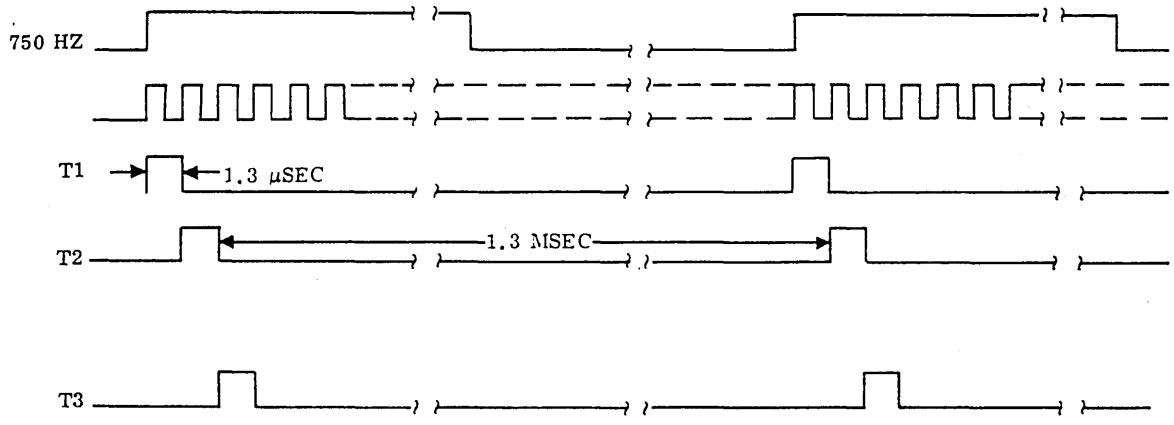
If the echo bit, RA05, is active (high), the echo condition is enabled by resetting the echo latch (C9). This enables the controller logic to manipulate any operations selected but does not activate the tape transport. When the echo mode is to be disabled, a clear controller function must be provided to produce the master clear (MC2) to set the echo latch.

MOTION FUNCTION DECODING

The motion function decoding (figure 4-7) receives control function bits RA03 and RA05 through RA10 and decodes them to determine the selected motion (table 4-4). In addition to the motion function command selections, the motion detector no. 2 logic decodes the auto-data transfer bit RA06 to ensure that all the ADT conditions are met, resulting in a legal ADT response to the reject decoder. These legal ADT conditions are detected by AND gate D11 and require that an end-of-operation interrupt has been selected (RA03), ADT mode has been selected (RA06), and write one record has been selected (RA07 and RA08). The echo select bit (RA05) is ANDed with the ADT result of AND gate D11 or the RA06 condition; if either the legal ADT or RA06 is low, this low is ANDed at gate D8 to ensure that the motion function is required. If the RA10 bit, clear function, and ready condition are all high at AND gate B8, MOTION DECODE 2 low is established. If any input



REPLY/REJECT TIMING



B CHARACTER TIMING

0285

Figure 4-5. Controller Timing

condition at B8 is low, a high output is established. MOTION DECODE 2 low inhibits the motion decode flip-flop (G11), and MOTION DECODE 2 high is combined with the output condition of motion detector no. 1 to provide an enable state to the motion decode flip-flop.

TABLE 4-3. REJECT CONDITIONS

Decode Gates	Condition
1	Protect violation
2	Mode conflict
3	Illegal echo command
4	Unit select with motion
5	Illegal auto-data transfer command
6	Illegal auto-data transfer command
7	Motion command when busy
8	Read data without data available
9	Motion command when not ready
10	Illegal motion command
11	Unit selection when busy
12	Write data without data request

The motion detector no. 1 detects the selection of erase and rewind in conjunction with the write condition. If either the erase or rewind condition is selected, a MOTION DECODE 1 low is applied to the motion decode flip-flop to enable the motion function selection to be determined by the RA07 through RA09 states. MOTION DECODE 2 is also ANDed with MOTION DECODE 1 by AND gate E10 to provide a legal motion function command (MFUNC) to clock the ADT latch G10 and enable master clear detector AND gate B5.

When enabled, the motion decode flip-flop selects the motion function associated with the conditions of control function motion bits RA07 through RA09 (table 4-4).

INTERRUPT DECODER

The interrupt decoder (figure 4-8) decodes the CPU control functions to produce the cassette controller micro and macro interrupts that, in turn, produce the applicable action (set program interrupt, RPINT; data interrupt, RDINT; terminate; alarm; and over/under flow). The program and data interrupts are used to initiate, run, and terminate the controller ADT operations. The alarm and overflow/underflow are malfunction interrupts that stop processes and advise the CPU of the applicable status.

The ADT mode is selected any time that ADT bit RA06, enable interrupt on data bit RA02, and end-of-operation bit RA03 are enabled in conjunction with a read or write motion command. The RA06 bit condition enables the ADT mode decoder. When the associated motion function, read or write one record, is high, the ADT signal conditions inhibit the character input decoder (G12), enable RDINT detector (L11), and set the ADT status bit RA16 (A register bit 15). The data request or data available signal triggers both the micro interrupt (RDINT) and the macro interrupt (RPINT) (AND gates L11 and B9) to increment the ADT program. The ADT program continues until a terminate (STERM) is applied. A clear interrupt, master clear, or alarm condition also terminates the ADT program by resetting the associated element of the interrupt enabler.

The macro interrupt (RPINT) can be activated by control function bits RA02 through RA04 when data is available, an end-of-operation occurs, or an alarm condition (malfunction) occurs. These conditions are detected by the interrupt enabler, which enables the interrupt driver (B9). If any one of these conditions occurs with these drivers enabled, the macro interrupt goes active. If the condition was caused by a malfunction, the applicable status (error, alarm, and/or overflow/underflow) is sent to the CPU. The tape runaway malfunction condition is detected by AND gate K11. If the time enable and time out signals are low, a runaway condition is activated by the runaway alarm latch G8.

WRITE DATA SEQUENCE

The write data logic (figure 4-9) controls the transcribing of data and tape mark records. All data records contain five basic parts: inter-record gap, preamble, data, cyclic redundancy check, postamble, and inter-record gap. A tape mark record contains all these except data between the preamble and cyclic redundancy check. Any time the tape is on the write one record motion and data requested and if data is not available, a tape mark is written. The record parts appear on the tape in the following form:

NOTE

Records are recorded on tape using Manchester code (phase transition coding) format.

- Inter-record gap (start) – A dc polarity approximately 240 milliseconds in duration, 1.6 inches (4 centimeters) tape length
- Preamble – One character (eight bits) length consisting of 10101010

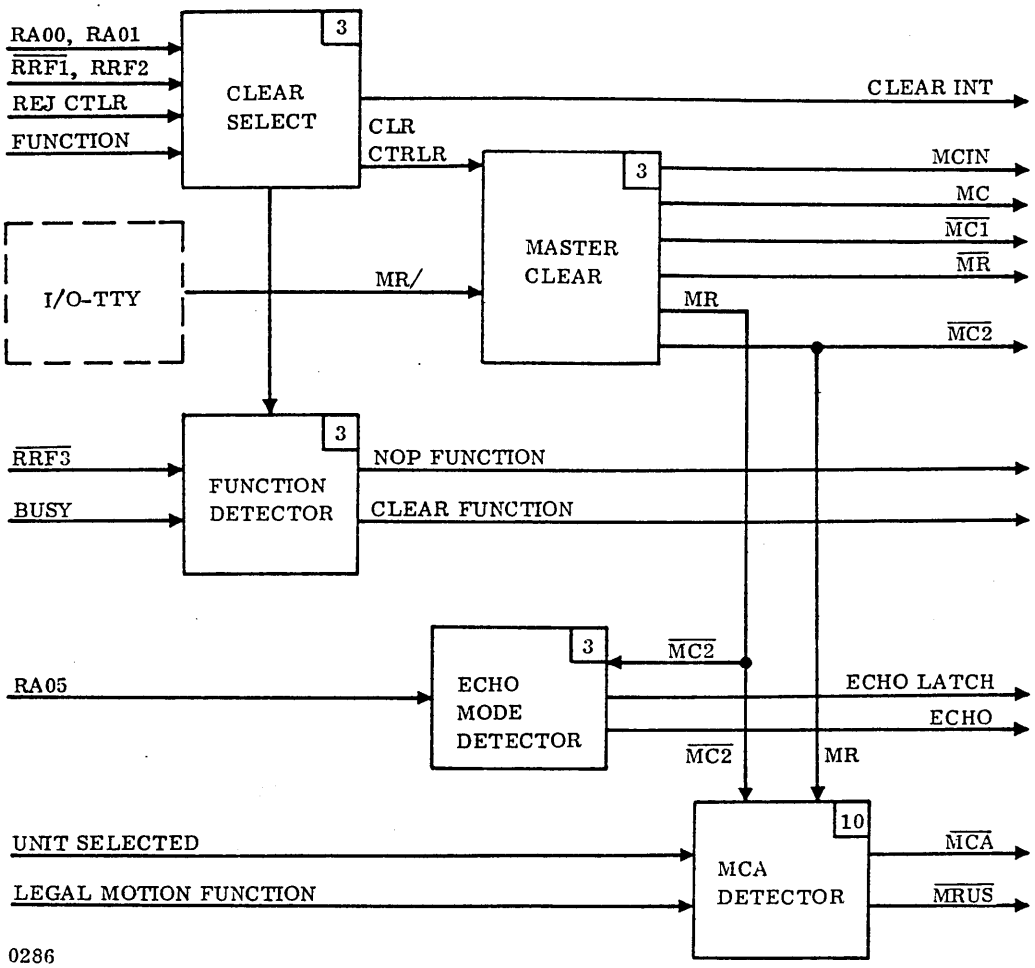


Figure 4-6. Clear and Echo Selection

- Data – Eight-bit coded characters not to exceed 256 characters in length †

NOTE

Data is never included in a tape mark record.

- Cyclic redundancy check – Two characters (16 bits)
- Postamble – Same as the preamble
- Inter-record gap (end) – A dc polarity approximately 36 milliseconds in duration, 0.27 inches (0.68 centimeters) tape length

After the READY indicator lights and the control function command, write one record (WRT, RA07, RA08, and RA10), is received, the tape moves forward. The WRT signal activates write select flip-flop B6 and write start delay one-shot B4. During the 240 millisecond delay time, the output drivers, write data unit 1 and write data unit 0 (G3 and A5, respectively), apply the inter-record gap dc polarity of approximately 5 volts. The write select flip-flop B6 output, W/SELF/F, activates the selected unit. When the write start delay one-shot goes low, the write sequencer flip-flop, C6, is enabled via OR gate B5. When time T1 is high and the write tape mark flip-flop resets, the low output of AND gate E7 sets the write sequencer flip-flop, C6, that enables write sequencer register C7, resets the write cyclic redundancy check generation register, and resets under-run latch E5. The next time T1 is high, preamble data sequence SQ1 is activated and, at the same time, the write sequencer latch Q output goes low.

†ECMA 34/ANSIx3B1/638 limitation. There is no hardware limitation to record length.

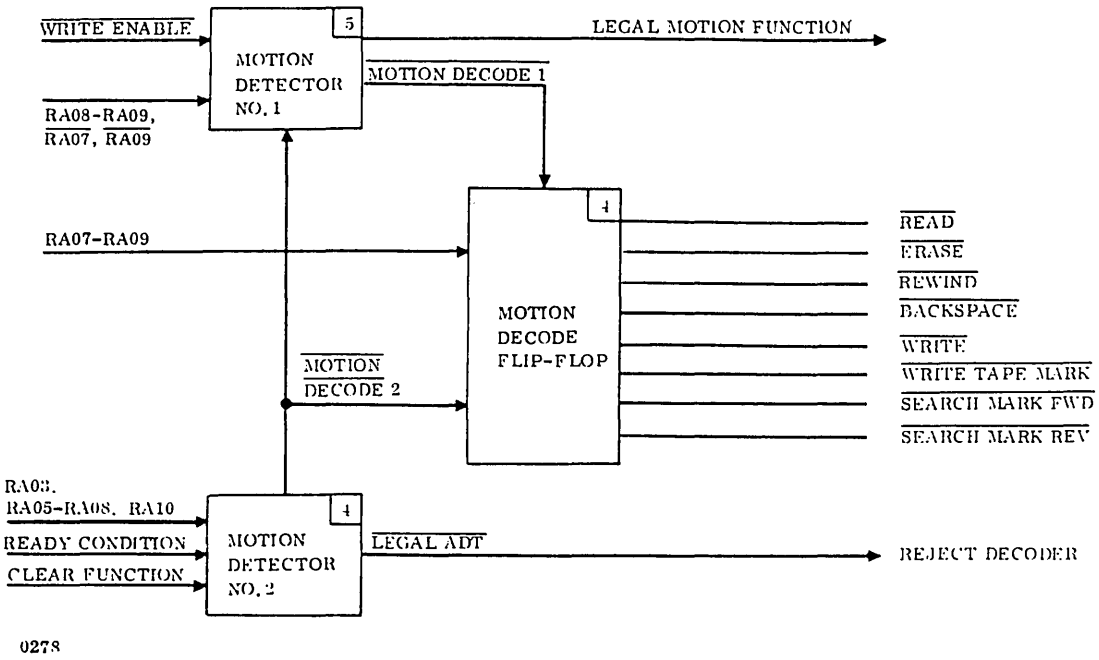


Figure 4-7. Motion Function Decoding

TABLE 4-4. MOTION COMMANDS

A Register Bits 10	9	8	7	Function
1	0	0	0	Search tape mark reverse
1	0	0	1	Search tape mark forward
1	0	1	0	Write tape mark
1	0	1	1	Write one record
1	1	0	0	Backspace one record (or tape mark)
1	1	0	1	Rewind
1	1	1	1	Erase
1	1	1	1	Read one record

Preamble

The SQ1 high output is inverted by OR gate B7 to produce SQ15, which is actually SQ1 or SQ5. SQ15 is ANDed with T2 low to provide the preamble load signal to the data input register (B10 and C11) with the high conditions applied to pins 1 and 3 by R1 and the low conditions applied to pins 2 and 4 by the ground connection. This preamble data is then strobed out of the registers in serial format by the 6 kHz frequency applied to the light register clock terminals. The serial data is inhibited from the CRC generator by the high condition of the gate CRC signal (GTCRC) and coupled through OR gates D6 and F6 to the write data encoder (Manchester data encoder C5) where the data is converted to phase transition. The phase transition codes are created by the 6KF high and 6KF low frequencies applied to the data encoder (refer to figure 4-10 for Manchester code details). These bit codes are clocked through write data output latch C6 at a 12 kHz rate to make the phase reversal transitions (transitions are required when several 1 or 0 states are together). The phase reversals are transparent to the data. This data is applied to the write head lines (WDTA/1 and WDTA/0) via level converters A5 and G3.

Data

After the preamble has been strobed from output shift registers B10 and C11, the write time sequencer advances to data position SQ2. When SQ2 and the tape mark are both high at AND gate E7, the gate CRC signal (GTCRC) enables data input to the CRC generator and enables AND gate B7. When T2 goes low, data that has been stored in data registers B11 and C12 is gated into the output shift

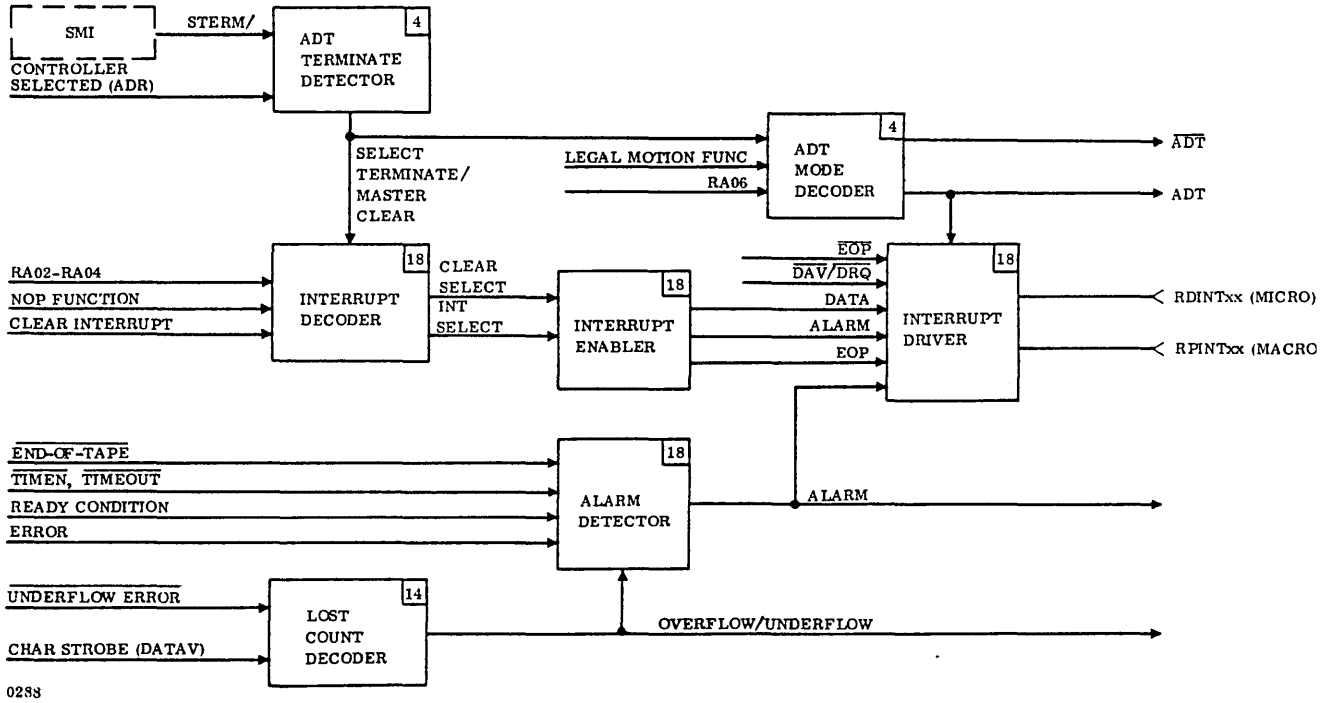


Figure 4-8. Interrupt Detector

registers, C11 and B10. This data is strobed from the shift registers by the 6 kHz signal applied to the clock input. The serial data is processed through the data logic in the same manner as the preamble. Since the GTCRC signal has enabled AND gate F7, the data is also processed in the CRC logic to produce the 16-bit CRC word that is stored on the tape immediately following the character data. This write CRC word is compared with the CRC word generated by the read operation. If an error is detected (the read comparator output goes high) the CRC error status and an alarm interrupt are set if requested.

Cyclic Redundancy Check

The CRC word (16 bits) is gated into CRC generation registers G6 and H6 by the low condition of GTCRC. The CRC is contained in the registers by SQ3 and SQ4 being low at OR gate D7. This D7 output enables AND gate E4 and inhibits AND gate F6. This permits data entry to the CRC registers and deters CRC data from reaching the write data encoder. Data to the CRC registers is processed in the CRC generator in accordance with the CRC polynomial of $x^{16}+x^{15}+x^2+1$ (refer to figure 4-11). The input data is exclusively ORed with the full register content (x^{16}). The resultant output is then exclusively ORed with x^2 and x^{15} to conform with the polynomial. These registers continually change as the character data for each word changes, and after completion of the data transfer to the tape, the CRC word retained in the register is clocked out. This is accomplished by SQ3 and SQ4 going high when the write time sequencer is advanced. These signals are consecutive and each permits one-half of the CRC's 16 bits to be strobed from the CRC generation registers. Data transmission is permitted when AND gate F6 is enabled via OR gates D7 and D6. Also at SQ3 and SQ4 time, GTCRC goes high and the input to AND gate E4 goes low; these two signals inhil additional input to the CRC generation registers. The CI data is coupled to the write data encoder via generati gates F6, where the data is transformed to phase transiti codes for application to the tape.

Postamble

When the write sequencer advances from SQ4 to SQ5, t postamble (10101010) is loaded into the output shift reg ters, C11 and B10. Loading is the same as for the preambl

Inter-Record Gap (End)

When the write sequencer advances to SQ6, the stop del one-shot is activated. This allows approximately 36 mil seconds for the application of dc polarity (high) to the ta by the active data output driver. At the end of this delay sequence inhibit (SQINH) is applied to the write data outp latch to inhibit data transitions. Approximately 40 mil seconds later the tape stops.

READ DATA DEVELOPMENT

After the tape is installed in the transport, positioned at t beginning-of-tape, and up to speed in a forward directi the character development begins (figure 4-12). Positi and negative signal transitions are converted to digi levels by the OR gates of J2. The OR gate outputs set a reset cassette data flip-flop K2 to produce composite re data that enables and disables read data latch flip-flop

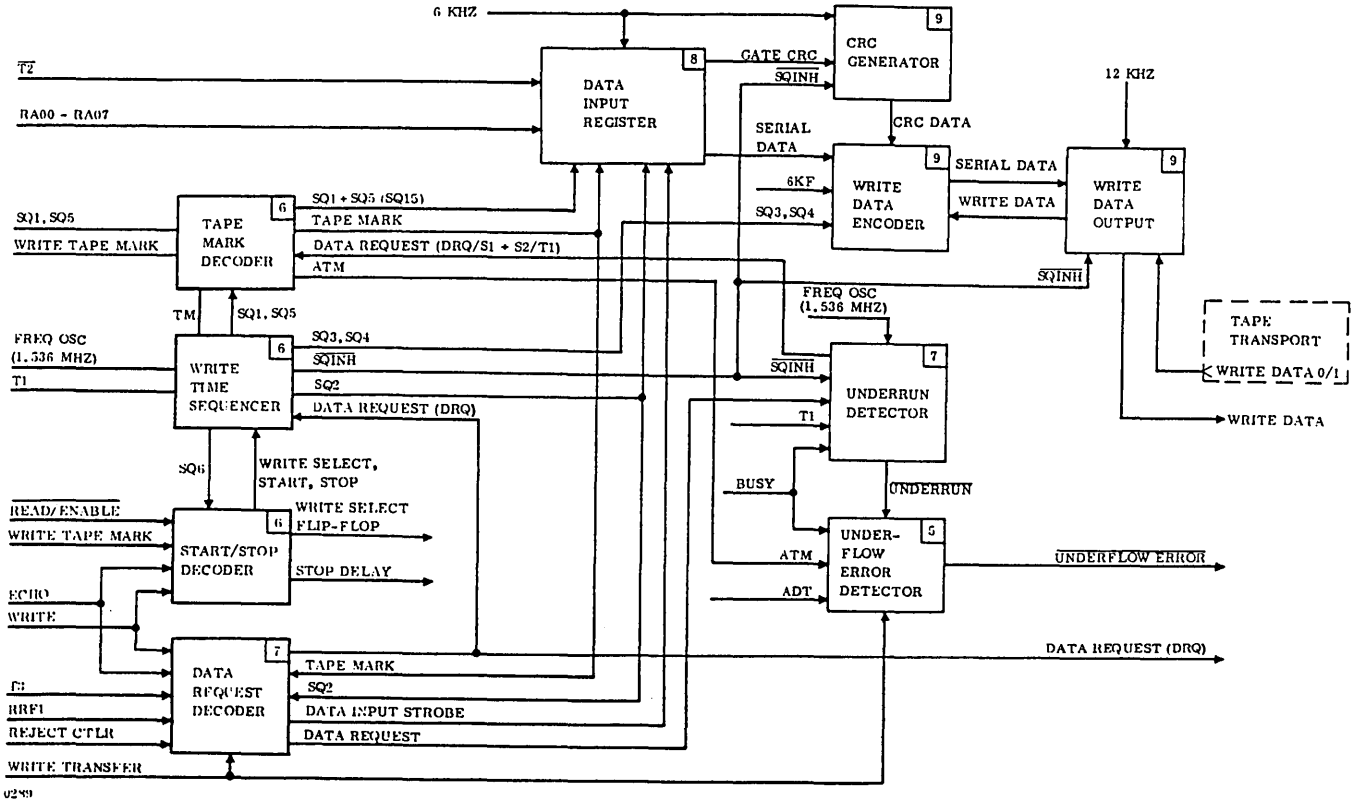


Figure 4-9. Write Data Sequence

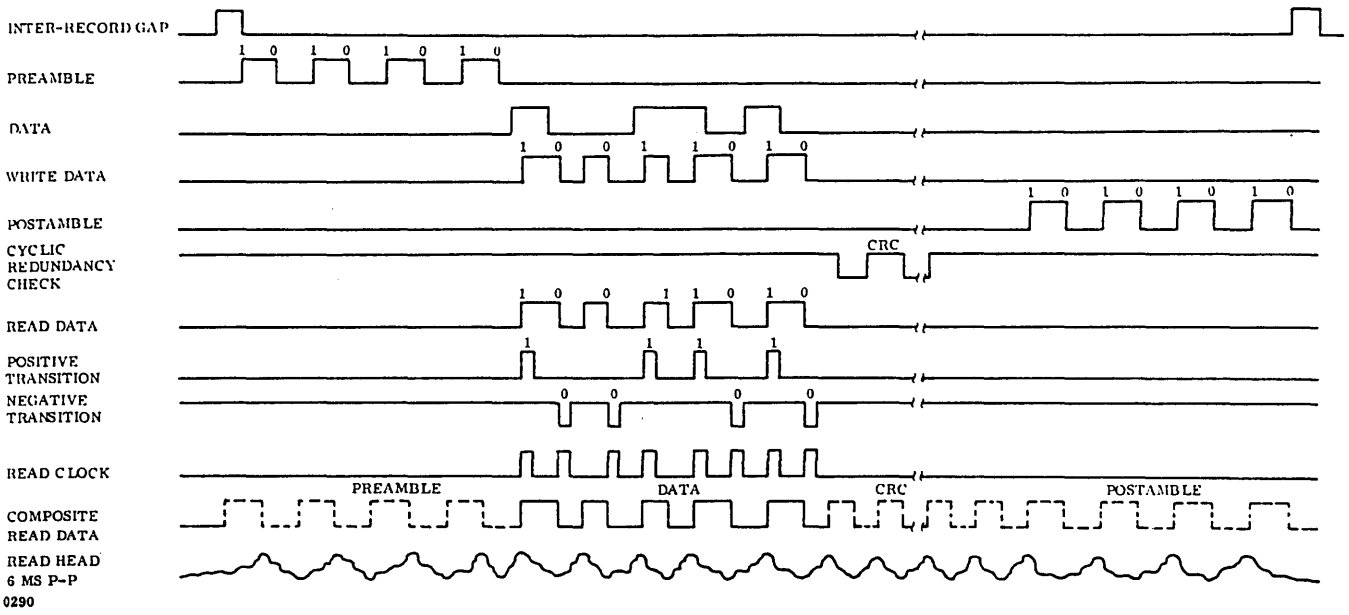


Figure 4-10. Manchester Code (Phase Encoded) Relationship

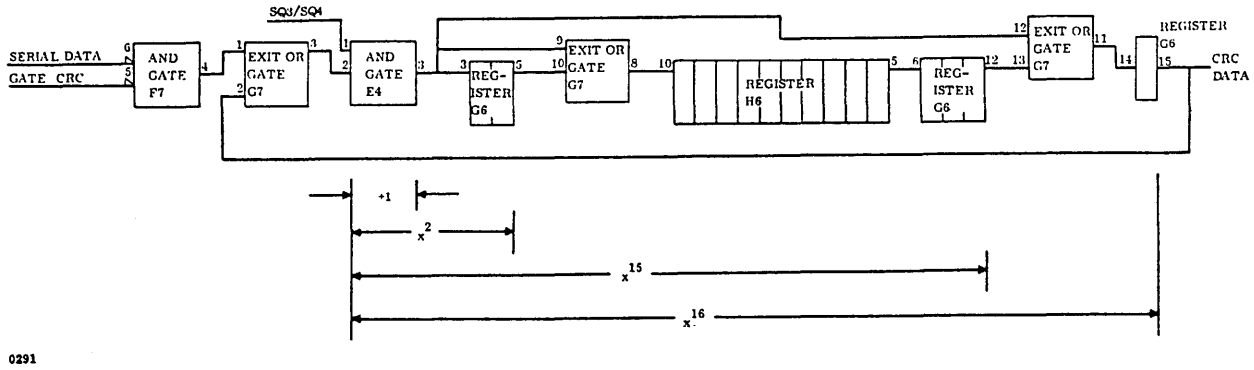


Figure 4-11. Simplified Logic Diagram of Write Cyclic Redundancy Check Generation

via AND/OR gate C5 when the echo latch ($\overline{\text{ECOL}}$) signal at D5-12 is low. If the cassette is in echo mode, the tape is motionless and the write data (WDTA), enabled by the ECOL signal at C5-10, enables and disables read data latch flip-flop D5. This permits the echo mode write data to be processed by the read logic without tape motion. The read data latch is clocked by the 192 kHz signal to produce the data bits (bit polarity). These data bits (D5 outputs) are loaded into read register 1 (D3) and are used to synchronize the phase lock loop to the recovered read data streams. The phase lock loop output triggers the bit clock to produce the bit clock signals that strobe the read data registers (D3, C3, C2, and A8), the character generator (E1), the read CRC decoder (A3 and B2), the error detector (F3), and the gap detector (C1).

The low and high bit polarity signals from the read data latch flip-flop (D5) are applied to exclusive OR gate D4. When D4 detects two low or high inputs, a transition-detected low signal is generated to reset the gap detector (C1) and enable the phase lock loop. Resetting the gap detector sets bit clock flip-flop F5 and enables OR gate F6. When the bit polarity signal strobes the F5 bit clock, the bit clock signals load the data bits into read register 1.

The gap detector (C1) is strobed by the bit clock pulses to detect the presence of a gap and to reset read register 1 and bit clock flip-flop F5. The transition-detected (TRN. DET) signal is applied to the gap detector (C1) to start the count when a gap is present. When data is present, the transition-detected signal keeps the counter alternately reset at intervals that do not permit the data-detected signals to be generated. When a gap is detected, the counter remains set long enough for the data-detected signals to be generated and to reset read register 1 (D3) and the bit clock (F5). The data-detected (D/D) output ensures that the first read buffer register is empty before it is reset, and the data-detected clock (D/D CLK) pulses ensure that the CRC bits are strobed through the buffer register before the preamble/postamble latch is reset to discard the postamble bits.

The character strobe generator produces the character strobe ($\overline{\text{CHRST}}$) and strobe enable latch (STB.ENA.L.) signals that gate CRC error detector F2 and tape mark detector F2 and reset read register 4. These strobes are generated by the character timing register (E1), which provides a high output coincident with the eighth bit of each character word in time coincidence with the bit clock. The character timing is parallel-loaded with seven lows and one high when the first bit is transferred from read register 3 (C2) to read register 4 (A8). Then the bit clock shifts the low states through the character timing register until the high is present at the output. This high sets character time latch D1, which produces the strobe enable. This strobe enable is ANDed with the character timing high and bit clock pulses to reset read register 4. The strobe enable also has a data available (DATAV) strobe that shifts the data from read output register A10 to data/status multiplexer A11.

The bit polarity signals are also present at the exclusive OR gate D4 (input to read register 1), and if the reverse (REV) signal is high, the bit polarity state enables read register 1 (D3). If the reverse signal at D4 is low, the bit polarity signal is inhibited. The bit polarity status is serial shifted through three read buffer registers, D3, C3, and C2, to parallel output read register 4 (A8). These three buffer registers are required to give enough delay to provide the cyclic redundancy check and postamble transmission. When read register 1 is filled, the bits are parallel-shifted to the preamble/postamble decoder. Since the preamble is a 10101010 bit configuration, AND gates D2, E2, and E3 decipher the preamble and postamble bits to determine that the word in read register 1 is either preamble or data. AND gate D2 senses the highs (1s), and AND gate E3 senses the lows (0s). The resultant output of AND gates D2 and E3 is high if the word is a preamble or postamble. This causes AND gate E2 to set preamble/postamble latch D1, enable CRC error detector AND gate E3, and set runaway detector K5 that enables the runaway alarm at AND gate K11. The preamble/postamble latch output ($\overline{\text{PRPOL}}/\overline{\text{EORL}}$) resets read registers 2 (C3) and 3 (C2) to discard the preamble word in read register 2 and the postamble word in read register 3. $\overline{\text{PRPOL}}/\overline{\text{EORL}}$ also enables format error detector AND gate F6 and resets CRC registers A3 and B2. Character data following the preamble is strobed through read registers 1, 2, and 3 in serial format to read register 4. Read registers 1, 2, and 3 provide the delay required to detect the cyclic redundancy check and postamble after an inter-record gap has been detected.

Data transferred from register 3 to register 4 passes through inverter C4 to provide a set input to latch D1, which senses the resetting of read register 3. When the S and R inputs

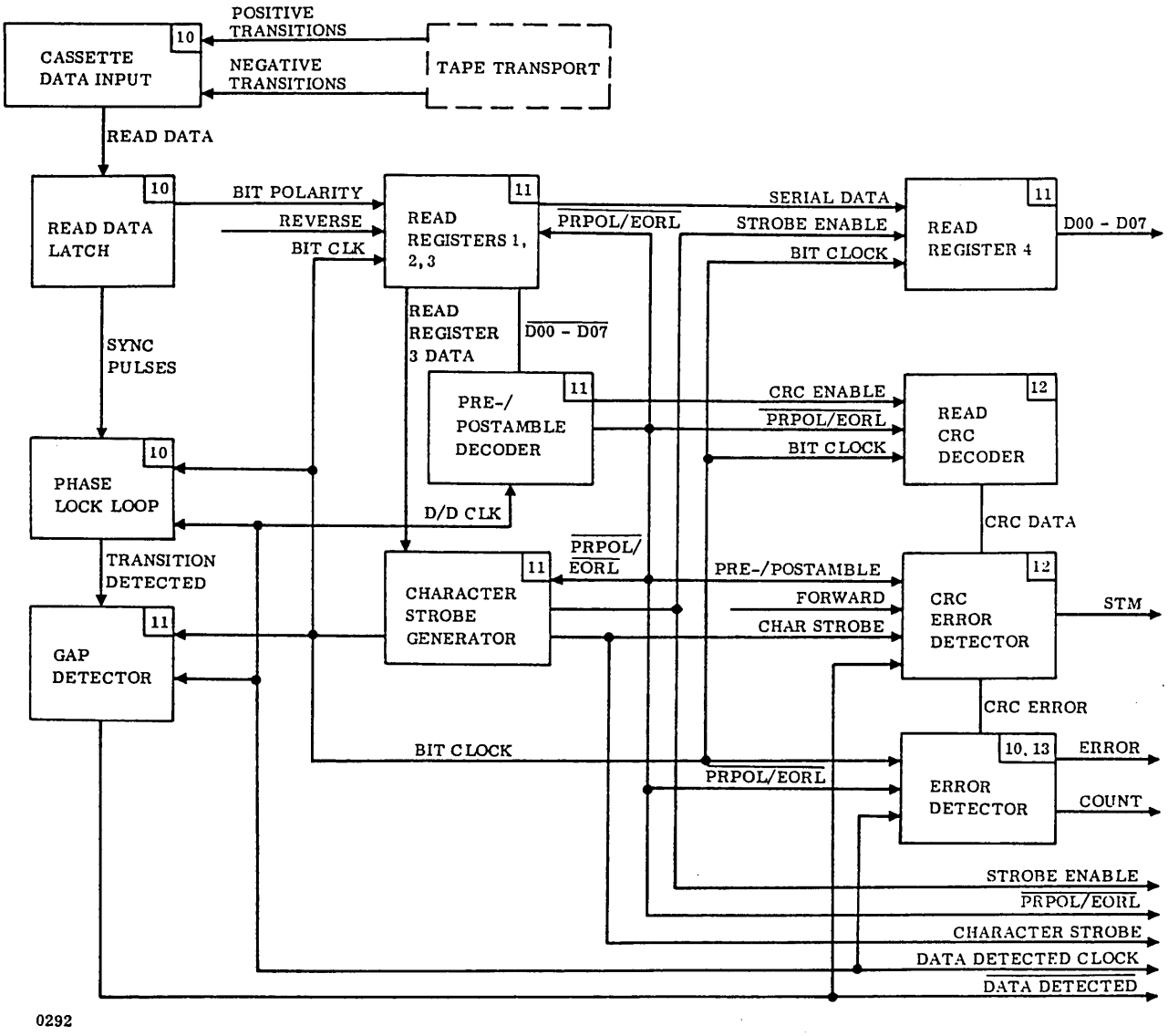


Figure 4-12. Read Data Development

are both low, the RR3DAT signal inhibits the load of character timing register E1 to stop generation of the character strobe and thereby stop the loading of read register 4 and the strobing of the read output register (A10). All character data is parallel-loaded from read register 4 to the read output registers (A10 and A7) by the strobe enable latch signal each time the character timing register output goes high indicating the read register is full and ready for transfer of data.

CYCLIC REDUNDANCY CHECK

The cyclic redundancy check logic accumulates a read CRC word in CRC registers B2 and A3 (figure 4-13) in accordance with the same polynomial ($x^{16}+x^{15}+x^2+1$) as the write CRC generator. When the write CRC word is shifted into the read CRC registers, the resultant output to AND gates A2 and B1 must be zero. If AND gate A1 detects any low, indicating a data error, the CRC error latch is not enabled and a CRC error is sent via data/status AND gates F1 and E12 to the I/O-TTY controller for relaying to the CPU. If AND gate A1 detects all highs, the CRC error latch is enabled and set by the character strobe. This produces a low output which inhibits the CRC error condition at AND gate F1. This polynomial method of verifying write/read data is required by the ECMA-34 standard and is a reliable method of redundancy checking.

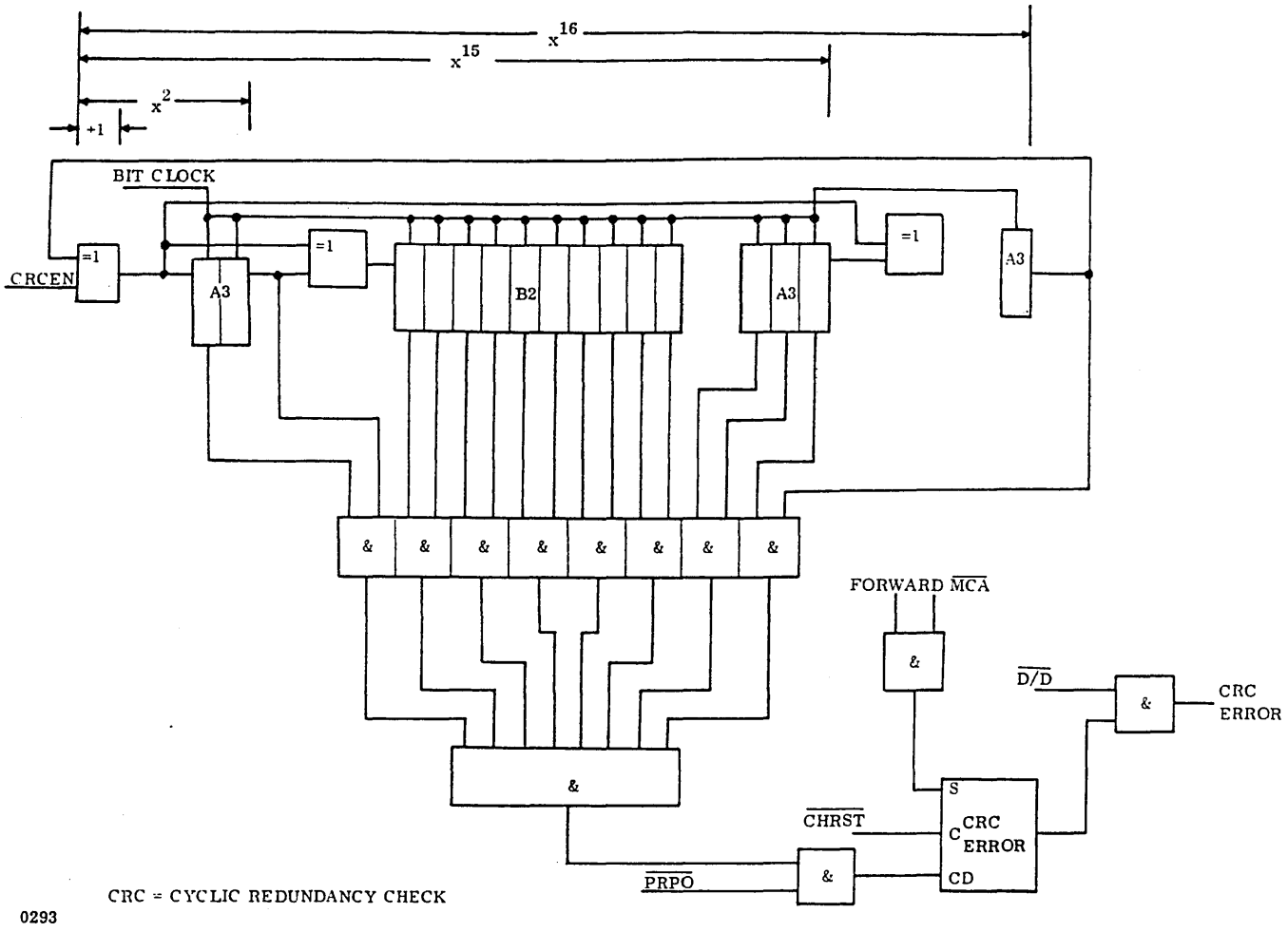


Figure 4-13. Read Cyclic Redundancy Check Analyzer

DEADSTART SELECTION

Deadstart data can be loaded into the CPU from the tape cassette over the same lines as the other deadstart devices (figure 4-14). When the deadstart loading from the cassette is selected (the deadstart switch on the operators panel is activated), deadstart enable signal SM204 goes low. If the tape transport is ready (RDY COND high) and not busy, the deadstart select detector (deadstart latch J5) is then set; output is high. The set input inhibits the deadstart latch if any of the inhibit conditions, error, auto-rewind, end-of-operation, stop delay, or master clear, are active in the deadstart inhibit detector G5, E2, or J3. Since the set condition of the latch is high and deadstart is selected, deadstart output register A9 is enabled to load deadstart data (Z00 through Z07). This read data is developed as discussed in Read Data Development above and is obtained from read register 3 (A8). The read data is also applied to the deadstart character delete decoder (L9, L7, J11, and K5) to detect the time control (ASCII space) code A0 (20 with even parity). This code is present, singly or in groups, immediately following deadstart data bytes to provide the panel interface and the CPU time to manipulate the deadstart data. This byte is not transmitted but allows the tape to run until the panel interface is ready for the next significant data byte. This code is inhibited by setting and resetting latch K5. When data is available and AND gate L9 output is high (indicating the $A0_{16}$ code is not present), latch K5 is set. This applies an enable to AND gate K12 to permit the serialized data from the deadstart output register (A9) to be placed on the deadstart data bus (terminal 41). When the $A0_{16}$ code is present or data is not available, the output of OR gate L7 resets the latch. When reset, the latch applies a low to AND gate K12 to inhibit the flow of data to the deadstart data bus. The deadstart data is clocked out of the deadstart output register when the register is enabled (S0 input high) and data available is high (S1 input) at the 9600 baud rate by the 96 kHz strobe signal:

S0	S1	Operation
0	0	Hold
0	0	Clear
0	0	Load
0	0	Shift

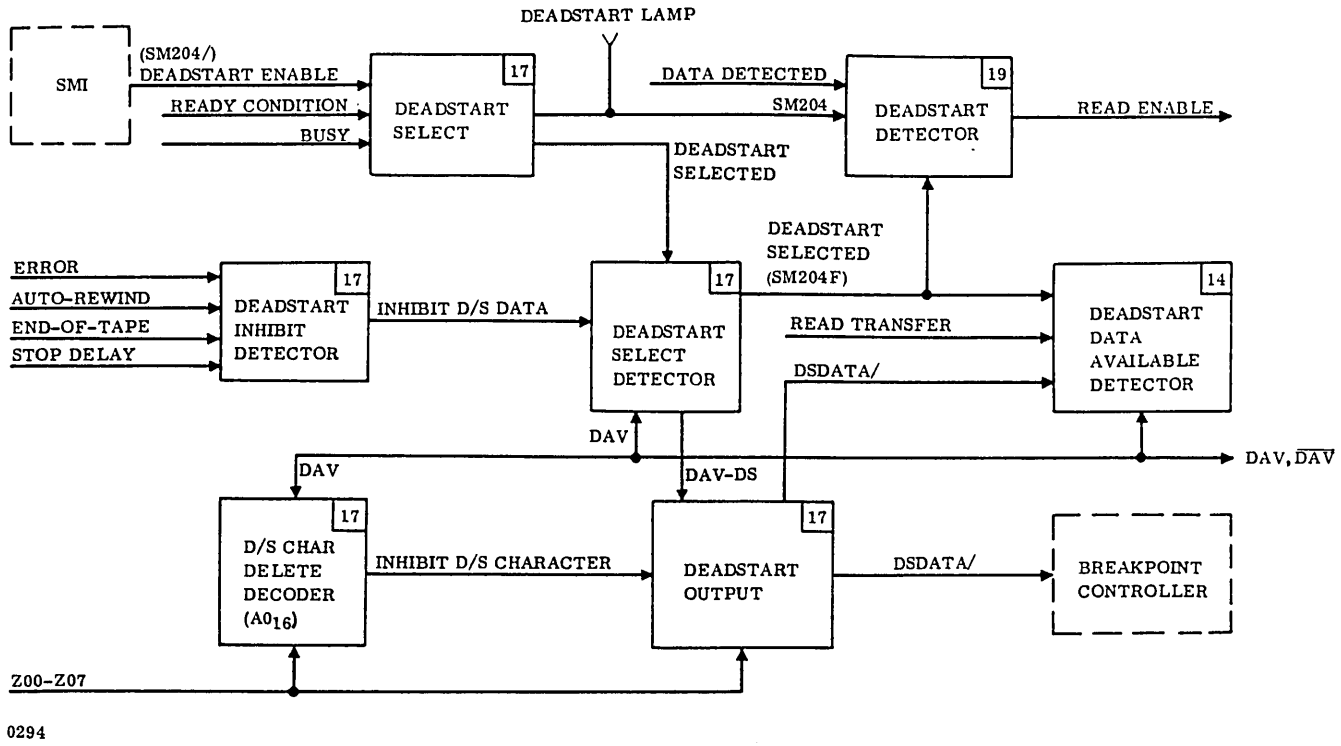


Figure 4-14. Deadstart Selection

The deadstart select detector outputs (SM204F high and low) are also used to continue the deadstart loading until all deadstart data is transferred to the breakpoint controller. As long as data is detected and the deadstart flip-flop is set, read enable latch L2 is set and character strobe (DATAV) latch K2 is reset. The read enable is held set by the presence of the data detected, SM204F, and deadstart-selected signals at AND gate L5. Likewise, character strobe DATAV is inhibited by the SM204F signal resetting the read character enable latch K2 via OR gate J2.

DATA/STATUS READ OUTPUT

Character data transferred from read register 4 (A8) is parallel-loaded into read output register A10 (figure 4-15). This data is then strobed to the data/status selector by character strobe DATAV. This data is transferred to the I/O-TTY controller open collector lines via lines RD01 through RD16 when the data/status selector strobe (DSMSEL) signal is low. The strobe is derived by the data/status detector F8. When the inputs (read transfer, reject controller, and reply/reject frequency 1) are all high, the strobe clocks either the data or status through the multiplexer depending upon the status signal condition. When the status signal and strobe are low, the director status data is transferred to the CPU via the I/O-TTY controller, and when the status signal is high, the strobe transfers character data (D00 through D07). The director status bit definitions are described under Cassette Controller Input/Output Bit Descriptions in section 2. Character data (D00 through D07) is transferred in ASCII code via the panel interface to the CPU.

TAPE TRANSPORT INTERFACE

The tape transport control logic (figure 4-16) determines that the tape cassette and tape transports are ready for service (read or write). This logic determines that the tape cassette is installed, tape side A or B is active, the unit is selected, and the tape lid is closed. When these are accomplished, the tape transport is ready.

After the tape transport is ready, the tape is positioned to the beginning-of-tape by the auto-rewind or external rewind facilities. When the tape has been positioned to beginning-of-tape, the READY indicator lights, the ready status goes high, and the active ready condition enables the motion control, reject decoding, read data/status, deadstart, and alarm logic.

Tape Transport Select

Drive multiplexer H4 determines the operating transport through the application of the unit 1 switch selection. If the

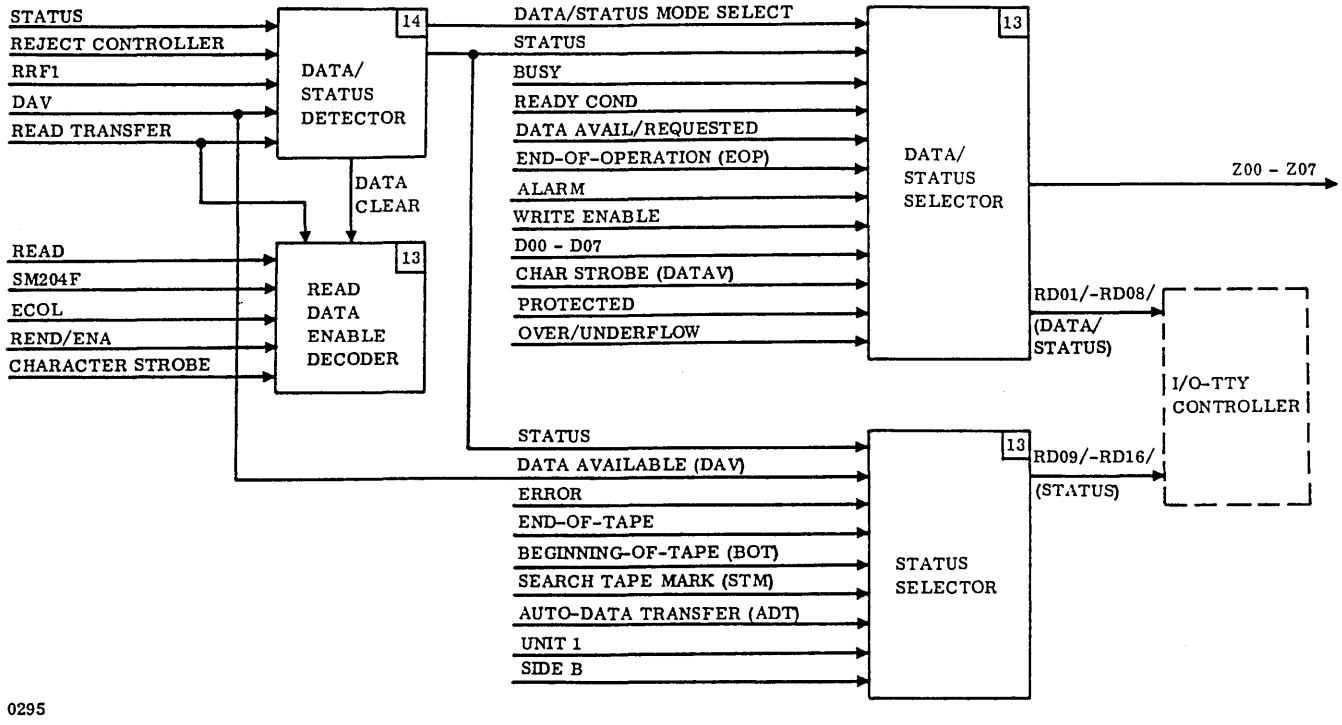


Figure 4-15. Data/Status Read Output

select unit 1 switch (SW2) is closed, the unit select latch is set. When control function bit RA12 is high and no operation function is high, the unit select latch is forced to the select unit 1 condition. Otherwise, unit 1 can be selected by control function bit RA11 being high and the select unit 1 switch being open. When either condition exists, the associated lamp driver applies ground to the UNIT 1 SELECT LED† on the operators panel. If the switch or control function bit is not selecting unit 1, then unit 0 is selected and the UNIT 0 SELECT LED illuminates. If either lamp is illuminated, it indicates that a unit has been selected.

Tape Rewind

If unit 1 has been selected, the drive multiplexer is set to provide the enable (write, TB-EOT, and auto-rewind) to the respective logic (motion detector number 1, clear leader detector, end-of-tape, deadstart, rewind, tape mark, and tape movement). The write enable and side B status is applied to the read data/status logic. These signals all initiate at the tape transport, with the exception of the automatic rewind (A-RWND), which is activated by setting the applicable A-RWND ENA switch (SW2 segment 1 or 2). When the lid signal is low (lid closed) and the associated A-RWND ENA switch segment is set, AND gate H3 applies a high to AND gate K8 for unit 0 or J7 for unit 1. This high is inverted by K6 and ANDed with the output from H3. The resultant high from K8 is applied to the drive multiplexer and couples the selected condition to the auto-rewind logic. If the A-RWND ENA switches are not enabled, the auto-rewind function commands are always operational.

Unit Ready

When the unit has been selected, the selected unit 0 or 1 condition is ANDed with the transport ready (TRDY). If the unit selected and transport ready conditions coincide, the respective AND gate (H10) provides the associated unit (0 or 1) ready to the write select (unit 0 or 1), read enable (unit 0 or 1), and stop/go (unit 0 or 1) logic of the transport control. The selected ready conditions are ORed by H10 and inverted by M7 to generate the tape transport ready condition. The ready condition is ANDed with the error and rewind conditions at AND gate H7. If no error exists and rewind is complete, indicating the tape is at the beginning-of-tape, the READY lamp illuminates when driver G3 applies ground to the LED.

TAPE TRANSPORT CONTROL

The tape transport control logic (figure 4-17) provides the interface between the micro processor and the tape transport. This logic detects and controls the tape transport

†The controller provides LED drivers; however, a particular configuration may or may not include the LEDs.

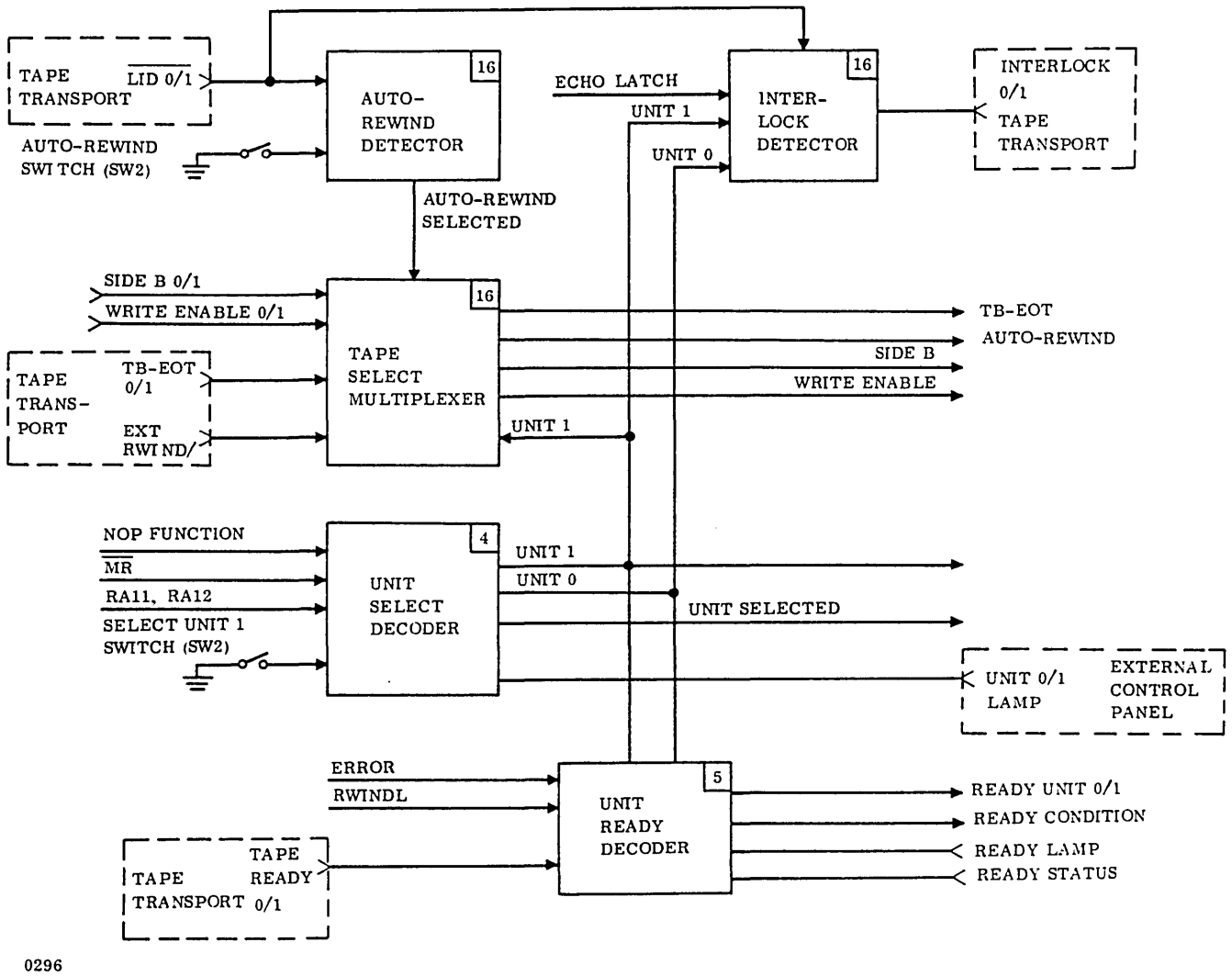


Figure 4-16. Tape Transport Interface

operation. The controlled operations are: tape motion (stop/go, forward/reverse, fast/slow, and end-of-operation), tape position (clear leader, dark tape, beginning-of-tape, and end-of-tape), and tape transcription (write, read, and erase).

Tape Motion

The tape motions slow/fast and forward/reverse are controlled by the respective speed and direction logic associated with the slow and forward latches (G1). When the slow and forward latches are set, the tape moves in fast reverse. A tape advance enable from OR gate J10 that is determined by search tape mark forward, sequence 2, read, or deadstart, and a write select or a rewind/beginning-of-tape one-shot high at K7 enables the slow and forward latches (G1). At the next high applied to the clock, the forward latch sets (determined by the tape at the beginning-of-tape, reverse not selected, no rewind, not auto rewind, and not backspace), and a high applied to the slow latch sets the slow latch to select the slow forward action. When these latches (G1) are reset, the slow and reverse motions are selected. Write, read, or erase are never accomplished during a reverse or fast motion, except for tape mark search.

Read Enable

Read enable is active and the tape is set in motion whenever the conditions read, deadstart, or search tape mark are active (OR gate J10). If any J10 input is low, READ ENA 1

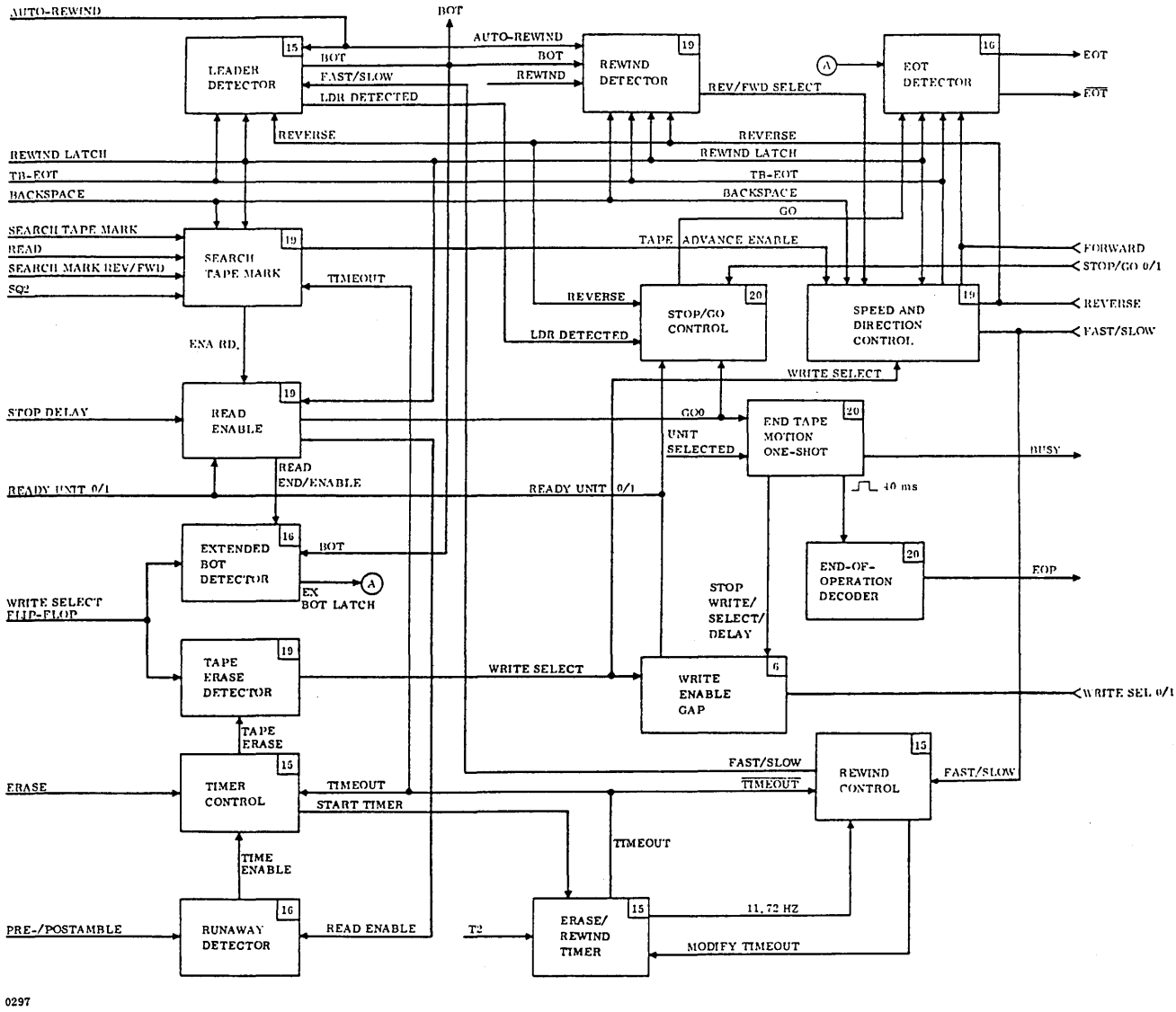


Figure 4-17. Tape Transport Control

latch L2 is enabled. When data is detected and count 8 is high at AND gate L1, the READ ENA 1 latch is set. This enables READ ENA 2 latch L2 via OR gate L3. When the frequency oscillator (FO) pulse clocks L2, the high output at pin 5 provides the READ ENA signal to the active transport, determined by the RDY signal at READ ENA AND gate H12. If the stop delay input to OR gate L3 is also low, the enable of the READ ENA 2 latch is also inhibited. With the READ ENA 2 latch set, the low output at pin 6 initiates the GO0 signal at OR gate K3. This K3 low is applied to AND gate J3 and inverter K6. With the rewind/beginning-of-tape one-shot L6 output low, AND gate J3 activates the readied transport, determined by the activated RDY signal present at stop/go AND gate H12. The GO0 signal also causes the controller to go busy. As long as these two latches remain latched, the tape is in motion. When the READ ENA 2 latch resets, the GO signal is inhibited. This causes the transpor to stop, the read end is enabled, and the controller goes nc busy.

Tape Position

When the tape cassette is inserted into the tape transport the tape is automatically positioned at beginning-of-tap before the READY lamp lights. This is accomplished by th position logic that detects the TB-EOT signal from th transport via the transport interface. The detected TB-EO condition indicates clear tape, dark tape, and beginning-of tape/end-of-tape. The logic tests for light when the tape i moving toward the clear leader. When a clear leader ha

been detected, the tape moves forward until light is sensed again; this is the beginning-of-tape hole, and the tape comes to a halt just in front of the beginning-of-tape. If light (clear leader) has not been detected after three seconds, the transport moves to fast rewind (50 inches per second). The fast speed continues until the transparent leader is sensed, then stops and moves forward at slow speed until beginning-of-tape is detected.

When the dark tape area is detected, a high state is applied to pin 5 of AND gate J8 and a low state is applied to AND gates F11 (pin 13) and J7 (pin 9). The high at J8 causes a disenable of the clear leader latch and an enable of the erase/ rewind (3-second) timer, since the rewind latch and forward latches are reset. This causes the tape to move toward the clear leader at slow speed until a clear leader is detected or 3 seconds have elapsed. When light (clear leader) is detected, the TB-EOT inputs to J8 (pin 5), F11 (pin 13), and J7 (pin 9) change. This causes the rewind and forward latches to set and change the tape direction to forward at slow speed. When the beginning-of-tape hole is detected (light is sensed), the rewind and forward latches reset. AND gate J8 must have two low inputs to cause a high output to disenable the timer and produce a low output from J7 (pin 6). This low and the high from AND/OR gate K1 cause the clear leader latch to reset and thereby halt tape motion and set beginning-of-tape latch K4. The beginning-of-tape status is sent to the CPU via the read/ status RD lines, and the halt tape motion is controlled by the rewind/ beginning-of-tape one-shot that allows a 40-millisecond delay so that the usable tape area is positioned under the read/write heads.

If the end-of-tape latch is set any time during normal operation, the end-of-tape and alarm status is sent to the CPU. This condition occurs if the extended beginning-of-tape latch is not set. Any of the conditions applied to AND gates F7 and F11 or OR gate E8 can cause the extended beginning-of-tape latch to set.

If a clear leader is not detected within 3 seconds, the erase/ rewind timer will provide a timeout condition to rewind control latch J9 and AND gate J8. This inhibits the slow input to AND/OR gate K1 and causes the slow and forward latches to reset. This reset causes a fast reverse of the tape to detect the clear leader and ignore light detected from the beginning-of-tape/ end-of-tape holes. When the clear leader is detected, the tape stops and then proceeds forward at a slow rate until beginning-of-tape is detected.

CONTROLLER TIMING

The controller timing (figure 4-18) provides the reply/reject timing sequence, character time sequence, and various clock frequencies used throughout the controller logic. Refer to figure 4-5 for the timing relationship.

The reply/reject timing is produced by a four-bit register, H11, that is clocked by the crystal oscillator. When the read or write signal is high, the A/Q clock (H11) is set. If the cassette controller select condition is high, the register is enabled and the oscillator frequency activates the timing sequence. Each time the condition remains high or low until the read or write signal drops to reset the register.

The character timing sequence is produced by flip-flops M1 and M2. A 750-Hz frequency clocks flip-flop M2 to set T1 high and enable the T2 flip-flop M1. When the 768 kHz frequency clocks the T2 flip-flop M1, the T2 line goes high and enables the T3 flip-flop M1. At the same instant the T2 signal goes low and resets the T1 flip-flop. When the 768 kHz signal is high once again, T3 goes high and T2 is reset. The T2 reset disables the T3 flip-flop, and at the next high period of the 768 kHz signal, T3 drops. All flip-flops remain idle until the next high period of the 750 Hz signal. The timer then produces another signal sequence.

Sequence

The other clock frequencies are produced by dividing the oscillator frequency in the 12-bit counter provided by the tandem-connected counters M3, M4, and M5, except for the 9.6 kHz signal that is produced by clocking shift register M6 with the 96 kHz frequency created by the divide-by-16 (2^4) output of counter M5. After shifting the register through five positions to divide by 10, the output frequency is 9.6 kHz.

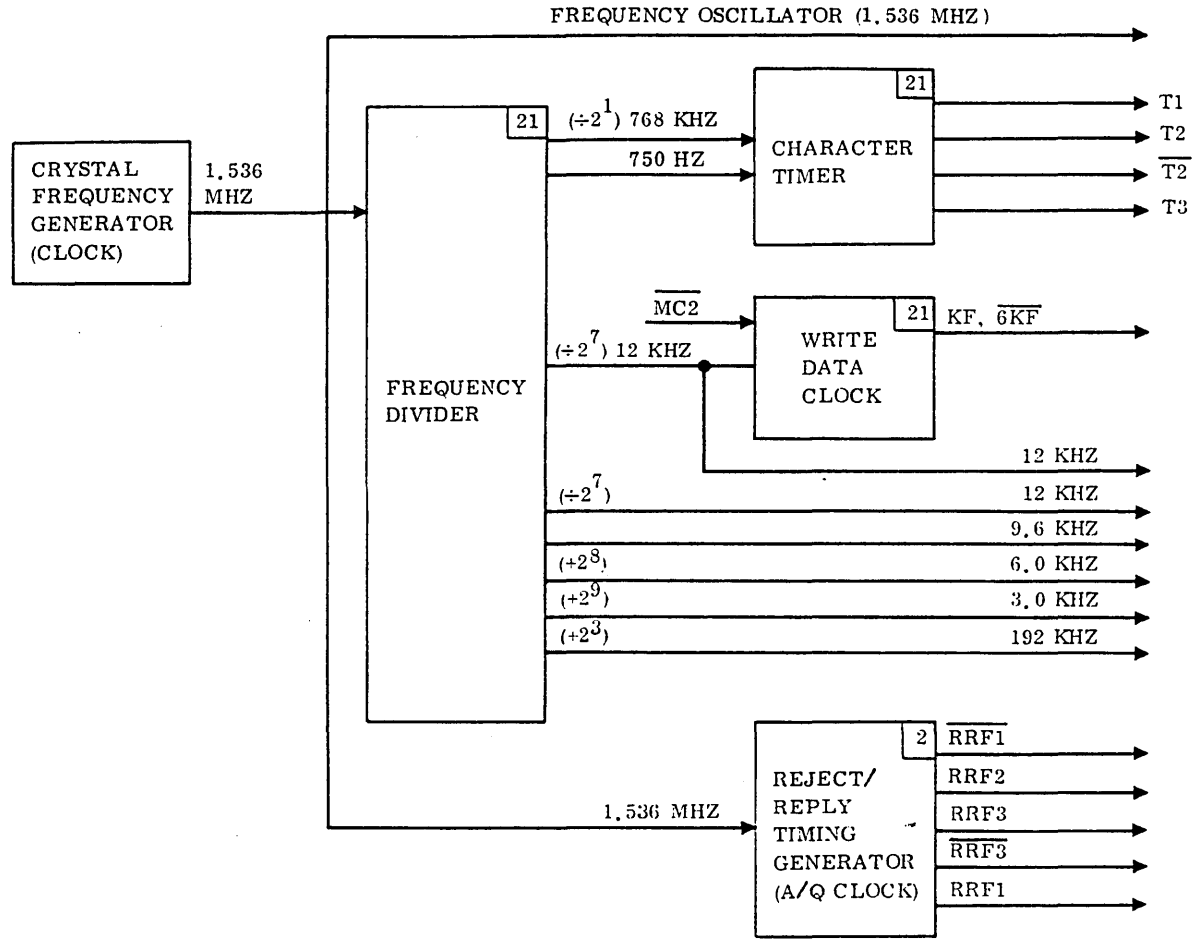


Figure 4-18. Controller Timing Function

TABLE 4-5. GLOSSARY

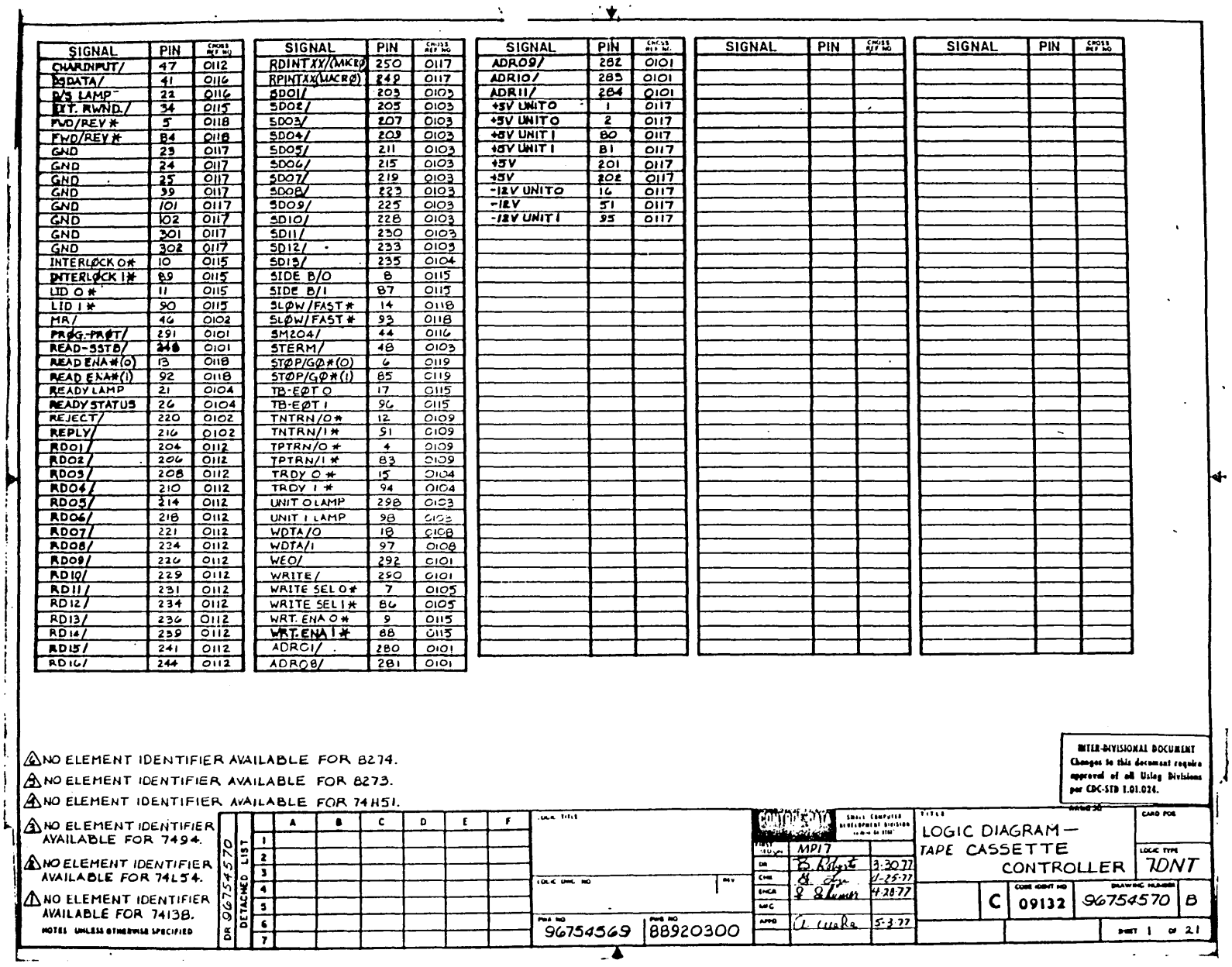
Term	Definition	Term	Definition
ADR	Address (Q register) bits	LID	Transport lid (open or closed)
ADT	Auto-data transfer	MCA	Master clear auxiliary
A-RWND	Automatic rewind	MC1	Master clear no. 1
ATM	Auto-data transfer mode	MC2	Master clear no. 2
BOT	Beginning-of-tape	MFUNC	Legal motion function
B. SPC	Backspace	MOD. T/O	Modify time out
BUSY	Transport busy	MR	Master reset
CFUNC	Clear function	MRUS	Master reset unit select
CHRST	Character strobe	NOP FUNC	No operation function
CLRINT	Clear interrupt	OVFL/UNFL	Overflow/underflow
CNT 8	Count of eight	PRO-PROT	Program protect command
CRCEN	Cyclic redundancy check enable	PROTECTED	Program protect selected
CRC ERROR	Cyclic redundancy check error	PRPOL/EORL	Preamble postamble latch/end-of-record latch
D00-D07	Data bits	RA	Read (A register) bits
DAISTB	Data input strobe	RD	Read data
DAV	Data available	RDY	Ready
DATAV	Data available (character strobe)	RDXFER	Read transfer
D/D	Data detected	RDINT	Data interrupt
D/D CLK	Data detected clock	READ-SSTB	Read-send strobe
DRQ	Data request	RENA	Read enable
D/S DATA	Deadstart data	RDWT	Read or write
DSMSEL	Data status mode selected	RD3DAT	Read register no. 3 data
ECO	Echo	RDY COND	Ready condition
ECOL	Echo latch	REND/ENA	Read end enable
EOT	End-of-tape	RJCTL	Reject controller
FO	Frequency oscillator	REV	Reverse
FUNC	Control Function	RPINT	Program interrupt
FWD	Forward	RRF	Reject/reply timing
FWD/REV	Forward/reverse	RWND	Rewind
GO0	Tape motion (GO)	RWNDL	Rewind latch
GTCRC	Gate cyclic redundancy check	SD01-SD13	Send data lines (write)
LDRDET	Leader detected		

TABLE 4-5. GLOSSARY (Continued)

Term	Definition	Term	Definition
SM204	Deadstart enable	TPTRN	Tape positive transition (read)
SQ1-SQ6	Write sequences	TRDY	Transport ready
SQINH	Write sequence inhibit	TRNDET	Transition detected
SRDATA	Serial data	UNFL	Underflow
STB ENAL	Strobe enable latch	UNFL ERROR	Underflow error
STERM	Send terminate	UNRUN	Under-run
STM	Search tape mark	USEL	Unit selected
STMF	Search tape mark forward	WDTA	Write data
STMR	Search tape mark reverse	WE0	W (Q register) field equals zero
T	Clock time	WRT ENA	Write enabled
TB-EOT	Tape beginning or end-of-tape	WRT XFER	Write transfer
TERASE	Tape erase	WTM	Write tape mark
TIMEN	Timer enable	W/SEL	Write select
TM	Tape mark	W/SELFF	Write select flip-flop
TNTRN	Tape negative transition (read)		

The logic diagrams for the tape cassette controller are contained in figure 5-1. The numbers boxed in the upper right corners of the blocks on the functional block diagrams (section 4) are references to the logic diagram sheet numbers containing the elements used to produce the functional block.

Figures 4-1 and 4-2 show the external data and control interface of the tape cassette controller with other assemblies of the processor and the tape cassette transports.



SIGNAL	PIN	CROSS REF NO
CHARINPUT/	47	0112
DATA/	41	0116
D/S LAMP	22	0116
DT. RWND./	34	0115
FWD/REV *	5	0118
FWD/REV *	B4	0118
GND	23	0117
GND	24	0117
GND	25	0117
GND	99	0117
GND	101	0117
GND	102	0117
GND	301	0117
GND	302	0117
INTERLOCK 0*	10	0115
INTERLOCK 1*	89	0115
LID 0 *	11	0115
LID 1 *	90	0115
MR/	46	0102
PROG-PROT/	291	0101
READ-GSTB/	248	0101
READ ENA*(0)	13	0118
READ ENA*(1)	92	0118
READY LAMP	21	0104
READY STATUS	26	0104
REJECT/	220	0102
REPLY/	216	0102
RD01/	204	0112
RD02/	206	0112
RD03/	208	0112
RD04/	210	0112
RD05/	214	0112
RD06/	218	0112
RD07/	221	0112
RD08/	224	0112
RD09/	226	0112
RD10/	229	0112
RD11/	231	0112
RD12/	234	0112
RD13/	236	0112
RD14/	239	0112
RD15/	241	0112
RD16/	244	0112

SIGNAL	PIN	CROSS REF NO
RDINTAX/(MACRØ)	250	0117
RPINTAX(MACRØ)	248	0117
SD01/	203	0103
SD02/	205	0103
SD03/	207	0103
SD04/	209	0103
SD05/	211	0103
SD06/	215	0103
SD07/	219	0103
SD08/	223	0103
SD09/	225	0103
SD10/	228	0103
SD11/	230	0103
SD12/	233	0103
SD13/	235	0104
SIDE B/0	8	0115
SIDE B/1	87	0115
SLØW/FAST*	14	0118
SLØW/FAST*	93	0118
SM204/	44	0116
STERM/	48	0103
STØP/GØ*(0)	6	0119
STØP/GØ*(1)	85	0119
TB-EØT 0	17	0115
TB-EØT 1	96	0115
TNTRN/0*	12	0109
TNTRN/1*	91	0109
TPTRN/0 *	4	0109
TPTRN/1 *	83	0109
TRDY 0 *	15	0104
TRDY 1 *	94	0104
UNIT 0 LAMP	298	0103
UNIT 1 LAMP	98	0103
WDTA/0	18	0108
WDTA/1	97	0108
WEO/	292	0101
WRITE/	290	0101
WRITE SEL 0*	7	0105
WRITE SEL 1*	86	0105
WRT. ENA 0 *	9	0115
WRT. ENA 1 *	88	0115
ADRC1/	280	0101
ADRC0/	281	0101

SIGNAL	PIN	CROSS REF NO
ADR09/	282	0101
ADR10/	285	0101
ADR11/	284	0101
+5V UNIT 0	1	0117
+5V UNIT 0	2	0117
+5V UNIT 1	80	0117
+5V UNIT 1	81	0117
+5V	201	0117
+5V	202	0117
-12V UNIT 0	16	0117
-12V	51	0117
-12V UNIT 1	95	0117

SIGNAL	PIN	CROSS REF NO

SIGNAL	PIN	CROSS REF NO

⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 8274.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 8273.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 74H51.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 7494.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 74L54.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 74138.
NOTES: UNLESS OTHERWISE SPECIFIED

DR 96754570 DETACHED LIST

	A	B	C	D	E	F
1						
2						
3						
4						
5						
6						
7						

LOGIC TITLE
LOGIC UNIT NO — REV
PWB NO 96754569 | PWB NO 88920300

CONTROL DATA CORPORATION — SMALL COMPUTER DEVELOPMENT DIVISION

DRAWN	MPI7	
DR	B. Wright	3-30-77
CHK	[illegible]	4-25-77
ENGR	S. Skinner	4-28-77
MFG		
APPD	[illegible]	5-3-77

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

TITLE: LOGIC DIAGRAM — TAPE CASSETTE CONTROLLER
CARD POS
LOGIC TYPE 7DNT
C | CODE IDENT NO 09132 | DRAWING NUMBER 96754570 | B
SHEET 1 OF 21

Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 1 of 22)

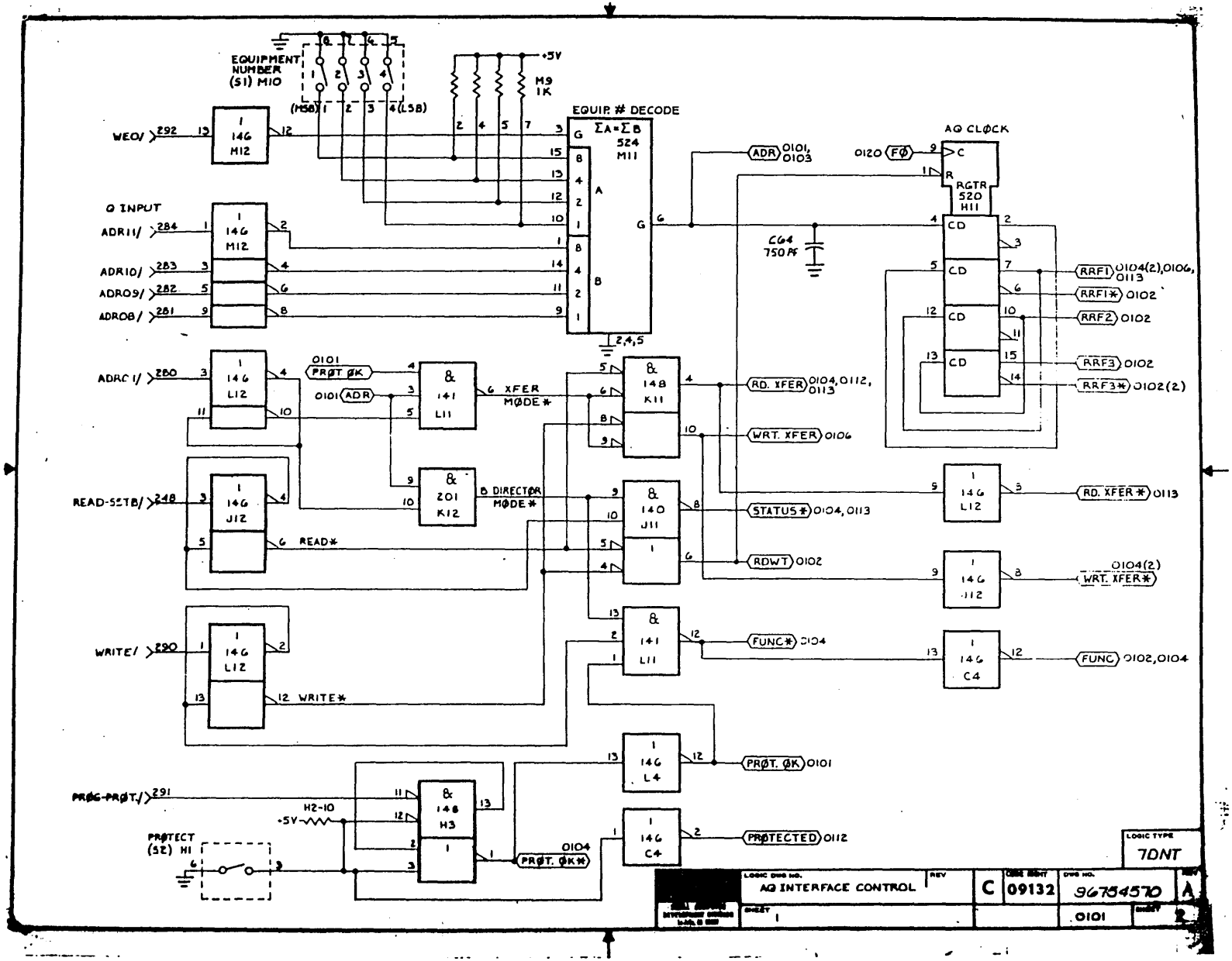


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 2 of 22)

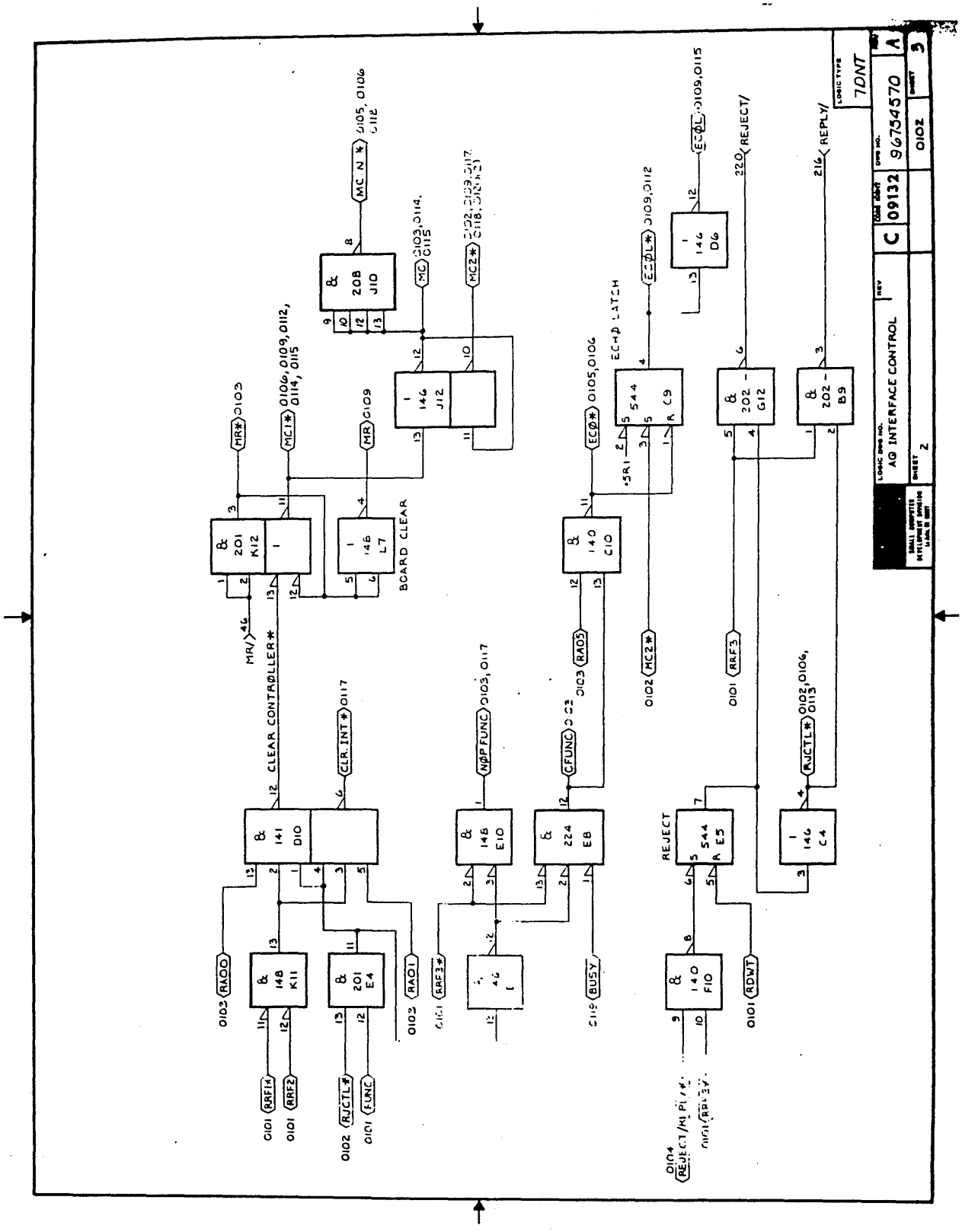


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 3 of 22)

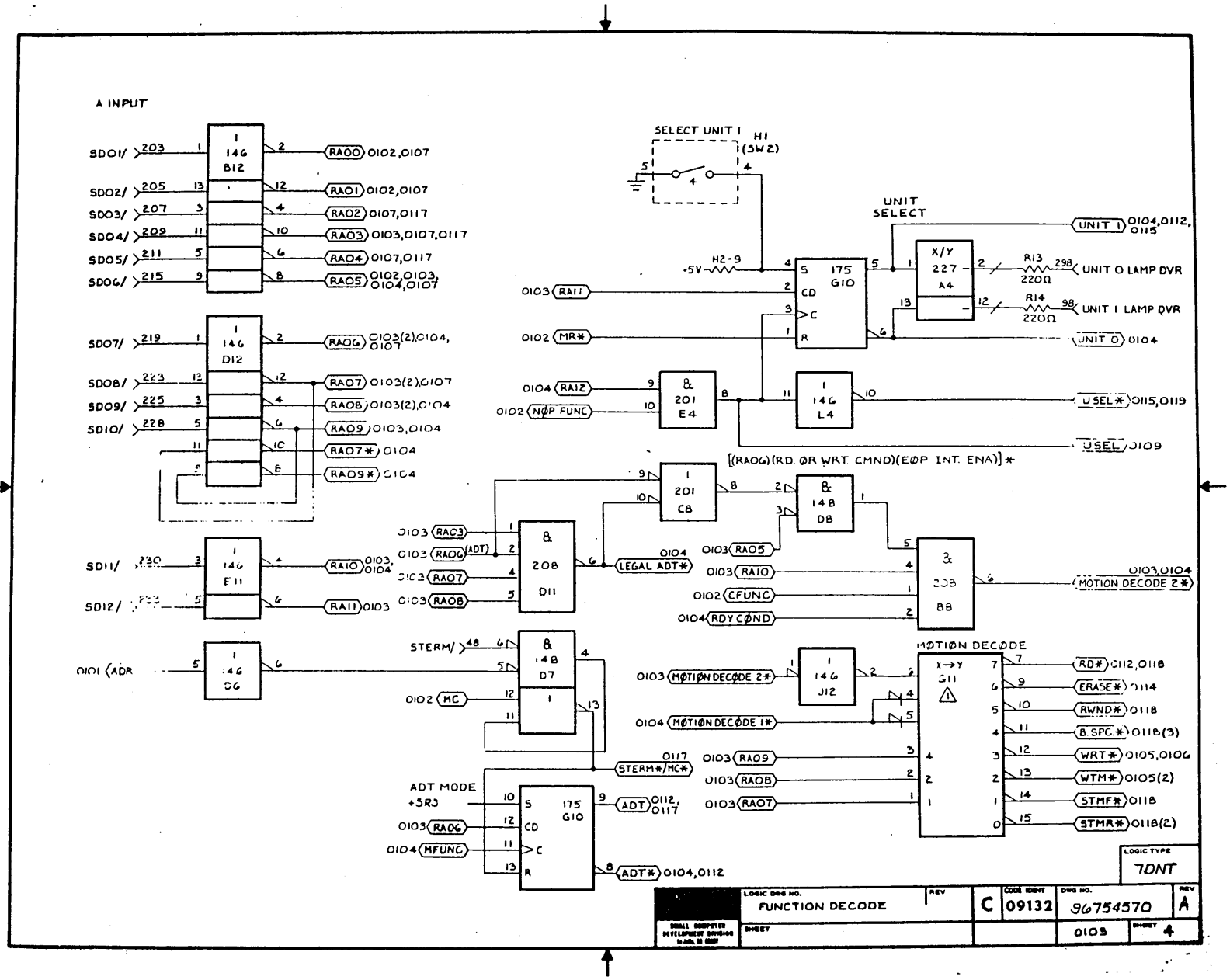


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 4 of 22)

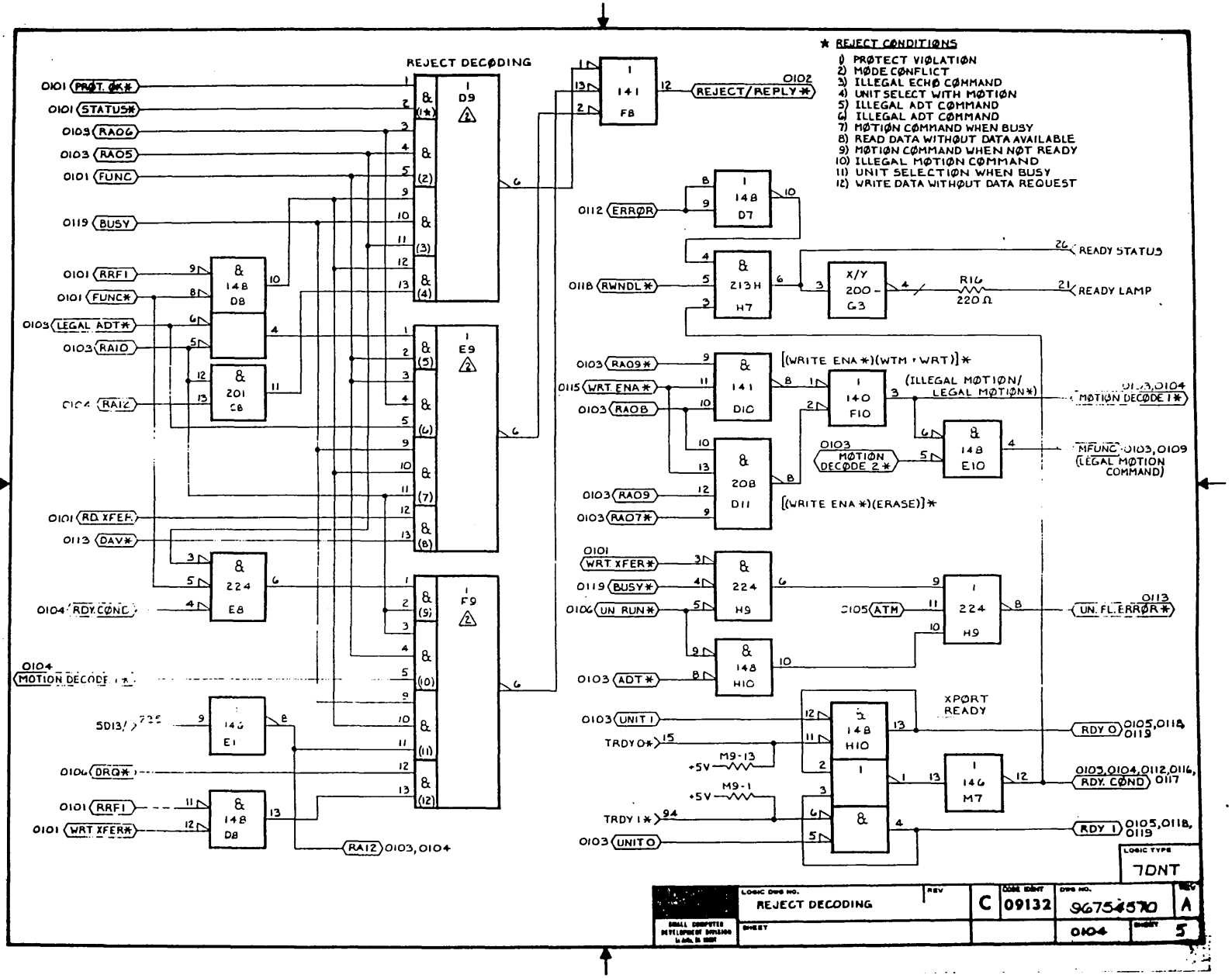


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 5 of 22)

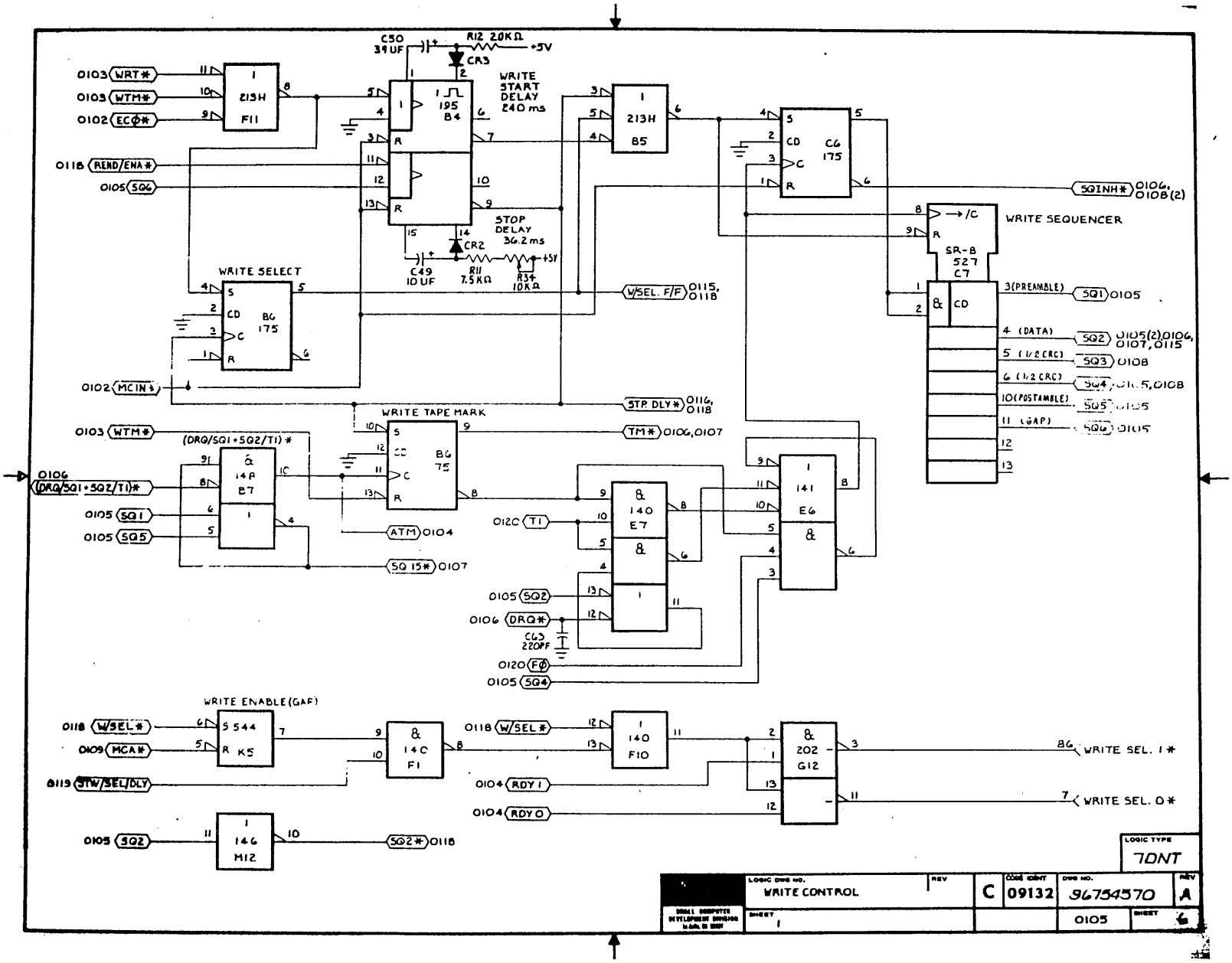


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 6 of 22)

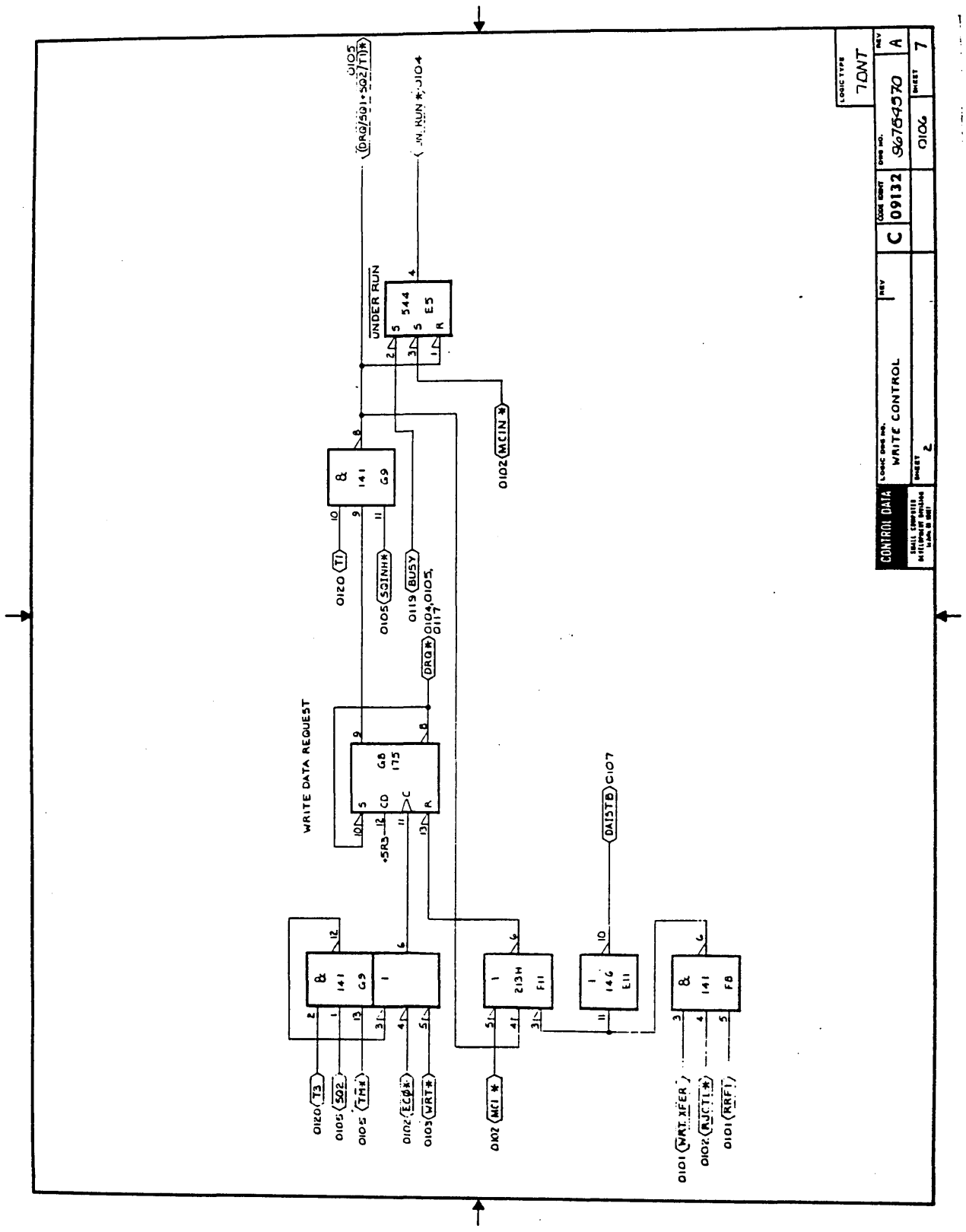


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 7 of 22)

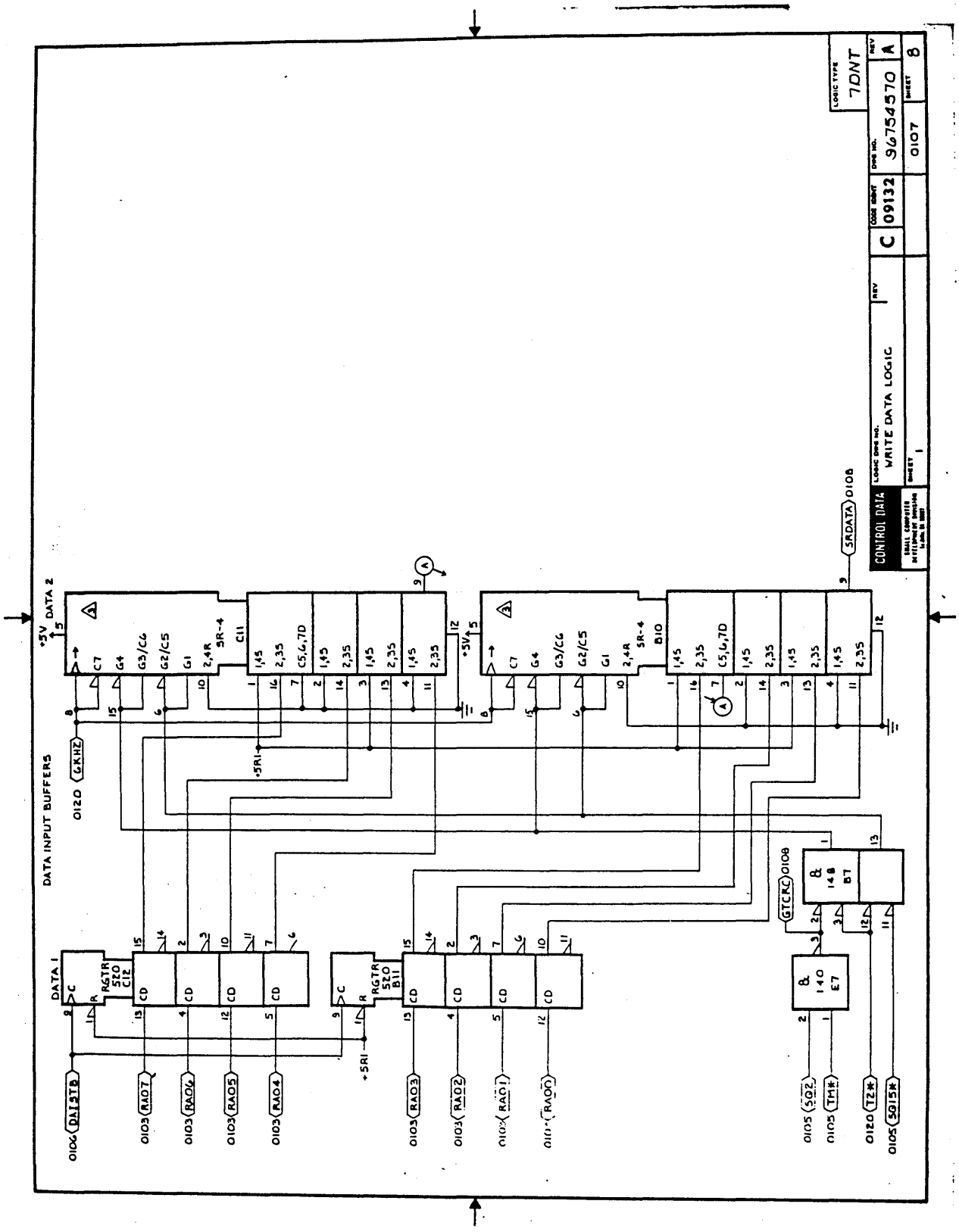


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 8 of 22)

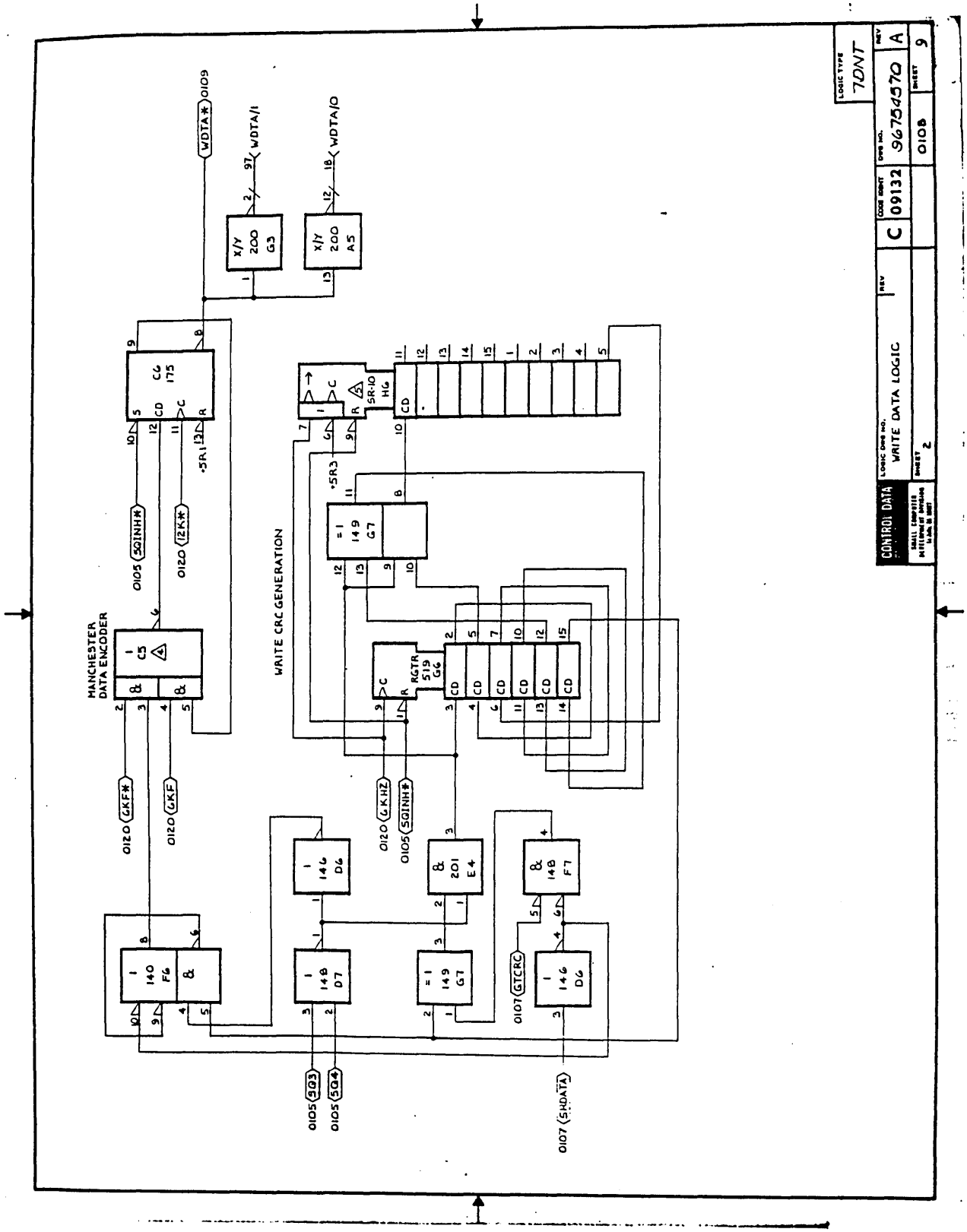


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 9 of 22)

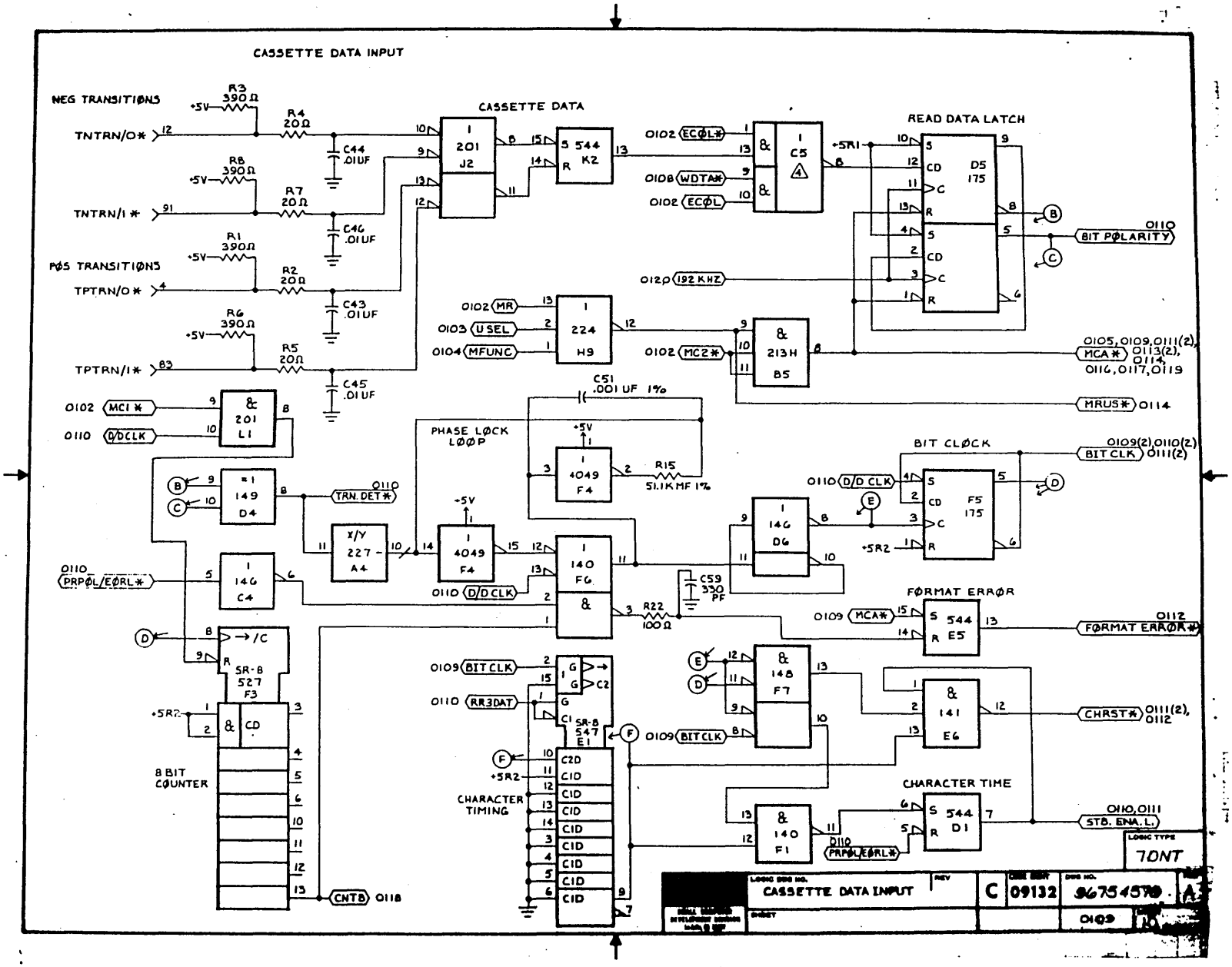


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 10 of 22)

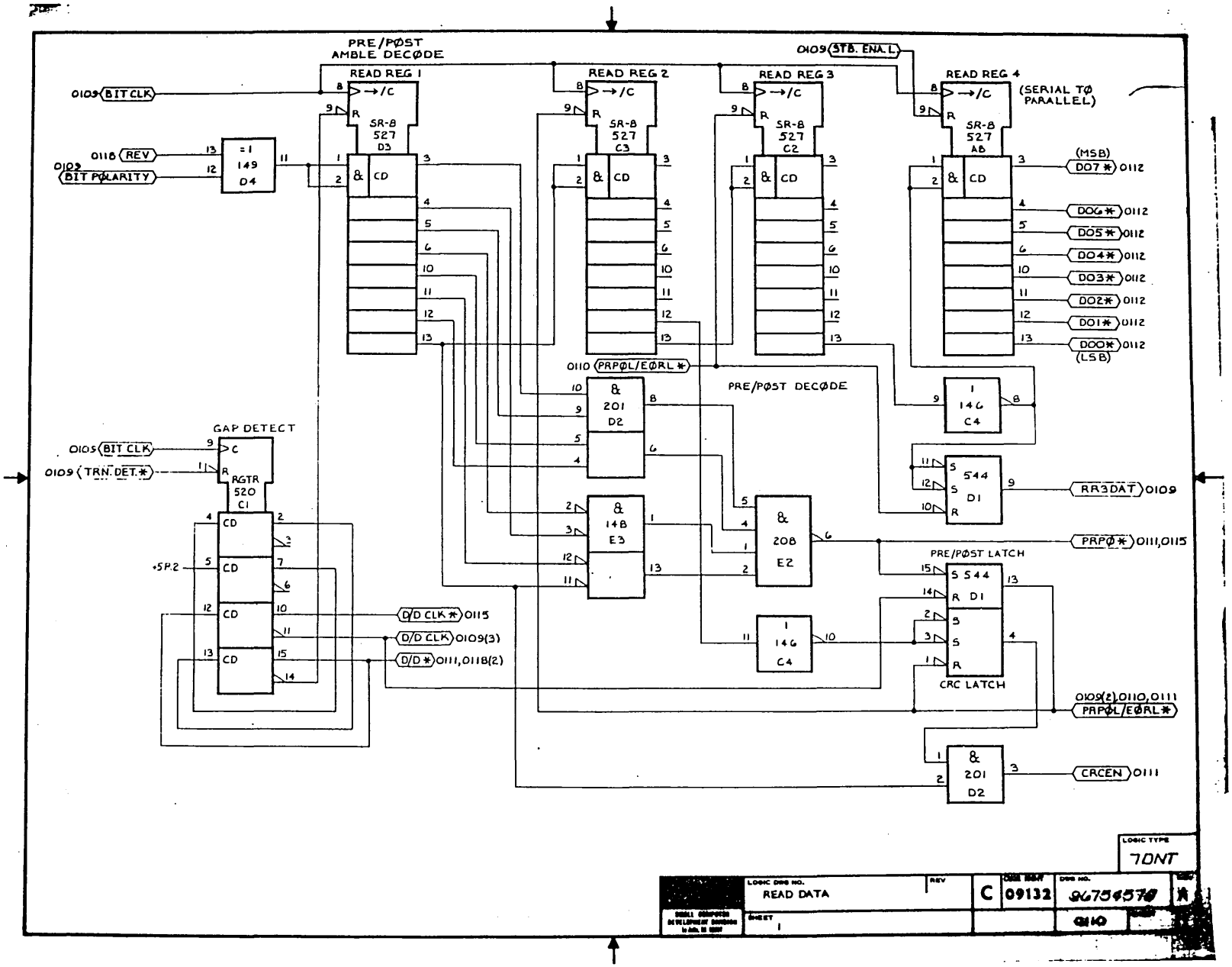


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 11 of 22)

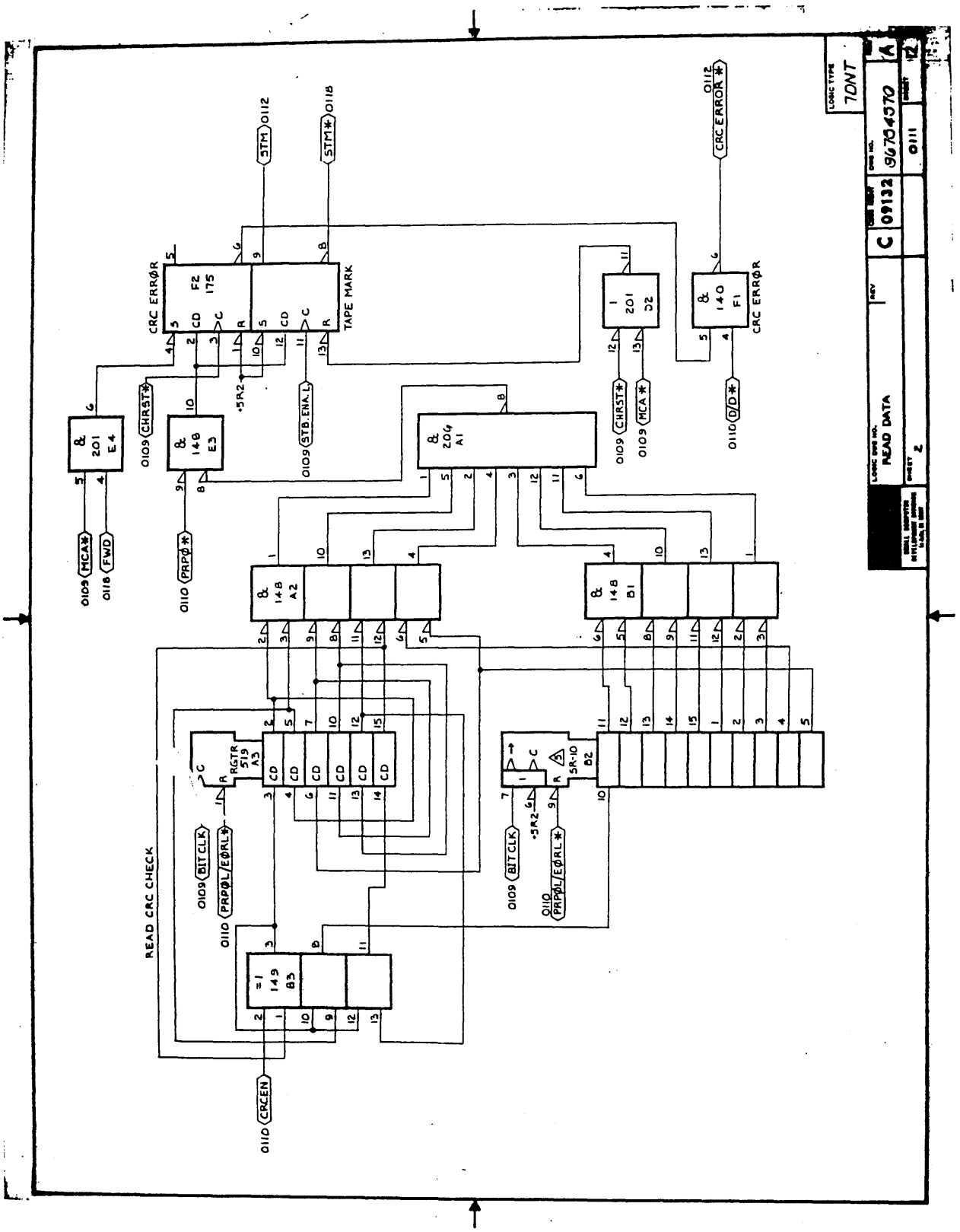


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 12 of 22)

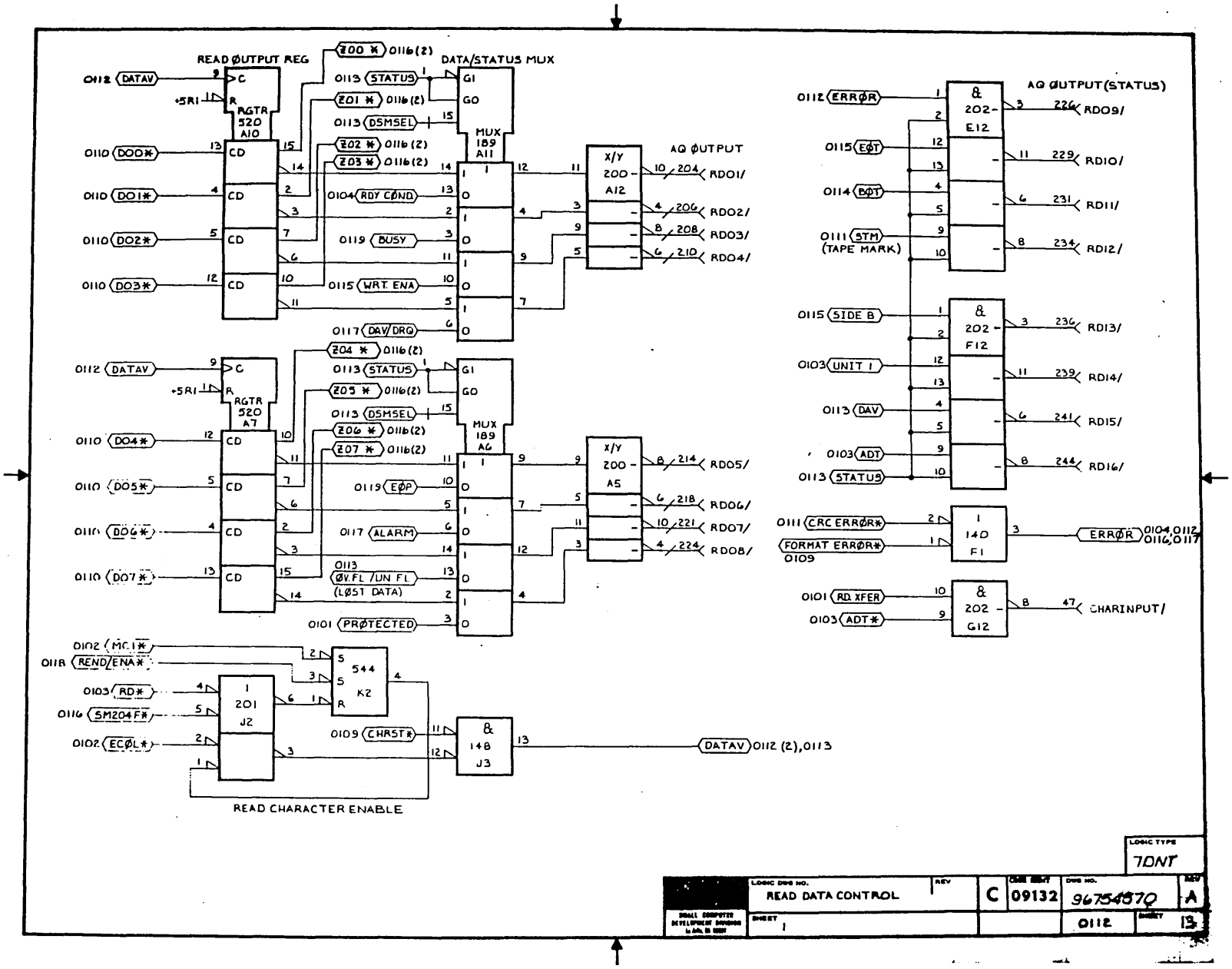


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 13 of 22)

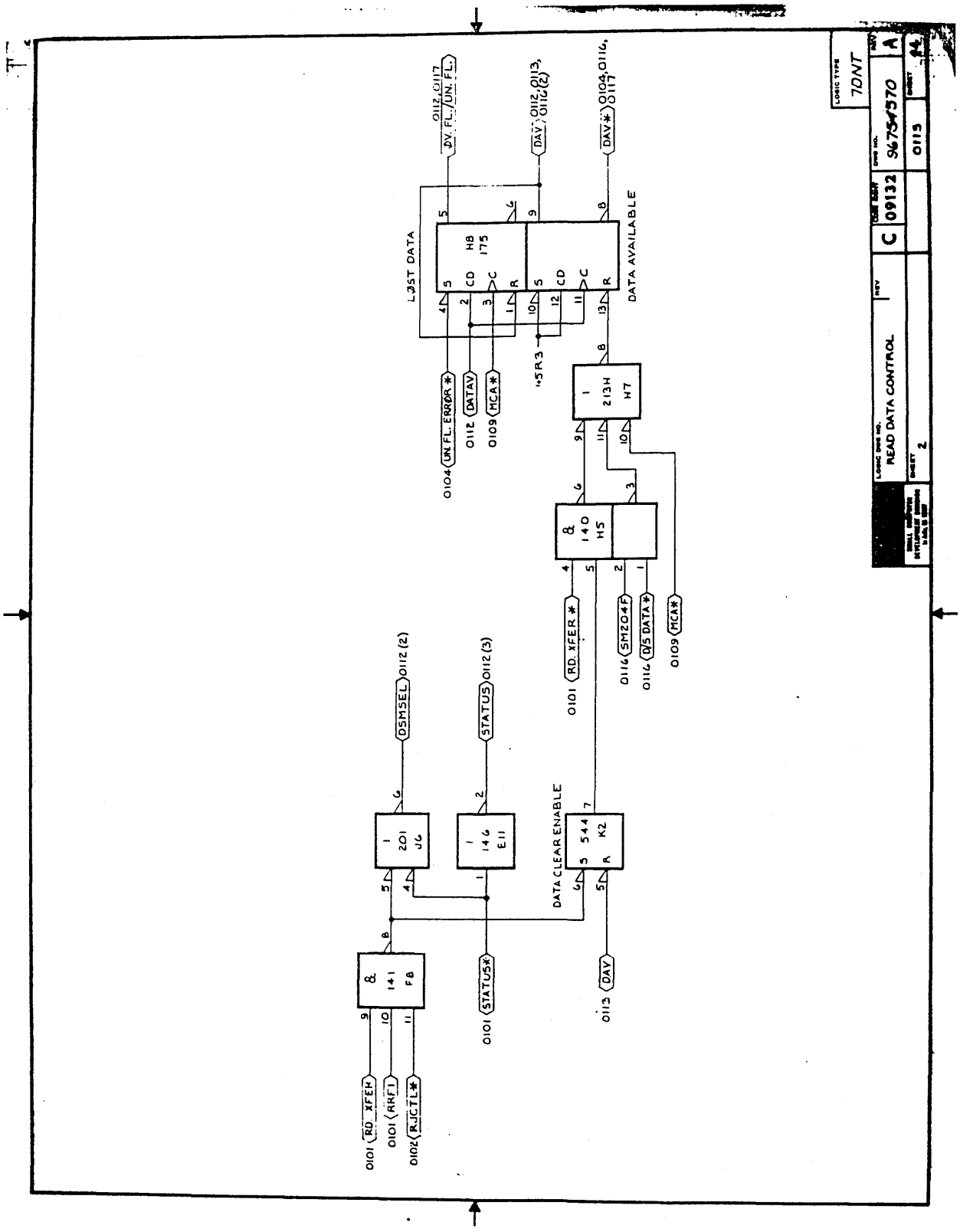


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 14 of 22)

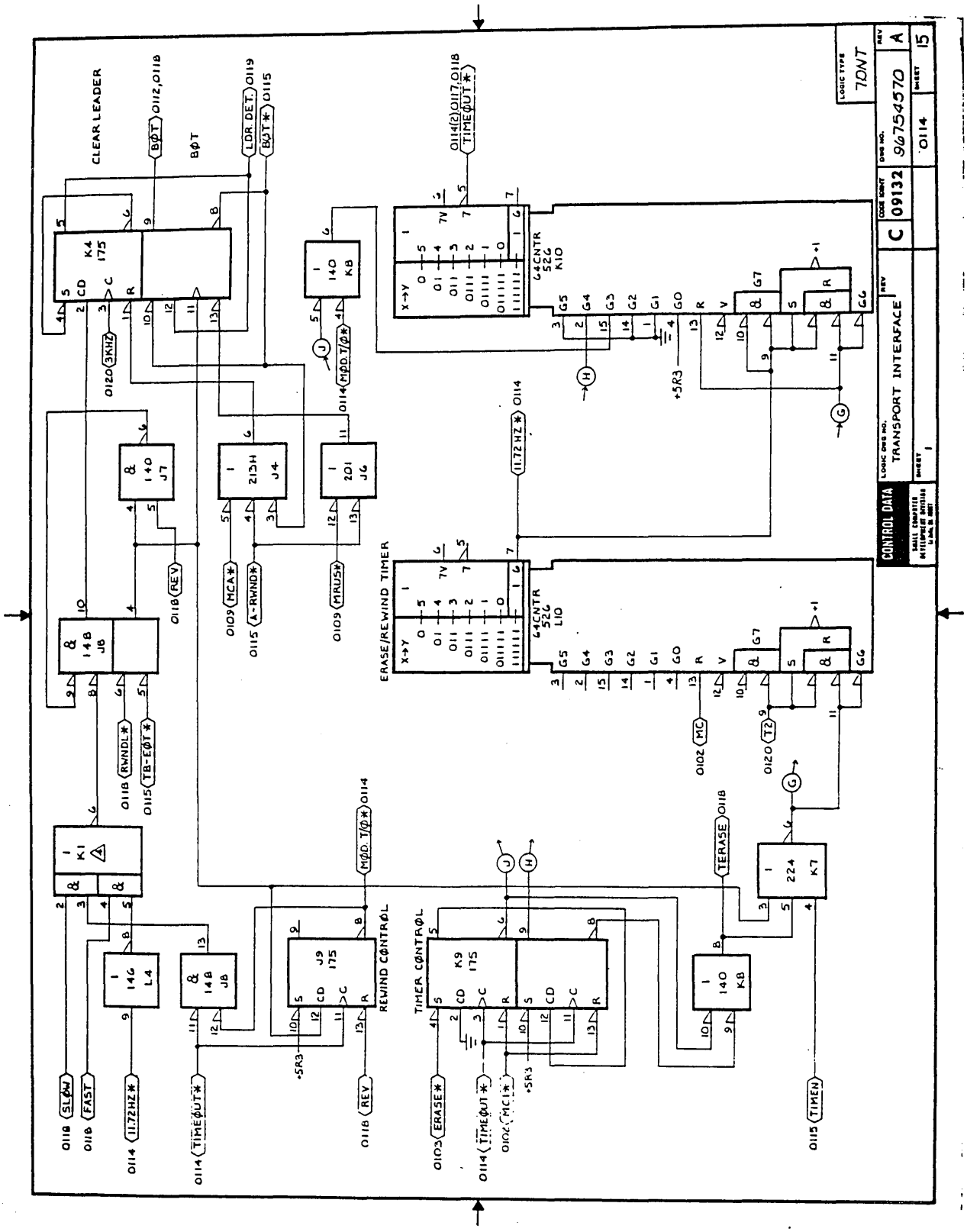


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 15 of 22)

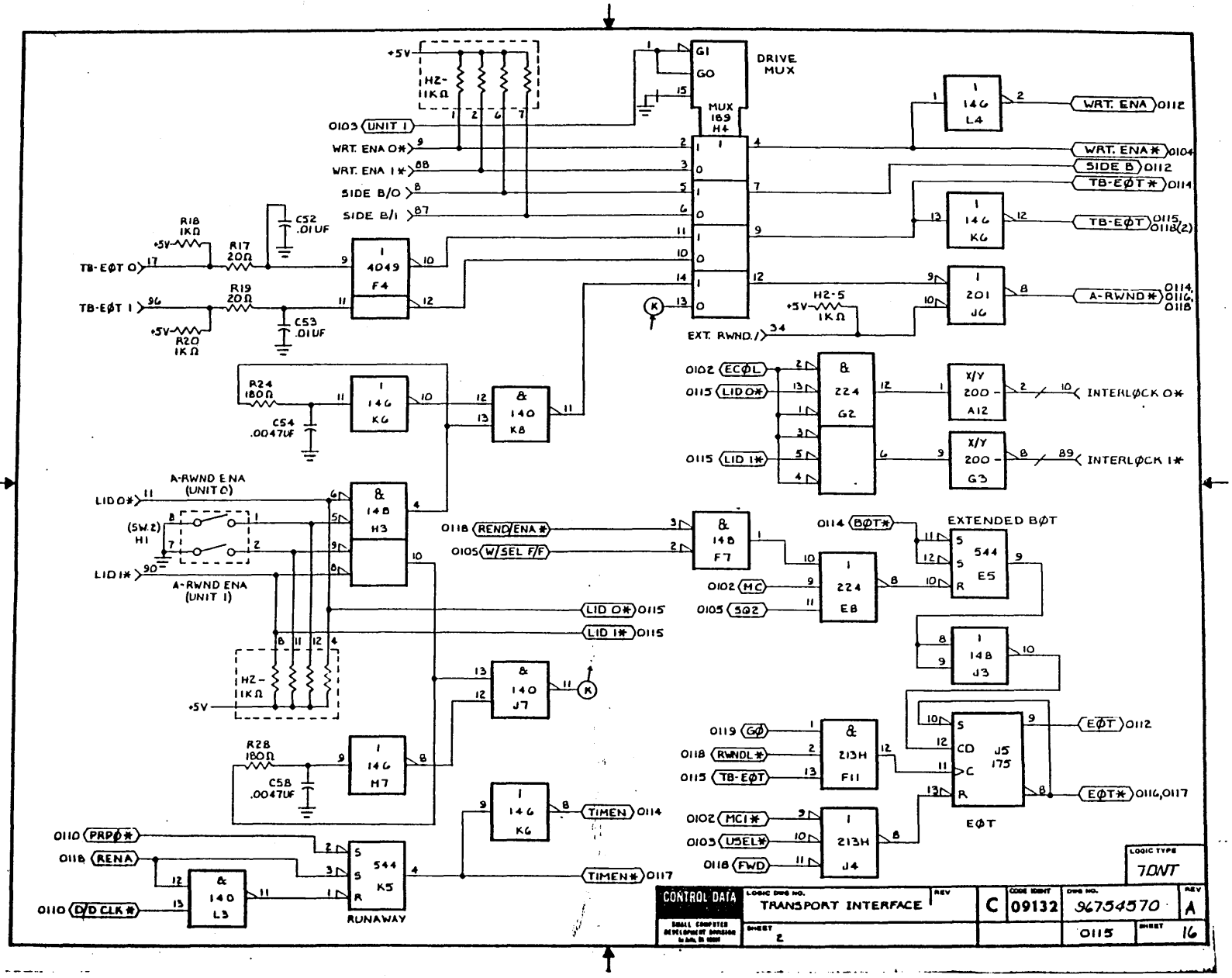


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 16 of 22)

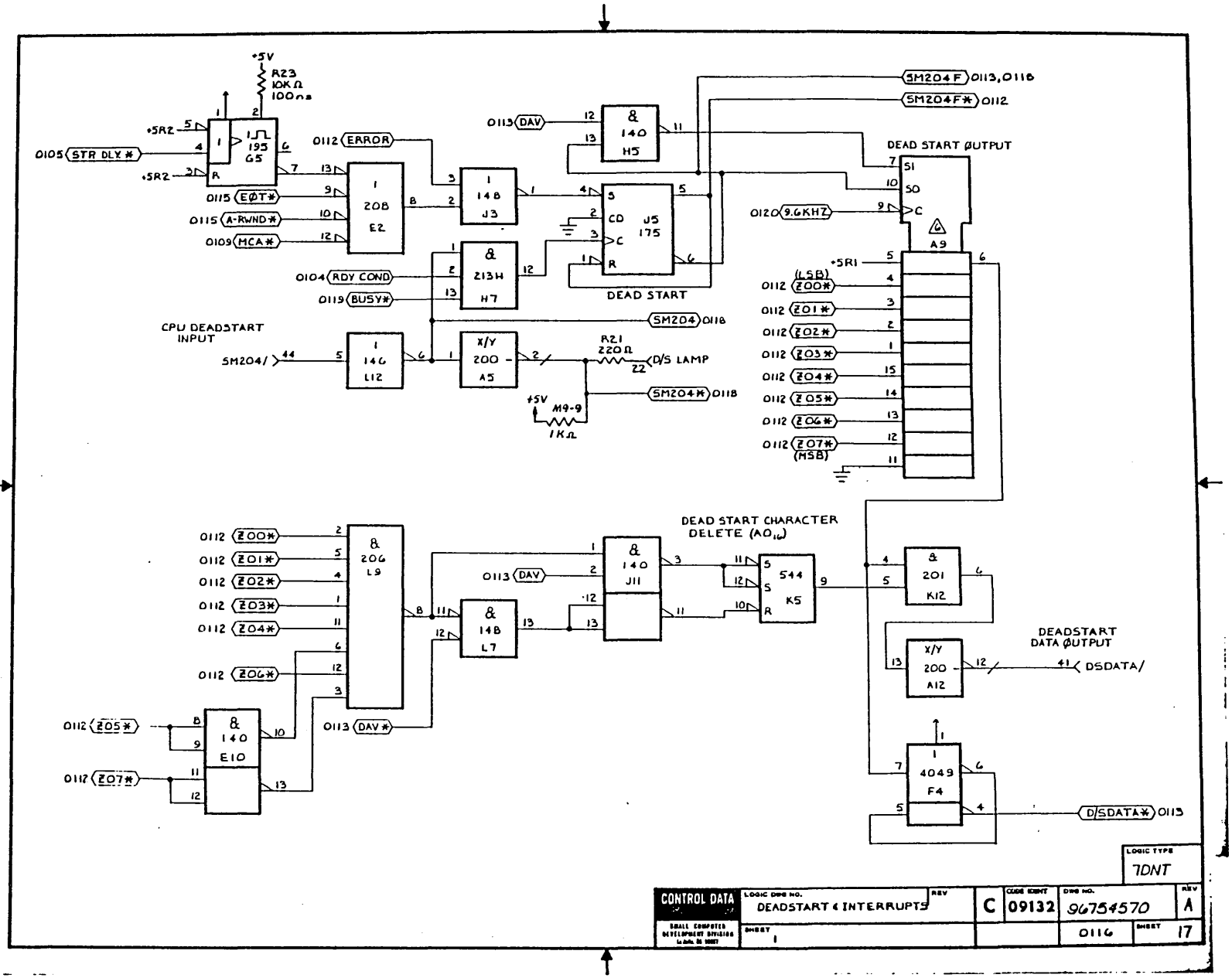


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 17 of 22)

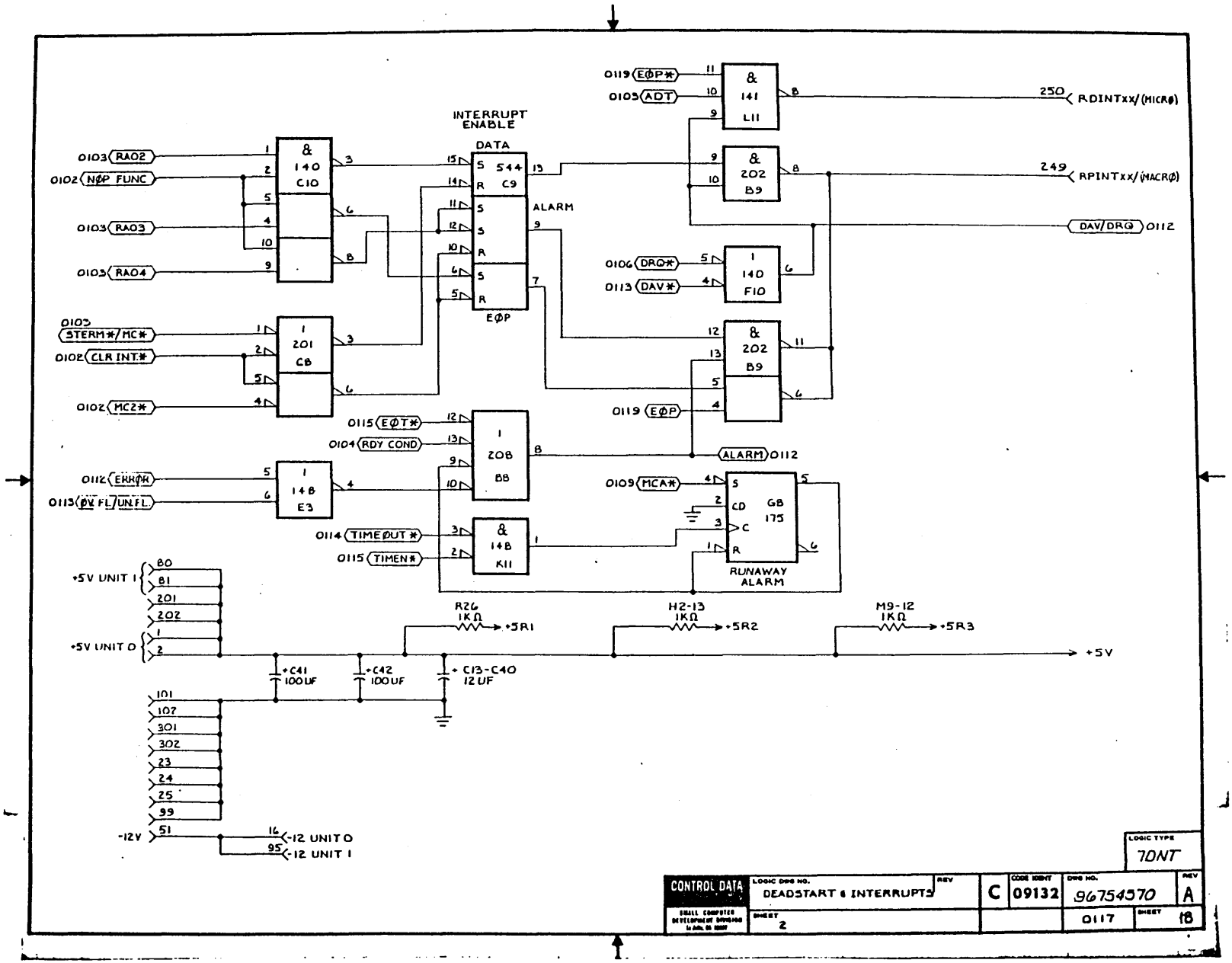


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 18 of 22)

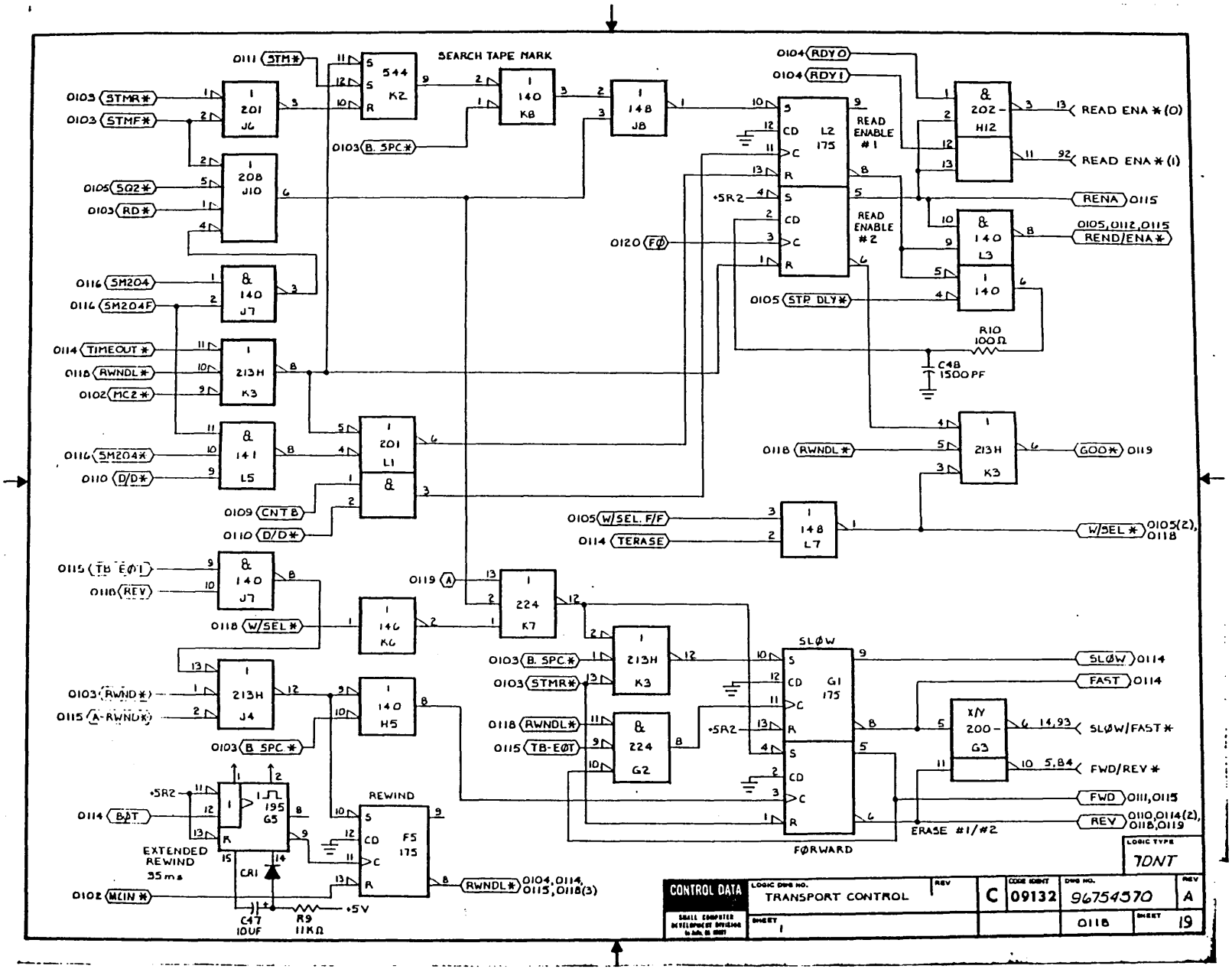


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 19 of 22)

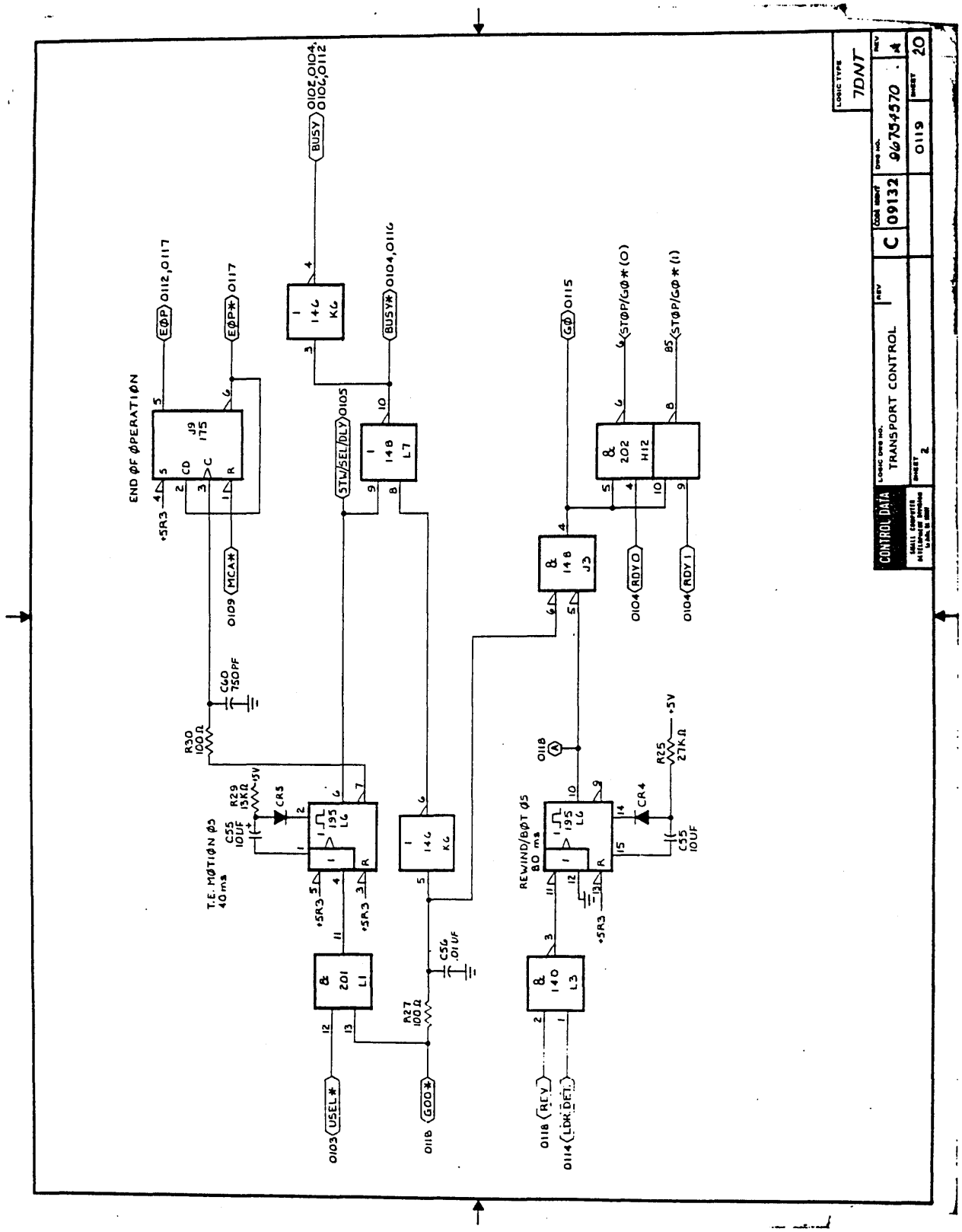


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 20 of 22)

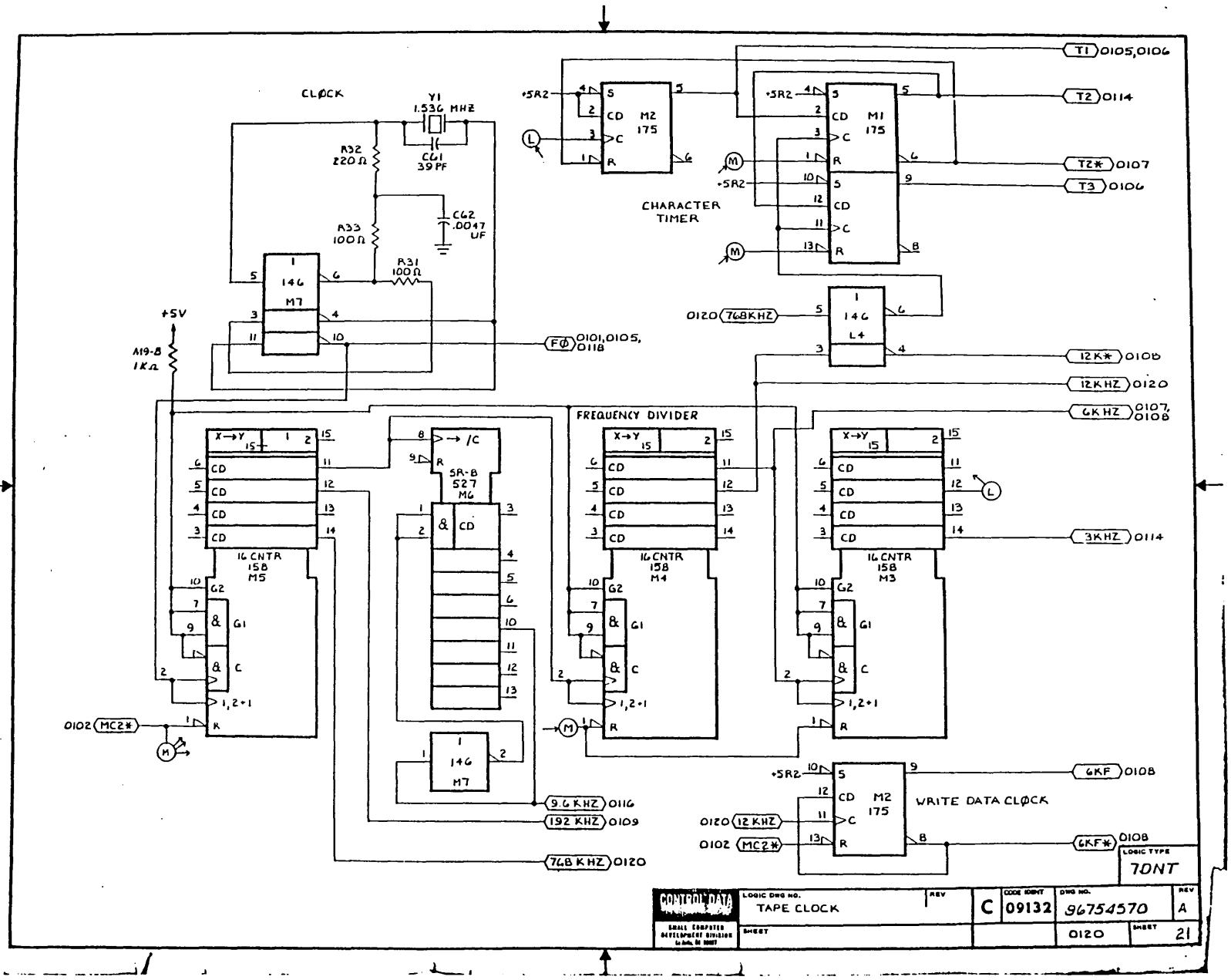


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 21 of 22)

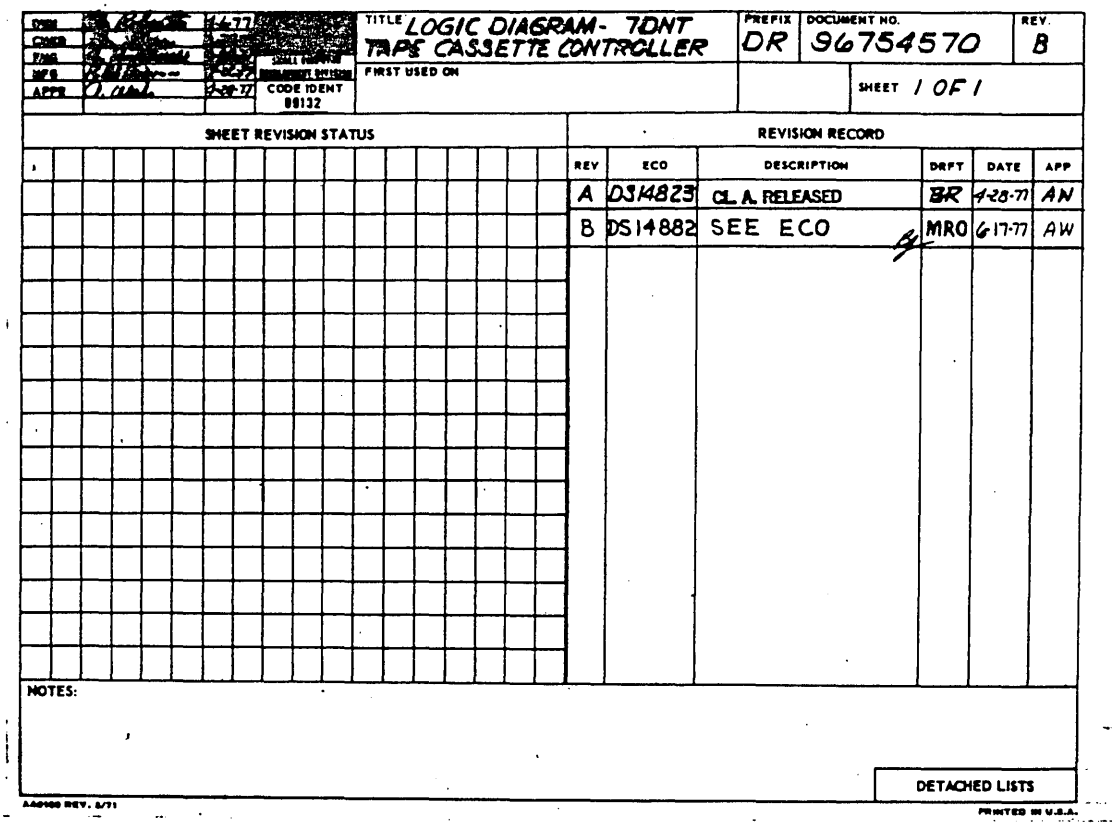
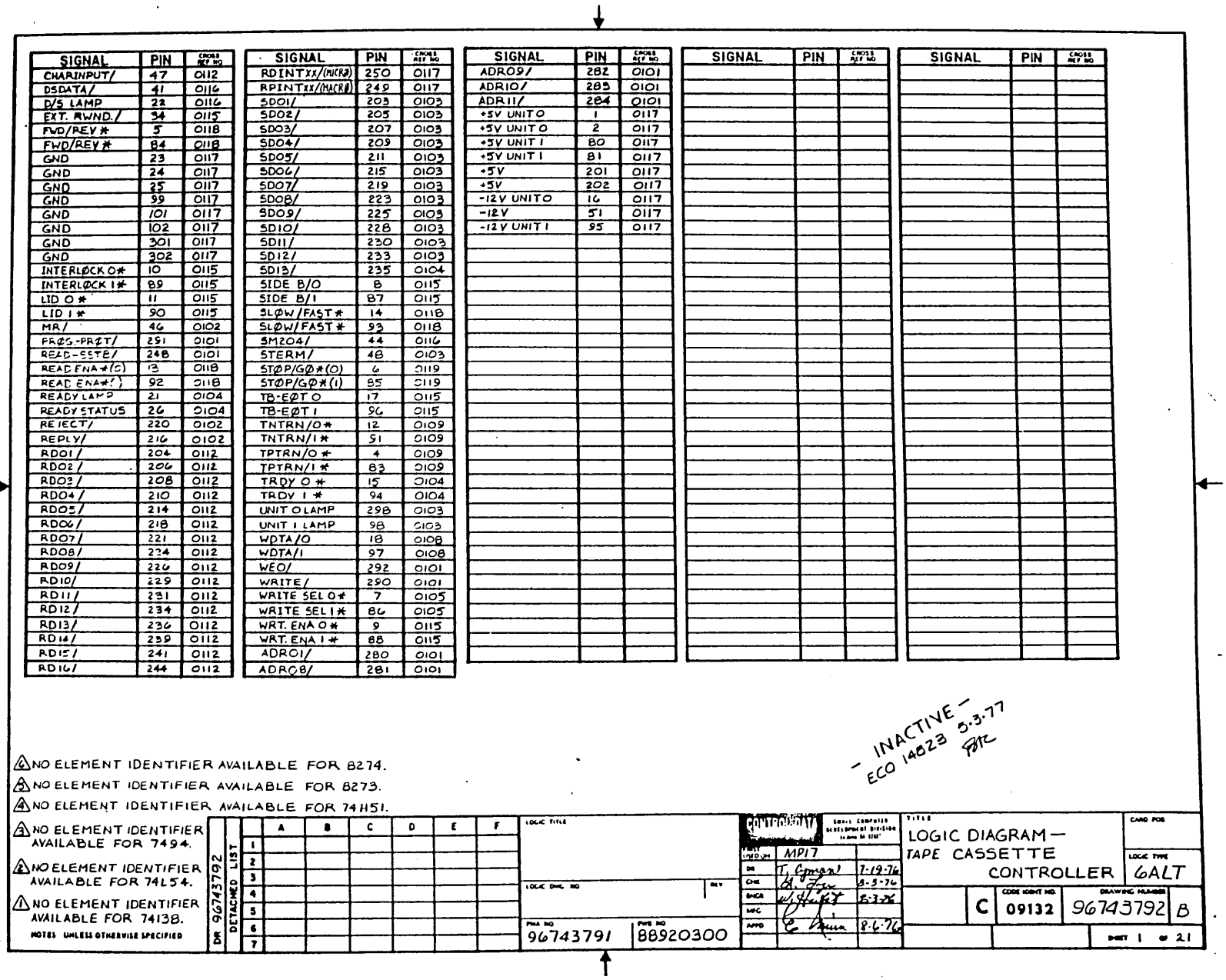


Figure 5-1. Tape Cassette Controller (PWA 96754569) Logic Diagram (Sheet 22 of 22)



SIGNAL	PIN	CROSS REF NO
CHARINPUT/	47	0112
DSDATA/	41	0116
D/S LAMP	22	0116
EXT. RWND./	34	0115
FWD/REV *	5	0118
FWD/REV *	84	0118
GND	23	0117
GND	24	0117
GND	25	0117
GND	99	0117
GND	101	0117
GND	102	0117
GND	301	0117
GND	302	0117
INTERLOCK 0*	10	0115
INTERLOCK 1*	89	0115
LID 0 *	11	0115
LID 1 *	90	0115
MR/	46	0102
PROG-PROT/	251	0101
READ-STB/	248	0101
READ ENA*(0)	13	0118
READ ENA*(1)	92	0118
READY LAMP	21	0104
READY STATUS	26	0104
REJECT/	220	0102
REPLY/	216	0102
RDO1/	204	0112
RDO2/	206	0112
RDO3/	208	0112
RDO4/	210	0112
RDO5/	214	0112
RDO6/	218	0112
RDO7/	221	0112
RDO8/	224	0112
RDO9/	226	0112
RD10/	229	0112
RD11/	231	0112
RD12/	234	0112
RD13/	236	0112
RD14/	239	0112
RD15/	241	0112
RD16/	244	0112

SIGNAL	PIN	CROSS REF NO
RDINTXX/(MICRO)	250	0117
RPINTXX/(MACRO)	249	0117
SDO1/	203	0103
SDO2/	205	0103
SDO3/	207	0103
SDO4/	209	0103
SDO5/	211	0103
SDO6/	215	0103
SDO7/	219	0103
SDO8/	223	0103
SDO9/	225	0103
SDI0/	228	0103
SDI1/	230	0103
SDI2/	233	0103
SDI3/	235	0104
SIDE B/0	8	0115
SIDE B/1	87	0115
SLOW/FAST *	14	0118
SLOW/FAST *	93	0118
SM204/	44	0116
STERM/	48	0103
STOP/GO*(0)	6	0119
STOP/GO*(1)	85	0119
TB-EOT 0	17	0115
TB-EOT 1	96	0115
TNTRN/0*	12	0109
TNTRN/1*	51	0109
TPTRN/0 *	4	0109
TPTRN/1 *	83	0109
TRDY 0 *	15	0104
TRDY 1 *	94	0104
UNIT 0 LAMP	298	0103
UNIT 1 LAMP	98	0103
WDTA/0	18	0108
WDTA/1	97	0108
WEO/	292	0101
WRITE/	290	0101
WRITE SEL 0*	7	0105
WRITE SEL 1*	86	0105
WRT. ENA 0 *	9	0115
WRT. ENA 1 *	88	0115
ADRO1/	280	0101
ADRO8/	281	0101

SIGNAL	PIN	CROSS REF NO
ADRO9/	282	0101
ADR10/	285	0101
ADR11/	284	0101
+5V UNIT 0	1	0117
+5V UNIT 0	2	0117
+5V UNIT 1	80	0117
+5V UNIT 1	81	0117
+5V	201	0117
+5V	202	0117
-12V UNIT 0	16	0117
-12V	51	0117
-12V UNIT 1	95	0117

SIGNAL	PIN	CROSS REF NO

SIGNAL	PIN	CROSS REF NO

- INACTIVE - ECO 14023 5.3.77

⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 8274.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 8273.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 74H51.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 7494.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 74L54.
⚠ NO ELEMENT IDENTIFIER AVAILABLE FOR 74138.
NOTES UNLESS OTHERWISE SPECIFIED

DR 96743792 DETACHED LIST

	A	B	C	D	E	F
1						
2						
3						
4						
5						
6						
7						

LOGIC TITLE
LOGIC DWG NO | REV
PWA NO 96743791 | PWB NO 88920300

CONTROL DATA — SMALL COMPUTER DEVELOPMENT DIVISION

DRAWN	MP17	
DES	T. Gomez	7-19-76
CHK	A. Fox	8-3-76
ENGR	W. Hurley	8-3-76
MFG		
APPD	E. Davis	8-6-76

TITLE: LOGIC DIAGRAM — TAPE CASSETTE CONTROLLER
CARD POS
LOGIC TYPE 6ALT
C | CODE IDENT NO. 09132 | DRAWING NUMBER 96743792 | B
SHEET 1 OF 21

Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 1 of 21)

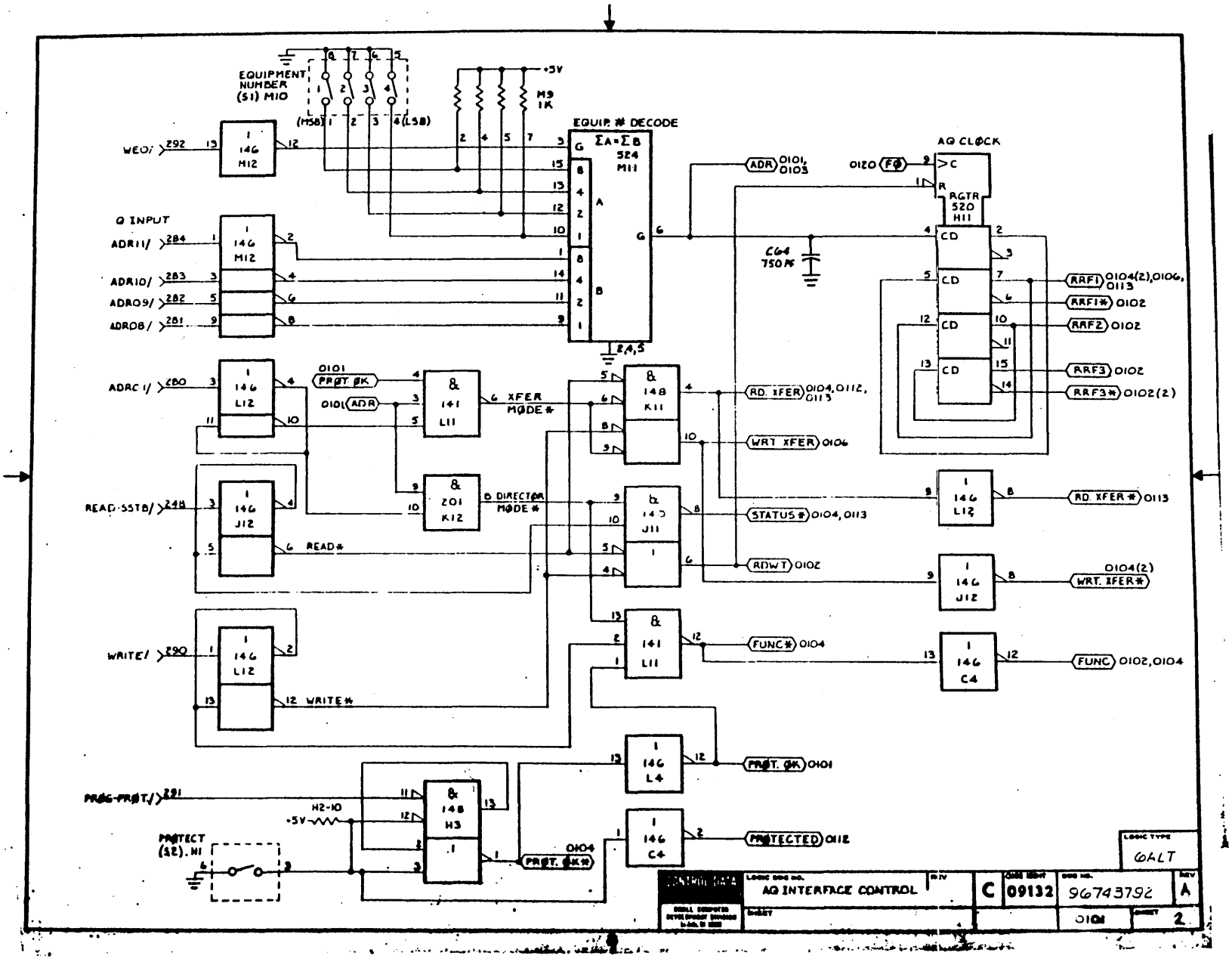


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 2 of 21)

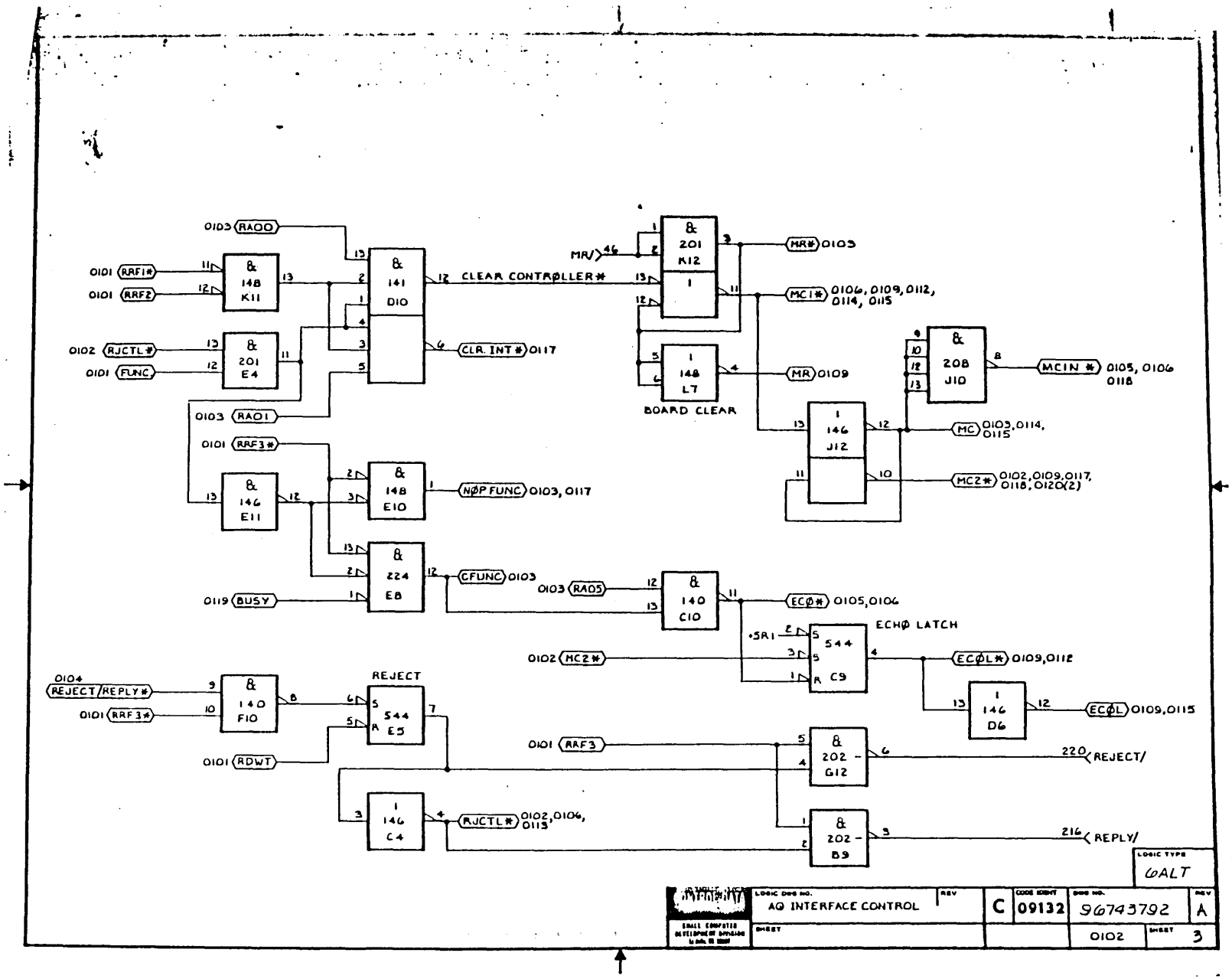


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 3 of 21)

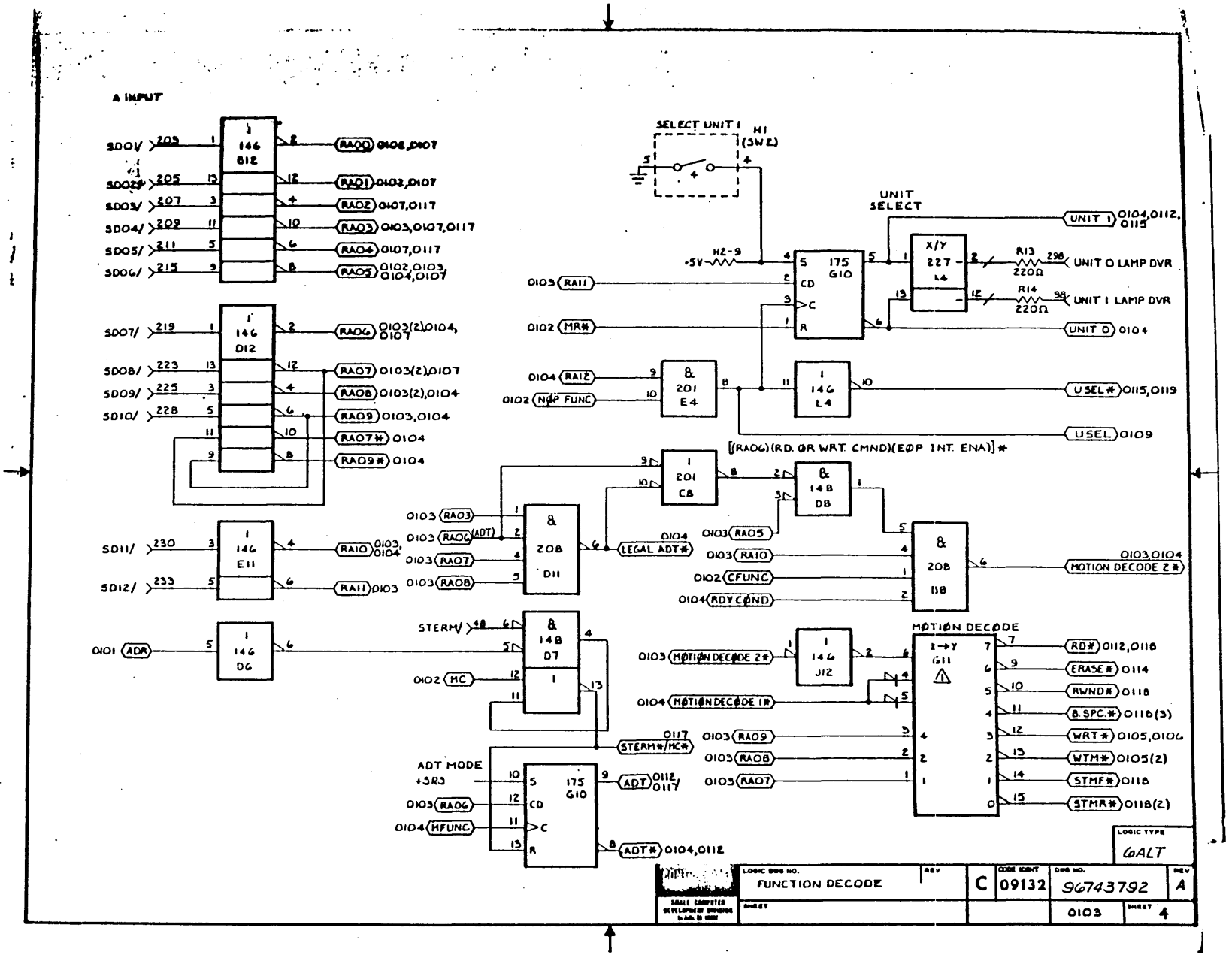


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 4 of 21)

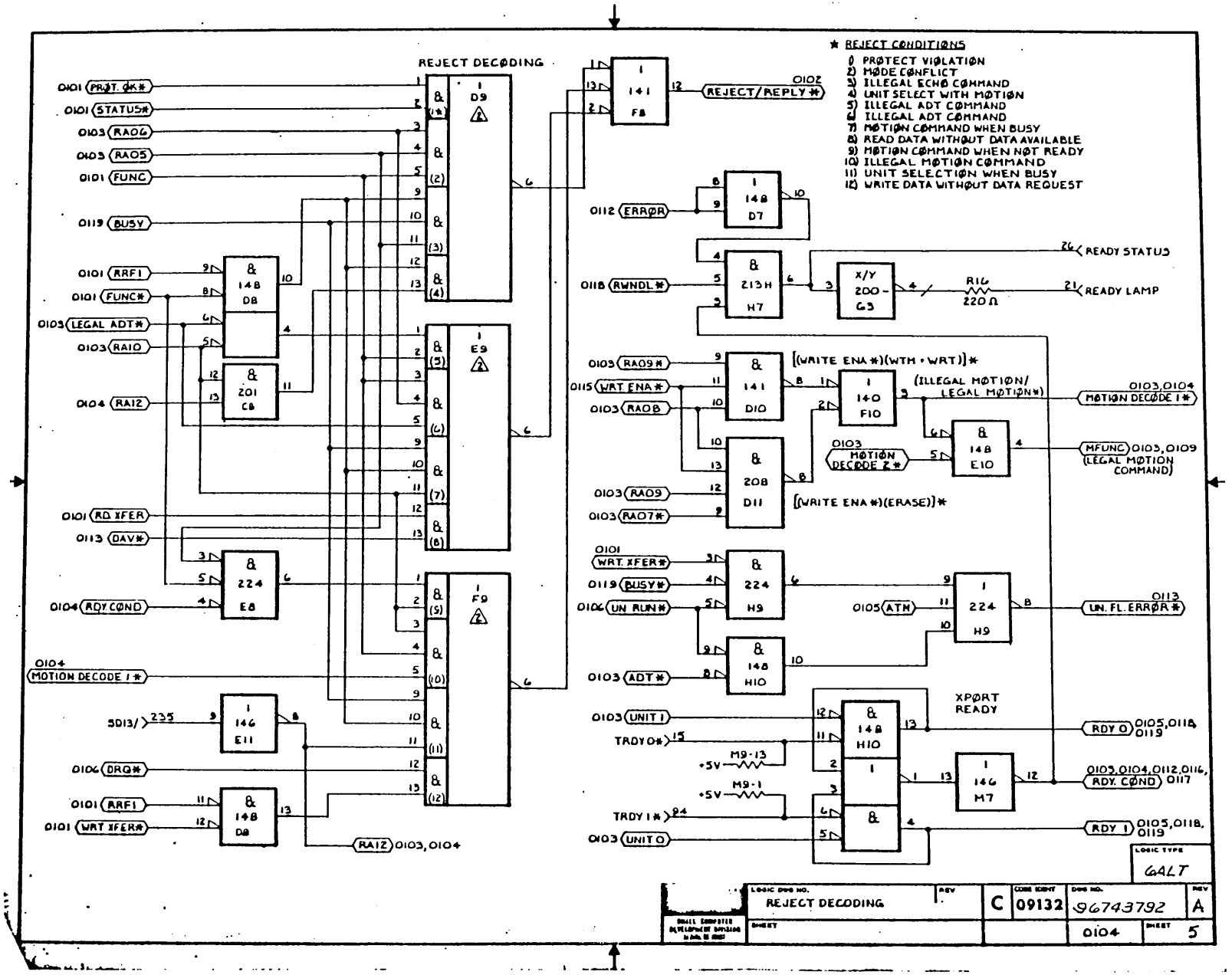


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 5 of 21)

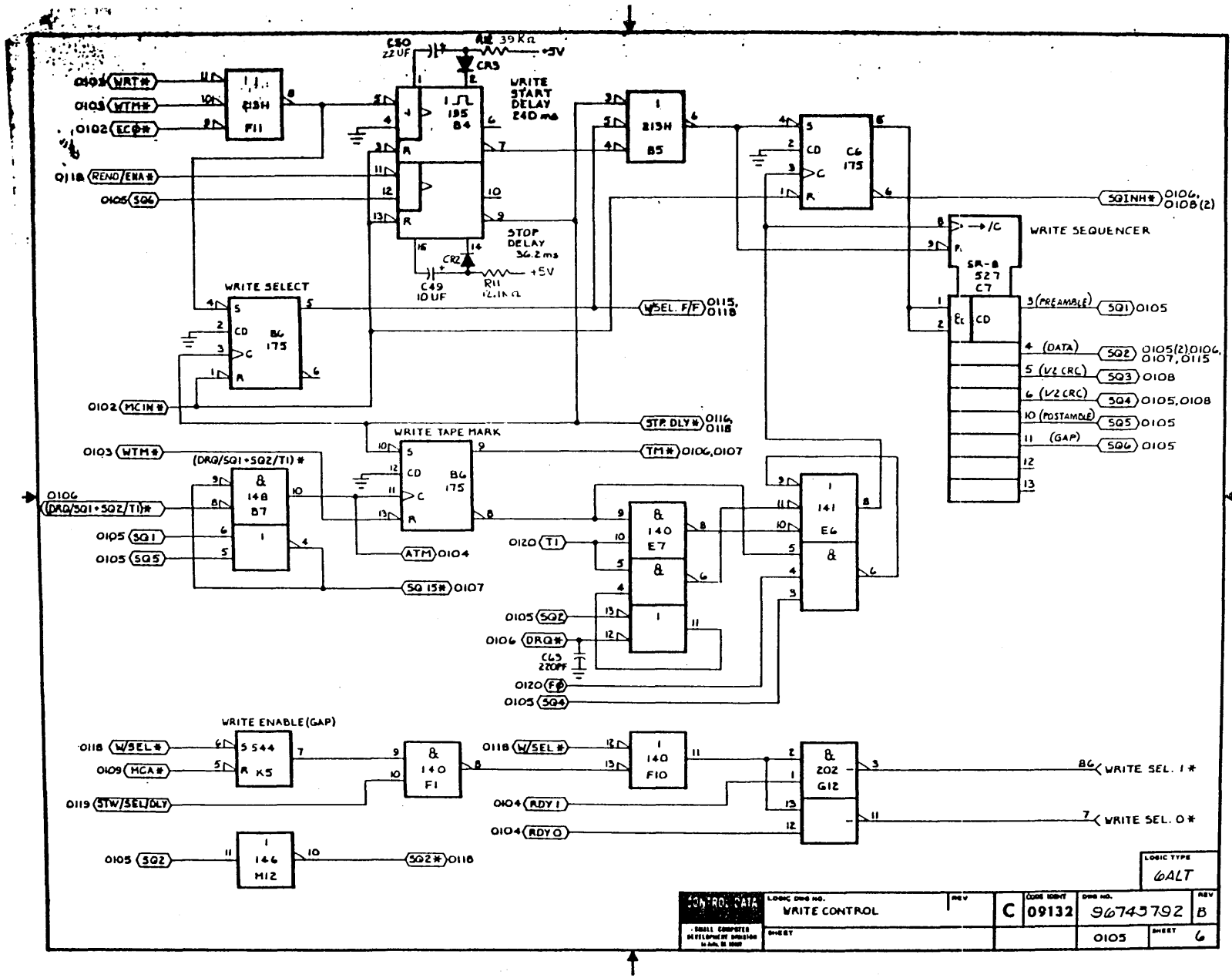


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 6 of 21)

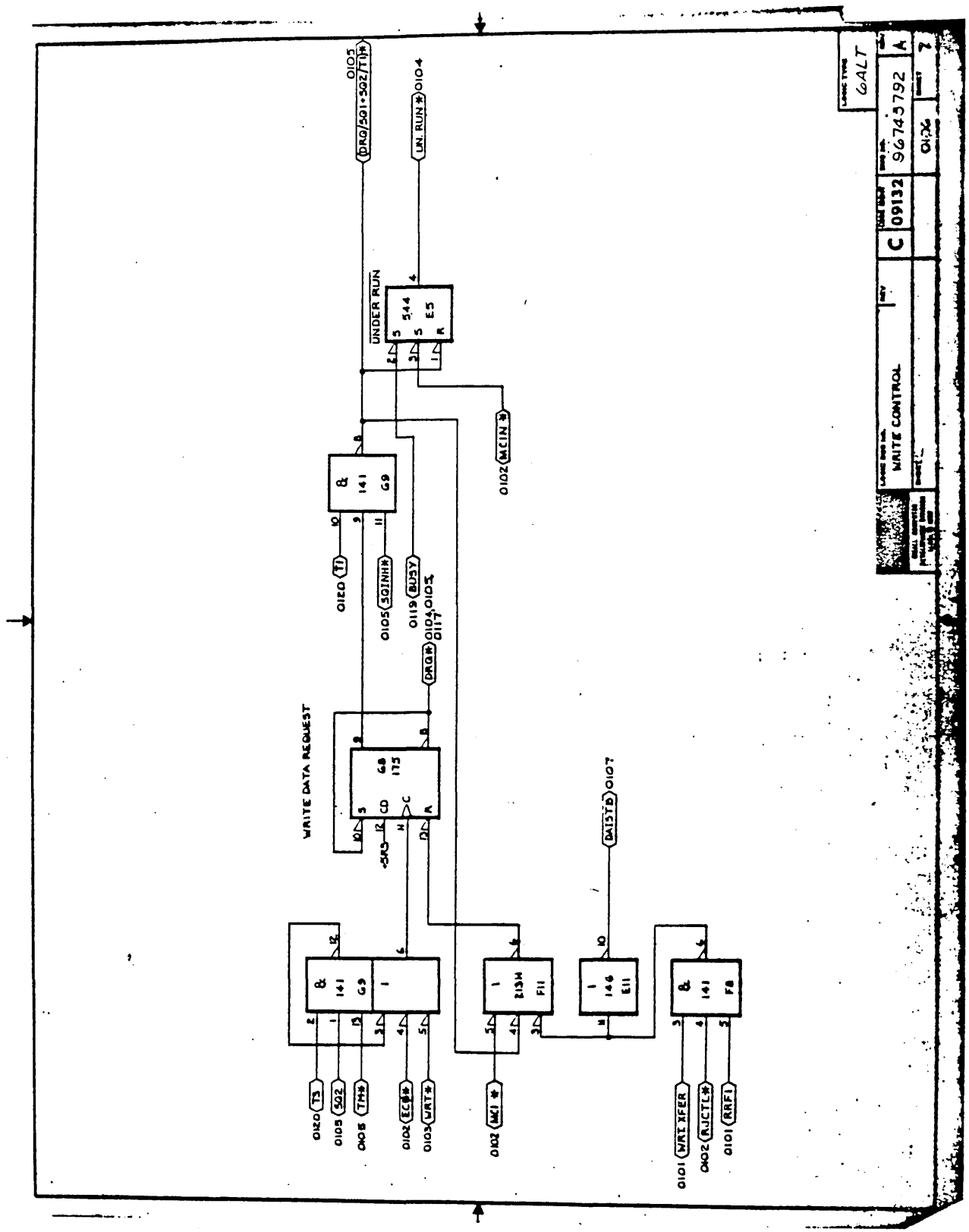


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 7 of 21)

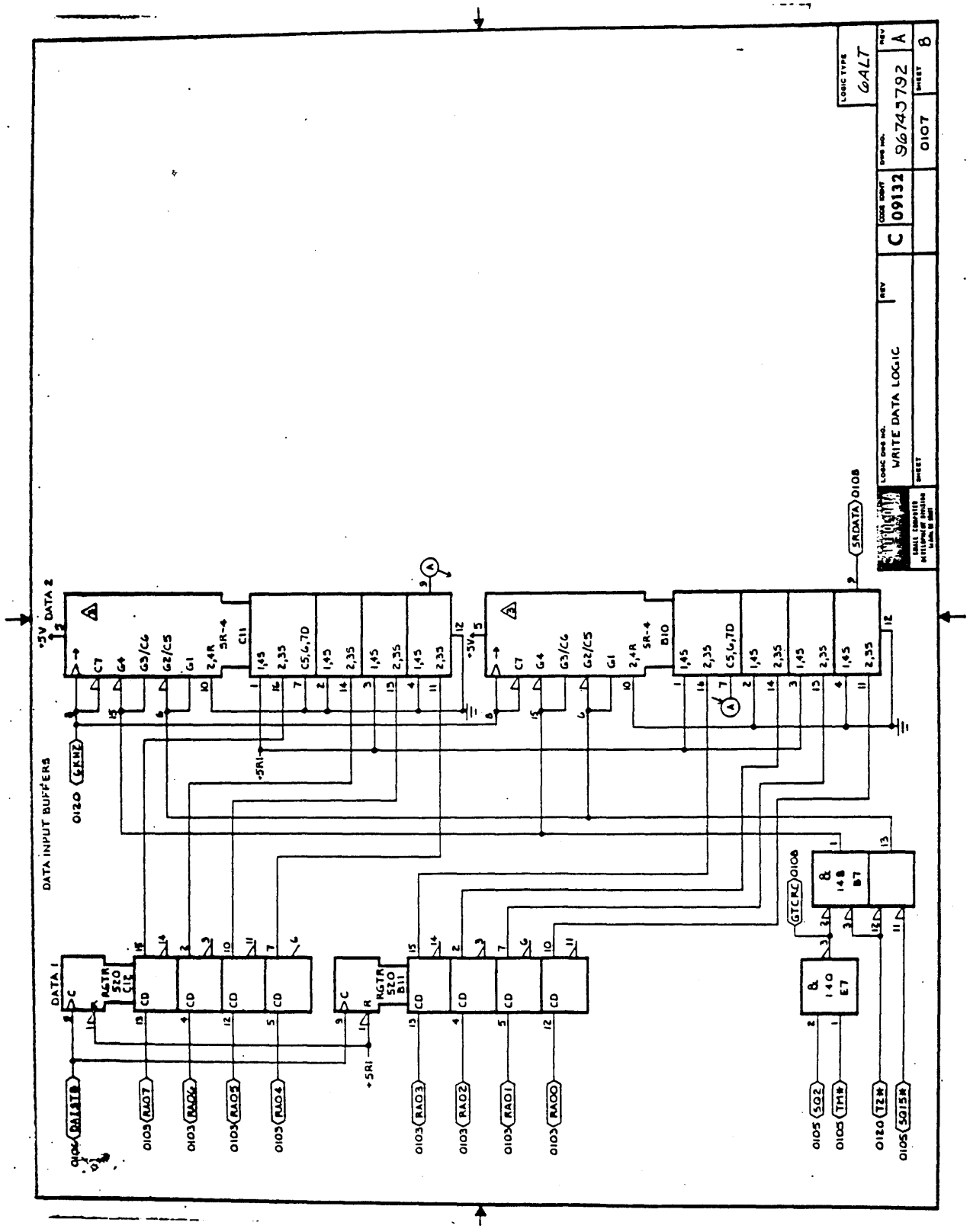


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 8 of 21)

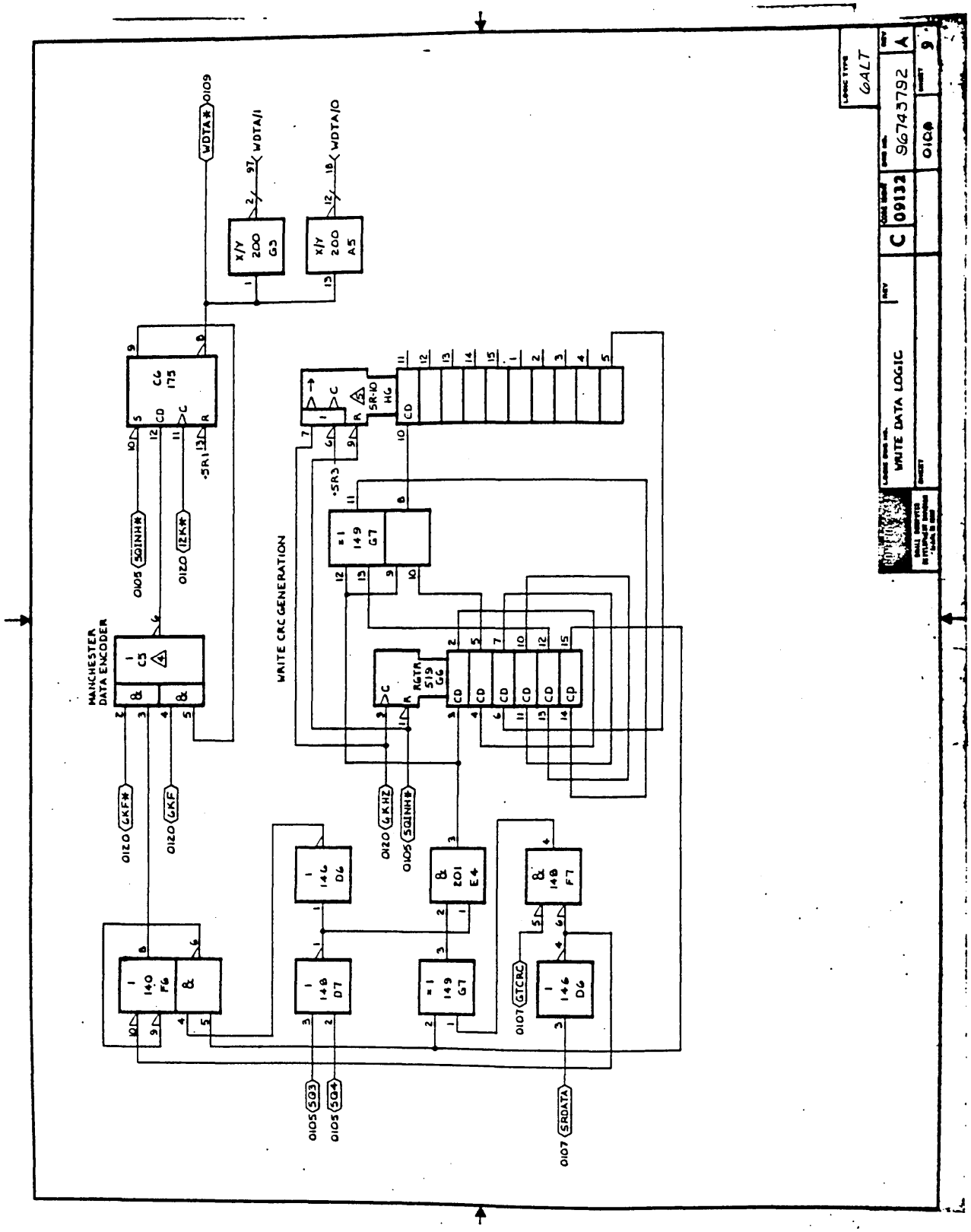


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 9 of 21)

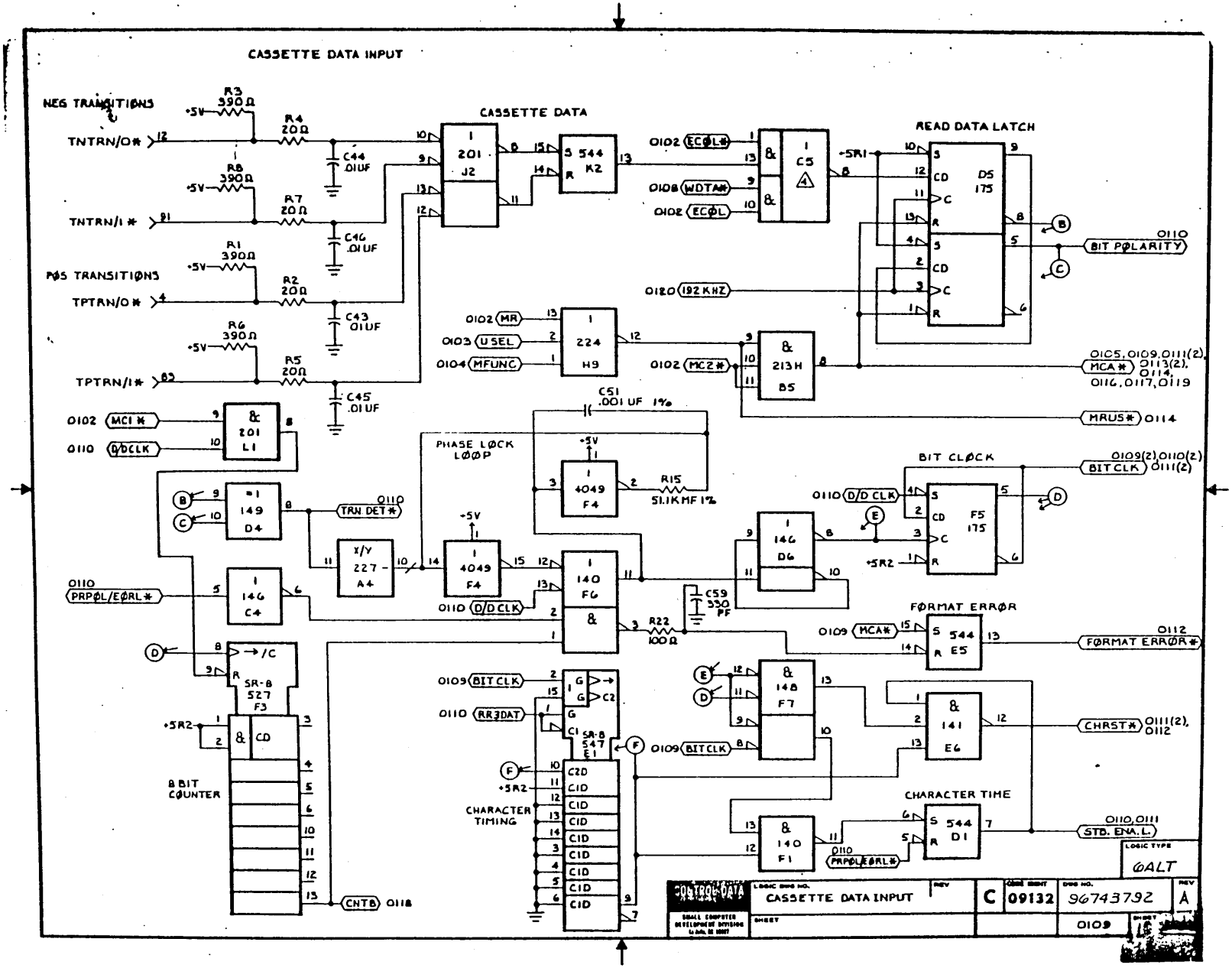


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 10 of 21)

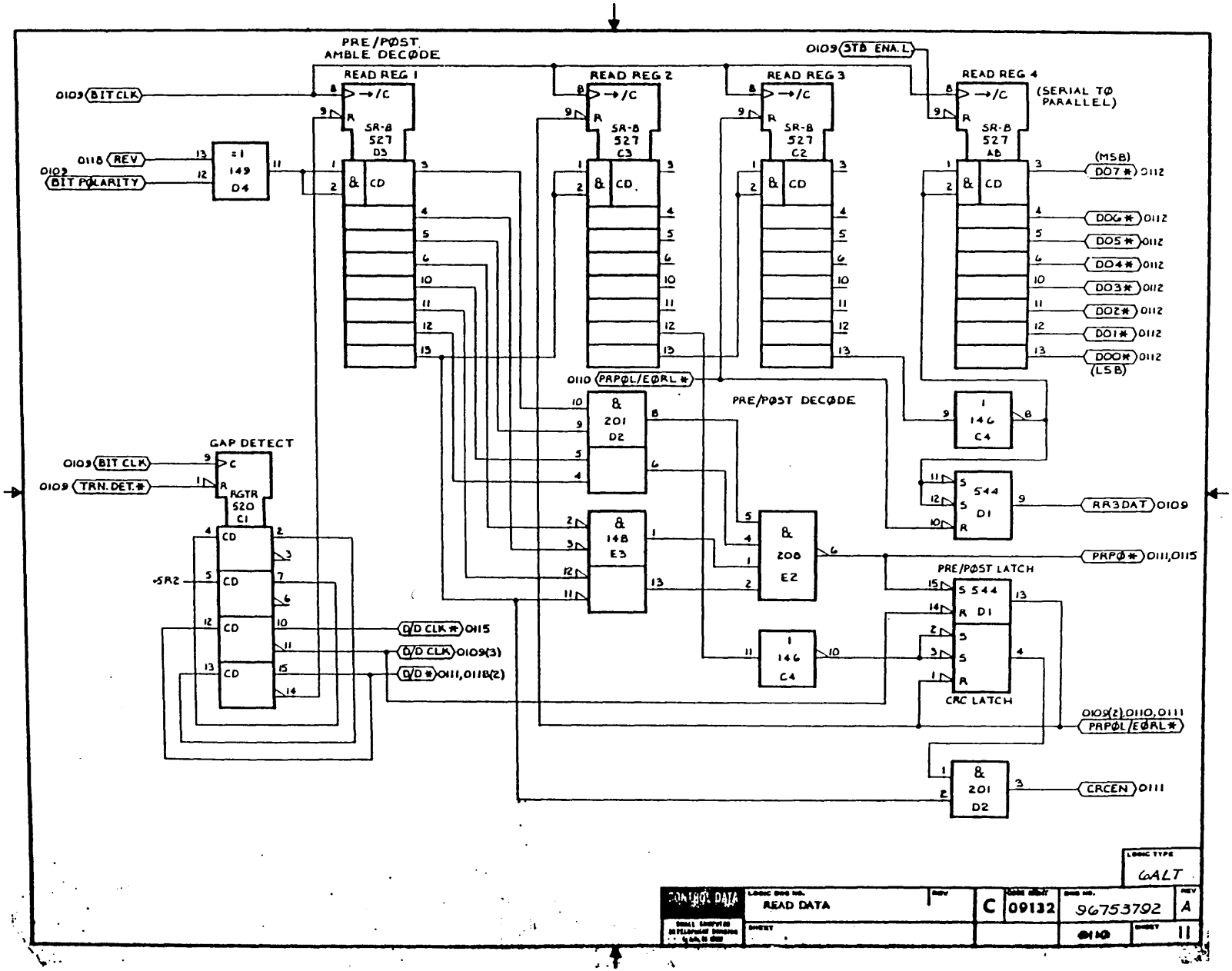


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 11 of 21)

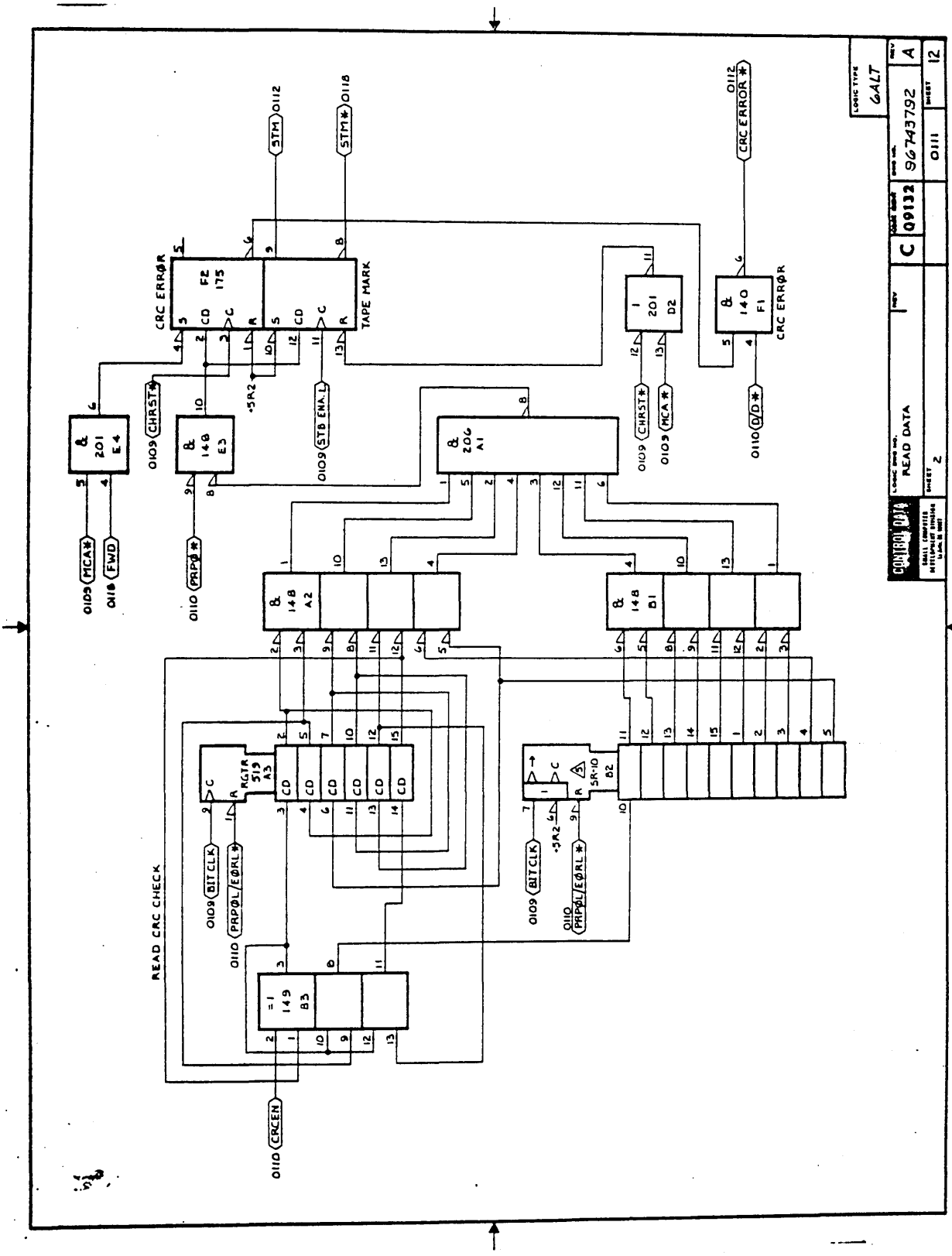


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 12 of 21)

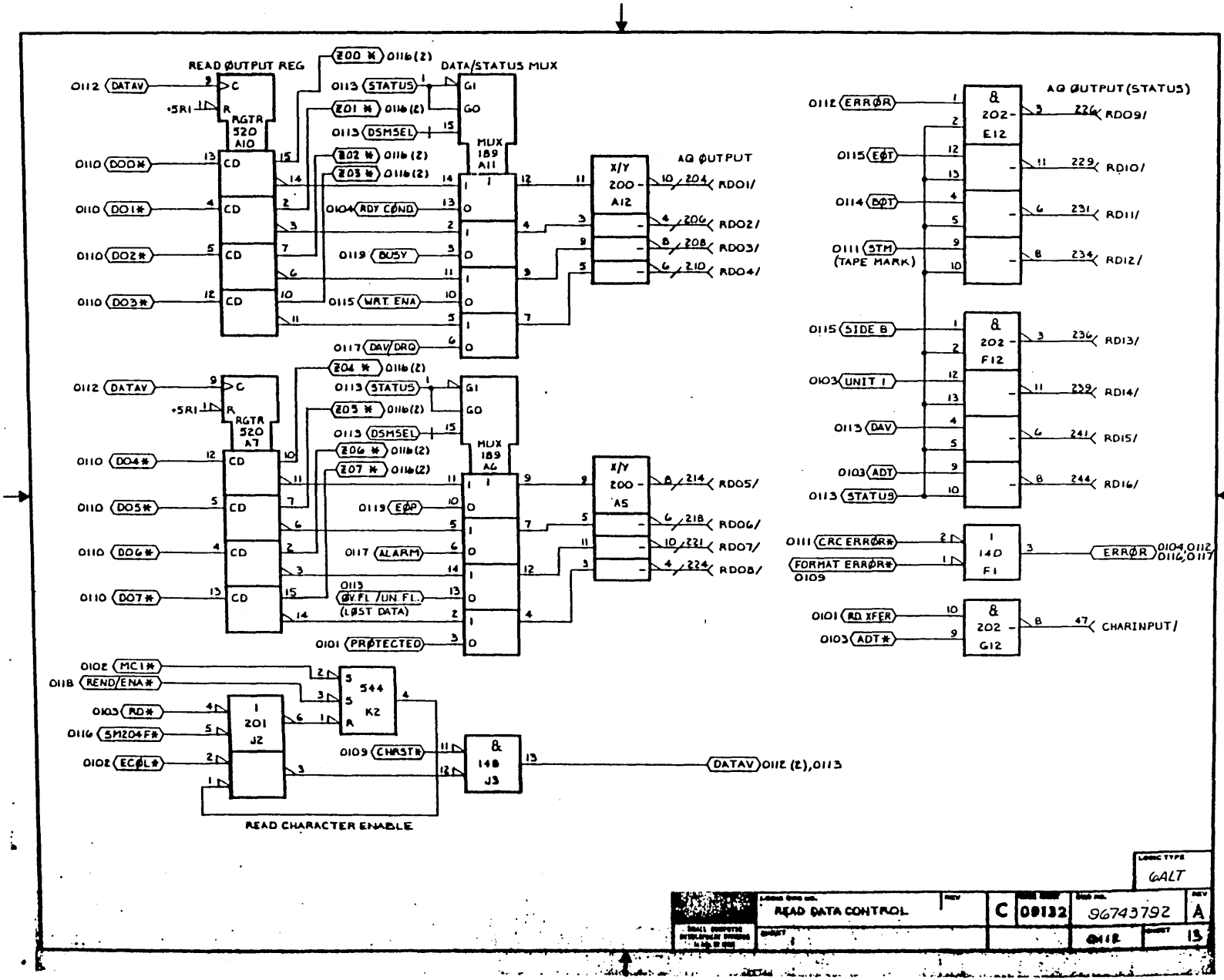


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 13 of 21)

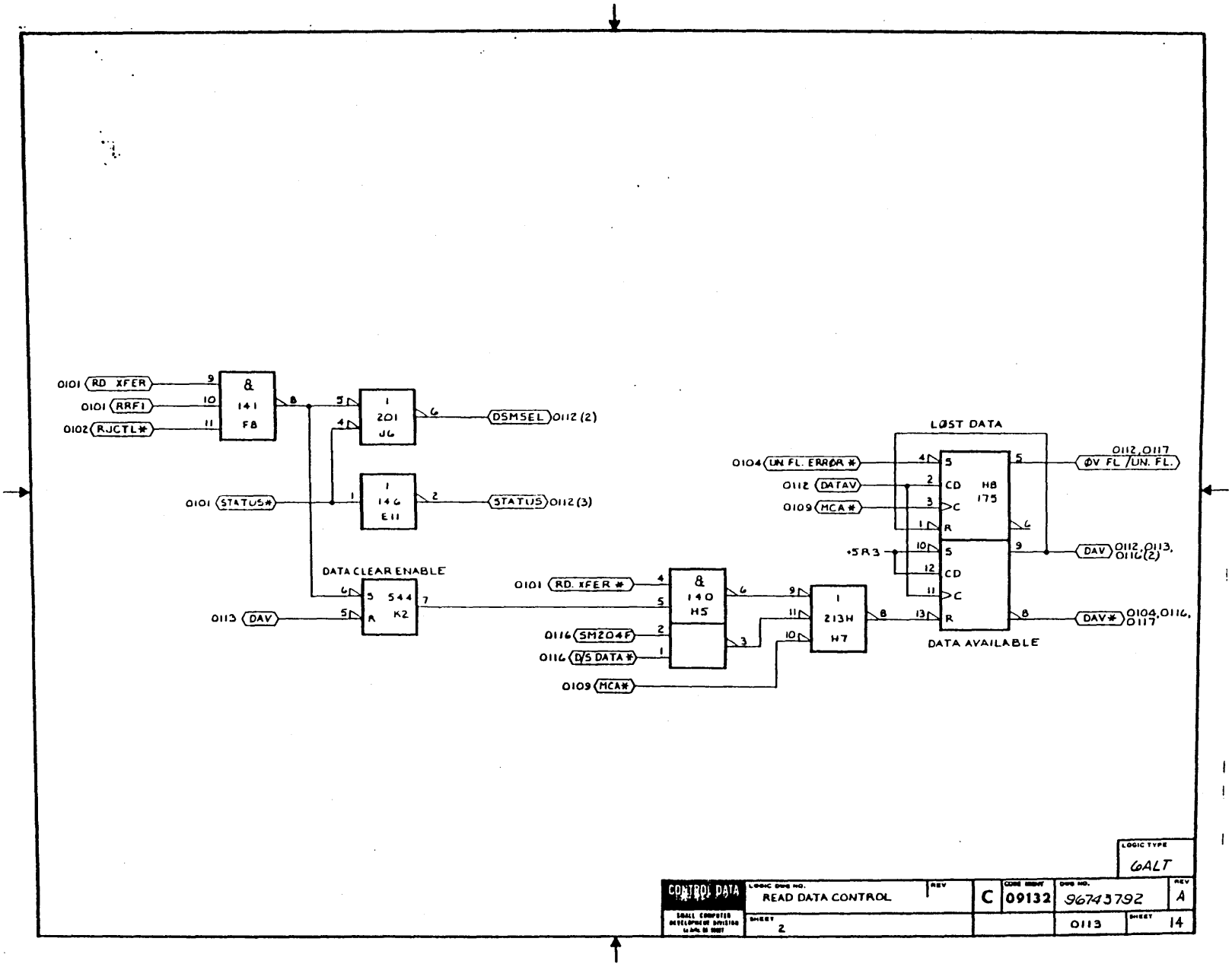


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 14 of 21)

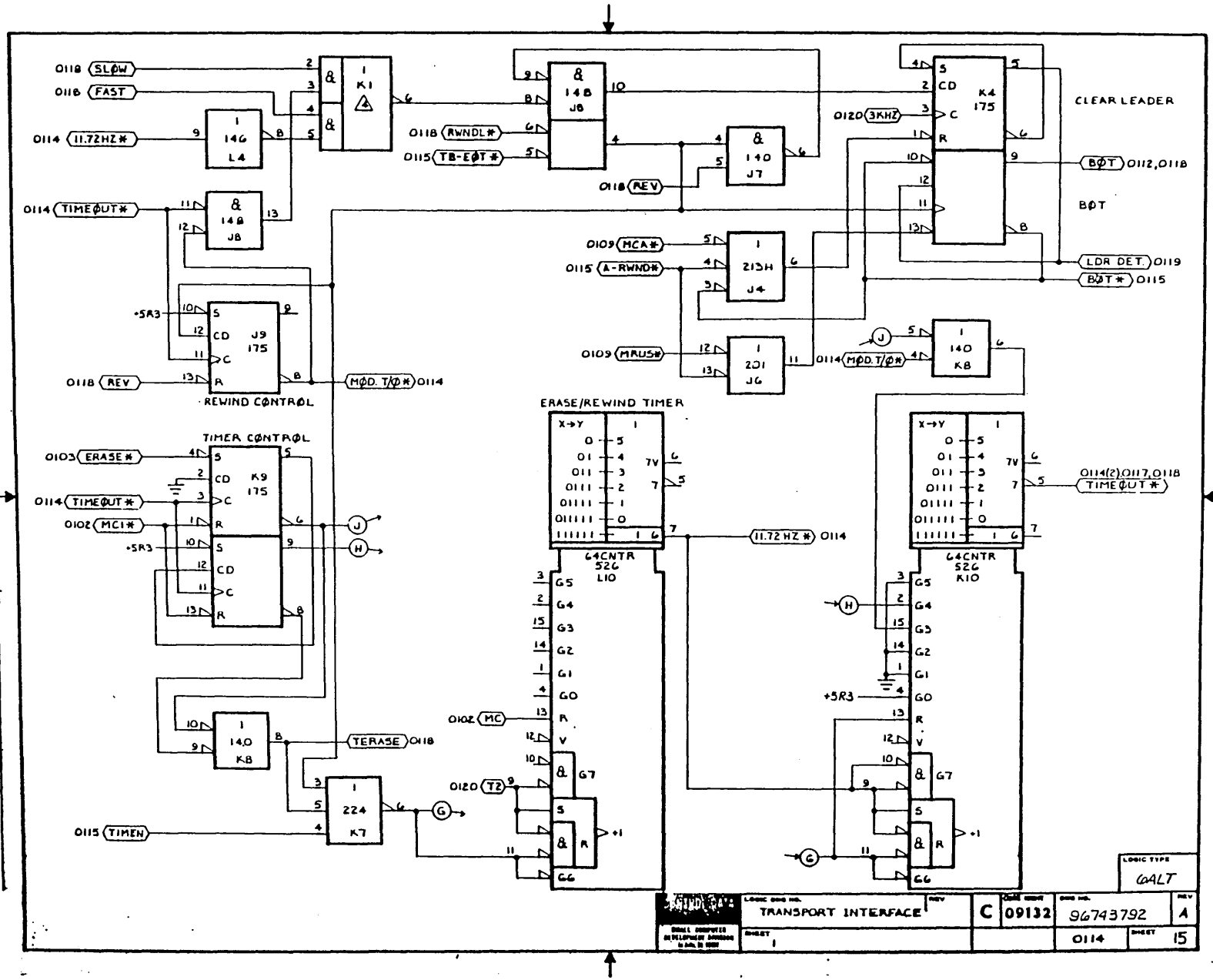


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 15 of 21)

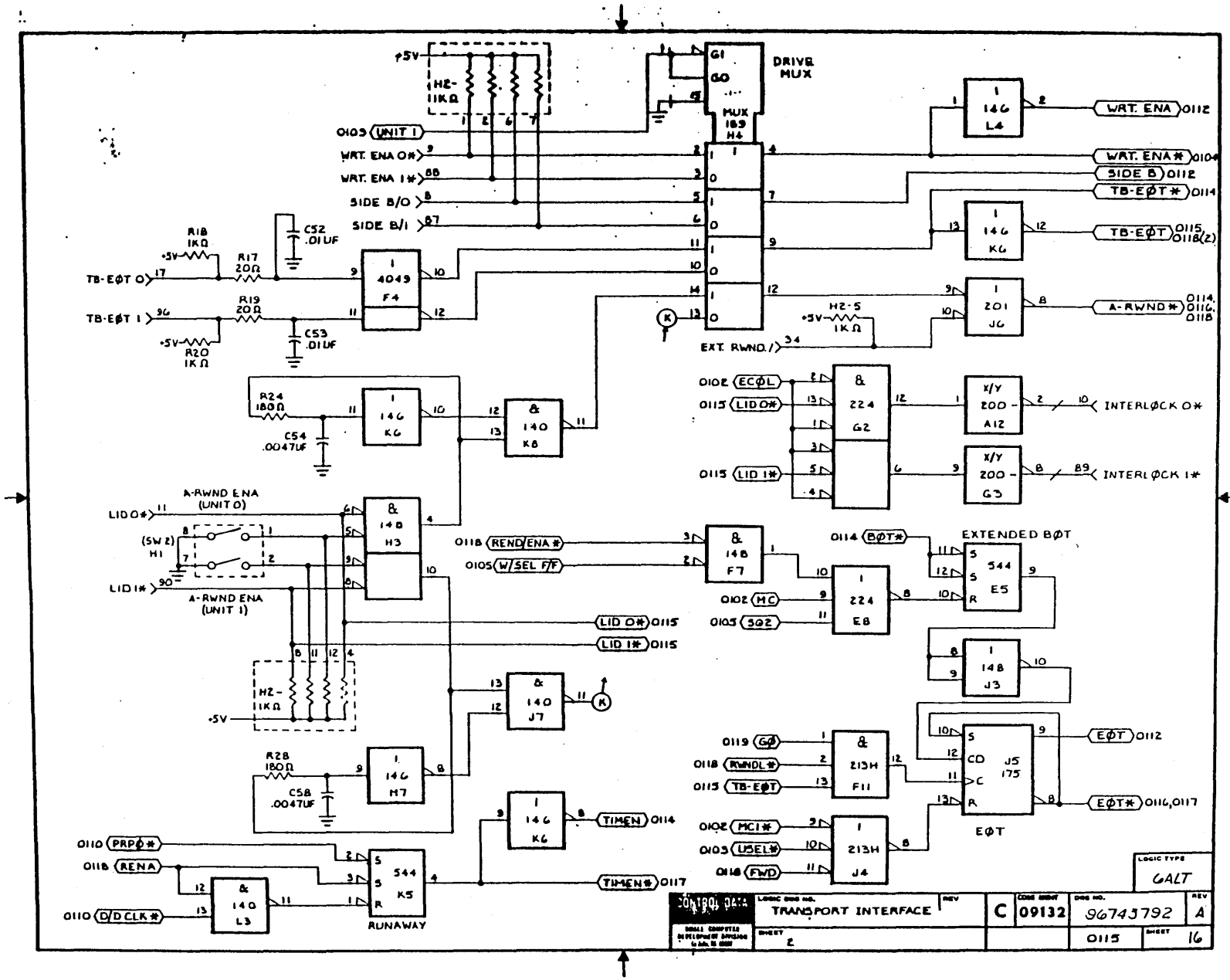


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 16 of 21)

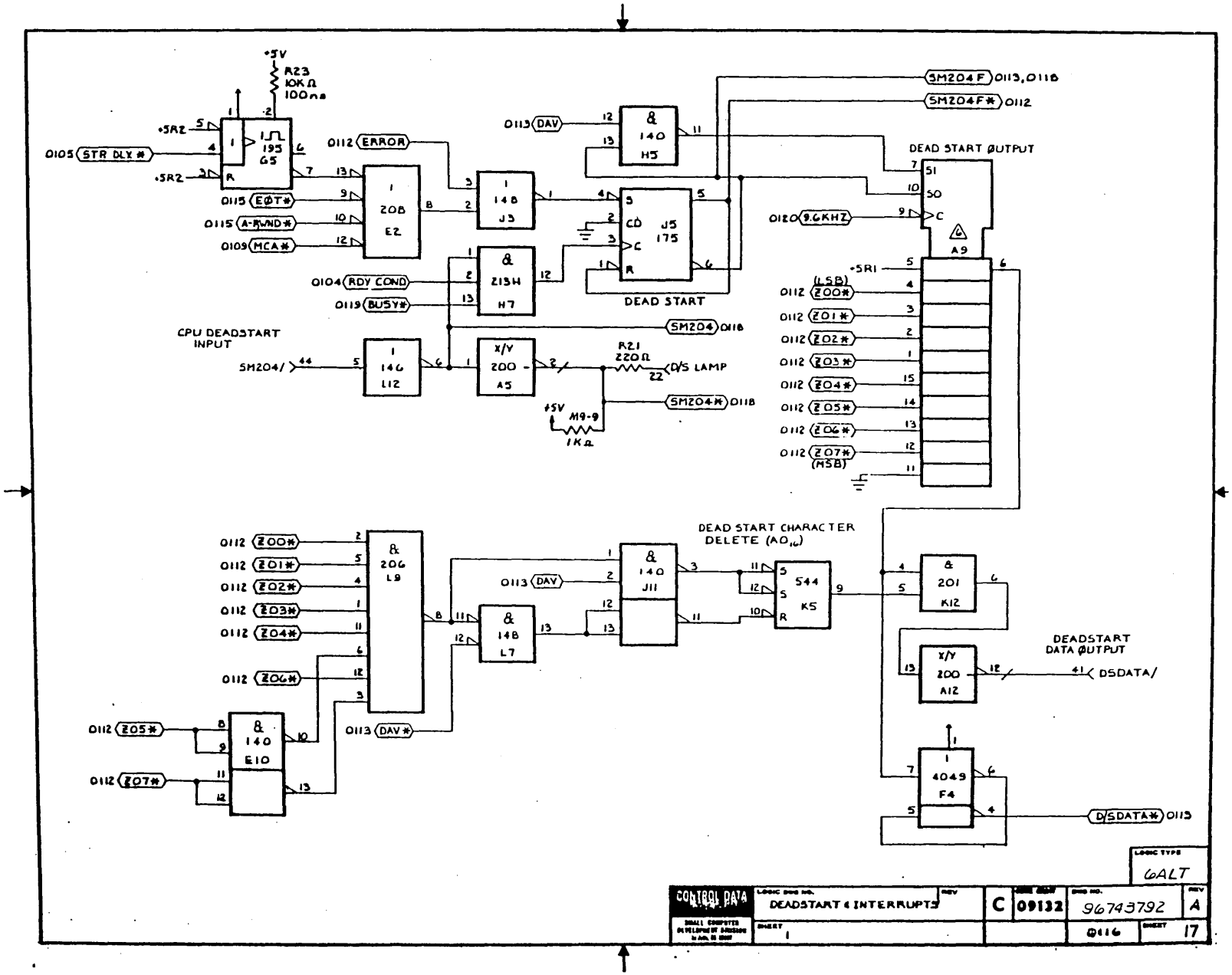


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 17 of 21)

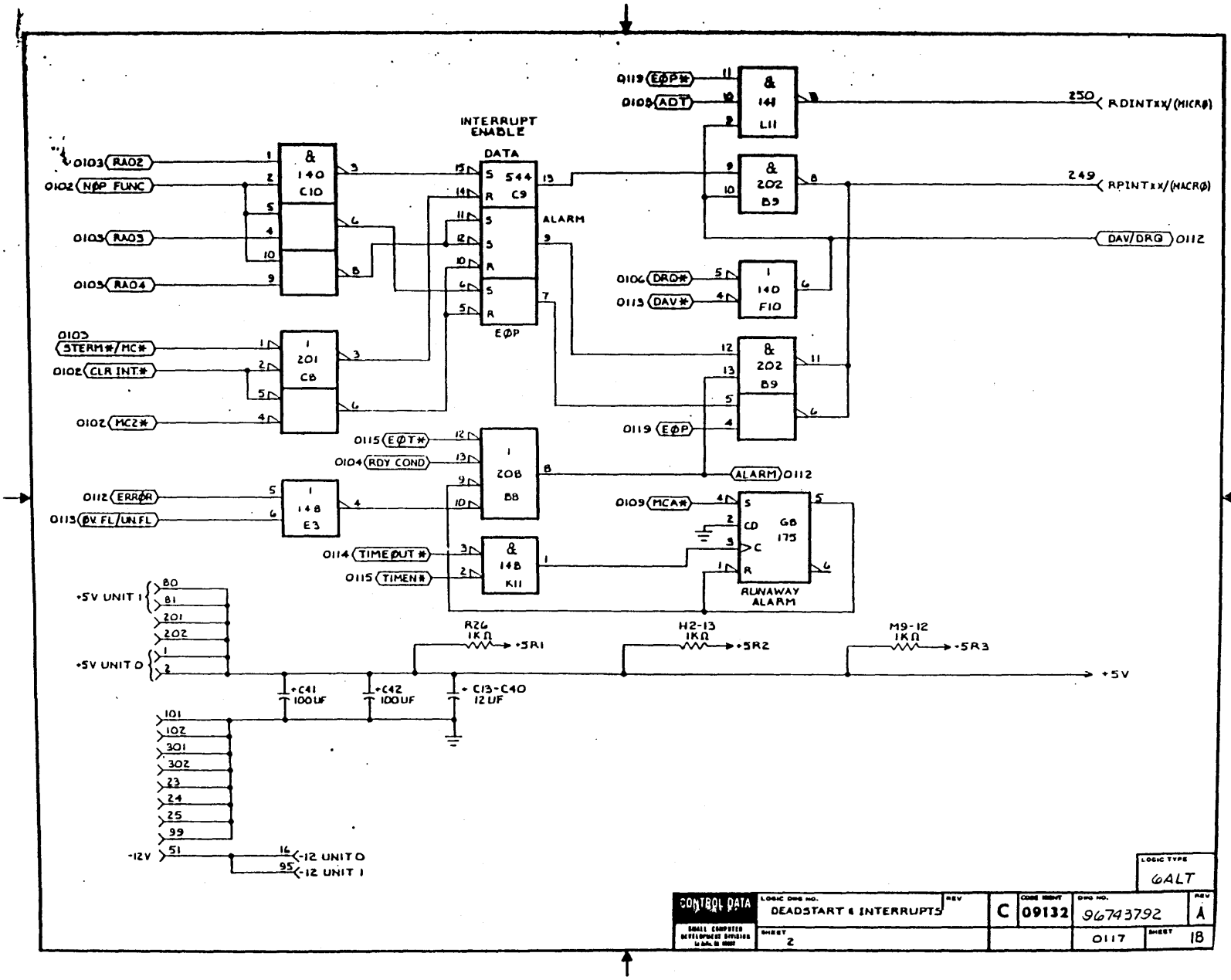


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 18 of 21)

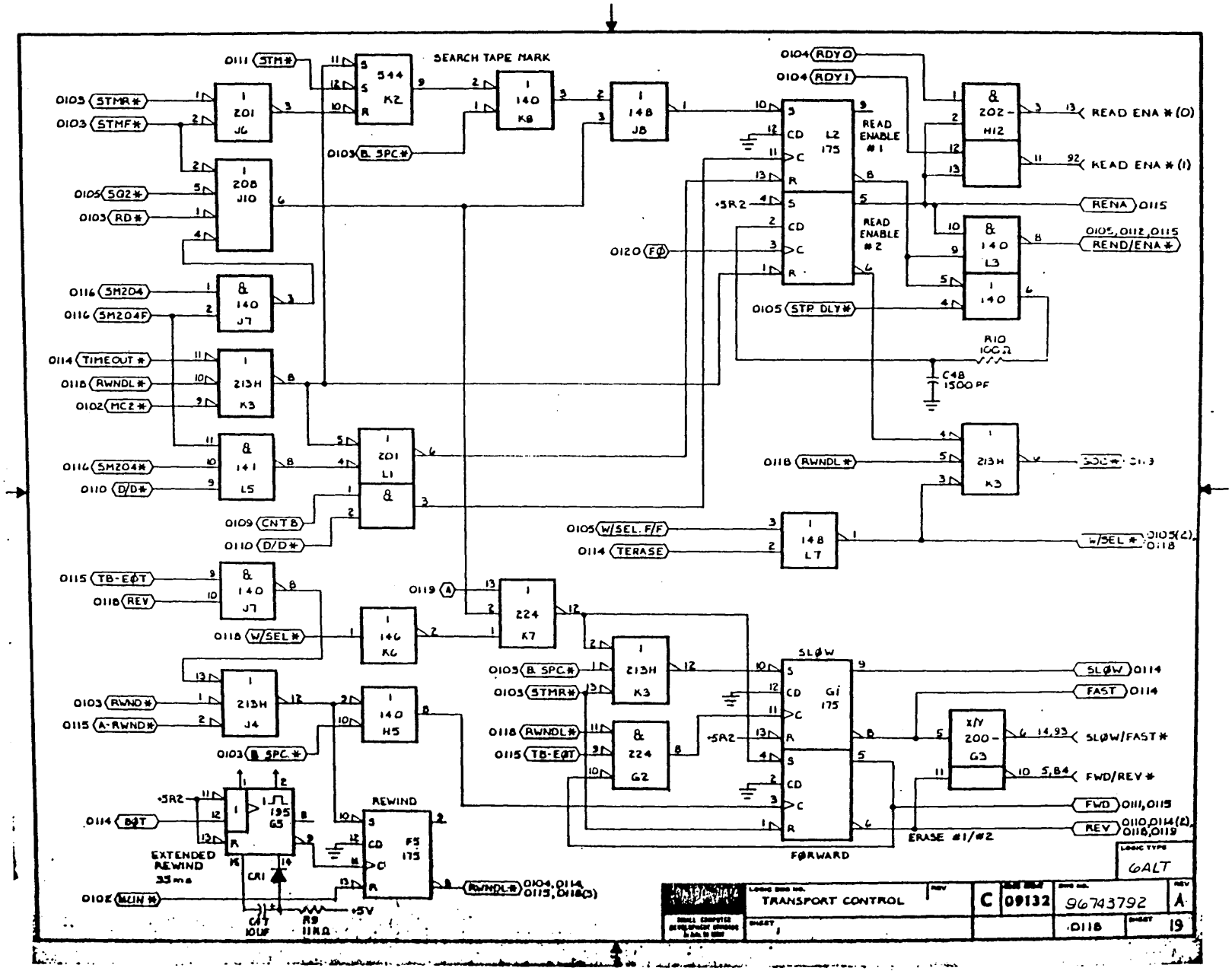


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 19 of 21)

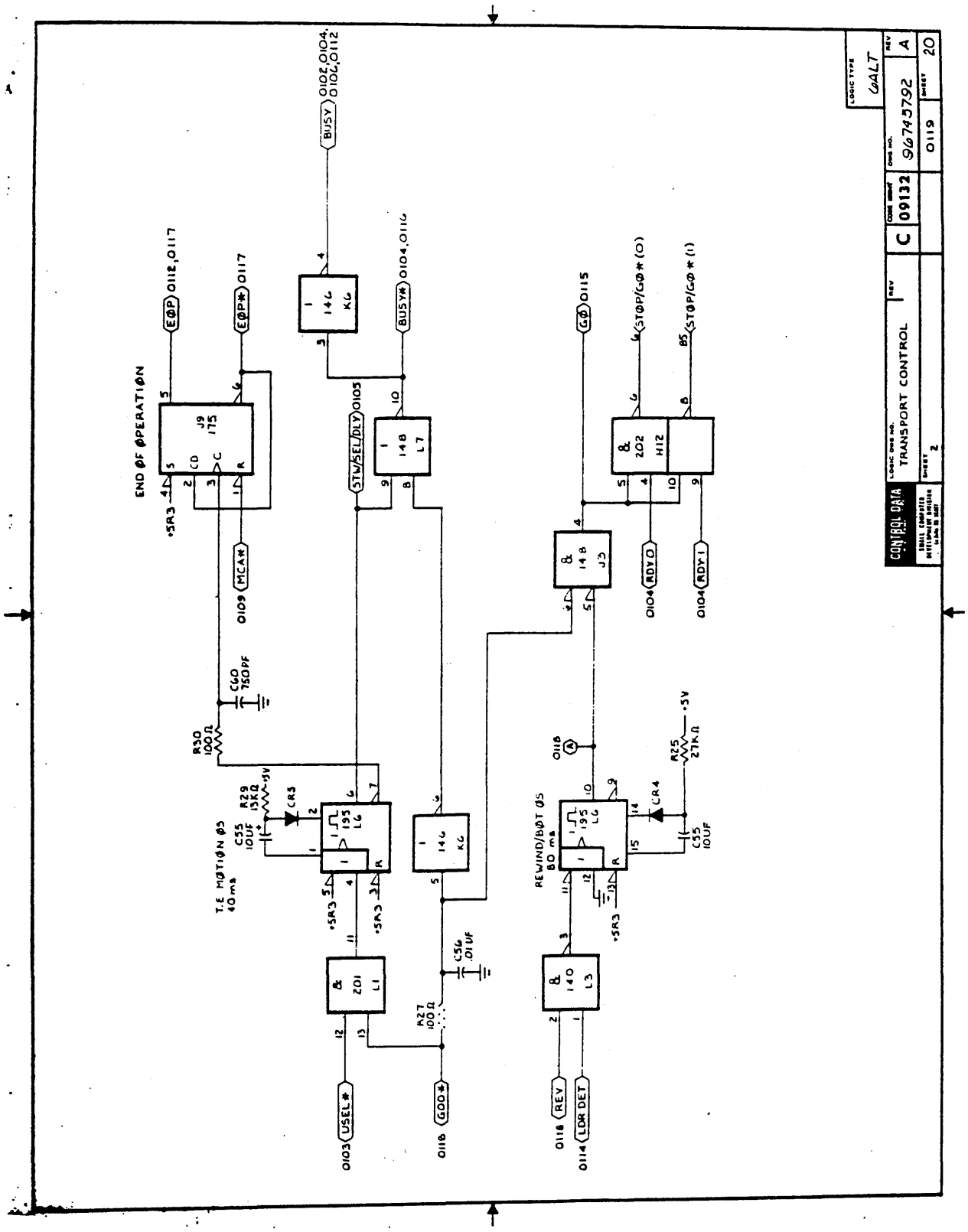


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 20 of 21)

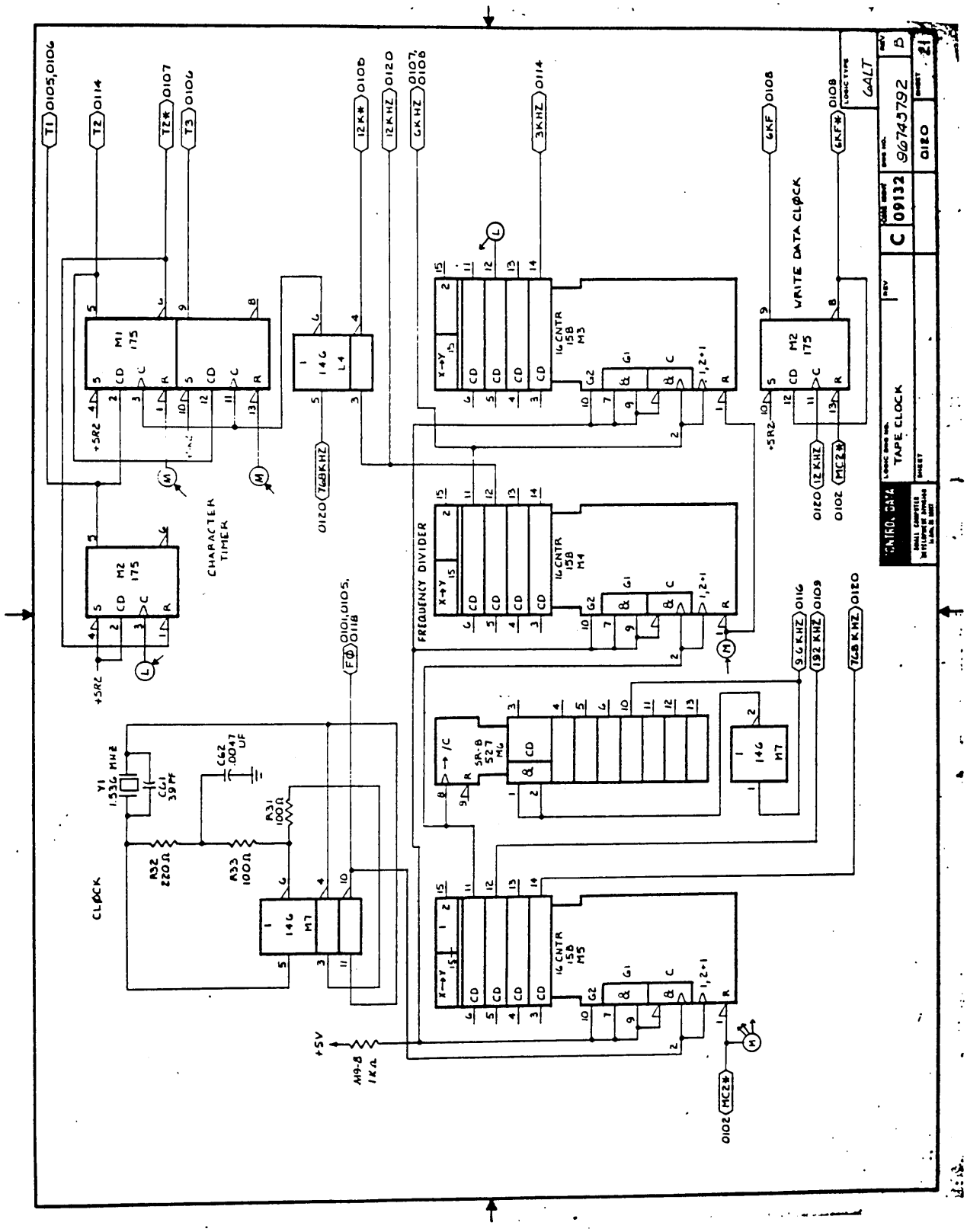


Figure 5-2. Tape Cassette Controller (PWA 96743791) (Sheet 21 of 21)

MAINTENANCE

Both emergency and preventive on-site maintenance is limited to isolating a fault to the replaceable subassembly, then effecting repair by replacing the faulty assembly with a previously tested spare.

SPARES TESTING

All spare subassemblies must be tested upon receipt, with retesting occurring annually.

PREVENTIVE MAINTENANCE

No preventive maintenance is required to the tape cassette controller.

SPECIAL HANDLING FOR ELECTROSTATIC SENSITIVE PRINTED WIRING ASSEMBLIES

CAUTION

The tape cassette controller printed wiring assembly contains MOS-type integrated circuit devices that are subject to damage from electrostatic discharge. This controller has a red solder mask on the noncomponent side to identify the printed wiring assembly as being electrostatic sensitive. When installing or removing the controller, exercise extreme care in handling. Observe common practices such as touching a grounded surface to discharge body potential before handling the printed wiring assembly, turning off processor power before installing or removing the printed wiring assembly, inserting the printed wiring assembly in a special antistatic bag when storing or transporting, and repairing the printed wiring assembly only at a properly equipped and grounded work station.

This section contains figures that provide parts data applicable to the respective tape cassette controller.

For signal cable parts data and point-to-point connector termination information refer to the CYBER 18 equipment cabinet hardware reference/maintenance manual, listed in the preface.

Refer to table 7-1 for spare parts information.

TABLE 7-1. SPARE PARTS LIST

Part No.	Description
96754569	PWA Tape Cassette Controller
96743791	PWA Tape Cassette Controller
NOTE: PWAs 96754569 and 96743791 are functionally equivalent.	

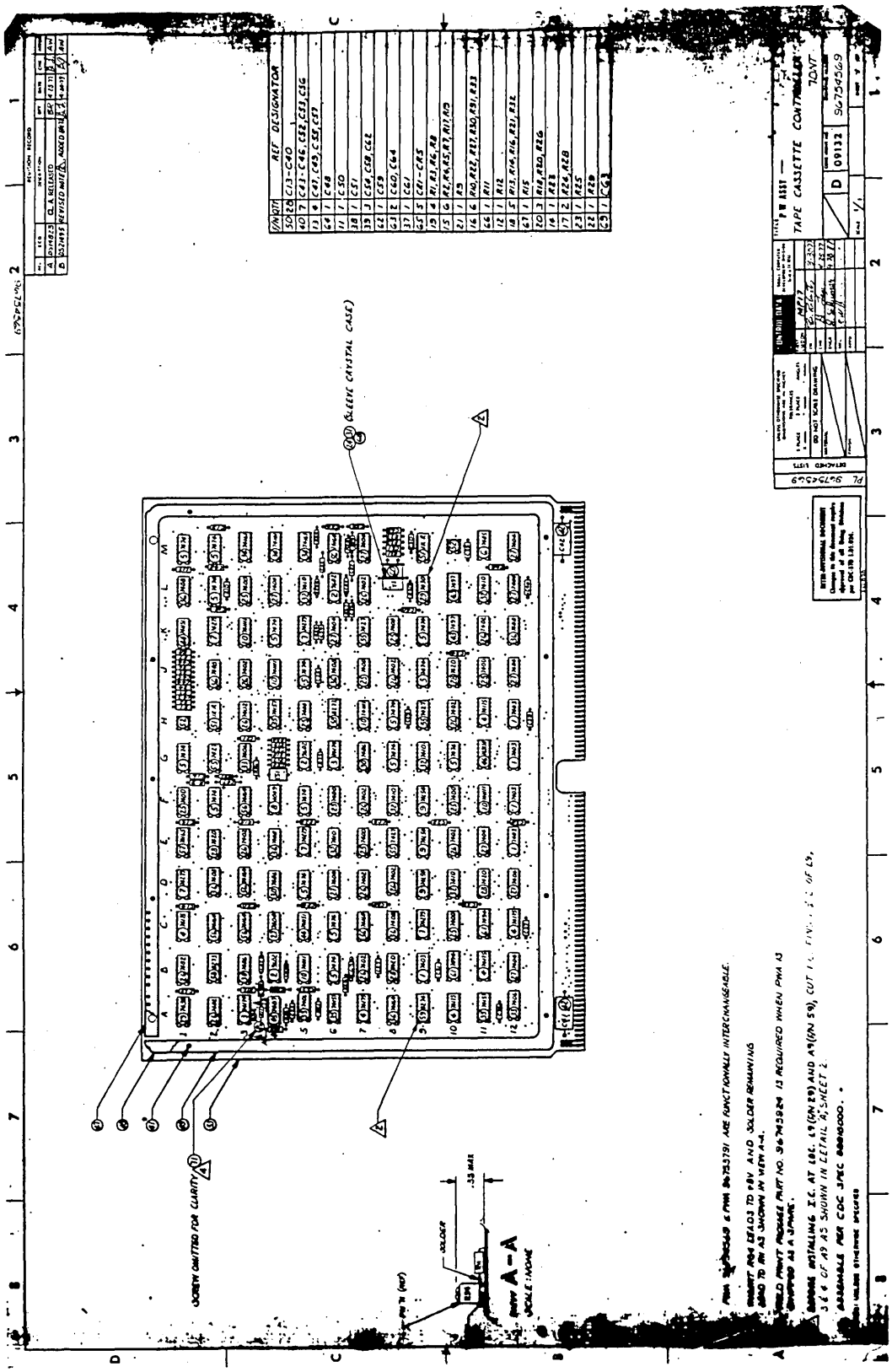


Figure 7-1. Tape Cassette Controller PWA (96754569) (Sheet 1 of 4)

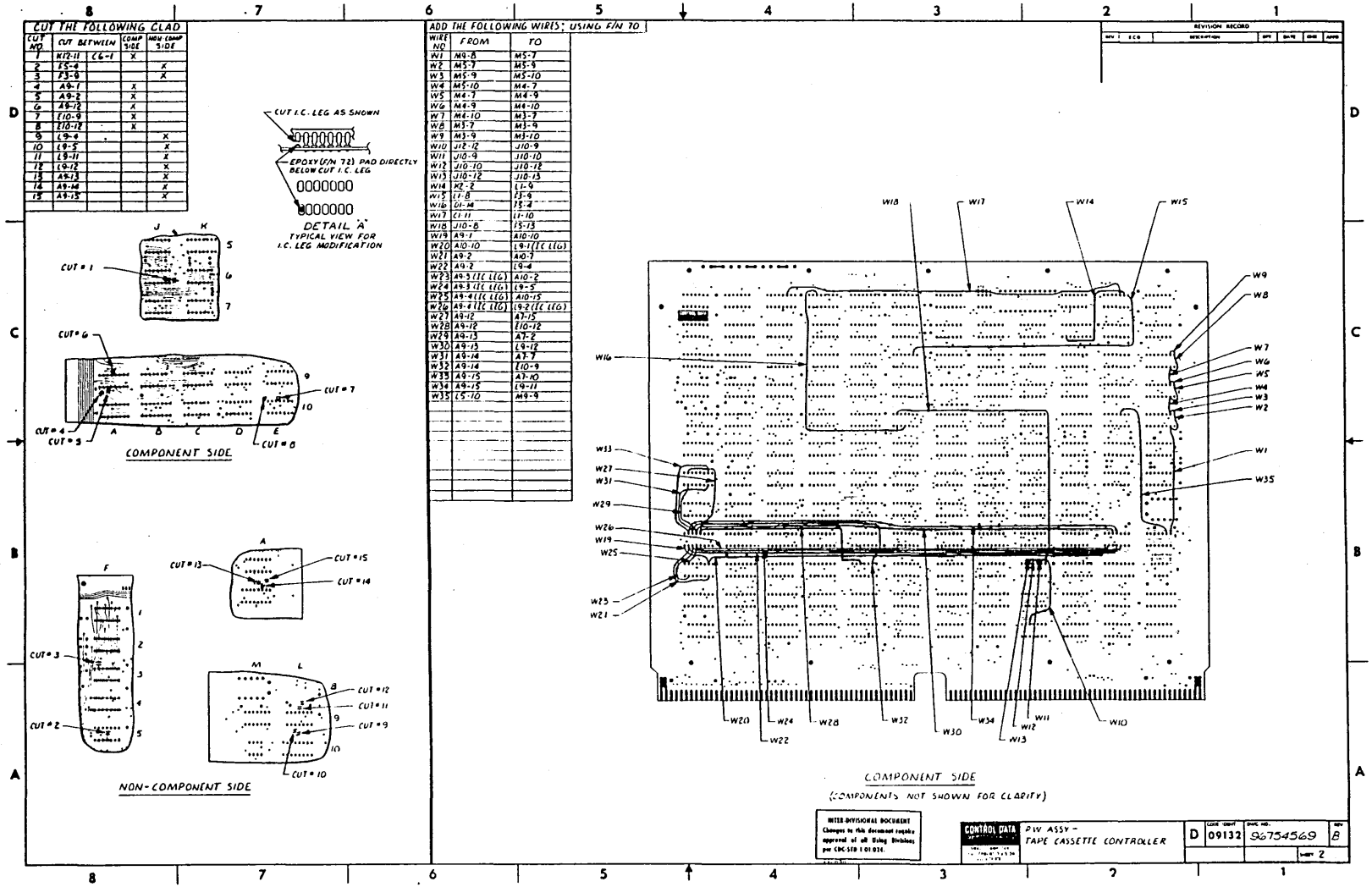
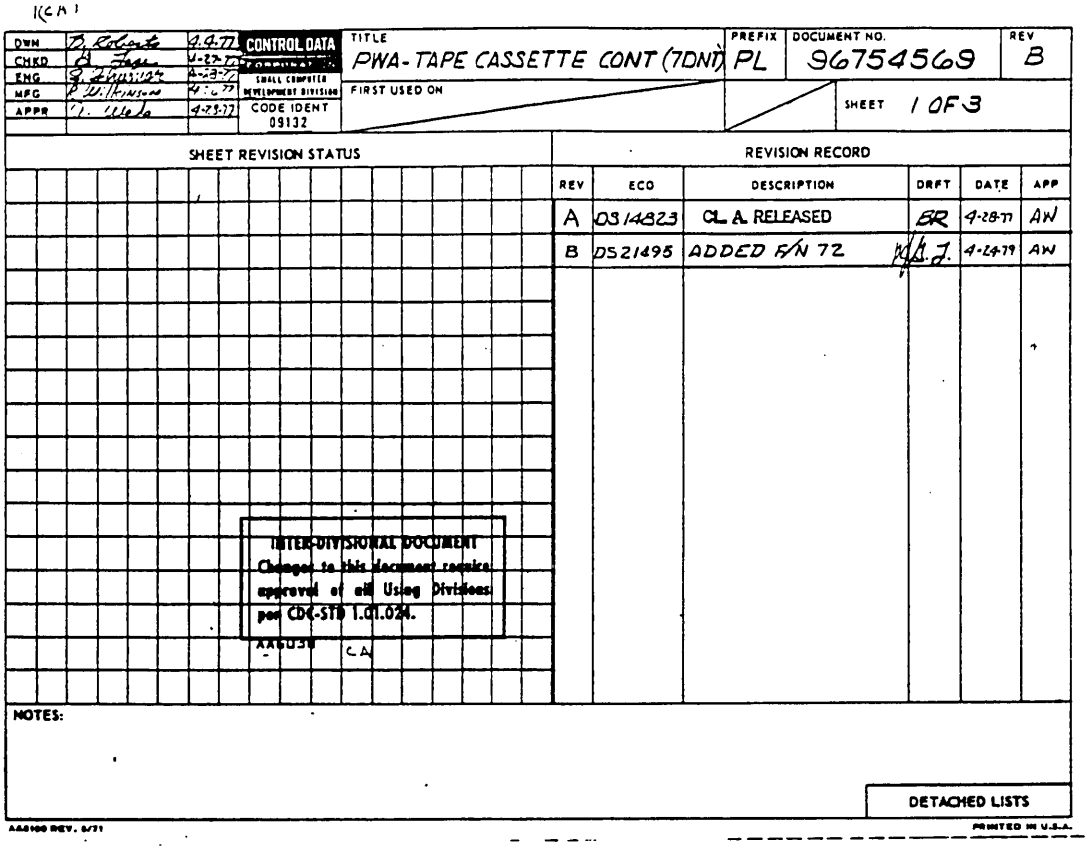


Figure 7-1. Tape Cassette Controller PWA (96754569) (Sheet 2 of 4)



DWN	B. Roberts	4-4-77	CONTROL DATA
CHKD	A. Jones	4-23-77	
ENG	G. Thurston	4-23-77	SMALL COMPUTER DEVELOPMENT DIVISION
MFG	D. Hinson	4-25-77	
APPR	M. Wade	4-25-77	CODE IDENT 09132

TITLE: PWA-TAPE CASSETTE CONT (7DNT) | PREFIX: PL | DOCUMENT NO.: 96754569 | REV: B | SHEET 1 OF 3 | FIRST USED ON

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	03/4823	CL A. RELEASED	BR	4-28-77	AW
B	05 21495	ADDED F/N 72	M.J.	4-24-79	AW

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
AA6038 CA

NOTES:

DETACHED LISTS

AA6100 REV. 6/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE: S = SPARE PARTS; N = NON SPARE PARTS

SH 2

MF

ASSEMBLY NUMBER	REV	CLASS	SW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96754569	B	CLA	D	PWA-TAPE CASSETTE CONT (7DNT)	DSM	MP17	04/18/77	04/21/79	1

FIND NUMBER	SW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE DOC. NUMBER	DATE EFFECTIVE	MASS/OUT PART TYPE	PRI ME	S A N
8	A	15134700	100	PC	IC 40498 HEX INVERTER	IN			PPP4		N
9	A	15143200	300	PC	IC 74L54 TTL 4-WD AND/OR INVRT	IN			PPP4		N
13	C	17706712	400	PC	CAP FIXED SOLID TANTALUM 110	IN			PPP4		N
11	C	17706719	100	PC	CAP FIXED SOLID TANTALUM 110	IN			PPP4		N
15	C	24500022	600	PC	RES FXD .25W 20 OHMS	IN			PPP4		N
16	C	24500039	600	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
17	C	24500045	200	PC	RES FXD .25W 180 OHMS	IN			PPP4		N
18	C	24500047	500	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
19	C	24500053	400	PC	RES FXD .25W 390 OHMS	IN			PPP4		N
20	C	24500063	300	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
66	C	24500084	100	PC	RES FXD .25W 7500 OHMS	IN			PPP4		N
14	C	24500087	100	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
21	C	24500088	100	PC	RES FXD .25W 11000 OHMS	IN			PPP4		N
22	C	24500090	100	PC	RES FXD .25W 13000 OHMS	IN			PPP4		N
12	C	24500094	100	PC	RES FXD .25W 20000 OHMS	IN			PPP4		N
23	C	24500097	100	PC	RES FXD .25W 27000	IN			PPP4		N
24	C	24501806	200	IN	WIRE ELECT SOLID COPPER 24 GA	IN			PPP1		N
38	C	24521201	100	PC	CAP FIXED MET MYLAR DIAL 1 PC	IN			PPP4		N
68	A	25196909	200	IN	INSUL SLEEVE SHRINK 1IN CLEAR	IN			PPP3		N
67	A	38811277	100	PC	RES FXD MF 51.1KOHMS 1/4W 1PCT	IN			PPP4		N
31	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN			PPP3		N
70	C	52629949	18000	IN	WIRE ELEC 30 GA WHITE	IN	039382		PPP1		N
72	A	62019900	100	OZ	EPOXY, 2 PART 5 MIN(CLEAR)TUBE	IN	021495	04 20 79	PPP3		N
51	A	75009901	200	PC	RESISTOR MODULE 1K OHM 2 O/O	IN			PPP4		N
71	A	84605226	100	PC	POT, TRIM, CER, 10K OHMS	IN			PPP4		N
37	A	84996706	100	PC	CAP,CER 100V 39 PF	IN			PPP4		N
69	A	84996717	100	PC	CAP,CER 100V 220 PF	IN			PPP4		N
62	A	84996719	100	PC	CAP,CER 100V 330 PF	IN			PPP4		N
63	A	84996726	200	PC	CAP,CER 100V 750 PF	IN			PPP4		N
64	A	84996731	100	PC	CAP,CER 100V 1500 PF	IN			PPP4		N
39	A	84996738	300	PC	CAP,CER 100V 4700 PF	IN			PPP4		N
40	A	84996743	700	PC	CAP,CER 100V .01 MF	IN			PPP4		N
41	A	88812400	900	PC	RIVET-SEMI-TUBULAR,HRS .312 LG	IN			PPP4		N
42	A	88880500	200	PC	CAP ELECT-ALUM 16VDC 100UF	IN			PPP4		N
43	A	88880800	200	PC	IC 7497 TTL 6-BIT BINARY MUX	IN			PPP4		N
6	A	88880900	100	PC	IC 7485 TTL 4-BIT MAGN COMPAR	IN			PPP4		N

PROJECT ENGINEER: S SCHUMER | SCMD | INTERDIVISIONAL DOCUMENT

AA 2708-1 REV 7-75

Figure 7-1. Tape Cassette Controller PWA (96754569) (Sheet 3 of 4)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH. 3

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96754569	B	CLA	D	PWA-TAPE CASSETTE CONT (7DNT)	DSM	MP17	04/18/77	04/21/79	2 of 3

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	SPARE CODE	A ON N
44	A	88882000	200	PC	IC 74H51 TTL DUAL 2-WIDE 2-INP	IN			PPP4		N
10	A	88882300	500	PC	IC 74H11 TTL TRIPLE 3-INP AND	IN			PPP4		N
3	A	88882800	200	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPP4		N
4	A	88882900	600	PC	IC 74175 TTL QUAD D F/F W/CLR	IN			PPP4		N
45	A	88883200	100	PC	IC 7407 TTL HEX BUFFER (OC)	IN			PPP4		N
46	A	88885100	100	PC	IC 74S138 TTL DECODER/MUX	IN			PPP4		N
26	A	88885500	1400	PC	IC 7402 TTL QUAD NOR GATE	IN			PPP4		N
30	A	88885700	300	PC	IC 7486 TTL QUAD 2-IN EXCL OR	IN			PPP4		N
34	A	88885800	300	PC	IC 74161 TTL 4-BIT BINARY CNTR	IN			PPP4		N
35	A	88886400	300	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN			PPP4		N
2	A	88886500	300	PC	IC 9602 TTL DUAL MONOSTAB MVB	IN			PPP4		N
47	C	88896600	100	PC	INSULATOR-CARD FRAME,UPPER	IN			PPP4		N
48	C	88896700	100	PC	INSULATOR-CARD FRAME,LOWER	IN			PPP4		N
49	C	88896800	100	PC	FRAME-CARD (CASTING)	IN			PPP4		N
36	A	88897000	700	PC	IC 7408 TTL QUAD 2-INPUT AND	IN			PPP4		N
65	A	88897100	500	PC	DIODE-SILICON SWITCHING	IN			PPP4		N
50	A	88897800	2800	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPP4		N
32	A	88898200	600	PC	IC 7410 TTL TRPL 3-IN POS NAND	IN			PPP4		N
28	A	88898400	400	PC	IC 7420 TTL DUAL 4-IN NAND	IN			PPP4		N
52	A	88899000	200	PC	SWITCH-DUAL IN-LINE 4 POSITION	IN			PPP4		N
53	D	88920300	100	PC	PWB-TAPE CASSETTE CONT (5WHT)	IN			PPP4		N
55	A	88923500	400	PC	IC 7427 TTL TRIPLE 3-INPUT NOR	IN			PPP4		N
56	A	88923600	700	PC	IC 74164 TTL 8-BIT SHIFT REG	IN			PPP4		N
57	A	88923700	100	PC	IC 74165 TTL 8-BIT SHIFT REG	IN			PPP4		N
58	A	88923800	200	PC	IC 8273 TTL 10-BIT SHIFT REG	IN			PPP4		N
59	A	88923900	100	PC	IC 8274 TTL 10-BIT SHIFT REG	IN			PPP4		N
25	A	88924400	1000	PC	IC 7400 TTL QUAD 2-I POS NAND	IN			PPP4		N
27	A	88924500	1100	PC	IC 7404 TTL HEX INVERTER	IN			PPP4		N
29	A	88924600	200	PC	IC 7430 TTL QUAD 2-IN POS NAND	IN			PPP4		N
60	C	94242518	100	PC	CRYSTAL,QUARTZ 1.536 MHZ	IN			PPP4		N
61	A	94913200	200	PC	IC 7494 4-BIT SHIFT REGISTER	IN			PPP4		N
1	A	96744154	500	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN			PPP4		N
33	A	96744155	300	PC	IC 7406 TTL HEX INVERTER (OC)	IN			PPP4		N
5	A	96744156	1600	PC	IC 7474 TTL DUAL D EDGE F/F	IN			PPP4		N
7	A	96744157	500	PC	IC 74279 TTL S-R LATCH	IN			PPP4		N
54	C	96754570	REF	PC	LOGIC DIAG-TAPE CASSETTE 7DNT	IN			RFE4		N

PROJECT ENGINEER: S SCHUMER

SCMD

INTERDIVISIONAL DOCUMENT

AA 87000-1 REV. 7-75

Figure 7-1. Tape Cassette Controller PWA (96754569) (Sheet 4 of 4)

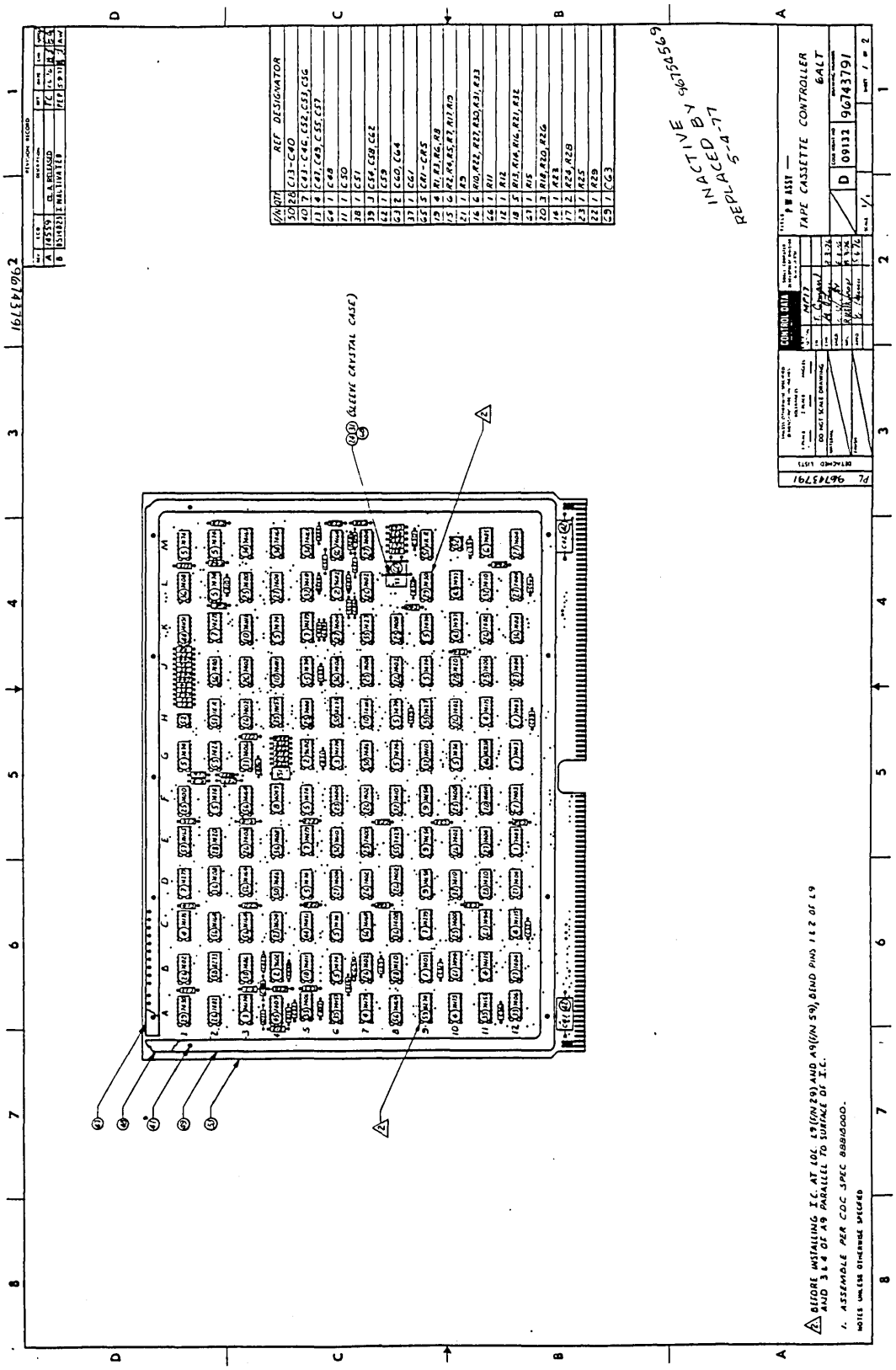


Figure 7-2. Tape Cassette Controller PWA (96743791) (Sheet 1 of 4)

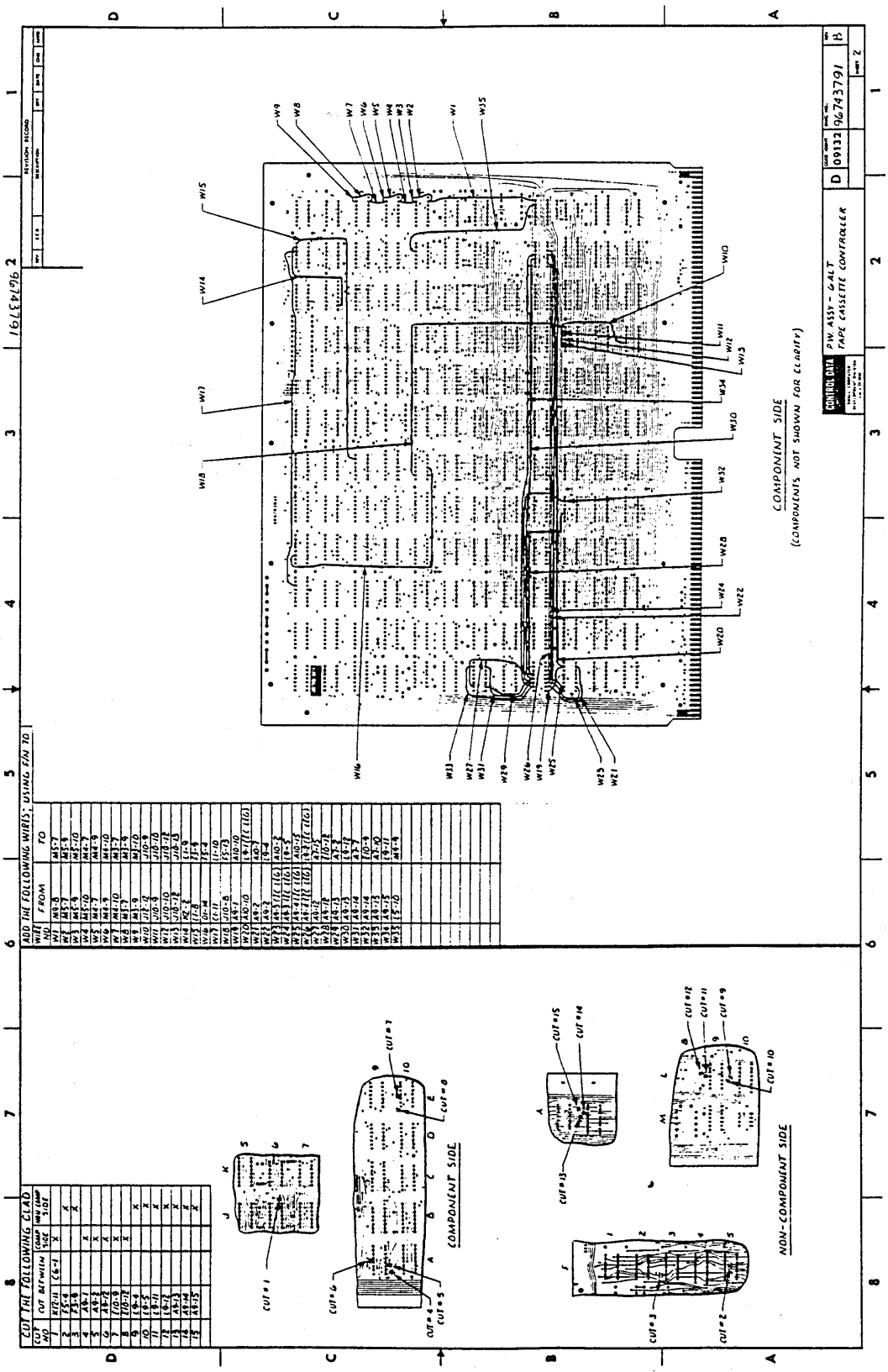


Figure 7-2. Tape Cassette Controller PWA (96743791) (Sheet 2 of 4)

DWN	T. Cyman	7-14-76	CONTROL DATA	TITLE P. W. ASSY - GALT TAPE CASSETTE CONTROLLER	PREFIX	DOCUMENT NO.	REV.
CHKD	A. J. Lage	8-3-76	SMALL COMPUTER DEVELOPMENT DIVISION		PL	96743791	B
ENG	W. Hackett	8-9-76		FIRST USED ON MP17		SHEET 1 OF 3	
MFG	R. Wilkinson	8-5-76					
APPR	G. Mossin	8-6-76	CODE IDENT 09132				

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A	14559	DL A. RELEASED	TC	8-6-76	E.G.
B	DS14823	INACTIVATED	PEP	5-9-77	AW

NOTES:

DETACHED LISTS

AA2100 REV. 6/71 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

SH 2

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USED	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96743791	B	INA	D	PWA-TAPE CASSETTE CONT (GALT)	DS	MP17	07/30/76	04/18/77	1/ 2

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PH PC	A QN N
8	A	15134700	100	PC	IC 40499 HEX INVERTER	IN			PPP4		N
9	A	15143200	300	PC	IC 74L54 TTL 4-WD AND/OR INVPT	IN			PPP4		N
12	C	17705902	100	PC	RES FXD .25W 39000 OHMS	IN			PPP4		N
13	C	17706712	400	PC	CAP FIXED SOLID TANTALUM 110	IN			PPP4		N
11	C	17706716	100	PC	CAP FXD SOLID TANTALUM	IN			PPP4		N
15	C	24500022	600	PC	RES FXD .25W 20 OHMS	IN			PPP4		N
16	C	24500039	600	PC	RES FXD .25W 100 OHMS	IN			PPP4		N
17	C	24500045	200	PC	RES FXD .25W 180 OHMS	IN			PPP4		N
18	C	24500047	500	PC	RES FXD .25W 220 OHMS	IN			PPP4		N
19	C	24500053	400	PC	RES FXD .25W 390 OHMS	IN			PPP4		N
20	C	24500063	300	PC	RES FXD .25W 1000 OHMS	IN			PPP4		N
14	C	24500087	100	PC	RES FXD .25W 10000 OHMS	IN			PPP4		N
21	C	24500088	100	PC	RES FXD .25W 11000 OHMS	IN			PPP4		N
22	C	24500090	100	PC	RES FXD .25W 13000 OHMS	IN			PPP4		N
23	C	24500097	100	PC	RES FXD .25W 27000	IN			PPP4		N
24	C	24501806	200	IN	WIRE ELECT SOLID COPPER 24 GA	IN			PPP1		N
38	C	24521201	100	PC	CAP FIXED MET MYLAR DIAL 1 PC	IN			PPP4		N
68	A	25196909	200	IN	INSUL SLEEVE SHRINK 1IN CLEAR	IN			PPP3		N
66	C	38811262	100	PC	RES FXD MF 12.1KOHMS 1/4W 1PCT	IN			PPP4		N
67	A	38811277	100	PC	RES FXD MF 51.1KOHMS 1/4W 1PCT	IN			PPP4		N
31	A	39181003	100	IN	INSULATION, TFFLON, 24 AWG	IN			PPP4		N
70	C	52629909	18000	IN	WIRE ELECT 30 GA SOLID WHITE	IN			PPP1		N
51	A	75009901	200	PC	RESISTOR MODULE 1K OHM 2 0/0	IN			PPP4		N
37	A	84996706	100	PC	CAP,CER 100V 39 PF	IN			PPP4		N
69	A	84996717	100	PC	CAP,CER 100V 220 PF	IN			PPP4		N
62	A	84996719	100	PC	CAP,CER 100V 330 PF	IN			PPP4		N
63	A	84996726	200	PC	CAP,CER 100V 750 PF	IN			PPP4		N
64	A	84996731	100	PC	CAP,CER 100V 1500 PF	IN			PPP4		N
39	A	84996738	300	PC	CAP,CER 100V 4700 PF	IN			PPP4		N
40	A	84996743	700	PC	CAP,CER 100V .01 MF	IN			PPP4		N
41	A	88812400	900	PC	RIVET-SEMI-TUBULAR,BRS .312 LG	IN			PPP4		N
42	A	88880500	200	PC	CAP-FIXED AL,16VDC,100UF	IN			PPP4		N
43	A	88880806	200	PC	IC 7497 TTL 6-BIT BINARY MUX	IN			PPP4		N
6	A	88880900	100	PC	IC 7485 TTL 4-BIT MAGN COMPAR	IN			PPP4		N
44	A	88882000	200	PC	IC 74H51 TTL DUAL 2-2-INP 2-INP	IN			PPP4		N
10	A	88882300	500	PC	IC 74H11 TTL TRIPLE 3-INP AND	IN			PPP4		N

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Figure 7-2. Tape Cassette Controller PWA (96743791) (Sheet 3 of 4)

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S : SPARE PARTS
N : NON SPARE PARTS

SH3

ASSEMBLY NUMBER	REV	CLASS	DW SS	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
96743791	B	INA	D	PWA-TAPE CASSETTE CONT (6ALT)	DS	MP17	07/30/76	04/18/77	2/ 2

MF

FIND NUMBER	DW SS	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MASS/UNIT PART TYPE	DN NC	A OR N
3	A	88882800	2.00	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN			PPPA		N
4	A	88882900	6.00	PC	IC 74175 TTL QUAD D F/F W/CLR	IN			PPPA		N
45	A	88883200	1.00	PC	IC 7407 TTL HEX BUFFER (OC)	IN			PPPA		N
46	A	88885100	1.00	PC	IC 74S138 TTL DECODER/MUX	IN			PPPA		N
26	A	88885500	14.00	PC	IC 7402 TTL QUAD NOR GATE	IN			PPPA		N
30	A	88885700	3.00	PC	IC 7486 TTL QUAD 2-IN EXCL OR	IN			PPPA		N
34	A	88885800	3.00	PC	IC 74161 TTL 4-BIT BINARY CNTR	IN			PPPA		N
35	A	88886400	3.00	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN			PPPA		N
2	A	88896500	3.00	PC	IC 9602 TTL DUAL MONOSTAB MVB	IN			PPPA		N
47	C	88896600	1.00	PC	INSULATOR-CARD FRAME,UPPER	IN			PPPA		N
48	C	88896700	1.00	PC	INSULATOR-CARD FRAME,LOWER	IN			PPPA		N
49	C	88896800	1.00	PC	FRAME-CARD (CASTING)	IN			PPPA		N
36	A	88897000	7.00	PC	IC 7408 TTL QUAD 2-INPUT AND	IN			PPPA		N
65	A	88897100	5.00	PC	DIODE-SILICON SWITCHING	IN			PPPA		N
50	A	88897800	28.00	PC	CAP-FIXED SOLID TANT,6VDC,12UF	IN			PPPA		N
32	A	88898200	6.00	PC	IC 7410 TTL TRPL 3-IN POS NAND	IN			PPPA		N
28	A	88898400	4.00	PC	IC 7420 TTL DUAL 4-IN NAND	IN			PPPA		N
52	A	88899000	2.00	PC	SWITCH-DUAL IN-LINE 4 POSITION	IN			PPPA		N
53	D	88920300	1.00	PC	PWA-TAPE CASSETTE CONT (5WHT)	IN			PPPA		N
55	A	88923500	4.00	PC	IC 7427 TTL TRIPLE 3-INPUT NOR	IN			PPPA		N
56	A	88923600	7.00	PC	IC 74164 TTL 8-BIT SHIFT REG	IN			PPPA		N
57	A	88923700	1.00	PC	IC 74165 TTL 8-BIT SHIFT REG	IN			PPPA		N
58	A	88923800	2.00	PC	IC 8273 TTL 10-BIT SHIFT REG	IN			PPPA		N
59	A	88923900	1.00	PC	IC 8274 TTL 10-BIT SHIFT REG	IN			PPPA		N
25	A	88924400	10.00	PC	IC 7400 TTL QUAD 2-I POS NAND	IN			PPPA		N
27	A	88924500	11.00	PC	IC 7404 TTL HEX INVERTER	IN			PPPA		N
29	A	88924600	2.00	PC	IC 7430 TTL QUAD 2-IN POS NAND	IN			PPPA		N
60	C	94242518	1.00	PC	CRYSTAL,QUARTZ 1.536 MHZ	IN			PPPA		N
61	A	94913200	2.00	PC	IC 7494 4-BIT SHIFT REGISTER	IN			PPPA		N
54	C	96743792	REF	PC	LOGIC DIAG-TAPE CASSETTE 6ALT	IN			PFEA		N
1	A	96744154	5.00	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN			PPPA		N
33	A	96744155	3.00	PC	IC 7406 TTL HEX INVERTER (OC)	IN			PPPA		N
5	A	96744156	14.00	PC	IC 7474 TTL DUAL D EDGE F/F	IN			PPPA		N
7	A	96744157	5.00	PC	IC 74279 TTL S-R LATCH	IN			PPPA		N
					NUMBER OF LINE ITEMS = 70						
					HIGHEST FIND NUMBER = 70						

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Figure 7-2. Tape Cassette Controller PWA (96743791) (Sheet 4 of 4)

COMMENT SHEET

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