96728600

CONTROL DATA
CORPORATION

CDC® MAGNETIC TAPE CONTROLLER
FA107-A

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAM DESCRIPTIONS
MAINTENANCE
MICRO CONTROL PROGRAM FLOW CHARTS
MICRO CONTROL PROGRAM LISTING

HARDWARE REFERENCE/MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01	Manual pre-released
(12/75)	
A	Manual released
(6/76)	
B	Manual revised; includes ECO 14640, which eliminates noise on tape following data errors. The front cover,
(12/76)	title page, pages iii, v, vi, and 2-4 are revised.
C	Manual revised; includes ECO 14699 providing conformity to CYBER 18 Computer Systems titles. Publication
(1/77)	change only. Pages iii, v, vii, 3-1, and 6-1 are revised.
D	Manual revised; includes ECO 14853, which corrects errors and improves manual consistency and
(7/77)	format. Pages vii, ix, xi, 1-1, 1-2, 2-1, 2-2, 2-4 through 2-7, 4-1 through 4-10, 4-12 through 4-21,
	4-23, 5-1 through 5-5, 5-7, 6-1 and 6-2 are revised. Pages 4-2.1/4-2.2, 4-6.1/4-6.2 and 5-2.1/5-2.2
	are added.
E	Manual revised; includes ECO DS21279 which corrects and clarifies sample maintenance programs. Pages iii/iv
(10/78)	v/vi, 6-5 through 6-7 are revised.
F	Manual revised; includes ECO DS21402, providing a new typical tape subsystem figure. Pages ii, iii/iv, v/vi,
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or use Comment Sheet in the back c
this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
FA107-A	01 02		

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual, are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

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6-5 thru 6-7	E								
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PHYSICAL DESCRIPTION

The entire logic and firmware of the magnetic tape controller is implemented on one 11 by 14 inch plug-in printed circuit board. The types of logic blocks that make up the magnetic tape controller (MTC) are:

- Micro-programmable processor I/O interface
- Read-only memory micro controller
- Programmable clock generator
- Digital timers
- Tape read registers
- Tape write registers
- Tape control registers

The MTC, consisting of a micro controller with read-only memory architecture, controls all operations of the digital timers, programmable clock generator, tape read registers, tape write registers, and tape control registers.

The magnetic tape controller receives instructions from the CPU to control the operating characteristics, via a translator, of up to four magnetic tape drives (MTDs). The MTC enables the magnetic tape subsystem (translators and tape drives) to create and read American National Standard Institute (ANSI)-compatible nine-track and seven-track, nonreturn-to-zero, inverted (NRZI) recorded tapes. Intermixing of tape drives is allowed, thus giving the subsystem the capability of producing seven- or nine-track, 800 bits per inch, NRZI tapes at 25 inches per second. See figure 1-1 for typical magnetic tape subsystems.

The MTC is constructed utilizing medium-scale integration (MSI) circuits. The controller resides in one A/Q input/output card slot of the micro-programmable (MP) processor chassis. Blowers, which are part of the MP processor chassis, provide forced air cooling for the magnetic tape controller.

Physical and environmental requirements for the magnetic tape controller are as follows.

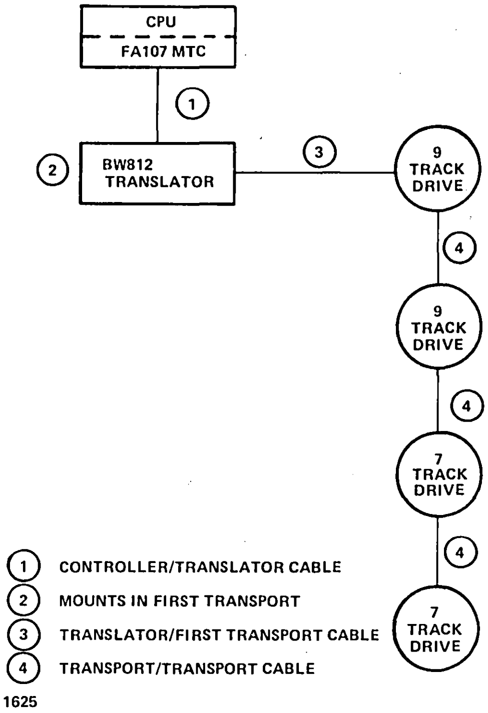
CPU
FA107 MTC
1
2
BW812 TRANSLATOR
3
9 TRACK DRIVE
4
9 TRACK DRIVE
4
7 TRACK DRIVE
4
7 TRACK DRIVE
1 CONTROLLER/TRANSLATOR CABLE
2 MOUNTS IN FIRST TRANSPORT
3 TRANSLATOR/FIRST TRANSPORT CABLE
4 TRANSPORT/TRANSPORT CABLE
1625

Figure 1-1. Typical Magnetic Tape Subsystem

Power:		+5 vdc at 3.1 amps
Temperature:		40° F to 120° F (4° C to 49° C) ambient room temperature
Humidity:		10 to 90 percent relative humidity with no condensation
Warm-Up Time:		None
Non-Operating Environment:		
	Temperature	-30° F to 150° F (-22° C to 65° C)
	Humidity	5 to 95 percent relative humidity with no condensation

FUNCTIONAL DESCRIPTION

The magnetic tape controller, unlike many peripheral controllers, has the flexibility of performing a unique sequence of operations for each of the different requests made by the computer. The exact sequence is determined by the micro program in the read-only memory and is interpreted by the micro controller portion of the magnetic tape controller. This design approach of stored logic (read-only memory) replaces the conventional decoding logic that is fixed (hardwired) for each computer request. The signals generated by each of the MTC's sequenced micro instructions directly control the required hardware processes; no further hardware interpretation procedure is involved (as would occur in conventional peripheral controllers).

TAPE FORMAT ASSIGNMENTS

The functional design of the MTC eliminates the need for switches for assigning the characteristics of each of the MTDs (in other words, track, density). These built-in selectable characteristics (part of the firmware program) are assigned and controlled by software during MTD selection, using the system's SIO set command (see Programming in section 2).

INTER-RECORD GAP

An inter-record gap that conforms to ANSI standards is generated for both seven- and nine-track recording. The timing for accomplishing it is set up internally by the magnetic tape controller.

TIMING

The start and stop timing for the MTCs is a function of the magnetic tape controller. In order to generate accurate gaps, the MTD maintains accurate start and stop times that are the same for all MTD units. No consideration is given to operating MTDs of different types or speed characteristics simultaneously. It is assumed that all MTDs have the same motion characteristics. Timing for data responses, selection, and status is compatible with the I/O timing of the central processor.

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PROGRAMMING

SET/SAMPLE MACRO INSTRUCTION

The MP ~~micro processor's~~ CPU's SIO macro instruction provides for both data output (set) and data input (sample) I/O commands. For data output, the A register's 16-bit word is set (output) to an external device. The word in the Q register is used to select (address) the receiving device. For data input, one 16-bit word from an external device is sampled by input to the A register and the word in the Q register selects the sending device (refer to figure 2-1).

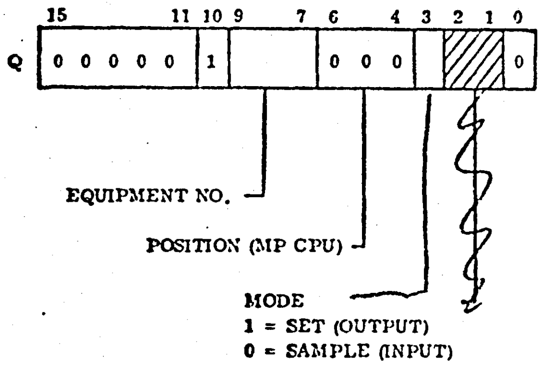

Figure 2-1. SIO Command Out

Bits 7 through 9 specify the equipment number of the MTC. For an NCR M05 CPU, this field is the I/O port address.

To determine the status of the magnetic tape controller, a set I/O command must be issued with any magnetic tape controller function in the A register.

INTERRUPT CONDITIONS (Insert pg 2-2A

~~The magnetic tape controller issues a macro interrupt at the termination of the selected function. Status is available during this interrupt. The macroprogram then responds with a sample I/O to bring the current status into the A register (see figure 2-2).~~

The A register contains the status bits (see Status Conditions) following execution of the SIO sample command.

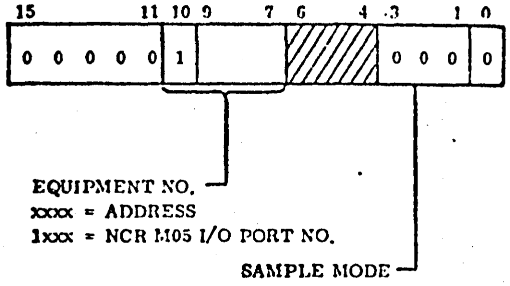

Figure 2-2. SIO Sample Status In

SELECTION

Since an intermix of tape drive track types and densities is allowed, the unit's characteristics must be assigned in the MTC during selection. The MTC and MTD is selected by use of the system's SIO set command; this consists of setting the unit, function, and MTD characteristics. Selection assignments and descriptions are contained in figure 2-3.

NOTE

Whenever a select command is issued by the system, the magnetic tape controller's internal controlware program performs all the required operations that are specified for each function.

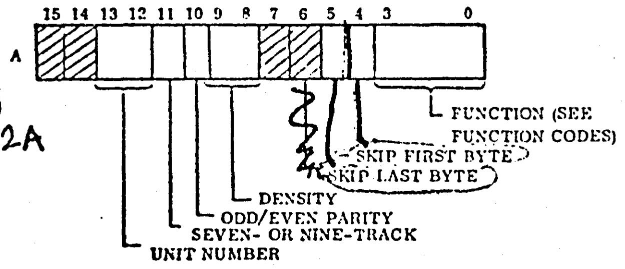

Figure 2-3. Selection Assignments

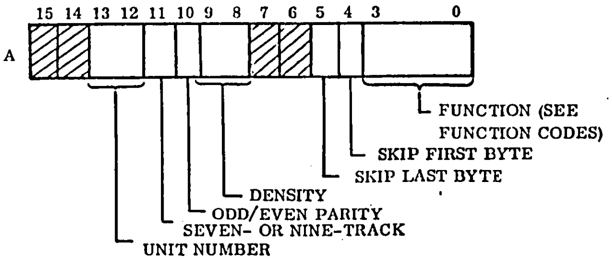

Figure 2-3. Selection Assignments

A-Register Bit Assignments

Skip First Byte

Since the CPU's data word consists of two eight-bit tape bytes, provisions must be made to allow starting a record at any half word. Bit 4 of the A register causes the magnetic tape controller to zero out the first eight bits sent over from the CPU and start recording the second eight bits as the first byte. During a read it causes the MTC to send zeros for the most significant byte to the CPU.

Skip Last Byte

A register bit 5 causes the MTC to ignore the last half of the last word during a write. During a read this bit is ignored.

Density

A register bits 8 and 9 are used to identify the density of the selected tape drive. The assignments are:

A09	A08	Density Selected
0	0	1600 bpi (not currently supported)
0	1	800 bpi
1	0	556 bpi[†]
1	1	200 bpi[†]

Odd/Even Parity

Odd parity is normally used, but in some cases even parity is required. A register bit 10 false means odd parity, and A10 true means even. Nine-track tapes are always odd parity.

Seven- or Nine-Track

A register bit 11 true indicates a seven-track handler, and bit 11 false indicates nine-track.

Unit Number

Unit number selection is made using A register bits 12 and 13 with the assignment being:

A13	A12	Unit Number Selected
0	0	0
0	1	1
1	0	2
1	1	3

FUNCTION CODES

As the channel and the unit are being selected, the function code field is decoded by the MTC. Bits 0 through 3 are used to assign the functions.

A03	A02	A01	A00	Function
0	0	0	0	Invalid MTC function
0	0	0	1	Read forward
0	0	1	0	Write forward
0	0	1	1	Erase
0	1	0	0	Backspace
0	1	0	1	Rewind
0	1	1	0	Rewind and unload
0	1	1	1	Write tape mark
1	0	0	0	Select
1	0	0	1	Recovery read
1	0	1	0	Controlled backspace
1	x	x	x	Diagnostic (B, C, D, E, and F)

[†] Requires hardware changes at tape subsystem level.

The A00 through A03 lines are coded to the above functions. A 0000 function code causes a program error and is reflected in the status word.

Read Forward

A read forward function (0001) causes the selected MTD to move forward at its assigned tape speed.† As read data is encountered, it is assumbled by the MTC and transferred to the memory buffer area in 16-bit words. Data transfer stops when the memory buffer is full, but the tape continues to move until properly positioned in the interblock gap.

In the event of an error, the tape always positions itself to the end of the block; however, data transfer may cease, depending on the type of error. For system overload conditions, data is assumed to be lost, and the transfer terminates immediately. For any data errors such as parity, longitudinal redundancy check (LRC), or cyclic redundancy check (CRC), the error condition is stored and the data transfer continues.

Error correction using CRC recovery may be performed on nine-track units only. Correction is automatically attempted by first initiating a backspace and then following that with a second read command. During the first read operation, the tape track in error is determined, and on the subsequent read the MTC tries to correct the data error. Following each read operation, the CRC check character at the end of the block is read and compared to the MTC's internally created CRC check character. When they are equal, the read data in the CPU's memory is considered valid. If repeated attempts to read (normally two, at a system software level) still result in data errors, then the error condition is considered to be uncorrectable.

If a read function is issued immediately following a write function, the read function is aborted and the read after write status flag is set. This is based on the theory that any write operation creates a new block of data and invalidates the original data block following it. This feature is bypassed by performing a backspace and a read following any write operation. A benefit of this imposed restriction is that it allows the software program to read verify the last block of data created.

Write Forward

The write forward function (0010) causes the selected MTD to write data in the forward direction, in the mode set up during selection. Writing continues until the processor interface terminates the function. An overload condition causes the operation to terminate immediately. A data error or dropout detection condition is stored with the operation continuing to its normal end. All data recorded has parity assigned and appropriate status stored. For correct repositioning following a data error or dropout, a controlled backspace (see function code 1010) is used.

Following an overload condition, a standard backspace command, as opposed to a controlled backspace; should be used because the number of characters missing is indeterminate.

During the write operation, the read head reads the just-written data and sends it to the MTC for error checks. If an error is detected, it is indicated in the status, but data continues to be written on tape until the processor interface completes the block.

When writing from BOT, the initial gap between BOT and the first block is a minimum of 8.5 inches (21.6 cm). The timing for this gap is in the MTC controlware program and allows for the distance between the BOT sensor and the write head.

Erase

The erase function (0011) causes the selected MTD to erase forward for a fixed distance of 6 inches (15.2 cm) and stop. During the erase operation the read head reads the erased portion and, if unerasable noise exists, the dropout/pickup status is set (see Status Conditions).

Backspace

The backspace function (0100) causes the MTD to move tape in the reverse direction over one record of data and stop with the head positioned properly (no closer than the start distance) in the inter-record gap. Timing for backspace is set up so that the gap spacing does not get smaller as a result of repeated forward-backspace functions. If backspace is issued when the tape is at load point (BOT), no tape motion results.

† 25 ips is the only speed presently support by the MTC.

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Rewind

The rewind function (0101) causes the selected MTD to move tape in a reverse direction at high speed. Once the rewind function has started, the MTD is deselected but continues to rewind and the MTC sends the appropriate terminating status. If a rewinding MTD is

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Rewind

The rewind function (0101) causes the selected MTD to move tape in a reverse direction at high speed. Once the rewind function has started, the MTD is deselected but continues to rewind and the MTC sends the appropriate terminating status. If a rewinding MTD is accessed, it flags a rewinding at selection time status. Rewind continues until load point (BOT) is reached and the MTD is left in a ready state.

Rewind and Unload

This function (0110) is the same as rewind, except that the MTD is placed in a not ready state upon reaching BOT. To continue using the tape unit,it is necessary to manually set it back to a ready state. The tape is not physically unloaded.

Write Tape Mark

This function (0111) causes a tape mark to be written on nine-track NRZI tape units only. The tape mark is a 13_{16} code, as defined by ANSI standards.† If the tape is seven-track NRZI, this command causes the intermediate status for illegal command to be set. Tape mark on a seven-track tape must be written as data, using a write function. When reading tape marks, this data is sent to the processor interface. Reading any tape mark causes a tape mark terminating status to be set in the MTC.

Select

The select function (1000) causes the MTC to select an MTD and respond with a program interrupt without causing any action in the MTD. This allows the software to get status from the tape system without executing a function. This operation reports write lockout and inoperative during selection and rewinding.

Recovery Read

The recovery read function (1001) is identical to the read command except that the sensitivity of the read circuits in the MTD is increased. This permits reading data that might otherwise be lost. Before using recovery read, software should make at least two attempts to read using the normal read. This may recover some data by cleaning the tape with the repeated passes. If that fails, recovery read should then be tried.

Controlled Backspace

The controlled backspace function (function code 1010) causes the tape to move as many character frames in reverse as the number of eight-bit characters contained in the CPU's ADT memory buffer. This operation may be considered as being a reverse write, but without writing actual data on tape. When the MP micro processor has sent the desired number of characters, it terminates the function. The use of this function provides a means of reversing over dropouts without positioning errors.

Diagnostic

Function codes 1011 through 1111 are used to diagnostically check the operation of the controller. They are accomplished by dedicated micro routines within the controller. Section 6 presents a complete description of tests, function codes, significance of tests, and expected test results. Hexadecimal notation is used for ease in expressing the four-bit groups that occur in the instruction format. A brief description of the controller's self-test function codes and micro diagnostic tests follows:

Function Codes (Hexadecimal)	Test Group	Description
x01B	B	Controller jump and return instruction
x02B	B	Controller counter number 1
x04B	B	Controller counter number 2
x10B	B	Controller timers
x20B	B	Controller parity (using zeros)

† If additional information on tape marks is required, refer to CDC Standard 1.10.000.

Function Codes (Hexadecimal)	Test Group	Description
x50B	B	Controller parity (using ones)
x40B and x00B	B	Status interrupt with inoperative during selection status set
x48B	B	Clear status register, generate status interrupt
xxxC	C	Controller branch checks
xxxD	D	Set status bits, return with a status interrupt
xxxE	E	Simple branch test
xxxF	F	Issue interrupt only

STATUS CONDITIONS

Status is sent to the CPU by executing a SIO sample command either during selection or after completion of the function. In either case, the MTC sends a program interrupt indicating that status is available to be read. The intermediate status received during selection is sent as a result of a condition arising from selection and the requested function is not started. The terminating status (operating complete) reports status arising from the execution of the function. Status is sent to the CPU A register as a 16-bit word from the MTC status register (see figure 2-4).

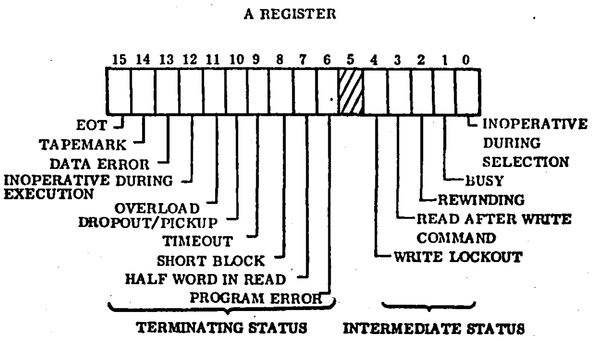

Figure 2-4. Status Assignments

Inoperative During Selection

Inoperative status is set when the MTC is accessed but it is unable to be selected. Selection cannot be completed because of an MTC malfunction or the MTD is not ready.

Busy

Busy status is set if the MTD is busy performing or terminating the previous command (except rewinding) when the MTC is accessed.

Rewinding

If the selected unit is busy rewinding, it sets this status bit and an attempted selection is not completed.

Write Lockout

This status indicates that a write forward, write tape mark, or erase function was issued but the write enable ring was not installed on the reel. The MTD does not perform the write function.

Read After Write

This status is set if a read function is given and the previous command was a write function. Attempting to read an old record, after record new data before it, is not allowed.

Program Error

This status is set if any of the following occur:

- An attempt is made to write nine-track data on a seven-track unit

- Any illegal function bit or set of bits, including a 0 function code, is received by the MTC
- Any data format function other than odd parity at 800 bpi for a nine-track unit is received

Half Word on Read

The CPU word is 16 bits long and the byte on tape is eight bits maximum (plus parity). When reading from tape, the number of bytes may not fill an even number of CPU words. If not, this status is set. In addition, reading a nine-track tape mark causes this status bit to be set.

Short Block

The minimum block length for nine-track NRZI is 18 ANSI characters. If a record short than this is detected, this status is stored. The intent is to detect short blocks that may be noise or partial records. This status does not apply to seven-track format.

Timeout

Timeout status is set for three conditions. During a write function, if read data is not received at the time that the just-written data should be at the read head, then this status is set. During a non-write function, if tape moves 30 feet without termination (runaway), this status is set and the function is terminated. In the case of initiating a backspace while at BOT, no tape motion results and this status is set after 15 seconds.

Dropout/Pickup

This status is set if a character dropout is detected during a read or read back during write function, or if noise pickup is detected during erase.

Overload

A system overload condition (lost data) occurs when the processor interface does not send or receive data in time to keep up with the tape system. The amount of data lost is indeterminate. Data transfer with the CPU stops, following on overload, but tape moves to the gap and positions properly.

Inoperative During Execution

Inoperative status is set up when a condition occurs to cause the MTD to go out of the ready state during execution of a function.

Data Error

This status is set for any or all of the following conditions:

- Parity error detected
- Longitudinal redundancy check error detected
- With nine-track tape, a cyclic redundancy check error detected

End of Tape (EOT)

This status indicates that the end of usable tape has been reached and sensed. This status is set for all commands that are performed while EOT is true from the drive.

Tape Mark

If, during a read or recovery read operation, a tape mark record is sensed, this status is set. For nine-track tape, an ANSI tape mark character is used and is sent to the CPU. For seven-track tape, any one- or two-character record constitutes a tape mark and is sent to the CPU as data.

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ion for this section is contained in the CYBER ~~Micro-mable~~ Computer ~~Family~~ SYSTEM Installation Manual and in the ~~CYBER 18-10/734-2 Micro-Programmable Processor~~ Cyber 18-05/18-10 Computer System. Hardware Maintenance Manual.

INSTALLATION AND CHECKOUT 3

Information for this section is contained in the Micro-Programmable Computer Family Installation Manual and in the CYBER 18-10/734-2 Micro-Programmable Processor Hardware Maintenance Manual.

MTC INTERFACE CONNECTIONS

Figure 4-1 illustrates the MTC's front-end interface to the micro-programmable computer family and the back-end interface to the magnetic tape drives (MTDs).

CPU I/O commands and write data are transmitted to the MTC over the SD backplane lines. Tape read data and MTC/MTD status are input to the CPU's A register from the MTC via the RD backplane lines. Table 4-1 lists the CPU backplane lines used by the MTC and their functions.

As the MTC was originally an NCR M05 peripheral controller, the backplane lines have been reconfigured to reflect the M05 addressing scheme. Physically, the MTC interfaces to the MTD system through a 58-twisted-pair cable connected to the CPU backplane. The specific definition of MTD interface signals may be obtained from the Magnetic Tape Transport Field Service Manual. Backplane pin assignments are noted in the logic drawings in the field print package for the magnetic tape controller.

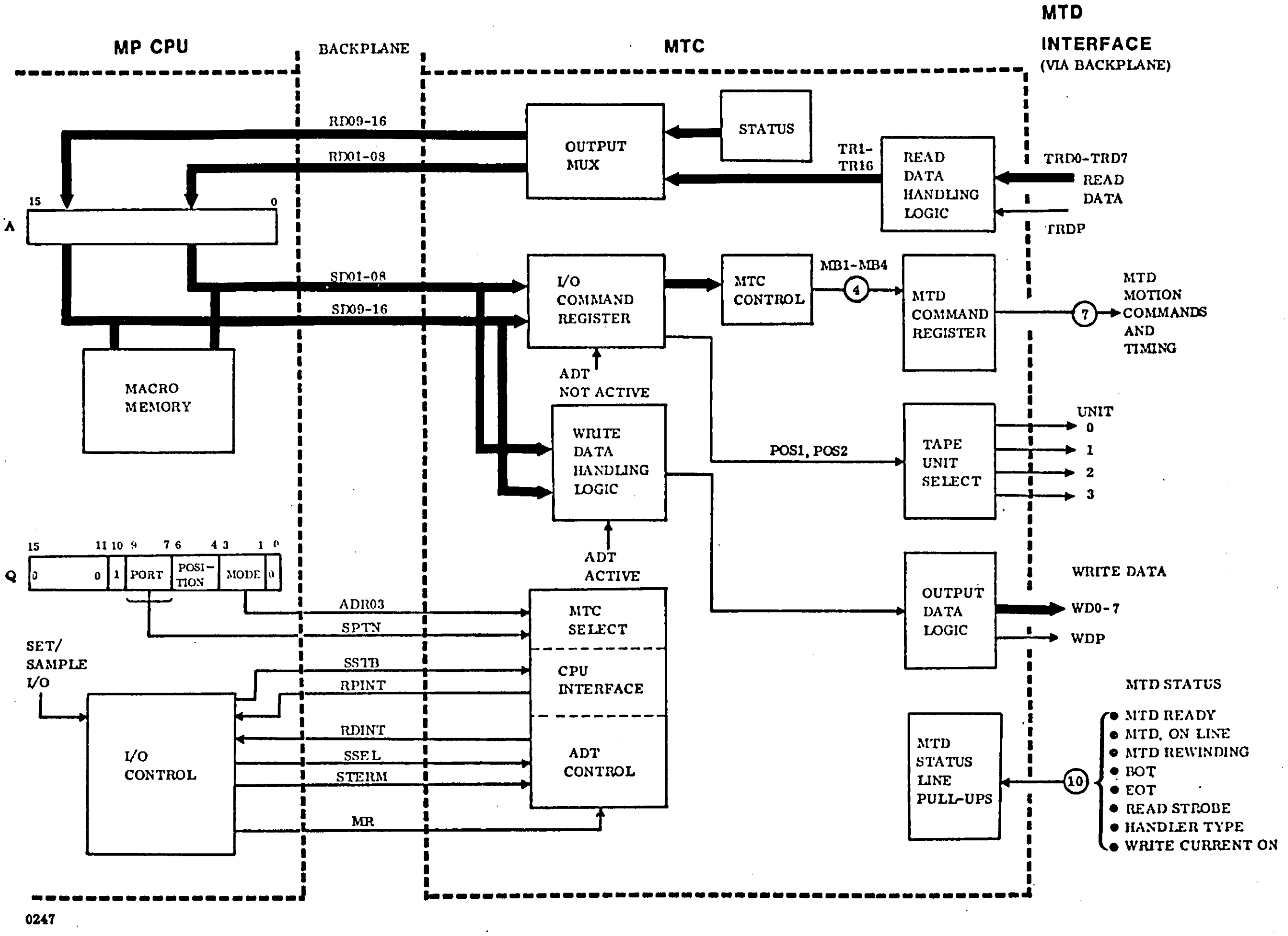


Figure 4-1. MTC Interface

TABLE 4-1. MTC/CPU INTERFACE SIGNALS

Signal	Function
RD01/- RD16/	Data input lines from the peripheral controller. In an ADT read operation, one 16-bit data word is input to the A register. The Q register selects the sending device. RD01/ - RD04/ are also used by the SPS command to sample (input) the status of an M05 device to the A register.
SD01/- SD16/	Data output lines to the peripheral controller. In an ADT write operation, one 16-bit data word is output from the A register to the external device. The Q register selects the receiving device.
SMB9/	This mode bit is always the set/sample condition bit. If it is 1 (i.e., 1700 Q03 = 1), one data word is set (output); if 0, one data word is sampled (input).
SSTB/	A strobe signal to the peripheral controller that occurs twice with each execution of an SIO command. The signal occurs once near the beginning and once near the end of an output data operation. Data out (SD01/ - SD16/) is guaranteed to be stable by strobe time.
SPT00- SPT07/	Port selection signal (discrete port address line). One of these 8 lines is made active with each execution of an SIO or SPS macro instruction. The particular line that goes active depends upon the code specified in bits 07, 08, and 09 (1700 convention) of the Q register. The appropriate line is custom-wired to the associated controller port at the time of installation.
SSEL0- SSEL7/	When the emulator detects and acknowledges the occurrence of a data interrupt (micro interrupt) for an ADT transfer, one of these eight lines goes active. The particular line that goes active depends upon the code specified in bits 7 - 9 of word 1 in the ADT table. This table is referenced by the occurence of the data interrupt. Word 1 of the referenced ADT table also tells the emulator what type of equipment (single or multiple M05, etc.) is involved. The association of a micro interrupt with a particular ADT table is initially set up at the macro level with the DMI macro instruction.
STERM/	When the emulator detects that the last data transfer of a current ADT operation is in progress, it causes this line to go active. This terminate line (which signifies the end of the ADT sequence) causes the controller to finish the current operation and to generate a macro (program) interrupt.
MR/	This signal is activated by a system master clear. It is furnished to clear the peripheral controller and external equipment.
RDINT/	Micro (data) interrupt line from the peripheral controller. This line signals the CPU that the device is ready for another data word transfer during ADT operation.
RPINT/	Macro (program) interrupt line from the peripheral controller. This line causes the macro program to branch to an interrupt trap location in macro memory. This facility allows peripherals to inform the macro program of peripheral occurences, such as initializing operations, terminations, malfunctions, or errors, and is used to permit macro control of the peripheral.
RDIR OUT	This line is used by the device to signal the direction of data flow, after the device receives the ADT micro interrupt acknowledge (SSEL0-SSEL7) from the CPU during an ADT operation.

INTERFACE COMMUNICATION

Communication between the CPU and the MTC are implemented using the NCR M05 I/O scheme; basically, I/O commands are still initiated using the A and Q registers, but the NCR macro set/sample I/O instructions are used in lieu of CDC's input/output A macros. There are also slight differences in the addressing of an I/O device and interface handshaking. The I/O philosophy for the M05 system is explained in detail in the 1700 Enhanced Processor with Core Memory Reference Manual. Figure 4-1 shows the A/Q register interface for initiating I/O commands to the MTC.

ADT WRITE MODE

Data transfers between the MTC and CPU are handled under auto-data transfer mode (ADT). The micro-processor CPU, upon receiving a micro interrupt (transparent to software), transfers the data in a fashion similar to A/Q I/O operations. For an MTD write operation, the micro-processor CPU's firmware program is directed through the MTC's micro interrupt to perform the following steps:

- Address the MTC via the Q register backplane lines.
- Fetch the 16-bit data word from memory and place it on the A-register backplane lines (SD1 through SD16).
- Toggle the appropriate I/O control lines to the MTC, indicating that data is available to it.
- Determine if this is the last data word to be transferred, and if so, assert the ADT terminate signal to the MTC (STERM).

ADT READ MODE

The ADT sequence is the same for an MTD read operation, except for the direction of data flow. Instead of fetching the data from memory, the ADT micro program in the CPU inputs the read data from the A-register backplane lines (RD1 through RD16). This data word is then placed in memory at the buffer address designated by the ADT table. For additional ADT information, refer to the 1700 Enhanced Processor reference manual.

DATA FLOW

CPU data that is to be written on the selected MTD is sent to the MTC's input data register and then output to the MTD via the output drivers. Read data from the selected MTD is input to the MTC read data in register and then passed to the CPU through the MTC's output multiplexer. This data flow is shown in figure 4-2, MTC Block Diagram.

WRITE DATA FLOW

Write data, upon entering the MTC, is split into two eight-bit bytes. The MTC then disassembles each byte into serial form for ease of control and logic packaging.

Each data bit processed is also sampled by the write check logic, where byte parity is weighed and assigned, and CRC check characters may be generated.

Each data byte is then reassembled into parallel form by the write data output register. A six- or eight-bit tape character with its parity bit is then presented to the MTC interface for writing.

READ DATA FLOW

Read data appears at the inputs to the MTC's read data in register as a six- or eight-bit byte with parity. The byte is serialized and reassembled by the read data output register for transfer to the CPU. The read data check logic also samples the serial bit stream, where individual byte parity and the CRC and LRC at the end of the record are checked.

The MTC's output multiplexer is enabled when two consecutive bytes have been processed by the MTC. The 16-bit data word is applied to the A register input backplane lines RD01 through RD16.

FUNCTIONAL DESCRIPTION

The MTC is comprised of the following major logic blocks:

- Write data registers and check/control logic
- Read data registers and check/control logic
- Master clock and MTD speed timers
- ROM and program address control
- CPU and MTD interface
- Program loop counters

MTC CONTROL

Within each of the major logic blocks there exist logic sub-blocks, such as registers, counters, and decoders. These sub-blocks interconnect through multiplexer and selector logic. By enabling individual multiplexers/selectors, the data and its path between MTC sub-blocks can be connected, disconnected, or altered. In this way, the data flow is directed through different active logic elements for a given operation.

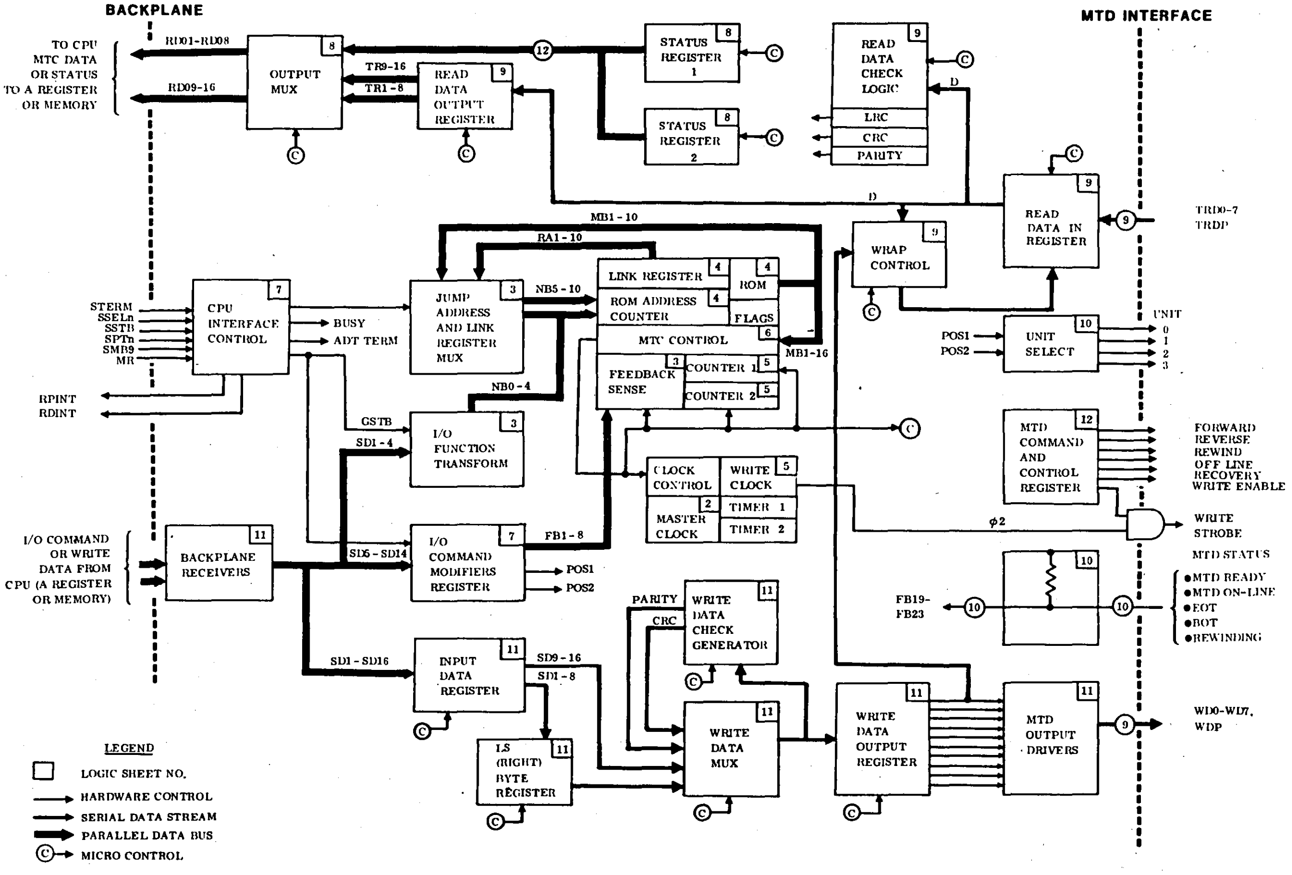


Figure 4-2. MTC Block Diagram

The selection of any data path is a function of the MTC control logic. This control is primarily an internally stored micro program that not only steers the read or write data bits from one sub-block to another, but manipulates that data as well. This is accomplished by steering the data through shift registers, inverters, or exclusive OR logic, which achieves the shift, complement, or combine functions.

This type of micro program is known as controlware, in that the processing logic does not have arithmetic/boolean capability, only control. The micro control program is composed of subprograms called micro routines, which in turn consist of anywhere from four to 20 micro instructions.

Each micro instruction is divided into segments known as fields. There may be three or four fields, depending upon the type of micro instruction. For some micro instructions, these fields are secondary micro functions, or subfunctions, in that each subfunction directly controls a logic sub-block. For other micro instructions, these fields are pure data, used as a constant by the micro instruction.

Each micro instruction resides at an assigned address within a read-only memory that has 1024 addresses/locations.

MTC control also contains the necessary hardware to decode the micro functions to lower level micro steps as well as implement them.

WRITE DATA LOGIC

Figure 4-3 shows the magnetic tape controller write data logic.

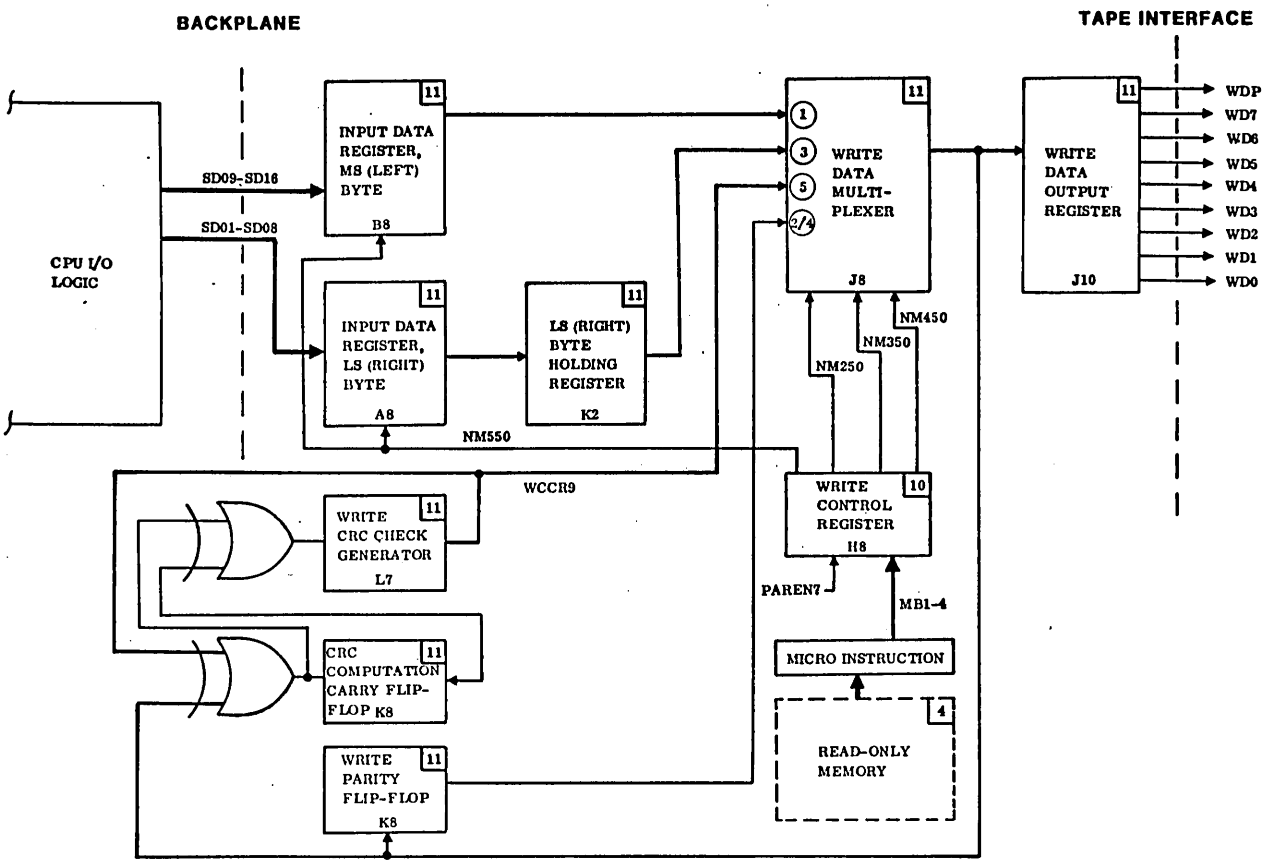


Figure 4-3. Write Data Logic

Input Data Registers (Left/Right Byte)

This register holds MTD write data from the CPU's SD backplane lines. It converts each eight-bit byte to eight-bit serial data. The two data bytes are latched into this register under control of a backplane strobe emanating from the CPU interface. Left-byte serial output is processed first, with the data being applied to the write data multiplexer.

At the same time that the left byte is being shifted under micro control through the multiplexer, the right byte is being shifted into the least significant (right) byte holding register.

LS Byte Holding Register

This register provides temporary storage for the right byte while the left byte is being processed. It also allows the input data registers to be emptied in one byte time period, making them available for loading with the next 16-bit data word from the CPU. The LS byte is serially output to the write data multiplexer.

Write Data Multiplexer

The write data multiplexer receives its inputs from the write data logic. It passes through to its output in the following sequence, serial data from:

- Input data register, MS (left) byte
- Write parity flip-flop (single bit)
- LS (right) byte holding register
- Write parity flip-flop
- Write CRC check generator

As each serial bit of data is output from the multiplexer, it is applied to the write data output register. It is also fed back to the write parity flip-flop for parity bit assignment on each byte, and sampled by the CRC computation logic, which uses it to create the CRC check character.

When the last byte of data has been written and only if a nine-track tape unit has been selected, the multiplexer selects the output of the write CRC generator and this character is passed through the multiplexer.

Write Data Output Register

This register assembles serial data from the multiplexer into seven- or nine-bit tape characters (including parity bit) for transmittal to the MTD.

CRC Generation

Each tape character output to a nine-track MTD is exclusive-ORed against the previous tape character that was written. The overflow or carry generated in creating the final CRC character is wrapped around and combined with the next data bit being written into the CRC generator.

Write Parity Flip-Flop

The parity flip-flop may be initially primed (set) where odd parity assignment is desired. Each data bit of a tape character is applied to this flip-flop. Every data bit to be written that is a 1 results in this flip-flop toggling to its opposite state. Its final state becomes the actual parity bit that is assigned to that data byte. After six or eight bits have been packed in the write data output register, the parity flip-flop's output is selected by the multiplexer and is used to drive the WDP (write data parity) line.

Write Control Register

Set by the micro control program, this register issues micro steps that control the loading or shifting of the input data registers and the input selection for the write data multiplexer. The sequence of selection is shown by the circled numbers in the multiplexer block in figure 4-3.

READ DATA LOGIC

The tape character, composed of seven or nine bits (including parity), is presented in parallel to the input of the MTC's read data in register. Refer to figure 4-4, Read Data Logic.

Read Data In Register

Under MTC micro control, this character is latched into the read data in register with its serialized output then fanning out to the read data handling logic.

Each data bit is shifted at the MTC's clock rate, out of the data in register, into the:

- LRC register
- CRC accumulator
- Read parity flip-flop

At the same time, this data is also shifted into its associated byte handling register.

MS (Left) Byte Assembly Register

The MS byte, which is the first character to be read from tape, is processed first unless the current I/O command specified that the first byte should be skipped.

This byte, appearing as a serial input, is converted back to parallel form by the MS byte assembly register. As each successive bit appears at the outputs of this register, it is automatically clocked into the read data output register.

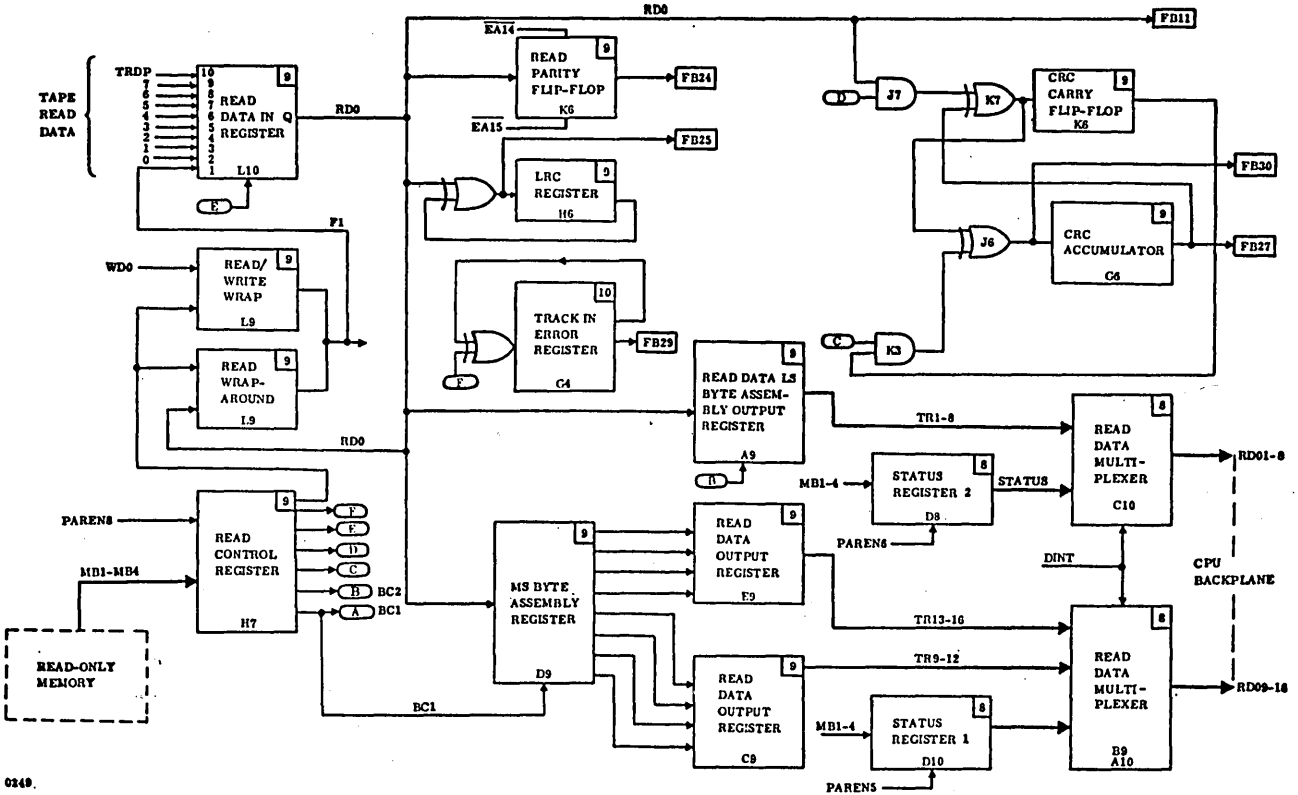


Figure 4-4. Read Data Logic

Read Data Output Register

This register is essentially a buffer that holds the full MS byte while the LS byte is being formed. It transmits its contents to the read data multiplexer under MTC micro control.

Byte Assembly Output Register

The second byte read from tape, and every other byte following, is shifted into this register under micro control. When both bytes have been packed in their respective registers, they are input to the read multiplexer for transmittal to the CPU.

Read Data Multiplexer

This multiplexer provides the ADT data path to the CPU's A register via the RD backplane lines. Data read from tape is combined into 16-bit words by the multiplexer and placed, under MTC micro control, onto the backplane lines.

The remaining half of the multiplexer receives its inputs from the MTC's status registers. Upon receipt of an I/O status request command, the multiplexer selects the status register as its input and outputs their contents onto the RD backplane lines.

Status Registers

Hardware and software conditions are sensed by the MTC micro control program by sampling feedback bits (refer to table 4-2). Upon detection of specific status-related feedback bits being true during MTC operations, micro control selectively sets the respective flag within the status register. These status flags are provided as inputs to the read data multiplexer for transmitting to the CPU during a status sample (SIO) command.

TABLE 4-2. FEEDBACK BITS

Select Code	Feedback Bit	Description	
0	FB0	Unconditional 1	
1	FB1	Skip first byte	From CPU's I/O command
2	FB2	Skip writing last byte	
3	FB3	Reserved for tape speed identifier	
4	FB4	Not used	
5	FB5	Density selection	
6	FB6		
7	FB7	Parity: 0 = odd; 1 = even	
8	FB8	Seven-/nine-track identifier	
9	FB9	Terminate B	
A	FB10	Program/data interrupt (PODINT)	
B	FB11	Read data bit	
C	FB12	Tape mark	
D	FB13	Write clock ϕ 2	
E	FB14	Short timer complete (=0)	
F	FB15	Long timer complete (=0)	
10	$\overline{\text{FB16}}$	Read data strobe (read clock)	From selected MTD
11	$\overline{\text{FB17}}$	Write current on (write status)	
12	$\overline{\text{FB18}}$	Write enable ring (file unprotected)	From selected MTD
13	$\overline{\text{FB19}}$	Ready	
14	$\overline{\text{FB20}}$	BOT (load point)	
15	$\overline{\text{FB21}}$	EOT	
16	$\overline{\text{FB22}}$	On line	
17	$\overline{\text{FB23}}$	Rewinding	
18	FB24	Read parity count flip-flop	
19	FB25	LRC test bit	
1A	FB26	Checksum bit	
1B	FB27	CRC test bit	
1C	FB28	Write current enable	
1D	FB29	Track in error bit	
1E	FB30	CRC check bit	
1F	FB31	Write data bit	
20	FB32	Density status (not used)	
21	FB33		
22	FB34	Not used	
23	FB35	Half word on read flag	
24	FN36	Micro program flag (flag 4)	
25	FB37	Write clock pulse memory latch	

Read Parity Flip-Flop

Read data (seven- or nine-bit) is clocked into this flip-flop during the byte packing time. Each data one bit is counted by this flip-flop, with its final state indicating an odd (set) or even (reset) amount of one bits received for that byte. Its output is sampled as a feedback bit for each byte's parity determination.

LRC Register

This register accumulates the exclusive ORing of all data read from tape. The final byte read from the tape record is the LRC character, which, when combined with this register's contents, should provide an all-zero result.

That result is verified by sampling the LRC output feedback bit.

CRC Logic

The cyclic redundancy check logic consists of a CRC checkword accumulator and a CRC carry/overflow flip-flop. Data read from tape is basically exclusive-ORed, bit for bit, against the previous byte read and then shifted. When unlike bits are combined, the CRC carry condition is set. To conform to the standard CRC algorithm, MTC micro control functions are asserted during the accumulation of the CRC partial sum. This allows for inverting the data bit being shifted into the CRC bit stream at specific stages of the CRC checkword makeup.

Read/Write Wrap-Around

Under MTC micro control, the read data in register is normally connected as a wrap-around (circular) shift register. This provides for testing through shifting and sampling of the current byte's bit configuration (such as tape mark characters) without destroying the original data.

The write-to-read wrap configuration is utilized for housecleaning functions (clearing registers) and maintenance test.

Read Control Register

Each of the read data registers and flip-flops previously mentioned has some form of external mode control or enabling inputs. Typically, a shift register would have a clock input line, a mode control line (shift, load, clear), and perhaps a shift direction (left/right) control line.

Relating this to the MTC read logic, the micro control program instructions contain subfunction codes. These codes are decoded and, in the case of a PAREN8 control code, the parameter information associated with it is loaded into the read control register. This in turn creates eight possible micro step control lines. One of these eight lines connects to one mode control/enable input of eight different read data logic elements (registers, flip-flops, etc.).

As each micro step control line is asserted true, it directly controls the function through the mode control logic of its particular read data logic element.

During a tape read operation, data is inverted and/or shifted through and directed to various registers and flip-flops by the particular micro steps set up for that phase of the operation.

CONTROL LOGIC

With the exception of the front-end CPU interface, the controlware (micro program) is the only active element within the MTC.

Program micro instruction subfunctions that are explained in detail in this section selectively switch the data flow into passive logic elements. These elements are then activated by the micro controls or steps set up by the program instruction.

To achieve this, the control section has its own logic elements that are directed in their functions by the micro instructions. They in turn control the read and write logic.

The MTC control logic is shown in the block diagram, figure 4-5.

MTC control is activated when its I/O interface logic recognizes that it is being selected through the mode and port addressing bits in the CPU's Q register.

The resulting I/O start signal, which is generated from the selection process, enables the I/O function code from the CPU's A register to be transformed to a controlware program address.

Transform

Upon receiving the I/O command from the CPU, the four-bit function code field (see section 2) of this command is applied to the transform logic. The remaining 10 bits are held in the I/O command register to be sampled as feedback bits by the controlware program. The transform logic applies this function code directly to the program address register as a four-bit read-only memory (ROM) address, in the range of 1 through D_{16}. When read out, this address contains a pointer micro instruction that, in reality, is a branch instruction to the starting ROM address of a micro routine.

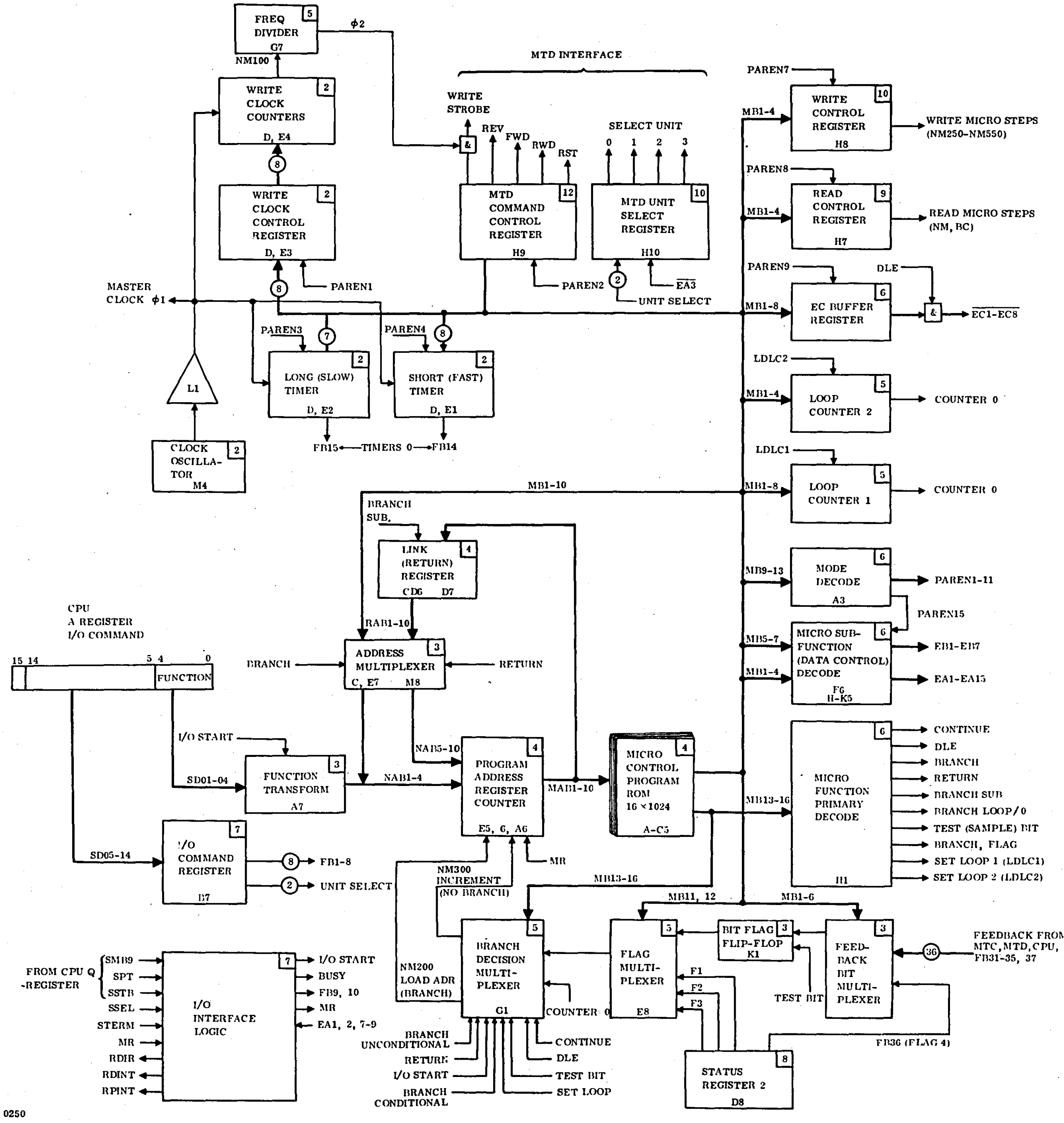


Figure 4-5. MTC Control Logic Block Diagram

Each I/O function has an associated micro routine that directs the MTC control logic to enable specific multiplexers and selectors, toggle interface lines, and process the data.

In this way, each I/O operation is performed through the execution of dedicated micro routines combined with several common routines. At completion of the I/O operation, the control program halts. It is triggered into running again by the next I/O command transform.

PROGRAM ADDRESS (RPA) REGISTER

The RPA register receives its initial start address from the transform logic. Thereafter, it is incremented by +1 as a counter for each sequential ROM address unless the following conditions occur:

- A branch format or a subroutine return micro instruction is fetched and executed. This causes a nonsequential 10-bit address to be loaded into the RPA via the NAB lines originating from the address multiplexer.
- An I/O master reset (MR) occurs that resets the RPA register to zero and terminates the current operation within the MTC.
- A micro halt (rest) instruction is encountered in the control program. The RPA register ceases incrementing, and its contents point to the next sequential ROM address following the halt instruction.

Read-Only Memory

The read-only memory contains 1024 addresses, with each address containing a 16-bit-wide micro instruction. It receives its inputs from the 10 memory address bit lines (MAB) of the RPA register and fetches the micro instruction residing at that address.

It then outputs the instruction onto the memory bit lines, where, as shown in figure 4-5, they are fanned out to all of the MTC's control logic.

MICRO INSTRUCTIONS

Each MTC instruction is a 16-bit word, divided into a four-bit primary function code field (MB13 through MB16) and up to three variable-length secondary fields. The secondary fields can be subfunctions of the primary function or immediate operand data used by the prime function to set or select a register. The secondary field may also be the next instruction address (branch address) to be referenced by the micro program.

Figure 4-6 illustrates the micro instruction fields.

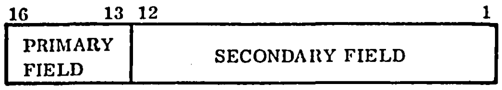


Figure 4-6. Micro Instruction Fields

There are three micro instruction formats in the MTC, branch format, register load format, and address/data control format.

Branch Format

The branch format allows the micro program to change its sequence by loading a program address other than the next sequential address into the ROM program address register/counter (RPA). This may be accomplished unconditionally; that is, the current micro instruction forces the loading of the new ROM address, or it may be done conditionally. A conditional branch or jump implies that some internal condition of the hardware had to first be sampled or tested. If the state of the specified hardware met the conditions being tested for, then the program branch would be executed. Otherwise, program execution would continue in sequence. Conditional tests that may be made in the MTC by branch micro instructions are:

- Selected register ≠ 0
- Specified flag flip-flops set or clear

Figure 4-7 illustrates the branch format.

Register Load Format

This format allows specific registers, counters, and flag flip-flops to be set to a desired state. The data used to load the registers or flags is contained in the secondary field area of the register load format micro instruction. Figure 4-8 illustrates the register load

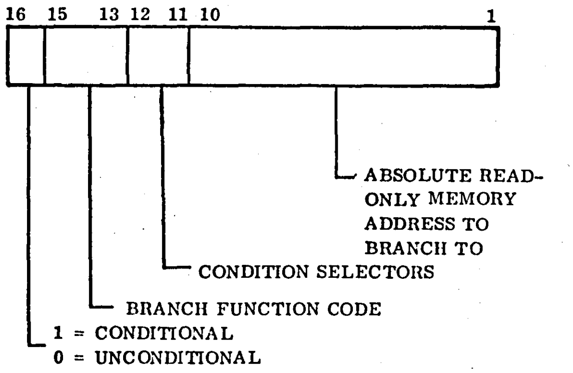


Figure 4-7. Branch Format

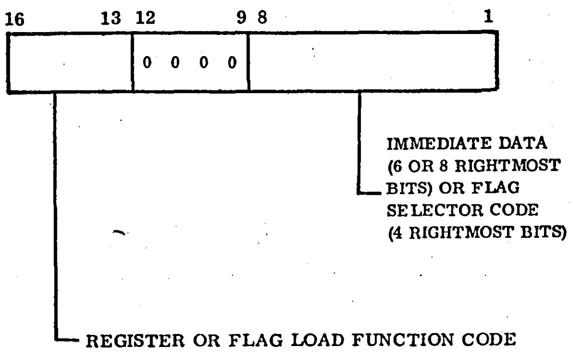

16
13
12
9
8
1
0 0 0 0
IMMEDIATE DATA (6 OR 8 RIGHTMOST BITS) OR FLAG SELECTOR CODE (4 RIGHTMOST BITS)
REGISTER OR FLAG LOAD FUNCTION CODE

Figure 4-8. Register Load Format

format. Note that the immediate data field length is variable due to the different types of register load operations.

These registers and flag flip-flops may be sampled as to their current state by the previously mentioned conditional branch micro instructions.

Address/Data Control Format

This format is a combination of the two previously mentioned formats. It provides the capability of changing the program flow through the primary function code. In addition, its secondary function fields allow for setting/clearing of registers, flip-flops, and logic states (A, B, and C logic) or presetting of registers (DD logic). The primary function code controls the stopping, starting, incrementing, and changing of the ROM program address register.

Within the same micro instruction the secondary function code fields enable or disable data paths in the MTC. This is accomplished by setting or clearing control logic used by the hardware in executing MTC/MTD operations. Figure 4-9 illustrates the address/data control format.

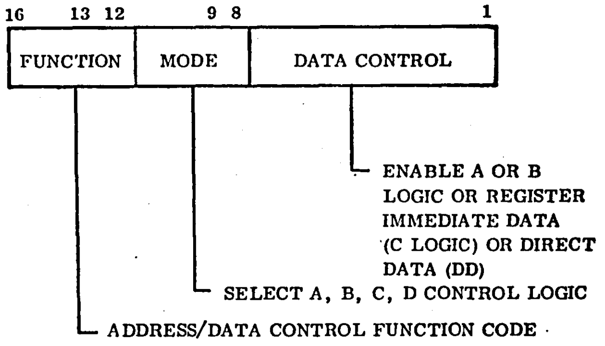

16
13
12
9
8
1
FUNCTION
MODE
DATA CONTROL
ENABLE A OR B LOGIC OR REGISTER IMMEDIATE DATA (C LOGIC) OR DIRECT DATA (DD)
SELECT A, B, C, D CONTROL LOGIC
ADDRESS/DATA CONTROL FUNCTION CODE

Figure 4-9. Address/Data Control Format

Mode Field

The mode field (MB9 through MB12) contains a 4-bit number in the range of 0 to F_{16}. This mode code selects and qualifies the data control field. Combining these two fields (mode and data control) actually equates to an MTC control subfunction. The mode field code, also known as PAREN0 through PAREN15, is basically decoded as follows:

Mode code = 0 — C data logic is enabled
1 - 14 — D data logic is selected
15 — Enable A and B (EA, EB) control logic

Data Control Field

The data control fields (EA, EB, EC, and DD) are used primarily for the following:

- EA selects data control latches and flip-flops to be set
- EB selects data registers and control latches to be cleared
- EC selects data registers to be shifted
- DD indicates data to be loaded into registers and counters, or the address of the register to be referenced. The mode field code further defines the operation to be performed with the referenced register.

MTC FUNCTION CODES

The MTC function codes are listed below in numerical order. The first four primary codes are explained with their associated secondary fields, followed by the remaining primary function codes.

Return to Rest

Format: Address/data
Function code: 0

16 15 14 13	12 9	8 1
0 0 0 0	MODE	DATA CONTROL

Halt. This command causes read-only memory access to stop at the completion of this micro instruction. Data control subfunctions are performed as defined by bits MB1 through MB12.

The MTC controlware program executes this instruction following completion of MTC I/O command operations.

Once halted, the micro program does not begin again until receipt of another I/O command.

The assembler mnemonic is REST.

The valid subfunctions are:

Mode	Data Control
PAREN1 - PAREN11 (1-B_{16})	DD
PAREN15 (F_{16})	EA, EB

Continue

Format: Address/data
Function code: 1

16 15 14 13	12 9	8 1
0 0 0 1	MODE	DATA CONTROL

NOP. The read-only memory program address (RPA) register is incremented by 1 at the completion of this micro instruction. Data control subfunctions are performed as defined by bits MB1 through MB12.

This micro instruction is used to allow the MTC controlware program to execute instructions in sequence.

The assembler mnemonic is CONT.

The valid subfunctions are:

Mode	Data Control
PAREN1 - PAREN11 (1-B_{16})	DD
PAREN15 (F_{16})	EA, EB

Subroutine Return

Format: Address/data
Function code: 2

16 15 14 13	12 9	8 1
0 0 1 0	MODE	DATA CONTROL

Exit from subroutine and return to the main program. Upon entering the subroutine, the contents of the RPA register are stored in the link register. Executing a SUBROUTINE RETURN instruction gates the current contents of the link register into the RPA register, allowing return to the main program.

Branching to another subroutine from the original (chaining) causes the original link contents to be lost.

Data control subfunctions are performed as defined by bits MB1 through MB12.

The assembler mnemonic is RETURN.

The valid subfunctions are:

Mode	Data Control
PAREN1 - PAREN11 (1-B_{16})	DD
PAREN15 (F_{16})	EA, EB

Data Logic Enable

Format: Address/data
Function code: 3

16	15	14	13	12 9	8 1
0	0	1	1	MODE	DATA CONTROL

This function enables the MTC's data handling registers for shifting. The particular register shifted are defined by the zero bits initially stored in the EC control register by a PAREN9 subfunction (reference PAREN Code 9). The registers enabled by their respective EC control bits are shifted or clocked once with each execution of this function.

Execution of a DLE micro instruction always implies the use of EC control bits. In addition, data control subfunctions are performed as defined by bits MB1 through MB12.

Use of this micro instruction with the EC control bits previously set by a PAREN9 subfunction allows the MTC to manipulate tape read or write data through its LRC, CRC, and data handling registers.

Following completion of this micro instruction, the RPA register is incremented to the next sequential address.

The assembler mnemonic is EC.

The valid subfunctions are:

Mode	Data Control
PAREN0	Zeros
PAREN1 - PAREN8	DD
PAREN10 - PAREN11 ($10\text{-}B_{16}$)	DD
PAREN15 (F_{16})	EA, EB

Data Control Subfunctions

The four-bit PAREN (mode) code may be a stand-alone operation for setting control flip-flops, or it may be combined with the data control field to select a register for:

- Receiving the lower-order bits (DD) from the current micro instruction, or
- Setting or clearing a particular register bit, as defined by a bit select code in the lower-order bits of the current micro instruction.

PAREN Code — Description

0000 (0) No data control operation. Generally used with data logic enable functions or for register load format.

0001 (1) Load the write clock control register from MB1 through MB8 of this micro instruction. This number represents a division integer in the range of 1 to 256, which shall be used to control the frequency of the tape write clock. The write clock divider divides the MTC clock by the positive integer selected, and provides a basic write clock frequency. The actual phase 2 write clock generated to the MTD is one-fourth the result of this division.

0010 (2) Select the MTD command/control register. MB1 through MB3 in this micro instruction contain the function select code for the MTD:

0 (000) — Forward

1 (001) — Reverse

2 (010) — Rewind

3 (011) — Off-line

4 (100) — Read recover

5 (101) — Write reset (write LRC character)

6 (110) — Write strobe (enable phase 2 write clock)

7 (111) — Write enable

MB4 sets or clears the selected MTC function.

0011 (3) Load and start long (slow) timer. MB2 through MB8, representing any positive integer greater than 1 and up to 256, are loaded into the long timer, which then begins incrementing this number at a 5 kHz rate until an all-ones count is reached. The next increment results in overflow, which sets feedback (FB) status bit 15 (long timer complete).

0100 (4) Load and start short (fast) timer. Similar to PAREN3 except the short timer increments at a 400 kHz rate, with overflow sensed by short timer complete status FB14.

PAREN Code — Description

0101 (5) Load status register 1. MB1 through MB3 select one of eight status bits, while MB4 sets or clears the selected bit.

0 (000) — Tape mark sensed

1 (001) — Data error

2 (010) — Inoperative while executing

3 (011) — System overload (lost data)

4 (100) — Data dropout/pickup

5 (101) — Timed out

6 (110) — Short record

7 (111) — Half word on read

0110 (6) Load flag and status register 2. Same as status register 1.

0 (000) — Program flag (F1)

1 (001) — Program flag (F2)

2 (010) — Program flag (F3)

3 (011) — Micro flag (FB36)

4 (100) — Inoperative at selection time

5 (101) — Write lockout

6 (110) — Unit rewind

7 (111) — Macro program error

0111 (7) Load write data control register. MB1 through MB4 are loaded into this register and control the data sent to the MTD. MB1 through MB3 select one of eight sources of serial data to be loaded into the write data output register and sent to the tape unit. The source selection is:

0 (000) — Logical zero

1 (001) — Write parity flip-flop

2 (101) — Write CRC generator

3 (011) — Write CRC generator (complement)

4 (100) — First data byte (MS)

5 (101) — Second data byte (LS)

6 (110) }
7 (111) } Logical one

MB4 when true sets the MTC's input data register from load mode to serial shift mode.

1000 (8) Load read data control register. MB1 through MB3 select one of eight logic enables for a tape read operation. MB4 is used to set the selected logic enable to a true or false state.

	MB1 - MB4	Micro Operation
	0 (000) • MB4=1/0	Enable/disable read data output register to assemble least significant (right) data byte (BC1).
	1 (001) • MB4=1/0	Enable/disable most sigficant (left) byte assembly by the read data output register (BC2).
	2 (010) • MB4=1	Enable inverting the serial tape read data bit input to the LRC and read data output registers.
	MB4=0	Gate the serial tape read data bit input to the LRC and read data output registers.
1000 (8)	3 (011) • MB4=0	Enable loading the read data in register.
	MB4=1	Enable shift mode on the read data in register (see PAREN code A).
	4 (100) • MB4=1/0	Enable/disable the CRC computation exclusive OR result (CRC carry) to the CRC accumulator.
	5 (101) • MB4=1	Enable tape read data bits to the CRC computation logic.
	MB4=0	Enable CRC accumulator output to CRC carry flip-flop.
	6 (110) • MB4=1	Set track in error register input to a logical 1.
	MB4=0	Enable track in error register wrap-around.

PAREN Code	Description	
	MB1 - MB4	Micro Operation
	7 (111) • MB4=1	Connect bit output of write data output register into input of read data in register.
	MB4=0	Enable end-around shift on read data in register.

1001 (9) Load EC control register directly from bits MB1 through MB8 of this micro instruction. When zero, these EC bits are combined with a data logic enable micro instruction and allow the following logic conditions to be clock controlled:

$\overline{\text{EC/MB1}}$	Enable clocking the MTC's write data parity flip-flop, the LS byte holding register, and the input data register for shifting parallel CPU data bytes to serial data.
$\overline{\text{EC/MB2}}$	Enable shifting the track in error register one bit position.
$\overline{\text{EC/MB3}}$	Enable shifting the write data output register one bit position.
$\overline{\text{EC/MB4}}$	Enable shifting the write CRC generator one bit position.
$\overline{\text{EC/MB5}}$	Enable shifting the read data in register one bit position and clock the read data parity flip-flop. Also enable shifting of the LS and MS byte assembly in the read data output registers.
$\overline{\text{EC/MB6}}$	Enable shifting the LRC register one bit position.
$\overline{\text{EC/MB7}}$	Invert the serial read data input to the read CRC accumulator.
$\overline{\text{EC/MB8}}$	Enable shifting the read CRC accumulator one bit position.

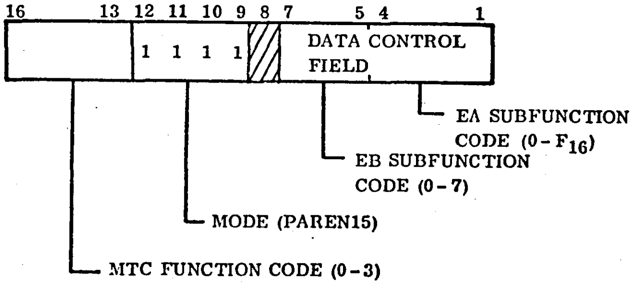
1010 (A_{16}) Controls the clearing, loading, and shifting of the MTD read data in register, in conjunction with PAREN code 8 and MB1 through MB3 equal to 3.

1011 (B_{16}) Sets the read (command received) after write (command completed) status flip-flop (RAWS).

PAREN Code	Description
1100 - 1110 (C-E_{16})	Not used; no operation performed on hardware.
1111 (F_{16})	Enable EA/EB selection according to MB1 through MB8.

EA Bit Assignments

The EA field occupies bits MB1 through MB4 in the MTC micro instruction and selects one of 16 possible EA micro subfunctions for the MTC control logic. Enabled by an F_{16} code in the mode/PAREN field of the micro instruction, the EA codes are used primarily to set control flip-flops and latches.



EA Code	EA Subfunction Description
EA0	Not used. No operation performed by hardware.
EA1	Resets the data direction flip-flop, indicating to CPU's I/O control logic that the direction of ADT data will be from the CPU to the MTC.
EA2	Clear ADT terminate. Resets the TERM B flip-flop that was set by the CPU's terminate signal (STERM).
EA3	Enable tape select. Enables the selection of one of four tape units.
EA4	Not used
EA5	Gates CRC carry. Enables write CRC carry flip-flop output to the write CRC generator.
EA6	TR9-TR16 enable. Enables the output of the MS byte of the read data output register to the input of the output multiplexer.

EA Code	EA Subfunction Description
EA7	See EA1. Sets the data direction flip-flop to notify the CPU via backplane signal RDIROUT that the direction of data flow for this ADT operation is MTC to CPU.
EA8	Program interrupt. Sets the program interrupt latch.
EA9	ADT interrupt. Sets the auto-data transfer (micro) interrupt.
EA10	Write odd parity. Primes the write parity flip-flop so that odd data parity is generated.
EA11	Write even parity. Primes the write parity flip-flop so that even parity is generated.
EA12	Clear write CRC. Zeros the write CRC generator.
EA13	Clear tape data output. Zeros the write data output register.
EA14	Read odd parity. Primes the read parity flip-flop to test for odd parity.
EA15	Read even parity. Primes the read parity flip-flop to test for even parity.

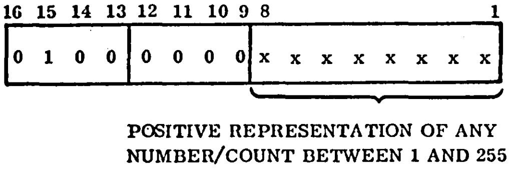
EB Bit Assignments

The EB subfunction field is decoded from bits MB5 through MB7. It is used primarily for clearing control latches in the MTC.

EB Code	EB Subfunction Description
EB0	Not used
EB1	Read registers. Clears the MTC read and unit select registers.
EB2	Command register. Clears the tape command/control register.
EB3	TIE register. Clears the track in error register.
EB4	Read data strobe. Resets RDS (FB16).
EB5	CRC read carry. Stores the read carry bit when calculating the read CRC.
EB6	CRC write carry. Stores the CRC write carry bit.
EB7	Clear FB37. Resets the write clock pulse memory flip-flop.

Set Loop Counter 1

Format: Register load
Function code: 4



16	15	14	13	12	11	10	9	8							1
0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x

POSITIVE REPRESENTATION OF ANY NUMBER/COUNT BETWEEN 1 AND 255

Bits MB1 through MB8 are loaded into loop counter 1, with bit 1 the least significant bit. This 8-bit counter is decremented by 1 and tested for zero by the branch loop 1 ≠ 0 micro instruction. This command is used by the program to set up shift iterations for the data handling register and preset pass counts of control operations as well as any other repetitive control operation that requires counting.

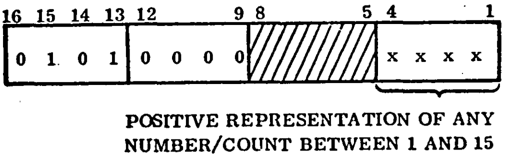
Following completion of this micro instruction, the RPA register is incremented to the next sequential address.

The assembler mnemonic is LDLC1.

There are no valid subfunctions.

Set Loop Counter 2

Format: Register load
Function code: 5



16	15	14	13	12			9	8			5	4			1
0	1	0	1	0	0	0	0	▨	▨	▨	▨	x	x	x	x

POSITIVE REPRESENTATION OF ANY NUMBER/COUNT BETWEEN 1 AND 15

Bits MB1 through MB4 are loaded into loop counter 2 with bit 1 the least significant bit. This four-bit counter is decremented by 1 and tested for zero by the branch loop 2 ≠ 0 micro instruction. This command is used by the program to set up shift or control iterations.

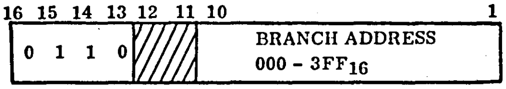
Following completion of this micro instruction, the RPA register is incremented to the next sequential address.

The assembler mnemonic is LDLC2.

There are no valid subfunctions.

Unconditional Branch

Format: Branch
Function code: 6



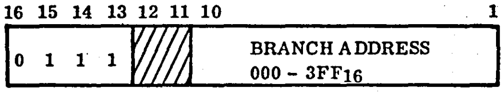
Branch to the read-only memory address specified by MB1 through MB10 and execute the micro instruction at that address. Load the RPA register with bits MB1 through MB10.

The assembler mnemonic is BRANCH.

There are no valid subfunctions.

Branch to Subroutine

Format: Branch, unconditional
Function code: 7



Branch to the read-only memory address specified by MB1 through MB10 and execute the micro instruction at that address. Save return.

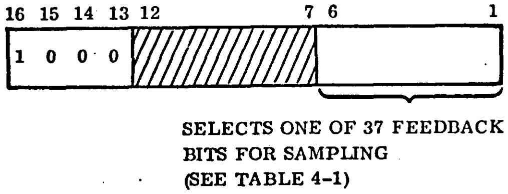
Transfer the current contents of the RPA register + 1 to the link/return register (save return). Then load the RPA register with bits MB01 through MB10.

The assembler mnemonic is JUMP.

There are no valid subfunctions.

Sample/Test Bit

Format: Register load
Function code: 8



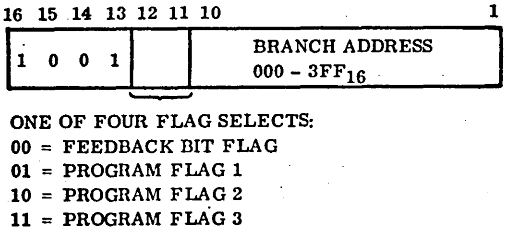
Input the state of the feedback bit as selected by MB1 through MB6 to the bit flag flip-flop. The feedback bits reflect internal MTC hardware status, MTD interface lines, CPU control/command signals, and software status. Sampling of an individual feedback bit sets or does not set the bit flag flip-flop. This bit flag's state may then be tested by the branch, flag on/off micro instructions. Following completion of a sample bit micro instruction, the next sequential instruction is executed.

The assembler mnemonic is TEST B.

There are no valid subfunctions.

Branch, Flag Off

Format: Branch, conditional
Function code: 9



Branch to the read-only memory address specified by MB1 through MB10 if the selected flag is not set. If the selected flag is set, execute the next sequential micro instruction.

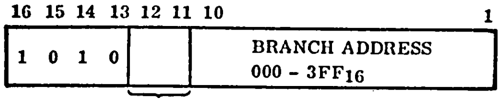
Flags 1, 2, and 3 are set by PAREN6.

The assembler mnemonic is BRNB.

There are no valid subfunctions.

Branch, Flag On

Format: Branch, conditional
Function code: A



ONE OF FOUR FLAG SELECTS:
00 = FEEDBACK BIT FLAG
01 = PROGRAM FLAG 1
10 = PROGRAM FLAG 2
11 = PROGRAM FLAG 3

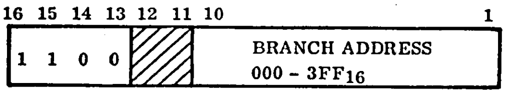
Branch to the read-only memory address specified by MB1 through MB10 if the selected flag is set. If the selected flag is zero, execute the next sequential micro instruction.

The assembler mnemonic is BRB.

There are no valid subfunctions.

Branch Loop 1≠0

Format: Branch, conditional
Function code: C



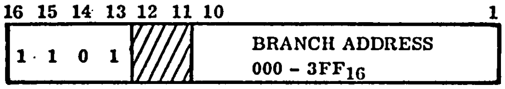
Decrement the loop 1 counter by 1. If the counter is not equal to zero, branch to the read-only memory address specified by MB1 through MB10. If the counter is equal to zero, execute the next sequential micro instruction.

The assembler mnemonic is LOOP1.

There are no valid subfunctions.

Branch Loop 2≠0

Format: Branch, conditional
Function code: D



Decrement the loop 2 counter by 1. If the counter is not equal to zero, branch to the read-only memory address specified by MB1 through MB10. If the counter equals zero, execute the next sequential micro instruction.

The assembler mnemonic is LOOP2.

There are no valid subfunctions.

Unused Micro Function Codes

The primary function codes E and F_{16} are not used. The following secondary subfunction codes are not used:

- PAREN12, PAREN13, PAREN14 (C, D, E_{16})
- EA0, EA4
- EB0

Feedback Bits

Feedback bits are essentially feedback from the MTC and MTD logic. They reflect the current state of control lines and latches as well as the bit level of read or write data and check characters (LRC, CRC, parity) within the MTC. Each individual feedback bit may be selected for test (sample bit) and tested (branch bit, flag on/off) as to its current state by the control program. Table 4-2 lists these bits in numerical order, followed by a functional description of the feedback functions.

The micro control program uses the feedback bits to guide it in its selection of the proper logic elements during an I/O operation. An example of this would be in the initial I/O command setup for an MTD read operation. Backplane line SD11, when true, equates to A-register bit 10 in the I/O command. If this bit is set, the MTC is requested to read tape data and test for even parity on each data byte. The I/O command register latches on SD11 and makes it available to the micro program for testing as FB7. As each byte of data is processed by the MTC program, it samples the state of FB24, the read data parity flip-flop. If this feedback bit were false at the end of a byte transfer, it would indicate an odd parity for the last byte. The micro program, after sensing this case, would test FB7 and confirm that all data should have had even parity. Since this indicates an error condition, the micro program must flag this to the software program. Referencing PAREN code 5, the reader will note that the micro control program can set the data error flag in status register 1. At the end of the MTD read operation, the software will indeed find that status bit set for the example given here.

FB Bit — Feedback Function Description

I/O Command Bits from the CPU:

FB1 Skip first byte. Reflects state of CPU A-register bit 04 in the MTC I/O command. When set during an MTC read operation, causes zeros to be placed in most significant byte and first character from tape in least significant byte of 16-bit word sent to CPU. For MTC write operations, the most significant byte of the CPU data is skipped and the least significant byte is recorded as the first tape character.

FB2 Skip last byte. Skips writing the last data byte (least significant) of last word on tape. Equates to A-register bit 05. Ignored for MTC read operations.

FB3 Tape speed. Identifies speed of transport being used. Not currently implemented

FB4 Null character insert. Not used

FB5, FB6 Density identifer. Reflects A-register bits 08 and 09 in CPU's I/O command to MTC. Identifies read or write density of selected unit as follows:

FB5	FB6	
0	0	1600 bpi, nine-track (not currently supported)
0	1	800 bpi, nine-track or seven-track
1	0	556 bpi, seven-track
1	1	200 bpi, seven-track

FB7 Parity assignment. Reflects A-register bit 10. Identifies parity to be assigned/checked on the current data operation. Set for even parity, false for odd parity (nine-track).

FB8 Track identifier. Reflects A-register bit 11. Identifies number of tracks on selected MTD. True for seven-track, false for nine-track unit.

MTD Interface Feedback:

$\overline{\text{FB16}}$ RDS, read data strobe. When false, indicates to MTC that its read data register has received a character of data from the MTD's read circuitry. Also known as read clock.

$\overline{\text{FB17}}$ Write current on. When false, the write current is active in the selected MTD.

$\overline{\text{FB18}}$ Write enable ring. When false, write operations are enabled in the selected MTD.

$\overline{\text{FB19}}$ Ready. When false, selected MTD is loaded with tape, powered up, and ready to accept an I/O command.

$\overline{\text{FB20}}$ BOT. When false, selected MTD is positioned at beginning of tape or load point (reflective strip under photo cell).

$\overline{\text{FB21}}$ EOT. When false, the selected MTD has run out to end of tape. This feedback bit is also used to set software status bit A15.

$\overline{\text{FB22}}$ On-line. The selected MTD transport is busy in a motion forward/backward but not rewinding condition. When this line is false, it equates to the busy status bit, A01.

$\overline{\text{FB23}}$ Rewinding. False when the selected MTD is rewinding. Equates to A-register bit 02 when MTC status is requested.

FB32 through FB34 Transport density status. Three identifying lines from the selected MTD.

MTC Data Handling:

FB11 Read data bit. Serial bit output of 8-bit byte in the MTC's read data register.

FB24 Read parity. When true, indicates the reset state of the MTC's read parity flip-flop.

FB Bit	Feedback Function Description
FB30	CRC check bit. State of bit currently being applied to MTC's CRC accumulator.
FB27	CRC test bit. Serial output of CRC accumulator.
FB31	Write data bit. Serial bit (data/parity/CRC) output from the MTC's write data multiplexer to the MTD.
FB25	LRC bit. Serial bit output from the MTC's read LRC register.
FB29	Track in error. Serial bit output from the MTC's track-in-error register.
FB26	Checksum. When set, indicates a mismatch in the exclusive OR compare of the read CRC accumulator and write CRC generator serial bit outputs.

MTC Control:

FB Bit	Feedback Function Description
FB12	Tape mark. Set by the MTC control program upon detecting that the last character read from the MTD was a tape mark. Also sets A-register bit 14 during a software status request.
FB13	Write clock phase 2. The output from the write clock counter in the MTC. Indicates to the MTC control program that a data character may be output to the selected MTD when FB13 is true.
FB37	Write clock memory. When true, indicates the set condition of a flip-flop that captures every write clock phase 2.
FB14	Short timer complete. Indicates to the MTC control program that the count/time that was preset in the short timer by a PAREN4 subfunction has decremented to zero.
FB15	Long timer complete. Long timer count, set by PAREN3, has decremented to zero.
FB28	Write current enable. Indicates to the MTC that a write operation is currently enabled on the selected MTD.
FB36	Micro flag. Similar to flags 1 through 3. Internal bit flag that may be set or cleared and tested. Also known as flag 4.
FB09	Terminate B. Set by the CPU's auto data transfer terminate control line. Indicates to the MTC that the current data transfer operation is complete. May be reset by executing subfunction code EA2.
FB10	PODINT. Program or data interrupt generated by the MTC to the CPU. PODINT/FB10 stays true until the interrupt is answered by the CPU.
FB35	Half word read. Sets bit A07 in the status word when MTC detects an odd number of bytes sent to the CPU.

MICRO INSTRUCTION DECODE

The output of the MTC program read-only memory is divided into two paths. The primary field, or micro function code, occupies bits 13 through 16 of the 16-bit micro instruction. The secondary field, consisting of bits MB1 through MB12, is applied to the mode and data control decoders.

Primary Micro Function Decode

Of the 13 possible micro functions, this decoder only translates for 12 functions. Function code 9, branch, flag off, is decoded within the branch decision multiplexer. Function codes B, E, and F are not used and execution of these OP codes results in an NOP within the MTC.

Mode Decode

This decoder generates a PAREN signal, based on bits MB9 through MB12 of each micro instruction executed. The output signals PAREN1 through PAREN11 enable the micro controls used by the read and write data logic when processing data. The PAREN15 output enables the selection of the data control subfunction outputs EA and EB.

EB Subfunction Decode

Micro instruction bits MB5 through MB7 are decoded by this logic and generate one of seven EB subfunction codes. The decode is only enabled when the mode decode logic detects a PAREN15 and the inputs to the EB decode are nonzero. Only one EB output may be active during a micro instruction and has to have been selected by that micro instruction. The selected EB subfunctions are used primarily to clear the MTC registers.

EA Subfunction Decode

Micro instruction bits MB1 through MB4 are decoded to select one of 15 possible EA subfunctions. Enabled and selected exactly the same as the EB subfunctions, the EA codes are used primarily for setting data control flip-flops and latches in the MTC.

EC Buffer Register

This register contains eight addressable latches that are individually set or reset by bits MB1 through MB8 during a PAREN9 code. The EC outputs, when low, control the shift controls of the read and write data handling registers and are activated by the data logic enable micro instruction.

PROGRAM CONTROL LOGIC

Several logic elements are covered under this category. Those elements that fall under the control category directly affect the program flow and sequencing. Further on in this section, the program auxiliary logic is covered. That logic is considered as auxiliary in that it does not affect the data flow and only affects the program flow when the program logic desires it. The control category consists of the following (see figure 4-5):

- Status register 2
- Feedback bit multiplexer
- Bit flag flip-flop
- Flag multiplexer
- Branch decision multiplexer

Status Register 2

There are four bits of interest in this eight-bit status register: micro program flags F1, F2, F3, and micro flag 4 (FB36). Set or cleared by the control program, they denote the type of data operation (read or write) currently active in the MTC. They are also used to capture the occurrence of pulse-type signals from the MTD interface (read data strobe — RDS) as well as any other conditions that must be remembered for use later by the micro-control program.

Feedback Multiplexer

Receiving inputs from the MTD interface (status), CPU interface (control signals), and the internal logic of the MTC itself (data, parity, and data correction registers), the feedback multiplexer provides feedback from the logic. One of 38 possible inputs is selected through the feedback multiplexer, based on the bit configuration of bits MB1-6. This allows for testing the logic state of any feedback by the micro program (see table 4-2).

Bit Flag Flip-Flop

Clocked by the test/sample bit micro instruction, this flip-flop latches to the logic state of the currently selected feedback bit. It provides, by its output, a bit (B) flag to the program flag multiplexer.

Flag Multiplexer

One of the four program flags, F1 through F4, or the last feedback bit sampled in the bit flag flip-flop is selected by bits MB11 and MB12 of the branch, flag on/off micro instruction. The output of the flag multiplexer is also enabled to the branch decision logic by the same micro instruction.

Branch Decision Multiplexer

This logic element generates one of two logic signals for each micro instruction executed. The increment signal (NM300) to the read-only memory program address register (RPA) is created when any of the following input conditions to this multiplexer exist:

1. A non-branch micro function is fetched from the read-only memory (DLE, CONT, TESTB, etc.)
2. The logic state of a feedback bit or program flag was not the state or condition being tested for. This results in a no-branch condition.
3. The loop counter specified by the current test loop and branch micro instruction contains zero.

The increment signal to the RPA causes the next sequential micro instruction to be fetched and executed.

The branch decision multiplexer samples the primary micro function code via MB13 through MB16. When bit MB16 is true, a conditional branch function is implied. Based on MB13 through MB15, one of four possible conditions that can be tested by a branch function is selected through the multiplexer. The multiplexer output signal, load branch address (NM200), is sent to the RPA if any one of the following conditions is met:

- The micro instruction fetched from the read-only memory is an unconditional branch.
- The selected loop counter is nonzero and it is being tested by a branch, loop counter = nonzero micro instruction.
- A branch on flag micro instruction specifies a micro program flag that meets the tested-for condition (flag on/off).
- The bit flag's state meets the condition being tested for.
- The current micro instruction is a subroutine return or branch subroutine.
- A CPU I/O command has just been latched up in the MTC (transform operation).

The address field of the current branch micro instruction, MB1 through MB10, is applied through the address multiplexer and appears on the input to the RPA register as the next address bits (NAB1-NAB10). Loaded into the RPA by the load address (NM200) signal from the branch decision multiplexer, the micro instruction at that address is fetched next and executed.

Link Register

The link register saves the address of the next sequential micro instruction following a branch subroutine instruction. In effect, this saves the main program address that is returned to following execution of a micro subroutine. As illustrated in figure 4-5, if the current micro instruction is a branch subroutine type, the loading of the RPA register's MAB1 through MAB10 bits into the link register is enabled. These bits represent the next address in the main program following the branch subroutine instruction. Through this action, the return address has been saved.

Bits MB1 through MB10, which are the read-only memory address of the subroutine being branched to, are loaded through the address multiplexer and into the RPA register. A read-only memory (ROM) fetch cycle is initiated and the first micro instruction of the subroutine is executed.

At completion of the subroutine operation, the final micro instruction exits from the subroutine back to the main program. This exit instruction is known as a subroutine return; it enables the contents of the link register to be loaded into the RPA register. At the next ROM fetch cycle, the micro instruction executed is the one following the branch subroutine instruction in the main program.

PROGRAM AUXILIARY LOGIC

The auxiliary logic elements are the loop counters, the track-in-error register, and the MTD speed timers. These digital timers are known as the long (slow) timer and short (fast) timer in the MTC.

Long Timer

The long timer is preset to a count representing a time range of from 500 microseconds to 64 milliseconds. This count is loaded into the long timer by a PAREN3 code and direct data bits MB2 through MB8. Upon being loaded, the counter is incremented at a 250-microsecond rate by the MTC master clock, until an overflow condition is reached. When this occurs, its output (feedback bit 15) goes true, indicating long timer complete. This bit, FB15, may then be sampled by the program, indicating that the preset time period has elapsed. The MTC micro program uses the long timer to time the tape drive's BOT/load point delay on read and write operations, as well as other MTD delays.

Short Timer

The short timer is preset by MB1 through MB8 and a PAREN4 code. Its count represents a time period of 2.5 microseconds to 640 microseconds with an increment rate of 2.5 microseconds (400 kHz). Its overflow condition (short timer complete) drives feedback bit 14. One of its applications, as used by the micro program, is to time the proper occurrence of read clocks (read data strobe) from the MTDs, relative to their assigned density.

Loop Counters

Two counters are used in the MTC for tracking the micro program through various instruction loops or counting data shift operations. Loop counter 1 is an eight-bit counter, loaded by the LDLC1 micro instruction from MB1 through MB8. It is incremented by 1 towards positive zero with every execution of a branch, loop 1≠ zero micro instruction. Its true output (ZERO 1) disables the branch decision logic, allowing the next micro instruction following the branch to be executed. Since it can track up to 256 iterations of a micro operation, it is used throughout the control program.

Similar to loop counter 1, loop counter 2 can only be set to a maximum count of 16 by its LDLC2 micro instruction. It is used primarily for counting the shift operations when packing and unpacking the data bytes in the MTC.

Track In Error Registers

The TIE register is a working register used by the micro program for error correction on nine-track read operations. Read data is not routed through this register nor is it activated except upon data error detection by the control program. Under micro control, any one of its 10 bits may be set to a one. This is done to mark the tape track in error. Its output is then used to invert (correct) the current data bit being processed by the error correction micro routine.

MTD INTERFACE REGISTERS

Upon receiving an I/O command from the CPU, the transforming of the I/O function code, consisting of A register bits 0 through 3, directs the MTC control to a dedicated micro routine for that I/O function. Each micro routine shares a common MTD select subroutine, where the specified tape unit is selected. Following MTD selection, the appropriate MTD command is output to the selected MTD.

Unit Select Register

Bits 9 and 10 of the MTC's I/O command reflect the MTD unit number to be selected. These two bits equate to the CPU's A register bits 12 and 13 that were output during the I/O command. When applied to the MTC's unit select register, they enable selecting one of the four possible tape units connected to the MTC. Upon application of subfunction EA3, one of the MTD select lines (0 through 3) then goes true. The clearing of all select lines is also a function of micro control in that subfunction EB1 clears this register.

MTD Command Control Register

The application of any command to the selected tape unit is performed by the micro routine associated with that operation. For both a read or a write function, the forward (FWD) line to the MTD interface is asserted. Micro code PAREN2 and instruction bits MB1 through 4 = 8 would perform this function by setting the Q0 latch in this register. If the current function was a write, PAREN2 would again address this register, this time setting the write current enable and write strobe (Q7 and Q6) latches in this register.

This register drives eight lines to the MTD interface. Their names and associated operations are as follows:

- Forward — Read, write, erase, and write tape mark
- Reverse — Backspace and controlled backspace
- Rewind — Return to load point (BOT)
- Offline — Rewind and go offline
- Recovery Read — Programmable threshold
- Write Reset — Write LRC
- Write Strobe — Write data clock
- Write Current Enable — Write/set write

This register is cleared to zero by micro subfunction EB2.

MTC TIMING

The timing circuitry of the MTC covers two logic areas: internal timing for instruction execution and data shifting. These timed operations are controlled by the MTC clock.

The other area of timing is MTD interface timing. The actual recording of data on tape is governed by the write clock. Based on the bit-packing density of the particular unit in use (NRZI; 800 bpi, 9-track; 800, 556, and 200 bpi, 7-track) the frequency of the write clock must be programmable. This variable timing is controlled and generated in the write clock logic.

MTC Clock

The clock consists of an 8-MHz crystal oscillator that drives a phase splitter flip-flop. The outputs of the splitter circuit are one active high and one active low 4 MHz clock signal (MC-1).

The active high clock signal steps the RPA register (counter) through the instruction addresses. This sets the timing of each micro instruction cycle (fetch/execute) at the master clock rate of 250 nanoseconds. The active low clock signal clocks the data handling shift registers. As the contents of the RPA register are changed by the high clock signal, the micro instruction at that address is fetched.

Within the same instruction cycle, the data shift registers that were enabled from the previous instruction are shifted one bit position by the low clock signal. Each data byte can be processed through the MTC in approximately 2.5 microseconds.

Write Clock Logic

The write clock control register may be preset to any value representing 4 to 500 kHz. This write frequency is inserted through a PAREN1 code and direct data bits MB1 through MB8.

The write clock counter, which has been preset from its control register, now increments at the master clock rate. When overflow occurs, the counter outputs to a divide-by-4 counter, where the actual write strobe (phase 2) is generated on every fourth NM100 input to the divide-by-4 counter.

This counter also sets the write clock pulse memory flip-flop, which allows the logic to remember that a write clock/phase 2 has occurred through feedback bit FB37.

TABLE 4-3. LIST OF MNEMONICS

Mnemonics/ Abbreviations	Description
ADT	Auto data transfer
B	Feedback bit flag flip-flop
DDx	Direct data
DINT	Micro (ADT) interrupt
DLE	Data logic enable function
EAx	Micro subfunction code, Enable A logic
EBx	Micro subfunction code, Enable B logic
ECx	Enable shift control logic
F1, F2, F3	Program flags 1, 2, 3
FBx	Feedback bits
INV	Invert read data bit currently being processed
LC1, LC2	Loop counter 1, 2
MABx	Read-only memory address bits
MBx	Read-only memory bits
MC-1	MTC clock phase 1
MR-T	Master reset from CPU (system clear)
MTC	Magnetic tape controller
MTD	Magnetic tape drive
NABx	Next read-only memory address bits
NMx	Logic micro step or micro time signal
OC	Open collector output
PARENx	Mode control or micro control function
RABx	Link register bits (subroutine return address)
RAWS	Read after write status flag
RDx	I/O data received from micro-processor CPU
RDS	Read data strobe (read character clock)
RPINT	Macro program interrupt to CPU
SEL	MTC selected for an I/O operation
SDx	Tape data or status sent to CPU
TIE	Track in error
TRx	Processed tape read data
TRD	Data read from tape and not yet processed
TS	Three-state output
TWRLS	Tape write data load strobe
WCCR9	Output of write CRC generator
WDx	Write data to tape unit
ZERO 1, 2	Loop counter 1, 2 equals zero

DIAGRAM DESCRIPTIONS 5

The following section provides facing page logic theory of operation for the magnetic tape controller (MTC). The logic diagrams for the MTC are part of the field print package.

Since section 4 covers the micro codes used to enable the magnetic tape controller logic, this section only details the logic operation of the MTC. Table 5-1 contains the logic functions of the integrated circuits used in the magnetic tape controller.

TABLE 5-1. MTC INTEGRATED CIRCUITS

Number	Generic Reference	Function Abbreviation	Description
755	8274	PSREG	10-to-1-line parallel-to-serial register
756	8273	SPREG	1-to-10-line serial to parallel register
758	74S257	MUX	8-to-4-line multiplexer
766	8205	ROM	Read-only memory
943	74173	REG	4-bit D flip-flop register
950	7400	NAND	2-input NAND gate
951	7420	NAND	4-input NAND gate
953	7404	INV	Inverter
954	9024	FF	J-K flip-flop
959	—	NAND	3-input NAND gate
962	7402	NOR	2-input NOR gate
963	7437	NAND.	2-input NAND gate
964	—	OR	2-input OR gate
967	74154	DCDR	4-to-1-of-16-line decoder
971	74195	SREG	4-bit shift register
972	9301	DCDR	4-to-1-of-10-line decoder
973	9312	MUX	8-to-1-line multiplexer
974	9316	CO	Counter
980	9322	MUX	8-to-4-line multiplexer
987	9334	ADLA	4-to-8-line decoder/ demultiplexer
988	8202	REG	10-bit D flip-flop register
993	7408	AND	2-input AND gate
994	7403	NAND	2-input NAND gate

MTC TIMING—SHEET 2

MTC CLOCK

The clock oscillator consists of inverters L2 and an 8-MHz crystal, Y1. Clock flip-flop M4 toggles at the basic clock rate of 8 MHz. Its Q output is ANDed with the basic clock output through drivers L1. The two signals coincide on every other clock cycle, which generates a master clock (MC-1) cycle of 4 MHz/250 nanoseconds.

FREQUENCY DIVIDERS

Three counters, B1, C2, and C1, are constantly being preset to a count of 6. The counter is considered full at count 15, but an output does not occur at TC pin 15 (carry out) until the 16th increment. This TC output goes high at 10 increments of the counter, following the initial preset. Since the B1 counter is incremented by the master clock cycle, this counter effectively multiplies the clock cycle of 250 nanoseconds by 10. The TC output of counter B1 is true every 2.5 microseconds. In turn, it enables counter C2 to increment, and upon reaching count 16, outputs a high at its TC output every 25 microseconds. Counter C1 outputs a high pulse every 250 microseconds, which is used by the long timer.

SHORT/LONG TIMERS

The short timer E1 and D1 and long timer E2 and D2 are loaded from the false side of the MB bits. In effect, the negative representation of the preset value is loaded by their respective PAREN code, and the timers are incremented to positive zero rather than being decremented. Since both timers are identical except for their increment rate, only the short timer is discussed here.

The lower rank of the short timer, E1, is clocked at its pin 2 by the basic clock rate of 4 MHz. However, the counter is not allowed to actually increment until its count enable pin 10 is high. This enable is asserted initially by NAND gate F3 pin 2 from the 2.5-microsecond counter B1. Short timer E1 is then incremented every 2.5 microseconds until it overflows at pin 15.

This output is applied as an increment enable to the upper rank of short timer D1. Upon its overflow, short timer complete feedback bit FB14 goes true and, via inverter C4, disables the incrementing of the counters.

The long timer receives its increment enable every 250 microseconds from counter C1.

WRITE CLOCK CONTROL

The eight-bit write clock control register E3 and D3 is loaded from the false side of the MB bits by PAREN1. The EQA/EQB output control gate constantly enables the three-state Q outputs of this register to the write clock counter E4 and D4, by being grounded.

WRITE CLOCK COUNTER

The clock counter increments at the master clock rate until a count of FF_{16} is reached. The next clock cycle increment to the counters results in overflow and the generation of the low active write clock pulse, NM100. Through inverter C4 the counters are again preset to the control register's contents by NM100 low at pins 9 of D4 and E4.

Clock pulse NM100 is used to generate the actual MTD write strobe (phase 2) on sheet 5.

FEEDBACK AND ROM ADDRESS LOGIC—SHEET 3

FEEDBACK MULTIPLEXER

One of five 8-to-1 multiplexers is selected by the feedback group select decoder, M8. The false side of the upper three bits of the feedback bit select code (MB4 through MB6) in the sample/test bit micro instruction are decoded. This results in an octal-numbered group selection (FBGx) that is the complement of the binary number applied to the A0 through A3 inputs of M8. The group select signal enables its associated multiplexer to decode from the false side of the lower three MB1 through MB3 instruction bits. Using multiplexer B6 (FB0x) as an example, note that FB7 is selected on this multiplexer as the D0 input, where FB0 (a constant 1) is selected as the D7 input. Again, the selection of the S0 through S2 inputs to the multiplexer is the complement of the octal number represented by instruction bits MB1 through MB3. Multiplexer M6 decodes for FB1x, multiplexer M10 for FB2x, multiplexer L6 for FB3x, and multiplexer M9 decodes for a select code of $40\text{-}45_8$ ($20\text{-}25_{16}$). Since the active state of feedback bits FB16 through FB23 is low, the output for multiplexer M10 is taken from the false side to indicate a logical one when any of these FB inputs is selected and active.

One output is selected from the five multiplexers through multiplexer M7 and applied to the bit flag flip-flop, K1. If the selected feedback bit is true and the current micro instruction is a sample/test bit, then the Q output of the bit flag flip-flop (pin 10) is clocked to a high. When the feedback bit is false, pin 10 of the bit flag flip-flop is low, following the sample/test bit instruction.

ROM ADDRESSING MULTIPLEXER

The 10-bit address supplied to the read-only memory program address (RPA) originates from address multiplexers E7, F7, and C7. These lines, designated as NAB1 through NAB10, are loaded into the RPA register as the next address fetched from the read-only memory during a branch or subroutine return micro instruction. The inputs to these multiplexers are the contents of the link (save return) register bits (RAB1 through RAB10) and the lower ten bits (MB1 through MB10) of the current micro instruction.

If the current MTC operation is not an I/O transform, then logic signal $\overline{\text{START}}$ being false enables the address multiplexers. Any micro instruction other than a subroutine return selects instruction bits MB1 through MB10 through the multiplexer onto the NAB lines. However, the NAB lines are not loaded into the RPA register unless the current micro instruction is a successful branch operation. A subroutine return instruction selects the link, register RAB inputs through the multiplexer, onto the NAB lines, and into the RPA register.

I/O TRANSFORM REGISTER

The MTC's I/O interface logic (sheet 7), once it has been initially selected by the CPU, generates an I/O START signal. When true, the address multiplexers E7, F7, and C7 are disabled, causing read-only memory address bits NAB5 through NAB10 to go low. This results in the selection of read-only memory address 00x, with the x value being supplied by transform register A7. Receiving its inputs from the I/O function code portion (SD01 through SD04) of the command register, these bits are always stored. The low $\overline{\text{START}}$ signal applied to the EQA/EQB output enable of this three-state output register causes the 4-bit I/O function code to be output as the x value read-only memory address on the NAB1 through NAB4 lines. The address loaded into the RPA register by the transform register is in the range of 000 to $10F_{16}$.

ROM AND ROM ADDRESSING—SHEET 4

READ-ONLY MEMORY

The ICs BC5 and A5 comprise the first 512 address/sixteen-bit words of read-only memory. This is the result of the decoding of memory address bit 10 being a zero at inverter B2. When MAB10 is set, then BC4 and A4 supply the upper 512 addresses. Each ROM IC that is enabled outputs eight bits of the micro instruction approximately 40 nanoseconds after application of the MAB bits to the A0 through A8 lines. The ROM strobe, pin 18, is tied high, bypassing the internal latching function of this chip.

ROM PROGRAM ADDRESS REGISTER

The read-only memory program address register, A6, E6, and E5, is a combined register and counter. Incremented by 1 by the master clock cycle when NM300 count enable is high, this register supplies the address, MAB1 through MAB10, of the next micro instruction to be executed. Upon reaching the end address of $3FF_{16}$, the next increment bumps it to a count of 400_{16}. Since only the lower 10 bits are decoded as an address, this, in effect, achieves wrap-around back to address 000_{16}. Logic signal NM200 when low implies a branch operation. This loads address multiplexer lines NAB1 through NAB10 into the RPA register.

LINK REGISTER

The link register is used to save the read-only memory address of the instruction immediately following a branch subroutine micro instruction. This allows the micro program to eventually find its way back to the next instruction it would have executed, after the branch subroutine instruction in the main program. The link register, C6, D6, and D7, is loaded directly from the RPA register output (MAB1 through MAB10) by the branch subsignal being low. The link is loaded with the address of the branch subinstruction and not the address following. Therefore, logic micro control NM400 is applied to count enable pins 7 and 10 of the link register for one clock cycle only. During that clock cycle, the contents of the link are incremented by 1, so the link now points to the correct return address.

BRANCH DECISION LOGIC—SHEET 5

LOOP COUNTERS 1, 2

Loop counter 1, consisting of four-bit counters F2 and A1, is loaded with the complement of instruction bits MB1 through MB8 by micro instruction SETLC1. Each BRANCH ON LC1 instruction causes the counter to increment by 1 towards positive zero. Upon overflowing, A1 pin 15 goes high, indicating that loop counter 1 contains zero.

The loop 2 counter is identical except that it is a four-bit counter. When pin 15 of F1 is a high level this indicates that the counter is in an all zero condition.

ROM ADDRESS CONTROL

Micro control NM300, when high, enables the RPA register to increment on each clock cycle. Any of the micro functions shown as the active low inputs to NAND gate H2-8 causes a no branch condition via the assertion of NM300 to a high. Of special interest is H2 pin 13, which is driven by the branch decision multiplexer G1 pin 14. It is low when no branch operation is active or the branch condition is not met.

Micro control NM200, when active low, initiates the branch operation by enabling the loading of the NAB lines (next address) into the ROM program address register. It is controlled by NAND gate H2, inputs 1, 4, and 5, which are driven low by any one of the three unconditional branch instructions shown. Pin 1, START (transform), forces a branch to the address specified by the transform register's (sheet 3) contents. Pin 2 of H2 is low only when a successful conditional branch test micro instruction is executed.

BRANCH DECISION MULTIPLEXER

Eight-to-one multiplexer G1 is enabled when micro function code bit MB16 is set. This condition exists for all conditional branches and for the test/sample bit micro instruction as well. The remaining three bits of the function code (MB13 through MB15) then select one of the four conditions used for branch testing through the multiplexer. A branch on loop 1≠0 micro instruction is a micro code C (1100). Since MB16 is a one in this example, the G1 multiplexer is enabled. The remaining function code bits (x100) select D4 pin 5 of the multiplexer. If the loop counter is zero, no branch occurs. Assuming this, logic signal ZERO 1 high sets the output latch in the multiplexer. Output pin 14 low asserts NM300 and disables branch signal NM200. Had the loop counter been nonzero, multiplexer pin 14 would be high. ANDed at NAND gate G3-3 with MB16, the resultant low causes H2 pin 6 to drive $\overline{\text{NM200}}$ low true. Note that the unused inputs on multiplexer G1 are hanging high, causing output pin 14 to be low (no branch) for function codes 8, B, E, and F_{16}.

FLAG MULTIPLEXER

Flag multiplexer E8 selects one of the four program flags that may be tested by the branch, flag on/off micro instructions. Bits MB11 and MB12 of this instruction select one of the four high true (flag set) inputs to its output pin 14. Exclusive OR gate J6 has like inputs when the flag being tested is in the same condition that the branch flag on/off instruction is testing for. This resulting low is applied to the D1 and D2 inputs of multiplexer G1, causing a branch operation when either function code 9 or A_{16} is selected.

WRITE CLOCK FREQUENCY DIVIDER

Shift register G7 is clocked by the write clock pulse NM100. The state of the data bit shifted into this register at NM100 time is a function of NAND gate G9. Normally, all four bits of this register would have to fill to ones before G9 pin 6 output goes low, causing a zero to be shifted in. However, the Q3 output of this register goes low first precluding this register from ever normally going to an all-ones state. The prime function of this register is to generate a write clock phase 2 to the MTD on the occurrence of every fourth NM100. Assume at some point that output Q3 pin 12 went low. This caused the register to preset to 0111 as shown in table 5-2. As the bits are shifted through this register, the Q1 output going low generates the write clock phase 2. When the zero bit that caused the Q1 output to go low is shifted to the Q3 position, this register is again preset to 0111.

TABLE 5-2. WRITE CLOCK SHIFT REGISTER

Step	Condition	Action at G7	Resultant Output				Write Clock Phase 2
			Q0	Q1	Q2	Q3	
Initial	Q3 = 0	Enable Preset	X	X	X	0	Don't care
1	NM100 low	Preset via G7-9	0	1	1	1	High
2	NM100 low	Shift in a 1 (G7-2)	1	0	1	1	Low active
3	NM100 low	Shift in a 1	1	1	0	1	High
4	NM100 low	Shift in a 1	1	1	1	0	High
–	Q3 = 0	Return to step 1					

WRITE CLOCK PULSE MEMORY FLIP-FLOP

This J-K flip-flop remembers that a write clock phase 2 has been generated. Q0 of shift register G7 is only low immediately following its presetting. NOR gate L3 is then enabled to set the memory flip-flop when the first NM100 clock signal pulsing low is applied to NOR gate L3-8. The output of this flip-flop and its resetting is a function of the control program.

MICRO INSTRUCTION DECODE—SHEET 6

MICRO FUNCTION DECODE

Four-to-one decoder H1 decodes the micro function field (MB13 through MB16) of the instruction word. Function code 9 (branch flag off) is not decoded here, but instead is decoded where it is used in the branch decision logic (sheet 5). Micro function codes B, E, and F are not used and are therefore not decoded.

PAREN/MODE DECODE

Decoder A3 only decodes the PAREN code when micro function bits MB15 and MB16 are both zeros. Micro function codes 0 through 3 are the only functions that support PAREN/mode decoding. One of the 11 active low PAREN micro controls is applied to the MTC logic for that instruction cycle. PAREN/mode code 15 being decoded at the Q15 output of A3 pin 17 enables the decoding of the EA and EB subfunctions by the low applied to NOR gate K4 pin 6.

EA DECODE

NAND gate L4 enables the decoding of the upper eight EA subfunctions when MB4 is set, the PAREN code equals 15, and the clock cycle is not active. When clock MC-1 goes low, the next micro instruction is being fetched. The resulting high at decoder K5 pin 2 forces a decode of a nonexistent EA subfunction that disables the EA8 through EA15 outputs.

The decode of the lower EA outputs is allowed to float during instruction fetches, as evidenced by the MB1 through MB4 inputs only at EA decoder H5.

EC BUFFER REGISTER

The two three-state buffer registers, M5 and L5, are loaded by a PAREN9 code applied to their input terms EDA/EDB. A data logic enable micro instruction gates their outputs via the EQA/EQB terms to the MTC logic. Note that the active state of the EC terms is a low, and that the selection of any EC shift control term is performed by the setting of its associated D latch to a zero. The register clear term is not used (pin 15) since this would set all EC outputs active.

CPU INTERFACE—SHEET 7

MTC SELECTION

The CPU's Q-register contents select the MTC for I/O operations. This addressing is achieved through application of low true backplane signals SMB9 (Q03), SPT (Q07-Q09), and the CPU's I/O data strobe SSTB/READ. NAND gate J2 low output sets the MTC selected flip-flop J3 pin 10 if the MTC is not busy. This flip-flop, upon setting, strobes the CPU's A register data (SD05 through SD14) into the MTC's I/O command register B7, via NAND gate G3 (GSTB). Logic signal $\overline{\text{GSTB}}$ also enables the I/O function transform (sheet 3) and sets the I/O command latched flip-flop J3 pin 6.

The next flip-flop to be set in the I/O control chain is the start transform, H3 pin 10. Following that, on the next clock cycle, the busy flip-flop H3 sets, which then resets the first two flip-flops in the chain. The MTC remains in a busy state until the micro control program returns to rest (halts). NAND gate F3 detects this and resets the busy flip-flop, H3 pin 3.

When the MTC was selected and went busy, NAND gate J2 low output set the macro program interrupt (RPINT) flip-flop, G8 pin 9. The macro program, resident in the CPU, acknowledges this interrupt and causes backplane signal SSEL/ to go low true to the MTC. NAND gate F8, which receives SEL, clocks the RPINT flip-flop G8 pin 10 reset and clears the interrupt condition.

Any low into NAND gate F9 creates low true $\overline{\text{NM650}}$ whenever MTC data is to be sent to the CPU. Pin 1 is low when an SIO sample (input) command is sent to the MTC. Pin 2 is low when an ADT input (read data) operation is active in the MTC.

Each time a data transfer is required between the CPU and the MTC, the DINT flip-flop (ADT micro interrupt), G8 pin 6, must be set by the micro program. In addition, the direction of that data (to/from CPU) must be flagged. Data direction flip-flop H4 pin 6 is set by $\overline{\text{EA7}}$ for an MTD read operation. As this means that ADT data flow will be from the MTC to the CPU, backplane signal RDIROUT must be driven low. This is done by NAND gate G10 each time the MTC is selected for data transfer at G10 pin 13. Conversely, for an MTD write operation, ADT data originates from the CPU. The direction flip-flop H4 pin 6 is now reset by EA1, and drives backplane signal RDIROUT high.

The data to be written to the MTD must be strobed into the MTC input data register (sheet 11) from the SD backplane lines. NAND gate G9 provides this active low load strobe ($\overline{\text{TWRLS}}$) during the time the CPU's I/O data available strobe, STB-T, is present.

ADT data transfers continue until the CPU determines that the data operation has completed. When this occurs, backplane signal STERM/ is ANDed with the CPU's micro interrupt acknowledge (SSEL/) signal, which was sent for the final ADT data transfer. NAND gate F9 pin 8 low output sets the ADT terminate flip-flop, H4 pin 10. Its output, FB9 (TERM B), is sensed by the micro control program, after which it is reset by the program.

OUTPUT MULTIPLEXERS—SHEET 8

The output multiplexers drive the RD backplane lines leading to the CPU's A register. Micro control NM650, when low, enables the multiplexers at pins 15 of the 8-to-4 line multiplexers A10, B9, C10, and E10. This indicates that the MTC's CPU interface has received a data request from the CPU. The data read from tape ($\overline{\text{TR1}}$ through $\overline{\text{TR15}}$) is selected through the multiplexer and onto the backplane lines if the DINT signal is high. This indicates that an ADT micro interrupt has been sent to the CPU for a data in transfer operation.

If signal DINT is low, this implies that the data request received from the CPU is a sample status command. The outputs of status register 1 (D10) and status register 2 (D8) are then selected through the multiplexer.

STATUS REGISTERS

Status register 1 (D10) and bits 4 through 7 of D8 for status register 2 make up the MTC's status word. Bits 0 through 3 of D8 are used as the program flag register. Accessed by a PAREN5 or PAREN6 code, instruction bits MB1 through MB3 select one of eight latches in this register. MB4 then sets or clears the selected latch. Since the backplane lines driven by the status registers are low true, setting of any particular status bit requires clearing its associated latch to a zero.

TAPE READ DATA HANDLING LOGIC—SHEET 9

Detailed theory of operation for this sheet is not given here, as section 4 of this manual provides sufficient theory along with descriptions of the micro instruction controls. Figure 4-4 identifies the IC functions and the read data flow chart contained in appendix A provides a logical flow for the MTC operations contained on this page.

READ DATA IN REGISTER

This register, L10, receives the low true tape read data ($\overline{\text{TRD}}$) from the MTD interface. When enabled for shift mode through PAREN10 and read data control register H7 pin 7, the 7- or 9-bit tape character is shifted out, starting with tape bit 0. Pin 6 of register L10 goes low for every data one bit shifted out, and is recirculated back via L9 pin 11, L9 pin 3, and pin 11 of this register. In this way, each data bit may be examined as to its state at inverter L8 (FB11), without disturbing the tape byte.

The data flow originating at L8 is applied to exclusive OR J6 pin 1. Its pin 2 normally low passes the high-true data to inverter C4, where it is assembled by the least and most significant byte registers (A9 and D9, respectively).

CONTROL LOGIC—SHEET 10

Several logic areas for the MTC are shown on this page. Only the highlights of specific logic blocks are detailed here, since much of the logic and its application is identified in section 4.

WRITE CONTROL REGISTER

A PAREN7 code enables the EDA/EDB input term of write control register H8, allowing instruction bits MB1 through MB4 to set or clear micro steps NM250, NM350, NM450, and NM550. Micro steps NM250, NM350, and NM450 select the data input through the write data multiplexer, while NM550 low enables loading of the CPU write data into the MTC. When NM550 is high, the write data is shifted serially through the write data handling logic (sheet 11).

MTD UNIT SELECT REGISTER

Logic signals POS1 and POS2, obtained from the MTC I/O command register, select one of the four possible tape units connected to the MTC. When subfunction EA3 is active low, and EB-1 ($\overline{\text{EBM-1}}$) is high, any latches previously set in this register remain set during the new selection operation.

FEEDBACK INPUTS

Status lines originating from the MTD interface are connected through the M11-type pull-up resistors into the MTC as feedback bits.

READ DATA STROBE FLIP-FLOP

The RDS flip-flop M4 pin 9 is sampled as $\overline{\text{FB16}}$ and sets on the trailing edge of the read clock from the MTD interface. Its resetting is a function of the control program only. This flip-flop, when set, indicates that a tape character has been loaded into the MTC from the MTD interface.

TRACK IN ERROR REGISTER

This 10-bit circular shift register, G4, is set when the read data control register micro step NM500 is asserted. If micro step NM600 is also asserted high, then the current tape data bit entering the MTC read data handling logic is inverted. Micro steps NM500 and NM600 are controlled by the nine-track error recovery micro routine. Data set into the TIE register continues to recirculate via NOR gate K4 until this register is reset by EB3.

WRITE DATA HANDLING LOGIC—SHEET 11

CRC LOGIC

The output of write data multiplexer J8 pin 15 is high for a data 1 being written to tape. Sampled as FB31, it is applied to the CRC logic consisting of the CRC generator L7 and CRC carry flip-flops K8 through K10. Pin 9 of the generator output (WCCR9) represents the combined state of all data bits written on track 0 of the tape. When the CRC generator is shifted one bit position by $\overline{\text{EC4}}$ low, WCCR9 represents the combined state of all data bits written on track 1 of the tape. When the CRC generator is again shifted one bit position by $\overline{\text{EC4}}$ low, WCCR9 represents the combining of all bits written in track 2. Picturing a nine-bit checkword in the CRC generator with each bit position equated to a tape track, the combining or generation of the CRC checkword is shown in table 5-3. Assume subfunctions $\overline{\text{EA5}}$ (inverter L2) and $\overline{\text{EB6}}$ (NOR F5) are true.

As seen from table 5-3, the input to the CRC generator is binary addition without regard to carries (half add operation). When either the data bit or the previous bit from that same track is a 1 (examples 2 and 3), the input to the CRC generator is a 1. The example of both FB31 and WCCR9 being 1s would normally result in a 0 input to the CRC generator unless the CRC carry flip-flop were set, as shown in examples 5 and 8. The CRC carry flip-flop is set for only two basic conditions: either input being a 1 (examples 2 and 3) and the carry flip-flop zero or either input being a 1 and the carry flip-flop set (examples 6 and 7). From these known conditions, the CRC correction algorithm is derived for read recovery on nine-track tape.

TABLE 5-3. COMBINATION/GENERATION OF CRC CHECKWORDS

Example	FB31 (Data)	WCCR9 (CRC Output)	CRC Carry Flip-Flop (Initial State)	Result to CRC Generator (L7-10)	CRC Carry Flip-Flop (Final State)
1	0	0	0	0	0
2	1	0	0	1	1
3	0	1	0	1	1
4	1	1	0	0	0
5	0	0	1	1	0
6	1	0	1	0	1
7	0	1	1	0	1
8	1	1	1	1	0

WRITE DATA REGISTERS

Data is serialized by the 10-bit MSI shift registers. In the case of disassembly, input registers B8 and A8 do not use the lower order bits and the first bit output is from D10 on B8 (pin 6). To reassemble the tape byte, one extra shift is performed on J10 to right-justify tape bit WD0. Note that an extra fanout for WD0 exists to allow write-to-read wrap around.

MTD COMMAND REGISTER—SHEET 12

Register H9 contains eight latches that are addressed by PAREN2 and instruction bits MB1 through MB3. MB4, when high, sets the addressed latch and its associated output command line low true.

ECO DS 14699
PAGE 25

section, combined with the MTC field print pack- (FPP), provides the procedures and references ed to diagnose, maintain, and verify that the MTC proper working order.

NOTE

In all circumstances and procedures specified herein, on-site maintenance is limited to the diagnosis of a malfunction and then to replacing the entire magnetic tape controller PC board with one that performs satisfactorily.

In addition to the magnetic tape controller's built-in self-test diagnostic program, the following maintenance support documentation is also available:

- The ~~CYBER 18~~ [illegible] ~~Processor~~ Hardware Maintenance Manual contains the necessary troubleshooting procedures to be used by the customer engineer.. Its maintenance approach is to fault-isolate through the use of diagnostic decision logic tables (DDLTs) and to accomplish repair by exchanging replaceable subassemblies rather than replacing faulty component parts.
- The Operational Diagnostic System (ODS) Reference Manual. ODS is a software diagnostic package that uses the LCTTA (diagnostic program) by accessing the MTC's self-test micro programs to verify that the controller is fully functional without the use of the tape transport. The diagnostic program LCTTB is used to test the MTC on-line with the tape transport.

PRINTED CIRCUIT BOARD REMOVAL

A special removal tool (NCR part number 315-0526169D) is used to remove the controller board. The tool is used to pry the card loose by placing the post in the tool over the hole near the top or bottom of the card and prying against the card cage frame. Additional details are contained in the ~~CYBER 18~~ [illegible] hardware maintenance manual.

PREVENTIVE MAINTENANCE

No preventive maintenance is required for the magnetic tape controller.

MAGNETIC TAPE CONTROLLER SELF-TESTS

The MTC contains a self-test capability through the use of an internal set of micro programs. Just as the MTC/MTD's characteristics can be assigned (software-programmed) using the system's SIO set command, so can the MTC's built-in diagnostics be implemented using the system's SIO sample command.†

The controller self tests are initiated from the CPU by the four least significant bits of the function word. Test subsections are further selected by the controller sampling the remaining function word bits. At the end of each test, the controller becomes not busy and returns an indication of a successful test execution. Since the MTC is considered a replaceable subassembly, any negative test results indicate controller replacement.

The goal of the controller tests is to verify that the controller is fully functional, from generating program interrupts to transferring data to and from the CPU. A list of controller tests that is used to accomplish this goal is as follows:

- Interrupt handling
- Micro instruction execution
- Function decoding
- Status reporting
- Internal timing
- Data handling
- Error detection and correction

In addition to detecting specific test failures, the test program monitors continuously for abnormal conditions such as unexpected status, unexpected interrupts, and failures in controller recognition of valid function words.

†See the 1700 Enhanced Processor with Core Memory Reference Manual for complete software programming formats and instructions.

Reduce to 75%

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NOTE

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PRINTED CIRCUIT BOARD REMOVAL

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- Status reporting
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In addition to detecting specific test failures, the test program monitors continuously for abnormal conditions such as unexpected status, unexpected interrupts, and failures in controller recognition of valid function words.

†See the 1700 Enhanced Processor with Core Memory Reference Manual for complete software programming formats and instructions.

Any magnetic tape drive that is connected to the magnetic tape controller should contain only 800 bpi certified initialized scratch tapes for testing purposes. The scratch tapes are used for writing test information during MTC/MTD verification tests. A description of specific tests follows, first by test type and then by test group type.

DIAGNOSTIC TESTS

Controller Access

Intent: Verify that the controller responds to the CPU.

Description: A function code of $xxxF_{16}$ issued to the controller produces a program interrupt using only two micro instructions.

Expected Test Results: The controller issues a program interrupt.

Branch Micro Instruction

Intent: Verify the controller's branch micro instruction.

Description: A function code of $xxxE_{16}$ causes the controller to attempt a branch instruction. This branch instruction, if executed successfully, bypasses an instruction that would generate an interrupt.

Expected Test Results: No interrupts from the controller.

Status Register All On

Intent: Verify that all the status bits that can be set by the micro program may be set.

Description: A function code of $xxxD_{16}$ directs the controller to set all its status lines. Bits 15, 5, 3, and 1 are not controlled by the micro program and are therefore unpredictable.

Expected Test Results: A program interrupt with status bits 00, 02, 04, 06 through 14 all ones.

Branch on Feedback Micro Instruction

Intent: Verify the test feedback and conditional branch micro instructions.

Description: A function code of $xxxC_{16}$ causes the controller to test a known internal condition (interrupt) and to branch on its absence. Next, the controller sets the interrupt and attempts to branch on its presence.

Expected Test Results: A program interrupt with the status word's bits 00, 02, 04, 06 through 14 all ones.

Jump Micro Instruction

Intent: Verify the jump and return micro instructions.

Description: A function code of $x01B_{16}$ causes the controller to execute a jump and then a return micro instruction. If either fails, the error condition is indicated by bit 11 set to a zero in the status register.

Expected Test Results: A program interrupt with the status word bits 00, 02, 04, 06 through 14 all ones.

Zero Status

Intent: Verify that the status bits can be cleared.

Description: A function code of $048B_{16}$ causes the controller to'clear status bits 00, 02, 04, 06 through 14 (bits 01, 03, and 05 are not under micro program control).

Expected Test Results: A program interrupt with status bits 00, 02, 04, 06 through 14 all zeros.

Loop Counters

Intent: Verify the controller's internal loop counters.

Description: A function code of $x02B_{16}$ causes the controller to issue 255 data interrupts, expecting the CPU to provide a data strobe in reply for each interrupt. After the 255th data interrupt, the controller issues a program interrupt.

A function code x04B$_{16}$ causes the controller to issue 15 data interrupts, expecting the CPU to provide a strobe in reply for each interrupt. After the 15th data interrupt the controller issues a program interrupt.

Expected Test Results: 255 data interrupts and 15 data interrupts.

Timers and Write Clock

Intent: Test the controller clock and clock-related micro instructions.

Description: A function code of x10B$_{16}$ causes the controller to exercise its long timer, short timer, and write clock. This operation should take 28.1 milliseconds from the output of the function code to the receipt of the program interrupt.

Expected Test Results: A program interrupt with status bits 00, 02, 04, 06 through 14 all zero; test execution time 28.1 milliseconds ±10 percent.

Internal Data Recirculation

Intent: To test the controller's ability to move data through its internal registers during a simulated tape write developing and checking parity.

Description: A function code of x50B$_{16}$ causes the controller to clear the controller input register from the CPU. Its contents are then moved through the tape write register and the tape read register to the controller's output register to the CPU. Parity generation and test are also included during the data transfer operation.

Expected Test Result: Data interrupt with the data word all zeroes. Program interrupt with status word all zeroes.

Miscellaneous Controller Checks

Intent: Verify the controller's ability to recognize invalid function commands.

Description: the following functions cause the controller to ignore the function and issue a program interrupt with:

- Program error (status bit 06 set)

  -Function code xxx0$_{16}$
  -Write or read nine-track with even parity
  -Write or read nine-track with other than 800 bpi
  -Write or read seven-track with 1600 bpi
  -Filemark on seven tracks

- Inoperative during selection (status bit 00 set)

  -Read or write function with the tape drive not ready (i.e., off line)

- Rewinding (status bit 02 set)

  -During a tape drive rewind, any function code other than a test mode function

- Write lockout (status bit 04 set)

  -Write protect ring removed from the tape reel and any function other than a test mode function issued

- Inoperative after execution (status bit 12 set)

  -Function code of x40B$_{16}$ or x00B$_{16}$

Expected Test Results: A program interrupt is issued with the appropriate status bits set. The function issued is not initiated on the tape transport.

The preceding checks verify the ability of the controller to execute its micro instructions. Since the controller is a micro processor, instruction verification is vital but not conclusive. The controller has been verified up to the point of executing the actual application controlware. The possibility of a controller micro program failure must be kept in mind in diagnosing apparent tape transport failures.

DIAGNOSTIC TESTS SUMMARY

B Test Group

Function Code x01B$_{16}$

Conditions: Successful execution of D test group (xxxD).

Intent: To verify the controller's most complex instruction, jump and return.

Description: If a jump and return is executed successfully:

- A program interrupt is generated.
- The overload status bit is cleared.

Function Code x02B$_{16}$

Conditions: None

Intent: To verify an internal counter (loop counter number 1)

Description: The controller issues 255 data interrupts expecting a data strobe for each. After the 255th data strobe, the controller goes not busy and issues a program interrupt.

Function Code x04B$_{16}$

Conditions: None

Intent: To verify an internal counter (loop counter number 2)

Description: Same as a loop counter number 2 check but with 15 interrupts.

Function Code x10B$_{16}$

Conditions: Loop counter number 1 and loop counter number 2 have been verified.

Intent: Test the controller's internal timers.

Description: The short timer is checked to 500 microseconds ± 50 microseconds. Dropout/pickup status indicates that the clock is too fast. Timeout status indicates clock is too slow.

The long timer is checked to 25 microseconds ± 2.5 microseconds using the short timer. Short record status indicates that the clock is too fast. A half word on read status indicates that the clock is too slow.

The write clock is checked to 50 microseconds. Program error status indicates write clock failure.

NOTE

The controller interrupts after all clocks are checked. If the short timer fails, the long timer test is invalid.

Function Code x20B$_{16}$

Condition: None

Intent: Check data handling and parity generation in tape read path.

Description: Zeroes (provided as 1s to the CPU on a data interrupt) are processed from the tape read register by the controller to the CPU on interrupt. Furthermore, a program interrupt is issued with the possible error bits; tape mark status indicates an even parity failure. Data error status indicates an odd parity failure.

Function Code x50B$_{16}$

Intent: Check data handling and parity generation in tape write path.

Description: The controller input register from the CPU is cleared and its contents are moved through the tape write register to the tape read register (data inversion occurs here). It then moves to the controller's output register to be presented as a data word of all 1s to the CPU on a data interrupt. Furthermore, a program interrupt is issued with error status.

Short record indicates odd parity failure. Half word on read indicates even parity failure.

Function Code x40B$_{16}$ or x00B$_{16}$

Condition: None

Intent: Simulate a controller busy condition.

Description: The controller generates a program interrupt with all the status bits set in test group D cleared, except inoperative during selection status bit.

Function Code x48B$_{16}$

Conditions: None

Intent: Clear status bits set in test group D.

Description: Status bit positions 00, 02, 04, 06 through 14 are cleared (see test group D).

C Test Group

Function Code xxxC$_{16}$

Conditions: Controller branch instruction verified

Intent: Check the controller test feedback bit and conditional instructions.

Description: A branch on testing the controller's interrupt flag not being set (BRNB) is attempted. Next, the interrupt is set and a branch on the test of the interrupt being set (BRB) is attempted.

Tape mark status indicates the branch on flag not set micro instruction failed.

Data error status indicates the branch on flag set micro instruction failed.

D Test Group

Function Code xxxD$_{16}$

Conditions: None

Intent: Set all status bits handled by the controller.

Description: Status bits positions 00, 02, 04, 06 through 14 are set. Note that bits 01, 03, and 05 are not under program control.

E Test Group

Function Code xxxE$_{16}$

Conditions: None

Intent: Attempt a simple branch (unconditional).

Description: A single instruction that branches over an interrupt generating instruction is executed. Executing this test function should release the controller without any controller response. Any interrupt indicates the unconditional branch micro instruction failed.

F Test Group

Function Code xxxF$_{16}$

Conditions: None

Intent: In the simplest way, get a response from the controller.

Description: Using the minimum controller instructions, a program interrupt is issued.

SAMPLE MAINTENANCE TEST PROGRAMS

The following sample test programs, provided for reference, are several examples that can be used by maintenance personnel to perform selected tests. Each test includes a functional description and a commented listing of the program.

Status Loop With Select Function

The program checks the status of the tape controller for any errors and halts if it finds any status bit set. If no status bits are set, the program continues setting the tape unit function word and outputs the select function. The program then jumps back to the beginning and repeats. The program does not terminate unless an error is found.

Program Listing

P0000	E000	Load Q register with equipment address (port, position)
P0001	0600	
P0002	0A00	Enter A register with zero
P0003	0B05	Sample position status to obtain status
P0004	0101	Skip if A register equals zero (no errors)
P0005	18FF	Hang here if status is set
P0006	0D08	Continue if status is OK; add 8 to Q register

P0007	C000	To set mode, load A register with tape unit and function word (select)
P0008	0908	Set for 7 track, 800 bpi, select function, unit 0
P0009	0B04	Set/sample output to controller
P000A	18F5	Jump back to start of program and repeat

Rewind

This program first checks the status of the tape controller for any errors and halts if it finds any status bits set. If no status bits are set, the program continues setting the tape unit and rewind function. The program outputs the function and again checks the status. It looks at bit 2 (rewinding), and if rewinding is set, it indicates that the rewind operation has started but is not yet completed. The program again checks status until bit 2 is clear and then halts. When checking bit 2, if any other status bit comes up, the program halts indicating an error. Normal operation is to execute the program, the selected drive rewinds to BOT, and the program halts. Check the A register at this time; the terminating status of 0004$_{16}$ indicates correct operation. Any other status indicates an error condition.

Program Listing

P0000	E000	Load Q register with equipment address (port, position)
P0001	0600	
P0002	0A00	Enter A register with zero
P0003	0B05	Sample position status to obtain status
P0004	0101	Skip if A register is zero (no errors)
P0005	18FF	Hang here if status is set
P0006	0D08	Continue if status is OK; add 8 to Q register
P0007	C000	To set mode, load A register with tape unit and function word (rewind)
P0008	0905	
P0009	0B04	Set/sample output to controller
P000A	0DF7	Subtract 8 from Q register
P000B	0A00	Enter A register with zero
P000C	0B05	Sample position status to obtain status
P000D	B000	Exclusive OR the contents of A register with 0004$_{16}$ to determine if rewind is in progress
P000E	0004	Set for 7 track, 800 bpi, rewind function, unit 0
P000F	0101	Skip if A=zero; rewind in progress
P0010	18FF	Hang here on error, or rewind complete
P0011	18F9	Rewind not complete; jump back to get status

Write or Read Variable Length Buffers

This program sets a specified buffer area in memory to a data pattern. The pattern, usually ones or zeros, is contained in P=0001. The buffer area can be modified as desired. This example used the area 0200$_{16}$ to 2000$_{16}$ as the buffer. The program then sets up the ADT table for the transfer of data. This example used 0160$_{16}$ to 0163$_{16}$ for the ADT table. The tape function is then output to start the operation. Next, the micro interrupt line is enabled and the mask register is set. The interrupt lines used here are 7 for the micro interrupt and 12 for the macro interrupt.

The data transfer is in progress under micro interrupt control as the macro program waits for an interrupt. Upon completion of the transfer, a macro interrupt is generated causing the code at location 0130$_{16}$ (interrupt trap for line 12) to be executed. This code filters out any erroneous interrupts and checks the status of the controller. Any status bits set cause the program to halt at 0140$_{16}$. The A register can then be checked for the status condition that caused the program to halt. If the status is returned as zero, the program continues repeating the ADT transfer until stopped by the operator.

Program Listing

P0000	E000	Load Q register with data pattern selected
P0001	FFFF	Data pattern used
P0002	C000	Load A register with FWA of buffer area
P0003	0200	
P0004	60FF	Store A register in I register
P0005	C000	Load A register with LWA of buffer area
P0006	2000	
P0007	44FF	Store Q register in cell specified by I register
P0008	B0FF	Exclusive OR the contents of I register and A register
P0009	0103	Skip if A=zero; buffer is loaded
P000A	D0FF	No; replace add 1 to I register

P000B	C8FA	Load (restore) A register with LWA
P000C	18FA	Jump back to continue loading buffer area
P000D	18FF	Halt here when buffer is loaded
P000E	C000	Load A register with (start of tape read/write operation)
P000F	8X00	ADT write/read function (8E00 for write/8600 for read)
P0010	6400	Store A register in first word of ADT table
P0011	0160	
P0012	C000	Load A register with FWA-1 of buffer area
P0013	01FF	
P0014	6400	Store A register in second word of ADT table
P0015	0161	
P0016	C000	Load A register with LWA of buffer area
P0017	2000	
P0018	6400	Store A register in third word of ADT table
P0019	0162	
P001A	0A00	Enter A register with zero
P001B	6400	Store A register in fourth word of ADT table
P001C	0163	
P001D	E000	Load Q register with equipment address (port, position)
P001E	0608	
P001F	C000	Load A register with tape function word (0902 for write/0901 for read)
P0020	090X	Set for 7 track, 800 bpi, unit 0
P0021	0B04	Set sample output to tape controller
P0022	E000	Load Q register with micro interrupt line number
P0023	8007	
P0024	C000	Load A register with FWA of ADT table
P0025	0160	
P0026	0B06	Define micro interrupt
P0027	C000	Load A register with macro interrupt line number
P0028	1000	
P0029	0821	Transfer to mask register
P002A	0400	Enable interrupts
P002B	18FF	Wait here for interrupt

Interrupt Response

P0130	0000	Return address of interrupt program
P0131	E000	Load Q register with equipment code (port, position)
P0132	0600	
P0133	0B05	Sample position status to get status
P0134	C400	Load A register indirect from second word of ADT table
P0135	0161	
P0136	B000	Exclusive OR the A register with FWA of buffer area
P0137	01FF	
P0138	0112	Skip if A register is not zero (determine if interrupt is true interrupt)
P0139	0400	No; re-enable interrupts
P013A	18FF	Wait again for completion of ADT transfer
P013B	E000	Yes; load Q register with equipment address (port, position)
P013C	0600	
P013D	0A00	Enter A register with zero
P013E	0B04	Set sample input to get status
P013F	0101	Skip if A=zero
P0140	18FF	Halt here if status set (indicates error)
P0141	1400	No errors; jump to start of program at $000E_{16}$
P0142	000E	

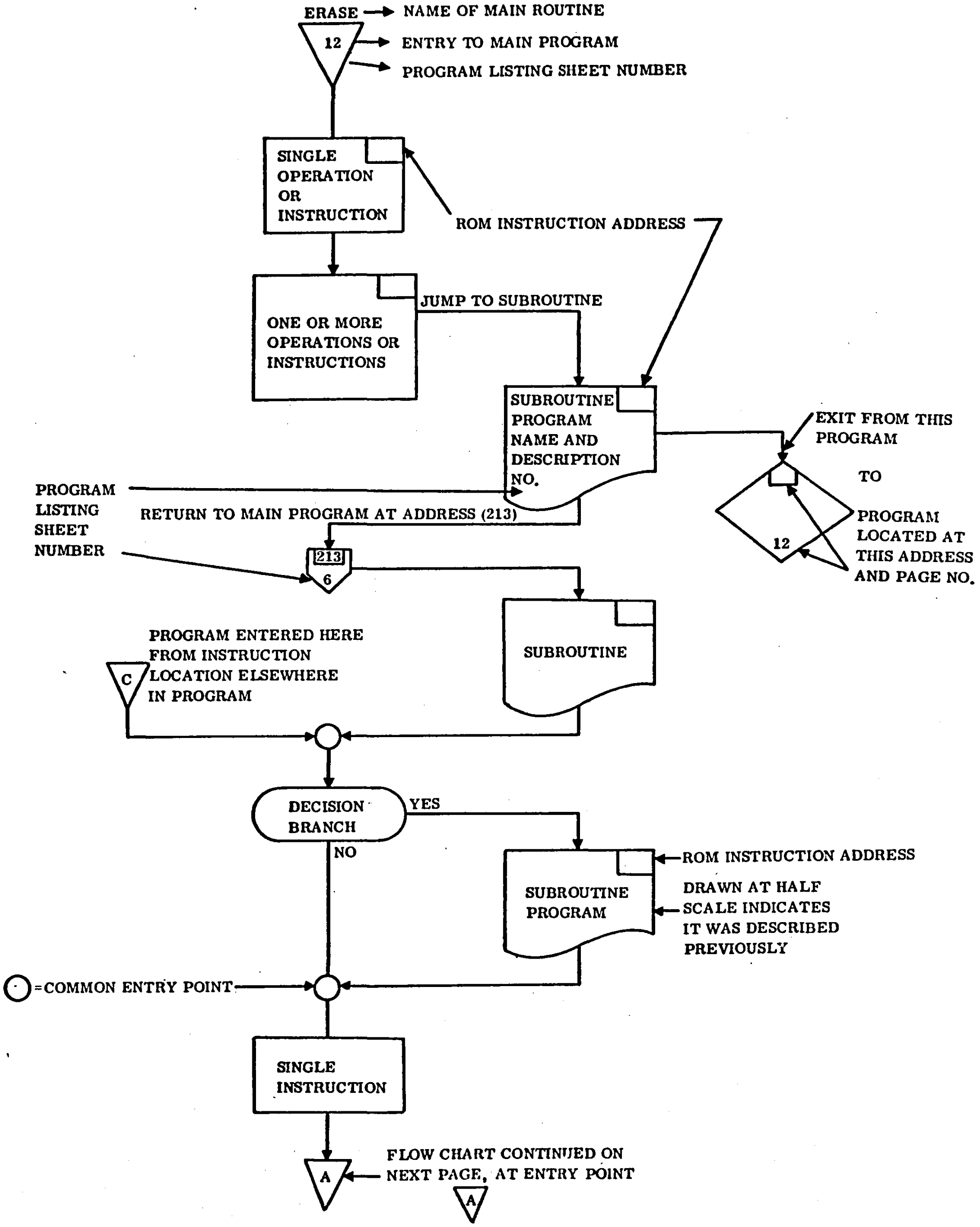
ERASE
NAME OF MAIN ROUTINE
12
ENTRY TO MAIN PROGRAM
PROGRAM LISTING SHEET NUMBER
SINGLE OPERATION OR INSTRUCTION
ROM INSTRUCTION ADDRESS
ONE OR MORE OPERATIONS OR INSTRUCTIONS
JUMP TO SUBROUTINE
SUBROUTINE PROGRAM NAME AND DESCRIPTION NO.
EXIT FROM THIS PROGRAM
TO
PROGRAM LOCATED AT THIS ADDRESS AND PAGE NO.
12
PROGRAM LISTING SHEET NUMBER
RETURN TO MAIN PROGRAM AT ADDRESS (213)
213
6
SUBROUTINE
PROGRAM ENTERED HERE FROM INSTRUCTION LOCATION ELSEWHERE IN PROGRAM
C
DECISION BRANCH
YES
NO
SUBROUTINE PROGRAM
ROM INSTRUCTION ADDRESS
DRAWN AT HALF SCALE INDICATES IT WAS DESCRIBED PREVIOUSLY
=COMMON ENTRY POINT
SINGLE INSTRUCTION
A
FLOW CHART CONTINUED ON NEXT PAGE, AT ENTRY POINT
A

Figure A-1. Flow Chart Symbol Descriptor

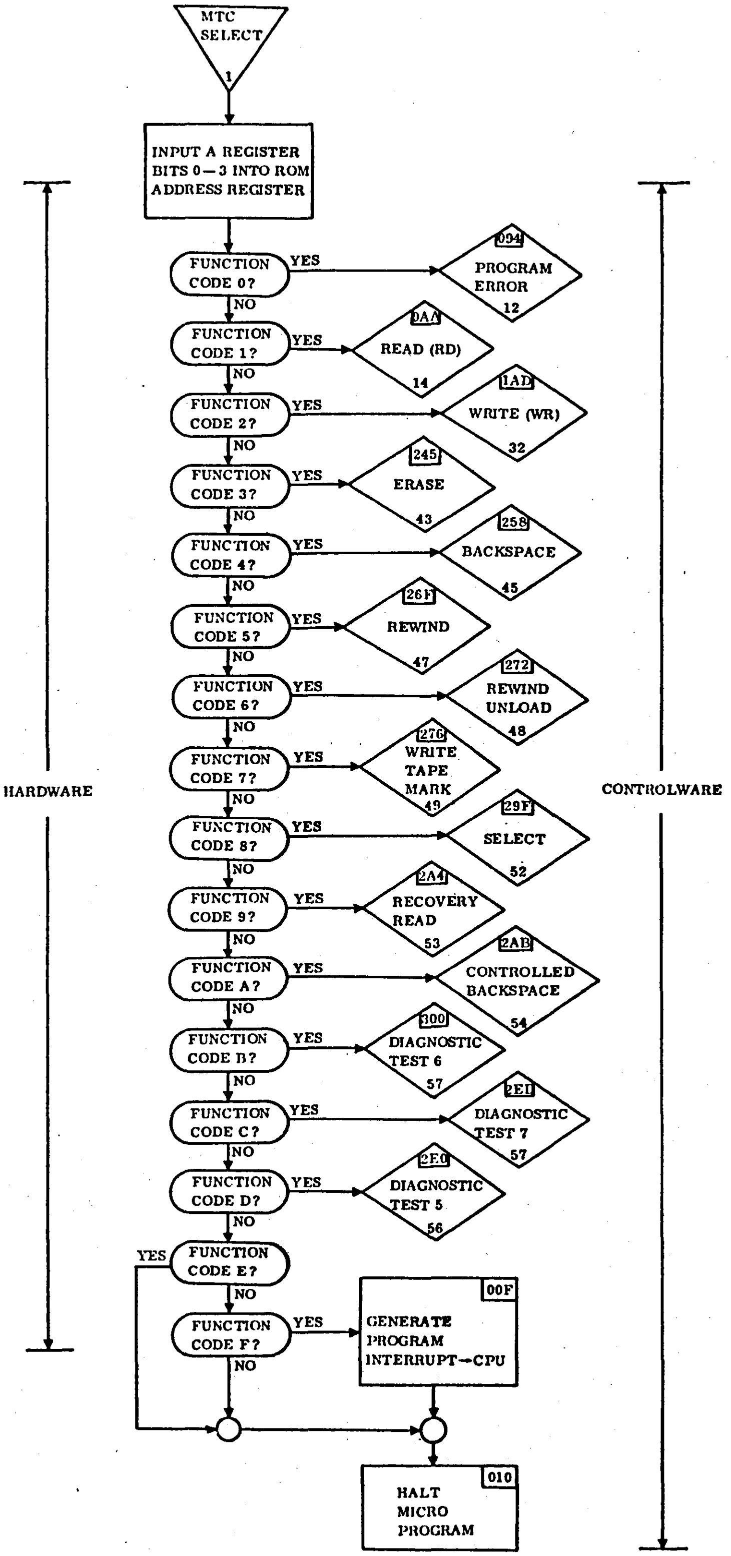

Figure A-2. Q Function Code Transform (XF)

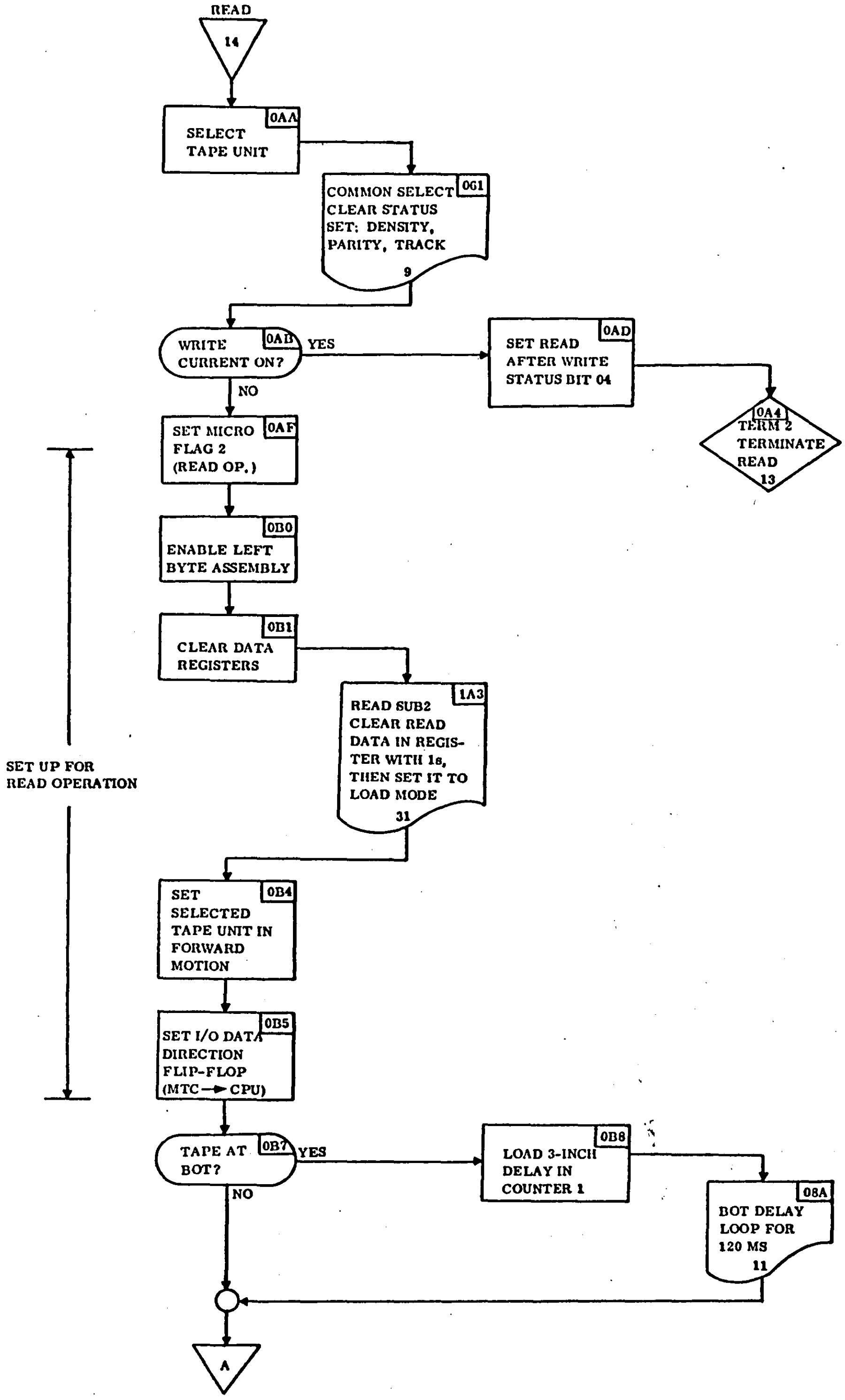
READ
14
0AA
SELECT TAPE UNIT
0G1
COMMON SELECT
CLEAR STATUS
SET: DENSITY, PARITY, TRACK
9
0AB
WRITE CURRENT ON?
YES
NO
0AD
SET READ AFTER WRITE STATUS BIT 04
0A4
TERM 2
TERMINATE READ
13
0AF
SET MICRO FLAG 2 (READ OP.)
0B0
ENABLE LEFT BYTE ASSEMBLY
0B1
CLEAR DATA REGISTERS
1A3
READ SUB2
CLEAR READ DATA IN REGISTER WITH 1s, THEN SET IT TO LOAD MODE
31
SET UP FOR READ OPERATION
0B4
SET SELECTED TAPE UNIT IN FORWARD MOTION
0B5
SET I/O DATA DIRECTION FLIP-FLOP (MTC → CPU)
0B7
TAPE AT BOT?
YES
NO
0B8
LOAD 3-INCH DELAY IN COUNTER 1
08A
BOT DELAY LOOP FOR 120 MS
11
A

Figure A-3. Tape Read (Sheet 1 of 4)

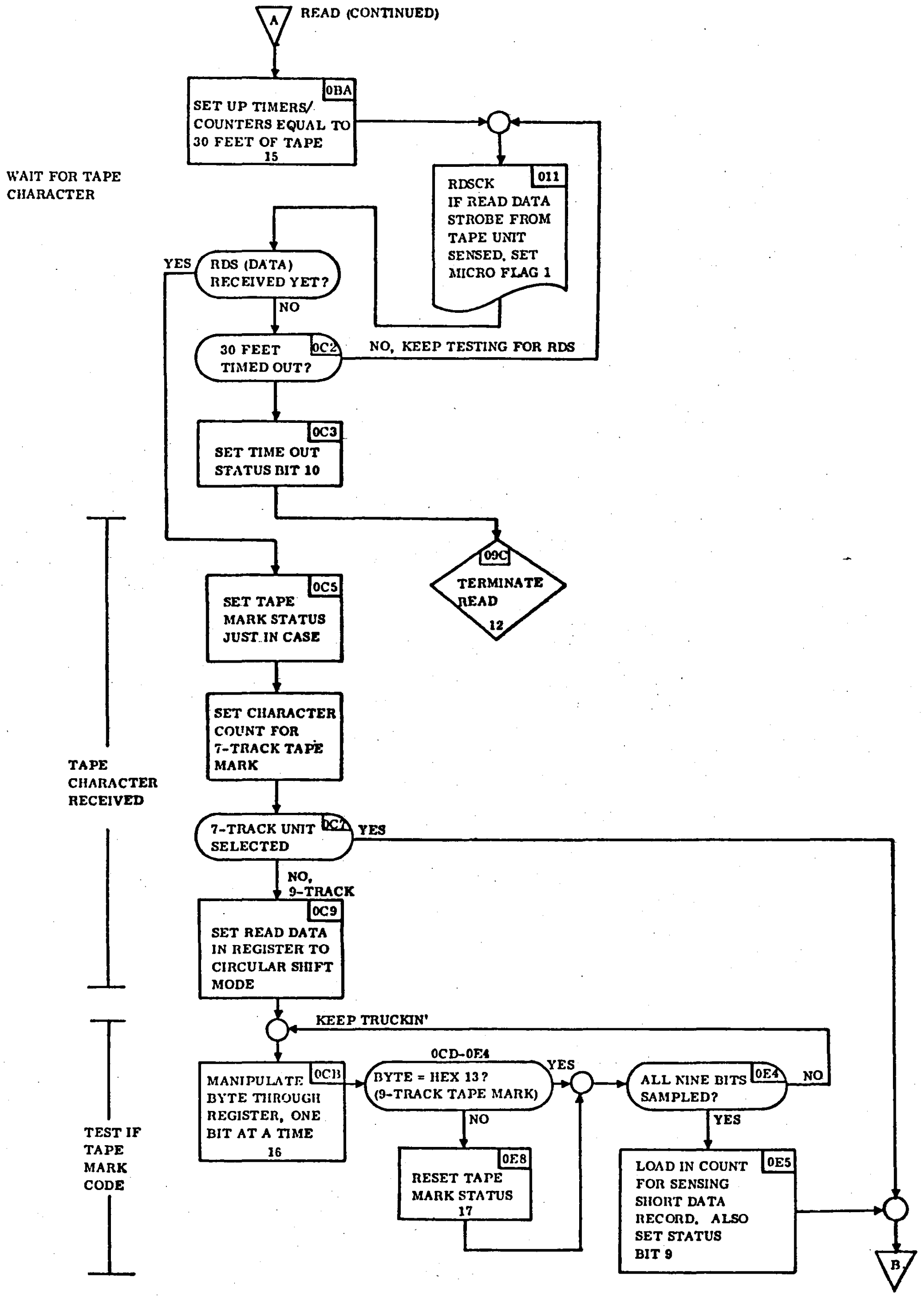
A
READ (CONTINUED)
0BA
SET UP TIMERS/ COUNTERS EQUAL TO 30 FEET OF TAPE
15
WAIT FOR TAPE CHARACTER
RDSCK
011
IF READ DATA STROBE FROM TAPE UNIT SENSED, SET MICRO FLAG 1
YES
RDS (DATA) RECEIVED YET?
NO
30 FEET TIMED OUT?
0C2
NO, KEEP TESTING FOR RDS
0C3
SET TIME OUT STATUS BIT 10
09C
TERMINATE READ
12
0C5
SET TAPE MARK STATUS JUST IN CASE
SET CHARACTER COUNT FOR 7-TRACK TAPE MARK
TAPE CHARACTER RECEIVED
7-TRACK UNIT SELECTED
0C7
YES
NO, 9-TRACK
0C9
SET READ DATA IN REGISTER TO CIRCULAR SHIFT MODE
KEEP TRUCKIN'
0CD-0E4
MANIPULATE BYTE THROUGH REGISTER, ONE BIT AT A TIME
0CB
16
BYTE = HEX 13? (9-TRACK TAPE MARK)
YES
NO
ALL NINE BITS SAMPLED?
0E4
NO
YES
TEST IF TAPE MARK CODE
0E8
RESET TAPE MARK STATUS
17
0E5
LOAD IN COUNT FOR SENSING SHORT DATA RECORD. ALSO SET STATUS BIT 9
B

Figure A-3. Tape Read (Sheet 2 of 4)

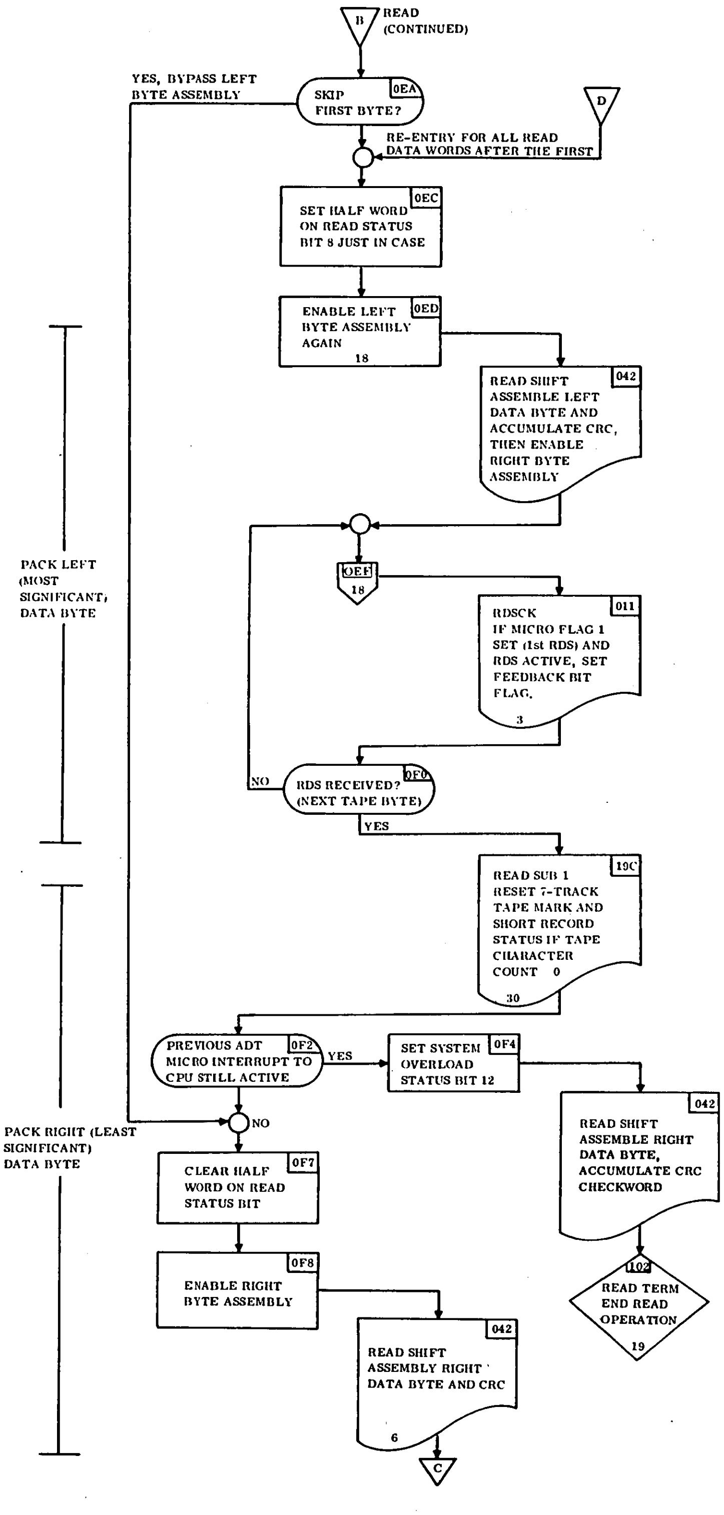
B
READ (CONTINUED)
YES, BYPASS LEFT BYTE ASSEMBLY
0EA SKIP FIRST BYTE?
D
RE-ENTRY FOR ALL READ DATA WORDS AFTER THE FIRST
0EC SET HALF WORD ON READ STATUS BIT 8 JUST IN CASE
0ED ENABLE LEFT BYTE ASSEMBLY AGAIN 18
042 READ SHIFT ASSEMBLE LEFT DATA BYTE AND ACCUMULATE CRC, THEN ENABLE RIGHT BYTE ASSEMBLY
PACK LEFT (MOST SIGNIFICANT) DATA BYTE
0EE 18
011 RDSCK IF MICRO FLAG 1 SET (1st RDS) AND RDS ACTIVE, SET FEEDBACK BIT FLAG. 3
NO
0F0 RDS RECEIVED? (NEXT TAPE BYTE)
YES
19C READ SUB 1 RESET 7-TRACK TAPE MARK AND SHORT RECORD STATUS IF TAPE CHARACTER COUNT 0 30
0F2 PREVIOUS ADT MICRO INTERRUPT TO CPU STILL ACTIVE
YES
0F4 SET SYSTEM OVERLOAD STATUS BIT 12
NO
PACK RIGHT (LEAST SIGNIFICANT) DATA BYTE
0F7 CLEAR HALF WORD ON READ STATUS BIT
0F8 ENABLE RIGHT BYTE ASSEMBLY
042 READ SHIFT ASSEMBLE RIGHT DATA BYTE, ACCUMULATE CRC CHECKWORD
102 READ TERM END READ OPERATION 19
042 READ SHIFT ASSEMBLY RIGHT DATA BYTE AND CRC 6
C

Figure A-3. Tape Read (Sheet 3 of 4)

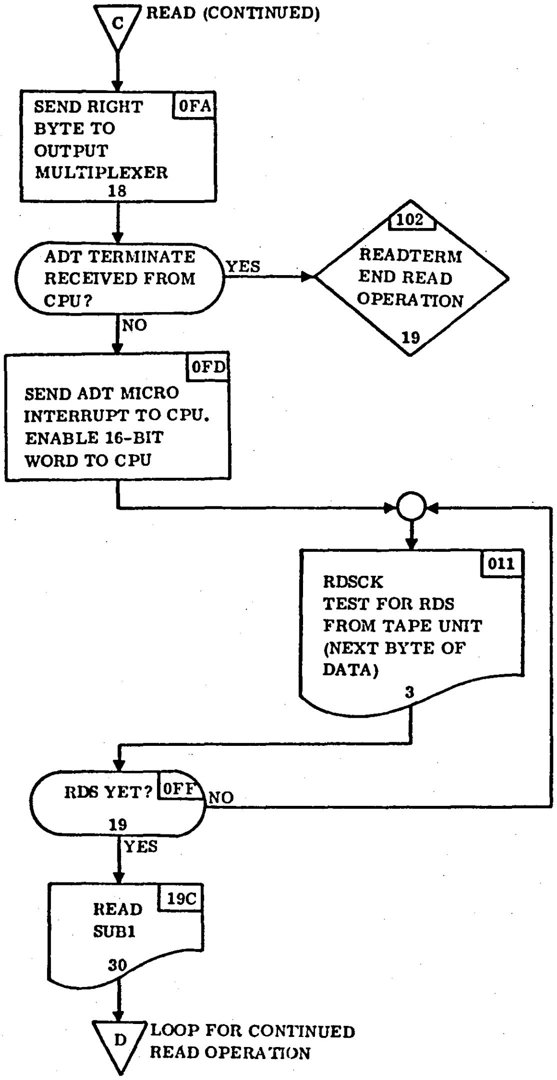
C
READ (CONTINUED)
SEND RIGHT BYTE TO OUTPUT MULTIPLEXER
0FA
18
ADT TERMINATE RECEIVED FROM CPU?
YES
102
READTERM END READ OPERATION
19
NO
0FD
SEND ADT MICRO INTERRUPT TO CPU. ENABLE 16-BIT WORD TO CPU
011
RDSCK TEST FOR RDS FROM TAPE UNIT (NEXT BYTE OF DATA)
3
RDS YET?
0FF
19
NO
YES
19C
READ SUB1
30
D
LOOP FOR CONTINUED READ OPERATION

Figure A-3. Tape Read (Sheet 4 of 4)

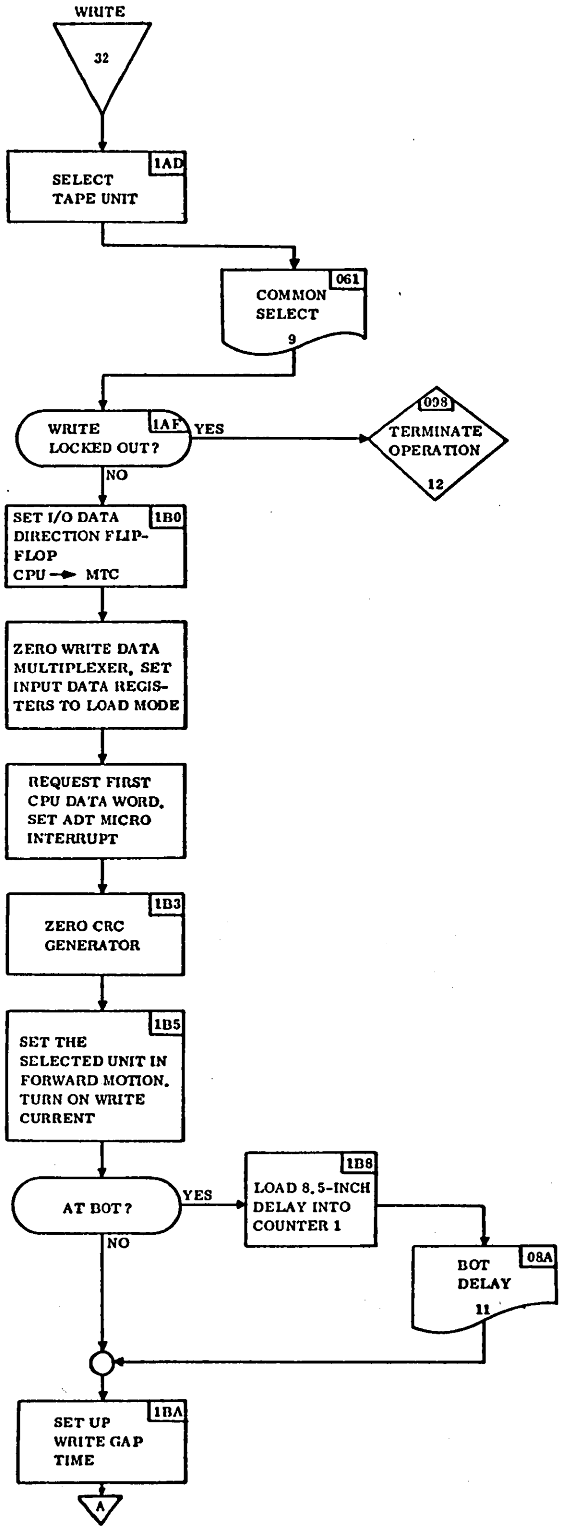
WRITE
32
1AD
SELECT TAPE UNIT
061
COMMON SELECT
9
WRITE LOCKED OUT?
1AF
YES
098
TERMINATE OPERATION
12
NO
SET I/O DATA DIRECTION FLIP-FLOP CPU → MTC
1B0
ZERO WRITE DATA MULTIPLEXER, SET INPUT DATA REGISTERS TO LOAD MODE
REQUEST FIRST CPU DATA WORD. SET ADT MICRO INTERRUPT
1B3
ZERO CRC GENERATOR
1B5
SET THE SELECTED UNIT IN FORWARD MOTION. TURN ON WRITE CURRENT
AT BOT?
YES
1B8
LOAD 8.5-INCH DELAY INTO COUNTER 1
NO
08A
BOT DELAY
11
1BA
SET UP WRITE GAP TIME
A

Figure A-4. Tape Write (Sheet 1 of 3)

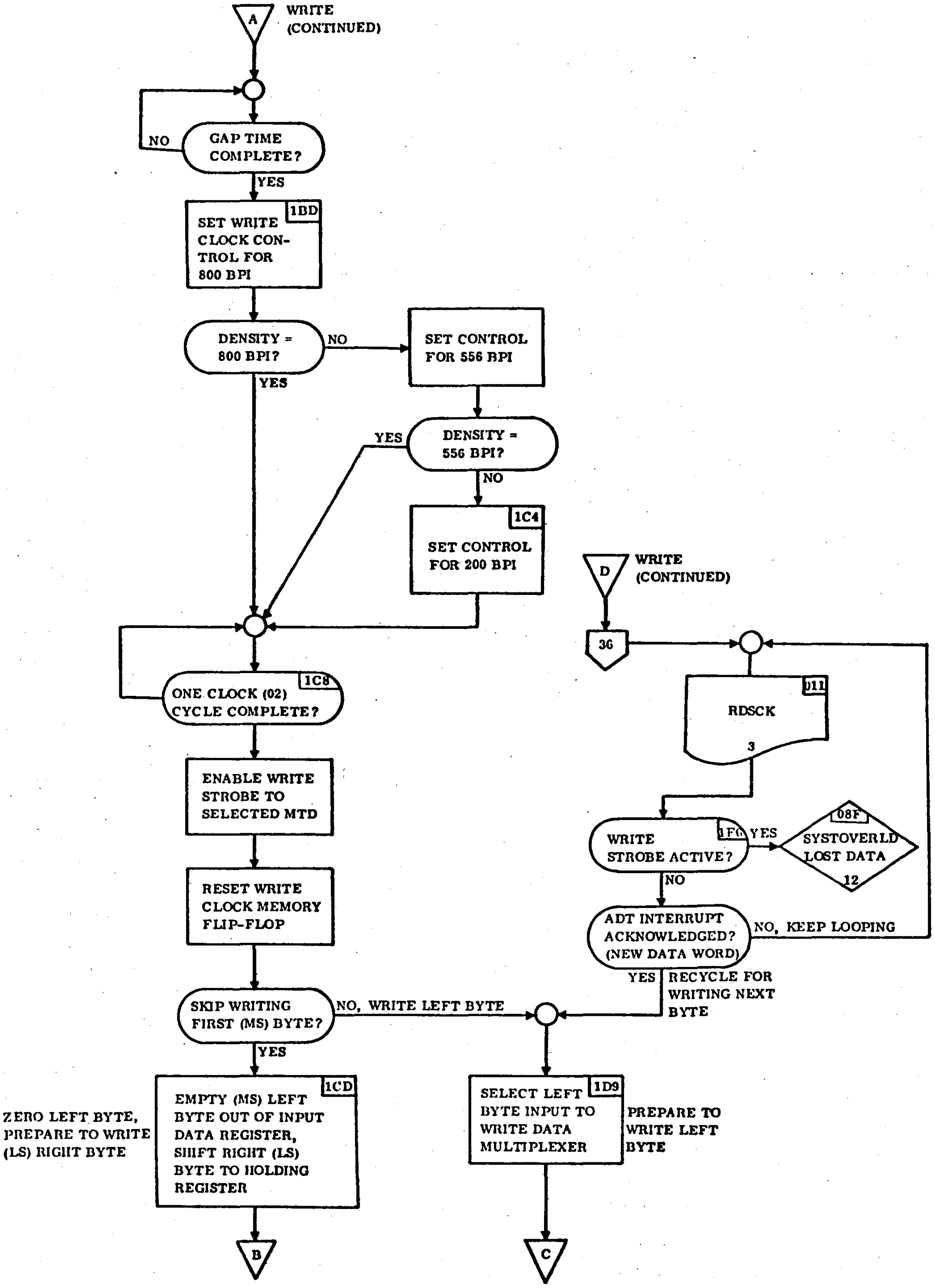
A
WRITE (CONTINUED)
NO
GAP TIME COMPLETE?
YES
1BD
SET WRITE CLOCK CONTROL FOR 800 BPI
DENSITY = 800 BPI?
NO
SET CONTROL FOR 556 BPI
YES
YES
DENSITY = 556 BPI?
NO
1C4
SET CONTROL FOR 200 BPI
D
WRITE (CONTINUED)
36
011
RDSCK
3
1C8
ONE CLOCK (02) CYCLE COMPLETE?
ENABLE WRITE STROBE TO SELECTED MTD
1FC
WRITE STROBE ACTIVE?
YES
08F
SYSTOVERLD LOST DATA
12
NO
RESET WRITE CLOCK MEMORY FLIP-FLOP
ADT INTERRUPT ACKNOWLEDGED? (NEW DATA WORD)
NO, KEEP LOOPING
YES
RECYCLE FOR WRITING NEXT BYTE
SKIP WRITING FIRST (MS) BYTE?
NO, WRITE LEFT BYTE
YES
1CD
ZERO LEFT BYTE, PREPARE TO WRITE (LS) RIGHT BYTE
EMPTY (MS) LEFT BYTE OUT OF INPUT DATA REGISTER, SHIFT RIGHT (LS) BYTE TO HOLDING REGISTER
1D9
SELECT LEFT BYTE INPUT TO WRITE DATA MULTIPLEXER
PREPARE TO WRITE LEFT BYTE
B
C

Figure A-4. Tape Write (Sheet 2 of 3)

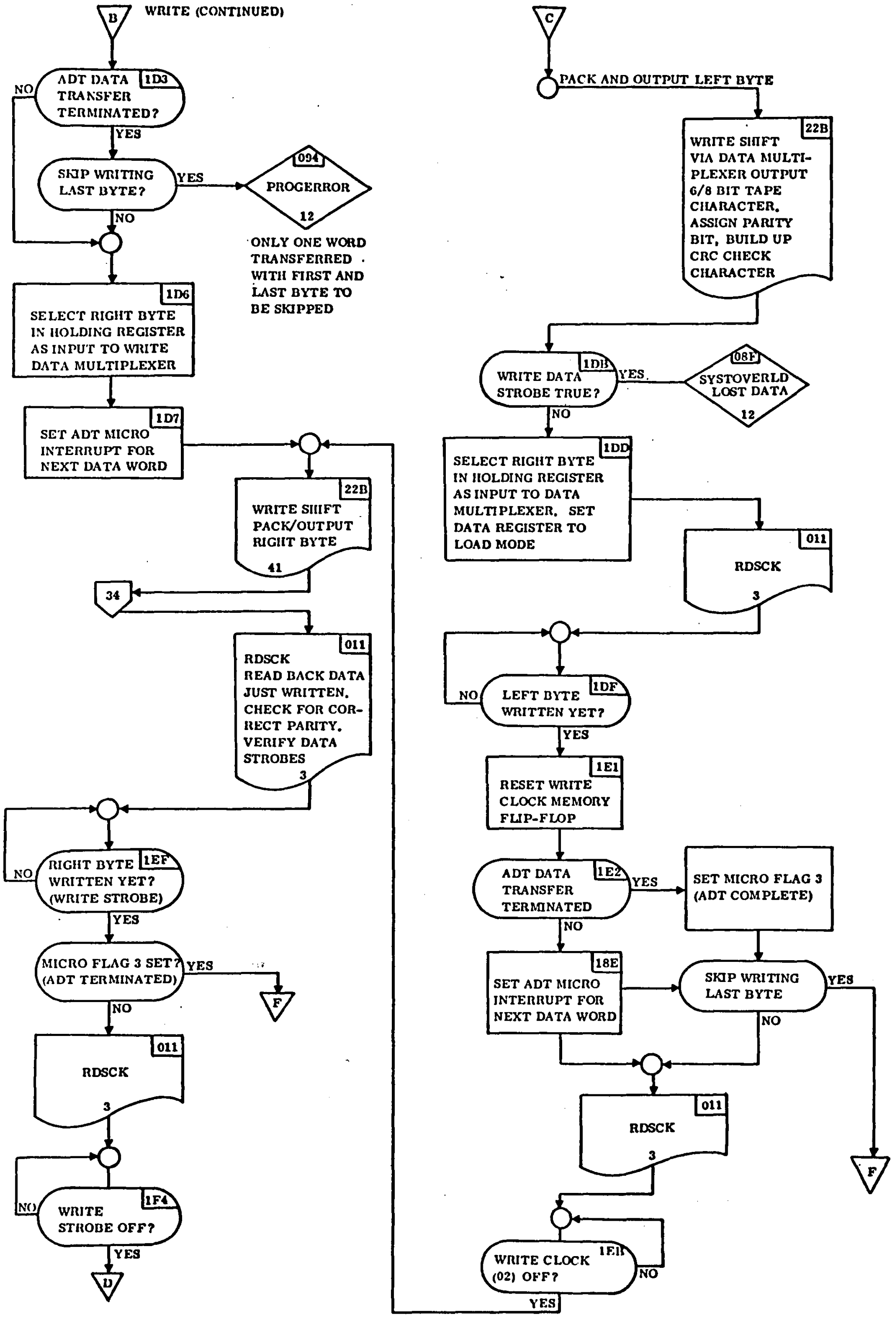
B
WRITE (CONTINUED)
ADT DATA TRANSFER TERMINATED?
1D3
NO
YES
SKIP WRITING LAST BYTE?
YES
094
PROGERROR
12
ONLY ONE WORD TRANSFERRED WITH FIRST AND LAST BYTE TO BE SKIPPED
NO
1D6
SELECT RIGHT BYTE IN HOLDING REGISTER AS INPUT TO WRITE DATA MULTIPLEXER
1D7
SET ADT MICRO INTERRUPT FOR NEXT DATA WORD
22B
WRITE SHIFT PACK/OUTPUT RIGHT BYTE
41
34
011
RDSCK
READ BACK DATA JUST WRITTEN. CHECK FOR CORRECT PARITY. VERIFY DATA STROBES
3
NO
RIGHT BYTE WRITTEN YET? (WRITE STROBE)
1EF
YES
MICRO FLAG 3 SET? (ADT TERMINATED)
YES
F
NO
011
RDSCK
3
NO
WRITE STROBE OFF?
1F4
YES
D
C
PACK AND OUTPUT LEFT BYTE
22B
WRITE SHIFT VIA DATA MULTIPLEXER OUTPUT 6/8 BIT TAPE CHARACTER. ASSIGN PARITY BIT, BUILD UP CRC CHECK CHARACTER
WRITE DATA STROBE TRUE?
1DB
YES
08F
SYSTOVERLD LOST DATA
12
NO
1DD
SELECT RIGHT BYTE IN HOLDING REGISTER AS INPUT TO DATA MULTIPLEXER. SET DATA REGISTER TO LOAD MODE
011
RDSCK
3
NO
LEFT BYTE WRITTEN YET?
1DF
YES
1E1
RESET WRITE CLOCK MEMORY FLIP-FLOP
ADT DATA TRANSFER TERMINATED
1E2
YES
SET MICRO FLAG 3 (ADT COMPLETE)
NO
18E
SET ADT MICRO INTERRUPT FOR NEXT DATA WORD
SKIP WRITING LAST BYTE
YES
NO
011
RDSCK
3
F
WRITE CLOCK (02) OFF?
1EB
NO
YES

Figure A-4. Tape Write (Sheet 3 of 3)

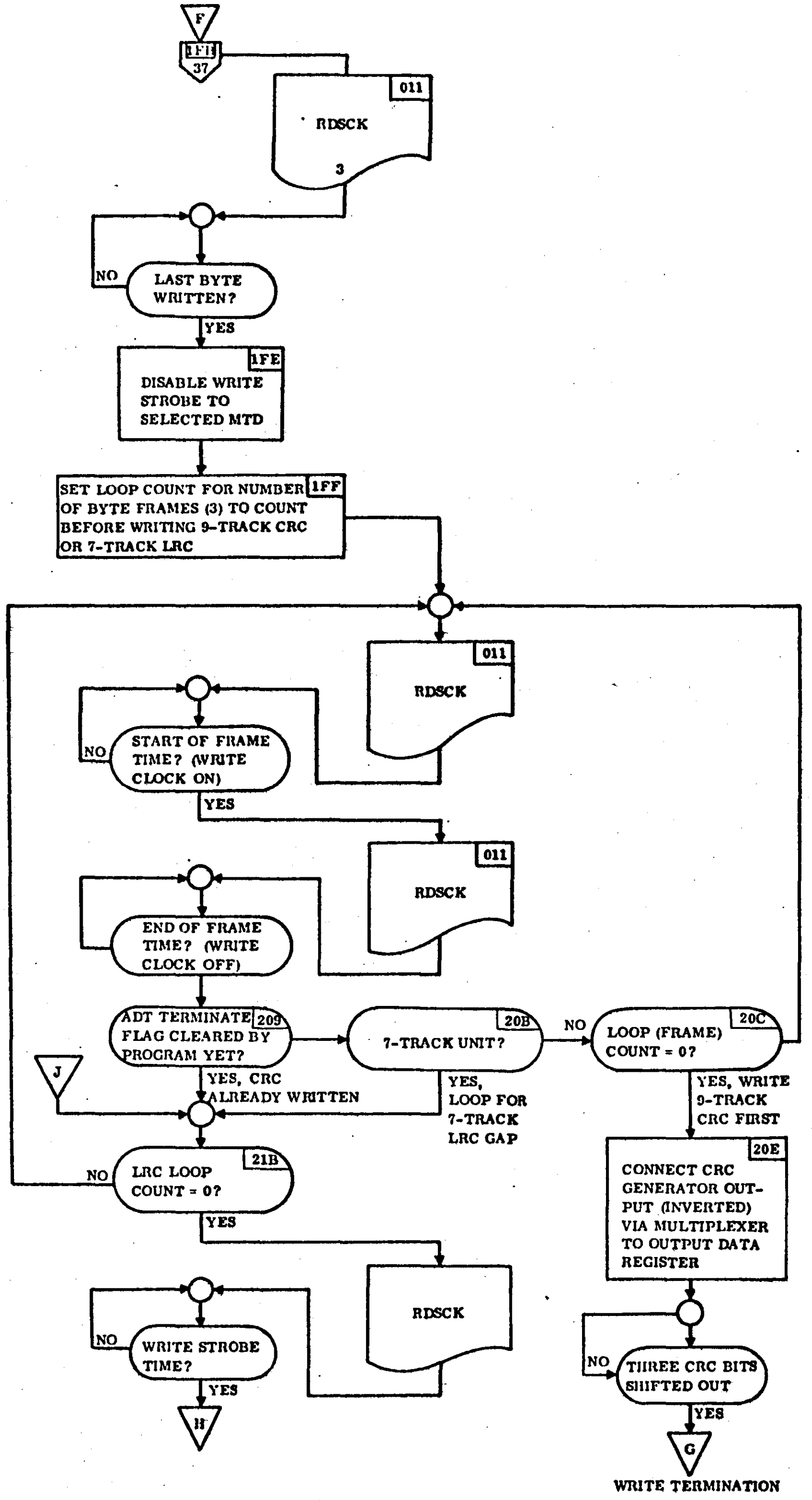
F
1FD
37
011
RDSCK
3
NO
LAST BYTE WRITTEN?
YES
1FE
DISABLE WRITE STROBE TO SELECTED MTD
SET LOOP COUNT FOR NUMBER OF BYTE FRAMES (3) TO COUNT BEFORE WRITING 9-TRACK CRC OR 7-TRACK LRC
1FF
011
RDSCK
NO
START OF FRAME TIME? (WRITE CLOCK ON)
YES
011
RDSCK
END OF FRAME TIME? (WRITE CLOCK OFF)
ADT TERMINATE FLAG CLEARED BY PROGRAM YET?
209
20B
7-TRACK UNIT?
NO
LOOP (FRAME) COUNT = 0?
20C
J
YES, CRC ALREADY WRITTEN
YES, LOOP FOR 7-TRACK LRC GAP
YES, WRITE 9-TRACK CRC FIRST
NO
LRC LOOP COUNT = 0?
21B
YES
20E
CONNECT CRC GENERATOR OUTPUT (INVERTED) VIA MULTIPLEXER TO OUTPUT DATA REGISTER
RDSCK
NO
WRITE STROBE TIME?
YES
H
NO
THREE CRC BITS SHIFTED OUT
YES
G
WRITE TERMINATION

Figure A-5. Write Termination (Sheet 1 of 2)

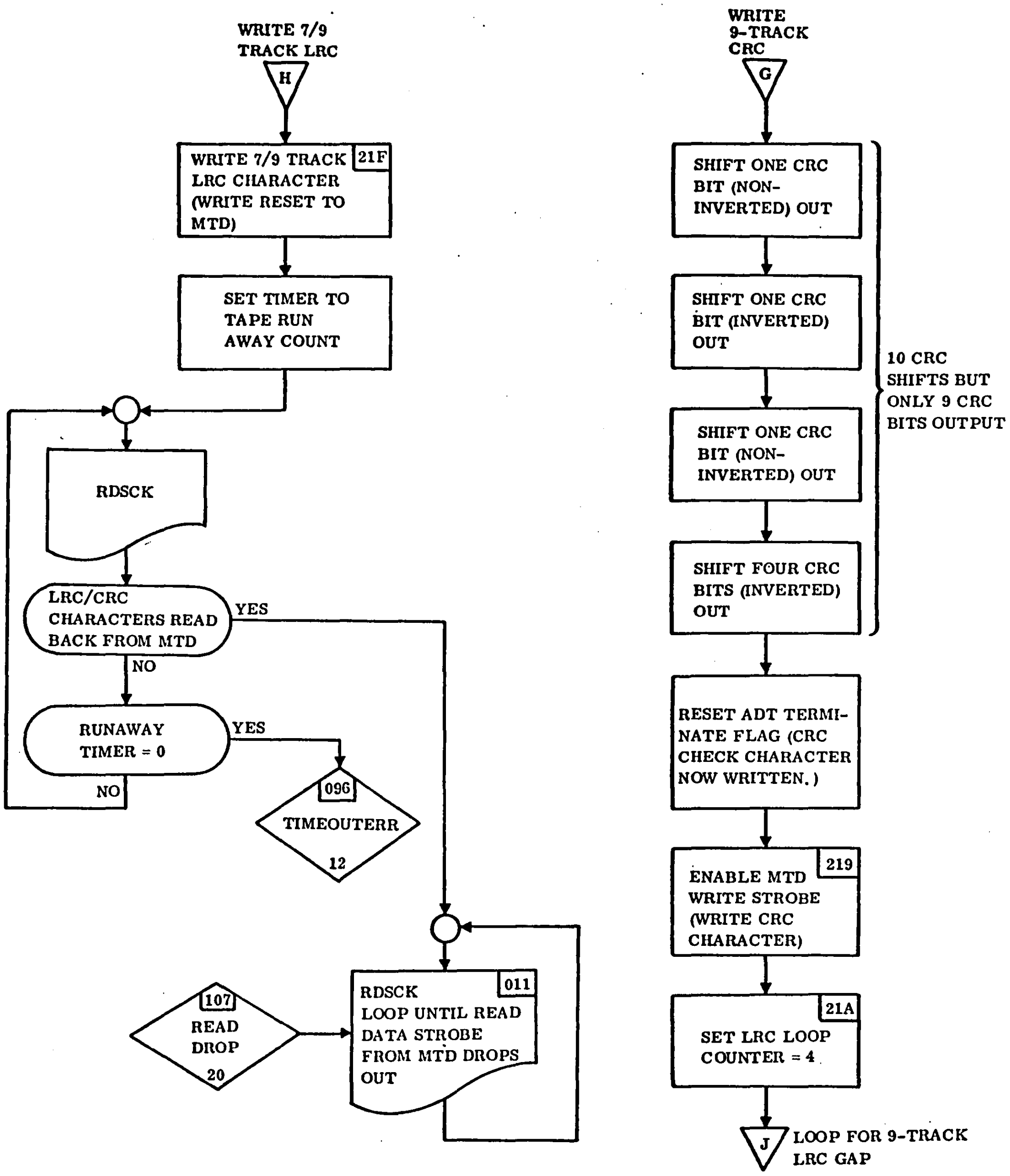
WRITE 7/9 TRACK LRC
H
WRITE 7/9 TRACK LRC CHARACTER (WRITE RESET TO MTD)
21F
SET TIMER TO TAPE RUN AWAY COUNT
RDSCK
LRC/CRC CHARACTERS READ BACK FROM MTD
YES
NO
RUNAWAY TIMER = 0
YES
NO
096
TIMEOUTERR
12
107
READ DROP
20
RDSCK LOOP UNTIL READ DATA STROBE FROM MTD DROPS OUT
011
WRITE 9-TRACK CRC
G
SHIFT ONE CRC BIT (NON-INVERTED) OUT
SHIFT ONE CRC BIT (INVERTED) OUT
SHIFT ONE CRC BIT (NON-INVERTED) OUT
SHIFT FOUR CRC BITS (INVERTED) OUT
10 CRC SHIFTS BUT ONLY 9 CRC BITS OUTPUT
RESET ADT TERMINATE FLAG (CRC CHECK CHARACTER NOW WRITTEN.)
ENABLE MTD WRITE STROBE (WRITE CRC CHARACTER)
219
SET LRC LOOP COUNTER = 4
21A
J
LOOP FOR 9-TRACK LRC GAP

Figure A-5. Write Termination (Sheet 2 of 2)

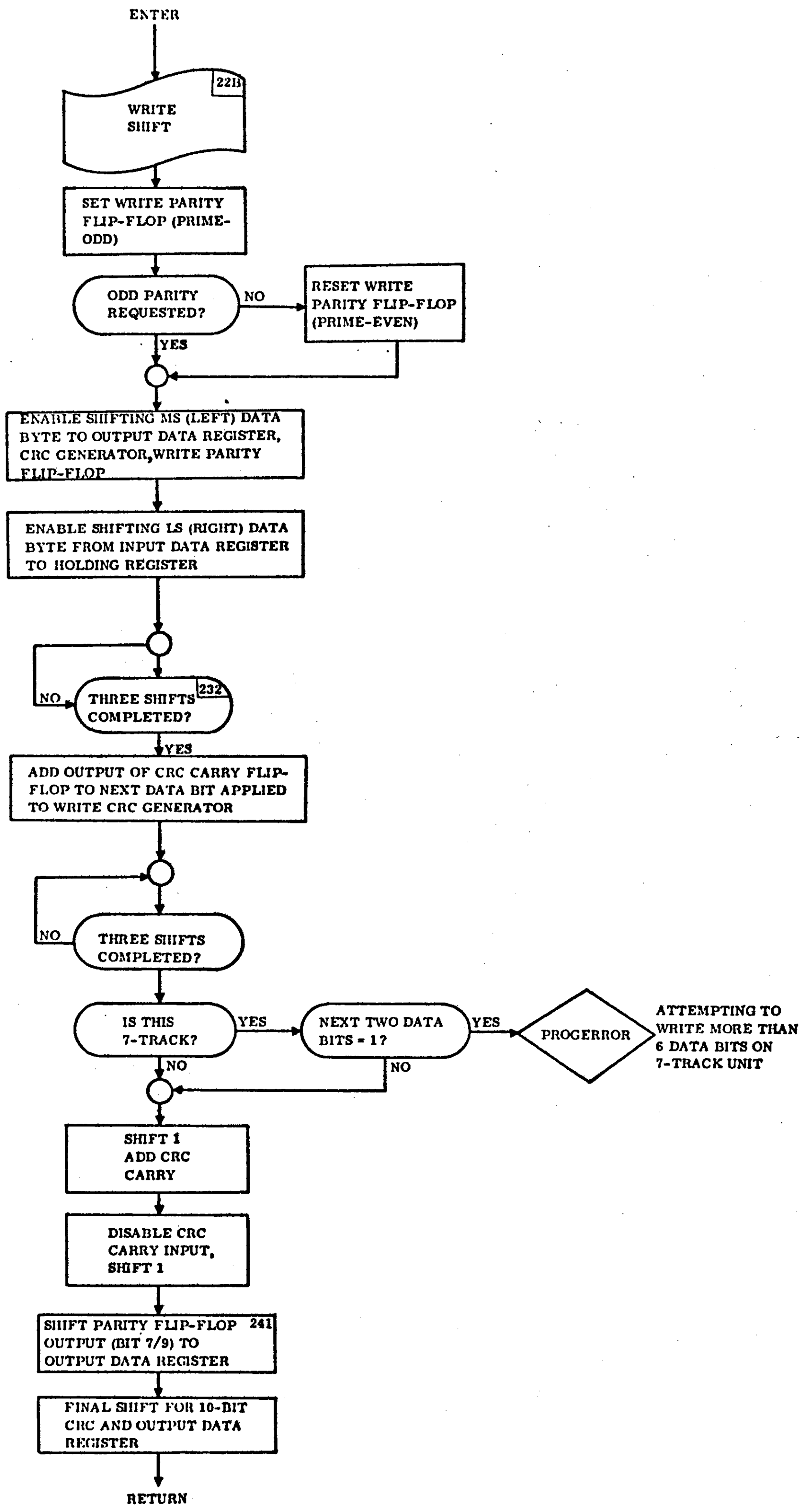
ENTER
22B
WRITE SHIFT
SET WRITE PARITY FLIP-FLOP (PRIME-ODD)
ODD PARITY REQUESTED?
NO
RESET WRITE PARITY FLIP-FLOP (PRIME-EVEN)
YES
ENABLE SHIFTING MS (LEFT) DATA BYTE TO OUTPUT DATA REGISTER, CRC GENERATOR,WRITE PARITY FLIP-FLOP
ENABLE SHIFTING LS (RIGHT) DATA BYTE FROM INPUT DATA REGISTER TO HOLDING REGISTER
NO
THREE SHIFTS COMPLETED?
232
YES
ADD OUTPUT OF CRC CARRY FLIP-FLOP TO NEXT DATA BIT APPLIED TO WRITE CRC GENERATOR
NO
THREE SHIFTS COMPLETED?
IS THIS 7-TRACK?
YES
NEXT TWO DATA BITS = 1?
YES
PROGERROR
ATTEMPTING TO WRITE MORE THAN 6 DATA BITS ON 7-TRACK UNIT
NO
NO
SHIFT 1 ADD CRC CARRY
DISABLE CRC CARRY INPUT, SHIFT 1
SHIFT PARITY FLIP-FLOP OUTPUT (BIT 7/9) TO OUTPUT DATA REGISTER
241
FINAL SHIFT FOR 10-BIT CRC AND OUTPUT DATA REGISTER
RETURN

Figure A-6. Write Shift Subroutine

```
634-HP-TAPE

MICRO CONTROL

PROGRAM

B. ROOT

27 SEPTEMBER 72
```

```
PAGE   1                               TAPEMCON06                                        DATE    27/09/78

SEQ NO  REFERENCE ORCODE MD EA EB EC OPERANDS   COMMENTS                                 ADRS  MEMORY  BINARY REPRESENTATION

000000            BRANCH             PROGERROR                                           0000  6094    0110 0000 1001 0100

000001            BRANCH             READ                                                0001  60AA    0110 0000 1010 1010

000002            BRANCH             WRITE                                               0002  61AD    0110 0001 1010 1101

000003            BRANCH             ERASE                                               0003  6245    0110 0010 0100 0101

000004            BRANCH             BACKSPACE                                           0004  6258    0110 0010 0101 1000

000005            BRANCH             REWIND                                              0005  626F    0110 0010 0110 1111

000006            BRANCH             REWINDUNLD                                          0006  6272    0110 0010 0111 0010

000007            BRANCH             WRITETMARK                                          0007  6276    0110 0010 0111 0110

000008            BRANCH             SELECT                                              0008  629F    0110 0010 1001 1111

000009            BRANCH             RECOVREAD                                           0009  62A4    0110 0010 1010 0100

000010            BRANCH             CONTBACKSP                                          000A  62AB    0110 0010 1010 1011

000011 ENTRY1B    BRANCH             DTEST6                                              000B  6300    0110 0011 0000 0000

000012 ENTRY1C    BRANCH             DTEST7                                              000C  62ED    0110 0010 1110 1101

000013 ENTRY1D    BRANCH             DTEST5                                              000D  62E0    0110 0010 1110 0000

000014 ENTRY1E    BRANCH             A                                                   000E  6010    0110 0000 0001 0000

000015 REST       EA          08                PROGRAM INT                              000F  1F08    0001 1111 0000 1000

000016 A          REST                                                                   0010  0000    0000 0000 0000 0000
```

```
PAGE   2                                          TAPEMCON06                                          DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION
```

```
PAGE  3                           TAPEMCON04                                          DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                              ADRS  MEMORY  BINARY REPRESENTATION
040020 **
040030 *          COMMON READ STROBE CHECK ROUTINE
040040 *                F2 IS ON IF READ, OFF IF WRITE
040050 *                F1 IS SET WHEN FIRST RDS DETECTED
040060 *                F0 IS SET ON IF RDS DETECTED ON ANY SPECIFIC ENTRY
040070 *
040120 RDSCK      BRNB   F1          RDSCK1    IF RDS YET, GO TO RDSCK1.             0011  9416    1001 0100 0001 0110
040140            TESTB              14        ST. COMPLETE?  (DROPOUT)              0012  800E    1000 0000 0000 1110
040160            BRNB               RDSCK1    NO, CHECK FOR RDS                     0013  9016    1001 0000 0001 0110
040180            BRB    F2          READDROP  YES, GO TO READDROP IF READ,          0014  A907    1010 1001 0000 0111
040200            BRANCH             WRITEDROP OTHERWISE GO TO WRITEDROP.            0015  6228    C110 0010 0010 1000
040220 RDSCK1     TESTB              16        RDS ON?                               0016  8010    1000 0000 0001 0000
040240            BRB                RDSCK1A   YES, PROCESS                          0017  A019    1010 0000 0001 1001
040260            RETURN                       NO, RETURN                            0018  2000    0010 0000 0000 0000
040280 RDSCK1A    PAREN  06          08        SET F1 ON                             0019  1608    0001 0110 0000 1000
040300            PAREN  04          30        LD ST. 75USEC, 800 BPI C25IPS         001A  141E    0001 0100 0001 1110
040320            TESTB              5         DENSITY 1 ON?                         001B  8005    1000 0000 0000 0101
```

```
PAGE   4                                            TAPEMCON04                                        DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                      ADRS  MEMORY  BINARY REPRESENTATION

040340            BRB                RDSCK2    YES, CHECK FOR 200 BPI                        001C  A01F    1010 0000 0001 1111

040360            PAREN  04          43        LD ST. 108USEC, 556 BPI 825IPS.               001D  142B    0001 0100 0010 1011

040380            BRANCH             RDSCK3                                                  001E  6022    0110 0000 0010 0010

040400 RDSCK2     TESTB              6         DENSITY 2 ON?                                 001F  8006    1000 0000 0000 0110

040420            BRNB               RDSCK3    NO, MUST BE 800 BPI.                          0020  9022    1001 0000 0010 0010

040440            PAREN  04          120       YES, LOAD S.T. 300 USEC (200 BPI)             0021  1478    0001 0100 0111 1000

040520 RDSCK3     TESTB              36        IS F4 ON?  (ODD-EVEN FLAG)                    0022  8024    1000 0000 0010 0100

040540            PAREN  06          03        SET F4 OFF                                    0023  1603    0001 0110 0000 0011

040560            BRB                RDSCK4    YES, GO TO RDSCK4                             0024  A026    1010 0000 0010 0110

040580            PAREN  06          0B        NO, SET F4 ON (ODD BYTE)                      0025  160B    0001 0110 0000 1011

041120 RDSCK4     EA&EB     15   4             RESET RDS, SET FF FOR ODD PARITY CHECK        0026  1F4F    0001 1111 0100 1111

041140            TESTB              7         EVEN PARITY DESIGNATED?                       0027  8007    1000 0000 0000 0111

041160            BRNB               RDSCK4A                                                 0028  902A    1001 0000 0010 1010

041180            EA        14                 SET FF FOR EVEN PARITY CHECK                  0029  1F0E    0001 1111 0000 1110

041200 RDSCK4A    PAREN  08          0B        PUT READ REG INTO SHIFT MODE                  002A  180B    0001 1000 0000 1011

041210            PAREN  08          02        RESET TIE INVERSION ENABLE TERM               002B  1802    0001 1000 0000 0010

041215            PAREN  08          07        RECIRCULATE READ REGISTER                     002C  1807    0001 1000 0000 0111
```

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PAGE    8                                        TAPEMCON06                                        DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION

041220            LDLC2                 8           SETUP TO SHIFT 9 TIMES                       002D  5008    0101 0000 0000 1000

041230            PAREN  09             EF          SET EC5                                      002E  19EF    0001 1001 1110 1111

041240 RDSCK4B    EC                                SHIFT 9 TIMES                                002F  3000    0011 0000 0000 0000

041250            LOOP2                 RDSCK4B                                                  0030  D02F    1101 0000 0010 1111

041260            TESTB                 24          PARITY ERROR FOUND?                          0031  8018    1000 0000 0001 1000

041270            EC                                                                             0032  3000    0011 0000 0000 0000

041280            BRNB                  RDSCK5      NO, GO TO RDSCK5                             0033  903F    1001 0000 0011 1111

041300            TESTB                 8           7 TRACK?                                     0034  8008    1000 0000 0000 1000

041320            BRNB                  RDSCK4C     NO, GO TO RDSCK4C                            0035  9038    1001 0000 0011 1000

041340 RDSCK4B1   PAREN  05             01          SET STATUS BIT 14 (DATA ERROR).              0036  1501    0001 0101 0000 0001

041360            BRANCH                RDSCK5                                                   0037  603F    0110 0000 0011 1111

041380 RDSCK4C    BRNB   F2             RDSCK4B1    IF NOT READ, GO TO RDSCK4B1                  0038  9836    1001 1000 0011 0110

041400            TESTB                 29          ERROR CORRECTION POSSIBLE?                   0039  801D    1000 0000 0001 1101

041420            BRB                   RDSCK4D     YES, GO TO RDSCK4D                           003A  A03E    1010 0000 0011 1110

041440            PAREN  07             07          NO, ENABLE 1 TO E REG.                       003B  1707    0001 0111 0000 0111

041460            PAREN  05             01          SET STATUS BIT 14 (DATA ERROR).              003C  1501    0001 0101 0000 0001

041480            BRANCH                RDSCKRET                                                 003D  6040    0110 0000 0100 0000
```

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PAGE   6                              TAPEMCON06                                                DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                 ADRS  MEMORY   BINARY REPRESENTATION

041490 RDSCKSD    PAREN  08          0A        ENABLE INVERSON ON ERROR TRACK.          003E  180A     0001 1000 0000 1010

041500 RDSCKS     BRNS   F2          RDSHIFT   IF NOT READ GO TO RDSHIFT                003F  9842     1001 1000 0100 0010

041520 RDSCKRET   TESTB              0         SET BIT FLAG TO A ONE,                   0040  8000     1000 0000 0000 0000

041540            RETURN                       RETURN                                   0041  2000     0010 0000 0000 0000

045120 RDSHIET    PAREN  08          0D                                                 0042  180D     0001 1000 0000 1101

045130            PAREN  09          4D        SET EC2,EC5,EC6,EC8                      0043  194D     0001 1001 0100 1101

045140            EC           5               ENABLE CRC FF, SHIFT NO. 1               0044  3F50     0011 1111 0101 0000

045160            EC                           SHIFT NO. 2                              0045  3000     0011 0000 0000 0000

045180            EC                           SHIFT NO. 3                              0046  3000     0011 0000 0000 0000

045200            PAREN  08          0C                                                 0047  180C     0001 1000 0000 1100

045220            LDLC2              3         SHIFT                                    0048  5003     0101 0000 0000 0011

045240 RDSHIET1   EC                                 FOUR                               0049  3000     0011 0000 0000 0000

045250            LOOP2              RDSHIFT1              TIMES                        004A  0049     1101 0000 0100 1001

045260            PAREN  08          04                                                 004B  1804     0001 1000 0000 0100

045280            EC                           SHIFT NO. 8                              004C  3000     0011 0000 0000 0000

045300            PAREN  08          00                                                 004D  1800     0001 1000 0000 0000

045320            PAREN  08          01                                                 004E  1801     0001 1000 0000 0001
```

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PAGE   7                                 TAPEMCON06                                      DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                        ADRS  MEMORY  BINARY REPRESENTATION

045340            EC                           SHIFT NO. 9                     004F  3000    0011 0000 0000 0000

045360            PAREN  C8          05                                        0050  1805    0001 1000 0000 0101

045380            BRNB   F2          RDSHIFTRET                                0051  9850    1001 1000 0101 1101

045390            PAREN  C9          F7        SET EC4                         0052  19F7    0001 1001 1111 0111

045400            EC           6               SHIFT 'E' REG. AND SET FF       0053  3F60    0011 1111 0110 0000

045420            PAREN  07          00                                        0054  1700    0001 0111 0000 0000

045430            EC                           SHIFT NO. 2                     0055  3000    0011 0000 0000 0000

045440            EC                           SHIFT NO. 3                     0056  3000    0011 0000 0000 0000

045450            LDLC2              3         SHIFT                           0057  5003    0101 0000 0000 0011

045460 RDSHIFT2   EC           5                  FOUR                         0058  3F05    0011 1111 0000 0101

045480            LOOP2              RDSHIFT2         TIMES                    0059  D058    1101 0000 0101 1000

045500            EC                           SHIFT NO. 8                     005A  3000    0011 0000 0000 0000

045510            EC                           SHIFT NO. 9                     005B  3000    0011 0000 0000 0000

045520            EC                           LHIFT NO. 10                    005C  3000    0011 0000 0000 0000

045540 RDSHIFTRET TESTB              0                                         005D  8600    1000 0000 0000 0000

045560            PAREN  09          7D        SET EC2, EC8                    005E  197D    0001 1001 0111 1101

045580            EC     08          03        FINAL SHIFT                     005F  3803    0011 1000 0000 0011
```

```
PAGE  8                              TAPEMCON06                                       DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                            ADRS  MEMORY  BINARY REPRESENTATION
048600            RETURN                                                           0060  2000    0010 0000 0000 0000
```

```
PAGE   9                                             TAPEMCON06                                   DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                 ADRS  MEMORY  BINARY REPRESENTATION

080020 **        COMMON SELECT ROUTINE

080060 COMSELECT  EAEEB     2  2                 RESET TERMINATE AND COMMAND REG.         0061  1F22    0001 1111 0010 0010

080080            EAEEB    12  1                 CLEAR WRITE CRC, READ REGS AND SELECT    0062  1F1C    0001 1111 0001 1100

080100 COMSELO    TESTB                15        LONG TIMER COMPLETE?                     0063  800F    1000 0000 0000 1111

080120            BRNB                 COMSELO   NO, WAIT                                 0064  9063    1001 0000 0110 0011

080140            EAEEB     3  4                 SET SELECT, CLEAR RDS.                   0065  1F43    0001 1111 0100 0011

080160            PAREN  06            0C        RESET STATUS BIT 1                       0066  160C    0001 0110 0000 1100

080180            PAREN  06            0E        RESET STATUS BIT 4                       0067  160E    0001 0110 0000 1110

080200            PAREN  06            0D        RESET STATUS BIT 5                       0068  160D    0001 0110 0000 1101

080220            PAREN  06            0F        RESET STATUS BIT 7                       0069  160F    0001 0110 0000 1111

080240            PAREN  05            0F        RESET STATUS BIT 8                       006A  150F    0001 0101 0000 1111

080260            PAREN  05            0E        RESET STATUS BIT 9                       006B  150E    0001 0101 0000 1110

080280            PAREN  05            0D        RESET STATUS BIT 10                      006C  150D    0001 0101 0000 1101

080300            PAREN  05            0C        RESET STATUS BIT 11                      006D  150C    0001 0101 0000 1100

080320            PAREN  05            0B        RESET STATUS BIT 12                      006E  150B    0001 0101 0000 1011

080340            PAREN  05            0A        RESET STATUS BIT 13                      006F  150A    0001 0101 0000 1010

080360            PAREN  05            09        RESET STATUS BIT 14                      0070  1509    0001 0101 0000 1001
```

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PAGE 10                                   TAPEMCON06                                  DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                          ADRS  MEMORY  BINARY REPRESENTATION
050380            PAREN  05          08        RESET STATUS BIT 15               0071  1508    0001 0101 0000 1000
050400            PAREN  06          00        CLEAR FLAG 1                      0072  1600    0001 0110 0000 0000
050420            PAREN  06          01        CLEAR FLAG 2                      0073  1601    0001 0110 0000 0001
050440            PAREN  06          02        CLEAR FLAG 3                      0074  1602    0001 0110 0000 0010
050460            PAREN  06          03        CLEAR FLAG 4                      0075  1603    0001 0110 0000 0011
050480            TESTB              23        REWINDING ?                       0076  8017    1000 0000 0001 0111
050500            BRB                REWINDING                                   0077  A09A    1010 0000 1001 1010
050520            TESTB              19        READY ?                           0078  8013    1000 0000 0001 0011
050540            BRB                COMSEL1   YES, GO TO COMSEL1                0079  A07C    1010 0000 0111 1100
050560            PAREN  06          04        NO, SET STATUS BIT 1.  (INOPERATIVE)  007A  1604    0001 0110 0000 0100
050580            BRANCH             TERM2                                       007B  60A4    0110 0000 1010 0100
051120  COMSEL1   TESTB              8         7 CHANNEL?                        007C  8008    1000 0000 0000 1000
051140            BRB                COMSEL2   YES, GO TO COMSEL2                007D  A085    1010 0000 1000 0101
051160            TESTB              7         NO, CHECK PARITY (9 CH. MUST BE ODD)  007E  8007    1000 0000 0000 0111
051180            BRB                PROGERROR ERROR IF EVEN.                    007F  A094    1010 0000 1001 0100
051200            TESTB              5         CHECK DENSITY 1.(800 BPI REQUIRED)  0080  8005    1000 0000 0000 0101
051220            BRNB               PROGERROR ERROR IF 0                        0081  9094    1001 0000 1001 0100
```

```
PAGE  11                                       TAPEMCON06                                         DATE    27/09/78
SEQ NO  REFERENCE OPCODE MO EA EB EC OPERANDS  COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

081240 COMSEL1A   TESTB            6           CHECK DENSITY 2                         0082  8006    1000 0000 0000 0110
081260            BRB              PROGERROR   ERROR IF 200 BPI                        0083  A094    1010 0000 1001 0100
081300            BRANCH           COMSELRET                                           0084  6089    0110 0000 1000 1001
081320 COMSEL2    TESTA            5           DENSITY 1 ON?                           0085  8005    1000 0000 0000 0101
081340            BRB              COMSELRET   YES, GO TO COMSELRET                    0086  A089    1010 0000 1000 1001
081360            TESTA            6           DENSITY 2 ON?                           0087  8006    1000 0000 0000 0110
081380            BRNB             PROGERROR   ERROR IF 1600 BPI                       0088  9094    1001 0000 1001 0100
081400 COMSELRET  RETURN                                                               0089  2000    0010 0000 0000 0000
060120 BOTDELAY   PAREN  03        16          LOAD LT.  4 MS.  (.1 INCH)              008A  1310    0001 0011 0001 0000
060140 BOTDELAY1  TESTB            15          LT. COMPLETE?                           008B  800F    1000 0000 0000 1111
060160            BRNB             BOTDELAY1   NO, LOOP                                008C  908B    1001 0000 1000 1011
060180            LOOP1            BOTDELAY                                            008D  C08A    1100 0000 1000 1010
060280            RETURN       4               RESET RDB AND RETURN                    008E  2F40    0010 1111 0100 0000
```

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PAGE 12                                  TAPEMCON06                                               DATE    27/09/78
SEQ NO REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

070020 **        ERROR EXITS

070120 SYSTOVERLD PAREN  05         03         SET STATUS BIT 12                      008F  1503    0001 0101 0000 0011

070130            PAREN  02         06         DISABLE WRITE STROBE                   0090  1206    0001 0010 0000 0110

070140            BRANCH            TERMINATE                                         0091  609C    0110 0000 1001 1100

070160 DROPOUTERR PAREN  05         04                                                0092  1504    0001 0101 0000 0100

070180            BRANCH            TERMINATE                                         0093  609C    0110 0000 1001 1100

070220 PROGERROR  PAREN  06         C7         SET STATUS BIT 7                       0094  1607    0001 0110 0000 0111

070240            BRANCH            TERM1                                             0095  60A3    0110 0000 1010 0011

070260 TIMOUTERR  PAREN  05         05                                                0096  1505    0001 0101 0000 0101

070280            BRANCH            TERMINATE                                         0097  609C    0110 0000 1001 1100

070320 WRITELOCK  PAREN  06         05         SET STATUS BIT 5.                      0098  1605    0001 0110 0000 0101

070340            BRANCH            TERM2                                             0099  60A4    0110 0000 1010 0100

070380 REWINDING  PAREN  06         C6         SET STATUS BIT 3                       009A  1606    0001 0110 0000 0110

070400            BRANCH            TERM2                                             009B  60A4    0110 0000 1010 0100

070440 TERMINATE  BRB    F2         TERMOA     IF READ, GO TO TERMOA                  009C  A8A0    1010 1000 1010 0000

070460            PAREN  03         16         SET L.T. FOR 4 MS (.10 INCH)           009D  1310    0001 0011 0001 0000

070480 TERMO      TESTB             15         L. T. COMPLETE?                        009E  800F    1000 0000 0000 1111
```

```
PAGE  13                                      TAPEMCONO4                                       DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

070700           BRNB             TERM0     NO, LOOP BACK-TEST AGAIN                 009F  909E    1001 0000 1001 1110

070720 TERM0A    TESTB            19        READY ?                                  00A0  8013    1000 0000 0001 0011

070740           BRB              TERM1     YES, GO TO TERM1                         00A1  A0A3    1010 0000 1010 0011

070760           PAREN  05        02        SET STATUS BIT 13=INOP DURING EXECUTION  00A2  1502    0001 0101 0000 0010

070780 TERM1     PAREN  03        64        SET TIMER FOR STOP DELAY                 00A3  1340    0001 0011 0100 0000

070800 TERM2     LDLC1            255                                                00A4  40FF    0100 0000 1111 1111

070820 TERM2A    TESTB            10        DATA REQUEST ACTIVE?                     00A5  800A    1000 0000 0000 1010

070840           BRNB             TERM3     NO, TERMINATE                            00A6  90A8    1001 0000 1010 1000

070860           LOOP1            TERM2A    IF STILL ACTIVE, CHECKAGAIN              00A7  C0A5    1100 0000 1010 0101

070880 TERM3     EA&EB      8  2            REQUEST INTERRUPT, RESET COMMAND REG'    00A8  1F28    0001 1111 0010 1000

070900           REST                                                                00A9  0000    0000 0000 0000 0000
```

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PAGE  1A                                  TAPEMCON06                                       DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                            ADRS  MEMORY  BINARY REPRESENTATION

100020 **        READ

100120 READ      JUMP              COMSELECT                                        00AA  7061    0111 0000 0110 0001

100140           TESTB             17         READ-AFTER-WRITE?                     00AB  8C11    1000 0000 0001 0001

100160           BRNB              READ1      NO, GO TO READ1                       00AC  90AF    1001 0000 1010 1111

100180           PAREN  11         00         SET READ-AFTER-WRITE STATUS (BIT 4)   00AD  1B00    0001 1011 0000 0000

100200           BRANCH            TERM2      TERMINATE                             00AE  60A4    0110 0000 1010 0100

101120 READ1     PAREN  06         09         SET FLAG 2                            00AF  1609    0001 0110 0000 1001

101130           PAREN  08         08         ENABLE BC1                            00B0  1808    0001 1000 0000 1000

101133           JUMP              READSUB2   PERFORM READSUB2-CLEAR LH BYTE        00B1  71A3    0111 0001 1010 0011

101136           PAREN  08         00         RESET BC1                             00B2  18C0    0001 1000 0000 0000

101138           EB          4                RESET RDS                             00B3  1F40    0001 1111 0100 0000

101140           PAREN  02         08         FWD ON                                00B4  1208    0001 0010 0000 1000

101150           EA        7                  INPUT DATA  (MTU TO PROC.)            00B5  1F07    0001 1111 0000 0111

101160           TESTB             20         BOT?                                  00B6  8014    1000 0000 0001 0100

101180           BRNB              READ2      NO, BYPASS BOT DELAY                  00B7  90BA    1001 0000 1011 1010

101200           LDLC1             30         LOAD LENGTH OF DELAY (3.0 INCHES)     00B8  401E    0100 0000 0001 1110

101220           JUMP              BOTDELAY   PERFORM DELAY                         00B9  708A    0111 0000 1000 1010
```

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PAGE  15                                    TAPEMCOND6                                          DATE   27/09/78

SEQ NO. REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                    ADRS  MEMORY  BINARY REPRESENTATION

102120 READ2      LDLC1              29        TIMEOUT COUNT (30 FEET)                     008A  401D    0100 0000 0001 1101

102140 READ2A     LDLC2              11        TIMEOUT COUNT (12 INCHES)                   008B  500B    0101 0000 0000 1011

102160 READ2B     PAREN  03          160       LOAD L.T. 40 MS. (1 INCH)                   008C  13A0    0001 0011 1010 0000

102180 READ2C     JUMP               RDSCK     CHECK FOR READ DATA STROBE                  008D  7011    0111 0000 0001 0001

102200            BRB    F1          READ3     IF RDS, GO TO READ3                         008E  A4C5    1010 0100 1100 0101

102220            TESTB              15        L.T. COMPLETE?                              008F  800F    1000 0000 0000 1111

102240            BRNB               READ2C    NO, CONTINUE SEARCH FOR RDS                 00C0  908D    1001 0000 1011 1101

102260            LOOP2              READ2B    YES, NEXT INCH                              00C1  D0BC    1101 0000 1011 1100

102280            LOOP1              READ2A    NEXT FOOT                                   00C2  C0BB    1100 0000 1011 1011

102300            PAREN  05          05        SET TIMEOUT STATUS (BIT 10)                 00C3  1505    0001 0101 0000 0101

102320            BRANCH             TERMINATE                                             00C4  609C    0110 0000 1001 1100

103120 READ3      PAREN  05          00        SET TAPE MARK STATUS                        00C5  1500    0001 0101 0000 0000

103140            LDLC1              1         LC1 USED TO DETECT TAPE MARK ON 7 CH'       00C6  4001    0100 0000 0000 0001

103160            TESTB              8         9 CHANNEL?                                  00C7  8008    1000 0000 0000 1000

103180            BRB                READ4     NO, GO TO READ 4                            00C8  A0EA    1010 0000 1110 1010

103200            PAREN  08          08        READ REG TO SHIFT MODE                      00C9  180B    0001 1000 0000 1011

103220            PAREN  08          07        RE-CIRCULATE READ REG                       00CA  1807    0001 1000 0000 0111
```

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SEQ NO. REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                          ADRS  MEMORY  BINARY REPRESENTATION

103240            LDLC1             9                                             00CB  4009    0100 0000 0000 1001
103250            LDLC2             1                                             00CC  5001    0101 0000 0000 0001
103260 READ3A     TESTB             11                                            00CD  800B    1000 0000 0000 1011
103280            BRNB              READ3I      RESET TAPE MARK STATUS IF NOT DC3 00CE  90E8    1001 0000 1110 1000
103290            PAREN  09         EF          SET ECB                           00CF  19EF    0001 1001 1110 1111
103300            EC                                                              00D0  3000    0011 0000 0000 0000
103310            LOOP1             READ3B                                        00D1  C0D2    1100 0000 1101 0010
103320 READ3B     LOOP2             READ3A                                        00D2  D0CD    1101 0000 1100 1101
103340            LDLC2             1                                             00D3  5001    0101 0000 0000 0001
103360 READ3C     TESTB             11                                            00D4  800B    1000 0000 0000 1011
103380            BRB               READ3I                                        00D5  A0E8    1010 0000 1110 1000
103400            EC                                                              00D6  3000    C011 0000 0000 0000
103410            LOOP1             READ3D                                        00D7  C0D8    1100 0000 1101 1000
103420 READ3D     LOCP2             READ3C                                        00D8  D0D4    1101 0000 1101 0100
103440            TESTB             11                                            00D9  800B    1000 0000 0000 1011
103460            BRNB              READ3I                                        00DA  90E8    1001 0000 1110 1000
103480            EC                                                              00DB  3000    0011 0000 0000 0000
```

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PAGE  17                                    TAPEMCON06                                           DATE    27/09/78
SEQ NO  REFERENCE OPCODE MC EA EB EC OPERANDS   COMMENTS                                    ADRS  MEMORY  BINARY REPRESENTATION

103490            LOOP1              READ3E                                                 000C  C0DD    1100 0000 1101 1101

103500 READ3E     LDLC2              3                                                      000D  5003    0101 0000 0000 0011

103520 READ3F     TESTB              11                                                     000E  800B    1000 0000 0000 1011

103540            BRB                READ3I                                                 000F  A0E8    1010 0000 1110 1000

103560            EC                                                                        00E0  3000    0011 0000 0000 0000

103570            LOOP1              READ3G                                                 00E1  C0E2    1100 0000 1110 0010

103580 READ3G     LOOP2              READ3F                                                 00E2  D0DE    1101 0000 1101 1110

103600 READ3H     EC                                                                        00E3  3000    0011 0000 0000 0000

103610            LOOP1              READ3H                                                 00E4  C0E3    1100 0000 1110 0011

103620            LDLC1              16         SHORT RECORD IF LESS THAN 16 BYTES          00E5  4010    0100 0000 0001 0000

103630            PAREN  05          06         SET STATUS BIT 9 (SHORT RECORD)             00E6  1506    0001 0101 0000 0110

103640            BRANCH             READ4                                                  00E7  60EA    0110 0000 1110 1010

103680 READ3I     PAREN  05          08         CLEAR TAPE MARK STATUS                      00E8  1508    0001 0101 0000 1000

103700            BRANCH             READ3H                                                 00E9  60E3    0110 0000 1110 0011

104120 READ4      TESTB              1          SKIP FIRST BYTE?                            00EA  8001    1000 0000 0000 0001

104140            BRB                READ5      YES, GO TO READ5                            00EB  A0F2    1010 0000 1111 0010

104160 READ4A     PAREN  05          07         SET STATUS BIT 8 (HALF WORD ON READ)        00EC  1507    0001 0101 0000 0111
```

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PAGE  18                                        TAPEMCON06                                          DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION
104180            PAREN  08           08        BYTE CONTROL 1                              00ED  1808    0001 1000 0000 1000
104200            JUMP                RDSHIFT   PERFORM READSHIFT                           00EE  7042    0111 0000 0100 0010
104220 READ4B     JUMP                RDSCK     RDS?                                        00EF  7011    0111 0000 0001 0001
104240            BRNB                READ4B    NO, LOOP                                    00F0  90EF    1001 0000 1110 1111
104260            JUMP                READSUB1  PERFORM READSUB1                            00F1  719C    0111 0001 1001 1100
105120 READ5      TESTB               10        DATA REQUEST ACTIVE?                        00F2  800A    1000 0000 0000 1010
105140            BRNB                READ5A    NO, BYPASS SYSTEM OVERLOAD FLOW             00F3  90F7    1001 0000 1111 0111
105160            PAREN  05           03        SET STATUS BIT 12 (SYSTEM OVERLOAD)         00F4  1503    0001 0101 0000 0011
105180            JUMP                RDSHIFT                                               00F5  7042    0111 0000 0100 0010
105200            BRANCH              READTERM                                              00F6  6102    0110 0001 0000 0010
105220 READ5A     PAREN  05           0F        CLEAR STATUS BIT 8                          00F7  150F    0001 0101 0000 1111
105240            PAREN  08           09        BYTE CONTROL 2                              00F8  1809    0001 1000 0000 1001
105260            JUMP                RDSHIFT   PERFORM READSHIFT                           00F9  7042    0111 0000 0100 0010
105280            EA        6         STASH BYTE  1 BUFFER                                  00FA  1F06    0001 1111 0000 0110
105300            TESTB               9         TERMINATE?                                  00FB  8009    1000 0000 0000 1001
105320            BRB                 READTERM  YES, GO TO READTERM                         00FC  A102    1010 0001 0000 0010
105340            EA        9                   REQUEST DATA INTERRUPT                      00FD  1F09    0001 1111 0000 1001
```

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PAGE  19                               TAPEMCON06                                   DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                     ADRS  MEMORY  BINARY REPRESENTATION
105360 READ5B     JUMP                RDSCK      RDS?                         00FE  7011    0111 0000 0001 0001
105370            BRNB                READ5B     NO, LOOP                     00FF  90FE    1001 0000 1111 1110
105380            JUMP                READSUB1   PERFORM READSUB1             0100  719C    0111 0001 1001 1100
105440 READ5D     BRANCH              READ4A     PROCESS NEXT BYTE            0101  60EC    0110 0000 1110 1100
110120 READTERM   JUMP                RDSCK      WAIT FOR RDS                 0102  7011    0111 0000 0001 0001
110140            BRNB                READTERM                                0103  9102    1001 0001 0000 0010
110160            JUMP                RDSHIFT    PERFORM SHIFT                0104  7042    0111 0000 0100 0010
110170            JUMP                READSUB1   PERFORM READSUB1             0105  719C    0111 0001 1001 1100
110180            BRANCH              READTERM                                0106  6102    0110 0001 0000 0010
```

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PAGE  20                                        TAPEMCOND6                                       DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

120020 **          THIS ROUTINE ENTERED WHEN RDS DOES NOT FALL WITHIN 1.5 CLOCK

120030 *                TIMES.

120120 READDROP    PAREN  04          20          LOAD ST. 50USEC. (800 BPI)               0107  1414    0001 0100 0001 0100

120140             TESTB              5           DENSITY 1 ON?                            0108  8005    1000 0000 0000 0101

120160             BRB                READDROP1   YES, CHECK FOR 200 BPI                   0109  A10C    1010 0001 0000 1100

120180             PAREN  04          29          LOAD ST. 72USEC. (556 BPI)               010A  141D    0001 0100 0001 1101

120200             BRANCH             READDROP2                                            010B  610F    0110 0001 0000 1111

120220 READDROP1   TESTB              6           DENSITY 2 ON?                            010C  8006    1000 0000 0000 0110

120240             BRNB               READDROP2   NO, MUST BE 800 BPI.                     010D  910F    1001 0001 0000 1111

120260             PAREN  04          80          LD ST 200 USEC (200 BPI & 25 IPS.)       010E  1450    0001 0100 0101 0000

121120 READDROP2   PAREN  08          09          ENABLE BC2.                              010F  1809    0001 1000 0000 1001

121140             JUMP               READSUB2    PERFORM READSUB2                         0110  71A3    0111 0001 1010 0011

121220             BRNB   F2          READDROP3   IF NOT READ, GO TO READDROP3.            0111  9919    1001 1001 0001 1001

121240             TESTB              9           TERMINATE?                               0112  8009    1000 0000 0000 1001

121260             BRB                READDROP3   YES, GO TO READDROP3.                    0113  A119    1010 0001 0001 1001

121280             TESTB              35          HALF WORD ON READ?                       0114  8023    1000 0000 0010 0011

121300             BRB                READDROP3   NO, GO TO READDROP3                      0115  A119    1010 0001 0001 1001
```

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PAGE  21                                           TAPEMCON0A                               DATE   27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

121320            EA          6      LOAD BYTE  1.                                      0116  1F06    0001 1111 0000 0110

121340            EA          9                 REQUEST DATA INTERRUPT                  0117  1F09    0001 1111 0000 1001

121360            PAREN  08          01         RESET BC2                               0118  1801    0001 1000 0000 0001

122120 READDROP3  PAREN  08          03         PUT READ REQ. IN LOAD MODE.             0119  1803    0001 1000 0000 0011

122140 READDROP3A TESTB              16         RDS?                                    011A  8010    1000 0000 0001 0000

122160            BRB                DROPOUTERR YES, ERROR                              011B  A092    1010 0000 1001 0010

122180            TESTB              14         ST. COMPLETE?                           011C  800E    1000 0000 0000 1110

122200            BRNB               READDROP3A NO, KEEP CHECKING FOR EARLY RDS.        011D  911A    1001 0001 0001 1010

123120 READDROP4  PAREN  04          60         LOAD S.T. 150USEC. (800 382)            011E  143C    0001 0100 0011 1100

123140            TESTB              5          IS DENSITY 1 ON?                        011F  8005    1000 0000 0000 0101

123160            BRB                READDROP4A YES, CHECK FOR 200 BPI                  0120  A123    1010 0001 0010 0011

123180            PAREN  04          115        LOAD S.T. 216USEC. (556 BPI)            0121  1473    0001 0100 0111 0011

123200            BRANCH             READDROP5                                          0122  6126    0110 0001 0010 0110

123220 READDROP4A TESTB              6          DENSITY 2 ON?                           0123  8006    1000 0000 0000 0110

123240            BRNB               READDROP5  NO, MUST BE 800 BPI                     0124  9126    1001 0001 0010 0110

123260            PAREN  04          240        LD S.T. 600 USEC (200 BPI @ 25 IPS.)    0125  14F0    0001 0100 1111 0000

124120 READDROP5  TESTB              8          7 TRACK?                                0126  8008    1000 0000 0000 1000
```

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PAGE  22                                        TAPEMCON06                                          DATE   27/09/78

SEQ NO  REFERENCE  OPCODE MD EA EB EC OPERANDS   COMMENTS                                      ADRS  MEMORY  BINARY REPRESENTATION

124140             BRB                READDROP8  YES, SKIP CRC CHECK                           0127  A17F    1010 0001 0111 1111

125120 READDROP6   TESTB              16         RDS?                                          0128  8010    1000 0000 0001 0000

125140             BRB                READDROP6A YES, GO TO READDROP6A.(CRC FOUND)             0129  A131    1010 0001 0011 0001

125160             TESTB              14         ST. COMPLETE?                                 012A  800E    1000 0000 0000 1110

125180             BRNB               READDROP6  NO, CHECK AGAIN FOR RDS.                      012B  9128    1001 0001 0010 1000

125200             PAREN  04          80         YES, ASSUME ZERO CRC. SET ST. 200 USEC.       012C  1450    0001 0100 0101 0000

125220             PAREN  06          0A         SET F3 TO INDICATE ZERO CRC                   012D  160A    0001 0110 0000 1010

125230             TESTB              12         TAPE MARK?                                    012E  800C    1000 0000 0000 1100

125240             BRNB               READDROPTM YES, GO TO READDROPTM                         012F  9193    1001 0001 1001 0011

125250             BRANCH             READDROP6B                                               0130  6134    0110 0001 0011 0100

125260 READDROP6A  PAREN  04          120        CRC FOUND, LOAD ST. 300 USEC.                 0131  1478    0001 0100 0111 1000

125280             PAREN  06          02         CLEAR F3 TO INDICATE NON-ZERO CRC.            0132  1602    0001 0110 0000 0010

125290             PAREN  05          08         RESET TAPE MARK STATUS IF ANY (BIT 18)        0133  1508    0001 0101 0000 1000

125300 READDROP6B  EA&EB      15  4   SET FF FOR  ODD PARITY CHECK, RESET RDS.                 0134  1F4F    0001 1111 0100 1111

125320             TESTB              36         ODD RECORD LENGTH?                            0135  8024    1000 0000 0010 0100

125340             BRNB               READDROP6C NO, EXPECT ODD PARITY CRC.                    0136  9138    1001 0001 0011 1000

125360             EA         14                 YES, EXPECT EVEN PARITY CRC.                  0137  1F0E    0001 1111 0000 1110
```

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PAGE 22                                    TAPEMC0006                                         DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

125380 READDROP6C BRNB   F2          READDROP6D IF NOT READ BYPASS CRC PARITY CHECK.   0138  993B    1001 1001 0011 1011
125390            PAREN  07          00                                               0139  1700    0001 0111 0000 0000
125400            JUMP               RDSCK4A    CHECK PARITY OF CRC                   013A  702A    0111 0000 0010 1010
126120 READDROP6D PAREN  06          03         CLEAR F4                              013B  1603    0001 0110 0000 0011
126140            PAREN  08          0B         PLACE READ REG. IN SHIFT MODE         013C  180B    0001 1000 0000 1011
126160            JUMP               RDSHIFT                                          013D  7042    0111 0000 0100 0010
126170            PAREN  09          3F         SET EC7, EC8.                         013E  193F    0001 1001 0011 1111
126180            LDLC1              2          SET LC FOR 2 TIMES                    013F  4002    0100 0000 0000 0010
126190 READDROP6E EC                            SHIFT                                 0140  3000    0011 0000 0000 0000
126200            LOOP1              READDROP6E LOOP BACK TO SHIFT AGAIN.             0141  C140    1100 0001 0100 0000
126210            PAREN  09          7F         SET EC8.                              0142  197F    0001 1001 0111 1111
126220            EC                            SHIFT                                 0143  3000    0011 0000 0000 0000
126230            PAREN  09          3F         SET EC7, EC8.                         0144  193F    0001 1001 0011 1111
126240            EC                 SHIFT                                            0145  3000    0011 0000 0000 0000
126250            PAREN  09          7F         SET EC8                               0146  197F    0001 1001 0111 1111
126260            EC                            SHIFT                                 0147  3000    0011 0000 0000 0000
126270            PAREN  09          3F         SET EC7, EC8.                         0148  193F    0001 1001 0011 1111
```

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PAGE  26                                  TAPEMCON06                                      DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION

126280            LDLC1              2          SET LOOP COUNT FOR 3 SHIFTS.               0149  4002    0100 0000 0000 0010

126290 READDROP6F EC                            SHIFT                                      014A  3000    0011 0000 0000 0000

126300            LOOP1              READDROP6F LOOP BACK TO SHIFT AGAIN.                  014B  C14A    1100 0001 0100 1010

126310            PAREN  09          7F         SET EC8.                                   014C  197F    0001 1001 0111 1111

126320            LDLC1              8          SET LOOP COUNT FOR 9 SHIFTS                014D  4008    0100 0000 0000 1000

126330 READDROP6G TESTB              30         CRC = 0 ?                                  014E  801E    1000 0000 0001 1110

126340            BRNB               READDROP6H YES, GO TO READDROP6H                      014F  9151    1001 0001 0101 0001

126350            PAREN  06          0B         NO, SET FLAG4                              0150  160B    0001 0110 0000 1011

126360 READDROP6H EC                            SHIFT                                      0151  3000    0011 0000 0000 0000

126370            LOOP1              READDROP6G LOOP BACK TO CHECK NEXT BIT                0152  C14E    1100 0001 0100 1110

126420            PAREN  08          03         SET READ REG TO LOAD MODE.                 0153  1803    0001 1000 0000 0011

126440            TESTB              36         ERROR FOUND ?                              0154  8024    1000 0000 0010 0100

126460            BRNB               READDROP8  NO, GO TO READDROP8                        0155  917F    1001 0001 0111 1111

126480            PAREN  05          01         SET STATUS BIT 14. (DATA ERROR)            0156  1501    0001 0101 0000 0001

126500            BRNB   F2          READDROP8  IF NOT READ, GO PROCESS LRC.               0157  997F    1001 1001 0111 1111

126520            TESTB              29         WAS ERROR CORRECTION ENABLED?              0158  801D    1000 0000 0001 1101

126540            EB        3                   RESET TIE REG.  (TRACK IN ERROR)           0159  1F30    0001 1111 0011 0000
```

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PAGE  25                                   TAPEMCON06                                            DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

126560            BRB                 READDROPS  YES, PROCESS LRC.                         015A  A17F    1010 0001 0111 1111

126580            BRB      F3         READDROPS  IF ZERO CRC, SKIP TIE LOCATION.           015B  AD7F    1010 1101 0111 1111
```

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PAGE 26                                         TAPEMCON06                                   DATE    27/09/78

SEQ NO REFERENCE OPCODE MO EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

127020 **      DETERMINE TRACK IN ERROR

127120 READDROP7  JUMP                TIESHFTLD1 PUT A 1 IN THE TIE REG.                0015C  7197    0111 0001 1001 0111

127140            LDLC2               8          SET COUNT FOR 9 COMPARES              015D  5008    0101 0000 0000 1000

127160 READDROP7A PAREN  06           02         RESET F3                              015E  1602    0001 0110 0000 0010

127180            LDLC1               8          CHECK 9 BITS                          015F  4008    0100 0000 0000 1000

127190            PAREN  09           77         SET EC4, EC8                          0160  1977    0001 1001 0111 0111

127200 READDROP7B TESTB               26         COMPARE CRC & E REGS.                 0161  801A    1000 0000 0001 1010

127220            BRNB                READDROP7C IF EQUAL, DO NOT SET FLAG             0162  9164    1001 0001 0110 0100

127240            PAREN  06           0A         SET F3                                0163  160A    0001 0110 0000 1010

127260 READDROP7C EC                             SHIFT                                 0164  3000    0011 0000 0000 0000

127270            LOOP1               READDROP7B CHECK NEXT BIT                        0165  C161    1100 0001 0110 0001

127280            BRNB   F3           READDROP7E IF EQUAL, GO TO READDROP7E            0166  9D77    1001 1101 0111 0111

127300            PAREN  09           7D                                               0167  197D    0001 1001 0111 1101

127320            EC            6                SHIFT FIE, CRC, AND SET FF            0168  3F50    0011 1111 0101 0000

127330            PAREN  09           7F         SET EC8.                              0169  197F    0001 1001 0111 1111

127340            EC                             SHIFT                                 016A  3000    0011 0000 0000 0000

127350            EC                             SHIFT                                 016B  3000    0011 0000 0000 0000
```

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PAGE  27                                        TAPEMCONDA                                       DATE    27/09/78
SEQ NO REFERENCE  OPCODE MD EA EB EC OPERANDS   COMMENTS                               ADRS  MEMORY   BINARY REPRESENTATION
127360            LDLC1              3          LOAD COUNT                             016C  4003     0100 0000 0000 0011
127380            PAREN  08          0C         ALLON INV                              016D  180C     0001 1000 0000 1100
127400 READDROP7D EC                            SHIFT                                  016E  3000     0011 0000 0000 0000
127410            LOOP1              READDROP7D     4X                                 016F  C16E     1100 0001 0110 1110
127420            PAREN  08          04         DISABLE INV                            0170  1804     0001 1000 0000 0100
127440            EC                            SHIFT                                  0171  3000     0011 0000 0000 0000
127460            EC                            SHIFT                                  0172  3000     0011 0000 0000 0000
127470            EC                            SHIFT                                  0173  3000     0011 0000 0000 0000
127480            LOOP2              READDROP7A SHIFT                                  0174  D15E     1101 0001 0101 1110
127500            EB           3                RESET TIE REG.                         0175  1F30     0001 1111 0011 0000
127520            BRANCH             READDROP8  PROCESS LRC.                           0176  617F     0110 0001 0111 1111
127540 READDROP7E JUMP               TIESHFTLD1 PUT A 1 IN TIE REG.                    0177  7197     0111 0001 1001 0111
127560            LOOP2              READDROP7F COUNT DOWN                             0178  D17A     1101 0001 0111 1010
127580            BRANCH             READDROP7G EXIT IF ZERO                           0179  617C     0110 0001 0111 1100
127620 READDROP7F EC                            SHIFT O'S INTO TIE REG                 017A  3000     0011 0000 0000 0000
127640            LOOP2              READDROP7F                                        017B  D17A     1101 0001 0111 1010
127660 READDROP7G EC                            SHIFT                                  017C  3000     0011 0000 0000 0000
```

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PAGE  28                                    TAPEMCON06                                                     DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                     ADRS  MEMORY  BINARY REPRESENTATION

127680            EC                            SHIFT                                        017D  3000    0011 0000 0000 0000

127700            BRANCH             READDROPS                                               017E  617F    0110 0001 0111 1111
```

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PAGE  29                                     TAPEMCON06                                   DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                          ADRS  MEMORY  BINARY REPRESENTATION
128020 **         CHECK LRC HERE
128120 READDROPB  TESTB              16         RDS?                              017F  8010    1000 0000 0001 0000
128140            BRB                READDROPBA YES, PROCESS LRC                  0180  A183    1010 0001 1000 0011
128160            TESTB              14         NO,TIMER COMPLETE?                0181  800E    1000 0000 0000 1110
128180            BRNB               READDROPB  NO,CHECK AGAIN                    0182  917F    1001 0001 0111 1111
128200 READDROPBA PAREN  08          0B         READ REG TO SHIFT MODE            0183  180B    0001 1000 0000 1011
128220            TESTB              8                                            0184  8008    1000 0000 0000 1000
128240            BRB                READDROPBB                                   0185  A189    1010 0001 1000 1001
128260            BRNB   F2          READDROPBB                                   0186  9989    1001 1001 1000 1001
128280            EA          15                                                  0187  1F0F    0001 1111 0000 1111
128300            JUMP               RDSCK4A                                      0188  702A    0111 0000 0010 1010
128320 READDROPBB LDLC1              8          CHECK 9 BITS                      0189  4008    0100 0000 0000 1000
128330            PAREN  09          CD         SET EC2, EC5, EC6                 018A  19CD    0001 1001 1100 1101
128340 READDROPBC TESTB              25         BITS EQUAL ?                      018B  8019    1000 0000 0001 1001
128360            BRNB               READDROPBD YES, SKIP ERROR PATH              018C  918E    1001 0001 1000 1110
128380            PAREN  05          01         NO, SET DATA ERROR STATUS (BIT 14)  018D  1501  0001 0101 0000 0001
128400 READDROPBD EC                            SHIFT                             018E  3000    0011 0000 0000 0000
```

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PAGE 33                                    TAPEMCON06                                        DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

128420             LOOP1               READDROPBC CHECK NEXT BIT                       018F  C18B    1100 0001 1000 1011

128440             PAREN  09           FD         SET EC2                              0190  19FD    0001 1001 1111 1101

128460             EC                             SHIFT                                0191  3000    0011 0000 0000 0000

128480             BRANCH              TERMINATE                                       0192  609C    0110 0000 1001 1100

129120 READDROPTM  PAREN  05           0E         RESET SHORT RECORD STATUS (BIT 9)    0193  150E    0001 0101 0000 1110

129140             BRB    F2           READDROPB  IF READ, GO TO READDROPB             0194  A97F    1010 1001 0111 1111

129160             PAREN  05           08         RESET TAPE MARK STATUS (BIT 15)      0195  1508    0001 0101 0000 1000

129180             BRANCH              READDROPB                                       0196  617F    0110 0001 0111 1111

140160 TIESHFTLD1  PAREN  08           0E         SET TIE INPUT TO 1.                  0197  180E    0001 1000 0000 1110

140180             PAREN  09           FD         SET EC2                              0198  19FD    0001 1001 1111 1101

140190             EC                             CLOCK IN A 1.                        0199  3000    0011 0000 0000 0000

140200             PAREN  08           06         SET TIE INPUT TO 0.                  019A  1806    0001 1000 0000 0110

140220             RETURN                         RETURN                               019B  2000    0010 0000 0000 0000

150120 READSUB1    TESTB               8          9 TRACK?                             019C  8008    1000 0000 0000 1000

150140             BRB                 READSUB1A  NO, GO TO READSUB1A                  019D  A19F    1010 0001 1001 1111

150160             PAREN  05           08         RESET TAPEMARK STATUS.               019E  1508    0001 0101 0000 1000

150180 READSUB1A   LOOP1               READSUB1B  IF COUNT NOT DEPLETED= RETURN        019F  C1A2    1100 0001 1010 0010
```

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PAGE  31                                       TAPEMCON04                                        DATE    27/09/78
SEQ NO  REFERENCE  OPCODE MD EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

150200             PAREN  05           08       RESET TAPEMARK STATUS.                     01A0  1508    0001 0101 0000 1000

150220             PAREN  05           0E       RESET SHORT RECORD STATUS                  01A1  150E    0001 0101 0000 1110

150240 READSUB1B   RETURN                       RETURN                                     01A2  2000    0010 0000 0000 0000

160120 READSUB2    PAREN  07           07       SELECT ONES AS INPUT TO WRITE REG.         01A3  1707    0001 0111 0000 0111

160140             PAREN  08           0B       PUT READ REG INTO SHIFT MODE               01A4  180B    0001 1000 0000 1011

160160             PAREN  08           0F       CONNECT READ AND WRITE REGS.               01A5  180F    0001 1000 0000 1111

160180             LDLC1               27       SET LOOP COUNTER FOR 28 SHIFTS             01A6  401B    0100 0000 0001 1011

160200             PAREN  09           EB       SET EC3, EC5                               01A7  19EB    0001 1001 1110 1011

160220 READSUB2A   EC                           CLOCK READ & WRITE REGS.                   01A8  3000    0011 0000 0000 0000

160240             LOOP1               READSUB2A LOOP BACK TO CLOCK AGAIN                  01A9  C1A8    1100 0001 1010 1000

160260             PAREN  08           07       RE-CIRCULATE READ REG.                     01AA  1807    0001 1000 0000 0111

160270             PAREN  07           00       RESET MUX TO LOGIC ZERO                    01AB  1700    0001 0111 0000 0000

160280             RETURN 08           03       RETURN, SET READ REG. TO LOAD MODE         01AC  2803    0010 1000 0000 0011
```

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PAGE  32                                  TAPEMCON06                                     DATE   27/09/78
SEQ NO  REFERENCE OPCODE MO EA EB EC OPERANDS  COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

200020 **         WRITE

200120 WRITE       JUMP                COMSELECT                                        01AD  7061    0111 0000 0110 0001

200140             TESTB               18         WRITE LOCKOUT?                        01AE  8012    1000 0000 0001 0010

200160             BRB                 WRITELOCK  YES, TERMINATE                        01AF  A098    1010 0000 1001 1000

200180             EA        1                    OUTPUT DATA (PROC TO MTU)             01B0  1F01    0001 1111 0000 0001

200200             PAREN  07           00         WRITE REGS TO LOAD MODE               01B1  1700    0001 0111 0000 0000

200220             EA        9                    REQUEST DATA INTERRUPT                01B2  1F09    0001 1111 0000 1001

200240             EA        12                   CLEAR WRITE CRC REG                   01B3  1F0C    0001 1111 0000 1100

200260             PAREN  02           0F         WRITE CURRENT ON                      01B4  120F    0001 0010 0000 1111

200280             PAREN  02           08         FORWARD ON                            01B5  1208    0001 0010 0000 1000

201120 *          START DELAY

201140 WRITE1      TESTB               20         BOT?                                  01B6  8014    1000 0000 0001 0100

201160             BRNB                WRITE1A    NO, GO TO WRITE1A                     01B7  918A    1001 0001 1011 1010

201180             LDLC1               84         YES, SPECIFY 8.5 INCHES               01B8  4054    0100 0000 0101 0100

201200             JUMP                BOTDELAY   PERFORM BOT DELAY                     01B9  708A    0111 0000 1000 1010

201220 WRITE1A     PAREN  03           76         SET LONG TIMER                        01BA  134C    0001 0011 0100 1100

201240 WRITE1B     TESTB               15         L. TIMER COMPLETE?                    01BB  800F    1000 0000 0000 1111
```

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PAGE  33                                          TAPEMCONDA                                  DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                 ADRS  MEMORY  BINARY REPRESENTATION

201260            BRNB                WRITE1B  NO, WAIT                                 01BC  91BB    1001 0001 1011 1011

202120 *         CLOCK START

202140 WRITE2     PAREN  01           32       LOAD CLOCK DIVIDER FOR 50 US. (800 BPI)  01BD  1132    0001 0001 0011 0010

202160            TESTB               5        DENSITY 1 ON?                            01BE  8005    1000 0000 0000 0101

202180            BRB                 WRITE2A  YES, GO TO WRITE2A                       01BF  A1C2    1010 0001 1100 0010

202200            PAREN  01           48       NO, MUST BE 556 BPI- SET CLOCK FOR 72US  01C0  1148    0001 0001 0100 1000

202220            BRANCH              WRITE3                                            01C1  61C5    0110 0001 1100 0101

202240 WRITE2A    TESTB               6        DENSITY 2 ON?                            01C2  8006    1000 0000 0000 0110

202260            BRNB                WRITE3   NO, MUST BE 800 BPI                      01C3  91C5    1001 0001 1100 0101

202280            PAREN  01           C8       YES, SET CLOCK FOR 200 USEC. (200 BPI)   01C4  11C8    0001 0001 1100 1000

203120 *         CLOCK SYNCH

203140 WRITE3     TESTB               13       PHASE2 ON?                               01C5  800D    1000 0000 0000 1101

203160            BRNB                WRITE3   NO, WAIT TILL ON                         01C6  91C5    1001 0001 1100 0101

203180 WRITE3A    TESTB               13       PHSE2 ON?                                01C7  800D    1000 0000 0000 1101

203200            BRB                 WRITE3A  YES, WAIT TILL OFF                       01C8  A1C7    1010 0001 1100 0111

203220            PAREN  02           0E       ENABLE WRITE STROBE                      01C9  120E    0001 0010 0000 1110

203240            EB             7    RESET FB37                                        01CA  1F70    0001 1111 0111 0000
```

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PAGE  3A                                     TAPEMCON06                                    DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                    ADRS  MEMORY  BINARY REPRESENTATION

203860            TESTB              1          SKIP FIRST BYTE?                            01CB  8001    1000 0000 0000 0001

203880            BRNB               WRITE5     NO, GO TO WRITE5                            01CC  91D9    1001 0001 1101 1001

204120 *         SKIP FIRST BYTE

204140 WRITE4     PAREN  07          08         WRITE REGS TO SHIFT MODE.                   01CD  1708    0001 0111 0000 1000

204160            LDLC1              8          SET COUNT FOR 9 SHIFTS                      01CE  4008    0100 0000 0000 1000

204180            PAREN  09          FE         SET EC1                                     01CF  19FE    0001 1001 1111 1110

204200 WRITE4A    EC                            SHIFT                                       01D0  3000    0011 0000 0000 0000

204220            LOOP1              WRITE4A    LOOP BACK TO SHIFT AGAIN.                   01D1  C1D0    1100 0001 1101 0000

204240            TESTB              9          TERMINATE WITH 1ST 605 WORD?                01D2  8009    1000 0000 0000 1001

204260            BRNB               WRITE4B    NO, SKIP ERROR CHECK                        01D3  91D6    1001 0001 1101 0110

204280            TESTB              2          SKIP LAST BYTE?                             01D4  8002    1000 0000 0000 0010

204300            BRB                PROGERROR  YES, PROGRAM ERROR                          01D5  A094    1010 0000 1001 0100

204320 WRITE4B    PAREN  07          05         SETUP FOR RH BYTE                           01D6  1705    0001 0111 0000 0101

204340            EA          9                 REQUEST DATA INTERRUPT                      01D7  1F09    0001 1111 0000 1001

204360            BRANCH             WRITE6     GO TO WRITE6                                01D8  61EC    0110 0001 1110 1100

205120 *         WRITE LH BYTE

205140 WRITE5     PAREN  07          0C         INDICATE LH BYTE.                           01D9  170C    0001 0111 0000 1100
```

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PAGE  35                                          TAPEMCON06                                          DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS    COMMENTS                                    ADDR  MEMORY  BINARY REPRESENTATION

205160            JUMP               WRITESHIFT PERFORM WRITESHIFT                          01DA  722B    0111 0010 0010 1011

205180            TESTB              37         HAS A WRITE STROBE OCCURRED?                 01DB  8025    1000 0000 0010 0101

205200            BRB                SYSTOVERLD YES, SYSTEM OVERLOAD                         01DC  A08F    1010 0000 1000 1111

205220            PAREN  07          05         INTERFACE REGS TO LOAD, MUX TO RH BYTE      01DD  1705    0001 0111 0000 0101

205240 WRITE5A    JUMP               RDSCK      PERFORM RDSCK                                01DE  7011    0111 0000 0001 0001

205260            TESTB              37         HAS WRITE STROBE BEGUN?                      01DF  8025    1000 0000 0010 0101

205280            BRNB               WRITE5A    NO, LOOP UNTILL IT HAS                       01E0  91DE    1001 0001 1101 1110

205300 * WRITE STROBE BEGINS HERE - LH BYTE

205320            EB        7                   RESET FB37                                   01E1  1F70    0001 1111 0111 0000

205340            TESTB              9          TERMINATE?                                   01E2  8009    1000 0000 0000 1001

205360            BRNB               WRITE5B    NO, GO TO WRITE5B                            01E3  91E8    1001 0001 1110 1000

205370            PAREN  06          0A         SET FLAG 3                                   01E4  160A    0001 0110 0000 1010

205380            TESTB              2          SKIP LAST BYTE?                              01E5  8002    1000 0000 0000 0010

205400            BRNB               WRITE5C    NO, GO TO WRITE5C                            01E6  91E9    1001 0001 1110 1001

205420            BRANCH             WRITE7     YES, GO TO WRITE7 (WRITE TERMINATE)          01E7  61FB    0110 0001 1111 1011

205440 WRITE5B    EA        9                   REQUEST DATA INTERRUPT                       01E8  1F09    0001 1111 0000 1001

205460 WRITE5C    JUMP               RDSCK      PERFORM RDSCK                                01E9  7011    0111 0000 0001 0001
```

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PAGE  36                                    TAPEMCONO6                                  DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

206080            TESTB              13         WRITE CLOCK OFF?                        01EA  800D    1000 0000 0000 1101

206100            BRB                WRITESC    NO, LOOP BACK UNTILL IT IS              01EB  A1E9    1010 0001 1110 1001

206120 *         WRITE RM BYTE

206140 WRITE6     JUMP               WRITESHIFT PERFORM WRITESHIFT                      01EC  722B    0111 0010 0010 1011

206160 WRITE6A    JUMP               RDSCK      PERFORM RDSCK                           01ED  7011    0111 0000 0001 0001

206180            TESTB              37         HAS WRITE STROBE BEGUN?                 01EE  8025    1000 0000 0010 0101

206200            BRNB               WRITE6A    NO, LOOP BACK                           01EF  91ED    1001 0001 1110 1101

206220 * WRITE STROBE BEGINS HERE - RM BYTE

206240            EB          7                 RESET FB37                              01F0  1F70    0001 1111 0111 0000

206260            BRB    F3          WRITE7     IF TERMINATE GO TO WRITE7               01F1  ADFB    1010 1101 1111 1011

206280 WRITE6B    JUMP               RDSCK      PERFORM RDSCK                           01F2  7011    0111 0000 0001 0001

206300            TESTB              13         IS WRITE STROBE OFF?                    01F3  800D    1000 0000 0000 1101

206320            BRB                WRITE6B    NO, LOOP BACK                           01F4  A1F2    1010 0001 1111 0010

206340 WRITE6C    JUMP               RDSCK      PERFORM RDSCK                           01F5  7011    0111 0000 0001 0001

206360            TESTB              37         HAS WRITE STROBE BEGUN?                 01F6  8025    1000 0000 0010 0101

206380            BRB                SYSTOVERLD YES, SYSTEM OVERLOAD                    01F7  A08F    1010 0000 1000 1111

206400            TESTB              10         DATA REQUEST STILL ACTIVE               01F8  800A    1000 0000 0000 1010
```

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PAGE  37                                         TAPEMCON06                                       DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                        ADRS  MEMORY  BINARY REPRESENTATION

206920            BRB                WRITE6C    YES, GO BACK TO WRITE6C                         01F9  A1F5    1010 0001 1111 0101
206940            BRANCH             WRITE5     NO, WRITE NEXT BYTE                             01FA  61D9    0110 0001 1101 1001
207120 *         WRITE TERMINATION
207140 WRITE7     JUMP               RDSCK      PERFORM RDSCK                                   01FB  7011    0111 0000 0001 0001
207160            TESTB              13         IS WRITE STROBE OFF                             01FC  800D    1000 0000 0000 1101
207180            BRB                WRITE7     NO, LOOP BACK TO WRITE7                         01FD  A1FB    1010 0001 1111 1011
207200            PAREN  02          06         DISABLE STROBE TO MTU.                          01FE  1206    0001 0010 0000 0110
207220            LDLC1              2          SET COUNT FOR 3 CLOCK TIMES                     01FF  4002    0100 0000 0000 0010
207240 WRITE7A    JUMP               RDSCK      PERFORM RDSCK                                   0200  7011    0111 0000 0001 0001
207260            TESTB              37         HAS WRITE CLOCK BEGUN?                          0201  8025    1000 0000 0010 0101
207280            BRNB               WRITE7A    NO, LOOP BACK UNTILL IT HAS                     0202  9200    1001 0010 0000 0000
207300            FB              7  RESET FB37                                                 0203  1F70    0001 1111 0111 0000
207320 WRITE7B    JUMP               RDSCK      PERFORM RDSCK                                   0204  7011    0111 0000 0001 0001
207340            TESTB              13         IS WRITE CLOCK OFF?                             0205  800D    1000 0000 0000 1101
207360            BRB                WRITE7B    NO, LOOP BACK UNTILL OFF                        0206  A204    1010 0010 0000 0100
207380            PAREN  02          06         DISABLE STROBE TO MTU                           0207  1206    0001 0010 0000 0110
207400            TESTB              9          TERMINATE? (USED AS A FLAG HERE)                0208  8009    1000 0000 0000 1001
```

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PAGE  38                                        TAPEMCON06                                       DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

207420           BRNB                WRITE7C    NO, GO TO WRITE7C                         0209  921B    1001 0010 0001 1011
207440           TESTB               8          7 TRACK?                                  020A  8008    1000 0000 0000 1000
207460           BRB                 WRITE7C    YES, GO TO WRITE7C                        020B  A21B    1010 0010 0001 1011
207480           LOOP1               WRITE7A    LOOP BACK UNTILL CRC TIME                 020C  C200    1100 0010 0000 0000
207500           PAREN  07           03         SET MUX TO CRC/                           020D  1703    0001 0111 0000 0011
207520           PAREN  C9           F3         SET EC3,EC4                               020E  19F3    0001 1001 1111 0011
207540           EC                             SHIFT, INVERT CRC                         020F  3000    0011 0000 0000 0000
207560           EC                             SHIFT, INVERT CRC                         0210  3000    0011 0000 0000 0000
207580           EC     07           C2         SHIFT, INVERT CRC, SET MUX TO CRC         0211  3702    0011 0111 0000 0010
207600           EC     07           03         SHIFT CRC, SET MUX TO CRC/                0212  3703    0011 0111 0000 0011
207620           EC     07           02         SHIFT, INVERT CRC, SET MUX TO CRC         0213  3702    0011 0111 0000 0010
207640           EC     07           03         SHIFT CRC, SET MUX TO CRC/                0214  3703    0011 0111 0000 0011
207660           EC                             SHIFT, INVERT CRC                         0215  3000    0011 0000 0000 0000
207680           EC                             SHIFT, INVERT CRC                         0216  3000    0011 0000 0000 0000
207700           EC                             SHIFT, INVERT CRC                         0217  3000    0011 0000 0000 0000
207720           EC        2                    SHIFT, CLEAR TERMB= USED AS A FLAG HERE   0218  3F02    0011 1111 0000 0010
207740           PAREN  02           CE         ENABLE WRITE STROBE.                      0219  120E    0001 0010 0000 1110
```

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PAGE  39                                      TAPEMCON06                                       DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

207760            LDLC1                 4      SET COUNT FOR LRC                         021A  4004    0100 0000 0000 0100

207780 WRITE7C    LOOP1                 WRITE7A DECREMENT COUNT AND LOOP BACK TILL LRC.  021B  C200    1100 0010 0000 0000

207800 WRITE7D    JUMP                  RDSCK  PERFORM RDSCK                             021C  7011    0111 0000 0001 0001

207820            TESTB                 37     HAS WRITE STROBE OCCURRED?                021D  8025    1000 0000 0010 0101

207840            BRNB                  WRITE7D NO, LOOP BACK                            021E  921C    1001 0010 0001 1100

207860            PAREN  02             0D     WRITE LRC                                 021F  120D    0001 0010 0000 1101

208140 WRITE8     PAREN  03             160    LOAD L.T. FOR TIMEOUT (RUNAWAY)           0220  13A0    0001 0011 1010 0000

208160 WRITE8A    JUMP                  RDSCK  PERFORM RDSCK                             0221  7011    0111 0000 0001 0001

208180            BRB    F1             WRITE8B IF RDS HAS OCCURRED, GO TO WRITE8B       0222  A626    1010 0110 0010 0110

208200            TESTB                 15     L.T. COMPLETE?                            0223  800F    1000 0000 0000 1111

208220            BRB                   TIMOUTERR YES, TIMOUTERR                         0224  A096    1010 0000 1001 0110

208240            BRANCH                WRITE8A CONTINUE CHECKING                        0225  6221    0110 0010 0010 0001

208260 WRITE8B    JUMP                  RDSCK  PERFORM RDSCK                             0226  7011    0111 0000 0001 0001

208280            BRANCH                WRITE8B WAIT FOR CRC OR LRC                      0227  6226    0110 0010 0010 0110

209140 WRITEDROP  BRB    F3             READDROP IF TERMINATE, GO TO READDROP            0228  AD07    1010 1101 0000 0111

209160            PAREN  05             01     SET DATA ERROR STATUS                     0229  1501    0001 0101 0000 0001

209180            RETURN                       RETURN                                    022A  2000    0010 0000 0000 0000
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PAGE  40                                   TAPEMCOND6                                              DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION
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PAGE 41                                       TAPEMCON06                                   DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA SB EC OPERANDS  COMMENTS                               ADRS  MEMORY  BINARY REPRESENTATION

220020 **         WRITE SHIFT

220120 WRITESHIFT EA          10               SET PARITY GEN FOR ODD                 022B  1F0A    0001 1111 0000 1010

220140            TESTB               7        ODD SPECIFIED?                         022C  8007    1000 0000 0000 0111

220160            BRNB                WRSHIFT1 YES, GO TO WRSHIFT1.                   022D  922F    1001 0010 0010 1111

220180            EA          11               NO, SET PARITY GEN FOR EVEN            022E  1F0B    0001 1111 0000 1011

220200 WRSHIFT1   PAREN 09            F2       SET EC1, EC3, EC4.                     022F  19F2    0001 1001 1111 0010

220220            EC             6             SHIFT 1 AND STORE CARRY                0230  3F60    0011 1111 0110 0000

220240            EC                           SHIFT 2                                0231  3000    0011 0000 0000 0000

220260            EC                           SHIFT 3                                0232  3000    0011 0000 0000 0000

220280            EC          5                SHIFT 4  (ENABLE INVERSION OF CRC BITS) 0233  3F05   0011 1111 0000 0101

220300            EC          5                SHIFT 5  (ENABLE INVERSION OF CRC BITS) 0234  3F05   0011 1111 0000 0101

220320            EC          5                SHIFT 6  (ENABLE INVERSION OF CRC BITS) 0235  3F05   0011 1111 0000 0101

220360            TESTB               8        7 TRACK?                               0236  8008    1000 0000 0000 1000

220380            BRNB                WRSHIFT1A NO, GO TO WRSHIFT1A                   0237  923A    1001 0010 0011 1010

220400            TESTB               31       YES, IS BIT 7 A ONE?                   0238  801F    1000 0000 0001 1111

220420            BRB                 PROGERROR YES, PROGERROR                        0239  A094    1010 0000 1001 0100

220440 WRSHIFT1A  EC          5                SHIFT 7 (ENABLE INVERSION OF CRC BITS) 023A  3F05    0011 1111 0000 0101
```

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PAGE  42                                       TAPEMCON06                                     DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

220460            TESTB             8          7 TRACK?                                  023B  8008    1000 0000 0000 1000
220480            BRNB              WRSHIFT1B  NO, GO TO WRSHIFT1B                       023C  923F    1001 0010 0011 1111
220500            TESTB             31         YES, IS BIT 8 A ONE?                      023D  801F    1000 0000 0001 1111
220520            BRB               PROGERROR  YES, PROGERROR                            023E  A094    1010 0000 1001 0100
220540 WRSHIFT1B  EC                            SHIFT 8                                  023F  3000    0011 0000 0000 0000
220545            PAREN  07         01         SET MUX TO PARITY BIT                     0240  1701    0001 0111 0000 0001
220560            EC     07         00         SHIFT 9  (SET MUX TO LOGIC ZERO)          0241  3700    0011 0111 0000 0000
220580            PAREN  09         F3         SET EC3, EC4.                             0242  19F3    0001 1001 1111 0011
220600            EC                           FINAL CRC SHIFT                           0243  3000    0011 0000 0080 0000
220620            RETURN                                                                 0244  2000    0010 0000 0000 0000
```

```
PAGE 43                                    TAPEMCON06                                   DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                             ADRS  MEMORY  BINARY REPRESENTATION

300020 **         ERASE

300120 ERASE      JUMP              COMSELECT                                        0245  7061    0111 0000 0110 0001

300140            TESTB             18          LOCKOUT?                             0246  8012    1000 0000 0001 0010

300160            BRB               WRITELOCK   YES, GO TO WRITELOCK                 0247  A098    1010 0000 1001 1000

300180            PAREN  02         CF          NO, SET WRITE CURRENT ON.            0248  120F    0001 0010 0000 1111

300200            PAREN  02         08          SET FORWARD ON.                      0249  1208    0001 0010 0000 1000

300220            TESTB             20          BOT?                                 024A  8014    1000 0000 0001 0100

300240            BRNB              ERASE1      NO, GO TO ERASE1.                    024B  924E    1001 0010 0100 1110

300260            LDLC1             84          8.5 INCHES.                          024C  4054    0100 0000 0101 0100

300280            JUMP              BOTDELAY    PERFORM DELAY.                       024D  708A    0111 0000 1000 1010

300300 ERASE1     LDLC1             63          6 INCHES + START DELAY               024E  403F    0100 0000 0011 1111

300320 ERASE1A    PAREN  03         16          LOAD L.T. 4 MS. (.1 INCH).           024F  1310    0001 0011 0001 0000

300340 ERASE1B    TESTB             16          RDS ?                                0250  8010    1000 0000 0001 0000

300360            BRNB              ERASE1C     NO, GO TO ERASE1C                    0251  9254    1001 0010 0101 0100

300380            PAREN  05         04          SET STATUS BIT 11 (DROPOUT/PICKUP).  0252  1504    0001 0101 0000 0100

300400            EB          4                 RESET RDS.                           0253  1F40    0001 1111 0100 0000

300420 ERASE1C    TESTB             15          LT. COMPLETE?                        0254  800F    1000 0000 0000 1111
```

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PAGE 44                                        TAPEMCONO6                                    DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                      ADRS  MEMORY  BINARY REPRESENTATION
300440            BRNB                ERASE1B   NO, GO BACK TO ERASE1B.                       0255  9250    1001 0010 0101 0000
300450            LOOP1               ERASE1A   LOOP BACK UNTIL COUNT DEPLETED.               0256  C24F    1100 0010 0100 1111
300460            BRANCH              TERMINATE                                               0257  609C    0110 0000 1001 1100
```

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PAGE  45                                     TAPEMCON06                                DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                               ADRS  MEMORY  BINARY REPRESENTATION

400020 **         BACKSPACE

400120 BACKSPACE  JUMP                COMSELECT                                        0258  7061    0111 0000 0110 0001

400200 BACKSPACE1 PAREN  02           09         SET REVERSE ON.                       0259  1209    0001 0010 0000 1001

400240            TESTB               20         BOT?                                  025A  8014    1000 0000 0001 0100

400260            BRB                 TERM2      YES, TERMINATE                        025B  A0A4    1010 0000 1010 0100

400280            LDLC1               29         TIMEOUT COUNT (30 FEET)               025C  401D    0100 0000 0001 1101

400290 BACKSP2    LDLC2               11         TIMEOUT COUNT (12 INCHES)             025D  500B    0101 0000 0000 1011

400300 BACKSPACE2 PAREN  03           160        LOAD L.T. 40 MS. (1 INCH)             025E  13A0    0001 0011 1010 0000

400320 BACKSPACE3 TESTB               16         RDS ?                                 025F  8010    1000 0000 0001 0000

400340            BRB                 BACKSPACE4 YES, GO TO BACKSPACE4                 0260  A267    1010 0010 0110 0111

400360            TESTB               15         LT. COMPLETE?                         0261  800F    1000 0000 0000 1111

400380            BRNB                BACKSPACE3 NO, CONTINUE SEARCH FOR RDS.          0262  925F    1001 0010 0101 1111

400400            LOOP2               BACKSPACE2 YES, NEXT INCH                        0263  D25E    1101 0010 0101 1110

400410            LOOP1               BACKSP2    NEXT FOOT                             0264  C25D    1100 0010 0101 1101

400420            PAREN  05           05         SET TIMEOUT STATUS (BIT 10)           0265  1505    0001 0101 0000 0101

400440            BRANCH              TERM2                                            0266  60A4    0110 0000 1010 0100

400460 BACKSPACE4 PAREN  03           4          LOAD L.T.  1 MS.                      0267  1304    0001 0011 0000 0100
```

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PAGE 46                                          TAPEMCOND6                                              DATE    27/09/78
SEQ NO. REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                         ADRS  MEMORY  BINARY REPRESENTATION
400480 BACKSPACE5 TESTB                16        RDS?                                             0268  8010    1000 0000 0001 0000
400500            BRNB                 BACKSPACE6 NO, CHECK TIMER                                 0269  926C    1001 0010 0110 1100
400520            EB           4                 YES, RESET RDS.                                  026A  1F40    0001 1111 0100 0000
400540            BRANCH               BACKSPACE4 RESET TIMER.                                    026B  6267    0110 0010 0110 0111
400560 BACKSPACE6 TESTB                15        L.T. COMPLETE?                                   026C  800F    1000 0000 0000 1111
400580            BRNA                 BACKSPACE5 NO, CHECK AGAIN                                 026D  9268    1001 0010 0110 1000
400600            BRANCH               TERMINATE  YES, TERMINATE                                  026E  609C    0110 0000 1001 1100
```

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PAGE 47                                     TAPEMCON06                                        DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                     ADRS  MEMORY  BINARY REPRESENTATION

800020 **        REWIND
800120 REWIND     JUMP              COMSELECT                               026F  7061    0111 0000 0110 0001
800200 REWIND1    PAREN  02         DA         SET REWIND                   0270  120A    0001 0010 0000 1010
800220            BRANCH            TERM2                                   0271  60A4    0110 0000 1010 0100
```

```
PAGE  48                                      TAPEMCON06                                  DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                    ADRS  MEMORY  BINARY REPRESENTATION

600020 **        REWIND AND UNLOAD

600120 REWINDUNLD JUMP            COMSELECT                                 0272  7061    0111 0000 0110 0001

600200 REWINDULD1 PAREN  02       0A          SET REWIND                    0273  120A    0001 0010 0000 1010

600220            PAREN  02       0B          SET OFF-LINE                  0274  120B    0001 0010 0000 1011

600240            BRANCH          TERM2                                     0275  60A4    0110 0000 1010 0100
```

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PAGE  49                                           TAPEMCOND6                                     DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                               ADRS  MEMORY  BINARY REPRESENTATION

700020 **          WRITE TAPE MARK

700120 WRITETMARK JUMP            COMSELECT                                            0276  7061    0111 0000 0110 0001

700140             TESTB           18        WRITE LOCKOUT ?                            0277  8012    1000 0000 0001 0010

700160             BRB             WRITELOCK YES, TERMINATE                             0278  A098    1010 0000 1001 1000

700180             TESTB           8         9 TRACK ?                                  0279  8008    1000 0000 0000 1000

700200             BRB             PROGERROR NO, PROGRAM ERROR                          027A  A094    1010 0000 1001 0100

700220             PAREN  08       00        SET TAPE MARK STATUS (USED AS FLAG)        027B  1800    0001 1000 0000 0000

700240             PAREN  02       0F        SET WRITE CURRENT ON                       027C  120F    0001 0010 0000 1111

700260             PAREN  02       08        SET FORWARD ON                             027D  1208    0001 0010 0000 1000

700280             TESTB           20        BOT?                                       027E  8014    1000 0000 0001 0100

700300             BRNB            WTMARK1   NO, GO TO WTMARK1                          027F  9282    1001 0010 1000 0010

700310             LDLC1           84        SPECIFY  8.5 INCHES                        0280  4054    0100 0000 0101 0100

700320             JUMP            BOTDELAY  PERFORM BCT DELAY                          0281  708A    0111 0000 1000 1010

700340 WTMARK1     PAREN  03       76        SET LONG TIMER FOR 12 MS.                  0282  134C    0001 0011 0100 1100

700360 WTMARK1A    TESTB           15        L. TIMER COMPLETE?                         0283  800F    1000 0000 0000 1111

700380             BRNB            WTMARK1A  NO, LOOP HERE UNTIL COMPLETE               0284  9283    1001 0010 1000 0011

700400             PAREN  01       32        LOAD WRITE CLOCK DIVIDER.                  0285  1132    0001 0001 0011 0010
```

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PAGE  90                                      TAPEMCOND6                                              DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

700420          PAREN  07          07          SET MUX TO 1                              0286  1707    0001 0111 0000 0111

700440          PAREN  09          FB          SET EC3                                   0287  19FB    0001 1001 1111 1011

700460          EC                             SHIFT IN A 1                              0288  3000    0011 0000 0000 0000

700480          EC     07          00          SHIFT IN A 1, SET MUX TO 0.               0289  3700    0011 0111 0000 0000

700500          EC                             SHIFT IN A 0                              028A  3000    0011 0000 0000 0000

700520          EC     07          07          SHIFT IN A 0, SET MUX TO 1.               028B  3707    0011 0111 0000 0111

700540          EC     07          00          SHIFT IN A 1, SET MUX TO 0.               028C  3700    0011 0111 0000 0000

700560          LDLC1              4           SET COUNT TO INDICATE 5 0'S.              028D  4004    0100 0000 0000 0100

700580 WTMARK2  EC                             SHIFT IN A ZERO                           028E  3000    0011 0000 0000 0000

700600          LOOP1              WTMARK2     LOOP BACK AND SHIFT AGAIN.                028F  C28E    1100 0010 1000 1110

700620 WTMARK3  TESTS              13          PHASE 2 CLOCK HIGH?                       0290  800D    1000 0000 0000 1101

700640          BRNS               WTMARK3     NO, WAIT UNTIL IT IS.                     0291  9290    1001 0010 1001 0000

700660 WTMARK3A TESTS              13          CLOCK HIGH?                               0292  800D    1000 0000 0000 1101

700680          BRS                WTMARK3A    YES, WAIT UNTIL IT IS LOW.                0293  A292    1010 0010 1001 0010

700700          PAREN  02          0E          ENABLE WRITE STROBE.                      0294  120E    0001 0010 0000 1110

700720 WTMARK3B TESTS              13          CLOCK HIGH?                               0295  800D    1000 0000 0000 1101

700740          BRNS               WTMARK3B    NO, WAIT UNTIL IT IS.                     0296  9295    1001 0010 1001 0101
```

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PAGE 51                                      TAPEMCON06                                                    DATE    27/09/78
SEQ NO  REFERENCE OPCODE MO EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION
700760            EASEB      2  7              RESET TERMINATE & FB37.                   0297  1F72    0001 1111 0111 0010
700780            PAREN  06           0A       SET F3                                    0298  160A    0001 0110 0000 1010
700800            PAREN  05           00       SET TAPEMARK STATUS                       0299  1500    0001 0101 0000 0000
700820  WTMARK3C  TESTB               13       IS WRITE STROBE OFF?                      029A  800D    1000 0000 0000 1101
700840            BRB                 WTMARK3C NO, LOOP BACK TO WTMARK3C                 029B  A29A    1010 0010 1001 1010
700860            PAREN  02           06       DISABLE STROBE TO MTU                     029C  1206    0001 0010 0000 0110
700880            LDLC1               6        SET COUNT FOR 7 CLOCK TIMES               029D  4006    0100 0000 0000 0110
700900            BRANCH              WRITE7A  WRITE LRC                                 029E  6200    0110 0010 0000 0000
```

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PAGE  52                                   TAPEMCON06                                       DATE    27/09/78
SEQ NO  REFERENCE OPCODE MO EA EB EC OPERANDS   COMMENTS                                ADRS  MEMORY  BINARY REPRESENTATION

800020 **        SELECT

800120 SELECT     JUMP              COMSELECT                                           029F  7061    0111 0000 0110 0001

800140            TESTB             18        WRITE LOCKOUT?                            02A0  8012    1000 0000 0001 0010

800160            BRNB              SELECT1   NO, GO TO SELECT1                         02A1  92A3    1001 0010 1010 0011

800180            PAREN  06         05        YES, SET STATUS BIT 5.                    02A2  1605    0001 0110 0000 0101

800200 SELECT1    BRANCH            TERM2                                               02A3  60A4    0110 0000 1010 0100
```

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PAGE  53                                            TAPEMCON06                                     DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA SB EC OPERANDS   COMMENTS                                    ADRS  MEMORY  BINARY REPRESENTATION

900020 **          RECOVERY READ

900120 RECOVREAD   JUMP                COMSELECT                                            02A4  7061    0111 0000 0110 0001

900140             TESTS               17          READ AFTER WRITE?                        02A5  8011    1000 0000 0001 0001

900160             BRB                 RECOVREAD1  YES, GO TO RECOVREAD1                    02A6  A2A9    1010 0010 1010 1001

900180             PAREN  02           0C          NO, SET RECOVERY LINE TO MTU.            02A7  120C    0001 0010 0000 1100

900200             BRANCH              READ1       GO TO READ1                              02A8  60AF    0110 0000 1010 1111

900220 RECOVREAD1  PAREN  11           00          SET READ-AFTER-WRITE STATUS (BIT 4)      02A9  1B00    0001 1011 0000 0000

900240             BRANCH              TERM2                                                02AA  60A4    0110 0000 1010 0100
```

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PAGE 54                                    TAPEMCON06                                   DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                               ADRS  MEMORY  BINARY REPRESENTATION

A00020 **        CONTROLED BACKSPACE

A00120 CONTBACKSP JUMP                 COMSELECT                                          02AB  7061    0111 0000 0110 0001

A00140            PAREN  03            84         LOAD LONG TIMER (21 MS.)                02AC  1354    0001 0011 0101 0100

A00240 CONTBACK1  PAREN  02            09         SET REVERSE ON                          02AD  1209    0001 0010 0000 1001

A00250 CONTBACK1A TESTB                15         L. TIMER COMPLETE?                      02AE  800F    1000 0000 0000 1111

A00260            BRNB                 CONTBACK1A NO, WAIT                                02AF  92AE    1001 0010 1010 1110

A00270            EA          1                   OUTPUT DATA (PROC TO MTU)               02B0  1F01    0001 1111 0000 0001

A00280 CONTBACK2  PAREN  04            40         LOAD SHORT TIMER (100 US. = 800 BPI)    02B1  1428    0001 0100 0010 1000

A00300            TESTB                5          DENSITY 1 ON?                           02B2  8005    1000 0000 0000 0101

A00320            BRB                  CONTBACK2A YES, GO TO CONTBACK2A (CHECK FOR 200)   02B3  A2B6    1010 0010 1011 0110

A00340            PAREN  04            58         NO, MUST BE 556 BPI= SET S.T. FOR 144US 02B4  143A    0001 0100 0011 1010

A00360            BRANCH               CONTBACK2B                                         02B5  62B9    0110 0010 1011 1001

A00380 CONTBACK2A TESTB                6          DENSITY 2 ON  ?                         02B6  8006    1000 0000 0000 0110

A00400            BRNB                 CONTBACK2B NO, MUST BE 800 BPI                     02B7  92B9    1001 0010 1011 1001

A00420            PAREN  04            160        LOAD SHORT TIMER (400 US. = 200 BPI)    02B8  14A0    0001 0100 1010 0000

A00440 CONTBACK2B TESTB                9          DATA TERMINATE?                         02B9  8009    1000 0000 0000 1001

A00460            BRB                  TERMINATE  YES, GO TO TERMINATE.                   02BA  A09C    1010 0000 1001 1100
```

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PAGE  55                                     TAPEMCON04                                        DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                           ADRS  MEMORY  BINARY REPRESENTATION

A00780            EA           9               REQUEST DATA WORD.                 028B  1F09    0001 1111 0000 1001

A00800 CONTBACK2C TESTB              14         B.T. COMPLETE?                     028C  800E    1000 0000 0000 1110

A00820            BRNB               CONTBACK2C NO, WAIT                           028D  92BC    1001 0010 1011 1100

A00840            BRANCH             CONTBACK2  YES, GO TO CONTBACK2.              028E  62B1    0110 0010 1011 0001
```

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PAGE 56                                           TAPEMCON06                                        DATE    27/09/78
SEQ NO REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION
A99995 **********************************************************************
A99996 *
A99997 *     DIAGNOSTIC  MICROPROGRAM ROUTINES
A99998 *
A99999 * ********************************************************************
B00000            ORIGIN             736
B01000 DTESTS     PAREN  05          00         CLEAR STATUS REGISTERS                  02E0  1500    0001 0101 0000 0000
B01200            PAREN  05          01         (ALL 1'S TO 605)                        02E1  1501    0001 0101 0000 0001
B01300            PAREN  05          02                                                 02E2  1502    0001 0101 0000 0010
B01400            PAREN  05          03                                                 02E3  1503    0001 0101 0000 0011
B01500            PAREN  05          04                                                 02E4  1504    0001 0101 0000 0100
B01600            PAREN  05          05                                                 02E5  1505    0001 0101 0000 0101
B01700            PAREN  05          06                                                 02E6  1506    0001 0101 0000 0110
B01800            PAREN  05          07                                                 02E7  1507    0001 0101 0000 0111
B01900            PAREN  06          04                                                 02E8  1604    0001 0110 0000 0100
B02000            PAREN  06          05                                                 02E9  1605    0001 0110 0000 0101
B02100            PAREN  06          06                                                 02EA  1606    0001 0110 0000 0110
```

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PAGE 67                                 TAPEMCONOA                                      DATE   27/09/78
SEQ NO REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                       ADRS MEMORY BINARY REPRESENTATION

B02800           PAREN  06          07                                       02EB 1607   0001 0110 0000 0111

B02900           BRANCH             REST                                     02EC 600F   0110 0000 0000 1111

C11100 DTEST2    TESTB              10        PODINT IS OFF                  02ED 800A   1000 0000 0000 1010

C11200           BRNB               B                                        02EE 92F0   1001 0010 1111 0000

C11300           PAREN  05          00        BIT 15  on , STATUS            02EF 1500   0001 0101 0000 0000

C11400 B         EA         0B                PROGRAM INT REQUEST            02F0 1F0B   0001 1111 0080 1000

C11500           TESTB              10                                       02F1 800A   1000 0000 0000 1010

C11600           BRB                C                                        02F2 A2F4   1010 0010 1111 0100

C11700           PAREN  05          01        BIT 14 on , STATUS             02F3 1501   0001 0101 0000 0001

C11800 C         BRANCH             A         REST                           02F4 6010   0110 0000 0001 0000

D01000 DTEST2    JUMP               D                                        02F5 72F7   0111 0010 1111 0111

D02000           BRANCH             REST                                     02F6 600F   0110 0000 0000 1111

D03000 D         PAREN  05          0B        BIT 12 STATUS OFF              02F7 150B   0001 0101 0000 1011

D04000           RETURN                                                      02F8 2000   0010 0000 0000 0000

E00000           ORIGIN             768

E01000 DTEST6    TESTB              01        TEST CONTROL WORD              0300 8001   1000 0000 0000 0001

E01100           BRB                DTEST3    JUMP/RETURN                    0301 A2F5   1010 0010 1111 0101
```

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PAGE  58                                        TAPEMCON06                                  DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                    ADRS  MEMORY  BINARY REPRESENTATION

E01200            JUMP            DCLRSTATUS                                                0302  731B    0111 0011 0001 1011

E01205            EB         01                                                             0303  1F10    0001 1111 0001 0000

E01210            TESTB           07                                                        0304  8007    1000 0000 0000 0111

E01220            BRB             A2                                                        0305  A311    1010 0011 0001 0001

E01300            TESTB           02                                                        0306  8002    1000 0000 0000 0010

E01400            BRB             DTEST8                                                    0307  A328    1010 0011 0010 1000

E01500            TESTB           03                                                        0308  8003    1000 0000 0000 0011

E01600            BRB             DTEST9                                                    0309  A32E    1010 0011 0010 1110

E01700            TESTB           04                                                        030A  8004    1000 0000 0000 0100

E01800            BRB             DTEST10                                                   030B  A334    1010 0011 0011 0100

E01900            TESTB           05                                                        030C  8005    1000 0000 0000 0101

E02000            BRB             DTEST11                                                   030D  A33F    1010 0011 0011 1111

E02100            TESTB           06                                                        030E  8006    1000 0000 0000 0110

E02200            BRB             DTEST12                                                   030F  A36A    1010 0011 0110 1010

E02210            BRANCH          A1                                                        0310  6319    0110 0011 0001 1001

E02610 A2         TESTB           02                                                        0311  8002    1000 0000 0000 0010

E02620            BRB             DTEST14                                                   0312  A3A6    1010 0011 1010 0110
```

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PAGE 58                               TAPEMCONDA                                         DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA SB EC OPERANDS   COMMENTS                             ADRS  MEMORY  BINARY REPRESENTATION

E02630            TESTS            04                                                0313  8004    1000 0000 0000 0100
E02640            BRB              REST                                              0314  A00F    1010 0000 0000 1111
E02650            TESTS            03                                                0315  8003    1000 0000 0000 0011
E02660            BRB              DTEST15                                           0316  A3E3    1010 0011 1110 0011
E02670            TESTS            05                                                0317  8005    1000 0000 0000 0101
E02680            BRB              DTEST13                                           0318  A3B8    1010 0011 1000 1011
E02700 A1         PAREN  06        04         BIT 1 STATUS                           0319  1604    0001 0110 0000 0100
E02800            BRANCH           REST                                              031A  600F    0110 0000 0000 1111
E12000 DCLRSTATUS PAREN  05        08         STATUS REGS TO ALL (LOGIC) ONES        031B  1508    0001 0101 0000 1000
E12100            PAREN  05        09            (ALL 0'S TO 605)                    031C  1509    0001 0101 0000 1001
E12200            PAREN  05        0A         BITS 8-15                              031D  150A    0001 0101 0000 1010
E12300            PAREN  05        0B                                                031E  150B    0001 0101 0000 1011
E12400            PAREN  05        0C                                                031F  150C    0001 0101 0000 1100
E12500            PAREN  05        0D                                                0320  150D    0001 0101 0000 1101
E12600            PAREN  05        0E                                                0321  150E    0001 0101 0000 1110
E12700            PAREN  05        0F                                                0322  150F    0001 0101 0000 1111
E12800            PAREN  06        0C         BIT 1                                  0323  160C    0001 0110 0000 1100
```

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PAGE 40                                      TAPEMCOM06                                          DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

E12900            PAREN  06           0D        BIT 5                                     0324  160D    0001 0110 0000 1101

E13000            PAREN  06           0E        BIT 3                                     0325  160E    0001 0110 0000 1110

E13100            PAREN  06           0F                                                  0326  160F    0001 0110 0000 1111

E13200            RETURN                                                                  0327  2000    0010 0000 0000 0000

E20100 DTEST8     LDLC1               255       LOAD LOOP COUNTER 1                       0328  40FF    0100 0000 1111 1111

E20200 F          EA         09                 DATA INT REQUEST                          0329  1F09    0001 1111 0000 1001

E20300 E          TESTB               10                                                  032A  800A    1000 0000 0000 1010

E20400            BRB                 E                                                   032B  A32A    1010 0011 0010 1010

E20500            LOOP1               F                                                   032C  C329    1100 0011 0010 1001

E20600            BRANCH              REST                                                032D  600F    0110 0000 0000 1111

E20700 DTEST9     LDLC2               15        LOAD LOOP COUNTER 2                       032E  500F    0101 0000 0000 1111

E20800 G          EA         09                 DATA INT REQUEST                          032F  1F09    0001 1111 0000 1001

E20900 H          TESTB               10                                                  0330  800A    1000 0000 0000 1010

E21000            BRB                 H                                                   0331  A330    1010 0011 0011 0000

E21100            LOOP2               G                                                   0332  D32F    1101 0011 0010 1111

E21200            BRANCH              REST                                                0333  600F    0110 0000 0000 1111

E22000 DTEST10    PAREN  06           08        SET FLAGS ON                              0334  1608    0001 0110 0000 1000
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```
PAGE 61                                            TAPEMCONDA                                                   DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION

E22100            PAREN  06          09                                                    0335  1609    0001 0110 0000 1001
E22200            PAREN  06          0A                                                    0336  160A    0001 0110 0000 1010
E22300            PAREN  06          0B                                                    0337  160B    0001 0110 0000 1011
E22500            BRNB   F1          I                                                     0338  973D    1001 0111 0011 1101
E22700            BRNB   F2          I                                                     0339  9B3D    1001 1011 0011 1101
E22900            BRNB   F3          I                                                     033A  9F3D    1001 1111 0011 1101
E23000            TESTB              36                                                    033B  8024    1000 0000 0010 0100
E23100            BRB                I1                                                    033C  A33E    1010 0011 0011 1110
E23200 I          PAREN  05          0B         RESET STATUS BIT 12                        033D  150B    0001 0101 0000 1011
```

NOTE: THIS INSTRUCTION TURNS STATUS BIT 12 OFF INSTEAD OF ON. WITH STATUS BIT 12 OFF, THE DIAGNOSTIC PROGRAM IS UNABLE TO DETECT ANY ERRORS THAT MAY POSSIBLY OCCUR. THE REASON THE INSTRUCTION CANNOT BE CHANGED TO TURN BIT 12 ON IS BECAUSE THE COST INVOLVED DOES NOT WARRANT CHANGING A ROM WORD IN ORDER TO LOCATE THE FAILURE OF AN EIGHT BIT ADDRESSABLE LATCH AND ASSOCIATED SIGNAL PATHS WHICH WILL NOT AFFECT THE NORMAL OPERATION OF THE CONTROLLER BOARD IN THE 725 and 734 SYSTEM.

```
E23300 I1         BRANCH             REST                                                  033E  600F    0110 0000 0000 1111
E24100 DTESTI1.   PAREN  04          200        2.5 MICROSX200X= 500 MICROSEC              033F  14C8    0001 0100 1100 1000
E24110            LDLC2              09                                                    0340  5009    0101 0000 0000 1001
E24200 J          LDLC1              179                                                   0341  40B3    0100 0000 1011 0011
E24300 K          LOOP1              K          DELAY  450 MICROSEC (10X180X2.5)           0342  C342    1100 0011 0100 0010
E24310            LOOP2              J                                                     0343  D341    1101 0011 0100 0001
E24500            TESTA              14         SHOULD NOT BE TIMED OUT                    0344  800E    1000 0000 0000 1110
E24600            BRNB               K1                                                    0345  9347    1001 0011 0100 0111
```

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PAGE  62                                      TAPEMCONO6                                    DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                 ADRS  MEMORY  BINARY REPRESENTATION

E24700            PAREN  05          04        BIT 11 STATUS                            0346  1504    0001 0101 0000 0100
E24800 K1         LDLC1              200                                                0347  40C8    0100 0000 1100 1000
E24810 K2         LOOP1              K2                                                 0348  C348    1100 0011 0100 1000
E24812            LDLC1              200                                                0349  40C8    0100 0000 1100 1000
E24814 K3         LOOP1              K3                                                 034A  C34A    1100 0011 0100 1010
E24820            TESTB              14        SHOULD HAVE TIMED OUT                    034B  800E    1000 0000 0000 1110
E24830            BRB                K4                                                 034C  A34E    1010 0011 0100 1110
E24850            PAREN  05          05        BIT 10 STATUS                            034D  1505    0001 0101 0000 0101
E24860 K4         PAREN  03          100       TEST LONG TIMER (250 MICROS/1)           034E  1364    0001 0011 0110 0100
E24870            LDLC1              100       DELAY                                    034F  4064    0100 0000 0110 0100
E24900 L          PAREN  04          90        (90X2.5X100 = 22500 MICROSEC             0350  145A    0001 0100 0101 1010
E25000 L1         TESTB              14                                                 0351  800E    1000 0000 0000 1110
E25100            BRNB               L1                                                 0352  9351    1001 0011 0101 0001
E25200            LOOP1              L                                                  0353  C350    1100 0011 0101 0000
E25300            TESTB              15        TEST LONG TIMER                          0354  800F    1000 0000 0000 1111
E25400            BRNB               L2          SHOULD NOT BE TIMED OUT                0355  9357    1001 0011 0101 0111
E25500            PAREN  05          06        BIT 9 STATUS                             0356  1506    0001 0101 0000 0110
```

```
PAGE  63                                        TAPEMCONDS                                                   DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION

E25600 L2         LDLC1               200      DELAY                                      0357  40C8    0100 0000 1100 1000
E25610 L4         PAREN  04           10       (200X10X2.5 = 5000 MICROSEC.               0358  140A    0001 0100 0000 1010
E25620 L3         TESTB               14                                                  0359  800E    1000 0000 0000 1110
E25630            BRNB                L3                                                  035A  9359    1001 0011 0101 1001
E25700            LOOP1               L4                                                  035B  C358    1100 0011 0101 1000
E25800            TESTB               15                                                  035C  800F    1000 0000 0000 1111
E25900            BRB                 V                                                   035D  A35F    1010 0011 0101 1111
E26000            PAREN  05           07       BIT 8 STATUS                               035E  1507    0001 0101 0000 0111
E27400 V          PAREN  01           32       LOAD WR. CLK DIVIDER                       035F  1132    0001 0001 0011 0010
E27410 V1         TESTB               13                                                  0360  800D    1000 0000 0000 1101
E27420            BRNB                V1                                                  0361  9360    1001 0011 0110 0000
E27500 W          TESTB               13                                                  0362  800D    1000 0000 0000 1101
E27600            BRB                 W        WAIT FOR PH2/                              0363  A362    1010 0011 0110 0010
E27700            LDLC1               194      STROBE INTERVAL = 50 MICROSECS.            0364  40C2    0100 0000 1100 0010
E27800 X          LOOP1               X        DELAY          (200X 250NSEC)              0365  C365    1100 0011 0110 0101
E27900            TESTB               13       SHOULD BE PH2                              0366  800D    1000 0000 0000 1101
E28000            BRB                 Y                                                   0367  A369    1010 0011 0110 1001
```

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PAGE 66                                          TAPEMCON06                                      DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                    ADRS MEMORY BINARY REPRESENTATION

E28100            PAREN  06          07        BIT 7 STATUS                                0368 1607   0001 0110 0000 0111
E28200 Y          BRANCH             REST                                                  0369 600F   0110 0000 0000 1111
E30100 DTESTI2    PAREN  08          0B        READ REG SHIFT MODE                         036A 180B   0001 1000 0000 1011
E30110            PAREN  09          EF        EC 8                                        036B 19EF   0001 1001 1110 1111
E30120            EC        10                 CLEAR READ REG                              036C 3A00   0011 1010 0000 0000
E30200            EA        14                 SET EVEN PARITY                             036D 1F0E   0001 1111 0000 1110
E30300            JUMP               MOVE•BYTE1                                            036E 7378   0111 0011 0111 1000
E30400            BRNB               Z         BIT 15 STATUS (BAD PARITY)                  036F 9371   1001 0011 0111 0001
E30500            PAREN  05          00        BIT 15 STATUS                               0370 1500   0001 0101 0000 0000
E30600 Z          EA        15                 SET ODD PARITY                              0371 1F0F   0001 1111 0000 1111
E30700            PAREN  08          09        DATA TO BYTE 2                              0372 1809   0001 1000 0000 1001
E30800            JUMP               MOVE•BYTE2                                            0373 7379   0111 0011 0111 1001
E30900            BRB                AA                                                    0374 A376   1010 0011 0111 0110
E31000            PAREN  05          01        BIT 14 STATUS                               0375 1501   0001 0101 0000 0001
E31100 AA         JUMP               SUB•DINT                                              0376 7381   0111 0011 1000 0001
E31200            BRANCH             REST                                                  0377 600F   0110 0000 0000 1111
E31300 MOVE•BYTE1        08          08                                                    0378 1808   0001 1000 0000 1000
```

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PAGE 48                                          TAPEMCONDA                                                   DATE   27/09/78
SEQ NO. REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                                   ADRS  MEMORY  BINARY REPRESENTATION

E31400 MOVE•BYTE2 LDLC1           7                                                         0379  4007    0100 0000 0000 0111

E31450            PAREN  08       0B            RD REQ TO SHIFT MODE                        037A  180B    0001 1000 0000 1011

E31500            PAREN  09       EF            EC 5.                                       037B  19EF    0001 1001 1110 1111

E31600 BB         EC                                                                        037C  3000    0011 0000 0000 0000

E31700            LOOP1           BB                                                        037D  C37C    1100 0011 0111 1100

E31800            TESTB           24            CHECK PARITY                                037E  8018    1000 0000 0001 1000

E31900            PAREN  08       00            DISABLE DATA TO BYTE 1                      037F  1800    0001 1000 0000 0000

E32000            RETURN 08       01            DISABLE DATA TO BYTE 2                      0380  2801    0010 1000 0000 0001

E32100 SUB•DINT   EA        06                  BYTE 1 TO OUTBUFFER                         0381  1F06    0001 1111 0000 0110

E32150                      7                   DATA TO 605                                 0382  1F07    0001 1111 0000 0111

E32300 SUB•DINT1  PAREN  04       20            SHORT TIMER                                 0383  1414    0001 0100 0001 0100

E32310            EA        09                  DATA INT REQUEST                            0384  1F09    0001 1111 0000 1001

E32400 DD         TESTB           10            PODINT                                      0385  800A    1000 0000 0000 1010

E32500            BRNB            CC                                                        0386  938A    1001 0011 1000 1010

E32600            TESTB           14                                                        0387  800E    1000 0000 0000 1110

E32700            BRNB            DD                                                        0388  9385    1001 0011 1000 0101

E32800            PAREN  06       05            BIT 05 STATUS(OVERLOAD)                     0389  1605    0001 0110 0000 0101
```

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PAGE 46                                           TAPEMCON06                                      DATE    27/09/78
SEQ NO REFERENCE OPCODE MC EA EB EC OPERANDS   COMMENTS                                 ADRS  MEMORY  BINARY REPRESENTATION
E34900 CC         RETURN                                                                038A  2000    0010 0000 0000 0000
E35000 DTESTX2    LDLC1              08                                                 038B  4008    0100 0000 0000 1000
E35100            EA         12                COMMENTS ODD PARITY                      038C  1F0C    0001 1111 0000 1100
E35200            PAREN  07          08                                                 038D  1708    0001 0111 0000 1000
E35300            PAREN  09          FB            EC3                                  038E  19FB    0001 1001 1111 1011
E35400 EE         EC                           FILL WRITE REQ N. 1'9                    038F  3000    0011 0000 0000 0000
E35500            LOOP1              EE                                                 0390  C38F    1100 0011 1000 1111
E35600            JUMP               WRITE-READ DATA TURNAROUND                         0391  739F    0111 0011 1001 1111
E35700            EA         14                SET ODD PARITY                           0392  1F0E    0001 1111 0000 1110
E35800            JUMP               MOVE.BYTE1                                         0393  7378    0111 0011 0111 1000
E35900            BRNB               FF                                                 0394  9396    1001 0011 1001 0110
E36000            PAREN  05          06        BIT 09 STATUS                            0395  1506    0001 0101 0000 0110
E36100 FF         PAREN  09          EF     EC5                                         0396  19EF    0001 1001 1110 1111
E36200            EC                                                                    0397  3000    0011 0000 0000 0000
E36300            EA         15                SET EVEN PARITY                          0398  1F0F    0001 1111 0000 1111
E36400            PAREN  08          0A        DATA TO BYTE 2 OUTBUFFER                 0399  180A    0001 1000 0000 1010
E36500            JUMP               MOVE.BYTE2                                         039A  7379    0111 0011 0111 1001
```

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PAGE  67                                  TAPEMCONO6                                         DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                                  ADRS  MEMORY  BINARY REPRESENTATION

E36600            SRS                GG                                                  039B  A39D    1010 0011 1001 1101
E36700            PAREN  05          07        BIT 8 STATUS                              039C  1507    0001 0101 0000 0111
E36800 GG         JUMP               SUB•DINT                                            039D  7381    0111 0011 1000 0001
E36900            BRANCH             REST                                                039E  600F    0110 0000 0000 1111
E40200 WRITESREAD PAREN  08          0F                                                  039F  180F    0001 1000 0000 1111
E40300            LDLC1              09                                                  03A0  4009    0100 0000 0000 1001
E40350            PAREN  08          0B        READ REG TO SHIFT MODE                    03A1  180B    0001 1000 0000 1011
E40400            PAREN  09          EB        EC3,5                                     03A2  19EB    0001 1001 1110 1011
E40500 HH         EC                           MOVE DATA FROM WRITE TO READ REG•         03A3  3000    0011 0000 0000 0000
E40600            LOOP1              HH                                                  03A4  C3A3    1100 0011 1010 0011
E40700            RETURN 08          07                                                  03A5  2807    0010 1000 0000 0111
E40800 DTESTI4           12 1                  CLR RD/WR  CRC REGS                       03A6  1F1C    0001 1111 0001 1100
E40900 DTESTI4A   EA        1                  OUTLATCH (FROM 605)                       03A7  1F01    0001 1111 0000 0001
E41000            PAREN  07          00        LOAD MODE                                 03A8  1700    0001 0111 0000 0000
E41100            JUMP               SUB•DINT1                                           03A9  7383    0111 0011 1000 0011
E41200            EA        10                 ODD PARITY (WR)                           03AA  1F0A    0001 1111 0000 1010
E41250            PAREN  07          0C                                                  03AB  170C    0001 0111 0000 1100
```

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PAGE  68                                   TAPEMCON04                                    DATE    27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS   COMMENTS                          ADRS  MEMORY  BINARY REPRESENTATION

E41300            JUMP                WRSHIFT1  SHIFT AND CALC WR CRC             03AC  722F    0111 0010 0010 1111
E41400            JUMP                WRITE-READ                                  03AD  739F    0111 0011 1001 1111
E41500            EA         14                 ODD PARITY (RD)                   03AE  1F0E    0001 1111 0000 1110
E41600            PAREN  06           01        F2 OFF (FOR RDSHIFT)              03AF  1601    0001 0110 0000 0001
E41610            PAREN  08           08        ENABLE BC1                        03B0  1808    0001 1000 0000 1000
E41620            JUMP                RDSHIFT                                     03B1  7042    0111 0000 0100 0010
E41630            TESTB               24                                          03B2  8018    1000 0000 0001 1000
E41700            BRNB                II                                          03B3  93B5    1001 0011 1011 0101
E41800            PAREN  05           02        BIT 13 STATUS                     03B4  1502    0001 0101 0000 0010
E41900 II         EA         11                 SET EVEN PARITY (WR)              03B5  1F0B    0001 1111 0000 1011
E42000            PAREN  07           0D                                          03B6  170D    0001 0111 0000 1101
E42100            JUMP                WRSHIFT1  SHIFT AND CALC WR CRC             03B7  722F    0111 0010 0010 1111
E42200            JUMP                WRITE-READ                                  03B8  739F    0111 0011 1001 1111
E42300            EA         15                 EVEN PARITY (READ)                03B9  1F0F    0001 1111 0000 1111
E42500            PAREN  08           09        ENABLE BC2                        03BA  1809    0001 1000 0000 1001
E42510            JUMP                RDSHIFT                                     03BB  7042    0111 0000 0100 0010
E42520            TESTB               24                                          03BC  8018    1000 0000 0001 1000
```

```
PAGE 69                                   TAPEMCOM06                                    DATE   27/09/78
SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                        ADRS  MEMORY  BINARY REPRESENTATION

E42600            BRNB               KK                                        03BD  93BF    1001 0011 1011 1111
E42700            PAREN  05          03          BIT 12 STATUS                 03BE  1503    0001 0101 0000 0011
E42800 KK         JUMP               SUB•DINT                                  03BF  7381    0111 0011 1000 0001
E42900            TESTB              9           TERMINATE                     03C0  8009    1000 0000 0000 1001
E43000            BRNB               DTEST14A                                  03C1  93A7    1001 0011 1010 0111
E43100            PAREN  07          0A                                        03C2  170A    0001 0111 0000 1010
E43200            LDLC1              09                                        03C3  4009    0100 0000 0000 1001
E43300            PAREN  09          F3          EC3/4                         03C4  19F3    0001 1001 1111 0011
E43400 KK1        EC                                                           03C5  3000    0011 0000 0000 0000
E43500            LOOP1              KK1                                       03C6  C3C5    1100 0011 1100 0101
E43600            JUMP               WRITE-READ                                03C7  739F    0111 0011 1001 1111
E43700            PAREN  03          255         DELAY  250 MICROS. TO LET  605   03C8  13FF    0001 0011 1111 1111
E43800 LL         TESTB              15                                        03C9  800F    1000 0000 0000 1111
E43900            BRNB               LL             RESET  NC.                 03CA  93C9    1001 0011 1100 1001
E43910            PAREN  08          09                                        03CB  1809    0001 1000 0000 1001
E44000            JUMP               RDSHIFT     'AND' RD/WR CRC'S             03CC  7042    0111 0000 0100 0010
E44010            PAREN  08          0B                                        03CD  180B    0001 1000 0000 1011
```

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PAGE  70                                  TAPEMCON06                                      DATE   27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                          ADRS  MEMORY  BINARY REPRESENTATION

E44020            LDLC1              16                                          03CE  4010    0100 0000 0001 0000

E44030            PAREN  08          08                                          03CF  1808    0001 1000 0000 1000

E44040            PAREN  09          EF                                          03D0  19EF    0001 1001 1110 1111

E44050 LL1        EC                                                             03D1  3000    0011 0000 0000 0000

E44060            LOOP1              LL1                                         03D2  C3D1    1100 0011 1101 0001

E44100            JUMP               SUB.DINT                                    03D3  7381    0111 0011 1000 0001

E44200            LDLC1              8                                           03D4  4008    0100 0000 0000 1000

E44300            PAREN  09          DF          EC 6                            03D5  19DF    0001 1001 1101 1111

E44400 MM         EC                                                             03D6  3000    0011 0000 0000 0000

E44500            TESTB              25          CHECK FOR 1 BIT IN LRC          03D7  8019    1000 0000 0001 1001

E44600            BRNB               NN                                          03D8  93DA    1001 0011 1101 1010

E44700            PAREN  05          04          BIT 11 STATUS                   03D9  1504    0001 0101 0000 0100

E44800 NN         LOOP1              MM                                          03DA  C3D6    1100 0011 1101 0110

E44900            LDLC1              08                                          03DB  4008    0100 0000 0000 1000

E45100            PAREN  09          7F          EC 8                            03DC  197F    0001 1001 0111 1111

E45200 PP         EC                                                             03DD  3000    0011 0000 0000 0000

E45300            TESTB              27          RD CRC ALL ZERO'S               03DE  801B    1000 0000 0001 1011
```

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PAGE  71                                      TAPEMCON06                               DATE    27/09/78

SEQ NO  REFERENCE OPCODE MD EA EB EC OPERANDS  COMMENTS                          ADRS  MEMORY  BINARY REPRESENTATION

E45400            BRNB                 00                                        03DF  93E1    1001 0011 1110 0001

E45500            PAREN  05            05        BIT 10 STATUS                   03E0  1505    0001 0101 0000 0101

E45600 00         LOOP1                PP                                        03E1  C3DD    1100 0011 1101 1101

E45700            BRANCH               REST                                      03E2  600F    0110 0000 0000 1111

E45800 DTEST15    LDLC1                10        INVERT ALL DATA BITS            03E3  400A    0100 0000 0000 1010

E45900                      12 01                                                03E4  1F1C    0001 1111 0001 1100

E46000            PAREN  08            0E                                        03E5  180E    0001 1000 0000 1110

E46100            PAREN  09            FD        EC2                             03E6  19FD    0001 1001 1111 1101

E46200 R          EC                             TIE TO ALL 1'S                  03E7  3000    0011 0000 0000 0000

E46300            LOOP1                R                                         03E8  C3E7    1100 0011 1110 0111

E46400            PAREN  08            0A        ENABLE INVERT                   03E9  180A    0001 1000 0000 1010

E46500            BRANCH               DTEST14A                                  03EA  63A7    0110 0011 1010 0111

END
```

COMMENT SHEET

MANUAL TITLE CONTROL DATA® FA107-A Magnetic Tape Controller

Hardware Reference/Maintenance Manual

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