96768610 03

CONTROL DATA CORPORATION

CDC® CYBER 18-25/30 TIMESHARE COMMUNICATIONS MULTIPLEXER

GENERAL DESCRIPTION
OPERATION
INSTALLATION
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE

HARDWARE REFERENCE/MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
01	Preliminary release.
(4/77)	
02	Manual revised; includes Engineering Change Order DS21799, providing new product information. The front
(1/80)	cover, pages vii/viii, x, 1-1, 1-3, 1-9, 2-4, 2-28 and 6-2 are revised.
03	Manual revised; includes Engineering Change Order DS21879, providing new product information. Pages vii/viii
(3/80)	1-6, 1-7 and 2-4 are revised.

Publication No.
96768610

REVISION LETTERS I, O, Q AND X ARE NOT USED

Printed in the United States of America

Address comments concerning this manual to:
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Publications and Graphics Division
4455 Eastgate Mall
La Jolla, California 92037
or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
DY 192-A DY 198-A			

LIST OF EFFECTIVE PAGES

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PREFACE

This manual provides programming reference and maintenance information relative to the CDC® CYBER 18-25/30 Timeshare System Communications Multiplexer. The communications multiplexer provides communication between terminal/modem communication lines and the CYBER 18-25/30 communication processors.

The manual is intended to serve programmers and customer engineers who require detailed machine-level information about the communications multiplexer. Detailed information regarding overall CYBER 18 system-level programming and maintenance is provided in several available system reference/maintenance manuals.

Additional information may be found in the following publications:

Publication	Publication Number
AA132, AA133, DT120, FC402 CYBER 18 Computer Systems Central Processor Field Repair Guide	60475001
CYBER 18 Computer Systems with MOS Memory Installation Manual	96768360
CYBER 18 MOS Processor Reference Manual	96768300
DY192, DY198, DU137, GH447, GH461 Communication Multiplexer Subsystem Hardware Maintenance Manual	60475080
MSMP Diagnostic Reference Manual	96700000
2561 Asynchronous Communication Line Adapter Hardware Reference/Maintenance Manual	74700900

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FIGURES

TABLE

This manual contains hardware maintenance and programming reference information relative to the Communications Multiplexer used in the CYBER 18-25/30 Timeshare system. The hardware information is provided to help maintenance personnel understand the functional operation of the communications multiplexer. The programming information provides reference data to help programming personnel understand the operational characteristics of the communications multiplexer.

COMMUNICATIONS MULTIPLEXER OVERVIEW

The communications multiplexer (COMMUX) contains the hardware, firmware, and software elements which provide the data and control paths for information flow between communications lines and user program software. Many of the line/protocol dependent functions that were performed by fixed hardware in previous systems are implemented in common alterable firmware/software. This allows reduced development and reoccurring hardware costs for each line and protocol that is added to the communications system.

The primary task performed by the COMMUX is to receive data from many communications lines and distribute the characters to line-related input buffers, and to obtain characters from line-related output buffers and distribute these to communications lines. The system provides for special table-driven and dynamically controlled processing on each character as it is being distributed from a communications line. Circuit, modem and system status is detected and transferred in the form of work demands to user programs for processing. Control information received from user programs in the form of commands to the COMMUX are decoded and executed within one or more system element.

The multiplexing scheme used in the COMMUX design is based on a demand-driven multiplex loop concept. The mechanism gathers input data and status from, and distributes output data and control to, many communications lines on a real-time basis. The design provides an economical method of connecting many communications lines to a controlling processor while using a minimum of the processor's resources to manage the mechanism.

The primary functional elements of the mechanism are the communications line adapters (CLAs) that provide character assembly/disassembly and communications line/modem interface; the input loop which transports data demands, data and status from the CLAs to the controlling processor (CP); the output loop which transports data and control from the controlling processor to the CLAs; the multiplex loop interface adapter (MLIA) which controls the movement of data demands, data and supervision between the input and output loops and the controlling processor; and the loop multiplexers (LMs) which provide access to the input and output loops by the CLAs.

MULTIPLEX LOOP INTERFACE ADAPTER

The multiplex loop interface adapter (MLIA) can connect the CP to as many as two loop multiplexers (LMs) (depending on whether there are one or two LM card cages in the system, where each cage contains one LM). Since each LM can interface with as many as 32 communications line adapters (CLAs), the MLIA accommodates as many as 64 communications channels. The MLIA operates each loop at a speed of 20×10^6 bits per second.

The MLIA comprises three functional units:

1. Processor interface
2. Output loop interface
3. Input loop interface

All communications between the CP and the MLIA are routed through the processor interface logic. The output loop interface logic controls the operation of the output loop, and distributes outbound traffic to the LMs. The input loop interface logic controls the input loop and gathers inbound traffic enroute to the CP.

LOOP MULTIPLEXER

The loop multiplexer (LM) serves as the interface between the CLAs and the input and output loops. The LM receives outbound traffic on the output loop and presents the data (in parallel form) to the CLAs. The LM also receives data in parallel form from the CLAs, serializes this data, and presents it to the input loop. The LM operates at a speed of 20×10^6 BPS (controlled by the MLIA).

COMMUNICATIONS LINE ADAPTERS

The communications line adapter (CLA) interfaces the specific terminal communications circuitry to the LM. A number of CLA types, each having differing electrical and functional characteristics, are presently available. In conjunction with parameter and mode control registers

which are set under program control, the CLAs interface with a wide variety of terminal types. In addition, the CLAs constitute a product line which is under continuing development. It is recommended that the user refer to the Hardware Reference and Maintenance manual(s) for the functional characteristics of the specific CLA type(s) selected for his system (see Preface).

PHYSICAL DESCRIPTION

COMMUNICATIONS MULTIPLEXER

The communications multiplexer comprises the following major system components:

1. Multiplex loop interface adapter (MLIA)
2. Loop multiplexer (LM)
3. Communications line adapters (CLAs)

MULTIPLEX LOOP INTERFACE ADAPTER

The multiplex loop interface adapter (MLIA) comprises the following three printed circuit cards which are located in the slots indicated in the CP card cage assembly (see figure 1-1):

Card Slot	Printed Circuit Card Nomenclature
E	Input loop interface
F	Output loop interface
G	Processor interface

Each of these circuit cards is 11 in. x 14 in. (28 cm x 36 cm).

LOOP MULTIPLEXER AND COMMUNICATIONS LINE ADAPTERS

The loop multiplexer (LM) is located in the second circuit card slot from the right, in the LM card cage assembly as shown in figure 1-2.

The 16-circuit card slots to the left of the LM can be used for CLAs. A typical CLA installation is shown in figure 1-2; however, the total number of CLAs used, as well as the types of CLAs, is determined by the user.

In systems with two LM card cages both cages have the same placement of LM and CLA cards as that described above for the LM card cage assembly.

The LM and CLA circuit cards are 11 in. x 14 in. (28 cm x 36 cm). A narrow (7/8-inch (2.2 cm)-wide) control panel is mounted on the front-facing edge of each card.

The LM printed circuit card contains a power (PWR) switch and the following four light-emitting diode (LED) indicators:

1. IN LOOP CLK
2. IN LOOP DATA
3. OUT LOOP CLK
4. OUT LOOP DATA

The function of these controls and indicators is described in section 2 of this manual.

The CLA controls and indicators vary according to the type(s) of CLAs selected, and the user should refer to the appropriate CLA manual(s) (see Preface).

REFERENCE DATA

WIRED CABINET ASSEMBLY

The following major system components are installed in the wired cabinet assembly:

1. Power supply
2. Air blower and filter assembly
3. Cabling

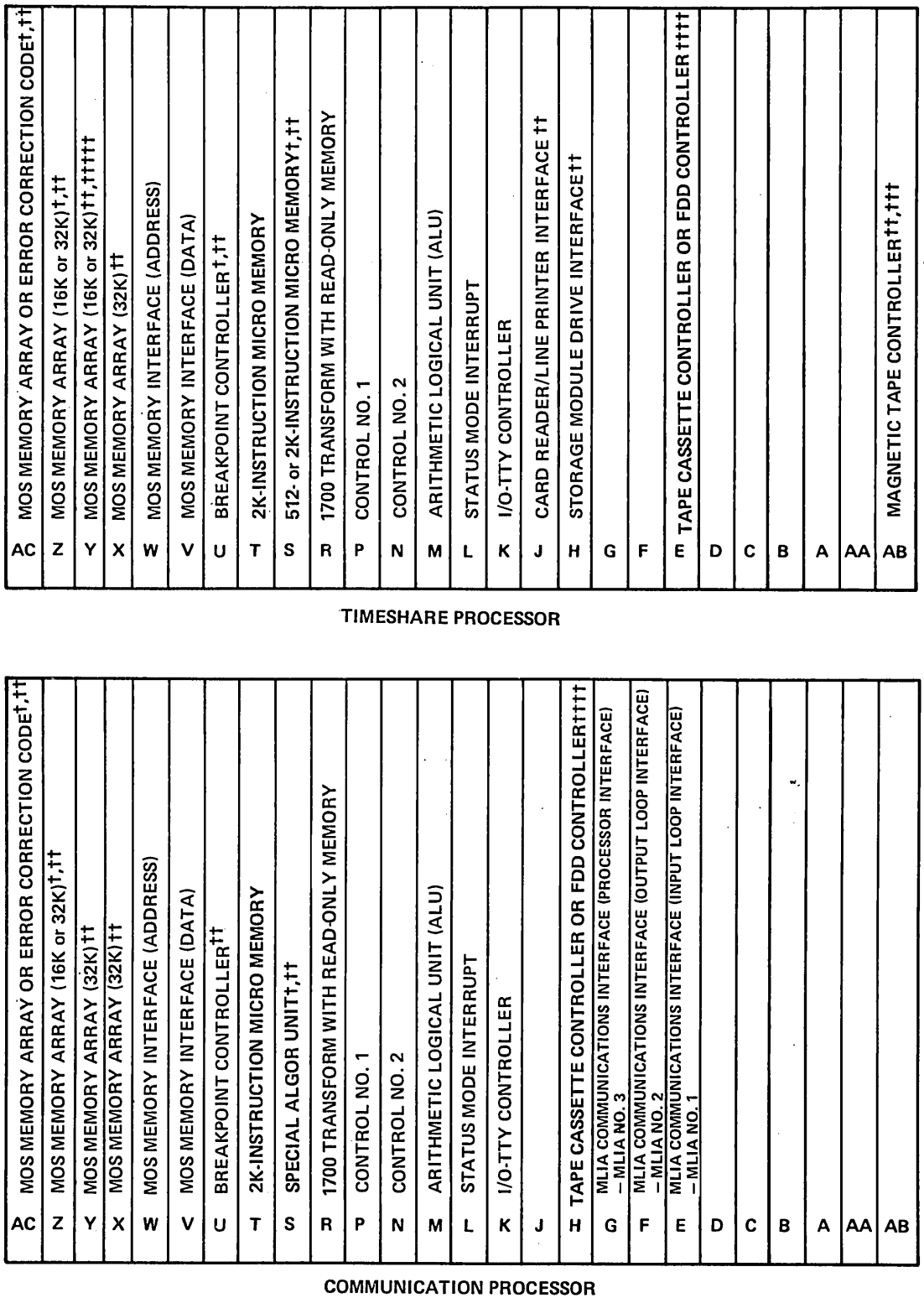
LOOP MUX CARD CAGE POWER SUPPLY

As shown in figure 1-3, one power supply is provided with the loop MUX card cage assembly.

The power supply is mounted on a bracket at the center-right side of the cabinet as seen from the rear door through which access to the supply is obtained (see figure 1-4). The power supply has the following dimensions:

Height:	11.75 in. (29.85 cm)
Width:	7.0 in. (17.78 cm)
Depth:	5.1 in. (12.95 cm)

This power supply is a single unit which comprises three functional elements. One of these is a +5V, 150 amp supply, the other two are both +12V units which have been



† CYBER 18-30 EXPANSION
†† CYBER 18-25 EXPANSION
††† NRZI ONLY
†††† TAPE CASSETTE CONTROLLER INCLUDED WITH THE CYBER 18-30
FDD CONTROLLER INCLUDED WITH THE CYBER 18-25
††††† 16K MOS MEMORY ARRAY INCLUDED WITH THE CYBER 18-30

Figure 1-1. CYBER 18-25/30 Timeshare Printed Wiring Assembly Slot Assignments

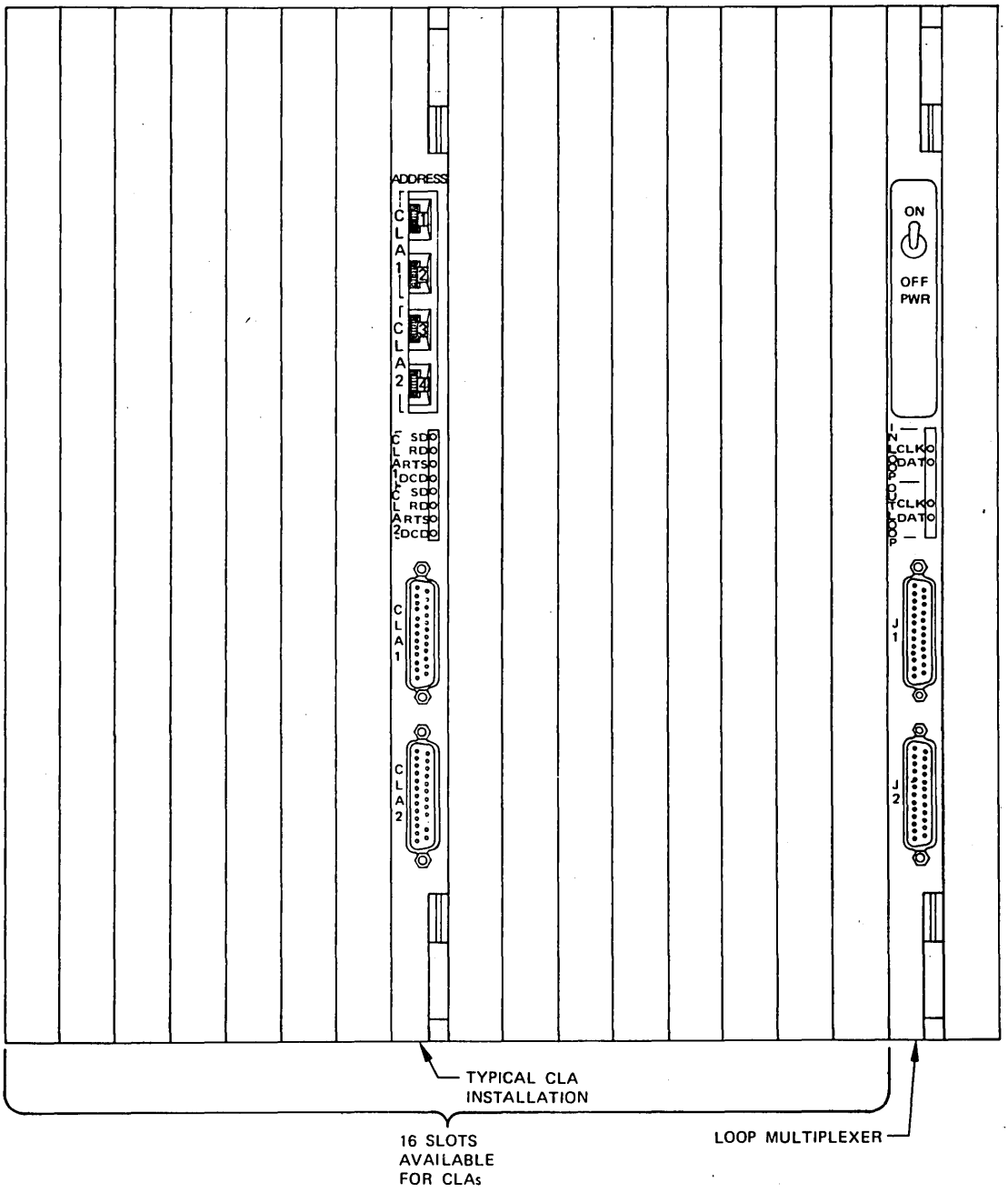


Figure 1-2. Location of Loop Multiplexer and Typical Communications Line Adapter

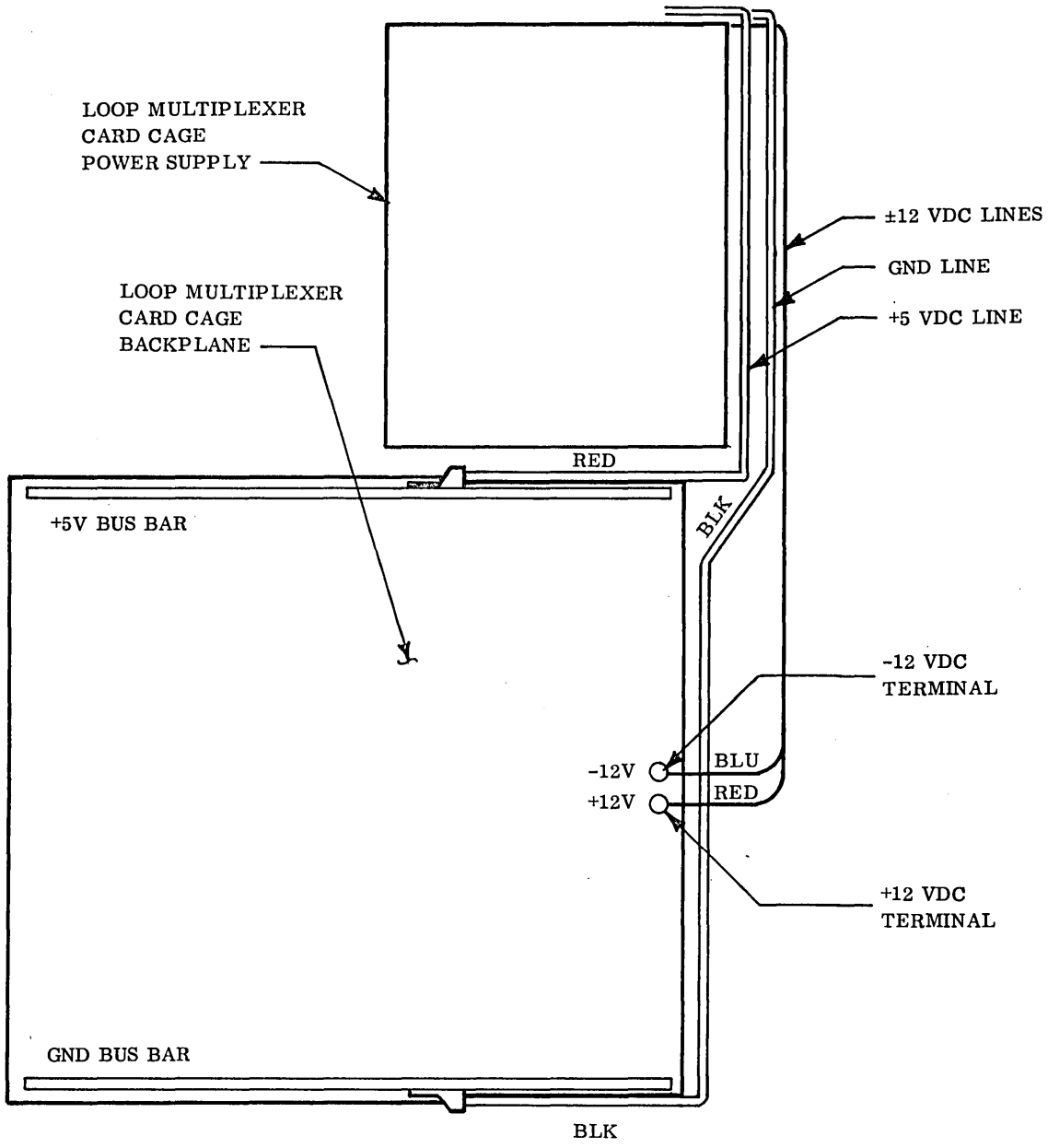


Figure 1-3. Rear View of Loop MUX Card Cage and Card Cage Power Supply

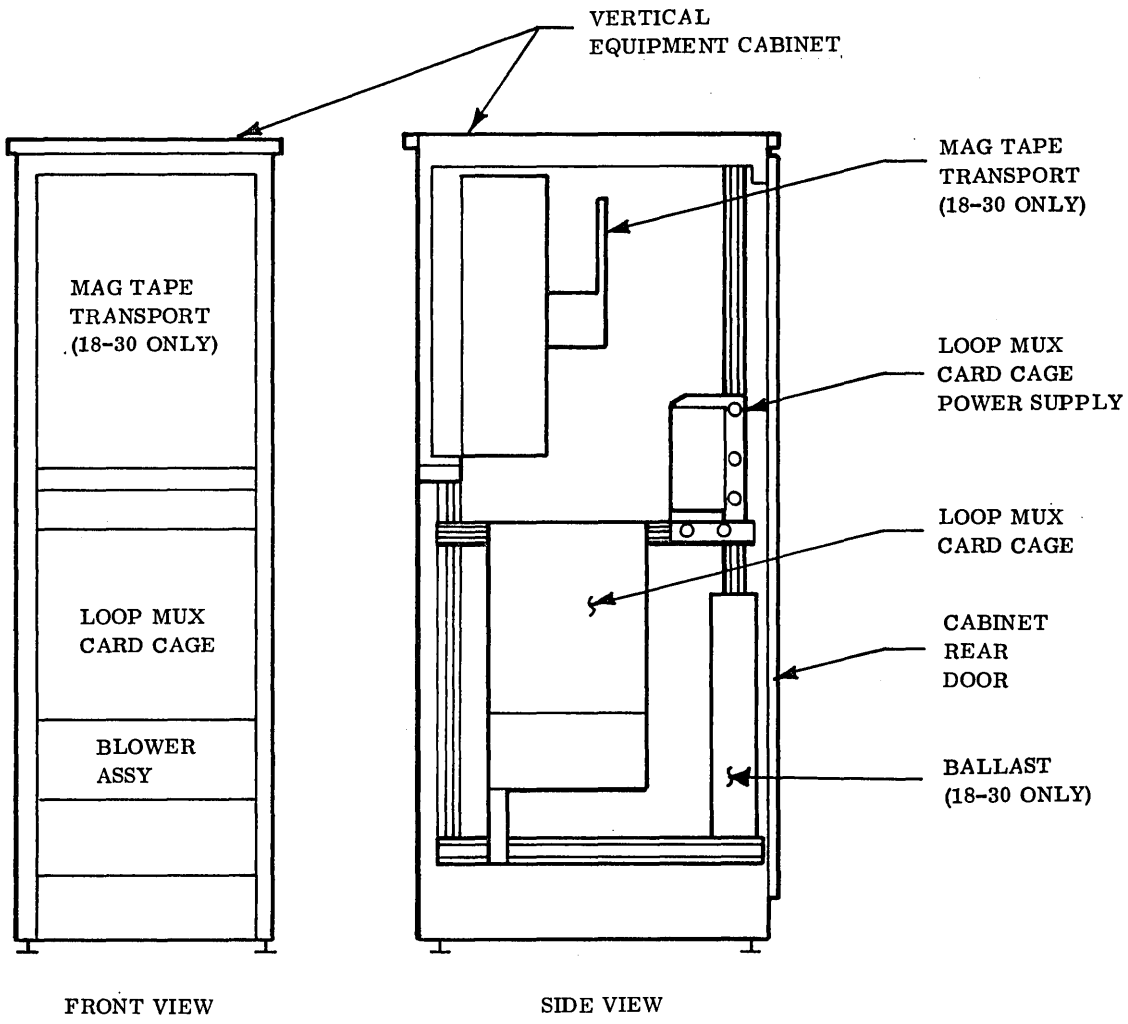


Figure 1-4. Loop MUX Card Cage Power Supply Location

interconnected to provide ±12V outputs. The power supply requires input power of 15 amps (worst case).

LOOP MULTIPLEXER AIR BLOWER AND FILTER ASSEMBLY

As shown in figure 1-5, one air blower and filter assembly (ABFA) is provided with the LM card cage assembly.

The loop multiplexer ABFA is mounted beneath the LM card cage assembly in the lower area of Bay O. This unit has the following dimensions:

Width:	19.0 in. (48 cm)
Height:	7.7 in. (20 cm)
Depth:	11.7 in. (30 cm)

The unit contains two fans which provide a flow of cooling air for the LM card cage. Each fan is rated at 260 CFM. The unit also contains a filter.

The general air circulation scheme provides for the intake of cooling air at the front and rear surfaces of the cabinet near the floor. Cooling air is then directed upwards through the card cage assembly and power supply, and warm air is exhausted through the top of the cabinet.

CABLING

The cabling for the COMMUX is described in detail in the Installation Manual (see Preface).

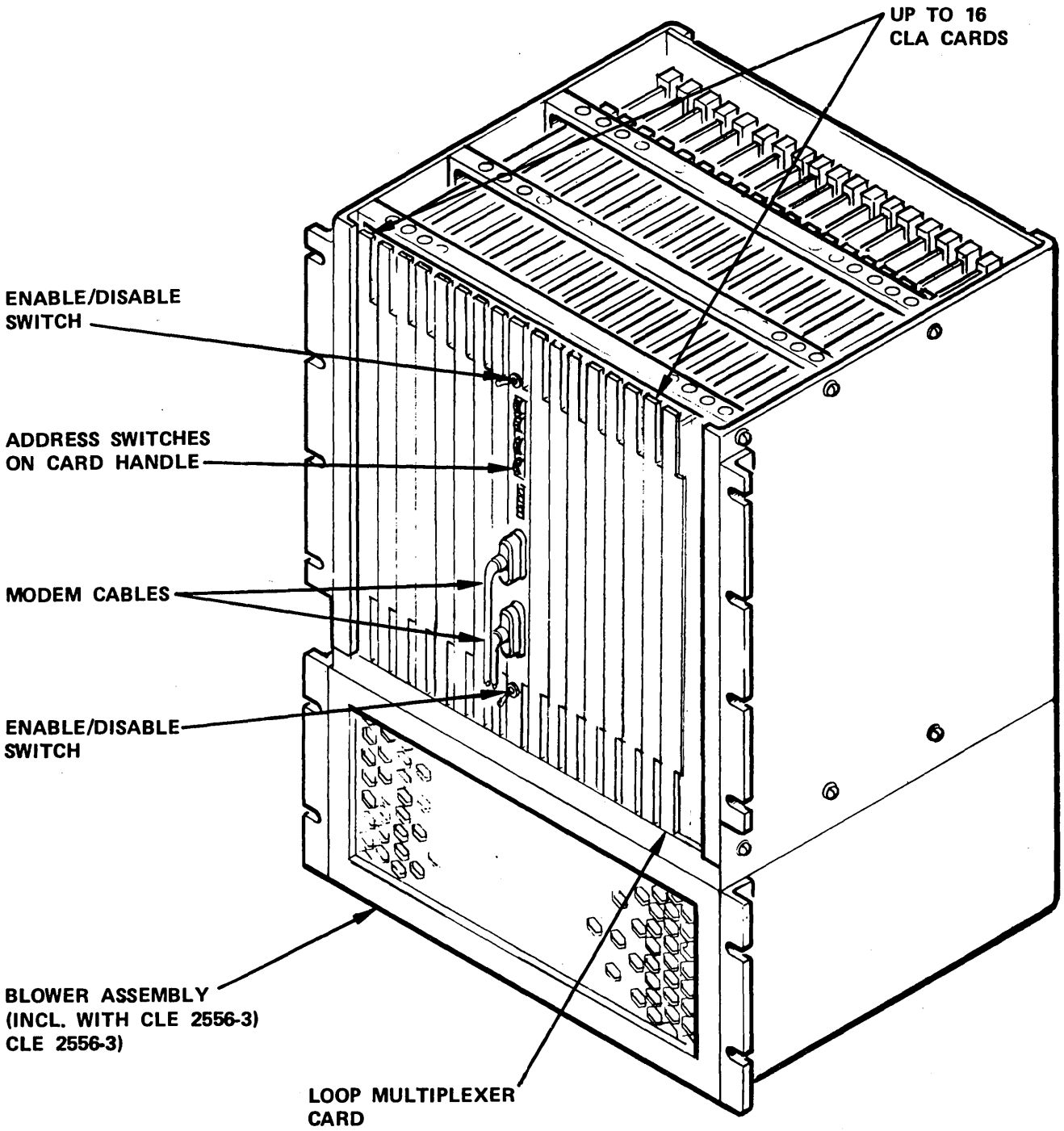


Figure 1-5. Typical LM Card Cage Assembly

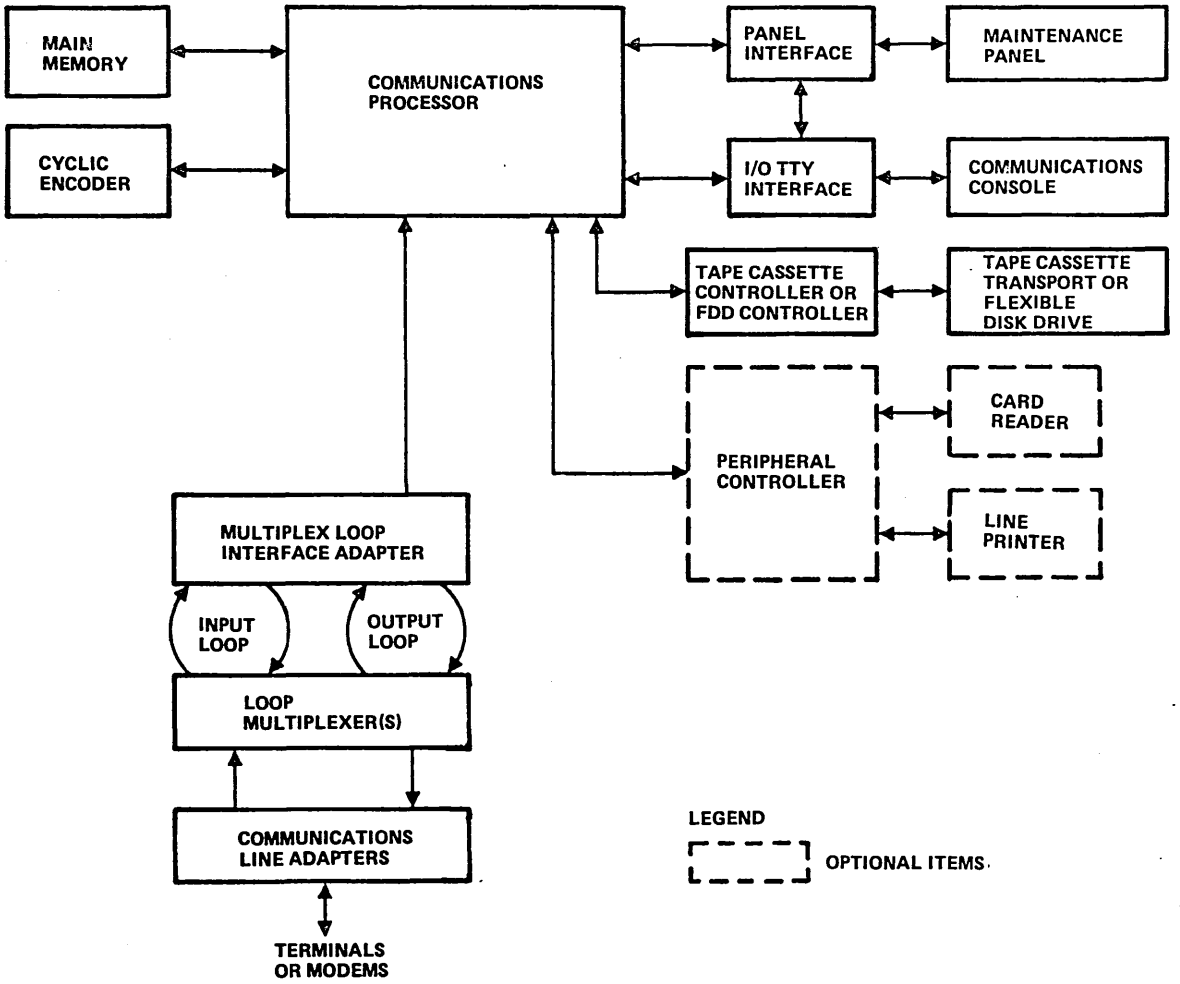


Figure 1-6. Main Data Paths

This section contains functional descriptions of internal and external controls, external indicators, and programming reference material for the communications multiplexer. External controls are switches which are used primarily for maintenance purposes. Internal controls are those elements of the software and firmware that control internal COMMUX functions such that external operations are affected. External indicators are used primarily for maintenance purposes. There are no operator controls in the COMMUX.

COMMUNICATIONS MULTIPLEXER

The communications multiplexer (COMMUX) contains the hardware, firmware, and software elements which provide the data and control paths for information flow between communication lines and user program software (figure 2-1). Many of the line/protocol dependent functions that were performed by fixed hardware in previous systems are implemented in common alterable firmware/software allowing reduced development and reoccurring hardware cost for each line and protocol that is added to the communications system.

The purpose of the COMMUX is to gather data from the various terminal devices and deliver this data to the CP, and to receive data from the CP for distribution to the appropriate terminal devices. In performing this data movement (e.g., from terminal to CP) all unique signal characteristics not requiring knowledge of the meaning of the bits are stripped out. These signal characteristics include: data rate, synchronous or asynchronous transmission, parity or no parity, number of bits (5, 6, 7 or 8), and serial or parallel form. All information arrives in CP memory in bit-parallel, right-justified form. Control codes, error control and other housekeeping bits are removed.

Similarly, information from the CP is formatted and conditioned sufficiently to permit transmission to any modem or local peripheral. Differences which require knowing the meaning of the bit (e.g., protocol, code type, etc.) are handled by CP software.

The heart of the COMMUX comprises two high-speed digital data circuits called multiplex loops (see figure 2-1). One of these loop circuits handles input data which is enroute to the CP from the terminal devices. This is designated as the input loop. The other loop handles output traffic from the CP to the terminals and is called the output loop. Loops serve to transport the data physically between terminals and CP, and also to resolve simultaneous input requests.

The multiplex loops are demand-driven. When action is required by a terminal circuit interface, a "demand service" request is generated and transmitted to the communications processor via the input loop.

The key to the ability of the system to operate in a demand-oriented fashion lies in the nature of the multiplex loop. The multiplex loop can be compared to a railroad track, and the multiplex loop interface adapter (MLIA) and the loop multiplexer (LM) which it connects can be compared to stations on the railroad. Data on the multiplex loop are analogous to the passengers on trains which are operating on this railroad track.

The primary functional elements of the mechanism are the communications line adapters (CLAs) that accomplish character assembly/disassembly and communications line/modem interface; the input loop which transports data demands, data and status from the CLAs to the controlling processor; the output loop which transports data and control from the controlling processor to the CLAs; the multiplex loop interface adapter (MLIA) which controls the movement of data demands, data and supervision between the input and output loops and the controlling processor; and the loop multiplexer(s) (LM) which provide access to the input and output loops by the CLAs.

Multiplex action on the input loop occurs when the multiplex loop interface adapter issues a loop end control signal on the input loop. As the signal propagates around the loop, each loop multiplexer in turn has an opportunity to put data and/or supervision from the CLAs on the loop. The loop multiplexers, that have information from one or more CLAs to place on the loop, monitor the loop for the "loop end" signal, place the information from the CLAs on the loop, and replace the "loop end" signal. The multiplex loop interface adapter transfer the information received on the input side of the input loop to buffer storage for processing by the controlling processor.

The multiplex loop interface adapter takes addressed information from buffer storage under direction of the controlling processor and transmits this information on the output loop. The loop multiplexer receives the addressed information blocks and presents the address to all CLAs. The CLA recognizing its address is selected and the information is transferred from the output loop to the CLA.

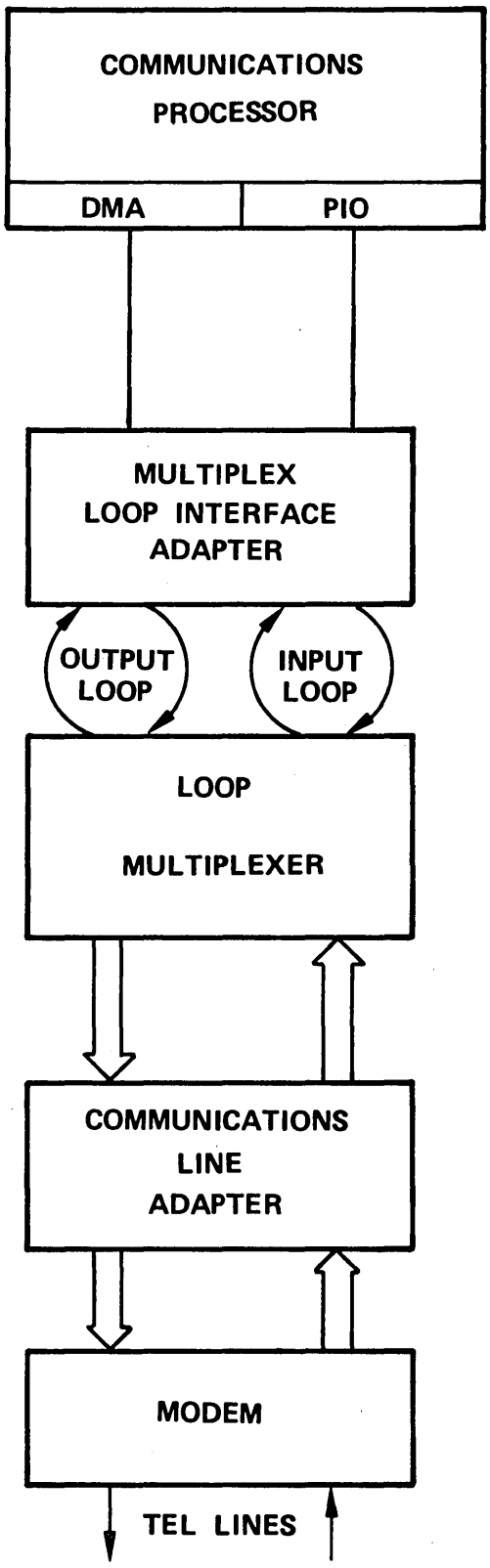


Figure 2-1. Typical Communications Multiplexer Application

LOOP TRANSMISSION

Data transmission on the multiplex loops is serial at a fixed rate of 20 mHz. Every twelfth bit is a cell frame marker that defines a 12-bit loop cell. The cell frame marker is followed by a cell identification field (3 bits); its contents define the meaning of the remaining field (8 bits) of the loop cell.

A contiguous group of loop cells starting with a CLA address and ending with a cyclic redundancy checksum (CRC) is called a line frame. A line frame contains data and/or supervision related to a single CLA. Line frames are made up of four different types of loop cells; "address," "data," "supervision," and "cyclic redundancy checksum (CRC)." Line frames carry data and supervision loop cells on the loops between the CLAs and the controlling processor.

The "CLA address" loop cell carries output data demands (ODDs) as well as a unique binary number (address) of the CLA which is independent of the CLA's physical location within the system. An output data demand is a request from a CLA to the controlling processor for data to be sent to the CLA for subsequent transmission on the communication line by the CLA.

"Data" loop cells contain up to 8 bits of information (one character) that is to be transmitted to or has been received from communication lines. The number of data characters per line frame is limited by the hardware to a maximum of 16, but best performance is obtained by sending only one instance of data and/or supervision per line frame. This will normally be one data and two supervision characters if supervision is present at all. Supervision takes the form of commands outbound and status inbound.

INPUT SEQUENCE

Data from remote terminals are received in serial fashion over the communications lines and placed into single character buffers in the communications line adapter (CLA). When an entire character is received, the CLA notifies the LM by signalling on a special line associated with each CLA. At this time the CLA buffer is acting as a waiting room for the passengers (data) wishing to board the train to the MLIA.

Empty trains are originated at the MLIA. The trains, called input loop batches, are composed of loop cells which are the cars of the train in the analogy. A loop cell contains 12 bits which comprise eight bits of cell information, three bits of cell identification and a 1-bit frame marker. The frame marker designates the start of a cell.

As an input train passes an LM which has input data to be forwarded to the CP, the LM marks the first empty frame as a CLA address by setting the appropriate cell identification, and places the CLA address in the eight information bit locations. The subsequent empty cell is marked as data and the data from the CLA is placed in the information bit locations. If a CLA has supervisory information it is placed in subsequent cells. The next empty cell is labeled as a cyclic redundancy checksum (CRC) cell; the information bit locations are filled with a special checking code.

The train returns to the MLIA which utilizes the CRC to verify the incoming data. If the data is incorrect, the next loop batch will identify the data that was incorrectly received, and the MLIA will initiate error recovery procedures. If the input data is found to be correct, the MLIA will transmit the data to the CP along with the associated address. The MLIA initiates action to start the next train on the input loop as soon as the previous one returns.

The above sequence is repeated for all other CLAs connected to that LM; then, CLAs connected to adjacent LMs are handled until there are either no data bits left in the CLAs, or no empty cells left in the train.

OUTPUT SEQUENCE

Data output is accomplished in a manner functionally similar to input. In this case, trains of data originated by the MLIA on the output multiplexer loop (usually in response to output data demands) are not empty. Here, the output loop batches are composed of cells which specify the destination and content of a message, as well as certain supervisory information regarding its transmission.

The destination portion of the data transmission is in the form of a loop cell which contains, in its information field, the address of the CLA which is to receive the data. The content portion of the data transmission is carried in the information field of the loop cell which immediately follows the CLA address cell. The third portion of the data transmission consists of one or more cells (usually two) identified as supervisory cells. The information contained in these cells is used for CLA command functions which are described later in this section.

Finally, there is a CRC cell signifying the end of the activity for that CLA. The output loop batch may contain output data and commands for a number of CLAs.

Once the data flow from the CLA to the remote terminal has begun, the CLA will initiate a demand signal when more data is required. The CLA signals the LM in a

manner similar to that for announcing the presence of data. The LM then uses an empty loop cell in the next input train to notify the MLIA that the CLA needs more data. This input train comprises two cells. The first cell contains the output data demand (ODD) signal and the CLA address. The second cell contains a CRC for error checking. Upon receipt of the ODD command, the MLIA in turn notifies the CP to transmit the next character.

This concludes an overview of the function of multiplexing subsystem as a whole. The following three subsections describe, in much greater detail, the function of the three principal hardware components of the multiplexing subsystem: MLIA, LM and CLA.

MULTIPLEX LOOP INTERFACE ADAPTER

The multiplex loop interface adapter (MLIA) provides the interface between the CP and the multiplex loop.

The MLIA is designed to gather input data from as many as eight LMs. Since each LM can interface with as many as 32 CLAs (16 cards), each MLIA is capable of receiving data from as many as 256 CLAs. The maximum number of CLAs used in the CYBER 18-25/30 configuration, however, is 64. In a single card cage system, a maximum of 32 CLAs (16 cards) can be used and in a dual card cage system 64 CLAs (32 cards) is the maximum.

The MLIA performs limited editing and checking functions on the input data, and deposits the data directly into a large circular buffer in main memory via the direct memory access (DMA) channel.

The MLIA receives ODD signals from the CLAs and forwards these to the CP as high-priority interrupts. The MLIA then receives output data from the CP via the internal data channel (IDC), and distributes the data to the LMs. The MLIA provides first-in, first-out (FIFO) buffering for input data, ODD signals and output data.

Input Functional Sequence

The following is the sequence of input functions performed by the MLIA:

1. The MLIA generates and transmits clock, loop end, empty and null cells on the output side of the input loop to solicit information from the CLAs.

2. It monitors the input side of the input loop for:

   a. Clock

   b. Loop synchronization

   c. Information placed on the loop by the LMs that must be stored in memory

   d. Loop end cells for error control

3. The MLIA checks the CRC character, and stores each line frame received on the input loop in the CP circular input buffer (CIB) via the DMA channel.

4. After receipt of the loop end cell on the input side of the input loop, anotherempty loop batch will be generated immediately. This provides the maximum rate of loop-end generation without allowing more than one loop end cell on the loop at any one time.

Output Functional Sequence

The following is the sequence of output functions performed by the MLIA:

1. The MLIA detects ODD signals received from the CLAs on the input loop and provides for special priority processing of the ODDs.

2. Processing of the ODDs requires that the MLIA obtain the next character from the CP and transmit this character on the output loop. (The ODD processing function is controlled by the firmware.)

3. The MLIA transmits line frames on the output loop on command from the CP.

   a. Output line frames contain CLA address, data characters, CLA commands (if any) and CRC.

   b. The CRC is generated for each line frame by the MLIA and is transmitted as the last cell of each line frame.

4. The MLIA monitors the input side of the output loop for loop synchronization and loop batch timeout, which are used for error recording and diagnostics.

MLIA PARTITIONING

The MLIA is functionally partitioned into three parts:

1. Processor interface

2. Input loop interface

3. Output loop interface

PROCESSOR INTERFACE

The processor interface controls the MLIA's communication with both the internal data channel (IDC) and direction memory access (DMA) channel of the CP.

Three operating parameter words are received from the CP via the IDA: flag, null and empty (FNE). These FNE parameters establish the amount of information that can be accumulated during each scan of the input loop. Two other words define the length and location of the CP's circular input buffer (CIB) where the incoming data is to be placed. Operational commands, such as ODD limit, are also received via the IDC channel.

The MLIA processor interface consists of the following eight function elements:

1. ODD Limit and CIB Length Parameters Registers — The ODD limit parameter sets the threshold for the number of ODD signals that the CP allows to be held in the MLIA. When this threshold is reached, the input loop train is temporarily halted. The CIB length parameter sets the size of the CIB in the CP. This parameter operates under firmware control.

2. CIB Location Address Parameter Registers — The CIB address parameter sets the locations within the CP memory that can be used for input storage. This parameter operates under firmware control.

3. FNE Parameters Register — The following FNE parameters operate under firmware control:

   a. The F parameter sets the quantity and types of flags that may be used in the input and output loop.

   b. The N parameter sets the number of null cells allowed on the input loop and changes with traffic load.

   c. The E parameter sets the number of empty cells allowed on the input loop and changes with the traffic load.

4. Status Registers — The status registers report the operational status of the MLIA to the CP.

5. Input Loop Launch Control — The input loop launch control is used to control the generation of the input loop train, and is controlled by the ODD limit and FNE parameters.

6. CIB Address Generator — The CIB address generator receives input parameters from the CIB length and CIB location registers, and chooses the location within the CIB for storing blocks of information. This generator operates under firmware control.

7. Last Frame Position Pointer — The last frame position (LFP) pointer is only changed after a complete block of information has been loaded into the CIB by the MLIA.

8. Interface Buses — Finally, the processor interface circuit card contains three buses which provide the proper electrical interfaces for the exchange of operating parameters.

INPUT LOOP INTERFACE

The input loop interface controls operation of the input loop which gathers ODDs and other incoming data. A serial, 20-megabit-per-second line is connected sequentially to each LM, and then returns to the input side of this logic. The loop is continually being scanned for any inbound traffic (ODDs, data or supervision).

The following is the functional sequence for the MLIA input loop interface:

1. Cell Generator — Starting here, the loop end cell, followed by empty and null cells, is generated. The loop end timer is activated and the train starts around the loop.

2. Parallel-to-Serial Converter — When the train arrives at this converter, the 12-bit cells are converted to a 20-megabit-per-second serial stream and sent via a clock and a data cable to the string of LM and CLAs.

3. Loop Multiplexers — If an LM has information from any of its 32 CLAs, it posts a flag; the LM then searches the loop for a loop end cell followed by at least one empty cell. When the LM detects this combination of cells, it removes the loop end cell and starts replacing the empty and null cells with data and/or supervision.

   Groups of cells are divided into line frames. Line frames start with a CLA address and end with a cyclic redundancy checksum (CRC).

A line frame contains data and/or supervision related to a single CLA. As the loop travels through an LM, each CLA associated with that LM can place one line frame on the loop. The LM replaces the loop end cell on the end of the train, and passes the loop batch on to the next LM.

The LM next in line then searches for the loop end cell followed by at least one empty cell. If this combination is detected, the LM removes the end cell, loads data on the loop, replaces the end cell, and passes the loop batch on. Each LM is serviced in turn until all have been serviced, or the loop has no more empty cells. If an LM has no data for the loop it will not inhibit loop progress. The amount of traffic that can be accepted by each loop batch is controlled by the CP via the FNE parameter in the MLIA.

4. Serial-to-Parallel Converter — After the last LM has been serviced the loop batch is sent back to the MLIA and converted from serial to parallel form.

   a. Sync Detector — Here the data is checked for synchronization, format, sequence, etc., to ensure a high degree of traffic integrity.

   b. CRC Check — Here the error control characters are checked to verify proper transmission.

5. Edit Logic — Edit logic strips off the ODDs and sends them to the ODD FIFO buffer with a flag for high-priority interrupt. The remainder of the data is sent to the main input FIFO buffer.

6. Main Input FIFO Buffer — The main input FIFO buffer can store 64 16-bit words, and is flagged with an interrupt (input line frame interrupt) whenever a complete line frame has been placed in the CIB. Its main purpose is to eliminate the need for the firmware comparing the CIB read and write pointers in order to detect recent activity. Data is extracted from the main FIFO buffer as required by the CP.

7. Output Data Demand FIFO Buffer — ODDs are removed from the data train by the edit logic and sent to the ODD FIFO buffer. Presence of ODDs is flagged with a high priority interrupt (output data demand interrupt). The ODD FIFO buffer can store eight characters containing eight bits each, and the buffer is serviced within 20 microseconds under firmware control.

8. Loop End Detector — Loop end cells are sent to the loop end detector. The loop end timer, started with the launching of the train, then stops and orders a new loop batch to be generated. If it appears that the MLIA input buffers may be overrun, the order to form a new loop batch will be delayed by firmware control until the probability of overrun is reduced.

OUTPUT LOOP INTERFACE

The output loop interface controls the operation of the output loop, which distributes outgoing information to the LMs. A serial, 20-megabit-per-second line connects sequentially to each LM and then to the input side of this logic. Information to be sent is received via the IDC and accumulated in the output buffer. As soon as all messages that are to be distributed during the next loop scan have been received (usually one), the characters are converted to serial form; error control and housekeeping characters are added and the entire batch is sent out on the loop. This starts the loop timer. The timer stops when the message is returned to the MLIA via the output loop. Should a problem occur on the loop and the message does not return to the MLIA within the allotted time, the timer generates an error signal. During period of no traffic, empty cells are sent to ensure loop continuity and maintain synchronization.

The following paragraphs describe the functional sequence for the MLIA output loop interface.

Loop and empty cells are continuously generated and transmitted. As soon as the loop end cell returns on the loop, another cell is transmitted even if data is not available in the output buffer; this ensures loop continuity and synchronization.

When the CP has output information to be transmitted, the data is routed from the IDC to the output buffer. The output buffer can store 16 words of 16 bits each; the buffer holds information until the next loop train is started. The parallel-to-serial converter places the output data on the serial loop. CRC signals are added for each CLA message and accumulated for error checking. The loop batch is then transmitted to the LMs.

The output section of each LM receives contiguous loop cells from the MLIA or the preceding LM on the loop. The LM utilizes empty cells to synchronize with

the data stream. When synchronized, the LM looks for a CLA address as frame boundary, and passes loop cells within the frame to the CLAs. All CLAs connected to the LM are connected on a common bus, and each CLA has a unique address.

When the LM has received a CLA address loop cell, it presents the cell to all CLAs on the common bus. The CLA with the corresponding address is selected and connects itself to the output bus. The following loop cells, containing data and/or commands, are then transferred from the output loop to the selected CLA; transfer continues until the LM detects the CRC cell which signals the end of the line frame. The LM checks the received CRC against the CRC accumulated for the line frame, and if a difference is detected, the selected CLA is notified of the error prior to deselection. The LM then passes the loop on to the next LM and back to the MLIA.

The loop batch then returns to the MLIA and is converted back to parallel form. Synchronization is checked, errors (if any) are accumulated, and loop time is stopped. An order to start a new loop batch is then initiated. Had the train not been received back, the timer would have timed out, signalling an error condition.

LOOP MULTIPLEXER

The loop multiplexer (LM) serves as the interface between the CLAs and the input and output loops. The LM assembles loop cells from the output loop, and presents data in parallel form to the CLAs. The LM also accepts data in parallel from the CLAs, serializes this data, and presents it to the input loop.

INPUT SECTION

The input section of the LM receives contiguous loop cells from the preceding LM or from the MLIA. When not synchronized to the data stream, the LM passes all information received to the next LM or to the MLIA. The clock signal is reconstructed to specification when passed sequentially to the next element in the system.

The LM utilizes the unique combination of a loop end cell and a subsequent empty cell to acquire synchronization. When synchronized, the LM accepts data from each CLA that has information for the system; the LM then outputs this information to the input loop, in a line frame. At each frame boundary, the LM examines the input loop for an empty cell. If the empty dell is detected, the LM places the next CLA frame on the loop. If an empty cell is not detected, the LM drops synchronization.

All CLAs plug into a common bus and control-line structure. Each CLA has a unique address and may be plugged into any CLA slot. Each CLA can inform the LM, via one of 32 lines, that it has information for the system. The LM can inform each CLA, via one of 32 control lines, that it can place information on the CLA bus in response to strobe signals. When a CLA has been selected, the LM will accept information from that CLA until either an information-end signal from that CLA is received, or 16 cells have been processed. When one of the above occurs, the LM deselects that CLA, and selects another CLA. When all CLAs requesting access to the loop have been serviced, the LM drops synchronization.

INPUT FUNCTIONAL SEQUENCE

The following is the sequence of functions for the input section of the LM:

1. The input loop data stream is examined at each bit time for a 24-bit code consisting of a loop end cell followed by an empty cell. Upon detection of this bit pattern, the LM is cell-synchronized to the data stream. The loop end cell is removed from the data stream and one empty cell replaces the loop end.

2. When synchronized, further storage of information-available signals from the CLAs is inhibited, and only those CLAs with stored-information-available signals can be selected. These CLAs are serviced on a priority basis determined by their slot position in the multiplexer card cage assembly. CLAs positioned closest to the primary LM circuit card have the highest priority. Frames placed on the loop by the LM are continuous with no empty or null cells between frames.

3. The selected CLA inhibits changes in its input information storage registers during selection. Provision is made in the CLA to capture critical status during selection.

4. Information is presented to the LM by the CLA in 11-bit bytes. These are identical to bits 1 thru 11 in the loop cell. Address information is presented first, followed by up to 15 other bytes of information. Null cells may be placed among these bytes and are included in the byte count.

5. The LM replaces each cell received on the loop with the information received from the CLAs.

When the CLA informs the LM that the last byte has been presented, the LM concludes the frame with a cyclic redundancy checksum (CRC) character.

6. The LM examines the cell received on the input loop prior to the CRC output to determine the presence or absence of an empty cell.

   a. Presence of an empty cell causes the LM to select the highest priority CLA not yet serviced. This process continues until all CLAs with stored requests have been serviced once.

   b. Absence of an empty cell causes the LM to halt CLA selection, and output the CRC cell of the last frame with a contiguous loop end cell.

7. When all stored requests have been serviced, the LM places a loop end cell and an empty cell on the input loop, and then drops synchronization.

INPUT ERROR PROTOCOLS

The LM utilizes the following four protocols to ensure the integrity of data on the input loop:

1. Cyclic redundancy checksum
2. Restart loop cell
3. Automatic secondary LM selection
4. CLA overrun

Cyclic Redundancy Checksum

The input section generates a CRC character for each frame placed on the loop. Accumulation of a CRC character begins with the first bit of the line frame, and ends with the fourth bit of the CRC cell in the line frame. The LM generates the CRC character by treating the serial information as a long binary number and dividing that number by a generator binary code, using modulus 2 arithmetic. The generator is 111000011, $X^8+X^7+X^6+X+1$ (in polynomial notation).

Restart Loop Cell

The MLIA notifies the LM of an input batch received in error via a restart loop cell. The restart loop cell is placed on the loop immediately following detection of the bad batch. The LM detects the restart loop cell, and notifies the CLA which last placed information on the loop, of the error.

Automatic Secondary Loop Multiplexer Selection

The multiplexer card cage assembly can contain two identical LM circuit cards. Each LM card can be connected to a separate loop. The software can disconnect the primary LM from the CLA bus, and activate the secondary LM, when a loop failure involving the primary LM has occurred.

CLA Overrun

If a CLA places more than 16 bytes of information on the bus, the LM will assume an error has occurred and will disconnect that CLA. The CRC will be added to the data stream as in a normal frame termination.

OUTPUT SECTION

The output section of the LM receives contiguous loop cells from the preceding LM or from the MLIA. The output section always passes all loop cells received to the next LM or to the MLIA. The clock signal is reconstructed to specification when passed sequentially to the next element in the system. The LM utilizes empty cells to synchronize itself to the data stream. When synchronized, the LM looks for frame boundaries, and passes loop cells within the frame to the CLAs. The LM checks the CRC character received with each frame.

When the LM has accepted the address of a frame. it presents this address to all CLAs. The CLA with the corresponding address then connects itself to the output bus. The selected CLA accepts the information directed to it until disconnected by the LM. If a CRC error is detected by the LM, it is reported to the CLA prior to termination.

OUTPUT FUNCTIONAL SEQUENCE

The following is the sequence of functions for the output section of the LM:

1. The LM examines the output loop data stream each bit time for the presence of an empty cell bit pattern. Upon empty cell detection the LM is cell-synchronized and begins a search for an address code in the identification field of each loop cell.

2. When the LM locates an address code, it presents the address with a select signal to all CLAs in the multiplexer card cage assembly. The CLA with the same address as that presented connects itself to the bus, and is prepared to accept 11-bit bytes from the LM. These bytes are identical to those contained in the loop cells that are part of the frame intended for the selected CLA.

3. When the LM receives an identification code indicating the presence of a CRC character, it halts byte transfer to the CLA bus. The CRC character is compared to that accumulated over all preceding bits of the received frame, and the results reported to the CLA.

4. After CRC verification, the LM again searches for address codes in the received loop cells.

OUTPUT ERROR PROTOCOLS

The LM utilizes the following two protocols to ensure the integrity of data on the output loop:

1. Cyclic redundancy checksum
2. CLA overrun.

Cyclic Redundancy Checksum

The output section accumulates a CRC character for every line frame received on the output loop. Accumulation begins with the first bit of the line frame and ends with the fourth bit of the CRC cell. The CRC character is generated by treating the serial information as a long binary number and dividing that number by a generator binary code, using modulus 2 arithmetic. The generator is 111000011 or $X^8+X^7+X^6+X+1$ (in polynomial notation).

CLA Overrun

If more than 16 cells are received by the LM in a given frame, the LM will report an error to the selected CLA and disconnect that CLA.

Communications Line Adapter

The function of the communications line adapter (CLA) is to provide the interface between the LM and a terminal with or without a modem. On input, the CLA serves as a serial-to-parallel converter assembling the serial data at the signalling rate of the terminal, and transferring the data to the LM in an 8-bit byte. On output, the CLA functions as a parallel-to-serial converter receiving the data characters in bytes of eight bits from the LM and outputting them serially at the signalling rate of the terminal.

In order to minimize the number of CLA types required, the CLA hardware is designed to accommodate most circuit characteristics under software/firmware control. Each circuit's individual characteristics are handled, for the most part, by associated software which detects the specifics and sets parameter registers within a particular CLA to handle them. Soft-ware-selected elements include: circuit speed, code set, mode of operation and, for synchronous circuits — the synchronization pattern(s), and for asynchronous circuits — different input and output speeds, parity detect and generation, and number of stop bits per character. This software detection is possible by means of an algorithm associated with the arrival of the first few characters of a data transmission.

The only remaining circuit variables are whether the circuit is synchronous or asynchronous, and if synchronous, the signal level standard to which the circuit interfaces. The terms synchronous and asynchronous refer to the way in which the data is transmitted: synchronously with a clock, or without reference to a clock (but at a fixed rate and with synchronization elements appended).

A number of CLA types, which have differing functional and/or electrical interface characteristics, are presently available. In addition, the CLAs constitute a product line which is under continuing development. Therefore, it is recommended that the user refer to the hardware reference and maintenance manual(s) for the functional descriptions of the specific CLA type(s) selected for his system (see Preface).

CONTROLS AND INDICATORS

LOOP MULTIPLEXER CIRCUIT CARD

A narrow vertical control panel is attached to the front-facing edge of each LM printed circuit card (refer to figure 2-2). This panel contains a power switch, four LED indicators, and a circuit legend as described below:

1. PWR Switch. This two-position toggle switch is used to control electrical power to the LM printed circuit card only.

2. IN LOOP CLK Indicator. When lit, this LED indicates that the input loop clock signal is receiving bit clocking from the multiplex/loop interface adapter (MLIA) or preceding LM.

3. IN LOOP DATA Indicator. When lit, this LED indicates that the input loop is receiving data cells from the MLIA or preceding LM.

4. OUT LOOP CLK Indicator. When lit, this LED indicates that the output loop clock signal is receiving bit clocking from the MLIA or preceding LM.

5. OUT LOOP DATA Indicator. When lit, this LED indicates that the output loop is receiving data cells from the MLIA or preceding LM.

6. Circuit Legend. This area is provided to permit each user to identify the circuits connected to the CLAs by insertion of small labels. There are no standard markings; customer may use as necessary to meet his particular needs.

NOTE

The four LED indicators are of particular use during maintenance activities should some form of loop problem occur, since they provide visual assurance of loop continuity.

COMMUNICATIONS LINE ADAPTER CIRCUIT CARD

Figure 2-3 shows the narrow vertical control panel on a typical asynchronous communicattons line adapter (ACLA) circuit card. For information on ACLA controls and indicators refer to document No. 74700900.

MULTIPLEX LOOP INTERFACE ADAPTER CIRCUIT CARDS

All three of the circuit cards which comprise the multiplex loop interface adapter (MLIA) contain LED indicators.

MLIA-Processor Interface Circuit Card

The MLIA-processor interface circuit card is illustrated in figure 2-4. This circuit card contains a single LED indicator which indicates the presence of +5V electrical power (when lit).

MLIA-Input Loop Interface Circuit Card

The MLIA-input loop interface circuit card is illustrated in figure 2-5. This circuit card contains a single LED indicator which indicates the presence of +5V electrical power (when lit).

MLIA-Output Loop Interface Circuit Card

The MLIA-output loop interface circuit card is illustrated in figure 2-6. This circuit card contains the following five LED indicators (the numbered items below correspond to the numbered callouts in figure 2-6):

1 MLIA RUNNING. When lit, this LED indicates that the MLIA is not reset.

2. OUTPUT ON. When lit, this LED indicates the presence of data and clock signals on the output loop.

3. INPUT ON. When lit, this LED indicates the presence of data and clock signals on the input loop.

4. INPUT BUSY. When lit, this LED indicates either the presence of loop batches on the input loop, or the absence of a valid restart loop end following an error.

5. POWER. When lit, this LED indicates the presence of +5V electrical power.

PROGRAMMING INFORMATION

LOOP MULTIPLEXER

The loop multiplexer (LM) and associated communications line adapters (CLAs) are under complete control of the multiplex loop interface adapter (MLIA). The format of the loop cells utilized to communicate between the MLIA and the LM is shown in figure 2-7.

Loop Cell Arrangement

The loop cells are arranged in line frames on both the input and output loop. Each frame must start with an address loop cell and end with a CRC loop cell. Each

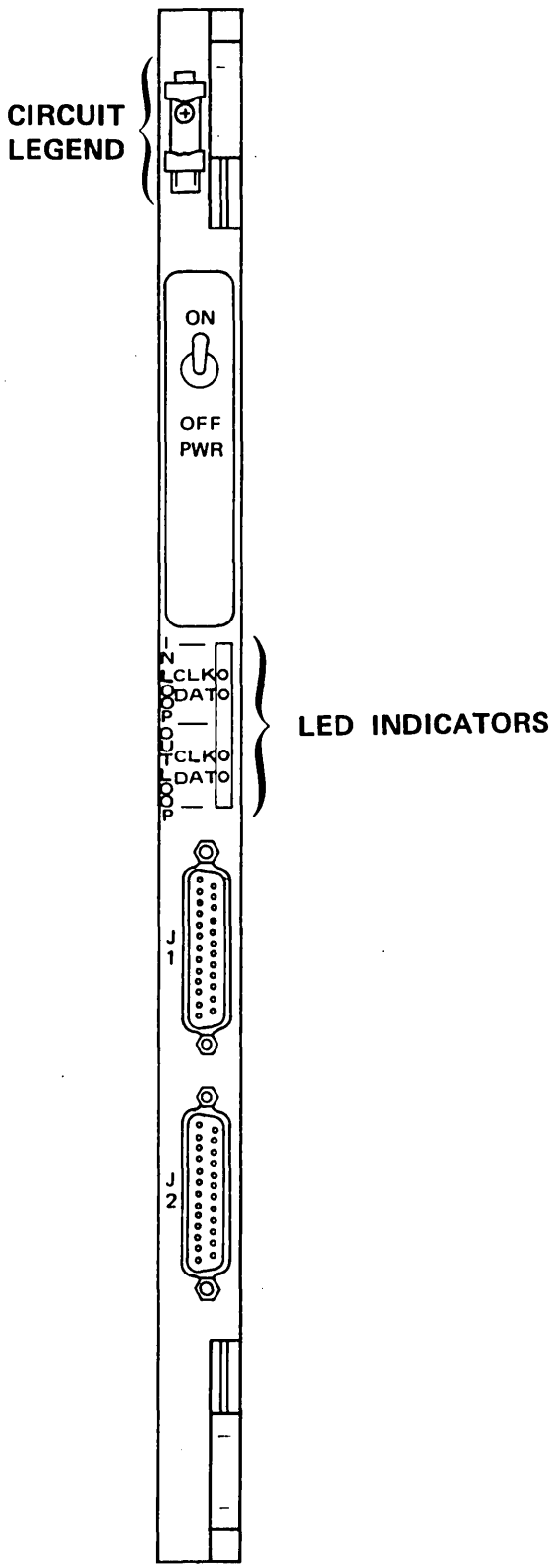


Figure 2-2. Loop Multiplexer Circuit Card PWR ON/OFF Switch Location

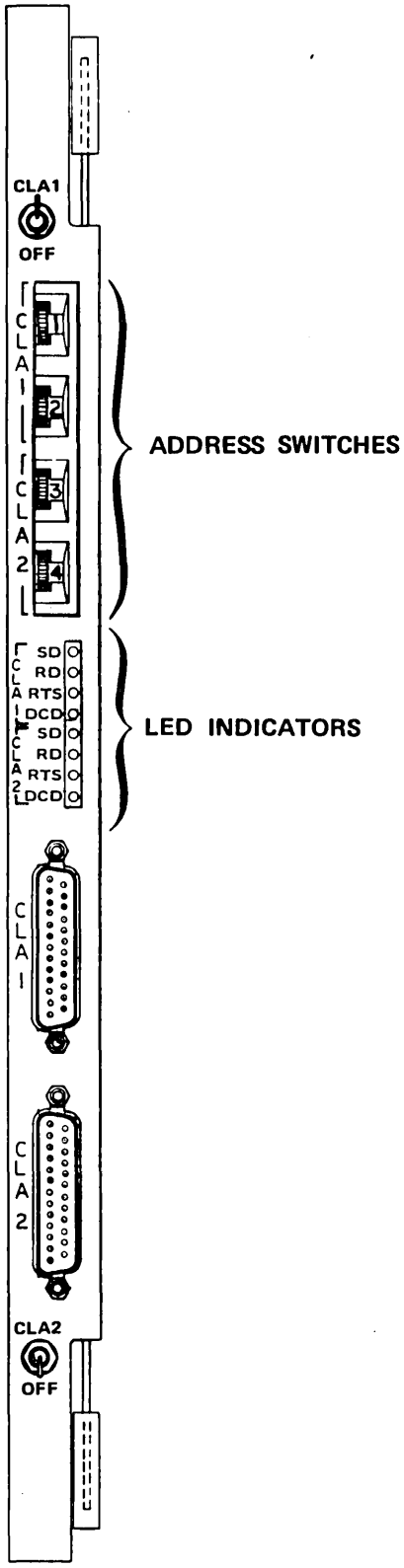


Figure 2-3. CLA Circuit Card Switch Locations

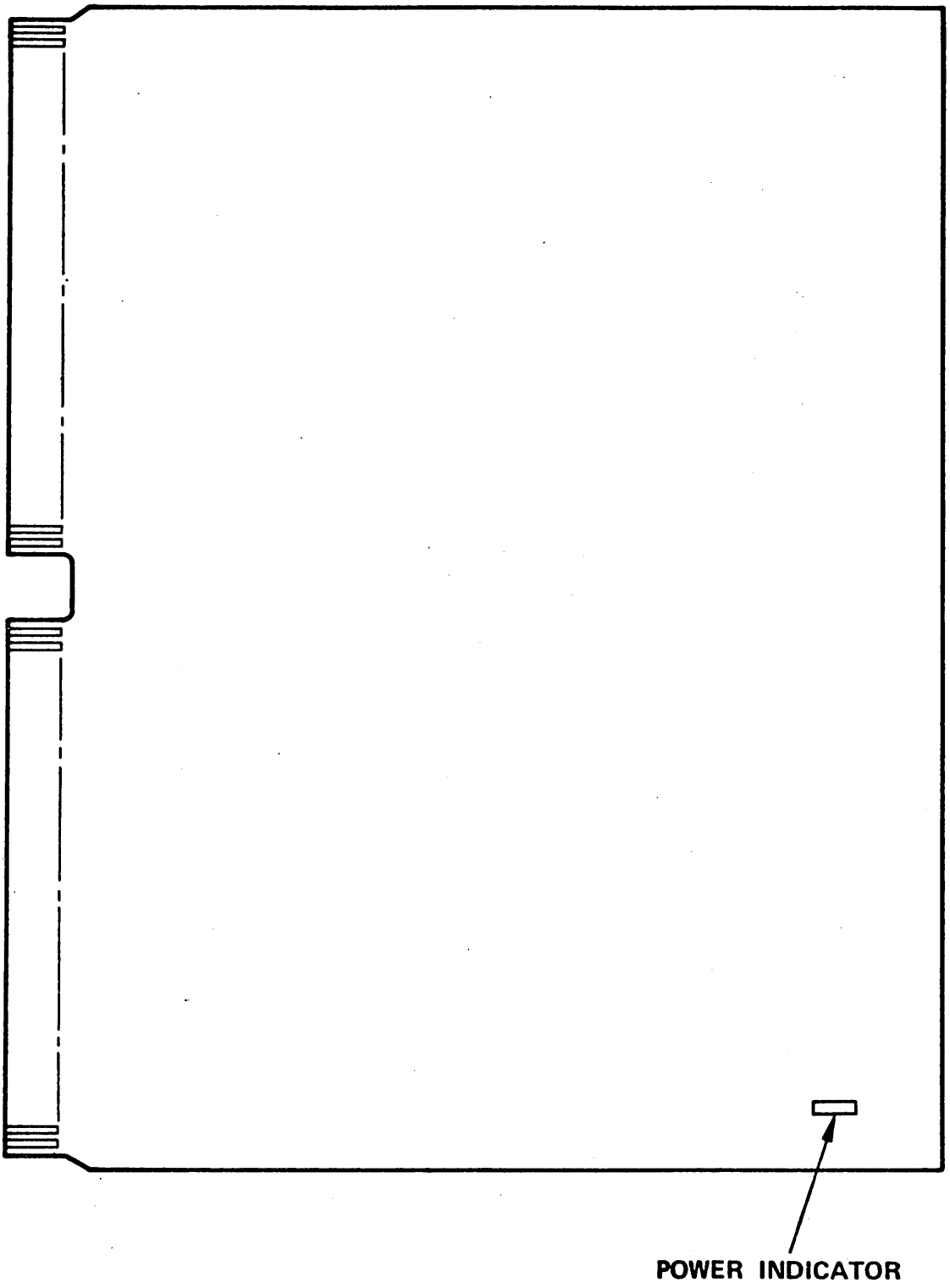


Figure 2-4. MLIA, Processor Interface Circuit Card Indicator

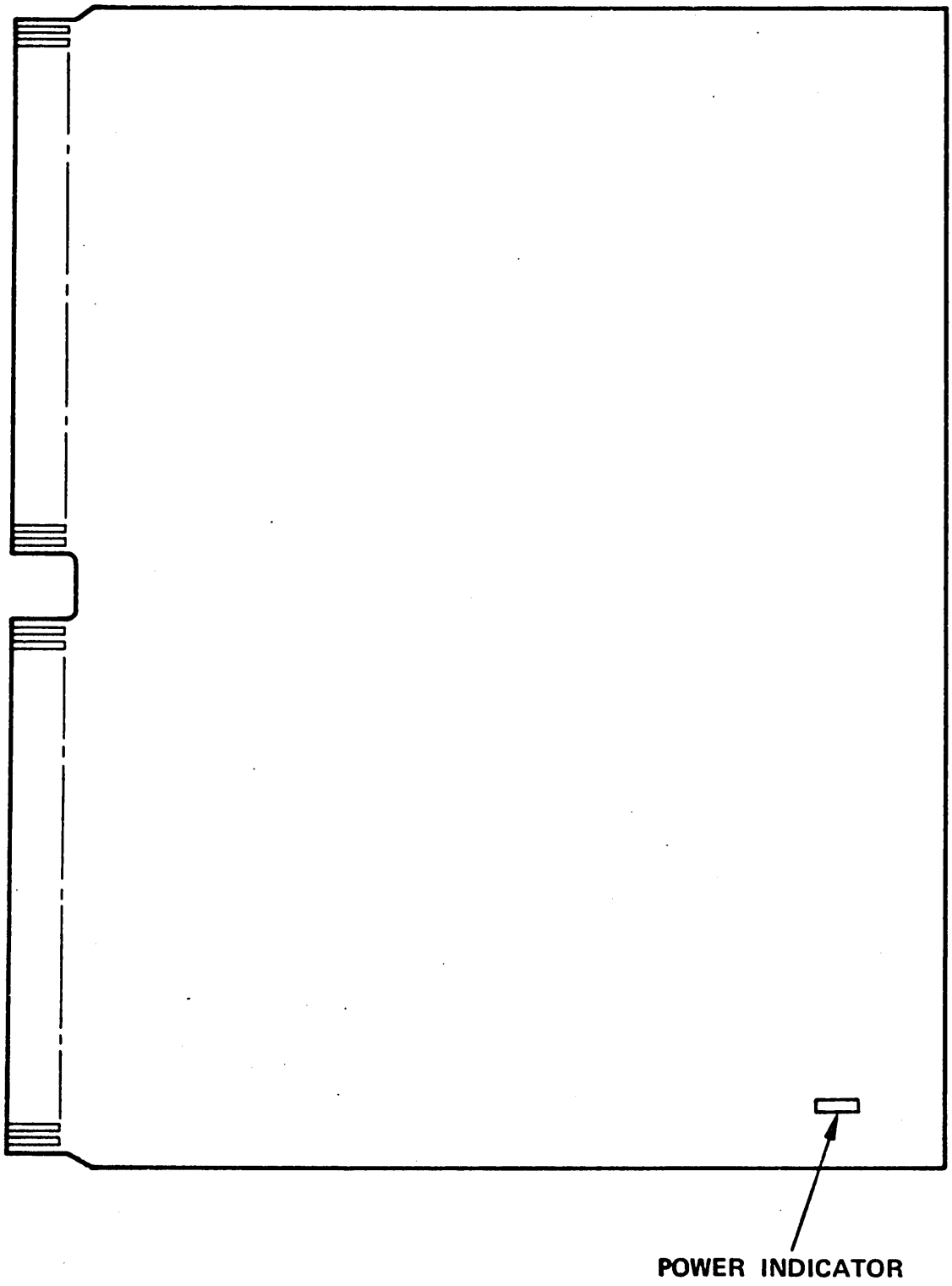


Figure 2-5. MLIA, Input Loop Interface Circuit Card Indicator

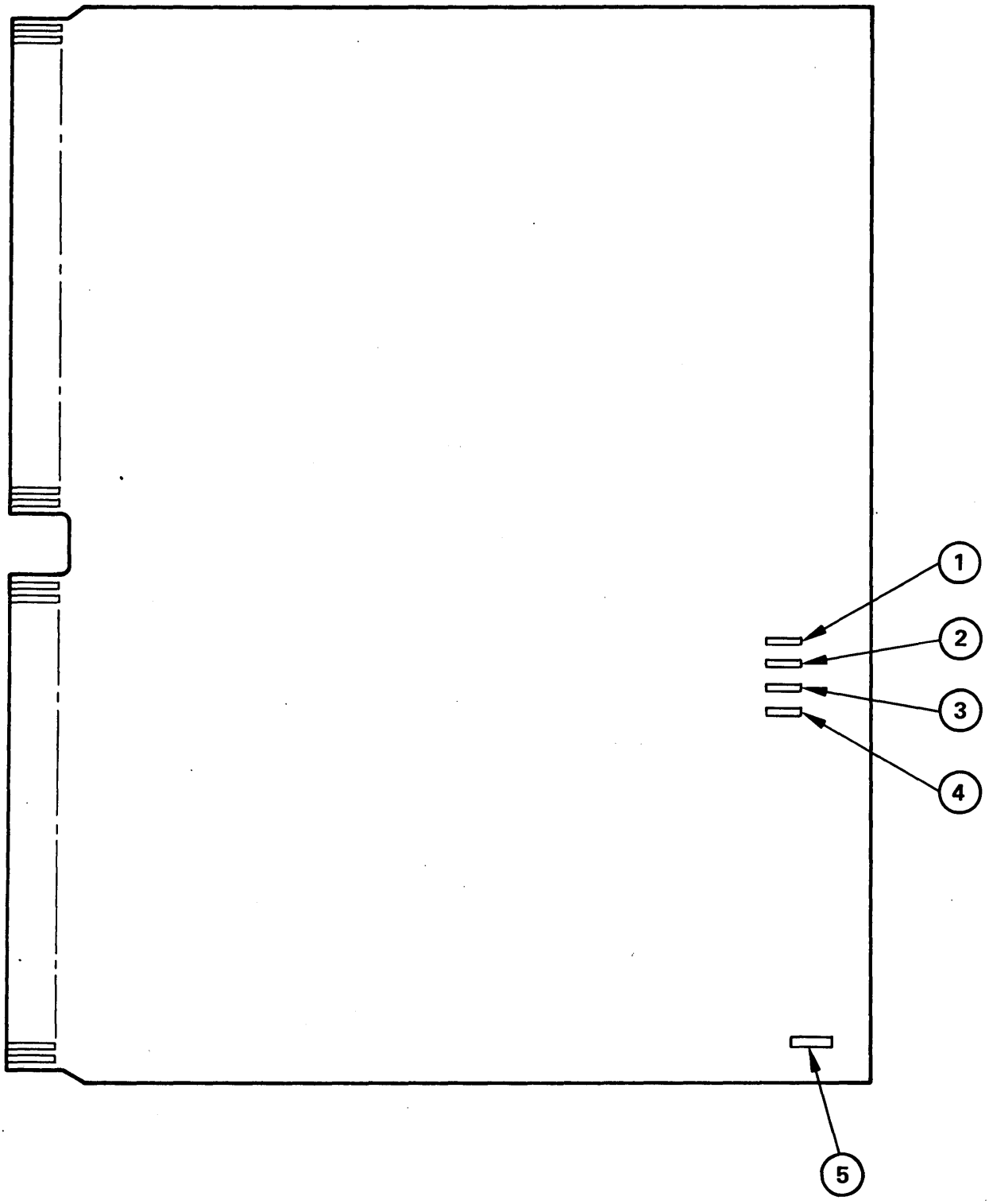


Figure 2-6. MLIA, Output Loop Interface Circuit Card Indicators

frame must not contain more than 16 loop cells, including address and CRC cells. Empty cells must not appear within line frames, but may appear between frames. Null cells may appear within or between frames.

Loop Batches

Line frames are always grouped in loop batches. Each loop batch must be followed by a loop end cell. Loop end cells to be utilized on the input loop, for response by the loop multiplexer, must be followed immediately by at least one empty cell. A loop batch may contain any number of line frames but is limited by the number of empties. A typical loop batch is shown in figure 2-8.

CLA

Each CLA, connected to LMs which interface a given loop, must have an address different from the address of any other CLA in that loop. If the LM is connected to two loops for redundant operation, each CLA in both loops must have an address different from the address of any other CLA in both loops.

Loop Multiplexer

The LM and all CLAs are reset and cleared when clock signals are not received for 20 microseconds on both input and output loops. The input section of the LM is reset and cleared when the clock is not received on the input loop for 20 microseconds; and the output section of the LM is reset and cleared when the clock is not received for 20 microseconds on the output loop. When two LM cards are present in a redundant configuration, the CLAs will be reset when the clock is absent for 20 microseconds on both loops. With a bit rate of 20 mHz, generation of approximately 34 loop cells requires a period in excess of 20 microseconds.

Input Loop

1. When the MLIA can accept data/supervision from the CLAs in the loop, it initiates an input loop batch by generating a loop end followed by a block of null cells (to mark the end of the available loop cells). If the MLIA can accept more than one frame, it places several empty cells on the loop. If it cannot accept more data supervision from the loop, the adapter halts generation of the loop batches. The number of empties and nulls to be sent are programmable parameters.
2. When the LM receives the loop end and empty cell combination and has information for the loop, it deletes the loop end and replaces it with an empty cell. It will immediately place contiguous line frames on the loop in cell synchronization with the received empties. The frames will have a structure similar to those illustrated in figure 2-8. If there are no CLAs with information for the loop, the LM will not disturb the passing loop cells.
3. If a null cell is encountered by the LM immediately prior to placement of a CRC character on the loop, it will place a loop end between the CRC cell and the null cell.
4. When all CLAs requesting access have placed one frame on the loop, the LM replaces the next cell received with a loop end cell.
5. Information regarding the cells within each line frame, relating to each CLA, is contained within the manual for that CLA type (see Preface).

Input Loop Restart

1. When the MLIA wishes to inform the CLAs of an input loop batch error, it places a restart loop end followed by an empty cell between each loop batch. The frames will always have the internal structure of figure 2-8.
2. The LM passes all output loop cells to the next LM or to the MLIA with a delay not to exceed two bit times.
3. Information regarding the cells within each loop frame, relating to each CLA, is contained within the manual for that CLA type (see Preface).

Redundant Operation

1. When two loops are to service a group of CLAs in a given LM cage, the LM card position and the presence or absence of a tag bit in the loop end determines which loop communicates with the CLAs.
2. An LM card in the primary card slot will process a loop end-empty cell combination if the secondary LM flag (B4) = 0.

CELL MARKER
CELL IDENTIFICATION
CELL INFORMATION

TYPE	FORMAT NUMBER	M	ID			INFORMATION								CELL DESIGNATION
		B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	
LOOP MANAGEMENT FORMAT	0	1	0	0	0	0	0	0	0	0	0	0	0	EMPTY
	0	1	0	0	0	1	0	1	0	1	0	1	0	NULL
	1	1	0	0	1	F3	F2	1	1	1	0	0	0	LOOP END
	1	1	0	0	1	F3	F2	0	0	0	1	1	1	LOOP END RESTART
RESERVED FORMATS	2	1	0	1	0	R	R	R	R	R	R	R	R	UNDEFINED
	3	1	0	1	1	R	R	R	R	R	R	R	R	UNDEFINED
LOOP USAGE FORMATS	6/7	1	1	1	F1	A1	A2	A3	A4	A5	A6	A7	A8	CLA ADDRESS
	4	1	1	0	0	D1	D2	D3	D4	D5	D6	D7	D8	DATA
	5	1	1	0	1	S1	S2	S3	S4	S5	S6	S7	S8	SUPERVISION
	6	1	1	1	0	C1	C2	C3	C4	C5	C6	C7	C8	CRC

INPUT LOOP CODING

F1 = 0 NO OUTPUT DATA DEMAND
F1 = 1 OUTPUT DATA DEMAND
F2 = X UNDEFINED
F3 = 0 PRIMARY DECODES LOOP END; SECONDARY IGNORES LOOP END
F3 = 1 PRIMARY IGNORES LOOP END; SECONDARY DECODES LOOP END

OUTPUT LOOP CODING

F1 = 1
F2 = X UNDEFINED
F3 = X UNDEFINED

CODING ON BOTH LOOPS

A1 TO A8 = BINARY CODE OF CLA ADDRESS; A1 IS MOST SIGNIFICANT BIT
D = DATA
C = CYCLIC REDUNDANCY CHECK CHARACTER (CRC), C1 IS MOST SIGNIFICANT BIT
R = X RESERVED AND UNDEFINED

Figure 2-7. Format of Loop Cells

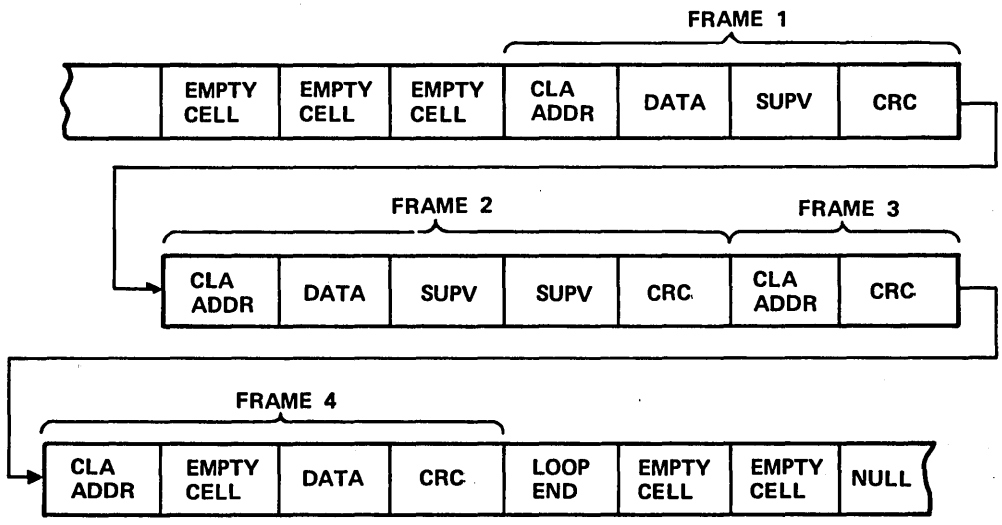


Figure 2-8. Input Loop Batch and Line Frame Structure

3. A LM card in the secondary card slot will process loop end-empty cell combinations if the secondary LM flag (B4) = 1.

4. The MLIA, in conjunction with system hardware and software, will prevent both loops from accessing the CLAs in a single LM cage at the same time.

5. The input section of a given LM card determines the connection of the output section to the CLA bus. If the input section is active in a redundant system, the output section will also be active. If the input section is disconnected from the CLA bus, the output section will also be disconnected from the CLA bus.

LOOP MULTIPLEXER TO CLA LOGIC SIGNAL DEFINITIONS (INPUT)

1. IAV1 to IAV32 — Input Available

   A single line from each CLA to the LM indicating:

   Logic 1 = CLA has input information

   Logic 0 = CLA has no input information

2. INS1 to INS32 — Input Select

   A single line from the LM to each CLA indicating:

   Logic 1 = CLA selected

   Logic 0 = CLA not selected

3. IF1, IF2, IF3 — Input Format

   Three bused lines from the CLAs to the LM identifying the contents of the information bits. Only the selected CLA has access to these lines. The line codes are as indicated below.

IF1	IF2	IF3	Definition
0	0	0	Not used
0	0	1	Not used
0	1	0	Spare
0	1	1	Spare
1	0	0	Data present
1	0	1	Supervision present
1	1	0	Address without output data demand
1	1	1	Address with output data demand

4. II1 to II 8 — Information Input

   Eight bused signals from the CLAs to the LM containing information characters. Only the selected CLA has access to the bus. Each bit is coded as below.

   Logic 1 = Information bit is 1

   Logic 0 = Information bit is 0

5. IEN — Input End

   A single bused signal from the CLAs to the LM indicating:

   Logic 1 = Selected CLA is presenting the last word to LM

   Logic 0 = Selected CLA is not presenting the last word to LM

6. IST — Input Strobe

   A single bused signal from the LM to the CLAs. The LM controls the information flow between the selected CLA and the LM via this signal. The LM has accepted the bused information on the logic "1" to logic "0" transition of the input strobe.

7. IER — Input Error

   A single bused signal from the LM to the CLAs. When the LM is informed of an input batch error, this line will be set to a logic "1". Each CLA that used the last batch will be selected and will receive a strobe signal. The CLAs will not place information on the bus, when selected, with IER at a logic "1".

8. MCL — Master Clear

   A single bused signal from the LM to all CLAs. When clock signals have not been received on the input and output loops for 20 microseconds, this line will be set to a logic "1". At all other times it will be set to a logic "0".

LOOP MULTIPLEXER TO CLA LOGIC SIGNAL DEFINITIONS (OUTPUT)

All output section signals are bused and directed from the LM to the CLAs.

1. OSL — Output Select

   A logic "1" on this line informs all CLAs that a CLA address is presented on the information bus for examination. A logic "0" indicates CLA selection is not in progress.

2. OSC — Output Select Clear

   A logic "1" on this line indicates that the LM has no further information for the selected CLA. A logic "0" on this line indicates that selection and information transfer may continue.

3. OF1, OF2, OF3 — Output Format

   These three signals identify the contents of the information bits. The line codes are as indicated below.

OF1	OF2	OF3	Definition
0	0	0	Not used
0	0	1	Not used
0	1	0	Spare
0	1	1	Spare
1	0	0	Data
1	0	1	Supervision
1	1	0	CRC
1	1	1	Address

4. IO1 to IO8 — Information Output

   These eight lines contain the data, commands, or other information required by the CLAs. A logic "1" on a line indicates the information bit is "1". A logic "0" on a line indicates the information bit is "0".

5. OST — Output Strobe

   The LM controls the signal flow between the selected CLA and the LM via this signal. The CLA has accepted information from the bus on the logic "1" to logic "0" transition.

6. OER — Output Error

   When a CRC error is detected by the LM, this line is set to a logic "1" prior to CLA deselection. When no CRC error is detected, this line remains at a logic "0".

MULTIPLEX LOOP INTERFACE ADAPTER

The MLIA maintains a logical interface with both input and output MUX loops, a logical interface with both IDC and DMA channels of the CP, plus the physical interface of each of the MLIA cards to the CP and the other MLIA cards.

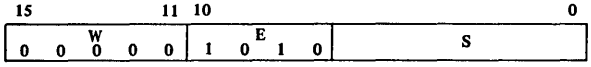
CHANNEL ADDRESSING (Q REGISTER)

The MLIA is addressed on the CP in M05 (NCR) address format.

Since there are no devices, station, or other subdivisions within theMLIA, six bits are available to distinguish between commands uniquely. Thus the contents of the address ("Q") register alone define the operation. The data ("A") register is only required when parameters are being transferred. The need to load only one register instead of two results in greater efficiency and permits greater throughput with no loss of versatility (figure 2-9).

CDC 1700-AQ CHANNEL

CDC 1700 addressing divides the addressing into three major fields, as shown below.



Since the MLIA is not operated on the buffer data channel, the W parameter is always zero. There is only one MLIA in the CP and it is assigned a fixed address determined by CP wiring. Tentatively, the equipment address to "A" has been assigned.

AQ CHANNEL OUTPUT OPERATIONS

In the following sections, reference is made to A and Q registers.

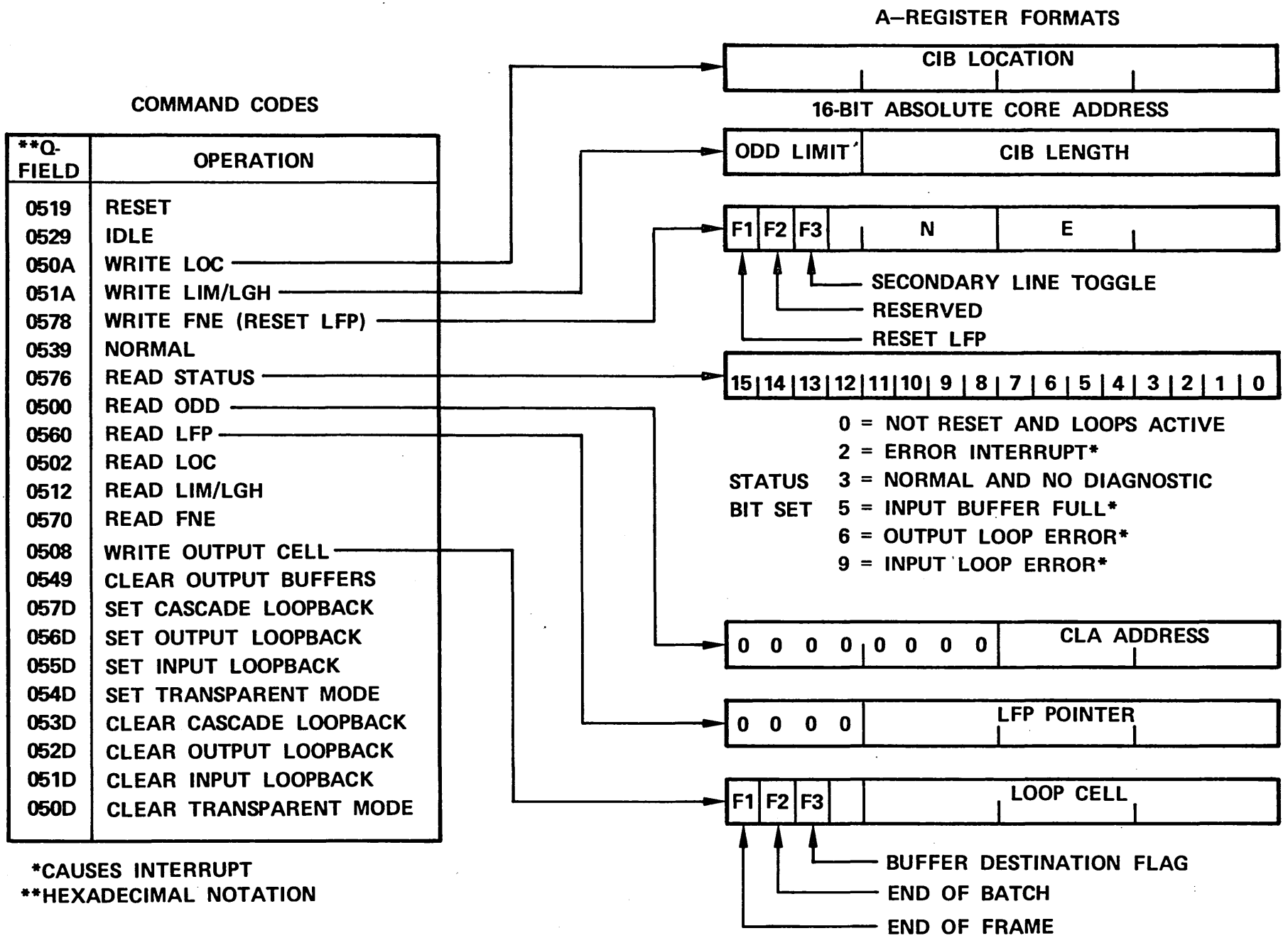


Figure 2-9. MLIA Commands

LOOP CELL FORMAT

	Format	11	10	9	8	7	6	5	4	3	2	1	0		
Loop Mgmt.	0	1	0	0	0	0	0	0	0	0	0	0	0		Empty
	0	1	0	0	0	1	0	1	0	1	0	1	0	*	Null
	1	1	0	0	1	P3	P2	1	1	1	0	0	0		Loop End
	1	1	0	0	1	P3	P2	0	0	0	1	1	1	*	Loop End Restart
Reserved	2	1	0	1	0										
	3	1	0	1	1										
Loop Usage	6/7	1	1	1	P1	Address									CLA Address
	4	1	1	0	0	Data									Data
	5	1	1	0	1	Supervision									Supervision
	6	1	1	1	0	CRC									CRC ($X^8 + X^7 + X^6 + X + 1$)

Cell I/D — Cell Information

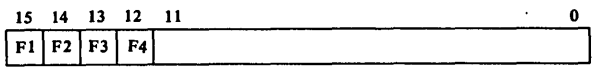
Cell Marker

P1 = Output Data Demand
P2 = ---
P3 = Input from Secondary Lines (redundant configuration)
* = Not currently used in output stream

Output Command (Q = 0508)

Upon receive of this code, the contents of the 16 output data lines (A register) are transferred to the MLIA and stored in an output data holding buffer. Additional words are similarly transferred and stored. Whenever a word is transferred in where the end-of-loop-batch flag is set, the buffer empties its contents to form a loop batch, a CRC is added, and line frames are transferred on to the LMs. The process continues until a word in the output buffer is reached containing both end-of-loop-batch and end-of-line-frame. This terminates the output operation.

OUTPUT DATA (08_{16})



F1 = End of Line Frame (EOF)
F2 = End of Loop Batch (EOB)
F3 = ---
F4 = ---

RESET COMMAND (Mode), (Q = 0519)

Upon receipt of this command, all operations are terminated, all buffers are reset, stored status is set to 0268 and interrupts are reset, all timing is reset, and all parameters are set to zero. Loop clock and data lines are inactive. Sync lock is lost. All diagnostic commands are reset.

IDLE COMMAND (Mode), (Q = 0529)

Upon receipt of this command, all output operations resume as in the NORMAL mode, but input loop batches are not sent. Continuous empty cells will be sent, there will be no loop ends or nulls. Note that immediately following a change from RESET mode to IDLE mode, restart loop end may or may not be sent depending on random timing factors.

All error sensors are enabled. Note that upon entering this mode, interrupt status will indicate that the unit was out of sync and now is (or soon will be) back in sync.

Input loop batch E and N parameter, all flags, input buffer location and length, etc., must all be properly initialized prior to entering NORMAL mode since operation starts immediately.

In idle mode the unit can output if desired, but all input is inhibited. This mode is used following a RESET command in order to load parameters; another use is to stop all input (risking CLA overrun) if the processor circular input buffer approaches capacity. (The E parameter controls the number of empty cells sent in each loop batch.)

NORMAL (Mode), (Q = 0539)

Upon receipt of this command, the unit begins performing both input and output functions. As soon as one input loop batch returns, another is initiated. Output data is transmitted upon CP command (as in the IDLE mode). The MLIA remains in sync when switched from IDLE to NORMAL or from NORMAL to IDLE mode.

NOTE

Use extreme caution in issuring commands and/or parameters to this unit while running in NORMAL mode since the new changes are implemented immediately and the resulting state may not be a desirable condition.

Clear Output Buffer, (Q = 0549)

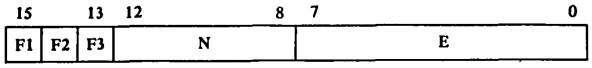
Clears both output buffers. The output data buffers read out only upon receipt of an end-of-loop-batch flag, and prior processing may inadvertently leave residuals in the FIFOs. This command will initialize the buffer to the cleared condition prior to beginning a new operation. (Note that this command need not be sent if the RESET command was just used. This command should not be issued while the MLIA is still outputting in response to the EOB bit.)

Write FNE Parameters, (Q = 0578)

Upon receipt of this code, the contents of the sixteen output data lines (A register) are sampled and the resulting word transferred to the loop parameter register.

Data format is shown below. F1 is an embedded command (rather than a parameter per se) and results in the pointer for writing data into the CP circular input buffer (CIB) being set to zero (i.e., beginning of buffer). The remaining two flags are transmitted in the loop end cell.

SET LOOP PARAMETERS (78_{16})



F1 = Reset LFP (last frame position) pointer (immediate command)
F2 = - (part of loop end cell)
F3 = Input from secondary lines (part loop end cell)
N = Number of null cells generated for input loop batch
E = Number of empty cells generated for input loop batch

The F1 bit in the A field momentarily resets both the next word position pointer (NWP) and the last frame position pointer (LFP). The act of issuing the command with F1 set is what generates the reset, not the presence of the F1 bit itself. Hence, the F1 bit remains set but its effect is only momentary.

Presently, F2 is a spare flag. F3, however, is the controlling flag in dual systems. In this mode there are two MLIA units, each driven by a separate CP. Thus each LM cage connects to two sets of loops, each one through a separate LM card. In normal operation (flag F3 not set), each loop services half the traffic (its "primary" lines). Should either loop become inoperative for any reason, the other loop then alternately services the primary and secondary lines when loop end cell flag F3 is set.

Although flag F3 is set and stored, only alternate loop cells have the corresponding bit set. This is necessary to service high priority lines in the same sequence as the original service. This assures proper handling of high speed lines on both loops.

Care must be exercised in establishing values for N and E since too conservative an approach could slow down input loop response time unnecessarily. Generation of input loop batches will be suspended any time either the ODD buffer or the input FIFO cannot accommodate the worst case data pattern. Worst case for the ODD buffer occurs when only ODDs are received back (i.e., a CLA address containing an ODD, followed by the CRC). Worst case for the input FIFO occurs when a maximum length line frame is begun by the last empty cell in the loop batch (the last empty prior to the string of nulls). Specific ground rules are as follows:

- The N parameter does not specify the exact number of nulls in the generated input loop batch. Rather, the number of nulls will be two greater than the value of the N parameter. Thus, the MLIA will always generate at least two nulls, even if N is set to zero.

- If a loop end cell is received by MLIA on the input loop while the input loop batch is still

being generated, the generation sequence will be terminated and a new input loop batch will be started immediately. Hence, the number of nulls and empties actually present on the input loop can be considerably less than the settings of the N and E parameters if no cells were inserted by a connected LM.

- The MLIA tests only the main FIFO for worst-case data pattern; it does not test the ODD FIFO. The only space-available test on the ODD FIFO is controlled by the ODD limit parameter or programmed by the Write LIM/LGH command (Q=051) (A=051A). Hence, the maximum permissible value of the E parameter is determined by the size of the ODD FIFO.

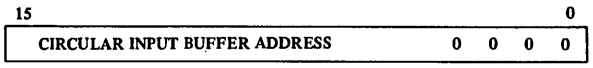
NOTE

This operation is also affected by the ODD threshold parameter.

Set Buffer Location (Q = 050A)

Upon receipt of this code, the contents of the 16 data lines (A register) are sampled and the resulting word transferred to the CIB location register. The lower four bits are not presently used.

SET BUFFER LOCATION ($0A_{16}$)



Contents of the buffer location register determine the beginning of the area in CP memory into which the input FIFO is unloaded. Storage is sequential, continuing until the end of buffer is reached (determined by the buffer length parameter, see below). At that time, the internal working pointer is reset to zero and writing resumes at the beginning of the buffer. Firmware must assure that unused information is not overwritten and thus lost.

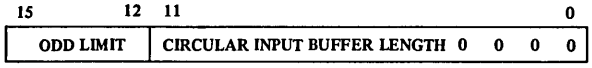
Set Buffer Length/ODD Limit (Q = 051A)

Upon receipt of this code, the contents of the 16 output data lines (A register) are sampled. The middle eight bits are transferred to the CIB length register; the lower four bits are not used at this time.

The length parameter is a full 12-bit field specifying the main memory address of the final word of the CIB. The address is relative to the location parameter programmed by the write location command (Q=050A).

Thus, the absolute main memory address of the last word in the CIB will be the sum of the length and location parameters, and the total number of words spanned by the buffer will be one greater than the value of the length parameter. (See below for use of this parameter.)

SET BUFFER LENGTH/ODD LIMIT ($1A_{16}$)



The upper four bits are transferred to the ODD threshold register. Whenever the number of entries in the ODD FIFO register exceeds this threshold value, initiation of input loop batches is suspended until the number of stored ODDs again goes below this threshold.

Set Transparent Mode (Q = 054D)

Upon receipt of this diagnostic mode command, normal editing functions performed on input loop batches received from the loop are inhibited. Thus all bits received are forwarded to the CP for subsequent analysis.

Several cautions should be noted in conjunction with this command. End of line frame and end of loop batch flags are not set. CRC errors or sequence errors are not tested (although now the CRC character is included). Normally the characters on the line outside loop batches are not sent, although this is dependent upon the ability of the MLIA to detect the loop end character. Should this not be recognized for some reason, characters would continue to fill the buffer until the loop end timeout was reached. Thus the buffer may be overrun.

Clear Transparent Mode (Q = 050D)

Upon receipt of this diagnostic mode command, the effect of the above ($4D_{16}$) command is cancelled.

Set Input Loopback (Q = 055D)

Upon receipt of this diagnostic mode command, input loop signals are shunted across an internal path rather than going through the normal external loop. Specifically, the input to the loop transmitter is connected as the output of the loop receiver (in lieu of the normal connections). Thus no traffic (data or clock) appears on the external loop.

This command can be used alone or in conjunction with the other diagnostic commands.

Clear Input Loopback (Q = 051D)

Upon receipt of this diagnostic mode command, the effect of the above ($5D_{16}$) command is cancelled.

Set Output Loopback (Q = 056D)

Upon receipt of this diagnostic mode command, output loop signals are shunted across an internal path rather than going through the normal external loop. Specifically, the input to the loop transmitter is connected as the output of the loop receiver (in lieu of the normal connections). Thus no traffic (data or clock) appears on the external loop.

This command can be used alone or in conjunction with the other diagnostic commands.

Clear Output Loopback (Q = 052D)

Upon receipt of this diagnostic mode command, the effect of the above ($6D_{16}$) command is cancelled.

Set Cascade Loopback (Q = 057D)

Upon receipt of this diagnostic mode command, the two loops, whether normal external or internal loopback (or any combination), are linked together in a serial chain. Thus the output data passes through the output loop, then through the input loop, and finally back to the CIB as input data.

Virtually any data format can be sent over the chain, although the effects of the stream on the various LMs and CLAs must be considered. To provide total flexibility, the entire loop batch is issued by the CP. End of line frame flags are ignored. End of loop batch flags only trigger unloading of the buffer. In addition to the array of line frames to be sent (each consisting of CLA address, data or supervision, and the CRC character), the buffer must contain a loop end cell followed by at least one null (to define the end of loop batch). At all other times, empty cells (between loop batches) will be sent.

Clear Cascade Loopback (Q = 053D)

Upon receipt of this diagnostic mode command, the effect of the above ($7D_{16}$) command is cancelled.

Clear Interrupt

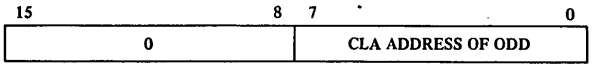
This code is reserved for the stated function for 1700 I/O compatibility, but is not implemented.

AQ CHANNEL INPUT OPERATIONS

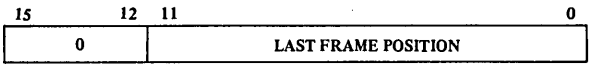
Read ODD (Q = 0500)

Upon receipt of this code, the oldest entry in the ODD FIFO buffer is placed on the data lines and transferred into the low order eight bits of the A register. This 8-bit field contains the address of the CLA demanding output data. Upper eight bits are zero. If ODD FIFO is empty, the value returned will always be 00FF (since the M05 channel is incapable of generating a REJECT). Data lines can assume any value and in general are not specified as to content. Future ODDs will not be lost.

READ ODD (00_{16})



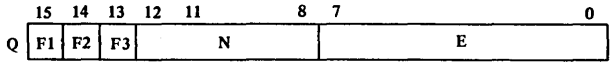
Read Last Frame Position (LFP) Pointer (Q = 0560)



Upon receipt of this code, the current value of the last frame position pointer is placed on the data lines and transferred into the low-order 12 bits of the A register. This field contains the displacement from the buffer origin of the last cell of the last complete line frame. The upper four bits are zero.

This 12-bit field contains the value of the CIB write pointer (measured as a displacement from the buffer origin) at which the last cell of the last complete line frame was written, plus one. It thus points to the location in which the first cell of the next line frame will be written. The value of this pointer is not updated until the next complete line frame has been written. Thus data in the next few buffer locations may have already been overwritten (and thus lost, if not already read) Note that whenever the value of the pointer equals the buffer length, it resets to zero and begins incrementing from that point (in the manner of a true CIB). Issuance of this code also resets the input data available interrupt.

Read FNE Parameters (Q = 0570)



F1 = - (Reserved)
F2 = - (Part of loop end cell)
F3 = Input from secondary lines (part of loop end cell)
N = Number of null cells generated for input loop batch
E = Number of empty cells generated for input loop batch

Upon receipt of this code, the current value of the loop parameter register is placed on the data lines and transferred into the A register.

Note that through the use of this read command and the corresponding set command (78_{16}), 16-bit words can be transferred bidirectionally across the channel, thus serving as a vehicle for testing data integrity across the PIO channel while in a diagnostic (non-operational) mode.

As described above, the F1 bit of the A-field retains the state to which it was programmed by the last write FNE command (Q=0578). It does not automatically clear itself after its function has been performed.

Read Buffer Location (Q = 0502)

Upon receipt of this code, the current value of the CIB location register is placed on the data lines and transferred into the A register. The value is the location into which one loop cell will be written when the pointer is zero (reset). All 16 bits will be programmed by the WRITE LOC command (Q=050A).

Read Buffer Length/ODD Limit (Q = 0512)

Upon receipt of this code, the current value of the ODD threshold register is placed on the data lines and transferred into the upper four bits of the A register.

Concurrently the current value of the CIB length register is placed on the data lines and transferred into the lower 12 bits of the A register; the lower four bits are not used at this time. All 16 bits will be as programmed by the WRITE LIM/LGH (Q=051A).

Read Status (Q = 0576)

Upon receipt of this code, the current value of the MLIA status register is placed on the data lines and transferred into the A register. Issuance of this code also resets the normal MLIA external interrupt.

As noted in the format illustration on the next page, several of the status bits represent stored conditions. These are reset after their state is reported to the CP.

Many of the bits, when on, represent error conditions. These are indicated in the format illustration. Bits not so marked are normally on.

Several of the bits, when on, cause the normal MLIA external interrupt line to be enabled. These are indicated in the format illustration. Note that the MLIA uses two additional, special-purpose interrupts: ODD present and input data available.

If MLIA is in RESET mode, the value returned in A register will be 0268. Upon entering IDLE mode from RESET, first status command will yield 0265. Subsequent status commands will yield 0001 unless an abnormal or diagnostic condition is present. Upon entering NORMAL mode, status should be 0009, if no diagnostics or errors are present.

The function of each status bit is as follows:

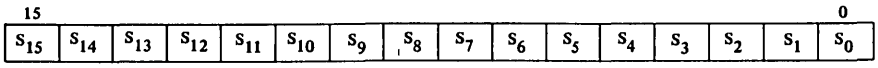
S0 Ready — Begin ready implies that the static operational requirements have been met: cards are plugged in, power applied, cables connected, etc. If this bit is not true for some reason, operator (and/or maintenance personnel) intervention is required. Activity sensors connected to the returning clock and data lines of each loop are conditions required to be ready.

Since the NCR M05 channel does not provide the ability to reject a command, this bit must be tested before becoming operational and during maintenance.

Bit S0 is true if the MLIA is not RESET and the input and output loops are active. Since the loops become inactive when loopback conditions are set, this status bit will be false if either the input loopback, or output loopback, or both are set.

Removal of a circuit board causes the MLIA to RESET immediately and remain reset after the card has been reinstalled. If all MLIA boards are in place and operating properly, issuance of an IDLE

STATUS (76_{16})



Bit	Function	Error	Interrupt	Reset
S0	Ready	E	I	
S1	(Busy)			
S2	Error Interrupt		I	
S3	Normal and No Diagnostic			
S4	(End of Operation)			
S5	Input Buffer Full	E	I	R
S6	Outout Loop Error	E	I	R
S7	Protected			
S8	Parity Error	(E)	(I)	(R)
S9	Input Loop Error	E	I	R
S10				
S11				
S12				
S13	(Reserved)			
S14	(Reserved)			
S15	(Reserved)			

or NORMAL command will clear the RESET condition. Thus, bit S0 will be false if a card is missing or was temporarily removed.

S1 Busy — Being busy usually implies a condition that will clear with time. Normally it is sensed as one reason for a channel reject. However, this reject capability is not available on the NCR M05 channel. Since there is no time when the MLIA is busy and yet still capable of reading status, this bit is not implemented and is permanently off.

S2 Error Interrupt — When true, this bit indicates that one or more causes of the normal MLIA external interrupt are present. The exact cause may be found by examination of other status bits. It represents the logical OR of these bits. Upon responding to the READ STATUS code, these interrupt conditions (and therefore the external interrupt line) are reset.

S3 NORMAL Mode — Unlike some systems, this bit being true does not signal the presence of an interrupt requesting data. The ODD in the MLIA is a separate interrupt line. Furthermore, it does not represent a data interrupt in the context of the NCR ADT feature (which is not implemented in the MLIA). Rather, NORMAL is a status bit indicating that data transfers can occur. It signifies the "on-line" (non-diagnostic mode) condition.

S4 End of Operation — In most systems, this bit being true signifies that a block of data has been written, read, etc., over a DMA channel. Within the MLIA, this function, signifying that a line frame has been written into CP memory, is performed by a unique interrupt. This bit is currently not implemented within the MLIA.

S5 Input Buffer Full — When true, causes an interrupt. Set whenever the generation of a new input loop

batch was delayed owing to lack of room in either the input FIFO or ODD FIFO buffer. Occurrence of this bit suggests that the number of empty/null cells parameter should be modified (or all loop operations halted). Reset by status read.

S6 Output Loop Error — When true, causes an interrupt. Set whenever output loop sync loss, output buffer overrun, or output loop end timeout is detected. (Note that, unlike the input loop, multiple loop batches can exist on the output loop, thus allowing the possibility of losing some loop end timeouts. However, the effect is sensed and reported by the CLA units.) Reset by status read.

Bit S6 does not respond to output buffer overrun. The MLIA does not detect overrun of the output buffers since writing of cells into the buffers is under direct control of the firmware/software.

S7 Protected — Normally true; indicates that the MLIA is capable of writing into protected memory. At present, no means are provided for inhibiting this bit.

S8 Parity Error — Not used in the MLIA since the DMA read capability is not implemented.

S9 Input Loop Error — When true, causes an interrupt. Set whenever input loop CRC error, illegal format, sync loss, or loop timeout is sensed. Reset by status read.

In addition to the conditions listed above, bit S9 is also set by malfunction of the up/down counters for the main FIFO and ODD FIFO (i.e., invalid counter state). Such a malfunction normally will not occur, but can be induced under certain diagnostic conditions.

S10 (Unassigned)

S11 (Unassigned)

S12 (Unassigned)

S13 (Reserved)

S14 (Reserved)

S15 (Reserved)

NOTE

Bits S1, S4, S7, S8, and S10 through S15 are not implemented in the MLIA and will always be zero.

DMA/DEVICE INTERFACE

Each DMA device connected to the MP DMA bus must have the logic to interface to the following signal lines:

16 Data Lines Into Memory $\overline{\text{DTM01-16}}$

16 Data Lines From Memory $\overline{\text{DFM01-16}}$

16 Address Lines $\overline{\text{MAB01}}$ - $\overline{\text{MAB16}}$

3 Control Lines from Memory

a) Memory Acknowledge ($\overline{\text{MCA}}$)

b) Data Strobe ($\overline{\text{MDS}}$)

c) Memory Cycle Timing ($\overline{\text{MCT}}$)

1 Control Line to Memory

a) Memory Cycle Request ($\overline{\text{MCR}}$)

2 Error Signals from Memory

a) Parity Error ($\overline{\text{MPE}}$)

b) Address Error ($\overline{\text{MAE}}$)

The DMA signal line usage is shown on the following page.

The DMA signal timing usage is defined below:

- $\overline{\text{MCR}}$ (Memory Request) must be held low until it is reset (goes high) by $\overline{\text{MCA}}$-$\overline{\text{MCT}}$ or $\overline{\text{MCA}}$-$\overline{\text{MDS}}$. Address, data and write lines must be stable† within 50 ns after $\overline{\text{MCR}}$ is lowered. $\overline{\text{MCR}}$ must be high within 300 ns after the leading edge of $\overline{\text{MDS}}$ unless an additional memory cycle is requested. $\overline{\text{MCR}}$ may be held continuously low for consecutive memory cycles; however, data, address, and write lines must be stable† within 700 ns after the trailing edge of the previous $\overline{\text{MDS}}$. $\overline{\text{MCR}}$ must drive two TTL loads. $\overline{\text{MCR}}$ must be high at power initiation time. A way to guarantee that $\overline{\text{MCR}}$ is a high is to use $\overline{\text{MR}}$ to set (or reset) the latch that creates $\overline{\text{MCR}}$.

- $\overline{\text{MCA}}$ (Memory Acknowledge) is used to gate data and address lines and the write line to a common bus connected to the memory interface logic. Address, data, and write lines must not change when $\overline{\text{MCA}}$ is low. Loading on $\overline{\text{MCA}}$ must not exceed eight TTL loads.

†Stable at the input of the open collector gates used to drive common bus into memory.

DMA Signal Line Usage

Function	Name	Logic Level	Open Collector	Common Signal
Address Lines	$\overline{\text{MAB01-16}}$	Low	Yes	Yes
Data Lines to Memory	$\overline{\text{DTM01-16}}$	Low	Yes	Yes
Data Lines from Memory	DFM01-16	High	Yes	Yes
Memory Write	MW	High	Yes	Yes
Memory Request	$\overline{\text{MCR}}$†	Low	No	No
Memory Acknowledge	$\overline{\text{MCA}}$†	Low	No	No
Memory Timing	$\overline{\text{MCT}}$	Low	No	Yes
Data Strobe	$\overline{\text{MDS}}$	Low	No	Yes
Parity Error	$\overline{\text{MPE}}$	Low	No	Yes
Address Error	$\overline{\text{MAE}}$	Low	Yes	Yes

†Each DMA device is assigned a unique pair of these signal lines.

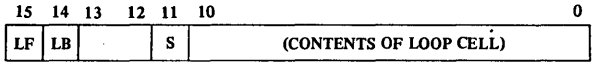
- $\overline{\text{DTM01-16}}$ are data lines from the CP or DMA to memory. Each data line must be driven with an open collector gate.
- MW is the memory write line. MW must be driven with an open collector gate.
- $\overline{\text{MAB01-16}}$ are address lines with MAB01 the least significant line. Address lines are driven with an open collector gate.
- $\overline{\text{MCT}}$ (Memory Timing) is a logic signal which occurs 160 ns before data strobe. This signal is used by a DMA interface; loading should not exceed one TTL load. A common $\overline{\text{MCT}}$ signal is sent to all DMAs.
- $\overline{\text{MDS}}$ (Data Strobe) is used to strobe data out of memory. Data out of memory will be valid for 30 ns before the leading edge of $\overline{\text{MDS}}$ and remain valid until the start of the next memory cycle (800 ns minimum). Loading on $\overline{\text{MDS}}$ must not exceed eight TTL loads.
- DFM01-16 are data lines from memory. Loading must not exceed two TTL loads on each data line.
- $\overline{\text{DMA-MPE}}$ (Parity Error) is sent when a parity error occurs in memory. $\overline{\text{DMA-MPE}}$ is common signal sent to all DMAs. $\overline{\text{MPE}}$ occurs shortly after data strobe but before $\overline{\text{MCA}}$ goes high. Loading on $\overline{\text{DMA-MPE}}$ should not exceed one TTL load.
- $\overline{\text{DMA-MAE}}$ is signal sent on a common signal line to all DMAs. It indicates that the DSA scanner control is in the out position and access to CP memory cannot be achieved.

DMA Channel Input Operations

The MLIA uses the DMA channel to store input line frames directly in the CP memory (CIB). Except in the transparent mode, CRC characters are deleted. Line frames containing only ODD and CRC are deleted even when they are in the last frame in the loop batch; under these conditions, the end-of-loop-batch flag will be dropped and will not appear in the CP. Note that in the CIB, mode six and seven have no distinction in terms of meaning and should be equated by the user.

Input Data

This operation moves information from the main input FIFO to the CIB in CP memory. Format is as follows:



LF = End of Line Frame Flag
LB = End of Loop Batch Flag
S = Sync bit of Loop Cell

Loop cell contents are forwarded right-justified exactly as received from the loop. Bit 11 is the sync bit, bits 10-8 are the format bits, and bits 7-0 contain the specific information (CLA address, data, supervision, etc.)

End of line frame flag is set in the last word stored in a line frame. It is associated with the loop cell immediately preceding the CRC and typically contains the data (or supervision) character. It is set in the CLA address character only when the CLA address contains an ODD and is the last line frame of a loop batch. This flag is not set when in the transparent mode.

End of loop batch is set along with end of line frame in the last word stored in a loop batch. It cannot occur without an accompanying end of line frame and thus meets all of the preceding requirements. This flag is set when in the transparent mode.

At the conclusion of each line frame transfer into the CIB, a special interrupt is turned on (if not already on). It alerts the firmware that the CIB read and write pointers are unequal owing to the storage of added information. The interrupt resets whenever the LFP pointer value is read.

DMA Channel Output Operations

The low performance MLIA does not use the DMA output capabilities.

INTERRUPTS

Operation of the MLIA interrupt system differs markedly from more conventional users owing to the need for high processing efficiency plus the unique capabilities of the CP hardware and firmware.

CP Interrupt System

Conventional processors, upon receipt of an external interrupt, halt processing at the conclusion of the present instruction and execute special interrupt code before resuming normal operation. In the CYBER 18-25/30 CP however, interrupt lines are merely external data sources for loading a special register. Under firmware control, these register inputs are strobed and thus available for any use by reading through a programmable mask register.

Two approaches are used depending on whether, at the time of interrupt occurrence, control is held by the emulation firmware or the special system firmware. The latter approach is used by the multiplex subsystem portion of the communications processing package, while the former approach is used both by higher level (macro) code and all diagnostics.

Standard emulation samples the interrupt register as part of the read next instruction (RNI) phase of each software instruction execution. Should either an internal (special system) or external (standard macro) interrupt be detected, control is then passed to the special firmware or the emulation package (respectively).

Special multiplex system firmware samples the interrupt register on a time basis. Under this plan, the register is sampled a minimum of once every 20 microseconds. During the interval between samples, numerous macroinstructions can be processed. Further, this sampling can be delayed until any level of critical processing is completed without incurring time penalties in extensive interrupt lockouts. It is also possible to assign some of these interrupts as internal and others as external.

Interrupt Implementation

Within the NCR M05 channel specification, two interrupts are specified: one program and one data interrupt. The MLIA uses the program interrupt as the "normal" external interrupt and uses the bits of the status word to identify the specific cause. The data interrupt is not implemented within the MLIA since it is used in conjunction with the ADT feature. However, two additional, unique interrupts are provided as described below.

Program Interrupts

Main use of this interrupt is to report MLIA error conditions. The MLIA protects itself against data loss, forcing the effect to show up on a per-line basis as overruns and/or underruns. Using the bit of the status word to identify error causes, error statistics are accumulated and recorded. When the number of errors exceeds some programmable threshold, software/firmware marks the unit down as in need of maintenance.

This interrupt is not cleared by setting bit one in the A register and then issuing a function code. To preserve operating efficiency, the A register is not used. Instead, a unique code (76_{16}) in the address (Q register) requests that MLIA status be read. As a part of this operation, stored conditions are reset and, since it is the logical OR of these bits that drives the interrupt, it becomes reset.

Output Data Demand Interrupt

Whenever the ODD FIFO contains any entry (or entries), this line is true. Its presence (or absence) is controlled

entirely by the contents, of this ODD FIFO. Whenever, through reading out the FIFO contents, the internal contents counter goes to zero, the interrupt automatically resets.

Input Line Frame Interrupt

Each time a complete line frame has been stored in CP memory, this interrupt is raised. Since input data is a low priority task, several frames may accumulate before the firmware uses this interrupt. Its main purpose is to eliminate the need for firmware comparing the CIB read and write pointers in order to detect recent activity.

Whenever the current value of the last frame position (LFP) pointer is sensed (60_{16}), this interrupt is automatically reset.

NOTE

Each of the three interrupts uses DC-type (rather than pulse-type) signalling and thus does not depend on CP internal storage. Depending upon system requirements, any or all of these interrupts can be wired as both "internal" and "external" simultaneously, thus providing ready access for operational software, firmware, and diagnostics.

COMMUNICATIONS LINE ADAPTERS

Interface to external modems and/or locally attached terminals is via a limited number of communications line adapters (CLAs). Different types of CLA units are required for major electrical differences (e.g., synchronous versus asynchronous, RS232/V-24 versus differential/V-35 versus coaxial).

Other parameters such as speed, sync code, character length, parity, etc., are controlled by software/firmware through the use of parameter registers. Supervisory commands are sent to the CLA units to set up these parameter registers/ correspondingly, status can be received back from the CLA units, either upon command or upon the occurrence of a specified event.

For inbound traffic, CLA units strip off all communications-oriented distinctive characteristics which can be removed without knowing the meaning of the bits (e.g., code set, line protocol). At the interface to the LM, each CLA presents characters one at a time (character serial — at a rate determined by the external communication channel speed), bit paralleled, right-justified, properly framed, with "house-keeping" characters (start/stop bit, parity, etc.) removed. At this interface all CLA units present an identical interface. Outbound this process is reversed.

As each inbound character is received, it is converted to bit-parallel form and transferred to a one-word buffer where it is held until it can be placed on the loop. Similarly, outbound characters leave a one-word buffer as they become serialized and are sent out. Each time this outbound buffer is empty (and the CLA is active), an ODD is sent to the CP for the next character. Failure to provide or accept characters in a timely manner results in an overrun/underrun condition.

In summary, the CLA accepts supervision (i.e., control word) and output data from the loop and yields status, input data and ODDs to the loop.

Specific programming information for any specific CLA can be obtained from the corresponding CLA hardware reference/maintenance manual (see Preface).

Procedures for installation of the COMMUX equipment are provided in the CYBER 18 Computer Systems Installation Manual. Refer to that manual for detailed instructions on initial system installation or on adding new equipment to the system.

This section provides a detailed functional description of the basic assemblies and control elements of the COMMUX. References to other manuals are provided for those items covered separately. Detailed logic diagrams referred to in this section are presented in section 5.

MULTIPLEX LOOP INTERFACE ADAPTER

The multiplex loop interface adapter (MLIA) consists of three circuit boards. The input loop interface board contains most of the logic associated with sending and receiving serial data over the 20-MHz input loop. The output loop interface board contains most of the logic associated with sending and receiving data over the 20-MHz output loop. The processor interface board contains most of the logic associated with writing and reading various MLIA registers via the M05 (A/Q) channel of the MP17. Refer to figure 1-1 for card location and figure 1-6 for functional block diagram.

The output loop interface board also contains some of the control logic for the input loop, plus master oscillator logic and timing and control for all direct memory access (DMA) operations.

INPUT LOOP INTERFACE LOGIC

Refer to figure 4-1 for a functional block diagram of the input loop interface board. There are eight functional sections: loop cell generator, loopback switches, receive registers, sync detect and CRC check, cell decoder, edit logic, data input buffer, and data demand buffer.

LOOP CELL GENERATOR

Twelve-bit loop cells are generated according to the loop end and restart loop end control signals (R-LE and R-RLE). These signals originate on the output loop interface board and affect the input loop cell generator as follows:

R-LE	R-RLE	Action
HIGH	HIGH	Generate an EMPTY cell
HIGH	LOW	Generate a Restart Loop END
LOW	HIGH	Generate a normal loop END
LOW	LOW	Generate a NULL cell

The loop cells are loaded into a shift register in sync with the 600-ns clock (CP600). The shift register converts the loop cells from parallel to serial and feeds the serial bit stream to the transmit and receive selectors (loopback switches).

LOOPBACK SWITCHES

The transmit selector sends serial data (signal TDI) onto the input loop from one of three possible sources: the input cell generator discussed above, the output loop cell generator (signal W-LD), or the output loop receiver (signal W-RD). The latter two signals originate on the output loop interface board. In addition, the transmit selector can also shut off the input loop entirely.

Similarly, the receive selector can accept serial data from one of four possible sources: the receiving end of the input loop (RD1), the input loop cell generator, the output loop cell generator (W-LD), or the output loop receiver (W-RD). The loopback control logic, located on the input loop interface board, selects the appropriate data sources needed to achieve any combination of input, output and cascade loopbacks.

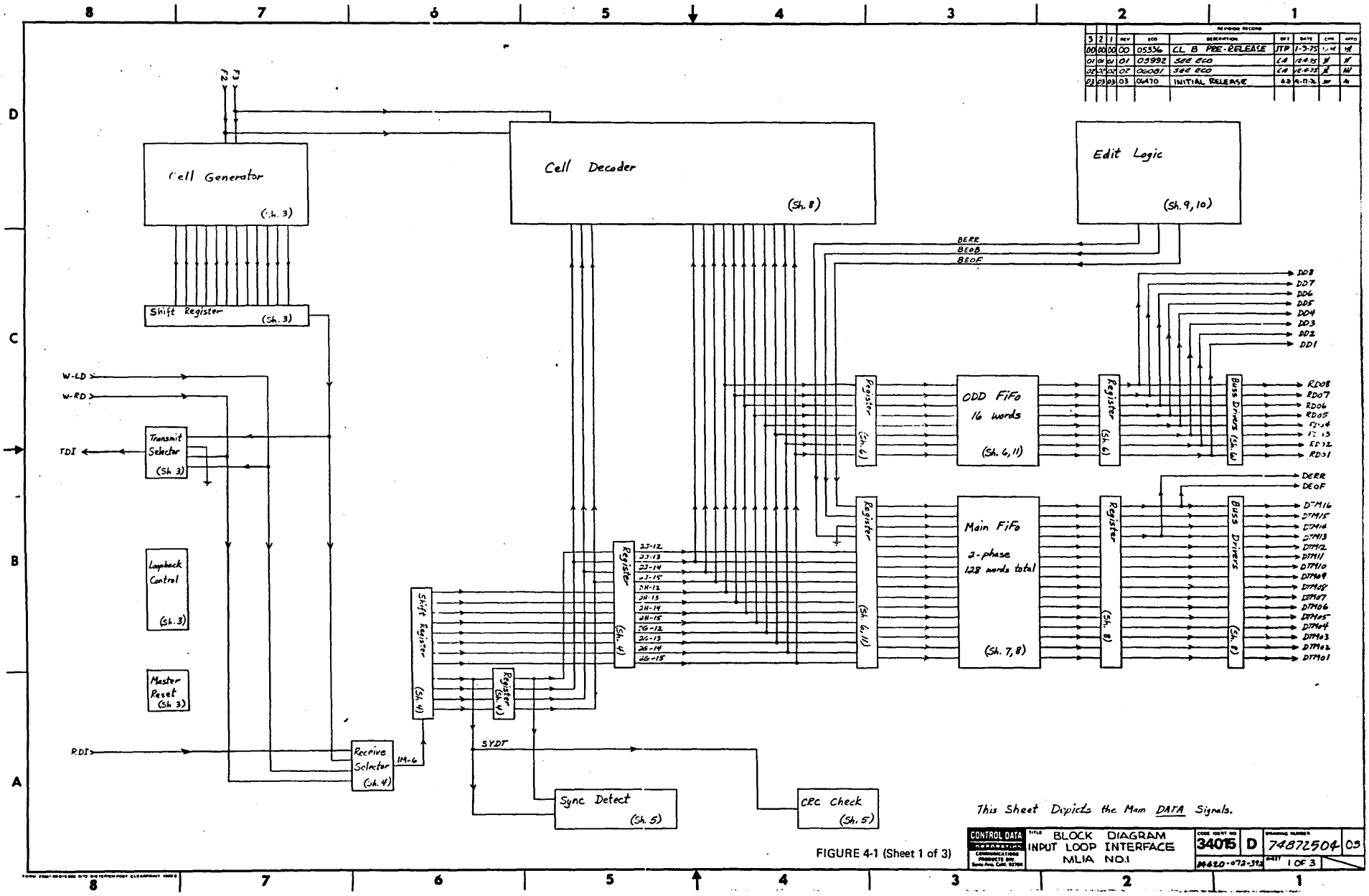
RECEIVE REGISTERS

The receive selector feeds serial data into a 12-bit shift register. When the sync bit of the incoming loop cell has reached stage four (signal SYDT), the previous loop cell is parallel loaded into the main holding register, where it is retained for one complete cell time. The content of the main holding register feeds the cell decoder, data demand (ODD) buffer, and data input buffer. The cell decoder, in turn, drives the edit logic, which determines whether or not the cell should be loaded into the ODD or data input buffers.

A 4-bit look-ahead register is loaded at the same time as the main holding register. The look-ahead register contains the first four bits of the next loop cell following the cell currently trapped in the main holding register. This allows the edit logic to anticipate the type of loop cell that will next enter the main holding register.

SYNC DETECT AND CRC CHECK

The receive logic operates independently of the transmit logic. The receive logic must therefore acquire synchronization (i.e., determine where the sync bit is)



REVISION RECORD									
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00	00	00	00	05356	CL B PRE-RELEASE	JTP	1-5-75		
01	01	01	01	05992	SEE ECO	LA	12-4-75		
02	02	02	02	06081	SEE ECO	LA	12-6-75		
03	03	03	03	06470	INITIAL RELEASE	KD	9-17-76		

This Sheet Depicts the Main DATA Signals.

FIGURE 4-1 (Sheet 1 of 3)

CONTROL DATA CORPORATION	TITLE: BLOCK DIAGRAM INPUT LOOP INTERFACE MLIA NO.1	CODE IDENT NO 34015	D
		74872504	03
		84420-072-312	SHEET 1 OF 3

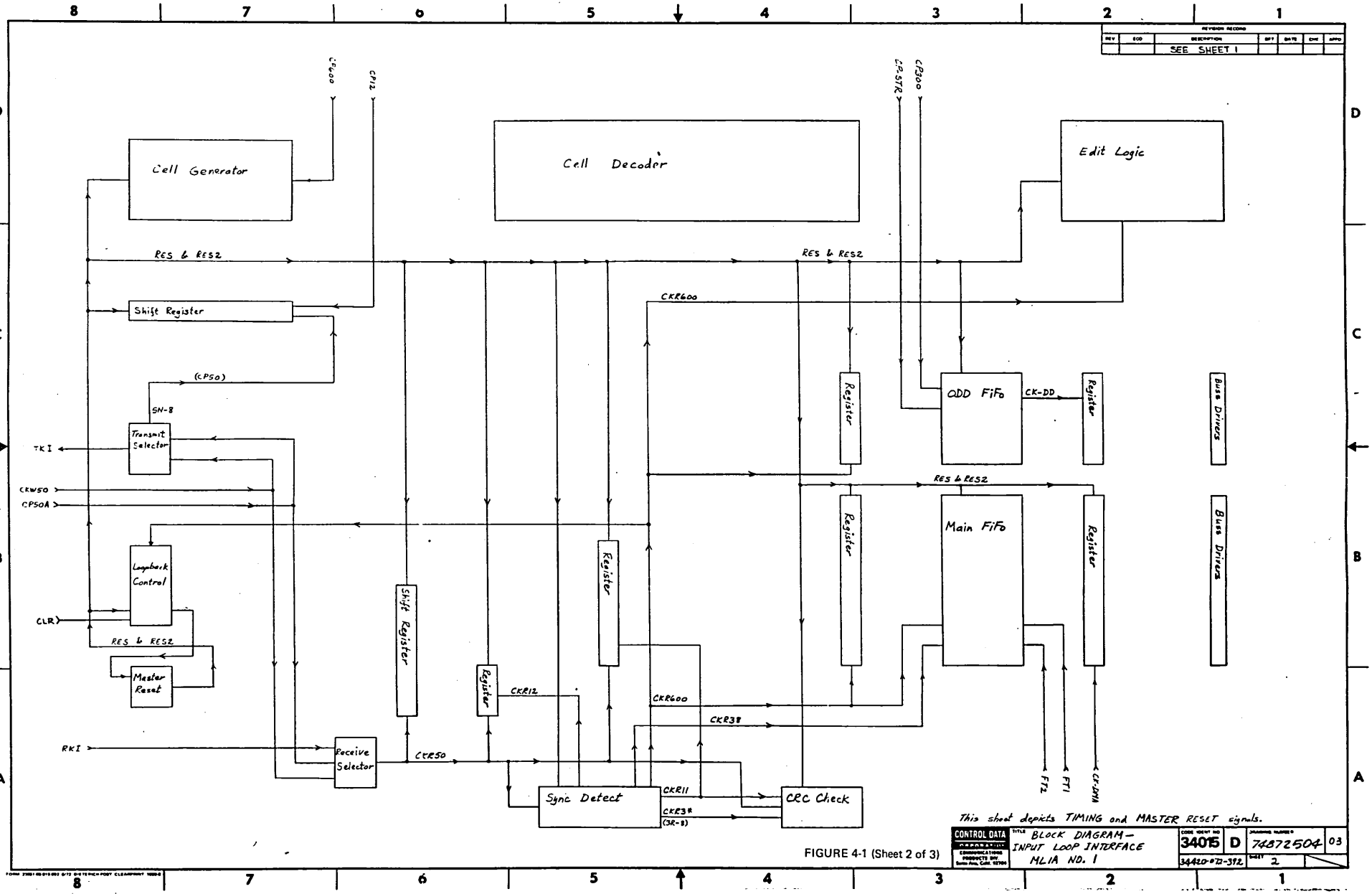


FIGURE 4-1 (Sheet 2 of 3)

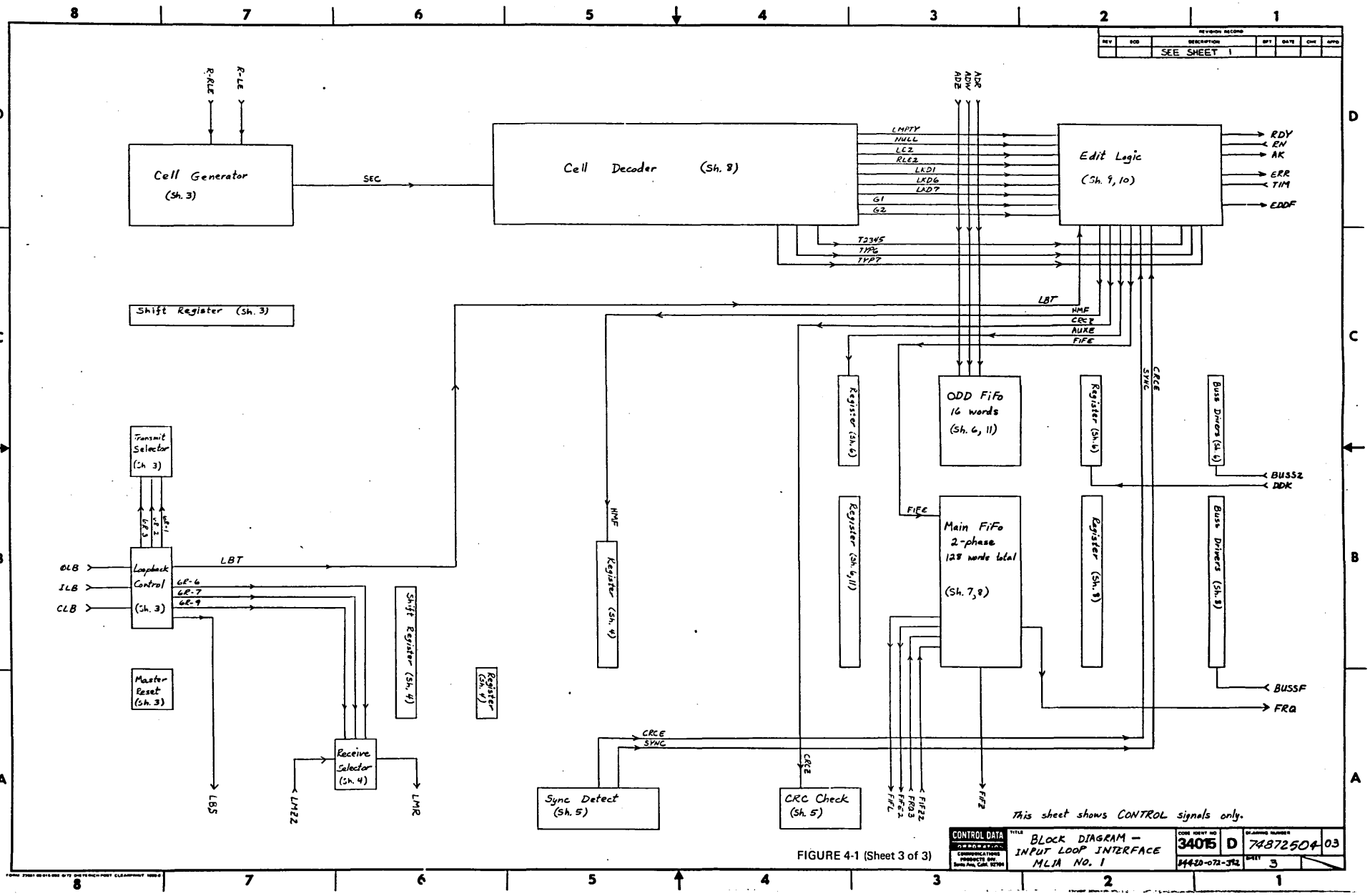


FIGURE 4-1 (Sheet 3 of 3)

using only the incoming serial data. This function is performed by the sync detect logic according to the following algorithm:

(a) If the receive logic is out of sync, a divide-by-twelve counter gets reset whenever the current sync data (SYDT) is one. The counter counts normally whenever SYDT is zero (low).

(b) Whenever the counter reaches the twelfth count, the look-ahead and main holding registers are loaded. Since there had to be eleven consecutive zeros in order to reach the twelfth count, the twelfth bit of the cell should be a one (the sync bit of an empty cell). If it is a one, then the receive logic will be in sync from that point on.

(c) Once sync has been acquired, the counter no longer gets reset by a one on the SYDT line. Consequently, the logic remains in sync as long as every twelfth bit is a one.

The sync data signal (SYDT) also feeds the cyclic redundancy check (CRC) logic, which performs a serial CRC computation and sends a CRC error signal (CRCE) to the edit logic.

Most of the clock signals driving the receive registers and edit logic are derived from the sync detect counter.

CELL DECODER

The contents of the main holding register and look-ahead register are examined by the cell decoder, which sends the following control signals to the edit logic:

Empty indicator

Null indicator

Loop end indicator (LE2)

Restart loop end indicator (RLE2)

Cell type 7 indicator (TYP7)

Cell type 6 indicator (TYP6)

Cell type 2, 3, 4, 5 indicator (T2345)

Each of these signals is normally low and goes high whenever the main holding register contains the corresponding type of loop cell. In decoding a loop end cell, the decoder uses the secondary line signal (SEC) in conjunction with the two flat bits, F2 and F3, to determine the proper settings of the corresponding bits in the loop end cell. SEC originates in the loop cell generator; it toggles whenever a normal loop end is sent. The loop and flag bits, F2 and F3, originate on the processor interface board and are programmed directly by the processor.

The cell decoder also checks the look-ahead register and issues three decode signals to the edit logic:

Look-ahead cell type 7 (LKD7)

Look-ahead cell type 6 (LKD6)

Look-ahead cell type 1 (LKD1)

Each of these signals is normally low and goes high whenever the look-ahead register contains the corresponding type of loop cell.

Two additional signals, G1 and G2, are generated by the cell decoder. They are used by the edit logic whenever the MLIA is in transparent mode. The signals refer to the content of the main holding register as follows:

G1	G2	Type of Loop Cell
HIGH	HIGH	1000 101X XXXX
HIGH	LOW	1001 XXXX XXXX
LOW	HIGH	1000 011X XXXX
LOW	LOW	None of the above

"X" means "don't care." The first case above is the same as a null for the first seven bits. The second case includes loop ends and restart loop ends. The third case is a non-standard cell type used only for diagnostic purposes.

EDIT LOGIC

The edit logic accepts the decode signals from the cell decoder and decides:

1. Whether or not to load the current loop cell into the data input buffer

2. What flag bits (end of frame, end of batch, error) to set

3. Whether or not to load the lower eight bits of the current loop cell into the data demand buffer

4. When to restart the cyclic redundancy check logic

5. When to issue the error signal (ERR) to the input loop launch controller located on the output loop interface board

6. When to freeze the main holding register while the cyclic redundancy checksum is being checked

Operation of the edit logic is monitored by the input launch controller located on the output loop interface board. Whenever the edit logic is ready to handle a new loop batch, the ready line (RDY) goes low. When a new loop batch is started by the launch controller, the run line (RN) toggles (changes state). The edit logic then responds by raising the ready line (RDY) and toggling the acknowledge line (AK). As soon as a complete loop batch has been correctly received, the edit logic again lowers the ready line (RDY) to signify that it is ready for the next loop batch.

If the loop batch is incorrect because of an illegal cell, cyclic redundancy checksum error, or loss of sync, the edit logic lowers the error line (ERR) instead of lowering the ready line (RDY). This signals the launch controller to issue a restart loop end. As soon as the restart loop end returns and is detected by the edit logic, the error signal (ERR) goes high and ready (RDY) goes low, signifying that a new loop batch may begin.

If the edit logic fails to respond properly within the time interval allotted by the launch controller, the timeout (TIM) signal is activated. The edit logic should then respond by lowering the error line (ERR). If the edit logic still fails to respond or fails to recover properly from the error condition, the launch controller on the output loop interface board will continue to issue restart loop ends unless that function has been inhibited by some other condition such as idle mode or cascade loopback.

DATA INPUT BUFFER

The data input buffer is a first-in, first-out (FIFO) memory having 128 words of 16 bits each. The lower 12 bits of each word contain the loop cell exactly as received from the input loop. The upper four bits contain the end of frame flag (BEOF and DEOF), the end of batch flag (BEOB), the error flag (BERR and DERR), and one unused bit which is always zero. Whenever the edit logic decides that a loop cell should be loaded, it lowers the FIFO enable line (FIFE) for one cell time. At the end of that interval, the FIFO loaded signal (FIFL) generated by the FIFO will toggle (change state). Whenever that signal toggles, an up-down counter located on the processor interface board records the fact that a loop cell was loaded.

The output side of the FIFO operates independently of the input side. Whenever a 16-bit word has propagated through the FIFO and is available for transfer over the direct memory access (DMA) channel, the FIFO request line (FRQ) goes low. The DMA controller on the output loop interface board then obtains access to the DMA channel and toggles the FIFO timing lines (FT1 and FT2). When the channel is ready for the data, the DMA controller also activates the bus enable line (BUSSF), causing the data to be gated directly onto the DMA bus.

Meanwhile, the FIFO responds to the toggling of FT1 and FT2 by raising the FIFO request line (FRQ) until the next data word is available. Toggling of FT1 also causes the up-down counter on the processor interface board to record the fact that a loop cell was unloaded from the FIFO.

Whenever there is no data present at the FIFO output and no data was loaded into the FIFO for approximately 64 cell times, the FIFO is presumed to be empty and is forced into the master reset condition. This causes the FIFO to generate the FIFO zero signal (FIFZ) which clears the up-down counter on the processor interface board. It also clears portions of the DMA controller on the output loop interface board. The forced reset is triggered by the secondary FIFO zero (FIFZ2) and auxiliary FIFO request (FRQ3) signals, which originate on the output loop interface board. FRQ3 goes low whenever there is no FIFO output data ready and no DMA transfer in progress. FIFZ2 goes low whenever 64 loop cells (including empties) have been received without being loaded into the FIFO. The forced reset is the only mechanism available for insuring that the FIFO and associated logic on other boards will always remain properly synchronized.

DATA DEMAND BUFFER

The data demand (ODD) buffer is separate from the data input buffer. It, too, is a first-in, first-out buffer (FIFO) but it has only 16 words of eight bits each. It operates at very high speed to store communications line adapter (CLA) addresses until they can be read by the processor via the M05 (A/Q) channel.

Whenever the edit logic decides to load the data demand (ODD) FIFO, it toggles the enable data demand FIFO signal (EDDF). This triggers logic on the processor interface board, which activates the data write line (ADW) to enable loading. Whenever the processor reads an ODD, the read line (ADR) causes the next entry in the ODD FIFO to become available. If the ODD FIFO is empty, the zero line (ADZ) and data demand clear (DDK) line will go low, forcing the ODD FIFO to remain reset. The ODD FIFO is thus under total control of the read-write logic on the Processor Interface board.

The ODD FIFO actually consists of a random access memory (RAM) and two address counters. One

counter specifies the write address, while the other counter specifies the read address. Functionally, however, it operates in a true first-in, first-out manner.

Output Loop Interface Logic

Refer to figure 4-2 for a functional block diagram of the output loop interface board. There are nine functional sections: channel interface registers, output buffer, loop cell generator, output launch controller, output loop receive logic, input loop launch controller, direct memory access controller, status report logic, master oscillator logic.

CHANNEL INTERFACE REGISTERS

Output data from the processor is loaded into a 16-bit holding register where it remains until the output buffer is ready to accept it. There are two holding registers: one register interfaces the A/Q channel while the other register is used only in the high-performance MLIA. Loading of the A/Q interface register is controlled by the loop cell write clock (CK-WLC), which originates on the processor interface board and is synchronized with A/Q channel timing. Loading of the high-performance interface register is controlled by the direct memory read clock (CK-WDM), which remains unconnected in the present MLIA design. Hence, the high-performance interface register can never be loaded in the present design and will always remain reset.

The lower 12 bits of each word loaded into the holding register must contain a complete loop cell. The upper four bits contain the end of frame flag (EOF), end of batch flag (EOB), data destination flag (DDF), and data present flag (DAT). EOF, EOB, and DDF are controlled by the processor; DAT is reserved for internal use by the MLIA and cannot be loaded by the processor. The end of frame flag (EOF) causes insertion of a cyclic redundancy check cell into the output stream. The end of batch flag (EOB) initiates the output stream and causes a loop end cell to be added to the end of the stream. The data destination flag determines which half of the output buffer is to be loaded.

The data present flag (DAT1 or DAT2) is used as a "register loaded" indicator. Since loading of the channel interface registers is completely independent of output buffer timing, the output launch controller relies on the data present flag to indicate the presence of new data. The flag is wired to toggle (change state) whenever the register is loaded. Either register can be loaded at any time; a source selector combined with priority logic in the launch controller determines which register will be read into the output buffer on any one clock cycle (CP300).

OUTPUT BUFFER

The output buffer is a random access memory (RAM) having 16 words of 16 bits each. Addressing is determined by two counters and a selector. One counter is initially set to memory address 15 and counts down whenever it is used as the load address. The other counter is initially set to memory address zero and counts up whenever it is used as the load address. The address selector determines which counter is used as the load address. The output buffer is thereby divided into an upper area and a lower area. The upper area begins at address 15 and proceeds downward, while the lower area begins at address zero and proceeds upward.

The data destination flags (DDF1 and DDF2) determine which half of the buffer is to be loaded. Either half may be loaded from either holding register, and the two halves may be loaded in any order. Either half may contain up to 16 loop cells, provided that the combined total in both halves does not exceed 16.

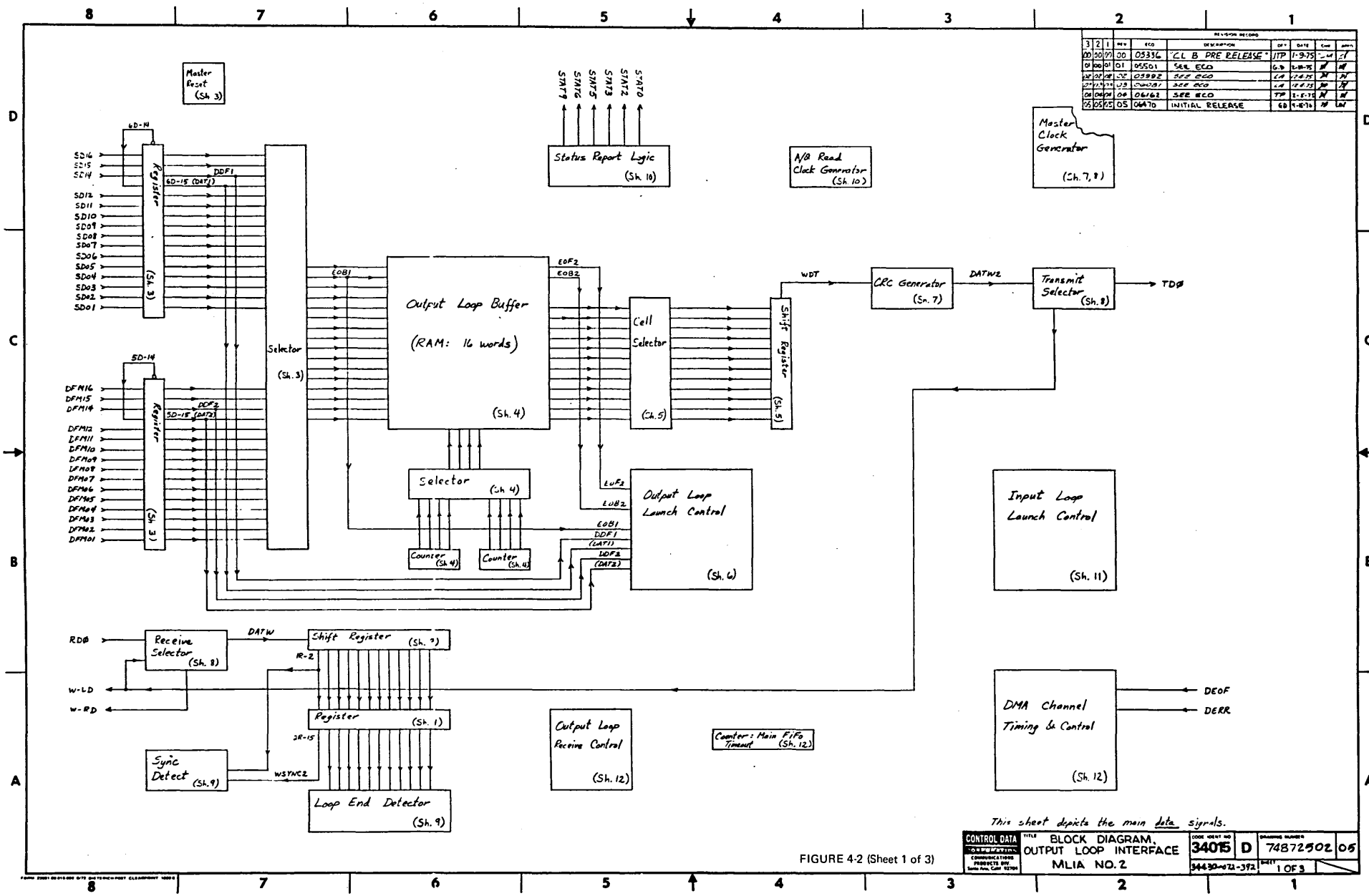
Either half can continue to load while the other half is being transmitted. In addition, the holding register can store one cell destined for the same half that is being transmitted. In this case the holding register will then become unavailable for any further loading until the output buffer has finished transmitting. Availability of the holding register is signalled by the auxiliary data present line (DAT1A*).

LOOP CELL GENERATOR

When the end of batch flag (EOB) is detected, emptying of the corresponding half of the output buffer begins. The outgoing data first passes through a cell selector and then enters a shift register. The serial output from the shift register passes through the cyclic redundancy checksum (CRC) generator and a loopback switch before going out onto the output loop.

The cell selector generates empty cells whenevever the output buffer is not being transmitted. It also generates loop end cells and the upper four bits of cyclic redundancy check cells. The CRC generator then fills in the lower eight bits of CRC cells. The cell selector and CRC generator are controlled by four signals: RAM select (W-RAM), loop end select (W-LE), CRC select (WCRC), and CRC reset (CRC=0).

The loopback switch generates the internal output launch data (W-LD) signal used in cascade and output loopbacks. It also shuts off the output loop whenever the output loopback control (LBS) is on.



REVISION RECORD									
3	2	1	REV	ECO	DESCRIPTION	BY	DATE	CHK	APPR
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01	00	01	01	05501	SEE ECO	GJS	4-30-75	JM	JM
02	02	02	02	05982	SEE ECO	CA	7-14-75	JM	JM
03	03	03	03	06081	SEE ECO	CA	9-8-75	JM	JM
04	04	04	04	06162	SEE ECO	TJP	11-5-75	JM	JM
05	05	05	05	06470	INITIAL RELEASE	GB	1-8-76	JM	LM

This sheet depicts the main data signals.

CONTROL DATA CORPORATION COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92705	TITLE: BLOCK DIAGRAM. OUTPUT LOOP INTERFACE MLIA NO. 2	CODE IDENT NO 34015	D	DRAWING NUMBER 74872502 05
		34430-022-392		SHEET 1 OF 3

FIGURE 4-2 (Sheet 1 of 3)

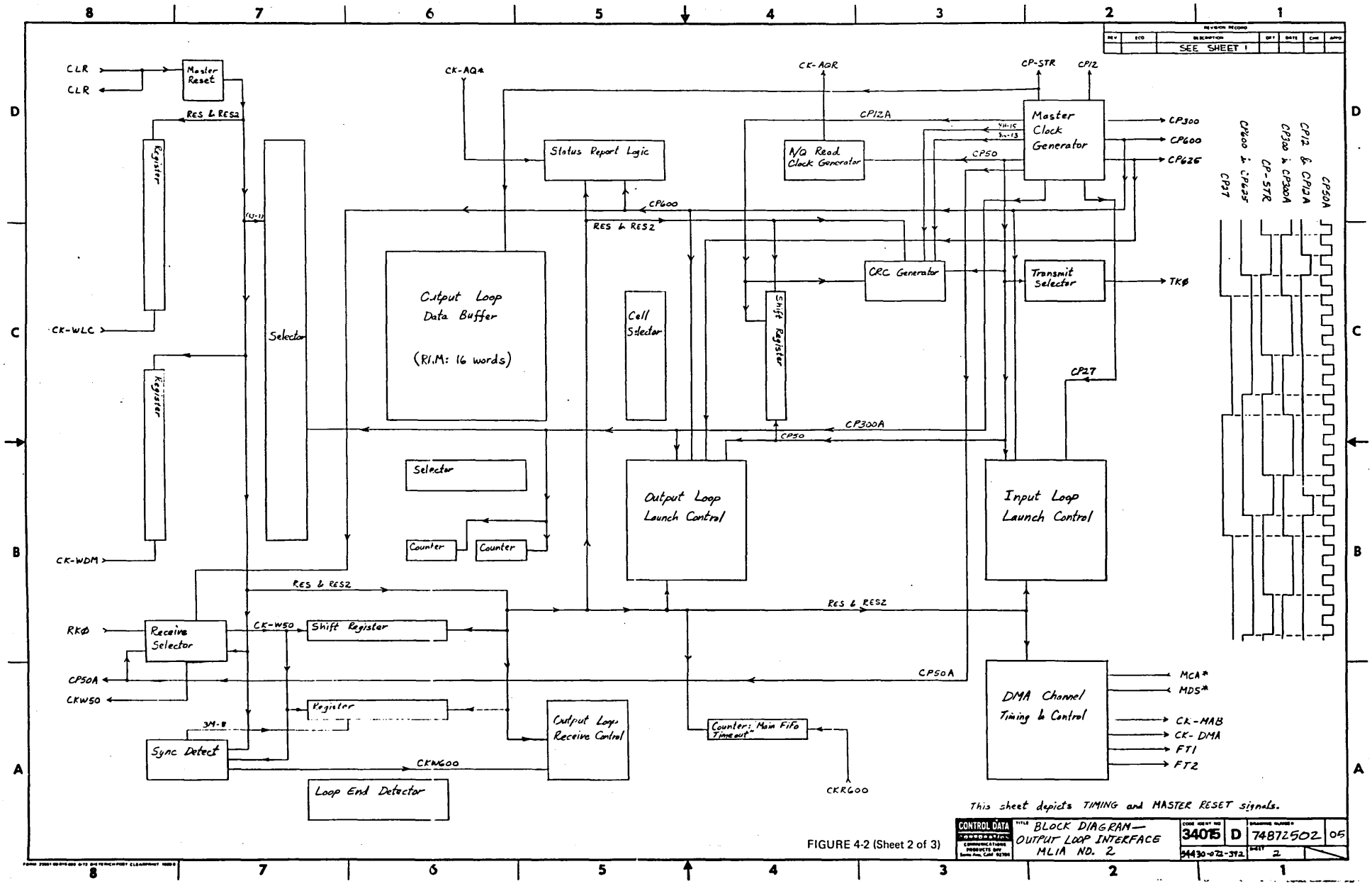


FIGURE 4-2 (Sheet 2 of 3)

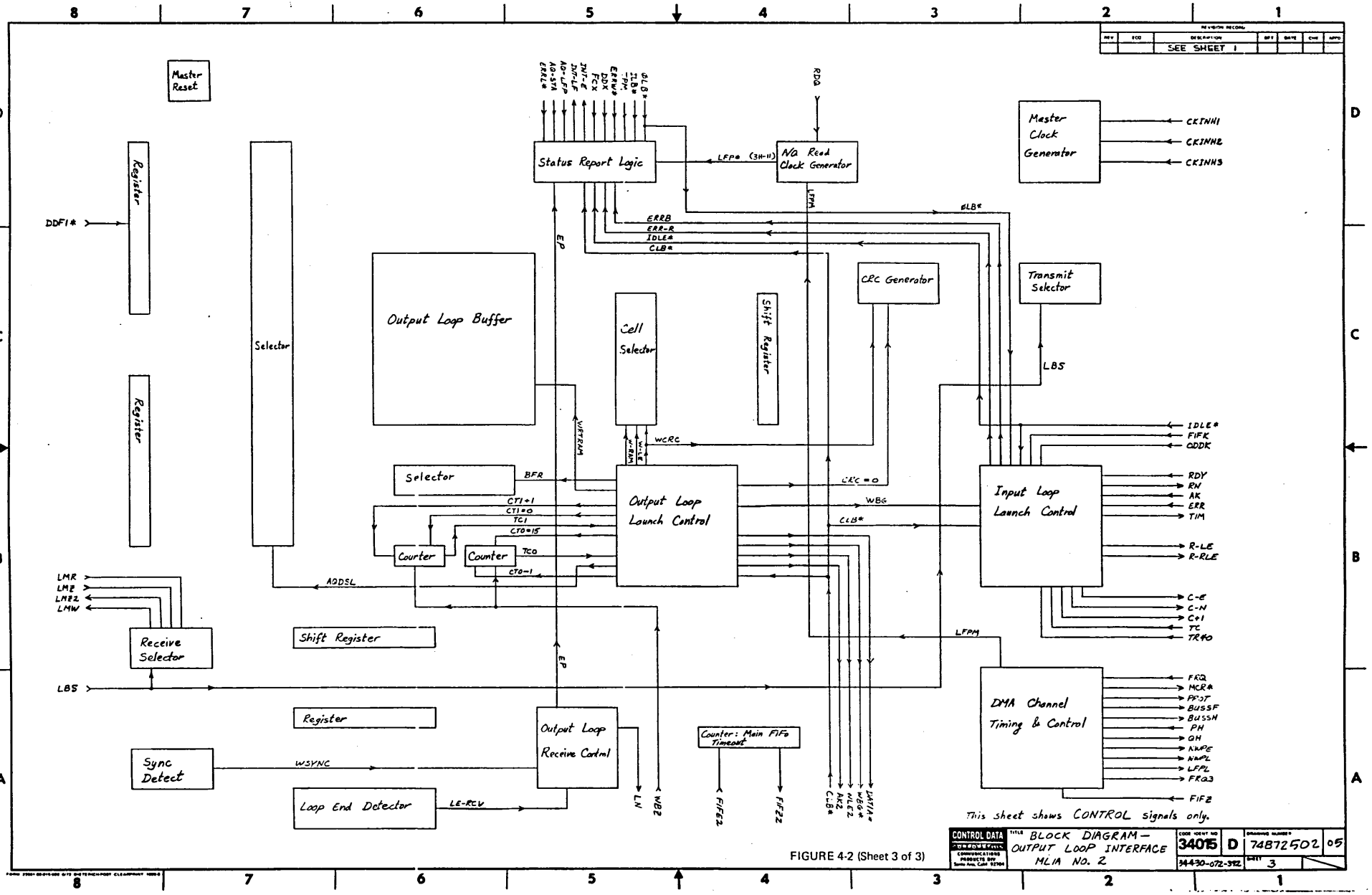


FIGURE 4-2 (Sheet 3 of 3)

OUTPUT LAUNCH CONTROLLER

The output launch controller senses the flag bits discussed above and decides:

1. Whether or not the output buffer will be loaded
2. Which half to load
3. Which holding register to select
4. Whether or not the output buffer will be transmitted
5. Which half to transmit
6. When to insert a cyclic redundancy check cell
7. When to insert a loop end cell
8. When to shut off the cyclic redundancy checksum generator
9. When to enable, inhibit, or reset the RAM address counters

The output launch controller also issues the launch begin signal (WBG) to the input loop launch controller. WBG is used only in cascade loopback mode: it synchronizes the input launch controller with release of the output stream. A similar signal (WBG*) is available as a test point for triggering an oscilloscope.

OUTPUT LOOP RECEIVE LOGIC

Serial data returning on the output loop passes through a loopback switch and then enters a shift register. Whenever the sync bit of the loop cell is present in the first stage of the register, the entire loop cell is transferred in parallel to a holding register. The holding register feeds a loop end detector, which issues the loop end received signal (LE-RCV) to the output receive controller.

The loopback switch selects data from one of two possible sources: the receiving end of the output loop (RDO), or the output launch data (W-LD). It also generates the internal output receive data signal (W-RD) used in cascade loopback.

The output of the first stage of the receive shift register is used for sync detection. The algorithm is the same as in the input loop receive logic on the input loop interface board.

The output receive controller senses the loop synchronization signal (WSYNC) and issues an error signal (EP) whenever sync loss occurs. It also senses the loop end received line (LE-RCV) and toggles the loop-end-in (LN) line whenever a loop end cell is received. The toggling of LN is sensed by the output loop timer located on the processor interface board.

INPUT LOOP LAUNCH CONTROLLER

The input launch controller decides:

1. When to begin a new loop batch
2. What loop cells to generate
3. When to issue the timeout signal (TIM)
4. When to load the loop cell counter located on the processor interface board
5. Which of three possible values to load into the counter
6. When to issue loop error (ERR-R) and buffer full (ERRB) signals to the status report logic

A new loop batch normally begins as soon as the edit logic on the input loop interface board is ready. This is signalled by the RDY line. Initiation of loop batches is suspended whenever:

1. The MLIA is in idle mode. This is indicated by the IDLE* signal originating on the processor interface board.
2. The MLIA is in cascade loopback. This is indicated by the CLB* signal originating on the processor interface board. A new loop batch will be initiated when the output-begin signal (WBG) is detected, except that the resulting data will be blocked by the loopback switch on the input loop interface board. The main purpose of WBG is to allow the edit logic on the input loop interface board to be turned on.
3. There is insufficient space available in the data input buffer on the input loop interface board. This condition is indicated by the FIFO "OK" signal (FIFK) originating in the up-down counter logic on the processor interface board.

4. There is insufficient space available in the data demand buffer on the input loop interface board. This condition is indicated by the data demand "OK" signal (ODDK) originating on the processor interface board.

There is a counter on the processor interface board which the input launch controller uses to count loop cells. Whenever a new loop batch is started, the launch controller sets this counter to the value of the "E" field in the "FNE" register on the processor interface board. The launch controller then generates one loop end and as many empty cells as it takes for the counter to decrement to zero. Next, the counter is set to the value of the "N" field and null cells are generated until the count again reaches zero.

Finally, the launch controller generates empty cells again until the counter reaches 40 (indicated by the TR40 signal) or until the edit logic on the input loop interface board responds with ready (RDY) or error (ERR). If the counter reaches 40 (indicating 40 loop cells sent) before the edit logic responds, a malfunction is assumed to have occurred and the timeout (TIM) signal is issued to the edit logic.

The empty count (C-E), null count (C-N) and count enable (C+1) signals control the cell counter. When the count has been exhausted, the terminal count line (TC) signals the input launch controller. If the edit logic responds with ready or error before the count is exhausted, and if the output loopback is off (indicated by OLB*), then the launch controller will immediately terminate the launch and prepare for the next launch. For diagnostic purposes, however, this speed-up feature can be inhibited by setting the output loopback. The launch controller will then proceed through the complete launch sequence, issuing the full number of empties and nulls.

Whenever initiation of the next loop batch is inhibited by conditions 3 or 4 above, the input launch controller issues a buffer full signal (ERRB) to the status report logic. Whenever the edit logic issues an error signal (ERR) or a timeout occurs (TIM), the launch controller issues an input error signal (ERR-R) to the status logic.

The ready line (RDY) also triggers the INPUT BUSY indicator light. Since RDY goes high (off) whenever a new batch or error restart is initiated, the indicator light goes on whenever the edit logic on the input loop interface board is expecting a loop end or restart loop end.

DIRECT MEMORY ACCESS CONTROLLER

The direct memory access (DMA) controller senses the FIFO request (FRQ), end of frame (DEOF) and error (DERR) signals originating on the input loop interface board. It also senses the high-performance request line (PH), which is permanently grounded in the present MLIA design. The DMA controller then makes the following decisions:

1. When to request access to the DMA channel
2. When to update the last frame position (LFP) pointer located on the processor interface board
3. When to backspace the next word position (NWP) pointer located on the processor interface board
4. When to increment the NWP pointer
5. When to release the channel

Whenever there is data present at the output end of the data input buffer (FIFO) on the input loop interface board, the FIFO request line (FRQ) will go low. If the memory cycle request line (MCR*) is high, it will go low immediately to request access to the channel. The channel will eventually respond by lowering and later raising the memory cycle acknowledge line (MCA*).

The channel is released automatically after each memory cycle unless the end-of-frame flag (DEOF) is set. Whenever the flag is set, the channel will be held for one additional cycle to allow updating of the line frame position pointer (LFP) in the memory address logic on the channel interface board. If new data is available during this additional memory cycle, it will be written. Otherwise, old data will be written and later overwritten with new data. The channel will be released after the holding cycle even if more new data is available. The data will remain in the FIFO until the channel has been released and later re-acquired. Thus, the channel will never be held for more than two consecutive memory cycles, and will be held for two only on end-of-frame.

Updating of the FIFO output data is triggered by the FIFO timing lines, FT1 and FT2. These lines are always the inverse of each other and are toggled whenever FRQ is low (new data present) at the instant when the data clock (CK-DMA) goes high.

he address logic is driven by the address clock
:K-MAB). Whenever new data is written into mem-
:y, the DMA controller causes the next word position
›inter (NWP) to advance to the next address. If the
ıd of frame flag (DEOF) was present, then on the
:xt memory cycle the last frame position pointer
.FP) will be enabled for updating. The LFP will
ıus end up pointing to the start of the next line frame.
the error flag (DERR) is present, then the DMA con-
'oller will enable the NWP to backspace to the same
ıdress as the LFP. The erroneous line frame will
ıerefore be overwritten by the next line frame. This
:fectively deletes the erroneous line frame from
ıemory.

TATUS REPORT LOGIC

he status report logic monitors various internal MLIA
ignals and generates the MLIA status word. Bit zero
:TAT0) is controlled by the master reset line (RES)
nd the loop monitor error signal (ERRL*), originating
n the processor interface board. ERRL* goes low
henever either clock or data is interrupted on either
ıe input loop or output loop.

:it 3 (STAT3) is controlled by the three loopback
ıdicators (ILB*, OLB*, CLB*), the transparent mode
ıdicator (TPM), and the idle mode indicator (IDLE*).

:it 6 (STAT6) is turned on by either the output sync
rror signal (EP) or the output timeout signal (ERRW*).
'he latter signal originates on the processor interface
oard. Bit 6 is turned off by the status read signal
AQ-STA).

:it 5 (STAT5) is turned on by the buffer full signal
ERRB) and turned off by AQ-STA.

:it 9 (STAT9) is turned on by any one of three signals:
ıe input loop error signal (ERR-R) issued by the input
ıunch controller, the data demand malfunction flag
DDX) originating on the processor interface board,
nd the FIFO counter malfunction flag (FCX) also origi-
ating on the processor interface board. Bit 9 is turned
ff by AQ-STA.

'he logical OR of bits 5, 6, and 9 serves as bit 2 (STAT2)
nd as the error interrupt (INT-E) going to the processor.

'he status report logic also generates the line frame
nterrupt going to the processor (INT-LF). The inter-
upt is turned on whenever the last frame position point-
r is updated, as indicated by a short pulse on the LFP*
ine. The interrupt is turned off by the LFP read signal
AQ-LFP).

MASTER OSCILLATOR LOGIC

The master oscillator logic is the source of most of the timing and clock signals throughout the entire MLIA. The only clock signals that are not derived from the master oscillator logic, directly or indirectly, are the DMA channel clocks (CK-DMA, CK-MAB) and the A/Q channel clocks (SPT, CK-AQ*). The principal clock signals generated by the master oscillator logic are the 600-ns clocks (CP600, CP625, CP627), the 300-ns clocks (CP300, CP300A), the 50-ns clocks (CP50, CP50A), the 300-ns strobe (CP-STR), the 100-ns A/Q read clock (CK-AQR), and the twelfth bit marker (CP12, CP12A).

With the exception of CK-AQR, all of these clocks are free running (noninterruptable). Waveforms and phase relationships are shown on sheet 2 of the block diagram (74712300). CP50 is the main clock from which all the other clocks are derived. During card test, CP50 can be shut off by grounding clock inhibit 1 (CKINH1). A single 25-ns pulse can then be triggered by momentarily grounding clock inhibit 3 (CKINH3) and then momentarily grounding clock inhibit 2 (CKINH2). In the normal system installation, the three inhibit signals are left unconnected, thereby allowing CP50 and all the clocks derived from it to run continuously.

The A/Q read clock (CK-AQR) is used on the processor interface board to clock the holding register that interfaces the A/Q read data bus. Whenever an A/Q read operation is performed by the processor, the data to be read is loaded into the holding register. The read request signal (RDQ) then shuts off CK-AQR to prevent the register contents from being altered during the read operation. The data read by the processor will thus remain stable during the read, even if the source data changes. CK-AQR shut-off is delayed slightly if the last frame position pointer (LFP) happens to be changing at the same time as the read request signal (RDQ). The delay action is triggered by the LFP modify signal (LFPM) issued by the DMA controller. LFPM toggles (changes state) whenever the LFP is updated. Toggling of LFPM also triggers the LFP modify pulse (LFP*), which sets the line frame interrupt.

PROCESSOR INTERFACE LOGIC

Refer to figure 4-3 for a functional block diagram of the processor interface board. There are seven functional sections: parameter registers, output data demand controller, DMA address registers, input loop launch counter, data input counter, A/Q timing generator, output timer and loop monitor.

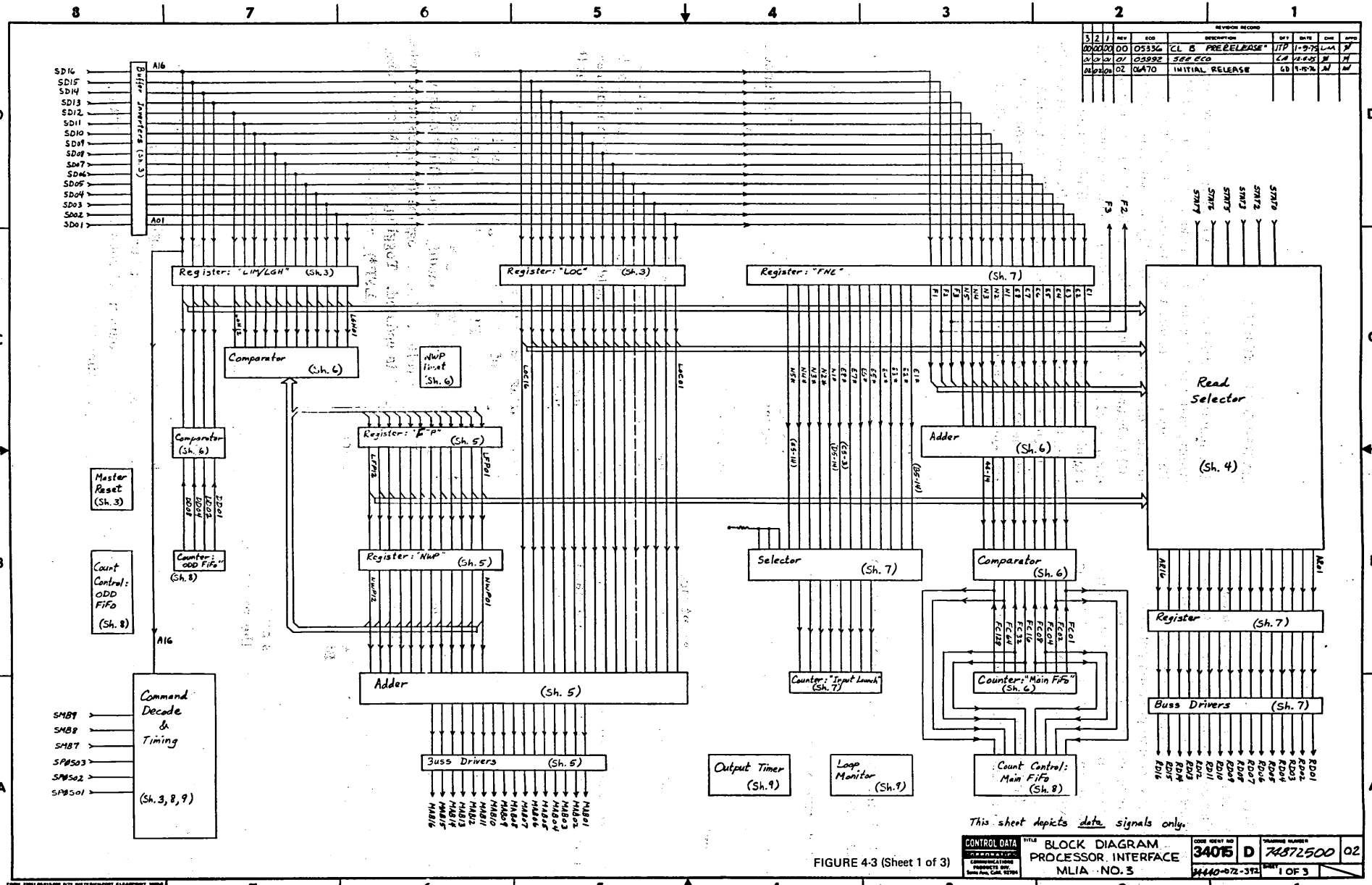


FIGURE 4-3 (Sheet 1 of 3)

REVISION RECORD								
3	2	1	REV	ECO	DESCRIPTION	BY	DATE	CHK
00	00	00	00	05336	CL B PRERELEASE*	JTP	1-9-75	LM
N/A	N/A	N/A	01	05992	SEE ECO	LA	12-8-75	M
00	00	00	02	06470	INITIAL RELEASE	GB	1-15-76	M

CONTROL DATA CORPORATION	TITLE BLOCK DIAGRAM PROCESSOR INTERFACE MLIA NO. 3	CODE IDENT NO 34015	D	DRAWING NUMBER 74872500	02
		84440-072-372		SHEET 1 OF 3	

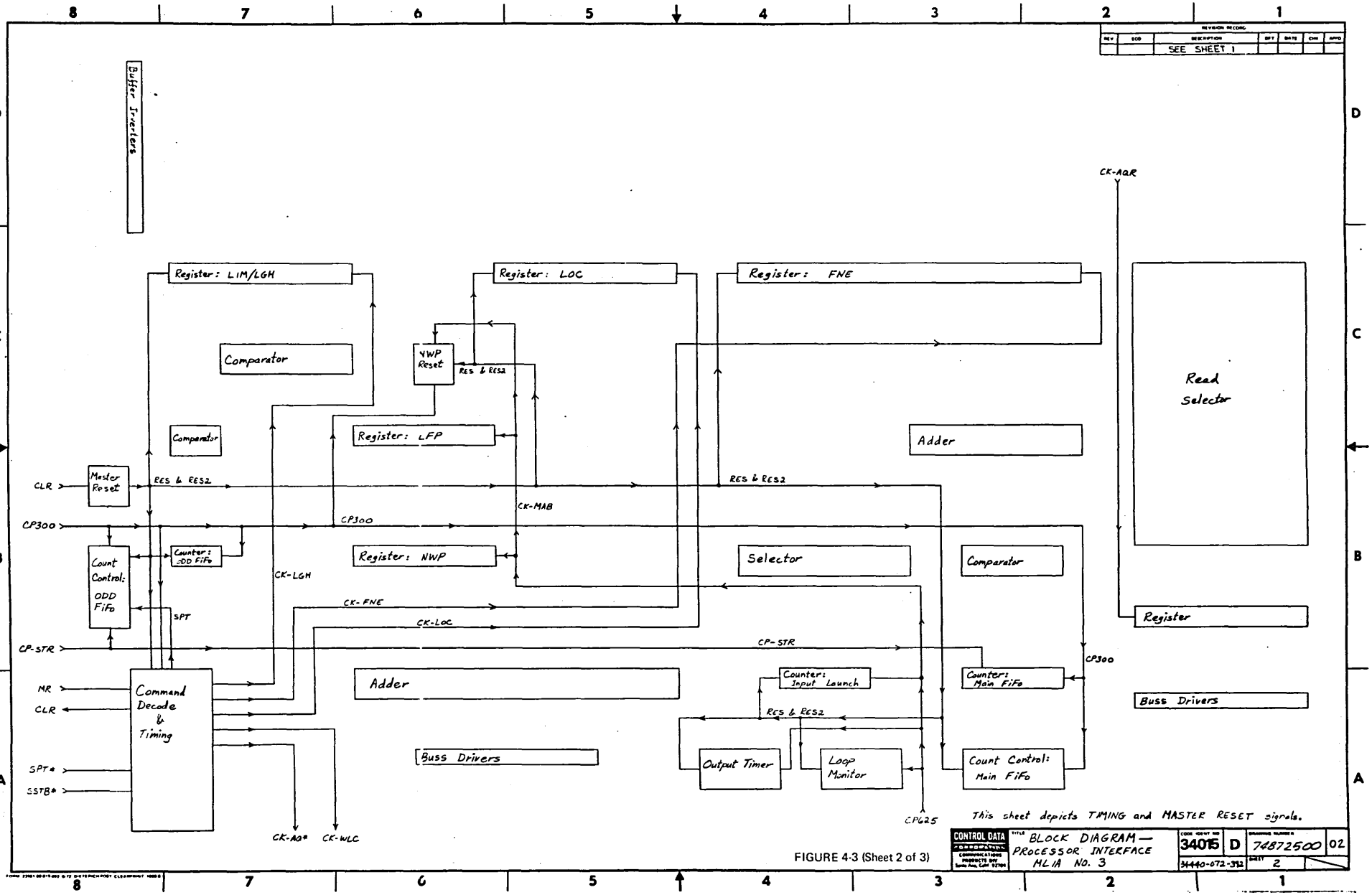


FIGURE 4-3 (Sheet 2 of 3)

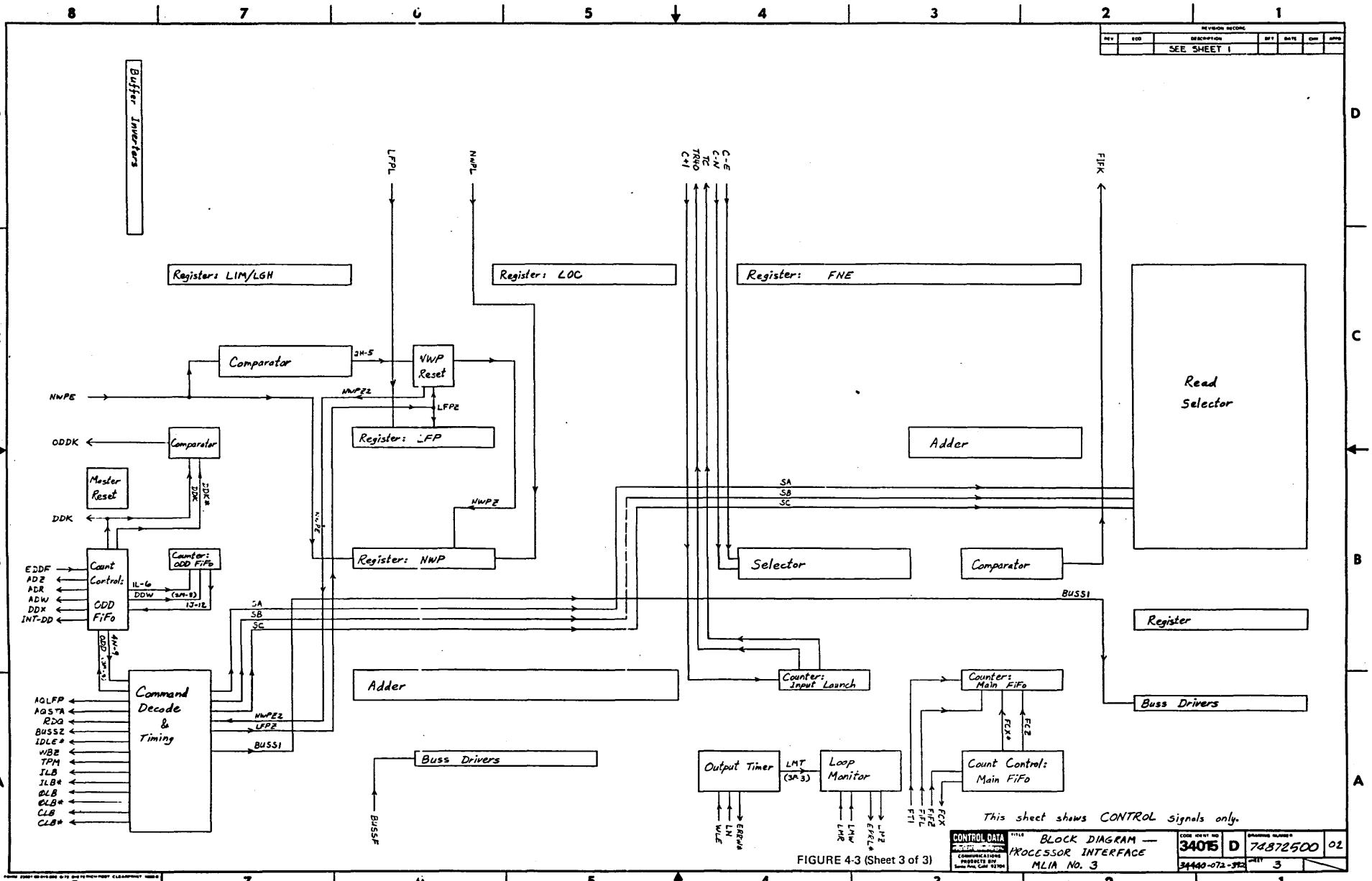


FIGURE 4-3 (Sheet 3 of 3)

CONTROL DATA	BLOCK DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3
CODE IDENT NO	34015
SIZE	D
DRAWING NUMBER	74872500 02
SHEET	3

Parameter Registers

There are three 16-bit registers which can be written and read directly by the processor: the limit and length register, the location register, and the flag-null-empty register. These registers obtain data from an internal 16-bit MLIA bus which interfaces the A/Q channel through a bank of inverters. Each register also furnishes its contents to the A/Q read selector.

Whenever one of the registers must be read, the A/Q read selector loads the content of the selected register into a holding register. The holding register content is then gaged onto the A/Q channel.

The A/Q read selector can also select MLIA status or the last frame position pointer (LFP) for reading by the processor.

Output Data Demand Controller

The upper four bits of the limit and length (LIM/LGH) register are continuously compared with the state of the output data demand (ODD) up-down counter. Whenever the counter state exceeds the limit specified in the LIM/LGH register, the ODDK signal is issued to the input launch controller located on the output loop interface board. This causes generation of loop batches on the input loop to be suspended until the ODD counter again equals or falls below the programmed limit.

The ODD counter, in turn, is controlled by the counter control logic. The counter increments whenever an output data demand is detected on the input loop interface board and signalled by the enable data demand FIFO line (EDDF). The counter decrements whenever an ODD read command is executed by the processor.

The control logic also decides:

1. When to turn on the ODD interrupt (INT-DD) and data demand clear (DDK) signals
2. When to increment or reset the ODD control counters located on the input loop interface board
3. When to issue the overflow error signal (DDX)
4. When to allow the next ODD read command to turn off the interrupt

DMA Address Registers

The lower twelve bits of the LIM/LGH register are continuously compared with the state of the next word position pointer (NWP). Whenever the NWP is equal to the programmed limit (LGH), then on the next cycle of the memory address clock (CK-MAB) the NWP will be reset to zero (NWPZ).

In addition to the automatic reset, NWP can also be incremented or inhibited or loaded from the last frame position register (LFP). Counting is controlled by the NWP enable line (NWPE) and loading is controlled by the NWP load line (NWPL). The LFP, in turn, can also be loaded from the NWP. This is controlled by the LFP load signal (LFPL). Finally, both NWP and LFP can be cleared by the LFP reset command (LFPZ).

Whenever a valid loop cell is written into memory by the DMA controller located on the output loop interface board, the controller causes the NWP to increment. After a complete line frame is written, the controller sets LFP equal to the incremented NWP. If the error flag is set, the controller sets NWP equal to LFP.

The output of the NWP is added to the contents of the location (LOC) register to form the absolute memory address.

Input Loop Launch Counter

The input loop launch counter is used to meter the number of empties and nulls to be sent on the input loop. It can be loaded from the lower eight bits of the flag-null-empty (FNE) register to set the number of empties, or it can be loaded from the middle five bits to set the number of nulls. It can also be set to zero to begin the input loop timeout interval.

Main FIFO Counter

The lower eight bits of the FNE register are added to the middle five bits and continuously compared with the state of another up-down counter. The counter indicates the amount of space available in the data input buffer located in the input loop interface board. Whenever a loop cell is loaded into the buffer, the counter decrements. Whenever a loop cell is removed from the buffer and written into memory, the counter increments. Whenever the buffer is empty, the FIFO zero signal (FIFZ) sets the counter to 131, indicating that there is sufficient space available in the buffer to accommodate a 131-cell loop batch. (The buffer itself is 128 words long, but every loop batch always contains at least three cells which are not loaded into the buffer: a loop end, one or more trailing nulls, and one or more cyclic redundancy check cells.) Whenever the count falls below the programmed limit (N+E), the FIFO "OK" signal (FIFK) goes low, causing generation of new input loop batches to be suspended. If the count ever falls below

three or rises above 131, an error is reported (FCX) and the counter is held equal to zero until the buffer is empty (FIFZ).

A/Q Timing Generator

A/Q timing is determined by the port enable (SPT*) and A/Q strobe (SSTB*) signals. The A/Q operation to be performed is selected by the mode and position lines (SMB9, SMB8, SMB7, SPOS03, SPOS02, SPOS01). If the LIM/LGH register is to be written, its clock (CK-LGH) is activated during the A/Q cycle. Similarly, clocks CF-FNE, CK-LOC, or CK-WLC are activated for a write FNE, write LOC, or write output loop cell, respectively.

The A/Q timing generator also issues the loopback flags (ILB, OLB, CLB), the transparent and idle mode flags (TPM, ILDE*), and output buffer reset control (WBZ).

A/Q read commands are executed by selecting the appropriate source (SA, SB, SC) and issuing the read request signal (RDQ) to shut off the holding register clock (CK-AQR). Another clock signal (CK-AQ*) is used in conjunction with the status (AQSTA) and LFP (AQLFP) controls to reset status or reset the line frame interrupt whenever the corresponding A/Q command is executed.

Each of the three MLIA boards has two master clear signals (CLR). One signal is an input to the board; the other is an output. On the input and output loop interface boards, the CLR input directly feeds the CLR output. A high logic level occurring on the CLR input causes a high level on the CLR output; it also resets the board.

On the processor interface board, the CLR input operates in the same way as on the other two boards. A high level resets the board and forces a high level on the CLR output. But on the processor interface board, the CLR input is not directly connected to the CLR output. Instead, the CLR output is driven by the A/Q timing generator. The CLR output can be forced high by a reset command or by a low on the master reset (MR) line as well as by a high on the CLR input. If no forcing condition is present and an idle or normal command is executed, then the CLR output will go low.

The CLR output of each MLIA board is wired through the backpanel to the CLR input of the next board in a closed serial loop. In order for the CLR input to the processor interface to be low (not reset), there must be a low on the CLR output which passes through each MLIA board and finally returns to the CLR input on the processor interface board. Removal of any MLIA board thus causes a high level on the CLR inputs of all other boards. When the missing board is re-inserted, the CLR line will remain high until an idle or normal command is executed by the processor.

On the output loop interface board, CLR drives the MLIA RUNNING indicator light. The light goes on whenever the CLR line is low (MLIA not reset).

Output Timer and Loop Monitor

The output timer consists of a counter which gets initialized whenever a loop end cell is sent on the output loop. This is signalled by the loop end write line (WLE) originating in the output launch controller on the output loop interface board. If the counter advances by 40 counts (one count for each loop cell sent) before the loop end returns, a malfunction is inferred and an error is reported (ERRW*) to the status report logic on the output loop interface board. If the loop end returns, the loop-end-in (LN) signal will inform the output timer control logic, which will then ignore the counter until another loop end goes out (WLE). The counter itself will continue to count.

If the cascade loopback is set, no loop ends will be generated automatically and no WLE signals will be issued. Thus, in cascade loopback the output timer is effectively disabled.

The same counter is also used by the loop monitor. On every fourth count, the loop monitor timeout line (LMT) signals the loop monitor to sample the states of the input loop monitor signal (LMR) and output loop monitor signal (LMW). If either signal indicates loss of data or clock on the respective loop, the monitor reports an error (ERRL*) to the status report logic on the output loop interface board.

Whether an error is reported or not, the monitor also issues the monitor reset signal (LMZ) to reset the activity indicators (LMR and LMW). Once reset, the activity indicators remain reset until transitions are detected on both the loop data and clock. Once set, LMR and LMW remain set until cleared by LMZ. Since LMR and LMW are sampled once every four cell times (LMT), data and clock transitions must occur on both loops within that period, or an error will be reported.

LMR originates in the receive selector on the input loop interface board. It also drives the INPUT ON indicator light on the output loop interface board. LMW originates in the receive selector (loopback switch) on the output loop interface board, where it also drives the OUTPUT ON indicator light.

MULTIPLEX SUBSYSTEM

Loop Multiplexer

The loop multiplexer theory of operation is divided into two parts: a description of the output section and a description of the input section. A glossary of signal mnemonics and terms (table 4-1) defines the function of the signals associated with the loop multiplexer.

OUTPUT SECTION

A block diagram of the output section is shown in figure 4-4. The output section passes information from the high-speed (20 MHZ nom) serial loop to the communications line adapters (CLAs) in a manner that will minimize interchange with the information passed on to the other multiplexers and the CLAs. Each function of the output section is assigned a separate functional block, and coordination and operation of these blocks are accomplished by the register control. The output section always operates in a fixed sequence and is designed to place itself in a condition of minimum interface activity when external or internal errors occur. The function of each block will be described as required to explain the following sequence of operations. Figure 4-5 is a general timing diagram for the output section of the loop multiplexer.

Selection

When the output loop multiplexer senses an address code in its shift register, it initiates the output selection process. The address is placed on the output bus along with a select signal to all CLAs in the loop multiplexer cage. The CLA with the same address as that presented, connects itself to the bus and is prepared to accept 11-bit bytes from the LM. These bytes are identical to the information contained in the loop cells. All subsequent non-CRC cells are presented to the CLA. Selection is terminated when the CRC code is detected. At this time select-clear signal is sent to all CLAs in the LM cage. The output section accumulates a cyclic redundancy check character for every line frame beginning with the first bit of the address cell and ending with bit 3 of the CRC cell. The polynomial for the CRC is $X^8 + X^7 + X^6 + X + 1$.

Output Shift Register

The output shift register dynamically stores and decodes bit patterns from the serial data stream. It consists of a clock and data receiver, 12-bit shift register, decode networks, and a clock and data driver. All information received from the output serial data stream is passed on, with a reconstituted clock signal, unaltered (except for a 1.5 ms delay), to the next element (LM or MLIA) in the serial data stream. Five decode gates are used to sense the presence of empty, address, or CRC cells, which, in turn, are used to enable and/or control the counter and the register control logic. All data strobed to the output bus originates from the shift register. The clock regeneration circuit guarantees that the falling edge of OCT* occurs 20 to 30 ns after the rising edge of OCT*; in other words, OCT* is active at the data bit center ±5 ns.

Counter

The counter is implemented as a ring counter and is composed of a 12-bit shift register. This circuitry provides the timing for the control of the output section. The counter is resynchronized every time an empty cell is decoded by the output shift register. The C0 flip-flop is set with the decode of empty cells on the rising edge of clock and is reset 10 to 25 msec after a four-gate delay. This pulse from the output of C0 flip-flop resets the three registers that make up the counter, leaving a single bit at C0 to circulate.

CRC Checker

The CRC checker is composed of two D-type registers and four exclusive OR elements. When the address format at time C3 is decoded, the Accum CRC flip-flop is set, releasing the CRC checker to accumulate. The CRC checker, until this time, is loaded with zeros. The input to the CRC checker comes from bit 7 (B7) of the output shift register; thus the first bit of data accumulated is the first bit of the address cell. Accumulation continues until CRC format at time C7 is decoded from the output shift register. At this time the test CRC flip-flop is set, allowing the accumulated CRC to be compared with the 8-bit expected CRC. During this test operation, the input to the checker is forced low by the test CRC flip-flop so that zeros are shifted into the CRC's checker. Comparison is done two bits at a time, taking four bit times to check the 8-bit CRC. B7 of the output shift register is compared with the first four bits of the CRC checker and B11 with the second four bits using exclusive OR elements. If a miscomparison is detected, the CRC error flip-flop sets. When CRC format is decoded from the output shift register, the test CRC flip-flop is reset. After one bit time the Accum CRC flip-flop is reset, which in turn resets the CRC checker.

Buffer Register

The buffer register is an 11-bit D-type register, whose D-inputs tap off of the output shift register. It is clocked every cell time as long as the counter is synchronized with the serial data stream. The buffer clock is produced by

TABLE 4-1. LOOP MULTIPLEXER GLOSSARY OF MNEMONICS

Mnemonic	Definition
A	Bit A (Input Select States Register)
A'	Bit A' (Input CRC States Register)
A''	Bit A'' (Input Restart States Register)
A0	A Encode - Group 0
A1	A Encode - Group 1
A2	A Encode - Group 2
A3	A Encode - Group 3
ADD	Address Formal Decode
B	Bit B (Input Select States Register)
B'	Bit B' (Input CRC States Register)
B''	Bit B'' (Input Restart States Register)
B0	B Encode - Group 0
B1	B Encode - Group 1
B2	B Encode - Group 2
B3	B Encode - Group 3
B0 thru B11	Output Shift Register Bit 0 thru Bit 11
BCK	Buffer Clock
BRST	Buffer Reset
C'	Bit C' (Input Select States Register)
C''	Bit C'' (Restart States Register)
C0	C Encode - Group 0
C1	C Encode - Group 1
C2	C Encode - Group 2
C3	C Encode - Group 3
C0 thru C11	Output Counter Time 0 thru Time 11
CLACR	CLA Clear
CLASL	CLA Select
END	End (Select State)
ENP1	Enable Priority Encode 1
ENP2	Enable Priority Encode 2
ENP3	Enable Priority Encode 3
ERR	Error (Output Loop)

TABLE 4-1. LOOP MULTIPLEXER GLOSSARY OF MNEMONICS (Contd)

Mnemonic	Definition
F1	Format Bit 1 (Input)
F3	Format Bit 3 (Input)
IAV1 thru IAV32	Input Available Bit 1 thru Bit 32
IAVLD	Input Available Load
ICKA	Input Clock A
ICKA1	Input Clock A1
ICKA2	Input Clock A2
ICKA3	Input Clock A3
ICKB	Input Clock B
ICKC	Input Clock C
ICKIND	Input Clock Indicator
ICR	Input Clock Receive
ICRCS	Input Cyclic Redundancy Checksum
ICRCSEN	Input Cyclic Redundancy Checksum Enable
ICRGD	Input Clock Receive Ground
ICT	Input Clock Transmit
ICTGD	Input Clock Transmit Ground
IDIND	Input Data Indicator
IDR	Input Data Receive
IDRGD	Input Data Receive Ground
IDT	Input Data Transmit
IDTGD	Input Data Transmit Ground
IEC	Input Empty Cell
IEN	Input End
IENF	Input End (Stored)
IER	Input Error
IF1 thru IF3	Input Format Bit 1 thru Bit 3
IF1F thru IF3F	Input Format Bit 1 thru Bit 3 (Stored)
IFREN	Input Frame End
II1 thru II8	Information Input Bit 1 thru Bit 8

TABLE 4-1. LOOP MULTIPLEXER GLOSSARY OF MNEMONICS (Contd)

Mnemonic	Definition
II1F thru II8F	Information Input Bit 1 thru Bit 8 (Stored)
IM	Inhibit Master Reset
INAV	Input Available
IO1 thru IO8	Information Output Bit 1 thru Bit 8
IOVFL	Input Overflow
IST	Input Strobe
LCLA	Last CLA
LE	Loop End
LOAD	Load (an Input Select state)
M1	Master Clear Control 1
M2	Master Clear Control 2
M3	Master Clear Control 3
MCL	Master Clear
OCKIND	Output Clock Indicator
OCLK	Output Clock
OCR	Output Clock Receive
OCRCS	Output Cyclic Redundancy Checksum
OCRGD	Output Clock Receive Ground
OCT	Output Clock Transmit
OCTGD	Output Clock Transmit Ground
OD1	Output Disable 1
OD2	Output Disable 2
ODIND	Output Data Indicator
ODR	Output Data Receive
ODRGD	Output Data Receive Ground
ODT	Output Data Transmit
ODTGD	Output Data Transmit Ground
OER	Output Error
OF1 thru OF3	Output Format Bit 1 thru Bit 3
OOVFL	Output Overflow
OSC	Output Select Clear

TABLE 4-1. LOOP MULTIPLEXER GLOSSARY OF MNEMONICS (Contd)

Mnemonic	Definition
OSEL	Output Select
OSL	Output Select
OST	Output Strobe
OUTCLK	Output Clock
P1 thru P32	Priority 1 thru Priority 32
PCK	Priority Clock
PCKEN	Priority Clock Enable
PE0 thru PE3	Priority Encode 0 thru Priority Encode 3
PLUS	Plus (Pull-up)
PLUS1 thru PLUS3	Plus 1 (Pull-up) thru Plus 3 (Pull-up)
REND	Restart End
RES	Restart
RESLD	Restart Load
RF1	Reference Frequency 1
RF2	Reference Frequency 2
RF3	Reference Frequency 3
RLE	Restart Loop End
RSTIN	Reset Input
RORST	Redundant Output Reset
RSTOUT	Reset Output
S1 thru S32	Select 1 thru Select 32
SEN	Secondary Enable
SLA	Select Encode A
SLB	Select Encode B
SLC	Select Encode C
SLD0	Select Enable 0
SLD1	Select Enable 1
SLD2	Select Enable 2
SLD3	Select Enable 3

TABLE 4-1. LOOP MULTIPLEXER GLOSSARY OF MNEMONICS (Contd)

Mnemonic	Definition
SP1 thru SP32	Set Priority 1 thru Set Priority 32
SYNC	Sync (a Select State)
T1 thru T12	Time 1 thru Time 12 (Input Counter)

the buffer clock flip-flop. This flip-flop is clocked by the clock regeneration circuit 20 to 30 nsec after the rising edge of CLOCK. The flip-flop sets during C11 and resets one bit time later.

Error Control

There are three error conditions that the output LM is sensitive to: CRC error, loss of sync bit (M-bit) in the serial data stream, and overflow (more than 15 cells presented to CLA). For each of these conditions, an error flag (OER) is brought TRUE on the output bus, informing the selected CLA of the error condition.

1. CRC Error: When a CRC error is detected by the CRC checker (between time C8 and C0) the CRC error flip-flop is set. It resets at C0 (one bit time after test CRC TEST resets). If a CRC error has been detected, the ERROR flip-flop sets at C0, raising OER flag.

2. Loss of Sync: If B0 is not a logic one at C11, the error flip-flop sets,

3. Overflow: Each time that a cell is presented to the CLA, a 4-bit binary counter is incremented (clocked at C9). Initially the count value is zero. After 15 cells have been presented, the overflow (carry-out) comes true and remains for one cell time. At C11 the error flip-flop sets.

The error control section is only operative during the selection of a CLA. Only one CLA can detect any particular error flag.

Sequence of Operations

After the initialization of the CRC checker (at ADD 0 · C3) eight bit-times later, ADD 0 · C11 is decoded off of the output shift register. This signal sets both the Select and CLASEL flip-flops. Select enables the error control section and the connection of CLACR, CLASEL, ERROR, and the buffer register to the output bus. At this time the address cell, having already been locked into the buffer register by the buffer clock, is put on the bus along with OSL* (produced by CLASEL). At leading edge of C1 the output strobe latch is set and then reset at leading edge of C7, making OST* a 50% duty cycle signal. The output strobe latch will continue to toggle as long as the counter is operating. While address is on the bus and on the rising edge of OST*, the output section of the CLA with this unique address, will be selected. The CLA will now be in a state where it will accept any further information from the LM, i.e., data or commands.

CLASEL will reset at C11 making OSL inactive. All subsequent non-CRC cells are placed on the bus along with OST*. The bus signals will change with the rising edge of the buffer clock (in the center of C11). This process will continue until one of three things happens: A CRC format code is detected, more than 15 cells have been strobed to the CLA, or a loss of sync bit. In any case, OSC* will go true at C11 and remain until the next C11. The CLA disconnects itself from the bus on the trailing edge of strobe providing OSC* is active. In normal operation (no error conditions) CLACR is produced by the SEL CLR flip-flop. It is clocked with C11* and is set when CRC · C11 is decoded - resets on the next C11*. Under all error conditions, the CLA is deselected (OSC*), since CLACR in this instance is derived from the error flip-flop.

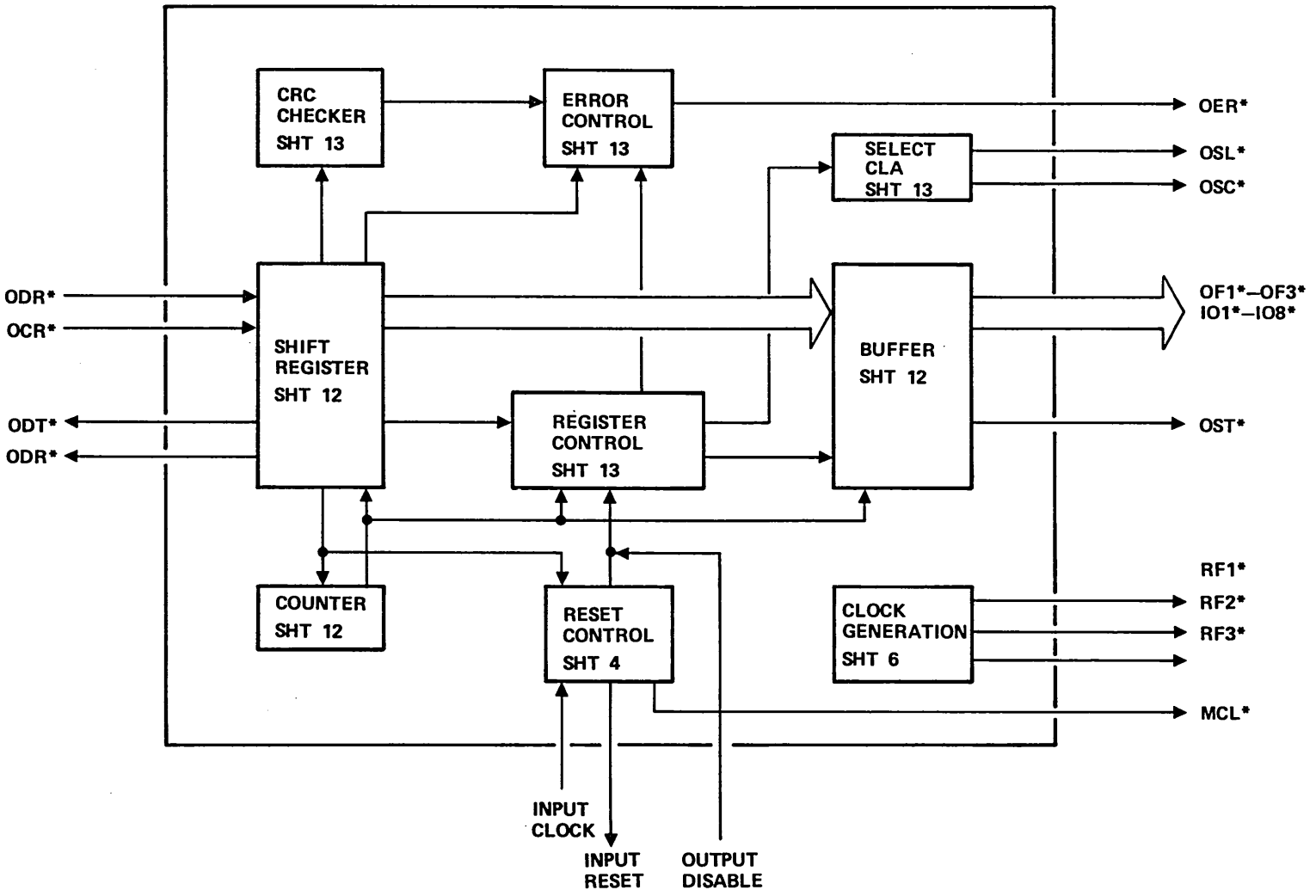


Figure 4-4. Loop Multiplexer - Output Section

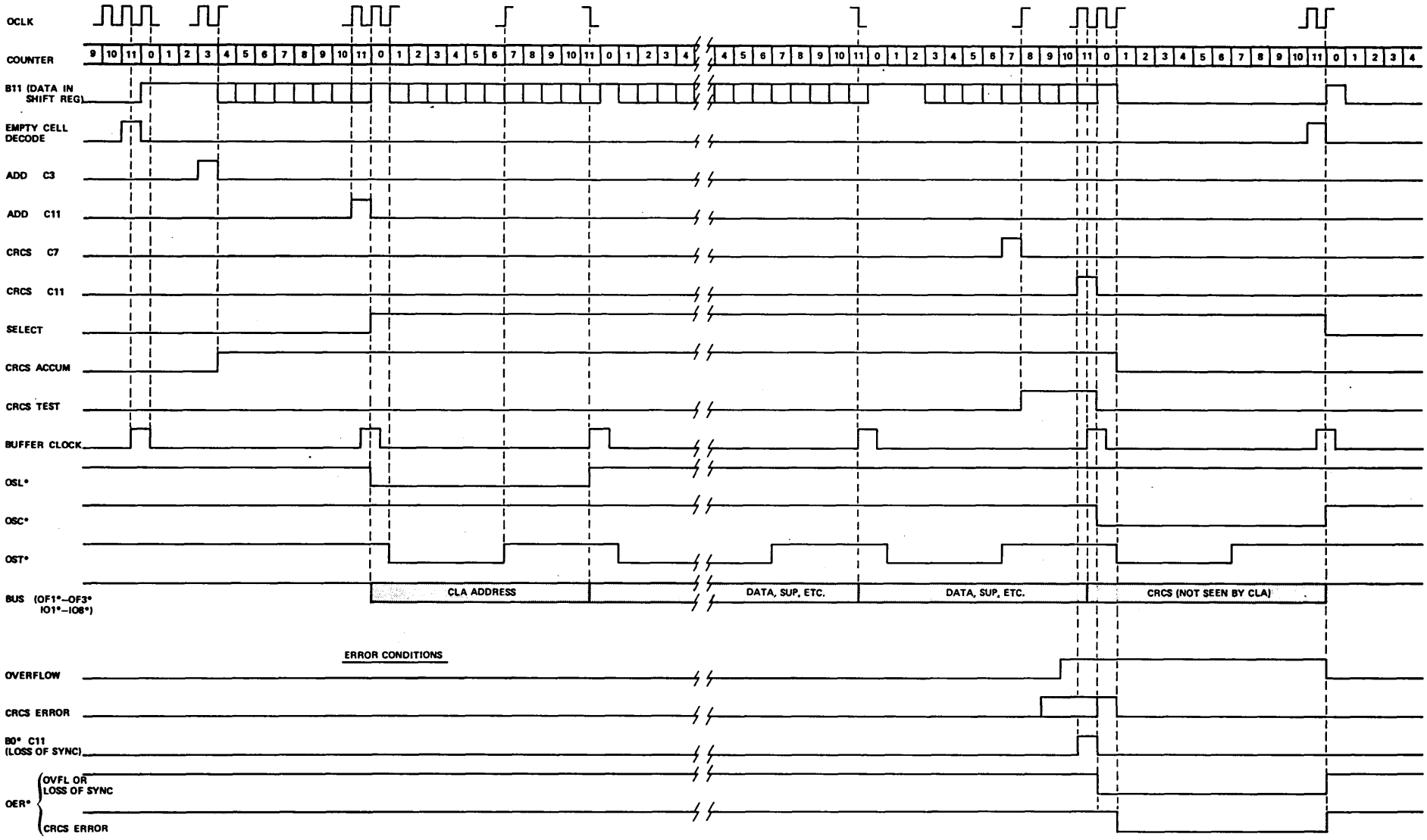


Figure 4-5. Loop Multiplexer Output Timing

Reset Control

Both the input and output section of the LM will eventually end up in an idle condition as long as empty cells or any cells with an unused format are received on their respective loops. Also, the input section will be reset to an idle state when the input loop clock is not received for more than 30 μs. Likewise, the output section will be reset to an idle condition when the output loop clock is absent for more than 30 μs. All CLAs in the LM will be master cleared (MCL*) when check signals are not received for more than 30 μs, on both the input and output loops. When two loop multiplexers are present in a redundant configuration, the CLAs will be master cleared only when both the primary and secondary input and output clocks are not present for more than 30 μs. (See Redundant Operation.) The reset control section is implemented using retriggerable monostable multivibrators (one-shots), one for the input section and one for the output section, each being triggered by its respective clock.

Under reset conditions, in the output section the SELECT and CLASEL flip-flops are directly cleared, in the input section all "STATES" elements are directly reset. These one-shots are also used for a power-up reset lasting for approximately 1 msec. Output and input sections and CLAs are reset when power is applied to the LM.

Clock Generation

The clock generator supplies three bused, square wave, reference clock signals to all CLAs in the LM cage. They are RF1 = 4.8 kHz, RF2 = 19.2 kHz, and RF3 = 153.6 kHz. There is also a fourth clock bus to all CLAs designated RF4, which is to be an optional frequency. The clock generator consists of a crystal-controlled gate oscillator and a four-stage binary counter. The generator is enabled only after the input loop multiplexer has received valid loop ends on the input loop, and disabled when the LMUX is inactive in a redundant configuration (see Redundant Operation).

INPUT SECTION

The input section of the loop multiplexer passes information from communications line adapters (CLAs) via a high-speed (20 mHz nom) serial data stream through the MLIA to the processor. Information from the CLAs is given to the input section in 11-bit bytes: three bits of format code and eight bits of address, data, or supervision, as detailed in the functional description. A block diagram of the input section is shown in figure 4-6. Each function of the input section is assigned a separate block and the following description is keyed to those blocks.

There are three basic modes of operation for the input section. The first is the normal or select mode, where a loop end followed by one or more empty cells is received on the input loop, initiating information transference from the CLAs. The second is the restart or error mode, where a restart loop end followed by at least one empty cell is received causing input loop error to be reported to each CLA that used the preceding loop batch. The third is the idle mode, where all data received on the loop is retransmitted back onto it, unaltered.

Input Shift Register

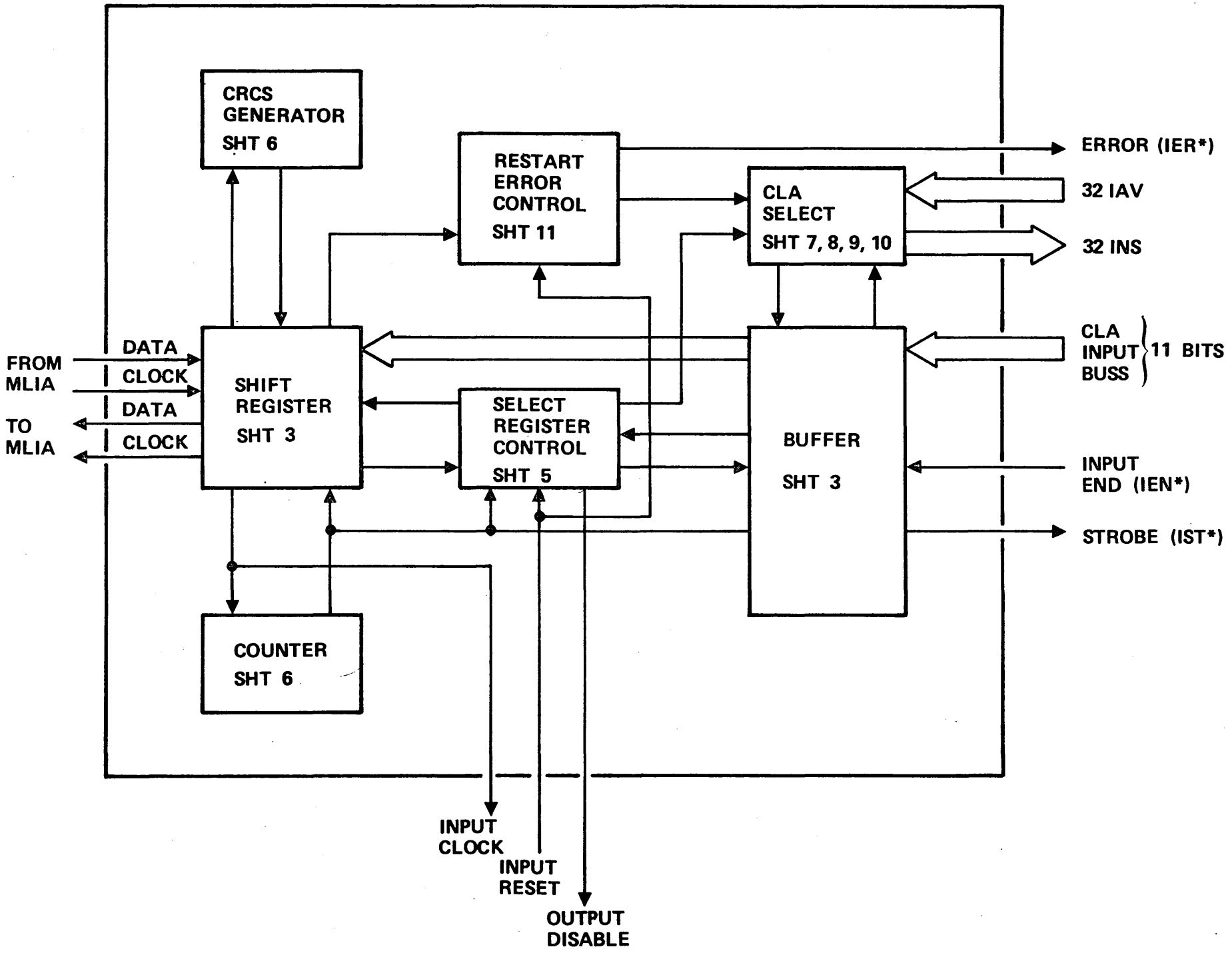
The shift register dynamically stores bit patterns from the serial data stream, which in turn, triggers off certain events in the select and restart control sections. It consists of clock and data receivers, clock and data drivers, a 25-bit shift register, decode gates for loop end, restart loop end, an empty cell, and a multiplexer that parallel loads information from the CLAs into the shift register.

The input shift register is divided into two sections: bits DSR0 through DSR11, and bits DSR12 through DSR23. During the select mode or restart mode the respective loop end or restart loop end is recirculated in shift register elements DSR0 through DSR11, to be released onto the loop at the end of the respective mode. Elements DSR12 through DSR23 are parallel loaded, via the multiplexer, with information from the CLAs during the select mode. When in the idle mode, the two sections DSR0 through DSR25 are strung together, so that all loop information entering the input loop multiplexer is passed on to the loop with 26-1/2 bits of delay.

All decodes are used one bit before the transition into select or restart mode. Therefore, empty cell is decoded from the element between DSR13 and DSR24, and loop end and restart loop end are decoded from the elements between DSR1 and DSR12.

Counter

The counter is implemented as a ring counter and is basically a 12-bit shift register. It provides the control timing for the input section while in the select or restart modes. It is held reset at time T12, until the beginning of the restart or select mode, at which time it is released, shifting T12 to T1 to T2, etc., on the rising edge of the received loop clock. The counter is again reset at the end of either mode.


CRCS GENERATOR SHT 6
RESTART ERROR CONTROL SHT 11
CLA SELECT SHT 7, 8, 9, 10
ERROR (IER*)
32 IAV
32 INS
CLA INPUT BUSS
11 BITS
FROM MLIA
DATA
CLOCK
TO MLIA
DATA
CLOCK
SHIFT REGISTER SHT 3
SELECT REGISTER CONTROL SHT 5
BUFFER SHT 3
INPUT END (IEN*)
STROBE (IST*)
COUNTER SHT 6
INPUT CLOCK
INPUT RESET
OUTPUT DISABLE

CRC Generator

The CRC generator is composed of two D-type registers and an exclusive OR element. It is controlled by the CRC states register. The polynomial used is the same as in the output section, namely, $X^8 + X^7 + X^6 + X + 1$. The CRC is accumulated for, and appended to the end of every input line frame. Accumulation begins with the first word given to the LM from the CLA (address cell) and ends with the fourth format bit of the CRC cell. Bits are serially inputted to the generator at frame input during accumulation. After accumulation and while outputting the CRC, zeros are fed into the generator. The generator only functions when in the select mode and remains in a reset state at all other times.

Buffer

The buffer is composed of three D-type registers which provide the parallel interface to the CLA to LM bus. This register is loaded one bit time before the rising edge of IST*. The bus signals loaded into it are IF1* - IF3*, II1* - II8* and IEN*. IST* falls at T6 and rises at T12 making it a 50% duty cycle signal.

CLA Select

The CLA select logic is responsible for storing all of the IAVs, resolving the selection priority, and selecting the input section of each CLA. It is under the control of the select register control section when in the select mode and controlled by the restart error control section when in the restart mode. The CLA select logic is composed of four identical subsections, one of which is shown in figure 4-7.

Referring to figure 4-7, IAVs *9 thru 16 are signals from the respective CLAs informing the input LM that they have information to be put on the input loop. Assume for the moment, that all of these IAVs are active (low). At the beginning of the select mode, the D registers used for the storing of IAVs are clocked with IAV clock. One bit-time later, IAV LOAD comes true enabling the three-state outputs of the IAV registers. Since all of the IAVs are "active low" at these outputs, the $\overline{S}$ - $\overline{R}$ latches are brought to a reset state, making the latch outputs "low." IAV load lasts for only one bit-time. The latch outputs are fed to an octal priority encoder. Cascading input ENPE1 and output ENPE2 are used to link the higher and lower priority encoders. PE1 is active when ENPE1 is active and at least one input is active. In this case, ENPE1 and all inputs are active. "7" having the highest priority is encoded causing all outputs to be active (including PE1). These are then inverted and clocked into a D register with priority clock. The $\overline{Q}$ outputs of this register are applied to the inputs of a 1 of 10 decoder. PE1 along with PE0, PE2 and PE3 of the other priority encoders are also inverted and clocked into the trailing edge of priority clock. The $\overline{Q}$ associated with PE1, SLD1, is applied to the MSB input of the decoder enabling the 0-7 outputs, and since at this time the other inputs to the decoder are also "low," bit zero of the decoder goes "low," causing IS9* to go "low." The "active low" output from the decoder feeds back to the $\overline{S}$ and $\overline{R}$ latch and "sets" it, causing its output to go "high." IS9* goes high when the SLD register is reset by the select control logic, since at this time the MSB to the decoder goes "high," disabling outputs 0-7, terminating the selection of that CLA. Now, "6" of the priority encoder is the highest priority. Its octal code will be present on the outputs of the encoder, which will be clocked into the register at T3, causing IS10* to fall. Thus, this selection process will continue in the above manner until the select control logic leaves the select mode by having selected all CLAs whose IAVs were stored during that selection cycle or having received a nonempty cell on the input loop.

In the restart mode, selection is handled exactly the same way except that the IAV register is not clocked.

Select Control

The select register control logic coordinates the functioning of the input shift register, buffer, CRC generator, and CLA select logic during the select mode. It can be expressed in terms of a pair of double-bit states registers. A diagram of the sync states is shown in figure 4-8. Figure 4-9 represents the CRC states. A timing diagram (figure 4-10) shows the key signals used during a select cycle and their relationship to each other. Three states registers are also depicted in this diagram: SELECT states, CRC states, and restart states.

The select control is best described by going step-by-step through a typical select cycle. In this case, the input loop multiplexer is in an idle mode with one IAV active. The select states register is in state "0" (idle). The CRC states register is also at state "0" (format). Now, a loop end followed by an empty cell is received by the input shift register and is decoded. If no CLA IAVs were active, the loop end and empty cell would pass through the shift register and back onto the loop. But, an IAV is active. It is ORed together with the other 31 IAV signals to bring input avail true. This resulting signal enables the loop end and empty cell decode to be seen by the select states.

The select states will switch to state "1" on the next rising edge of clock. At this time, SYNC is active and will remain until the end of the select cycle at select state "0". In select state "1", the counter is allowed to start, and DSR0 of the input shift register is gated back

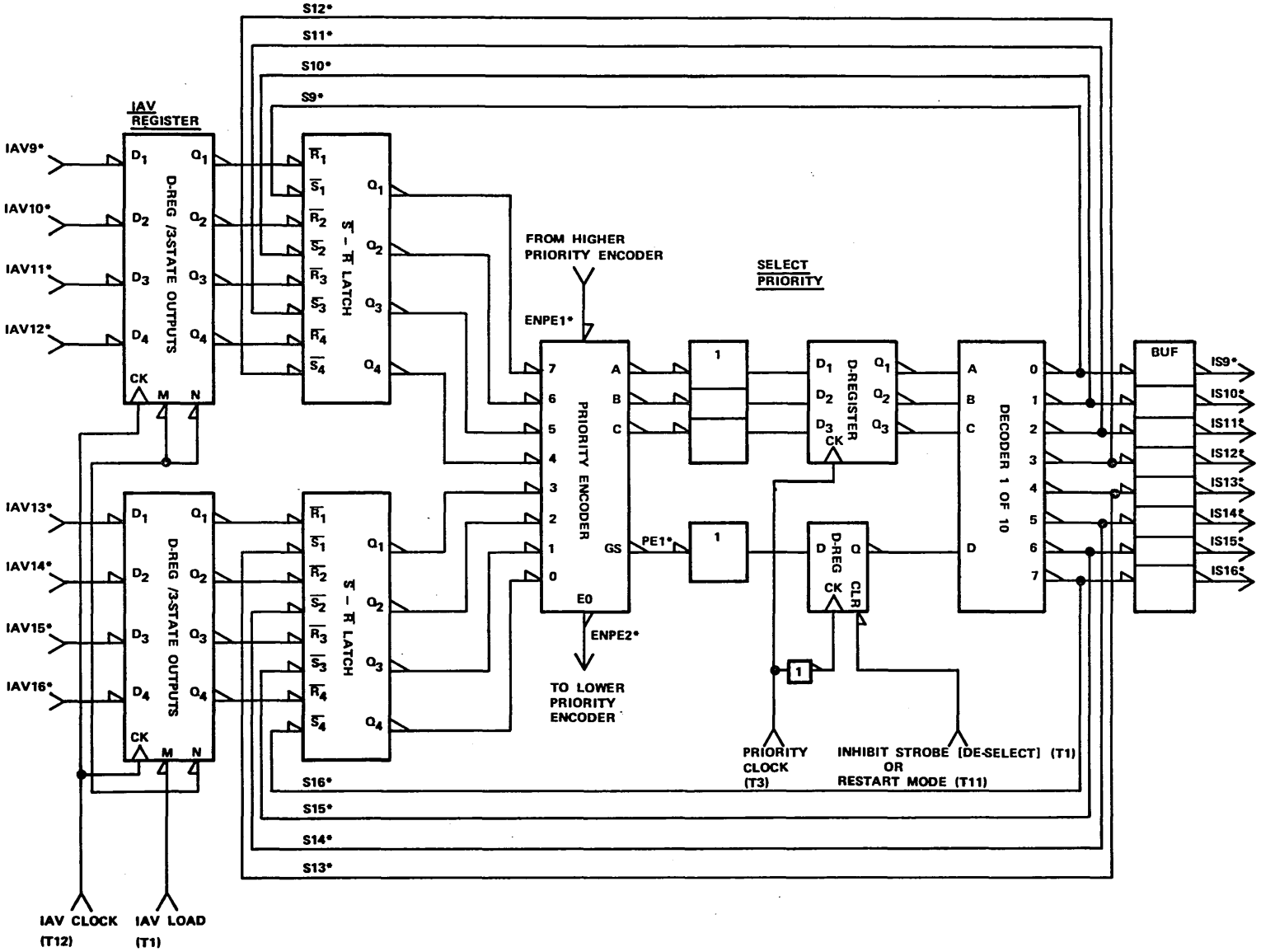
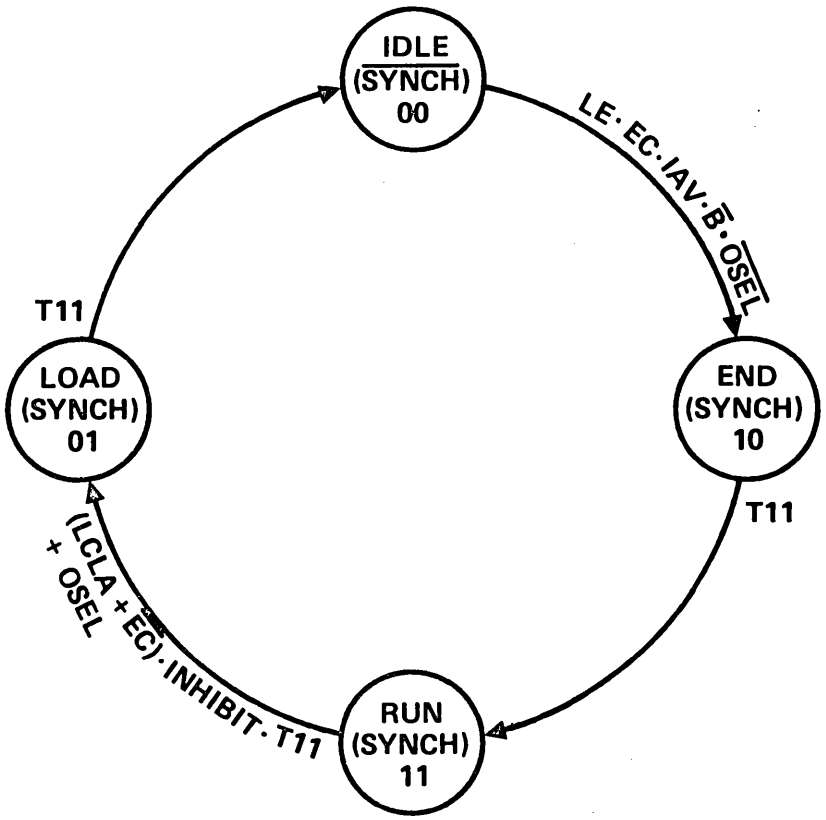


Figure 4-7. CLA Select Logic



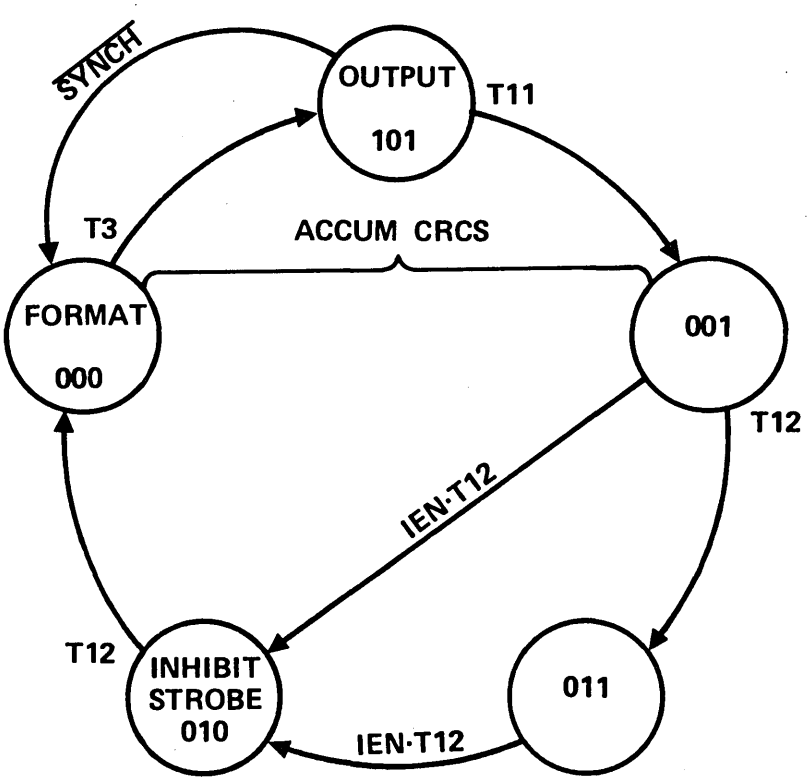
IDLE – NO LOOP BATCHES RECEIVED OR NO IAVs ACTIVE. INPUT LOOP MULTIPLEXER INACTIVE.

LOAD – THE START OF THE SELECT CYCLE. IAVs ARE STORED IN THE CLA SELECT LOGIC.

RUN – CLAs ARE SELECTED AND THEIR INFORMATION IS PUT ON THE LOOP.

END – THE END OF THE SELECT CYCLE – EITHER ALL CLAs HAVE BEEN SELECTED OR A NON-EMPTY CELL WAS RECEIVED ON THE LOOP.

Figure 4-8. Input Loop Multiplexer Select States (B-A)



FORMAT (000) – CRCS FORMAT CODE IS OUTPUTTED. PRIORITY CLOCK ENABLED IF SELECT STATE 1 OR 3 IS ACTIVE.

OUTPUT (101) – CRCS OUTPUTTED TO THE LOOP.

ACCUM CRCS (001) (011) (010) (000) – CRCS IS ASSEMBLED BY THE CRCS GENERATOR IN THESE FOUR STATES.

INHIBIT STROBE (010) – IST INHIBITED, LAST FRAME FROM CLA JUST RECEIVED.

Figure 4-9. Input Loop Multiplexer CRCS States (C'-B'-A')

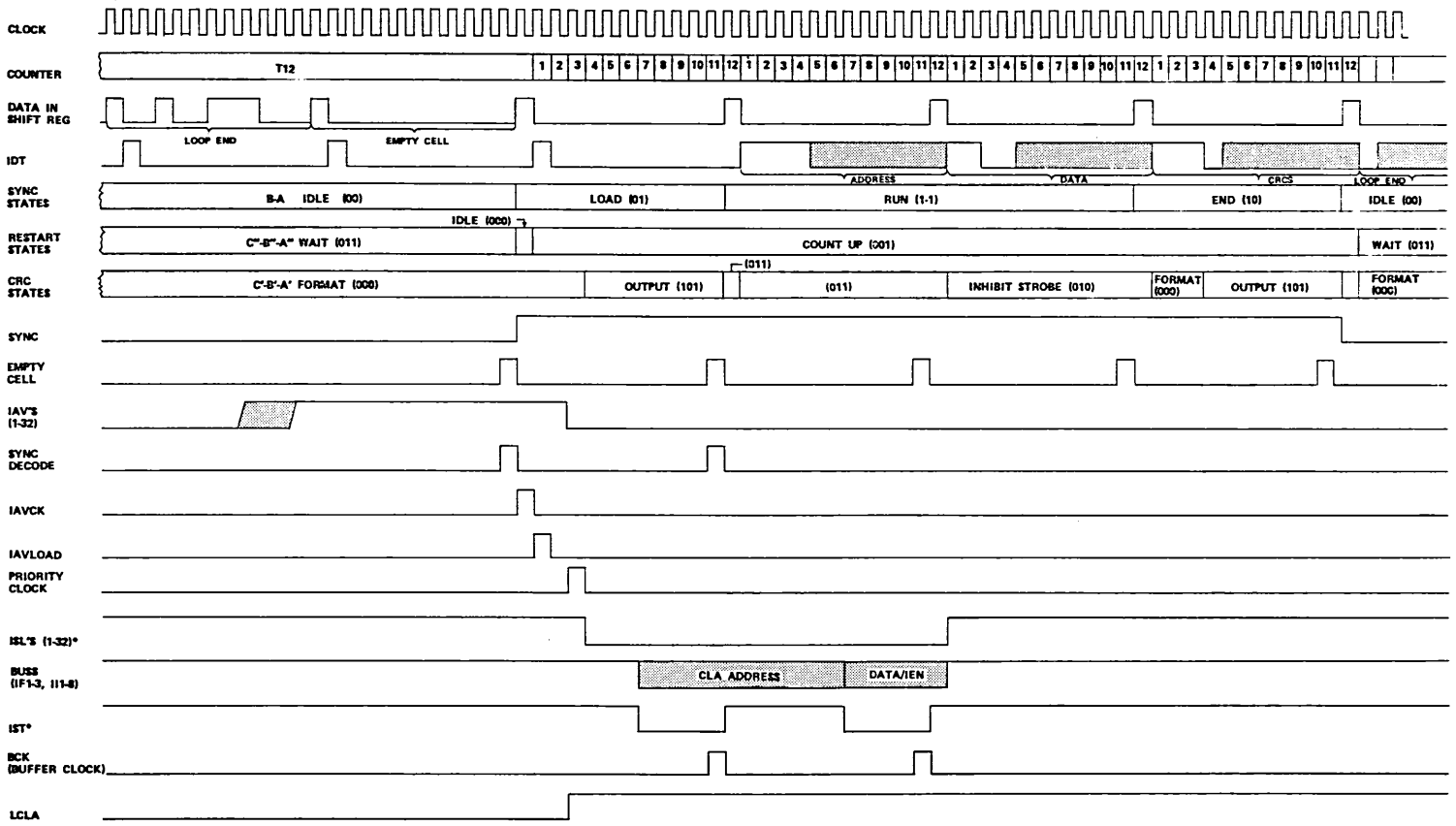


Figure 4-10. Input Loop Multiplexer Select Cycle (One CLA with IAV)

to the input of DSR11 allowing this portion of the shift register to recirculate, thus trapping the loop end.

This load state also allows the CLA selector to store the IAV in its IAV register (figure 4-4). This register is clocked with IAV clock, which is derived from LOAD and T12, only happening once during a select cycle. The S - R latches are enabled to "reset" with IAV load at LOAD and T1. The CLA select logic will now operate as previously described. While in load state the decoded empty cell is placed back on the loop.

IST* is produced by a flip-flop which turns on at T7 and off at T12. It is used by the CLAs in such a way that they should place information on the input bus on the falling edge of IST*. The input buffer is clocked one bit before the rising edge of IST* at T11.

The select control logic changes to the RUN state (state 3) following the LOAD state when T11 is true. This causes B to go true enabling the multiplexer of the input shift register section to parallel load DSR12 through DSR23 with the information in the input buffer. The shift register now contains a CLA address loop cell which is sent out onto the loop with the next 12 loop clocks. The select control will stay in the RUN state during the selection of all CLAs for that loop batch.

The CRC states register cycles through its states once for every CLA selected. It handles the timing for the accumulation and transmission of the CRC. While the select control goes through its LOAD the CRC states changes from the format state (0) to the output state (5) at T3 and then to the first of its accumulation states at the same instant as the select control switches to RUN. The CRC states register is reset in the LOAD state thus letting an empty cell be transmitted onto the input loop before the first line frame.

In state 1 of the CRC states, the CRC generator is enabled, allowing the first bit of the CLA address cell to be accumulated. At T12 and clock, it will change to CRC state 3 if IEN is not present, or to CRC state 2, if IEN is present. In CRC states 1, 2, 3, and 0 the CRC generator is enabled. In state 3, contiguous cells are inputted to the buffer at buffer clock and clocked into the input shift register at T12 and then onto the input loop. IEN is placed on the input bus by the CLA telling the LM that the information on the bus at that time is the last that the CLA has for the LM. This signal is also clocked into the buffer with buffer clock. IEN is seen by the CRC states at T12 and switches to state 2 (inhibit strobe). This state is decoded and fed to the reset of the select enable register of the selector causing the input select signal to the CLA to go high, terminating information transference from the CLA to LM. This last cell is accumulated by the CRC generator while the IST flip-flop and the buffer are held reset; at T12 the CRC states register goes to the format state (0).

In the format state (0), the CRC format code is sent out onto the loop. This code is produced by the buffer and is parallel-loaded into the input shift register at T12 just as the preceding cells were loaded. At T3, after the fourth CRC format bit is clocked onto the loop, the CRC states go to the output state (5). In the output state, zeros are fed into the input of the CRC generator while the output is gated onto the loop with the CRC out signal.

The select states register changes to the end state after RUN at T11 if either LCLA signal is true or if an empty cell is not detected by the empty cell decode gate. LCLA is the signal that comes from the last priority encoder indicating that none of its inputs is active. This means that all CLAs that had IAVs active at the beginning of the select cycles have been selected. At T11, the select states register goes to the idle state, ending the select cycle and resetting the CRC states register to the format state (0).

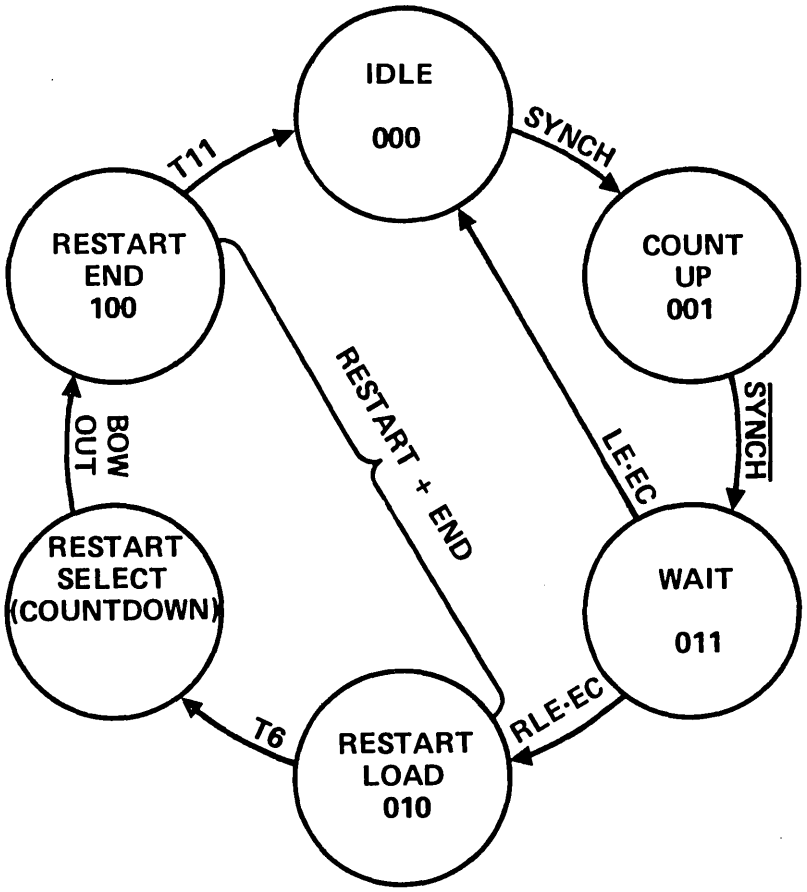
Restart Mode

When the MLIA wishes to inform the CLAs of an input loop batch error, it places a restart loop end followed by an empty cell on the loop. If the loop multiplexer had used the preceding loop batch to place CLA information on the loop, it will inform those CLAs that used that last loop batch of an input loop error.

The restart mode is a function of the restart states as represented in figure 4-11. The timing diagram in figure 4-12 shows the key signals used by the restart states register and their relationship to each other.

As an initial condition it is assumed that the restart state is idle (000). One bit-time after select state LOAD is active, the restart states change to count-up (001). It will remain in this state until the end of the select cycle. During this state, two cascaded up-down binary counters (select counter) are incremented one count by PCK for each CLA selected. At the end of the present select cycle the restart states change to the wait state (011). Thus, in the wait state the select counter's value is equal to the number of CLAs selected in the preceding select cycle. The IAVs associated with those CLAs remain stored in the IAV register.

If LE · EC is detected in the wait state, signifying that there was no input loop error in the last input loop batch, the restart states will again enter the idle (000) state to await the next select cycle. But, if a combination of restart loop end and empty cell (RLE · EC) is detected, indicating that there was indeed a loop error in the last input loop batch, the restart states register will switch to the restart load state (010).



IDLE (000) – SELECT AND RESTART STATES INACTIVE.

COUNT-UP (001) – RESTART COUNTER ALLOWED TO INCREMENT ON EVERY PRIORITY CLOCK.

WAIT (011) – SEARCHING FOR LE·EC OR RLE·EC

RESTART LOAD (010) – S-R LATCH LOADED WITH IAVs.

RESTART SELECT (110) – IER STROBED TO CLAs. RESTART COUNTER DECREMENTS

RESTART END (100) – LAST RESTART STATE; WAIT FOR T11.

Figure 4-11. Loop Multiplexer Restart States C"-B"-A"

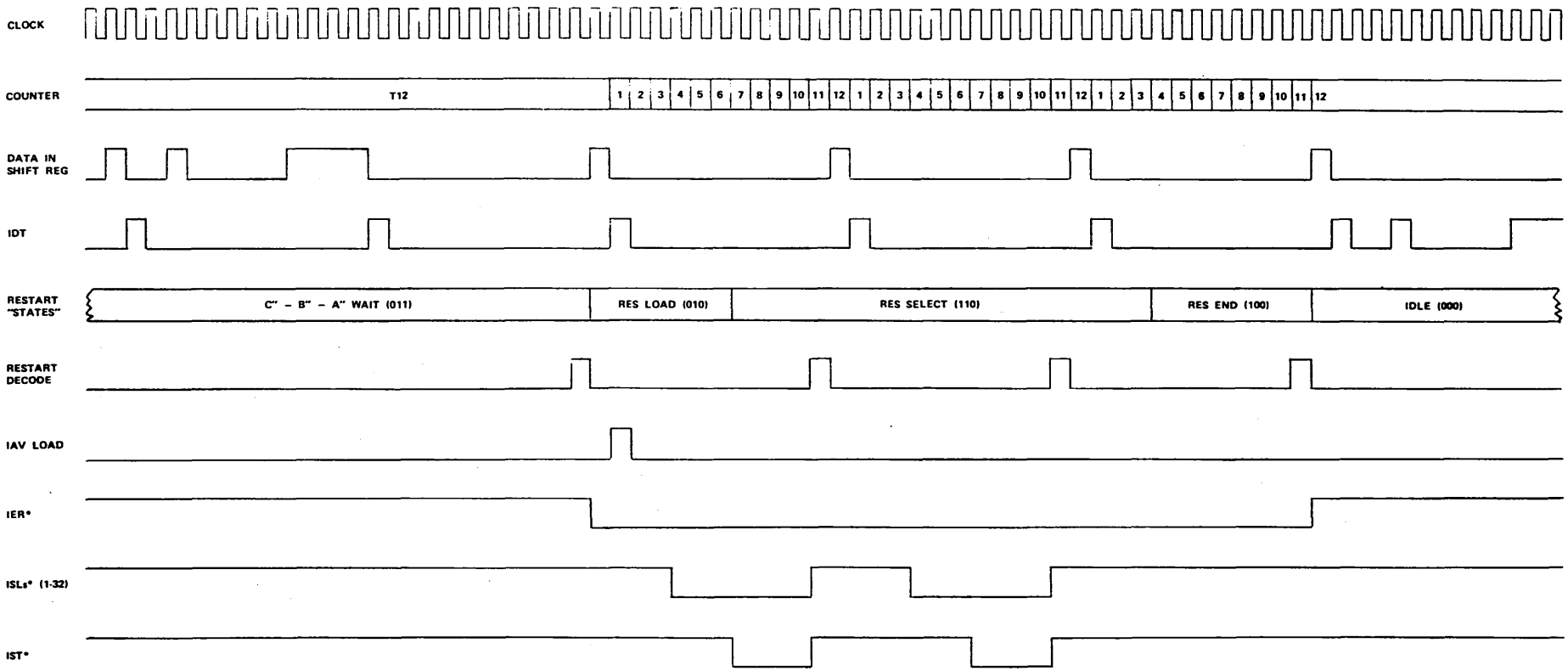


Figure 4-12. Loop Multiplexer Restart Mode Timing

IER, the bussed input error flag, is set to a logic one, in the restart load state, and remains active until the idle state is again attained. In restart load state, at T1, the S-R latches of the CLA select logic are reset by the IAVs in the IAV register. From this point on, the CLA select logic will function as previously described, with each input select signal activating on the trailing edge of PCK and deactivating at T11. Also, along with each input select, the IST signal is sent to all CLAs, setting to logic one at T7 and resetting at T11. As noted in the discussion on the input shift register, the restart loop end is recirculated, or "trapped," to be released onto the input loop at the complettion of the restart cycle.

On T7 after the restart load state is entered the restart states will switch to the restart select state (110). Selection of CLAs is continued. The select counter is decremented one count for each CLA selected with the trailing edge of PCK. When all CLAs that were selected in the last loop batch are selected in the restart cycle, the borrow-outs from both of the binary counters that make up the select counter will be active, causing the transition into the RES END state (100). At T11 the restart states switch to idle, ending the restart cycle. At this time the recirculating restart loop end is released onto the input loop.

Redundant Operation

When it is desired to use the LM in a redundant system, two LM logic cards are required per each LM card cage, one primary and the other secondary. Both cards have access to all CLAs in their cage, but only one can be active at a time. The only difference between the primary and secondary LM card slots in the card cage is that pin 215 on the secondary slot is connected to ground. When the LM logic card is plugged into this slot, grounding SEN, it is enabled to decode secondary loop end.

The only way that either the primary or secondary LM knows that it is supposed to be active is through detection of a loop end or secondary loop end on their respective input loops. This being the case, the primary LM, when active, must enable its output section and disable the output section of the secondary LM. The same corresponding action will occur when the secondary LM is active. The disabling is accomplished with OD1 and OD2. OD1 and OD2 of the primary LM are connected to OD2 and OD1 of the secondary LM, respectively.

In redundant operation, master clear (MCL) can only be activated when input and output loop clocks on both the primary and secondary LMs are inactive for approximately 30 μs. This is accomplished by connecting the primary and secondary LM cards as shown in figure 4-13.

Communications Line Adapter

For information on communications line adapters refer to the following:

- 2550 Series Asynchronous Communications Line Adapter Reference/Maintenance Manual, Pub. No. 74700900.

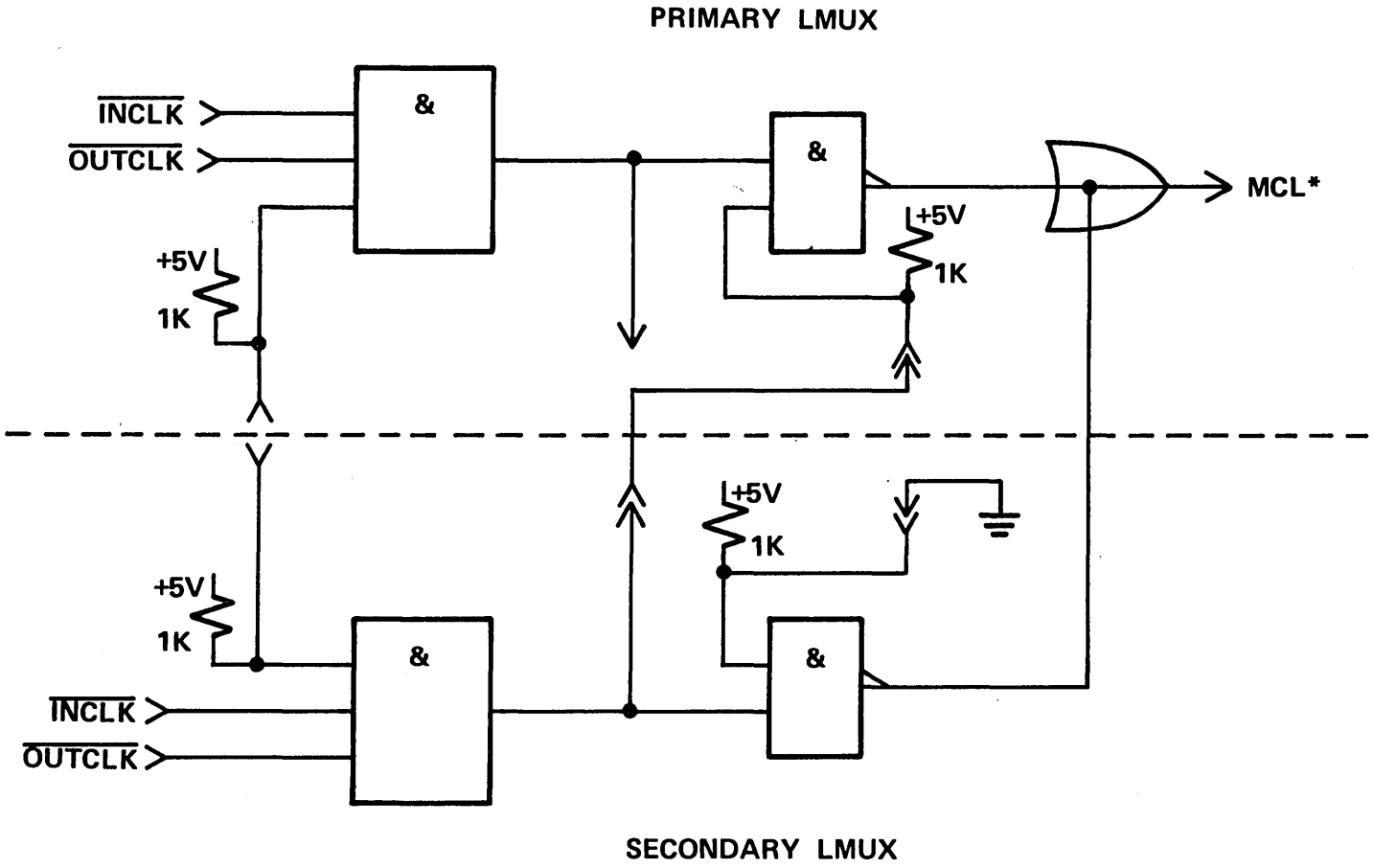


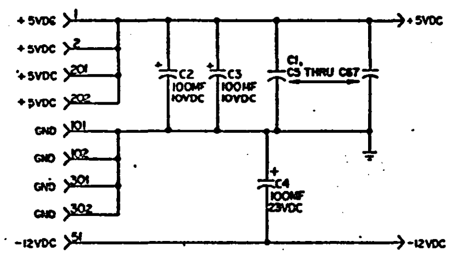
Figure 4-13. Loop MUX Master Clear (MCL) Logic

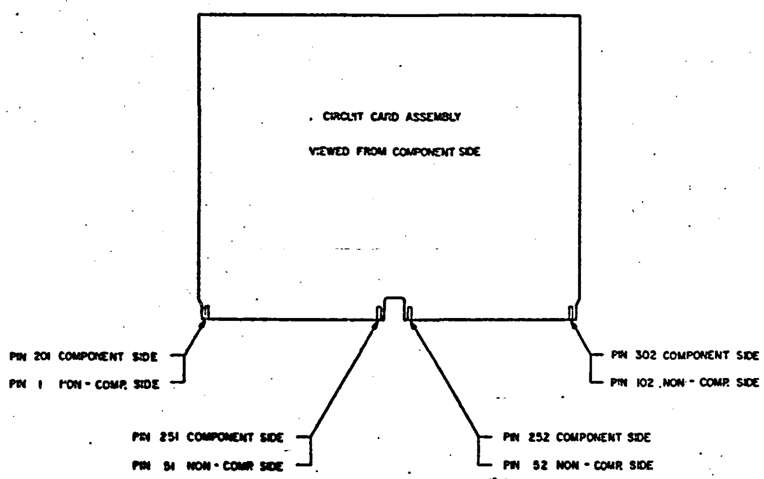
This section contains the logic diagrams for the circuit cards comprising the Communications Multiplexer.

Logic diagrams for the ACLA circuit card are found in the Asynchronous Communications Line Adapter, 2561-1 Hardware Reference/Maintenance Manual.

Drawing Number	Title
74544901 (32800-03-012)	Input Loop Interface, MLIA No. 1
74558501 (32780-04-013)	Output Loop Interface, MLIA No. 2
74544800 (30280-04-012)	Processor Interface, MLIA No. 3
74541200 (30250-00-012)	Loop Multiplexer

REV	ECO	DESCRIPTION
02	05336	"CL.B PRERELEASE"
03	05579	SEE ECO
04	05901	SEE ECO
05	05992	SEE ECO
06	06081	SEE ECO
07	06470	INITIAL RELEASE





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES 5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: .01 MF, 25VDC, +80-20%
   ALL DIODES: DIALCO 547-2003, 5V, 6MA

2. COMPONENT ASSEMBLY 74872399

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL-IN-LINE	14	7
16 PIN DUAL-IN-LINE	16	8

NON-STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

4AAY

DO NOT SCALE DRAWING

COMMUNICATIONS PRODUCTS DIV

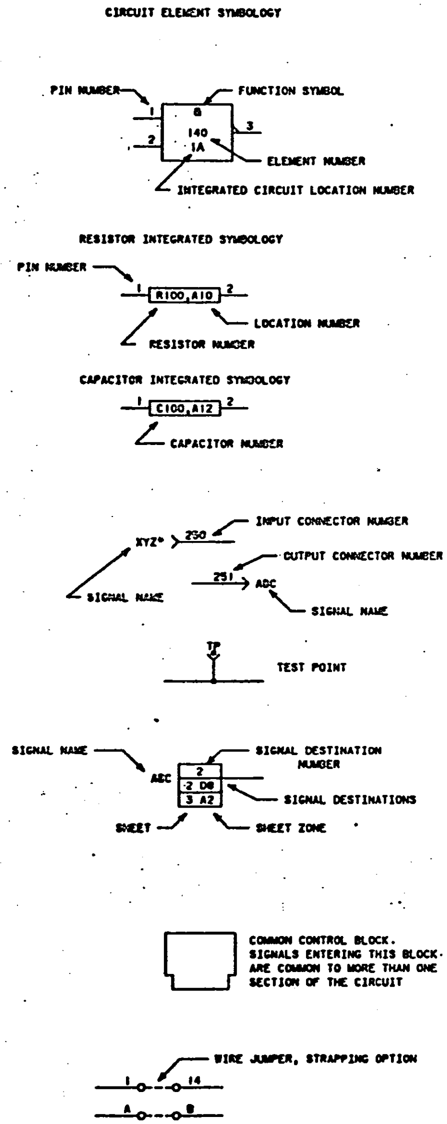
DR A. MARREK 11-12-73

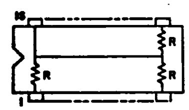
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1

D 34015 74872400

SCALE NONE 54420-012-104 SHEET 1 OF 11

REV	ECO	DESCRIPTION				
		SEE SHEET 1				





I.C. RESISTOR PACK
LOCATION U1,U47,U48,U74,
U81,U89,U119
1.5K, 1/8W, ±2%

IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
143S	74S40	TTL DUAL 4-INPUT NAND BUFFER
140	7400	TTL QUAD 2-INPUT NAND GATE
140S	74S00	TTL QUAD 2-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146S	74S04	TTL HEX INVERTER
148	7402	TTL QUAD 2-INPUT NOR GATE
149	7486	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
158	74161	COUNTER, TTL 4-BIT BINARY
175	7474	TTL DUAL D-TYPE F/F
175S	74S74	TTL DUAL D-TYPE F/F
—	74S140	TTL LINE DRIVER DUAL 4-INPUT
189	74157	MULTIPLEXER, TTL QUAD 2-INPUT
—	3341	QUAD 64 BIT SHIFT MEMORY (FIFO)
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE (OPEN COLL)
—	74S03	TTL QUAD 2-INPUT NAND GATE (OPEN COLL)
528	74194	REG, TTL 4-BIT SHIFT
528S	74S194	REG, TTL 4-BIT SHIFT
—	TYB 12-20	DELAY LINE
520	74175	LATCH, TTL 4-BIT D-TYPE
520S	74S175	LATCH, TTL 4-BIT D-TYPE
—	IM5600	PROGRAMMED READ ONLY MEMORY (32 X 8)
—	74S153	TTL DUAL MULTIPLEXER
—	74S86	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
774	7489	MEMORY TTL 64 BIT 16 X 4 RAM

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE; NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
	SCHMITT TRIGGER
1	ONE-SHOT MULTIVIBRATOR
	TIME DELAY
OO	EVEN PARITY
OOO	ODD PARITY
X → Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
¬	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

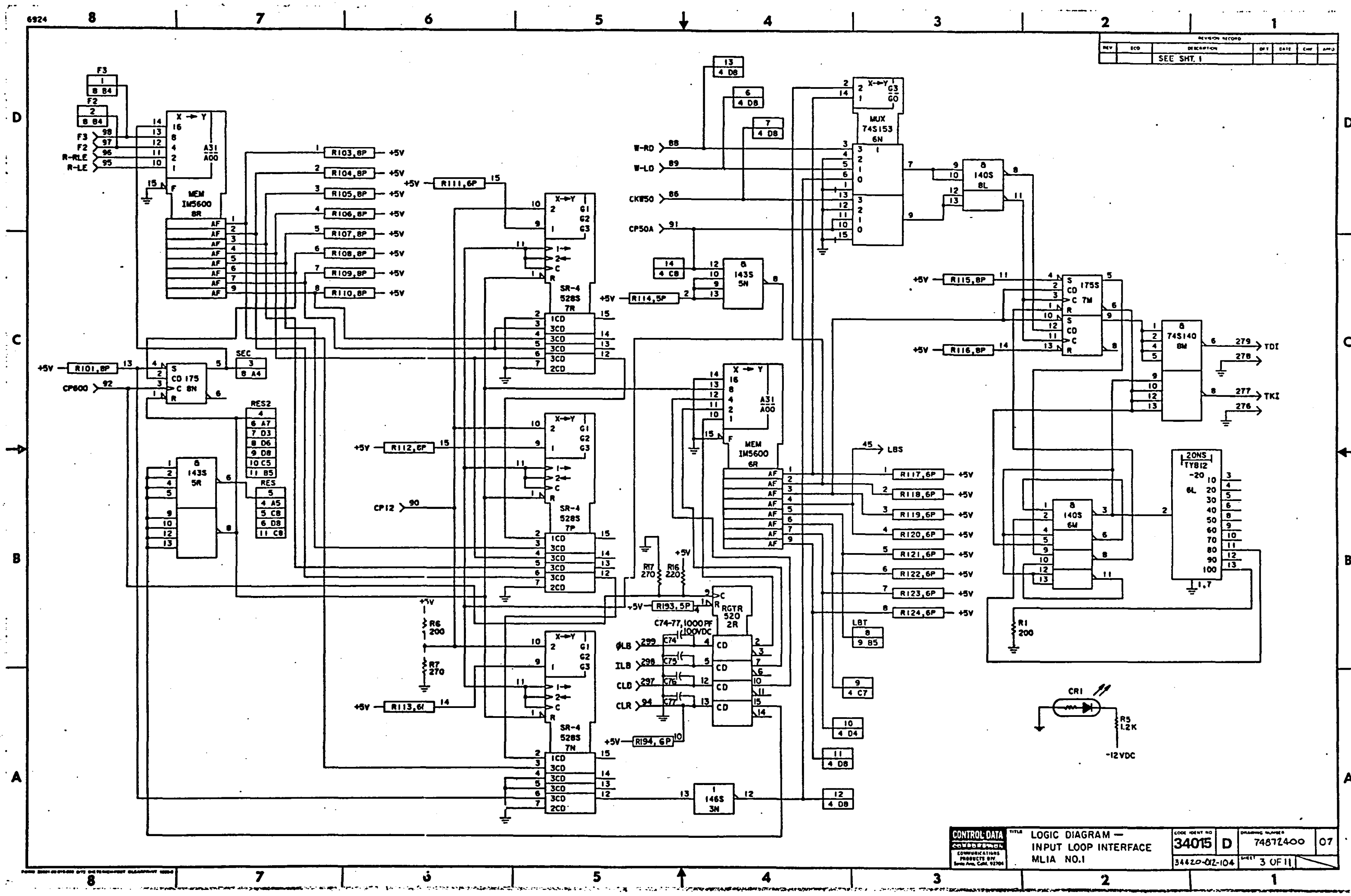
SIGNAL LINE INDICATORS

◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
	NON-STANDARD LOGIC LEVEL
	ANALOG OR NON-LOGIC LEVEL
	VARIABLE PARAMETER CONTROL
	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
	INHIBIT DESIGNATOR

FUNCTION ABBREVIATIONS

ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

CONTROL DATA	TITLE	CODE IDENT NO	SIZE	DRAWING NUMBER	REV
COMMUNICATIONS PRODUCTS DIV	LOGIC DIAGRAM— KEY TO SYMBOLS	34015	D	74812400	07
		54420-012-104		SHEET 2 OF 11	

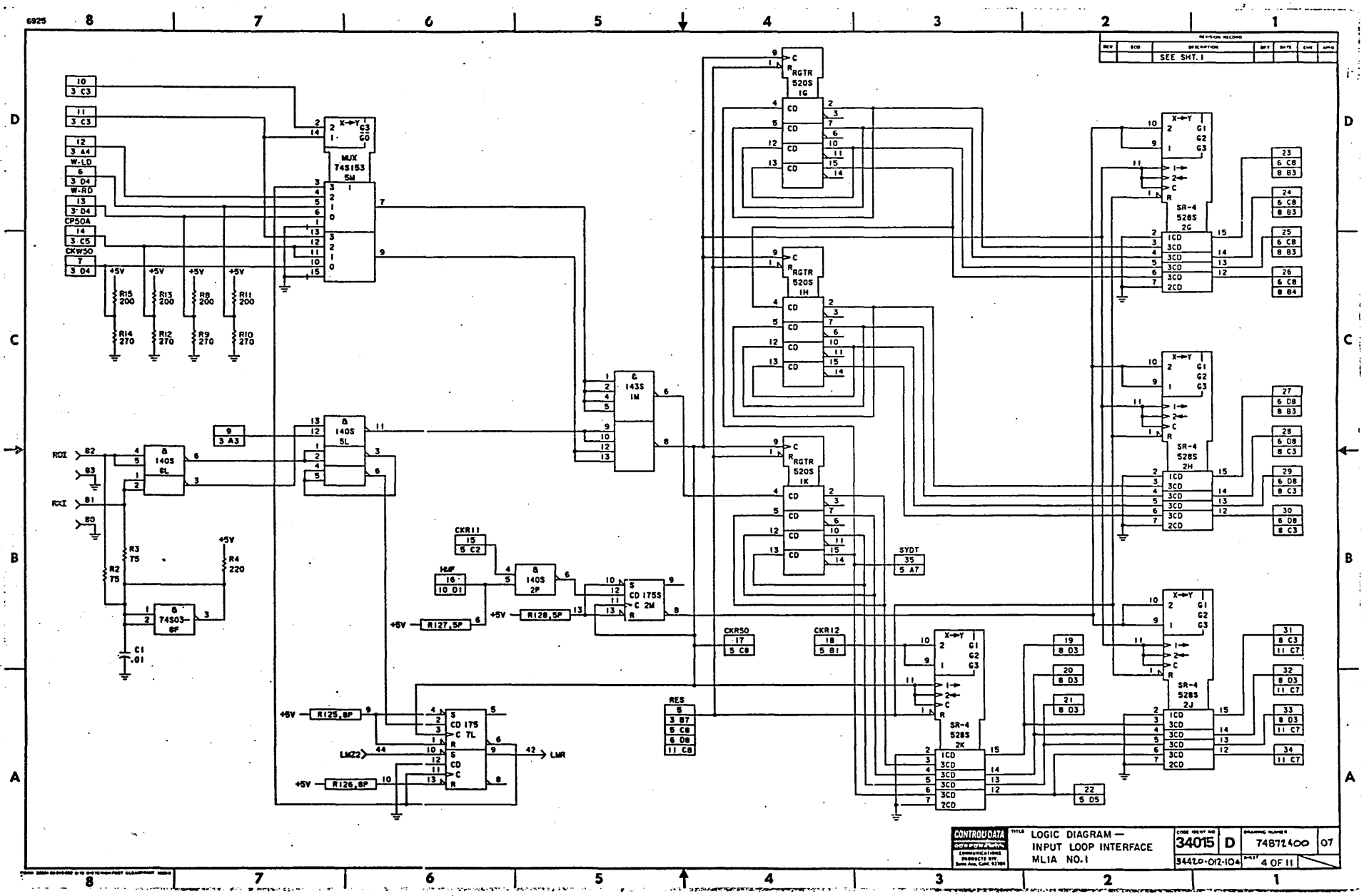


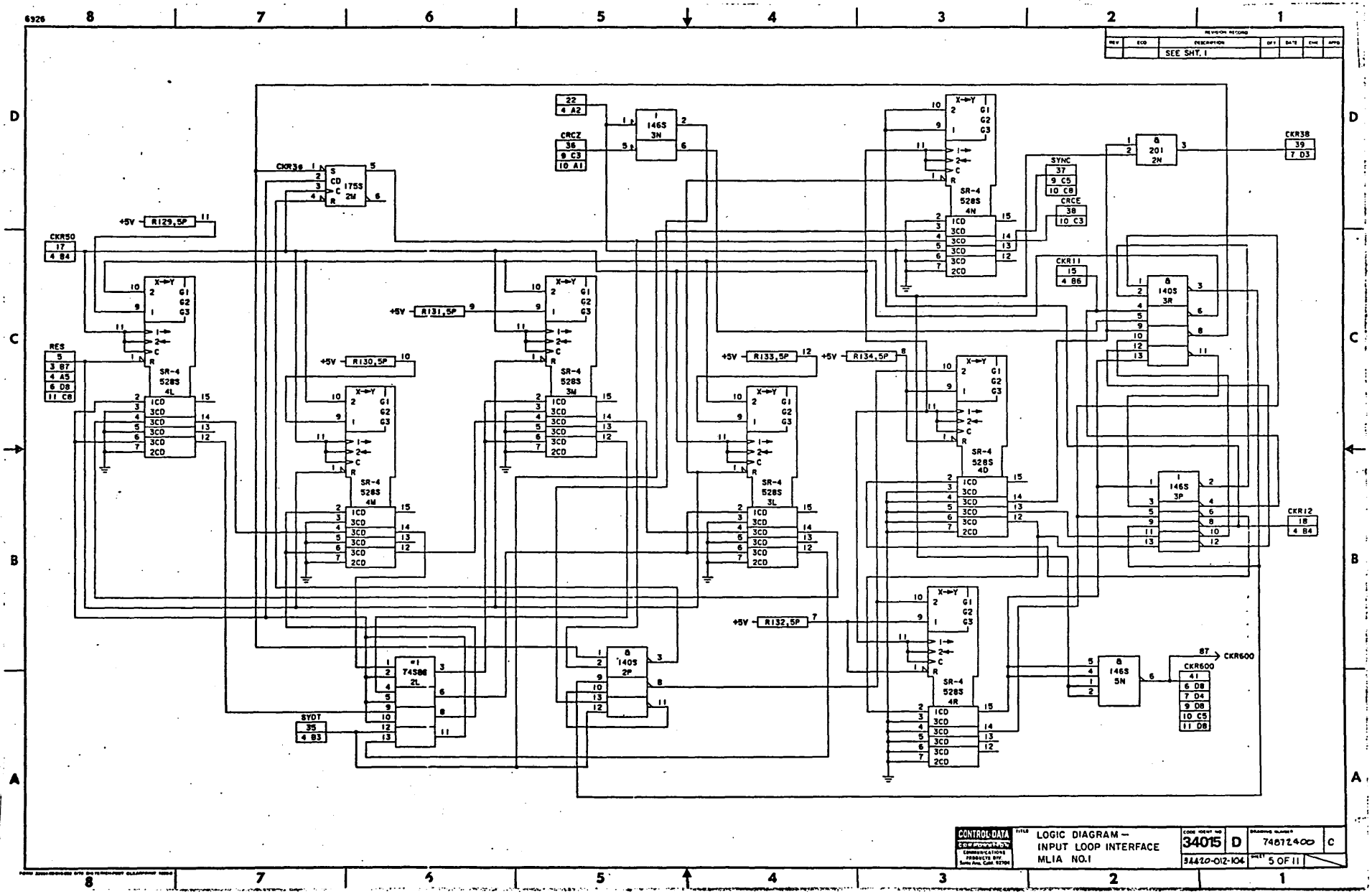
CONTROL DATA CORPORATION
COMMUNICATIONS PRODUCTS DIV.

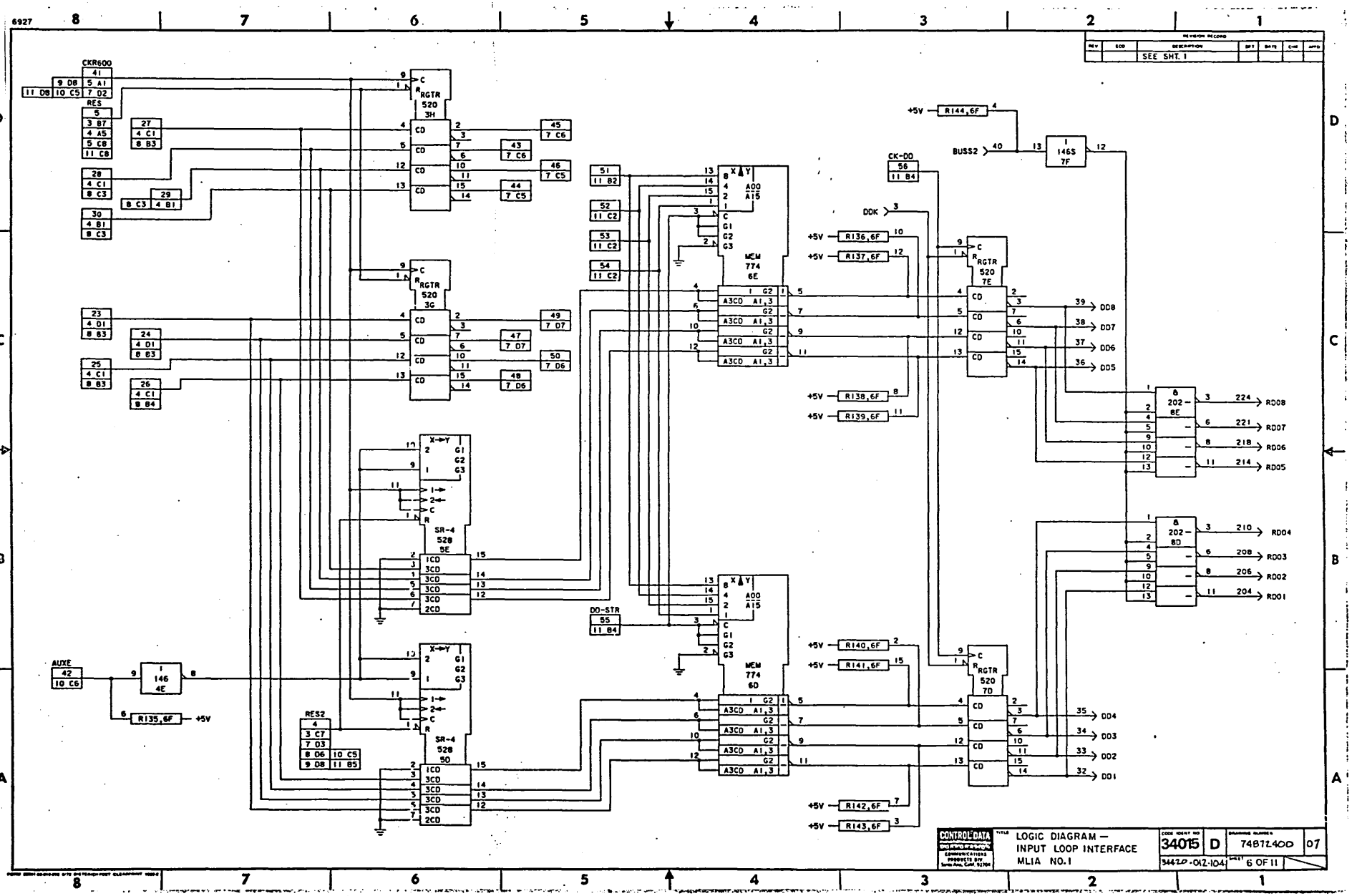
LOGIC DIAGRAM —
INPUT LOOP INTERFACE
MLIA NO.1

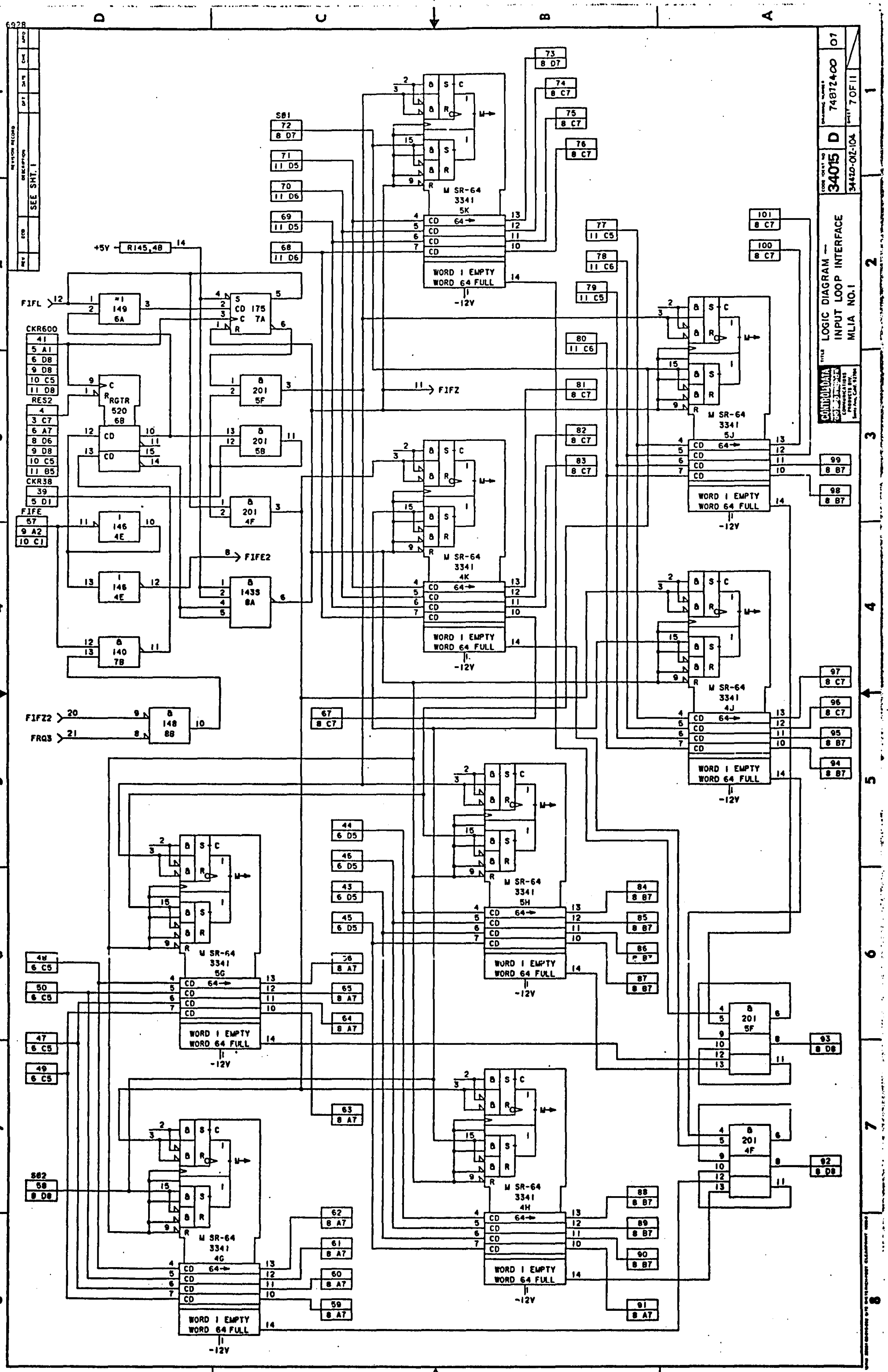
34015 D 74872400 07

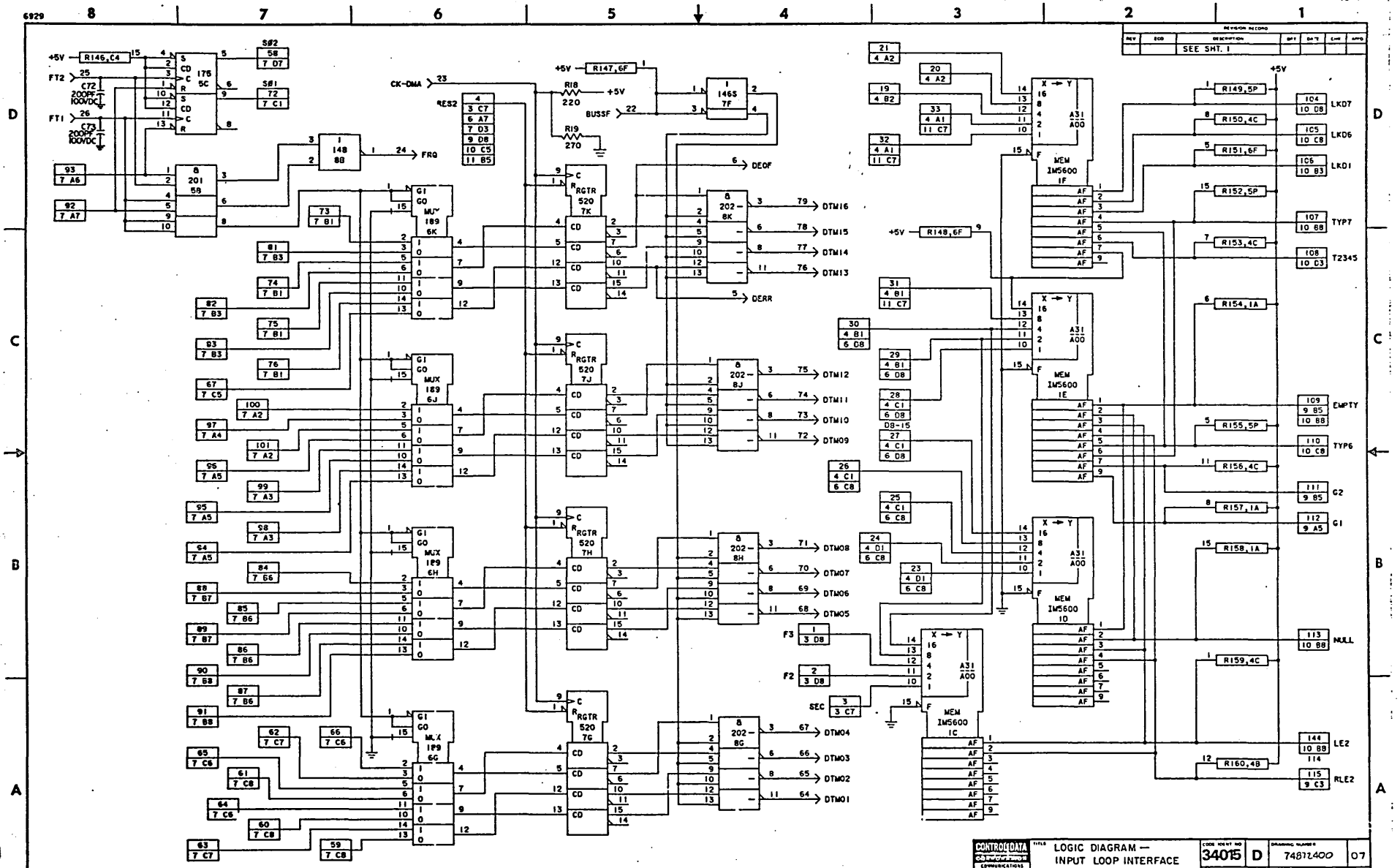
34420-012-104 SHEET 3 OF 11

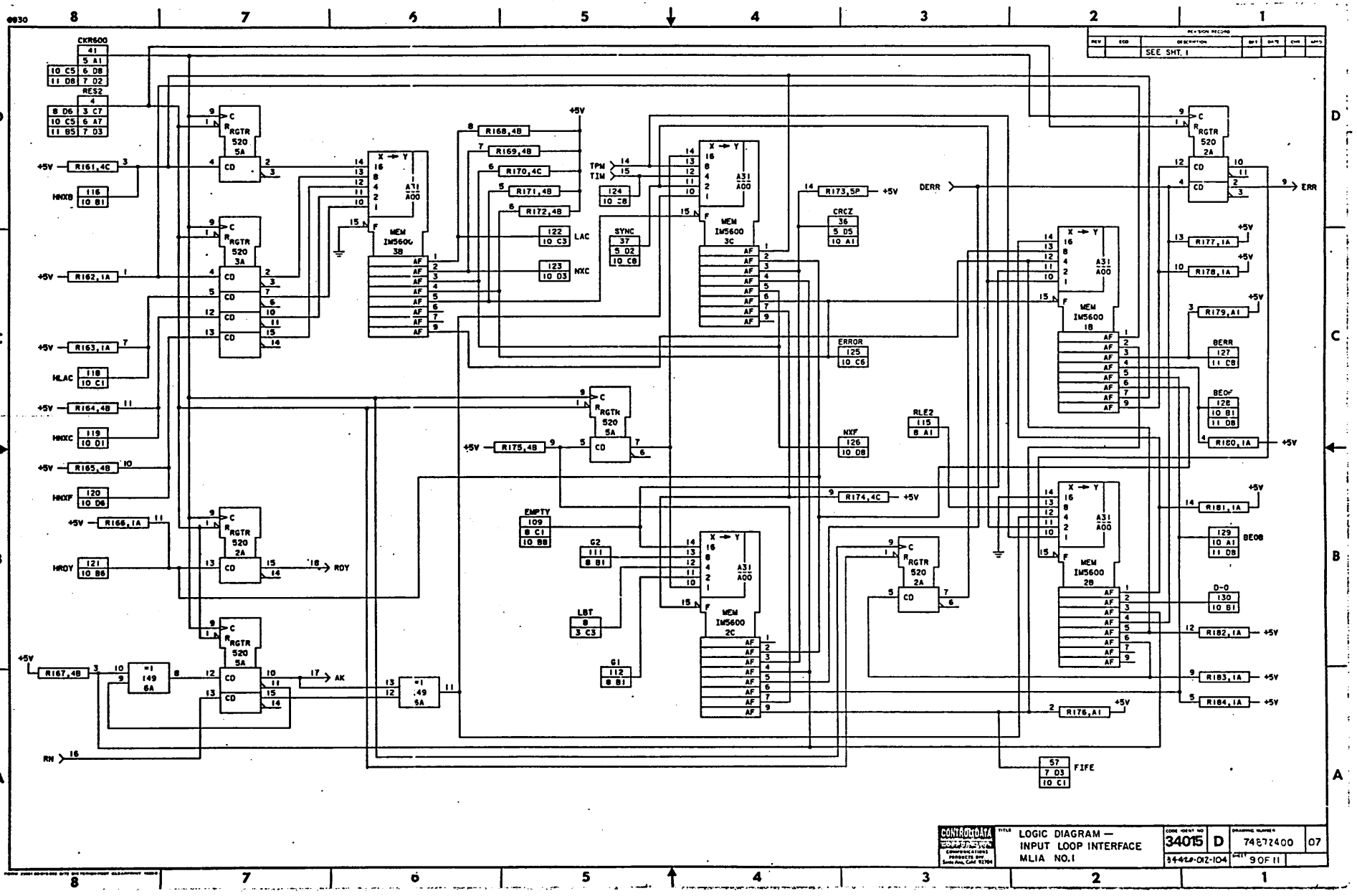

6925
8
7
6
5
4
3
2
1
REVISION RECORD
REV
ECO
DESCRIPTION
SEE SHT. 1
MUX 74S153 5M
W-LD
W-RD
CP50A
CKW50
+5V
R15 200
R13 200
R8 200
R11 200
R14 270
R12 270
R9 270
R10 270
RGTR 520S 1G
RGTR 520S 1H
RGTR 520S 1K
SR-4 528S 2G
SR-4 528S 2H
SR-4 528S 2J
SR-4 528S 2K
1CD
3CD
2CD
& 14S 1M
& 14S 5L
& 14S 6L
& 14S 2P
74S03 8F
CD 175S 2M
CD 175 7L
RDI
RDI
R1 75
R2 75
R3 75
R4 220
C1 .01
CKR11
CKR50
CKR12
HMF
SYDT
RES
R127,5P
R128,5P
R125,8P
R126,8P
LMZ2
LMR
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1
CONTROL DATA
34015
D
74872400
07
34420-012-104
SHEET 4 OF 11


SEE SHT. 1
CKR38
CKR50
RES
SYDT
SYNC
CRCE
CKR11
CKR12
CKR600
CRCZ
+5V R129,5P
+5V R130,5P
+5V R131,5P
+5V R132,5P
+5V R133,5P
+5V R134,5P
SR-4 528S 4L
SR-4 528S 4M
SR-4 528S 3M
SR-4 528S 3L
SR-4 528S 4N
SR-4 528S 4D
SR-4 528S 4R
175S 2M
146S 3N
201 2N
140S 3R
146S 3P
140S 2P
74S86 2L
146S 5N
CONTROL DATA
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1
34015
D
74812400
C
SHEET 5 OF 11

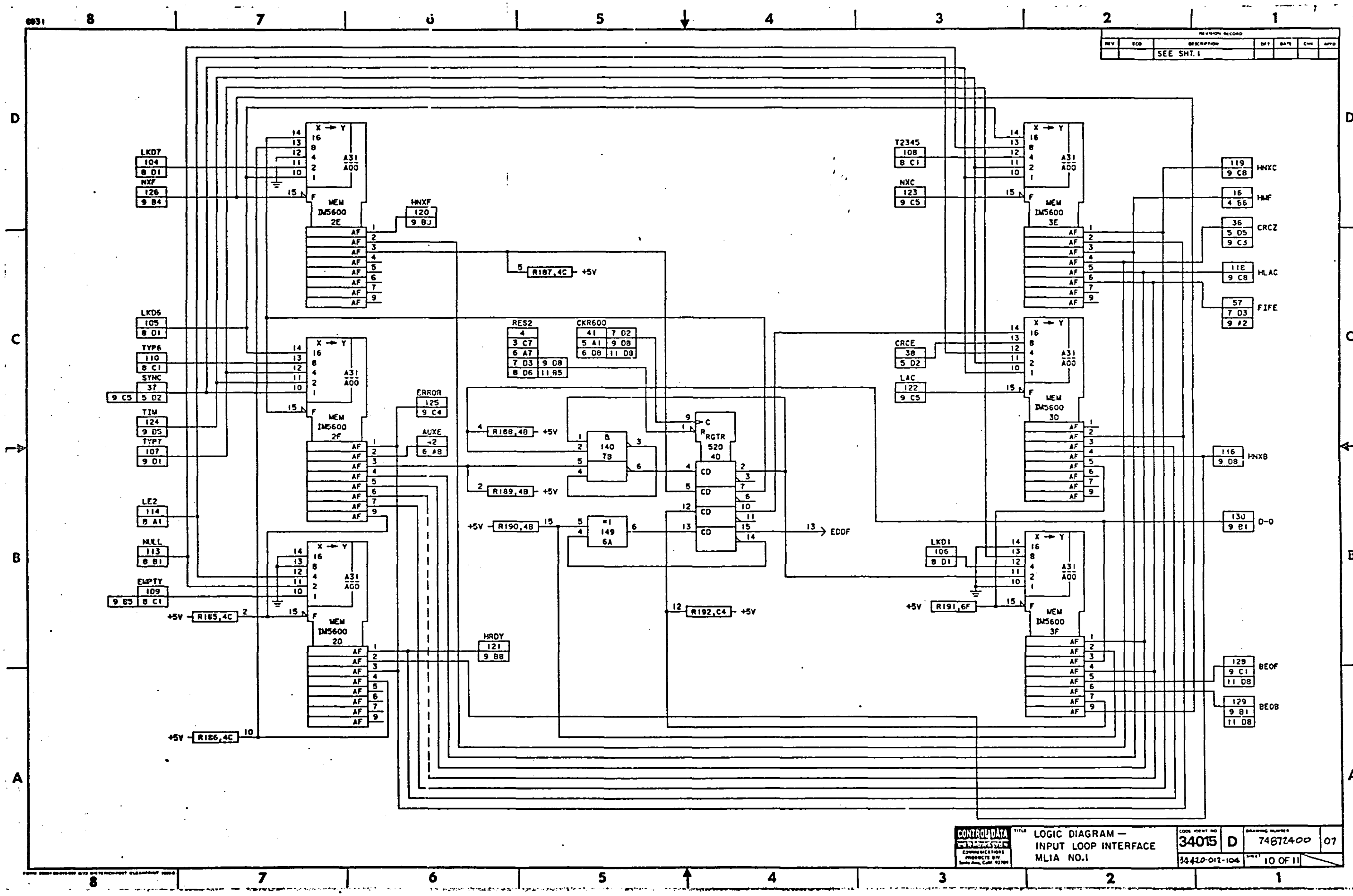

6927
REVISION RECORD
SEE SHT. 1
CKR600
RES
AUXE
RES2
DDK
CK-DO
DO-STR
BUSS2
+5V
RGTR 520 3H
RGTR 520 3G
RGTR 520 7E
RGTR 520 7D
MEM 774 6E
MEM 774 6D
SR-4 528 5E
SR-4 528 5D
146 4E
146S 7F
202 8E
202 8D
DD8
DD7
DD6
DD5
DD4
DD3
DD2
DD1
RD08
RD07
RD06
RD05
RD04
RD03
RD02
RD01
CONTROL DATA
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO. 1
34015
D
74B7L400
07
34420-042-104
SHEET 6 OF 11


LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1
34015
D
74B72400
7 OF 11
SEE SHT. 1
M SR-64 3341 5K
M SR-64 3341 4K
M SR-64 3341 5J
M SR-64 3341 4J
M SR-64 3341 5H
M SR-64 3341 4H
M SR-64 3341 5G
M SR-64 3341 4G
WORD 1 EMPTY
WORD 64 FULL
-12V
F1FL
CKR600
RES2
CKR38
F1FE
F1FZ
F1FE2
F1FZ2
FRQ3
+5V
R145,48

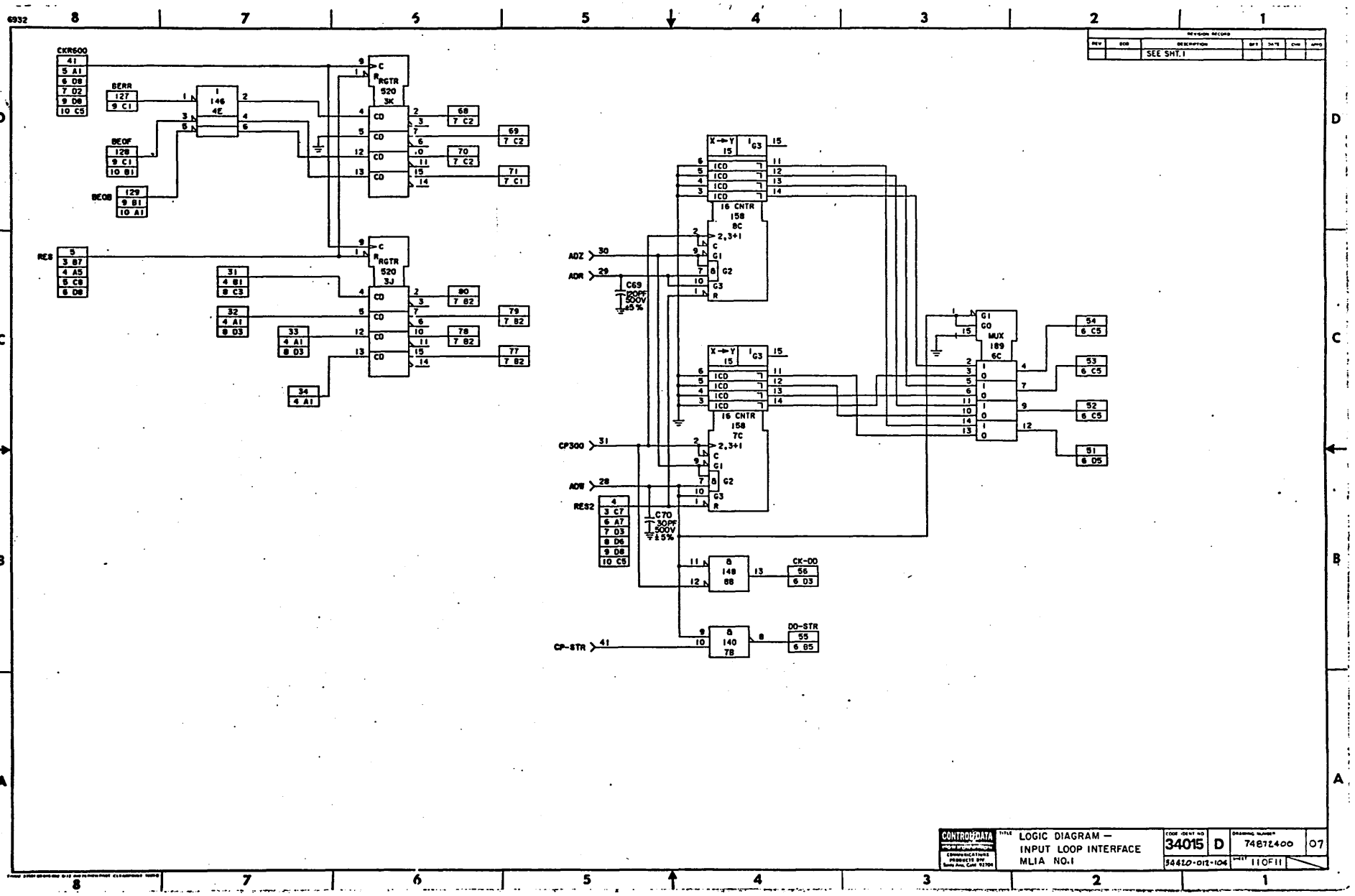

6929
REVISION RECORD
SEE SHT. 1
+5V
FT2
FT1
CK-DMA
RES2
BUSSF
FRQ
DEOF
DERR
DTM16
DTM15
DTM14
DTM13
DTM12
DTM11
DTM10
DTM09
DTM08
DTM07
DTM06
DTM05
DTM04
DTM03
DTM02
DTM01
F3
F2
SEC
MEM IM5600 1F
MEM IM5600 1E
MEM IM5600 1D
MEM IM5600 1C
LKD7
LKD6
LKD1
TYP7
T2345
EMPTY
TYP6
G2
G1
NULL
LE2
RLE2
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1
CONTROL DATA
34015
D
74812400
07
34410-012-104
SHEET 8 OF 11



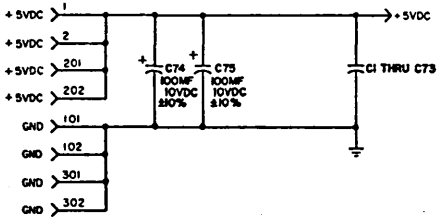
CONTROL DATA CORPORATION	TITLE: LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1	CODE IDENT NO 34015	D	DRAWING NUMBER 74872400	07
		84428-012-104		SHEET 9 OF 11	

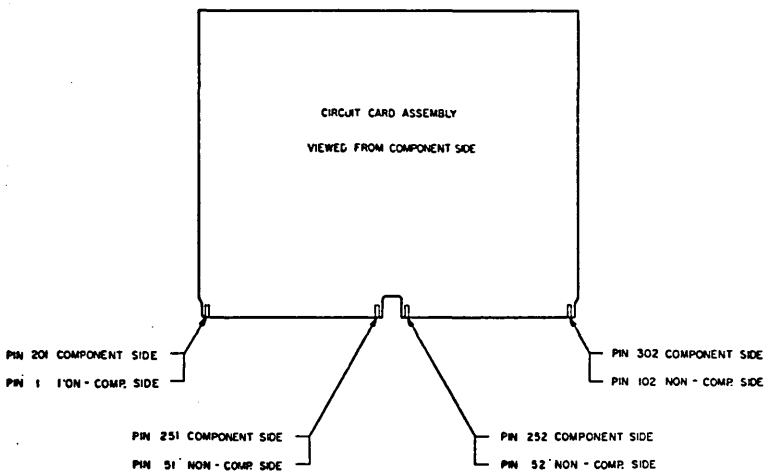


SEE SHT. I
LKD7 104 8 D1
NXF 126 9 B4
LKD5 105 8 D1
TYP6 110 8 C1
SYNC 37 9 C5 5 D2
TIM 124 9 D5
TYP7 107 9 D1
LE2 114 8 A1
NULL 113 8 B1
EMPTY 109 9 B5 8 C1
+5V R185,4C
+5V R186,4C
MEM IM5600 2E
MEM IM5600 2F
MEM IM5600 2D
MEM IM5600 3E
MEM IM5600 3D
MEM IM5600 3F
X → Y
A31 A00
HNXF 120 9 B3
ERROR 125 9 C4
AUXE 42 6 A8
HRDY 121 9 B8
R187,4C +5V
RES2 4 3 C7 6 A7 7 D3 9 D8 8 D6 11 B5
CKR600 41 7 D2 5 A1 9 D8 6 D8 11 D8
R188,4B +5V
R189,4B +5V
& 140 7B
RGTR 520 4D
CD
=1 149 6A
+5V R190,4B
EDDF
R192,C4 +5V
T2345 108 8 C1
NXC 123 9 C5
CRCE 38 5 D2
LAC 122 9 C5
LKD1 106 8 D1
+5V R191,6F
HNXC 119 9 C8
HMF 16 4 B6
CRCZ 36 5 D5 9 C3
HLAC 11E 9 C8
FIFE 57 7 D3 9 A2
HNXB 116 9 D8
D-O 130 9 B1
BEOF 128 9 C1 11 D8
BEOB 129 9 B1 11 D8
CONTROL DATA
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1
34015 D 74672400 07
54420-012-104
10 OF 11


6932
REVISION RECORD
SEE SHT. 1
CKR600
BERR
BEOF
BEOB
RES
RGTR 520 3K
RGTR 520 3J
146 4E
ADZ
ADR
ADW
CP300
RES2
CP-STR
C69 200PF 500V ±5%
C70 30PF 500V ±5%
16 CNTR 158 8C
16 CNTR 158 7C
MUX 189 6C
148 88
140 78
CK-DD
DD-STR
CONTROL DATA
LOGIC DIAGRAM — INPUT LOOP INTERFACE MLIA NO.1
34015
D
74872400
07
SHEET 1 OF 11

02	05336	CL. B PRERELEASE	
03	05467	SEE ECO	
04	05529	SEE ECO	
05	05901	SEE ECO	WJM
06	05992	SEE ECO	
07	06081	SEE ECO	
08	06162	SEE ECO	
09	06470	INITIAL RELEASE	





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: .01 MF, 25 VDC, +80 - 20%
   ALL DIODES: DIALCO 847-2003, 5V, 6MA

2. COMPONENT ASSEMBLY 74872408

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL - IN - LINE	14	7
16 PIN DUAL - IN - LINE	16	8

NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

4AAY

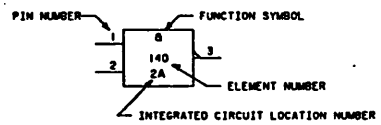
LOGIC DIAGRAM –
OUTPUT LOOP INTERFACE
MLIA NO. 2

D 34015 74872409

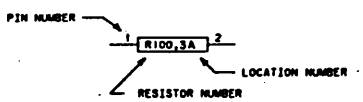
6650

SEE SHEET 1

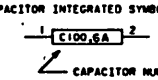
CIRCUIT ELEMENT SYMBOLOGY

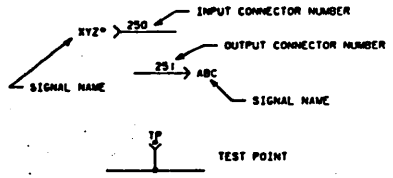


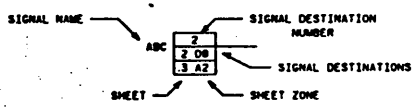
RESISTOR INTEGRATED SYMBOLOGY



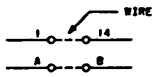
CAPACITOR INTEGRATED SYMBOLOGY

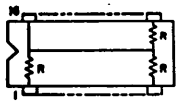






COMMON CONTROL BLOCK. SIGNALS ENTERING THIS BLOCK ARE COMMON TO MORE THAN ONE SECTION OF THE CIRCUIT





I.C. RESISTOR PACK
LOCATION U4,U9,U22,U70, U72,U75,U126
1.5K,1/8W,±2%

IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
1433	74S40	TTL DUAL 4-INPUT NAND BUFFER
140	7400	TTL QUAD 2-INPUT NAND GATE
140S	74S00	TTL QUAD 2-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146S	74S04	TTL HEX INVERTER
143	7440	TTL DUAL 4-INPUT NAND BUFFER
149	7486	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
158	74161	COUNTER, TTL 4-BIT BINARY
175	7474	TTL DUAL D-TYPE F/F
175S	74S74	TTL DUAL D-TYPE F/F
—	74S140	TTL LINE DRIVER DUAL 4-INPUT
189	74157	MULTIPLEXER, TTL QUAD 2-INPUT
189S	74S157	MULTIPLEXER, TTL QUAD 2-INPUT
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE (OPEN COLL)
—	74S03	TTL QUAD 2-INPUT NAND GATE (OPEN COLL)
528	74194	REG, TTL 4-BIT SHIFT
528S	74S194	REG, TTL 4-BIT SHIFT
—	TYB12-20	DELAY LINE
520	74175	LATCH, TTL 4-BIT D-TYPE
520S	74S175	LATCH, TTL 4-BIT D-TYPE
—	IM5600	PROGRAMMED READ ONLY MEMORY (32 X 8)
—	74S53	TTL DUAL MULTIPLEXER
—	74S86	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
774	7489	MEMORY TTL 64 BIT 16 X 4 RAM
243S	74S112	TTL DUAL J-K NET F/F
512	74191	COUNTER, TTL 4-BIT BINARY UP-DOWN

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
8	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
1⊓	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X → Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
I	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⊓	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→+	SHIFT RIGHT (OR DOWN)
+←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

◇8 OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◺	POLARITY CONVENTION, NEGATIVE POTENTIAL
⊏>	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
—/—	NON-STANDARD LOGIC LEVEL
—≠—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PARAMETER CONTROL
—○—	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
—○—	INHIBIT DESIGNATOR

FUNCTION ABBREVIATIONS

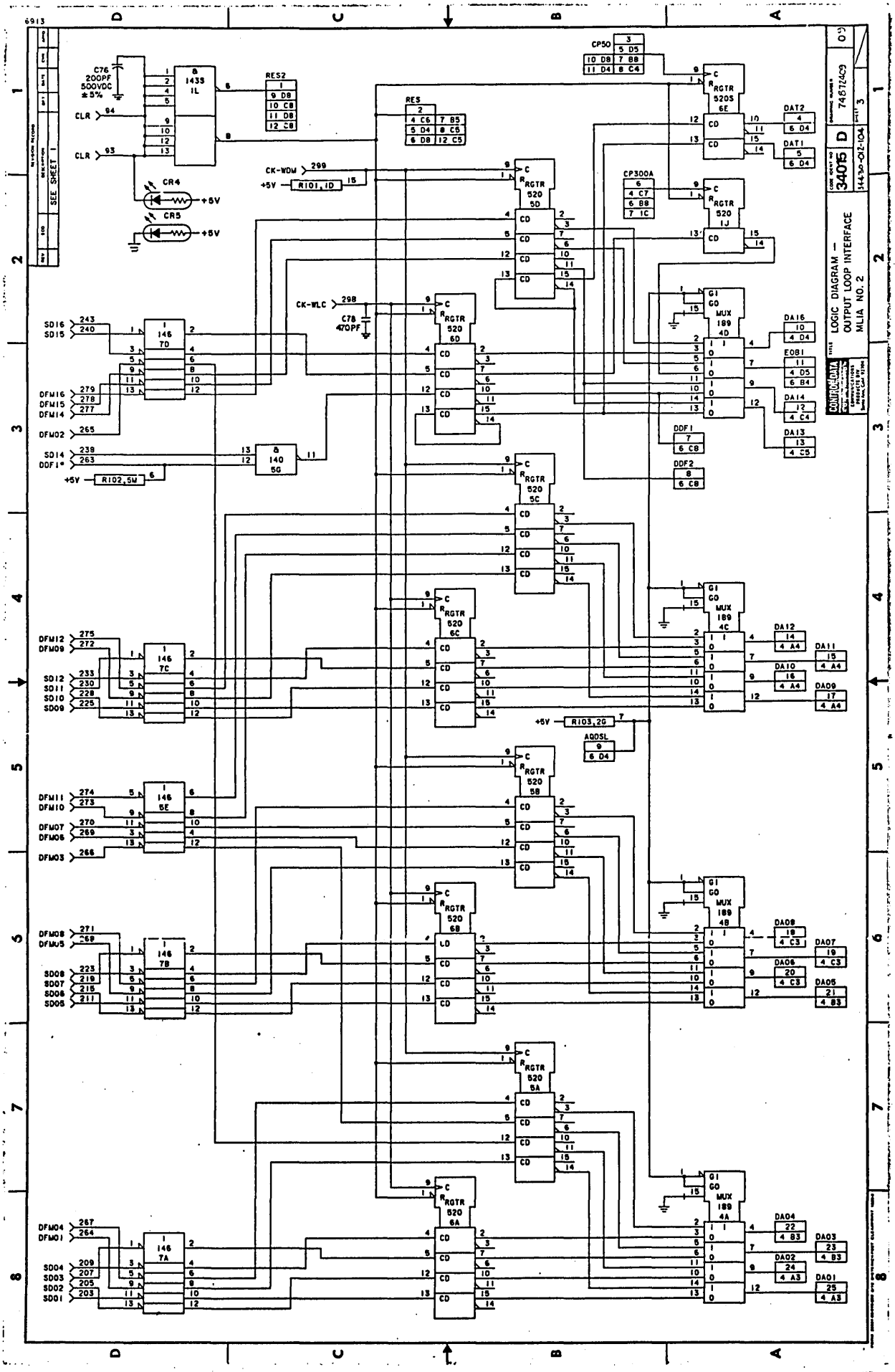
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

CONTROL DATA

TITLE: LOGIC DIAGRAM— KEY TO SYMBOLS

34015 D 74872409 09

34430-012-104 SHEET 2


LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO. 2
CONTROL DATA
34015 D
74672409
SEE SHEET 1
C76 200PF 500VDC ±5%
CLR
CR4
CR5
+5V
RES2
RES
CP50
CP300A
CK-WDW
CK-WLC
C78 470PF
R101,1D
R102,5W
R103,2G
AQDSL
DDF1
DDF2
RGTR 520 5D
RGTR 520 6D
RGTR 520 5C
RGTR 520 6C
RGTR 520 5B
RGTR 520 6B
RGTR 520 5A
RGTR 520 6A
MUX 189 4D
MUX 189 4C
MUX 189 4B
MUX 189 4A
SD16
SD15
SD14
SD13
SD12
SD11
SD10
SD09
SD08
SD07
SD06
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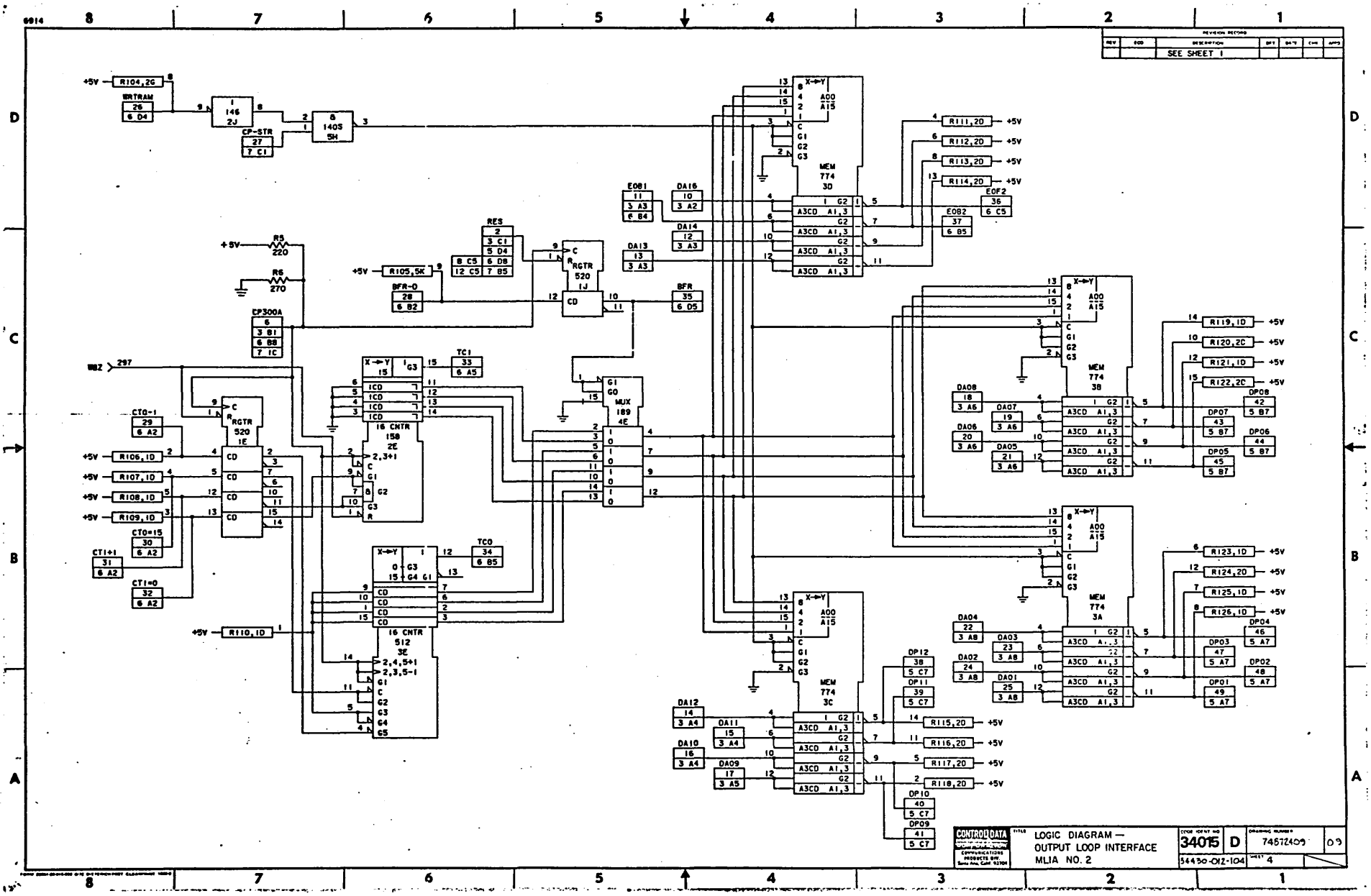
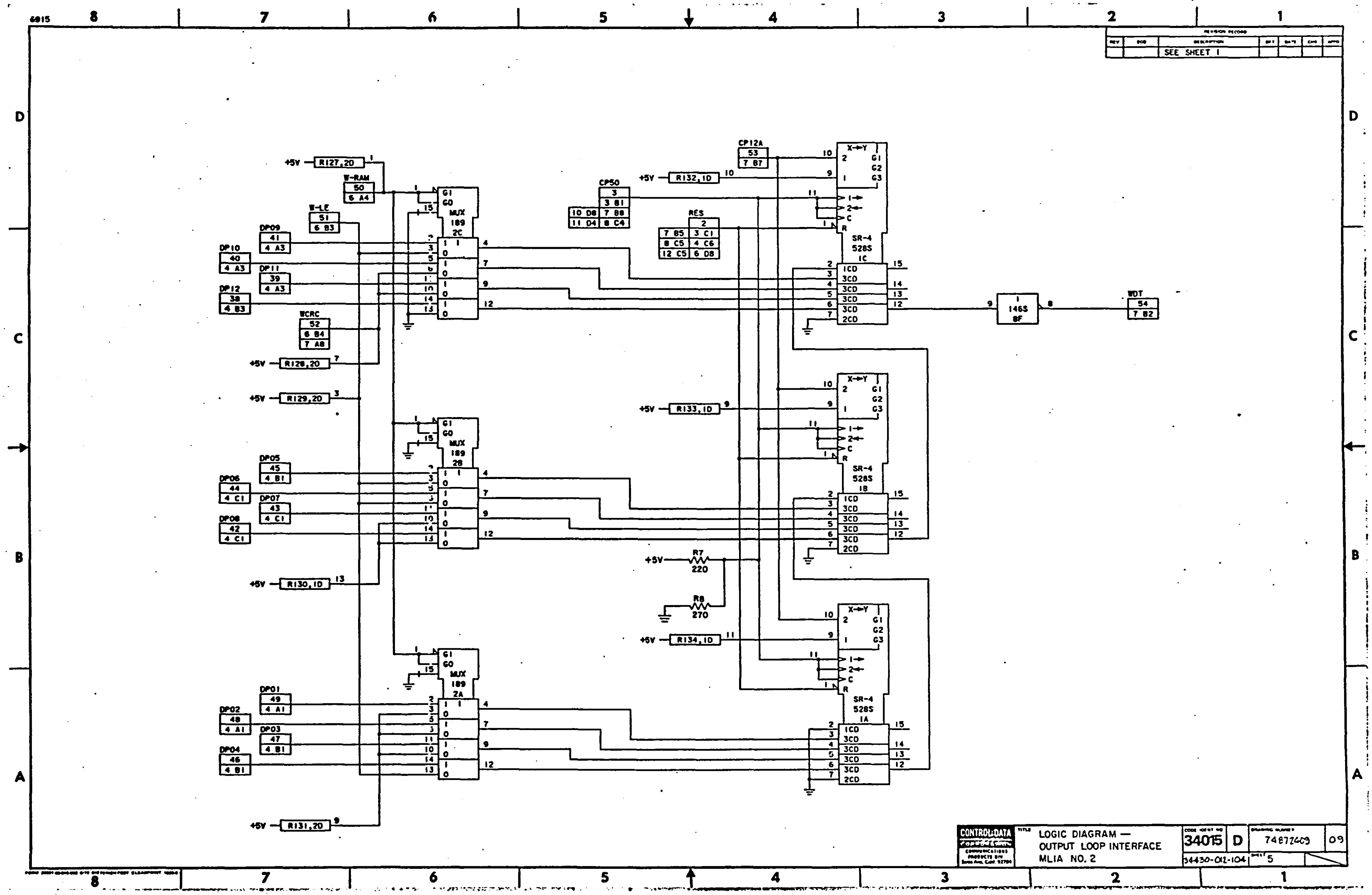
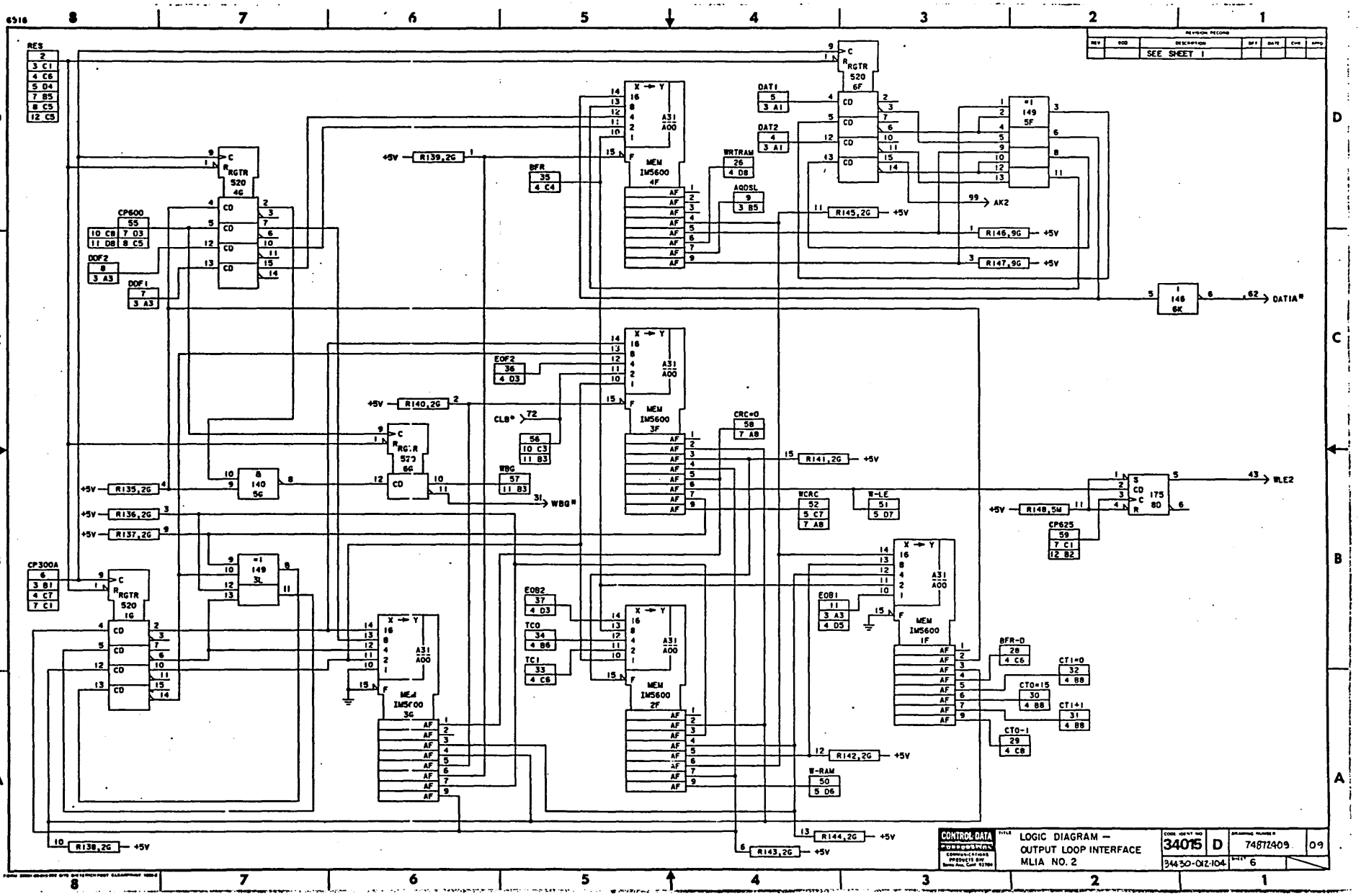
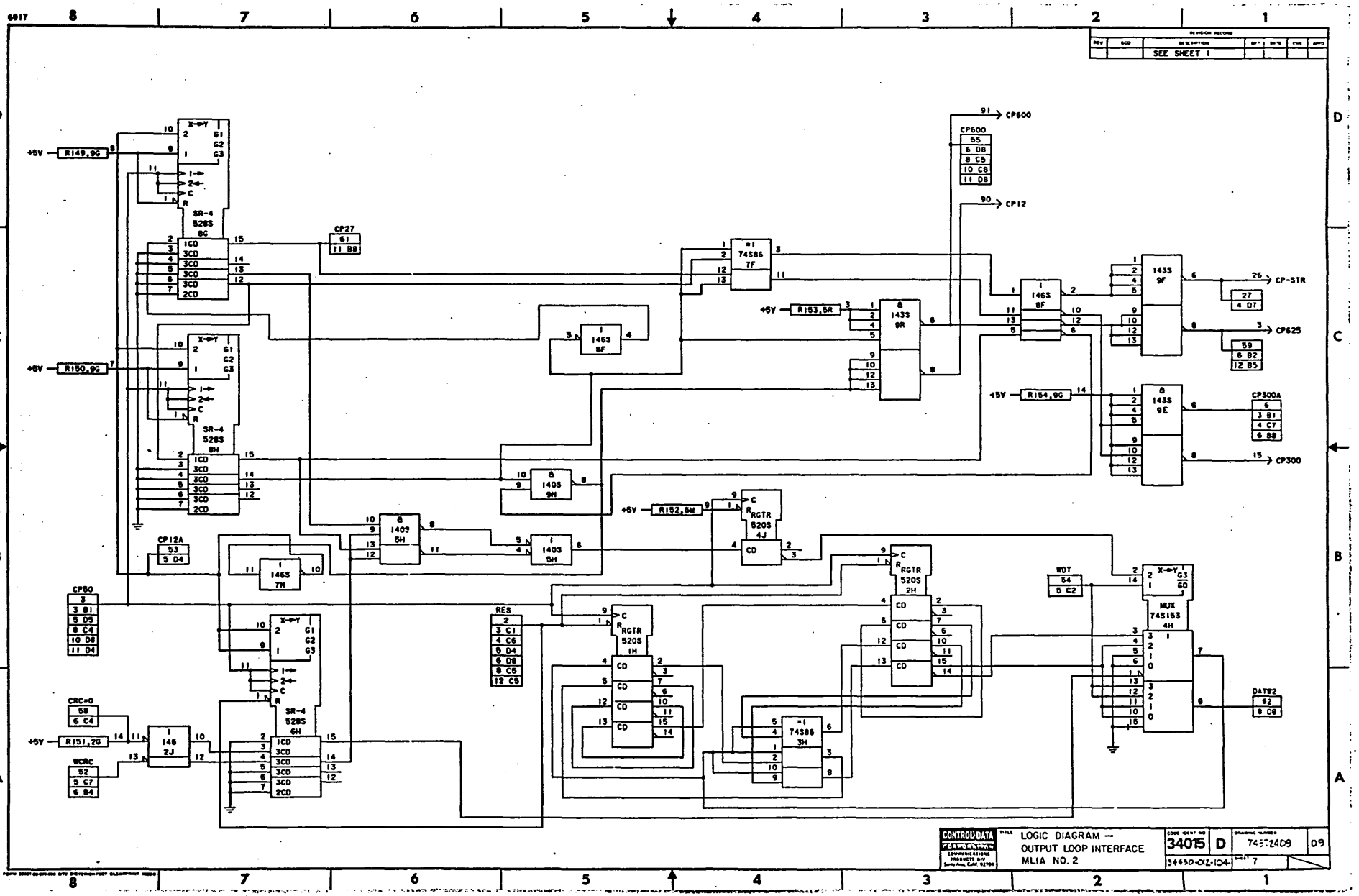
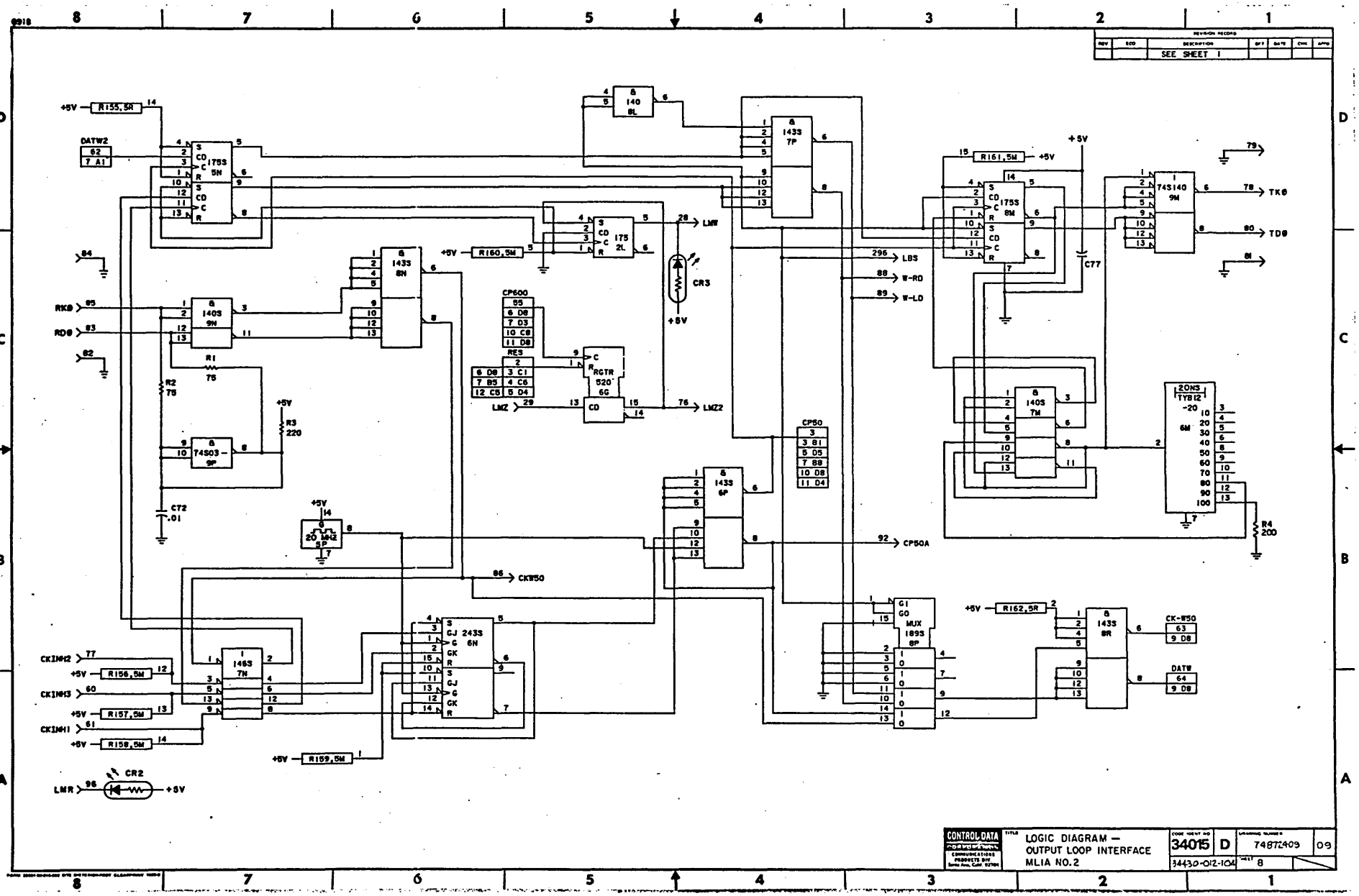
SD04
SD03
SD02
SD01
DFM16
DFM15
DFM14
DFM02
DFM12
DFM09
DFM11
DFM10
DFM07
DFM06
DFM03
DFM08
DFM05
DFM04
DFM01
DA16
DA14
DA13
DA12
DA11
DA10
DA09
DA07
DA06
DA05
DA04
DA03
DA02
DA01
EO81
DAT2
DAT1

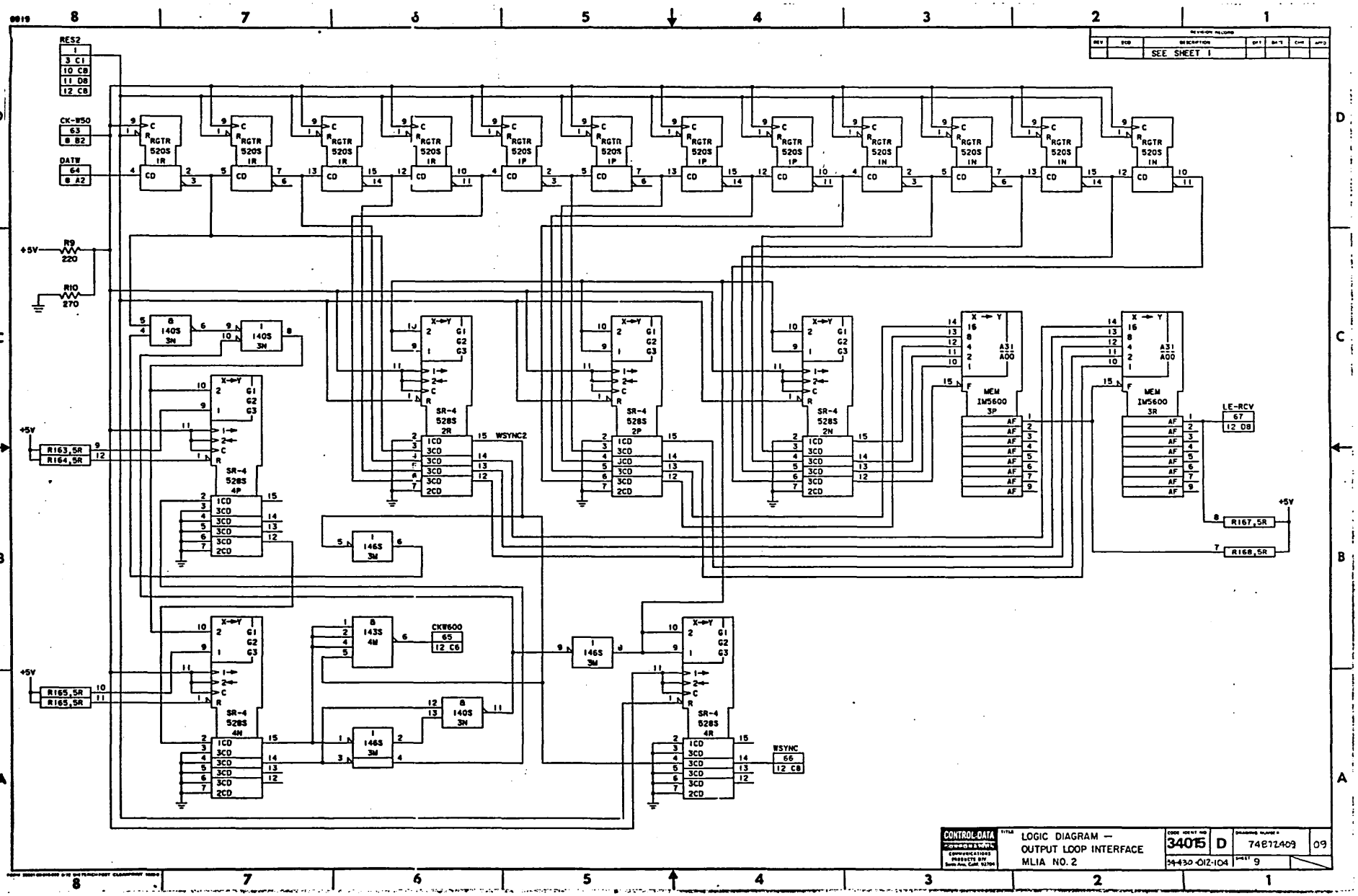

SEE SHEET 1
LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO. 2
CONTROL DATA
34015
D
74617409
09
SHEET 4
MEM 774 3D
MEM 774 3B
MEM 774 3A
MEM 774 3C
MUX 189 4E
16 CNTR 15B 2E
16 CNTR 512 3E
R REGTR 520 1E
R REGTR 520 1J
X→Y A00 A15
A3CD A1,3
+5V
R104,2G
R105,5K
R106,1D
R107,1D
R108,1D
R109,1D
R110,1D
R111,2D
R112,2D
R113,2D
R114,2D
R115,2D
R116,2D
R117,2D
R118,2D
R119,1D
R120,2C
R121,1D
R122,2C
R123,1D
R124,2D
R125,1D
R126,1D
R5 220
R6 270
BRTRAM
CP-STR
RES
BFR-0
BFR
CP300A
WBZ
CTO-1
CTI+1
CTI=0
CTO=15
TC1
TC0
EOF2
EOB2
EOB1
DA16
DA15
DA14
DA13
DA12
DA11
DA10
DA09
DA08
DA07
DA06
DA05
DA04
DA03
DA02
DA01
DP12
DP11
DP10
DP09
DP08
DP07
DP06
DP05
DP04
DP03
DP02
DP01

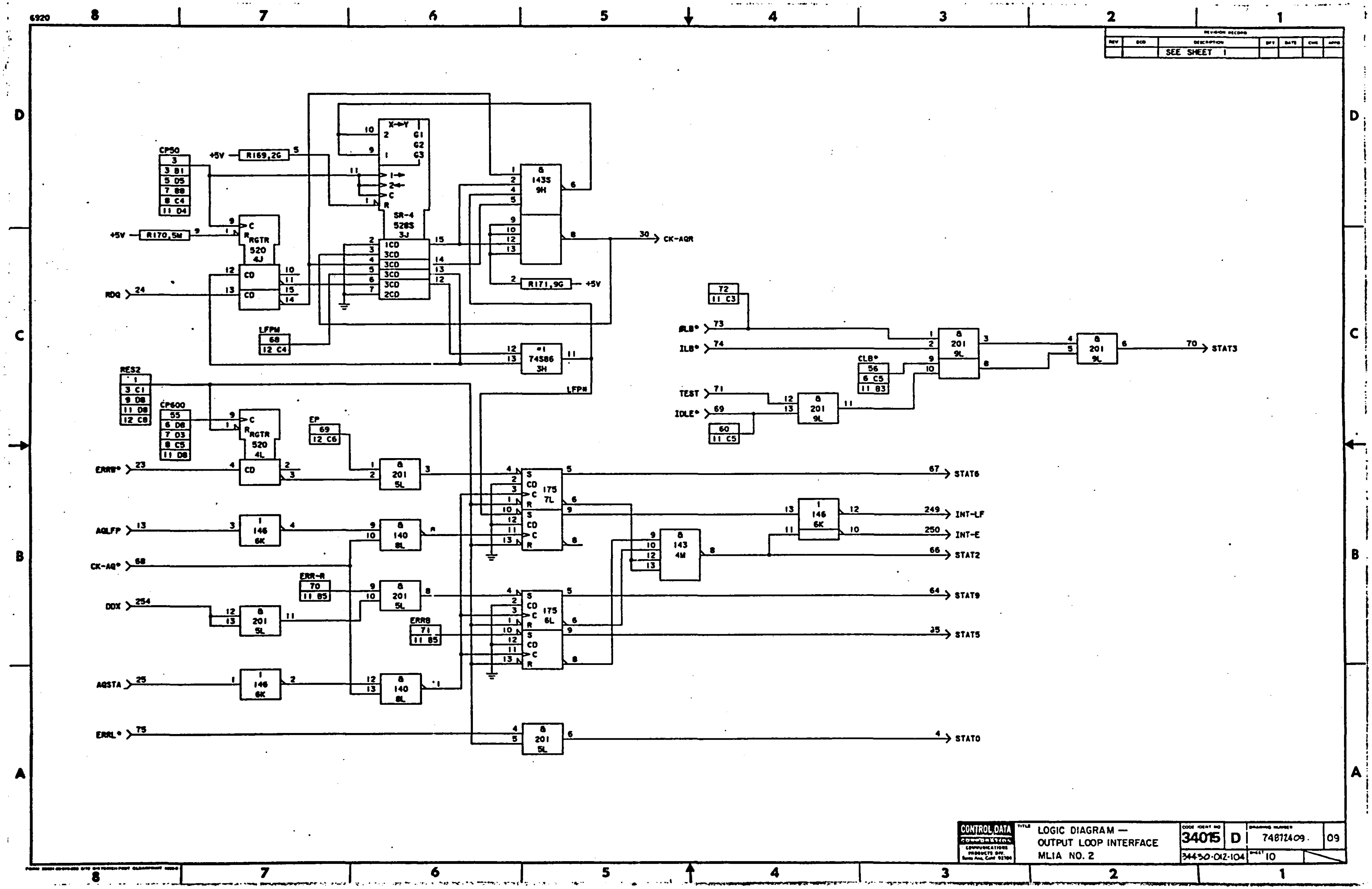

SEE SHEET 1
+5V
R127,20
W-RAM
50
6 A4
W-LE
51
6 B3
DP09
41
4 A3
DP10
40
4 A3
DP11
39
4 A3
DP12
38
4 B3
WCRC
52
6 B4
7 A8
R128,20
R129,20
MUX
189
2C
2B
2A
CP12A
53
7 B7
CP50
3
3 B1
10 D8
7 B8
11 D4
8 C4
R132,1D
RES
2
7 B5
3 C1
8 C5
4 C6
12 C5
6 D8
X↔Y
G1
G2
G3
SR-4
528S
1C
1B
1A
1CD
3CD
2CD
146S
8F
WDT
54
7 B2
R133,1D
DP05
45
4 B1
DP06
44
4 C1
DP07
43
4 C1
DP08
42
4 C1
R7
220
R8
270
R130,1D
R134,1D
DP01
49
4 A1
DP02
48
4 A1
DP03
47
4 B1
DP04
46
4 B1
R131,20
CONTROL DATA
LOGIC DIAGRAM —
OUTPUT LOOP INTERFACE
MLIA NO. 2
34015
D
74872409
09
34430-012-104
SHEET 5

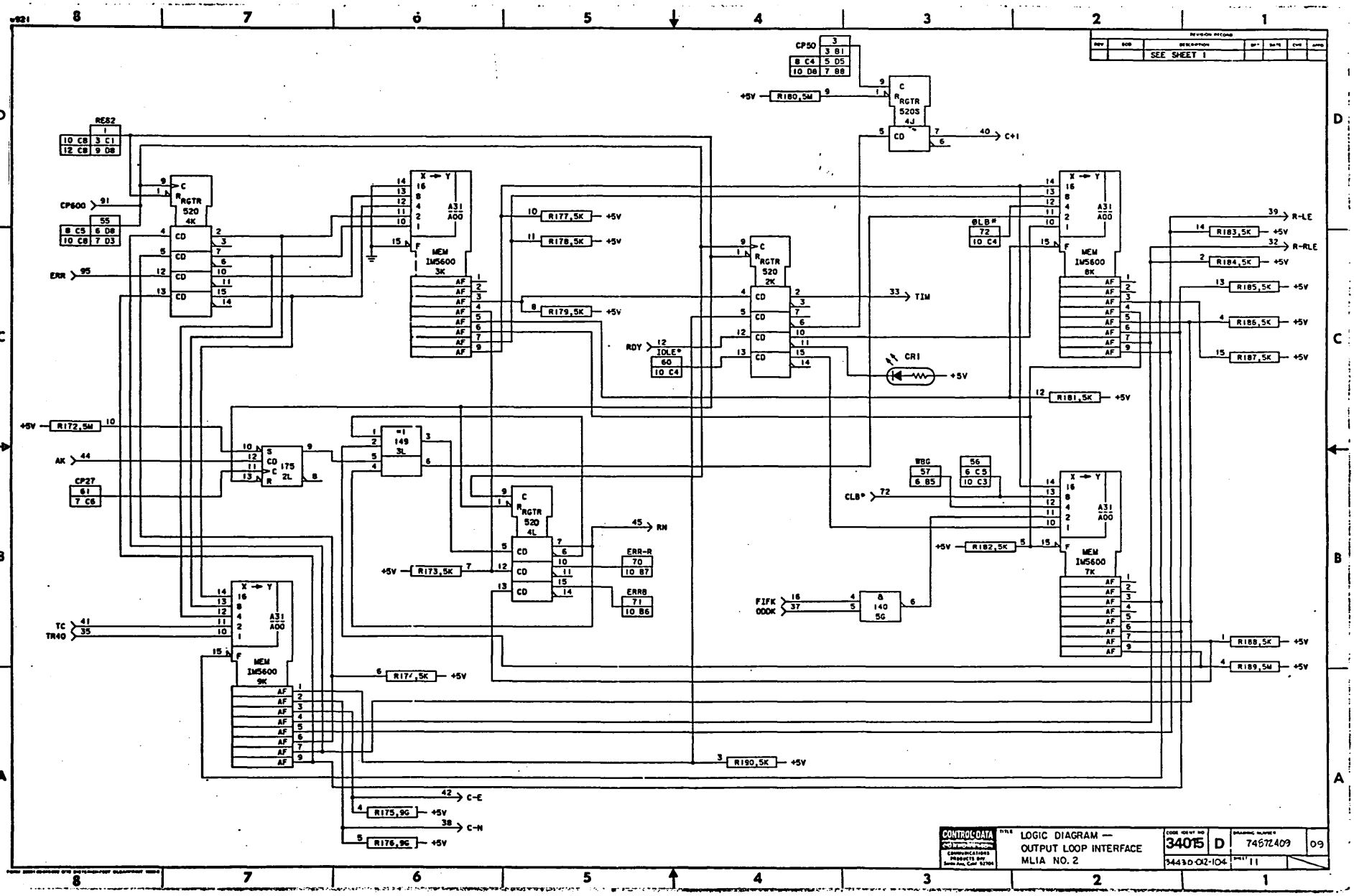

SEE SHEET 1
RES
CP600
DOF2
DOF1
CP300A
BFR
WRTRAM
AQDSL
DAT1
DAT2
EOF2
CLB*
WBG
CRC=0
WCRC
W-LE
EOB2
EOB1
TCO
TC1
BFR-D
CT1=0
CT0=15
CT1+1
CT0-1
W-RAM
CP625
WLE2
DATIA*
AK2
MEM IM5600 4F
MEM IM5600 3F
MEM IM5600 3G
MEM IM5600 2F
MEM IM5600 1F
RGTR 520 4G
RGTR 520 6F
RGTR 520 1G
RGTR 520 6G
149 5F
149 3L
140 5G
175 8D
146 6K
R139,2G
R140,2G
R135,2G
R136,2G
R137,2G
R138,2G
R141,2G
R142,2G
R143,2G
R144,2G
R145,2G
R146,9G
R147,9G
R148,5M
LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO. 2
CONTROL DATA
34015
D
74872409
09
34430-012-104
6

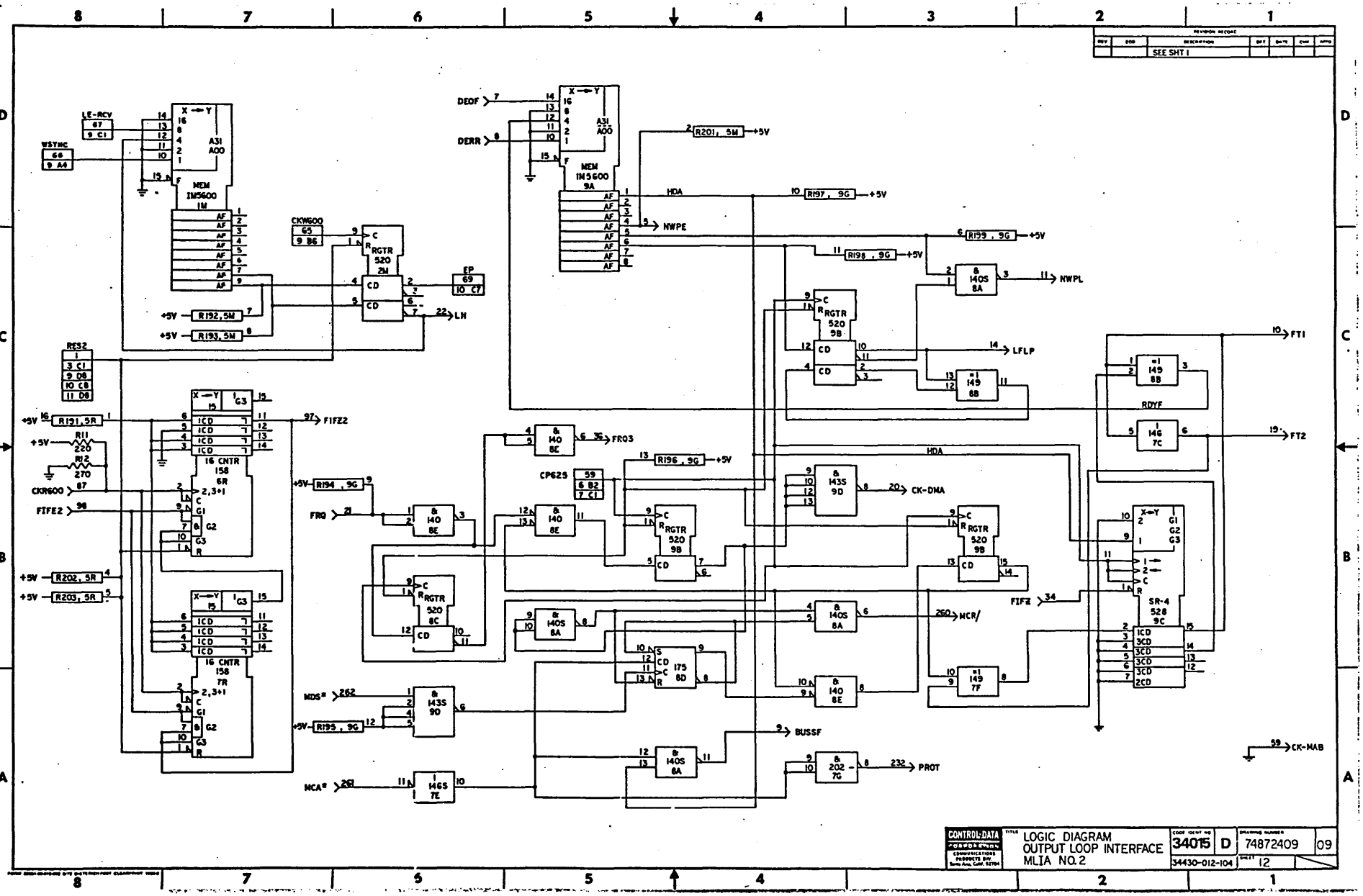

SEE SHEET 1
CONTROL DATA
LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO. 2
34015
D
74572409
09
SHEET 7
+5V
R149,9G
R150,9G
R151,2G
R152,5M
R153,5R
R154,9G
SR-4 528S 8G
SR-4 528S 8H
SR-4 528S 6H
CP27
CP600
CP12
CP-STR
CP625
CP300A
CP300
CP12A
CP50
RES
WDT
CRC=0
WCRC
DATA2
MUX 74S153 4H
RGTR 520S 4J
RGTR 520S 2H
RGTR 520S 1H


REVISION RECORD
SEE SHEET 1
+5V
R155,5R
DATW2
62
7 A1
R160,5M
R161,5M
R162,5R
R156,5M
R157,5M
R158,5M
R159,5M
CKINH2
CKINH3
CKINH1
LMR
CR2
CR3
LMW
LMZ
LMZ2
LBS
W-RD
W-LD
CP50
CP50A
CK-W50
DATW
TK0
TD0
C72
.01
C77
R1
R2
R3
R4
20 MHz
CONTROL DATA
LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO.2
34015
D
74872409
09
34430-012-104
SHEET 8


SEE SHEET 1
RES2
CK-W50
DATW
R9 220
R10 270
+5V
SR-4 528S 2R
SR-4 528S 2P
SR-4 528S 2N
SR-4 528S 3P
SR-4 528S 4P
SR-4 528S 4N
SR-4 528S 4R
MEM IM5600 3P
MEM IM5600 3R
WSYNC2
WSYNC
CKW600
LE-RCV
R163,5R
R164,5R
R165,5R
R165,5R
R167,5R
R168,5R
CONTROL DATA
LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO. 2
34015
D
74872409
09
34-430-012-104
SHEET 9

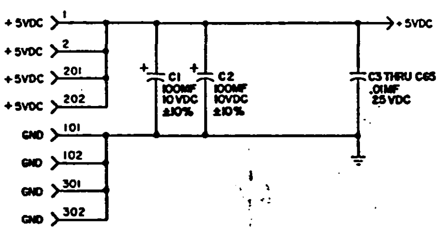

SEE SHEET 1
CP50
RES2
CP600
EP
ERR-R
ERRB
LFPM
SR-4
528S
3J
RGTR
520
4J
4L
143S
9H
74S86
3H
201
5L
9L
146
6K
140
8L
175
7L
6L
143
4M
R169,2G
R170,5M
R171,9G
+5V
RDQ
ERRB*
AQLFP
CK-AQ*
DDX
AQSTA
ERRL*
ALB*
ILB*
TEST
IDLE*
CLB*
CK-AQR
LFPM
STAT3
STAT6
INT-LF
INT-E
STAT2
STAT9
STAT5
STAT0
CONTROL DATA
LOGIC DIAGRAM —
OUTPUT LOOP INTERFACE
MLIA NO. 2
34015
D
74872409
09
34450-012-104
10

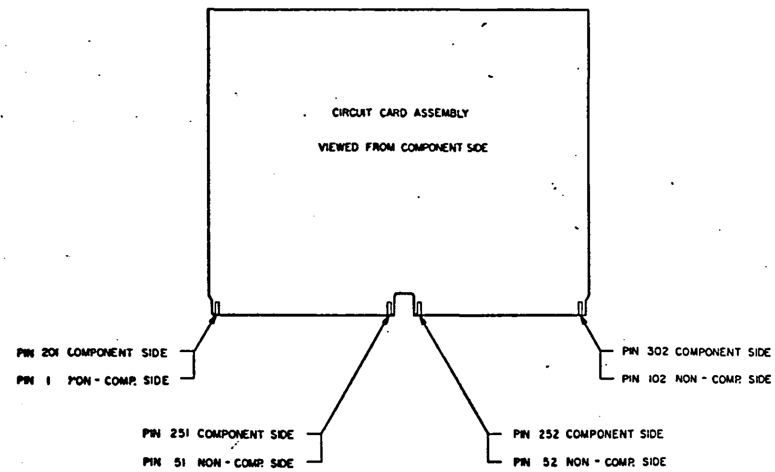

SEE SHEET 1
CP50
+5V R180,5W
RGTR 520S 4J
C+1
RE82
CP600
ERR
RGTR 520 4K
MEM IM5600 3K
R177,5K +5V
R178,5K +5V
R179,5K +5V
RGTR 520 2K
TIM
RDY
IOLE*
CR1 +5V
MEM IM5600 8K
R181,5K +5V
R-LE
R-RLE
R183,5K +5V
R184,5K +5V
R185,5K +5V
R186,5K +5V
R187,5K +5V
+5V R172,5W
AK
CP27
175 2L
RGTR 520 4L
RN
ERR-R
ERR8
+5V R173,5K
WBG
CLB*
MEM IM5600 7K
+5V R182,5K
FIFK
OOOK
R188,5K +5V
R189,5W +5V
TC
TR40
MEM IM5600 9K
R174,5K +5V
R190,5K +5V
C-E
R175,9G +5V
C-N
R176,9G +5V
CONTROL DATA
LOGIC DIAGRAM — OUTPUT LOOP INTERFACE MLIA NO. 2
34015
D
74672409
09
3443D-012-104
11


REVISION RECORD
SEE SHT 1
LE-RCV
WSYNC
MEM IM5600 1M
MEM IM5600 9A
DEOF
DERR
HDA
NWPE
NWPL
CKW600
EP
LN
RES2
R191,5R
R202,5R
R203,5R
R11 220
R12 270
CKR600
FIFE2
FIFZ2
FRQ
FR03
CPG25
RDYF
FT1
FT2
LFLP
FIFZ
MCR/
CK-DMA
MDS*
MCA*
BUSSF
PROT
CK-MAB
16 CNTR 15B 6R
16 CNTR 15B 7R
SR-4 52B 9C
CONTROL DATA
TITLE LOGIC DIAGRAM OUTPUT LOOP INTERFACE MLIA NO.2
34015 D
74872409 09
34430-012-104
SHEET 12

9676861001

REV	ECO	DESCRIPTION	DFT / DATE	APP
02	05336	CL B PRERELEASE	JTP 1-7-75	
03	05443	SEE ECO	JTP	
04	05751	SEE ECO		
05	05992	SEE ECO		
06	06470	INITIAL RELEASE		





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: .01 MF, 25 VDC, +80-20%
   ALL DIODES: DIALCO 547-2003, 5V, 6MA
2. COMPONENT ASSEMBLY 74872417
3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL - IN - LINE	14	7
16 PIN DUAL - IN - LINE	16	8

NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

4AAY

DO NOT SCALE DRAWING

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV

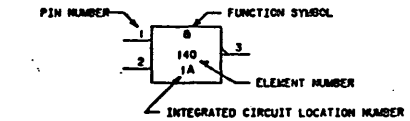
LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3

D 34015 74872418

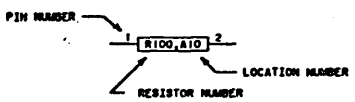
SCALE NONE 34440-012-104 SHEET 1 OF 9

REV	ECO	DESCRIPTION	BY	DATE	CHK	APPD
		SEE SHEET 1				

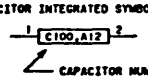
CIRCUIT ELEMENT SYMBOLOGY

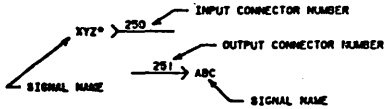


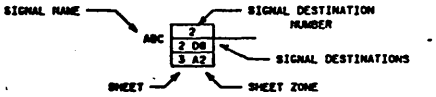
RESISTOR INTEGRATED SYMBOLOGY

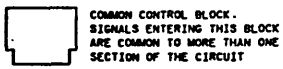


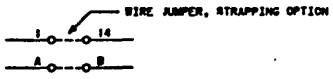
CAPACITOR INTEGRATED SYMBOLOGY

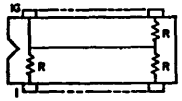












LC RESISTOR PACK
LOCATION U26,U53,U74,U100
1.5K,1/8W,± 2%

IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
143	7440	TTL DUAL 4-INPUT NAND BUFFER
143S	74S40	TTL DUAL 4-INPUT NAND BUFFER
140	7400	TTL QUAD 2-INPUT NAND GATE
146	7404	TTL HEX INVERTER
148	7402	TTL QUAD 2-INPUT NOR GATE
149	7486	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
158	74161	COUNTER, TTL 4-BIT BINARY
175	7474	TTL DUAL D-TYPE F/F
189	74157	MULTIPLEXER, TTL QUAD 2-INPUT
202	7403	TTL QUAD 2-INPUT NAND GATE (OPEN COLL)
505	74151	MULTIPLEXER, TTL 8-INPUT
512	74191	COUNTER, TTL 4-BIT BINARY UP-DOWN
520	74175	LATCH, TTL 4-BIT D-TYPE
521	7483	ADDER, TTL 4-BIT BINARY FULL
524	7485	COMPARATOR, TTL 4-BIT MAGNITUDE
528	74194	REG. TTL 4-BIT SHIFT
—	IM5600	PROGRAMMED READ ONLY MEMORY (32 X 8)

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
1⊓	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A 'D' INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT: ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT: ALL HIGH STATE OUTPUTS ARE INHIBITED
⌐	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→|	SHIFT RIGHT (OR DOWN)
|←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
▷	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM '0' STATE TO '1' STATE
—/—	NON-STANDARD LOGIC LEVEL
—≈—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PARAMETER CONTROL
—o—	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
—o	INHIBIT DESIGNATOR

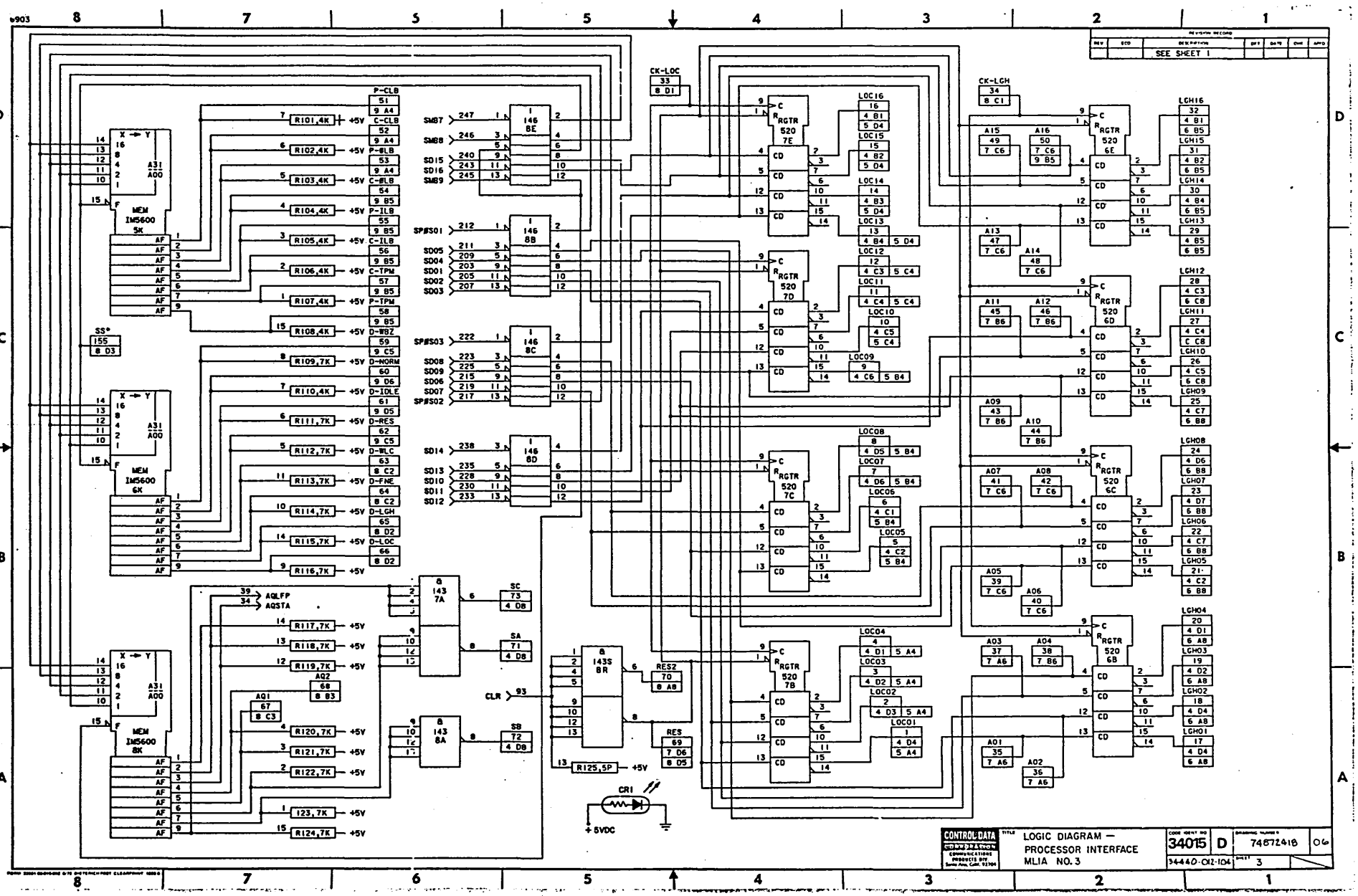
FUNCTION ABBREVIATIONS

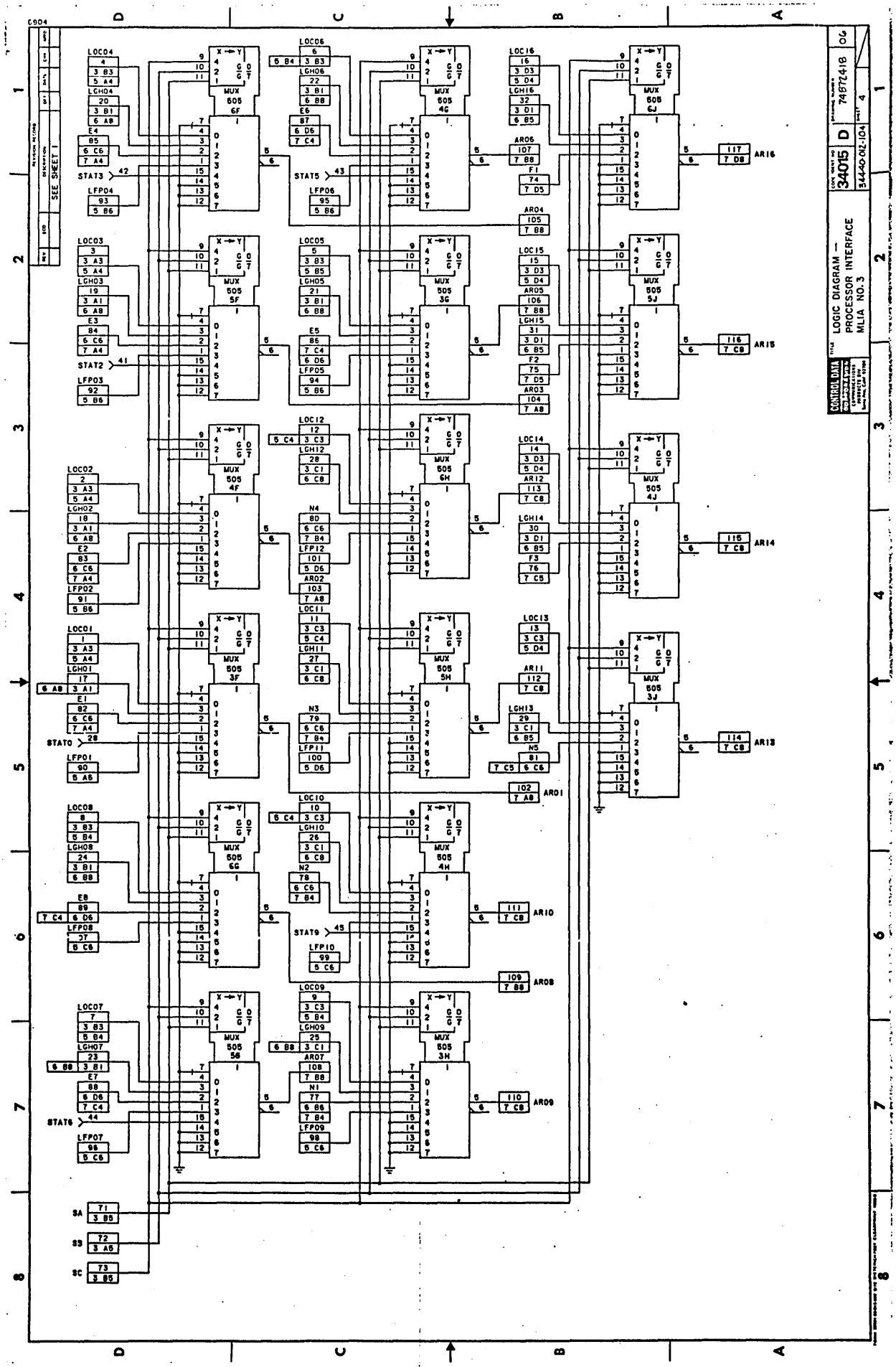
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

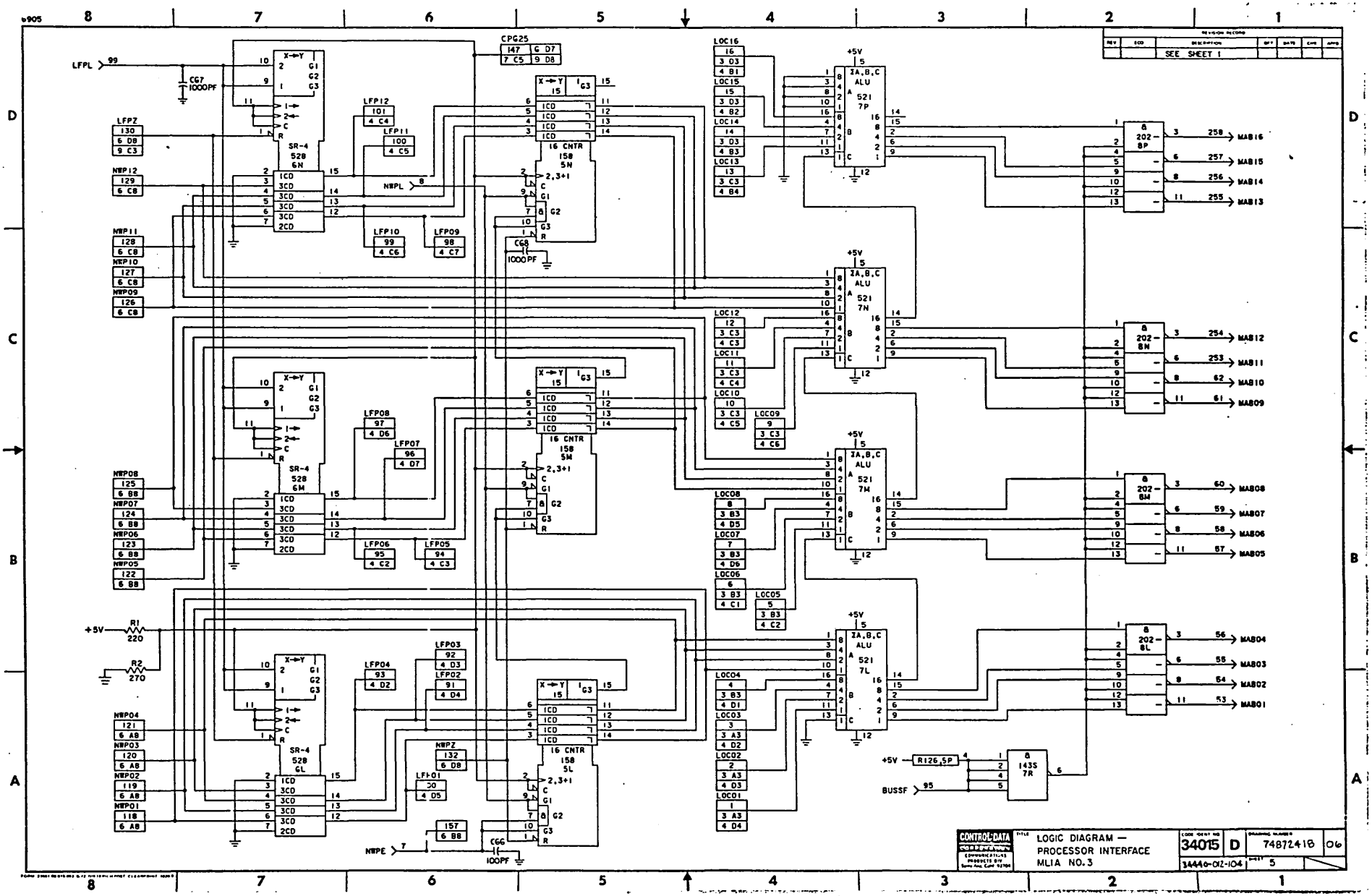
CONTROL DATA — TITLE: LOGIC DIAGRAM— KEY TO SYMBOLS

CODE IDENT NO 34015 | D | DRAWING NUMBER 74872418 | 06

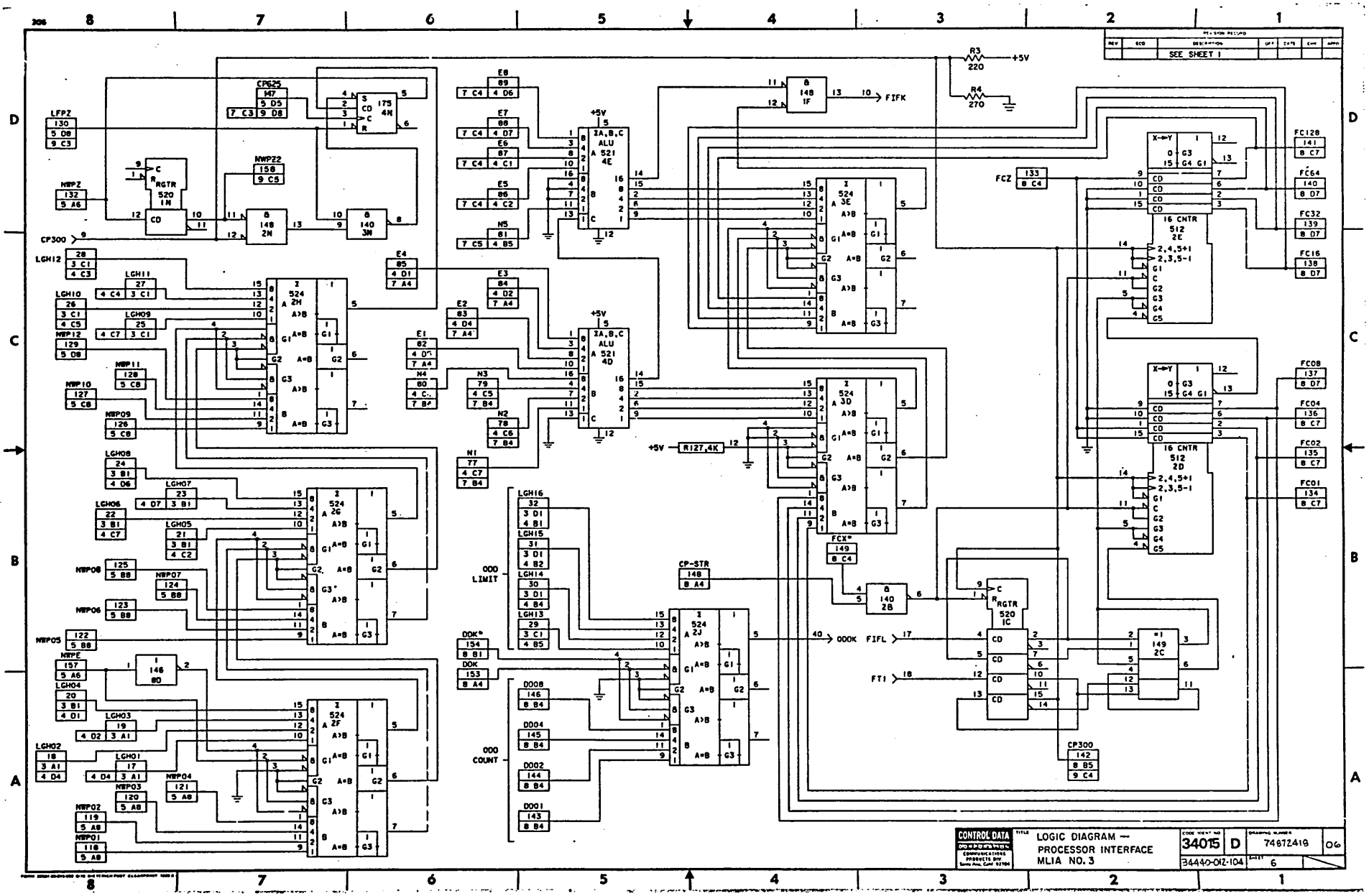
34440-92-104 | SHEET 2

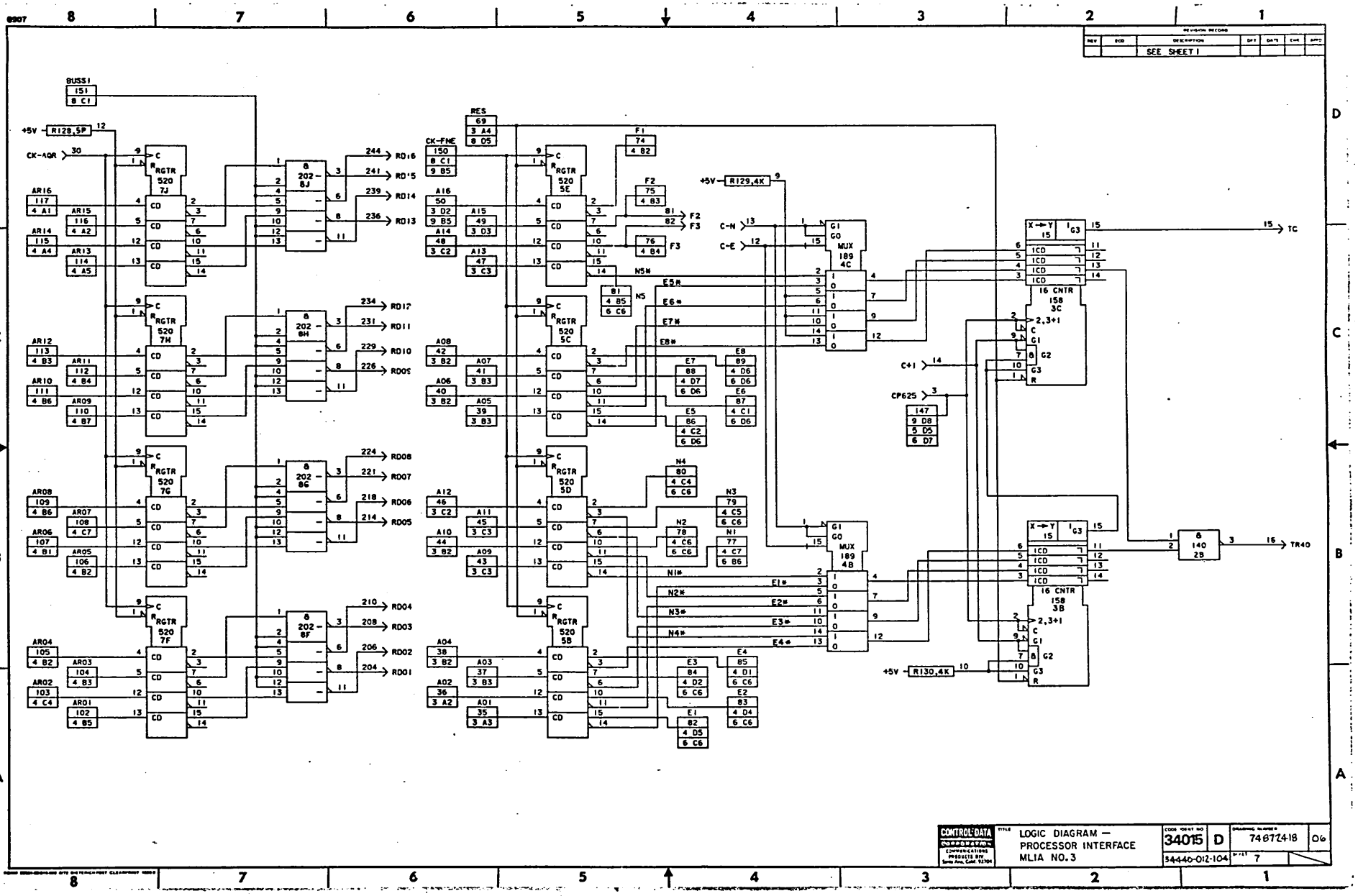

SEE SHEET 1
CK-LOC
CK-LGH
P-CLB
MEM IM5600 5K
MEM IM5600 6K
MEM IM5600 8K
R101,4K
R102,4K
R103,4K
R104,4K
R105,4K
R106,4K
R107,4K
R108,4K
R109,7K
R110,4K
R111,7K
R112,7K
R113,7K
R114,7K
R115,7K
R116,7K
R117,7K
R118,7K
R119,7K
R120,7K
R121,7K
R122,7K
123,7K
R124,7K
R125,5P
+5V
AQLFP
AQSTA
CLR
CR1
+5VDC
RGTR 520 7E
RGTR 520 7D
RGTR 520 7C
RGTR 520 7B
RGTR 520 6E
RGTR 520 6D
RGTR 520 6C
RGTR 520 6B
CONTROL DATA
LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3
34015
D
74872418
06
SHEET 3


LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO.3
CONTROL DATA
34015
74972418
34440-02-104
SEE SHEET 1
MUX 505 6F
MUX 505 4G
MUX 505 6J
MUX 505 5F
MUX 505 3G
MUX 505 5J
MUX 505 4F
MUX 505 6H
MUX 505 4J
MUX 505 3F
MUX 505 5H
MUX 505 3J
MUX 505 6G
MUX 505 4H
MUX 505 5G
MUX 505 3H
LOC04
LOC06
LOC16
LOC03
LOC05
LOC15
LOC02
LOC12
LOC14
LOC01
LOC11
LOC13
LOC08
LOC10
LOC07
LOC09
STAT3
STAT5
STAT2
STAT0
STAT9
STAT6
AR16
AR15
AR14
AR13
AR12
AR11
AR10
AR09
AR08
AR07
AR06
AR05
AR04
AR03
AR02
AR01
SA
SB
SC



CONTROL DATA	LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3	34015 D	74872418 06
		34440-012-104	SHEET 5


SEE SHEET 1
LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3
CONTROL DATA
34015
D
74672416
06
34440-012-104
SHEET 6
16 CNTR 512 2E
16 CNTR 512 2D
520 1N RGTR
520 1C RGTR
524 2M
524 2G
524 2F
524 2J
524 3E
524 3D
ALU 521 4E
ALU 521 4D
175 4N
148 2N
140 3N
148 1F
140 2B
146 8D
149 2C
R3 220 +5V
R4 270
R127,4K +5V
FIFK
FIFL
FCX*
FCZ
CP-STR
CP300
ODD LIMIT
ODD COUNT
ODDK*
DDK
FC128
FC64
FC32
FC16
FC08
FC04
FC02
FC01
LFPZ
NWPZ
NWPZ2
LGH12
LGH11
LGH10
LGH09
LGH08
LGH07
LGH06
LGH05
LGH04
LGH03
LGH02
LGH01
LGH16
LGH15
LGH14
LGH13
NWP12
NWP11
NWP10
NWP09
NWP08
NWP07
NWP06
NWP05
NWP04
NWP03
NWP02
NWP01
NWPE
E8
E7
E6
E5
E4
E3
E2
E1
N5
N4
N3
N2
N1
D008
DD04
DD02
DD01

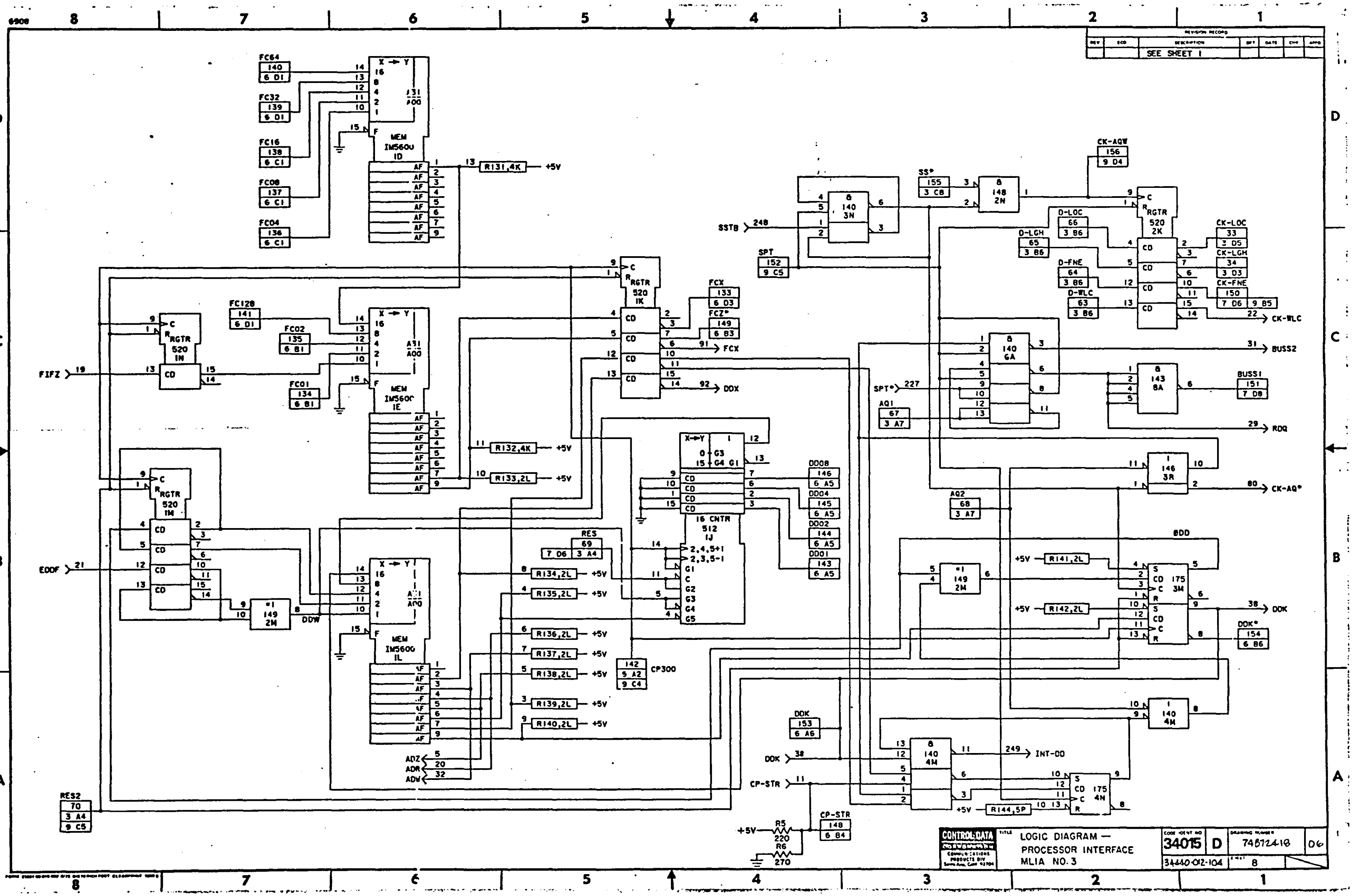


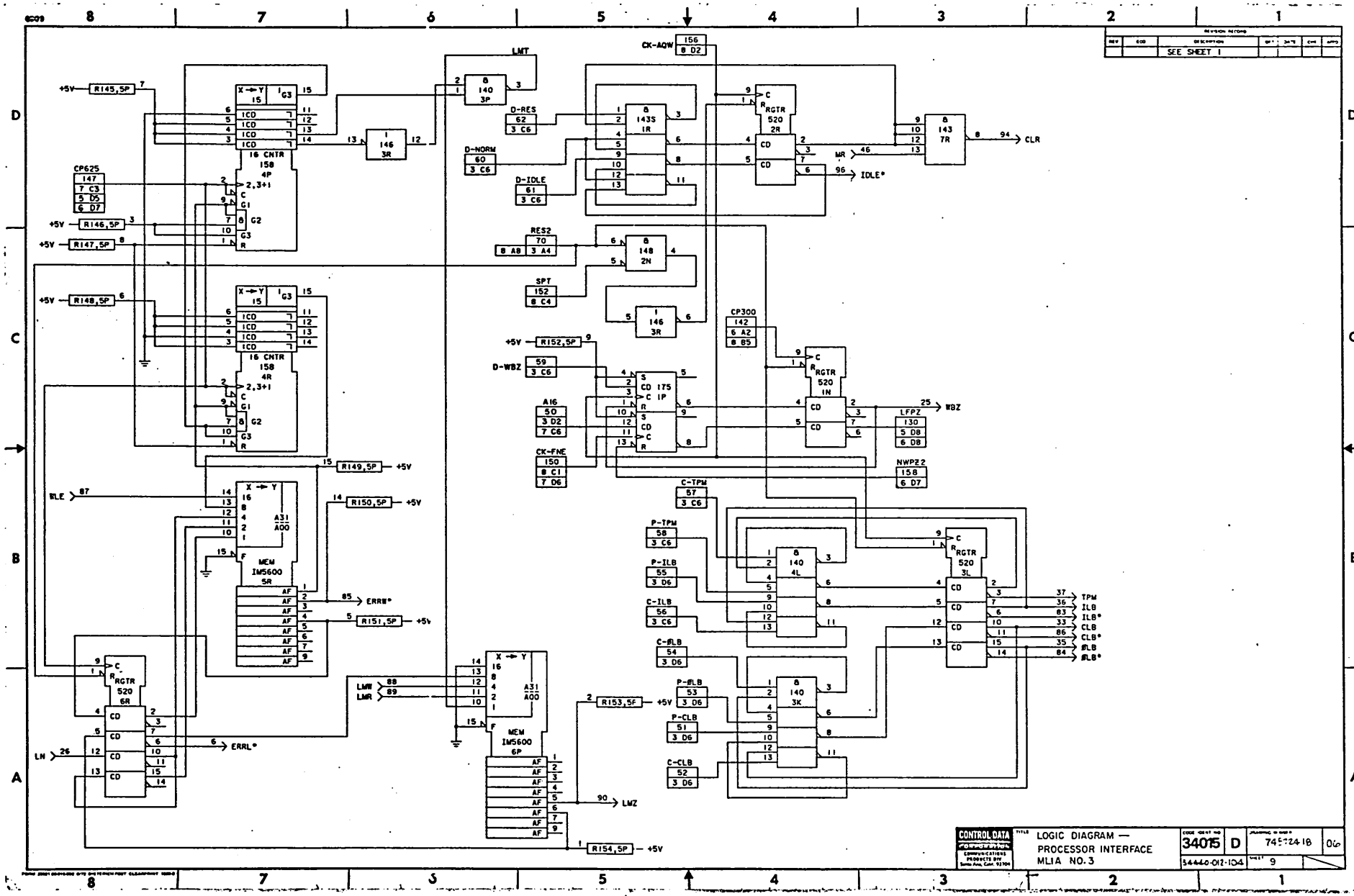
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
		SEE SHEET 1				

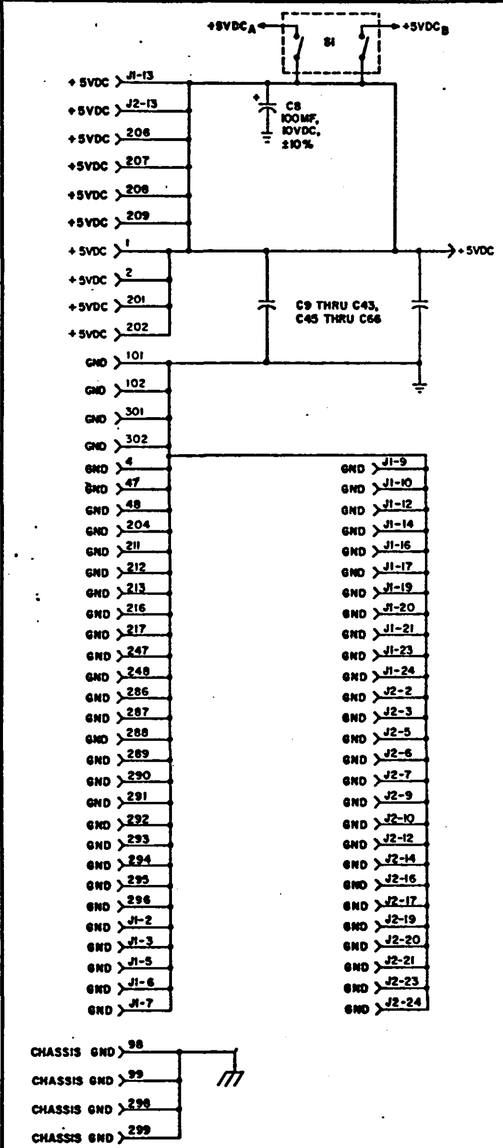
CONTROL DATA CORPORATION
COMMUNICATIONS PRODUCTS DIV.

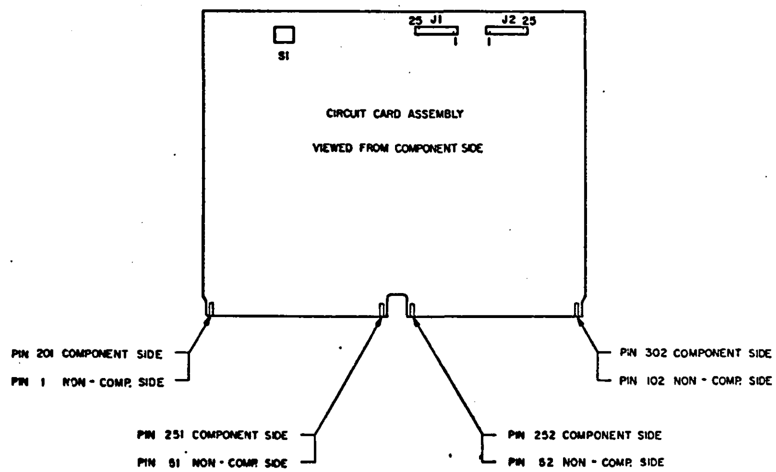
LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3

CODE IDENT NO		DRAWING NUMBER	
34015	D	7487Z418	06
54440-012-104		SHEET 7	


SEE SHEET 1
FC64
FC32
FC16
FC08
FC04
FC128
FC02
FC01
MEM IM5600 ID
MEM IM5600 IE
MEM IM5600 IL
RGTR 520 IN
RGTR 520 IK
RGTR 520 IM
RGTR 520 2K
FIFZ
EDOF
DDW
FCX
FCZ*
DDX
16 CNTR 512 IJ
DD08
DD04
DD02
DD01
RES
RES2
CP300
SS*
SSTB
SPT
SPT*
AQ1
AQ2
CK-AQW
D-LOC
D-LGH
D-FNE
D-WLC
CK-LOC
CK-LGH
CK-FNE
CK-WLC
BUSS2
BUSS1
RDQ
CK-AQ*
BDD
DDK
DDK*
INT-00
CP-STR
ADZ
ADR
ADW
+5V
LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO. 3
CONTROL DATA
34015
D
74872418
06
34440-012-104
8


SEE SHEET 1
CK-AQW
LMT
D-RES
D-NORM
D-IDLE
RES2
SPT
CP625
CP300
D-WBZ
A16
CK-FNE
LFPZ
NWPZ2
C-TPM
P-TPM
P-ILB
C-ILB
C-RLB
P-RLB
P-CLB
C-CLB
WLE
LN
LMW
LMR
CLR
IDLE*
WBZ
TPM
ILB
ILB*
CLB
CLB*
RLB
RLB*
ERRH*
ERRL*
LWZ
MEM IM5600 5R
MEM IM5600 6P
16 CNTR 158 4P
16 CNTR 158 4R
RGTR 520 2R
RGTR 520 1N
RGTR 520 3L
RGTR 520 3K
RGTR 520 6R
CD 175 1P
CONTROL DATA
LOGIC DIAGRAM — PROCESSOR INTERFACE MLIA NO.3
34015
D
74572418
06
54440-012-104
9





REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPR
00	05418	INITIAL RELEASE				
01	06452	INITIAL RELEASE	G.D.			

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES ±5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: .01MF, 25VDC, +80-20%

2. COMPONENT ASSEMBLY 74872526

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL - IN - LINE	14	7
16 PIN DUAL - IN - LINE	16	8

NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

DO NOT SCALE DRAWING

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV

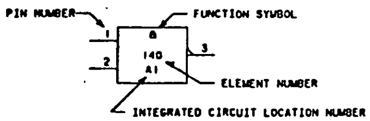
S. Peterson

LOGIC DIAGRAM — LOOP MULTIPLEXER

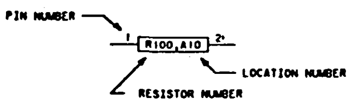
D 34015 74872527

SCALE NONE 34490-012-104 SHEET 1 OF 13

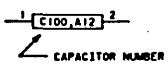
CIRCUIT ELEMENT SYMBOLOGY

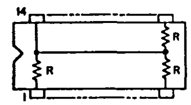


RESISTOR INTEGRATED SYMBOLOGY

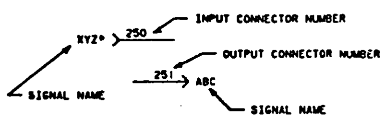


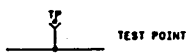
CAPACITOR INTEGRATED SYMBOLOGY

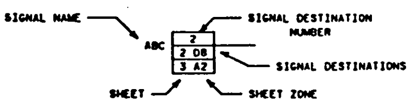


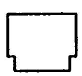


I.C. RESISTOR PACK
1K, 1.5W, ±2%
LOCATION: D7, L4, S6

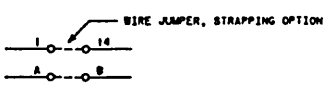








COMMON CONTROL BLOCK. SIGNALS ENTERING THIS BLOCK ARE COMMON TO MORE THAN ONE SECTION OF THE CIRCUIT



IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
—	4049	HEX BUFFER-INVERTER
200	7406	DRIVER, HEX INVERTER-BUFFER
—	7407	HEX BUFFER-DRIVER
204	7438	TTL QUAD 2-INPUT NAND BUFFER
507	7442	DECODER, TTL BCD-TO-DECIMAL
193	74123	MULTIVIBRATOR, TTL DUAL RETRIGGER
532	74148	ENCODER, TTL 8-INPUT PRIORITY
531	74150	MUX, TTL 16-INPUT
158	74161	COUNTER, TTL 4-BIT BINARY
—	74173	REGISTER, 4-BIT D-TYPE
500	74193	COUNTER, TTL 4-BIT BINARY UP-DOWN
—	74279	QUAD NOR R-S LATCH
140S	74S00	TTL QUAD 2-INPUT NAND
—	74S02	TTL QUAD 2-INPUT NOR
146S	74S04	TTL HEX INVERTER
141S	74S10	TTL TRIPLE 3-INPUT NAND
213S	74S11	TTL TRIPLE 3-INPUT AND
208S	74S20	TTL DUAL 4-INPUT NAND
206S	74S30	TTL 8-INPUT NAND
204S	74S38	TTL QUAD 2-INPUT NAND BUFFER
205S	74S64	TTL 4-WIDE 4-2-3-2 IN AND-OR-INVERT
175S	74S74	TTL DUAL D-TYPE F/F
149S	74S86	TTL QUAD 2-INPUT OR
243S	74S112	TTL DUAL J-K NET F/F
—	74S134	TTL 12-INPUT NAND
—	74S140	TTL DUAL 4-INPUT NAND
189S	74S157	MUX, TTL QUAD 2-INPUT
—	74S174	HEX DUAL F/F
520S	74S175	LATCH, TTL 4-BIT D-TYPE
—	74S260	DUAL 5-INPUT NOR

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
		SEE SHEET 1				

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
	SCHMITT TRIGGER
	ONE-SHOT MULTIVIBRATOR
	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X → Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT: ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT: ALL HIGH STATE OUTPUTS ARE INHIBITED
⌐	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS

◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
	POLARITY CONVENTION, NEGATIVE POTENTIAL
	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
	NON-STANDARD LOGIC LEVEL
	ANALOG OR NON-LOGIC LEVEL
	VARIABLE PARAMETER CONTROL
	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
	INHIBIT DESIGNATOR

FUNCTION ABBREVIATIONS

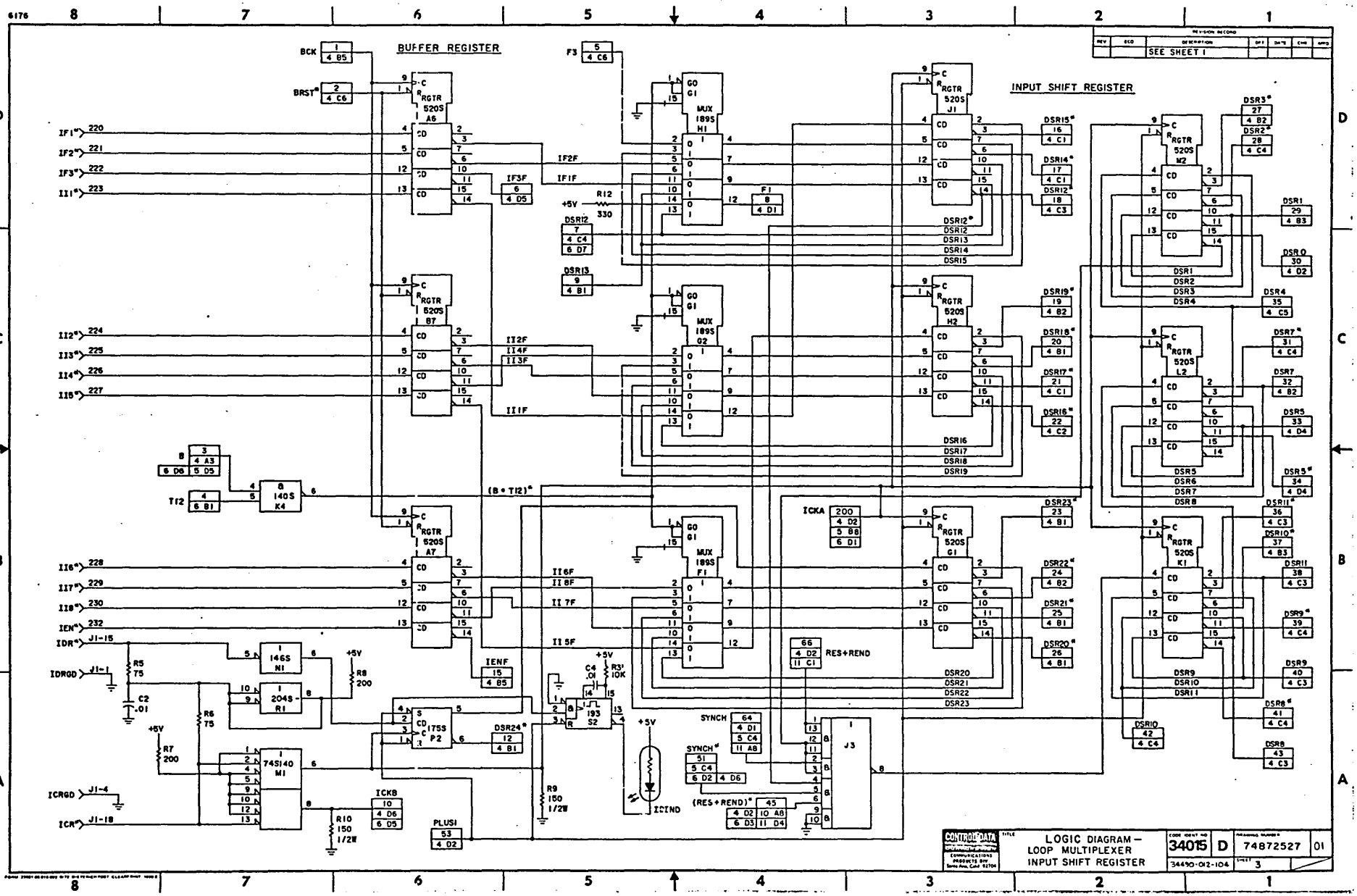
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX. NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

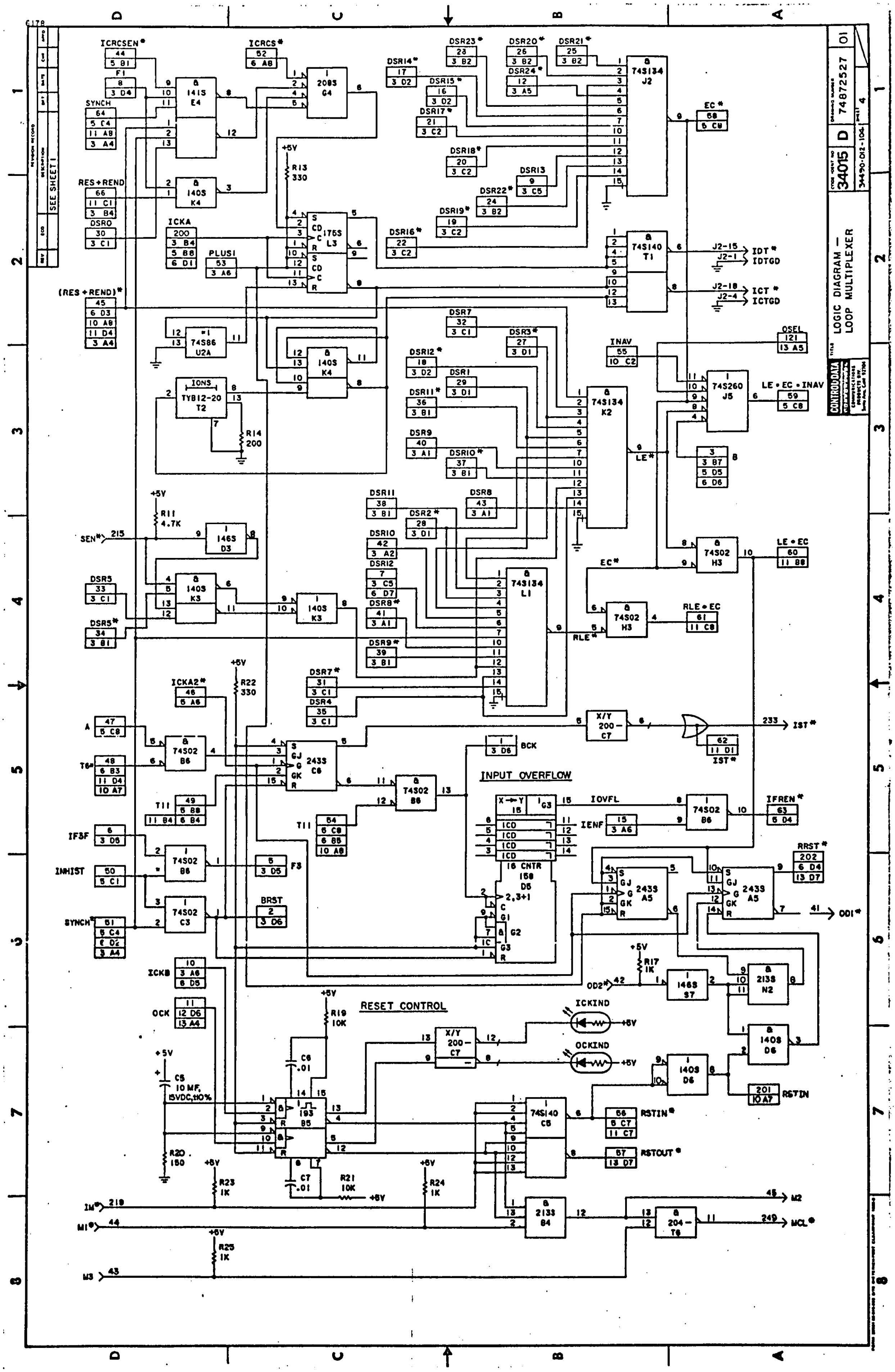
CONTROL DATA COMMUNICATIONS PRODUCTS DIV

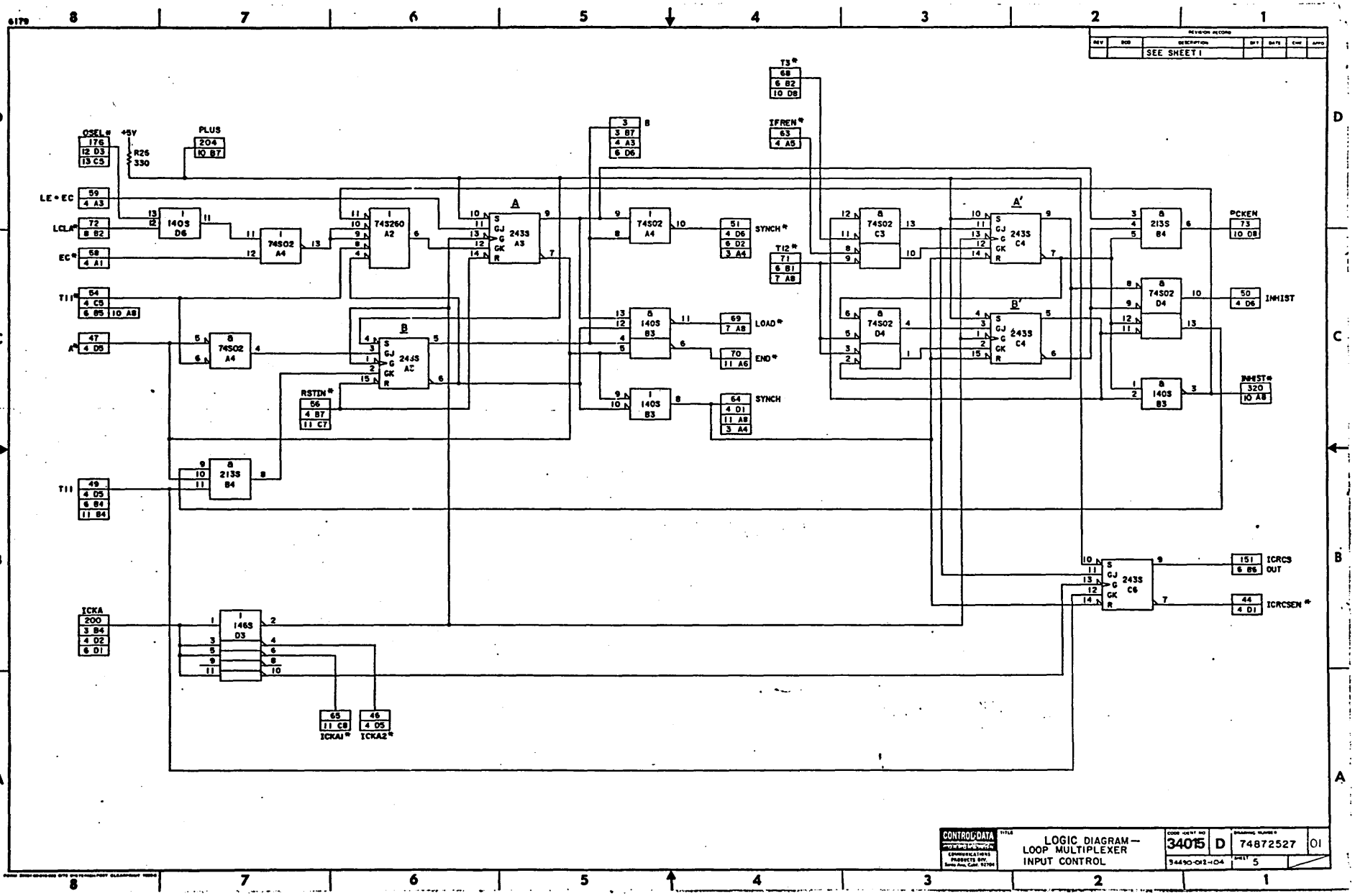
LOGIC DIAGRAM— KEY TO SYMBOLS

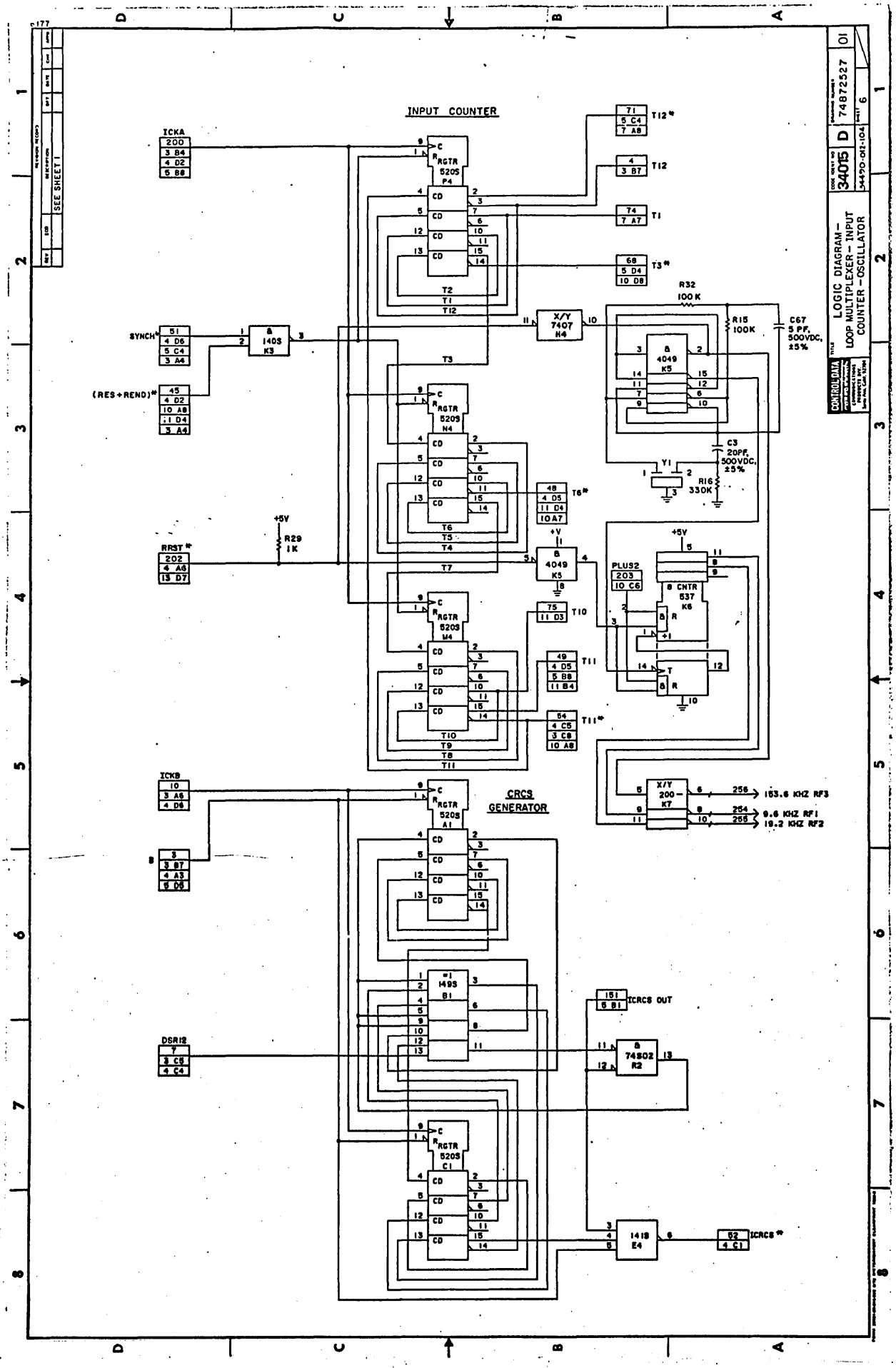
34015 D 74872527 01

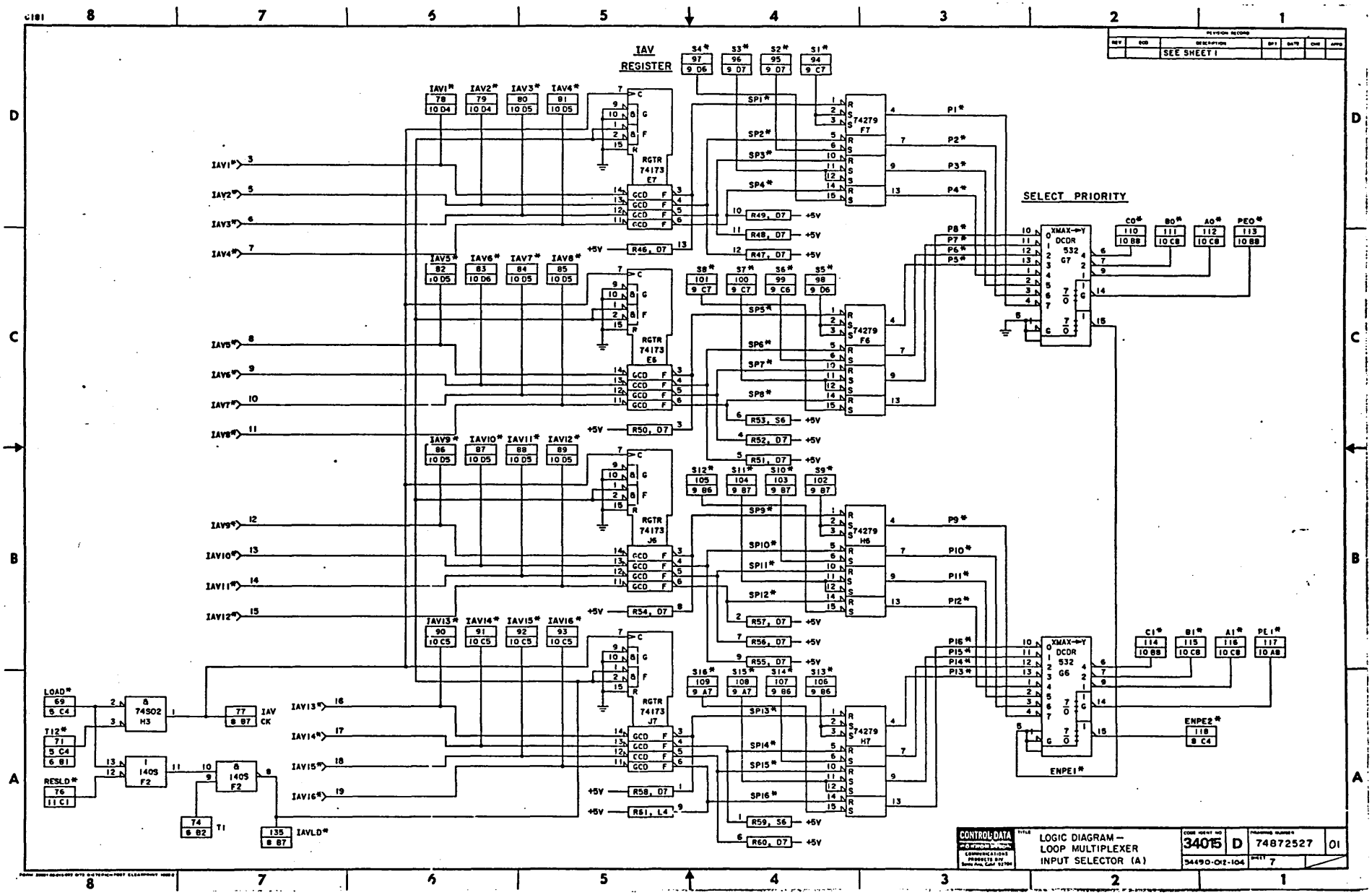
SHEET 2

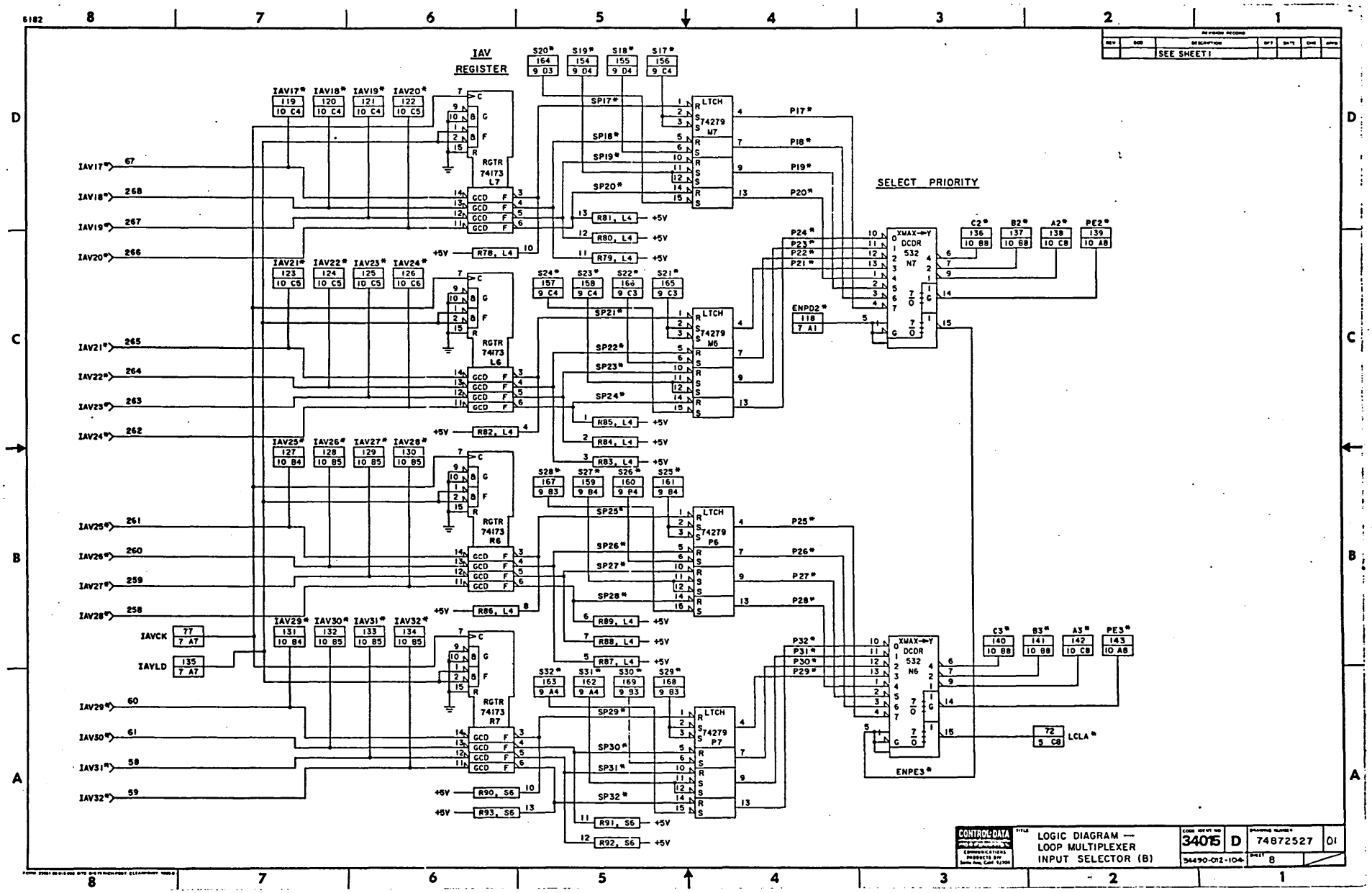

BUFFER REGISTER
INPUT SHIFT REGISTER
BCK
BRST*
F3
IF1*
IF2*
IF3*
II1*
II2*
II3*
II4*
II5*
II6*
II7*
II8*
IEN*
IDR*
IDRGD
ICRGD
ICR*
TI2
IF2F
IF1F
IF3F
II2F
II4F
II3F
II1F
II6F
II8F
II7F
II5F
IENF
(B • TI2)*
ICKA
RES+REND
(RES+REND)*
SYNCH
SYNCH*
ICKB
PLUS1
ICIND
DSR24*
DSR0
DSR1
DSR2
DSR3
DSR4
DSR5
DSR6
DSR7
DSR8
DSR9
DSR10
DSR11
DSR12
DSR13
DSR14
DSR15
DSR16
DSR17
DSR18
DSR19
DSR20
DSR21
DSR22
DSR23
SEE SHEET 1
LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT SHIFT REGISTER
CONTROL DATA
34015
D
74872527
01
34490-012-104
SHEET 3

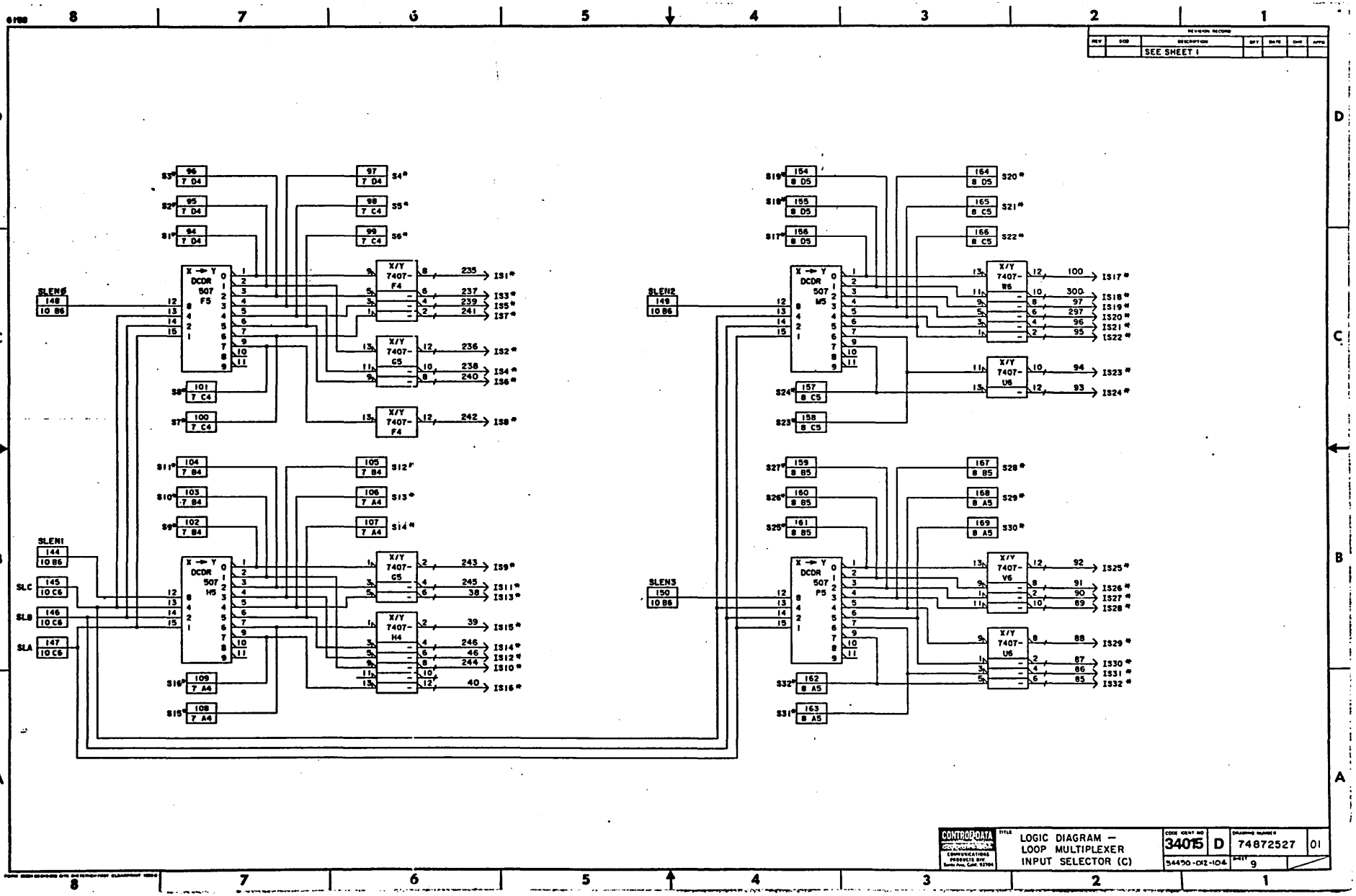

LOGIC DIAGRAM — LOOP MULTIPLEXER
CONTROL DATA
34015
D
74872527
01
SEE SHEET 1
INPUT OVERFLOW
RESET CONTROL
ICRCSEN*
ICRCS*
F1
SYNCH
RES+REND
DSR0
ICKA
PLUS1
(RES+REND)*
SEN*
DSR5
DSR5*
ICKA2*
A
T6*
T11
IF3F
INHIST
SYNCH*
BRST
ICKB
OCK
IM*
MI*
M3
M2
MCL*
IDT*
IDTGD
ICT*
ICTGD
EC*
OSEL
INAV
LE•EC•INAV
LE*
LE•EC
RLE•EC
RLE*
IST*
BCK
IOVFL
IENF
IFREN*
RRST*
ODI*
OD2*
ICKIND
OCKIND
RSTIN
RSTIN*
RSTOUT*
74S134
74S140
74S260
74S02
74S86
2433
193
X/Y 200-C7


6179
REVISION RECORD
REV
DESCRIPTION
SEE SHEET 1
CSEL*
176
12 D3
13 C5
+5V
R26
330
PLUS
204
10 B7
LE*EC
59
4 A3
LCLA*
72
8 B2
EC*
58
4 A1
T11
64
4 C5
6 B5
10 A8
A*
47
4 D5
T11
49
4 D5
6 B4
11 B4
ICKA
200
3 B4
4 D2
6 D1
RSTDN*
56
4 B7
11 C7
ICKA1*
65
11 C8
ICKA2*
46
4 D5
1405 D6
74S02 A4
74S260 A2
A
2433 A3
74S02 A4
B
2433 A2
8 74S02 A4
8 2135 B4
1 146S D3
3
3 B7
4 A3
6 D6
B
1 74S02 A4
8 1405 B3
1 1405 B3
T3*
68
6 B2
10 D8
IFREN*
63
4 A5
T12*
71
6 B1
7 A8
51
4 D6
6 D2
3 A4
SYNCH*
69
7 A8
LOAD*
70
11 A6
END*
64
4 D1
11 A8
3 A4
SYNCH
8 74S02 C3
8 74S02 D4
A'
2433 C4
B'
2433 C4
2433 C6
8 2135 B4
8 74S02 D4
8 1405 B3
PCKEN
73
10 D8
50
4 D6
INHIST
INHIST*
320
10 A8
151
6 B6
ICRCS OUT
44
4 D1
ICRCSEN*
CONTROL DATA
TITLE
LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT CONTROL
CODE IDENT NO
34015
D
DRAWING NUMBER
74872527
01
SHEET
5
34490-012-104


INPUT COUNTER
CRCS GENERATOR
ICKA
ICKB
SYNCH*
(RES+REND)*
RRST*
DSR12
T12*
T12
T1
T3*
T6*
T10
T11
T11*
ICRCS OUT
ICRCS*
R32 100K
R15 100K
C67 5 PF, 500VDC, ±5%
C3 20PF, 500VDC, ±5%
R16 330K
R29 1K
+5V
PLUS2
8 CNTR 537 K6
X/Y 200-K7
153.6 KHZ RF3
9.6 KHZ RF1
19.2 KHZ RF2
LOGIC DIAGRAM-
LOOP MULTIPLEXER-INPUT
COUNTER-OSCILLATOR
74872527
34015
54490-012-104


IAV REGISTER
SELECT PRIORITY
RGTR 74173
74279
XMAX→Y DCDR 532
LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT SELECTOR (A)
CONTROL DATA
34015
D
74872527
01
34490-012-104
SEE SHEET 1


IAV REGISTER
SELECT PRIORITY
SEE SHEET1
RGTR 74173 L7
RGTR 74173 L6
RGTR 74173 R6
RGTR 74173 R7
LTCH 74279 M7
LTCH 74279 M6
LTCH 74279 P6
LTCH 74279 P7
XMAX→Y DCDR 532 N7
XMAX→Y DCDR 532 N6
ENPD2*
ENPE3*
LCLA*
IAVCK
IAVLD
+5V
CONTROL DATA
LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT SELECTOR (B)
34015
D
74872527
01
SHEET 8
5-41

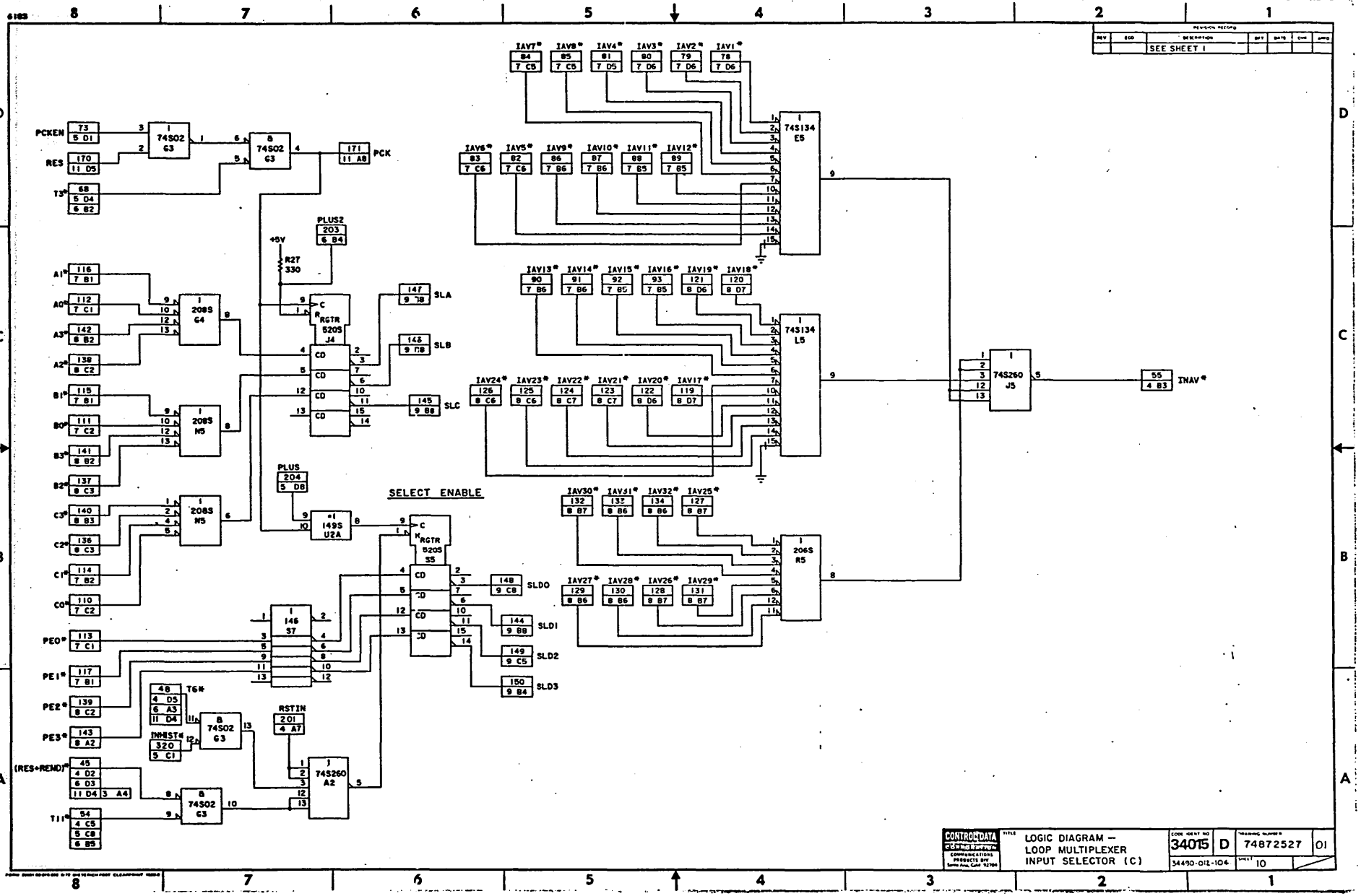


CONTROL DATA COMMUNICATIONS PRODUCTS DIV.

LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT SELECTOR (C)

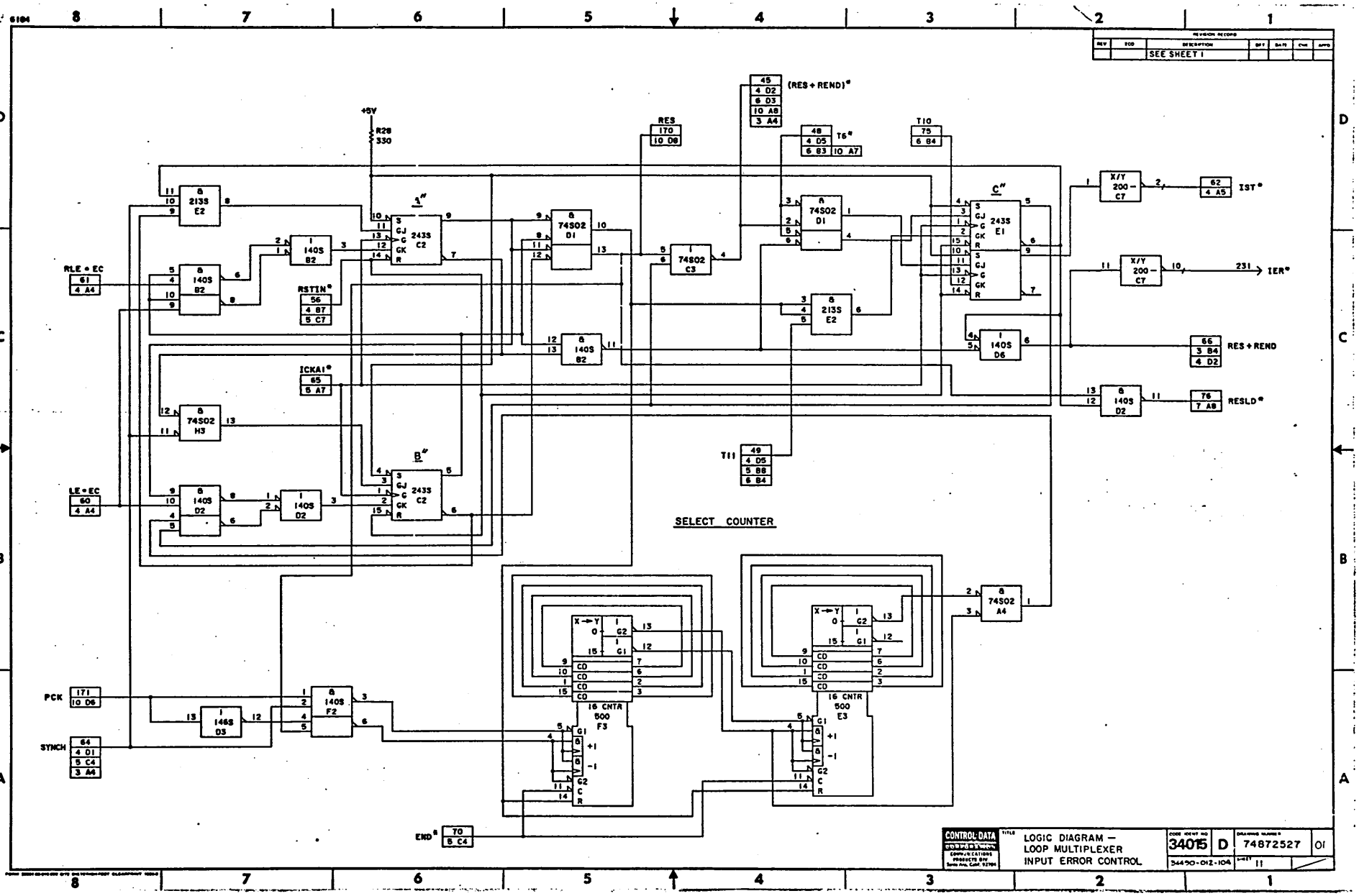
CODE IDENT NO		DRAWING NUMBER	
34015	D	74872527	01

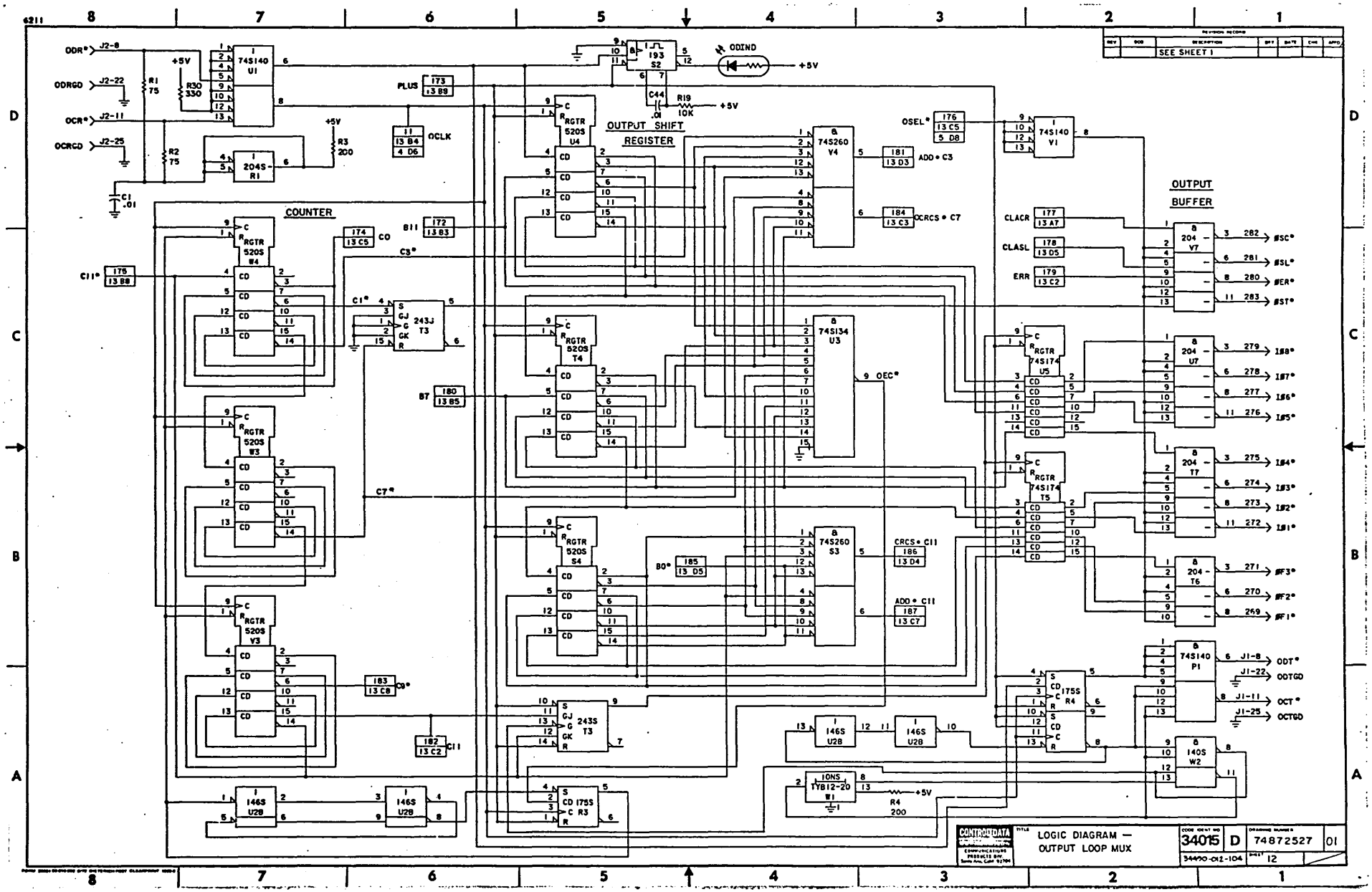
54450-012-104 SHEET 9

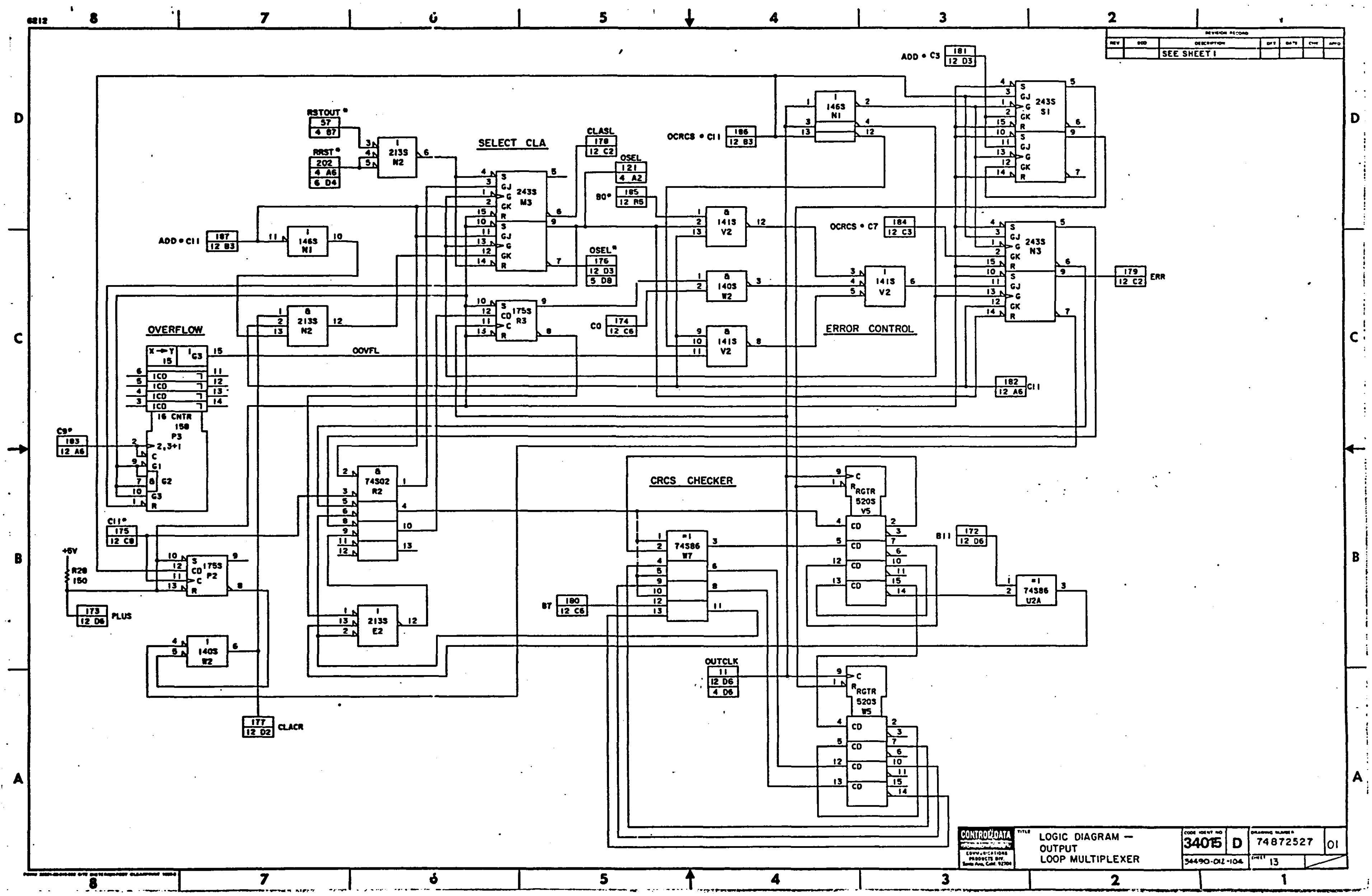


CONTROL DATA — LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT SELECTOR (C)

CODE IDENT NO		TRAINING NUMBER	
34015	D	74872527	01
34490-012-104		SHEET 10	


SEE SHEET 1
+5V
R28
330
RES
170
10 D8
(RES+REND)*
T6*
T10
RLE+EC
LE+EC
RSTIN*
ICKAI*
T11
SELECT COUNTER
PCK
SYNCH
END*
IST*
IER*
RES+REND
RESLD*
16 CNTR
500
F3
E3
CONTROL DATA
LOGIC DIAGRAM — LOOP MULTIPLEXER INPUT ERROR CONTROL
34015
D
74872527
01
34450-012-104


OUTPUT SHIFT REGISTER
COUNTER
OUTPUT BUFFER
SEE SHEET 1
LOGIC DIAGRAM — OUTPUT LOOP MUX
CONTROL DATA
34015
D
74872527
01
34490-012-104
SHEET 12


SEE SHEET 1
SELECT CLA
OVERFLOW
ERROR CONTROL
CRCS CHECKER
RSTOUT*
RRST*
ADD • C11
ADD • C3
OCRCS • C11
OCRCS • C7
CLASL
OSEL
OSEL*
B0*
C0
OOVFL
16 CNTR
C9*
C11*
+5V
R28
150
PLUS
CLACR
ERR
C11
B11
B7
OUTCLK
RGTR
CONTROL DATA
LOGIC DIAGRAM —
OUTPUT
LOOP MULTIPLEXER
34015
D
74872527
01
34490-012-104
13

MAINTENANCE 6

Maintenance procedures include preventive maintenance, troubleshooting and corrective action.

SPECIAL TOOLS

None required

PREVENTIVE MAINTENANCE

Preventive maintenance is limited to inspection of cables and connectors and periodic replacement of air blower filters.

TROUBLESHOOTING

INITIAL SYMPTOMS

Initial indications of a hardware failure or malfunction may appear as one of the following:

1. System Halt — Occurs if the system detects an unrecoverable problem, such as memory parity error, bad coupler status or others. When the system halts, a "halt code" is given in the host which gives the reason for the halt.

2. "On-line diagnostic response messages" which can be used when isolating a line problem to a vendor level, such as CLA, modem, or phone lines.

ON-LINE DIAGNOSTIC TROUBLESHOOTING (18-30 ONLY)

1. If all lines handled by the COMMUX are experiencing trouble, the most likely cause is the MLIA or loop MUX.

2. If only groups of lines are experiencing problems, the failure is probably within the loop MUX.

3. If only one line is out of service, problem could be in the ACLA, local modem, telephone service, remote modem or terminal. In this instance, on-line diagnostics, coupled with procedures described here, can be used to isolate the problem to the vendor level.

PROCEDURE FOR ISOLATING AND CORRECTING LINE PROBLEMS

1. Run on-line internal loopback test on failed line (refer to CCP1.0 on-line diagnostic handbook or User Bulletin, CCP1.0 operating instructions, used with CCP1.0 cassette tape (P/N 12323184 32K). If the test fails, replace the affected ACLA.

2. If test passes, connect external loopback connector. For ACLA type 2561-1 use connector 74715600.

3. Run external loopback diagnostic. If test fails, replace ACLA. If test passes, reconnect the local modem and proceed with the next step.

4. If available, utilize the digital test facilities of the modem to loop data from the ACLA through the modem and back to the ACLA. Run the external loopback test. If the test fails, the problem is either in the modem or ACLA-to-modem cable. If the test passes, proceed with the next step.

5. Release the digital test switch on the local modem. Request that the telephone company loop the line back at the local central office. Run the external loopback test. If the test fails, the problem could be the local modem or telephone company equipment. If the test passes, proceed to the next step.

6. Request that the local central office loopback be removed. Request that the analog loopback feature, if available, on the remote modem be engaged. Run the external loopback diagnostic. If the test fails, the problem could be in the line between the local and remote telephone offices, in the remote office, the line to the remote modem, or the remote modem itself. Request that the telephone company check out the associated lines and central office equipment. If the test passes, the problem is either the remote modem, modem-to-terminal cable, or the terminal itself. Notify the remote station and request that they have the equipment checked.

OFF-LINE TROUBLESHOOTING (18-25/30)

When the timeshare system detects an unrecoverable error, a system halt will result. This halt will be accompanied by a halt code. Off-line diagnostics must be used to isolate the problem.

OFF-LINE DIAGNOSTICS

1. Off-line diagnostics are to be performed utilizing the special UTOPIA formatted MSMP 17 cassette (P/N 12323182) or flexible disk (P/N 96820416) and the DDLTs contained in the Communication Multiplexer Subsystem Hardware Maintenance Manual, (P/N 60475080).

COMMENT SHEET

MANUAL TITLE CDC® CYBER 18-25/30 Timeshare Communications Multiplexer Hardware Reference/Maintenance Manual

PUBLICATION NO. 96768610 REVISION 03

FROM NAME: _____

BUSINESS ADDRESS: _____

COMMENTS: This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number.

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