

CONTROL DATA

1700

1500 SERIES
EQUIPMENT CODES
FOR PROGRAMMERS

CONTROL DATA
CORPORATION



CONTROL DATA® 1500 SERIES
EQUIPMENT CODES
FOR PROGRAMMERS

Publication NO. X0010418

CONTROL DATA CORPORATION
ANALOG-DIGITAL SYSTEMS DIVISION
La Jolla, California

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DATE 7/18/66
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REV. E

CONTROL SYSTEMS DIVISION

1700 A/D SYSTEMS RECOMMENDED EQUIPMENT
CODES, STATION AND CHANNEL ADDRESSES,
AND INTERRUPT LINE ASSIGNMENTS

M

| | | | | | |
|-------------------------|---------|---------|--|--|--|
| ORIGINATOR M. P. ... | AD. ... | 7/18/66 | | | |
|-------------------------|---------|---------|--|--|--|



CONTROL DATA CORPORATION

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LA JOLLA, CALIFORNIA

ENGINEERING

SPECIFICATION

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REV.

39005300

6

DATE 7/18/66

REVISION RECORD

| REV. | PAGE | PARAGRAPH | DATA | E.C.O. | APP. | DATE |
|------|------|-----------|---|--------|-----------|---------|
| A | | | Released | | | 8/8/66 |
| B | 5 | 3.7 | Delete sentence "A suggested...b". | 11882 | <i>Am</i> | 3/10/67 |
| B | 5 | 3.8 | Delete | | | 3/10/67 |
| B | 8 | | Table changed | | | 3/10/67 |
| B | 16 | | Table changed | | | 3/10/67 |
| B | 17 | All | Delete | | | 3/10/67 |
| B | 18 | All | Delete | | | 3/10/67 |
| B | 19 | All | Delete | | | 3/10/67 |
| C | 9 | 08 | DELETE 1577 STALL ALARM } 1 DEVICE | 12127 | <i>Am</i> | 7-12-67 |
| C | 9 | 09 | ADD STATUS FUNCTION | | | |
| D | 8 | Item 6.7 | CHG. CONTR. #1 TO 2 + #2 TO 1 PER | 12364 | | 12-28-7 |
| D | 14 | — | RETYPE PG. TO ACCOMODATE CHG PER ECO 12364 | 12364 | <i>Am</i> | 12-28-7 |
| D | 16 | Item 11 | ADD "1742 LINE PRINTER" | 12429 | | 12-28-7 |
| E | B.16 | — | RETYPE PGS TO ALLOW FOR ADD'S AND DELETIONS. - SEE ECO | 12467 | <i>Am</i> | 1-12-68 |
| | | | | | | |



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ENGINEERING SPECIFICATION

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1.0 SCOPE

1.1 This specification presents a system of standard equipment, codes, station and channel addresses, and interrupt line assignments recommended for use in 1700 A/D systems.

2.0 APPLICABLE DOCUMENTS

E. S. 25190900 - 1750 Decoded Data Channel

3.0 GENERAL REQUIREMENTS

3.1 Definitions

3.1.1 **Equipment** - An equipment is defined as any device which occupies a position on the 1705 data channel from the 1700. A maximum of eight equipments may be attached. A maximum of 16 addresses (0 through F) are available.

3.1.2 **Station** - A station is contained within an equipment. Up to 128 station addresses are possible within an equipment.

3.1.3 **Channel** - A channel is contained within an equipment. See Figure 2 for addressing mode.

3.2 Connect Command

Execution of the connect command (configuration shown in Fig. 1) allows addressing of a specific equipment and a station within that equipment.

3.3 Continue Command

Execution of continue commands (configuration shown in Fig. 2) allows channel read and write instructions to be issued to channels within a specific equipment.

3.4 Standard Equipment Addresses

Figure 3 shows the recommended equipment codes.

3.5 Standard Station and Channel Addresses

3.5.1 The standard addresses listed in Fig. 4 allow for a system equal to or less than the following tabulations. Hardware restrictions may prevent these maximums from being realized. For systems exceeding the maximum in one or more areas, it is recommended that the additional devices be assigned in the "unassigned" areas, even though addresses for a particular class of equipment may not be contiguous.



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| <u>Quantity</u> | <u>Type of Equipment</u> |
|-----------------|---|
| 4096 | Digital Inputs |
| 6144 | Latching Contact Closure Outputs or 384 Latching DAC Outputs, or combination. |
| 2048 | External Register Relay Outputs or 128 DAC Outputs, less two words/Digital Display, or combination. |
| 128 | Event Counters |
| 128 | External Interrupts |
| 12 | I/O Typewriters |
| 2048 | Analog Input Relay Multiplexer Channels |
| 1024 | 1538 High-Speed, High-Level Analog Input Channels |
| 1024 | 1561 High-Speed DAC Outputs |
| 1 | Stall Alarm |
| 1 | 1573 Limit Comparison Option |
| 1 | 1572 Sample Rate Option |
| 1 | 1797 Cyclic Buffer |
| 2 | 160A I/O Channels |
| 10 | Unassigned Station Addresses |
| 382 | Unassigned Channel Addresses |

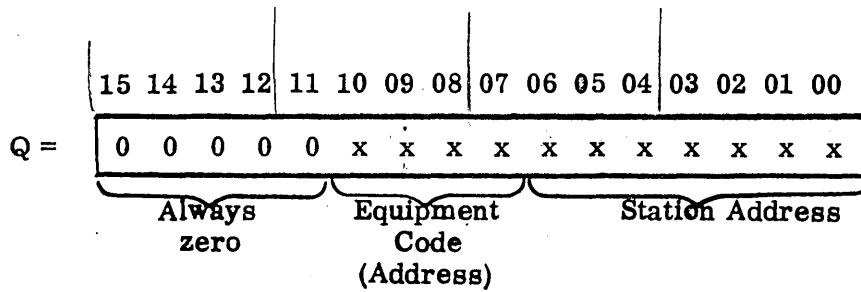
3.5.2 All devices operating on the DCB will be delivered from production with the the first address assigned to that class of equipment plugged up. Incrementing of the address for subsequent devices of the same type shall be done by engineering during checkout.

3.6 Standard Interrupt Line Assignments

Figure 5 shows the recommended interrupt line assignments.

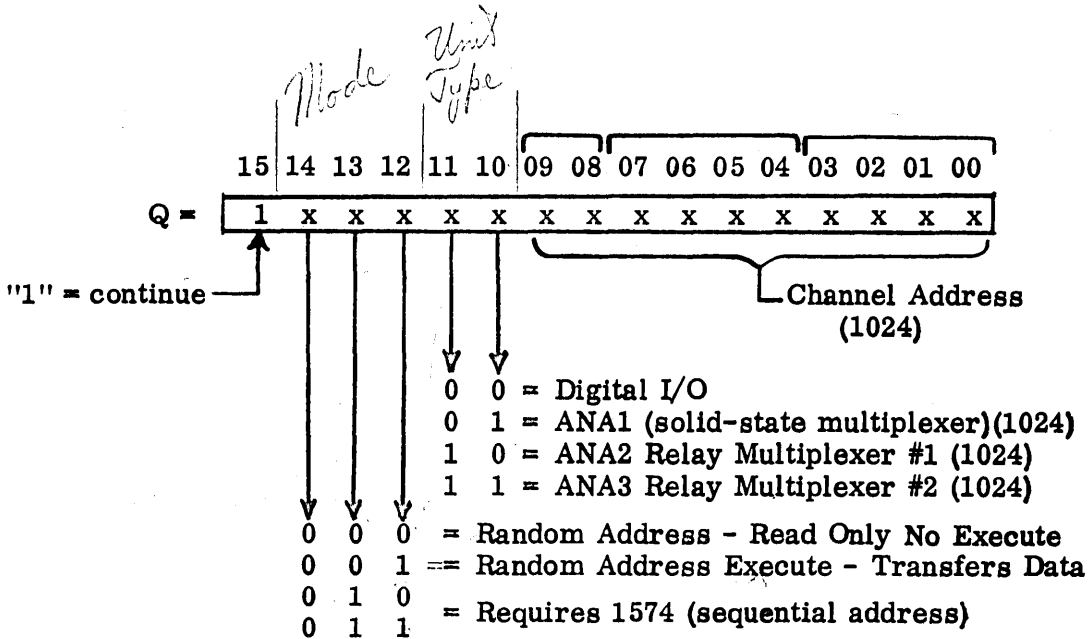
3.7 Documentation

The final installed system addresses shall be documented in the system documentation.



CONNECT COMMAND

Fig. 1



CONTINUE COMMAND

Fig. 2



ENGINEERING SPECIFICATION

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Equipment Codes
{Hexadecimal}

Description

| | |
|---|---|
| 0 | Unassigned |
| 1 | Low-Speed I/O {1711, 1713, 1721, 1729, etc. |
| 2 | 1751 Drum Controller |
| 3 | 1738 Disk Controller |
| 4 | 1742 Line Printer |
| 5 | 1749 Communications Terminal |
| 6 | Remote I/O Controller #2 |
| 7 | 1731 Mag Tape Controller {601's} |
| 8 | DCT #1 |
| 9 | DCT #2 |
| A | Remote I/O Controller #1 |
| B | |
| C | |
| D | |
| E | |
| F | |

EQUIPMENT CODE ASSIGNMENTS

Fig. 3

LA JOLLA STANDARD ASSIGNMENTS

EQUIPMENT NUMBER (E FIELD)

- 1 - Low-Speed I/O
- 2 - 1751 Drum Interface
- 3 - 1738 Disk Pack Controller
- 4 - 1742 Line Printer (300 LPM)
- 5 - 1749 Communications Terminal Controller
- 6 - Remote I/O Controller NO. 2
- 7 - 1731 Magnetic Tape Controller
- 8 - 1750 NO. 1 - DCT
- 9 - 1750 NO. 2 - DCT
- A - Remote I/O Controller NO. 1 (Remote DCT)

INTERRUPT LINES

- 0 - Internal
- 1 - Low-Speed I/O + 1750
- 2 - 1573 Line Sync Timing
- 3 - 1728 Card Read-Punch Controller
- 4 - 1738 Disk Pack Controller
- 5 - 1751 Drum Interface
- 6 - 1500 I/O Typewriter - 1581/1583
- 7 - 1545 Digital Input Sync Input
- 8 - 1530/1534 Analog Input Interface
- 9 - 1558 Latching Relay Output
- 10 - 1547 Event Counter Interface
- 11 - 1549 Communications Terminal Controller
- 12 - 1742 Line Printer (300 LPM)
- 13 - 1749 Communications Terminal Controller
- 14 - 1731/8000 Tape

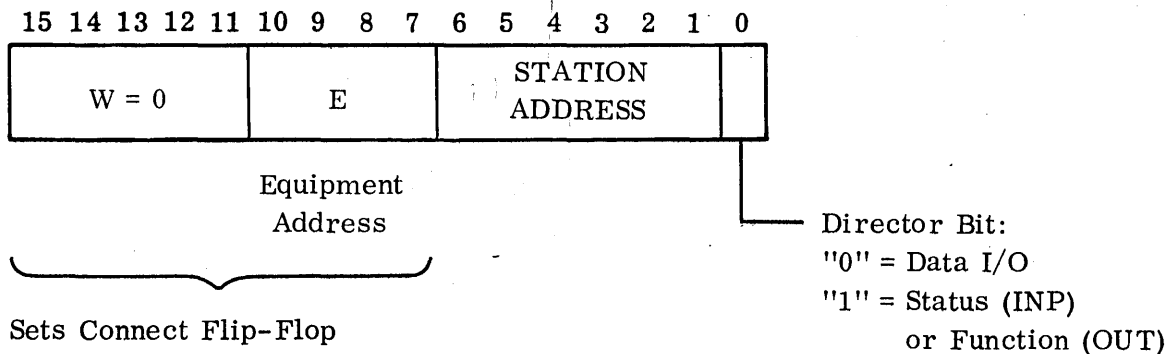


1750 DATA AND CONTROL TERMINAL (DCT)

The 1750 Data and Control Terminal (DCT) is the heart of the CONTROL DATA[®] 1700 Computer A/D System. All CDC[®] 1500 Series equipment is connected to the Data and Control Bus (DCB). To activate any of the various 1500 Series units, the 1750 has to be first connected to the 1700 A/Q line. This relationship between the 1700 (A/Q, DSA), the 1750 (DCB, BDCB), and the 1500 units is shown on page 2-2.

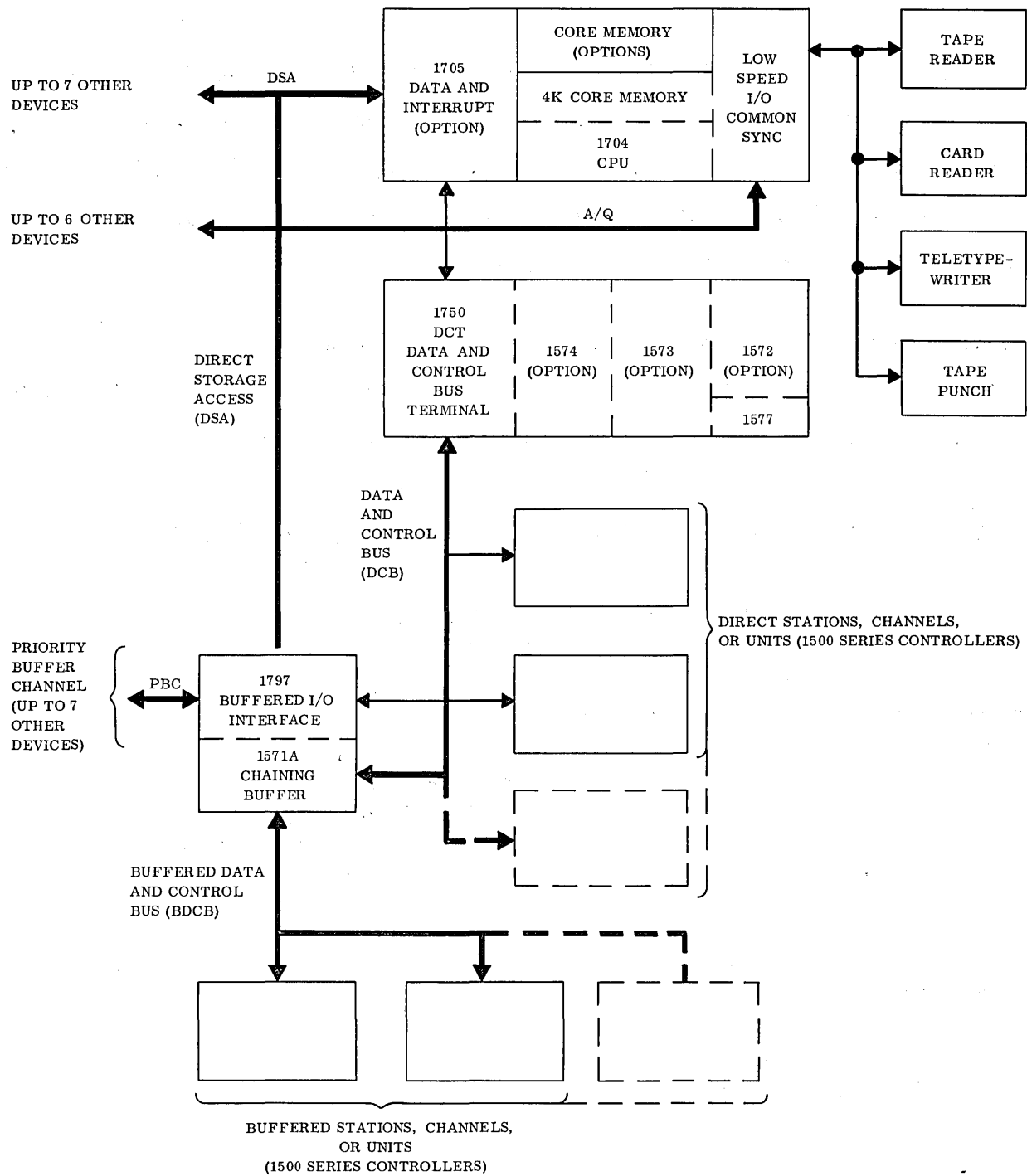
After the 1750 is connected (DCB activated), a Continue command may be executed to the 1500 units that respond only to channel addresses. A discussion of the 1750 Connect command is shown below and the 1750 Continue command is shown on page 2-3.

CONNECT COMMAND CONFIGURATION ON READ (INP) OR WRITE (OUT)



Q15 = "0," Address in Station

Q00-Q06 = 7X, NAD (no address
command) 1574
Sequential Addressing
Unit Supplies Channel
Address (refer to
page 13-3)



P-0137

1700 A/D AND 1500 I/O SYSTEM

1750 DATA AND CONTROL TERMINAL (DCT) (Continued)

CONTINUE OR DATA TRANSFER COMMAND CONFIGURATION IN Q-REGISTER WITH CONNECT F/F SET AND Q15 = "1"

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|----|------|----|----|--|----|--|---|---|---|---|---|---|---|---|---|---|
| 1 | MODE | | | CHANNEL (UNIT) ADDRESS | | | | | | | | | | | | |
| | | | | Unit Type | | 1024 Addresses | | | | | | | | | | |
| | | | | 0 | 0 | Digital or Contact Closure I/O (discrete or D/A) | | | | | | | | | | |
| | | | | 0 | 1 | High-Speed Analog, Solid-State MUX | | | | | | | | | | |
| | | | | 1 | 0 | Low-Speed Analog, Relay MUX | | | | | | | | | | |
| | | | | 1 | 1 | Low-Speed Analog, Relay MUX | | | | | | | | | | |
| | | | | 0 | 0 | 0 | Random Address, Read Data Only - No Execute | | | | | | | | | |
| | | | | 0 | 0 | 1 | Random Address and Execute, Data Transfer | | | | | | | | | |
| | | | | 0 | 1 | 0 | Random Address and Lock-Up (1574 next address = Q-Register) | | | | | | | | | |
| | | | | 0 | 1 | 1 | Random Address and Increment (1574 next address = Q-Register + "1") | | | | | | | | | |
| | | | | 1 | 0 | 0 | Sequential Address Option (1574) Setup and Status | | | | | | | | | |
| | | | | Write = Setup Q00-Q11, First Channel Address to First and Next Address Registers | | | | | | | | | | | | |
| | | | | A00-A11 to Last Address Register | | | | | | | | | | | | |
| | | | | Read = Status Next Address Register Input to A-Register | | | | | | | | | | | | |
| | | | | 1 | 0 | 1 | SAM 1 | | | | | | | | | } 1571 Chaining Buffered Data Channel(s) Setup (Write) and Status (Read) |
| | | | | 1 | 1 | 0 | SAM 2 | | | | | | | | | |
| | | | | 1 | 1 | 1 | SAM 3 | | | | | | | | | |

1750 DATA AND CONTROL TERMINAL (DCT) (Continued)

1500 SERIES UNITS ADDRESSED BY STATIONS

- 160A I/O Interface
- 1530 Low-Speed A/D Input Interface
- 1534 Low-Speed A/D Input Interface
- 1538 High-Speed, High-Level A/D Input Interface
- 1547 Event Counter Interface
- 1549 External Interrupt Interface
- 1558 Latching Relay Output Interface
- 1561 High-Speed D/A Output Interface
- 1572 Sample Rate Generator
- 1573 Line Sync Timing Generator
- 1574 Sequential Addressing Unit
- 1577 Stall Alarm
- 1581 Logging Typewriter Interface (Flexowriter)
- 1583 Logging Typewriter Interface (Selectric)
- 1750 Data and Control Terminal (DCT) (DCB Terminator)
- 1797 Buffered I/O Interface (PBC 0-7)

1500 SERIES UNITS ADDRESS BY CHANNELS

- 160A I/O Channels
- 1531 Multiplexer
- 1532 Multiplexer
- 1533 Multiplexer
- 1535 Multiplexer
- 1539 Multiplexer
- 1544 Digital Input Interface
- 1547 Event Counters
- 1553 External Register Output Interface
- 1558 Latching Relay Output Interface
- 1562 High-Speed DAC Output
- 1567 Simultaneous Sample-and-Hold Unit

1750 DATA AND CONTROL TERMINAL (DCT) (Continued)

1750 STATION ADDRESS ASSIGNMENTS

| STATION ADDRESS | EQUIPMENT ASSIGNED | INPUT COMMAND | OUTPUT COMMAND |
|-----------------|---|----------------------------|---------------------|
| 00* | 1750 DCB | 1750 Status | 1750 Function |
| 01* | 1750 DCB | System Status | Ack. Int. from 1573 |
| 02* | 1572 Sample Rate Generator } 1 device | | |
| 03* | | 1572 Sample Rate Generator | |
| 04 | | | |
| 05 | | | |
| 06 | | | |
| 07 | | | |
| 08 | | | |
| 09 | 1577 Stall Alarm | Status | Function |
| 0A | 1575 Limit Comparison Option } 1 device | | |
| 0B | | ↕ | |
| 0C | | ↕ | |
| 0D | | ↕ | |
| 0E | 1575 Limit Comparison Option | | |
| 0F | | | |
| 10 | 1549 External Interrupts #1 (00-15) | Status | Ack. Int. |
| 11 | #2 | ↕ | ↕ |
| 12 | #3 | ↕ | ↕ |
| 13 | #4 | Status | Ack. Int. Set Mask |
| 14 | #1 | | ↕ |
| 15 | #2 | | ↕ |
| 16 | #3 | | ↕ |
| 17 | #4 | | Set Mask |
| 18 | #5 | Status | Ack. Int. |
| 19 | #6 | ↕ | ↕ |
| 1A | #7 | ↕ | ↕ |
| 1B | #8 | Status | Ack. Int. Set Mask |
| 1C | #5 | | ↕ |
| 1D | #6 | | ↕ |
| 1E | #7 | | ↕ |
| 1F | 1549 External Interrupts #8 (00-15) | | Set Mask |
| 20 | 1547 Event Counters #1 (0-F) | Status | Ack. Int. |
| 21 | #1 | ↕ | ↕ |
| 22 | #2 | Status | Ack. Int. |
| 23 | #2 | | Set Mask |
| 24 | #3 | Status | Ack. Int. |
| 25 | #3 | | Set Mask |
| 26 | #4 | Status | Ack. Int. |
| 27 | #4 | | Set Mask |
| 28 | #5 | Status | Ack. Int. |
| 29 | #5 | | Set Mask |
| 2A | #6 | Status | Ack. Int. |
| 2B | #6 | | Set Mask |
| 2C | #7 | Status | Ack. Int. |
| 2D | #7 | | Set Mask |
| 2E | #8 | Status | Ack. Int. |
| 2F | 1547 Event Counters #8 (0-F) | | Set Mask |

*Fixed Address

1750 DATA AND CONTROL TERMINAL (DCT) (Continued)

1750 STATION ADDRESS ASSIGNMENTS (Continued)

| <u>STATION ADDRESS</u> | <u>EQUIPMENT ASSIGNED</u> | <u>INPUT COMMAND</u> | <u>OUTPUT COMMAND</u> |
|------------------------|--|----------------------|-----------------------|
| 30 | 1581-1583 Typewriter #1 | data | data |
| 31 | ↑ #1 | status | function |
| 32 | ↑ #2 | data | data |
| 33 | ↑ #2 | status | function |
| 34 | ↑ #3 | data | data |
| 35 | ↑ #3 | status | function |
| 36 | ↑ #4 | data | data |
| 37 | ↑ #4 | status | function |
| 38 | ↑ #5 | data | data |
| 39 | ↑ #5 | status | function |
| 3A | ↑ #6 | data | data |
| 3B | ↑ #6 | status | function |
| 3C | ↑ #7 | data | data |
| 3D | ↑ #7 | status | function |
| 3E | ↑ #8 | data | data |
| 3F | ↑ #8 | status | function |
| 40 | ↑ #9 | data | data |
| 41 | ↑ #9 | status | function |
| 42 | ↑ #10 | data | data |
| 43 | ↑ #10 | status | function |
| 44 | ↑ #11 | data | data |
| 45 | ↑ #11 | status | function |
| 46 | ↑ #12 | data | data |
| 47 | 1581-1583 Typewriter #12 | status | function |
| 48 | 1558 Latching Relay Outputs #1 | status | function |
| 49 | ↑ #2 | ↑ | ↑ |
| 4A | ↑ #3 | ↑ | ↑ |
| 4B | ↑ #4 | ↑ | ↑ |
| 4C | ↑ #5 | ↑ | ↑ |
| 4D | 1558 Latching Relay Outputs #6 | status | function |
| 4E | 1538 High-Speed, High-Level A/D Input #1 | ↑ | ↑ |
| 4F | ↑ #2 | ↑ | ↑ |
| 50 | ↑ #3 | ↑ | ↑ |
| 51 | 1538 High-Speed, High-Level A/D Input #4 | ↑ | ↑ |
| 52 | 1561 High-Speed D/A Output #1 | ↑ | ↑ |
| 53 | ↑ #2 | ↑ | ↑ |
| 54 | ↑ #3 | ↑ | ↑ |
| 55 | 1561 High-Speed D/A Output #4 | ↑ | ↑ |
| 56 | 1530 or 1534 Low-Speed A/D Input #1 | ↑ | ↑ |
| 57 | ↑ #2 | ↑ | ↑ |
| 58 | ↑ #3 | ↑ | ↑ |
| 59 | 1530 or 1534 Low-Speed A/D Input #4 | status | function |
| 5A | 160A I/O #1 | ↑ | ↑ |
| 5B | 160A I/O #2 | ↑ | ↑ |
| 5C | ↑ | ↑ | ↑ |
| thru | Unassigned | | |
| 5F | | | |
| 60 | | | |
| thru | 1797 PBC Channels 0-7 | status | start |
| 67 | | | |
| 68-6F | 1797 PBC Channels 0-7 | next address | function |
| 70-7F | 1574 Sequential Addressing Unit | | |

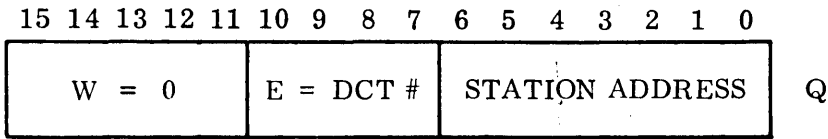
00-03
 04-07
 08-08
 0C-0F

1750 DATA AND CONTROL TERMINAL (DCT) (Continued)

CHANNEL ASSIGNMENTS

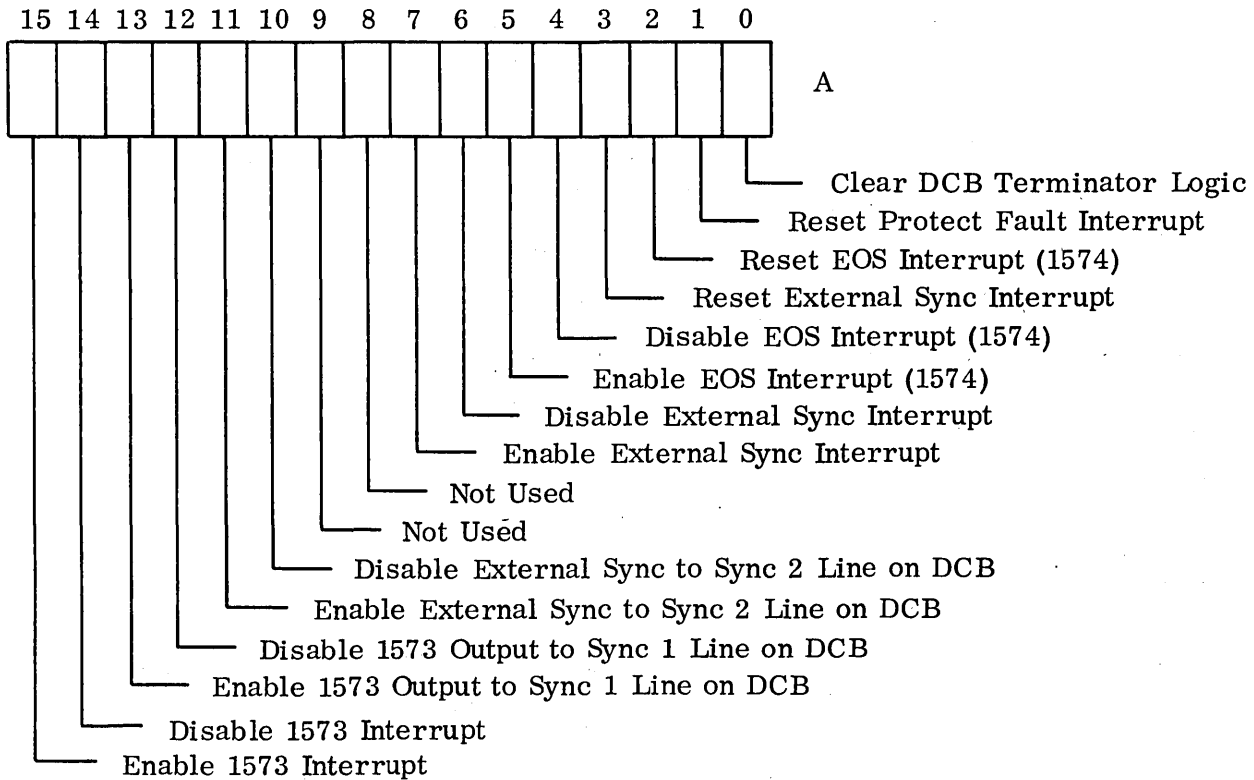
| <u>DIGITAL CHANNEL ADDRESSES</u> | <u>I/O COMMAND</u> | <u>EQUIPMENT ASSIGNED</u> |
|--|--------------------|--|
| 000-0FF | Read | 1544 Digital Inputs (256 words, 4096) |
| 080-1FF | Write | 1558 Latching Relay Output (384 equals 6144 contact closures or 384 DAC's), assign least significant addresses to DAC's if mixed |
| 000-07F | Write | 1553 Digital Outputs (128 words equals 2048 contact closures or 128 DAC's) less 2 words for each digital display |
| 200-27F | Read/Write | 1547 Event Counters (128) |
| 3FE-3FF | Read/Write | 160A I/O Channel (2) |
| 100-1FF | Read | Not Assigned |
| 280-3FD | Read/Write | Not Assigned |
| | | |
| <u>HIGH-SPEED ANALOG CHANNEL ADDRESSES</u> | | |
| 400-7FF | Read | 1538 High-Speed, High-Level A/D Inputs |
| 400-7FF | Write | 1561 High-Speed D/A Outputs |
| | | |
| <u>LOW-SPEED ANALOG CHANNEL ADDRESSES</u> | | |
| 800-BFF | Read | 1530 or 1534 A/D Relay Multiplexer NO. 1 ✓ |
| C00-FFF | Read | 1530 or 1534 A/D Relay Multiplexer NO. 2 |

1750 DATA AND CONTROL TERMINAL (DCT) (Continued)



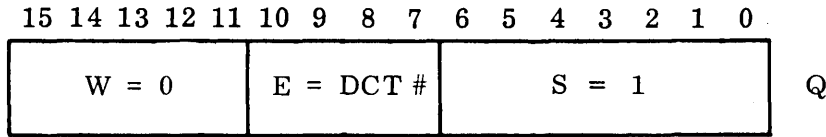
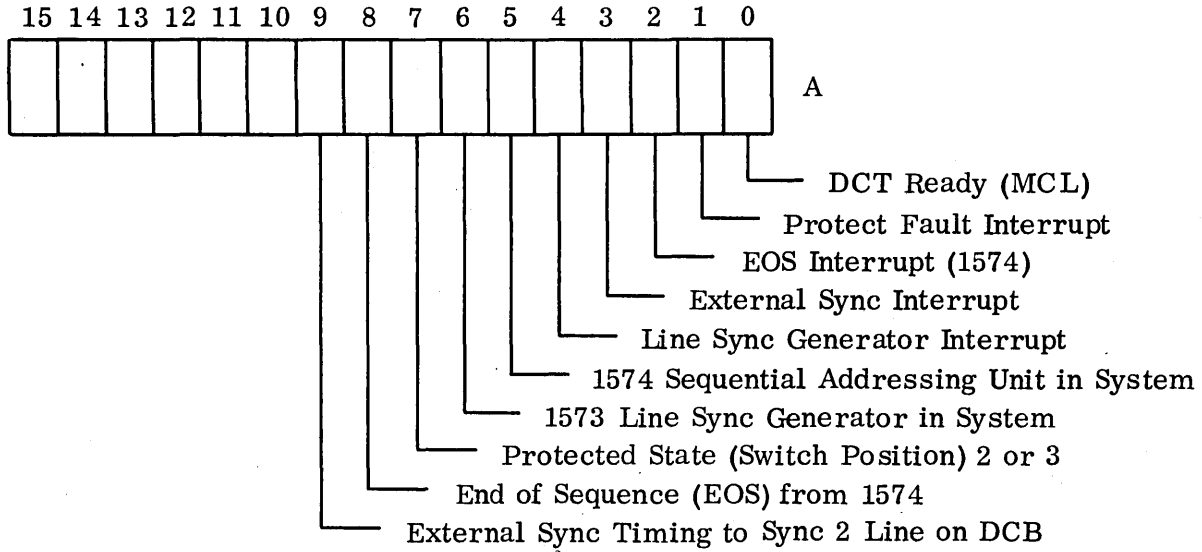
S = 0

FUNCTION (OUT)

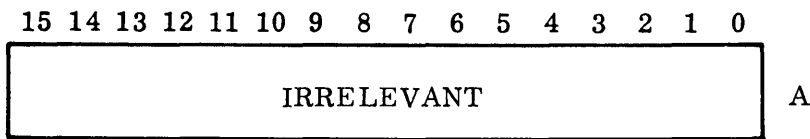


1750 DATA AND CONTROL TERMINAL (DCT) (Continued)

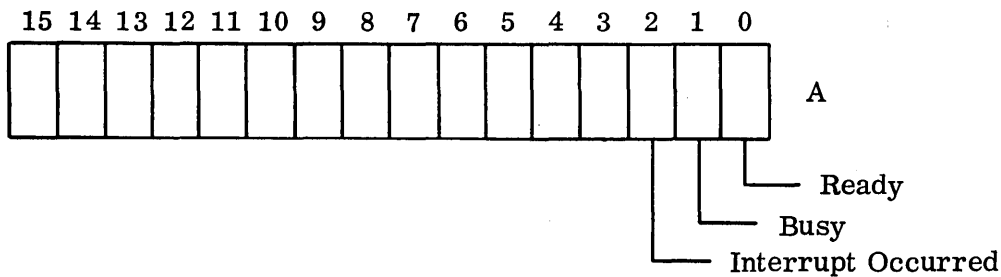
STATUS (INP)



FUNCTION (OUT)

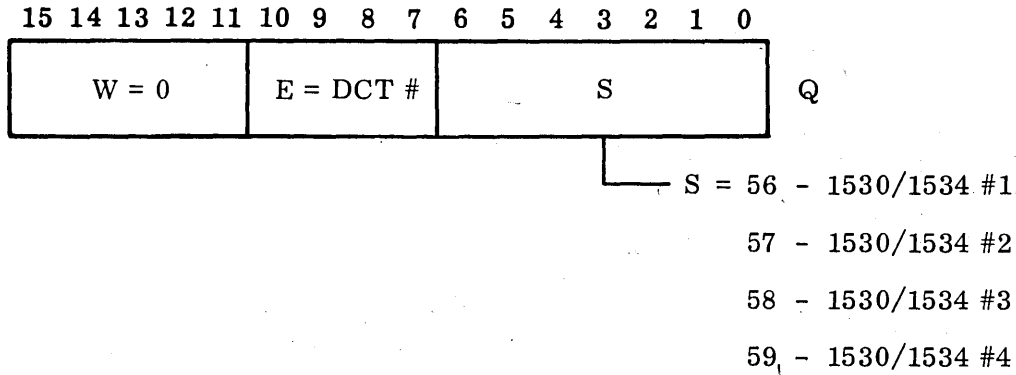


SYSTEM STATUS FROM DCB LINES (INP)

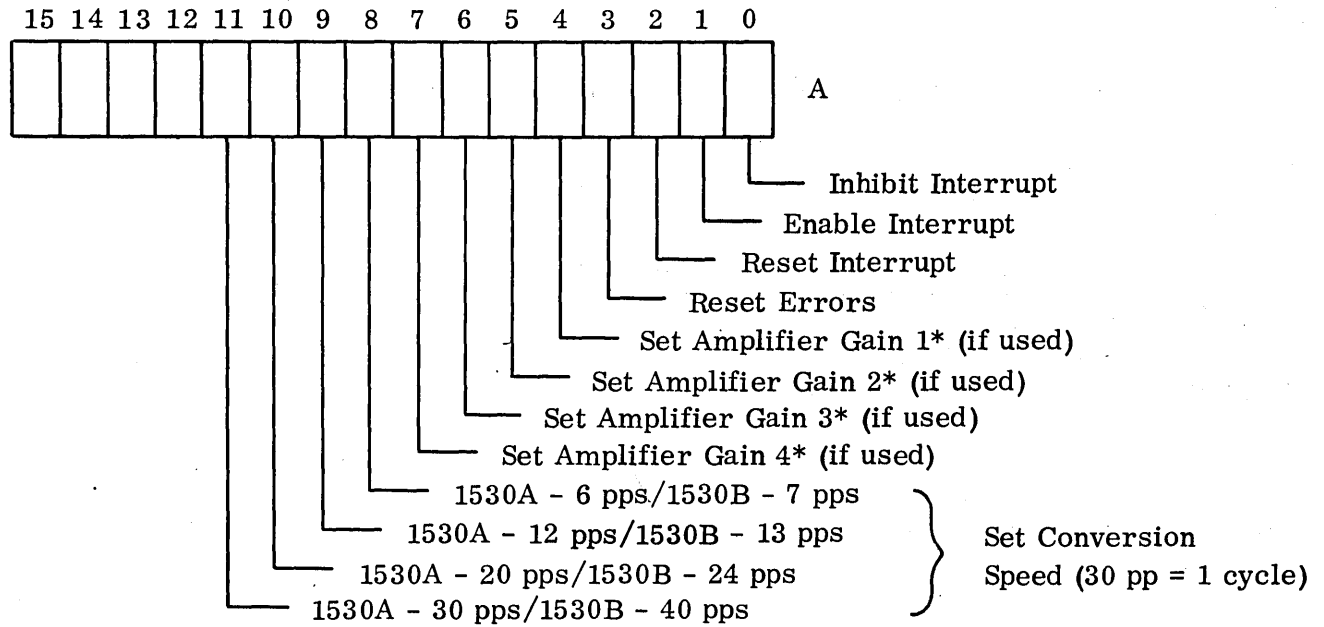




1530/1534 ANALOG INPUT CONTROLLER



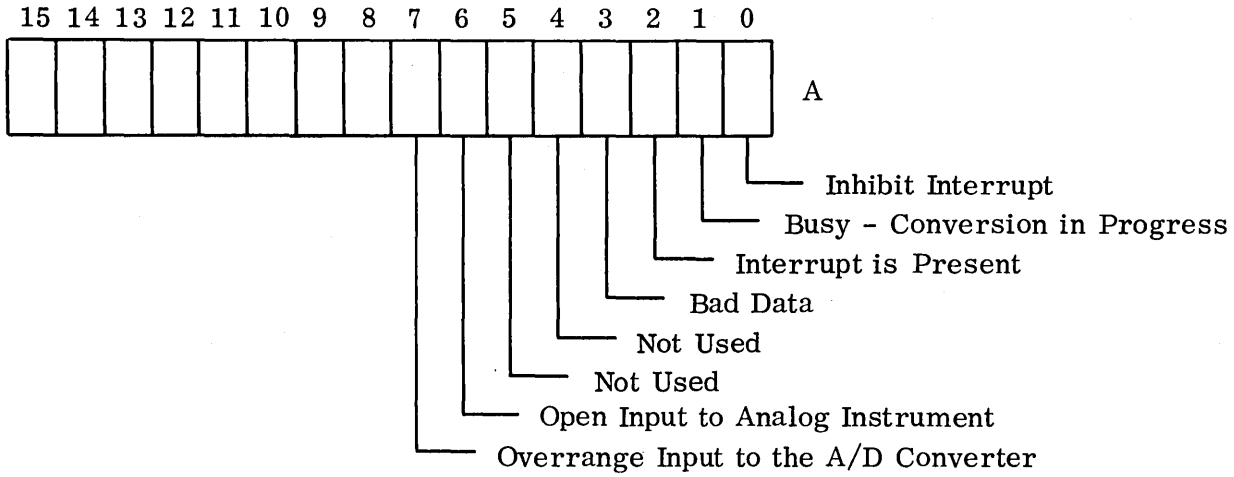
FUNCTION (OUT)



*If computer control option is chosen: Gains 1, 2, 3, 4 are system variable.
 Gain = 1 is lowest; Gain = 4 is highest.

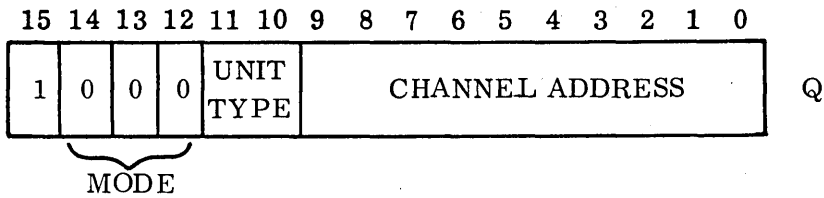
1530/1534 ANALOG INPUT CONTROLLER (Continued)

STATUS (INP)



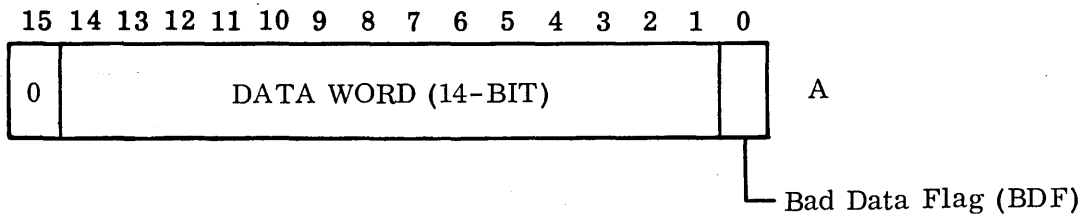
After 1530 or 1534 has been connected to DCB or BDCB:

DATA TRANSFER (INP)



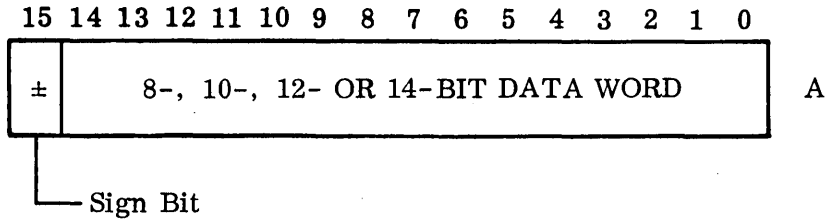
A-Register will contain:

1530 A/B

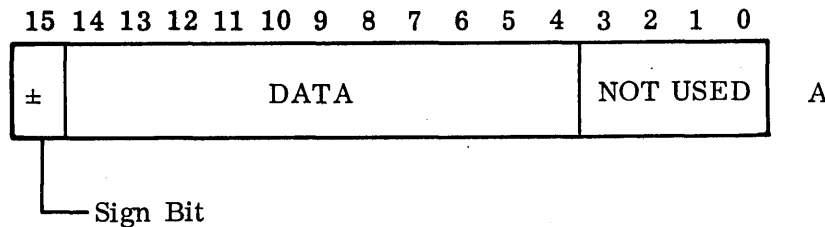


1530/1534 ANALOG INPUT CONTROLLER (Continued)

1534



The data word received in the A-register may be an 8-, 10-, 12- or 14-bit word. The most significant bit of the input word is the sign bit. The input is left justified with the sign bit in bit 15*. See example below for a 12-bit word input.



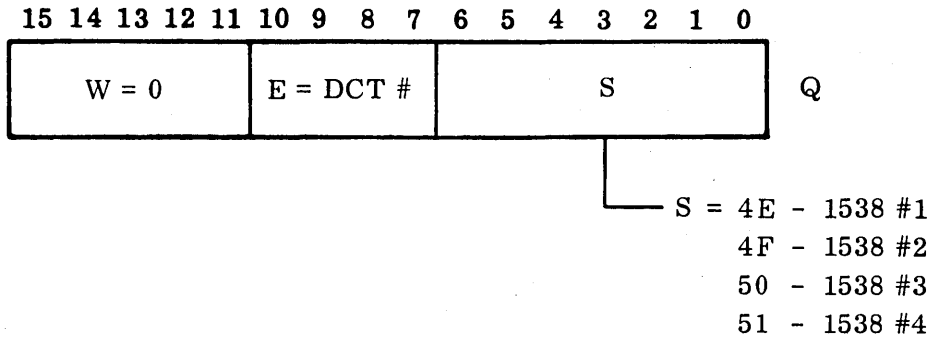
NOTE

1. The data read in is the data converted from the previous channel address. The data from the present channel address will be read on the next input instruction.
2. The channel addressed will not be connected and converted unless a "Read Execute" is used (see page 2-3).

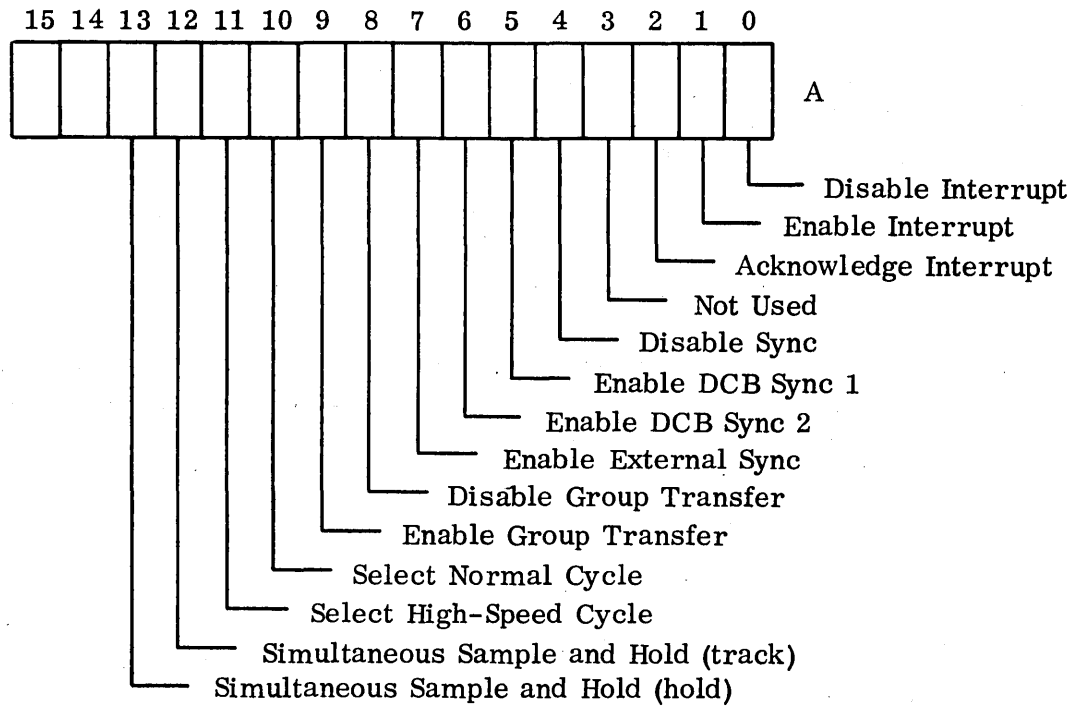
*Program option may specify right justification. In this case, the input data is shifted right and the sign bit extended to bit 15.



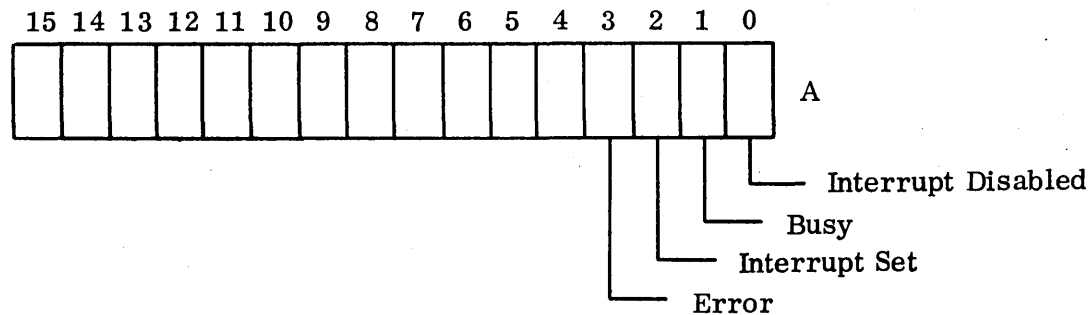
1538 HIGH-SPEED, HIGH-LEVEL, ANALOG INPUT INTERFACE



FUNCTION (OUT)



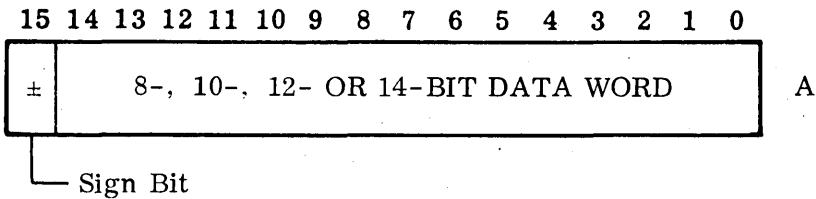
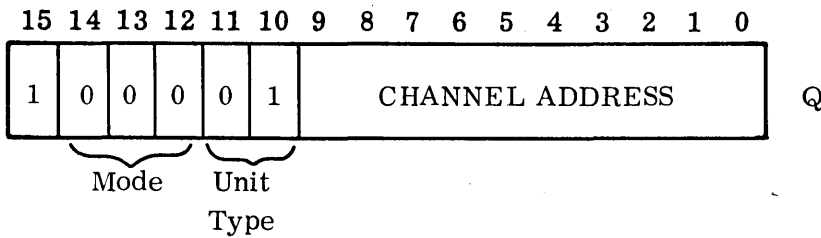
STATUS (INP)



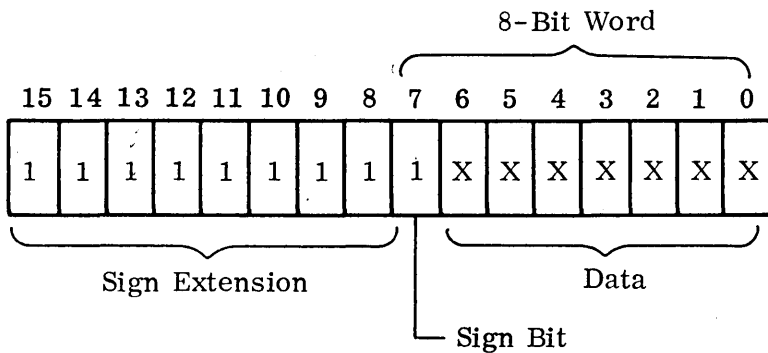
1538 HIGH-SPEED, HIGH-LEVEL, ANALOG INPUT INTERFACE (Continued)

After 1538 has been connected to DCB or BDCB:

DATA TRANSFER (INP)



The Data Word received in the A-Register may be an 8-, 10-, 12- or 14-bit word. The most significant bit of the input word is the sign bit. The sign bit is extended through the unused bits to bit 15. See example below for an 8-bit word input.



Assuming a negative sign bit (bit 7 = "1") the sign of bit 7 is extended through bit 8 to bit 15. If bit 7 was positive ("0"), zeros would be extended.

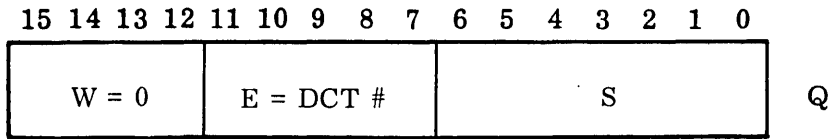
*Standard Word Size

NOTE

1. The data read in is the data converted from the previous channel address. The data from the present channel address will be read on the next input instruction.
2. The channel addressed will not be connected and converted unless a "Read Execute" is used (see page 2-3).



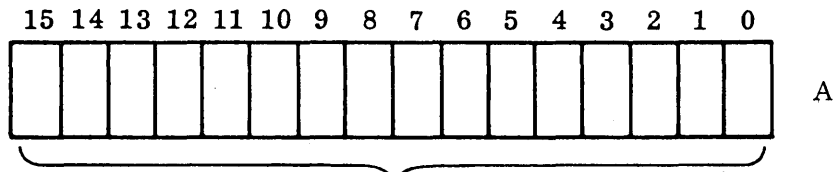
1546/1547 EVENT COUNTER SUBSYSTEM



Station Address

- S = 20 - 1547 #1
- 22 - 1547 #2
- 24 - 1547 #3
- 26 - 1547 #4
- 28 - 1547 #5
- 2A - 1547 #6
- 2C - 1547 #7
- 2E - 1547 #8

STATUS (INP) [S]

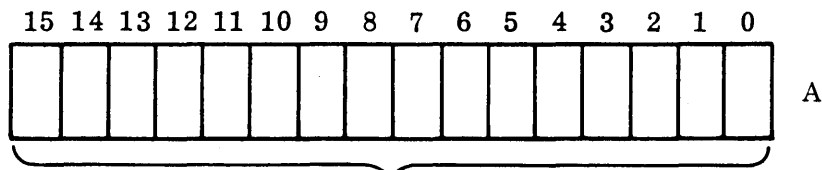


Interrupt F/F in 1547

"0" = Cleared

"1" = Set (counter overflow) (256_{10})

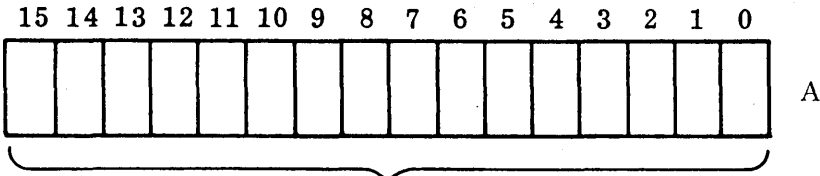
FUNCTION (OUT) [S]



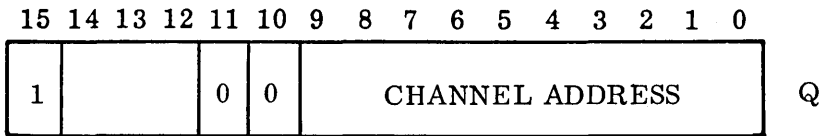
= "1," Acknowledge Interrupt
(reset interrupt F/F) (1547)

1546/1547 EVENT COUNTER SUBSYSTEM (Continued)

MASK (OUT) [S+1]



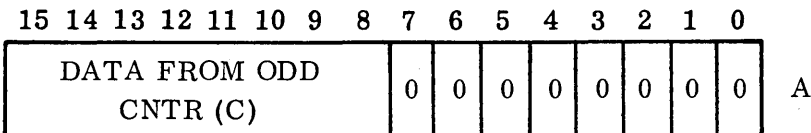
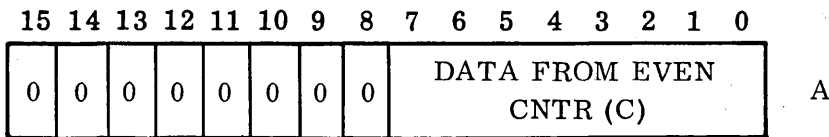
Bit = "1," Set Corresponding Bit in Mask Register
 Bit = "0," Clear Corresponding Bit in Mask Register



- Channel = 200-20F - 1547 #1
- 210-21F - 1547 #2
- 220-22F - 1547 #3
- 230-23F - 1547 #4
- 240-24F - 1547 #5
- 250-25F - 1547 #6
- 260-26F - 1547 #7
- 270-27F - 1547 #8

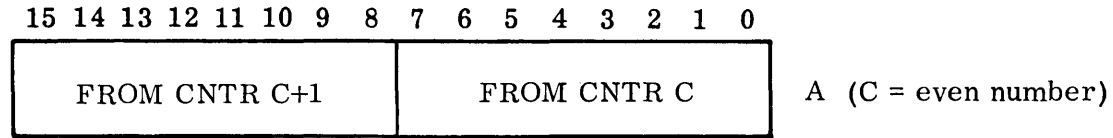
Indicates Channel Address

DATA INPUT (8-BIT COUNTER) (INP)

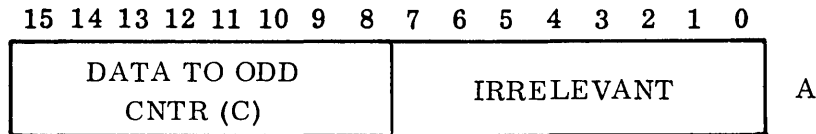
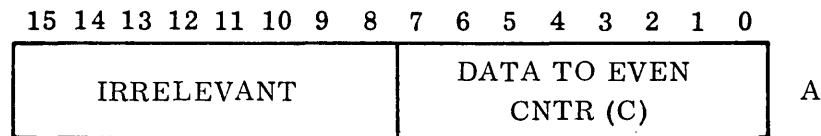


1546/1547 EVENT COUNTER SUBSYSTEM (Continued)

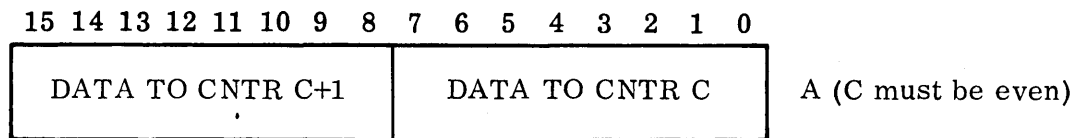
DATA INPUT (16-BIT COUNTER) (INP)



DATA OUTPUT (8-BIT COUNTER) (OUT)

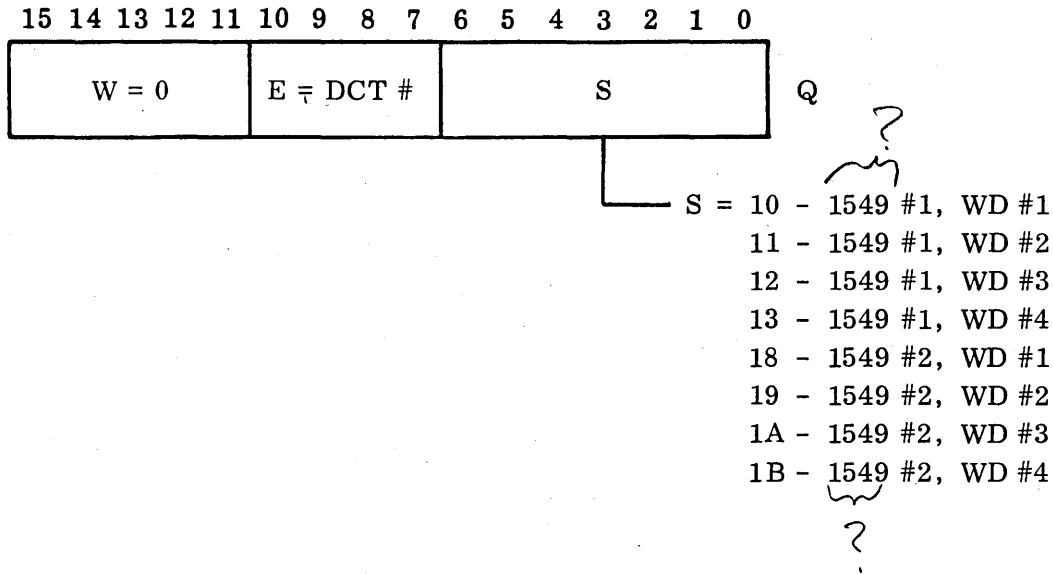


DATA OUTPUT (16-BIT COUNTER) (OUT)

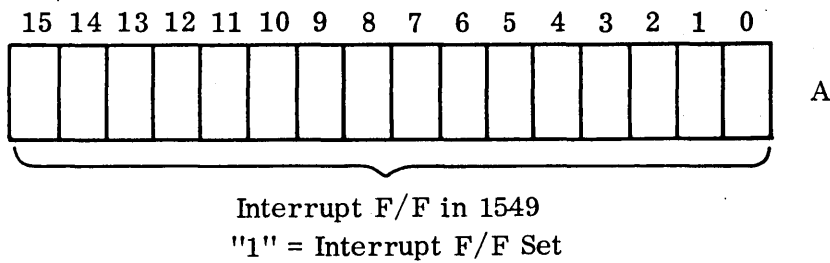




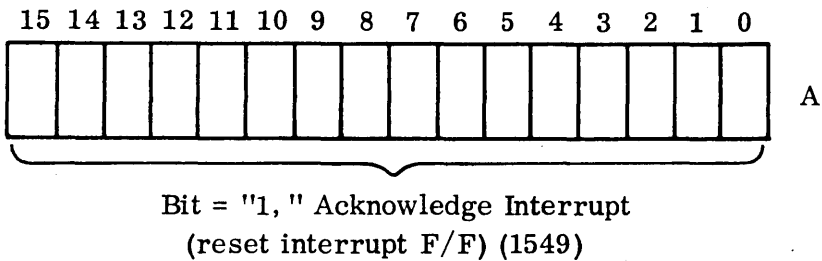
1548/1549 EXTERNAL INTERRUPT SUBSYSTEM



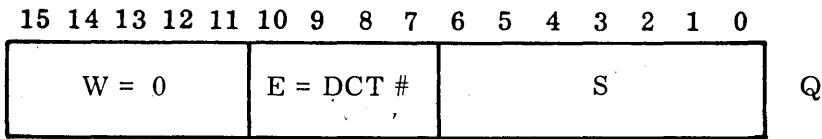
STATUS (INP)



ACKNOWLEDGE INTERRUPT (OUT)

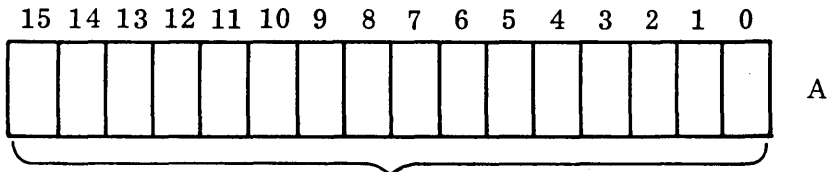


1548/1549 EXTERNAL INTERRUPT SUBSYSTEM (Continued)



- S = 14 - 1549 #1, WD #1
- 15 - 1549 #1, WD #2
- 16 - 1549 #1, WD #3
- 17 - 1549 #1, WD #4
- 1C - 1549 #2, WD #1
- 1D - 1549 #2, WD #2
- 1E - 1549 #2, WD #3
- 1F - 1549 #2, WD #4

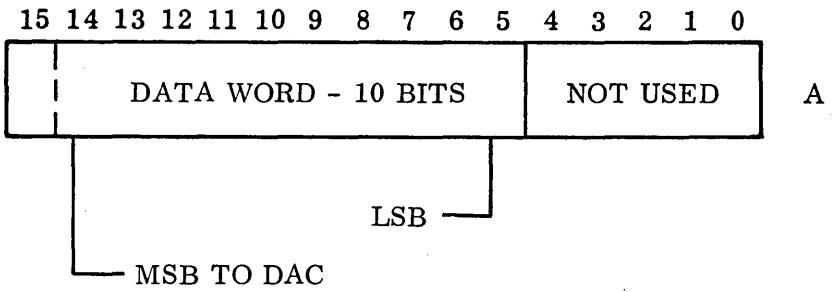
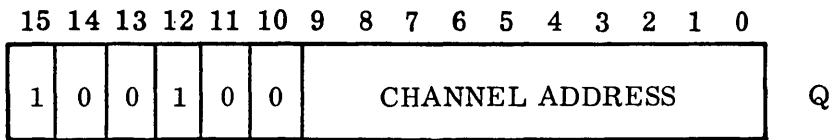
SET MASK (OUT)



Bit = "1," Set Corresponding Bit in
Mask Register (1549)

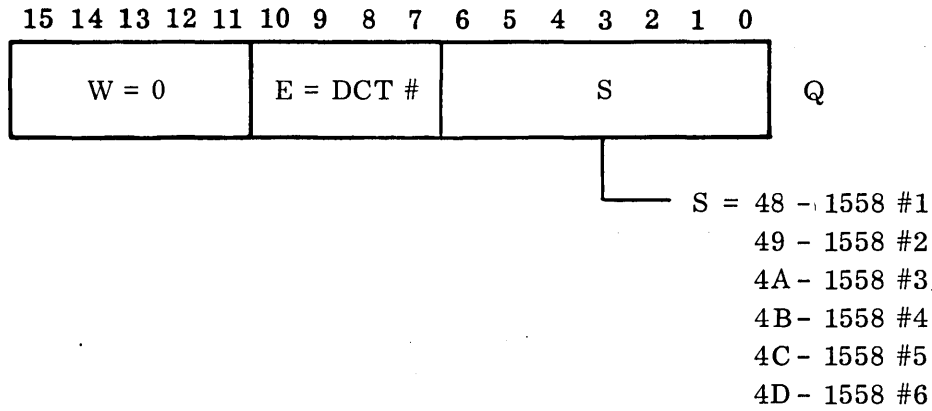
Bit = "0," Clear Corresponding Bit in
Mask Register (1549)

1556 ANALOG (DAC) OUTPUT UNIT

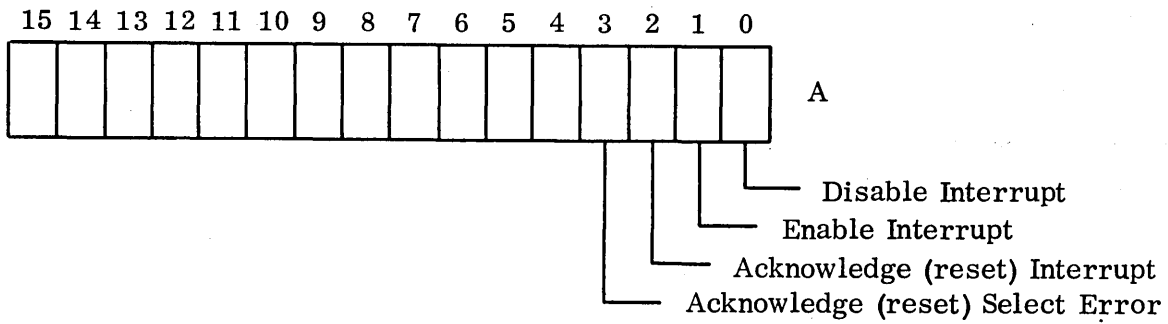




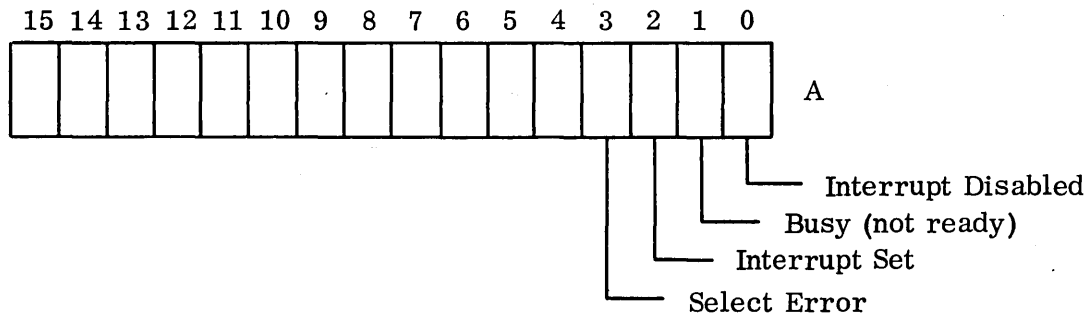
1558 LATCHING RELAY OUTPUT INTERFACE



FUNCTION (OUT)



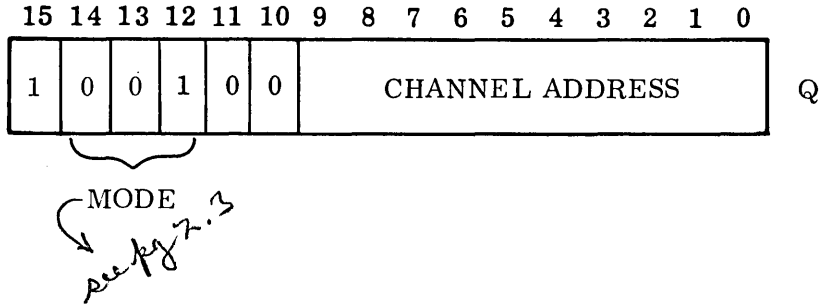
STATUS (INP)



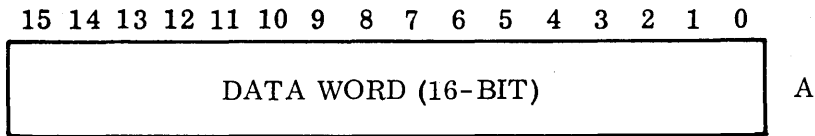
1558 LATCHING RELAY OUTPUT INTERFACE (Continued)

After 1558 is connected to DCB or BDCB

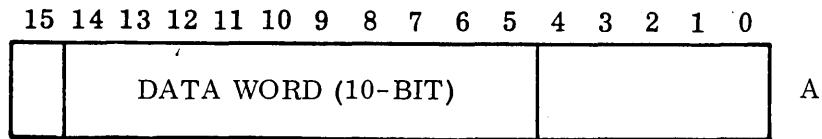
DATA OUTPUT (OUT)



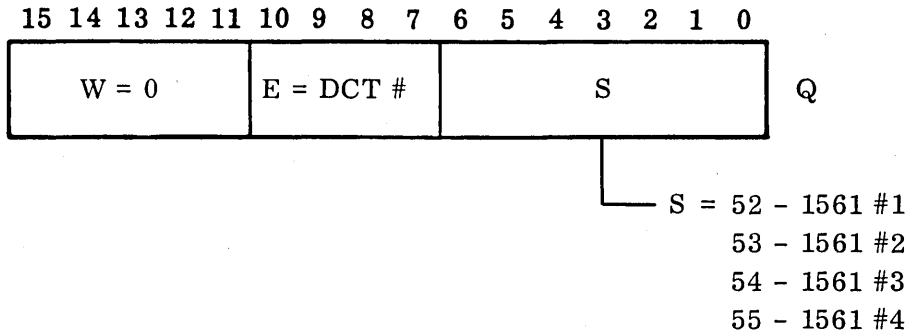
1559 Latching Relay Contact Output Unit



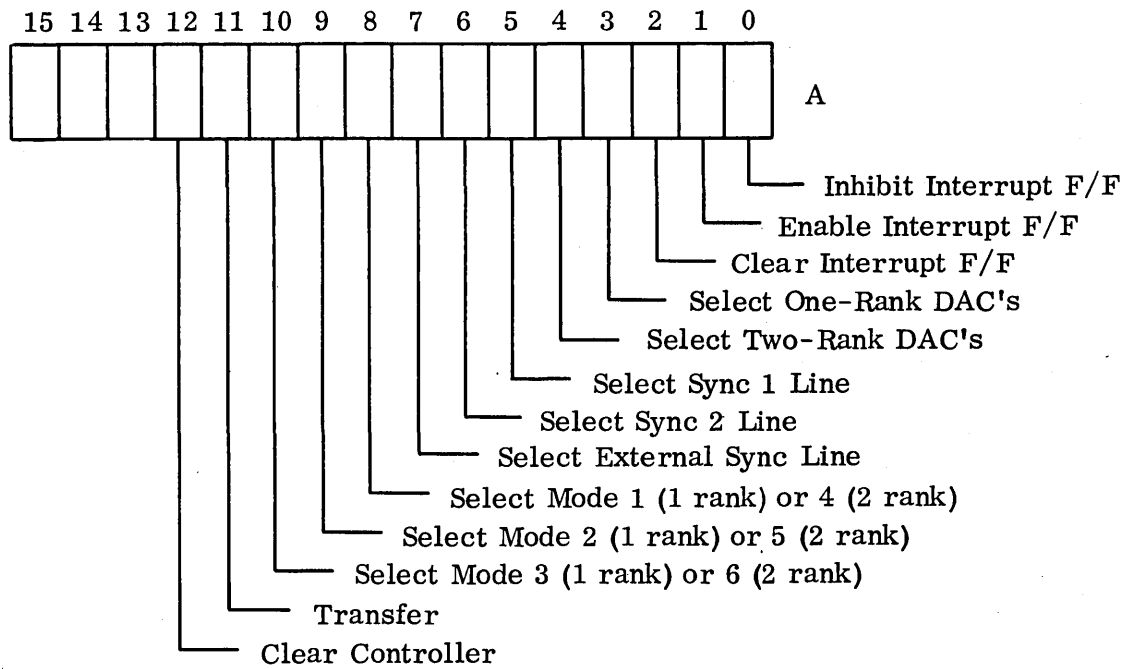
1560 Latching Relay Analog (DAC) Output Unit



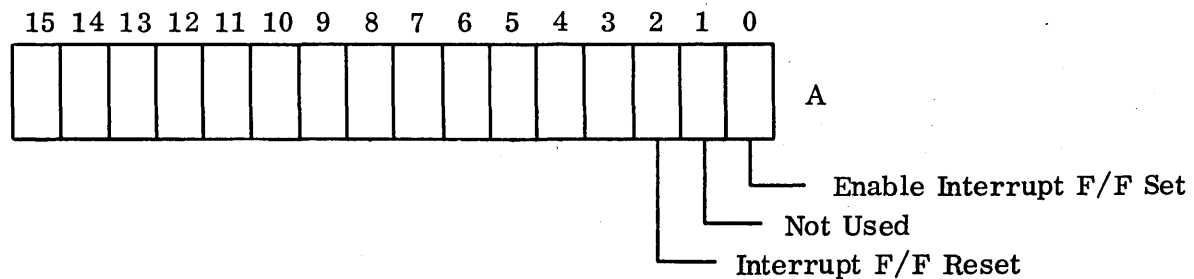
1561 ANALOG OUTPUT INTERFACE



FUNCTION (OUT)



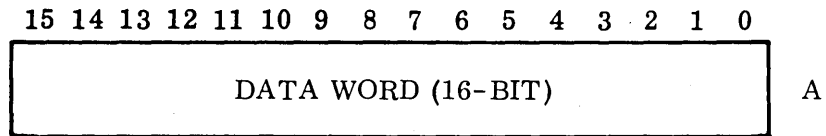
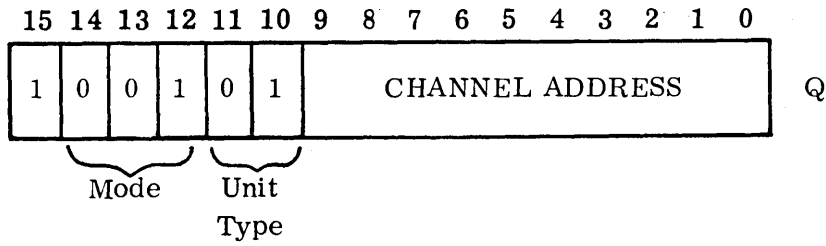
STATUS (INP)



1561 ANALOG OUTPUT INTERFACE (Continued)

After 1561 is connected to DCB or BDCB:

OUTPUT DATA TRANSFER (OUT)

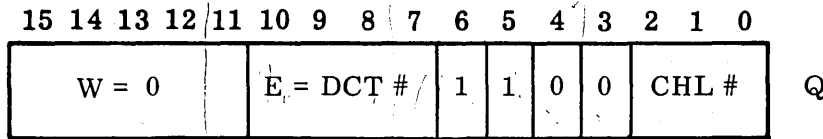


| MODE | MNEMONIC | DESCRIPTION | DATA TRANSFER | | | FUNCTION COMMAND | | SIGNALS REQUIRED | | INHIBITED | TIME BUSY |
|---|-----------------------------------|---|-----------------------------|--------------------|--|---|---|---|----------------|--|--|
| | | | FROM | TO | AT | DCT | 1561 | PREPARATION | EXECUTION | | |
| 1 | One-Rank Normal | Transfers on Address • WEX | (a) DCB (b) DR | DR R1/R2 ANA | WEX WEX + 1 μs | None | AW03, AW08 | ME2T and Data | WEX | Never | 1.5 μsec (DAC's) or 7.5 μsec (Analoks) |
| 2* | One-Rank Synced | Transfers on Sync Pulse | (a) DCB (b) DR | DR R1/R2 ANA | WEX Sync | One of AW05, AW11, AW13 ⁽²⁾ | AW03, AW09 one of AW05- AW07 ⁽¹⁾ | ME2T Data, WEX | Sync | After Loading, ⁽²⁾ Inhibits Further Transfers Until Sync | Same as 1 |
| 3*† | One-Rank Block Sync | Transfer Inhibited Between EOS and Sync | (a) DCB (b) DR | DR R1/R2 ANA | WEX • BLKF ⁽³⁾ WEX • BLKF ⁽³⁾ + 1 μs | One of AW05, AW11, AW13 ⁽¹⁾⁽⁴⁾ | AW03, and One of AW03- AW07 ⁽¹⁾ | Load 1574 Sequential Addressing Unit ME2T and Data | WEX | Between EOS ⁽²⁾ and Sync | Same as 1 |
| 4* | Two-Rank Normal ⁽⁵⁾ | Transfer-C on Sync | (a) DCB (b) DR (c) R1 | DR R1 R2 | WEX WEX + 1 μs Sync ⁽¹⁾ | One of AW05, AW11, AW13 ⁽¹⁾ | AW04, AW08 One of AW05- AW07 | Load All First DAC Ranks as in Mode 1 | Sync | Never | 1.5 μs for Loading Each First DAC Rank; None For Transfer to Second Rank ⁽⁵⁾ |
| 5 | Two-Rank Word Sync ⁽⁵⁾ | Transfer-C on Function Word | (a) DCB (b) DR (c) R1 | DR R1 R2 | WEX WEX + 1 μs Function + 1 μs | None | (a) AW04, AW10 (b) AW11 | Load All First DAC Ranks as in Mode 1 | Function #2 | Never | Same as 4 ⁽⁵⁾ |
| 6† | Two-Rank EOS Sync ⁽⁵⁾ | Transfer-C on EOS Signal | (a) DCB (b) DR (c) R1 | DR R1 R2 | WEX WEX + 1 μs EOS ⁽⁴⁾ | None ⁽⁴⁾ | AW04, AW09 | (a) Load 1574 (b) Load All First DAC Ranks as in Mode 1 | EOS | Never | Same as 4 ⁽⁵⁾ |
| <p>GLOSSARY</p> <p>WEX - Write Execute DCB - Data and Control Bus DR - Data Register, 1561 R1 - 1st Rank of DACs (input) R2 - 2nd Rank of DACs (output) BLKF - EOS • SYNC (approximately) EOS - End of Sequence ME2T - ANA1 • CHAT • CHL ANA - Analok Channel Selected</p> <p>* Requires a Sync Source † Requires a 1574 Sequential Addressing Unit</p> <p>NOTES (1) Sync Interrupt Available in DCT or 1561. (2) Transfer Inhibited by Write Ready Remaining False After ME2T. No WEX Command is Generated. (3) Transfer Inhibited from EOS to Sync. (4) EOS Interrupt Available. (5) Analoks not normally used in this Mode.</p> | | | | | | | | | | | |

MODES OF OPERATION IN THE 1561 ANALOG OUTPUT INTERFACE UNIT

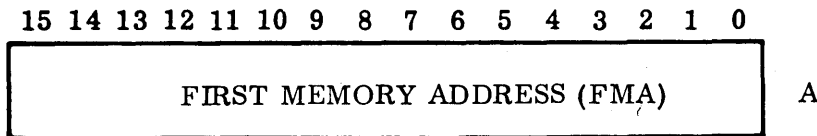


1571 CHAINING BUFFER CHANNEL

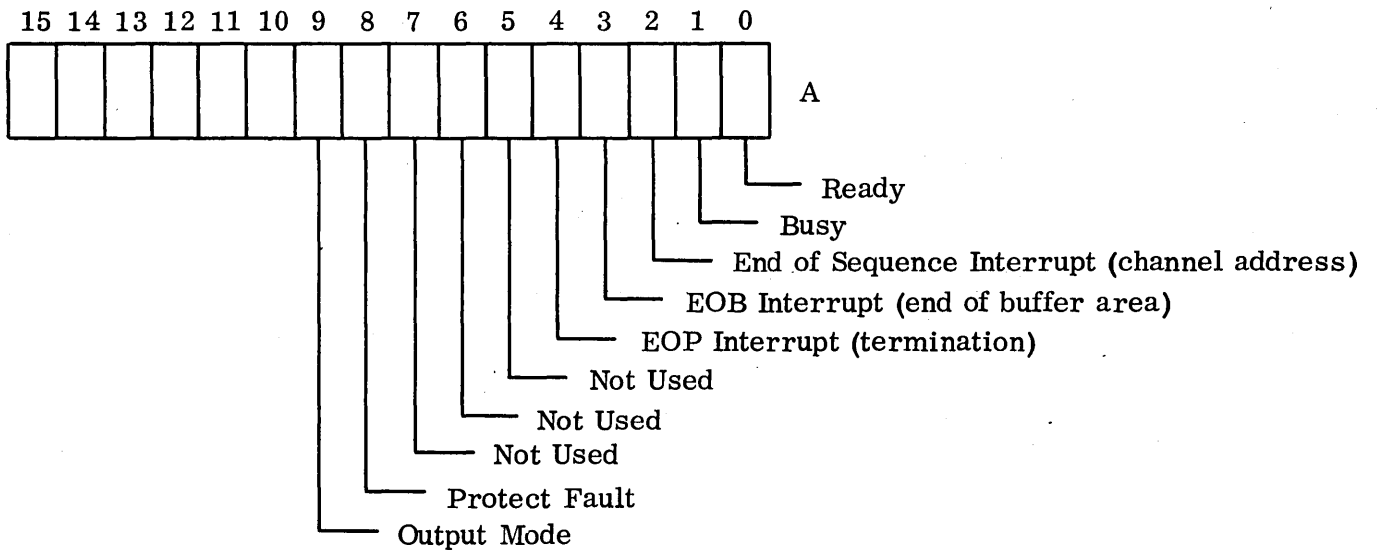


Channel Number - must equal the number of the BDC (buffered data channel) being addressed (0→7) and selects one of the 8 possible PBC connected to the 1797 buffered I/O Interface

START COMMAND (OUT)



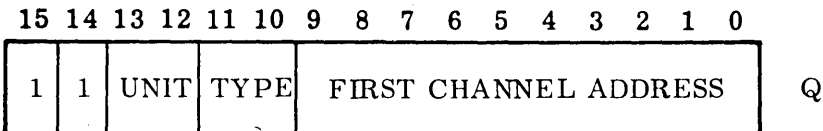
STATUS (INP)



1571 CHAINING BUFFER CHANNEL (Continued)

CHANNEL-ADDRESS-SETUP COMMAND (OUT)

The command is a mode 5, 6, or 7 Continue command and is identical to the Setup command for the 1574 Sequential Addressing Unit.



CONTINUE
operation
addr
1571

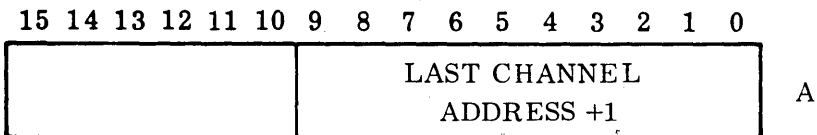
ANALOG/DIGITAL

"0" = 1574 Sequential Address (BIT 14)

"1," "2," or "3" = Channel Address Control Section for each of three 1571's connected to a 1797 Buffered I/O Interface (BITS 13+12)

0 = 1574
 1 = 1571A #1
 2 = 1571B #2
 3 = 1571C

FCA specifies the first address in the sequence of channel addresses to be generated



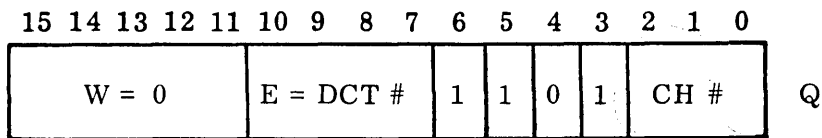
NOTE: Channel Address - Setup command is rejected by the 1571 (External Reject) except when the channel is in the direct mode; i. e., is not performing a Buffered I/O operation.

CHANNEL-ADDRESS-STATUS COMMAND (INP)

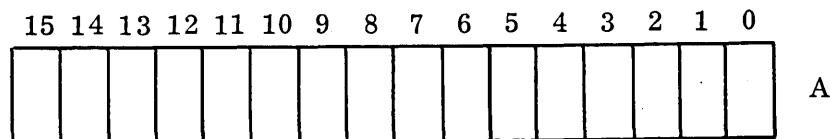
Q-register has same format as Setup command (channel address) except an INP is executed. The A-register will contain the contents of the Next-Channel-Address (NCA) register. The 1571 accepts and responds to this command at all times.

1571 CHAINING BUFFER CHANNEL (Continued)

FUNCTION COMMAND (OUT)



Channel Number must equal the number of the PBC (priority buffered channel)

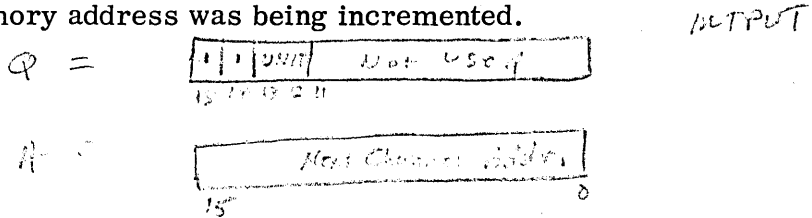


Bit 15: Stop Buffered I/O Operation*
 Bit 14: Restart Buffered I/O Operation
 Bit 13: Acknowledge EOS Interrupt
 Bit 12: Acknowledge EOB Interrupt
 Bit 11: Acknowledge EOP Interrupt

MEMORY-ADDRESS-STATUS COMMAND (INP)

The Q-register has same format as a Buffer Channel Function command except that an INP is executed.

The A-register will contain the contents of the next-memory-address register. If the command is received at the instant that the 1571 is performing a data transfer, the 1571 makes Bit 15 (of the status word) a "1." This indicates that a data transfer was taking place and the memory address was being incremented.



*If a Stop function is used during an I/O operation, transfer of the current data word is completed before the channel stops.

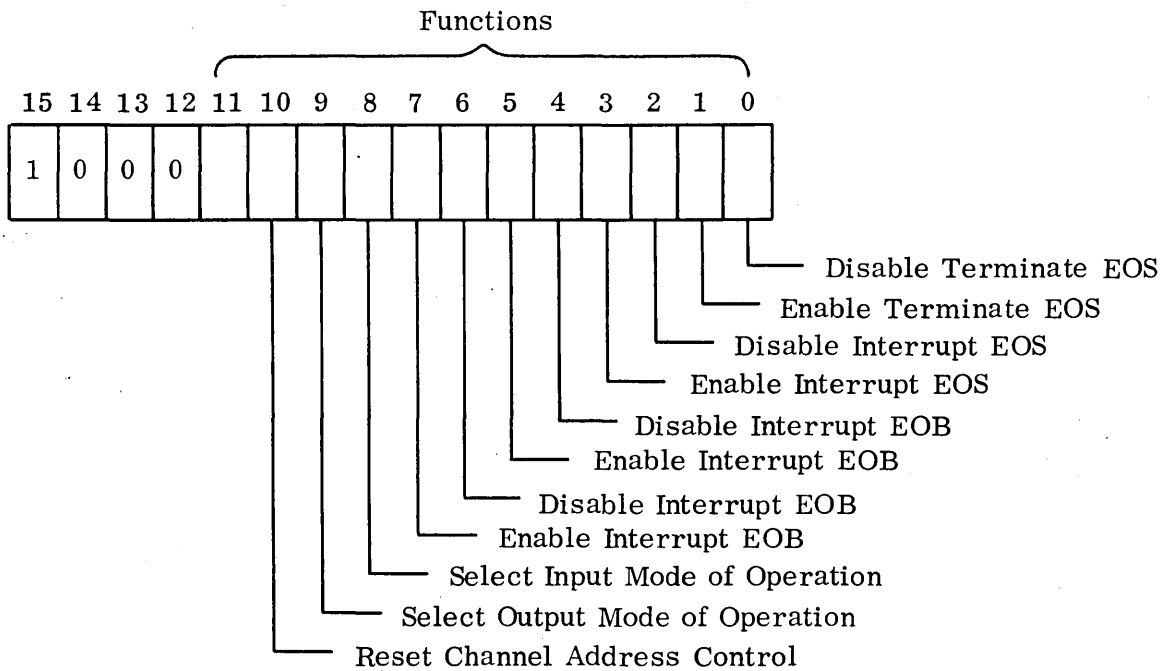
1571 CHAINING BUFFER CHANNEL (Continued)

NOTE: The computer program should check for a negative value status word (bit 15 = "1"). If this occurs, the Status command should be repeated until such time as bit 15 = "0."

After the 1571 has been either initiated or set up, the 1571 reads a word out of memory. If bit 15 = "1," it is either a control function word or a channel address word. The control function word establishes operating conditions within the 1571.

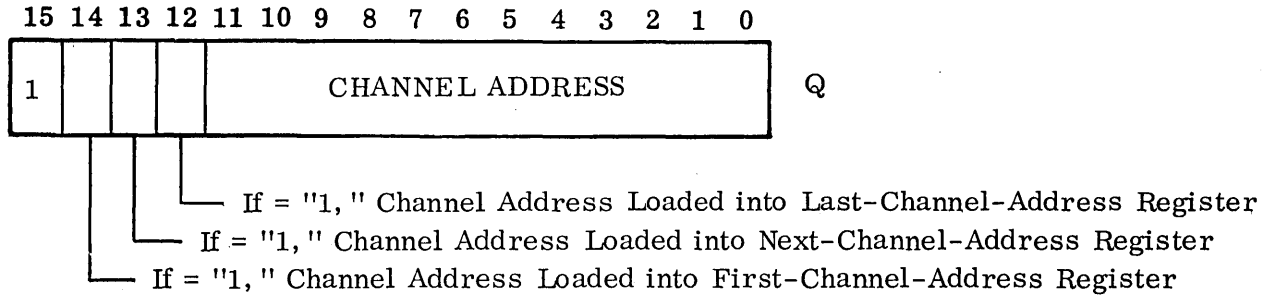
The channel address words are used to initialize the channel address control of the 1571.

CONTROL FUNCTION WORD FORMAT



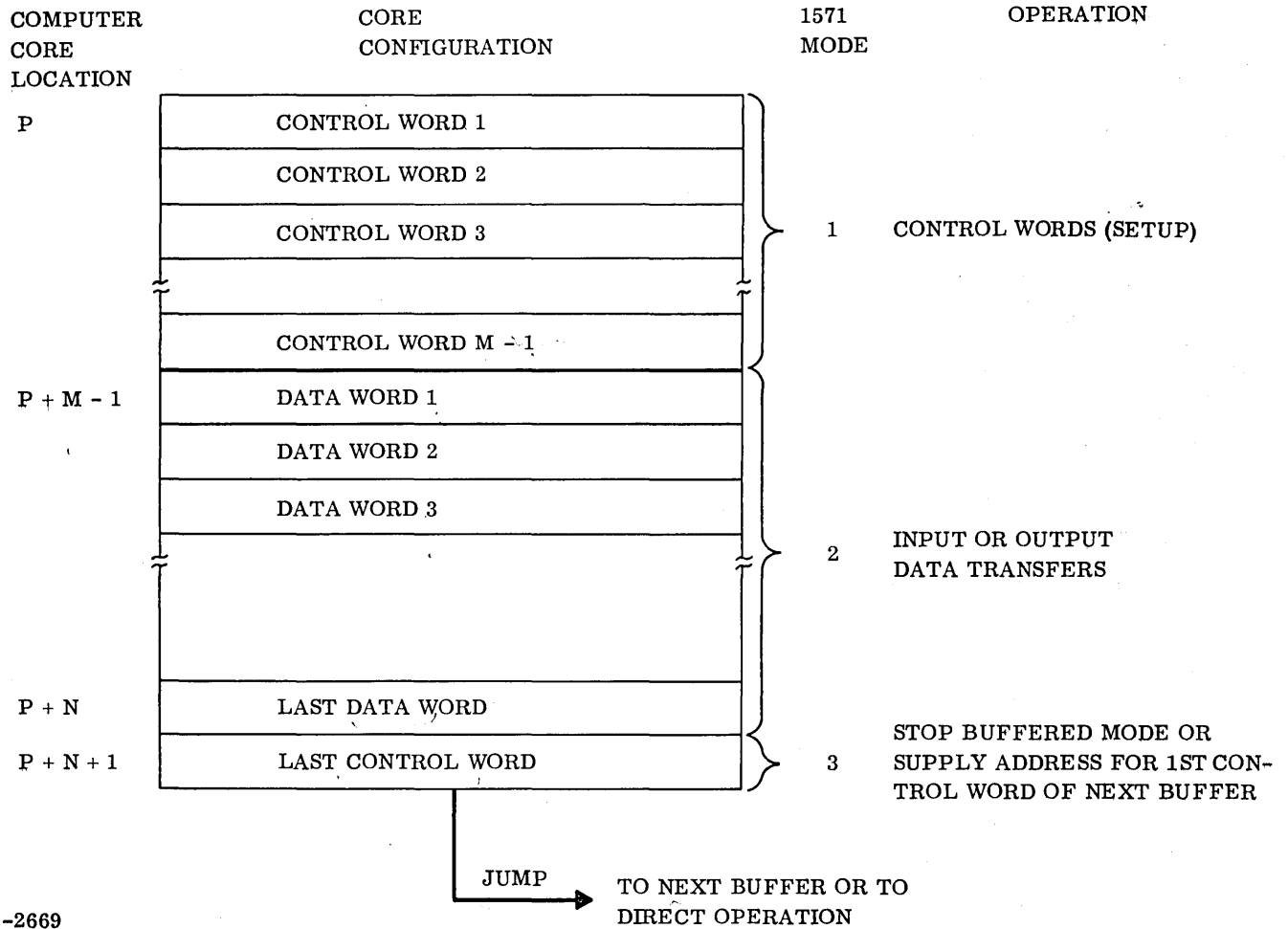
1571 CHAINING BUFFER CHANNEL (Continued)

CHANNEL ADDRESS WORD FORMAT



NOTE: At least one of the 3 bits (12, 13, 14) must be a "1." A single address word can cause a channel address to be loaded into more than one of the registers.

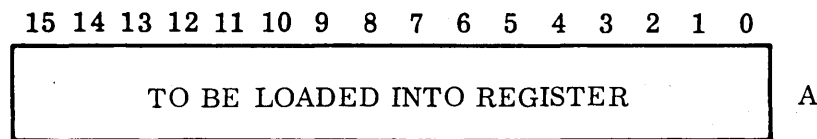
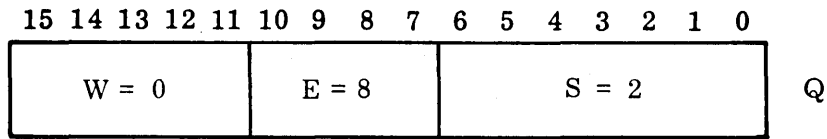
TYPICAL BUFFER AREA STRUCTURE FORMAT FOR 1571





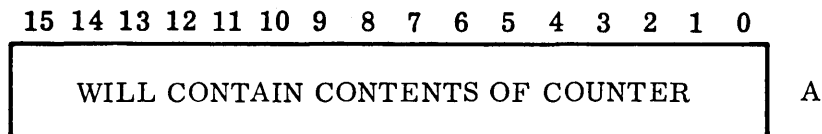
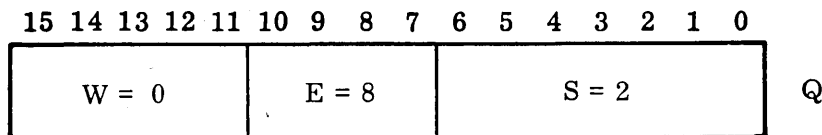
1572 PROGRAMMABLE SAMPLE RATE UNIT

REGISTER LOAD (OUT)



When this is executed, the counter is cleared (sample rate generator mode).

COUNTER READ (INP)

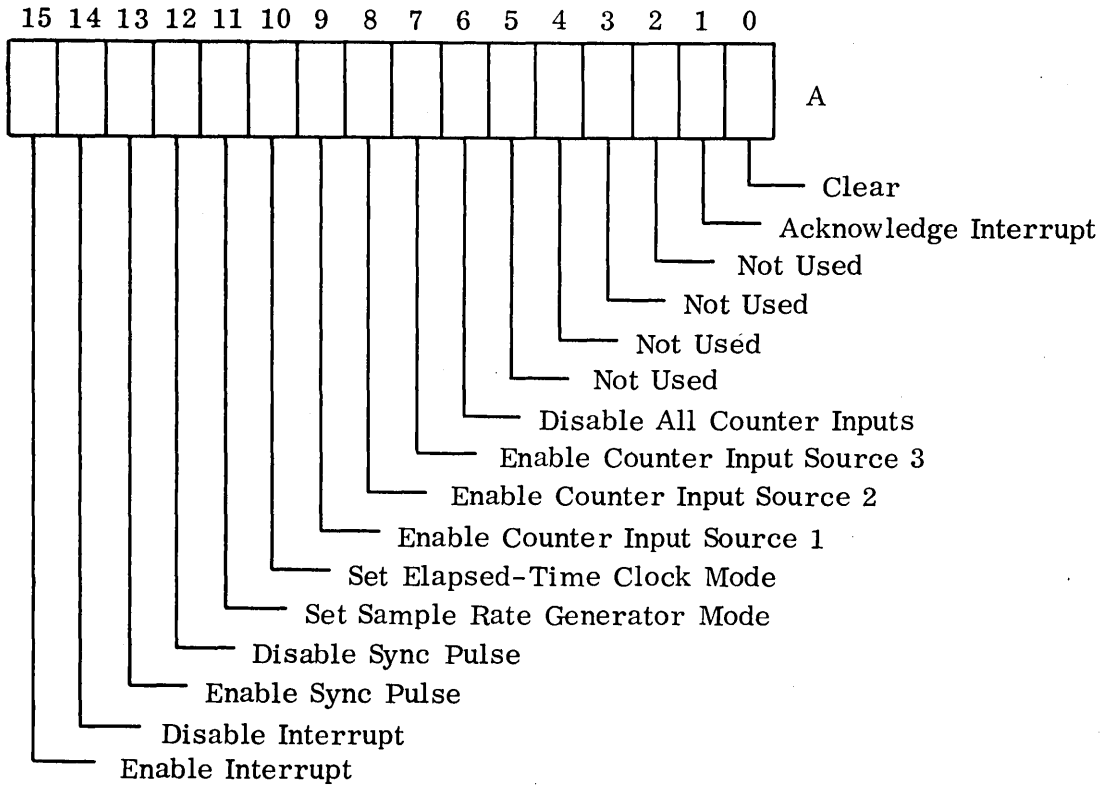


STATUS:

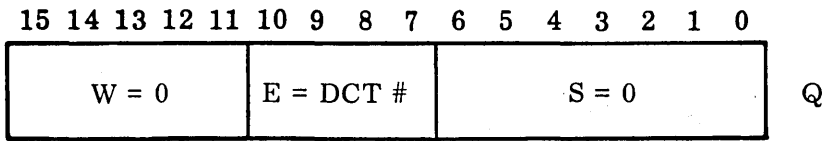
Interrupt bit set in system status word.

1572 PROGRAMMABLE SAMPLE RATE UNIT (Continued)

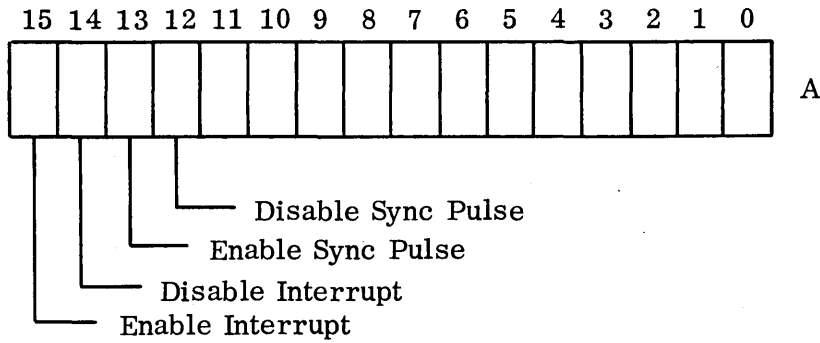
FUNCTION (OUT): W = 0 E = DCT # S = 3



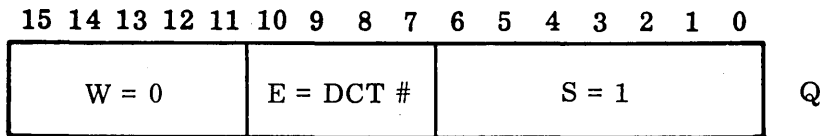
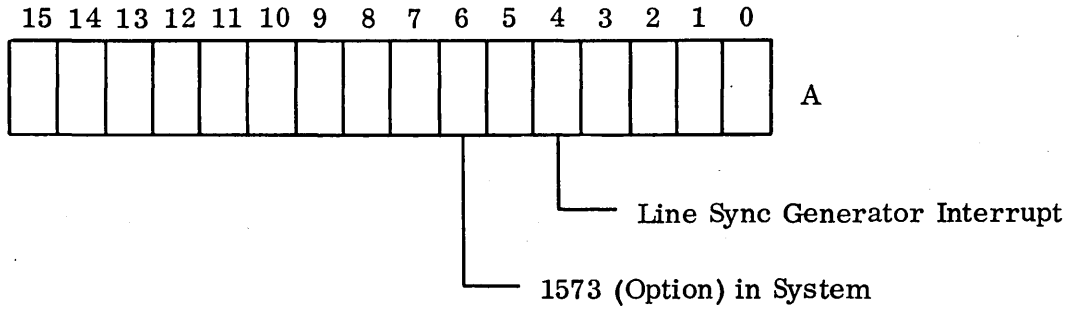
1573 LINE SYNCHRONIZED TIMING GENERATOR



FUNCTION (OUT)



STATUS (INP)



1573 LINE SYNCHRONIZED TIMING GENERATOR (Continued)

ACKNOWLEDGE INTERRUPT (OUT)*

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0



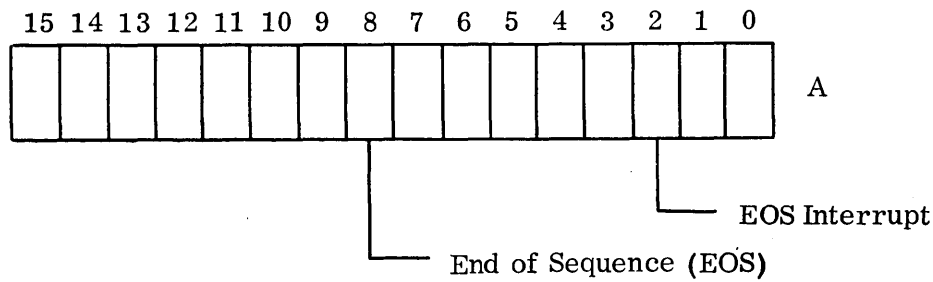
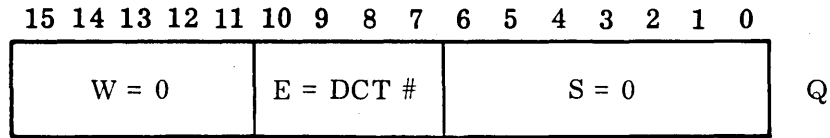
A

*Resets sync interrupt F/F; if F/F was not set, a reject is generated.

1574 SEQUENTIAL ADDRESSING UNIT

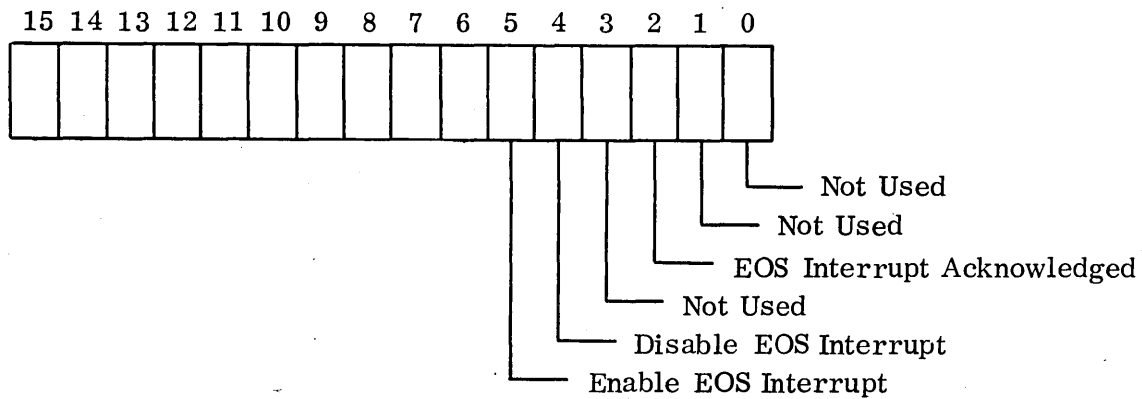
TO ACTIVATE 1574 (CONNECT DCT)

TO STATUS 1574 (MEANINGFUL STATUS OF 1574) (INP)



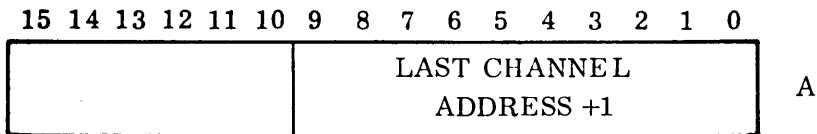
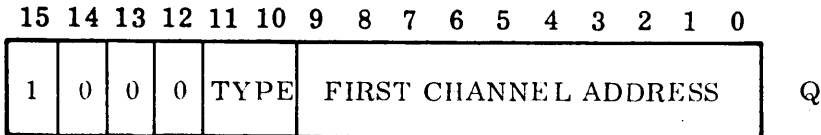
TO ACTIVATE 1574 (CONNECT DCT)

TO FUNCTION 1574 (OUT)

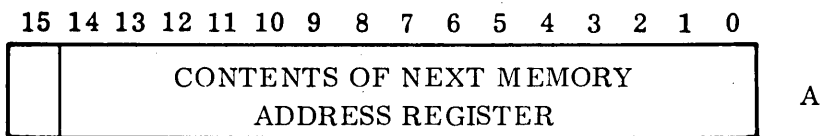
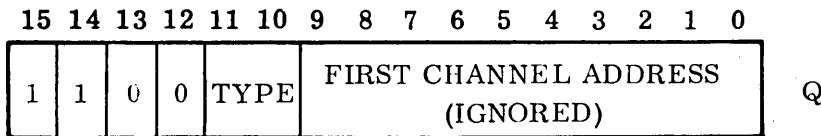


1574 SEQUENTIAL ADDRESSING UNIT (Continued)

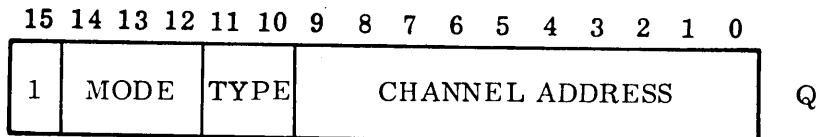
SETUP (OUT)



STATUS (INP)



RANDOM ADDRESS COMMANDS



(INP)

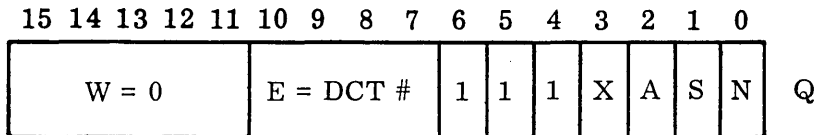
MODE = 0 Random Address Read Only: Reads data from the specified channel address but does not initiate any actions within the addressed unit. The 1574 is not affected by this command.

1574 SEQUENTIAL ADDRESSING UNIT (Continued)

(OUT)

- MODE = 1 Executes a normal data transfer with the specified channel and does not affect the 1574.
- MODE = 2 Random Address and Hold: Executes a normal data transfer with the specified channel. The specified channel address is then placed in the 1574's Next-Address register, changing the sequence. An External Reject occurs if this command is executed when the 1574 is not present in the system.
- MODE = 3 Random Address and Increment: Executes a normal data transfer with the specified channel. The specified channel address is incremented by one and placed in the 1574's Next-Address register modifying the sequence. An external reject occurs if this command is executed when the 1574 is not present in the system.

SEQUENTIAL I/O COMMANDS (NAD)

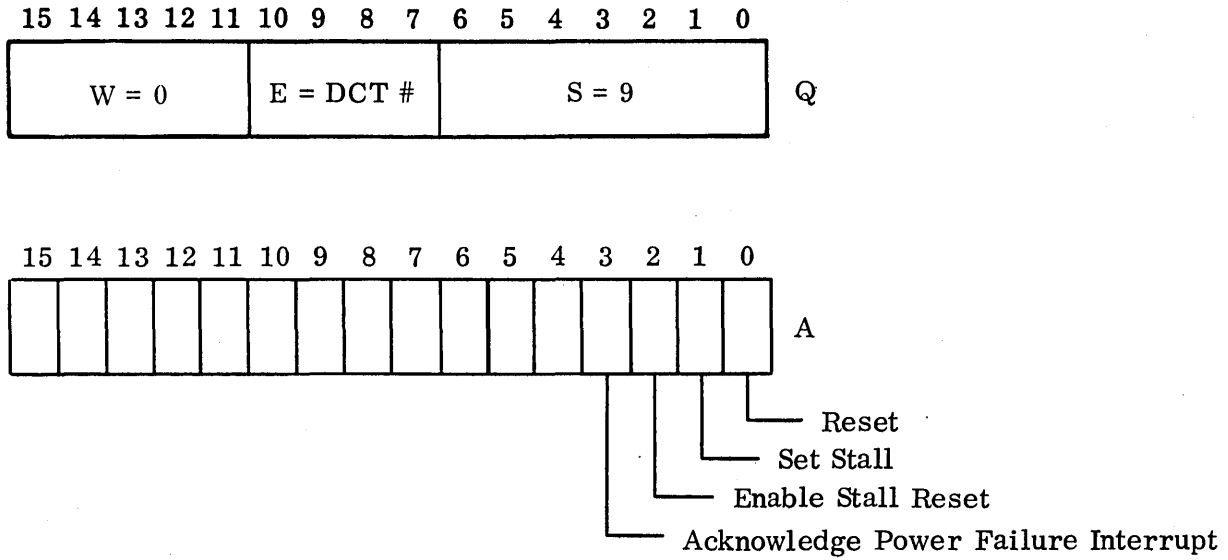


- A (BIT 2) = "1" "A" Bit replaces Bit 10 of the channel address to be used for this I/O operation provided that Bit 11 of the address is zero. This enables switching between Digital Input/Output Group and Analog Input/Output Group I without changing the 1574's sequence.
- S (BIT 1) = "1" The Present-Address register contents are incremented when transferred back to the Next-Address register.
- = "0" The transfer occurs without incrementing
- N (BIT 0) = "1" Inhibits Execute signal to peripheral. Reply response and data transfer occur for input operations. Internal reject occurs for output operations.
- = "0" Normal data transfer, address modification, etc. occurs.

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1577 STALL ALARM

FUNCTION (OUT)

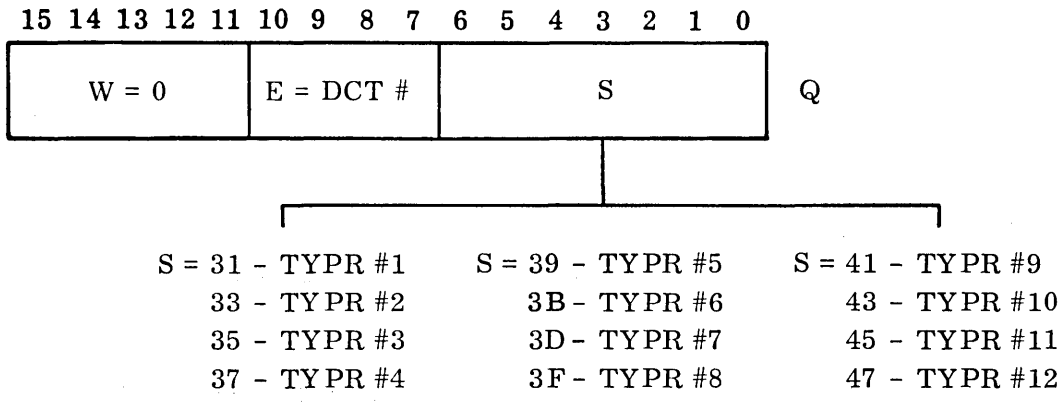


STATUS (INP)

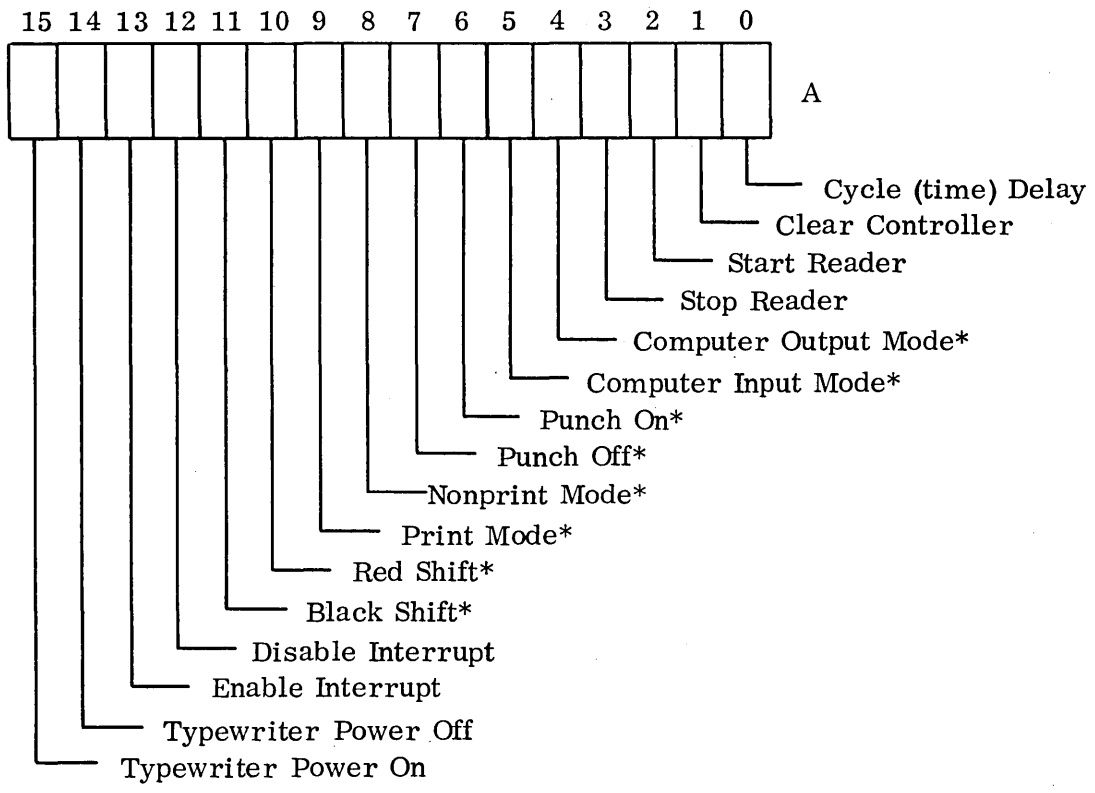
NOTE: See DCT Station 1 status word on page 2-9.



1581/1582 LOGGING TYPEWRITER (FLEXOWRITER)



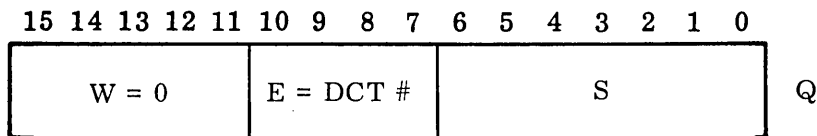
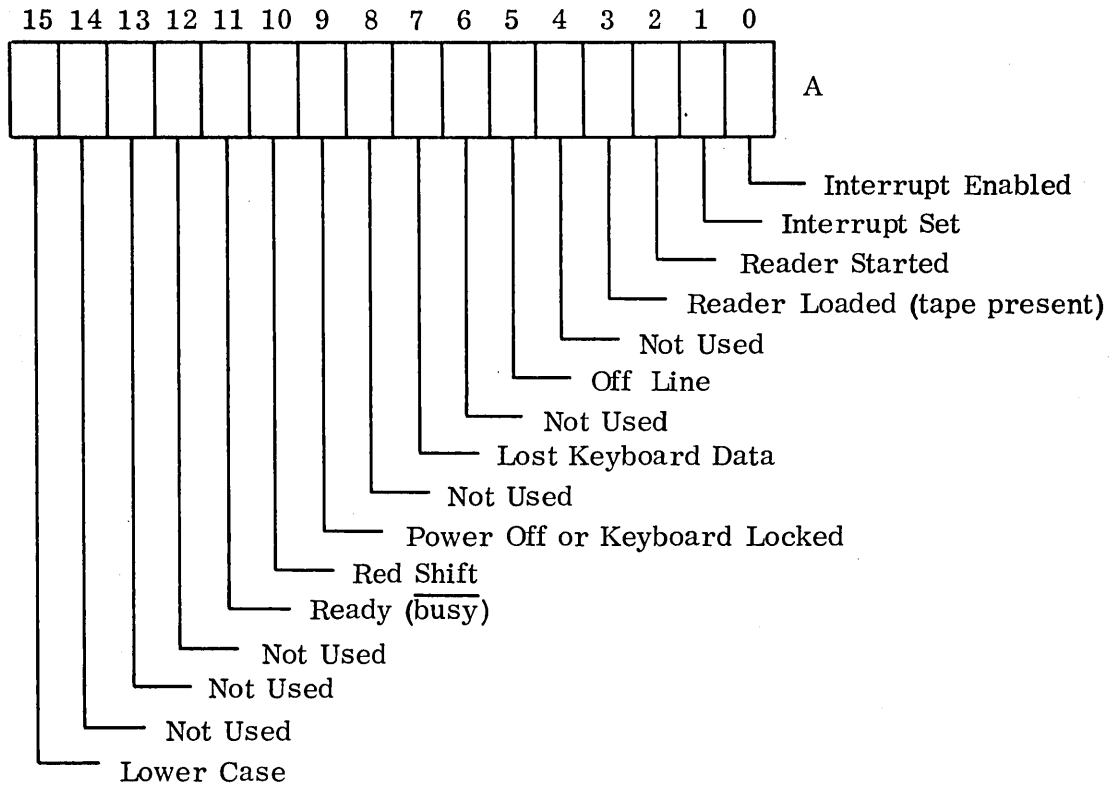
FUNCTION (OUT)



*Must be used with time delay Function command.

1581/1582 LOGGING TYPEWRITER (FLEXOWRITER) (Continued)

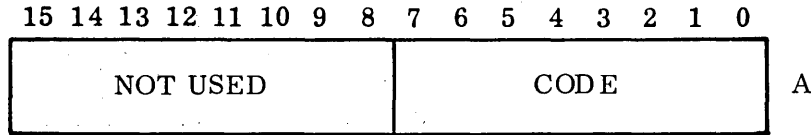
STATUS (INP)



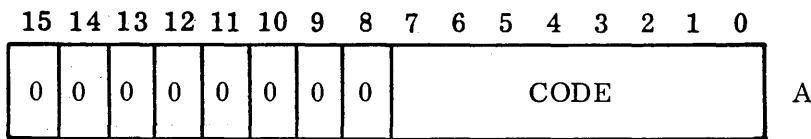
- | | | |
|------------------|------------------|------------------|
| S = 30 - TYPR #1 | S = 38 - TYPR #5 | S = 40 - TYPR #9 |
| 32 - TYPR #2 | 3A - TYPR #6 | 42 - TYPR #10 |
| 34 - TYPR #3 | 3C - TYPR #7 | 44 - TYPR #11 |
| 36 - TYPR #4 | 3E - TYPR #8 | 46 - TYPR #12 |

1581/1582 LOGGING TYPEWRITER (FLEXOWRITER) (Continued)

DATA (OUT)



DATA (INP)



INTERRUPT:

- | | |
|-------|---|
| SET | Input from the keyboard Input from the reader End of an output cycle to printer and/or punch START READ pushbutton pushed NONPRINT pushbutton pushed Line Delay Function Command |
| CLEAR | Executing an Input Instruction Executing an Output Instruction Executing a Clear Controller Function Command |

1581/1582 LOGGING TYPEWRITER (FLEXOWRITER) (Continued)

STANDARD ASCII CODE

| | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | |
|----|---|-----|---|---|---|----|---|---|----|----|---|---|---|----|----|----|-----|
| | 0 | | | | | | | | BS | HT | | | | CR | SO | SI | |
| | 1 | SOH | | | | | | | | | | | | | | | |
| LC | 2 | SP | ! | | # | \$ | % | ' | (|) | * | + | , | - | . | / | |
| UC | 3 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | : | : | < | = | > | ? |
| UC | 4 | ' | A | B | C | D | E | F | G | H | I | J | K | L | M | N | O |
| UC | 5 | P | Q | R | S | T | U | V | W | X | Y | Z | [| ~ |] | ^ | _ |
| LC | 6 | @ | a | b | c | d | e | f | g | h | i | j | k | l | m | n | o |
| LC | 7 | p | q | r | s | t | u | v | w | x | y | z | { | ~ | } | | DEL |

Control Functions:

CR = Carriage Return

BS = Back Space

HT = Tab

SO = Lower Case

SOH = Stop Code

SP = Space

DEL = Delete

SI = Shift in or Upper Case

1581/1582 LOGGING TYPEWRITER (FLEXOWRITER) (Continued)

1581/1582 LOGGING TYPEWRITER CODE (ASCII SUBSET)

PAPER TAPE

| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|----|---|----|-----|---|---|----|---|---|---|----|----|---|---|---|----|----|-----|
| | 0 | | | | | | | | | | HT | | | | | | S1 |
| | 8 | | | | | | | | | BS | | | | | CR | S0 | |
| | 9 | | S0N | | | | | | | | | | | | | | |
| | A | SP | | | | | | | | | | | | | | | |
| | F | | | | | | | | | | | | | | | | DEL |
| UC | 3 | 0 | | | 3 | | 5 | 6 | | | 9 | : | | < | | | ? |
| UC | B | | 1 | 2 | | 4 | | | 7 | 8 | | | ; | | = | > | |
| UC | 4 | | A | B | | D | | | G | H | | | K | | M | N | |
| UC | C | | | | C | | E | F | | | I | J | | L | | | O |
| UC | 5 | P | | | S | | U | V | | | Y | Z | | | | | |
| UC | D | | Q | R | | T | | | W | X | | | [| |] | | |
| LC | 3 | | | | # | | % | & | | |) | * | | , | | | / |
| LC | B | | ! | " | | \$ | | | ' | (| | | + | | - | . | |
| LC | 4 | | a | b | | d | | | g | h | | | k | | m | n | |
| LC | C | @ | | | c | | e | f | | | i | j | | l | | | o |
| LC | 5 | p | | | s | | u | v | | | y | z | | | | | |
| LC | D | | q | r | | t | | | w | x | | | { | | } | | |

PARITY
BIT
(EVEN)

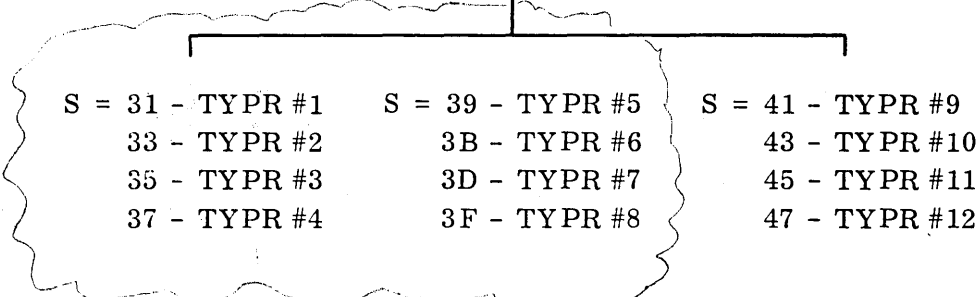
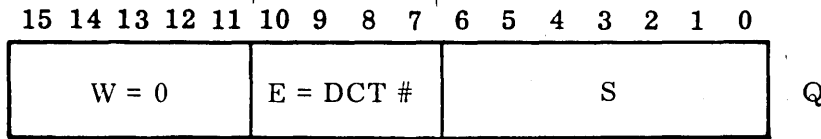


PAPER TAPE CHANNELS

| | | | | | | | | |
|---|---|---|---|---|------|---|---|---|
| 8 | 7 | 6 | 5 | 4 | FEED | 3 | 2 | 1 |
|---|---|---|---|---|------|---|---|---|



1583/1584 LOGGING TYPEWRITER (SELECTRIC)



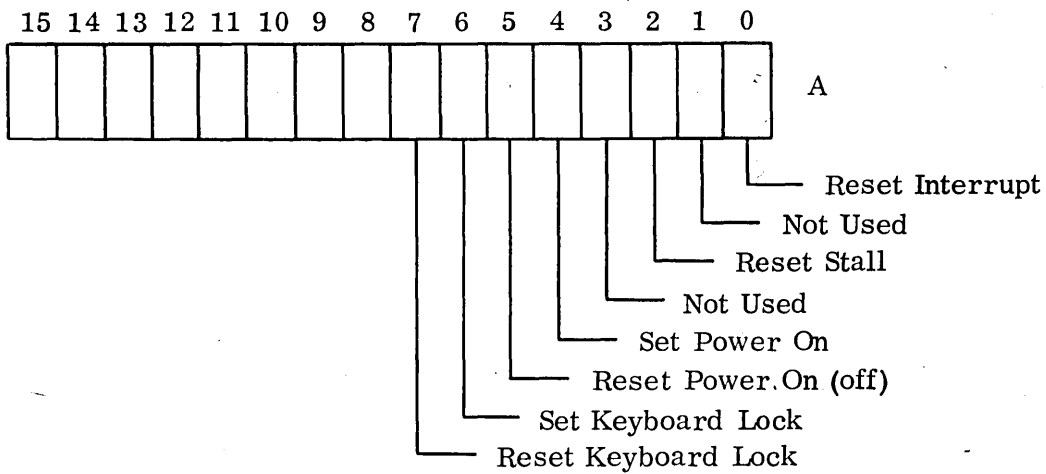
D=1

| WES | SAC | NAC |
|------|------|------|
| 0431 | AP-A | CU-A |
| 0433 | AP-U | CU-U |
| 0435 | RU-A | CO-A |
| 0437 | RU-U | CO-U |
| 0439 | DH-A | CK-A |
| 043B | DH-U | CK-U |
| 043D | HH-A | --- |
| 043F | HH-U | --- |

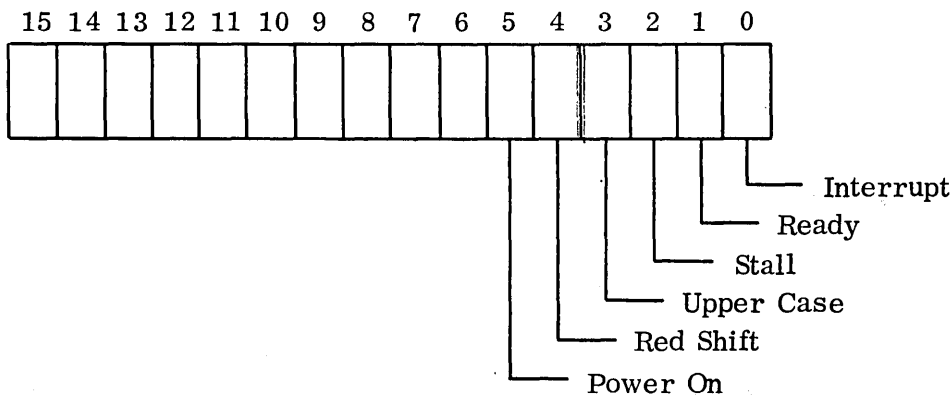
D=0 (see pg. 16-2)

| WES | SAC | NAC |
|------|------|------|
| 0430 | AP-A | CU-A |
| 0432 | AP-U | CU-U |
| 0434 | RU-A | CO-A |
| 0436 | RU-U | CO-U |
| 0438 | DH-A | CK-A |
| 043A | DH-U | CK-U |
| 043C | HH-A | --- |
| 043E | HH-U | --- |

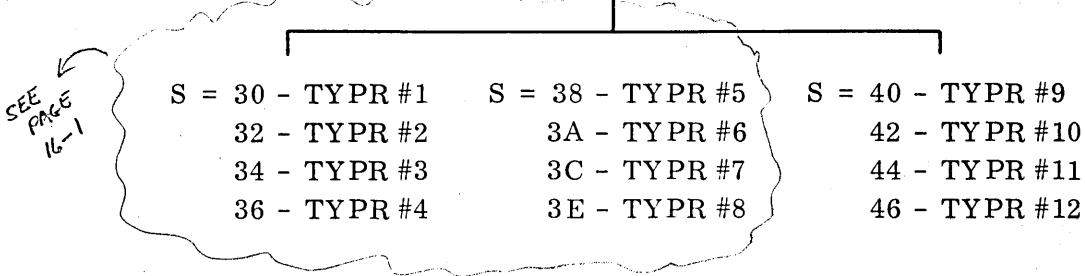
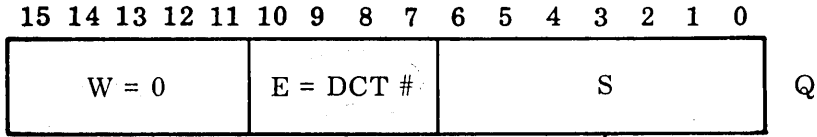
FUNCTION (OUT)



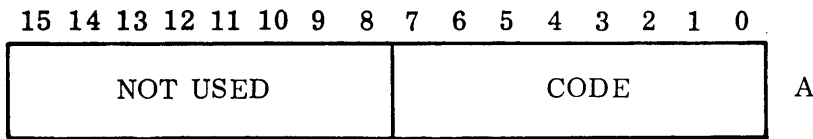
STATUS (INP)



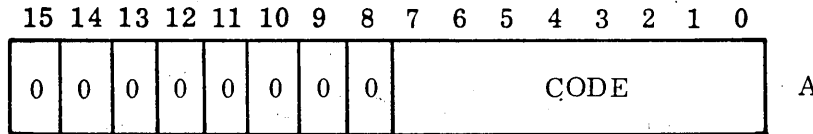
1583/1584 LOGGING TYPEWRITER (SELECTRIC) (Continued)



DATA (OUT)



DATA (INP)



SEE PAGE 16-3

1583/1584 LOGGING TYPEWRITER (SELECTRIC) (Continued)

1583 SELECTRIC I/O CODES

| UC | LC | CODE |
|----|----|------|
| A | a | 1C |
| B | b | 20 |
| C | c | 2C |
| D | d | AD |
| E | e | 25 |
| F | f | 0E |
| G | g | 8F |
| H | h | A1 |
| I | i | 94 |
| J | j | 07 |
| K | k | A4 |
| L | l | 29 |
| M | m | 1F |
| N | n | 26 |
| O | o | 19 |
| P | p | 85 |
| Q | q | 04 |
| R | r | 9D |
| S | s | 91 |

| UC | LC | CODE |
|----|----|------|
| T | t | A7 |
| U | u | AE |
| V | v | 9E |
| W | w | 10 |
| X | x | 2F |
| Y | y | 01 |
| Z | z | 37 |
| ± | 1 | BF |
| @ | 2 | B6 |
| # | 3 | 3E |
| \$ | 4 | B9 |
| % | 5 | B5 |
| ¢ | 6 | 34 |
| & | 7 | 3D |
| * | 8 | BC |
| (| 9 | B0 |
|) | 0 | 31 |
| - | - | 80 |
| ° | ! | 97 |

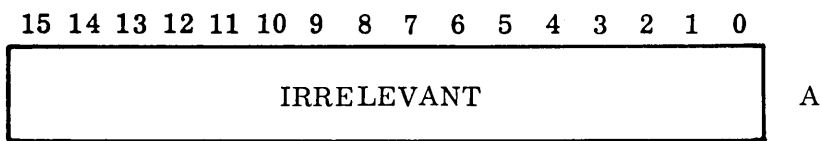
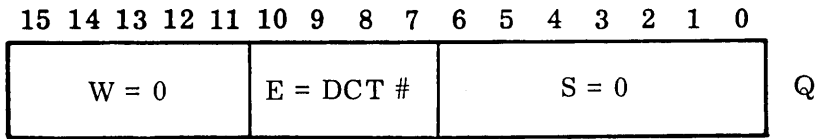
| UC | LC | CODE |
|-----------------|----|------|
| : | ; | 0D |
| " | ' | 15 |
| , | , | 8C |
| . | . | 16 |
| ? | / | 89 |
| | | |
| Space | | 40 |
| Upper Case | | 41 |
| Lower Case | | 42 |
| Carriage Return | | 43 |
| Tab | | 44 |
| Black Shift | | 45 |
| Red Shift | | 46 |



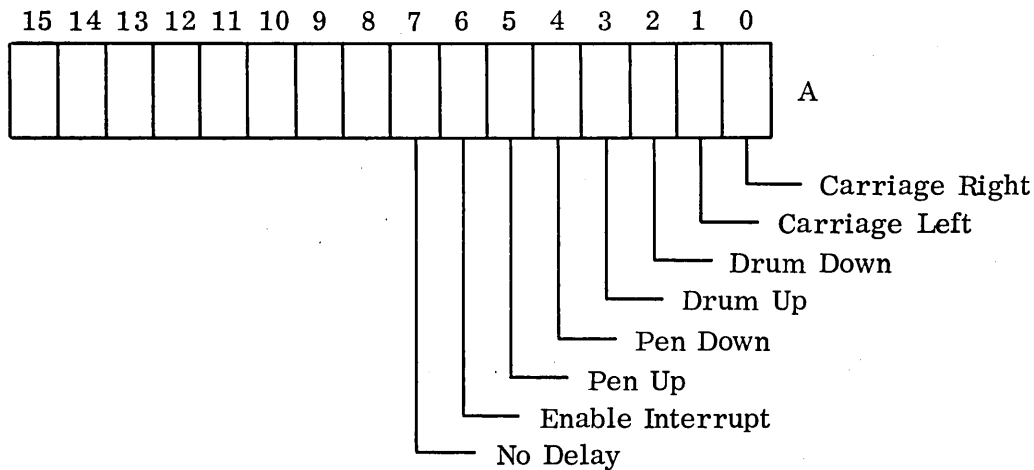
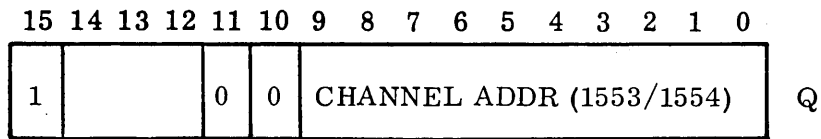
1585 INCREMENTAL PLOTTER CONTROLLER

TO OPERATE:

1. Connect DCT (1750) (INP)



2. Function Plotter (OUT)



1585 INCREMENTAL PLOTTER CONTROLLER (Continued)

PLOTTER MOVEMENT:

1. Carriage Right -Y
2. Carriage Left +Y
3. Drum Down +X
4. Drum Up -X

(0.01-inch movement/execution)

At completion of Plot OP, an interrupt (if enabled) is sent on the DCB.

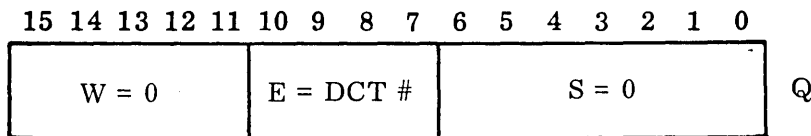
1587 MONITOR AND CONTROL PANELS

COMMUNICATION:

1. From 1587 to 1700, via Input Digital subsystem (1544/1545).
2. From 1700 to 1587, via External Register Output Interface (1553/1554).

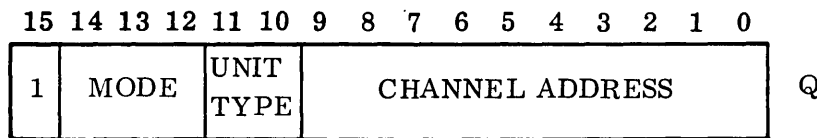
Have to connect DCT (activate) before communicating with 1587.

(INP)



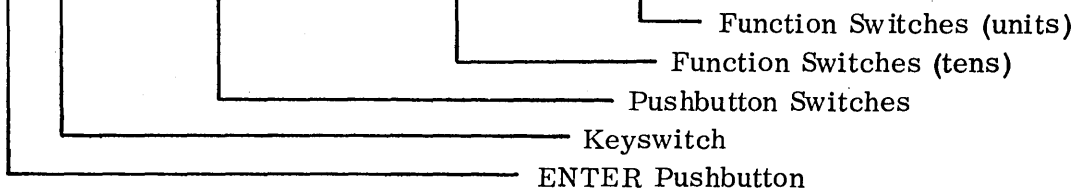
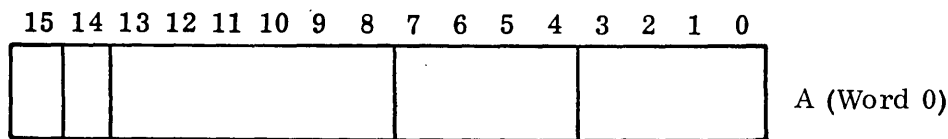
CONTINUE:

see fig 2 page 7 of 39005300 and page 2-3



1544/1545 or 1553/1554
(depending on input or output required)

1587A (INP) MASTER CONTROL PANEL



1587 MONITOR AND CONTROL PANELS (Continued)

1587A (INP)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

REX* NEEDED TO ILLUMINATE
ENTER/READY SWITCH

A (Word 1)

1587A (INP)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

REX* NEEDED TO ILLUMINATE REJECT
PUSHBUTTON

A (Word 2)

1587A (INP)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

REX* NEEDED TO ILLUMINATE
ILLEGAL ENTRY PUSHBUTTON

A (Word 3)

1587B DIGISWITCH PANEL

After connecting the DCT to the 1700, information from the 1587B enters the 1700 via a Digital Input Subsystem. The requirements of the 1544 are: four words (sequential), unsync, contact closure.

There are two groups of switches (identical) per 1587B; however, there are two special group configurations besides the standard group:

Standard Group

- 1 Sign Switch: + and - (+ = "0", - = "1") (BCD)
- 6 Decimal Switches: "0" → 9 (BDC)
- 1 Multiplier Switch: -6 → +3 ("0" → +3 = "0" → 3 (BCD), -6 → -1 = 4 → 9 (BCD))

*REX = Read Execute. Contents of "A" irrelevant unless 1587C and 1587E are hooked into the 1587A.

1587 MONITOR AND CONTROL PANELS (Continued)

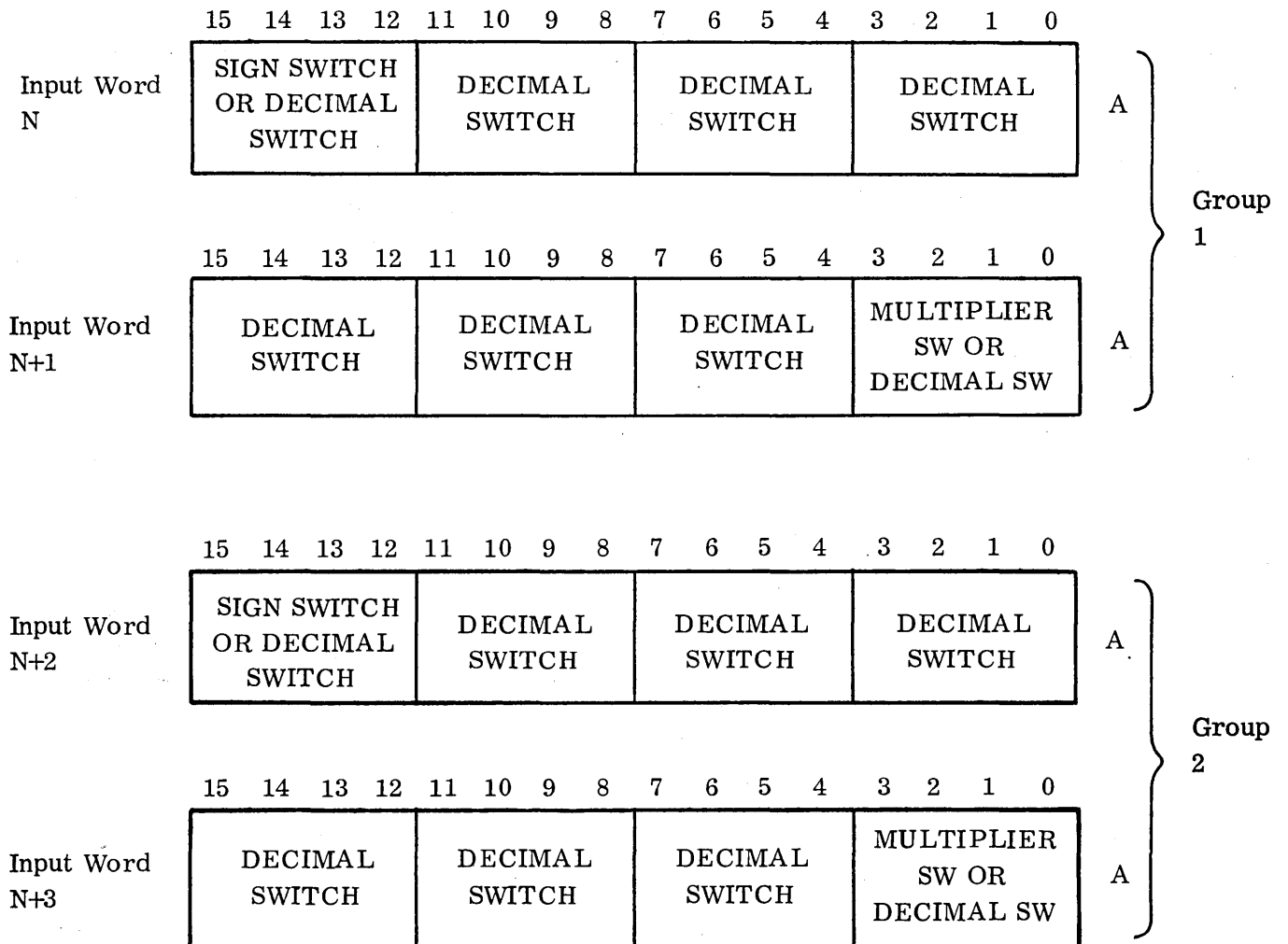
Special Group #1

- 1 Sign Switch: + and - (+ = "0," - = "1") (BCD)
- 7 Decimal Switches: "0" → 9 (BCD)

Special Group #2

- 8 Decimal Switches: "0" → 9 (BCD)

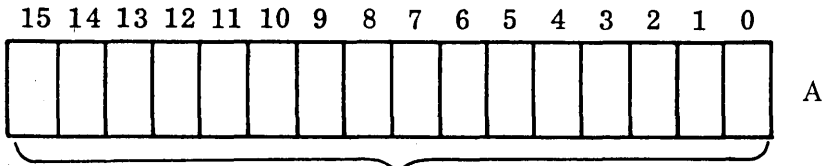
1587B READ (INP)



1587 MONITOR AND CONTROL PANELS (Continued)

1587C PUSHBUTTON PANEL (Enters 1700 via 1544 or can be connected to 1587A
1544 - Unsync, Contact Closure)

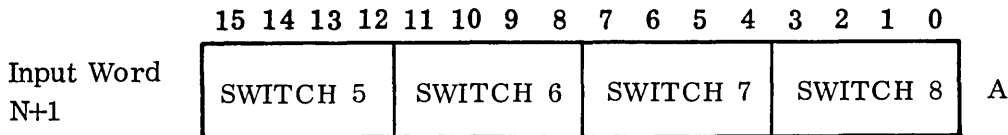
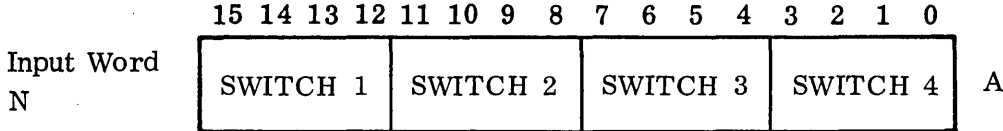
1587C READ (INP)



From 16 Pushbuttons (1587C)
"1" = On
"0" = Off

1587E ROTARY SWITCH PANEL (Enters 1700 via 1544 (Unsync) (Contact Closure) or it can
be connected directly to 1587A)

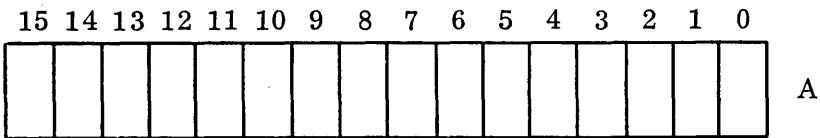
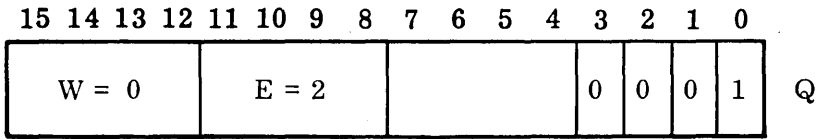
1587E READ (INP)



NOTE: The rotary switches on the 1587E are functionally equivalent to one group of the thumbwheel switches on the 1587B Digitswitch Panel and have an identical character set and data word format.

1751 DRUM CONTROLLER

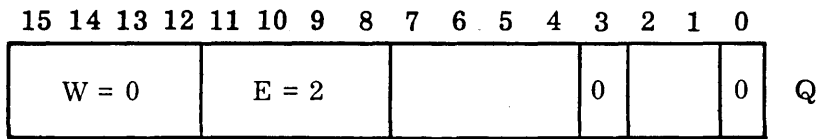
DIRECTOR FUNCTION (OUT)



Clear Interrupt

End of Operation Interrupt Requested

INITIATE OPERATION (OUT)



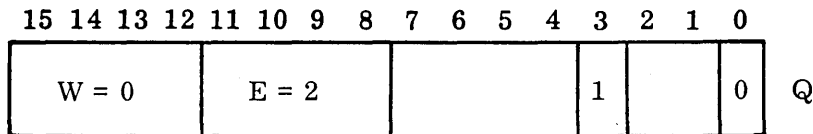
0 0 = Write Core → Drum

0 1 = Write Zeroes on Drum

1 0 = Read Drum → Core

1 1 = Check Read (for P. E., no transfer)

LOAD CONTROLLER ADDRESS REGISTERS (OUT)



0 0 = Track

0 1 = Initial Sector (Word)

1 0 = Initial Core

1 1 = Final Core

1751 DRUM CONTROLLER (Continued)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0



A

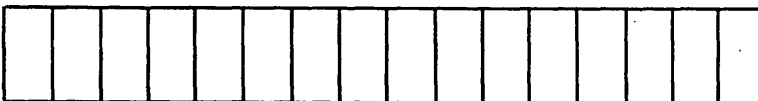
STATUS I (INP)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

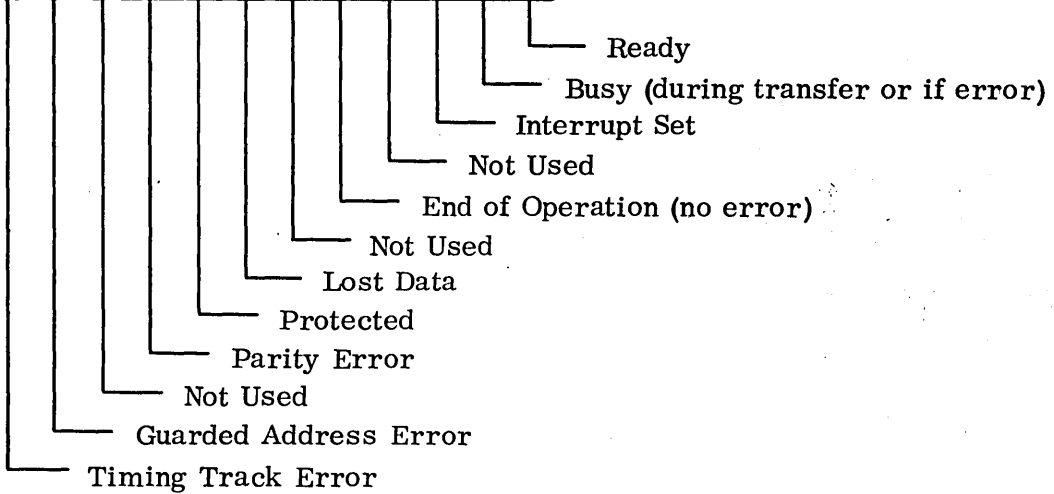


Q

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0



A



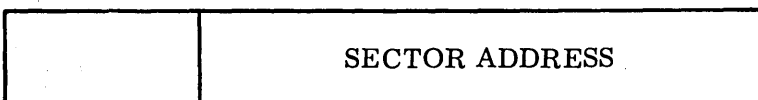
STATUS II (INP)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0



Q

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0



A

1797 BUFFERED I/O INTERFACE

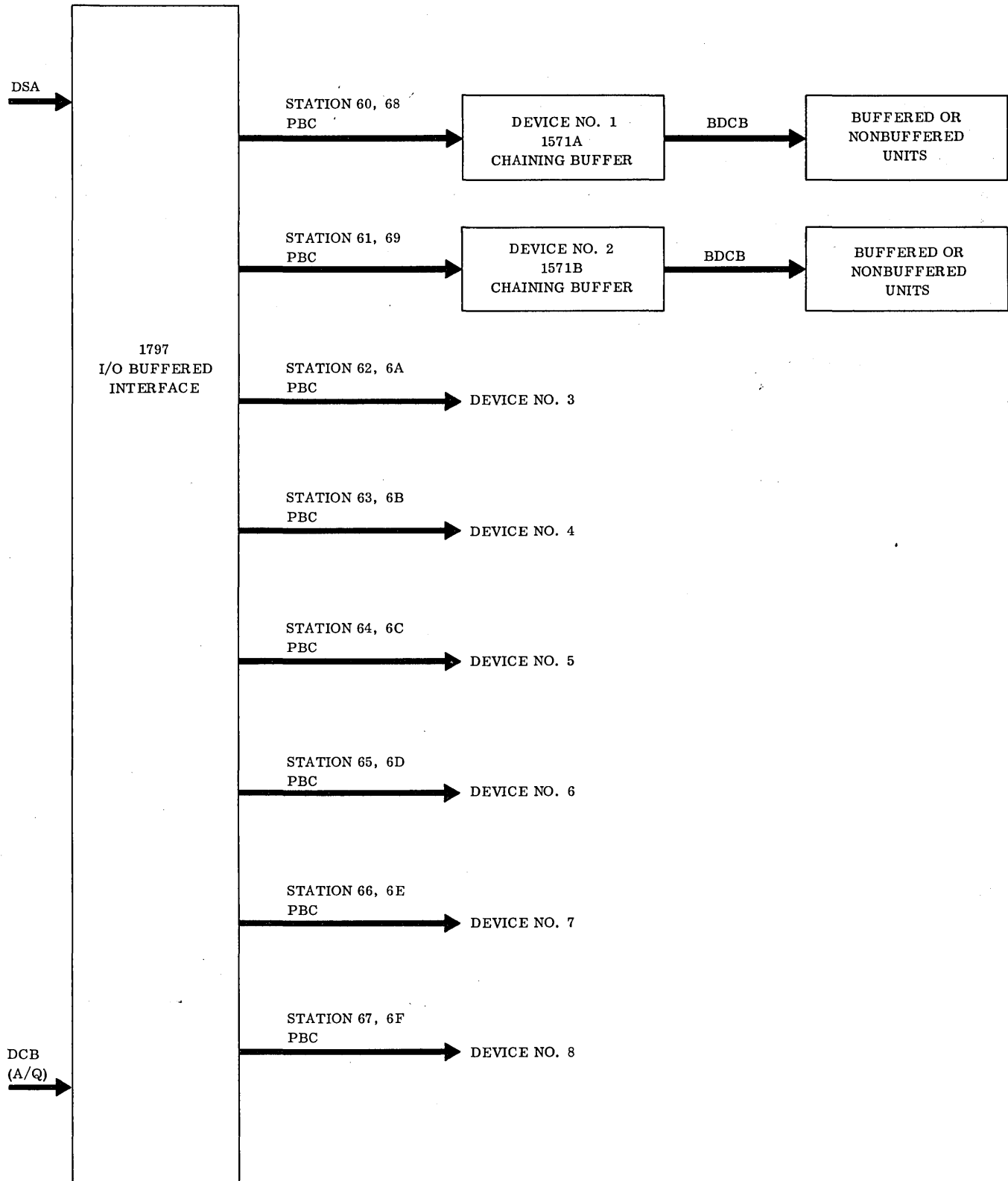
This interface requires no programming; however, the buffered devices connected to the priority buffer channel (PBC) are programmed through the 1750 DCT via the extended DCB. The devices can either work in a nonbuffered mode (on the DCB) or they can operate in a buffered mode (on the BDCB). Usually the 1571 Chaining Buffer is the device that is connected to the PBC (see diagram on next page). Up to eight devices can be connected to the 1797. Each device has its own PBC, and has two addressable stations.

NOTE: All devices on BDCB must be functioned before activating 1797/1571.

STATION (DEVICE) ADDRESSES ON PBC

| <u>Device NO.</u> | <u>Start (OUT)/ Status (INP)</u> | <u>Function (OUT)/ Next Memory Address (INP)</u> |
|-------------------|--------------------------------------|--|
| 1 | 60 | 68 |
| 2 | 61 | 69 |
| 3 | 62 | 6A |
| 4 | 63 | 6B |
| 5 | 64 | 6C |
| 6 | 65 | 6D |
| 7 | 66 | 6E |
| 8 | 67 | 6F |

Refer to 1571 Chaining Buffer Channel (page 10-5) for more details.



P-0136

COMMENT SHEET

CONTROL DATA 1700

**1500 SERIES EQUIPMENT CODES
FOR PROGRAMMERS**

FROM: NAME: _____

**BUSINESS
ADDRESS:** _____

THESE COMMENTS REFER TO REV. ____ OF THIS PROPOSAL.

COMMENTS: (DESCRIBE ERRORS, SUGGESTED ADDITIONS OR DELETIONS, ETC.;
INCLUDE PAGE NUMBER.)

CUT ALONG LINE

STAPLE

STAPLE

FOLD

CONTROL DATA CORPORATION
ANALOG-DIGITAL SYSTEMS DIVISION
4455 EASTGATE MALL
LA JOLLA, CALIFORNIA 92037

CUT ALONG LINE

ATTN: DOCUMENT CONTROL

FOLD

STAPLE

STAPLE