89637500

CONTROL DATA CORPORATION

CONTROL DATA®
CARD READER CONTROLLER
FE119-A

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA
WIRE LIST

HARDWARE MAINTENANCE MANUAL

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PREFACE

This manual supplies reference information for the CONTROL DATA® FE119-A Card Reader Controller. This equipment is used with the AB107/AB108 Computer to control the 1729 Card Reader. A knowledge of the computer and card reader is required before using this card reader controller.

The following CONTROL DATA® publications may be useful as references:

Publication	Pub. No.
1784 Computer Reference Manual	89633400
AB107/AB108 Computer Customer Engineering Manual	89633300
I/O Specification Manual	89673100
Installation Manual	88996000

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CONTENTS (continued)

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Continued

TABLES

SECTION 1
GENERAL DESCRIPTION

INTRODUCTION

This section contains the functional and operational description of the CONTROL DATA® FE119-A Card Reader Controller.

The card reader controller logic circuitry is mounted on a single 50-PAK printed wiring board. The controller interfaces with the A/Q channel of the AB107/AB108 Computer to control the operation of the card reader and transfer of the data. Interrupts are also generated within the controller. The card reader controller may be accommodated within the AB107/AB108 Computer or the BT148 Expansion Enclosure.

FUNCTIONS

The controller provides the following functions:

1. Provides four basic interrupt signals:
   a. Data Interrupt
   b. End-of-Operation Interrupt (EOP)
   c. Alarm Interrupt
   d. Common Interrupt
2. Interface signals
3. Timing for interrupt and interface signals
4. Address decoding
5. Reply and reject
6. Data reading and transfer
7. Program protection

FUNCTIONAL DESCRIPTION

System Relationships

The controller interfaces the Card Reader with the 1784 Computer AQ data channel. Its typical configuration is shown in Figure 1-1. Data is transferred from the Card Reader to the lower 12 bits of the Computer A Register (A00 through A11) containing the information for one

column of a card. Data bit A00 corresponds to card row 9.

The address of the Card Reader and controller is selected by inserting jumper plugs in positions Q7 through Q10, at location 56 on the CARD READER Printed Wiring Assembly. The jumper plugs are stored in location 15.

Any of 16 different equipment codes may be set up by these jumper plugs. Refer to Section 3, Installation and Checkout for details about jumper plug selections and codes.

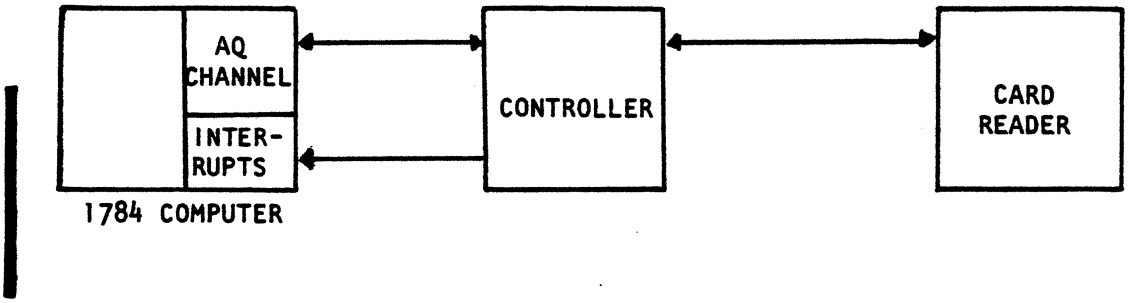


Figure 1-1. Typical Configuration

INTERFACE CABLES AND CONNECTORS

The cables required for operation of the controller and Card Reader are listed in Section 8, Parts Data.

The wire list for each cable used with the card reader controller, and the PWB pin list are given in Section 9.

The following page gives the table of specifications.

TABLE 1-1. SPECIFICATIONS

Specifications	Explanation
PHYSICAL CHARACTERISTICS	
Dimensions	
Width	$6\frac{13}{16}$ inches
Length	$12\frac{3}{8}$ inches
Depth	$\frac{3}{8}$ inches
Weight	(to be furnished)
ENVIRONMENT	
Temperature	
Shipping	-40°F to 158°F (-40°C to 70°C)
Storage	14°F to 122°F (10°C to 50°C)
Operating	40°F to 120°F (5°C to 50°C)
Humidity	
Shipping	0 to 100% RH non-condensing
Storage	10% to 90% RH non-condensing
Operating	10% to 90% RH non-condensing
POWER	
Input Requirements	5 Volts dc
Signal Level	
Low State (0)	0.4 Volts dc, or less
High State (1)	2.4 Volts dc, or more
Ground	Logic ground is connected to computer logic ground

SECTION 2

PROGRAMMING AND OPERATION

INTRODUCTION

This section describes the programming for the FE119 Card Reader Controller. Preparation for operation and operation are described in Section 3.

Table 2-1 and Figures 2-1 through 2-3 provide programming information. A description of the codes follows the figures.

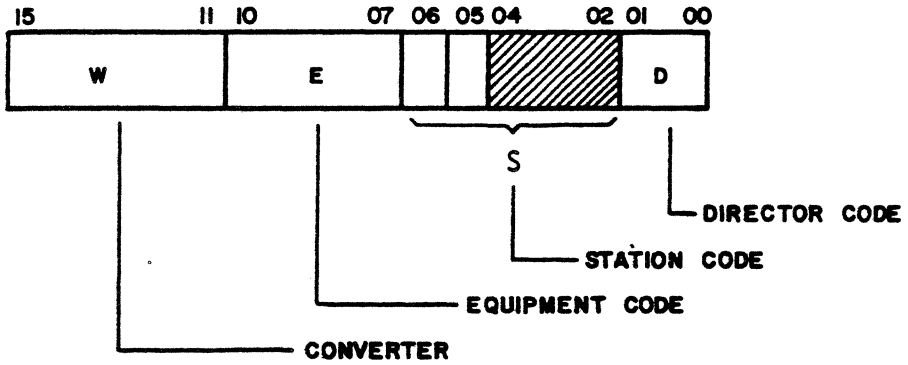


Figure 2-1. Q Register Format

TABLE 2-1. ADDRESSING CODES

DIRECTOR CODE	READ Signal	WRITE Signal
Q00 = 0, Q01 = 0	Read Data	Illegal
Q00 = 1, Q01 = 0	Illegal	Director Function
Q00 = 1, Q01 = 0	Director Status 1	Illegal
Q00 = 1, Q01 = 1	Director Status 2	Illegal

CODES

Converter — The W portion of the Q register (Q11 - Q15) must be all 0's for all Card Reader operations.

Equipment — The E portion of the Q register (Q07 - Q10) defines the Card Reader Equipment Code. The code is set up by the plugs shown in Figure 2-4. If the switch settings match bits 07 - 10 of Q, the equipment responds.

Station — The S-part of the Q register (Q05, Q06) must have the following settings for Director Functions and for Data transfer: Q05 = 1, Q06 = 0.

Command — When accompanied by an Equipment Code and either a Read or Write signal, a command code defines the operation to be performed. The D portion of Q (Q00 and Q01) defines the operation to be performed by the Controller.

DATA TRANSFER

Read Data (Q00 = 0, Q01 = 0, Q05 = 1, Q06 = 0)

When bits Q00, Q01 and Q06 are 0, and Q05 = 1, and they are accompanied by the Equipment Code and a Read signal, the Controller is directed to perform a data transfer. A reject occurs if there is no data to be transferred. The Card Reader rejects when

a. The Card Reader is not ready
b. The computer attempts to input data at a rate that exceeds the capabilities of the Card Reader, that is, Data Status is not set.
c. Protect Violation occurred.

DIRECTOR FUNCTIONS (Q00 = 1, Q01 = 0, Q05 = 1, Q06 = 0)

When Q00 and Q05 are 1's and Q01 and Q06 are 0's and they are accompanied by an Equipment Code and a Write signal, the controller is directed to perform the following operations. Director functions may be stacked (i.e. two or more functions sent simultaneously), but when a function is sent which should be rejected, the Controller rejects the Director Function.

NOTE

The Card Reader executes and replies to the Clear function if it is Not Ready, provided that no other director bit (except A01) is transmitted with it (bits A02 through A08 must be zero). Care should be taken in using this function while the Card Reader is busy, as this condition results in the operation being aborted.

Clear Controller (A00 = 1)

This function directs the clearing of all interrupt requests and responses, motion requests, errors, and other logic which may be cleared. This bit is subordinate to bits A02 through A07 of the Director Function.

NOTE

The Card Reader will execute and reply to the Clear Interrupts function if it is Not Ready, provided that no other director bit (except A00) is transmitted with it (bits A02 through A08 must be zero).

Clear Interrupts (A01 = 1)

This function directs that all interrupt requests and their responses be cleared; it is subordinate to the interrupt request bits A02 through A04.

Data Interrupt Request (A02 = 1)

This function sets the Data Interrupt Request flag which causes an interrupt to be generated when information is available. The interrupt is cleared by a reply to data transfer. The interrupt request and response is cleared by bit A00 and A01. Interrupt Request takes precedence over function clears.

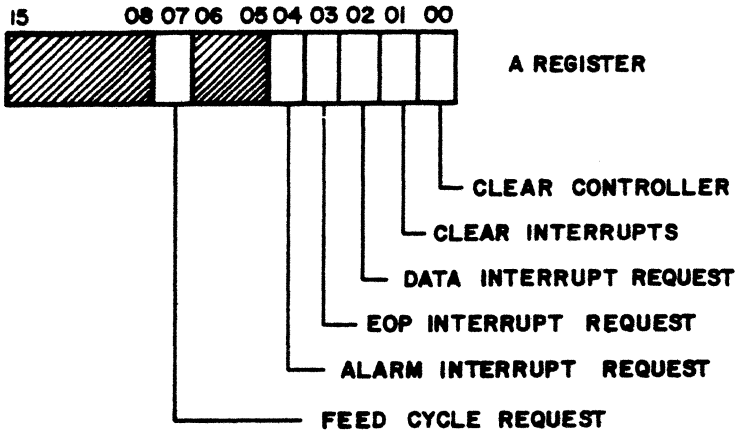


Figure 2-2. Director Function Code Format

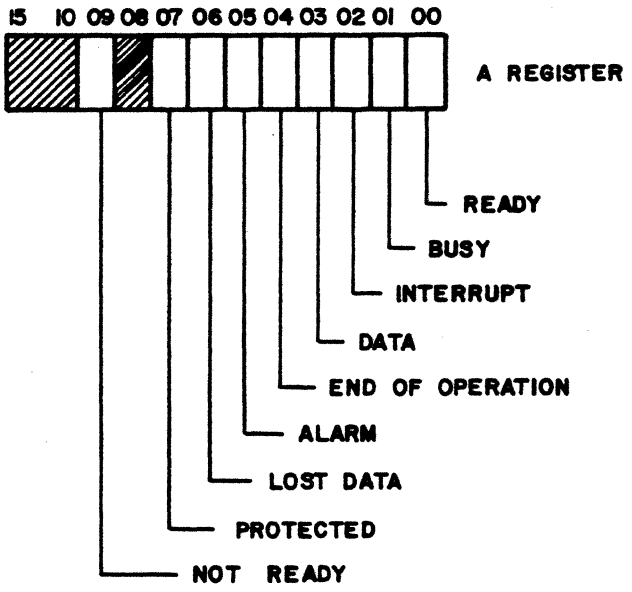


Figure 2-3. Director Status Code Format - Level 1

End of Operation Interrupt Request (A03 = 1)

This function sets the EOP Interrupt Request flag. The purpose of this interrupt is to notify the computer that the unit is finished with an operation. The interrupt Request and Response is cleared by bit A00 or A01. Interrupt Request takes precedence over function clears.

The interrupt may be selected before or during the operation. An interrupt response does not occur for an operation which terminated before the selection was made.

Alarm Interrupt Request (A04 = 1)

This function sets the Alarm interrupt request flag and so enables the generation of an interrupt when an Alarm condition exists. These conditions are listed in the Alarm section. An Alarm condition that exists at the time of the interrupt request immediately provides a response; if the Alarm condition does not exist at the time of the interrupt request the interrupt response is provided as soon as the Alarm condition is detected.

The Alarm Interrupt Request function is cleared by a Master Clear or when A00 = 1, or A01 = 1 with A04 = 0.

The interrupt response is cleared by a Master Clear or when A00 = 1 or A01 = 1. When the interrupt response is cleared by Director Function A00 = 1, or A01 = 1, the interrupt request may be reset with the same operation if A04 = 1.

Director functions A05 and A06 are not used.

Feed Request (A07 = 1)

This function directs the Card Reader to initiate a feed cycle.

If a new Feed Request is issued before EOP occurred, data transfer in that card is truncated and will continue on the next card being fed. No EOP interrupt is generated. This function takes precedence over the clear controller function.

Director Function A08 is not used; it is accepted by the Controller.

Director Function A09 through A15 are not used, and are ignored by the Controller.

DIRECTOR STATUS (Q00 = 1, Q01 = 0) LEVEL I

When Q00 is a 1 and Q01 is a 0, and a Read signal is present, the computer is requesting Level 1 status. The Controller will always reply to this operation.

Ready (A00 = 1)

This bit indicates that the Ready signal is active on the Card Reader.

Busy (A01 = 1)

This bit indicates that the Card Reader is busy. The Card Reader becomes busy when a feed cycle is initiated and remains busy until an End of Operation occurs.

Interrupt (A02 = 1)

This bit indicates that an interrupt response was generated by the controller. The other status bits must be monitored to determine the cause of the interrupt. The controller may generate interrupts on four different lines due to three different conditions which may occur at the controller and their logical "OR" function.

a. Data Interrupt

   Data Interrupt will be generated when both the Data Interrupt Request flag and the Data Status are active.

b. EOP Interrupt

   EOP Interrupt will be generated when both the EOP Interrupt Request flag and the EOP status are active.

c. Alarm Interrupt

   Alarm Interrupt will be generated when both the Alarm Interrupt Request flag and the Alarm status are active.

d. Common Interrupt

   Common Interrupt will be generated when any or any combination of the Data Interrupt, the EOP Interrupt or the Alarm Interrupt are generated.

Data (A03 = 1)

This bit indicates that a data transfer may occur, that is data is available in the controller ready for transfer to the computer. The status and interrupt drops when data has been transferred to the computer.

End of Operation (EOP) (A04 = 1)

This bit indicates that the Card Reader has completed reading a card.

Alarm (A05 = 1)

This bit indicates the presence of an alarm. Two kinds of alarm condition can occur:

a. The Card Reader Ready signal becomes not active. Ready status becomes false.

b. When Lost Data occurs, no further transfers occur from that card. The Ready status is unchanged.

Lost Data (A06 = 1)

This bit indicates that data was not transferred out of the Controller to the computer, before the next column of a card being read appeared. No further data transfer will occur until Clear Controller is issued.

Protected (A07 = 1)

This bit indicates that the Controller is in the Protect state, that is, the Protect jumper plug is out. The Controller then accepts only those instructions which have their protect bit set. All other instructions are rejected. A protected instruction can be used with either a protected or an unprotected Card Reader. For setting the protect bit see Operation.

Director status is not rejected if Protected Violation occurred.

Director status bit A08 is not used and is always zero.

Not Ready (A09 = 1)

This bit indicates that sometime during a card cycle there was a failure in the transport of the card. It is always the inverse of Ready (bit 00).

Director status bits A10 through A15 are not used and are always 0.

DIRECTOR STATUS (Q00 = 1, Q01 = 1), LEVEL 2

The Controller will always accept Director Status, level 2, but will load the A-register with the constant 0000_{16}.

OPERATION

Prepare the Controller for operation as described in Section 3.

SECTION 3

INSTALLATION AND CHECKOUT

INSTALLATION

Unpacking

1. Carefully remove wrapping from the 50-PAK controller card. Check for physical damage to card and record damage on the packing list. Check that part number agrees with parts list.

2. Remove wrapping from cable and check for physical damage. Record damage on packing list. Check that part number agrees with packing list.

Physical Limitations

Care must be taken to prevent damage to the controller card. The card must not be flexed or dropped.

Power Requirements

The controller card requires +5vdc derived from the power supply of the computer.

Cabling and Connectors

An external interconnecting cable is available for use with the controller for connection between the computer and the card reader. The external shielded cable (part no. 89818600) is 10 feet long.

The internal cable (part no. 89641800) used between the back of the computer and the connector pins on the back plane, is 15.5 inches long.

The interrupt cable (part no. 89724702) is 13.8 inches in length.

The wire lists for pin assignments will be found in Section 9.

Cooling Requirements

The controller card is cooled by the forced air system of the computer. No further cooling is required. Refer to the computer customer engineering manual (89633300) for further information concerning cooling capabilities of the computer.

Environmental Considerations

The environmental considerations necessary for operation (or storage) of the controller are listed in the specifications (Table 1-1).

Preparation and Installation

Before installing the controller card perform the following:

1. Remove the air-flow block from lower slide of card slot to be used.
2. Inspect the enclosure, card slot, PW board slides and connector pins, for physical damage.
3. Place the Equipment Code jumper plugs and Protect jumper plug in the proper positions on the PWB. Refer to Tables 3-1 and 3-2 and Figure 3-1. Note that the Controller is protected when the Protect jumper plug is absent.

CAUTION

Do not install or remove controller card or cables from computer or expansion enclosure with power on.

4. Carefully install the controller card in the assigned A/Q slot. The PWA must slide in smoothly. The slot must be selected according to equipment configuration. Refer to Figure 3-2 and to Computer CE manual (89633300) for card placement.

5. Place the Interrupt Cable in the position on the back-plane as indicated in Table 3-3.

6. Install the Internal Cable between connector P2 of the position the controller PWA is placed in and the applicable output connector position of the CPU or Expansion Enclosure connector panel.

7. Install the External Cable between the Internal Cable output connector and the card reader.

CHECKOUT

1. Refer to Section 2 of this manual and the Computer Reference Manual for operation of the controller.

2. Determine that proper voltages are supplied to the controller card by measuring +5vdc between test points 1 (ground) and 63 on the PWA.

3. Perform diagnostics check as-described in the Systems Maintenance Monitor (SMM17) Manual, Publication Number 60182000.

TABLE 3-1. JUMPER PLUG SELECTION AT PWB LOCATION 56

SELECTION	JUMPER PLUG	PINS	BIT	REMARKS
Protect	S5	5 and 6	PRT	Protected when jumper plug is out
Equipment Code	S2	2 and 9	Q07	Selected when jumper plug is in.
	S1	1 and 10	Q08	Selected when jumper plug is in.
	S3	3 and 8	Q09	Selected when jumper plug is in.
	S4	4 and 7	Q10	Selected when jumper plug is in.

TABLE 3-2. HEXADECIMAL CODES FOR EQUIPMENT SELECTION

HEXADECIMAL CODE	BINARY BITS (JUMPER PLUGS)			
	Q10 (S4)	Q09 (S3)	Q08 (S1)	Q07 (S2)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

Note: A '1' in the binary code indicates the presence of a jumper plug for the setting of the equipment code; a '0' indicates its absence.

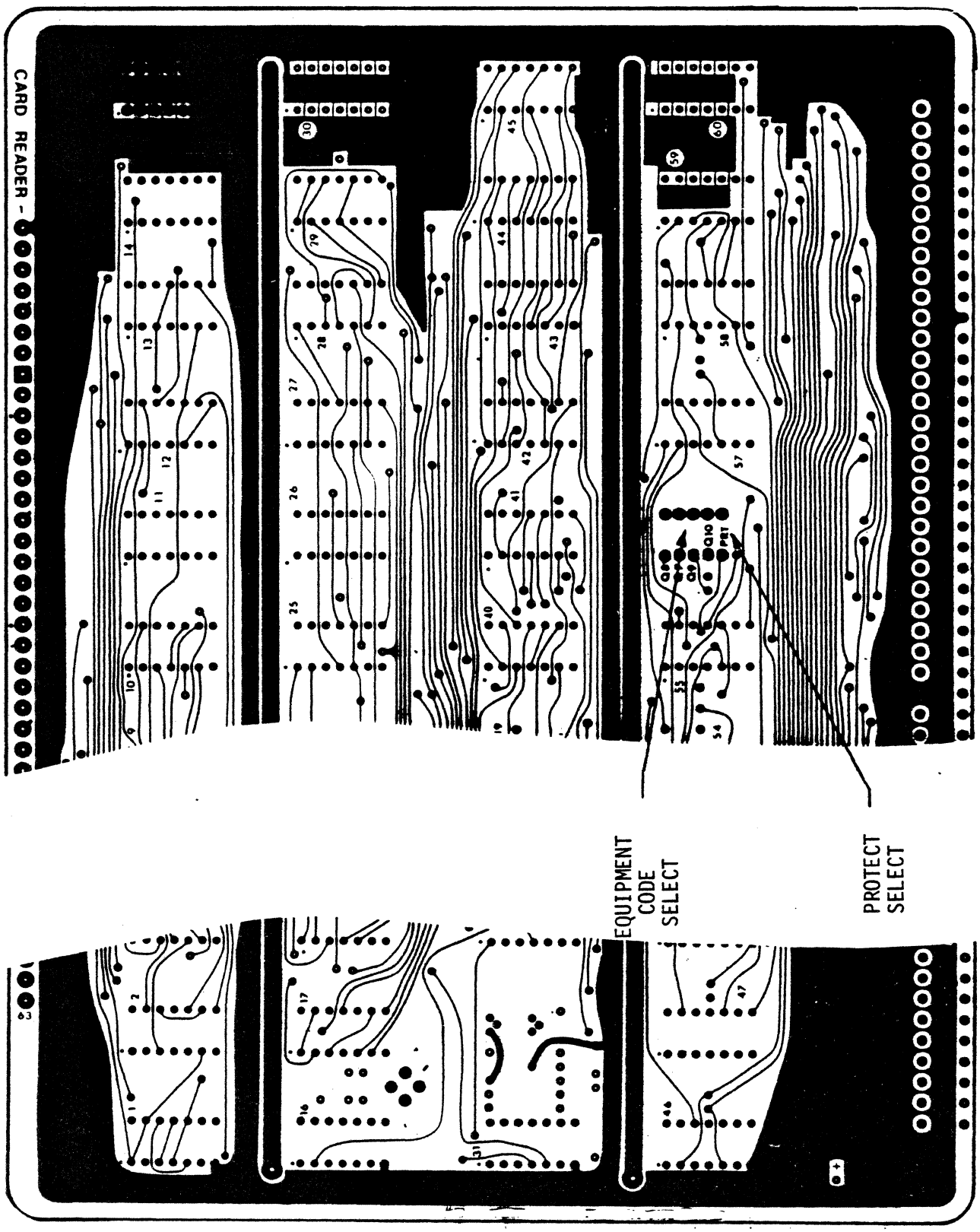


Figure 3-1. Jumper Plug Location on PWB

TABLE 3-3. INTERRUPT PIN ASSIGNMENTS

Card Reader Controller

EØP Interrupt	P1B25
Common Interrupt	P1B27
Data Interrupt	P1B24
Alarm Interrupt	P1B26

Connections may be made to any of the following:

CPU	(Position)	
Line 1	25	P1B10
" 2	25	P1A7
" 3	25	P187
" 4	25	P1A5
" 5	25	P1A6
" 6	25	P1B6
" 7	25	P1B5
" 8	26	P1A10
" 9	26	P1B10
" 10	26	P1A7
" 11	26	P1B7
" 12	26	P1A5
" 13	26	P1A6
" 14	26	P1B6
" 15	26	P1B5

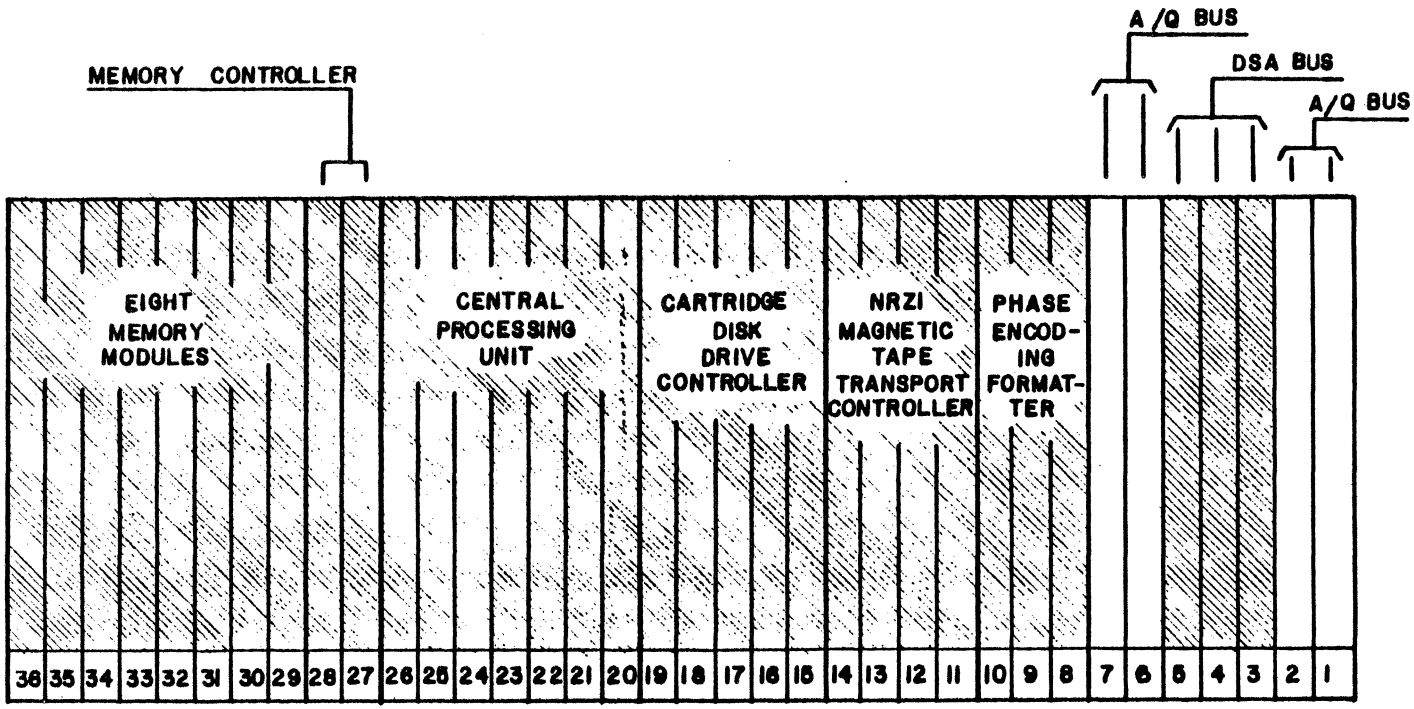


Figure 3-2. Location for Installation of Controller PW Assembly (A/Q Bus)

SECTION 4
THEORY OF OPERATION

INTRODUCTION

This section presents a wgeneral description of the equipment, using an overall block diagram and timing diagrams. Descriptions are keyed to the detailed logic diagrams in the Diagram Section (Section 5) and afford a basis in understanding the detailed description of the specific circuit in that section.

NOTE

It is assumed that the reader is familiar with the programming characteristics of the Computer as described in the 1784 Computer System Reference Manual, Publication Number 89633400.

GENERAL

The controller interfaces the computer through the A/Q channel.
In Read Data operation, the data previously read into the controller's data buffer is transferred through the 12 least significant bits of the A register to the computer, bit 0 corresponding to card row 9.
Card motion is initialized by the FEED signal from the controller. Once the motion is started, it will continue until all 80 columns of the card have been read. While the card is moving, the columns are read and the data transmitted to the controller together with a STROBE signal. Upon receiving the STROBE signal, the controller gates the data into the data register and sets the DATA FF. This FF is reset by the Read Data operation. If the STROBE signal arrives when the previous data has not yet been read, the LOST DATA FF is set, preventing the new data from being strobed into the data register.

A/Q Receivers/Transmitters

The receivers of the A/Q channel are TTL inverters or gates. Each receiver dissipates one TTL load from the channel. The transmitters are open collector type 7438 TTL buffers.

Protection Logic

The Protect circuit disables the controller from operating for I/O instructions issued from an unprotected core. When the Protect jumper is out and A/Q Protect bit Q00 is set at time of Read or Write, the POK (Protect OK) signal is generated. If the A/Q Protect bit is not active at that time, a POK cannot be generated. The POK signal is always generated when the Protect jumper is in position, that is, the controller is in the unprotected state.

Equipment and Operation Decoder

When the bits Q07-Q10 match the Equipment Number of the Controller, bits Q11-Q15 are all zeros (W=0 is active) and READ or WRITE signals are present, flip-flop U24-5,6 sets on the leading edge of clock pulse T1. Its output signal enables the operation decoder which selects the operations to be executed, according to the following table.

TABLE 4-1. Q REGISTER READ/WRITE

Q00	Q01	READ	WRITE
0	0	READ DATA (RDTA)	Illegal
1	0	DIRECTOR STATUS 1 (DS1)	FUNCTION (FCN)
0	1	Illegal	Illegal
1	1	DIRECTOR STATUS 2 (DS2)	Illegal

After the selection is made, a check is performed to determine whether the operation can be executed. If it can, the REPLY signal is generated to the computer; otherwise the REJECT signal is generated. The illegal operation is always rejected. Director Status 1 and Director Status 2 are always executed. Director Status 1 transfers the current status bits of the controller to the computer. Director Status 2 always transfers zeros to the computer.

Data Transfer

Data transfer from the card reader is performed by the Read Data operation, which requires that the following equation hold true:

$$DATA \cdot POK \cdot Q05 \cdot \overline{Q06} = 1$$

That is, the conditions for REPLY are:

1. The DATA FF is set (the STROBE signal has been received).
2. No Protect Violation has occurred.
3. Q05 = '1' and Q06 = '0'. Q05 and Q06 are the Station Code.

When the controller executes the Read Data operation it does the following:

1. Resets the DATA Flip-Flop.
2. Enables the data to the A channel.
3. Generates a REPLY to the computer.

In case the STROBE signal appears when the DATA FF is still set, the LOST DATA FF is set. A Lost Data disables the Strobe from entering data into the Data Register, and sets the ALARM status. When a Lost Data occurs, no further data transfer can take place from that card. To reset the LOST DATA FF, either CLEAR CONTROLLER (CRLC) or the FEED functions have to be issued.

Director Function

The DIRECTOR FUNCTION operation is performed provided the following equation holds:

$$POK.Q05.\overline{Q06}\ (READY + \overline{A02}\cdot\overline{A03}\cdot\overline{A04}\cdot\overline{A07}) = 1$$

The DIRECTOR FUNCTION is further decoded according to the contents of the A register as follows:

A00 = 1	CLEAR CONTROLLER (CLRC)
A01 = 1	CLEAR INTERRUPT (CLRI)
A02 = 1	REQUEST INTERRUPT on DATA (DTARQST)
A03 = 1	REQUEST INTERRUPT on EØP (EOPRQST)
A04 = 1	REQUEST INTERRUPT on ALARM (ALRMRQST)
A05, A06	Not used
A07 = 1	FEED command ($\overline{FEED}$)
A08 - A15	Not used

The Reply conditions can be divided as follows:

a. If the controller is Not Ready, the REPLY will be generated only for CLRC, CLRI or Request Interrupt functions.

b. If the controller is Ready, a REPLY will be generated for all functions.

The FEED command starts card motion in the card reader. While a card is moving, a STROBE signal is received at the controller each time the data is read from a column. On the leading edge of the pulse, a check for Lost Data is performed. When the whole card has been read, the card reader generates the End Data pulse to the controller. This pulse clears the Feed FF and sets the EOP FF.

When the Continuous Feed mode of operation is used, i.e. the Feed command will be issued before the end of the current card, the Lock FF is set disabling further strobe until the next card is being fed and normal operation continues. In this way less than 80 columns can be read from each card. EOP will be generated only for the last card read.

Interrupt Logic

The controller generates Interrupt signals to the CPU on any one or any combination of the following conditions, provided an Interrupt has been requested:

1. DATA FF is set.
2. EØP occurred.
3. Alarm occurred.

Interrupt generation is selected by the software by means of A02-A04 with FCN.

When the bit in A is set, the proper Request FF will be set on trailing edge of the Write pulse, enabling the interrupt transmitting gate. CLRI function clears all Request FF's, therefore disabling interrupts from being transmitted.

The CLRI and Request functions can be issued in the same FCN operation. In this case the Request function will take precedence over the CLRI.

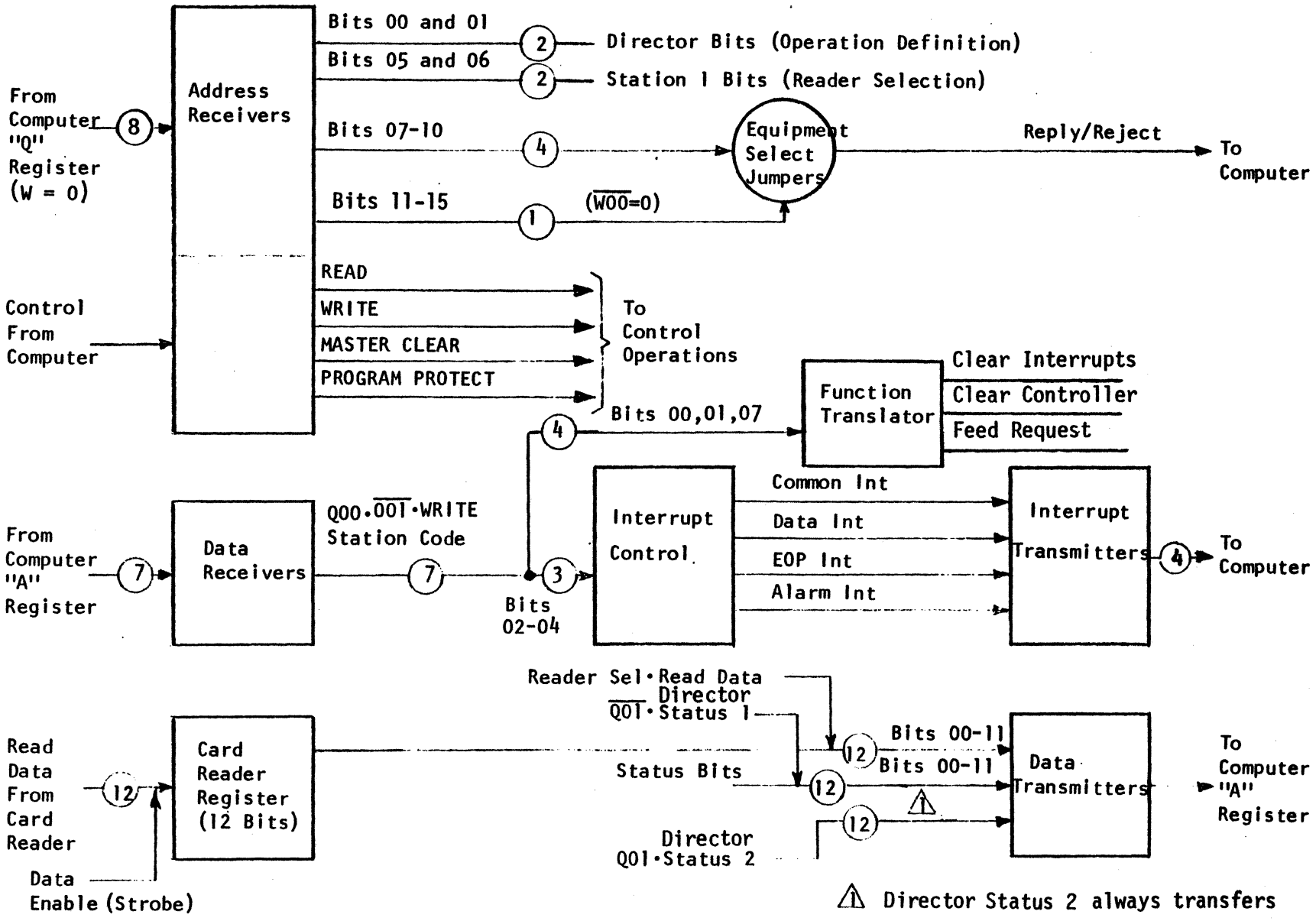


Figure 4-1. Card Reader Controller Block Diagram

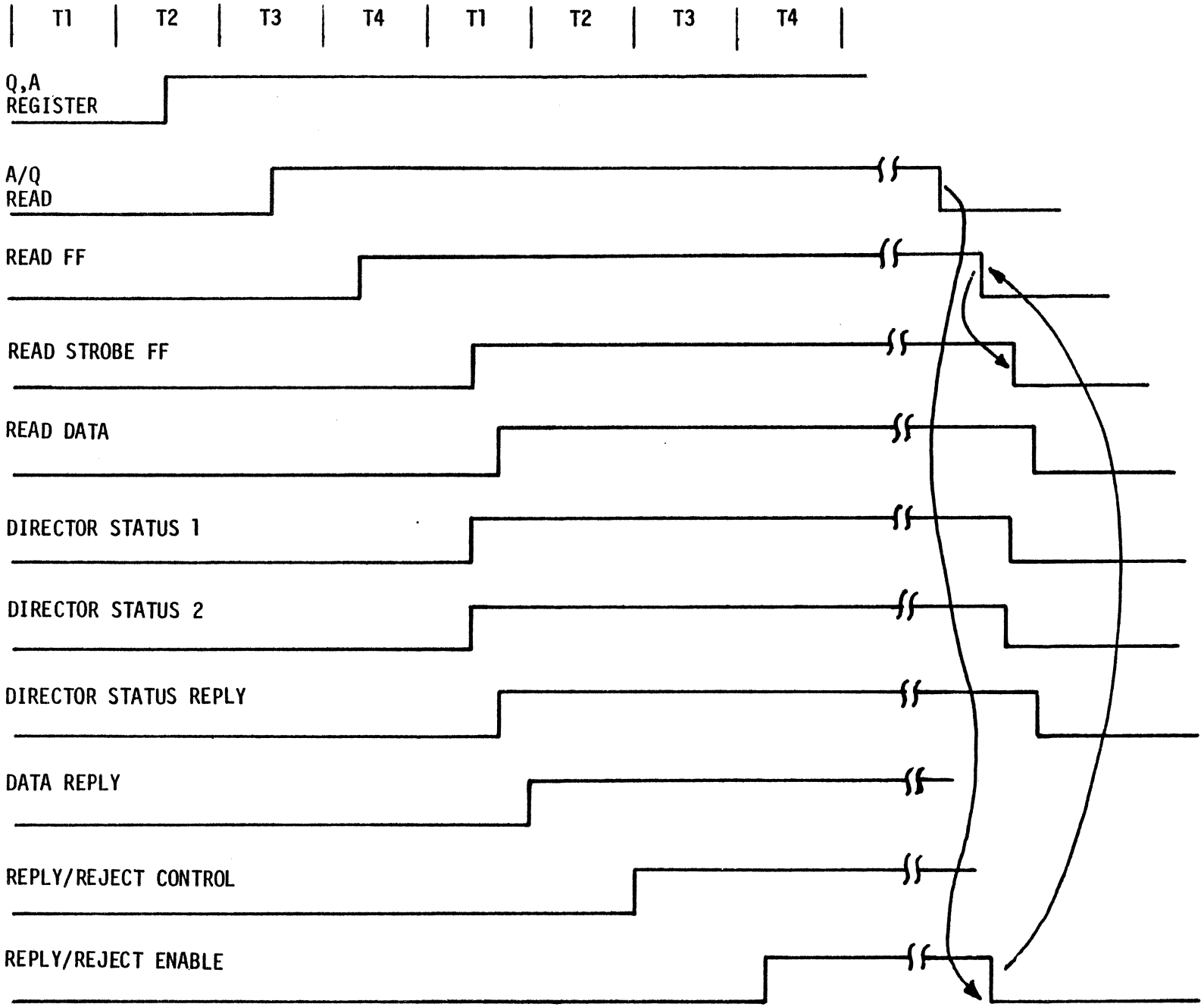


Figure 4-2. A/Q Read/Reply Timing Diagram

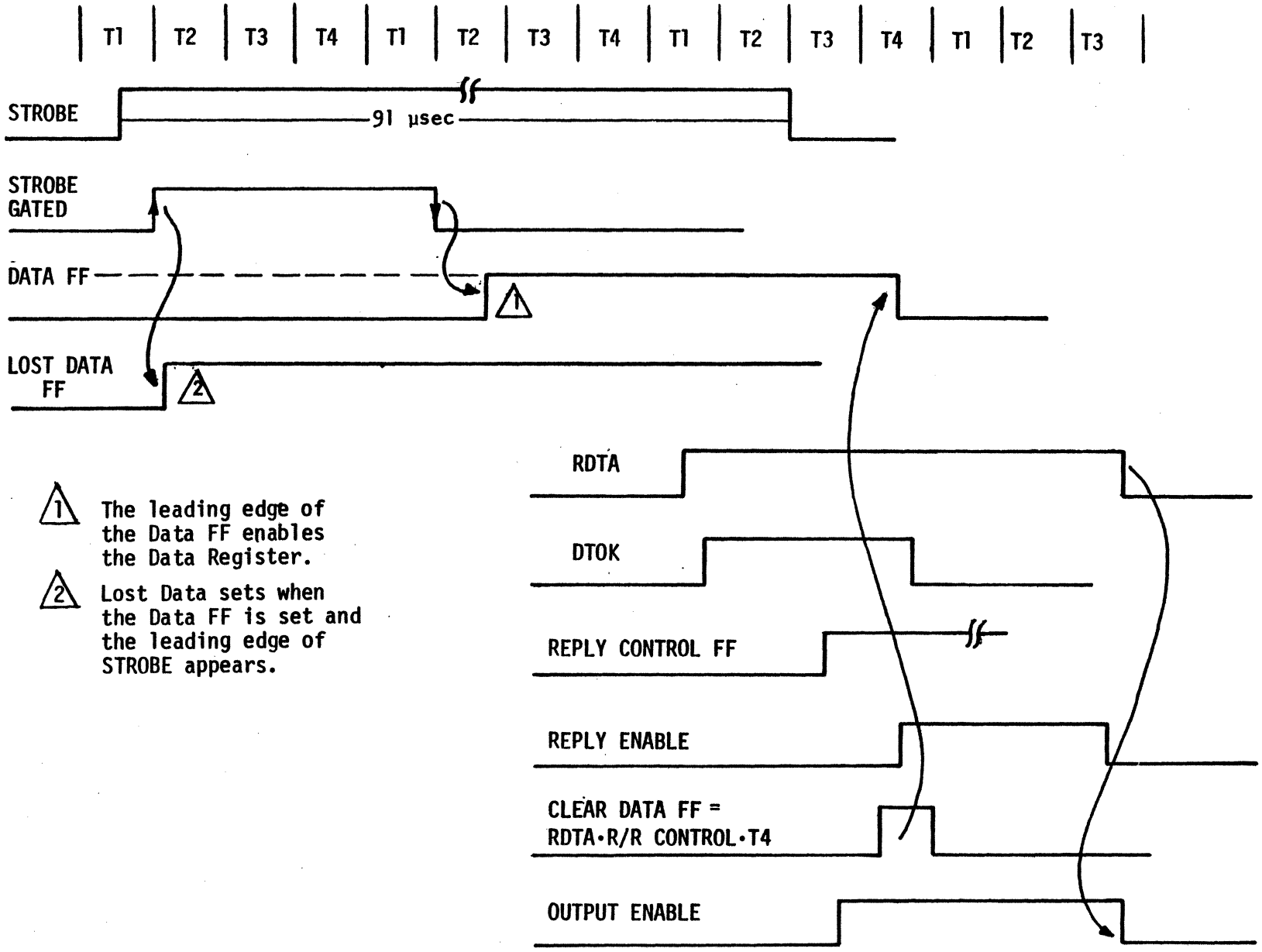


Figure 4-3. Data Transfer Timing Diagram

SECTION 5
LOGIC DIAGRAMS

KEY TO LOGIC SYMBOLS

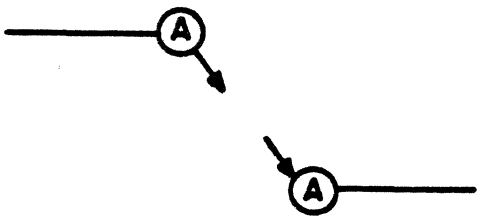
Publication 89723700 (Key to Logic Symbols) or equivalent, lists the symbols used in the logic diagrams in this manual and gives a short description of the functions they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention.

The following paragraphs describe the signal flow conventions used.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down.

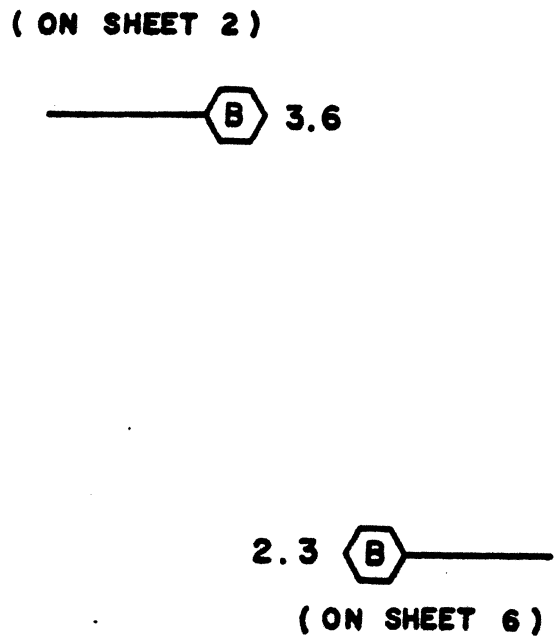
The signal lines are sometimes interrupted to allow logical grouping of components. At each such interruption one of the following indicators is used:



On-Sheet Continuation Reference Symbols

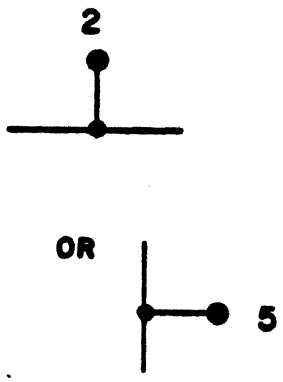
These symbols when used with the logic symbols in the following diagrams indicate that a connection exists between two points on a sheet. The arrows attached to each circle point from signal origin to signal destination. The letters, C, H, I, O and P are not used inside the circles, since they bear special significance on logic diagrams.

Off-Sheet Continuation Reference Symbols



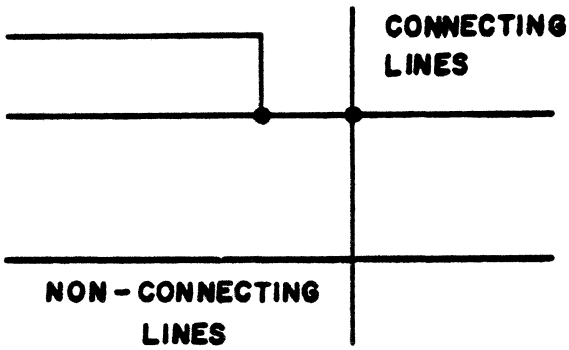
These symbols when used with the logic symbols in the following diagrams indicate that a common signal point exists between two sheets in a series of related drawings. These symbols point from output to direction of input as shown in the illustration. The letters C, H, I, O and P are not used in the hexagons, since they bear special significance on logic diagrams. The number(s) next to each hexagon indicate the sheet(s) that the signal is continued from or on. For instance, the numbers 3.6 refer to sheets 3 and 6, while 2.3 refers to sheets 2 and 3. It should be noted that the referenced sheet number(s) is always placed opposite the line extending from the hexagon.

Test Points



The test point symbol on the logic diagram shows the connection of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point one is labeled on the edge of the PWB.

Connecting and Non-Connecting Lines

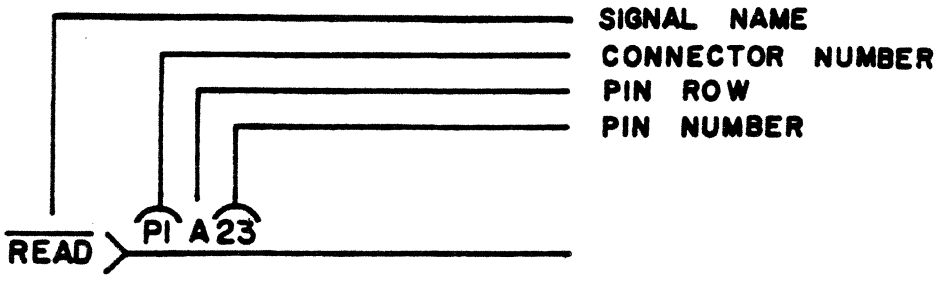


Lines connected to a common point or at a junction point are shown in the upper part of this illustration. No more than four lines are connected to a common point in the diagrams.

Lines crossing but not connected are shown in the lower part of this illustration.

Connectors

Connectors are represented on the logic diagram by the symbol for a female connector, for both input and output signals. The name of the signal is placed in the open end of the connector symbol (shown below), using the full name of the signal or the common abbreviation applicable to logic diagrams. The connector number, pin row and pin number are located above the line extending from the connector symbol.



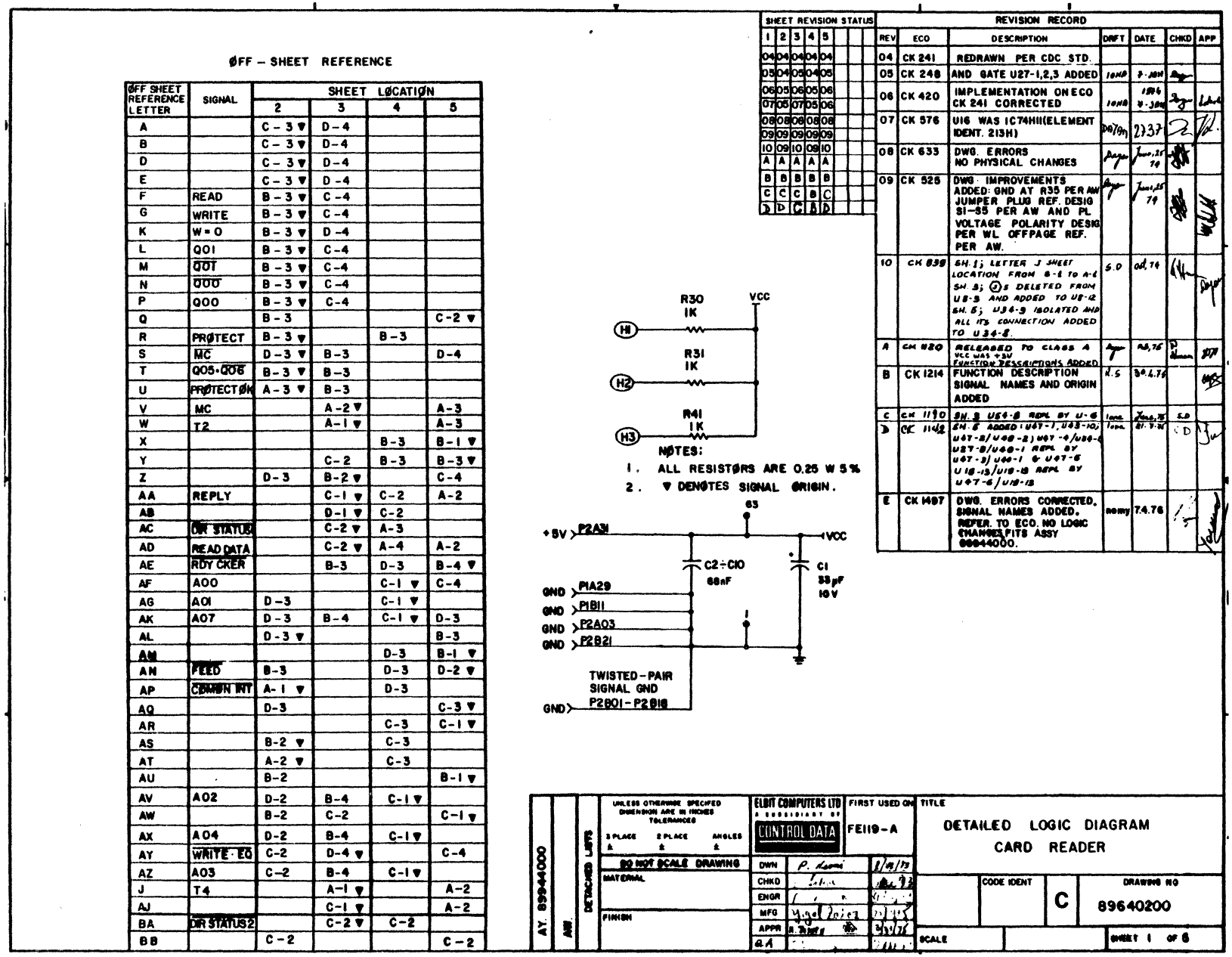


Figure 5-1. CARD READER PWA Detailed Logic Diagram : Cover Sheet

Figure 5-1. CARD READER PWA Detailed Logic Diagram : Cover Sheet

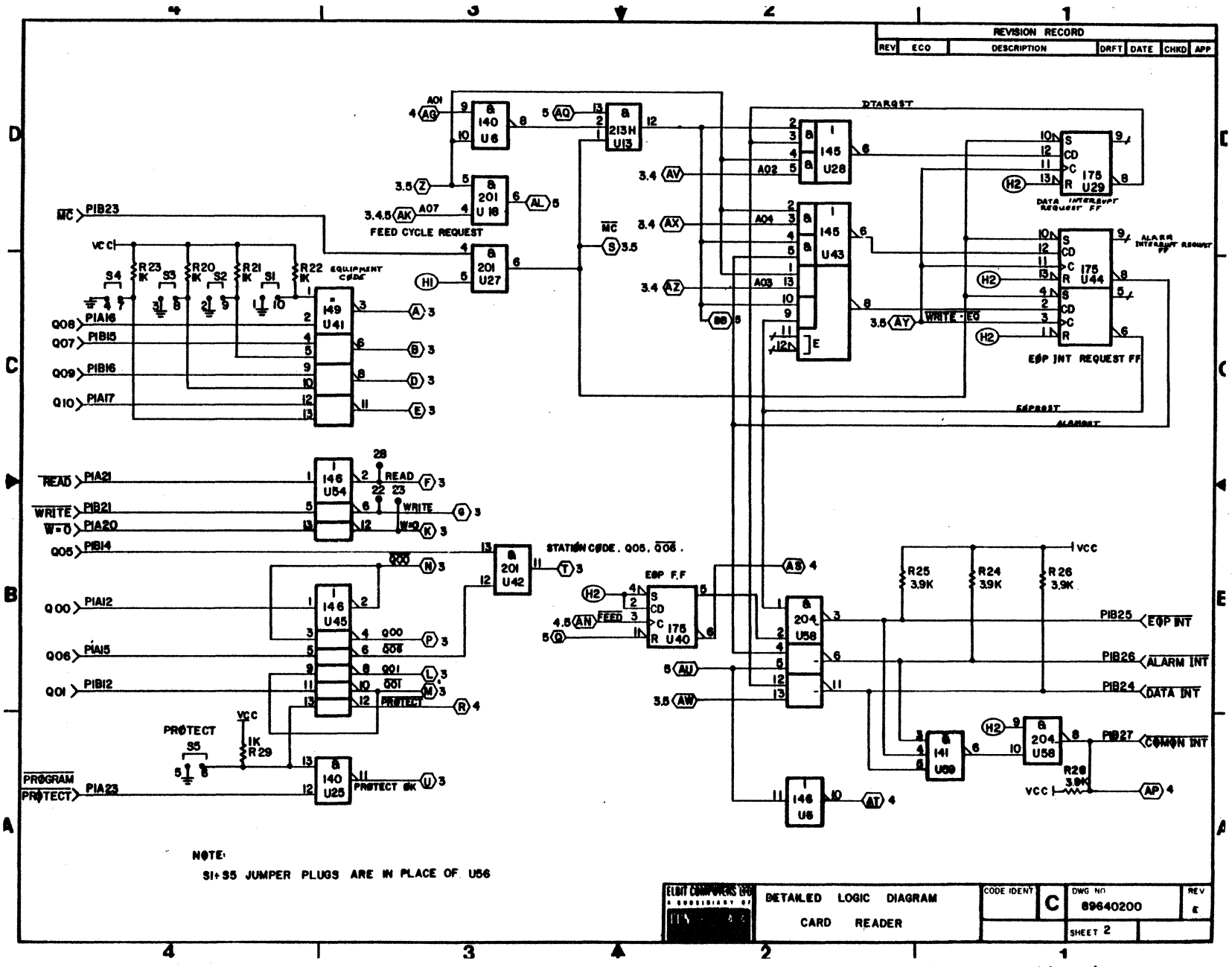


Figure 5-2: CARD READER PWA Detailed Logic Dgm: Interrupt Logic, Q Receivers and Protect Circuitry

INTERRUPT LOGIC, Q-RECEIVING EQUIPMENT & PROTECT CIRCUITRY (Figure 5-2)

Q-Receiver

The function of this circuit is to receive the signals of the Q-Register. The signals are received by TTL 7404 inverters (U45) or 7486 Exclusive OR (XOR) gate U41.

Equipment and Protect Setup Jumpers

Bits 07-10 of the Q-register are received by U41 the 7486 XOR gate. The bits are compared to the setting of the associated Equipment jumper plug. Whenever a match exists the output is a Low (logical "0"). The outputs of the four XOR gates are fed into the Equipment Decoder U26 (on Sheet 3). When protect jumper is not inserted and a High appears at U25-12 the Controller is in the Protected state.

Interrupt Logic

The function of this circuit is to generate the proper Interrupt responses for the computer.

Four Interrupts may be generated: Data U, Alarm, EOP and the Common Interrupt which is a logical OR of the other three through U59-3, 4, 5 → 6 and U58-10 → 8.

An interrupt is generated when the proper Q-Register, Read-Reply/Reject, Write, Error-Check, Ready Protect and A-Register Input/Output condition exists and an Interrupt has been requested.

Three interrupt request FF's exist: Data Interrupt Request FF U29-8 (DTARQST), Alarm Interrupt Request FF U44-8 (ALRMQST) and EOP Request FF U44-6 (EOPRQST). These FF's are reset by $\overline{MC}$ from the computer.

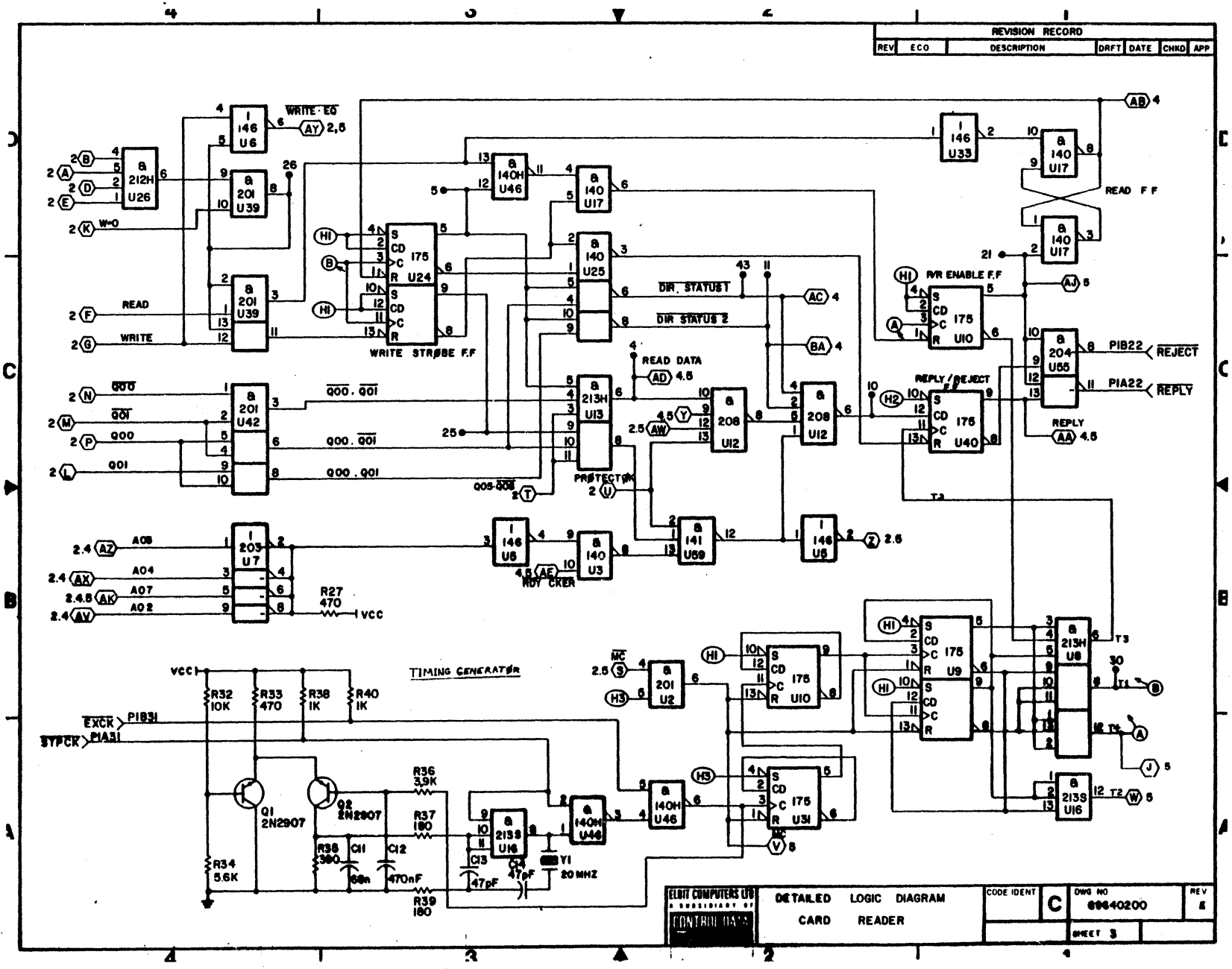


Figure 5-3. CARD READER PWA Detailed Logic Diagram: Timing Generator and Data Control

TIMING GENERATOR AND DATA CONTROL (Figure 5-3)

Timing Generator

The Timing Generator produces 20 MHz from a Johnson type oscillator through U16 and U46. STPCK (P1A31) and EXCK (P1B31) are not used, and U16-9 and U46-2 & 5 are held high, normally. Four clock pulses (T1, T2, T3 and T4) at an 800 nsec rate, 100 nsec in duration, are produced. T1 is provided at U8-8, T2 at U16-12, T3 at U8-6 and T4 at U8-12. T3 and T4 produce the timing pulse for the Reply/Reject output through U10-5 and U40-8 & 9. T2 provides timing for the Strobe FF (U1, Sheet 5). T1 provides timing for the Write Strobe FF (U24).

Data Control

The Equipment Code receiver (U41, Sheet 2) produces a NOTed output which is ANDed at U26-6 and together with the W=0 input produces the required high (through U39-8) to gate-in the Read/Write instruction (U39-2→3 for Read and U39-13→11 for Write). The Read/Write receivers (U54-1→2 and U54-5→6 are on sheet 2 of the Logic Diagram.

The Write signal is strobed through U24, ANDed with T3 through U25-1& 2→3 and U17-4 & 5→6 to the Reset of U40-13 and U10-5, respectively, to produce the $\overline{\text{Reply}}/\overline{\text{Reject}}$ output to the CPU. Reply is also supplied to U17-12 (Sheet 5) along with the Read Strobe (to U17-13) produced through the Read FF U17-8 (Sheet 5), to gate data from the card reader to the CPU.

A02, A03, A04 and A07 from the Q-Receivers (Sheet 2) are NORed together through U47 and inverted through U5-3→4, combined with the Ready CKError signal through U3-9&10→8, and with the Protect and Write signals in U59-1,2 & 13→12 to gate the Interrupt Transmitters (U58, Sheet 2). It is also used to gate the Reply signal through U55.

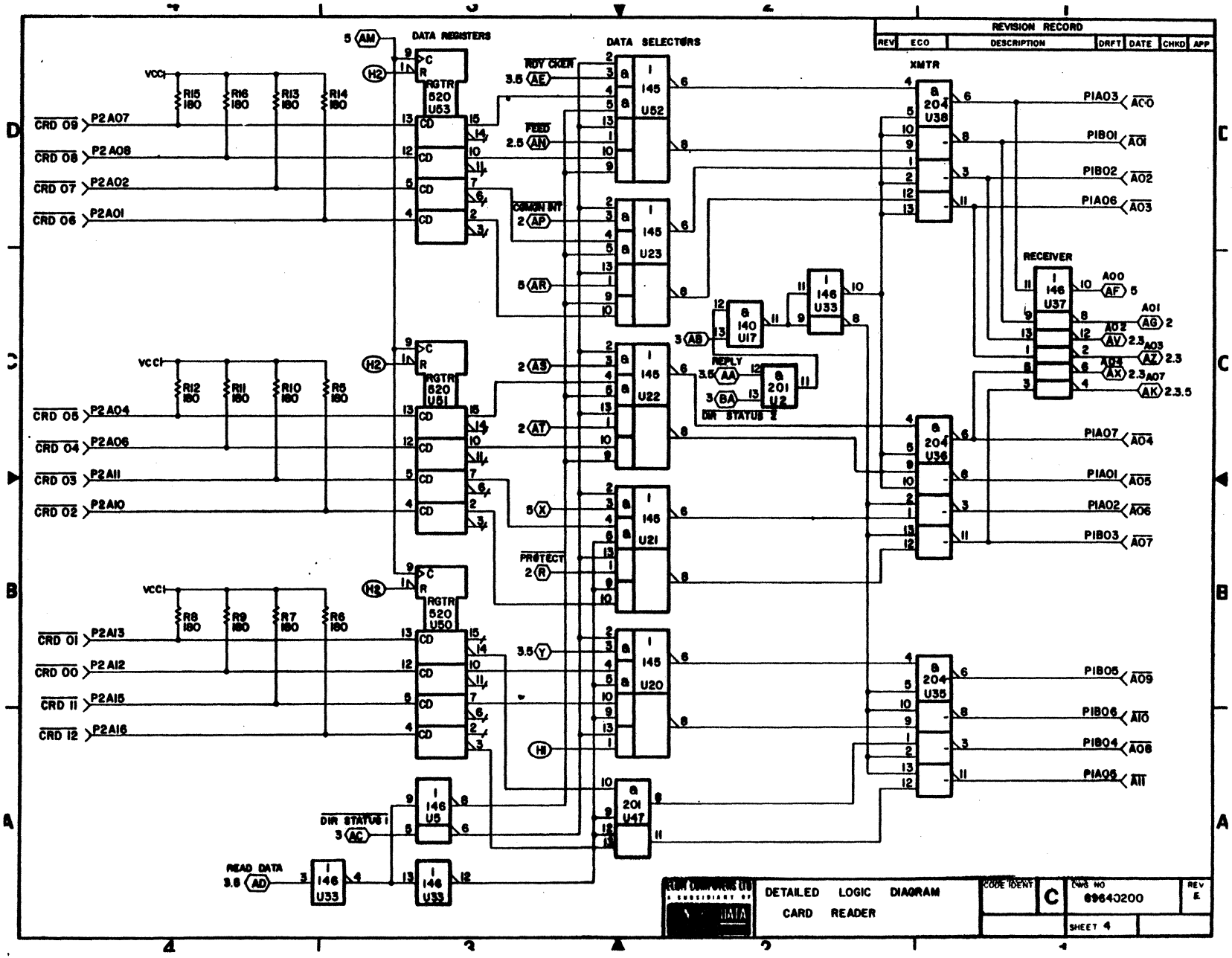


Figure 5-4. CARD READER PWA Detailed Logic Diagram: Data Transfer Logic

DATA TRANSFER LOGIC (Figure 5-4)

The Data Transfer logic enables data exchange between the computer and the card reader. The circuit consists of data registers (U50, U51, U53) data selectors (U20, U21, U22, U23, U52) and A-channel transmitters/receivers (U35, U36, U37, U38). Data from the card reader is transmitted in bits A00 through A11 of the A-channel. Bit A00 corresponds to row nine of the punched card.

Data Register

This 12 bit register stores data from the card columns present on the data lines when the Strobe pulse appears from the card reader. This data is transferred to the computer when Read Data operations are detected. The data is then transferred to the computer by A-channel bits 0 through 11.

Data Selection

The Data Selection logic selects the data to be transferred to the computer according to the operation being executed. When data is executed U18-8 (on Sheet 5) goes active enabling the data from the Data register. When Director Status 1 is executed, signal $\overline{\text{DIR STATUS 1}}$ goes true enabling the Status bits to the A-channel, through U17-12 & 13→11 and U33-9 & 11→8 & 10 to the A-Register Transmitters. When DS2 operation is executed, the output is not enabled and zeros are transferred to the computer through the A-Register Transmitters U35, U36 & U38.

A-Register Transmitters/Receivers

The circuit performs the data exchange between the computer and the controller. Data from the computer is received by a 7404 inverter gate. Data to computer is transmitted by a 7438 open collector buffer, U37.

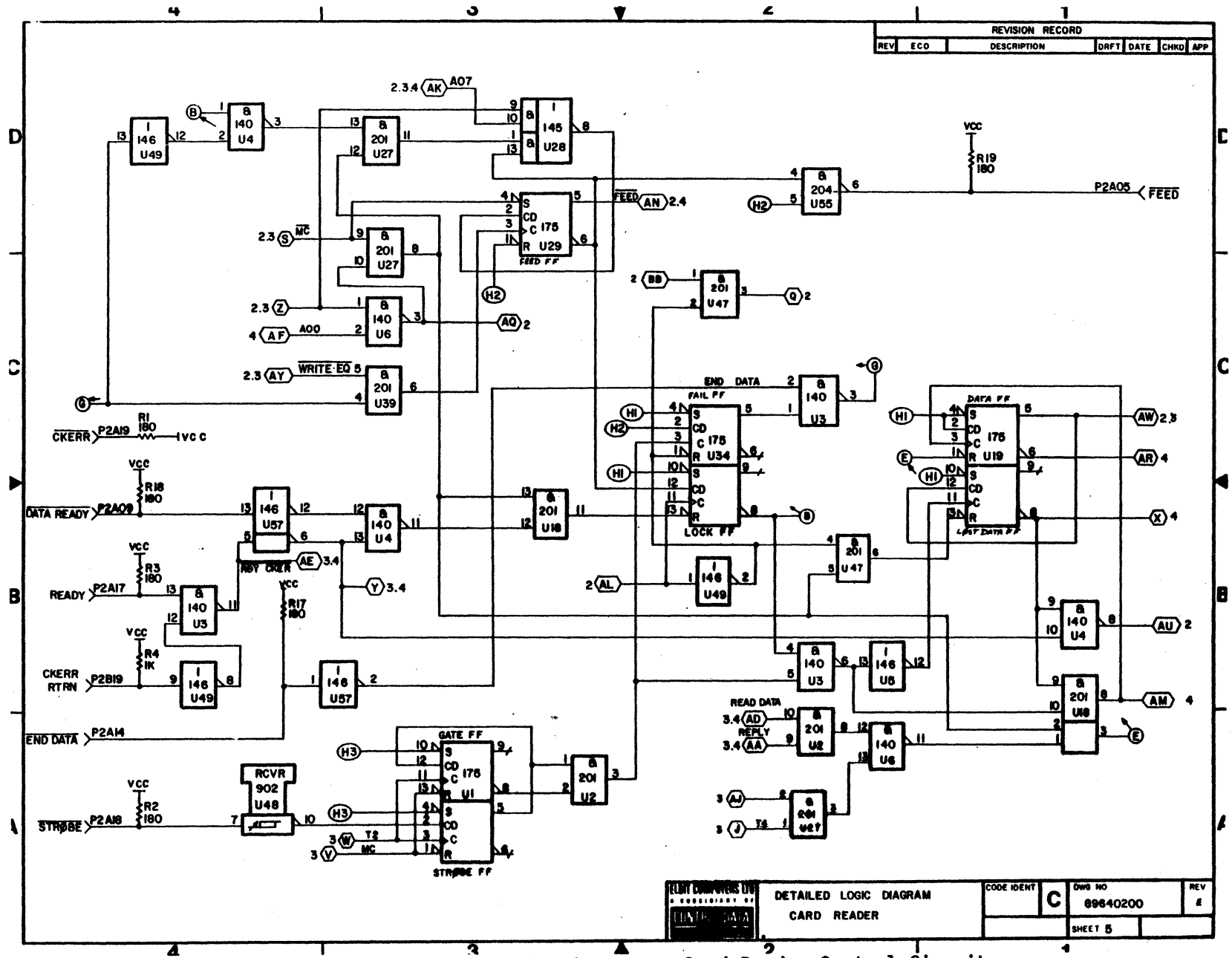


Figure 5-5. CARD READER PWA Detailed Logic Diagram: Card Reader Control Circuit

CARD READER CONTROL CIRCUIT (Figure 5-5)

When the Feed command (as a result of A07, End Data, Strobe, MC, T1, $\overline{\text{WRITE}}$ $\overline{\text{DATA READY}}$, Ready and $\overline{\text{CKERR}}$ signals) is accepted by the controller, the Feed FF (U29-6) sets and the $\overline{\text{FEED}}$ signal is sent to the card reader through U55. The signal initializes the motion of the card into the Read head of the card reader.

When the Read head of the card reader detects a column it generates the Strobe signal. A signal of 800 nsec is generated by gate U2-3. The trailing edge of the signal sets the Data FF (U19-5), and strobes the data into the Data Register(U50,U51,U53 on Sheet 4). On the leading edge of STRGTED, the Data FF (U19 upper half)is checked, if it is set the Lost Data (LSD) FF (U19 lower half) is set, inhibiting further data transfer and setting the Alarm conditions.

The operation goes on until all 80 columns are read. After this time, the card reader generates the End Data signal which resets the Feed FF (U29). When the FF resets the EØP FF (U34-9) is set signifying that the operation is terminated.

The function of the Fail FF (U34-5) is to detect and store when the Strobe pulse is not received, after a Feed has been issued (Card Jam). When this condition is present U34-5 inhibits the generation of the EØP signal. The Lock FF (U34-5) is used when the continuous Read mode is used. When the intention is to read only a part of the card, the Feed Request can be generated before the EØP. When this happens the U34-9 sets inhibiting further strobes and EØP until the next card enters the read station. At that time it resets and reading proceeds from that card. See timing diagram (Read Data) Figure 4-2.

Then the FF's are set when the corresponding bits in the A-Register at the time of Director Function are set. When the FF is set it enables the Interrupt Transmitter (U58 on Sheet 2) to transmit the Interrupt when this condition exists.

The FF's can be cleared by the CLRI (Clear Interrupts) operation. Clearing the FF's terminates the response to the computer.

SECTION 6
MAINTENANCE

SCOPE

This section supplies maintenance references and procedures for the equipment listed in Section 1 of this manual.

TOOLS AND SPECIAL EQUIPMENT

The following is a list of maintenance tools recommended for maintenance of this equipment:

Part Number	Part Description	Quantity
89688700	Board Extender	1
89670300	Board Extractor	1
	Oscilloscope Tektronix 453 or Equivalent	1
	Voltmeter	1

The publications listed below are applicable to the equipment:

Publication	Pub. No.
1784 Computer Customer Engineering Manual	89633300
1784 Reference Manual	89633400
1700 Computer System Codes Manual	60163500
System Maintenance Monitor (SMM 17)	60182000

MAINTENANCE

Preventive maintenance of the controller is not required. After it is determined that the controller has failed, remove and replace the PW assembly with an identical problem-free assembly. For removal and replacement of the assembly, refer to Section 3 of this manual. After replacement, a diagnostic check should be run as described in SMM 17.

CAUTION

Do not remove or replace cables or PW Assembly with power on.

SECTION 7

MAINTENANCE AIDS

(NOT APPLICABLE)

PARTS DATA

The following parts list is applicable to the FE119-A Card Reader Controller:

NOMENCLATURE	PART NUMBER
CARD READER Printed Wiring Assembly	89944000
Interrupt Cable Assembly	89724702
Internal Cable Assembly	89641800
External Shielded Cable Assembly	89818600

SECTION 9

WIRE LISTS

WIRE LISTS

The following wire lists are applicable to the FE119-A Card Reader Controller. Wire size, color, origin, destination and name of the signal normally found on that wire are included in Table 9-1 for the external cable and in Table 9-2 for the internal cable.

A pin list for the Card Reader Controller printed wiring board is also included in this section in Table 9-3.

Note: The symbol NC means Not Connected.

TABLE 9-1. WIRE LIST - EXTERNAL CABLE

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
1	WHT	1	X	$\overline{\text{CRD06}}$
2	BLK	2	b	GND
3	WHT	3	V	$\overline{\text{CRD07}}$
4	ORN	4	Z	GND
5	WHT-RED	5		GND
6		6		N.C.
7	WHT	7	U	$\overline{\text{CRD05}}$
8	RED	8	Y	GND
9	WHT	9	C	$\overline{\text{FEED}}$
10	YEL	10	H	GND
11	WHT	11	W	$\overline{\text{CRD04}}$
12	BRN	12	a	GND
13	WHT	13	c	$\overline{\text{CRD09}}$
14	BLU	14	h	GND
15	WHT	15	e	$\overline{\text{CRD08}}$
16	VIO	16	k	GND
17	WHT	17	A	$\overline{\text{DATA READY}}$
18	GRN	18	E	GND
19	BLK	19	N	$\overline{\text{CRD02}}$
20	BRN	20	T	GND
21	BLK	21	L	$\overline{\text{CRD03}}$
22	YEL	22	R	GND
23	BLK	23	f	$\overline{\text{CRD00}}$
24	BLU	24	m	GND
25	BLK	25	K	$\overline{\text{CRD01}}$
26	RED	26	P	GND
27	BLK	27	M	$\overline{\text{END DTA}}$
28	VIO	28	S	GND
29	BLK	29	d	$\overline{\text{CRD11}}$
30	GRN	30	j	GND

CONT.

TABLE 9-1. WIRE LIST - EXTERNAL CABLE (continued)

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
31	BLK	31	r	$\overline{\text{CRD12}}$
32	ORN	32	v	GND
33	YEL	33	n	READY
34	RED	34	t	GND
35	YEL	35	B	$\overline{\text{STROBE}}$
36	BLU	36	F	GND
37	YEL	37	D	$\overline{\text{CKERR}}$
38	GRN	38	J	CKERR

TABLE 9-2. WIRE LIST - INTERNAL CABLE

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
1	WHT-BLK	P2A01	1	$\overline{\text{CRD06}}$
2	BLK	P2B01	2	GND
3	WHT-BRN	P2A02	3	$\overline{\text{CRD07}}$
4	BLK	P2B02	4	GND
5	WHT-RED	P2A03	5	GND
6	BLK	P2B03	6	N.C.
7	WHT-ORN	P2A04	7	$\overline{\text{CRD05}}$
8	BLK	P2B04	8	GND
9	WHT-YEL	P2A05	9	$\overline{\text{FEED}}$
10	BLK	P2B05	10	GND
11	WHT-GRN	P2A06	11	$\overline{\text{CRD04}}$
12	BLK	P2B06	12	GND
13	WHT-BLU	P2A07	13	$\overline{\text{CRD09}}$
14	BLK	P2B07	14	GND
15	WHT-VIO	P2A08	15	$\overline{\text{CRD08}}$
16	BLK	P2B08	16	GND
17	WHT-GRA	P2A09	17	$\overline{\text{DATA READY}}$
18	BLK	P2B09	18	GND
19	WHT-BLK	P2A10	19	$\overline{\text{CRD02}}$
20	BRN	P2B10	20	GND
21	WHT-BRN	P2A11	21	$\overline{\text{CRD03}}$

CONT.

TABLE 9-2. WIRE LIST- INTERNAL CABLE (continued)

CONDUCTOR IDENTITY	COLOR	ORIGIN	DESTINATION	REMARKS/ SIGNAL NAME
22	BRN	P2B11	22	GND
23	WHT-RED	P2A12	23	$\overline{\text{CRD00}}$
24	BRN	P2B12	24	GND
25	WHT-ORN	P2A13	25	$\overline{\text{CRD0T}}$
26	BRN	P2B13	26	GND
27	WHT-YEL	P2A14	27	$\overline{\text{END DTA}}$
28	BRN	P2B14	28	GND
29	WHT-GRN	P2A15	29	$\overline{\text{CRD 11}}$
30	BRN	P2B15	30	GND
31	WHT-BLU	P2A16	31	$\overline{\text{CRD 12}}$
32	BRN	P2B16	32	GND
33	WHT-VIO	P2A17	33	READY
34	BRN	P2B17	34	GND
35	WHT-GRA	P2A18	35	$\overline{\text{STROBE}}$
36	BRN	P2B18	36	GND
37	WHT-BLK	P2A19	37	$\overline{\text{CKERR}}$
38	RED	P2B19	38	CKERR
39	WHT-BRN	P2A20	39	N.C.
40	RED	P2B20	40	N.C.
41	WHT-RED	P2A21	41	N.C.
42	RED	P2B21	42	GND

TABLE 9-3. PWB PIN LIST

CONNECTOR/PIN	SIGNAL NAME
P1A01	$\overline{\text{A05}}$
02	$\overline{\text{A06}}$
03	$\overline{\text{A00}}$
05	$\overline{\text{A11}}$
06	$\overline{\text{A03}}$
07	A04
12	Q00
15	Q06
16	Q08
17	Q10
20	$\overline{\text{W=0}}$
21	$\overline{\text{READ}}$
22	$\overline{\text{REPLY}}$
23	$\overline{\text{PRØTECT}}$
P1A31	$\overline{\text{STPCK}}$
P2A01	$\overline{\text{CRD 06}}$
02	$\overline{\text{CRD 07}}$
04	$\overline{\text{CRD 05}}$
05	$\overline{\text{FEED}}$
06	$\overline{\text{CRD 04}}$
07	$\overline{\text{CRD 09}}$
08	$\overline{\text{CRD 08}}$
09	$\overline{\text{DATA READY}}$
10	$\overline{\text{CRD 02}}$
11	$\overline{\text{CRD 03}}$
12	$\overline{\text{CRD 00}}$
13	$\overline{\text{CRD 01}}$
14	$\overline{\text{END DATA}}$
15	$\overline{\text{CRD 11}}$
16	$\overline{\text{CRD 12}}$
17	READY
18	$\overline{\text{STROBE}}$
P2A19	$\overline{\text{CKERR}}$

CONNECTOR/PIN	SIGNAL NAME
P1B01	$\overline{\text{A01}}$
02	$\overline{\text{A02}}$
03	$\overline{\text{A07}}$
04	$\overline{\text{A08}}$
05	$\overline{\text{A09}}$
06	A10
12	Q01
14	Q05
15	Q07
16	Q09
21	$\overline{\text{WRITE}}$
22	$\overline{\text{REJECT}}$
23	$\overline{\text{MC}}$
24	$\overline{\text{DATA INT}}$
25	$\overline{\text{EØP INT}}$
26	$\overline{\text{ALARM INT}}$
27	$\overline{\text{COMMON INT}}$
P1B31	$\overline{\text{EXCK}}$
P2B19	CKERR RTRN

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COMMENT SHEET

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Reference/Customer Engineering Manual

PUBLICATION NO. 89637500 REVISION B

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