CONTROL DATA® 8490
COMPUTER SYSTEM

COMPUTE UNIT,
AUXILIARY MEMORY UNIT,
AND I/O UNIT

THEORY OF OPERATION
EQUIPMENT DIAGRAMS

CONTROL DATA
CORPORATION

CUSTOMER ENGINEERING MANUAL

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Address comments concerning this manual to:

Control Data Corporation
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Technical Publications Department
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CONTENTS

SECTION 1 COMPUTE UNIT

THEORY OF OPERATION

FIGURES

FOREWORD

SCOPE AND ORGANIZATION

This manual is divided into three sections corresponding to the three major units in a CONTROL DATA® 8490 Computer System. Each section contains the theory of operation (circuit description) and the equipment diagrams associated with that unit.

The other customer engineering manuals provide additional information for the 8490 Computer. The Maintenance/Command Timing manual provides the information necessary to maintain the equipment and to understand the step-by-step sequencing of the instructions. The Equation Summary, Card Placements, and Wire List manuals provide detailed information concerning the Boolean equations, card types, and a listing of all wires for every term for each unit in the system.

PUBLICATIONS REFERENCE LIST

The following is a list of publications associated with the 8490 Computer System.

Manual	Pub. No.
8490 Computer System Reference Manual	14091600
8490 Customer Engineering Manuals	
Maintenance/Command Timing	14092000
Compute Unit Equation Summary, Card Placements, and Wire List	14092100
I/O Unit Equation Summary, Card Placements, and Wire List	14092200

Manual	Pub. No.
Auxiliary Memory Unit Equation Summary, Card Placements, and Wire List	14092300
8490 Site Preparation and Installation Manual	14091800
8490 ADSAS and FORTRAN Operations Manual	14091900
8490 System Maintenance Monitor Reference/Program Listing Manual	14094700
Printed Circuit Manual (Volumes 1 and 2)	60042900

SYSTEM CONCEPTS

The CONTROL DATA 8490 Computer System is a high-speed, modular computing system suited to real-time control and data processing applications. The flexible characteristics of the 8490 system permit it to be expanded into a system with large-scale storage, input/output, and computational capabilities. With several options available, the 8490 can be tailored to meet particular data needs and can later grow with increased demands for data processing.

SYSTEM DESCRIPTION

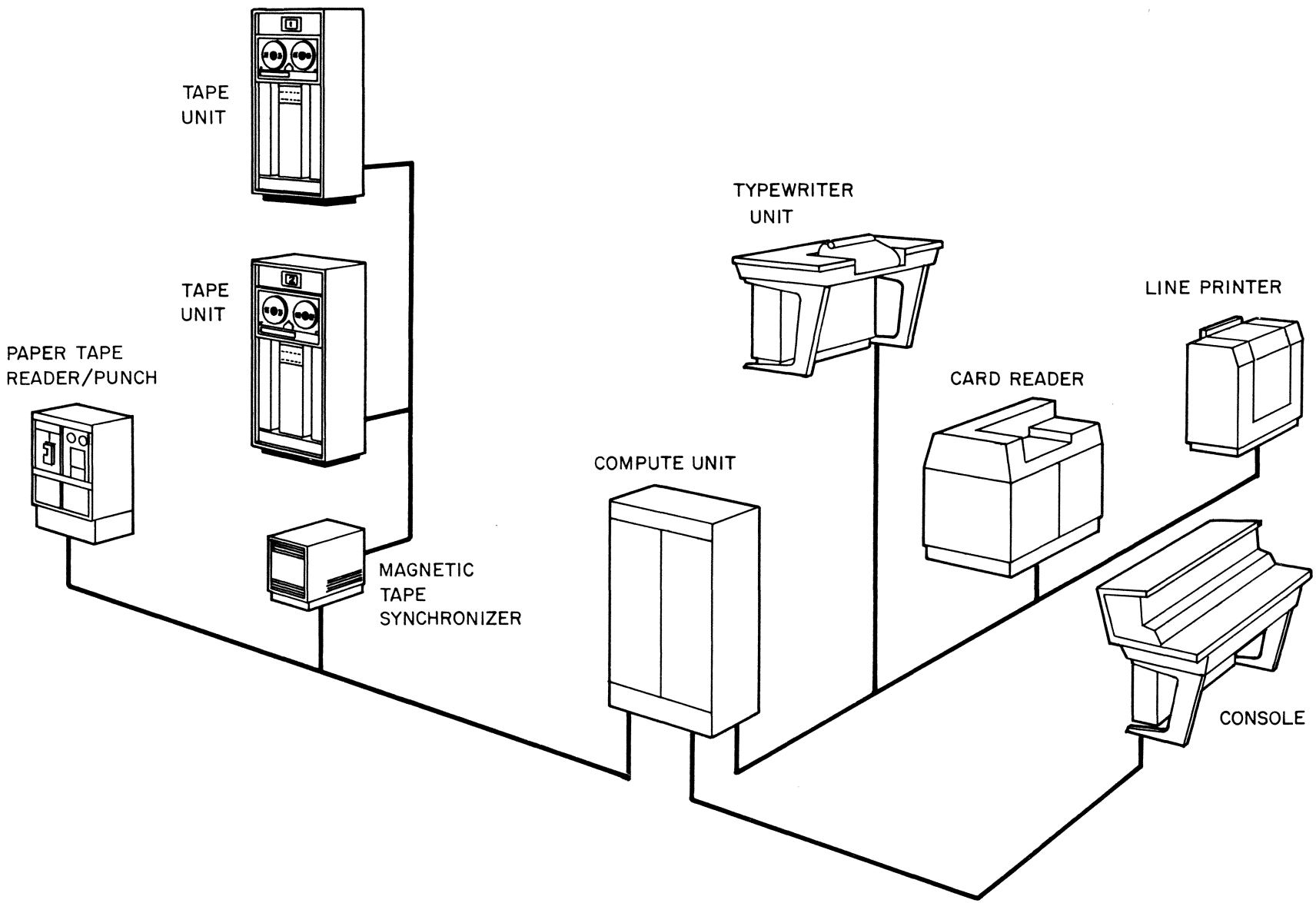
The 8490 Computer System is a data processing device expandable on a modular basis. A minimum system consists of a single Compute Unit and associated Console. An illustration of a typical 8490 system is found on on the facing page.

KEY TO LOGIC SYMBOLOGY

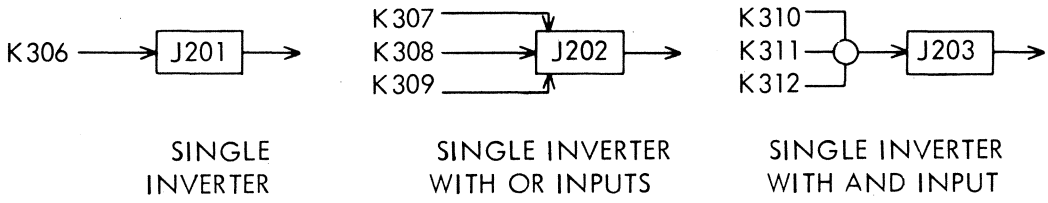
SYMBOLS

Single Inverter

A single inverter inverts input signals so that a 1 input gives a 0 output and a 0 input gives a 1 output. Inputs to the symbol are indicated by arrowheads.



Typical 8490 Computer System



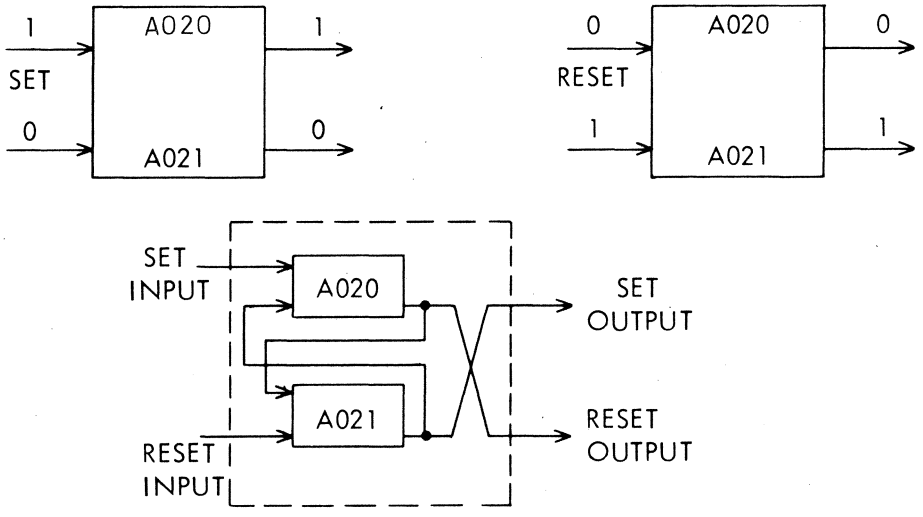
SINGLE INVERTER

SINGLE INVERTER WITH OR INPUTS

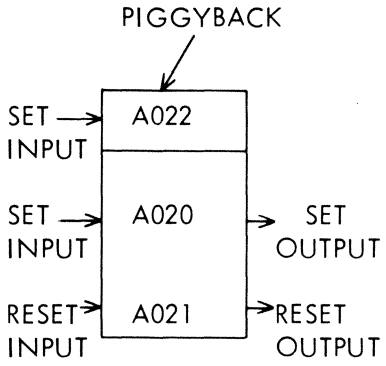
SINGLE INVERTER WITH AND INPUT

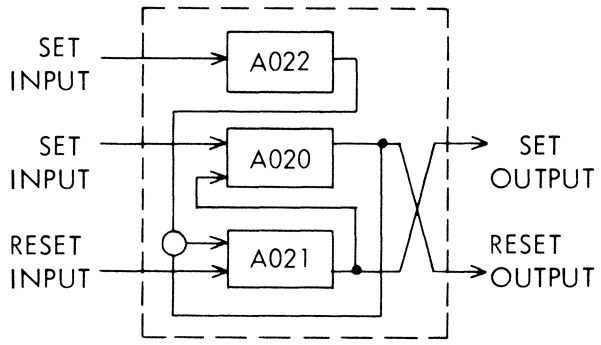
Flip-Flops

A flip-flop is a temporary storage device with two stable states designated set and reset. When a flip-flop is set, the set output is a logic 1; when reset, the reset output is a 1. The logic symbol for a flip-flop is a square formed by combining two single inverter symbols. The flip-flops are pre-wired to receive a limited number of inputs. When the necessity for additional inputs develops at an inverter of a flip-flop, an additional inverter is used "piggyback fashion". By convention, set inputs and outputs are shown at the even-numbered inverter; reset inputs and outputs are shown at the odd-numbered inverter. The first two digits contained in the flip-flop number pertaining to flip-flop grouped together as a register indicate stage nomenclature. For example, the inverters used in the flip-flop diagrams indicate STAGE 2 if they were used as a particular stage of a register.



INTERCONNECTION OF THE TWO INVERTERS





INTERCONNECTION OF PIGGYBACK INVERTER WITH FLIP-FLOP INVERTERS

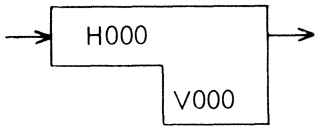
Control Delay

A control delay consists of an H--- term, which receives the input, and a V--- or N--- term, which provides the output. The output is a clocked pulse which is delayed with respect to the input by one phase time of the clock (62.5 nanoseconds). The H--- term of the control delay is prewired to receive a limited number of inputs. When the necessity for additional inputs develops, an additional H--- term is used "piggyback fashion". Conventions applicable to control delays are as follows:

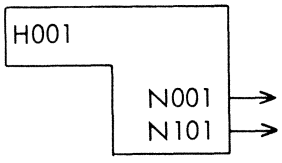
1. Clock pulse inputs to control delays are not shown on the diagrams and must be obtained from the equation file.

2. An odd number indicates a clock output of odd phase time and an even number of even phase time.

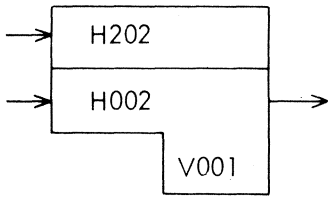
3. The timing on all sequence diagrams is in 62.5-nanosecond (one phase time) intervals.



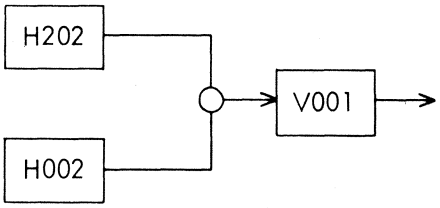
SINGLE INPUT AND OUTPUT



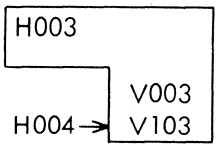
MULTIPLE OUTPUT



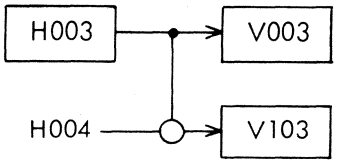
PIGGYBACK CONTROL DELAY



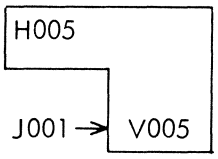
INTERCONNECTION OF PIGGYBACK CONTROL DELAY



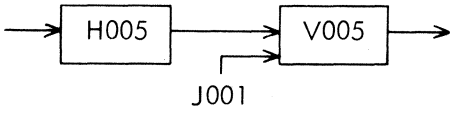
MULTIPLE INPUT (ONLY WHEN SECOND INPUT IS AN H----TERM)



INTERCONNECTION OF MULTIPLE INPUT



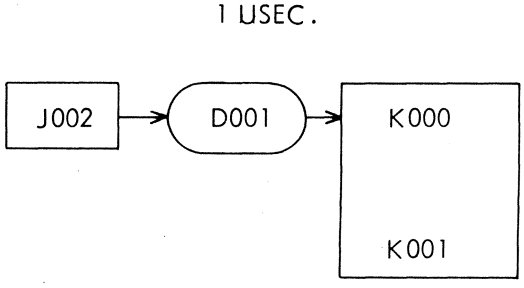
CONDITIONED OUTPUT (WHEN SECOND INPUT IS OTHER THAN H- - - TERM)



INTERCONNECTION OF CONDITIONED OUTPUT

Capacitive Delay

The function of a capacitive delay is to provide an interval of time delay between successive logical operations. This is accomplished by regulating the length of time for a 1 input to pass through the delay circuit. The delay time for a 0 input is approximately one-tenth of the delay time for a 1 input.

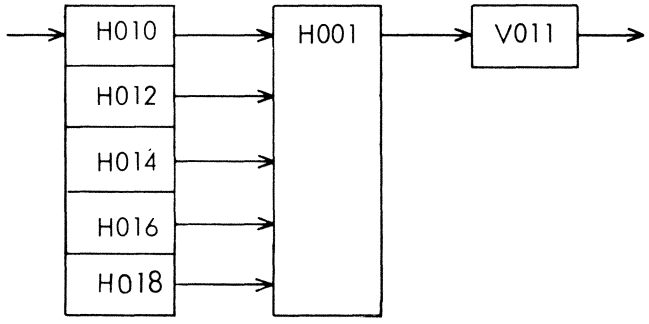


CAPACITIVE DELAY

Resync Circuit

The function of a resync circuit is to synchronize an asynchronous signal of random length with the master clock. A 1 input of random length produces a 1 output of 62.5-nanosecond duration.

RESYNC CIRCUIT

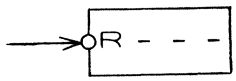


Miscellaneous

The rectangular box, symbol for an inverter, is also the symbol for the following circuits:

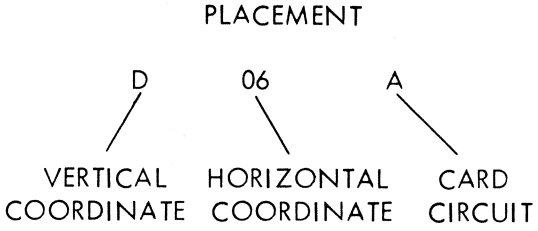
C - - -	MASTER CLOCK
D - - -	TRANSFORMER DRIVER
G - - -	GATE
L - - -	INDICATOR DRIVER
R - - -	RECEIVER
T - - -	TRANSMITTER
T8 - -	DRIVER TRANSFORMER
T9 - -	DRIVER TRANSFORMER
Y - - -	SENSE AMPLIFIER

The normal receiver, as previously illustrated, does not logically invert the input signal. The following symbol is used to denote logical inversion through a receiver.

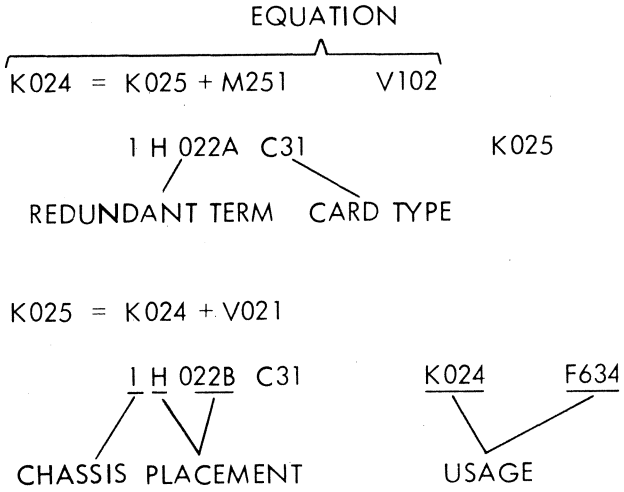


PLACEMENTS

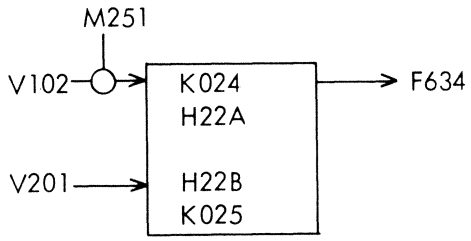
Placements indicate the physical location of a printed-circuit card. On logic diagrams, the placement associated with each symbol appears near it. Only the horizontal and vertical placements and the test point of the symbol are given (except for the Memory Unit where chassis number is included for access channel logic). In the Compute Unit the chassis number is always 1. In a Memory Unit (except access channel logic) or an I/O Unit, the chassis number is determined by unit placement in the cabinet. Units are numbered from right to left within a cabinet or as viewed from the front. Redundant terms and card types are given in the equation file.



SYMBOLIC REPRESENTATION OF EQUATIONS



The last three digits of the placement number in the equation file indicate card type. This number can be obtained to find the card schematic in the logic diagrams by referencing the equation file from the logic diagrams. For a functional analysis of the card schematic, refer to the Maintenance manual.



SYMBOL INDEX

The symbol index, at the front of each section of logic diagrams, lists in alphanumeric order each subject term, its card placement, the function name, and the sheet number on which the term is shown with all its inputs.

SECTION 1

COMPUTE UNIT

THEORY OF OPERATION

SECTION 1

COMPUTE UNIT

The Compute Unit functions as a complete computer without any I/O or Memory Units. It contains two bidirectional data channels, one normal and one buffered; 8,192 words of magnetic core storage; and arithmetic and control logic.

GENERAL THEORY OF OPERATION

The 8491 Compute Unit is a parallel, single address, electronic data processor. It performs calculations and processes data internally in a parallel binary mode. The internally stored program, located in sequential storage locations, controls the step-by-step execution of individual instructions. Individual instructions in a Compute Unit are executed in one to six storage cycle times. (One storage cycle is 1.35 microseconds.)

The 8491 Compute Unit, which functions as a complete small-scale computer in the basic system, provides the arithmetic and control characteristics in an expanded system.

An 8491 Compute Unit includes a Console for operation and maintenance purposes. The Console contains the controls and indicators necessary to operate the Compute Unit and any associated I/O Units and Auxiliary Memory Units. Figure 1-1 is a simplified functional block diagram of the 8491 Compute Unit.

MEMORY REFERENCE

The contents of the S register and the bank control for a given instruction determine which storage location in memory is referenced. If the address is

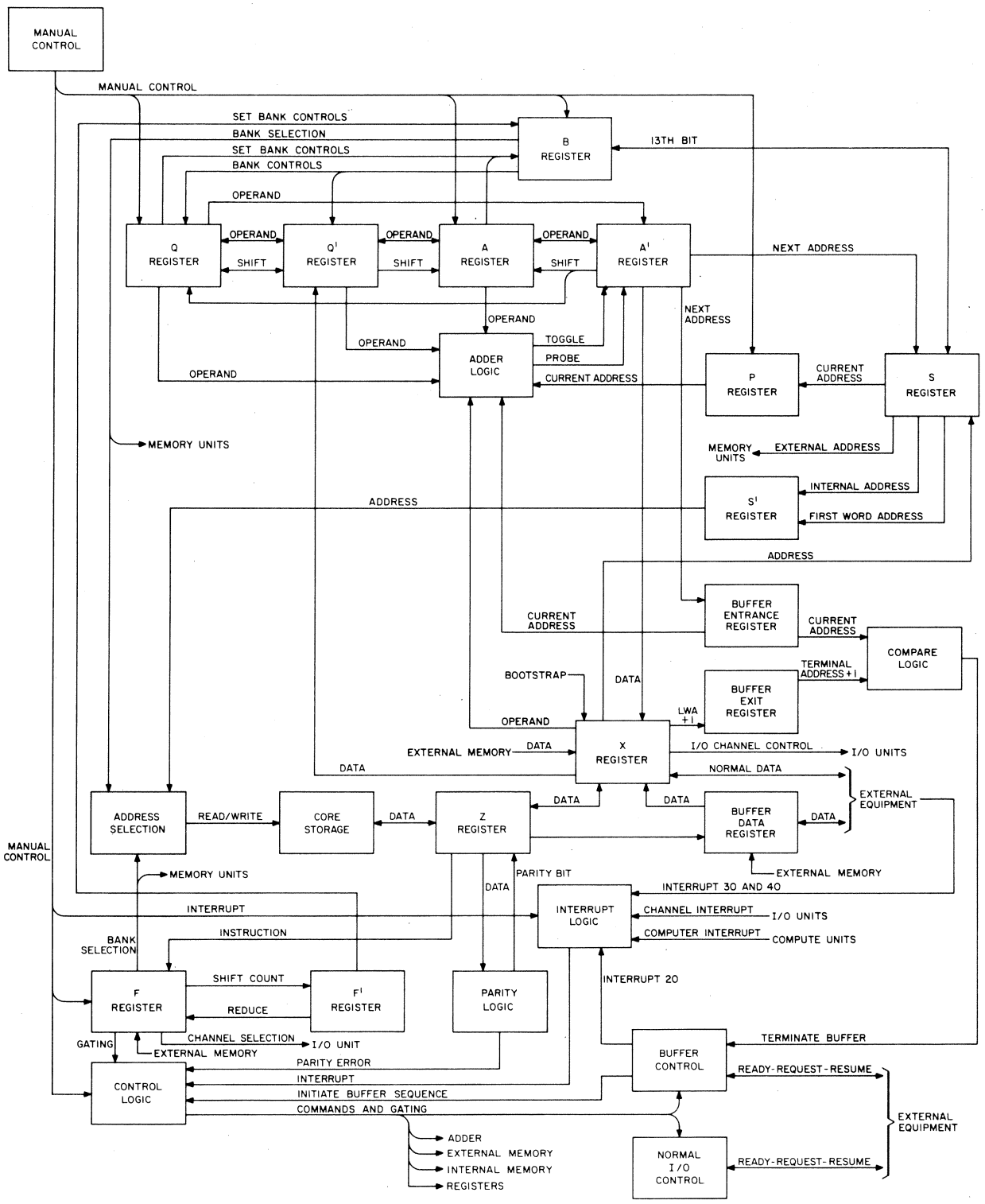


Figure 1-1. Compute Unit - Simplified Functional Block Diagram

in a Memory Unit bank, the contents of S is placed on the address selection lines to external memory (where it is placed in the S' register in the Memory Unit). If the bank selected is in the Compute Unit, the contents of S is transferred to internal S'. The latter register then conditions the address selection logic to reference the location specified by the contents of S'. The following description considers references involving Compute Unit memory.

Read

For a read operation, the contents of the selected location is transferred through the Z register to the X register where the data is available for manipulation. After the transfer is complete, the Z register restores the data in the original location. While the data is in the Z register, a parity check is performed; if parity is wrong, a parity error signal, which tells the computer that data is faulty, is generated. An interrupt 10 is then generated and bit 2^{10} of the error register is set.

Write

For a write operation, the data is transferred from X to Z. The selected location is then cleared, and the contents of Z is written into this location. The data in Z is also sampled by the parity logic. This circuit generates a parity bit, as required, to accompany each word that is written into core storage.

PROGRAM CONTROL

An 8490 program consists of a number of routines. Each routine contains a series of instructions that is stored in sequential memory locations. The instruction being executed is called the current instruction. At the completion of a routine, control is normally transferred to the next routine.

The Compute Unit is ready to begin the routine when the P register contains the first address in a routine as a result of a manual or programmed entry. The contents of P is transferred to the S register. The instruction at the location specified by the contents of S (current instruction) is read from memory. This instruction is transferred to the X and F registers. Once it is in the F register, the instruction conditions the control logic to execute this same instruction. Sometime before the execution of the instruction has been completed, the contents of P is transferred to the adder. The commands are then generated which increment the current address to the address of the next instruction.

This address appears in A' which serves as the output of the adder. The address is then transferred to S and then from S to P. This address now represents the new current instruction address. Unless the Compute Unit is interrupted, the preceding procedure is repeated until all of the steps in

the routine have been completed. At the completion of each routine, control is transferred to the next routine until a manual or programmed stop occurs.

ARITHMETIC OPERATION

When an arithmetic instruction is executed, the control logic conditions the subtractive adder and the A, A', Q, and Q' registers to perform the necessary arithmetic.

The subtractive adder provides the necessary signals to form in A', by one's complement addition, the sum of an operand from X and an operand from A or Q. Whether the resultant in A' represents the sum or difference of two numbers is determined by the operand from X. If the operand is the contents of X, the resultant equals the sum. If the operand is the complement of the contents of X, the resultant equals the difference.

The 8491 Compute Unit performs multiplication by repeated additions and right shifts, and division by repeated subtractions and left shifts. The shifts are necessary to maintain the proper bit position of the resultant.

EXTERNAL FUNCTION

When the Compute Unit executes an external function (EF) instruction, a 12-bit EF code is read from the Compute Unit memory and placed in the X register. This EF code is then sent to one of the I/O channels, either internal or external, to the equipment for which the code is intended. The channel used is determined by the instruction in the F register. Generally, EF codes are used to sense the status of a particular equipment or to activate equipment for a particular type of operation.

INPUT/OUTPUT

The I/O circuitry of the Compute Unit permits the transfer of data between the Compute Unit and external equipment. This transfer may be either normal or buffered. A normal operation completely ties up the Compute Unit; however, during a buffer operation the Compute Unit is free most of the time to perform other operations.

NORMAL INPUT

A normal input occurs only when it is programmed as part of a routine. An EF code must be generated by the Compute Unit before the normal input can occur. This EF code activates the appropriate input device. The control logic in the Compute Unit also enables the normal I/O control logic for an exchange-of-status signal with the input device. At the appropriate time

during the exchange, the input data is transferred through the X register into the Z register and then stored at the address specified by the contents of the S register.

The normal input instruction specifies a first word address (FWA) and a last word address plus one (LWA + 1) of a storage area. The first word address is contained in A. After an input word has been stored, the contents of A is increased by one. The resultant is formed in A' and then gated into A. The new address is then compared with the LWA + 1. If the two addresses are not equal, the new address is transferred to S and the cycle is repeated to store another word. This process continues until the two addresses are equal. The normal input operation then terminates.

NORMAL OUTPUT

Normal output operation is similar to the preceding description of normal input; however, the contents of the address placed in the S register is read from core storage and transferred through Z and X to the selected output device. The number of words to be transmitted to the output device is specified by the difference between the FWA and the LWA + 1. The normal output operation is terminated in the same manner as the normal input operation.

BUFFERED INPUT

When the Compute Unit performs an input buffer routine, instructions are executed to perform the following steps:

1. Load BER with the FWA of the I/O.
2. Load the BXR with the LWA + 1 of the I/O area.
3. Set the buffer bank control to the proper storage bank.
4. Select the I/O equipment.
5. Initiate the buffer input.

The particular order of the first three steps is optional, but these steps are always performed before initiating the buffer input. The I/O equipment must be selected before initiating the input buffer.

The buffer control logic causes the Compute Unit to interrupt the current routine to perform a buffer sequence. This sequence generates the commands which perform the following steps:

1. Gate the data word into BFR.

2. Transfer the FWA to S.

3. Store the input word at the address specified by the contents of S.

4. Enable the contents of the BER (current address) to the subtractive adder.

5. Increase the current address by one to form the next address.

6. Transfer the next address to BER register where this address becomes the new current address.

7. Clear the I/O control logic if the contents of the BER and BXR are equal.

The preceding steps are repeated by each input word until the current address equals the LWA + 1. At this time, the buffer control logic generates a terminate buffer signal. The resulting interrupt 20 enables the interrupt logic and causes the control logic to terminate the buffer and to continue with the interrupted routine.

BUFFERED OUTPUT

The operation of the Compute Unit for an output buffer is similar to the operation for an input buffer. The preliminary steps are the same. The Compute Unit then executes an IBO instruction which causes the Compute Unit to perform the buffer sequence. This sequence reads the contents of the location specified by the FWA from core storage and transfers this data through the Z register to BFR. When the output data is ready, an information ready signal is sent to the output device.

INTERRUPTS

If interrupt is not locked out, a signal on any of the interrupt lines into the interrupt logic results in a signal to the control logic which interrupts the routine being performed. Program control is then transferred to the routine which services the active interrupt. Regardless of the type of interrupt, the same general procedure is followed. The Compute Unit stores the address of the next instruction to be executed in the interrupted routine and reads the instruction contained in the special storage location associated with the active interrupt. At the completion of the interrupt routine, the next instruction in the interrupted routine is read from memory and program control is returned to the interrupted routine.

DETAILED THEORY OF OPERATION

REGISTERS

Temporary storage units for operands, instructions, and control words are called registers. The contents of the registers can be displayed on the Console. When referring to a stage of a register, a subscript designates stage number; for example, the A register contains 13 stages, A_{00} through A_{12}. The following discussion analyzes typical stages of the A and A' registers and the control logic which conditions the inputs to these registers. Only the function is given for all other registers; however, these registers can be analyzed in the same manner as the A and A' registers.

Basic Register Controls

The logic circuits that condition the registers are known as controls. These controls generate the signals that gate information into a register, clear a register, or shift data from one register to another.

Basically, the controls for all registers are similar. These controls can be categorized as clear, transfer, or shift controls. These three types of controls are discussed in the following paragraphs. A detailed logic analysis of the A register controls is included in the paragraphs on registers. All other register controls, except set X, can be analyzed in a similar manner.

Clear: A clear control is shown with the transfer of 1's example in Figure 1-2. The output of the clear control enters the reset side of every flip-flop in the register. Thus, when the output of the clear control is a 1, every flip-flop in the register is reset.

Register-to-Register Transfer: Three types of register transfers are used in the Compute Unit; forced transfer, transfer of 1's, and transfer of 0's, Figure 1-2. For a transfer of 1's, an output from the transfer control and a set output from a flip-flop in the lower register form an AND gate input to the corresponding stage in the upper register. When the output of the transfer control is a 1, each flip-flop in the upper register is set if the corresponding stage in the lower register is set. However, before any transfer of 1's can be made, the upper register must be cleared.

For a forced transfer, a set output of a flip-flop in the lower register and an output of the transfer control form a set input AND gate to the corresponding stage of the upper register. The reset output forms a similar input to the reset side. When the output of the transfer control is 1, the contents of the lower register is duplicated in the upper register, regardless of the previous contents of the upper register. Thus, it is not necessary to clear a register before a forced transfer.

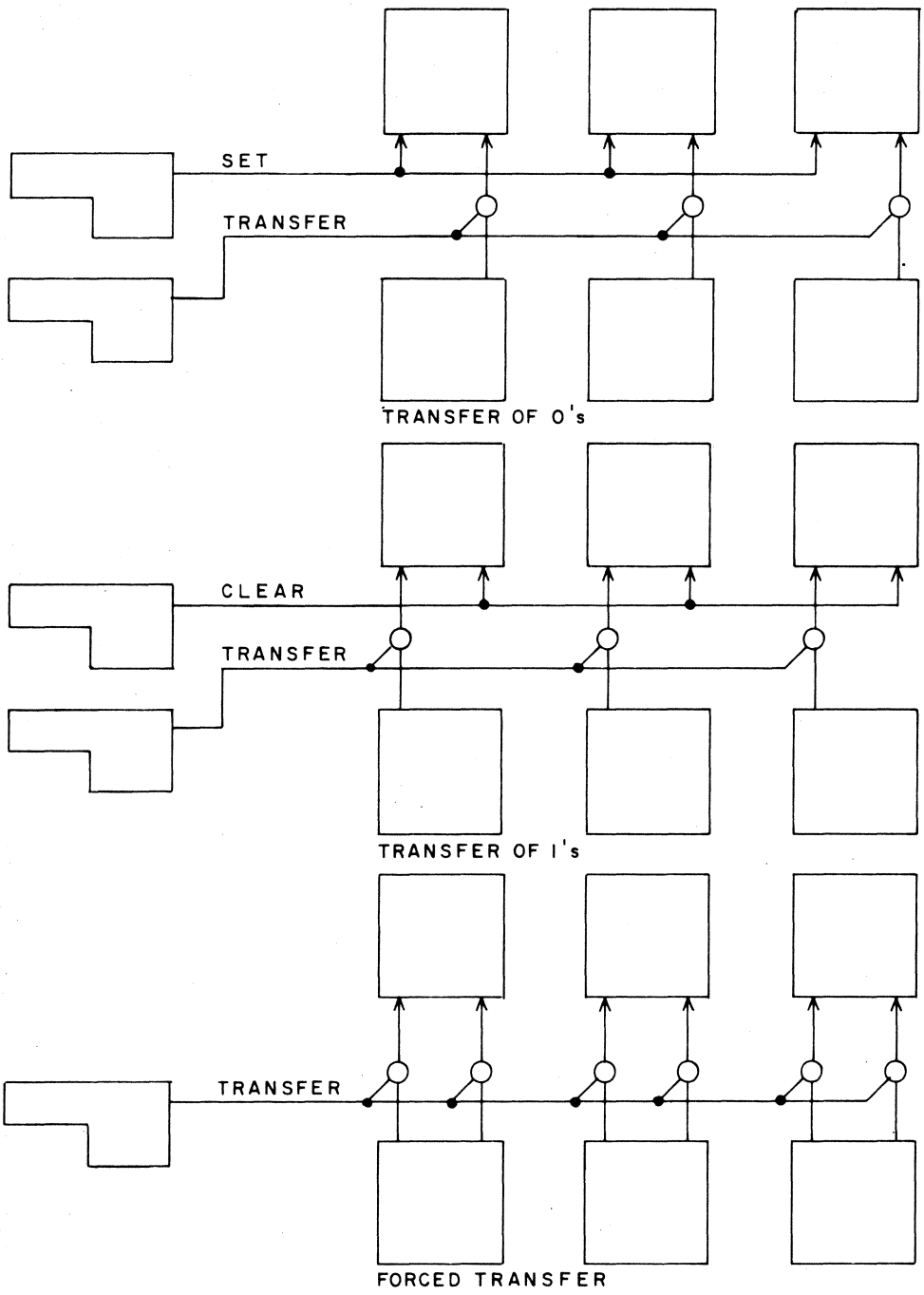


Figure 1-2. Register-to-Register Transfer

Before a transfer of 0's, it is necessary to set every stage of the upper register. When the output of the transfer control is 1, each stage of the upper register is reset if the corresponding stage of the lower register is reset.

Shift: Data can be shifted right or left from A' to A or from Q' to Q. Furthermore, AQ and A'Q' can be treated as double length registers, and data can be shifted right or left from A'Q' to AQ. Figure 1-3 illustrates the stage-to-stage transfers that occur for all types of shifts. All left shifts are end around; the highest order bit is shifted to the lowest order stage. Right shifts are end off; the lowest order bit is discarded and the sign bit is extended. All shifting is done by forced transfer.

Arithmetic Register (A)

The 13-bit A register functions as the primary arithmetic register. This register holds operands and resultants during most arithmetic and shifting operations, Figure 1-4.

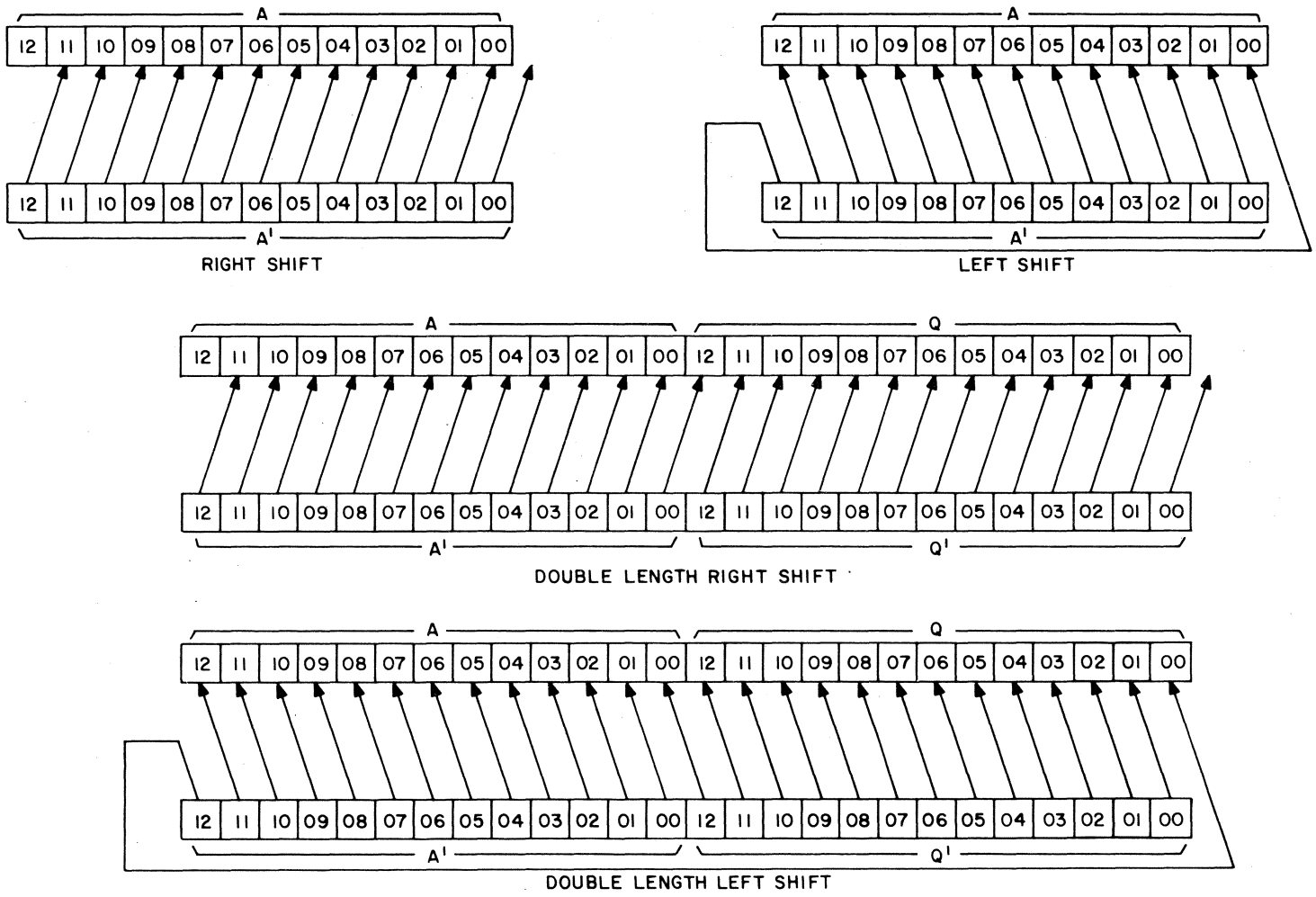
The A register provides the following outputs:

Output	Subject Terms
A' Register	A--4, A--5
Q' Register	Q--4, Q--5
I Inverters	I001 - I111
U Inverters	U001 - U121
Display	L001 - L121
B Register	B100 - B190

The lowest order stage of the A register has two inverters (A002 and A003) which act as extensions of this stage. These inverters are necessary because more inputs are required to A000/A001 than can be connected to the printed-circuit card which contains this flip-flop. Logically, inputs to A002 are identical to inputs to A000. Similarly, inputs to A003 are logically identical to inputs to A001. The following controls, Figure 1-5, affect the inputs to the A register.

Clear A: The output of clear A control delay H901/N-01 is connected to the reset side of every stage in the A register. When any one of the inputs to H901/N-01 is a 1, the resultant 1 outputs clear the A register. The clear A command occurs when any of the following conditions are satisfied:

1. When master cleared (W140).



NOTE: SIMILAR SINGLE LENGTH SHIFTS CAN BE PERFORMED FROM Q' TO Q.

Figure 1-3. Shifting

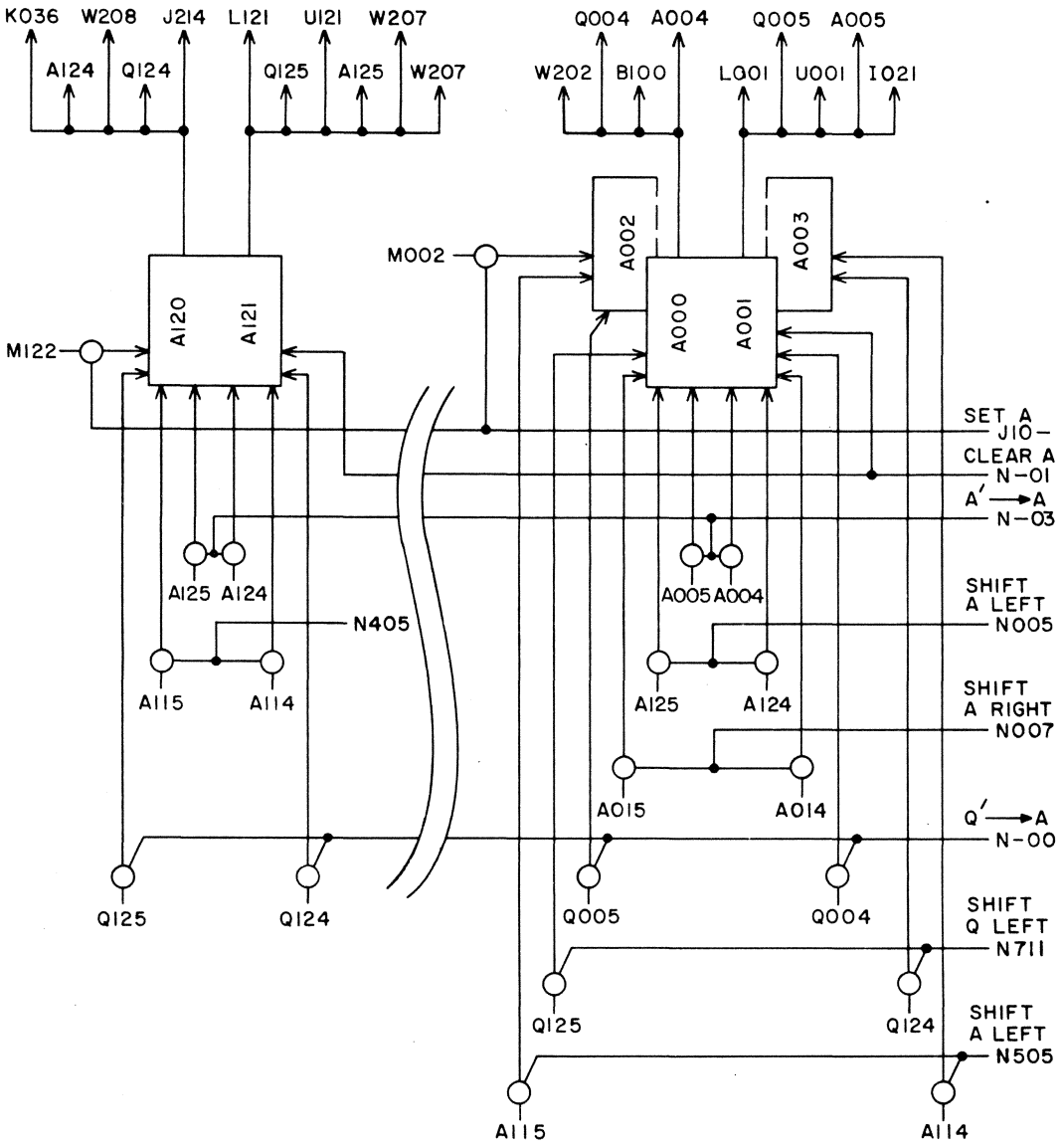


Figure 1-4. Typical A Register Stages

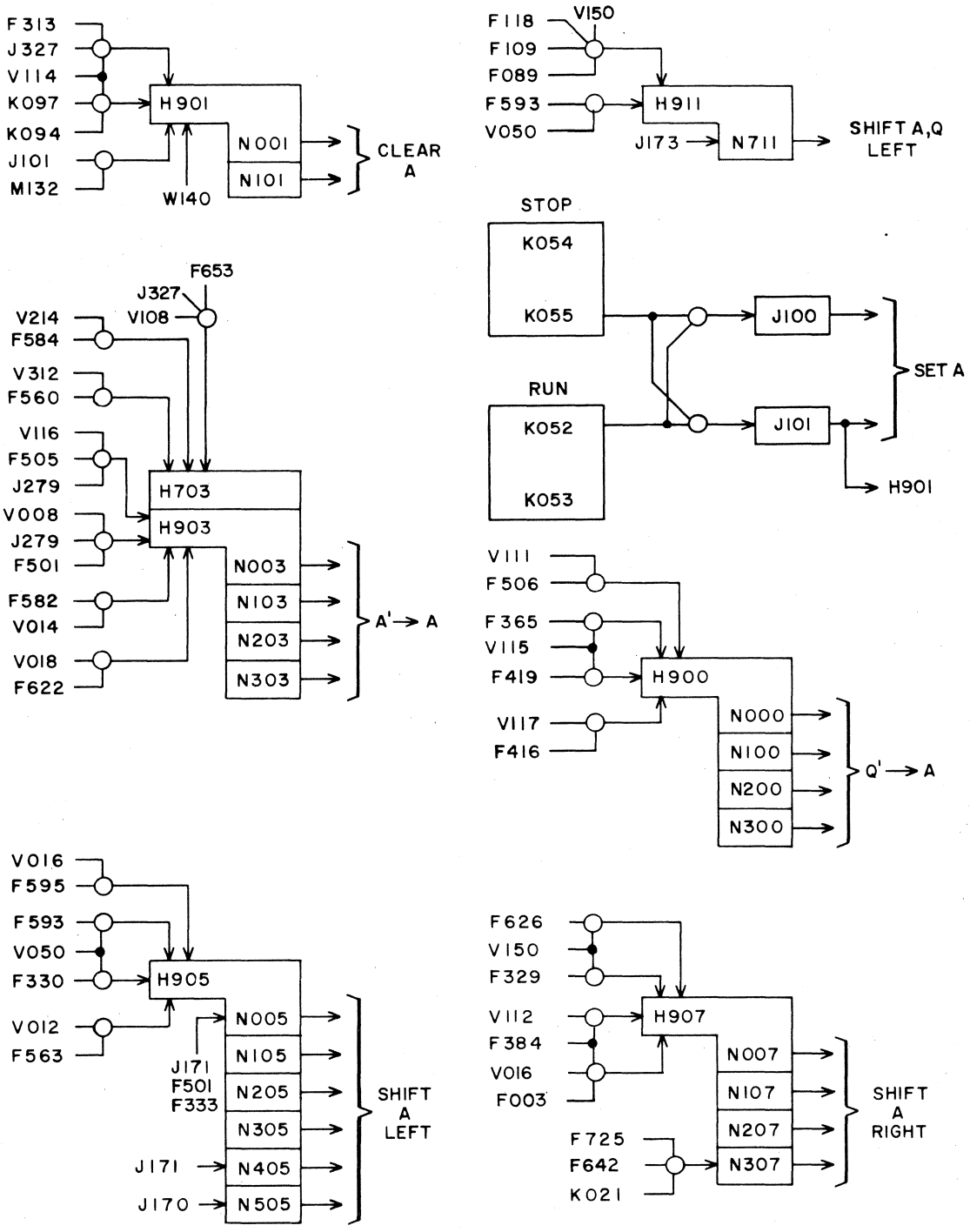


Figure 1-5. A Register Controls

2. When depressing the clear A pushbutton on the Console when the computer is not running (J101 M132).

3. At ø14 in the D cycle of an MU instruction (F313 J327 V114).

4. At ø14 of a manual enter except when the EM pushbutton is depressed (V114 K097 K094).

A' to A: Control delay H703-H903/N-03 regulates the transfer of data between the A' and A registers. Whenever either H703 or H903 receives a 1 input, the resultant 1 outputs from N-03 gate the contents of A' to A by a forced transfer. The A' to A command occurs when any of the following conditions are satisfied.

1. At ø8 of the D cycle for an OUT instruction (F653 J327 V108).

2. At ø14 of the D cycle for instruction AD, SB, LC, LP, RA, AO, or INP (V214 F584).

3. At ø12 of a D or E cycle for an MU or DV instruction, at ø12 of a PTA or XAQ instruction, at ø12 of the B cycle for an INP or OUT instruction (V312 F560).

4. At ø16 of the E cycle for an MU or DV instruction (V116 F505 J289).

5. At ø8 of the E cycle for a DV instruction (V008 J279 F501).

6. At ø14 of an LPN, ADN, SBN, SCN, LCN, or ETA instruction (V014 F582).

7. At ø18 of an MUT or MUH instruction (V018 F622).

Set A: The set A logic enables and disables the manually set pushbutton switches associated with the A register display on the console. Whenever the computer is running, the set A logic disables the set switches to prevent the accidental entry of data into A. If the computer is stopped, the 1 outputs of J100 and J101 enable the switch outputs. Then, when a given switch is depressed, the associated stage of A is set. The 1 outputs of J100 and J101 occur when the stop flip-flop is set or the run flip-flop is reset.

Shift A Left: A 1 output from the shift A left control gates A' to A in such a manner that the resultant is shifted one bit position to the left. The highest order bit of A' is shifted end-around to the lowest order stage of A. The shift A left command occurs whenever any of the following conditions are satisfied:

1. At ø16 of an LS2, LS3, or LS6 instruction (V016 F595).

2. At Ø50 of a DV instruction (V050 F593).

3. At Ø50 of an ALS or LLS instruction in the 8490 mode (V050 F330).

4. At Ø12 of an SR, LS1, LS2, LS6, MUT, or MUH instruction (V012 F563).

Three of the output inverters in the shift A left control contain additional gating to provide the correct resultant for shifts in either the 8090 or 8490 mode. When the shift A left command occurs, N005, N405, and N505 have 1 outputs only if all other OR inputs to the inverter are 0. For an A left shift in the 8090 mode, J170 has a 0 output which enables N505 to gate A_{11} to A_{00}. The 1 output from J171 disables N005 and N405.

For an A left shift in the 8490 mode, the 1 output of J170 disables N505. The 0 output from J171 enables N405 to gate A_{11} to A_{12}. Inverter N005 gates A_{12} to A_{00} only when J171, F501, and F333 have 0 outputs. Thus, this transfer occurs for all A left shifts in the 8490 mode except those which are a part of the 26-bit shifts in DV and LLS instructions. For 26-bit left shifts, Q_{12} is gated to A_{00}; hence, the A_{12} to A_{00} transfer must be disabled.

Shift AQ Left: Part of the shift Q left control affects the A register for an AQ left shift. This control gates Q_{12} to A_{00}. The outputs of H911 also control inverters N011 through N611; however, these inverters affect the Q register. Whenever there is a 1 input to H911, inverters N-11 receive 0 inputs. However, N711 has a 1 output only if J173 (AQ shift) has a 0 output. A 1 input to H911 occurs for either of the following conditions:

1. At Ø50 of an AQ left shift instruction (V150 F118 F109 F089).

2. At Ø50 of a DV instruction (V150 F593).

Q' to A: Control delay H900/N-00 gates the contents of the Q' register to the A register by a forced transfer. When there is a 1 input to H900, the Q' to A transfer occurs. Any of the following conditions produce this command:

1. At Ø11 of an LDN instruction; at Ø11 of the B cycle for an EXC, EXF, or EXCY instruction; or at Ø11 of the D cycle for an INA or LD instruction (V111 F506).

2. At Ø15 of a CTA or CTAQ instruction (F365 V115).

3. At Ø15 of an INAY, ETAY, or ERTA instruction (V115 F419).

4. At Ø17 of the C cycle for an INP or OUT instruction (V117 F416).

Shift A Right: An A right shift can be either a 12- or a 13-bit shift, as determined by the 8090 or 8490 mode of operation. The lower order 12 bits of A' are shifted right one bit position if there is a 1 input to H907. However, A_{12} is shifted to A_{11} only if there is also a 0 input to N307. The A right shift command occurs when any of the following conditions are satisfied:

1. At ø50 of an MU instruction (V150 F626).
2. At ø50 of an ARS or LRS instruction in the 8490 mode (V050 F329).
3. At ø12 of an RS1 or RS2 instruction (V112 F384).
4. At ø16 of an RS1 or RS2 instruction if F_{00} is set (F384 V016 F003).

However, the 1 output from N307 occurs only if one of the following conditions indicating a 13-bit shift is present:

1. An MU instruction when the contents of X is negative or a DV instruction when the contents of X is positive (F642).
2. An 8490 shift (F725).
3. An 8090 mode flip-flop reset (K021).

Adder Output Register (A')

The A' register functions as a second rank of the A register. However, the A' register also serves as the output register of the subtractive adder. The A' register contains 13 stages, Figure 1-6. It provides the following outputs:

Output	Subject Terms
A Register	A--0, A--1
S Register	S--0, S--1
X Register	X--0, X--1
Q Register	Q--0, Q--1
B Register	B--6

The following control circuits, Figure 1-7, regulate the inputs to the A' register.

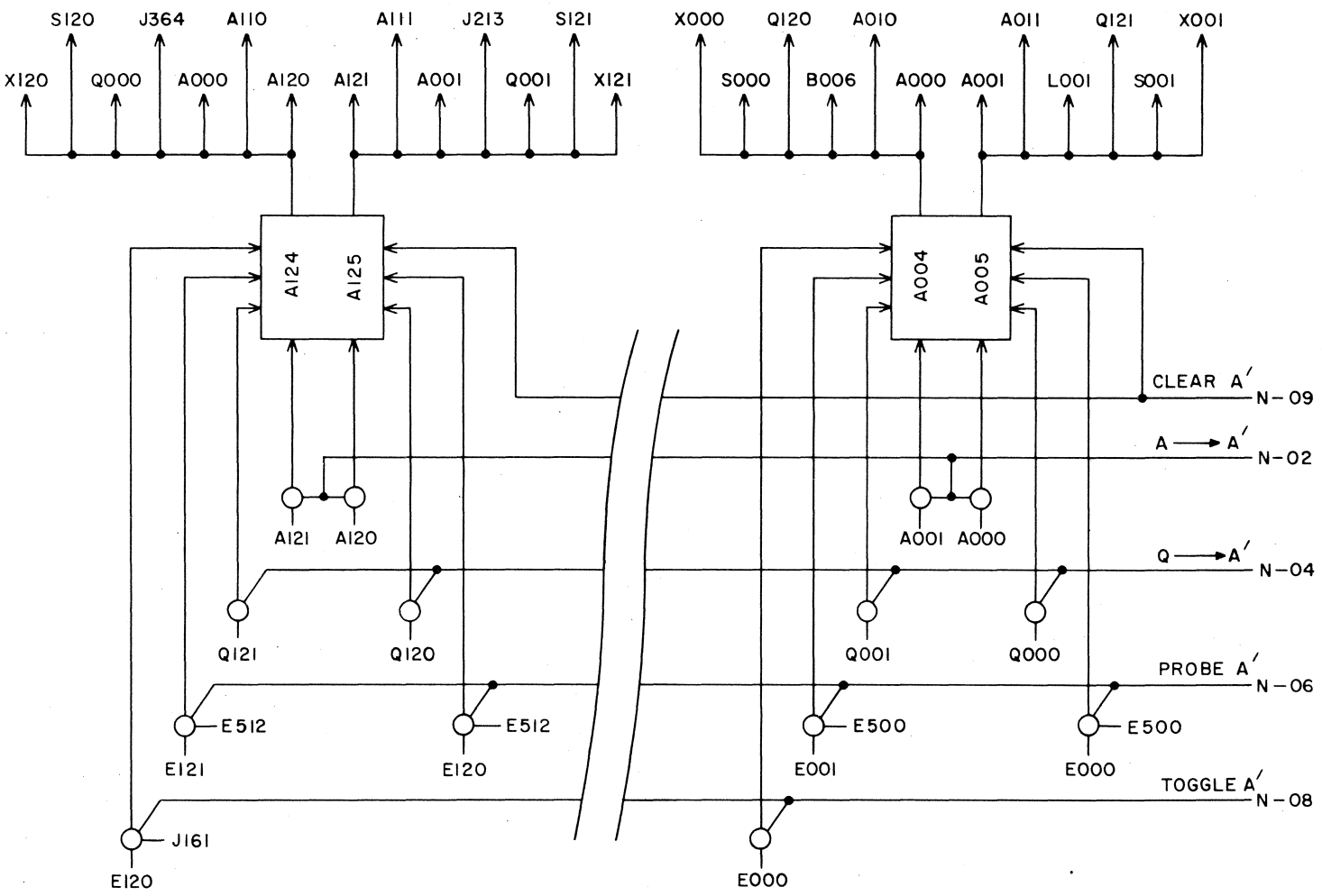


Figure 1-6. A' Register

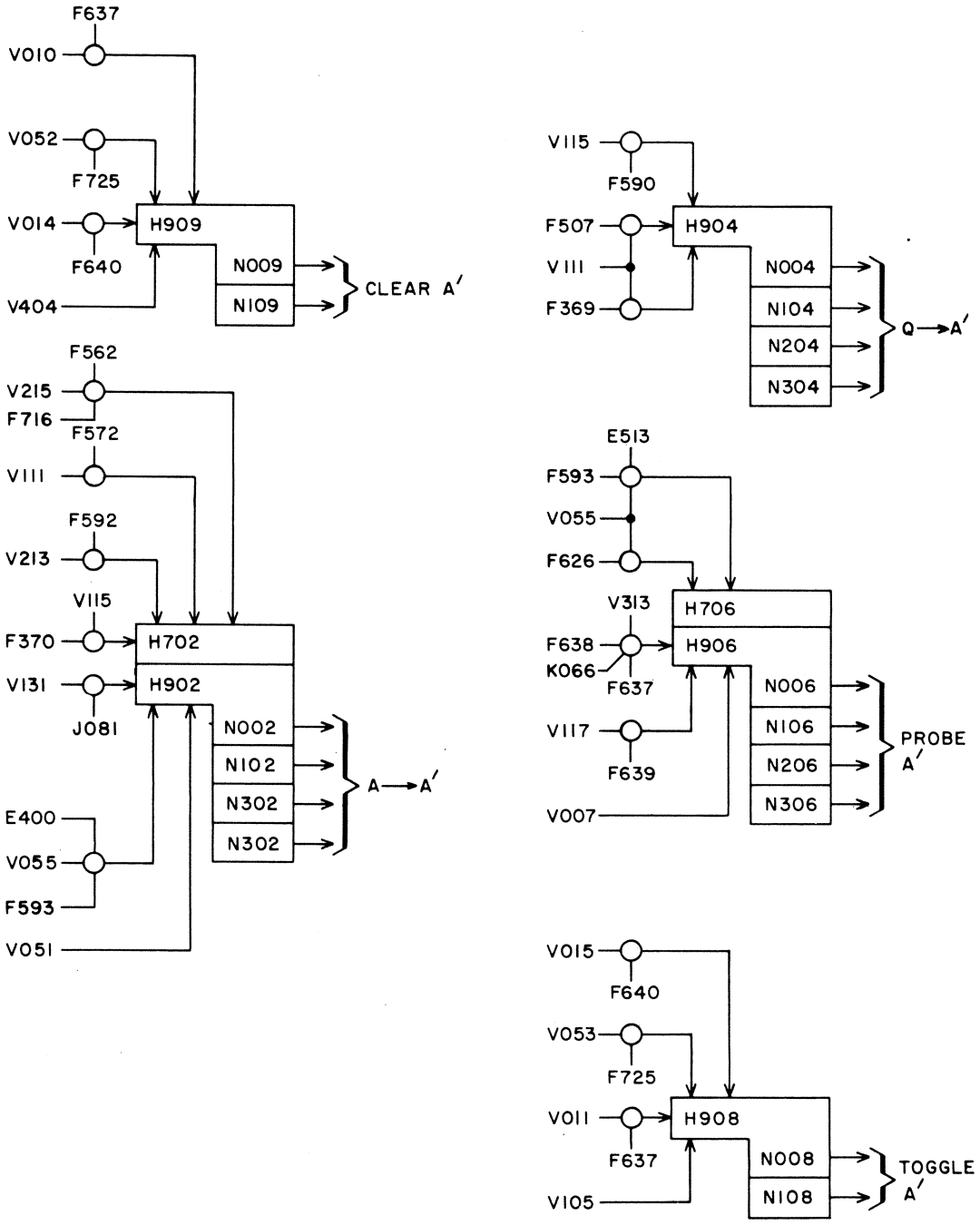


Figure 1-7. A' Register Controls

Clear A': The output of the clear A' control is connected to every stage of A'. When there is a 1 input to H909, the resulting 1 outputs from N-09 reset every stage of A'.

A to A': A 1 output from the A to A' control gates the contents of A into A' by a forced transfer. Whenever any one of the inputs to H702 or H902 is a 1, the A to A' transfer occurs.

Q to A': The Q to A' control gates the contents of the Q register into the A' register by a forced transfer. The Q to A' command occurs when any one of the inputs to H904 is 1.

Toggle A': The toggle A' command is generated as part of the operation of the subtractive adder. When any one of the inputs to H908 is a 1, the toggle A' command is generated. This command sets selected stages of A' as determined by control signals from the subtractive adder.

Probe A': The probe A' command also occurs as part of the operation of the subtractive adder. A 1 input to H706 or H906 produces this command, which complements selected stages of A' as directed by control signals from the subtractive adder.

Auxiliary Arithmetic Register (Q)

The 13-bit Q register assists the A register in performing arithmetic and logical operations. For multiply and divide instructions, the Q register serves as an extension of the A register to form a 26-bit AQ register.

The functional composition and operation of the Q register and its controls are basically the same as those of the A register.

Secondary Auxiliary Arithmetic Register (Q')

The 13-bit Q' register serves as a second rank of the Q register. The Q' register and its controls operate in the same manner as the A' register, except that Q' register has no controls which cause it to function as part of the subtractive adder.

Exchange Register (X)

The 13-bit X register functions as an exchange register for the transfer of data within the Compute Unit. All data being transferred from internal memory passes through the X register. Similarly, data from a Memory Unit, I/O Unit, or normal I/O is stored temporarily in the X register. Data leaving the Compute Unit for a Memory Unit, I/O Unit, or normal I/O is placed in the X register prior to being placed on the appropriate transmission lines.

The X register controls, except set X, are similar to the A register controls. Most of these controls gate data into the X register by a forced transfer, transfer of 1's, or transfer of 0's.

The large number of inputs to the X register necessitates a different method of setting X because there is no input pin available for this function. Thus, the set X control actually disables the feedback from the reset output to the reset input of every stage of X, Figure 1-8. The following discussion assumes no 1 inputs to the X register from any of the other X register controls. When there are 1 inputs to H947 and H949, the resulting 0 outputs disable the feedback path from the reset output to the reset input of every X register flip-flop.

Stage X_{00} is shown in the reset condition. When the set X command occurs, the AND input to X001 is disabled. The output of X001 goes to 1 forcing the output of X000 to 0. Thus, X000/X001 is switched to the set condition.

Stage X120/X121 is shown in the set condition. When the set X command occurs, the AND input to X121 is already disabled by the feedback from X120. Hence, X120/X121 remains set. Therefore, after a set X command occurs, every stage of the X register is in the set condition. When the set X control is not active, the 1 outputs of H947 and H949 permit the flip-flops in X to function normally. After the set X command, a transfer of 0's is executed to gate the contents of another register into X.

Memory Address Register (S)

The 13-bit S register holds the memory address currently being referenced for an instruction, operand, or addressing operation. The address may apply to either internal or external memory as determined by the bank controls. In the 8090 mode, only the lower order 12 bits of S are used. When switching from the 8090 to 8490 mode, bit 00 of the relative bank control is gated to S_{12} (and then to P) to provide correct addressing.

Internal Memory Address Register (S')

When a memory reference is made to internal memory, the current memory address in the S register is placed in the S' register. The S' register provides outputs which condition the address selection logic to reference the correct address. In the 8090 mode, S'_{12} is supplied by B_{00}. In the 8490 mode, S'_{12} is supplied by S_{12}.

Program Address Register (P)

The 13-bit P register contains the memory address of the current instruction. In the 8090 mode of operation, the highest order bit is not used. After execution of an instruction which does not jump program control to another routine, the contents of P is increased by 1 or 2. The P register receives data

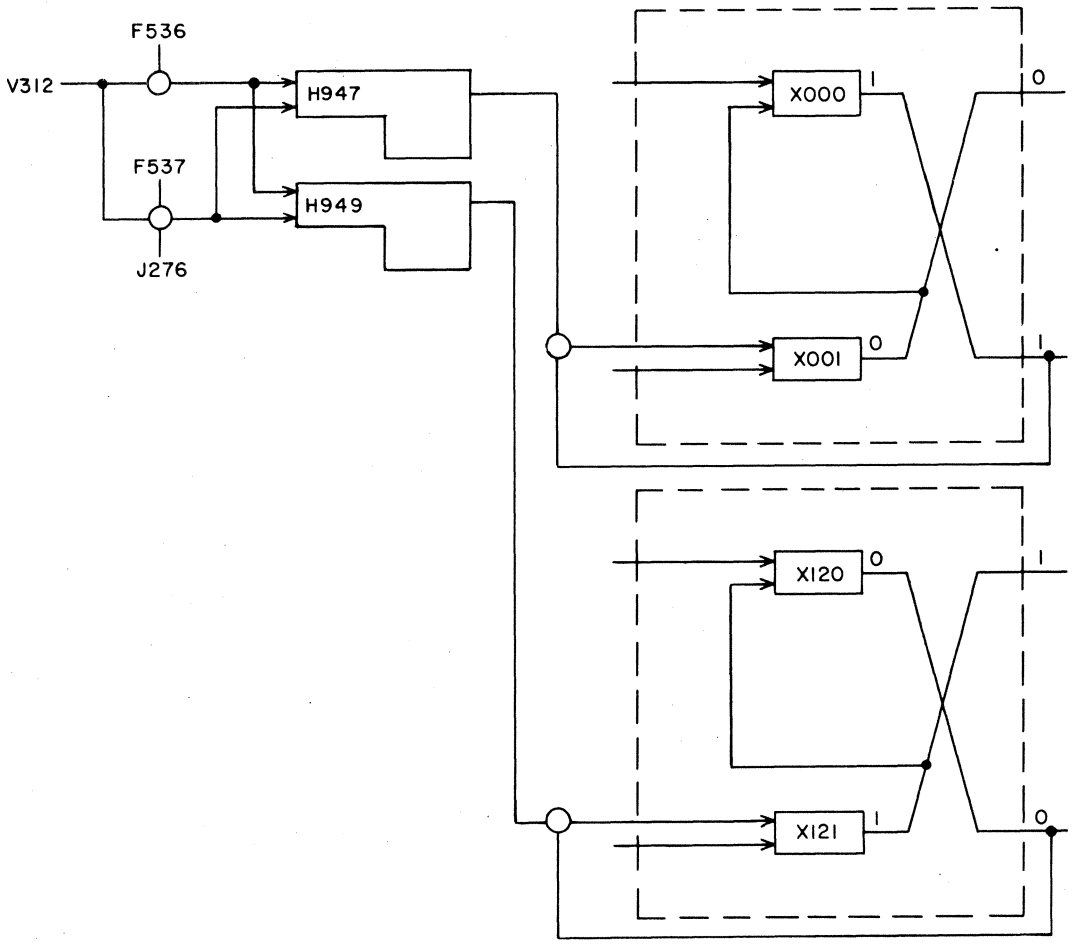


Figure 1-8. Set X Control

only from the S register. The three P register controls operate in a manner similar to the corresponding A register controls.

Function Register (F)

The 13-bit F register holds the instruction currently being executed by the Compute Unit.

Data is transferred directly from memory to the F register. The F register is also affected by set and clear controls, a set-F-to-15_8 control, and a reduce control. The reduce control transfers F' to F in such a manner that the resultant is reduced by 1.

Secondary Function Register (F')

The 5-bit F' register serves as the second rank of the lower order five stages of F. Data is transferred to F' only from F. Controls are provided to clear and set F' for I/O control.

Storage Bank Control Register (B)

Functionally, the 16-bit B register consists of four 4-stage bank controls. These controls operate independently of one another to provide the bank selection for the various addressing modes available to the 8490. Figure 1-9 shows the stages of the B register which are assigned to the respective bank controls.

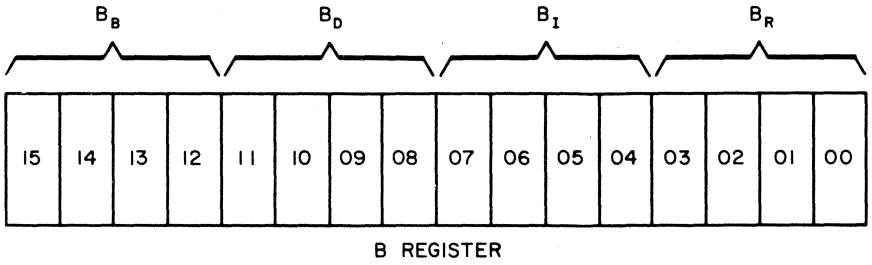


Figure 1-9. Bank Controls in B Register

The B register controls are basically similar to the A register controls. However, some B register controls affect only the four stages assigned to a given bank. These controls are used to set and clear a given bank control.

Memory Restoration Register (Z)

The 14-bit Z register operates with core memory. All data entering or leaving core memory is stored temporarily in the Z register.

Data to be written into core memory is entered into the Z register and then written into the correct location. Data read from core memory is placed in the Z register. After this data has been transferred to another register, the data also is gated from Z back into the same location. Thus, Z permits a memory reference to be nondestructive. The 14th bit of the Z register is a parity bit.

Buffer Data Register (BFR)

The 13-bit BFR holds the data word being transferred to or from memory over the Compute Unit buffer channel. The BFR controls can gate data into the BFR from internal memory, external memory, or the buffer channel

data lines. Data from the BFR can be transferred to the X inverters or placed on the data lines to the external equipment on the Compute Unit buffer channel.

Buffer Entrance Register (BER)

During buffered I/O operations on the Compute Unit channel, the 13-bit BER holds the address to or from which information is being transferred. The contents of this register may be transferred to memory or to the subtractive adder. In the 8090 mode, only the lower order 12 bits are used.

After the word has been buffered, the subtractive adder increases the contents of BER by one. The buffering process continues until the contents of BER and BXR are equal.

Only two controls affect the BER. One control clears the BER; the other control gates the contents of A' to the BER by a transfer of 1's. Whenever the clear BER control is activated, the A' to BER control is activated in sequence.

Buffer Exit Register (BXR)

During buffered I/O operations on the Compute Unit channel, the 13-bit BXR holds the last word address plus 1 for the buffering operation. In the 8090 mode, only the lower order 12 bits are used. The BXR controls are similar to the BER controls.

Error Register (ER)

The error register contains six stages. Each stage represents a different error condition. Generally, after an operation is performed for which a certain type of error could occur, the Compute Unit senses for the error condition. If the error is present, the appropriate flip-flop is set.

The contents of the error register can be transferred through X to A by the ERTA instruction. The output of the error register also conditions the COMPUTER STATUS indicator to display the correct error indication.

MAIN TIMING

A group of control delays are combined in a main timing chain. This ensures that the correct commands are performed at the proper time for a given instruction. Figure 1-10 shows a sample control delay chain.

The control delays in the main timing chain have V--- output terms. The last two digits of the H--- and V--- terms correspond to the phase time of the output of this control delay. In the 8490, one phase time equals 62.5

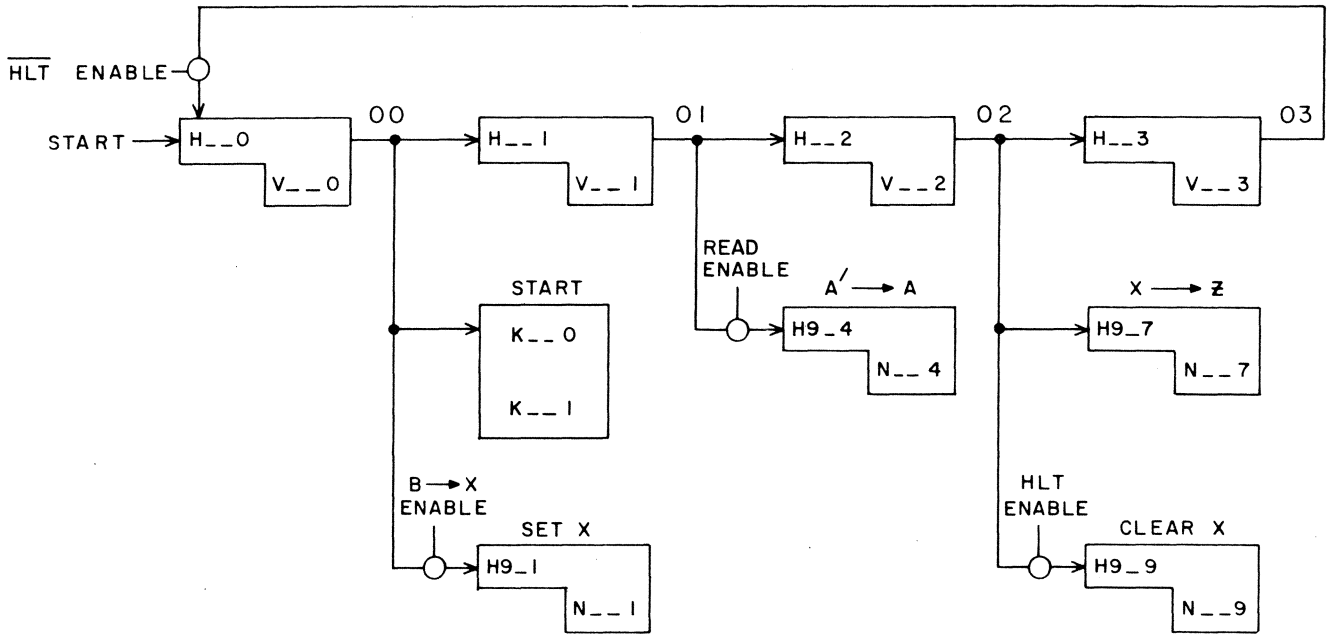


Figure 1-10. Control Delay Chain

nanoseconds, which is equal to the delay introduced between the input and output of a control delay and the length of the pulse.

The outputs of the main timing control delays supply inputs to various other control delays, flip-flops, and inverters. These inputs may be either direct or gated. A direct input produces a function or command unconditionally. A gated input produces a function or command only if the enabling conditions are present.

All of the commands which occur for an instruction form a command timing chart. In these charts, input times are listed for flip-flops and output times are listed for control delays. Thus, K--0/K--1 is set at time 00, but the command represented by H9-1/N--1 occurs at time 01. The last digit in the subject term in a control delay is odd if its output occurs at an odd phase time and even if its output occurs at an even phase time.

At time 03, the output of H--3/V--3 provides a 1 input to H--0/V--0 if the enabling condition is present. Thus, the control delay chain continues to repeat until the enabling condition is removed.

Figure 1-11 illustrates the main timing chain as a block diagram. The start portion is entered whenever it is necessary to establish or change program control. When the computer is started, the start sequence is used to enable the autoload feature if memory has not been previously loaded. The start sequence then loads the starting address in S and P and generates a read instruction signal. RNI is initiated which generates a memory reference. A resume II continues RNI and gates the instruction to F. The F translators then form the gating signal necessary to enable the commands which execute the instruction.

An output from the RNI sequence then initiates the instruction sequence. This instruction sequence consists of one or more cycles. One cycle is performed for each memory reference required. The A, B, and C cycles form the correct address or operand required for the addressing mode of the instruction. The A (if only A cycle is performed), D, and E cycles are performed as required to execute the instruction. Minimally, an instruction might require only an A cycle or an A and D cycle. A complex instruction could require all five cycles. The main cycle sequences are A, AD, ABD, and ABCD. Also used are ADE, ABCE, and ABCDE.

For multiply, divide, and shift instructions which require the use of a shift sequence, the shift sequence is initiated. This sequence generates the proper commands to perform the required shift and add or subtract. This sequence is repeated until the required number of shifts have been performed.

Multiply and divide instructions then enter the end correction sequence. At some time before the end of the instruction sequence, this sequence initiates the RNI sequence.

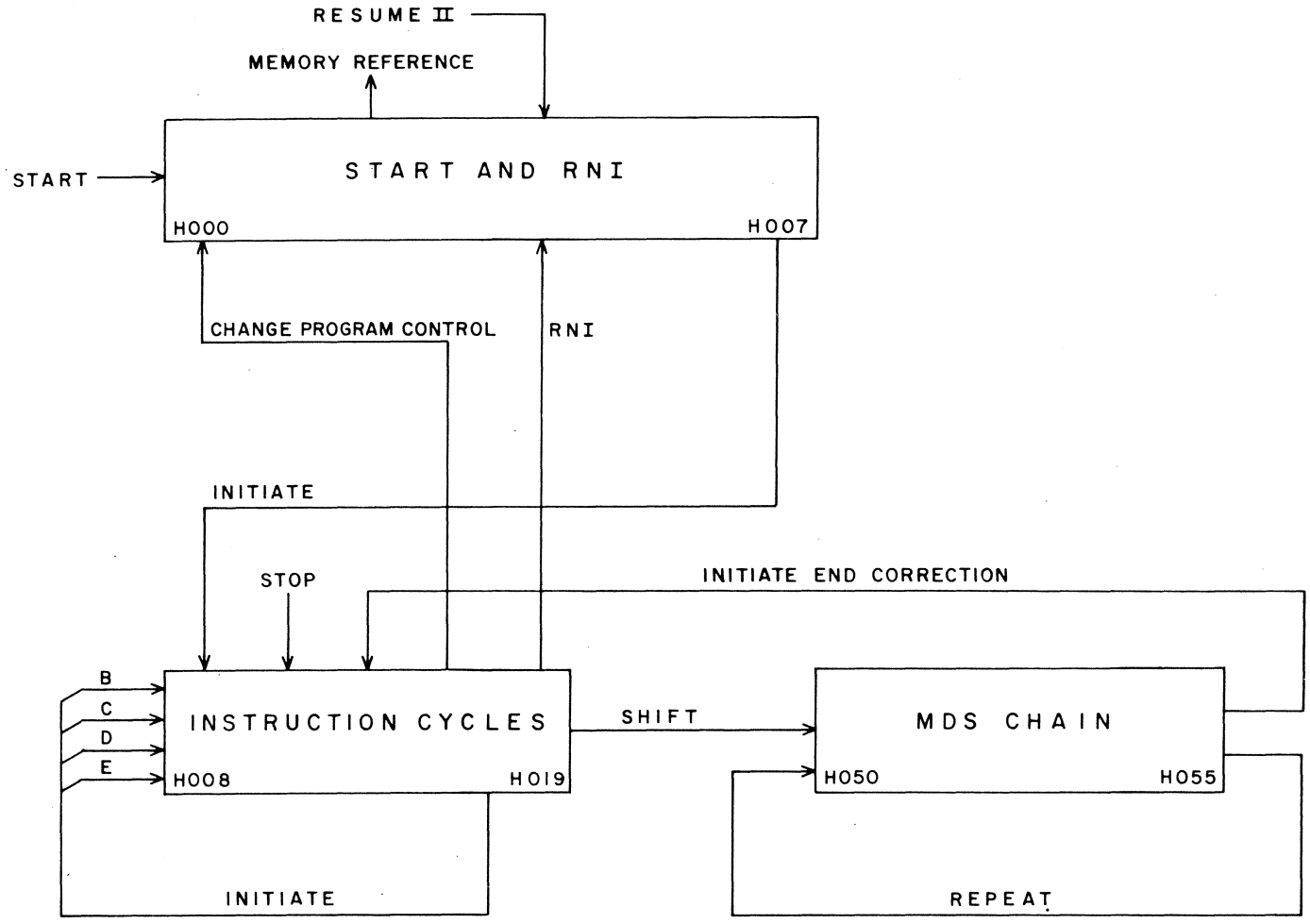


Figure 1-11. Main Timing - Block Diagram

MANUAL CONTROL

The manual controls on the Console are used to stop, start, or condition the operation of the Compute Unit. With the exception of the set and clear controls, most controls set control flip-flops, the outputs of which condition the operation of the Compute Unit.

F TRANSLATION

A network of inverters translates the contents of the F and F' registers. The output signals from these inverters provide the gating which enables the Compute Unit to perform the steps which execute the instruction in the F register.

The first level of inverters translates the contents of a particular stage. Thus, F013 has a 1 output when F_{01} is a 1, and F012 has a 1 output when F_{01} is a 0, Figure 1-12. For functional purposes, the outputs of the first level inverters are combined in octal digits. The outputs of the higher level inverters are expressed as combinations of octal digits or instruction mnemonics. The condition given for an F term is present when that F term has a 1 output. The output of an inverter represents the Boolean inversion of its input.

Inverter F221 senses when the lowest order octal digit of F is not a 1. When the lowest order three stages of F contain 001, the AND input to F221 is satisfied and a 0 output results. This 0 produces a 1 output from F831, which represents X1 (the X is the other octal digit of E). For any other combination of bits in the lower order three stages, the AND input to F221 is disabled and the output of F221 is a 1.

Inverters F370 and F456 translate the instruction ATE. When F contains 00105, all of the OR inputs to F370 are 0. The resultant 1 output produces a 0 output from F456. Therefore, F370 equals ATE, and F456 equals $\overline{\text{ATE}}$.

The output of an inverter may represent several instructions. For example, F428 and F430 are combined in an AND input to F404. When the F register contains the code for EXC, EXF, or EXCY, the AND is disabled and the output of F404 is 1.

ADDER

The adder is a device consisting of the subtractive adder and the I and U inverters, which is used to find the sum of two operands.

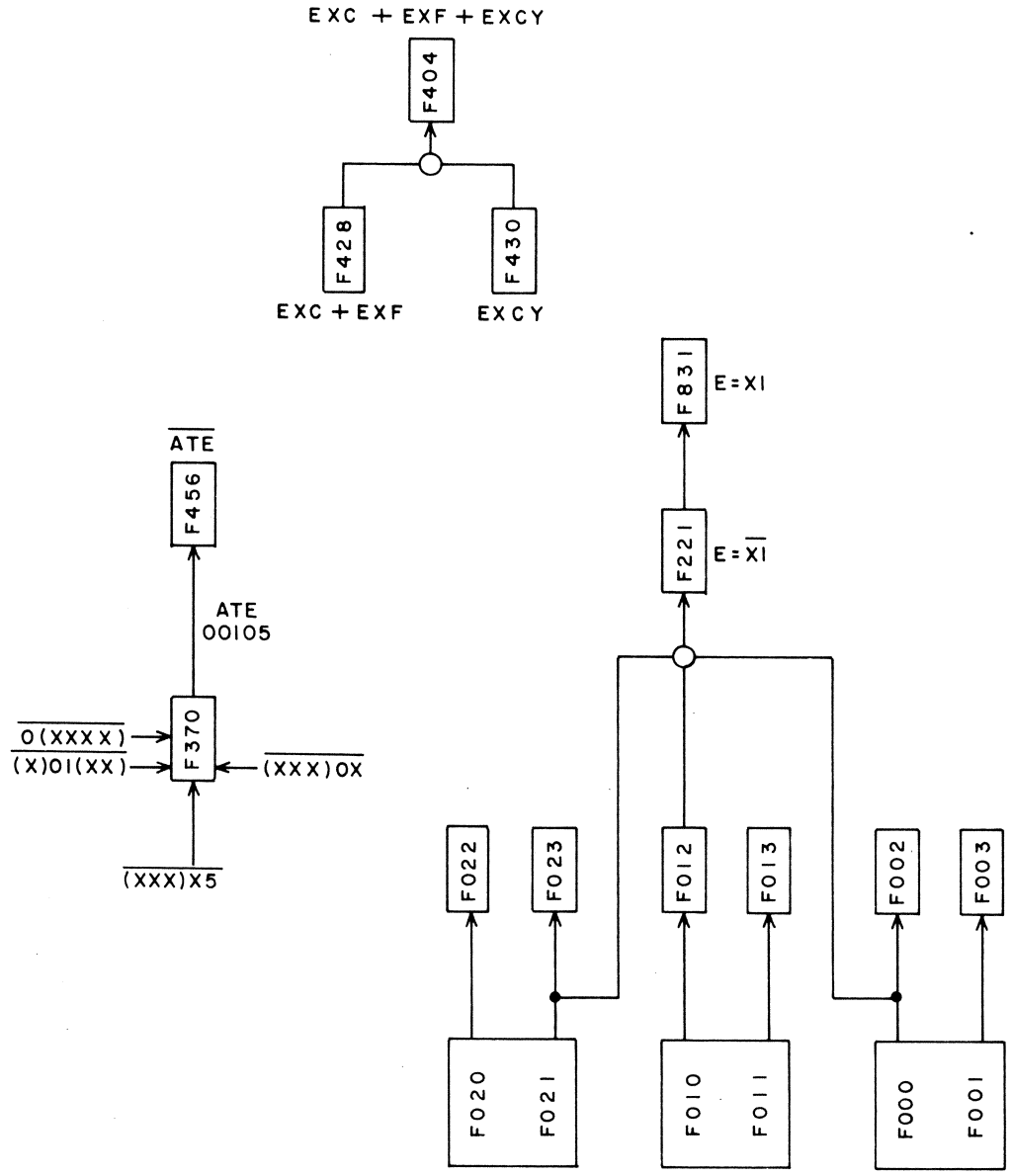


Figure 1-12. Function Translation

Theory of the Adder

The internal arithmetic is based on subtraction. Addition is performed by subtracting the complement of the addend from the augend. The adder recognizes the borrow signals generated by one's complement subtraction. The theory of the subtractive adder is the recogniation of whether or not a borrow was generated.

For addition, the complements of the actual operands are gated from the reset side of the flip-flops in the A and X registers to the I and U inverters. For subtraction, the complement of A and the actual value of X are gated to the I and U inverters. The I and U inverters then invert their inputs. In this manner the proper operands are gated into the base of the subtractive adder. At this point the two operands are considered as additive operands.

There are four possible states in the bit-by-bit subtraction of a one-bit minuend and subtrahend.

Minuend	1	0	1	0
Subtrahend	-1	-0	-0	-1
Difference	0	0	1	1

In the preceding examples there is only one case in which the minuend is unable to satisfy the subtrahend. This happens when one is subtracted from zero. It is implicit from arithmetic that a borrow must be made from the next higher order stage. There are two cases in which the difference is zero. This means, after the initial bit-by-bit subtraction, that stage is unable to satisfy a borrow made on it by some lower order stage and must pass the borrow on to the next higher order position. These cases exist whenever 1 is subtracted from 1, or when 0 is subtracted from 0. The act of transferring an unsatisfied borrow to the next higher stage is termed an "enable". An enable is generated whenever the bit in the minuend and the bit in the subtrahend are the same. In the remaining case, when 0 is subtracted from 1, the minuend is able to satisfy the subtrahend and is also able to satisfy a borrow, if necessary.

Stage-Generated Signal: The stage-generated signal is the lowest level in the subtractive adder. It is at this level that the borrow or enable signals are determined for each bit position (stage) of the operand. There are 13 stages in the subtractive adder, one stage for every flip-flop in the A or X register. The stages are grouped into 3-bit groups. The highest order bit (bit 12) is included in the last group of the adder. The following rules can be formed with respect to the operand inputs to the adder since the adder effectively complements one of these operands and subtracts:

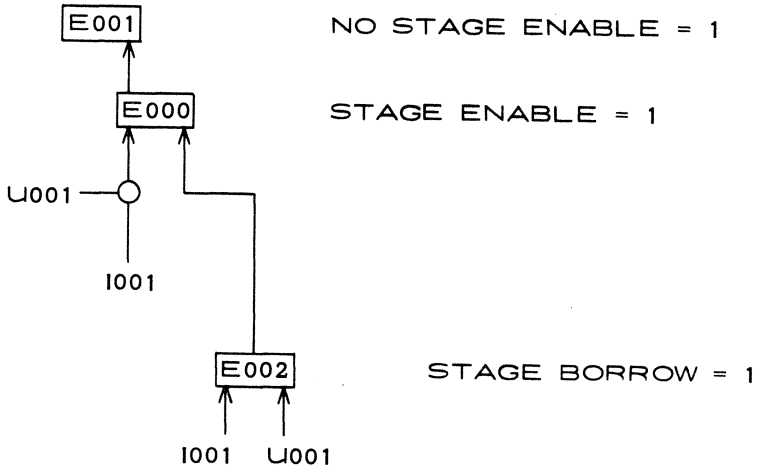
1. When corresponding bits in the two operands are both zero, a borrow is generated to the next higher order stage.

2. When corresponding bits in the two operands are unlike in value, that bit position is enabled.

3. When corresponding bits in the two operands have like values, that bit position is not enabled.

The preceding rules are determined at the stage level and are used throughout the remainder of the subtractive adder.

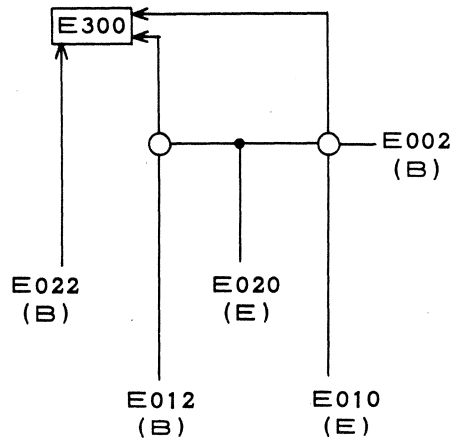
The functions, as given in the following illustration, are for the lowest order bit in the subtractive adder. A 1 output from each of the stages satisfies one of the previously stated rules.



If unlike signals (0 and 1) are gated to E002, the resulting output is 0. A 0 output from E002 does not satisfy the stage borrow condition. At the same time, these signals are gated, via an AND gate, to E000. The 0 outputs from U001 or I001 and E002 produce a 1 output from E000. A 1 output indicates the stage enable condition. If both the U001 and I001 inputs are 0, the output from E002 is 1. The 1 output indicates a stage borrow condition. If both inputs are 1, E000 and E002 both have 0 outputs. The 0 output from E000 produces a 1 output from E001. This output indicates the no stage enable condition.

Group Borrow Signal: A group borrow signal is generated whenever a higher order stage (if any) in an octal group cannot satisfy a borrow generated within that group. This signal passes the borrow to the next higher order group. The conditions for creating a group borrow are shown in the following example. The example is for the lowest order group in the subtractive adder.

GROUP BORROW = 0



A group borrow is generated when the output of E300 is 0. The three inputs to E300 are as follows:

> NOTE: The outputs of stage enables and stage borrows are 1's when the condition they represent is present.

1. The right-most input to E300 is satisfied when the lower order stage (E002) generates a borrow and the next two stages (E010 and E020) are enabled.

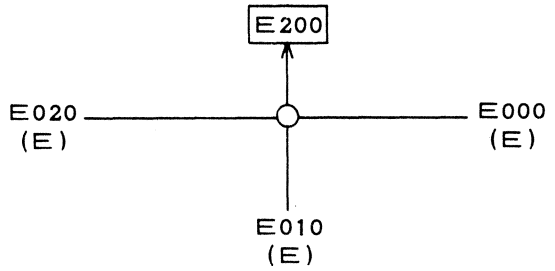
2. The middle input to E300 is satisfied when the middle stage (E012) generates a borrow and the higher order stage (E020) is enabled.

3. The left-most input to E300 is a 1 when the higher order stage (E022) generates a borrow.

Group Enable Signal: If every stage within a group is enabled, a group enable signal is generated. The following example is for the lowest order group enable in the subtractive adder.

The preceding rules apply, regardless of the number of stages or groups involved, for a subtractive adder.

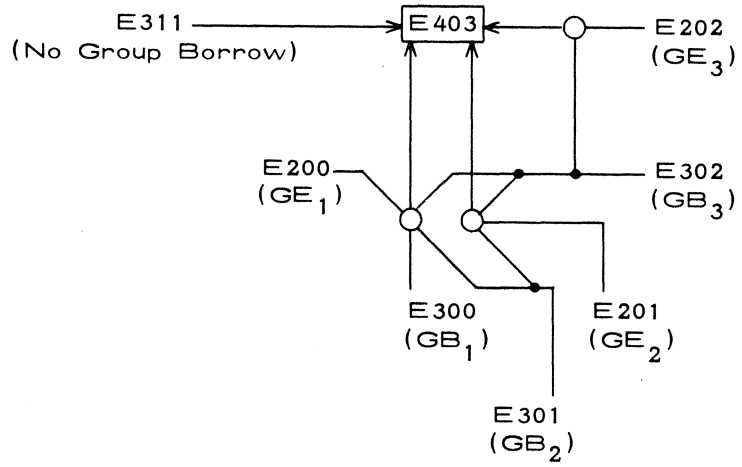
GROUP ENABLE = 0



Group Borrow Input: A group borrow input inverter is associated with each of the four groups comprising the adder. A group borrow input is present if a borrow is generated in an adjacent lower order group, or in some remote group if accompanied by intervening group enable signals.

The following example is for the highest order group in the subtractive adder:

GROUP BORROW INPUT = 1



Because of the inverter logic used in the adder, the group borrow input is present when all inputs are 0. This means that at least one of the terms in the AND gates must be 0 in the preceding example. The letters stand for group borrows (GB) and group enables (GE) generated from the lower levels of the adder. Outputs from group enables and group borrows are 0 if they exist. The subscript number refers to the group in which each was generated.

E311 must have a 0 output, indicating there is one or more group borrows, or the group borrow input logic is disabled.

The following four possible conditions produce a group borrow input to E403 if E311 is 0.

1. The highest order group generates a borrow and all lower order groups are enabled.

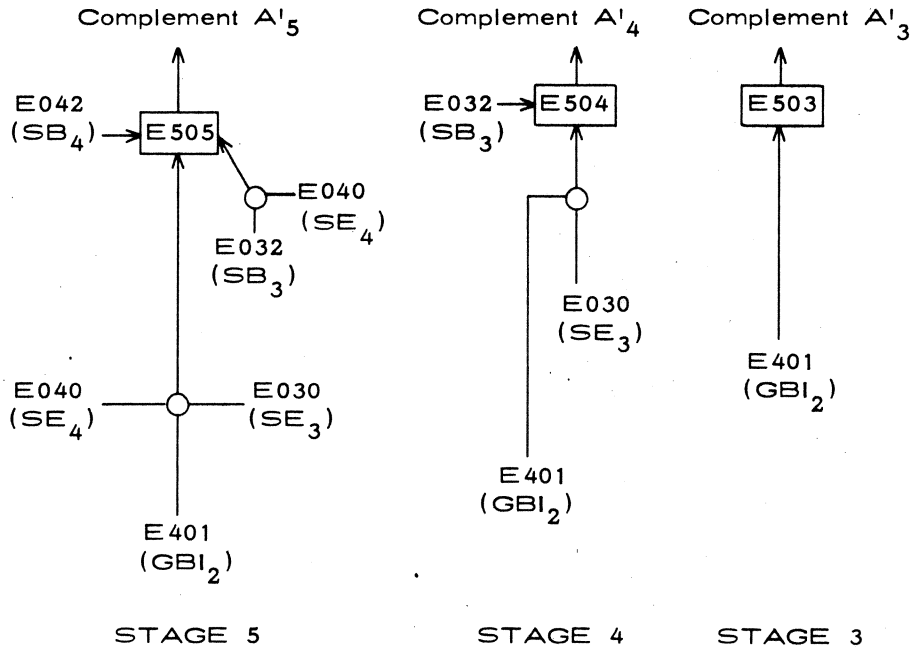
2. There is a group borrow generated from the next lower order group (E302).

3. The second group (E301) generates a borrow and the third group (E202) is enabled.

4. The lowest order group (E300) generates a borrow and the second (E201) and third (E202) groups are enabled.

No Stage Borrow Input: There is a no stage borrow input inverter ($\overline{SBI}$) for every bit in the adder. Outputs from the no stage borrow input inverters are used to complement the corresponding A' register flip-flops when no borrow exists. The following example illustrates the three $\overline{SBI}$ terms for the second octal group (stages 3, 4, and 5) of the adder.

NO STAGE BORROW INPUT = 1



The symbols represent stage enables (SE), stage borrows (SB), and group borrow inputs (GBI). The subscript numbers represent the stage number in which each was generated.

A 1 output, which indicates no stage borrow input, is present except when one of the inputs to an inverter is a 1. One of the inputs is satisfied when a stage borrow condition is present. Thus, E503 has a 0 output when E401 is 1, which indicates a group borrow for group 1 input. Similarly, E504 has a 0 output when E032 is a 1 or E030 and E401 are both 1's. Inverter E505 has a 0 output when one of the following conditions is present:

1. E042 is a 1.
2. E040, E401, and E030 are 1's.
3. E032 and E040 are 1's.

Adder Operation

There are three signals used in conjunction with the stage borrow and stage enable signals to set the final sum in the A' register. The order of the operation and purposes are as follows:

1. Clear — The first of these signals resets every stage of the A' register.
2. Toggle — This signal places each stage in the condition that results for a given pair of inputs as if there were a borrow from that stage. The toggle signal sets the A' register flip-flops if there is an enable signal present in that stage. If there is no enable signal present in that stage, the A' register is left in the reset stage.
3. Probe — This signal complements each stage from which there actually was a no borrow. If there was a borrow, the A' register is not changed by the probe signal.

It has been previously stated that the internal arithmetic of the 8491 is based on subtraction. This is true only to the degree that the adder recognizes borrow and enable signals that are generated at the stage level. Addition was defined as the subtracting of the complement of the addend from the augend. The operands are considered to be subtractive operands for the purposes of defining borrows and enables. The adder determines which signal was generated according to the rules formulated for the stage generated signals. The following problem is an example of how the signals are determined:

Addition is performed as:

A =	1	1 1 1	0 0 1	0 1 0	1 0 0	=	-653_8
X =	1	1 1 1	0 1 0	0 0 1	0 1 1	=	(+)	-564_8
	1	1 1 0	0 1 1	0 1 1	1 1 1			
					+ 1			
	1	1 1 0	0 1 1	1 0 0	0 0 0	=	-1437_8

Complementing X and subtracting produces:

A =	1	1 1 1	0 0 1	0 1 0	1 0 0		
X =	-0	0 0 0	1 0 1	1 1 0	1 0 0		
	1	1 1 0	0 1 1	1 0 0	0 0 0	=	-1437_8

Figure 1-13 illustrates the total operation of the preceding problem in the subtractive adder. The order of operation is from bottom to top, the same way it appears on the logic diagram. The inverter number is noted if it satisfies the condition.

Bit numbers 3, 4, and 5 are typical stages in the subtractive adder. These stages make up the second octal group. All other groups have similar logic associated with them and are not discussed.

For the purpose of recognizing borrow and enable signals, inverters have been arranged in such a manner that 1 outputs satisfy the stage borrow, stage enable, and no stage enable condition. Only one condition results from any two inputs.

Stage 3 is enabled because the inputs are unlike in value. The inputs from I031 to U031 form an AND gate to E030. Unlike values result in a 1 output from E030 satisfying the stage enable condition. Also, if the inputs from I021 and U021 are gated to E032, they also result in a 0 input to E030.

Stage 4 is also enabled. Unlike values, from I041 and U041, gated to E040 and E042 result in a 1 output from E040.

Stage 5 generates a stage borrow according to the definition. The 0 inputs, from I051 and U051, result in a 1 output from E052 satisfying the stage borrow condition. The 1 output from E052 forces E050 to 0.

By definition, a group is enabled only if all stages are enabled. E201 does not satisfy the condition (has a 1 output) because E050 is not enabled.

STAGE NO.	12	11	10	9	8	7	6	5	4	3	2	1	0
TOTAL	1	1	1	0	0	1	1	1	0	0	0	0	0
PROBE	A124	A114	A104					A054	A045	A035	A025	A015	A005
TOGGLE						A074	A064		A044	A034	A024	A014	A004
CLEAR	Set all stages of A' equal to zero (reset FF.)												
NO STAGE BORROW INPUT	E512	E511	E510					E505	E504	E503	E502	E501	E500
GROUP BORROW INPUT		E403			E402								
GROUP BORROW *					E302			E301					
GROUP ENABLE *											E200		
NO STAGE ENABLE	E121	E111	E101	E091	E081			E051					
STAGE ENABLE						E070	E060		E040	E030	E020	E010	E000
STAGE BORROW					E082			E052					
I Outputs	1	1	1	1	0	0	1	0	1	0	1	0	0
U Outputs	1	1	1	1	0	1	0	0	0	1	0	1	1
STAGE NO.	12	11	10	9	8	7	6	5	4	3	2	1	0

NOTES: 1. The elements shown produce 1 outputs except where otherwise indicated.
2. * These symbols represent 1 inputs, not the state of the outputs.

Figure 1-13. Subtractive Adder

The 0 output from E050 breaks the AND gate formed by E030, E040, and E050.

Because stage 5 (the highest order stage in the group) generates a borrow, this group cannot satisfy the borrow and must pass it on to the next higher order group. The 1 input to E301 from E052 satisfies the group borrow condition.

The outputs from the group borrows form an AND gate to determine if one or more group borrows exist. E300 and E303 do not generate borrows. The AND gate is broken, resulting in a 0 output from E311.

The group borrow input determines if a borrow exists. E401, the group borrow input inverter, has a 0 output, which does not satisfy the condition; therefore, no borrow exists. The group borrow input is not realized because E203 is not enabled and E300 is not generating a group borrow.

A 1 output from the no stage borrow input inverters satisfies the condition that no borrow exists. E503 has a 1 output because E401 has a 0 output. E504 has a 1 output because E032 does not generate a borrow and E401 breaks the AND gate. E505 has a 1 output because all inputs are 0. There are no borrows generated in either E032 or E042 (breaks the AND gate). The other AND gate is not satisfied because E401 has a 0 output.

All flip-flops in the A' register are reset to 0 by the clear signal. The toggle signal sets all flip-flops to 1 if an enable signal is present in that stage. A034/A035 is set to 1 because E030 is enabled. A044/A045 sets because E040 is enabled. E050 is not enabled; therefore, there is no change in A054/A055 (left in the 0 state).

Stages 3, 4, and 5 are complemented by the probe signal because there is no borrow. The probe signal resets (complements) A034/A035 because there is no borrow (E503) and E030 is enabled. A044/A045 is reset because there is no borrow (E504) and E040 is enabled. A054/A055 is set because there is no borrow (E505) and E051 indicates a no enable.

MEMORY

Each 8491 Compute Unit contains a memory section of 8,192 storage locations; this is the internal memory. Memory sections located in 8492 Memory Units are external memories. The physical arrangement of the core storage and method of readout, write-in, and address selection of the internal memory are practically identical to an external memory. The major differences lie in the access channels. The 8491 memory section cannot be used by other 8490 units whereas the 8492 memory may be used by any combination of 8491 Compute or 8495 Input/Output Units that totals three or less.

Therefore, the 8491 memory section does not need a scanning circuit or a line receiver and transmitter circuit with its associated control and translation circuitry, Figure 1-14.

The 8490 Computer may be operated in either the 8090 mode or the 8490 mode. The 8090 mode may be manually selected by depressing the 12 pushbutton which illuminates on the Console. The 8490 mode is the normal mode of operation during which the 12 pushbutton is not illuminated. In the 8090 mode, addressing is made directly to one of two internal or one of a maximum of 14 external memory banks (4,096 storage locations); whereas, in the 8490 mode, addressing is made to one internal or one of a maximum of seven external Memory Units. Selection of the odd or even bank in one of the seven external units depends on the odd or even bit 12. A 16-bit address in the 8090 mode consists of 4 bank address bits and 12 core address bits. The bank address bits are transferred between the B register and the select circuitry in the memory banks, and the core address bits are transferred between the S and S' registers. A 16-bit address in the 8490 mode consists of 3 memory unit address bits, 1 bank designator bit, and 12 core address bits.

A maximum of 14 bits can be stored in a given address. The data word or an instruction word is comprised of 13 bits. The 14th bit is a parity bit. The parity bit allows a malfunction of the memory to be detected.

The storage function within a memory section is controlled by a delay line for timing, and Z and S' registers to directly affect a memory reference to a specific location. Control of readout and write-in within the memory section is accomplished by pulsing the delay line once each time a memory reference is made.

The control section of the 8491 places a memory request, a select code, and a read, write, or partial-write command on the lines to all accessible Memory Units, including the internal memory. When the internal memory senses its select code and request, the active flip-flop sets, causing the following events:

1. Enabling of a transfer of the address from S to S'.

2. Setting of the busy flip-flop to lock out other memory references for the remainder of the cycle.

3. Setting of the gate, read drive, and discharge drive flip-flops to enable read currents to flow through the selected X and Y drive lines of the memory stack.

4. Starting of a pulse down the delay line to time each function in the memory reference cycle.

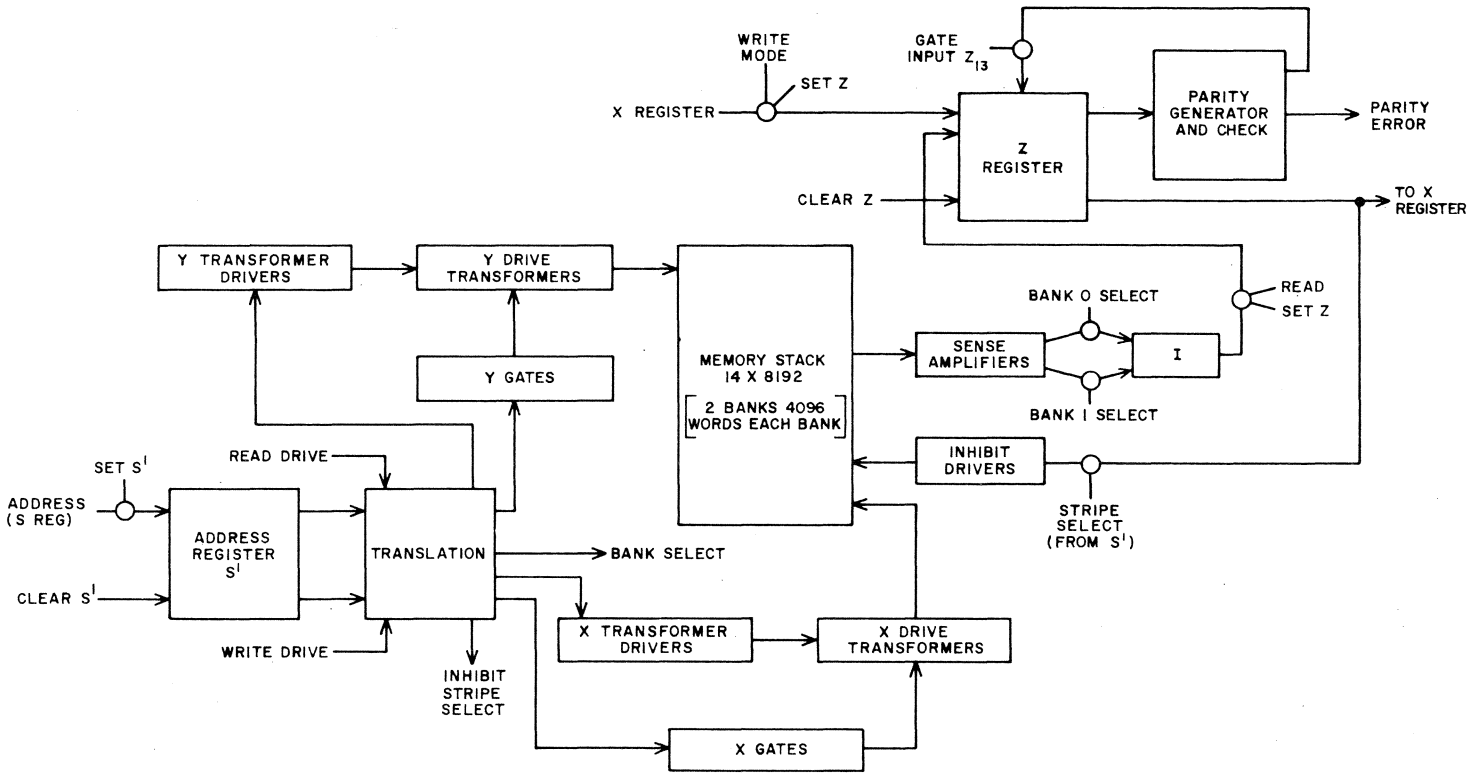


Figure 1-14A. Internal Memory- Block Diagram

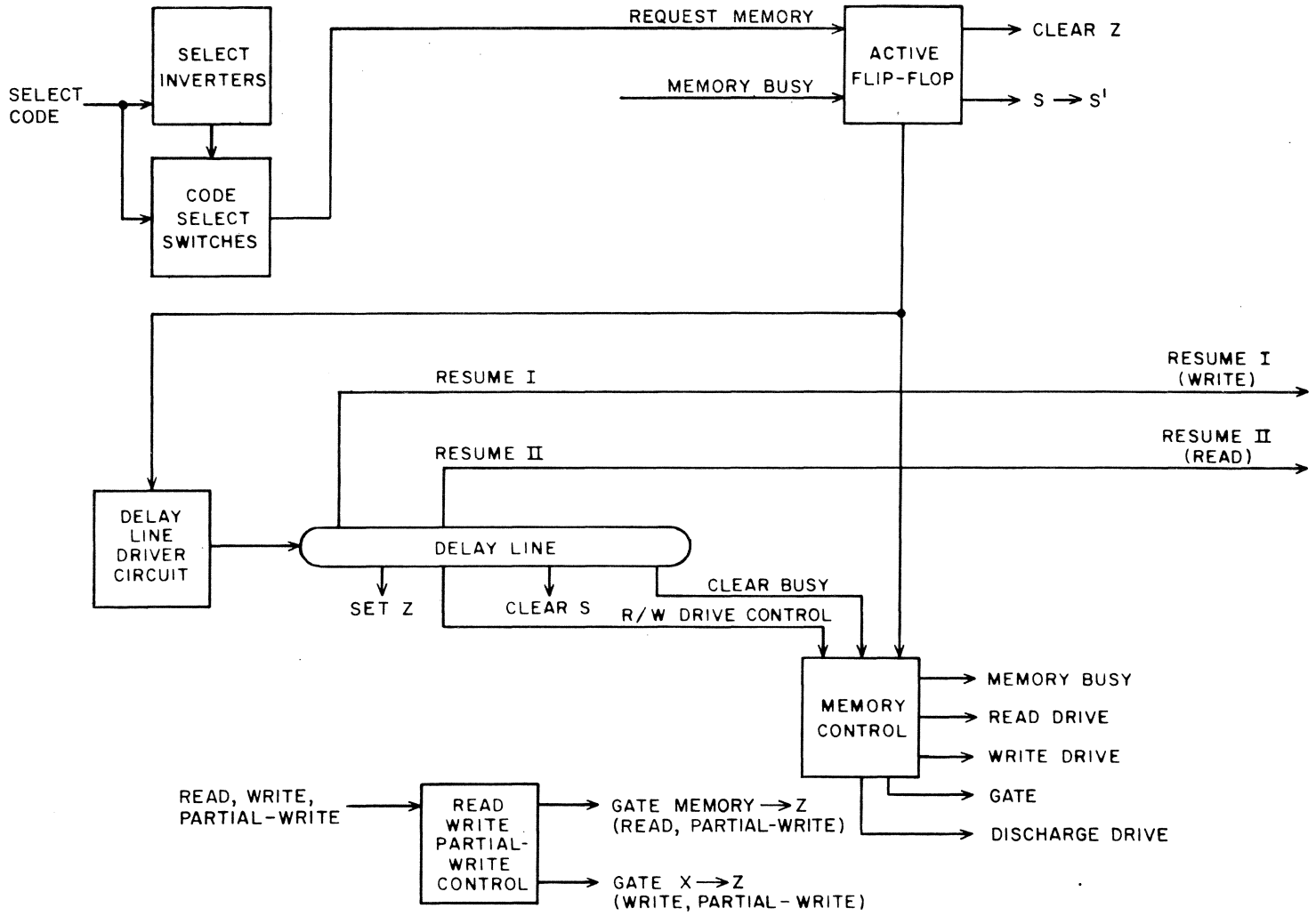


Figure 1-14B. Internal Memory - Block Diagram (Control)

5. Clearing of the Z register in preparation for a transfer of 1's.

A mode command places the memory section in the write, read, or partial-write mode of operation.

In the write mode, the control section places data for a specific address into the X register. When the write gate is enabled, the data is transferred into the Z register of the memory section and stored in the core memory during the write portion of the memory reference.

In the read mode, the data from the memory address selected by the S' register appears on the outputs of the sense amplifiers during the read portion of the memory reference. When the read transfer occurs, the data is transferred into the Z register of the memory section. The output of the memory section Z register is then gated to the computer. The data word read from memory during the read portion of the memory reference is restored in memory during the write portion of the memory reference cycle.

In the partial-write mode, both the read and write functions are employed in one memory cycle. The upper 7 bits of the 13-bit word are processed in the read mode, and the lower 6 bits plus parity are processed in the write mode. The result is that the lower six bits of the word are changed in the partial-write mode while the upper seven bits are not affected.

By the end of the cycle, the active and busy flip-flops are cleared, the S' register is cleared, and the memory section is ready to respond to the next memory reference.

Selection and Start of Cycle

The 8491 control section starts a memory reference by placing the internal memory select code on the inputs to the translation inverters J800, J801, and J802. The select code switches, S800 through S802, are associated with the input translation inverters to use or bypass the inverters. The setting of these switches determines the 3-bit selection code to enable the internal memory. The switches and inverters are connected so that the correct selection code places enabling 1's on three inputs of the 4-input AND gate at the set side of the active flip-flop K800/K801. The busy flip-flop K802/K803 was reset during the end of the preceding cycle; its set output and the memory request pulse from the reset output of the memory request flip-flop K212/K213 place enabling 0's on the inputs to J804. The 1 output of J804 combines with the select code switches to set active flip-flop K800/K801, Figure 1-15. The 1 output of J804 can be delayed 1 microsecond by placing D105 in the logic using switch S900. The lower memory request repetition rate provided by the 1-microsecond delay is a maintenance provision.

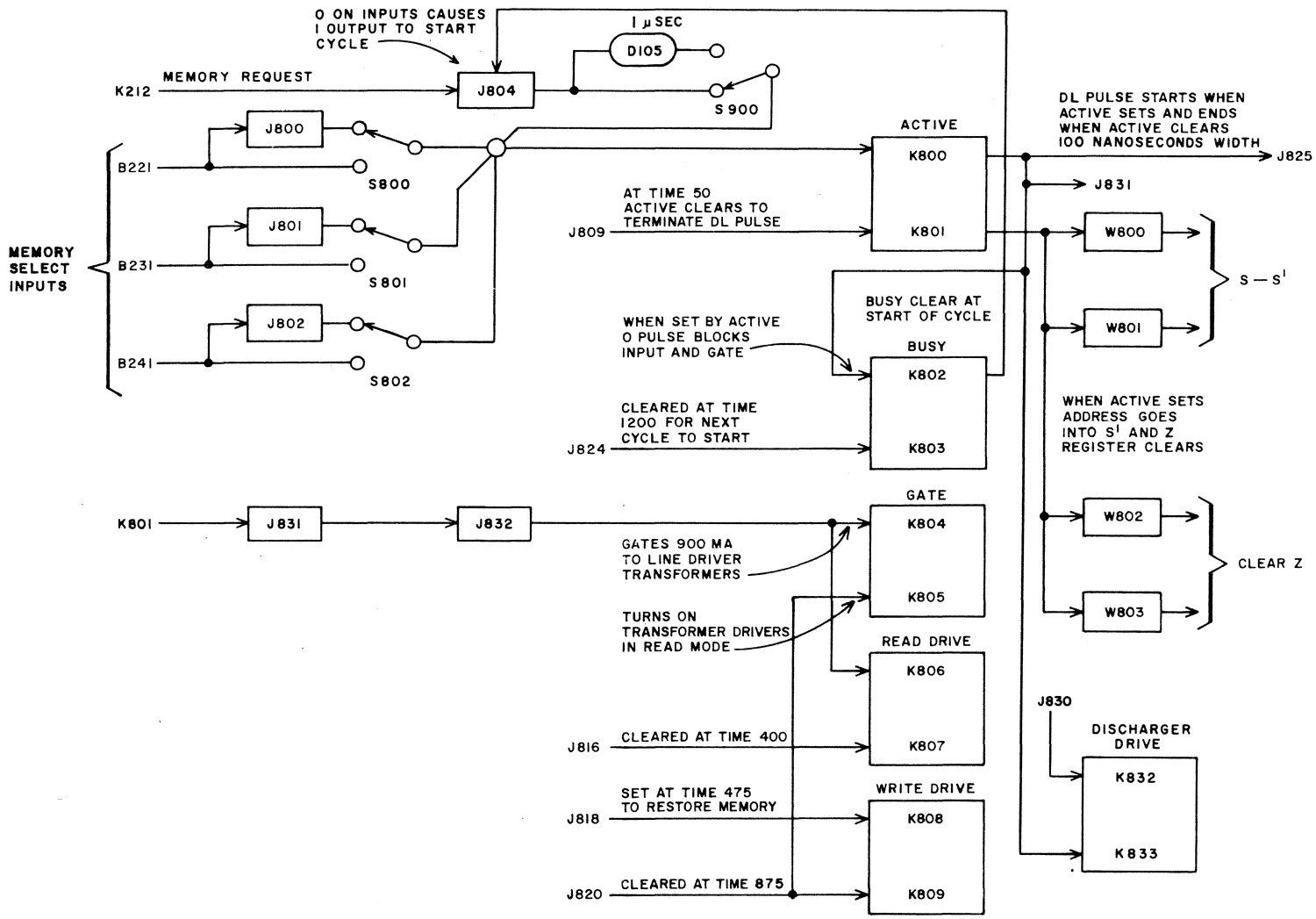


Figure 1-15. Start of Cycle Circuit

The set output of K800/K801 causes the following four events:

1. The 1 output is inverted through J825 to start a 0 pulse down the delay line. The delay line is normally held at a logic 1. When the output of J825 occurs, this 0 pulse is started down the delay line. When this 0 pulse is picked off the delay line by emitter-follower E902, the resulting 1 output of J809 clears the active flip-flop K800/K801. The set output of K800/K801 is inverted through J825 to place a 1 on the input of the delay line. This establishes the width of the delay line pulse. The 0 pulse is now about 90 to 100 nanoseconds wide and travels the length of the delay line in about 1200 nanoseconds. As this 0 pulse travels down the delay line, it is sensed by emitter-followers tapped into the line at positions corresponding to time points between 0 and 1200 nanoseconds. The busy, gate, and read-drive flip-flops remain set until they receive clear pulses timed by the delay line later in the cycle.

2. The 1 output sets busy flip-flop K802/K803. The set output of the busy flip-flop blocks the OR gate input at J804, thereby allowing the active flip-flop to be cleared. If the busy flip-flop did not block the OR gate input to J804, the 0 pulse would be as wide as the length of the delay line. The active flip-flop must be cleared and remain cleared throughout the remaining cycle to establish the 100-nanosecond width of the 0 pulse on the delay lines.

3. The 1 output, through inverters J831 and J832, sets gate flip-flop K804/K805. The 1 output of K804/K805 is inverted placing an enabling 0 on the inputs of the 900-milliampere gates for the X and Y drive. K832/K833 is reset to place a disabling 1 on the inputs to the transformer dischargers for the X and Y drive.

4. The 1 output, through inverters J831 and J832, sets read-drive flip-flop K806/K807. The 1 output of K806/K807 is inverted through E820, E822, E823, E830, E832, and E833 to enable transformer drivers along both axes of the memory stack. These transformer drivers switch the gated current through the line-driver transformers in a direction to switch selected cores from a 1 to 0.

The reset output of K800/K801 causes the following events:

1. The 0 output is inverted through W800 and W801 to cause a transfer of 1's of the address word from the S to S' registers. As a result of the S to S' register transfer, the 0 and 1 output configuration of the S' register is applied to the transformer drivers and 900-milliampere gates to turn on selected line-driver transformers to switch the cores. The current pulses from the switched cores are amplified in the sense amplifiers to enable the inputs of the I inverters. The S

to S' transfer of bit 12 satisfies either the bank 00 or bank 01 AND gate inputs to the I inverters and a transfer of 1's occurs in the I inverters of the selected bank. The cores containing 1's are switched and these 1's appear on the outputs of the I inverters. Cores containing 0's are not switched and the corresponding I inverter remains with a 0 on its output.

2. The 0 output is inverted through W802 and W803 to clear the Z register flip-flops. This prepares the Z register for a transfer of 1's from the I inverters or from the X register depending on the mode of read, write, or partial write.

Mode Selection: When the control section makes a memory reference to the memory section of the 8490 Computer, the reference is for a read, write, or partial-write operation, Figure 1-16. The mode of operation is determined by setting one of the following flip-flops:

1. Read flip-flop K810/K811 for a read mode.

2. Write flip-flop K812/K813 for a write mode.

3. Partial-write flip-flop K814/K815 for reading the upper seven bits and writing the lower six bits of a data word.

Read Mode: A read command is placed on the input control line to the AND gate of the read mode select flip-flop by the control section. The read command combines with the 1 output of J810 to set read flip-flop K810/K811. The 0 output of K810/K811 places an enabling 0 on one of the inputs of J814 and J815. At time 350 a satisfying 0 is placed on the other input of J814 and J815. The resulting 1 output of J814 and J815 satisfies the AND gate inputs to the Z register from the I inverters. A transfer of 1's occurs from I to Z, thereby placing the contents of memory for the selected address in the Z register. At this time the data in core memory at the selected address is destroyed since the memory cores were all switched to 0's during the address selection. When the I to Z transfer occurs, the output of the Z register appears on the AND gate inputs to the X register. Since this is a read operation, the data is subsequently gated into the X register by the control function of the computer. The 0's on the mode select lines leave the write and partial-write flip-flops in a clear status. These flip-flops were cleared during the preceding cycle by the 1 output of J819 at time 900. The 1 output of the write and partial-write flip-flops maintains a 0 on the outputs of J811 and J812.

Write Mode: The control section places the input control line to the AND gate of the write mode select flip-flop. The write command combines with the 1 output of J810 to set write flip-flop K812/K813. The reset output of K812/K813 enables one of the two inputs to J812. At time 150 the 0 output of emitter-follower E906 places a satisfying 0 on the other input of J812. The 1 output of J812 enables the AND gate inputs for bits 6 through 12 of the Z

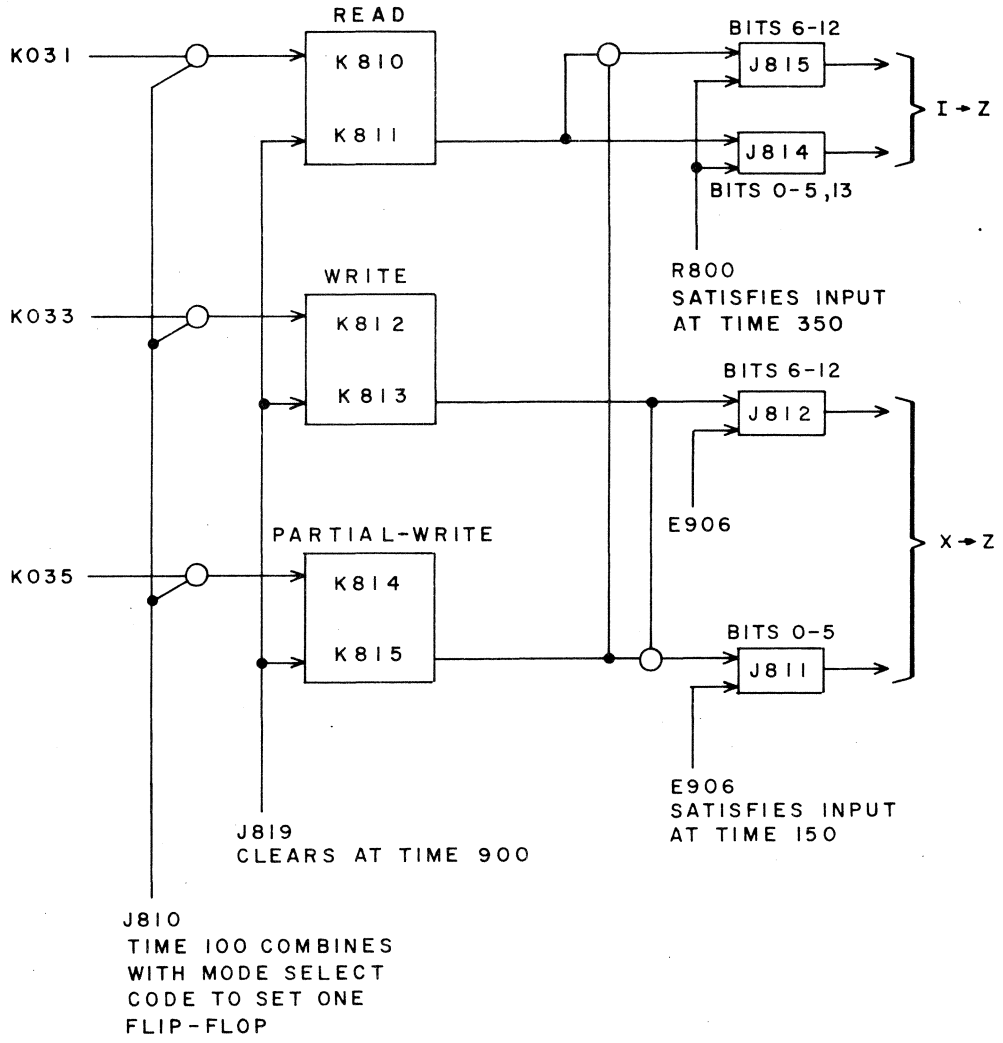


Figure 1-16. Mode Select Circuit

register from the X register. The 0 output of K812/K813 does not enable the AND gate to one of the inputs to J811, so a 0 remains on this input. At time 150, the 0 output of E906 satisfies the inputs to J811. The 1 output of J811 enables the AND gate inputs for bits 0 through 5 of the Z register from the X register.

Since a data word is on the output lines of the X register at this time, a transfer of 1's occurs from X to Z.

The term transfer of 1's implies that the transfer was made into a previously cleared register. The Z register flip-flops were cleared when the active flip-flop was set at the start of the memory reference cycle. The 0's in the other mode commands leave the read and partial-write flip-flops in a cleared status. These flip-flops were cleared during the preceding cycle by the 1 output of J819 at time 900. The 1 output of the read and partial-write flip-flops maintains a 0 on the outputs of J814 and J815. The 0 output of J814 and J815 blocks the AND gate inputs to the Z register flip-flops from the I inverters.

The 0 output of the set flip-flops in the Z register blocks the AND gates to the associated inhibit generators thereby preventing a turn-on of inhibit current of time 450 for those cores that are to be switched from 0 to 1 when the write drive turns on at time 475.

Partial Write: A partial-write command is placed on the input control line to the AND gate of the partial-write mode select flip-flop by the control section. The partial-write command combines with the 1 output of J810 to set the partial-write flip-flop K814/K815. The 0 output of K814/K815 blocks the AND gate input to one of the two inputs to J811 and J815. This leaves an enabling 0 on these inputs. At time 150, the 0 output of emitter-follower E906 places a satisfying 0 on the input to J811. The 1 output of J811 causes a transfer of 1's from X to Z for bits 0 through 5. The 1 output of K812/K813 blocks the 1 output of J812; therefore, the 0 output of E906 does not satisfy J812 to place a 1 on the output of J812. The 0 output of J812 blocks the AND gate inputs from X to Z for bits 6 through 12. At time 350, the 0 output of R800 satisfies the inputs of J815 to place a 1 on the outputs of J815. The 1 output of J815 satisfies the AND gate inputs to the Z register from I inverters for a transfer of 1's of the upper seven bits. The 1 output of K810/K811 blocks the inputs to J814 so the output of J814 remains 0. The 0 output of J814 blocks the AND gate inputs to the Z register from the I inverter for the lower six bits and for bit 13. The Z register now contains a word, the upper seven bits from existing storage, and the lower six bits from new input data. At time 450, bit 13 is set if the parity generator has enabled it. When the write drive turns on at time 475, the Z register flip-flops containing 1's transfer these 1's back into memory at the address specified by the contents of the S' register. The transfer of 0's from the Z register to memory cores is controlled by the inhibit generators as described under inhibit circuits.

Address Selection: In order to accommodate a 14-bit word in a seven plane memory stack, two bits must be stored on each plane. This is done by dividing a plane into two banks, each consisting of one odd quadrant and one even quadrant. Even bits 00 and 02 through 12 are stored in the even quadrants of seven successive planes in a bank, and odd bits 01 and 03 through 13 are stored in the odd quadrant of the same seven planes in the same bank. Storage across the seven planes of the other bank uses the remaining odd and even quadrant of each plane. Since a quadrant contains a 64 by 64 matrix of cores, and two quadrants are used to store a word, each bank effectively accommodates words of 14 bits in 4,096 storage locations.

Since a memory stack contains two banks, 4,096 times 2 equals 8,192 storage locations which are available in a memory stack. For addressing purposes, the X drive lines run through the even quadrants of bank 00, continue through all the planes on the south side through the transposition plane and down through all the planes on the north side, and return to termination through the odd quadrant of bank 00, Figure 1-17. Therefore, 64 X drive lines thread all cores in all four quadrants of all seven planes in a memory stack. In the Y axis, 64 Y drive lines run through both quadrants of all seven planes and terminate. A second set of 64 Y drive lines threads through the odd and even quadrants of the seven planes of the 01 bank. Therefore, both banks are energized along the X axis and only one bank is energized along the Y axis so the Y drive lines serve to select the 00 or 01 bank. Addressing consequently energizes one of 64 lines in the X axis and one of 128 lines in the Y axis. The energized X line crosses the energized Y line once in the odd quadrant and once in the even quadrant of the seven planes of a selected bank. The drive lines are energized by turning on line-driver transformers, Figure 1-18.

The 0 and 1 output configuration of the S' register resulting from an input address acts to turn on line-driver transformers. Bits 01, 02, and 04 combine to enable certain 900-milliampere gates on the X axis. These 900-milliampere gates are satisfied when the gate flip-flop K804/K805 is set by the 1 output of the active flip-flop at the start of the cycle, Figure 1-15. This gate flip-flop remains set until time 875 when it is cleared by the 1 output of J820.

Bits 00, 03, and 05 combine to enable certain transformer drivers to complete the circuit from the 900-milliampere gates via the primary winding of the line-driver transformers. These transformer drivers are satisfied by the output of read flip-flop K806/K807 or write flip-flop K808/K809. The read or write flip-flops serve to turn on transformer drivers which complete the circuit through the primary windings of the line-driver transformers. This produces a current in the connected drive lines in one direction for read and the opposite direction for write. Two transformers are used together for selection of two drive lines; the parallel-aiding primary windings are driven

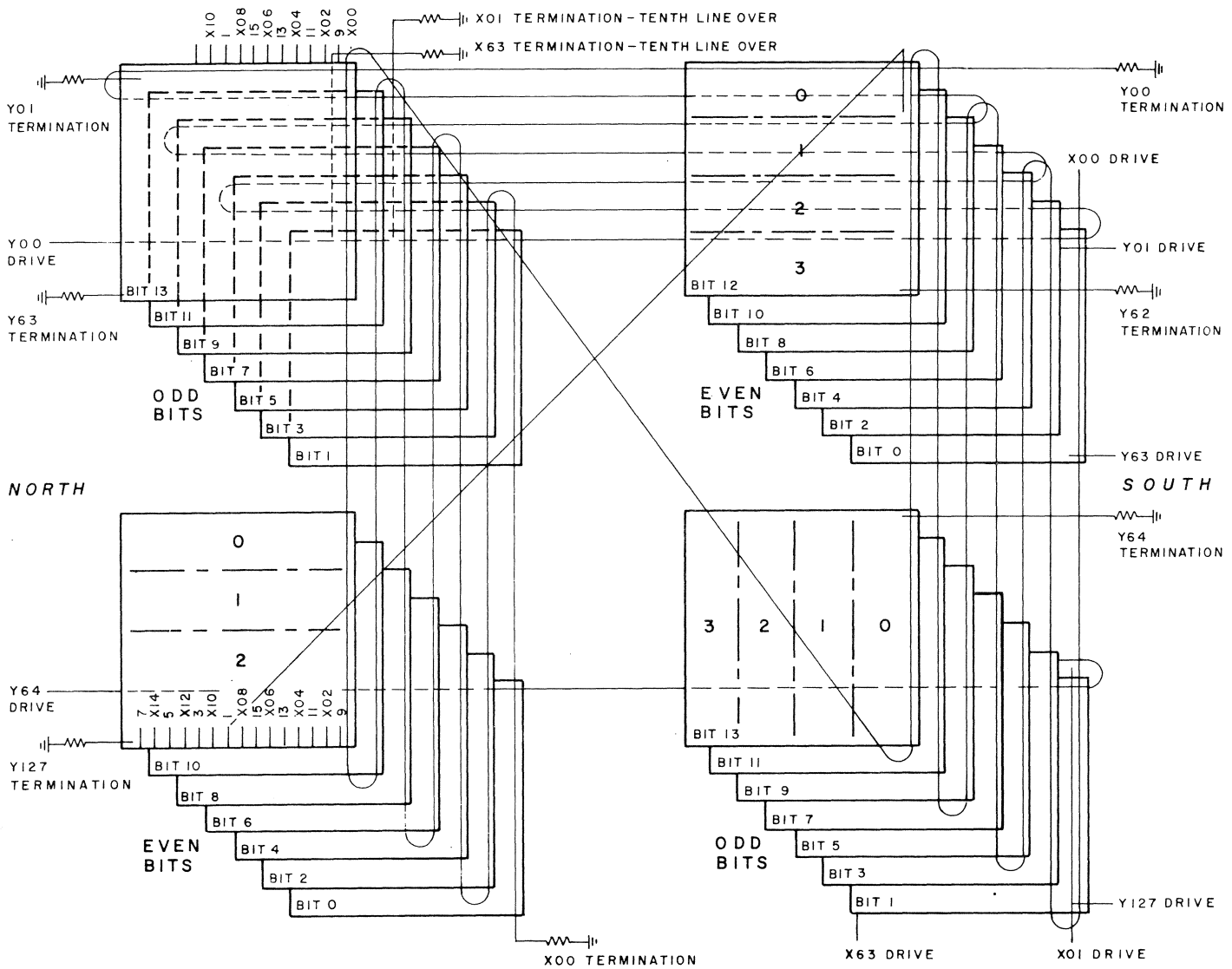


Figure 1-17. Memory Arrangement

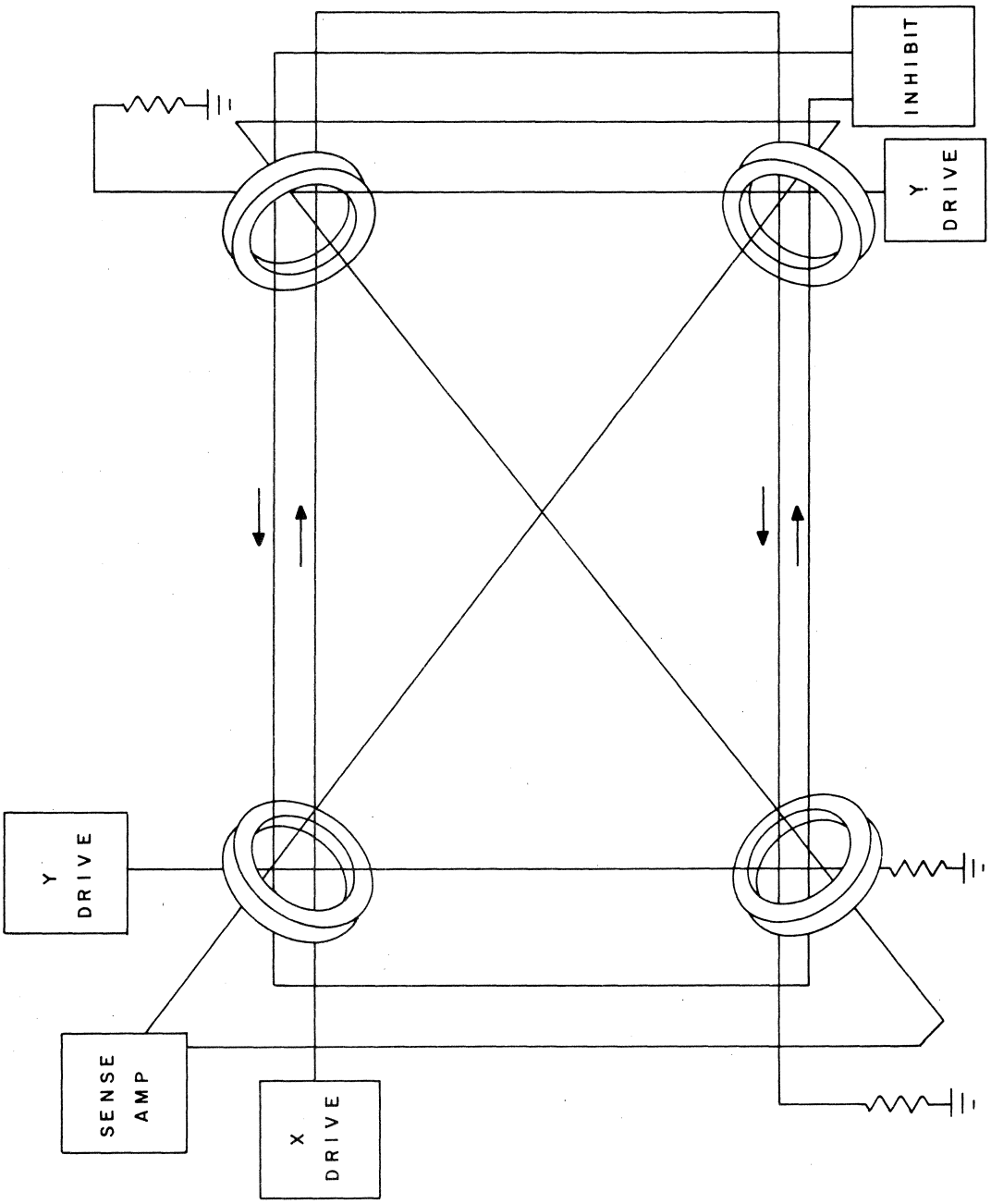


Figure 1-18. Core Matrix, Functional Brief

to energize one of the two drive lines connected to the series-aiding secondary windings.

If K806/K807 is set, as it is during the read time, the current comes into the center tap of both primary windings of a line-driver transformer and splits out via the half of the primary connected to the transformer driver for read drive and half of the primary connected to the transformer driver for one of the two drive lines.

If K808/K809 is set, as it is during the write time, the current comes into the center tap of both primary windings of a line-driver transformer and splits out via the half of the primary connected to the transformer driver for write drive and the half of the primary connected to the transformer driver for one of the two drive lines. This allows control of current flow in two directions for one line, and control of current flow in two directions for the other line. One arrangement controls current flow in one direction to energize one line, as would be the case where line 0 was energized in the read mode, and line 32 would be quiescent. Or, by selecting the proper transformer drivers, line 32 could be energized and line 0 quiescent in either read or write mode. Bits 07, 08, and 10 combine to enable certain 900-milliampere gates in the Y axis to accomplish the same functions as corresponding 900-milliampere gates in the X axis. Bits 06, 09, 11, and 12 combine to enable certain transformer drivers in the Y axis to accomplish the same functions as corresponding transformer drivers in the X axis. All cores containing 1's at the intersections of the energized and coincident X and Y drive lines are switched to 0 during the read time. During the write time, all cores containing 0's at the intersections of the energized and coincident X and Y drive lines are switched to 1's unless the inhibit current is flowing through that core.

Memory Arrangement

The maximum number of bits that can be stored in a given memory location is 14 bits (13 bits containing information, and 1 bit used for parity checking). Information access time for the memory and its associated control and sensing circuits is approximately 0.5 microsecond, and the time for a complete memory reference cycle is less than 1.35 microseconds. Figure 1-17 shows the quadrants, planes, and X and Y drive lines arranged to form a memory stack, and Figure 1-18 shows a functional brief of memory cores with the drive lines, inhibit line, and sense line threaded through a set of four cores. All cores are wired in the same manner. The following paragraphs describe the circuits that are directly connected to these drive lines and affect storage, location, and removal of bits stored in the memory stack.

Core Storage: The memory operates in the coincident current mode, using currents of one direction to read, and the opposite direction to write. These coincident half-currents are approximately 340 milliamperes and are produced by the circuits contained in the drivers, gates, and transformers associated with the storage and sensing functions of the core memory stacks.

As shown in Figure 1-17, each core is threaded by four wires; X and Y half-current drive lines, an inhibit line, and a sense line. When information is written into a core, the core is switched to the 1 state by two coincident 340-milliampere currents on the X and Y drive lines. Similarly, when information is read from a core, it is switched to the 0 state by two coincident 340-milliampere currents of the opposite polarity. The inhibit line carries a current of 340-milliamperes parallel to one of the drive lines, but in a direction opposite to that of the half-write current. If the inhibit current is flowing during a write phase, it cancels the effect of one of the half-currents, and thereby prevents any core through which the inhibit current passes from being switched from a 0 to 1 state. If the drive currents were not inhibited during the write phase, all cores would be switched to a 1 state. If the write coincident X and Y currents act to switch a core from 0 to 1, and if that core is already a 1, it remains a 1. Conversely, if the read coincident X and Y drive currents act to switch a core from 1 to 0, and if that core is already a 0, it remains a 0. The sense line is connected to a differential sense amplifier card. When a core switches state in either direction, the sense amplifier card produces a logic 0 output; however, this output is sampled only during the memory read phase.

The memory core material has an approximately rectangular hysteresis loop. The high remanent magnetization of the core enables it to function as a memory element. The magnetic properties of a core are represented by its hysteresis loop, Figure 1-19, in which magnetic flux density B is plotted as a function of field intensity H. If sufficient current flow to cause a field intensity of $+H_m$ is applied to the core, the flux density increases to saturation $+B_s$. When current is removed, the flux drops to residual value $+B_r$ and remains there. Sufficient current flow in the opposite direction to cause a field intensity of $-H_m$ reverses the flux density to $-B_s$. When current is removed, the flux density drops to the residual value $-B_r$.

The basic memory cycle is composed of 340-milliampere, half-current pulses capable of producing a field intensity of $H_m/2$. A half-current pulse is insufficient to switch a core; however, the coincidence of two half currents results in an effective current of 680 milliamperes, producing a net field intensity which is sufficient to switch the core.

X and Y Drive Circuits: The X and Y drive is developed by three circuits: gates, transformer-drivers, and line-driver transformers.

The function of a line-driver transformer circuit is to provide half-currents of 340 milliamperes at approximately 44 volts to X and Y drive lines in the memory stack when supplied with 450 milliamperes of current through the primary windings at +22.5 VDC. A line-driver transformer circuit contains two voltage step-up transformers, in a ratio of 4 to 3, each having two secondary windings of 32 turns and a center-tapped primary of 24 turns. The transformers are connected so that two transformers operate

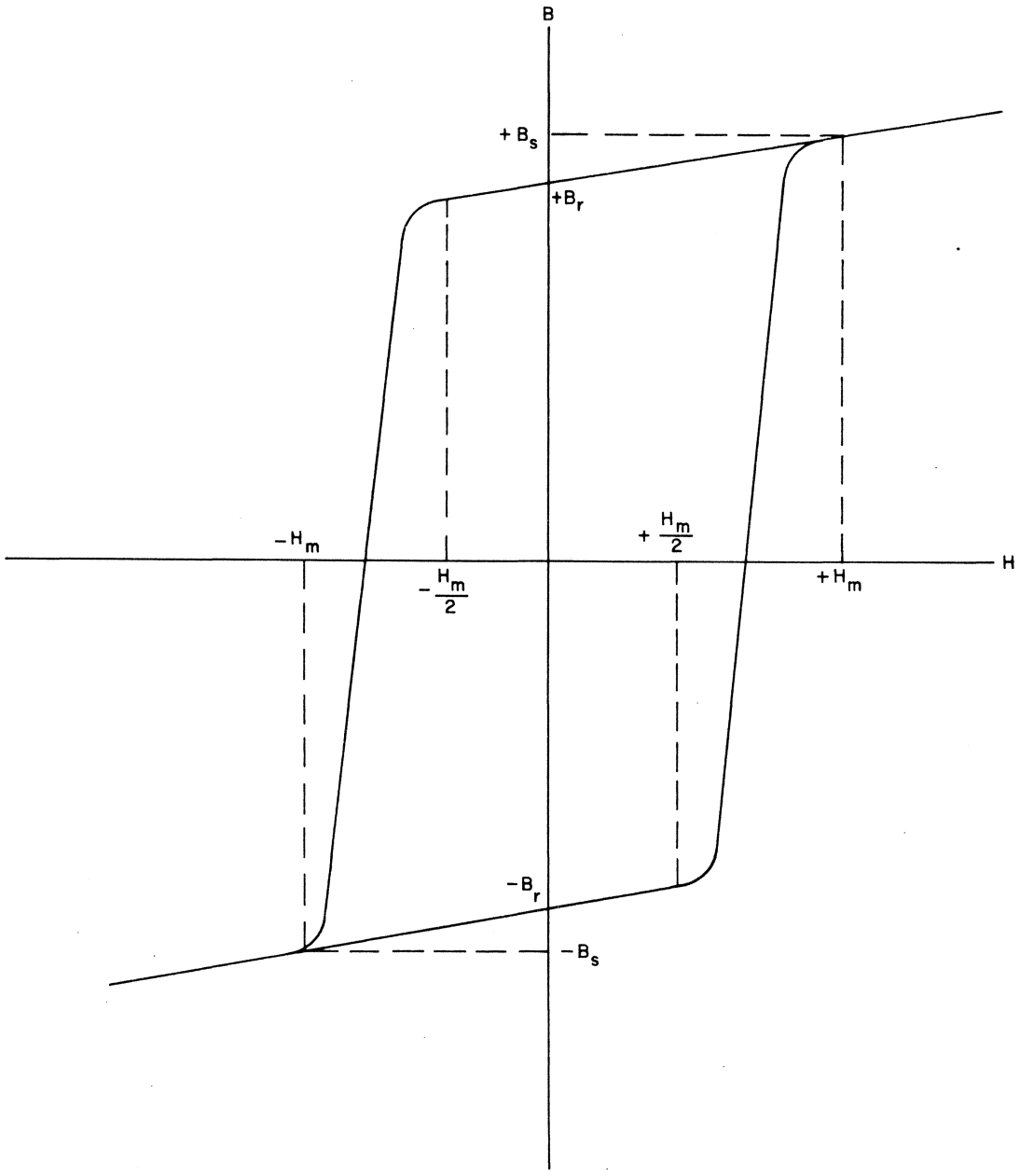


Figure 1-19. Typical Hysteresis Loop

simultaneously with their primary windings energized in parallel from +22.5 VDC and their secondaries connected in series. The output voltages are therefore additive, resulting in levels of approximately 44-volt pulses of current. Two line-driver transformer circuits are mounted on one card. The source of the 450-milliampere current is the +22.5 VDC, 900-milliampere output of the gate circuit connected to the center tap of the primary windings of the two transformers in the line-driver transformer card. This gate is satisfied when all inputs to the circuit are at the logic 0 level of -1.1 VDC. The gate card also contains a discharger circuit which grounds the primary windings of the two line-driver transformers which were previously energized. This removes the stored charge from the windings and neutralizes the transformers. The discharger circuit is satisfied by a -1.1 VDC 0 input.

In the line selection process, the gate is satisfied, thereby making 450 milliamperes of current available through two transformer windings in the line-driver transformer card. Two transformer-driver circuits are used to complete the current path in one direction, the read drive (arbitrarily). Two transformer-driver circuits are used to complete the current path in the opposite direction, the write drive. The read or write selection is accomplished by switching the current path in two transformer primaries connected in parallel-aiding. One end of two line-driver transformer primaries is common through the transformer-driver circuit that enables read or write. The other ends of the two line-driver transformer primaries are each tied to a separate transformer-driver circuit that enables a drive line.

Translation of an address in the S' register requires 13 bits plus the set or clear output of the read-drive and/or write-drive flip-flops. K807 of flip-flop K806/K807 enables or disables the read drive, and the output of K809 of flip-flop K808/K809 enables or disables the write drive. Bit 12 selects the 00 or 01 bank by gating the sense amplifier for read and by enabling certain transformer drivers for write.

Inhibit Circuits: Whenever an address is selected and the read drive is on, coincident currents are present on each core of that address. These currents attempt to switch all cores of that address. Cores magnetized in the direction resulting from a previous 1 storage are switched, and cores magnetized in the direction resulting from a previous 0 are not switched. Inhibit currents are not used during read: those cores that switch are allowed to switch. If a core is switched, a small voltage is induced in the sense line threaded through that core and a pulse appears along the sense line, Figure 1-17. The readout process switches every core containing a 1 to a 0; this is a destructive readout and the memory must be restored. The output of the sense line is amplified and gated into the Z register as 1's. During the write drive, the information is written back into memory; at the end of the memory reference cycle, the contents of the particular selected address is restored.

Whenever an address is selected and the write drive is on, two coincident currents are present on each storage bit of that address. Unless the effect of one of these drive currents is cancelled, every core in that address is switched to a 1. Because of the effect of the inhibit lines during the write phase of the memory cycle, only those bits which were 1's are switched back to 1's. In order to prevent core-switching in cores that are not to store a 1, a current flowing in opposition to one of the drive currents is generated to cancel the effect of this drive current, thereby inhibiting a core from being switched. This function is performed by the inhibit circuits consisting of inhibit generators and inhibit lines.

The function of these circuits is to allow a 340-milliampere current to flow from the +40 VDC source through the inhibit lines in the memory planes. This occurs whenever all inputs to the respective inhibit generator circuit are at the logic 1 level of -5.8 VDC. The inhibit circuit contains a 125-ohm terminating resistor so that the resulting current is approximately 340 milliamperes.

The inhibit lines in each plane are arranged in eight groups or stripes. Each stripe is 16 cores wide and extends across the two even quadrants or the two odd quadrants; thus, each inhibit stripe controls (16 x 128) 2,048 cores. In even-bit quadrants, the flux generated by the Y inhibit line current opposes the flux of the Y half-write currents. In odd-bit quadrants, the flux generated by the X inhibit line current opposes the flux of the X half-write currents. Since the inhibit lines extend through two quadrants, four inhibit generators are required to inhibit even quadrants. An inhibit circuit is turned on by a logic 1 output from one of the stripe select flip-flops in the series K816/K817 through K830/K831 which combines with the logic 1 output from the clear side of one of the Z register flip-flops.

Sense Circuits: Each sense circuit consists of the sense line threaded through all cores of a quadrant of a plane, and the sense amplifier which is tied to the two ends of the sense line. Whenever a core is switched, a pulse of about 35 millivolts appears on the sense line. This pulse may be either positive-going or negative-going depending on the direction in which the core was switched. The sense amplifier consists of a differential voltage amplifier and a discriminator. Regardless of the pulse polarity at the sense amplifier input, the output is always a positive-going pulse. The residual output of the sense amplifier is -13.6 volts which represents a logic 1. When a 35-millivolt pulse appears on the sense line, the output of the sense amplifier switches to approximately -1.6 VDC. The logic card (1 inverter) following the sense amplifier interprets any positive-going pulse more positive than -3 volts as a logic 0.

Parity Circuit: The address in the S' register selects a location from 4,096 possible locations in a memory bank. Bit 13 in each location is used to provide a comparison bit for parity check. Bit 13 is generated by the parity logic, Figure 1-20, and placed into the Z register before a word is written into memory.

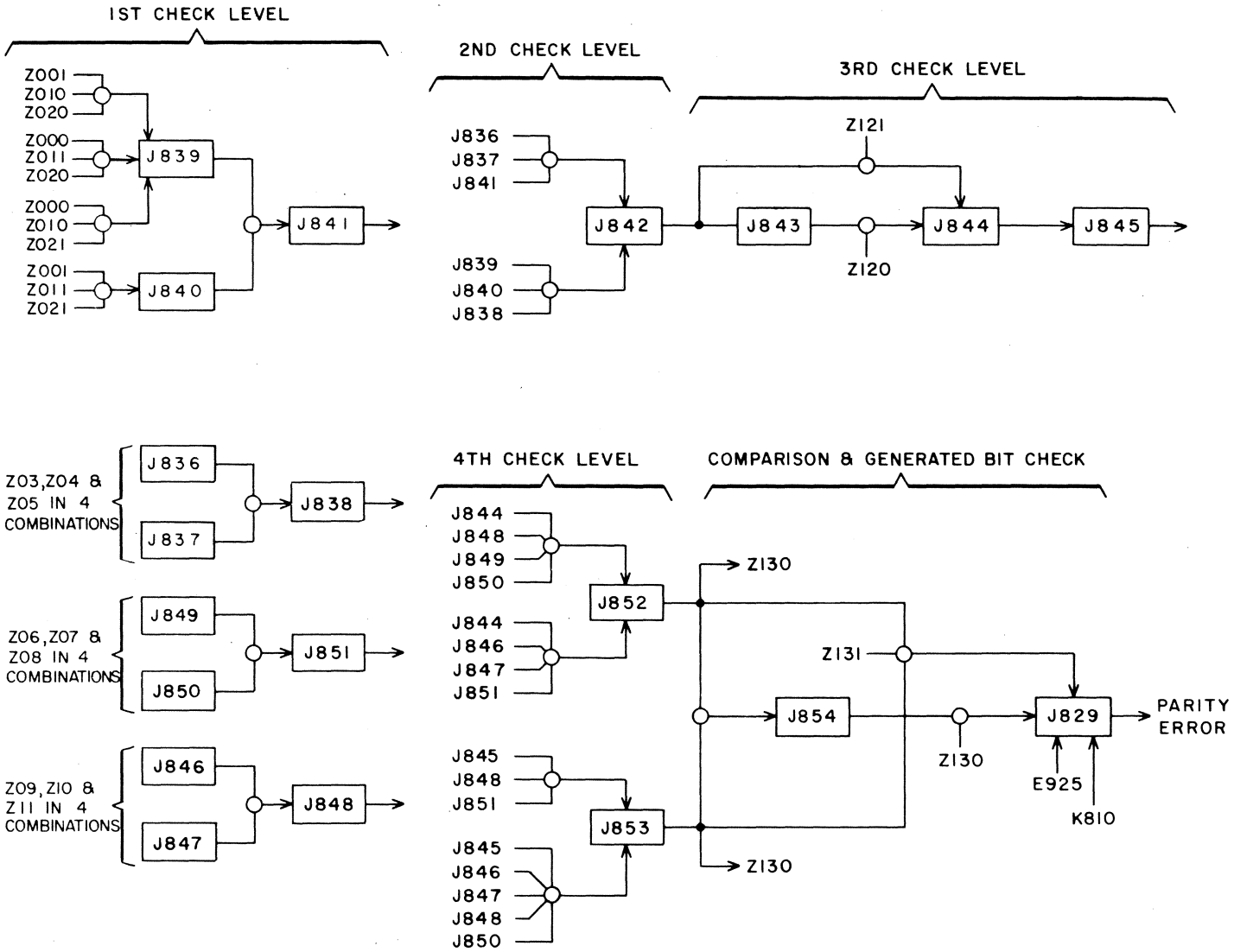


Figure 1-20. Parity Logic

The number of 1's contained in the Z register determines whether a parity bit should be generated by the parity logic as a 1 or 0. The parity check on the 8491 memory operates on an odd-parity basis; that is, the word which is read out of or written into memory must contain an odd number of 1's. If the number of 1's in the operand is odd, a parity bit 0 is generated; if the number of 1's in the operand is even, a parity bit 1 is generated. The parity logic, Figure 1-20, determines generation of parity bit 13 by checking the contents of the Z register at four levels.

At the first check level, three bits are examined in four combinations. A 0 output at J839 indicates one 1 in the group containing Z00, Z01, and Z02. A 0 output at J840 indicates three 1's in this group. Since a 0 output at both J839 and J840 cannot occur at the same time, the AND gate input to J841 is disabled and a 1 output at J841 indicates an odd configuration in the group. A 1 output at J839 indicates zero, two, or three 1's in the group. A 1 output at J840 indicates zero, one, or two 1's. Both stages agree that either zero or two 1's exist in the group. The AND gate input to J841 is enabled and a 0 output at J841 indicates an even configuration in the group. Regardless of the contents of Z00, Z01, and Z02, a 0 output at J841 indicates an even configuration and a 1 output indicates an odd configuration. The remaining bits in the Z register are checked for an odd or even configuration in the same manner.

At the second check level, the output of group 1 (Z00, Z01, and Z02) and the output of group 2 (Z03, Z04, and Z05) are logically added; that is, the sum of two odd configurations is an even configuration, the sum of two even configurations is an even configuration, and the sum of an odd configuration and an even configuration is an odd configuration. A 0 output at J842 indicates that the result of this operation is an even configuration. A 1 output at J842 indicates an odd configuration.

At the third check level, the condition of Z12 is examined and added to the result of the second check level. A 0 output at J844 indicates an even configuration. A 1 output indicates an odd configuration.

At the fourth check level, the output of group 3 (Z06, Z07, and Z08), the output of group 4 (Z09, Z10, and Z11), and the result of the third check level are logically added. An even configuration is indicated by a 1 output at both J852 and J853; an odd configuration is indicated by a 0 output at either J852 or J853.

The outputs of J852 and J853 are combined with a 1 or 0 bit 13 at the input of J829 to indicate a parity or no-parity error. This parity error is sampled at time 625 of the memory cycle. The pyramid reduction of the 13 bits in the stored word results in the generated bit, and the bit 13 in storage is the comparison bit. When the comparison bit and the generated bit are the same, the word passes parity check and the computer proceeds with the function

being executed. If the comparison bit and the generated bit are not the same, a fault indication is indicated in the error register and an interrupt 10 is generated.

Memory Timing (Select Mode)

The select code, mode command, first word address, data word, and memory request to a specific memory bank are originated by the computer to start a memory reference cycle, Figure 1-21. (The phase times shown on the delay line are cross-reference points to the command timing charts in publication number 14092000.) After a memory bank is selected, address transferred, and mode command received, a timing pulse starts down the delay line in the memory section. At this time, time 0, temporary control of the read, write, or partial-write reference is held by the memory section. The computer stays on the line until the memory section completes its cycle in a period of less than 1.35 microseconds. At the end of the memory cycle, the memory section returns control to the computer and becomes quiescent until receipt of another memory request. The computer cannot make more than one memory reference simultaneously. The functions occurring during the first 200 nanoseconds of the 1.35-microsecond memory reference period are described in the previous paragraphs. At 0 time the delay line is activated, and the following events occur at the times indicated.

Time 0: The 0 pulse from J825 drives the delay line to a logic 0 and starts the 0 pulse down the delay line.

Time 50: After the leading edge of the 0 pulse on the delay line passes emitter-follower E902, 1 appears on the output of J809. The 1 output of J809 is applied to clear K800/K801, the active flip-flop. The set output of K800/K801 causes a 1 output from J825. The 1 output of J825 returns the delay line to a logic 1. This action forms a pulse about 100 nanoseconds wide. K800/K801 remains clear until the next memory reference. K802/K803, the busy flip-flop, remains set until time 1200; K804/K805, the gate flip-flop, remains set until time 875; and K806/K807, the read-drive flip-flop, remains set until time 375. The address remains in the S' register until time 1000.

The remaining events in a memory cycle vary depending on the mode of operation. One cycle may be either a read, write, or partial-write cycle; therefore, each mode as it occurs in a memory cycle is discussed separately.

Memory Timing (Write Mode)

Time 100: The 0 pulse on the delay line passes emitter-follower E904. A 1 appears on the output of J810. The 1 output of J810 satisfies the AND gate input to set K812/K813, the write flip-flop, thereby starting resume 1 function. The 0 output of the write flip-flop enables J811 to gate bits 0 through 5 into the Z register and J812 to gate bits 6 through 12 into the Z register.

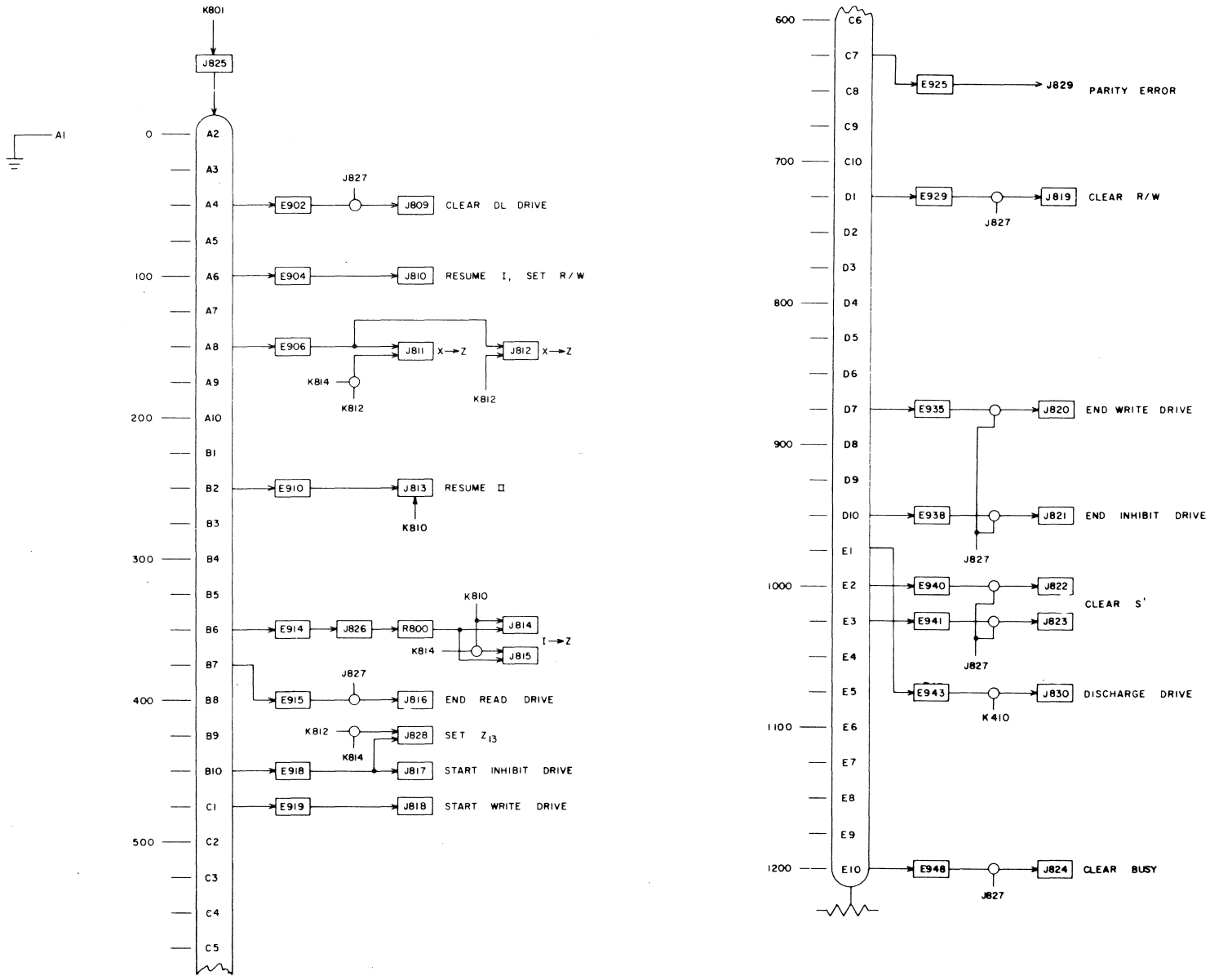


Figure 1-21. Memory Cycle

Time 250: The 0 pulse on the delay line passes emitter-follower E910 causing a 1 to appear on the output of J813. The 1 output at J813 indicates a resume II operation has occurred. However, since the inverters following the cleared read flip-flop K810/K811 have 0 outputs, no transfer of data from the sense amplifier inverters to the Z register can occur. The resume II operation in write mode is equivalent to an all 0 transfer from I to Z.

Time 350: The 0 pulse on the delay line passes emitter-follower E914 causing a 0 on the output of R800. The 0 output of R800 is a shaped pulse which enables J814 and J815 to satisfy the AND gate to the Z register from the I inverters. However, the reset output of the cleared read flip-flop K810/K811 blocks the 0 input to J814, and the reset output of the cleared partial-write flip-flop K814/K815 combines with the reset output of K810/K811 to place a blocking 1 on the input to J815. The output of J814 and J815 is 0. Since a 1 output of J814 and J815 is required to cause a transfer of 1's from memory core inverters (the I inverters) to the Z register, this I to Z transfer does not occur during this cycle.

Time 375: The 0 pulse on the delay line passes emitter-follower E915. The 0 output of E915 blocks the AND gate to inverter J816, thereby placing a 0 on the input to J816. J827, the other input to the J816 AND gate, is normally a 1 unless a master clear (a 0 at this AND gate) is activated. The 1 output of J816 is applied to the clear side of the read-drive flip-flop K806/K807, thereby ending the read drive currents. The contents of memory at the selected address is destroyed during a read drive; however, the contents of that address is restored during the write drive phase of a read mode or replaced by the contents of the X to Z transfer during the write drive phase of a write mode.

Time 450: The 0 pulse on the delay line passes emitter-follower E918 causing a 1 output of J817 and enabling J828. The reset output of K812/K813 (the write flip-flop) is a 0 which satisfies the inputs to J828 to place a 1 on the output. The 1 output of J817 is applied to enable the AND gate inputs to the inhibit stripe selection flip-flops K816/K817 through K830/K831. This 1 combines with 1's depending on address bits 4 and 5 for the odd inhibit drivers or bits 10 and 11 for the even inhibit drivers to set certain stripe selection flip-flops. The outputs of the stripe selection flip-flops combine with the reset outputs to Z register flip-flops to turn on certain inhibit drivers. The Z register 1 output occurs when a data bit input is 0; therefore, the inhibit driver prevents a core switch from 0 to 1. The cores in the selected memory address were switched to 0 during the read drive.

The 1 output of J828 enables the AND gate input to Z130/Z131, the parity flip-flop. If parity is 1, the reset output of Z130/Z131 prevents a turn-on of the inhibit driver, and the core receiving a parity bit switches from 0 to 1. If parity is 0, the core is not switched.

Time 475: The 0 pulse on the delay line passes emitter-follower E919 causing a 1 on the output of J818. The 1 output of J818 is applied to set

K808/K809 (the write-drive flip-flop). The set output of K808/K809 is inverted and applied as 0's to turn on transformer drivers in the X and Y axes. The direction of current through the line-driver transformers as determined by the write transformer drivers is to switch cores from 0 to 1. Any cores that do not have an opposing inhibit current flowing through them are switched from 0 to 1 when the drive current turns on.

Time 625: The 0 pulse on the delay line passes emitter-follower E925 placing a 0 enable on the input of J829. The reset output of K810/K811 (the read flip-flop) blocks the inverter J829 causing a 0 output to remain on J829. The 0 output of J829 blocks a transmission of 1 along the parity error line. The other two inputs to J829 from the comparison bit and generated bit have no effect because the 1 output of J829 is blocked by the reset output from the read flip-flop K810/K811. In the write mode, the parity bit is only generated and stored. It is not sent back out along the parity error line. During a subsequent memory readout, this stored bit is compared to a bit generated from the number of 1's in the Z register. Therefore, if the number of 1's in the Z register equaling odd parity is written into memory and the number of 1's equaling odd parity is read out of memory, an error did not occur. If parity was written in as odd and read out as even, or vice versa, then an error did occur. This parity error bit is only generated during the read mode.

Time 725: The 0 pulse on the delay line passes emitter-follower E929 causing a 1 output of J819. The 1 output of J819 is applied to clear K810/K811 (the read flip-flop), K812/K813 (the write flip-flop), and K814/K815 (the partial-write flip-flop). The reset outputs of these flip-flops are inverted, placing a 0 on the AND gate inputs to the Z register flip-flops. This prevents any Z register flip-flops from being set by a 1 input from any source. The 0 input to the set side of the Z register flip-flops allows them to be cleared when the next clear pulse appears at the beginning of the next memory reference cycle.

Time 875: The 0 pulse on the delay line passes emitter-follower E937 causing a 1 output from J820. The 1 output of J820 is applied to clear K804/K805 (the gate flip-flop) and K808/K809 (the write-drive flip-flop). The set output of K804/K805 is inverted through J806 to block a turn-on of the 900-milliampere gates to the Y line-driver transformers, and to J808 to block a turn-on of the 900-milliampere gates in the X line-driver transformers. This prevents any drive current from switching any cores for the remaining time of the present memory cycle. The set output of K808/K809 is inverted through the inverters to block a turn-on of transformer drivers in the X and Y axes of the memory banks. Clearing of the gate flip-flop and the write-drive flip-flop ends the write drive.

Time 950: The 0 pulse on the delay line passes emitter-follower E938 causing a 1 output of J821. The 1 output of J821 is applied to clear K816/K817 through K830/K831, the stripe-selection flip-flops. The 0 output of

these stripe-selection flip-flops blocks the AND gate inputs to the inhibit generators, thereby ending the inhibit drive.

Time 975: The 0 pulse on the delay line passes emitter-follower E943 causing a 1 output of J830. The 1 output of J830 is applied to clear K832/K833 (the discharger flip-flop) and turn on discharger circuits to neutralize the line-driver transformers.

Time 1000: The 0 pulse on the delay line passes emitter-follower E940 to cause a 1 output of J822. The 1 output of J822 is applied to clear the six lower-bit flip-flops in the S' register.

Time 1025: The 0 pulse on the delay line passes emitter-follower E941 to cause a 1 output of J823. The 1 output of J823 is applied to clear the upper six bits of the S' register.

Time 1200: The 0 pulse on the delay line passes emitter-follower E948 to cause a 1 output of J824. The 1 output of J824 is applied to clear K802/K803 (the busy flip-flop). The reset output of K802/K803 is applied to enable the AND gates to the active flip-flop, thereby preparing it for selection in a subsequent cycle. The 0 pulse on the delay line dissipates across the terminating resistor which prevents a reflection back through the delay line to enable every function in reverse time. END OF CYCLE.

Memory Timing (Read Mode)

Only the times and events that differ from the write mode are listed for the read mode. Otherwise, the times and events are the same for both modes.

Time 100: Basically, the read mode is the same as write mode except the write flip-flop K812/K813 is not set by the mode command. Since this cycle is to be in the read mode, the read flip-flop K810/K811 is set by the process described in mode selection. The read drive to switch the cores containing 1's to 0's occurs when the S register transfers the address to the S' register. The Z register is cleared in preparation for a transfer of 1's from the I inverters. So, at time 100, the Z register is cleared and a transfer of 1's from I to Z is enabled but has not yet occurred.

Time 150: The reset outputs of K812/K813 (the write flip-flop) and K814/K815 (the partial-write flip-flop) place a blocking 1 on the inputs to J811 and J812. This prevents an X to Z transfer; therefore, nothing happens to the Z register at this time. The Z to X transfer is enabled by the control section for an output transfer of 1's. This output transfer does not occur until 1's are in the Z register following the I to Z transfer at time 350.

Time 250: The 0 pulse on the delay line passes emitter-follower E910 causing a 1 output from J813. The 1 output of J813 is applied to enable resume II for the Z to X transfer. Because the inverters following the read flip-flop K810/K811 have 1 outputs, a transfer of 1's from Z to X occurs following the I to Z transfer.

Time 350: The 0 pulse on the delay line passes emitter-follower E914 causing a 0 output from R800. The output of R800 is a 50-nanosecond shaped pulse which enables inverters J814 and J815, and places a pulse of the proper duration on their outputs. The reset output of the read flip-flop K810/K811 satisfies J814 to set a 1 on its output. The reset output of K814/K815 (the partial-write flip-flop) and the reset output of K810/K811 leave a 0 to satisfy the input of J815, thereby setting a 1 on the output of J815. The 1 output of J814 enables the AND gate between the I inverters and the Z register flip-flops for the lower six data bits. The 1 output of J815 enables the AND gate between the I inverters and the Z register flip-flops for the upper seven data bits. These AND gates are satisfied by any I inverters having 1's on their outputs. This causes the corresponding Z register flip-flop to set. The 1 outputs of the set flip-flops in the Z register are applied as satisfying 1's to the AND gate inputs of the X register. Also, the inhibit generators attached to the set Z register flip-flops do not turn on, thereby allowing the cores that were switched from 1 to 0 to be switched back from 0 to 1 when the write drive turns on at time 475. This action restores memory to the same status as it was before the read occurred. The parity bit is written back into memory the same as before the readout occurred.

Time 375: The events are the same as in the write mode except that an I to Z transfer did occur and the original contents of memory at the selected address is written back into memory at time 475.

Time 450: The events are the same as in the write mode except that the reset outputs of cleared flip-flops K812/K813 and K814/K815 combine to maintain a 1 on the input to inverter J828. When the 0 pulse on the delay line passes E918, the 0 output from the delay line does not satisfy the inputs to J828 to cause a 1 output. The 0 output of J828 blocks the AND gate from the parity bit generating circuitry to Z130/Z131.

Time 625: The 0 pulse on the delay line passes emitter-follower E925 to place an enabling 0 on the input to J829. The reset output of flip-flop K810/K811 enables a second input to J829. The parity comparison network of J852, J853, J854 is combined with the set or clear status of Z130/Z131. If the generated bit and the bit read out of storage are identical, the third and fourth inputs to J829 are 1's and J829 has a 0 output. Conversely, if the comparison network and Z130/Z131 differ, a 1 output of J829 is transferred to the control section as a parity indication.

The remaining time of the cycle is the same as the write mode.

Memory Timing (Partial Write)

Time 100: The partial-write mode is identical to the read mode except that the partial-write flip-flop K814/K815 is set by the process described under mode selection. The reset output of K814/K815 enables the inverters J815 and J811. The reset output of K810/K811 (the read flip-flop) places a blocking 1 on the input to J814 to prevent an enabling 1 output for an I to Z

transfer of the lower six bits and the parity bit at time 350. The set output of cleared K812/K813 (the write flip-flop) places a blocking 1 on the input to J812 to prevent an enabling 1 output for an X to Z transfer of the upper seven bits at time 150.

Time 150: The leading edge of the 0 pulse on the delay line passes emitter-follower E906 to place an enabling 0 on the input to J811 and J812. The reset output of K812/K813 blocks the reset output of K814/K815 to place a satisfying 0 on the inputs of J811. This sets the output of J811 to 1. The reset output of K812/K813 blocks inverter J812, thereby leaving a 0 on the output of J812. The 1 output of J811 satisfies the AND gates for a transfer of 1's from the X register into the six lower-bit flip-flops of the Z register. The 0 output of J812 blocks the AND gate inputs so an X to Z transfer of the seven upper bits does not occur. The reset output of the blocked seven upper-bit flip-flops and the reset output of the six lower-bit flip-flops that remain cleared after an X to Z transfer is applied to AND gates of the inhibit generators to prevent cores in memory from switching from 0 to 1 when the write drive turns on at time 475. This process of enabling the six lower bits and blocking the seven upper bits results in the six lower bits being replaced by an X to Z transfer and the seven upper bits remaining as they were in memory storage.

Time 350: The 0 pulse on the delay line passes emitter-follower E914 causing a 0 on the output of R800. The 0 output of R800 enables J814 and J815. The reset output of the cleared read flip-flop K810/K811 blocks the 0 input to J814 so a 0 remains on the output of J814. The reset output of the partial-write flip-flop K814/K815 blocks the AND gate input to J815. The 0 from the blocked AND gate satisfies the 0 inputs to J815 to place a 1 on the output of J815. The 1 output of J815 is applied to enable the AND gate inputs to the seven upper-bit flip-flops of the Z register. Any combining 1 outputs from the I inverters from memory satisfy the AND gate inputs to the seven upper-bit flip-flops to cause an I to Z transfer of 1's to occur. The AND gates to the six lower-bit flip-flops of the Z register are blocked by the 0 output of J814 so an I to Z transfer does not occur. The Z register six lower-bit flip-flops were set by a transfer of 1's from X to Z at time 150. The Z register now contains a word consisting of six lower bits from the X register and seven upper bits from those existing in memory.

The remainder of the cycle is identical to the write mode except that at time 450, the parity circuitry generates a parity bit to go into memory depending on the number of 1's in the new word.

NORMAL I/O (NORMAL CHANNEL)

The normal I/O control logic handles the exchange of control signals with the external equipment on the normal channel. This logic also initiates the normal cycle. The Compute Unit requests status or selects an I/O equipment

with an EF code. When this code is available on the normal data lines, flip-flop K126/K127 sets, Figure 1-22. A set output from this flip-flop causes a function ready signal to be sent to the I/O equipment and the COMPUTER STATUS indicator to display SEL.

Normal Input

When the Compute Unit is executing a normal input instruction, input request flip-flop K128/K129 is set. If no control signals are present at the input to J138, the 1 output from J138 produces a reset output from K260/K261 which ANDs with the set output of K128/K129 to cause T755 to place an input request on the normal channel control lines. The I/O wait flip-flop K120/K121 is also set at this time, which allows buffer cycles to occur while the normal I/O is waiting for resume or request signals.

When the input word is ready, the input equipment sends an input ready to the Compute Unit. The 1 output of R733 produces a 0 output from J138. If the buffer channel is not using the timing chain, the 0 output from J138 produces a 1 output from J139. If the buffer channel is using the timing chain, the output of J139 is held at 0 until the buffer cycle is complete.

The normal resync circuit synchronizes this 1 with the master clock. The 1 output of V131 occurs in phase with the odd outputs of the clock. The output of V131 resets the I/O wait flip-flop, which blocks the buffer channel from using the main chain while the normal sequence is using it.

During the input process, the input request flip-flop is reset which removes the input request. The external equipment in turn removes the input ready.

If the last word has not been read, the normal cycle again sets the input request flip-flops. The normal input process then repeats for the next word. This process is repeated until the last word has been read.

Normal Output

The normal I/O logic functions in a similar manner for both input and output operations. However, for an output operation, the information ready flip-flop is set when the output data word is placed on the normal channel data lines. The set output of K132/K133 ANDs with the reset output of K260/K261 to cause T737 to send an information ready signal to the external equipment.

After the output word has been processed, the external equipment returns an output resume signal to the Compute Unit. This signal is synchronized with the clock. The 1 output of V131 then resets K120/K121. The normal output either is terminated if the last word has been processed or repeated if additional words remain.

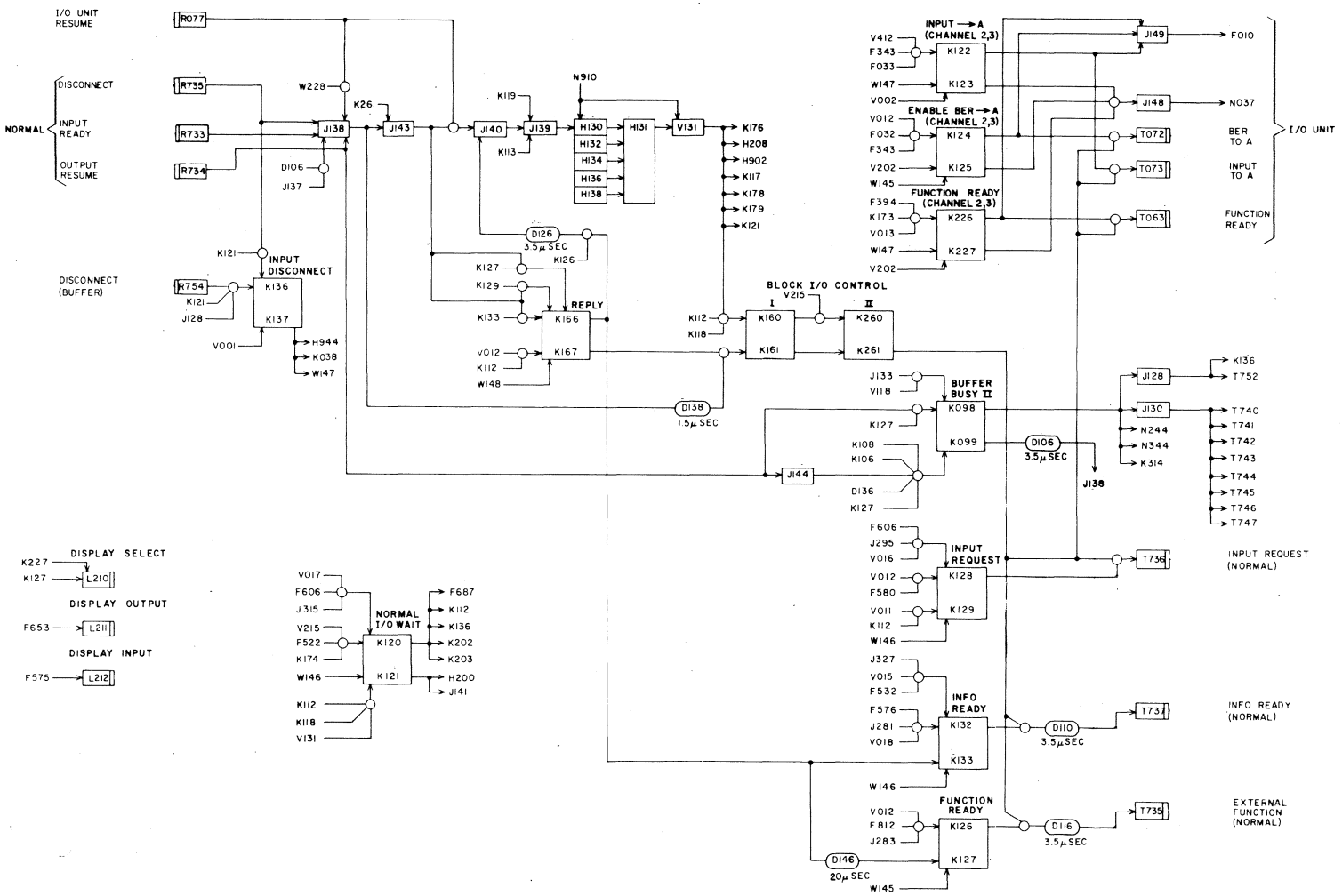


Figure 1-22. Normal I/O Control Logic

NORMAL I/O (BUFFER CHANNEL)

When the internal buffer channel is not busy, it is possible to perform a normal I/O operation over this channel. Most of the control logic is the same, except the receivers and transmitters activated are on the internal buffer channel. Figure 1-23 illustrates the logic involved for a normal I/O operation on the buffer channel. The operation of the logic is basically the same as described in the preceding paragraphs on normal input and normal output.

INTERNAL BUFFER I/O CONTROL

The buffer control logic conditions the Compute Unit logic to execute an input or output buffer operation.

Ready, Request, Resume Logic

The buffer control logic, Figure 1-24, is similar to the normal I/O logic. Ready, request, and resume signals are exchanged in the same manner as for normal I/O operation. The buffer control logic also contains logic which disables the normal control logic when the control signals are being exchanged for a buffer operation.

Input Buffer

When an input buffer instruction is read, the input request flip-flop K100/K101 is set, Figure 1-24. The reset output of K168/K169 gates a set output from this flip-flop into the set side of K104/K105. Setting this flip-flop causes T755 to send an input request to the external equipment. When the data is ready, this equipment returns an input ready signal to the Compute Unit. The resultant 1 output from R753 produces a 0 from J136 and a 1 from J137.

The 1 output from J137 activates the buffer resync circuit. An output occurs from V091 in phase with the odd clock. The output of H954/N054 sets the buffer gate flip-flop one phase time later, the output of N901 sets the buffer-normal flip-flop, and if the I/O logic is not busy with a normal I/O operation, initiates the execution of the buffer cycle. The buffer-normal path is used only if buffer and normal I/O operations are occurring simultaneously; otherwise, the buffer cycle is initiated at time 02 of RNI or by an input ready when a program is not running.

When N902 becomes a 1 at the next even phase time, the gating conditions are satisfied to set the buffer cycle flip-flop. The output from this flip-flop conditions the operation of the main timing chain to cause it to function as a buffer cycle.

At ø5 of the cycle, B_1 cycle flip-flop K114/K115 is set. The outputs of this flip-flop further condition the Compute Unit logic. At ø17, the B_2 cycle flip-flop is set.

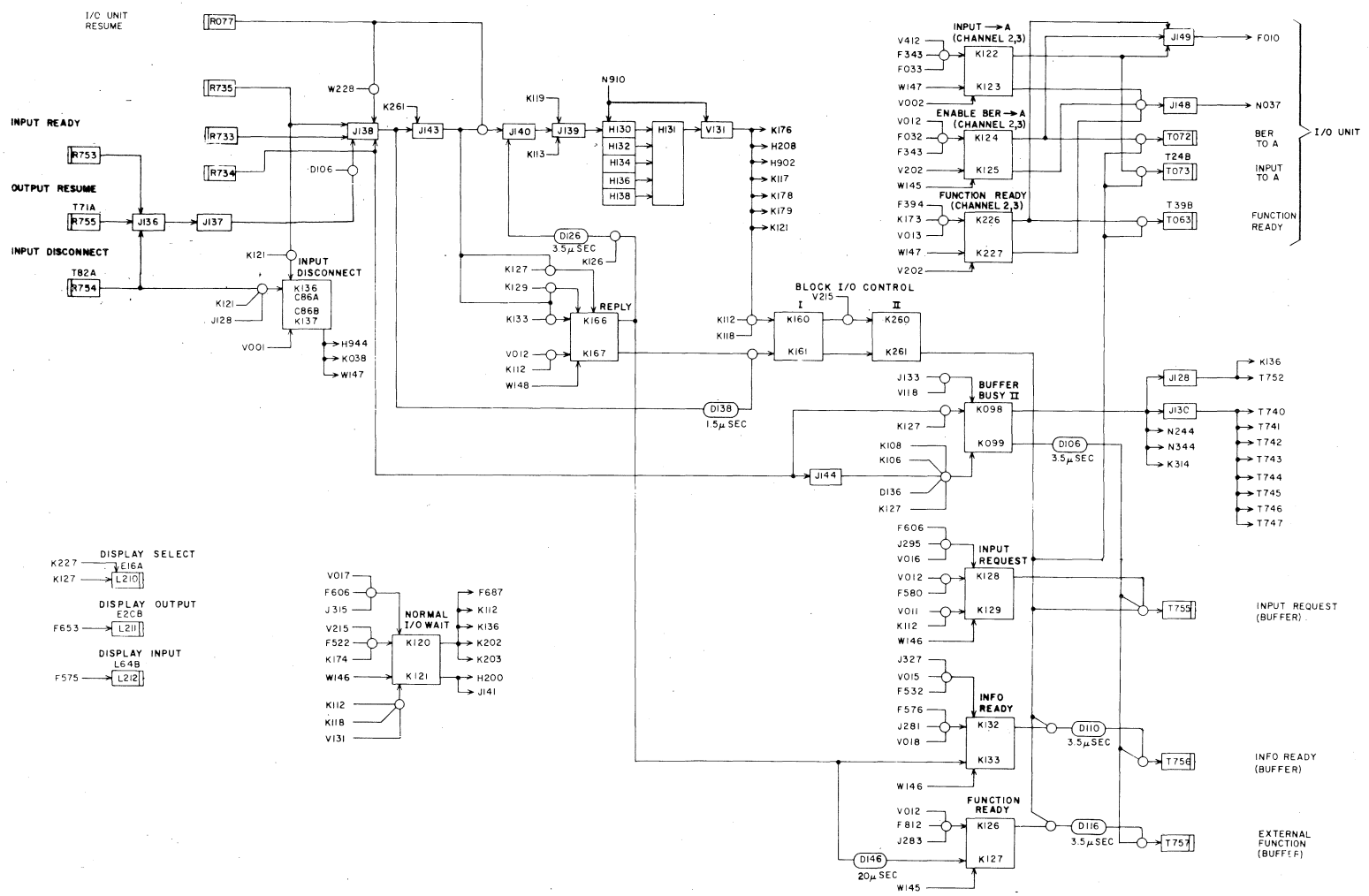


Figure 1-23. Normal I/O Control Logic (Buffer Channel)

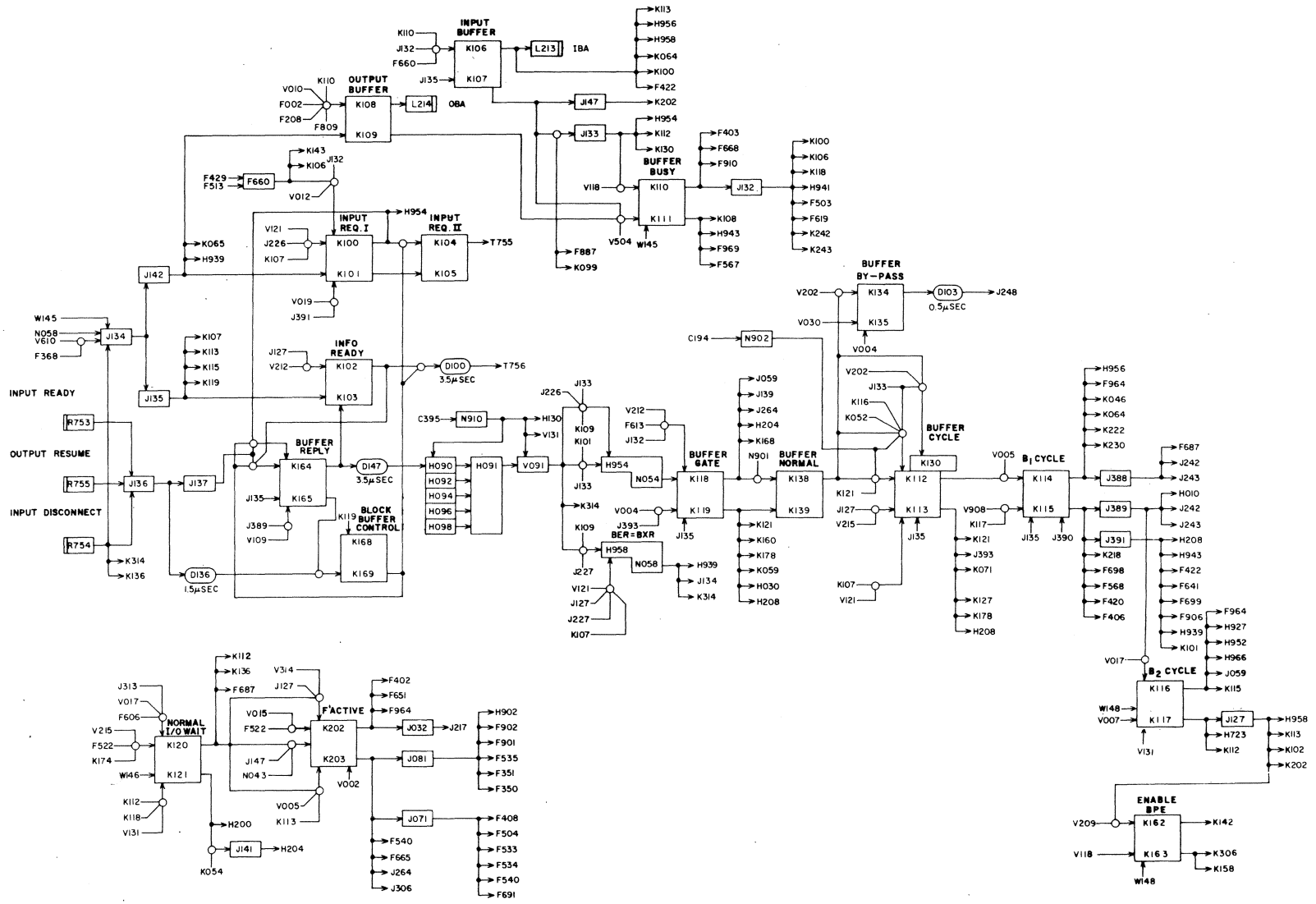


Figure 1-24. Internal Buffer Control Logic

The pulse from V121 (resume I) probes the inputs to H958/N058 and K100/K101. If the contents of BER and BXR are equal, a 1 output occurs from N058. This 1 causes the buffer control logic to be cleared, which terminates the buffer. If the contents of BER and BXR are not equal, the input request flip-flop is set and the cycle repeated.

Buffer Output

During the execution of an output buffer instruction, the buffer cycle flip-flop is set. The outputs from this flip-flop initiate the buffer cycle. During this cycle, the output buffer B_1 and B_2 flip-flops become set. The outputs of these flip-flops condition the operation of the main timing cycle to perform a buffer cycle.

When the output data is on the buffer data lines, information ready flip-flop K102/K103 sets. After a 3.5-microsecond delay, T756 sends an information ready signal to the external equipment. After the data has been processed, an output resume signal is returned to the Compute Unit. The resultant 1 output from J137 activates the buffer resync. The output of V091 produces a 1 output from H954/N094, which starts the repetition of the buffer operation.

However, when the contents of BER and BXR are equal, the output of V091 is gated into H958/N058. The resultant 1 output activates the logic which clears the buffer control logic before the next buffer cycle is initiated.

Miscellaneous Control Logic

Buffer busy flip-flop K110/K111 provides gating signals to various portions of the Compute Unit logic. This flip-flop is set if either the input buffer flip-flop or output buffer flip-flop is set.

Inverters J134, J135, and J142 function as clear logic for the buffer control logic. When there is a 1 output to J134, the resultant 1 outputs from J142 and J135 clear the buffer control logic.

Comparator

A network of inverters, Figure 1-25, compares the contents of the BER with the contents of the BXR. If contents of these registers are equal, the output of J227 is a 1. If they are not equal, the output of J226 is a 1.

Inverters J220 through J225 have AND inputs which consist of a set output from a stage of BER and a reset output from the corresponding stage in BXR or a reset output from a stage in BER and a set output from the corresponding stage of BXR.

The following combinations of inputs are possible for stage 00 or any other stage.

BER_{00}	BXR_{00}	B004	B007	B005	B006
0	0	1	0	0	1
1	1	0	1	1	0
1	0	1	1	0	0
0	1	0	0	1	1

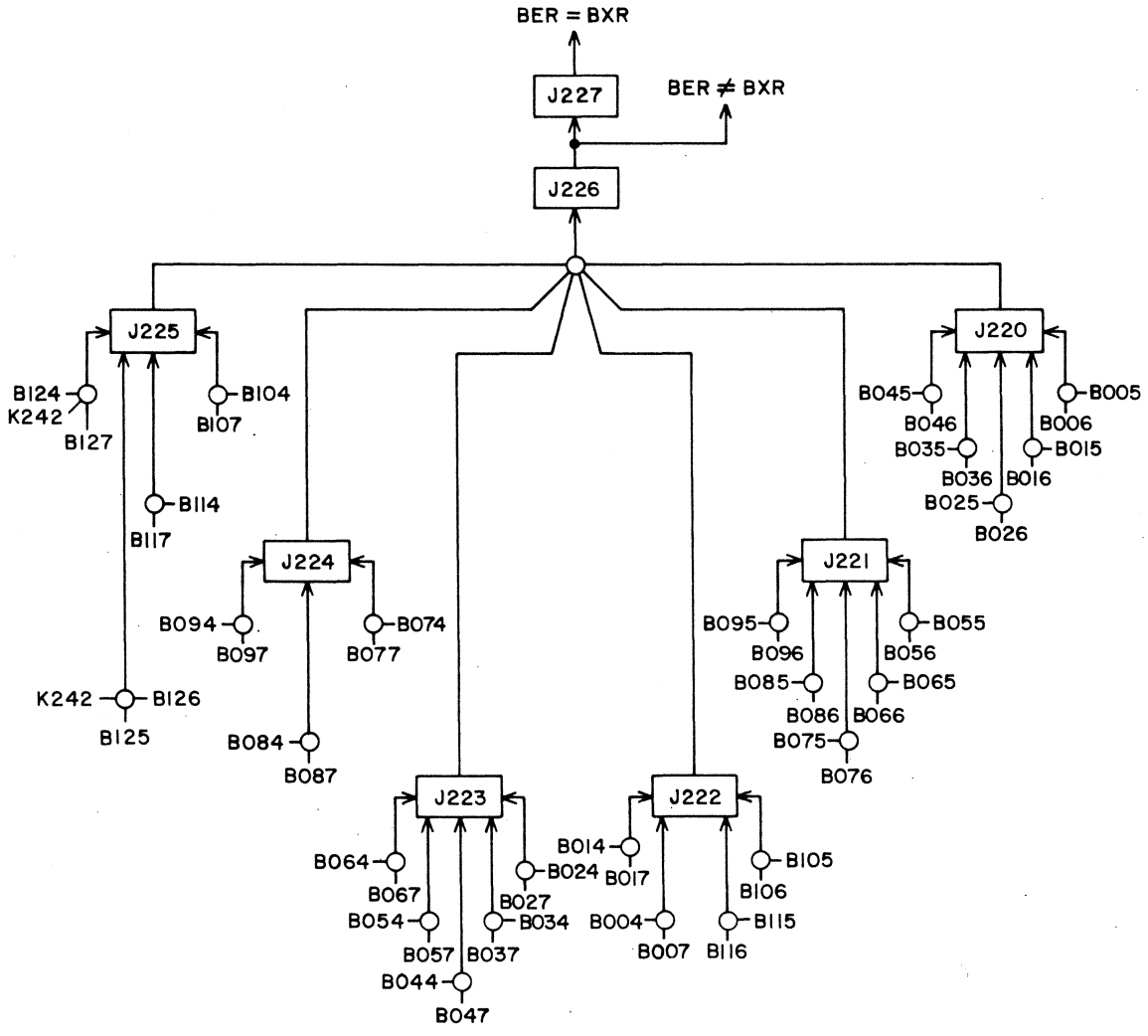


Figure 1-25. Comparator

When the contents of the two stages are equal, neither of the AND gates is satisfied. When the contents of the two stages are unequal, one of the AND gates is satisfied and the corresponding inverter has a 0 output.

Therefore, J220 through J225 all have 1 outputs only when the contents of BER equals the contents of BXR. If even one bit position is unequal, one of the preceding inverters has a 0 output.

When all of the inverters have 1 outputs, the AND input to J226 is satisfied. The resultant 0 produces a 1 output from J227. This 1 causes the buffer to be terminated.

INTERRUPTS

When the Compute Unit is first started, the start sequence initiates the interrupt timing chain, Figure 1-26. The chain continuously generates a 6-pulse count (from 0 through 5) as long as the Compute Unit is running.

The counter is a 4-stage, double-ranked counter. The transfer and advance pulses for this counter are generated by the timing chain. When the counter equals octal 13, the next advance pulse sets the counter to octal 01. Thus, the counter effectively counts from octal 01 through 13.

Each octal number represents one of the 11 (decimal) interrupts to the Compute Unit. The count assignments are as follows:

Interrupt	Count
Computer-to-computer (140)	01
Manual (10)	02
Channel 1, buffer termination (20)	03
Channel 1, interrupt 1 (30)	04
Channel 1, interrupt 2 (40)	05
Channel 2, buffer termination (100)	06
Channel 2, interrupt 1 (110)	07
Channel 2, interrupt 2 (114)	10
Channel 3, buffer termination (120)	11

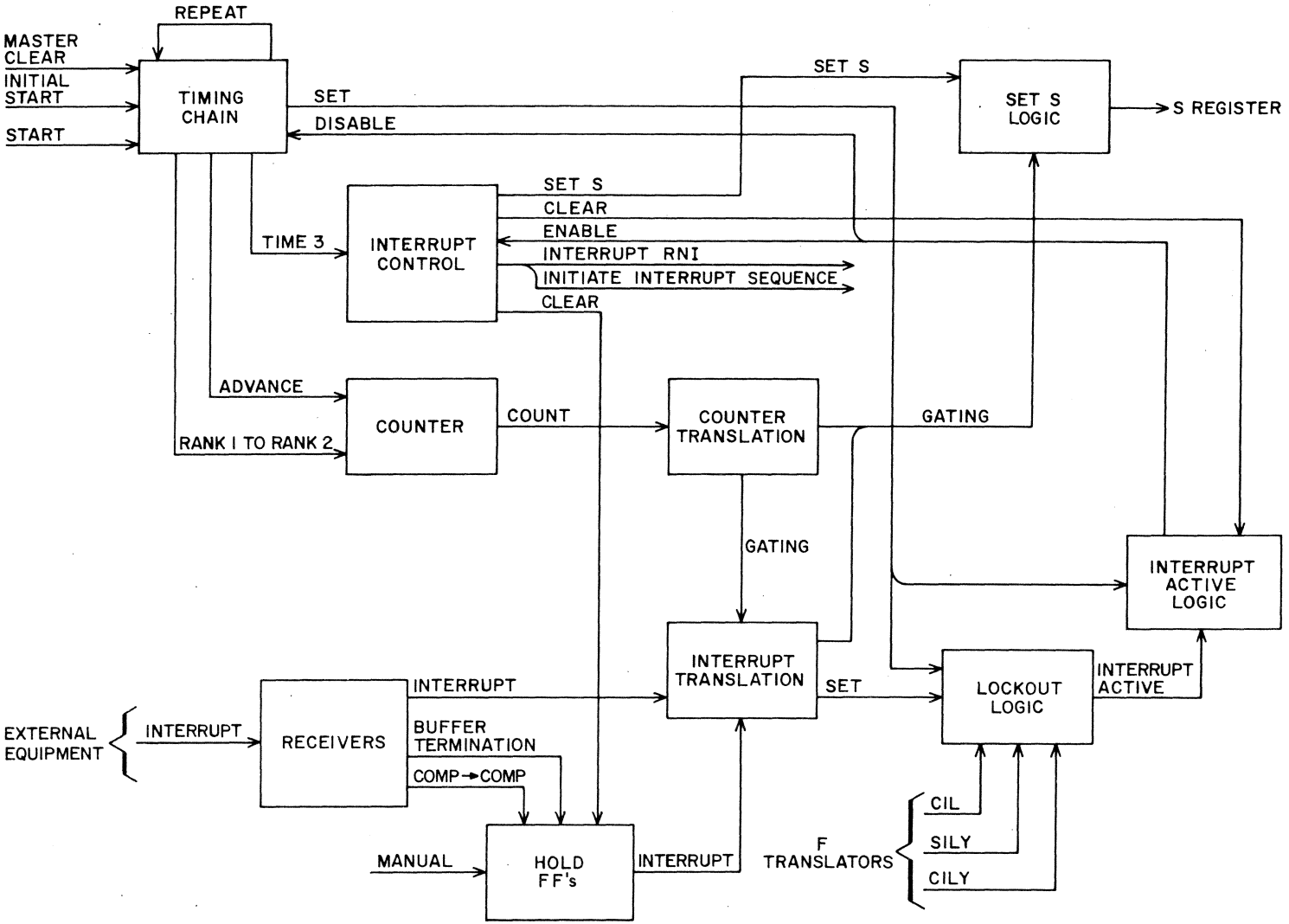


Figure 1-26. Interrupt Logic - Block Diagram

Interrupt	Count
Channel 3, interrupt 1 (130)	12
Channel 3, interrupt 2 (134)	13

The interrupt logic contains a receiver for each interrupt except manual. When a buffer termination, computer-to-computer, or manual interrupt is active, the corresponding hold flip-flop is set. The other interrupts are applied directly to the interrupt translation.

When the correct count occurs, the interrupt signal is gated into the interrupt translation. An output from this logic sets the appropriate lockout flip-flop when the interrupt is recognized.

A channel interrupt sets only the lockout for that channel. Manual or computer-to-computer interrupts set master lockout; any lockout flip-flop also can be set or cleared by programmed instruction. Execution of an EF instruction also sets master lockout.

When a set signal is generated by the timing chain, an interrupt active signal is gated into the interrupt active logic. The resultant disable signal prevents the timing chain from advancing the counter. An enable signal permits the timing chain to activate interrupt control.

Signals from the interrupt control then interrupt the next RNI sequence, cause the Compute Unit to begin an interrupt sequence, and set the S register to the control address for the active interrupt. In the 8090 mode, P is stored at the address in S in the direct bank. S is then transferred to P, and P+1 becomes the address of the next instruction. In the 8490 mode, the interrupt basically functions as a JR instruction which transfers program control to bank 00. The interrupt sequence stores (r) in the lower six bits of the location in bank 00 specified by the contents of S (the interrupt address). P is stored at the interrupt address plus one in bank 00. Program control is transferred to the interrupt address plus two in bank 00, which contains the first instruction in the interrupt routine.

The interrupt control logic also generates a clear signal which clears the interrupt active logic and the hold flip-flop associated with the interrupt designated by the counter if there is a hold flip-flop for that particular interrupt. The interrupt active logic then removes the disable signal, and the counter resumes operation.

MASTER CLOCK

The master clock network provides the timing pulses which ensure that events occur in their proper time relationship. The basic time in the Compute Unit

is the phase time, which equals 62.5 nanoseconds or one-half of the period of a clock oscillator.

The master clock consists of a master oscillator, various levels of amplification, and clock oscillators. The same type of circuit card is used throughout the master clock. The pin connections used determine the characteristics for the various usages.

The clock is connected in the form of pyramid to provide the required number of outputs with the proper synchronization. The levels of amplification provide more outputs rather than higher voltage level. The clock amplifiers are at the highest level. Each amplifier provides both even and odd outputs.

The clock amplifiers provide direct outputs only for gating internal to control delays. Timing pulses for gating between logic elements are provided by clock slaves, N9-- terms.

SECTION 1

COMPUTE UNIT

EQUIPMENT DIAGRAMS

SECTION 1

COMPUTE UNIT

LOGIC DIAGRAMS

- Symbol Index
- Logic Diagrams

A000	1H088A	A REGISTER	31
A001	1H087A	A REGISTER	31
A002	1H079A	PIGGY BACK FOR A REGISTER	31
A003	1H079B	PIGGY BACK FOR A REGISTER	31
A004	1H084A	A PRIME REGISTER	32
A005	1H083A	A PRIME REGISTER	32
A010	1I088A	A REGISTER	31
A011	1I087A	A REGISTER	31
A014	1I084A	A PRIME REGISTER	32
A015	1I083A	A PRIME REGISTER	32
A020	1J088A	A REGISTER	31
A021	1J087A	A REGISTER	31
A024	1J084A	A PRIME REGISTER	32
A025	1J083A	A PRIME REGISTER	32
A030	1K088A	A REGISTER	31
A031	1K087A	A REGISTER	31
A034	1K084A	A PRIME REGISTER	32
A035	1K083A	A PRIME REGISTER	32
A040	1L088A	A REGISTER	31
A041	1L087A	A REGISTER	31
A044	1L084A	A PRIME REGISTER	32
A045	1L083A	A PRIME REGISTER	32
A050	1M088A	A REGISTER	31
A051	1M087A	A REGISTER	31
A054	1M084A	A PRIME REGISTER	32
A055	1M083A	A PRIME REGISTER	32
A060	1M086A	A REGISTER	31
A061	1M085A	A REGISTER	31
A064	1M082A	A PRIME REGISTER	32
A065	1M081A	A PRIME REGISTER	32
A070	1L086A	A REGISTER	31
A071	1L085A	A REGISTER	31
A074	1L082A	A PRIME REGISTER	32
A075	1L081A	A PRIME REGISTER	32
A080	1K086A	A REGISTER	31
A081	1K085A	A REGISTER	31
A084	1K082A	A PRIME REGISTER	32
A085	1K081A	A PRIME REGISTER	32
A090	1J086A	A REGISTER	31
A091	1J085A	A REGISTER	31
A094	1J082A	A PRIME REGISTER	32
A095	1J081A	A PRIME REGISTER	32
A100	1I086A	A REGISTER	31
A101	1I085A	A REGISTER	31
A104	1I082A	A PRIME REGISTER	32
A105	1I081A	A PRIME REGISTER	32
A110	1H086A	A REGISTER	31
A111	1H085A	A REGISTER	31
A114	1H082A	A PRIME REGISTER	32
A115	1H081A	A PRIME REGISTER	32
A120	1G086A	A REGISTER	31
A121	1G085A	A REGISTER	31
A124	1G082A	A PRIME REGISTER	32
A125	1G081A	A PRIME REGISTER	32
B000	1G052A	RELATIVE BANK	52
B001	1H052A	RELATIVE BANK	52
B002	1H001A	BUFFER DATA REGISTER	50
B003	1H001B	BUFFER DATA REGISTER	50
B004	1H003A	BUFFER EXIT REGISTER	51
B005	1H003B	BUFFER EXIT REGISTER	51
B006	1H046A	BUFFER ENTRANCE REGISTER	51
B007	1H046B	BUFFER ENTRANCE REGISTER	51
B010	1I052A	RELATIVE BANK	52
B011	1I052B	RELATIVE BANK	52
B012	1I001A	BUFFER DATA REGISTER	50
B013	1I001B	BUFFER DATA REGISTER	50
B014	1I003A	BUFFER EXIT REGISTER	51
B015	1I003B	BUFFER EXIT REGISTER	51
B016	1I046A	BUFFER ENTRANCE REGISTER	51
B017	1I046B	BUFFER ENTRANCE REGISTER	51
B020	1J052A	RELATIVE BANK	52
B021	1J052B	RELATIVE BANK	52
B022	1J001A	BUFFER DATA REGISTER	50
B023	1J001B	BUFFER DATA REGISTER	50
B024	1J004A	BUFFER EXIT REGISTER	51
B025	1J004B	BUFFER EXIT REGISTER	51
B026	1J046A	BUFFER ENTRANCE REGISTER	51
B027	1J046B	BUFFER ENTRANCE REGISTER	51
B030	1K052A	RELATIVE BANK	52
B031	1K052B	RELATIVE BANK	52
B032	1K001A	BUFFER DATA REGISTER	50
B033	1K001B	BUFFER DATA REGISTER	50
B034	1K004A	BUFFER EXIT REGISTER	51
B035	1K004B	BUFFER EXIT REGISTER	51
B036	1K046A	BUFFER ENTRANCE REGISTER	51
B037	1K046B	BUFFER ENTRANCE REGISTER	51
B042	1L001A	BUFFER DATA REGISTER	50
B043	1L001B	BUFFER DATA REGISTER	50
B044	1L004A	BUFFER EXIT REGISTER	51
B045	1L004B	BUFFER EXIT REGISTER	51
B046	1L046A	BUFFER ENTRANCE REGISTER	51
B047	1L046B	BUFFER ENTRANCE REGISTER	51
B050	1H051A	INDIRECT BANK	52
B051	1H051B	INDIRECT BANK	52
B052	1M001A	BUFFER DATA REGISTER	50
B053	1M001B	BUFFER DATA REGISTER	50
B054	1M004A	BUFFER EXIT REGISTER	51
B055	1M004B	BUFFER EXIT REGISTER	51
B056	1M046A	BUFFER ENTRANCE REGISTER	51
B057	1M046B	BUFFER ENTRANCE REGISTER	51
B060	1I051A	INDIRECT BANK	52
B061	1I051B	INDIRECT BANK	52
B062	1M002A	BUFFER DATA REGISTER	50
B063	1M002B	BUFFER DATA REGISTER	50
B064	1M005A	BUFFER EXIT REGISTER	51
B065	1M005B	BUFFER EXIT REGISTER	51
B066	1M045A	BUFFER ENTRANCE REGISTER	51
B067	1M045B	BUFFER ENTRANCE REGISTER	51
B070	1J051A	INDIRECT BANK	52
B071	1J051B	INDIRECT BANK	52
B072	1L002A	BUFFER DATA REGISTER	50
B073	1L002B	BUFFER DATA REGISTER	50
B074	1L005A	BUFFER EXIT REGISTER	51
B075	1L005B	BUFFER EXIT REGISTER	51
B076	1L045A	BUFFER ENTRANCE REGISTER	51
B077	1L045B	BUFFER ENTRANCE REGISTER	51
B080	1K051A	INDIRECT BANK	52
B081	1K051B	INDIRECT BANK	52
B082	1K002A	BUFFER DATA REGISTER	50
B083	1K002B	BUFFER DATA REGISTER	50
B084	1K005A	BUFFER EXIT REGISTER	51
B085	1K005B	BUFFER EXIT REGISTER	51
B086	1K045A	BUFFER ENTRANCE REGISTER	51
B087	1K045B	BUFFER ENTRANCE REGISTER	51

B092	1J002A	BUFFER DATA REGISTER	50
B093	1J002B	BUFFER DATA REGISTER	50
B094	1J005A	BUFFER EXIT REGISTER	51
B095	1J005B	BUFFER EXIT REGISTER	51
B096	1J045A	BUFFER ENTRANCE REGISTER	51
B097	1J045B	BUFFER ENTRANCE REGISTER	51
B100	1H050A	DIRECT BANK	52
B101	1H050B	DIRECT BANK	52
B102	1I002A	BUFFER DATA REGISTER	50
B103	1I002B	BUFFER DATA REGISTER	50
B104	1I004A	BUFFER EXIT REGISTER	51
B105	1I004B	BUFFER EXIT REGISTER	51
B106	1I045A	BUFFER ENTRANCE REGISTER	51
B107	1I045B	BUFFER ENTRANCE REGISTER	51
B110	1I050A	DIRECT BANK	52
B111	1I050B	DIRECT BANK	52
B112	1H002A	BUFFER DATA REGISTER	50
B113	1H002B	BUFFER DATA REGISTER	50
B114	1H004A	BUFFER EXIT REGISTER	51
B115	1H004B	BUFFER EXIT REGISTER	51
B116	1H045A	BUFFER ENTRANCE REGISTER	51
B117	1H045B	BUFFER ENTRANCE REGISTER	51
B120	1J050A	DIRECT BANK	52
B121	1J050B	DIRECT BANK	52
B122	1G007A	BUFFER DATA REGISTER	50
B123	1G007B	BUFFER DATA REGISTER	50
B124	1G004A	BUFFER EXIT REGISTER	51
B125	1G004B	BUFFER EXIT REGISTER	51
B126	1G045A	BUFFER ENTRANCE REGISTER	51
B127	1G045B	BUFFER ENTRANCE REGISTER	51
B130	1K050A	DIRECT BANK	52
B131	1K050B	DIRECT BANK	52
B150	1H049A	BUFFER BANK	52
B151	1H049B	BUFFER BANK	52
B160	1I049A	BUFFER BANK	52
B161	1I049B	BUFFER BANK	52
B170	1J049A	BUFFER BANK	52
B171	1J049B	BUFFER BANK	52
B180	1K049A	BUFFER BANK	52
B181	1K049B	BUFFER BANK	52
B210	1H032B	B INVERTER	52
B211	1H030A	B INVERTER	52
B220	1I035B	B INVERTER	52
B221	1I030A	B INVERTER	52
B230	1J031B	B INVERTER	52
B231	1J030A	B INVERTER	52
B240	1K031B	B INVERTER	52
B241	1K030A	B INVERTER	52
C000	1T051A	MASTER OSC.	56
C001	1T052A	LEVEL 1 AMPLIFIER	56
C002	1S070A	LEVEL 2 AMPLIFIER	56
C003	1N080A	LEVEL 3 AMPLIFIER	56
C004	1N079A	CLOCK PYRAMID OUTPUT	56
C005	1N079B	CLOCK PYRAMID OUTPUT	56
C012	1S026A	LEVEL 2 AMPLIFIER	56
C013	1N076A	LEVEL 3 AMPLIFIER	56
C014	1L078A	CLOCK PYRAMID OUTPUT	56
C015	1L078B	CLOCK PYRAMID OUTPUT	56
C022	1S011A	LEVEL 2 AMPLIFIER	56
C023	1N073A	LEVEL 3 AMPLIFIER	56
C024	1N075A	CLOCK PYRAMID OUTPUT	56
C025	1N075B	CLOCK PYRAMID OUTPUT	56
C033	10069A	LEVEL 3 AMPLIFIER	56
C034	1G077A	CLOCK PYRAMID OUTPUT	56
C035	1G077B	CLOCK PYRAMID OUTPUT	56
C043	1P057A	LEVEL 3 AMPLIFIER	56
C044	1G078A	CLOCK PYRAMID OUTPUT	56
C045	1G078B	CLOCK PYRAMID OUTPUT	56
C053	1L027A	LEVEL 3 AMPLIFIER	56
C054	1G088A	CLOCK PYRAMID OUTPUT	56
C055	1G088B	CLOCK PYRAMID OUTPUT	56
C063	1K013A	LEVEL 3 AMPLIFIER	56
C064	1G049A	CLOCK PYRAMID OUTPUT	56
C065	1G049B	CLOCK PYRAMID OUTPUT	56
C073	1G023A	LEVEL 3 AMPLIFIER	56
C074	1G061A	CLOCK PYRAMID OUTPUT	56
C075	1G061B	CLOCK PYRAMID OUTPUT	56
C083	1F001A	LEVEL 3 AMPLIFIER	56
C084	1N057A	CLOCK PYRAMID OUTPUT	56
C085	1N057B	CLOCK PYRAMID OUTPUT	56
C093	1E001A	LEVEL 3 AMPLIFIER	56
C094	1N053A	CLOCK PYRAMID OUTPUT	56
C095	1N053B	CLOCK PYRAMID OUTPUT	56
C103	1K025A	SHIFTED CLOCK	56
C104	1N062A	CLOCK PYRAMID OUTPUT	56
C105	1N062B	CLOCK PYRAMID OUTPUT	56
C114	1G024A	CLOCK PYRAMID OUTPUT	56
C115	1G024B	CLOCK PYRAMID OUTPUT	56
C124	1R024A	CLOCK PYRAMID OUTPUT	56
C125	1R024B	CLOCK PYRAMID OUTPUT	56
C134	1P059A	CLOCK PYRAMID OUTPUT	56
C135	1P059B	CLOCK PYRAMID OUTPUT	56
C144	1N070A	CLOCK PYRAMID OUTPUT	56
C145	1N070B	CLOCK PYRAMID OUTPUT	56
C154	1D013A	CLOCK PYRAMID OUTPUT	56
C155	1D013B	CLOCK PYRAMID OUTPUT	56
C164	1D012A	CLOCK PYRAMID OUTPUT	56
C165	1D012B	CLOCK PYRAMID OUTPUT	56
C174	1P055A	CLOCK PYRAMID OUTPUT	56
C175	1P055B	CLOCK PYRAMID OUTPUT	56
C194	1C077A	CLOCK PYRAMID OUTPUT	56
C195	1C077B	CLOCK PYRAMID OUTPUT	56
C204	10068A	CLOCK PYRAMID OUTPUT	56
C205	10068B	CLOCK PYRAMID OUTPUT	56
C214	10045A	CLOCK PYRAMID OUTPUT	56
C215	10045B	CLOCK PYRAMID OUTPUT	56
C224	1L016A	CLOCK PYRAMID OUTPUT	56
C225	1L016B	CLOCK PYRAMID OUTPUT	56
C234	1N091A	CLOCK PYRAMID OUTPUT	56
C235	1N091B	CLOCK PYRAMID OUTPUT	56
C244	1N086A	CLOCK PYRAMID OUTPUT	56
C245	1N086B	CLOCK PYRAMID OUTPUT	56
C254	1M009A	CLOCK PYRAMID OUTPUT	56
C255	1M009B	CLOCK PYRAMID OUTPUT	56
C264	10074A	CLOCK PYRAMID OUTPUT	56
C265	10074B	CLOCK PYRAMID OUTPUT	56
C274	1F075A	CLOCK PYRAMID OUTPUT	56
C275	1F075B	CLOCK PYRAMID OUTPUT	56
C284	1E085A	CLOCK PYRAMID OUTPUT	56
C285	1E085B	CLOCK PYRAMID OUTPUT	56
C294	1E094A	CLOCK PYRAMID OUTPUT	56
C295	1E094B	CLOCK PYRAMID OUTPUT	56
C304	10019A	CLOCK PYRAMID OUTPUT	56
C305	10019B	CLOCK PYRAMID OUTPUT	56

C314	1N018A	CLOCK PYRAMID OUTPUT	56
C315	1N018B	CLOCK PYRAMID OUTPUT	56
C324	1L014A	CLOCK PYRAMID OUTPUT	56
C325	1L014B	CLOCK PYRAMID OUTPUT	56
C334	1K016A	CLOCK PYRAMID OUTPUT	56
C335	1K016B	CLOCK PYRAMID OUTPUT	56
C344	1H020A	CLOCK PYRAMID OUTPUT	56
C345	1H020B	CLOCK PYRAMID OUTPUT	56
C354	1H018A	CLOCK PYRAMID OUTPUT	56
C355	1H018B	CLOCK PYRAMID OUTPUT	56
C364	1G022A	CLOCK PYRAMID OUTPUT	56
C365	1G022B	CLOCK PYRAMID OUTPUT	56
C374	1F015A	CLOCK PYRAMID OUTPUT	56
C375	1F015B	CLOCK PYRAMID OUTPUT	56
C385	1K015B	SHIFTED CLOCK	56
C395	1D078B	SHIFTED CLOCK	56
C405	1P056B	SHIFTED CLOCK	56
D000	1A046A	X DRIVER ADDRESS - XX$_0$XX$_0$ R	44
D001	1A046B	X DRIVER ADDRESS - XX$_0$XX$_0$ W	44
D002	1A041A	X DRIVER ADDRESS - 0X$_0$XX$_0$ R OR 1X$_0$XX$_0$ W	44
D003	1A041B	X DRIVER ADDRESS - 0X$_0$XX$_0$ W OR 1X$_0$XX$_0$ R	44
D004	1A036A	X DRIVER ADDRESS - XX$_1$XX$_0$ R	44
D005	1A036B	X DRIVER ADDRESS - XX$_1$XX$_0$ W	44
D006	1A031A	X DRIVER ADDRESS - 0X$_1$XX$_0$ R OR 1X$_1$XX$_0$ W	44
D007	1A031B	X DRIVER ADDRESS - 0X$_1$XX$_0$ W OR 1X$_1$XX$_0$ R	44
D008	1B046A	X DRIVER ADDRESS - XX$_0$XX$_1$ R	44
D009	1B046B	X DRIVER ADDRESS - XX$_0$XX$_1$ W	44
D010	1B041A	X DRIVER ADDRESS - 0X$_0$XX$_1$ R OR 1X$_0$XX$_1$ W	44
D011	1B041B	X DRIVER ADDRESS - 0X$_0$XX$_1$ W OR 1X$_0$XX$_1$ R	44
D012	1B036A	X DRIVER ADDRESS - XX$_1$XX$_1$ R	44
D013	1B036B	X DRIVER ADDRESS - XX$_1$XX$_1$ W	44
D014	1B031A	X DRIVER ADDRESS - 0X$_1$XX$_1$ R OR 1X$_1$XX$_1$ W	44
D015	1B031B	X DRIVER ADDRESS - 0X$_1$XX$_1$ W OR 1X$_1$XX$_1$R	44
D100	1A080A	3.5 MICRO SEC DELAY-BUFFER INFO. READY	48
D103	1N085A	.5 MICRO SEC DELAY - BUFFER BY PASS	48
D104	1T075A	5.5 MILLISEC DELAY-CYCLE STEP	12
D105	1F046A	1 MICRO SEC DELAY-REQUEST MEMORY	41
D106	1A083A	3.5 MICRO SEC DELAY-BUFFER CABLE SELECT CONTROL	47
D110	1A085A	3.5 MICRO SEC DELAY-INFO READY-BUFFER AND NORMAL	47
D116	1B081A	3.5 MICRO SEC DELAY-FCTN READY-BUFFER AND NORMAL	47
D126	1D091A	3.5 MICRO SEC DELAY-NORMAL REPLY-NORMAL RESYNC	47
D134	1A081A	.2 MICRO SEC DELAY-BUFFER DISCONNECT	48
D136	1B089A	1.5 MICRO SEC DELAY-BLOCK BUFFER CONTROL(CLEAR)	48
D138	1D085A	1.5 MICRO SEC DELAY-BLOCK I/O CONTROL	47
D142	1G021A	5 MICRO SEC DELAY-MASTER CLEAR	41
D146	1B085A	20 MICRO SEC DELAY-FUNCTION READY	47
D147	1A084A	3.5 MICRO SEC DELAY-BUFFER RESYNC	48
D200	1C039A	Y DRIVER ADDRESS - 0XX0XX$_0$ R	45
D201	1C039B	Y DRIVER ADDRESS - 0XX0XX$_0$ W	45
D202	1C034A	Y DRIVER ADDRESS - 00X0XX$_0$ W RO 01X0XX$_0$ R	45
D203	1C034B	Y DRIVER ADDRESS - 00X0XX$_0$ R OR 01X0XX$_0$ W	45
D204	1C033A	Y DRIVER ADDRESS - 0XX1XX$_0$ R	45
D205	1C033B	Y DRIVER ADDRESS - 0XX1XX$_0$ W	45
D206	1C028A	Y DRIVER ADDRESS - 00X1XX$_0$ W OR 01X1XX$_0$ R	45
D207	1C028B	Y DRIVER ADDRESS - 00X1XX$_0$ R OR 01X1XX$_0$ W	45
D208	1C045A	Y DRIVER ADDRESS - 0XX0XX$_1$ R	45
D209	1C045B	Y DRIVER ADDRESS - 0XX0XX$_1$ W	45
D210	1C040A	Y DRIVER ADDRESS - 00X0XX$_1$ W OR 01X0XX$_1$ R	45
D211	1C040B	Y DRIVER ADDRESS - 00X0XX$_1$ R OR 01X0XX$_1$ W	45
D212	1D046A	Y DRIVER ADDRESS - 0XX1XX$_1$ R	45
D213	1D046B	Y DRIVER ADDRESS - 0XX1XX$_1$ W	45
D214	1D041A	Y DRIVER ADDRESS - 00X1XX$_1$ W OR 01X1XX$_1$ R	45
D215	1D041B	Y DRIVER ADDRESS - 00X1XX$_1$ R OR 01X1XX$_1$ W	45
D216	1D032A	Y DRIVER ADDRESS - 1XX0XX$_0$ R	46
D217	1D032B	Y DRIVER ADDRESS - 1XX0XX$_0$ W	46
D218	1D027A	Y DRIVER ADDRESS - 10X0XX$_0$ W OR 11X$_0$XX$_0$ R	46
D219	1D027B	Y DRIVER ADDRESS - 10X0XX$_0$ R OR 11X$_0$XX$_0$ W	46
D220	1E033A	Y DRIVER ADDRESS - 1XX1XX$_0$ R	46
D221	1E033B	Y DRIVER ADDRESS - 1XX1XX$_0$ W	46
D222	1E028A	Y DRIVER ADDRESS - 10X1XX$_0$ W OR 11X$_1$XX$_0$ R	46
D223	1E028B	Y DRIVER ADDRESS - 10X1XX$_0$ R OR 11X$_1$XX$_0$ W	46
D224	1E045A	Y DRIVER ADDRESS - 1XX0XX$_1$ R	46
D225	1E045B	Y DRIVER ADDRESS - 1XX0XX$_1$ W	46
D226	1E040A	Y DRIVER ADDRESS - 10X0XX$_1$ W OR 11X$_0$XX$_1$ R	46
D227	1E040B	Y DRIVER ADDRESS - 10X0XX$_1$ R OR 11X$_0$XX$_1$ W	46
D228	1E039A	Y DRIVER ADDRESS - 1XX1XX$_1$ R	46
D229	1E039B	Y DRIVER ADDRESS - 1XX1XX$_1$ W	46
D230	1E034A	Y DRIVER ADDRESS - 10X1XX$_1$ W OR 11X$_1$XX$_1$ R	46
D231	1E034B	Y DRIVER ADDRESS - 10X1XX$_1$ R OR 11X$_1$XX$_1$ W	46
D999	1B019A	.1 MICRO SEC DELAY-MANUAL INTERRUPT	54
E000	1H094A	STAGE ENABLE - BIT 0	39
E001	1H091A	NOT STAGE ENABLE - BIT 0	39
E002	1H089A	STAGE BORROW - BIT 0	39
E010	1I094A	STAGE ENABLE - BIT 1	39
E011	1I091A	NOT STAGE ENABLE - BIT 1	39
E012	1I089A	STAGE BORROW BIT 1	39
E020	1J094A	STAGE ENABLE - BIT 2	39
E021	1J091A	NOT STAGE ENABLE - BIT 2	39
E022	1J089A	STAGE BORROW - BIT 2	39
E030	1K094A	STAGE ENABLE - BIT 3	39
E031	1K091A	NOT STAGE ENABLE - BIT 3	39
E032	1K089A	STAGE BORROW - BIT 3	39
E040	1L090A	STAGE ENABLE - BIT 4	39
E041	1L091A	NOT STAGE ENABLE - BIT 4	39
E042	1L089A	STAGE BORROW - BIT 4	39
E050	1M090A	STAGE ENABLE - BIT 5	39
E051	1M091A	NOT STAGE ENABLE - BIT 5	39
E052	1M089A	STAGE BORROW - BIT 5	39
E060	1M090B	STAGE ENABLE - BIT 6	39
E061	1M091B	NOT STAGE ENABLE - BIT 6	39
E062	1M089B	STAGE BORROW - BIT 6	39
E070	1L090B	STAGE ENABLE - BIT 7	39
E071	1L091B	NOT STAGE ENABLE - BIT 7	39
E072	1L089B	STAGE BORROW - BIT 7	39
E080	1K094B	STAGE ENABLE - BIT 8	39
E081	1K091B	NOT STAGE ENABLE BIT 8	39
E082	1K089B	STAGE BORROW - BIT 8	39
E090	1J094B	STAGE ENABLE BIT 9	39
E091	1J091B	NOT STAGE ENABLE - BIT 9	39
E092	1J089B	STAGE BORROW - BIT 9	39
E100	1I094B	STAGE ENABLE - BIT 10	39
E101	1I091B	NOT STAGE ENABLE - BIT 10	39
E102	1I089B	STAGE BORROW - BIT 10	39
E103	1G091A	STAGE ENABLE - BIT 10	39
E110	1H094B	STAGE ENABLE - BIT 11	39
E111	1H091B	NOT STAGE ENABLE - BIT 11	39
E112	1H089B	STAGE BORROW - BIT 11	39
E113	1G091B	STAGE ENABLE - BIT 11	39
E120	1G090B	STAGE ENABLE - BIT 12	39
E121	1G090A	NOT STAGE ENABLE - BIT 12	39
E122	1G089B	STAGE BORROW - BIT 12	39
E200	1H092A	NOT GROUP ENABLE	39
E201	1M092A	NOT GROUP ENABLE	39
E202	1M092B	NOT GROUP ENABLE	39
E203	1H092B	NOT GROUP ENABLE	39
E300	1J092A	NOT GROUP BORROW	39

E301	1K092A	NOT GROUP BORROW	39
E302	1J090A	NOT GROUP BORROW	39
E303	1I092A	NOT GROUP BORROW	39
E310	1G092A	GROUP BORROW	39
E311	1G092B	NO GROUP BORROW	39
E400	1I093A	GROUP BORROW INPUT	39
E401	1J093A	GROUP BORROW INPUT	39
E402	1K093A	GROUP BORROW INPUT	39
E403	1L093A	GROUP BORROW INPUT	39
E500	1H093A	STAGE PROBE INPUT	39
E501	1H093B	STAGE PROBE INPUT	39
E502	1I090A	STAGE PROBE INPUT	39
E503	1K090A	STAGE PROBE INPUT	39
E504	1L094A	STAGE PROBE INPUT	39
E505	1M093A	STAGE PROBE INPUT	39
E506	1M094B	STAGE PROBE INPUT	39
E507	1L094B	STAGE PROBE INPUT	39
E508	1L092A	STAGE PROBE INPUT	39
E509	1G094A	STAGE PROBE INPUT	39
E510	1G094B	STAGE PROBE INPUT	39
E511	1H090A	STAGE PROBE INPUT	39
E512	1G093A	STAGE PROBE INPUT	39
E513	1G089A	END AROUND BORROW	39
E514	1F089B	NOT END AROUND BORROW GENERATED	39
E515	1F090B	END AROUND BORROW GENERATED	39
E820	1A030A	X DRIVE SELECTOR	44
E821	1A030B	X DRIVE SELECTOR	44
E822	1A029A	X DRIVE SELECTOR	44
E823	1A029B	X DRIVE SELECTOR	44
E824	1B030A	X DRIVE SELECTOR	44
E825	1B030B	X DRIVE SELECTOR	44
E826	1B029A	X DRIVE SELECTOR	44
E827	1B029B	X DRIVE SELECTOR	44
E830	1C026A	X DRIVE SELECTOR	45
E831	1C026B	X DRIVE SELECTOR	45
E832	1C025A	X DRIVE SELECTOR	45
E833	1C025B	X DRIVER SELECTOR	45
E834	1D026A	X DRIVER SELECTOR	45
E835	1D026B	X DRIVER SELECTOR	45
E836	1D025A	X DRIVER SELECTOR	45
E837	1D025B	X DRIVER SELECTOR	45
E838	1E026A	X DRIVER SELECTOR	46
E839	1E026B	X DRIVER SELECTOR	46
E840	1E025A	X DRIVER SELECTOR	46
E841	1F025B	X DRIVER SELECTOR	46
E902	1F033A	DELAY LINE-TIME 50	40
E904	1F033B	DELAY LINE-TIME 100	40
E906	1F033C	DELAY LINE-TIME 150	40
E910	1F033D	DELAY LINE-TIME 250	40
E914	1F026A	DELAY LINE-TIME 350	40
E915	1F026B	DELAY LINE-TIME 375	40
E918	1F026C	DELAY LINE-TIME 450	40
E919	1F026D	DELAY LINE-TIME 475	40
E925	1F025A	DELAY LINE-TIME 625	40
E929	1F025B	DELAY LINE-TIME 725	40
E935	1F025C	DELAY LINE-TIME 875	40
E938	1F025D	DELAY LINE-TIME 950	40
E940	1F024A	DELAY LINE-TIME 1000	40
E941	1F024B	DELAY LINE-TIME 1025	40
E943	1F024D	DELAY LINE-TIME 1075	40
E948	1F024C	DELAY LINE-TIME 1200	40
F000	1S001A	F REGISTER	14
F001	1S002A	F REGISTER	14
F002	1S003A	F REGISTER INVERTER	14
F003	1S003B	F REGISTER INVERTER	14
F004	1S004A	F PRIME REGISTER	14
F005	1S004B	F PRIME REGISTER	14
F010	1S006A	F REGISTER	14
F011	1S007A	F REGISTER	14
F012	1S008A	F REGISTER INVERTER	14
F013	1S008B	F REGISTER INVERTER	14
F014	1S009A	F PRIME REGISTER	14
F015	1S009B	F PRIME REGISTER	14
F020	1S012A	F REGISTER	14
F021	1S013A	F REGISTER	14
F022	1S014A	F REGISTER INVERTER	14
F023	1S014B	F REGISTER INVERTER	14
F024	1S015A	F PRIME REGISTER	14
F025	1S015B	F PRIME REGISTER	14
F030	1S017A	F REGISTER	14
F031	1S018A	F REGISTER	14
F032	1S019A	F REGISTER INVERTER	14
F033	1S019B	F REGISTER INVERTER	14
F034	1S020A	F PRIME REGISTER	14
F035	1S020B	F PRIME REGISTER	14
F038	1S021A	F REGISTER INVERTER	14
F040	1S022A	F REGISTER	14
F041	1S023A	F REGISTER	14
F042	1S024A	F REGISTER INVERTER	14
F043	1S024B	F REGISTER INVERTER	14
F044	1S025A	F PRIME REGISTER	14
F045	1S025B	F PRIME REGISTER	14
F048	1S027A	F REGISTER INVERTER	14
F050	1S028A	F REGISTER	15
F051	1S029B	F REGISTER	15
F052	1S030A	F REGISTER INVERTER	15
F053	1S030B	F REGISTER INVERTER	15
F058	1S031A	F REGISTER INVERTER	15
F060	1S032A	F REGISTER	15
F061	1S033B	F REGISTER	15
F062	1S034A	F REGISTER INVERTER	15
F063	1S034B	F REGISTER INVERTER	15
F068	1S031B	F REGISTER INVERTER	15
F070	1S040A	F REGISTER	15
F071	1S041B	F REGISTER	15
F072	1S042A	F REGISTER INVERTER	15
F073	1S042B	F REGISTER INVERTER	15
F078	1N092B	F REGISTER INVERTER	15
F079	1S043A	F REGISTER INVERTER	15
F080	1S049A	F REGISTER	15
F081	1S050B	F REGISTER	15
F082	1S051A	F REGISTER INVERTER	15
F083	1S051B	F REGISTER INVERTER	15
F088	1S052A	F REGISTER INVERTER	15
F089	1S052B	F REGISTER INVERTER	15
F090	1S057A	F REGISTER	15
F091	1S058B	F REGISTER	15
F092	1S059A	F REGISTER INVERTER	15
F093	1S059B	F REGISTER INVERTER	15
F098	1S060A	F REGISTER INVERTER	15
F099	1S060B	F REGISTER INVERTER	15
F100	1S065A	F REGISTER	15
F101	1S066B	F REGISTER	15
F102	1S067A	F REGISTER INVERTER	15

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F103  1S067B  F REGISTER INVERTER
F108  1S068A  F REGISTER INVERTER
F109  1S068B  F REGISTER INVERTER
F110  1S074A  F REGISTER
F111  1S075B  F REGISTER
F112  1S076A  F REGISTER INVERTER
F113  1S076B  F REGISTER INVERTER
F118  1S077A  F REGISTER INVERTER
F119  1Q063A  F REGISTER INVERTER
F120  1S082A  F REGISTER
F121  1S083B  F REGISTER
F122  1S084A  F REGISTER INVERTER
F123  1S084B  F REGISTER INVERTER
F126  1R072B  F REGISTER INVERTER
F128  1S085A  F REGISTER INVERTER
F129  1S087B  F REGISTER INVERTER
F140  1R010A  F PRIME = X0     INP
F141  1R010B  F PRIME = X1     EXF
F142  1R008A  F PRIME = X2
F143  1R008B  F PRIME = X3     EXC+EXCY
F144  1R007A  F PRIME = X4     INA
F145  1R007B  F PRIME = X5     OTA+OTN
F146  1R006A  F PRIME = X6     OUT
F147  1R006B  F PRIME = X7     INAY+ETAY
F180  1S002B  PIGGY BACK FOR F REGISTER - BIT 1
F182  1Q001A  PIGGY BACK FOR F REGISTER - BIT 2
F190  1R004B  F PRIME = XXXX0
F191  1R004A  F PRIME = XXXX1
F192  1R009B  F PRIME = XXX0X
F193  1R009A  F PRIME = XXX1X
F194  1R015B  F PRIME = XX0XX
F195  1R015A  F PRIME = XX1XX
F197  1R020A  F PRIME = X1XXX
F200  1S041A  F=1X3 OR 1X7
F201  1S050A  F=1X3 OR 1X7
F202  1S066A  F = 0X
F203  1S058A  F = 0X
F204  1S069B  F = 6X+7X
F205  1R017A  E = NOT 00
F206  1R018A  E = 00
F208  1R022B  E = 00+01
F210  1R021B  E = NOT 0X
F211  1R021A  E = NOT 1X
F212  1R028B  E=NOT 2X
F213  1R028A  E=NOT 3X
F214  1R029B  E=NOT 4X
F215  1R029A  E=NOT 5X
F216  1R030B  E=NOT 6X
F217  1R030A  E=NOT 7X
F220  1Q006B  E=NOT X0
F221  1Q006A  E=NOT X1
F222  1Q007B  E=NOT X2
F223  1Q007A  E=NOT X3
F224  1Q008B  E=NOT X4
F225  1Q008A  E=NOT X5
F226  1Q009B  E=NOT X6
F227  1Q009A  E=NOT X7
F228  1S056A  F=00
F229  1R059A  F=01
F231  1R016A  F=NOT 01
F232  1R055B  F=NOT 01
F233  1R054B  F=NOT 01

15    F234  1S055A  F=77                                  12
15    F235  1S065B  F=NOT 01                              17
15    F236  1S057B  F=NOT 01                              17
15    F240  1R056B  F=NOT 00                              17
15    F241  1R056A  F=NOT 00                              17
15    F250  1R031B  E=NOT 0X                              19
15    F251  1R031A  E=NOT 1X                              19
15    F260  1R073A  F=NOT 00XXXX                          17
15    F261  1R074B  F=NOT 10XXXX                          17
15    F262  1R074A  F=NOT 11XXXX                          17
15    F263  1R057B  F=NOT XX00XX                          17
15    F264  1R057A  F=NOT XX01XX                          17
15    F265  1R058B  F=NOT XX10XX                          17
15    F266  1R058A  F=NOT XX11XX                          17
15    F267  1S039B  F=NOT XXXX00                          17
15    F268  1S039A  F=NOT XXXX01                          17
14    F269  1S038B  F=NOT XXXX10                          17
14    F270  1S038A  F=NOT XXXX11                          17
14    F272  1R073B  F=NOT 11XXXX                          19
14    F301  1R070A  LP                                    16
14    F302  1S061A  SC                                    16
14    F303  1S061B  LD                                    16
14    F304  1S062A  LC                                    16
14    F305  1S062B  AD                                    16
14    F306  1S063A  SB                                    16
14    F307  1S063B  ST                                    16
14    F308  1S064A  SR                                    16
14    F309  1S064B  RA                                    16
14    F310  1S071B  AQ                                    16
14    F311  1S072A  LQ                                    16
14    F312  1S073A  SQ                                    16
14    F313  1S078A  MU                                    16
14    F314  1S079A  DV                                    16
16    F315  1S071A  A JUMPS FORWARD                       16
16    F316  1S080A  A JUMPS BACKWARD                      16
16    F317  1S080B  A JUMPS - EM                          16
16    F318  1S046B  DIRECT (D)                            16
16    F319  1R069A  MEMORY (M)                            16
16    F320  1R068A  INDIRECT (I)                          16
12    F321  1R067A  SPECIFIC                              16
16    F322  1R066A  BACKWARD                              16
19    F323  1R065A  CONSTANT                              16
19    F324  1R064A  FORWARD                               16
19    F325  1R063B  ENTIRE MEMORY (EM)                    16
19    F328  1R061B  MEMORY INDEX (MX)                     16
19    F329  1R060A  AR+AQR IF G SHIFT                     16
19    F330  1R060B  AL+AQL IF G SHIFT                     16
19    F333  1Q080A  AQL IF G SHIFT                        16
19    F334  1R072A  NOT-AQR IF G SHIFTS+MU                16
19    F335  1R061A  G SHIFTS                              16
19    F336  1R079A  NOP                                   16
19    F337  1S093B  BBCY                                  18
19    F338  1S092A  SIC                                   18
19    F339  1S094A  ATEY+ATXY                             18
19    F340  1S093A  IRJ                                   18
19    F341  1R064B  JPRG                                  17
19    F342  1S075A  SDC                                   18
12    F343  1P024A  ETAY+INAY                             18
17    F344  1R092A  DRJ                                   18
17    F345  1S091B  MTM2                                  19
17    F346  1R089A  SID                                   18
17    F347  1R091A  IBIY+IBOY                             18
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F348  1L058B  G SHIFTS                                                                  16
F350  1K028B  NOT-(ETAY+INAY)(F*)                                                       35
F351  1J028B  NOT-(ETAY+INAY)(F*)                                                       35
F358  1Q085B  ACJ                                                                       18
F360  1Q085A  BLS                                                                       18
F361  1R090A  CTCI                                                                      18
F362  1R088A  PTA                                                                       18
F363  1R081A  JPI                                                                       17
F364  1Q013A  LS1+LS2                                                                   18
F365  1S088B  CTA+CTAQ                                                                  19
F367  1Q028A  RCJP                                                                      18
F368  1Q027A  CBC                                                                       18
F369  1Q026A  XAQ                                                                       18
F370  1Q029A  ATE                                                                       18
F371  1P088A  ERTA                                                                      18
F372  1Q033A  ATX                                                                       18
F373  1R033A  NOP                                                                       18
F374  1R034A  ETA                                                                       18
F375  1R035A  NOP                                                                       18
F376  1R036A  LS3                                                                       18
F378  1S036A  LS6                                                                       18
F380  1R037A  MUT                                                                       18
F382  1R042A  MUH                                                                       18
F384  1R022A  RS1+RS2                                                                   18
F385  1R044A  NOP                                                                       18
F386  1S053A  NOP                                                                       19
F388  1S083A  CIL+CILY                                                                  19
F389  1Q025A  NOT SILY                                                                  19
F391  1S088A  SBU                                                                       19
F392  1S091A  CBCY                                                                      19
F393  1S089A  STP                                                                       19
F394  1S090B  EXCY                                                                      19
F395  1S090A  STE                                                                       19
F396  1Q071A  LPN                                                                       17
F397  1Q070A  SCN                                                                       17
F398  1Q068A  LDN                                                                       17
F399  1Q067A  LCN                                                                       17
F400  1S094B  NOT DV                                                                    16
F401  1M054B  NOT MU                                                                    16
F402  1Q062A  NOT-BLS+INP.F PRIME.D+(INP+OUT).C                                         22
F403  1D076B  BLS . BUFFER NOT BUSY                                                     28
F404  1N093B  EXC+EXF+EXCY                                                              54
F405  1P005A  INP . F PRIME                                                             26
F406  1G039B  STE+ETA+BLS. A. BUFFER NOT BUSY+B1                                        22
F407  1P084A  EXC+EXF+EXCY                                                              26
F408  1N064A  NOT - LDN+(EXC+EXF+EXCY).B+LD.D+INA(F*).D                                 24
F409  1Q084B  INP+OUT                                                                   24
F410  1S049B  NOT EM                                                                    16
F412  1S053B  NOT CONSTANT                                                              16
F413  1N061B  NOT-EXC+EXF+EXCY                                                          26
F414  1Q083A  NOT-OTN+ETAY+INAY+INA+OTA                                                 26
F415  1R027A  E=77                                                                      12
F416  1P011B  (INP+OUT).C                                                               26
F417  1P074A  NOT-(INP+OUT).B                                                           24
F418  1Q071B  NOT-(INP+OUT).C                                                           26
F419  1L043B  (INAY+ETAY)(F*)+ERTA                                                      24
F420  1H022A  OUT.C+B1                                                                  27
F421  1F060A  INP(F*).D+OUT.C                                                           22
F422  1E071B  NOT-INPUT BUFFER.B1                                                       27
F423  1I031A  NOT-(AD+SB+LC+SC+LP+RA+AO+INP(F*)).D+ADN+SBN                              55
F424  1J041B  (AD+SB+RA+AO).D+ADN+SBN                                                   55
F425  1Q087B  NOT BLS                                                                   18
F426  1P005B  NOT STE                                                                   19
F427  1R034B  NOT ETA                                                                   18
F428  1Q073B  NOT-EXC+EXF                                                               17
F429  1R078B  NOT-IRI+INP                                                               17
F430  1T094A  NOT EXCY                                                                  19
F431  1R077B  NOT-IRO+OUT                                                               17
F432  1R076B  NOT NOP                                                                   17
F433  1Q026B  NOT XAQ                                                                   18
F434  1Q025B  NOT SRJ                                                                   18
F435  1R094A  NOT BRCY                                                                  18
F437  1N036A  NOT-ATEY+ATXY                                                             18
F438  1R093B  NOT IRJ                                                                   18
F442  1R040B  NOT DRJ                                                                   18
F443  1Q066B  BLS                                                                       18
F446  1Q088B  NOT ACJ                                                                   18
F450  1R086B  NOT-LS1+LS2                                                               18
F451  1R084B  NOT JPI                                                                   17
F456  1Q029B  NOT ATE                                                                   18
F457  1Q032B  NOT ERTA                                                                  18
F458  1Q033B  NOT ATX                                                                   18
F459  1R033B  NOT NOP                                                                   18
F460  1R036B  NOT - LS3                                                                 18
F461  1R035B  NOT NOP                                                                   18
F462  1S036B  NOT - LS6                                                                 18
F466  1R042B  NOT - MUH                                                                 18
F467  1M006B  NOT RCJP                                                                  18
F468  1R087B  NOT - RS1+RS2                                                             18
F471  1R044B  NOP                                                                       18
F478  1T094B  NOT - STP                                                                 19
F483  1Q068B  NOT - LDN                                                                 17
F484  1Q067B  NOT - LCN                                                                 17
F486  1Q065B  NOT - SBN                                                                 17
F487  1Q064B  NOT UJ                                                                    17
F488  1Q083B  NOT DR                                                                    17
F491  1Q080B  NOT - HW                                                                  17
F492  1R083B  NOT - JPR+JFI                                                             17
F493  1Q074B  NOT - OTN                                                                 17
F494  1Q072B  NOT-INA+HW1+OTA                                                           17
F498  1Q069A  JR                                                                        17
F499  1Q069B  NOT JR                                                                    17
F500  1Q052B  (MU+DV).D                                                                 16
F501  1R038B  DV                                                                        16
F502  1P093B  MU                                                                        16
F503  1R053B  NOT-SWEEP+ENTER+BLS.BUFFER NOT BUSY                                       26
F504  1R005A  NOT-RNI+BLS.BUFFER NOT BUSY+INP(F*)+BUFFER CYCLE                          26
F505  1P084B  MU+DV                                                                     16
F506  1N063B  LDN+(EXC+EXF+EXCY).B+INA(F*).D+LD.D                                       24
F507  1P080B  SQ(EM+CONSTANT)                                                           24
F508  1Q049B  OUT(F*)                                                                   28
F509  1P083B  DV+MU                                                                     28
F510  1P088B  E=NOT 77                                                                  20
F511  1M036B  NOT-SBU+BBCY.F=X1                                                         23
F512  1Q086A  NOT EXF                                                                   21
F513  1R020B  E=NOT 00                                                                  20
F514  1R005B  E=00                                                                      26
F515  1Q027B  E=00                                                                      26
F516  1S018B  NOT-EXC+EXCY                                                              27
F517  1Q024B  NOT INA                                                                   14
F518  1Q024A  NOT OTA                                                                   14
F519  1S040B  NOT INP                                                                   26
F520  1S044B  (OTN+ETAY+INAY+INA+OTA).A                                                 27
F521  1Q032A  NOT-(OTN+ETAY+INAY+INA+OTA).A+(EXC+EXF+EXCY).B+                           27
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		OUT(F*)•D+(INP+OUT)•C+INP(F*)•E•A*(-)	
		F* ACTIVE, NORMAL I/O WAIT CONTROL	
F522	1R041B	(OTN+ETAY+INAY+INA+OTA)•A+(EXC+EXF+EXCY)•B+	27
		OUT(F*)•D+(INP+OUT)•C+INP(F*)•E•A*(-)	
		F* ACTIVE, NORMAL I/O WAIT-TIME 15	
F523	1S044A	NOT-CH_2 OR CH_3 SELECTED AND BUSY	20
F525	1S033A	NOT-CH_2 SELECTED • CH 3 BUSY	20
F526	1R051B	CH 2 NOT BUSY	20
F527	1R045B	I/O UNIT NOT BUSY	20
F528	1Q062B	CH 2 BUSY	20
F529	1T041A	I/O UNIT BUSY	20
F530	1R050B	SRJ+DRJ+ACJ+IRJ	23
F531	1R050A	JR+UJ+DR+A JUMPS EM+RCJP	23
F532	1S035B	OUT(F*)	23
F533	1K017A	NOT-OUT(F*)	20
F534	1Q005B	NOT-INP(F*)	21
F535	1R052A	NOT-(INAY+ETAY)(F*)	26
F536	1S032B	(INAY+ETAY)(F*)	26
F537	1L009A	ERTA+JR	26
F538	1Q053A	NOT-LOAD+ENTER+BFR+(MU+DU)E+(SR+RA+AO)NOT RNI	25
F539	1Q049A	SR+RA+AO	25
F540	1Q046A	NOT-EXC+EXF+EXCY+LQ•NOT C+INA(F*)+LD•D+	25
		MX•NOT C*(INP+OUT)•NOT F*ACTIVE	
		X TO Q PRIME CONTROL	
F541	1Q056A	(LDN+8490 MODE INT•B+NOT F540)•NOT E•NOT	25
		(MX•(A+C)+(ST+SQ)•MX•D)	
F541		GATE X TO Q PRIME AT 10 TIME	
F542	1L025B	SBU+BRCY•E=X1	23
F543	1R063A	ADN+SBN+SCN+LPN	22
F544	1Q075A	RA+LP+SC+AD+SB	22
F545	1Q076A	NOT-INP(F*)•D+OUT(F*)•E•SR_2 SET	22
F546	1Q077A	NOT-(RA+LP+SC+AD+SB)•D+DV•E+OUT(F*)•D+	22
		MU•D	
		ENABLE A TO U CONTROL	
F547	1Q078B	INP(F*)•D+OUT(F*)•E•SR_2 SET+ADN+SBN+SCN+	22
		LPN+(INP+OUT)•C+NOT F546	
		SET ENABLE A TO U AT 10 TIME	
F548	1Q078A	LP+SR+AO	22
F549	1Q079A	MX(A+C)+(ST+SQ)MX•D	22
F550	1Q079B	NOT-ST+SQ	22
F551	1R052B	JPRG+OUT(F*)	21
F552	1R084A	NOT-SPECIFIC•A+JR•B+HW•D	23
F553	1P076B	SPECIFIC•A+JR•B+HW•D	23
F554	1P087A	(ST+SQ+SR+RA+AO+NOT D)•(EM+SPECIFIC)•NOT A	23
F555	1P086A	ACJ+IRJ+SI+SIC+SID	23
F556	1P075A	ACJ+DR+SID+SDC+SD+DRJ	23
F557	1M044B	NOT-BLS•A+(SR+RA+AO+JR)•NOTB	26
F558	1S089B	(DV+MU)E	24
F559	1P075B	XAQ+LQ+(DV+MU)•(D+E)	24
F560	1P074B	(DV+MU)•(D+E)+PTA+XAQ+(INP+OUT)•B	24
F561	1R055A	NOT-(DV+MU)•(D+E)+PTA+XAQ	24
F562	1P073B	(NOT F565+NOT F566)•NOT DV	24
		A TO A PRIME CONTROL	
F563	1P073A	SR+LS_1+LS_2+LS_6+MUT+MUH	25
F564	1R092B	NOT-MUT+MUH	25
F565	1Q045A	NOT-ATX+LS_2+RS_2+MU•D+ATEY+ATXY	24
F566	1Q044A	A TO A PRIME CONTROL	24
		NOT-ST•(F+B+S)+MX•D+(INP+OUT)•C	
F567	1M051B	NOT-BLS•A•BUFFER NOT BUSY	25
F568	1M051A	BLS•A•BUFFER NOT BUSY+B1	25
F569	1M049B	D+I+M+CONSTANT	24
F570	1M049A	HW+ACJ+DRJ+SRJ+HWI	24
F571	1S086A	NOT-ENTER+HW+ACJ+DRJ+SRJ+HWI+OTA•A+	24
		ST•(EM+D+I+M+C)	
		A TO A PRIME CONTROL	
F572	1Q040B	IRJ+RS_1+RS_2+LS_1+LS_2+MUT+MUH+NOT F571	24
		GATE A TO A PRIME AT 11 TIME	
F573	1Q040A	NOT HWI	20
F574	1Q039B	OTA	24
F575	1R039B	INP(F*)	23
F576	1Q039A	OTN+OTA	14
F577	1P072B	INTERRUPT+JPR+SPECIFIC•A+JR•B+HW•D	25
F578	1Q038B	NOT JPR	20
F579	1Q002A	INP	26
F580	10037B	INP(F*)•E•SR_2 SET+INA•NOT D	28
F581	10036A	NOT-INP(F*)•E•SR_2 SET	28
F582	1Q086B	LPN+ADN+SBN+SCN+LCN+ETA	24
F583	1Q089A	NOT-AD+SB+LC+SC+LP+RA+AO	24
F584	1N001A	(AD+SR+LC+SC+LP+RA+AO+INP(F*))•D	24
F585	1J010A	ERTA+(INAY+ETAY)(F*)•NOTC	25
F586	10037A	MUT+MUH	22
F587	10035B	(HW+HWI)D	27
F588	1Q034B	NOT-DV•E	21
F590	1I011A	(SQ•MX)•NOT A+SQ•F	24
F591	1Q034A	NOT-STE+SR•D	24
F592	1M008A	STE+SR•D+BLS•A•BUFFER NOT BUSY	24
F593	1H064B	DV	16
F594	1P086B	NOT-BLS•BUFFER NOT BUSY•D•BER=BXR	20
F595	1Q052A	LS_2+LS_3+LS_6	25
F596	1Q023B	JPR	24
F597	1J009A	STP+STE+OTA+ENTER+8090 MODE INT+NOT F598	26
		GATE A PRIME TO X AT 12 TIME	
F598	1P044A	NOT-(ST+SQ)•(I+M+EM)•D+(ST+SQ)•(CONST+DIR)•A+	26
		(HW+HWI)•D+JPR•D	
		A PRIME TO X CONTROL	
F599	10008A	(ST+SQ)•(I+M+EM)•D	26
F600	1P045A	NOT-MU•E+DV•D	22
F601	1P045B	NOT - MU•E+DV•D	25
F602	1P046B	EXF	25
F603	1R025B	EXC+EXCY	27
F604	10041B	INA	14
F605	1M042B	OTA	26
F606	1Q035B	INP	23
F607	1Q041B	OUT	26
F608	10033A	(ST+SQ)•(CONSTANT+DIRECT)•A	26
F610	1J010B	(SR+RA+AO+JR)•NOT B	27
F611	10038B	NOT-(ST+SQ)•MX•D	20
F612	1K009B	ATEY+ATXY+ATX+ST•(F+B+S)+MX•D+(INP+OUT)•C	26
		GATE A PRIME TO X AT 16 TIME	
F613	10034A	IBO	22
F614	1Q051A	NOT-MX•C+(FORWARD+BACKWARD+SPECIFIC)•A	25
F615	10035A	(ST+SQ)•MX•D	20
F616	1N033A	NOT-(ST+SQ)•MX•D+(JFI+EXF)•A	25
		A* TO S, REQ MEM READ, P TO U CONTROL	
F617	1Q055B	(ST+SQ)•MX•D+(JFI+EXF)•A+	25
		MX•C+(F+B+S)•A	
		A PRIME TO S AND REQ MEM CONTROL	
F618	1M041B	JFI	20
F619	10063A	NOT-INP(F*)•D+(SR+RA+AO+JR)•D	27
		BLS•BUFFER NOT BUSY•BER NOT = BXR	
		REQ MEM WRITE CONTROL	
F620	10003B	STE+INP BUFFER•B1+BLS•A•BFR NOT BUSY+INP(F*)•D+	27
		(SR+RA+AO+JR)•D+BLS•BFRNOT BUSY•BER NOT=BXR	
		REQ MEM WRITE CONTROL-TIME 14	

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F622  1P026A  MUT+MUH                                                          24
F623  1S027B  NOT - OUT                                                       26
F624  1Q043B  NOT - MU.X(-)+DV.X(+)                                           21
F625  1Q042B  MU.X(-).D+DV.X(+).D                                             21
F626  1L054B  MU                                                              16
F627  1Q043A  NOT - MU.X(+)+DV.X(-)                                           21
F628  1Q042A  MU.X(+).D+DV.X(-).D                                             21
F629  1R062A  NOP TRANSLATION                                                 18
F630  1Q055A  NOT-(Q.F2+Q2)                                                   18
F631  1Q010A  NOT - (SLS+SJS).STOP CONDITION MET                              12
F632  1S045A  NOT-ERROR STOP+HALT+ENTER.NOT EM                                12
F633  1Q061A  (SLS+SJS). STOP CONDITION MET+ERROR STOP+HALT+                   12
              INSTRUCTION STEP+ENTER. NOT EM
              PROGRAM STOP
F634  1P006A  NOT - (SLJ+SJS).JUMP CONDITION MET                              13
F635  1Q006A  (A JUMPS BACKWARD+BACKWARD+LCN+SBN).A                           21
F636  1N004A  (LC+SR).D                                                       21
F637  1P078A  NOT-G SHIFTS+JPR+ENTER+LOAD.P NOT=5                             24
F638  1Q054A  NOT - SCN+STE+SC.D+SR.D+BLS.A+(INP+OUT).B                       24
F639  1P071B  MUT+MUH+B1 CYCLE                                                24
F640  1P082B  MUT+MUH+B1 CYCLE+LS6+(MU+DV).E+DV.D                             24
F641  1Q037A  NOT-MUT+MUH+B1 CYCLE                                            24
F642  1P030B  NOT - LS6+(MU+DV).E+DV.D                                        24
F643  1Q037B  HWI                                                            20
F644  1Q036A  NOT - HWI.D+INP(F*).D+OUT.C+OUT(F*).E                           23
F645  1Q035A  NOT-(I+M).B+MX.C                                                23
F646  1Q061B  HWI.D+INP(F*).D+OUT.C+OUT(F*).E+(I+M).B+                        23
              MX.C
              SELECT INDIRECT BANK AT 11 TIME
F647  1N007A  ST+SQ+SR+RA+AQ+(M+I+MX).D                                       23
F648  1N006A  NOT-(D+I).A+DIRECT.(SR+RA+AQ).D                                 23
F649  1Q005A  NOT-(JPI+HWI).A                                                 23
F650  1Q062A  (D+I).A+DIRECT.(SR+RA+AQ).D+(JPI+HWI).A+                        23
              JPIB.B+STE+STP+A MODE INTERRUPT
              SEL DIR BANK,REQ MEM READ CONTROL
              B+STE+STP+8090 MODE INTERRUPT
F651  1P028B  NOT - (EXC+EXF+FXCY)(F*)                                        21
F653  1L007B  OUT(F*)                                                         27
F654  1M007A  NOT-CONSTANT+F+BACKWAPD+JPR+(INP+OUT).B+JR.D                    23
              SELECT RELATIVE BANK CONTROL
F655  1Q005B  CONSTANT+F+BACKWARD+JPR+(INP+OUT).B+JR.D                        23
              SELECT REL BANK-TIME 11
F657  1Q015B  ((I+M).B+(F+BACKWARD+S+CONSTANT+DIRECT).A+                      28
              MX.C+EM.B.NOT(SR+RA+AQ).NOT(MU+DV)
              ENABLE R CONTROL
F658  1P002A  (F+BACKWARD+S+CONSTANT+DIRECT).A.NOT(SR+RA+AQ)                  28
F659  1L007A  NOT-EM.B+(F+BACKWARD+S+CONSTANT+DIRECT).A                       28
              NOT(SR+RA+AQ)
              ENABLE R CONTROL
F660  1P058B  IBI                                                             48
F662  1Q009A  M+EM+JR.NOT MD13 INTERRUPT.                                     26
F663  1Q010A  STE+JPI+HWI+STP+INDIRECT+DIRECT                                 26
F664  1Q004B  HWI+NOTF666+(UJ+DR+A JUMPS EM+RCJP).D+                          26
              OUT.NOT F*ACTIVE.C
              X TO S CONTROL-TIME 11
F665  1J008A  NOT-NOT F666+(SR+DR+A JUMPS EM+JR+                              26
              RCJP).D+OUT.C.NOT F*ACTIVE
              X TO S CONTROL
F666  1J007A  (ATE+ATX+JPI+IB1Y+IBOY+IBI+IB0+ATEY+ATXY+HW                     26
              +MTM2+BLS.BFR BUSY+RCJP+F=77+JPR+JFI+
              HILO.E).(D+E)---X TO S+TIME 10 TO 1
F667  1P071A  NOT - JPI+ATX+IBIY+IBOY+IBI+ATEY+ATXY                           26

F668  1L013A  NOT-HW+MTM2+BLS.BUFFER BUSY+IB0                                 26
F669  1M006A  NOT-RCJP+JPR+JFI+F=77                                           26
F670  1Q059B  F NOT = 77                                                      17
F671  1Q060B  SLJ+SLS+SJS                                                     20
F673  1Q070B  F=77                                                            20
F674  1Q058A  (SLJ+SJS).JUMP CONDITION MET                                    13
F677  1Q058B  MX.C+(FORWARD+BACKWARD+SPECIFIC).A                              27
F678  1Q057B  NOT-(ST+SQ).MX.D+(ST+SQ).(F+B+S).A                              27
              A PRIME TO X AND MEM WRITE CONTROL
F679  1Q046B  SET MEM WRITE AT 12 TIME                                        27
F681  1K006A  I+M+EM+INP+OUT                                                  27
F682  1L006A  NOT-(D+I).A+(JPI+HWI).A+(I+M+EM+                                27
              INP+OUT).B+OUT(F*).E.SR2 SET+STE+STP+
              MD12 INTERRUPT---REQ MEM. READ CONTROL
F683  1I010A  SET MEM READ AT 12 TIME                                         27
F684  1Q057A  MX.C+(F+B+S).A+(JFI+EXF).A+DIRECT.NOT D                         27
              SET MEM READ AT 12 TIME
F685  1F012A  ENTER+LOAD+MD12 INTERRUPT+STP                                   27
F686  1R054A  NOT-ENTER+JPR.D+(ST+SQ).(CONSANT+DIRECT).A+LOAD+                27
              STP+MD12 INT+(ST+SQ).(I+M+EM).D
              REQ MEM AND MEM WRITE CONTROL
F687  1Q060A  OUTPUT BUFFER.B1.NOT I/O NOT BUSY CYCLE                         28
F688  1J006A  SET REQ MEM AT 12 TIME                                          27
F691  1J006B  NOT - (INA+OTA+OTN)(F*)                                         22
F692  1I009A  ((INA+OTA+OTN+INAY+ETAY+EXC+EXF+EXCY)(F*)+BLS).D                22
              SET ENABLE P TO U AT 10 TIME
F693  1I008A  SET ENABLE P TO U AT 10 TIME                                    22
F694  1Q017A  (INP+OUT+(INP+OUT)(F*)).NOT(B+C+D)                              22
              ENABLE P TO U CONTROL
F695  1I006A  (A JUMPS(F+B)+JR+EXF+FORWARD+BACKWARD).A.NOT B                  22
              SET ENABLE P TO U AT 10 TIME
F696  1H011A  NOT-ATE+MTM2+INTERRUPT+IB0+STP+PTA                              22
F697  1H010A  NOT-BLS+DV.E.SR2 CLEAR+SR.D+MU.E.SR1 CLEAR+                     21
              (MU+DV).D.A(+)
              ENABLE I CONTROL
F698  1H009A  SET ENABLE I AT 10 TIME                                         21
F699  1Q072A  NOT-B1+ATX+IBIY+IBOY+ATEY+ATXY+A JUMPS EM+                      21
              IBI+STE
              ENABLE I(+2) CONTROL-TIME 10
F700  1F009A  MU.E+DV.D                                                       22
F701  1L009B  MU.E+DV.D+XAQ                                                   25
F702  1F008A  NOT - A JUMPS EM                                                16
F703  1M058B  NOT - A JUMPS BACKWARD                                          16
F704  1M064B  NOT - A JUMPS FORWARD                                           16
F705  1F008B  NOT - LP                                                        16
F706  1F006B  NOT - SC                                                        16
F708  1F006A  NOT - LC                                                        16
F709  1P076A  NOT - AD                                                        16
F710  1M056B  NOT - SB                                                        16
F711  1H006B  NOT - ST                                                        16
F712  1H006A  NOT - SR                                                        16
F713  1G006B  NOT - RA                                                        16
F714  1G006A  NOT - AO                                                        16
F715  1I005B  NOT - LQ                                                        16
F716  1I005A  NOT - SQ                                                        16
F717  1H005B  NOT DIR                                                         16
F718  1H005A  NOT - M                                                         16
F719  1G005B  NOT - I                                                         16
F720  1G005A  NOT SPECIFIC                                                    16
F721  1F005B  NOT BACKWARD                                                    16
F722  1F005A  NOT FORWARD                                                     16
F724  1Q002B  NOT - MX                                                        16
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F725  1L055B
F726  1R082A  NOP
F727  1R085A  NOP
F728  1J031A  NOT-OUT.C
F800  1Q066A  ADN
F801  1Q065A  SBN
F802  1Q064A  UJ
F803  1R087A  DR
F804  1R086A  SD
F805  1Q088A  SI
F806  1Q087A  HW
F807  1R083A  JPR+JFI (71XX)
F808  1R078A  IBI+INP (72XX)
F809  1R077A  IBO+OUT (73XX)
F810  1R076A  NOP
F811  1Q074A  OTN
F812  1Q073A  EXC+EXF (75XX)
F814  1S087A  F.12=0
F815  1R085B  F.12=1
F816  1S082B  F.12=0
F817  1R082B  F.12=1
F818  1S081B  F.12=0
F819  1R081B  F.12=1
F820  1S085B  F.12=0
F821  1R080B  F.12=1
F822  1S086B  F.12=0
F823  1R079B  F.12=1
F826  1Q072A  INA+HWI+OTA (76XX)
F831  1R051A  E=X1
F832  1Q021B  E=X2
F833  1P027A  E=X3
F839  1Q084A  MD12
F840  1S016A  F.12=1+M+MX+C
F841  1R093A  MD13
F900  1H007A  NOT-((EXC+EXF+EXCY+INAY+ETAY+INA+OTA+OTN)(F*)+
              AO+BLS).D+SLJ+SJS+INTERRUPT.
              ENABLE I CONTROL
F901  1G013A  (EXF+INAY+ETAY+INA+OTA+OTN)(F*)+AO
              ENABLE I(+1) CONTROL-TIME 10
F902  1N059B  (EXC+EXCY)(F*)+BLS
F903  1R046A  NOT-INP(F*).E+JR.A+OUT(F*).E.SR2 CLEAR
              ENABLE I(+2) CONTROL-TIME 10
F904  1F012B  DV.E
F905  1G010B  INP(F*).D+OUT(F*).E.SR2 SET+
              ((EXF+INAY+ETAY+INA+OTA+OTN)(F*)+AO).D
              PLUS 1 TO I CONTROL-TIME 10
F906  1G009A  PLUS 2 TO I CONTROL-TIME 10
F907  1G010A  NOT-((EXF+INAY+ETAY+INA+OTA+OTN)(F*)+AO).D
              PLUS 1 TO I INVERTERS CONTROL
F908  1G008A  SLJ+SJS+(EXC+EXCY)(F*).D+BLS.D+
              PLUS 2 TO I INVERTERS CONTROL
F909  10065A  ATE+ATX+IBI+IBO+BLS
F910  10066A  NOT-EXC+EXCY+OUT(F*)+(ATE+ATX+IBI+IBO+
              BLS).BFR BUSY+MTM2.I/O UNIT BUSY
              SEL REL BANK,REQ MEM READ CONTROL
F911  1P025A  NOT-JPR+UJ+DR+CONSTANT.NOT(ST+SQ)+
              (ATEY+ATXY).CH 2 BUSY
              SEL REL BANK,REQ MEM READ CONTROL
F912  1F011A  NOT-HW+(SLJ+SJS).JUMP CONDITION MET+BBCY
              SEL REL BANK,REQ MEM READ CONTROL
F914  10002A  NOT-A JUMPS EM.JUMP CONDITION MET+INP+OUT
              SEL REL BANK,REQ MEM READ CONTROL
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16    F915  10003A  NOT-M+EM+MX+JR+RCJP                                  27
16                  (IRIY+IBOY).CH 2 BUSY
18                  SEL REL BANK,REQ MEM READ CONTROL
27    F916  10001A  SEL REL BANK,REQ MEM READ-TIME 10                    27
17    F918  1N002A  (SC+RA+AD)                                           21
17    F919  1N003A  NOT-SCN+ADN+F.A                                      21
17    F920  1M008B  SCN+ADN+F.A+A JUMPS F+(INP+OUT).C                    21
17                  SET ENABLE X TO I AT 10 TIME
17    F921  1M003A  (OUT+INP+EXF+JFI).(A+B)                              21
17    F922  1N005B  NOT - JFI                                            21
17    F924  1P058A  NOT-(ST+SQ).(I+M+EM).D CYCLE+EM.B                    20
17    F925  1P080A  (BLS.BFR NOT BUSY.(A+BER NOT=BXR)+JR.NOT A+          20
17                  (SR+RA+AO).D+INP(F*).D+STE).NOT C CYCLE
17                  TIME 15 TO 4,CLEAR ENABLES CONTROL
17    F926  1L003A  NOT-JR.NOT A+BLS.BFR NOT BUSY.BER NOT=BXR+          20
17                  (SR+RA+AO).D+INP(F*).D
17    F926          TIME 15 TO 4,CLEAR ENABLES CONTROL
18    F927  1P081A  TIME 13 TO 4,CLEAR ENABLES CONTROL                   20
18    F928  1N005A  NOT-(BBCY+CONSTANT+DIRECT+ENTER).A+MD12 INT+         20
18                  (HW+HWI).D
18                  TIME 13 TO 4,CLEAR ENABLES CONTROL
17    F929  1N004B  (BBCY+CONSTANT+DIRECT+ENTER).A                       20
18    F930  1P082A  (INP+OUT).C+(ST+SQ)(MX.D)                            20
17                  TIME 17 TO TIME 4 CONTROL
17    F932  1Q014B  (M+MX+CONSTANT+F BIT 12=1).NOT(F+JR+                 21
17                  RNI+(INP+OUT).C)
17                  PLUS 2 TO I CONTROL-TIME 4
17    F933  1Q020A  F+RNI+JR.B+(INP+OUT).C+                              21
19                  NOT(M+MX+CONSTANT+F BIT 12=1)
19                  PLUS 1 TO I CONTROL-TIME 4
19    F934  1Q022B  NOT-JR.C CYCLE                                       21
18    F935  1P032B  ZJ                                                   17
21    F936  1R040A  NZ                                                   17
18    F937  1R039A  PJ                                                   17
21    F938  1R038A  NJ                                                   17
      F939  1F054B  SELECT MD12.MD13                                     10
      F941  1P093A  NOT-A JUMPS EM.JUMP CONDITION NOT MET                20
21    F942  1Q021A  INP(F*)                                              20
      F943  1Q053B  JR.B+BLS+INP(F*).D                                   17
21    F944  1Q022A  NOT-JR.B+BLS+INP(F*).D                               17
21    F945  1P029A  ZJF+ZJB                                              17
      F946  1Q018A  NZF+NZB                                              17
21    F947  1R053A  PJF+PJB                                              17
21    F948  1Q016A  NJF+NJB                                              17
      F949  1Q015A  NOT-A JUMPS(F+B).JUMP CONDITION MET                  20
      F950  1Q023A  NOT-A JUMPS(F+B).JUMP CONDITION NOT MET              17
21    F951  1Q028B  NOT-JR+EXC+EXF+EXCY+(EM+M+I).                        11
21                  NOT(ST+SQ)+MX+INP+OUT+OUT(F*)
                    CYCLE SELECT CONTROL - A TO D
21    F952  1Q019A  JR+EXC+EXF+EXCY+(EM+M+I).NOT(ST+S+                   11
                    MX+INP+OUT+OUT(F*)
27                  CYCLE SELECT CONTROL - A TO B
27    F953  1P008A  NOT JR+EXC+EXF+EXCY+(EM+M+I).                        11
                    NOT(ST+SQ)+(ST+SQ).MX
                    CYCLE SELECT CONTROL - B TO C
27    F954  1Q012A  NOT-INP+OUT+OUT(F*)+MX.NOT(ST+SQ)                    11
                    CYCLE SELECT CONTROL - B TO D
      F955  1Q094A  NOT SI+ERTA+SID+SIC+SPC+SBU+SD                       20
27    F956  1Q093A  NOT-ADN+SBN+LDN+LCN+SCN+LPN+MD13 SHIFTS.E=0          20
      F957  1Q092A  NOT-SLS+HLT+ERR+NOP+ENTER+CBCY+CBC+PTA+              20
27                  CTA+CTAQ+ETA+XAQ+F=77.D
                    TIME 10 TO TIME 1 AND SELECT REL.BANK CONTROL
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F958	10091A	NOT-CTC1•BBCY.D•C1L•C1LY•MD12PMD13•JFI.D	20	G024	1A038A	X GATE - 2	44
F959	1S046A	NOT-MUT•RS1•RS2•LS6•LS3•LS1•LS2	20	G025	1A038B	X GATE - DISCHARGER - 2	44
F960	1P091A	TIME 10 TO 1•SEL REL BANK CONTROL	20	G026	1D038A	Y GATE - 2	45
		TIME 10 TO TIME 1 AND SELECT REL•BANK CONTROL		G027	1D038B	Y GATE - DISCHARGER - 2	45
F961	10032A	TIME 10 TO TIME 1 CONTROL	20	G030	1R051A	STRIPE 0 INHIBIT - BIT 3	42
F963	1P090B	TIME 10 TO TIME 1 CONTROL	20	G031	1R051B	STRIPE 1 INHIBIT - BIT 3	42
F964	1P090A	NOT-F*ACTIVE•B1•B2•ENTER•LOAD•STP•	20	G032	1R052A	STRIPE 2 INHIBIT - BIT 3	42
		MD12 INTERRUPT		G033	1R052B	STRIPE 3 INHIBIT - BIT 3	42
F965	1P007B	(INAY•ETAY•INA•OTA•OTN•EXC•EXF•EXCY)(F*)	20	G034	1A037A	X GATE (3)	44
		TIME 13 TO TIME 0 CONTROL		G035	1A037B	X GATE - DISCHARGER (3)	44
F966	10018B	(INP•OUT)(F*).SIGN RECORD 2 CLEARED	20	G036	1D037A	Y GATE (3)	45
F967	1J003A	(A JUMPS EM.JUMP CONDITION NOT MET•	20	G037	1D037B	Y GATE - DISCHARGER (3)	45
		A JUMPS(F*B).JUMP CONDITION MET		G040	1R067A	STRIPE 0 INHIBIT - BIT 4	42
		TIME 13 TO TIME 0 CONTROL		G041	1R067B	STRIPE 1 INHIBIT - BIT 4	42
F968	1S069A	TIME 13 TO TIME 0 CONTROL	20	G042	1R068A	STRIPE 2 INHIBIT - BIT 4	42
F969	1R011A	NOT-MTM2•UNIT NOT BUSY•	20	G043	1R068B	STRIPE 3 INHIBIT - BIT 4	42
		(ATE•ATX•IBI•IBO).BUFFER NOT BUSY		G044	1R040A	X GATE (4)	44
		TIME 13 TO TIME 0 CONTROL		G045	1R040B	X GATE - DISCHARGER (4)	44
F970	1P085B	TIME 13 TO TIME 0 CONTROL	20	G046	1D036A	Y GATE (4)	45
F972	1K003B	NOT - ST•SQ	11	G047	1D036B	Y GATE - DISCHARGER (4)	45
F973	1L008A	ST•SQ	11	G050	1R053A	STRIPE 0 INHIBIT - BIT 5	42
F974	1P007A	EM•M•I	11	G051	1R053B	STRIPE 1 INHIBIT - BIT 5	42
F975	1P085A	MX	11	G052	1R054A	STRIPE 2 INHIBIT - BIT 5	42
F977	1P083A	GATE CLEAR SELECT ENABLES AT 16 TIME	22	G053	1R054B	STRIPE 3 INHIBIT - BIT 5	42
F978	10016B	NOT - SR•RA•A0	23	G054	1R039A	X GATE (5)	44
F979	1P001A	CONSTANT•BACKWARDS•JPR•FORWARD	23	G055	1R039B	X GATE DISCHARGER (5)	44
F980	10007B	MX	16	G056	1D035A	Y GATE (5)	45
F981	1K028A	NOT - SLS	20	G057	1D035B	Y GATE - DISCHARGER (5)	45
F983	1M043B	SLS•HLT•ERR•NOP•ENTER	20	G060	1R069A	STRIPE 0 INHIBIT - BIT 6	42
F984	1P072A	SILY	19	G061	1R069B	STRIPE 1 INHIBIT - BIT 6	42
F987	1T088A	NOT-SID•SDC•SD	23	G062	1R070A	STRIPE 2 INHIBIT - BIT 6	42
F988	1T088B	NOT-SI•SIC•SID	23	G063	1R070B	STRIPE 3 INHIBIT - BIT 6	42
F989	10059A	NOT - IBO	27	G064	1R038A	X GATE (6)	44
F991	10065B	NOT-(SLJ•SJS).A.JUMP CONDITION NOT MET	20	G065	1R038B	X GATE - DISCHARGER (6)	44
F992	1R014A	LOAD•SWEEP•ENTER•MUH•JFI	23	G066	1D034A	Y GATE - (6)	45
F993	1P079B	NOT IBI	27	G067	1D034B	Y GATE DISCHARGER (6)	45
F994	1R089B	NOT-(ATEY•ATXY•IBIY•IBOY).CH 2 NOT BUSY	20	G070	1R055A	STRIPE 0 INHIBIT - BIT 7	42
F995	1P094B	F*ACTIVE•B1•B2•ENTER•LOAD•	20	G071	1R055B	STRIPE 1 INHIBIT - BIT 7	42
		MD12 INTERRUPT•STP		G072	1R056A	STRIPE 2 INHIBIT - BIT 7	42
F996	1P004A	CLEAR SELECT RELATIVE BANK-TIME 11	23	G073	1R056B	STRIPE 3 INHIBIT - BIT 7	42
F997	10005A	A JUMPS FORWARD•A JUMPS BACKWARD	20	G074	1R037A	X GATE (7)	44
F998	1R080A	MD13 SHIFTS AND E NOT=00	32	G075	1R037B	X GATE - DISCHARGER (7)	44
G000	1R063A	STRIPE 0 INHIBIT - BIT 0	42	G076	1D033A	Y GATE (7)	45
G001	1R063B	STRIPE 1 INHIBIT - BIT 0	42	G077	1D033B	Y GATE DISCHARGER (7)	45
G002	1R064A	STRIPE 2 INHIBIT - BIT 0	42	G080	1R071A	STRIPE 0 INHIBIT - BIT 8	42
G003	1R064B	STRIPE 3 INHIBIT - BIT 0	42	G081	1R071B	STRIPE 1 INHIBIT - BIT 8	42
G004	1A040A	X GATE - 0	44	G082	1R072A	STRIPE 2 INHIBIT - BIT 8	42
G005	1A040B	X GATE - DISCHARGER- 0	44	G083	1R072B	STRIPE 3 INHIBIT - BIT 8	42
G006	1D040A	Y GATE - 0	45	G090	1R057A	STRIPE 0 INHIBIT - BIT 9	42
G007	1D040B	Y GATE - DISCHARGER - 0	45	G091	1R057B	STRIPE 1 INHIBIT - BIT 9	42
G010	1R049A	STRIPE 0 INHIBIT - BIT 1	42	G092	1R058A	STRIPE 2 INHIBIT - BIT 9	42
G011	1R049B	STRIPE 1 INHIBIT - BIT 1	42	G093	1R058B	STRIPE 3 INHIBIT - BIT 9	42
G012	1R050A	STRIPE 1 INHIBIT - BIT 1	42	G100	1R073A	STRIPE 0 INHIBIT - BIT 10	42
G013	1R050B	STRIPE 1 INHIBIT - BIT 1	42	G101	1R073B	STRIPE 1 INHIBIT BIT 10	42
G014	1A039A	X GATE - 1	44	G102	1R074A	STRIPE 2 INHIBIT BIT 10	42
G015	1A039B	X GATE - DISCHARGER - 1	44	G103	1R074B	STRIPE 3 INHIBIT BIT 10	42
G016	1D039A	Y GATE - 1	45	G110	1R059A	STRIPE 0 INHIBIT - BIT 11	42
G017	1D039B	Y GATE - DISCHARGER - 1	45	G111	1R059B	STRIPE 1 INHIBIT - BIT 11	42
G020	1R065A	STRIPE 0 INHIBIT - BIT 2	42	G112	1R060A	STRIPE 2 INHIBIT - BIT 11	42
G021	1R065B	STRIPE 1 INHIBIT - BIT 2	42	G113	1R060B	STRIPE 3 INHIBIT - BIT 11	42
G022	1R066A	STRIPE 2 INHIBIT BIT 2	42	G120	1R075A	STRIPE 0 INHIBIT - BIT 12	42
G023	1R066B	STRIPE 3 INHIBIT BIT 2	42	G121	1R075B	STRIPE 1 INHIBIT - BIT 12	42

G122	1B076A	STRIPE 2 INHIBIT - BIT 12
G123	1B076B	STRIPE 3 INHIBIT - BIT 12
G130	1B061A	STRIPE 0 INHIBIT - BIT 13
G130	1B061A	STRIPE 0 INHIBIT - BIT 13
G131	1B061B	STRIPE 1 INHIBIT - BIT 13
G132	1B062A	STRIPE 2 INHIBIT - BIT 13
G133	1B062B	STRIPE 3 INHIBIT - BIT 13
H000	10094A	MAIN TIMING - TIME ZERO
H001	10090A	MAIN TIMING - TIME ONE
H002	10088A	MAIN TIMING - TIME TWO
H004	10081A	MAIN TIMING - TIME FOUR
H005	10073A	MAIN TIMING - TIME FIVE
H006	10058A	MAIN TIMING - TIME SIX
H007	10056A	MAIN TIMING - TIME SEVEN
H008	10054A	MAIN TIMING - TIME EIGHT
H009	1P019A	MAIN TIMING - TIME NINE
H010	10017A	MAIN TIMING - TIME TEN
H011	1N016A	MAIN TIMING - TIME ELEVEN
H012	1M014A	MAIN TIMING - TIME TWELVE
H013	1J017A	MAIN TIMING - TIME THIRTEEN
H014	1H016A	MAIN TIMING - TIME FOURTEEN
H015	1G020A	MAIN TIMING - TIME FIFTEEN
H016	1G017A	MAIN TIMING - TIME SIXTEEN
H017	1F021A	MAIN TIMING - TIME SEVENTEEN
H018	1F019A	MAIN TIMING - TIME EIGHTEEN
H019	1F016A	MAIN TIMING - TIME NINETEEN
H030	1L021A	START LOGIC
H032	10018A	START LOGIC
H050	1E073A	MULTIPLY+DIVIDE+SHIFT
H051	1E076A	MULTIPLY+DIVIDE+SHIFT
H052	1E078A	MULTIPLY+DIVIDE+SHIFT
H053	1E080A	MULTIPLY+DIVIDE+SHIFT
H054	1E081A	MULTIPLY+DIVIDE+SHIFT
H055	1E083A	MULTIPLY+DIVIDE+SHIFT
H070	1D021A	INTERRUPT LOGIC
H071	1D020A	INTERRUPT LOGIC
H072	1D019A	INTERRUPT LOGIC
H073	1D017A	INTERRUPT LOGIC
H074	1D016A	INTERRUPT LOGIC
H075	1D014A	INTERRUPT LOGIC
H080	1L018A	START LOGIC RESYNC
H081	1L019A	START LOGIC RESYNC
H082	1L018B	START LOGIC RESYNC
H084	1L018C	START LOGIC RESYNC
H086	1L018D	START LOGIC RESYNC
H088	1L018E	START LOGIC RESYNC
H090	1D094A	BUFFER RESYNC
H091	1C094A	BUFFER RESYNC
H092	1D094B	BUFFER RESYNC
H094	1D094C	BUFFER RESYNC
H096	1D094D	BUFFER RESYNC
H098	1D094E	BUFFER RESYNC
H120	1P064A	RESUME I
H121	1P065A	RESUME I
H122	1P064B	RESUME I
H124	1P064C	RESUME I
H126	1P064D	RESUME I
H128	1P064E	RESUME 1
H130	1C090A	NORMAL RESYNC
H131	1C091A	NORMAL RESYNC
H132	1C090B	NORMAL RESYNC
H134	1C090C	NORMAL RESYNC

42	H136	1C090D	NORMAL RESYNC 47
42	H138	1C090E	NORMAL RESYNC 47
42	H140	1P067A	RESUME TWO 49
42	H141	1P068A	RESUME TWO 49
42	H142	1P067B	RESUME TWO 49
42	H144	1P067C	RESUME TWO 49
42	H146	1P067D	RESUME TWO 49
3	H148	1P067E	RESUME TWO 49
3	H200	10093A	TIME ZERO 3
3	H201	10089A	TIME ONE 3
3	H204	10080A	TIME FOUR 3
3	H208	10053A	TIME EIGHT 4
3	H250	1E074A	MULTIPLY+DIVIDE+SHIFT 6
3	H702	1N009A	A TO A PRIME 24
4	H703	1L012A	A PRIME TO A 24
4	H706	1F079A	PROBE A PRIME 24
4	H723	10085A	A PRIME TO S 25
4	H900	1N011A	Q PRIME TO A 24
4	H901	1H012A	CLEAR A REGISTER 24
4	H902	1E084A	A TO A PRIME 24
5	H903	1P054A	A PRIME TO A 24
5	H904	1N008A	Q TO A PRIME 24
5	H905	1F073A	A LEFT SHIFT 25
5	H906	10055A	PROBE A PRIME 24
5	H907	1H028A	A RIGHT SHIFT 25
5	H908	1N081A	TOGGLE A PRIME 24
12	H909	10077A	CLEAR A PRIME 24
12	H910	1N010A	A TO Q PRIME 25
6	H911	1F074A	Q LEFT SHIFT 25
6	H912	1F078A	Q TO Q PRIME 25
6	H913	1L011A	Q PRIME TO Q 24
6	H914	1N074A	Z INT. TO X 26
6	H915	1R071A	Q RIGHT SHIFT 25
6	H916	10070A	Z EXT. TO X 26
53	H917	10013A	X TO Q PRIME 25
53	H918	1E009A	INTERRUPT 53
53	H919	1L010A	A PRIME TO X 26
53	H920	1F077A	REDUCE F LOWER 14
53	H921	10076A	CLEAR X 26
53	H922	1I018A	FE TO INDIRECT BANK 23
12	H923	1P053A	A PRIME TO S 25
12	H924	1I017A	FE TO DIRECT BANK 23
12	H925	10012A	X TO S 26
12	H926	1I014A	FE TO BUFFER BANK 23
12	H927	10084A	P TO S 25
12	H928	1I015A	BANK TO Q AND Q PRIME 24
48	H929	1E086A	F TO F PRIME 14
48	H930	10064A	BANK TO A 25
48	H931	1G014A	SET FE 15
48	H932	10061A	Z INT TO F 15
48	H933	1P089A	SET INTERRUPT LOCKOUT 53
48	H934	10060A	Z EXT TO F 15
49	H935	10011A	A.Q PRIME TO BANK 23
49	H936	1G038A	A PRIME TO BER 28
49	H937	10075A	CLEAR F 15
49	H938	1G028A	X TO BXR 51
49	H939	1P050A	CLEAR BFR 50
49	H940	1S005A	REDUCE F UPPER 14
47	H941	1G015A	CLEAR BXR 5
47	H942	1I013A	INPUT OUTPUT TO X 26
47	H943	1P052A	CLEAR BER 28
47	H944	1P016A	NORMAL INPUT TO X 26

H945	10082A	S TO P	25
H946	1I012A	X TO BUFFER BANK	23
H947	1K010A	SET X LOWER	26
H948	1J012A	RELATIVE BANK TO X	26
H949	1M010A	SET X UPPER	26
H950	1P015A	FE TO RELATIVE BANK	23
H953	1P051A	CLEAR RELATIVE BANK	23
H954	1A078A	BUFFER RESYNC	48
H955	1K011A	CLEAR INDIRECT BANK	23
H956	1P014A	EXT. INPUT TO BFR	50
H957	1K012A	CLEAR DIRECT BANK	23
H958	1A082A	BER=BXR	48
H959	1K014A	CLEAR BUFFER BANK	23
H960	1J011A	ERROR REG. TO X	26
H962	1P013A	Z EXT. TO BFR	50
H964	10059A	CLEAR INTERRUPT LOCKOUT	53
H965	10083A	CLEAR SELECT ENABLES	22
H966	1P012A	Z INT. TO BFR	50
I001	1H059A	I INVERTERS	38
I011	1I059A	I INVERTERS	38
I021	1J059A	I INVERTERS	38
I031	1K059A	I INVERTERS	38
I041	1L059A	I INVERTERS	38
I051	1M059A	I INVERTERS	38
I061	1M058A	I INVERTERS	38
I071	1L058A	I INVERTERS	38
I081	1K058A	I INVERTERS	38
I091	1J058A	I INVERTERS	38
I101	1I058A	I INVERTERS	38
I111	1H058A	I INVERTERS	38
I121	1G058A	I INVERTERS	38
I800	1D067A	MEM. INFO TO Z - BIT ZERO	42
I801	1D067B	MEM. INFO TO Z - BIT ONE	42
I802	1D066A	MEM. INFO TO Z - BIT TWO	42
I803	1D066B	MEM. INFO TO Z - BIT THREE	42
I804	1D065A	MEM. INFO TO Z - BIT FOUR	42
I805	1D065B	MEM. INFO TO Z - BIT FIVE	42
I806	1D064A	MEM. INFO TO Z - BIT SIX	42
I807	1D064B	MEM. INFO TO Z - BIT SEVEN	42
I808	1E066A	MEM. INFO TO Z - BIT EIGHT	42
I809	1E066B	MEM. INFO TO Z - BIT NINE	42
I810	1E065A	MEM. INFO TO Z - BIT TEN	42
I811	1E065B	MEM. INFO TO Z - BIT ELEVEN	42
I812	1E064A	MEM. INFO TO Z - BIT TWELVE	42
I813	1E064B	MEM. INFO TO Z - BIT THIRTEEN	42
J001	1M062B	ENABLE P TO U INVERTER	38
J003	1L062B	ENABLE A TO U INVERTER	38
J005	1K063B	ENABLE X TO U INVERTER	38
J007	1K062B	ENABLE BER TO U INVERTER	38
J009	1J063B	ENABLE Q TO U INVERTER	38
J011	1J062B	ENABLE I INVERTER	38
J012	1L044B	ENABLE I INVERTER	38
J013	1I063B	ENABLE A.2 TO 2ND TO I INVERTER	38
J015	1I062B	ENABLE X TO I INVERTER	38
J017	1G062B	ENABLE -X TO I INVERTER	38
J019	1H058B	ENABLE Q PRIME TO I	38
J020	10050A	MD13 INVERTER	10
J021	10050B	MD12 INVERTER	10
J032	1H024A	NOT NORMAL I/O WAIT	48
J056	1N034A	START LOGIC	12
J058	1N034B	START LOGIC	12
J059	1F092A	START LOGIC	12
J061	1P061B	RNI	3
J062	1P061A	NOT RNI	3
J063	1F093B	X TO X INVERTERS	37
J064	1G035B	X TO X INVERTERS	37
J065	1F090A	BFR TO X INVERTER	37
J067	1L059B	LOAD INVERTER	37
J068	1J025A	X TO TRANSMITTERS	49
J069	1J025B	X TO TRANSMITTERS	49
J071	1M019B	F*ACTIVE	48
J072	1Q012B	NORMAL LOGIC	12
J077	1F092B	LOAD INVERTER	37
J081	1K058B	F*ACTIVE	48
J082	1R037B	NOT-REQUEST MEMORY	49
J083	1S037B	REQUEST MEMORY	49
J096	1K032B	NOT-SWEEP+ENTER	54
J100	1F094A	RUN DISABLE INVERTER	10
J101	1F094B	RUN DISABLE INVERTER	10
J102	1F093A	RUN DISABLE INVERTER	10
J103	1F093B	RUN DISABLE INVERTER	10
J104	1G036A	RUN DISABLE INVERTER	10
J105	1G036B	RUN DISABLE INVERTER	10
J106	1S043B	RUN DISABLE INVERTER	10
J107	1S077B	RUN DISABLE INVERTER	10
J108	1N092A	RUN DISABLE INVERTER	12
J109	1P028A	RUN DISABLE INVERTER	53
J110	1E007B	MASTER CLEAR	10
J111	1E012A	CLEAR P	10
J112	1J003B	MASTER CLEAR	53
J113	1E012B	CLEAR Q	10
J114	1M031B	RUN DISABLE INVERTER	12
J115	1D009B	SELECT RELATIVE BANK	9
J116	1E015A	SELECT RELATIVE BANK	9
J117	1E013A	RUN DISABLE	9
J118	1E013B	RUN DISABLE	9
J119	1N046B	RUN DISABLE	9
J120	1N044A	SET BANK CONTROL	9
J121	1N044B	SET BANK CONTROL	9
J122	1N045A	SET BANK CONTROL	9
J123	1N045B	SET BANK CONTROL	9
J127	1C078A	BUFFER 2 CYCLE	48
J128	1R080A	BUFFER NOT BUSY	47
J130	1B080B	BUFFER NOT BUSY	47
J132	1D087B	BUFFER NOT BUSY	48
J133	1A077A	BUFFER BUSY	48
J134	1R078B	CLEAR BUFFER CONTROLS	48
J135	1A077B	CLEAR BUFFER CONTROLS	48
J136	1R078A	BUFFER DISC. - INP. RDY - OUTPUT RESUME.	48
J137	1R079A	NOT-BUFFER DISC,INPUT RDY,OUTPUT RESUME	48
J138	1C087A	NORMAL DISC.-INP RDY-OUTPUT RESUME-I/O RESUME	47
J139	1C088A	NOT OF J138, NOT BUFFER GATE, NOT BUFFER CYCLE	47
J140	1C089B	NOT-INPDISC.INPRDY.OUT RESUME	47
J141	1B079B	NORMAL I/O WAIT+STOP	48
J142	1B077A	CLEAR BUFFER CONTROLS	48
J143	1C089A	INPDISC+INPRDY+OUT RESUME	47
J144	1C083B	NOT-NORMAL CHANNEL OUTPUT RESUME	47
J147	1H007B	INPUT BUFFER	48
J148	1D086B	ENABLE BER TO A CHY,ENABLE INP TO A CHY, EXT.FUNCT.RDY CHY	47
J149	1D086A	NOT-ENABLE BER TO A CHY,ENABLE INP TO A CHY, EXT.FUNCT.RDY CHY	47
J150	1N036B	START LOGIC	12
J151	1P042B	START LOGIC	12

J152	1L025A	START LOGIC	12
J155	1H037B	NOT XXXXXXXXXXXX0 IN P REGISTER.	37
J160	1C085B	8090+8490 MODE - BORROW PYRAMID	32
J161	1G058B	8090+8490 MODE - BORROW PYRAMID	32
J162	1R003A	SET F PRIME	14
J163	1R014B	SET F PRIME	14
J164	1S029A	SET F PRIME	14
J170	1Q050A	SHIFT A AND Q	25
J171	1K064B	SHIFT A AND Q	25
J173	1N058B	SHIFT A AND Q	25
J174	1B093B	A=ZEROS	31
J186	1G039A	A NOT = ZEROS	31
J206	1N041A	A NOT = TO ZERO	31
J213	1G083A	SET SIGN RECORD	28
J214	1F083A	A=+	31
J215	1E087B	A=-	31
J216	1E087A	A=ZEROS	31
J217	1F083B	SIGN RECORD LOGIC	28
J220	1D083A	BER=BXR TRANSLATOR	51
J221	1D082A	BER=BXR TRANSLATOR	51
J222	1D081A	BER=BXR TRANSLATOR	51
J223	1D080A	BER=BXR TRANSLATOR	51
J224	1F089A	BER=BXR TRANSLATOR	51
J225	1F081A	BER=BXR TRANSLATOR	51
J226	1D084A	BER NOT = TO BXR	51
J227	1D081B	BER = TO BXR	51
J230	1I024A	BREAKPOINT LOGIC	13
J231	1K024A	BREAKPOINT LOGIC	13
J232	1L024A	BREAKPOINT LOGIC	13
J233	1K023A	BREAKPOINT LOGIC	13
J234	1I023A	BREAKPOINT LOGIC	13
J235	1J024A	BREAKPOINT LOGIC	13
J236	1J023A	BREAKPOINT LOGIC	13
J237	1G032A	BREAKPOINT LOGIC	13
J238	1G030A	BREAKPOINT LOGIC	13
J239	1G030B	BREAKPOINT LOGIC	13
J240	1H031B	BREAKPOINT LOGIC	13
J242	1F076A	(NOT-B,+MD12).(B,+MD13)	10
J243	1F076B	(NOTB,+MD13).(B,+MD12)	10
J246	1P046A	RESUME ONE	49
J247	1N035B	RESUME ONE	49
J248	1P030A	RESUME TWO	49
J249	1M035B	RESUME TWO	49
J254	1K035B	P NOT = TO 5	37
J255	1I041B	P=ZERO OR TWO	37
J256	1G031B	P=3 OR 5	37
J257	1H041B	P=THREE	37
J258	1H042B	P=THREE	37
J259	1I032B	P=ONE	37
J260	1I031B	P=ONE	37
J261	1J035B	P=FOUR	37
J262	10027A	CYCLE F F INVERTER	11
J263	10025A	CYCLE F F INVERTER	11
J264	1P020A	CYCLE F F INVERTER	11
J270	1P021B	NOT A CYCLE	11
J271	10031A	A CYCLE	11
J272	1P021A	NOT B CYCLE	11
J273	10031B	B CYCLE	11
J274	10029B	NOT C CYCLE	11
J275	10030A	C CYCLE	11
J276	10028A	NOT D CYCLE	11
J277	10030B	D CYCLE	11
J278	10021B	NOT E CYCLE	11
J279	10029A	E CYCLE	11
J280	10021A	NOT A CYCLE	11
J281	10020B	A CYCLE	11
J283	10020A	B CYCLE	11
J285	1N021B	C CYCLE	11
J286	1N021A	NOT D CYCLE	11
J287	1N019B	D CYCLE	11
J289	1N020A	E CYCLE	11
J291	1M021B	A CYCLE	11
J293	1M021A	B CYCLE	11
J295	1M020B	C CYCLE	11
J296	1M020A	NOT D CYCLE	11
J297	1L023B	ENTER	12
J299	1L017B	E CYCLE	11
J301	10028B	A CYCLE	11
J303	1P027B	B CYCLE	11
J305	1P026B	C CYCLE	11
J306	1K017B	F*ACTIVE.D CYCLE.NOT BUFFER CYCLE	26
J307	1N019A	NOT - LOAD+SWEEP+INTERR.+BUFFER+ENTER	12
J308	1N020B	LOAD+SWEEP+8090 MODE INT+BUFFER+ENTER	12
J309	1P025B	E CYCLE	11
J311	1P035B	A CYCLE	11
J313	1P041B	B CYCLE	11
J315	10042B	C CYCLE	11
J317	1P034B	D CYCLE	11
J327	1Q013B	D CYCLE	11
J337	1P024B	D CYCLE	11
J347	10040B	D CYCLE	11
J357	10025B	D CYCLE	11
J361	1M059B	RNI	3
J362	1D087A	NOT 12TH BIT OF A PRIME	32
J363	1H024B	SIGN RECORD TWO	28
J364	1D088B	NOT 13TH BIT OF A PRIME	32
J365	1D088A	12TH BIT OF A PRIME	32
J366	1T041B	NOT SIGN RECORD 2	28
J367	1D089A	13TH BIT OF A PRIME	32
J377	1M019A	D CYCLE	11
J387	1L035B	D CYCLE	11
J388	1G054B	NOT BUFFER 1 CYCLE	48
J389	1G086B	BUFFER 1 CYCLE	48
J390	1D089B	NOT BUFFER CYCLE	48
J391	1D090A	BUFFER 1 CYCLE	48
J393	1D090B	BUFFER CYCLE	48
J400	1A012B	INTERRUPT TRANSLATION X0	53
J401	1A012A	INTERRUPT TRANSLATION X1	53
J402	1A008B	INTERRUPT TRANSLATION X2	53
J403	1A008A	INTERRUPT TRANSLATION X3	53
J404	1A007B	INTERRUPT TRANSLATION X4	53
J405	1A007A	INTERRUPT TRANSLATION X5	53
J406	1A004B	INTERRUPT TRANSLATION X6	53
J407	1A004A	INTERRUPT TRANSLATION X7	53
J408	1A011B	CARRY LOGIC IN INTERRUPT SCAN COUNTER	53
J409	1A003A	INTERRUPT SCAN COUNTER-ADV 13 TO 1	53
J411	1A011A	INTERRUPT - MANUAL HOLD CKTY.	54
J413	1D010B	INTERRUPT TRANS FOR SET S	53
J414	1D006B	INTERRUPT TRANS FOR SET S	53
J415	1D005B	INTERRUPT TRANS FOR SET S	53
J416	1D004B	INTERRUPT TRANS FOR SET S	53
J418	1D010A	INTERRUPT TRANS. FOR SET S	53
J419	1D009A	INTERRUPT TRANS. FOR SET S	53
J421	1D007A	INTERRUPT TRANS. FOR SET S	53

J422	1D002B	INTERRUPT TRANS. FOR CLEAR S	
J423	1D007B	INTERRUPT TRANS. FOR CLEAR S	
J424	1D005A	INTERRUPT TRANS. FOR SET S	
J425	1D004A	INTERRUPT TRANS. FOR CLEAR S	
J426	1D003A	INTERRUPT TRANS. FOR CLEAR S	
J428	1M037B	NOT MD12 INTERRUPT	
J438	1A019B	INTERRUPT LOGIC 1X	
J439	1A018B	INTERRUPT LOGIC 0X	
J448	1C014B	INTERRUPT SELECT	
J449	1C014A	INTERRUPT SELECT	
J450	1A019A	INTERRUPT LOGIC 1X	
J451	1D001A	INITIATE INTERRUPT	
J452	1A018A	INTERRUPT LOGIC 0X	
J454	1S054A	INTERRUPT 30	
J455	1F010B	NOT INTERRUPT 30	
J456	1S054B	INTERRUPT 40	
J457	1F011B	NOT INTERRUPT 40	
J460	1E021B	BLOCK INTERRUPT TIMING CHAIN	
J800	1F056A	BANK SELECT - BIT 1	
J801	1F056B	BANK SELECT - BIT 2	
J802	1F055A	BANK SELECT - BIT 3	
J804	1H044B	MEMORY NOT BUSY.REQUEST MEMORY	
J806	1E027D	NOT MEMORY GATE	
J808	1C027D	NOT MEMORY GATE	
J809	1F043A	CLEAR DL DRIVE	
J810	1F043B	RESUME 1,SET R/W	
J811	1D068B	X TO Z - BITS 0 THRU 5	
J812	1D068A	X TO Z - BITS 6 THRU 12	
J813	1F041A	RESUME TWO	
J814	1D069B	I TO Z - BITS 0 THRU 5	
J815	1D069A	I TO Z BITS 6 THRU 12	
J816	1F041B	END READ DRIVE	
J817	1F039A	START INHIBIT DRIVE	
J818	1F039B	START WRITE DRIVE	
J819	1F038A	CLEAR READ - WRITE	
J820	1F038B	END WRITE DRIVE	
J821	1F037A	END INHIBIT DRIVE	
J822	1F023A	CLEAR S PRIME	
J823	1F023B	CLEAR S PRIME	
J824	1F037B	CLEAR MEM. BUSY	
J825	1F034A	START DELAY LINE	
J826	1F036A	I TO Z	
J827	1F044A	NOT MASTER CLEAR	
J828	1F040A	SET 13TH BIT OF Z	
J829	1E070A	PARITY ERROR	
J830	1F044B	DISCHARGER DRIVE	
J831	1F045A	MEMORY NOT ACTIVE	
J832	1F045B	MEMORY ACTIVE	
J836	1C071A	PARITY CHECKING TRANSLATIONS	
J837	1C072A	PARITY CHECKING TRANSLATIONS	
J838	1C072B	PARITY CHECKING TRANSLATIONS	
J839	1C073A	PARITY CHECKING TRANSLATIONS	
J840	1C074A	PARITY CHECKING TRANSLATIONS	
J841	1C074B	PARITY CHECKING TRANSLATIONS	
J842	1C075A	PARITY CHECKING TRANSLATIONS	
J843	1C076A	PARITY CHECKING TRANSLATIONS	
J844	1D076A	PARITY CHECKING TRANSLATIONS	
J845	1C076B	PARITY CHECKING TRANSLATIONS	
J846	1D071A	PARITY CHECKING TRANSLATIONS	
J847	1D072A	PARITY CHECKING TRANSLATIONS	
J848	1D072B	PARITY CHECKING TRANSLATIONS	
J849	1D073A	PARITY CHECKING TRANSLATIONS	

53	J850	1D074A	PARITY CHECKING TRANSLATIONS 43
53	J851	1D074B	PARITY CHECKING TRANSLATIONS 43
53	J852	1D075A	PARITY CHECKING TRANSLATIONS 43
53	J853	1E072A	PARITY CHECKING TRANSLATIONS 43
53	J854	1E071A	PARITY CHECKING TRANSLATIONS 43
53	J860	1E027A	DISCHARGER INVERTER 45
53	J861	1E027B	DISCHARGER INVERTER 45
53	J862	1E027C	DISCHARGER INVERTER 45
54	J863	1C027A	DISCHARGER INVERTER 44
54	J864	1C027B	DISCHARGER INVERTER 44
53	J865	1C027C	DISCHARGER INVERTER 44
53	J980	1E019B	8090/8490 MODE INTERRUPT-SELECT 53
53	K000	1F059A	ENABLE P TO U 22
54	K001	1G057A	ENABLE P TO U 22
54	K002	1F062A	ENABLE A TO U 22
54	K003	1F063A	ENABLE A TO U 22
54	K004	1F064A	ENABLE X TO U 22
53	K005	1F064B	ENABLE X TO U 22
41	K006	1F065A	ENABLE BER TO U 22
41	K007	1F065B	ENABLE BER TO U 22
41	K008	1F066A	ENABLE Q TO U 22
41	K009	1F067A	ENABLE Q TO U 22
45	K010	1F068A	ENABLE I 21
44	K011	1F067B	ENABLE I 21
40	K012	1F061A	ENABLE A.2 TO 2ND TO I 21
40	K013	1F060B	ENABLE A.2 TO 2ND TO I 21
40	K014	1F069A	ENABLE X TO I 21
40	K015	1F069B	ENABLE X TO I 21
49	K016	1F070A	ENABLE -X TO I 21
40	K017	1F070B	ENABLE -X TO I 21
40	K018	1F071A	ENABLE Q PRIME TO I 21
40	K019	1F071B	ENABLE Q PRIME TO I 21
40	K020	10024A	8490 MODE 10
40	K021	10024B	8090 MODE 10
40	K022	10023A	INT. MEMORY 49
40	K023	10023B	INT. MEMORY 49
40	K024	10022A	SELECTIVE JUMP ONE 13
40	K025	10022B	SELECTIVE JUMP ONE 13
40	K026	1P023A	SELECTIVE JUMP TWO 13
40	K027	1P023B	SELECTIVE JUMP TWO 13
40	K028	1P022A	SELECTIVE JUMP FOUR 13
40	K029	1P022B	SELECTIVE JUMP FOUR 13
41	K030	1P010A	REQUEST MEMORY READ 27
40	K031	1P011A	REQUEST MEMORY READ 27
43	K032	1T085A	REQUEST MEMORY WRITE 27
40	K033	1T085B	REQUEST MEMORY WRITE 27
41	K034	1T086A	REQUEST MEMORY HALF WRITE 27
41	K035	1T086B	REQUEST MEMORY HALF WRITE 27
43	K036	1H021A	SIGN RECORD ONE 28
43	K037	1H022B	SIGN RECORD ONE 28
43	K038	10044A	SIGN RECORD TWO 28
43	K039	10039A	SIGN RECORD TWO 28
43	K040	1P038A	SELECT RELATIVE BANK 9
43	K041	1P039A	SELECT RELATIVE BANK 9
43	K042	1P040A	SELECT DIRECT BANK 9
43	K043	1P041A	SELECT DIRECT BANK 9
43	K044	1P042A	SELECT INDIRECT BANK 9
43	K045	10040A	SELECT INDIRECT BANK 9
43	K046	10038A	SELECT BUFFER BANK 9
43	K047	10041A	SELECT BUFFER BANK 9
43	K048	1P043A	SELECT ENTIRE MEMORY 9
43	K049	10043A	SELECT ENTIRE MEMORY 9

K050	10026A	INITIAL START	12
K051	10026B	INITIAL START	12
K052	1N026A	RUN	12
K053	1N026B	RUN	12
K054	1N025A	STOP	12
K055	1N024B	STOP	12
K056	1N023A	ENABLE	12
K057	1N023B	ENABLE	12
K058	1N022A	START	12
K059	1N024A	START	12
K060	1P060A	RNI	3
K061	1P060B	RNI	3
K064	1I021A	BFR TO X	37
K065	1I021B	BFR TO X	37
K066	1F092B	LOAD	37
K067	1F092A	LOAD	37
K068	1D092A	SWEEP	12
K069	1D092B	SWEEP	12
K070	10067B	CLEAR INTERRUPT LOCKOUT	3
K071	10067A	CLEAR INTERRUPT LOCKOUT	3
K072	1K027A	ENABLE R	28
K073	1K027B	ENABLE R	28
K074	1E093A	POSITIVE TEST F/F	28
K075	1F085A	POSITIVE TEST F/F	28
K076	1Q031A	E CYCLE PIGGY BACK	11
K078	1D079A	INITIATE DIVIDE	6
K079	1D079B	INITIATE DIVIDE	6
K080	1R002A	F PRIME LESS THAN 2	6
K081	1R001B	F PRIME LESS THAN 2	6
K082	1Q002B	F PRIME LESS THAN 8	6
K083	1R003B	F PRIME LESS THAN 8	6
K084	1M025A	SELECTIVE STOP ONE	12
K085	1M025B	SELECTIVE STOP ONE	12
K086	1M024A	SELECTIVE STOP TWO	12
K087	1M024B	SELECTIVE STOP TWO	12
K088	1M023A	SELECTIVE STOP FOUR	12
K089	1M023B	SELECTIVE STOP FOUR	12
K090	1M022A	INSTRUCTION STEP	12
K091	1M022B	INSTRUCTION STEP	12
K092	1N090A	CYCLE STEP	12
K093	1N090B	CYCLE STEP	12
K094	1M027A	ENT. MEMORY	12
K095	1M027B	ENT. MEMORY	12
K096	1L028A	ENTER	12
K097	1L028B	ENTER	12
K098	1C083A	BUFFER BUSY 2	47
K099	1C084A	BUFFER BUSY 2	47
K100	1B094A	INPUT REQUEST	48
K101	1B093A	INPUT REQUEST	48
K102	1B092B	INFO READY	48
K103	1B092A	INFO READY	48
K104	1B091A	INPUT REQUEST 2	48
K105	1B091B	INPUT REQUEST 2	48
K106	1B090B	INPUT BUFFER	48
K107	1B090A	INPUT BUFFER	48
K108	1I028B	OUTPUT BUFFER	48
K109	1I028A	OUTPUT BUFFER	48
K110	1B088B	BUFFER BUSY	48
K111	1B088A	BUFFER BUSY	48
K112	1B087A	BUFFER CYCLE	48
K113	1B086A	BUFFER CYCLE	48
K114	1F072A	BUFFER 1 CYCLE	48
K115	1F072B	BUFFER 1 CYCLE	48
K116	1B084B	BUFFER 2 CYCLE	48
K117	1B084A	BUFFER 2 CYCLE	48
K118	1B083B	BUFFER GATE	48
K119	1B083A	BUFFER GATE	48
K120	1C079A	NORMAL I/O WAIT	27
K121	1C078B	NORMAL I/O WAIT	27
K122	10004A	INPUT TO A - CHAN. 2	47
K123	10004B	INPUT TO A - CHAN. 2	47
K124	1C080A	ENABLE BER TO A -CHAN. 2	47
K125	1C080B	ENABLE BER TO A -CHAN. 2	47
K126	1C081B	EXTERNAL FUNCTION READY	47
K127	1C081A	EXTERNAL FUNCTION READY	47
K128	1C082A	INPUT REQUEST ONE	47
K129	1C082B	INPUT REQUEST ONE	47
K130	1C085A	PIGGY BACK FOR BUFFER CYCLE	48
K132	1N049A	INFO READY 1	47
K133	10046A	INFO READY 1	47
K134	10087B	BUFFER BYPASS	48
K135	10087A	BUFFER BYPASS	48
K136	1C086A	INPUT DISCONNECT	47
K137	1C086B	INPUT DISCONNECT	47
K138	1B082B	BUFFER - NORMAL	48
K139	1B082A	BUFFER - NORMAL	48
K140	1I027A	DIVIDE OVERFLOW	6
K141	1I027B	DIVIDE OVERFLOW	6
K142	1A093A	INTERNAL BUFFER PARITY ERROR	55
K143	1A093B	INTERNAL BUFFER PARITY ERROR	55
K144	1A092A	CHAN. 2 PARITY ERROR	55
K145	1A092B	CHAN. 2 PARITY ERROR	55
K146	1A091A	CHAN 3 PARITY ERROR	55
K147	1A091B	CHAN 3 PARITY ERROR	55
K156	1J027A	ADD OR SUBTRACT OVERFLOW	55
K157	1J028A	ADD OR SUBTRACT OVERFLOW	55
K158	1H027A	MEMORY PARITY ERROR	12
K159	1H027B	MEMORY PARITY ERROR	12
K160	1E091A	BLOCK I/O=CONTROL 1	47
K161	1E091B	BLOCK I/O=CONTROL 1	47
K162	1G025A	ENABLE BPE	48
K163	1G025B	ENABLE BPE	48
K164	1A089A	BUFFER REPLY	48
K165	1A088A	BUFFER REPLY	48
K166	1A087A	NORMAL REPLY	47
K167	1A086A	NORMAL REPLY	47
K168	1A090A	BLOCK BUFFER CONTROL	48
K169	1A090B	BLOCK BUFFER CONTROL	48
K170	1P037B	A CYCLE	11
K171	1P037A	A CYCLE	11
K172	1P036A	B CYCLE	11
K173	1P035A	B CYCLE	11
K174	10034B	C CYCLE	11
K175	1P034A	C CYCLE	11
K176	1P033A	D CYCLE	11
K177	1P032A	D CYCLE	11
K178	1P031A	E CYCLE	11
K179	1Q030A	E CYCLE	11
K180	1N032	BUFFER CHAN 2 BUSY	54
K181	1N032B	BUFFER CHAN 2 BUSY	54
K182	1N031A	BUFFER CHAN 3 BUSY	54
K183	1N031B	BUFFER CHAN 3 BUSY	54
K192	1K021A	INIT. BUFFER INPUT I, CH 2	54
K193	1K021B	INIT. BUFFER INPUT I, CH 2	54

K194	1K020A	BUFFER OUTPUT - CHAN 2	54
K195	1K020B	BUFFER OUTPUT - CHAN 2	54
K196	1K019A	CLEAR BUFFER CONTROL - CH 2	54
K197	1K019B	CLEAR BUFFER CONTROL - CH 2	
K198	1K018A	MTM2	54
K199	1K018B	MTM2	54
K200	1J021A	BUFFER BANK CONTROL - CH 2	54
K201	1J021B	BUFFER BANK CONTROL - CH 2	54
K204	1J019A	A TO BXR - CH 2	5
K205	1J019B	A TO BXR - CH 2	5
K206	1J018A	A TO BER - CH 2	5
K207	1J018B	A TO BER - CH 2	5
K208	1K008A	COMP TO COMP INTERRUPT	4
K209	1K008B	COMP TO COMP INTERRUPT	4
K210	1Q082A	MDS	32
K211	1Q082B	MDS	32
K212	1M016A	REQUEST MEMORY	27
K213	1L015A	REQUEST MEMORY PIGGY BACK	27
K214	1M015A	REQUEST MEMORY PIGGY BACK	27
K215	1Q090A	MUT-MUH	32
K216	1Q090B	MUT-MUH	32
K218	1M011A	REQUEST MEMORY PIGGY BACK	27
K220	1E011A	8090 OR 8490 MODE SELECT	10
K221	1E011B	8090 OR 8490 MODE SELECT	10
K222	1P062A	PLUS 1 TO I INVERTERS	21
K223	1P062B	PLUS 1 TO I INVERTERS	21
K224	1P063A	PLUS 2 TO I INVERTERS	21
K225	1P063B	PLUS 2 TO I INVERTERS	21
K226	1E088A	EXT. FUNCTION RDY. CH 2	47
K227	1E088B	EXT. FUNCTION RDY. CH 2	47
K230	1P009A	PIGGY BACK FOR READ	27
K242	1G027A	BUFFER MD12/MD13 MODE	10
K243	1G027B	BUFFER MD12/MD13 MODE	10
K260	1E090A	BLOCK I/O-CONTROL 2	47
K261	1E090B	BLOCK I/O-CONTROL 2	47
K278	1P070B	E PRIME CYCLE	11
K279	1P070A	E PRIME CYCLE	11
K280	1Q003A	PIGGY BACK - F LESS THAN 2	6
K300	1A006B	INTERRUPT SCAN COUNTER RANK 1	53
K301	1A006A	INTERRUPT SCAN COUNTER RANK 1	53
K302	1A005B	INTERRUPT SCAN COUNTER RANK 2	53
K303	1A005A	INTERRUPT SCAN COUNTER RANK 2	53
K304	1B018B	COMP.-COMP. HOLD	54
K305	1B018A	COMP.-COMP. HOLD	54
K306	1B017A	MANUAL HOLD	54
K307	1C017B	MANUAL HOLD	54
K308	1C018A	MASTER LOCKOUT	54
K309	1C017A	MASTER LOCKOUT	54
K310	1A010B	INTERRUPT SCAN COUNTER RANK 1	53
K311	1A010A	INTERRUPT SCAN COUNTER RANK 1	53
K312	1A009B	INTERRUPT SCAN COUNTER RANK 2	53
K313	1A009A	INTERRUPT SCAN COUNTER RANK 2	53
K314	1B016B	BUFFER TERM. 1 HOLD	54
K315	1B016A	BUFFER TERM 1 HOLD	54
K320	1A014B	INTERRUPT SCAN COUNTER RANK 1	53
K321	1A014A	INTERRUPT SCAN COUNTER RANK 1	53
K322	1A013B	INTERRUPT SCAN COUNTER RANK 2	53
K323	1A013A	INTERRUPT SCAN COUNTER RANK 2	53
K324	1C009B	BUFFER TERM. 2 HOLD	54
K325	1C009A	BUFFER TERM. 2 HOLD	54
K328	1C008B	CHAN 2 LOCKOUT	54
K329	1C008A	CHAN 2 LOCKOUT	54
K330	1A017B	INTERRUPT SCAN COUNTER RANK 1	53
K331	1A017A	INTERRUPT SCAN COUNTER RANK 1	53
K332	1A016B	INTERRUPT SCAN COUNTER RANK 2	53
K333	1A016A	INTERRUPT SCAN COUNTER RANK 2	53
K334	1C007B	BUFFER TERM 3 HOLD	54
K335	1C007A	BUFFER TERM 3 HOLD	54
K338	1C006B	CHAN 3 LOCKOUT	54
K339	1C006A	CHAN 3 LOCKOUT	54
K400	1B020B	MANUAL INTERRUPT	54
K401	1B020A	MANUAL INTERRUPT	54
K402	1C019B	SEQUENCE RESYNC-INTERRUPT	53
K403	1C019A	SEQUENCE RESYNC-INTERRUPT	53
K404	1C020B	INTERRUPT RNI	53
K405	1C020A	INTERRUPT RNI	53
K406	1P092B	INTERRUPT SEQUENCE	53
K407	1P092A	INTERRUPT SEQUENCE	53
K408	1C010A	MASTER LOCKOUT RESYNC-INTERRUPT	54
K409	1C011A	MASTER LOCKOUT RESYNC-INTERRUPT	54
K410	1E006A	POWER ON - M.C.	10
K411	1E006B	POWER ON - M.C.	10
K412	1C013A	CHANNEL 1 RESYNC-PIGGY BACK	54
K414	1E003A	MD13 INTERRUPT RNI	53
K415	1E003B	MD13 INTERRUPT RNI	53
K416	1E004A	MD13 INTERRUPT SEQUENCE	53
K417	1E004B	MD13 INTERRUPT SEQUENCE.	53
K418	1C012A	CHANNEL 1 RESYNC	54
K419	1C011B	CHANNEL 1 RESYNC	54
K420	1D011B	RESTART ENABLE	53
K421	1D011A	RESTART ENABLE	53
K422	1B005A	CHANNEL 2 RESYNC - PIGGY BACK	54
K428	1B004A	CHANNEL 2 RESYNC	54
K429	1B006A	CHANNEL 2 RESYNC	54
K432	1B005B	CHANNEL 3 RESYNC - PIGGY BACK	54
K438	1B007A	CHANNEL 3 RESYNC	54
K439	1B006B	CHANNEL 3 RESYNC	54
K500	1G055A	PIGGY BACK FOR ENABLE P TO U	22
K800	1F053A	MEMORY ACTIVE	41
K801	1F053B	MEMORY ACTIVE	41
K802	1F052A	MEMORY BUSY	41

K803	1F052B	MEMORY BUSY	41
K804	1F051A	MEMORY GATE	41
K805	1F051B	MEMORY GATE	41
K806	1F050A	READ DRIVE	41
K807.	1F050B	READ DRIVE	41
K808	1F049A	WRITE DRIVE	41
K809	1F049B	WRITE DRIVE	41
K810	1E069A	MEMORY READ	41
K811	1E069B	MEMORY READ	41
K812	1E068A	MEMORY WRITE	41
K813	1E068B	MEMORY WRITE	41
K814	1E067A	MEMORY HALF WRITE	41
K815	1E067B	MEMORY HALF WRITE	41
K816	1C056A	ODD INHIBIT - STRIPE ZERO	41
K817	1C056B	ODD INHIBIT - STRIPE ZERO	41
K818	1C055A	ODD INHIBIT - STRIPE ONE	41
K819	1C055B	ODD INHIBIT - STRIPE ONE	41
K820	1C054A	ODD INHIBIT - STRIPE TWO	41
K821	1C054B	ODD INHIBIT - STRIPE TWO	41
K822	1C053A	ODD INHIBIT - STRIPE THREE	41
K823	1C053B	ODD INHIBIT - STRIPE THREE	41
K824	1C052A	EVEN INHIBIT - STRIPE ZERO	41
K825	1C052B	EVEN INHIBIT - STRIPE ZERO	41
K826	1C051A	EVEN INHIBIT - STRIPE ONE	41
K827	1C051B	EVEN INHIBIT - STRIPE ONE	41
K828	1C050A	EVEN INHIBIT - STRIPE TWO	41
K829	1C050B	EVEN INHIBIT - STRIPE TWO	41
K830	1C049A	EVEN INHIBIT - STRIPE THREE	41
K831	1C049B	EVEN INHIBIT - STRIPE THREE	41
K832	1F042A	DISCHARGER	41
K833	1F042B	DISCHARGER	41
L000	1H036A	DISPLAY S P BER	8
L001	1H044A	DISPLAY BXR A A PRIME	8
L002	1H038A	DISPLAY BFR Q Q PRIME	7
L003	1H032A	DISPLAY Z F X	7
L004	1H053B	DISPLAY MCS	52
L005	1T091B	SELECT 8090 MODE	10
L010	1I036A	DISPLAY S P BER	8
L011	1I044A	DISPLAY BXR A A PRIME	8
L012	1I038A	DISPLAY BFR Q Q PRIME	7
L013	1I032A	DISPLAY Z F X	7
L014	1I053B	DISPLAY MCS	52
L020	1J036A	DISPLAY S P BER	8
L021	1J044A	DISPLAY BXR A A PRIME	8
L022	1J038A	DISPLAY BFR Q Q PRIME	7
L023	1J032A	DISPLAY Z F X	7
L024	1J053B	DISPLAY MCS	52
L025	1T074A	DISPLAY REL. BANK SELECT	9
L026	1T091A	DISPLAY DIR. BANK SELECT	9
L027	1T084B	DISPLAY IND. BANK SELECT	9
L028	1T073A	DISPLAY BUFFER BANK SELECT	9
L029	1T074B	DISPLAY ENTIRE MEMORY	9
L030	1K036A	DISPLAY S P BER	8
L031	1K044A	DISPLAY BXR A A PRIME	8
L032	1K038A	DISPLAY BFR Q Q PRIME	7
L033	1K032A	DISPLAY Z F X	7
L034	1K053B	DISPLAY MCS	52
L037	1T083B	LOAD INDICATOR	37
L038	1T073B	RUN DISABLE FOR CONSOLE	12
L039	1T083A	RUN INDICATOR	12
L040	1L036A	DISPLAY S P BER	8
L041	1L044A	DISPLAY BXR A A PRIME	8
L042	1L038A	DISPLAY BFR Q Q PRIME	7
L043	1L032A	DISPLAY Z F X	7
L045	1T084A	INTERRUPT INDICATOR	54
L050	1M036A	DISPLAY S P BER	8
L051	1M044A	DISPLAY BXR A A PRIME	8
L052	1M038A	DISPLAY BFR Q Q PRIME	7
L053	1M032A	DISPLAY Z F X	7
L060	1M035A	DISPLAY S P BER	8
L061	1M043A	DISPLAY BXR A A PRIME	8
L062	1M037A	DISPLAY BFR Q Q PRIME	7
L063	1M031A	DISPLAY Z F X	7
L070	1L035A	DISPLAY S P BER	8
L071	1L043A	DISPLAY BXR A A PRIME	8
L072	1L037A	DISPLAY BFR Q Q PRIME	7
L073	1L031A	DISPLAY Z F X	7
L080	1K035A	DISPLAY S P BER	8
L081	1K043A	DISPLAY BXR A A PRIME	8
L082	1K037A	DISPLAY BFR Q Q PRIME	7
L083	1K031A	DISPLAY Z F X	7
L090	1J035A	DISPLAY S P BER	8
L091	1J043A	DISPLAY BXR A A PRIME	8
L092	1J037A	DISPLAY BFR Q Q PRIME	7
L093	1N058A	DISPLAY Z F X	7
L100	1I035A	DISPLAY S P BER	8
L101	1I043A	DISPLAY BXR A A PRIME	8
L102	1I037A	DISPLAY BFR Q Q PRIME	7
L103	1N059A	DISPLAY Z F X	7
L110	1H035A	DISPLAY S P BER	8
L111	1H043A	DISPLAY BXR A A PRIME	8
L112	1H037A	DISPLAY BFR Q Q PRIME	7
L113	1H031A	DISPLAY Z F X	7
L120	1G035A	DISPLAY S P BER	8
L121	1G043A	DISPLAY BXR A A PRIME	8
L122	1G037A	DISPLAY BFR Q Q PRIME	7
L123	1G031A	DISPLAY Z F X	7
L201	1E021A	DISPLAY A CYCLE	11
L202	1E020A	DISPLAY B CYCLE	11
L203	1E019A	DISPLAY C CYCLE	11
L204	1E018A	DISPLAY D CYCLE	11
L205	1E017A	DISPLAY E CYCLE	11
L206	1L008B	DISPLAY ERR	12
L207	1E016B	DISPLAY COMPUTER PARITY ERROR	54
L208	1J032B	DISPLAY OVERFLOW ERROR	54
L209	1E014A	DISPLAY BUFFER PARITY ERROR	54
L210	1E016A	DISPLAY SELECT	47
L211	1E020B	DISPLAY OUT	47
L212	1L064B	DISPLAY INP	47
L213	1E018B	DISPLAY INPUT BUFFER	48
L214	1E017B	DISPLAY OUTPUT BUFFER	48
L215	1E015B	DISPLAY INTERRUPT	53
M800	1T016A	POWER FAILURE RECEIVER	12
N000	1G087A	Q PRIME TO A	24
N001	1N088A	CLEAR A	24
N002	1G080A	A TO A PRIME	24
N003	1H078A	A PRIME TO A	24
N004	1J078B	Q TO A PRIME	24
N005	1F087A	A LEFT SHIFT	25
N006	1G080B	PROBE A PRIME	24
N007	1H077A	A RIGHT SHIFT	25
N008	1N083A	TOGGLE A PRIME	25
N009	1N084A	CLEAR A PRIME	24
N010	1I076B	A TO Q PRIME	25

N011	1F088A	SHIFT Q LEFT	25
N012	1I077A	Q TO Q PRIME	25
N013	1G074A	Q PRIME TO Q	24
N014	1N065A	Z INT. TO X	26
N015	1I078A	SHIFT Q RIGHT	25
N016	1N068A	Z EXT. TO X	26
N017	1I078B	X TO Q PRIME	25
N018	1B021B	INTERRUPT	53
N019	1H057A	A PRIME TO X	26
N020	1R012A	REDUCE F LOWER	14
N021	1G066A	CLEAR X	26
N022	1G051A	-FE TO IND. BANK	23
N023	1H057B	A PRIME TO S	25
N024	1G051B	FE TO DIR. BANK	23
N025	1I057A	X TO S	26
N026	1G050B	FE TO BUF. BANK	23
N027	1G056A	P TO S	26
N028	1G076A	BANK TO Q AND Q PRIME	23
N029	1R013A	F TO F PRIME	25
N030	1G071B	BANK TO A	24
N031	1R023B	SET FE	14
N032	1R032B	Z INT. TO F	25
N033	1E010A	SET INTERRUPT LOCKOUT	15
N034	1R026A	Z EXT. TO F	15
N035	1G050A	A AND Q PRIME TO BANK	53
N036	1G044A	A PRIME TO BER	15
N037	1R013B	CLEAR F	23
N038	1G040A	X TO BXR	28
N039	1O049A	CLEAR BFR	15
N040	1R026B	REDUCE F UPPER	51
N041	1G041A	CLEAR BXR	50
N042	1N066A	INPUT OUTPUT TO X	14
N043	1G046A	CLEAR BER	5
N044	1N067A	NORMAL INPUT TO X	26
N045	1G034A	S TO P	28
N046	1N052B	X TO BUFFER BANK	26
N048	1G070B	RELATIVE BANK TO X	25
N050	1N052A	FE TO RELATIVE BANK	23
N053	1N051B	CLEAR RELATIVE BANK	23
N054	1A079A	BUFFER RESYNC	48
N055	1N051A	CLEAR INDIRECT BANK	23
N056	1G001B	EXT. INPUT TO BFR	50
N057	1N054A	CLEAR DIRECT BANK	23
N058	1A079B	BER=BXR	48
N059	1N054B	CLEAR BUFFER BANK	23
N060	1N060A	ERROR REGISTER TO X	26
N062	1G003B	Z EXT. TO BFR	50
N064	1D015B	CLEAR INTERRUPT LOCKOUT	53
N065	1E089A	CLEAR SELECT ENABLES	22
N066	1G002B	Z INT. TO BFR	50
N100	1N087A	Q PRIME TO A	24
N101	1N088B	CLEAR A	24
N102	1N082A	A TO A PRIME	24
N103	1L079A	A PRIME TO A	24
N104	1K078A	Q TO A PRIME	24
N105	1G084A	A LEFT SHIFT	25
N106	1M078A	PROBE A PRIME	24
N107	1J079B	A RIGHT SHIFT	25
N108	1N083B	TOGGLE A PRIME	24
N109	1N084B	CLEAR A PRIME	24
N110	1L076A	A TO Q PRIME	25
N111	1G075A	SHIFT Q LEFT	25
N112	1L077A	Q TO Q PRIME	25
N113	1J076B	Q PRIME TO Q	24
N114	1N065B	Z INT. TO X	26
N115	1J077B	SHIFT Q RIGHT	25
N116	1N068B	Z EXT. TO X	26
N117	1K077A	X TO Q PRIME	25
N118	1B021A	INTERRUPT	53
N119	1K057A	A PRIME TO X	26
N121	1G067A	CLEAR X	26
N122	1N050B	FE TO IND. BANK	23
N123	1M057A	A PRIME TO S	25
N124	1N055A	FE TO DIR. BANK	23
N125	1L057A	X TO S	26
N126	1N055B	FE TO BUF. BANK	23
N127	1N056A	P TO S	25
N128	1M077A	BANK TO Q AND Q PRIME	24
N129	1R012B	F TO F PRIME	14
N130	1N072B	BANK TO A	25
N132	1R032A	Z INT. TO F	15
N134	1R049A	Z EXT. TO F	15
N135	1M052A	A AND Q PRIME TO BANK	23
N136	1G044B	A PRIME TO BER	28
N137	1R023A	CLEAR F	15
N138	1G040B	X TO BXR	51
N139	1O049B	CLEAR BFR	50
N141	1G041B	CLEAR BXR	5
N142	1N066B	INPUT OUTPUT TO X	26
N143	1G046B	CLEAR BER	28
N144	1N067B	NORMAL INPUT TO X	26
N145	1M030A	S TO P	25
N150	1N050A	FE TO RELATIVE BANK	23
N156	1G001A	EXT. INPUT TO BFR	50
N160	1N060B	ERROR REGISTER TO X	26
N162	1G003A	Z EXT. TO BFR	50
N165	1E089B	CLEAR SELECT ENABLES	22
N166	1G002A	Z INT. TO BFR	50
N200	1N087B	Q PRIME TO A	24
N202	1N082B	A TO A PRIME	24
N203	1L079B	A PRIME TO A	24
N204	1K078B	Q TO A PRIME	24
N205	1M079A	A LEFT SHIFT	25
N206	1M078B	PROBE A PRIME	24
N207	1M079B	A RIGHT SHIFT	25
N210	1L076B	A TO Q PRIME	25
N211	1M076A	SHIFT Q LEFT	25
N212	1L077B	Q TO Q PRIME	25
N213	1M076B	Q PRIME TO Q	24
N215	1K076A	SHIFT Q RIGHT	25
N217	1K077B	X TO Q PRIME	25
N218	1E010B	INTERRUPT	53
N219	1K057B	A PRIME TO X	26
N223	1M057B	A PRIME TO S	25
N225	1L057B	X TO S	26
N227	1N056B	P TO S	25
N228	1G076B	BANK TO Q AND Q PRIME	24
N230	1G071A	BANK TO A	25
N235	1M052B	A AND Q PRIME TO BANK	23
N237	1R049B	CLEAR F	15
N244	1N069A	NORMAL INPUT TO X	26
N245	1M030B	S TO P	25
N300	1G087B	Q PRIME TO A	24
N302	1J078A	A TO A PRIME	24

N303	1H078B	A PRIME TO A
N304	1I079B	Q TO A PRIME
N305	1J079A	A LEFT SHIFT
N306	1G070A	PROBE A PRIME
N307	1G079A	A RIGHT SHIFT
N310	1I077B	A TO Q PRIME
N311	1J076A	SHIFT Q LEFT
N312	1I079A	Q TO Q PRIME
N313	1J077A	Q PRIME TO Q
N315	1K076B	SHIFT Q RIGHT
N317	1I076A	X TO Q PRIME
N319	1J057B	A PRIME TO X
N323	1J057A	A PRIME TO S
N325	1I057B	X TO S
N327	1G056B	P TO S
N328	1N072A	BANK TO Q AND Q PRIME
N344	1N069B	NORMAL INPUT TO X
N345	1G034B	S TO P
N405	1F086B	A LEFT SHIFT
N428	1M077B	BANK TO Q AND Q PRIME
N505	1F086A	A LEFT SHIFT
N528	1G084B	BANK TO Q AND Q PRIME
N711	1G066B	SHIFT Q LEFT
N900	1L017A	INV CLOCK - RESYNC CIRCUIT
N901	1D093B	INV. CLOCK
N902	1D077B	INV. CLOCK
N910	1D077A	INV CLOCK - RESYNC CIRCUIT
N920	1Q063B	INV CLOCK - RESYNC CIRCUIT
P000	1H034A	P REGISTER
P001	1H034B	P REGISTER
P010	1I034A	P REGISTER
P011	1I034B	P REGISTER
P020	1J034A	P REGISTER
P021	1J034B	P REGISTER
P030	1K034A	P REGISTER
P031	1K034B	P REGISTER
P040	1L034A	P REGISTER
P041	1L034B	P REGISTER
P050	1M034A	P REGISTER
P051	1M034B	P REGISTER
P060	1M033A	P REGISTER
P061	1M033B	P REGISTER
P070	1L033A	P REGISTER
P071	1L033B	P REGISTER
P080	1K033A	P REGISTER
P081	1K033B	P REGISTER
P090	1J033A	P REGISTER
P091	1J033B	P REGISTER
P100	1I033A	P REGISTER
P101	1I033B	P REGISTER
P110	1H033A	P REGISTER
P111	1H033B	P REGISTER
P120	1G033A	P REGISTER
P121	1G033B	P REGISTER
Q000	1H075A	Q REGISTER
Q001	1H074A	Q REGISTER
Q002	1H076A	Q REGISTER
Q003	1H076B	Q REGISTER
Q004	1H071A	Q PRIME REGISTER
Q005	1H070A	Q PRIME REGISTER
Q006	1H063B	Q PRIME REGISTER

24	Q007	1H062B	Q PRIME REGISTER 34
24	Q010	1I075A	Q REGISTER 33
25	Q011	1I074A	Q REGISTER 33
24	Q014	1I071A	Q PRIME REGISTER 34
25	Q015	1I070A	Q PRIME REGISTER 34
25	Q020	1J075A	Q REGISTER 33
25	Q021	1J074A	Q REGISTER 33
25	Q024	1J071A	Q PRIME REGISTER 34
24	Q025	1J070A	Q PRIME REGISTER 34
25	Q030	1K075A	Q REGISTER 33
25	Q031	1K074A	Q REGISTER 33
26	Q034	1K071A	Q PRIME REGISTER 34
25	Q035	1K070A	Q PRIME REGISTER 34
26	Q040	1L075A	Q REGISTER 33
25	Q041	1L074A	Q REGISTER 33
24	Q044	1L071A	Q PRIME REGISTER 34
	Q045	1L070A	Q PRIME REGISTER 34
26	Q050	1M075A	Q REGISTER 33
25	Q051	1M074A	Q REGISTER 33
25	Q054	1M071A	Q PRIME REGISTER 34
24	Q055	1M070A	Q PRIME REGISTER 34
25	Q060	1M073A	Q REGISTER 33
24	Q061	1M072A	Q REGISTER 33
25	Q064	1M069A	Q PRIME REGISTER 34
12	Q065	1M068A	Q PRIME REGISTER 34
3	Q070	1L073A	Q REGISTER 33
48	Q071	1L072A	Q REGISTER 33
48	Q074	1L069A	Q PRIME REGISTER 34
49	Q075	1L068A	Q PRIME REGISTER 34
29	Q080	1K073A	Q REGISTER 33
29	Q081	1K072A	Q REGISTER 33
29	Q084	1K069A	Q PRIME REGISTER 34
29	Q085	1K068A	Q PRIME REGISTER 34
29	Q090	1J073A	Q REGISTER 33
29	Q091	1J072A	Q REGISTER 33
29	Q094	1J069A	Q PRIME REGISTER 34
29	Q095	1J068A	Q PRIME REGISTER 34
29	Q100	1I073A	Q REGISTER 33
29	Q101	1I072A	Q REGISTER 33
29	Q104	1I069A	Q PRIME REGISTER 34
29	Q105	1I068A	Q PRIME REGISTER 34
29	Q110	1H073A	Q REGISTER 33
29	Q111	1H072A	Q REGISTER 33
29	Q114	1H069A	Q PRIME REGISTER 34
29	Q115	1H068A	Q PRIME REGISTER 34
29	Q120	1G073A	Q REGISTER 33
29	Q121	1G072A	Q REGISTER 33
29	Q124	1G069A	Q PRIME REGISTER 34
29	Q125	1G068A	Q PRIME REGISTER 34
29	R000	1T067A	EXT MEM.DATA TO X AND F 35
29	R001	1T067B	EXT MEM.DATA TO X AND F 35
29	R002	1T066A	EXT MEM.DATA TO X AND F 35
29	R003	1T066B	EXT MEM.DATA TO X AND F 35
29	R004	1T065A	EXT MEM.DATA TO X AND F 35
29	R005	1T065B	EXT MEM.DATA TO X AND F 35
33	R006	1T064A	EXT MEM.DATA TO X AND F 36
33	R007	1T064B	EXT MEM.DATA TO X AND F 36
33	R008	1T063A	EXT MEM.DATA TO X AND F 36
33	R009	1T063B	EXT MEM.DATA TO X AND F 36
34	R010	1T062A	EXT MEM.DATA TO X AND F 36
34	R011	1T062B	EXT MEM.DATA TO X AND F 36
34	R012	1T061A	EXT MEM.DATA TO X AND F 36

R041	1T049A	RESUME ONE	49
R042	1T049B	RESUME TWO	49
R043	1T037A	PARITY ERROR	55
R044	1T042B	POWER FAILURE RECEIVER FROM MEMORY UNIT-NORMAL 0	55
R050	1T055B	INPUT-OUTPUT DATA TO COMPUTE	35
R051	1T055A	INPUT-OUTPUT DATA TO COMPUTE	35
R052	1T056B	INPUT-OUTPUT DATA TO COMPUTE	35
R053	1T056A	INPUT-OUTPUT DATA TO COMPUTE	35
R054	1T057B	INPUT-OUTPUT DATA TO COMPUTE	35
R055	1T057A	INPUT-OUTPUT DATA TO COMPUTE	35
R056	1T058B	INPUT-OUTPUT DATA TO COMPUTE	36
R057	1T058A	INPUT-OUTPUT DATA TO COMPUTE	36
R058	1T059B	INPUT-OUTPUT DATA TO COMPUTE	36
R059	1T059A	INPUT-OUTPUT DATA TO COMPUTE	36
R060	1T060B	INPUT-OUTPUT DATA TO COMPUTE	36
R061	1T060A	INPUT-OUTPUT DATA TO COMPUTE	36
R062	1T061B	INPUT-OUTPUT DATA TO COMPUTE	36
R077	1T001A	INPUT READY	47
R081	1T003A	PARITY ERROR-CHAN. TWO	55
R082	1T003B	PARITY ERROR-CHAN. THREE	55
R083	1T042A	POWER FAILURE RECEIVER FROM I/O UNIT-NORMAL 0	54
R170	1T034A	COMP. TO COMP. INTERRUPT	54
R171	1T033B	INTERRUPT 30 - BUFFER	54
R172	1T033A	INTERRUPT 40 - BUFFER	54
R173	1T053A	INTERRUPT 30 - NORMAL	54
R174	1T053B	INTERRUPT 40 - NORMAL	54
R175	1T030A	POWER FAILURE RECEIVER FROM COMPUTE UNIT-NORM. 1	54
R183	1T004A	BUFFER TERMINATE-CHAN. TWO	54
R184	1T004B	BUFFER TERMINATE-CHAN. THREE	54
R185	1T005A	INTERRUPT ONE-CHAN. TWO	54
R186	1T005B	INTERRUPT TWO-CHAN. TWO	54
R187	1T006A	INTERRUPT ONE-CHAN. THREE	54
R188	1T006B	INTERRUPT TWO-CHAN. THREE	54
R279	1T034B	CHAN. 2 BUSY	54
R380	1T036B	CHAN. 3 BUSY	54
R720	1T007A	NORMAL INPUT DATA	35
R721	1T007B	NORMAL INPUT DATA	35
R722	1T008A	NORMAL INPUT DATA	35
R723	1T008B	NORMAL INPUT DATA	35
R724	1T009A	NORMAL INPUT DATA	35
R725	1T009B	NORMAL INPUT DATA	35
R726	1T010A	NORMAL INPUT DATA	36
R727	1T010B	NORMAL INPUT DATA	36
R728	1T011A	NORMAL INPUT DATA	36
R729	1T011B	NORMAL INPUT DATA	36
R730	1T012A	NORMAL INPUT DATA	36
R731	1T012B	NORMAL INPUT DATA	36
R732	1T013B	NORMAL INPUT DATA	36
R733	1T002B	INPUT READY-NORMAL	47
R734	1T013A	OUTPUT RESUME-NORMAL	47
R735	1T002A	INPUT DISCONNECT - NORMAL	47
R740	1T076A	BUFFER INPUT DATA	50
R741	1T076B	BUFFER INPUT DATA	50
R742	1T077A	BUFFER INPUT DATA	50
R743	1T077B	BUFFER INPUT DATA	50
R744	1T078A	BUFFER INPUT DATA	50
R745	1T078B	BUFFER INPUT DATA	50
R746	1T079A	BUFFER INPUT DATA	50
R747	1T079B	BUFFER INPUT DATA	50
R748	1T080A	BUFFER INPUT DATA	50
R749	1T080B	BUFFER INPUT DATA	50
R750	1T081A	BUFFER INPUT DATA	50
R751	1T081B	BUFFER INPUT DATA	50
R752	1T071B	BUFFER INPUT DATA	50
R753	1T082B	INPUT READY-BUFFER	48
R754	1T082A	INPUT DISCONNECT-BUFFER	48
R755	1T071A	OUTPUT RESUME-BUFFER	48
R800	1F035A	I TO Z	40
S000	1H056A	S REGISTER	30
S001	1H055A	S REGISTER	30
S004	1B025A	S PRIME REGISTER	41
S005	1B025B	S PRIME REGISTER	41
S010	1I056A	S REGISTER	30
S011	1I055A	S REGISTER	30
S014	1B024A	S PRIME REGISTER	41
S015	1B024B	S PRIME REGISTER	41
S020	1J056A	S REGISTER	30
S021	1J055A	S REGISTER	30
S024	1B023A	S PRIME REGISTER	41
S025	1B023B	S PRIME REGISTER	41
S030	1K056A	S REGISTER	30
S031	1K055A	S REGISTER	30
S034	1B022A	S PRIME REGISTER	41
S035	1B022B	S PRIME REGISTER	41
S040	1L056A	S REGISTER	30
S041	1L055A	S REGISTER	30
S044	1C024A	S PRIME REGISTER	41
S045	1C024B	S PRIME REGISTER	41
S050	1M056A	S REGISTER	30
S051	1M055A	S REGISTER	30
S054	1C023A	S PRIME REGISTER	41
S055	1C023B	S PRIME REGISTER	41
S060	1M054A	S REGISTER	30
S061	1M053A	S REGISTER	30
S064	1C022A	S PRIME REGISTER	41
S065	1C022B	S PRIME REGISTER	41
S070	1L054A	S REGISTER	30
S071	1L053A	S REGISTER	30
S074	1D024A	S PRIME REGISTER	41
S075	1D024B	S PRIME REGISTER	41
S080	1K054A	S REGISTER	30
S081	1K053A	S REGISTER	30
S084	1D023A	S PRIME REGISTER	41
S085	1D023B	S PRIME REGISTER	41
S090	1J054A	S REGISTER	30
S091	1J053A	S REGISTER	30
S094	1D022A	S PRIME REGISTER	41
S095	1D022B	S PRIME REGISTER	41
S100	1I054A	S REGISTER	30
S101	1I053A	S REGISTER	30
S104	1E024A	S PRIME REGISTER	41
S105	1E024B	S PRIME REGISTER	41
S110	1H054A	S REGISTER	30
S111	1H053A	S REGISTER	30
S114	1E023A	S PRIME REGISTER	41
S115	1E023B	S PRIME REGISTER	41
S120	1G054A	S REGISTER	30
S121	1G053A	S REGISTER	30
S122	1G059B	PIGGY BACK-13TH BIT OF S REGISTER.	30
S124	1E022A	S PRIME REGISTER	41
S125	1E022B	S PRIME REGISTER	41
S800	1F058A	MEMORY BANK SELECT SWITCH	41
S801	1F058B	MEMORY BANK SELECT SWITCH	41
S802	1F058C	MEMORY BANK SELECT SWITCH	41

S900	1F014A	MEMORY-REFERENCE TIME SELECT SWITCH	41
S980	1F014D	8090/8490 MODE INTERRUPT SELECT SWITCH	53
T000	1H025A	COMPUTE TO MEMORY-DATA	49
T001	1I025A	COMPUTE TO MEMORY-DATA	49
T002	1J022A	COMPUTE TO MEMORY-DATA	49
T003	1K022A	COMPUTE TO MEMORY-DATA	49
T004	1M018A	COMPUTE TO MEMORY-DATA	49
T005	1M017A	COMPUTE TO MEMORY-DATA	49
T006	1M018B	COMPUTE TO MEMORY-DATA	49
T007	1M017B	COMPUTE TO MEMORY-DATA	49
T008	1K022B	COMPUTE TO MEMORY-DATA	49
T009	1J022B	COMPUTE TO MEMORY-DATA	49
T010	1I025B	COMPUTE TO MEMORY-DATA	49
T011	1H025B	COMPUTE TO MEMORY-DATA	49
T012	1G026B	COMPUTE TO MEMORY-DATA	49
T019	1G029A	COMPUTE TO MEMORY-ADDRESS	52
T020	1H029B	COMPUTE TO MEMORY-ADDRESS	30
T021	1I029A	COMPUTE TO MEMORY-ADDRESS	30
T022	1J029A	COMPUTE TO MEMORY-ADDRESS	30
T023	1K029A	COMPUTE TO MEMORY-ADDRESS	30
T024	1L029A	COMPUTE TO MEMORY-ADDRESS	30
T025	1M029A	COMPUTE TO MEMORY-ADDRESS	30
T026	1M029B	COMPUTE TO MEMORY-ADDRESS	30
T027	1L029B	COMPUTE TO MEMORY-ADDRESS	30
T028	1K029B	COMPUTE TO MEMORY-ADDRESS	30
T029	1J029B	COMPUTE TO MEMORY-ADDRESS	30
T030	1I029B	COMPUTE TO MEMORY-ADDRESS	30
T031	1H029A	COMPUTE TO MEMORY-ADDRESS	30
T032	1G029B	COMPUTE TO MEMORY-ADDRESS	30
T033	1T026B	COMPUTE TO MEMORY-SELECT	52
T034	1T022A	COMPUTE TO MEMORY-SELECT	52
T035	1T019A	COMPUTE TO MEMORY-SELECT	52
T037	1T070A	REQUEST MEMORY-EXT.MEMORY	49
T038	1T070B	SELECT READ-EXT.MEMORY	49
T039	1T093A	SELECT WRITE-EXT.MEMORY	49
T040	1T093B	SELECT HALF WRITE-EXT.MEMORY	49
T044	1T022B	MASTER CLEAR TO MEMORY	10
T050	1H026A	COMPUTE TO I/O - DATA	35
T051	1I026A	COMPUTE TO I/O - DATA	35
T052	1J026A	COMPUTE TO I/O - DATA	35
T053	1K026A	COMPUTE TO I/O - DATA	35
T054	1L026A	COMPUTE TO I/O - DATA	35
T055	1M026A	COMPUTE TO I/O - DATA	35
T056	1M026B	COMPUTE TO I/O - DATA	36
T057	1L026B	COMPUTE TO I/O - DATA	36
T058	1K026B	COMPUTE TO I/O - DATA	36
T059	1J026B	COMPUTE TO I/O - DATA	36
T060	1I026B	COMPUTE TO I/O - DATA	36
T061	1H026B	COMPUTE TO I/O - DATA	36
T062	1G026A	COMPUTE TO I/O - DATA	36
T063	1T039B	FUNCTION READY - I/O	47
T064	1T038A	SELECT - I/O	14
T067	1T046B	INITIATE BUFFER INPUT	54
T068	1T050A	INITIATE BUFFER OUTPUT	54
T069	1T050B	SET BUFFER BANK	54
T070	1T023A	SET BER	5
T071	1T023B	SET BXR	5
T072	1T024A	BER TO A	47
T073	1T024B	INPUT TO A	47
T074	1T025A	CLEAR BUFFER CONTROL	54
T075	1T025B	MASTER CLEAR - I/O	10
T076	1T026A	MEM. TO MEM. XFER	54
T170	1T089B	COMP. TO COMP. INTERRUPT	4
T720	1H039A	NORMAL DATA	35
T721	1I039A	NORMAL DATA	35
T722	1J039A	NORMAL DATA	35
T723	1K039A	NORMAL DATA	35
T724	1L039A	NORMAL DATA	35
T725	1M039A	NORMAL DATA	35
T726	1M039B	NORMAL DATA	36
T727	1L039B	NORMAL DATA	36
T728	1K039B	NORMAL DATA	36
T729	1J039B	NORMAL DATA	36
T730	1I039B	NORMAL DATA	36
T731	1H039B	NORMAL DATA	36
T732	1T020A	NORMAL DATA	36
T735	1T020B	EXT. FUNCTION-NORMAL	47
T736	1T021A	INPUT REQUEST-NORMAL	47
T737	1T021B	INFO READY-NORMAL	47
T738	1T040A	MASTER CLEAR-NORMAL	10
T740	1H040A	BUFFER DATA	50
T741	1I040A	BUFFER DATA	50
T742	1J040A	BUFFER DATA	50
T743	1K040A	BUFFER DATA	50
T744	1L040A	BUFFER DATA	50
T745	1M040A	BUFFER DATA	50
T746	1M040B	BUFFER DATA	50
T747	1L040B	BUFFER DATA	50
T748	1K040B	BUFFER DATA	50
T749	1J040B	BUFFER DATA	50
T750	1I040B	BUFFER DATA	50
T751	1H040B	BUFFER DATA	50
T752	1T087B	BUFFER DATA	50
T755	1T090A	INPUT REQUEST - BUFFER	47
T756	1T090B	INFO. READY-BUFFER	47
T757	1T087A	EXT. FUNCTION-BUFFER	47
T758	1T040B	MASTER CLEAR-BUFFER	10
T800	1A045A	X DRIVE - ADDRESS XXX_{00} OR XXX_{40}	44
T801	1B045A	X DRIVE - ADDRESS XXX_{01} OR XXX_{41}	44
T802	1A045B	X DRIVE - ADDRESS XXX_{02} OR XXX_{42}	44
T803	1B045B	X DRIVE - ADDRESS XXX_{03} OR XXX_{43}	44
T804	1A044A	X DRIVE - ADDRESS XXX_{04} OR XXX_{44}	44
T805	1B044A	X DRIVE - ADDRESS XXX_{05} OR XXX_{45}	44
T806	1A044B	X DRIVE - ADDRESS XXX_{06} OR XXX_{46}	44
T807	1B044B	X DRIVE - ADDRESS XXX_{07} OR XXX_{47}	44
T808	1A035A	X DRIVE - ADDRESS XXX_{10} OR XXX_{50}	44
T809	1B035A	X DRIVE - ADDRESS XXX_{11} OR XXX_{51}	44
T810	1A035B	X DRIVE - ADDRESS XXX_{12} OR XXX_{52}	44
T811	1B035B	X DRIVE - ADDRESS XXX_{13} OR XXX_{53}	44
T812	1A034A	X DRIVE - ADDRESS XXX_{14} OR XXX_{54}	44
T813	1B034A	X DRIVE - ADDRESS XXX_{15} OR XXX_{55}	44
T814	1A034B	X DRIVE - ADDRESS XXX_{16} OR XXX_{56}	44
T815	1B034B	X DRIVE - ADDRESS XXX_{17} OR XXX_{57}	44
T816	1A043A	X DRIVE - ADDRESS XXX_{20} OR XXX_{60}	44
T817	1B043A	X DRIVE - ADDRESS XXX_{21} OR XXX_{61}	44
T818	1A043B	X DRIVE - ADDRESS XXX_{22} OR XXX_{62}	44
T819	1B043B	X DRIVE - ADDRESS XXX_{23} OR XXX_{63}	44
T820	1A042A	X DRIVE - ADDRESS XXX_{24} OR XXX_{64}	44
T821	1B042A	X DRIVE - ADDRESS XXX_{25} OR XXX_{65}	44
T822	1A042B	X DRIVE - ADDRESS XXX_{26} OR XXX_{66}	44
T823	1B042B	X DRIVE - ADDRESS XXX_{27} OR XXX_{67}	44
T824	1A033A	X DRIVE - ADDRESS XXX_{30} OR XXX_{70}	44
T825	1B033A	X DRIVE - ADDRESS XXX_{31} OR XXX_{71}	44
T826	1A033B	X DRIVE - ADDRESS XXX_{32} OR XXX_{72}	44

T827	1B033B	X DRIVE - ADDRESS XXX33 OR XXX73	44
T828	1A032A	X DRIVE - ADDRESS XXX34 OR XXX74	44
T829	1B032A	X DRIVE - ADDRESS XXX35 OR XXX75	44
T830	1A032B	X DRIVE - ADDRESS XXX36 OR XXX76	44
T831	1B032B	X DRIVE - ADDRESS XXX37 OR XXX77	44
T900	1C038A	Y DRIVE - ADDRESS 000XX OR 040XX	45
T901	1C044A	Y DRIVE - ADDRESS 001XX OR 041XX	45
T902	1C038B	Y DRIVE - ADDRESS 002XX OR 042XX	45
T903	1C044B	Y DRIVE - ADDRESS 003XX OR 043XX	45
T904	1C037A	Y DRIVE - ADDRESS 004XX OR 044XX	45
T905	1C043A	Y DRIVE - ADDRESS 005XX OR 045XX	45
T906	1C037B	Y DRIVE - ADDRESS 006XX OR 046XX	45
T907	1C043B	Y DRIVE - ADDRESS 007XX OR 047XX	45
T908	1C032A	Y DRIVE - ADDRESS 010XX OR 050XX	45
T909	1D045A	Y DRIVE - ADDRESS 011XX OR 051XX	45
T910	1C032B	Y DRIVE - ADDRESS 012XX OR 052XX	45
T911	1D045B	Y DRIVE - ADDRESS 013XX OR 053XX	45
T912	1C031A	Y DRIVE - ADDRESS 014XX OR 054XX	45
T913	1D044A	Y DRIVE - ADDRESS 015XX OR 055XX	45
T914	1C031B	Y DRIVE - ADDRESS 016XX OR 056XX	45
T915	1D044B	Y DRIVE - ADDRESS 017XX OR 057XX	45
T916	1C036A	Y DRIVE - ADDRESS 020XX OR 060XX	45
T917	1C042A	Y DRIVE - ADDRESS 021XX OR 061XX	45
T918	1C036B	Y DRIVE - ADDRESS 022XX OR 062XX	45
T919	1C042B	Y DRIVE - ADDRESS 023XX OR 063XX	45
T920	1C035A	Y DRIVE - ADDRESS 024XX OR 064XX	45
T921	1C041A	Y DRIVE - ADDRESS 025XX OR 065XX	45
T922	1C035B	Y DRIVE - ADDRESS 026XX OR 066XX	45
T923	1C041B	Y DRIVE - ADDRESS 027XX OR 067XX	45
T924	1C030A	Y DRIVE - ADDRESS 030XX OR 070XX	45
T925	1D043A	Y DRIVE - ADDRESS 031XX OR 071XX	45
T926	1C030B	Y DRIVE - ADDRESS 032XX OR 072XX	45
T927	1D043B	Y DRIVE - ADDRESS 033XX OR 073XX	45
T928	1C029A	Y DRIVE - ADDRESS 034XX OR 074XX	45
T929	1D042A	Y DRIVE - ADDRESS 035XX OR 075XX	45
T930	1C029B	Y DRIVE - ADDRESS 036XX OR 076XX	45
T931	1D042B	Y DRIVE - ADDRESS 037XX OR 077XX	45
T964	1D031A	Y DRIVE - ADDRESS 100XX OR 140XX	46
T965	1E044A	Y DRIVE - ADDRESS 101XX OR 141XX	46
T966	1D031B	Y DRIVE - ADDRESS 102XX OR 142XX	46
T967	1E044B	Y DRIVE - ADDRESS 103XX OR 143XX	46
T968	1D030A	Y DRIVE - ADDRESS 104XX OR 144XX	46
T969	1E043A	Y DRIVE - ADDRESS 105XX OR 145XX	46
T970	1D030B	Y DRIVE - ADDRESS 106XX OR 146XX	46
T971	1E043B	Y DRIVE - ADDRESS 107XX OR 147XX	46
T972	1E032A	Y DRIVE - ADDRESS 110XX OR 150XX	46
T973	1E038A	Y DRIVE - ADDRESS 111XX OR 151XX	46
T974	1E032B	Y DRIVE - ADDRESS 112XX OR 152XX	46
T975	1E038B	Y DRIVE - ADDRESS 113XX OR 153XX	46
T976	1E031A	Y DRIVE - ADDRESS 114XX OR 154XX	46
T977	1E037A	Y DRIVE - ADDRESS 115XX OR 155XX	46
T978	1E031B	Y DRIVE - ADDRESS 116XX OR 156XX	46
T979	1E037B	Y DRIVE - ADDRESS 117XX OR 157XX	46
T980	1D029A	Y DRIVE - ADDRESS 120XX OR 160XX	46
T981	1E042A	Y DRIVE - ADDRESS 121XX OR 161XX	46
T982	1D029B	Y DRIVE - ADDRESS 122XX OR 162XX	46
T983	1E042B	Y DRIVE - ADDRESS 123XX OR 163XX	46
T984	1D028A	Y DRIVE - ADDRESS 124XX OR 164XX	46
T985	1E041A	Y DRIVE - ADDRESS 125XX OR 165XX	46
T986	1D028B	Y DRIVE - ADDRESS 126XX OR 166XX	46
T987	1E041B	Y DRIVE - ADDRESS 127XX OR 167XX	46
T988	1E030A	Y DRIVE - ADDRESS 130XX OR 170XX	46
T989	1E036A	Y DRIVE - ADDRESS 131XX OR 171XX	46
T990	1E030B	Y DRIVE - ADDRESS 132XX OR 172XX	46
T991	1E036B	Y DRIVE - ADDRESS 133XX OR 173XX	46
T992	1E029A	Y DRIVE - ADDRESS 134XX OR 174XX	46
T993	1E035A	Y DRIVE - ADDRESS 135XX OR 175XX	46
T994	1E029B	Y DRIVE - ADDRESS 136XX OR 176XX	46
T995	1E035B	Y DRIVE - ADDRESS 137XX OR 177XX	46
U001	1H061A	U INVERTERS	38
U011	1I061A	U INVERTERS	38
U021	1J061A	U INVERTERS	38
U031	1K061A	U INVERTERS	38
U041	1L061A	U INVERTERS	38
U051	1M061A	U INVERTERS	38
U061	1M060A	U INVERTERS	38
U071	1L060A	U INVERTERS	38
U081	1K060A	U INVERTERS	38
U091	1J060A	U INVERTERS	38
U101	1I060A	U INVERTERS	38
U111	1H060A	U INVERTERS	38
U121	1G060A	U INVERTERS	38
V000	10092A	TIME ZERO	3
V001	10092B	TIME ONE	3
V002	1T044A	TIME TWO	3
V004	10086B	TIME FOUR	3
V005	1G074B	TIME FIVE	3
V006	10057A	TIME SIX	3
V007	10057B	TIME SEVEN	3
V008	10052A	TIME EIGHT	4
V009	1P018A	TIME NINE	4
V010	1P017A	TIME TEN	4
V011	1N015A	TIME ELEVEN	4
V012	1N012A	TIME TWELVE	4
V013	1J016A	TIME THIRTEEN	4
V014	1H015A	TIME FOURTEEN	5
V015	1G019A	TIME FIFTEEN	5
V016	1G018A	TIME SIXTEEN	5
V017	1F020A	TIME SEVENTEEN	5
V018	1F018A	TIME EIGHTEEN	5
V019	1F017B	TIME NINETEEN	5
V030	1L022A	START LOGIC	12
V050	1E075A	MULTIPLY + DIVIDE + SHIFT	6
V051	1E077A	MULTIPLY + DIVIDE + SHIFT	6
V052	1E079A	MULTIPLY + DIVIDE + SHIFT	6
V053	1E079B	MULTIPLY + DIVIDE + SHIFT	6
V054	1E082A	MULTIPLY + DIVIDE + SHIFT	6
V055	1E082B	MULTIPLY + DIVIDE + SHIFT	6
V070	1D018B	INTERRUPT TIMING CHAIN	53
V071	1C016B	INTERRUPT TIMING CHAIN	53
V072	1C016A	INTERRUPT TIMING CHAIN	53
V073	1D018A	INTERRUPT TIMING CHAIN	53
V074	1C015B	INTERRUPT TIMING CHAIN	53
V075	1D015A	INTERRUPT TIMING CHAIN	53
V081	1L020A	START LOGIC RESYNC	12
V091	1C093A	INT. BUFFER RESYNC	48
V101	1T045A	MAIN TIMING - TIME ONE	3
V102	1T044B	MAIN TIMING - TIME TWO	3
V104	10079A	MAIN TIMING - TIME FOUR	3
V105	10071A	MAIN TIMING - TIME FIVE	3
V106	1H077B	MAIN TIMING - TIME SIX	3
V108	10052B	MAIN TIMING - TIME EIGHT	4
V109	1P018B	MAIN TIMING - TIME NINE	4
V110	10016A	MAIN TIMING - TIME TEN	4

V111	1N015B	MAIN TIMING - TIME ELEVEN	4
V112	1M013A	MAIN TIMING - TIME TWELVE	4
V113	1J016B	MAIN TIMING - TIME THIRTEEN	4
V114	1H015B	MAIN TIMING - TIME FOURTEEN	5
V115	1G019B	MAIN TIMING - TIME FIFTEEN	5
V116	1G016A	MAIN TIMING - TIME SIXTEEN	5
V117	1H014B	MAIN TIMING - TIME SEVENTEEN	5
V118	1F018B	MAIN TIMING - TIME EIGHTEEN	5
V119	1P003A	MAIN TIMING - TIME NINETEEN	5
V121	1P066A	RESUME ONE RESYNC	49
V131	1C092A	NORMAL RESYNC	47
V141	1P069A	RESUME TWO RESYNC	49
V150	1F075B	MULT. + DIV. + SHIFT	6
V151	1F077B	MULT. + DIV. + SHIFT	6
V170	1A001A	INTERRUPT TIMING CHAIN	53
V174	1C015A	INTERRUPT TIMING CHAIN	53
V201	10091B	MAIN TIMING - TIME ONE	3
V202	10086A	MAIN TIMING - TIME TWO	3
V204	10079B	MAIN TIMING - TIME FOUR	3
V208	10051A	MAIN TIMING - TIME EIGHT	4
V209	1P017B	MAIN TIMING - TIME NINE	4
V210	10016B	MAIN TIMING - TIME TEN	4
V211	1N014A	MAIN TIMING - TIME ELEVEN	4
V212	1M013B	MAIN TIMING - TIME TWELVE	4
V213	1J015A	MAIN TIMING - TIME THIRTEEN	4
V214	1H014A	MAIN TIMING - TIME FOURTEEN	5
V215	1G018B	MAIN TIMING - TIME FIFTEEN	5
V218	1F017A	MAIN TIMING - TIME EIGHTEEN	5
V270	1C021A	INTERRUPT TIMING CHAIN	53
V274	1A001B	INTERRUPT TIMING CHAIN	53
V302	1L022B	MAIN TIMING - TIME TWO	3
V304	10078A	MAIN TIMING - TIME FOUR	3
V305	10071B	MAIN TIMING - TIME FIVE	3
V308	10051B	MAIN TIMING - TIME EIGHT	4
V310	10015A	MAIN TIMING - TIME TEN	4
V311	1N014B	MAIN TIMING - TIME ELEVEN	4
V312	1M012A	MAIN TIMING - TIME TWELVE	4
V313	1J015B	MAIN TIMING - TIME THIRTEEN	4
V314	1J014B	MAIN TIMING-TIME FOURTEEN	5
V370	1C021B	INTERRUPT TIMING CHAIN	53
V404	10078B	MAIN TIMING - TIME FOUR	3
V410	10015B	MAIN TIMING - TIME TEN	4
V411	1N013A	MAIN TIMING - TIME ELEVEN	4
V412	1M012B	MAIN TIMING - TIME TWELVE	4
V504	10091A	MAIN TIMING-TIME FOUR.RNI	3
V510	10014A	MAIN TIMING - TIME TEN	4
V511	1N013B	MAIN TIMING - TIME ELEVEN	4
V512	1N012B	MAIN TIMING - TIME TWELVE	4
V610	10014B	MAIN TIMING - TIME TEN	4
V611	1J014A	MAIN TIMING - TIME ELEVEN	4
V613	1J013A	MAIN TIMING - TIME THIRTEEN	4
V614	1H013A	MAIN TIMING - TIME FOURTEEN	5
V902	1M050B	TIME TWO OR TIME TWELVE	3
V908	1P049A	CLEAR BANK SELECT	9
W140	1N093A	MASTER CLEAR	10
W141	1G042B	MASTER CLEAR	10
W142	1A003B	MASTER CLEAR	10
W143	1N094B	MASTER CLEAR	10
W144	1D008B	MASTER CLEAR	10
W145	1N094A	MASTER CLEAR	10
W146	1D093A	MASTER CLEAR	10
W147	1M094A	M.C AND NOT INPUT DISCONNECT	10
W148	1H054B	MASTER CLEAR	10
W150	1M032B	CLEAR P	10
W151	1L032B	CLEAR P	10
W152	1M063B	CLEAR Q	10
W153	1L063B	CLEAR Q	10
W160	1H038B	SET BR	9
W161	1I044B	SET BR	9
W162	1J044B	SET BR	9
W163	1K044B	SET BR	9
W165	1G037B	SET BD	9
W166	1I043B	SET BD	9
W167	1J043B	SET BD	9
W168	1K043B	SET BD	9
W170	1H036B	SET BI	9
W171	1I038B	SET BI	9
W172	1J038B	SET BI	9
W173	1K038B	SET BI	9
W175	1H035B	SET B. BANK	9
W176	1I037B	SET B. BANK	9
W177	1J037B	SET B. BANK	9
W178	1K037B	SET B. BANK	9
W202	1J041A	A=0 TRANSLATION	31
W204	1K042A	A=0 TRANSLATION	31
W206	1K041A	A=0 TRANSLATION	31
W208	1H041A	A=0 TRANSLATION	31
W210	1C013B	NOT M.C - INTERRUPT	53
W215	1G042A	BOOTSTRAP TRANSLATION	37
W216	1I036B	BOOTSTRAP TRANSLATION	37
W217	1J036B	BOOTSTRAP TRANSLATION	37
W218	1K036B	BOOTSTRAP TRANSLATION	37
W219	1L036B	BOOTSTRAP TRANSLATION	37
W220	1M038B	BOOTSTRAP TRANSLATION	37
W221	1M042A	BOOTSTRAP TRANSLATION	37
W222	1L041A	BOOTSTRAP TRANSLATION	37
W223	1M041A	BOOTSTRAP TRANSLATION	37
W224	1N063A	BOOTSTRAP TRANSLATION	37
W225	1N061A	BOOTSTRAP TRANSLATION	37
W226	1L023A	BOOTSTRAP TRANSLATION	37
W227	1H043B	PARITY ERROR INVERTER	55
W228	1B017B	POWER FAILURE INVERTER-I/O UNIT-NORMAL 1	54
W800	1F022A	S TO S PRIME	41
W801	1F022B	S TO S PRIME	41
W802	1D070A	CLEAR Z	41
W803	1D070B	CLEAR Z	41
W808	1D063A	GATE BANK 0 SENSE AMPS.	41
W809	1D063B	GATE BANK 0 SENSE AMPS.	41
W810	1E063A	GATE BANK 1 SENSE AMPS.	41
W811	1E063B	GATE BANK 1 SENSE AMPS.	41
X000	1H067A	X REGISTER	35
X001	1H066A	X REGISTER	35
X003	1H063A	X INVERTER	37
X010	1I067A	X REGISTER	35
X011	1I066A	X REGISTER	35
X013	1I063A	X INVERTER	37
X020	1J067A	X REGISTER	35
X021	1J066A	X REGISTER	35
X023	1J063A	X INVERTER	37
X030	1K067A	X REGISTER	35
X031	1K066A	X REGISTER	35
X033	1K063A	X INVERTER	37
X040	1L067A	X REGISTER	35
X041	1L066A	X REGISTER	35

X043	1L063A	X INVERTER	37
X050	1M067A	X REGISTER	35
X051	1M066A	X REGISTER	35
X053	1M063A	X INVERTER	37
X060	1M065A	X REGISTER	36
X061	1M064A	X REGISTER	36
X063	1M062A	X INVERTER	37
X070	1L065A	X REGISTER	36
X071	1L064A	X REGISTER	36
X073	1L062A	X INVERTER	37
X080	1K065A	X REGISTER	36
X081	1K064A	X REGISTER	36
X083	1K062A	X INVERTER	37
X090	1J065A	X REGISTER	36
X091	1J064A	X REGISTER	36
X093	1J062A	X INVERTER	37
X100	1I065A	X REGISTER	36
X101	1I064A	X REGISTER	36
X103	1I062A	X INVERTER	37
X110	1H065A	X REGISTER	36
X111	1H064A	X REGISTER	36
X113	1H062A	X INVERTER	37
X120	1G065A	X REGISTER	36
X121	1G064A	X REGISTER	36
X122	1G064B	X REGISTER INVERTER-BIT 12	36
X123	1G062A	X INVERTER	37
X125	1G069B	X REGISTER INVERTER-BIT 12	36
Y000	1D049A	SENSE AMPS. - BANK 0	42
Y001	1E062A	SENSE AMPS. - BANK 1	42
Y010	1D056A	SENSE AMPS. - BANK 0	42
Y011	1E055A	SENSE AMPS. - BANK 1	42
Y020	1D050A	SENSE AMPS. - BANK 0	42
Y021	1E061A	SENSE AMPS. - BANK 1	42
Y030	1D057A	SENSE AMPS. - BANK 0	42
Y031	1E054A	SENSE AMPS. - BANK 1	42
Y040	1D051A	SENSE AMPS. - BANK 0	42
Y041	1E060A	SENSE AMPS. - BANK 1	42
Y050	1D058A	SENSE AMPS. - BANK 0	42
Y051	1E053A	SENSE AMPS. - BANK 1	42
Y060	1D052A	SENSE AMPS. - BANK 0	42
Y061	1E059A	SENSE AMPS. - BANK 1	42
Y070	1D059A	SENSE AMPS. - BANK 0	42
Y071	1E052A	SENSE AMPS. - BANK 1	42
Y080	1D053A	SENSE AMPS. - BANK 0	42
Y081	1E058A	SENSE AMPS. - BANK 1	42
Y090	1D060A	SENSE AMPS. - BANK 0	42
Y091	1E051A	SENSE AMPS. - BANK 1	42
Y100	1D054A	SENSE AMPS. - BANK 0	42
Y101	1E057A	SENSE AMPS. - BANK 1	42
Y110	1D061A	SENSE AMPS. - BANK 0	42
Y111	1E050A	SENSE AMPS. - BANK 1	42
Y120	1D055A	SENSE AMPS. - BANK 0	42
Y121	1E056A	SENSE AMPS. - BANK 1	42
Y130	1D062A	SENSE AMP - BANK 0 - PARITY	42
Y131	1E049A	SENSE AMP - BANK 1 - PARITY	42
Z000	1C070A	Z REGISTER	42
Z001	1C070B	Z REGISTER	42
Z010	1C069A	Z REGISTER	42
Z011	1C069B	Z REGISTER	42
Z020	1C068A	Z REGISTER	42
Z021	1C068B	Z REGISTER	42
Z030	1C067A	Z REGISTER	42
Z031	1C067B	Z REGISTER	42
Z040	1C066A	Z REGISTER	42
Z041	1C066B	Z REGISTER	42
Z050	1C065A	Z REGISTER	42
Z051	1C065B	Z REGISTER	42
Z060	1C064A	Z REGISTER	42
Z061	1C064B	Z REGISTER	42
Z070	1C063A	Z REGISTER	42
Z071	1C063B	Z REGISTER	42
Z080	1C062A	Z REGISTER	42
Z081	1C062B	Z REGISTER	42
Z090	1C061A	Z REGISTER	42
Z091	1C061B	Z REGISTER	42
Z100	1C060A	Z REGISTER	42
Z101	1C060B	Z REGISTER	42
Z110	1C059A	Z REGISTER	42
Z111	1C059B	Z REGISTER	42
Z120	1C058A	Z REGISTER	42
Z121	1C058B	Z REGISTER	42
Z130	1C057A	Z REGISTER	42
Z131	1C057B	Z REGISTER	42

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB19692	11-13-68	
B		SEE ECO CB 19674	12-10-68	
C		SEE ECO CB19783	6-23-69	
D		SEE ECO CB19782	9-9-69	
E		SEE ECO CB19972	3-10-70	

NOTES:

1. INTERPRET TO ENGINEERING STANDARD 3.01.002 "PREPARATION OF LOGIC DIAGRAMS."

2. CONNECTOR NUMBERS SHOWN ARE INTERPRETED IN THE FOLLOWING MANNER:

A. J101 C03 — CONNECTOR NO. J101, PIN NO. C03

B. J103 N — CONNECTOR NO. J103, PIN NO. N

3. THE FOLLOWING IS A LIST OF THE SUBTITLES AND THE SHEET NO'S OF EACH:

SUBTITLE	SHEET NO.
STATUS SHEET	1
BLOCK DIAGRAM	2
MAIN TIMING	3
MAIN TIMING	4
MAIN TIMING	5
MDS TIMING	6
REGISTER DISPLAY	7
REGISTER DISPLAY	8
SELECT/SET BANK CONTROL LOGIC	9
MANUAL CONTROL	10
CYCLE CONTROL	11
START & STOP LOGIC	12
BREAKPOINT LOGIC	13
F & F' REGISTER	14
F REGISTER	15
F TRANSLATION	16
F TRANSLATION	17
F TRANSLATION	18
F TRANSLATION	19
GATES 1-7	20
GATES 8-12	21
GATES 13-18	22
GATES 19-28	23
GATES 29-38	24
GATES 39-49	25
GATES 50-58	26
GATES 59-65	27
GATES 66-67	28
P REGISTER	29
S REGISTER	30
A REGISTER	31
A' REGISTER	32
Q REGISTER	33
Q' REGISTER	34
X REGISTER	35
X REGISTER	36
X INVERTERS	37
I & U INVERTERS	38
BORROW PYRAMID	39
MEMORY CYCLE	40
S' REGISTER & MEMORY CONTROL LOGIC	41
Z REGISTER	42
PARITY	43
X DRIVE	44
Y DRIVE	45
Y DRIVE	46
I/O CONTROL	47
BUFFER CONTROL	48
EXTERNAL MEMORY CONTROL	49
BFR REGISTER	50
BER, BXR & COMPARATOR	51
BANK CONTROL	52
INTERRUPT SEQUENCE	53
INTERRUPT LOGIC	54
ERROR REGISTER	55
MASTER CLOCK	56

4. LOGIC DIAGRAMS CORRESPOND TO REVISION F OF DOCUMENT NUMBER 16901300 (COMPUTE UNIT MECHANIZED DESIGN DATA).

—	—	—	—	—	—	—	—
—	—	—	—	C	C	D	—
—	—	—	—	C	C	—	—
—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—
SH49	SH50	SH51	SH52	SH53	SH54	SH55	SH56

REVISION STATUS OF SHEETS

—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A	A	—	—	B	B	—	—	C
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A	A	—	—	B	B	—	—	C
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A	A	—	—	B	B	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	A	A	—	—	—	—	—	—	—
SH25	SH26	SH27	SH28	SH29	SH30	SH31	SH32	SH33	SH34	SH35	SH36	SH37	SH38	SH39	SH40	SH41	SH42	SH43	SH44	SH45	SH46	SH47	SH48

REVISION STATUS OF SHEETS

E	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	E	—	—	—	—	—	—
D	—	C	C	D	—	—	—	—	C	—	—	—	—	—	—	—	—	—	—	—	—	—	—
C	—	C	C	C	—	—	—	—	C	—	—	—	—	—	—	—	—	—	—	—	—	—	—
B	—	—	—	—	—	—	—	—	A	—	—	—	—	—	—	—	—	—	—	—	—	—	—
A	—	—	—	—	—	—	—	—	A	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SH1	SH2	SH3	SH4	SH5	SH6	SH7	SH8	SH9	SH10	SH11	SH12	SH13	SH14	SH15	SH16	SH17	SH18	SH19	SH20	SH21	SH22	SH23	SH24

REVISION STATUS OF SHEETS

NEXT ASSY.	USED ON		
APPLICATION			

UNLESS OTHERWISE SPECIFIED TOLERANCES ON FRACTIONS: ± — DECIMALS: ± — ANGLES: ± —

DO NOT SCALE DRAWING

MATERIAL

CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA

CONTRACT		
APPROVED		5-4-67
ENGINEER		5-4-67
CHECKED		4-24-67
DRAWN		2-20-67
APPROVED		
APPROVED		

TITLE

COMPUTE UNIT

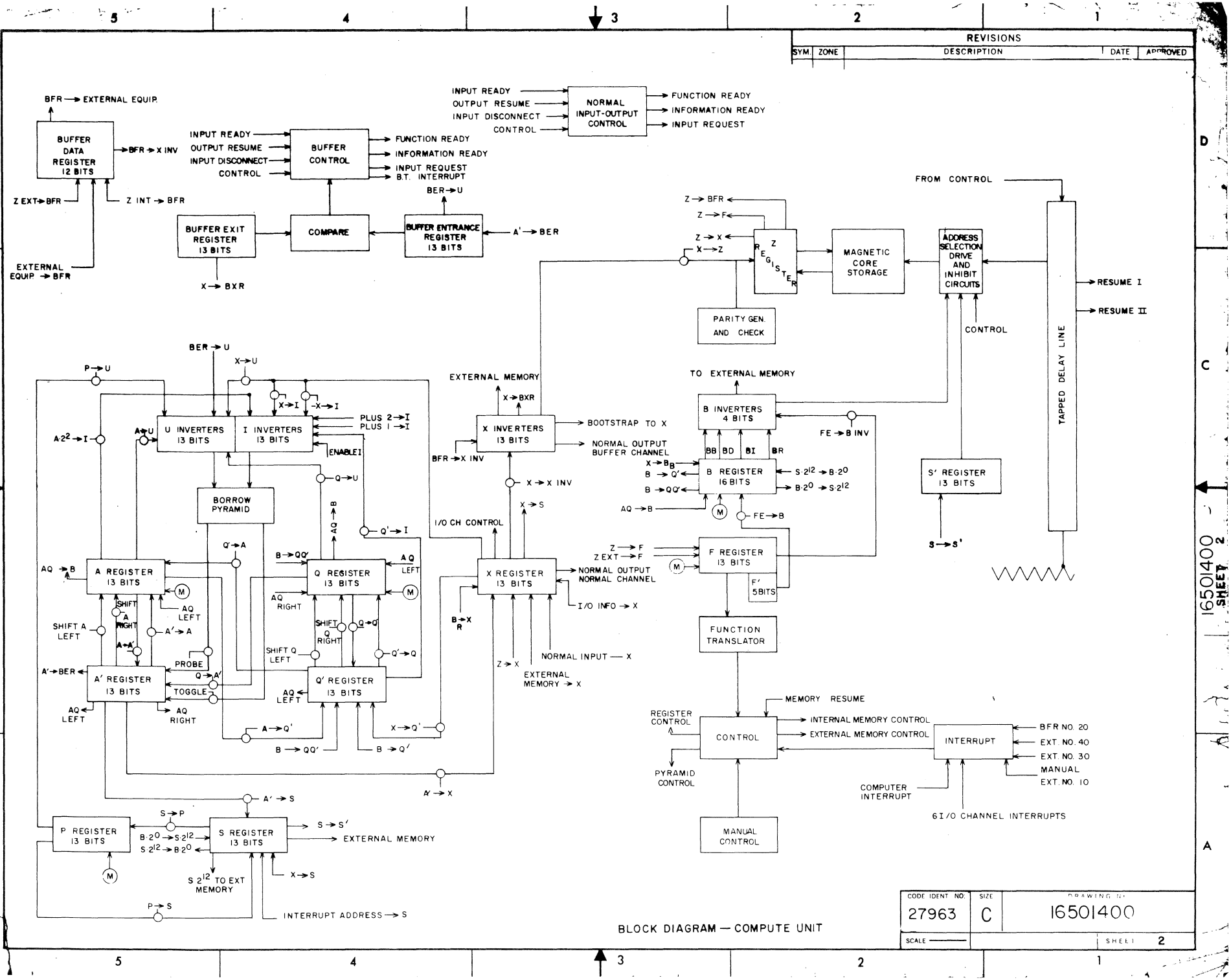
LOGIC DIAGRAM

SIZE	CODE IDENT. NO.	DRAWING NO.
C	27963	16501400

SCALE — SHEET 1 OF 56

16501400 SHEET 1 OF 56

AC 7491 A

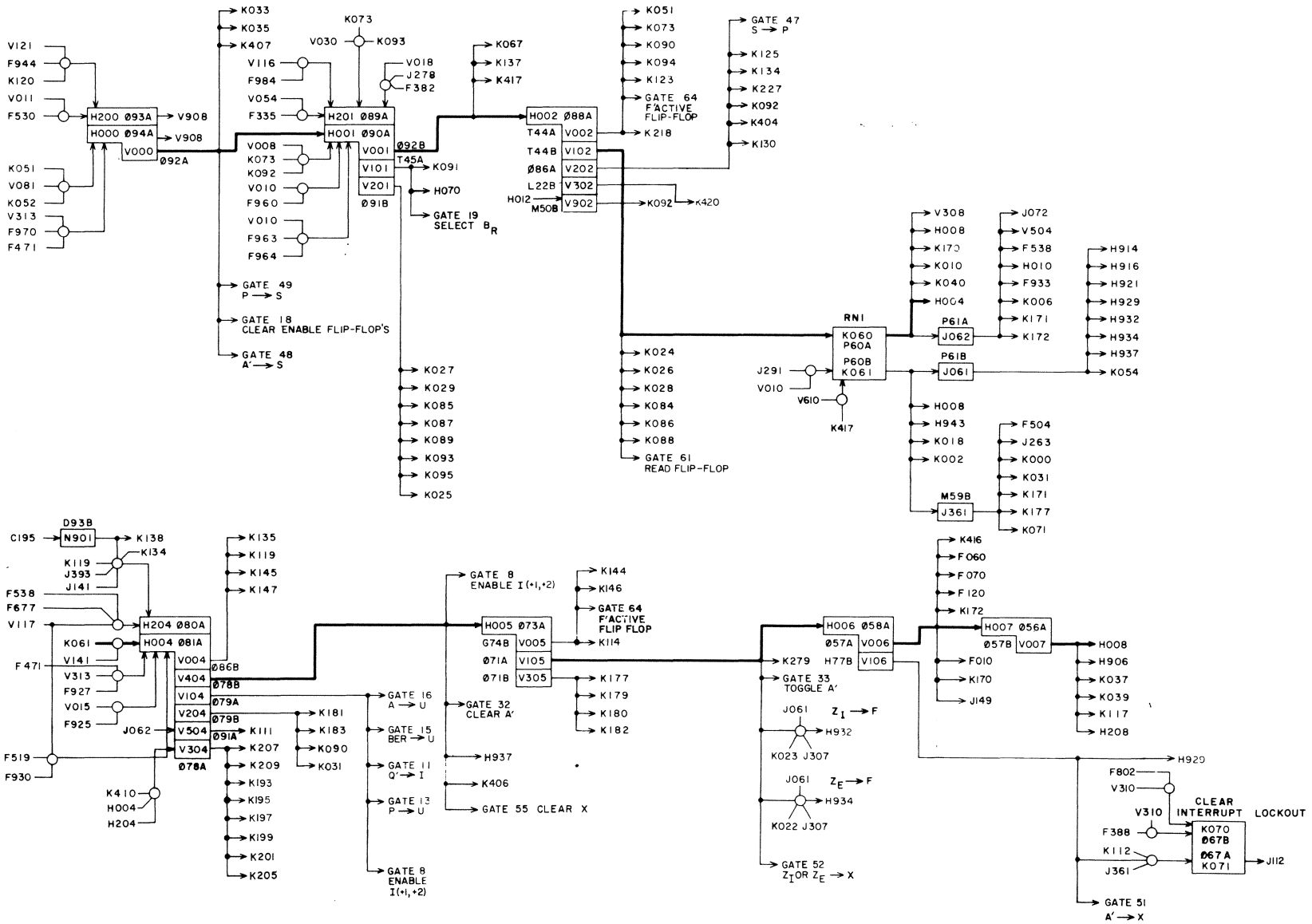


BLOCK DIAGRAM — COMPUTE UNIT

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 2

16501400 SHEET 2

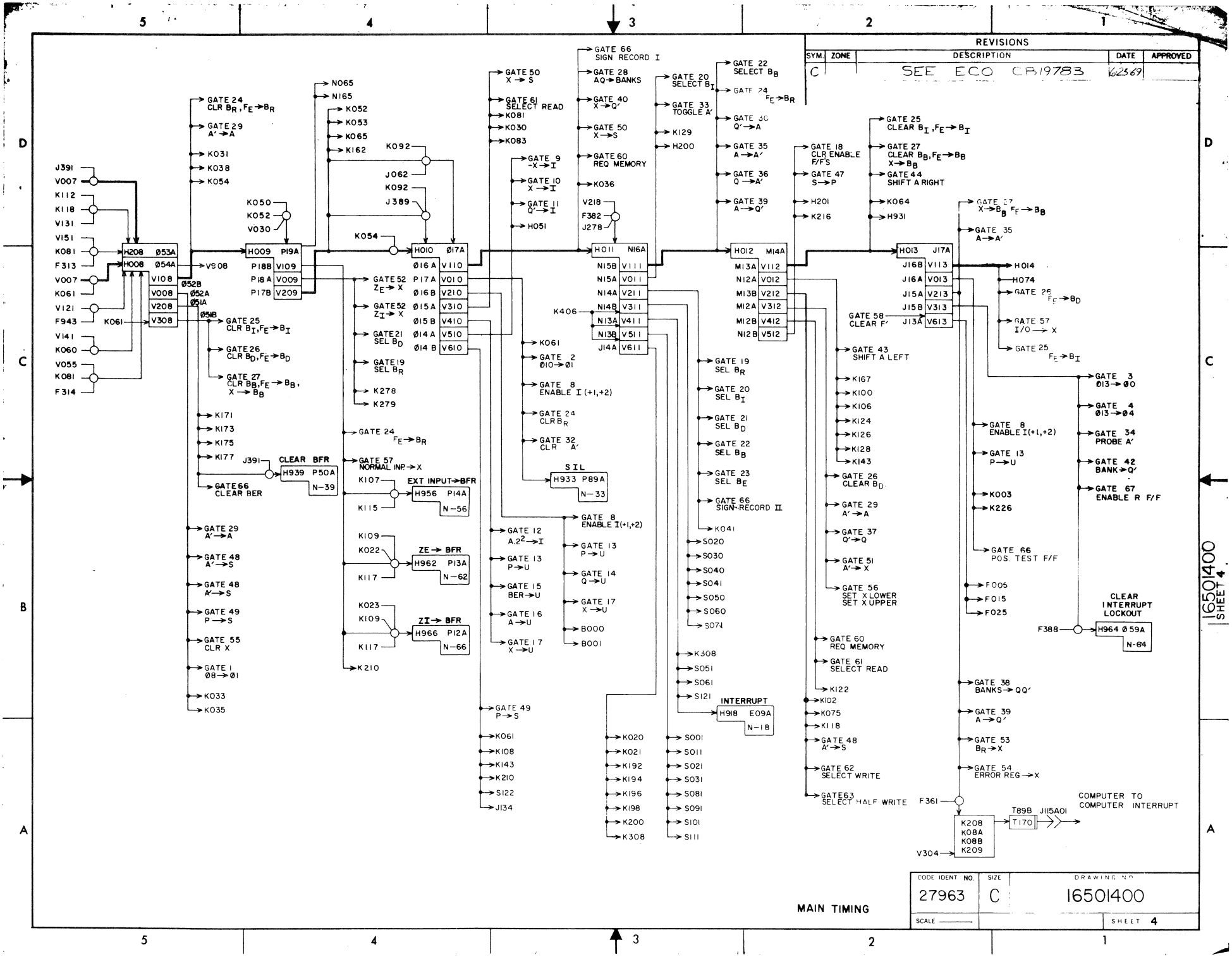
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
C		SEE ECO CB19783	6-23-69	



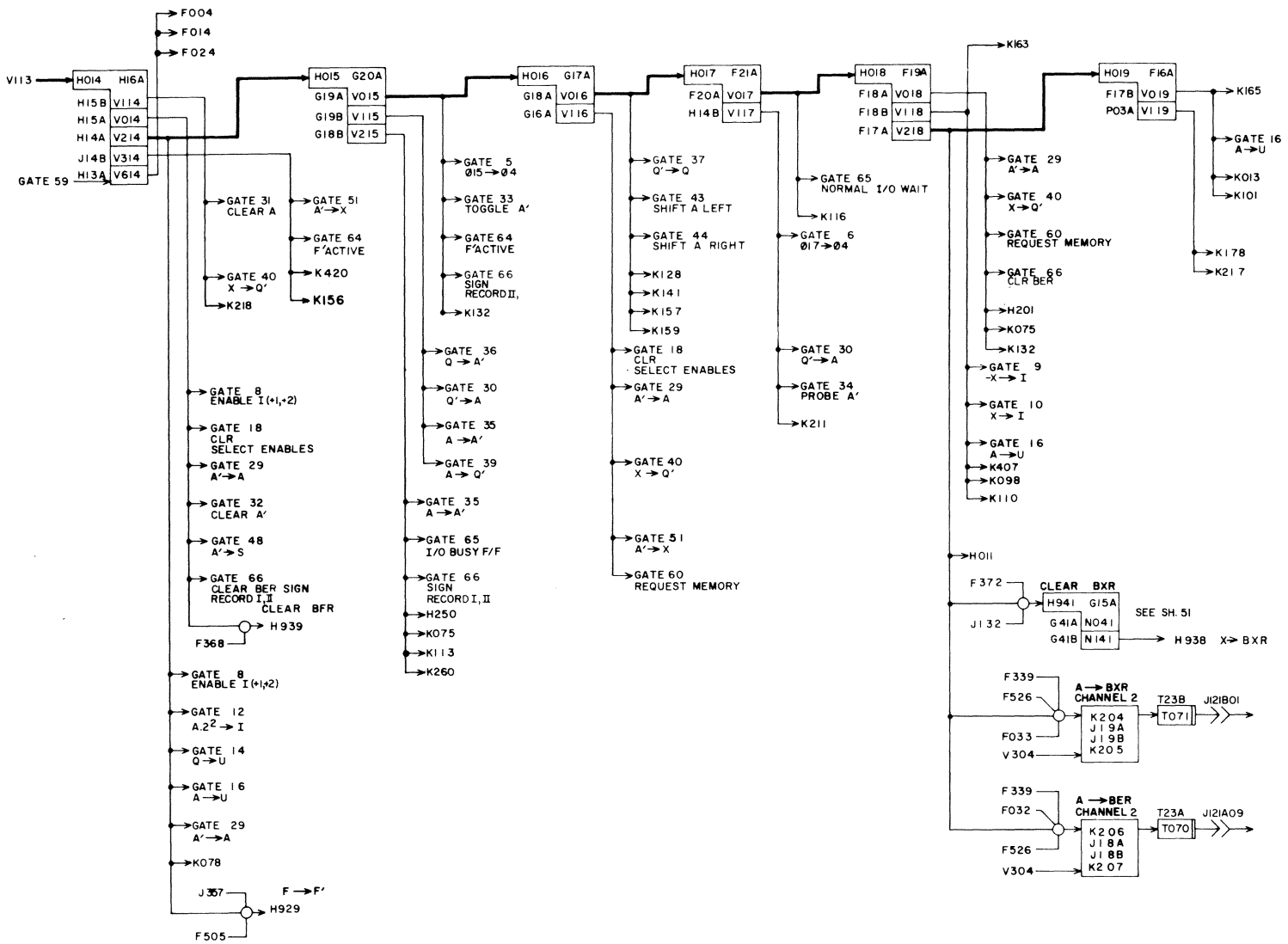
MAIN TIMING

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 3

16501400
SHEET 3


REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
C SEE ECO CB19783 623569
MAIN TIMING
CODE IDENT NO. 27963
SIZE C
DRAWING NO. 16501400
SCALE
SHEET 4
16501400 SHEET 4

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
C		SEE ECO CB 19783	6-24-69	
D		SEE ECO CB 19782	9-4-69	

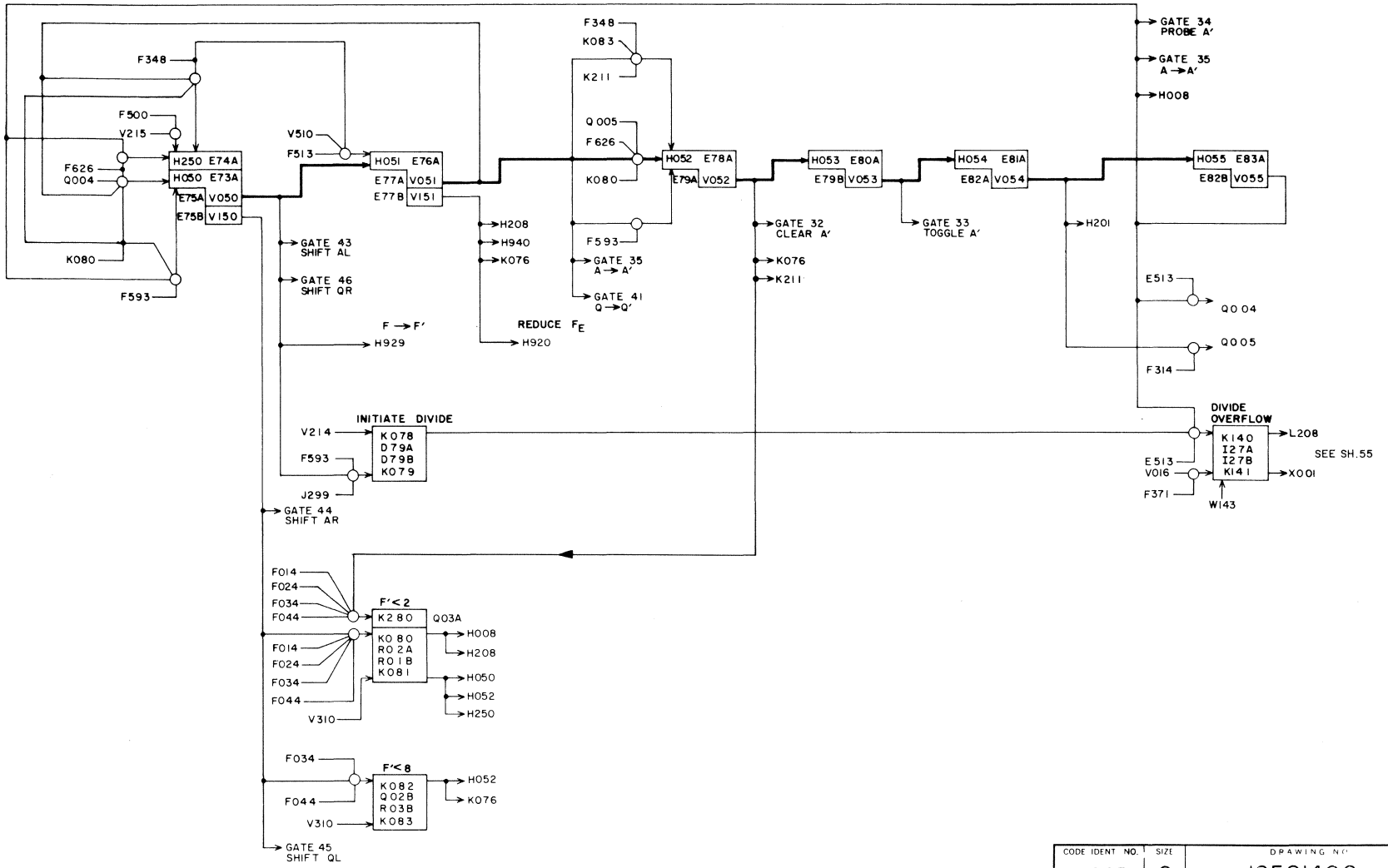


MAIN TIMING

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 5

16501400 SHEET 5

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

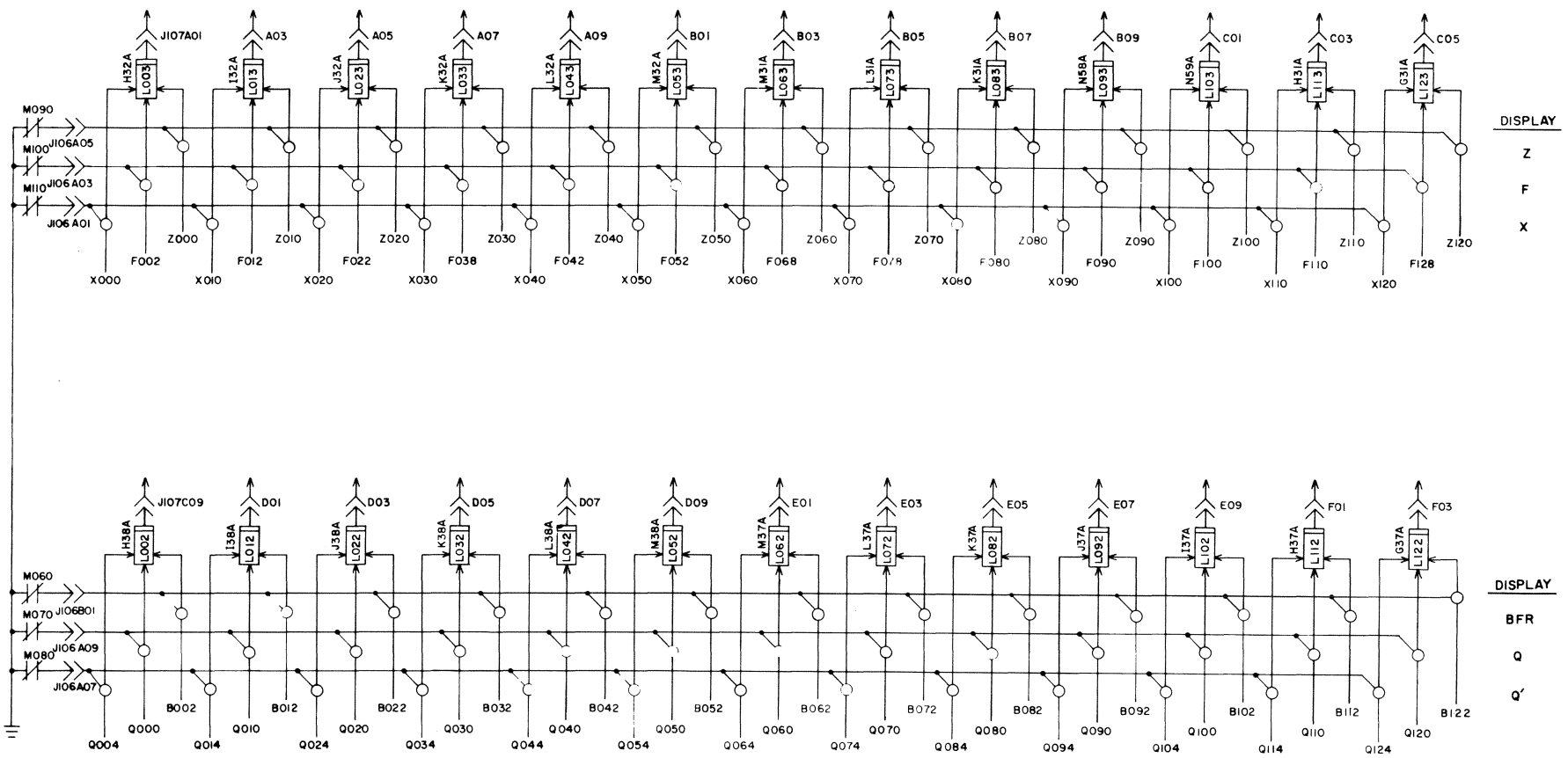


MDS TIMING

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE ——		SHEET 6

16501400
SHEET 6

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

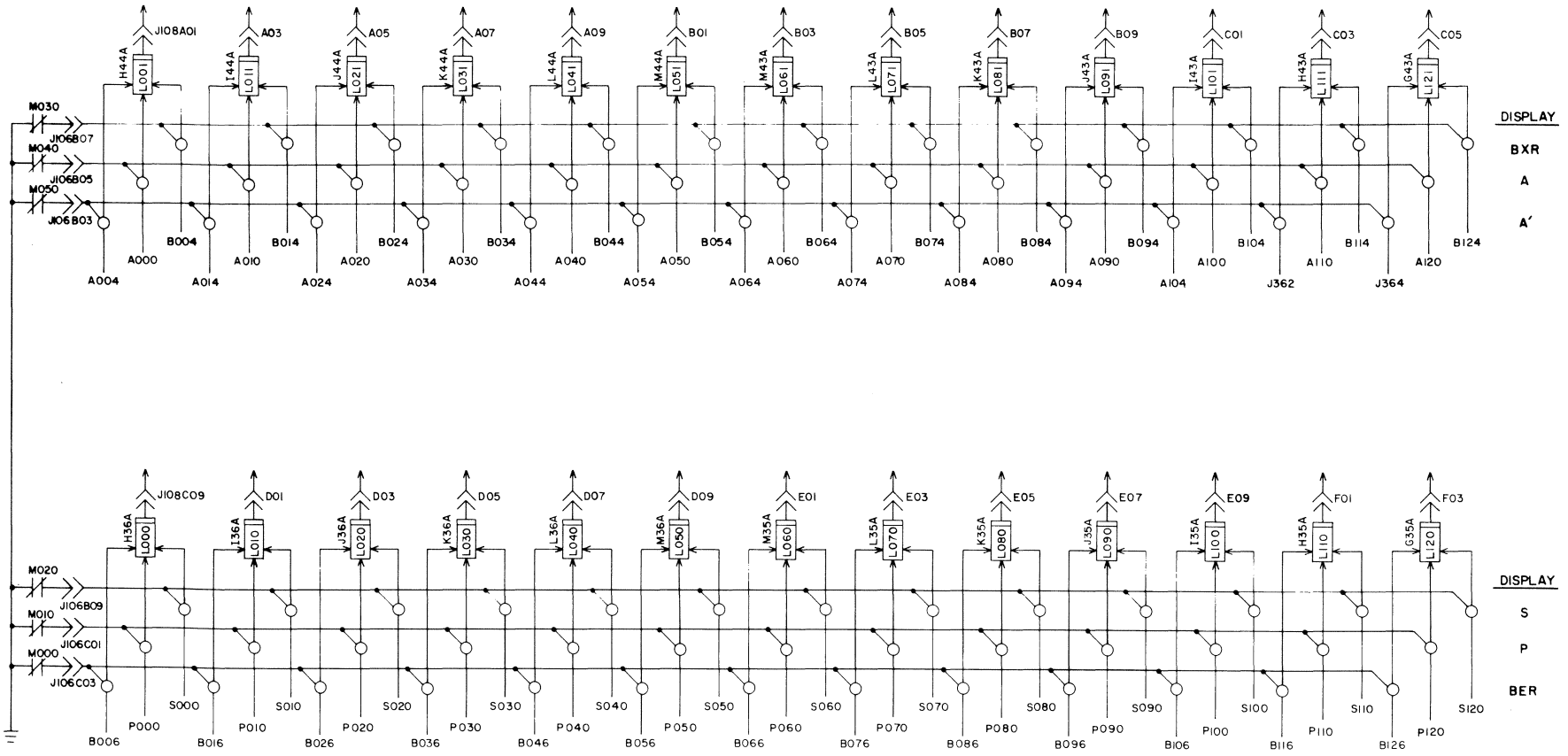


REGISTER DISPLAY

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 7

16501400 SHEET 7

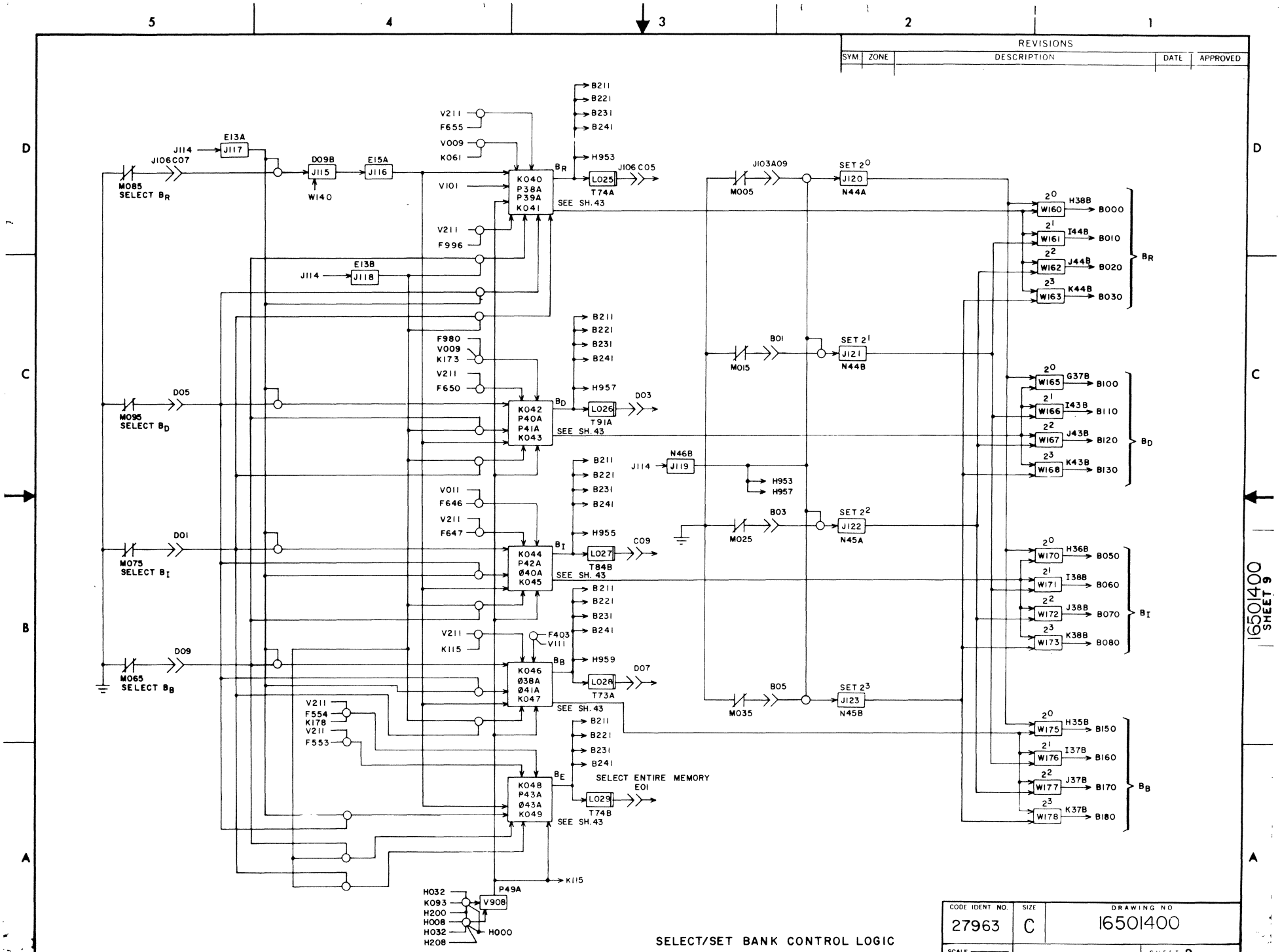
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



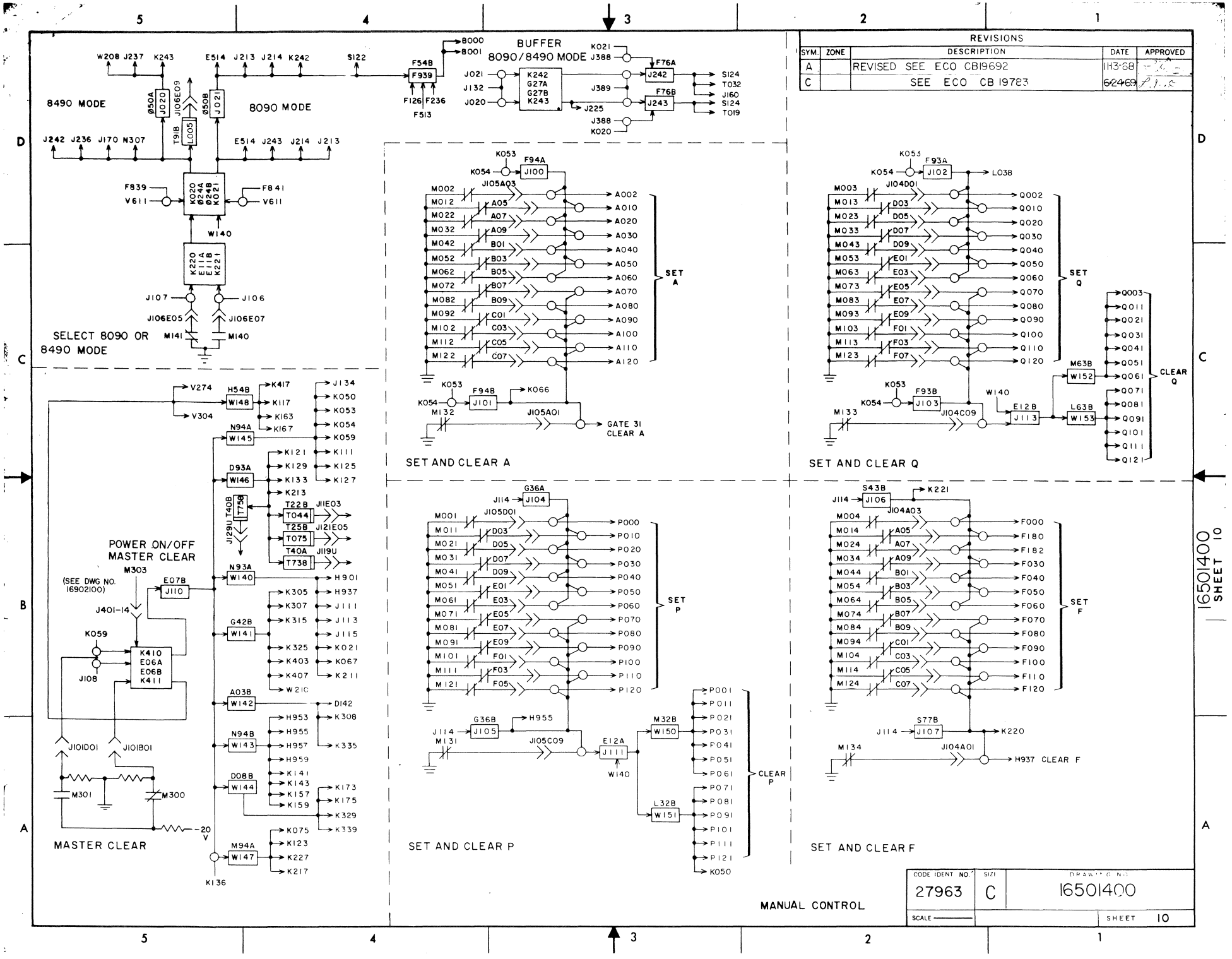
REGISTER DISPLAY

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE ——		SHEET 8

16501400
SHEET 8

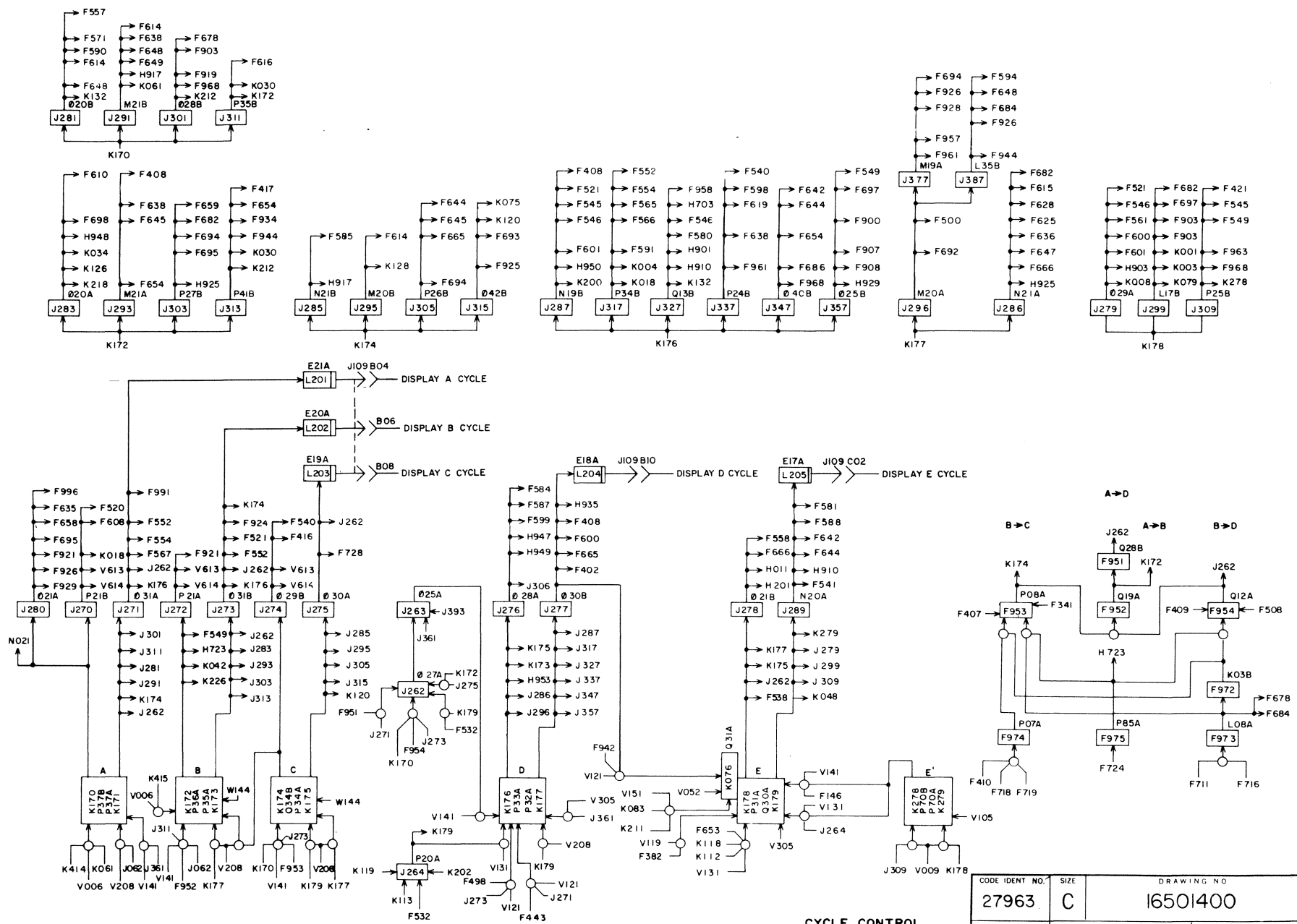

REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
SELECT/SET BANK CONTROL LOGIC
CODE IDENT NO. 27963
SIZE C
DRAWING NO 16501400
SCALE
SHEET 9
16501400 SHEET 9
SELECT ENTIRE MEMORY E01
SEE SH. 43

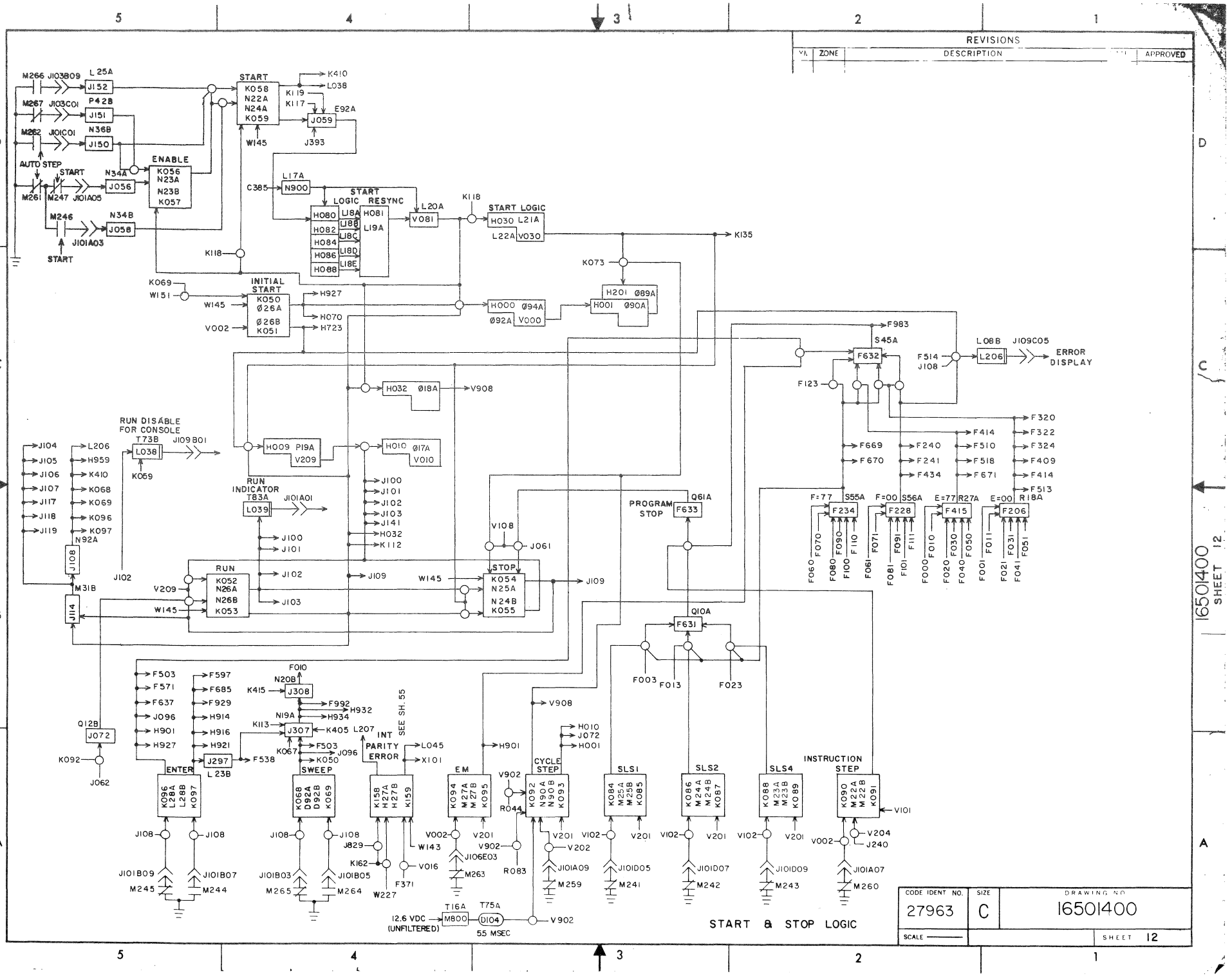
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB19692	11-3-68	
C		SEE ECO CB 19783	6-24-69	



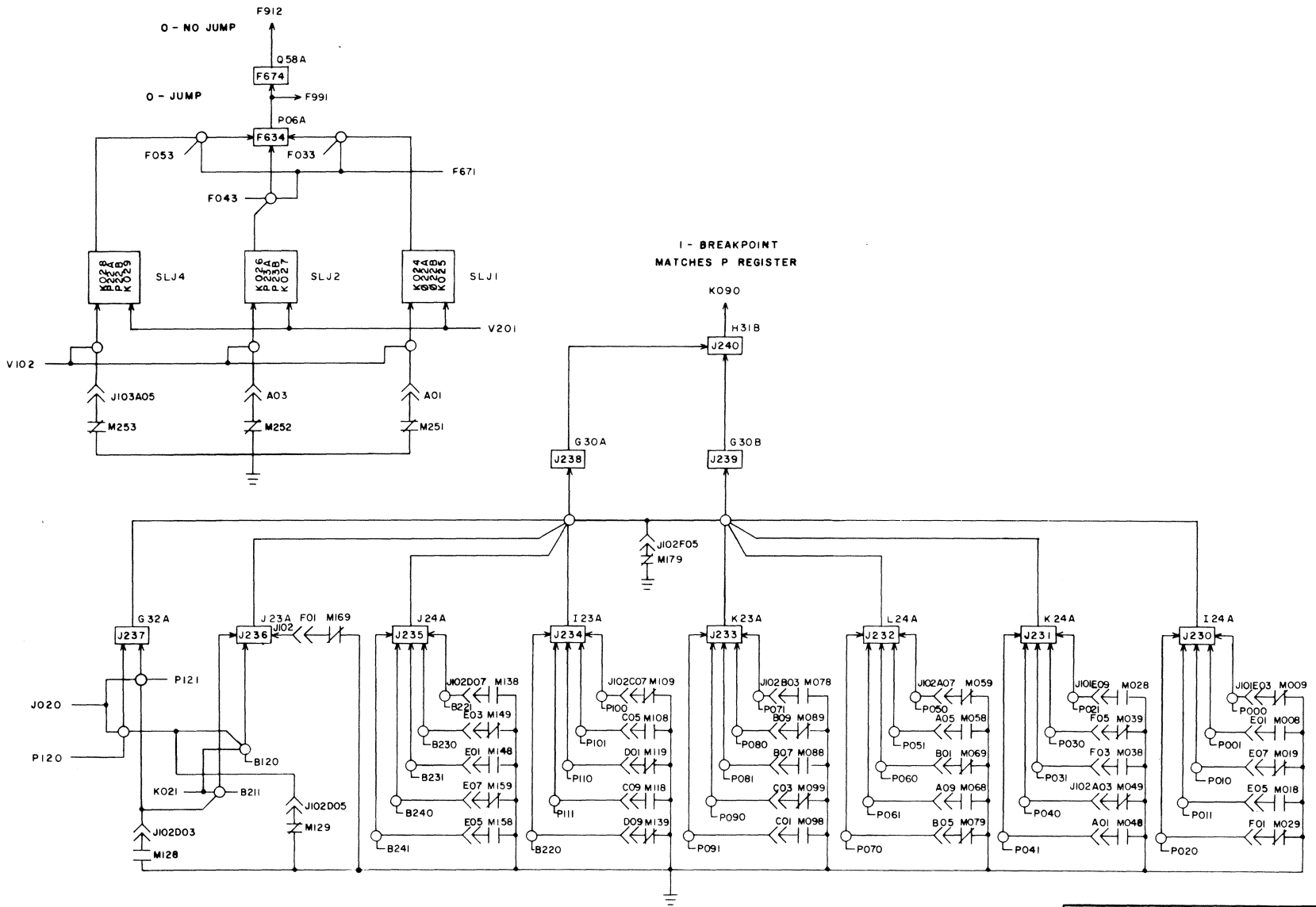
CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 10

16501400 SHEET 10


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
DISPLAY A CYCLE
DISPLAY B CYCLE
DISPLAY C CYCLE
DISPLAY D CYCLE
DISPLAY E CYCLE
CYCLE CONTROL
CODE IDENT NO. 27963
SIZE C
DRAWING NO 16501400
SCALE
SHEET 11
16501400 SHEET 11


REVISIONS
VR | ZONE | DESCRIPTION | APPROVED
START
ENABLE
AUTO STEP
START LOGIC RESYNC
START LOGIC
INITIAL START
RUN DISABLE FOR CONSOLE
RUN INDICATOR
RUN
STOP
PROGRAM STOP
ERROR DISPLAY
ENTER
SWEEP
INT PARITY ERROR
EM
CYCLE STEP
SLS1
SLS2
SLS4
INSTRUCTION STEP
12.6 VDC (UNFILTERED)
55 MSEC
START & STOP LOGIC
CODE IDENT NO. 27963
SIZE C
DRAWING NO 16501400
SCALE
SHEET 12
16501400 SHEET 12

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

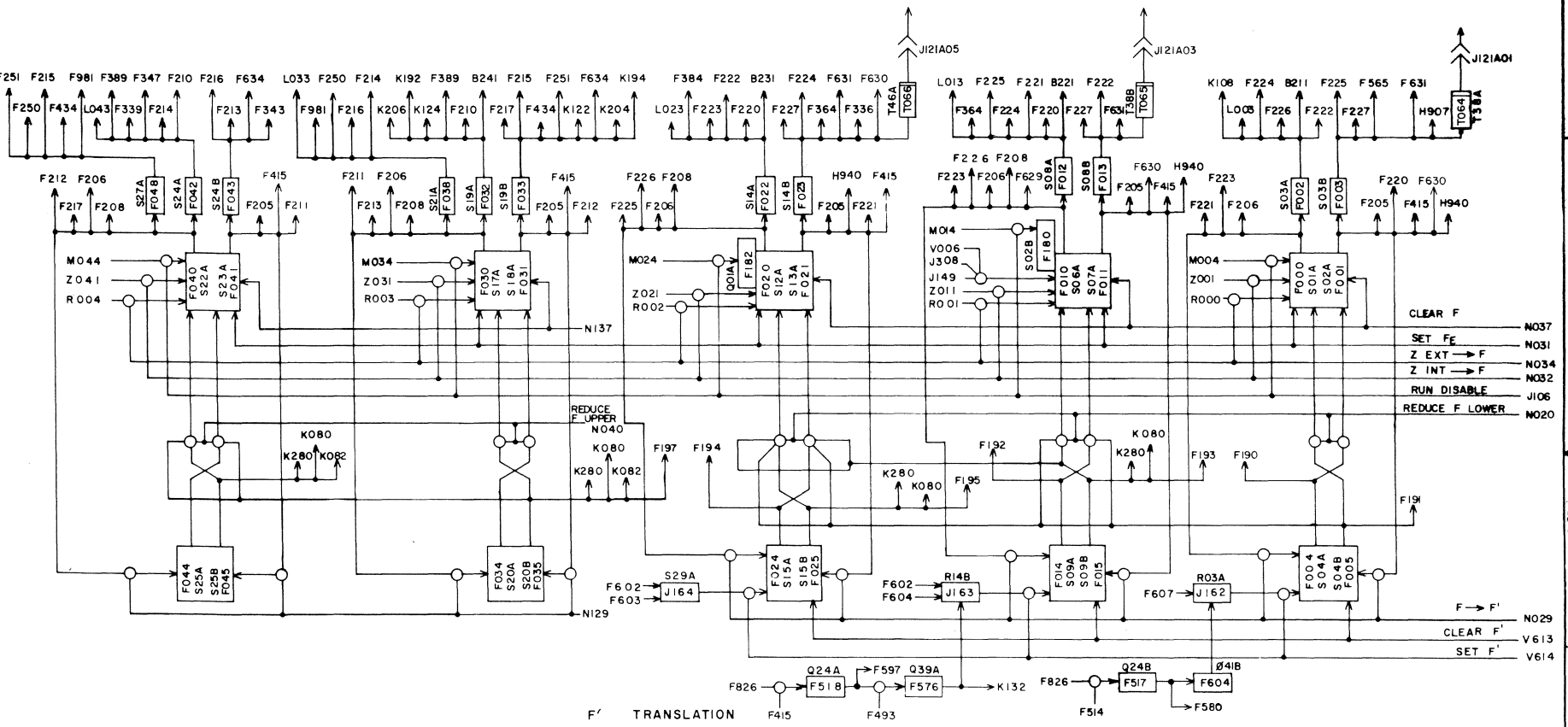


BREAKPOINT LOGIC

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 13

16501400 SHEET 13

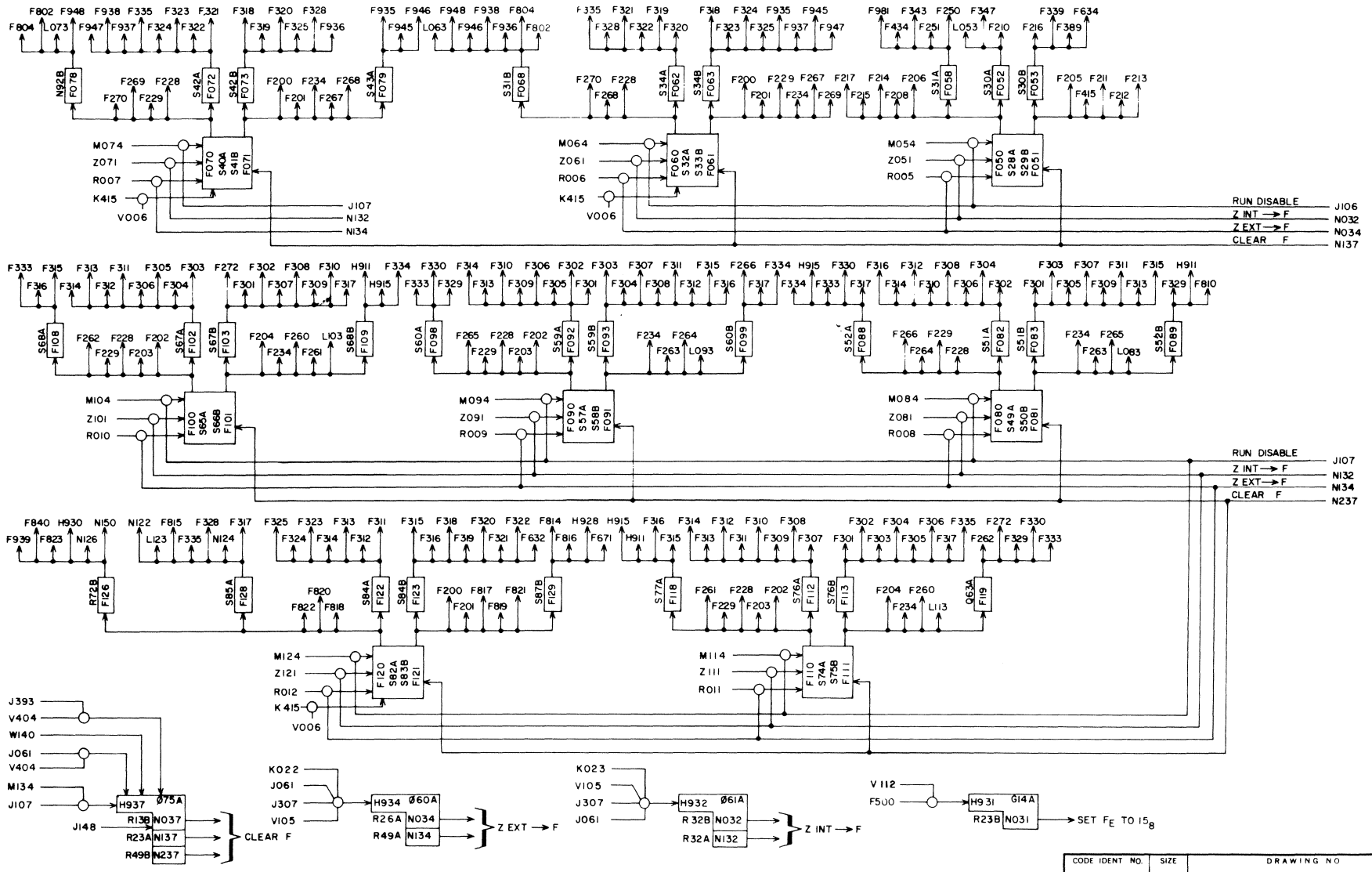
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE ——		SHEET 14

16501400 SHEET 14

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

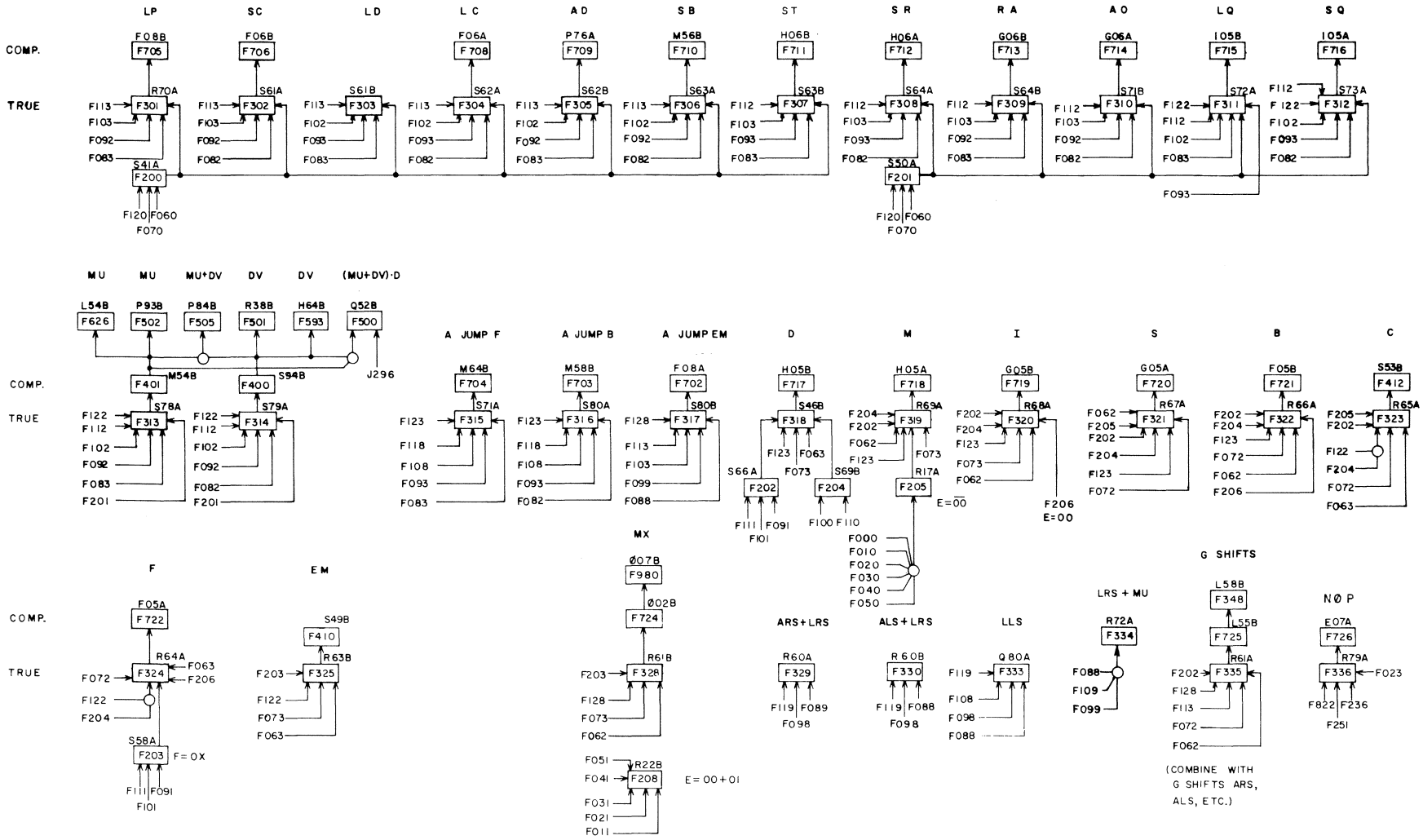


F REGISTER

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 15

16501400 SHEET 15

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

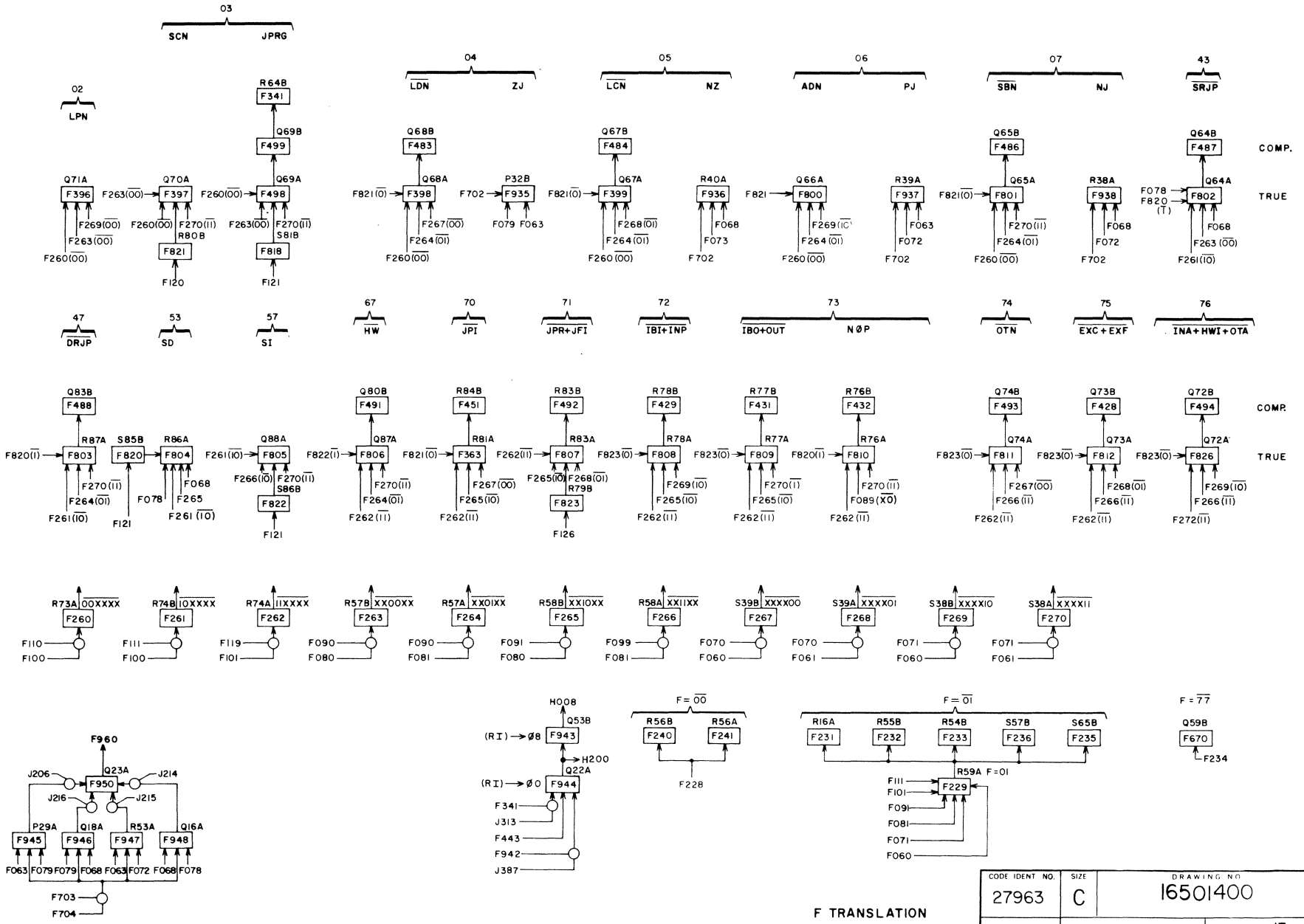


F TRANSLATION

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 16

16501400 SHEET 16

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

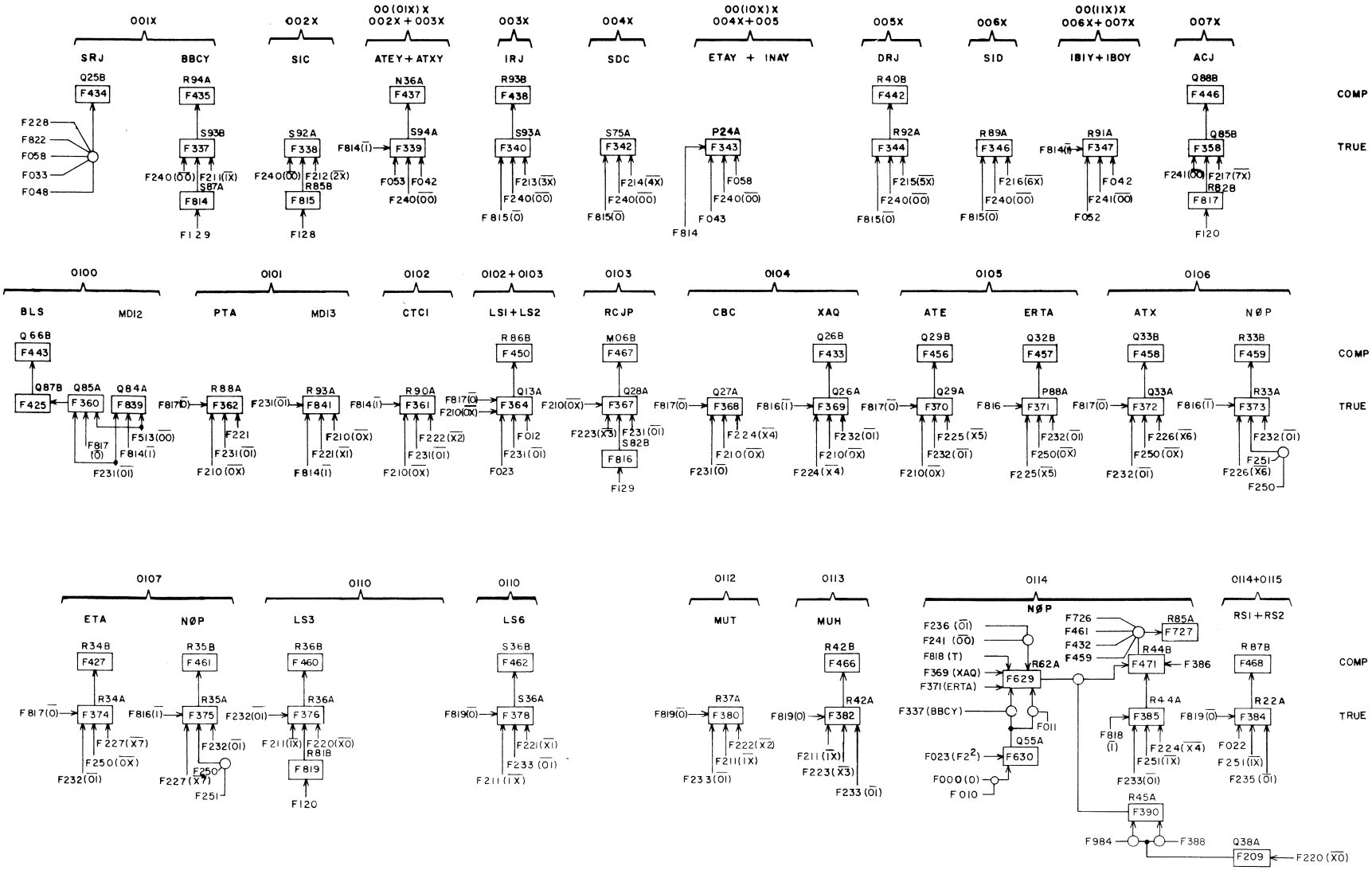


F TRANSLATION

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 17

16501400 SHEET 17

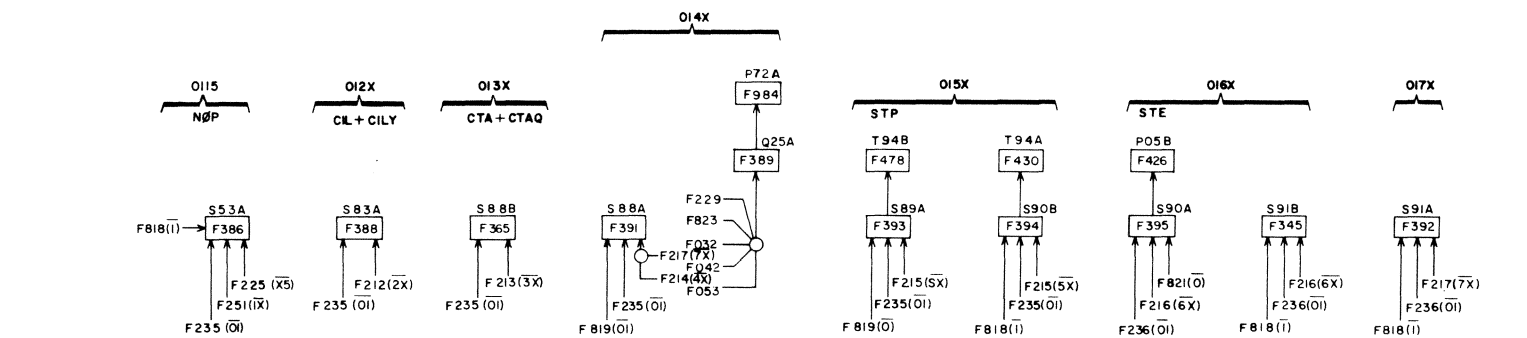
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
E		REVISED SEE ECO CB19772		



CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 18

16501400 SHEET 18

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

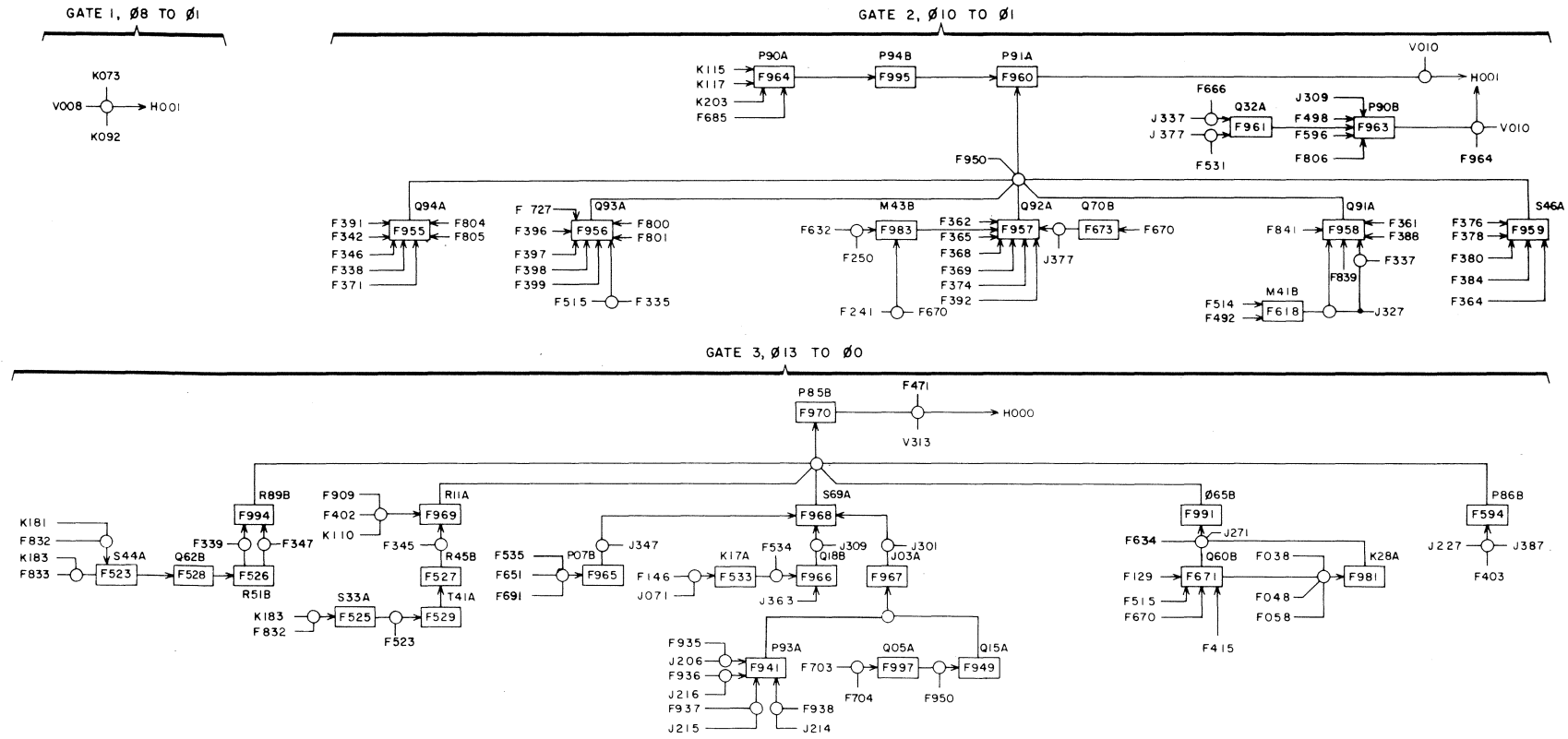


F TRANSLATION

CODE IDENT NO.	SIZE	DRAWING
27963	C	16501400
SCALE		SHEET 19

16501400
SHEET 19

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

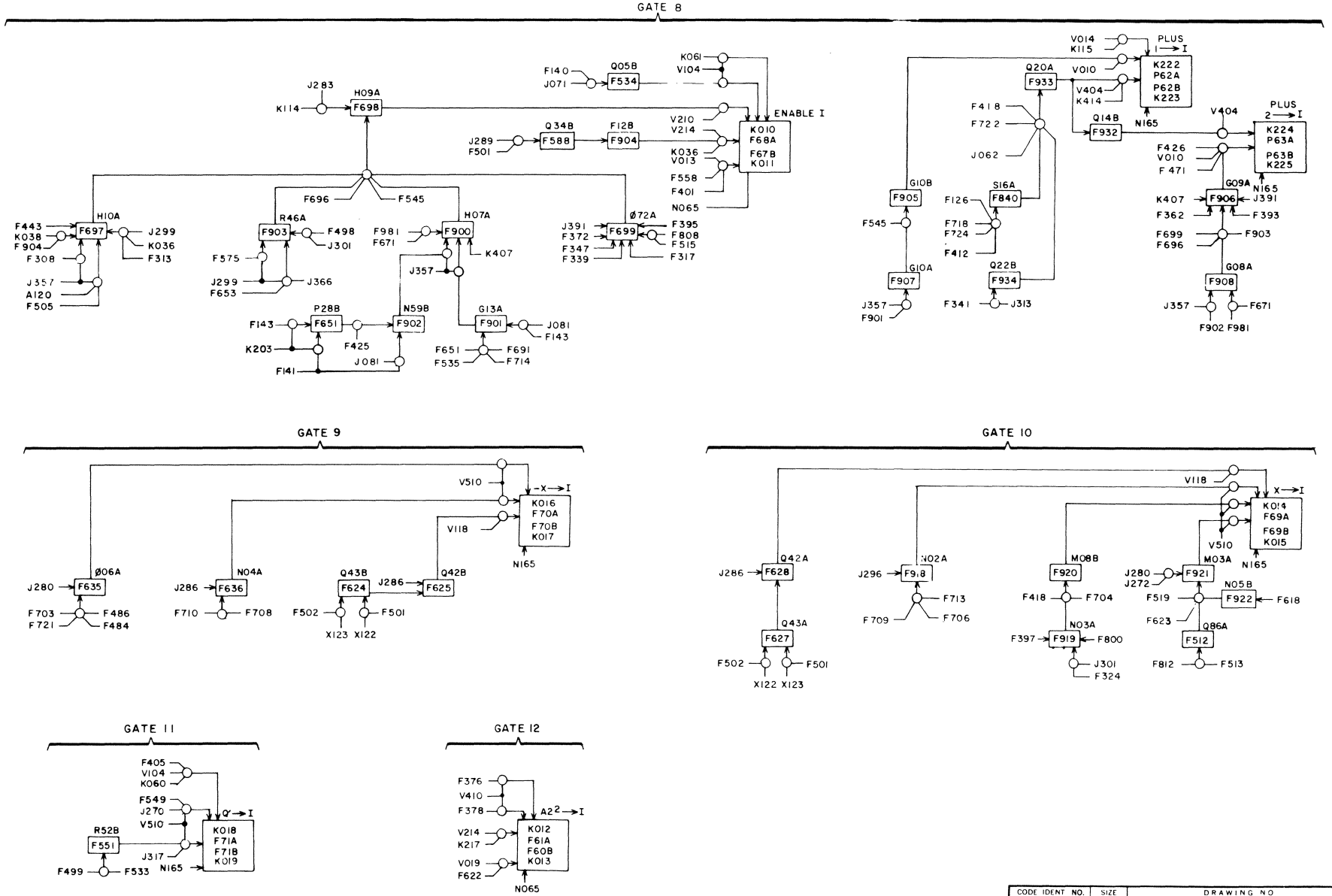


GATES 1 — 6

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 20

16501400 SHEET 20

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



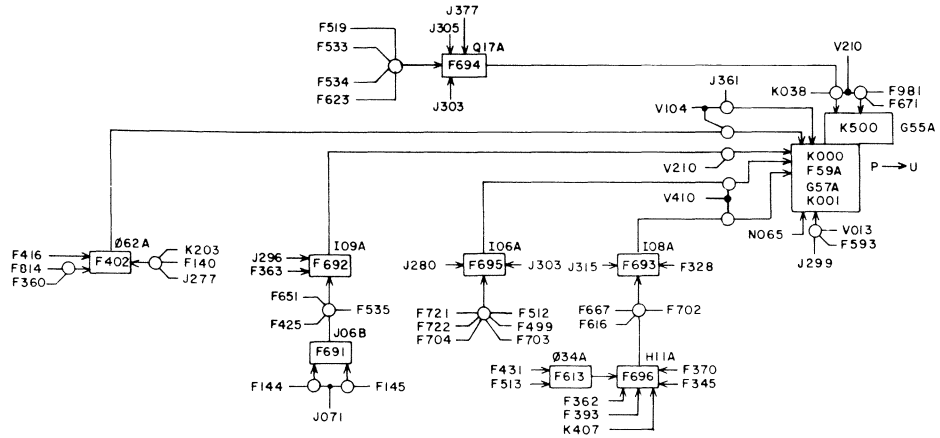
GATES 8-12

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 21

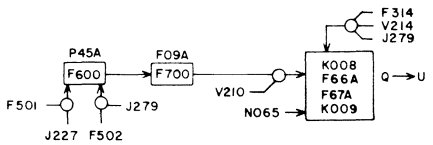
16501400
SHEET 21

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

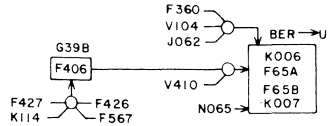
GATE 13



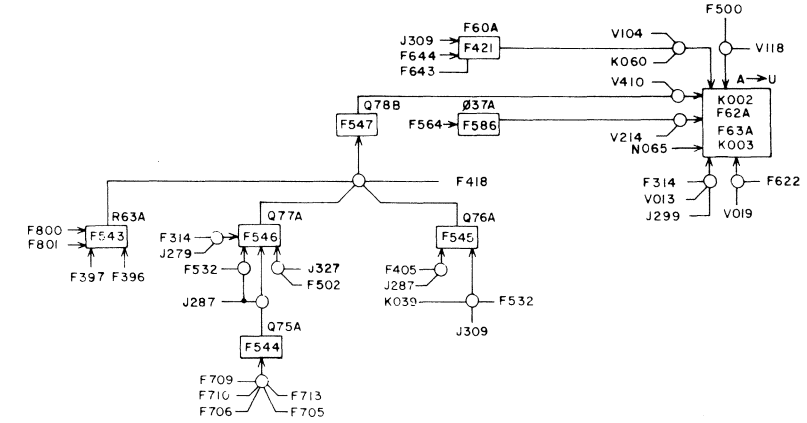
GATE 14



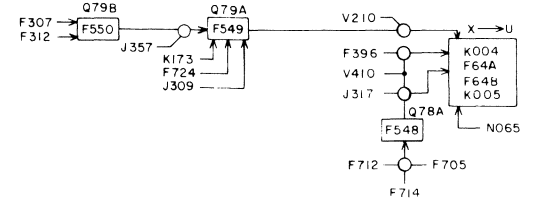
GATE 15



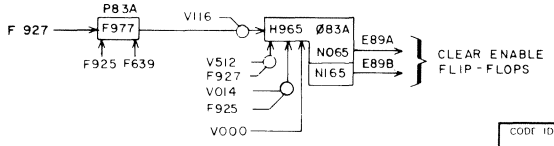
GATE 16



GATE 17



GATE 18



GATES 13—18

CODE IDENT NO.	SIZE	DRAWING NO.
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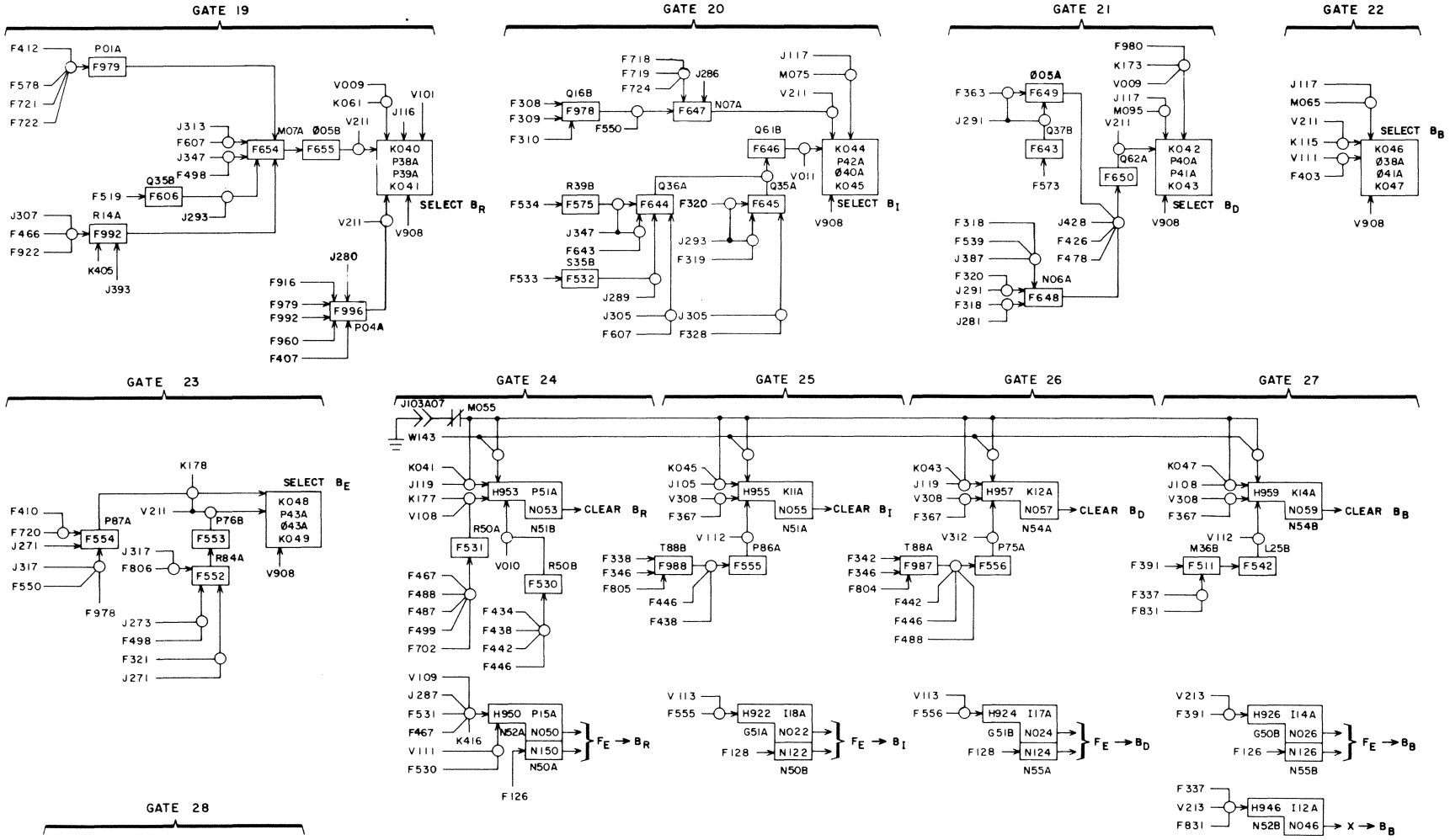
SCALE		SHEET 22

16501400
SHEET 22

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



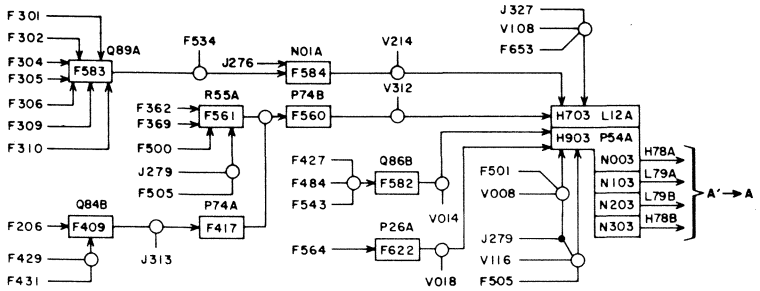
GATES 19—28

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 23

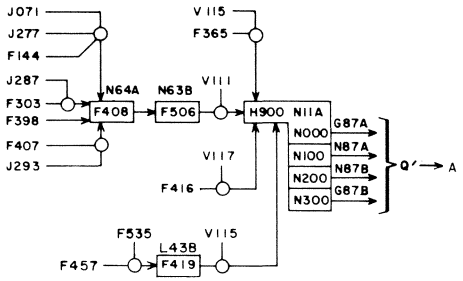
16501400
SHEET 23

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

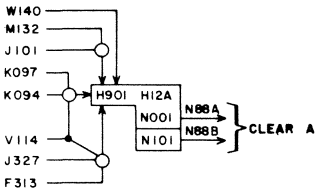
GATE 29



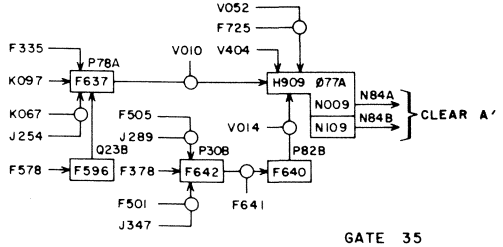
GATE 30



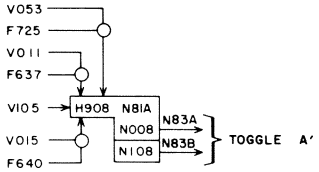
GATE 31



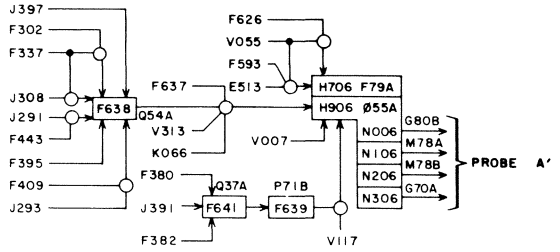
GATE 32



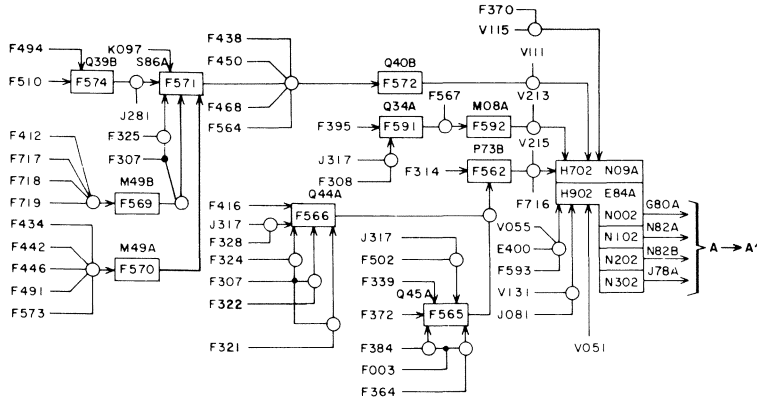
GATE 33



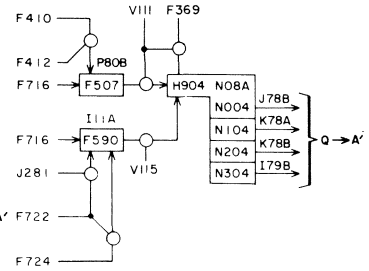
GATE 34



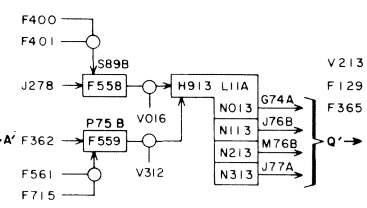
GATE 35



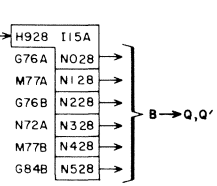
GATE 36



GATE 37



GATE 38

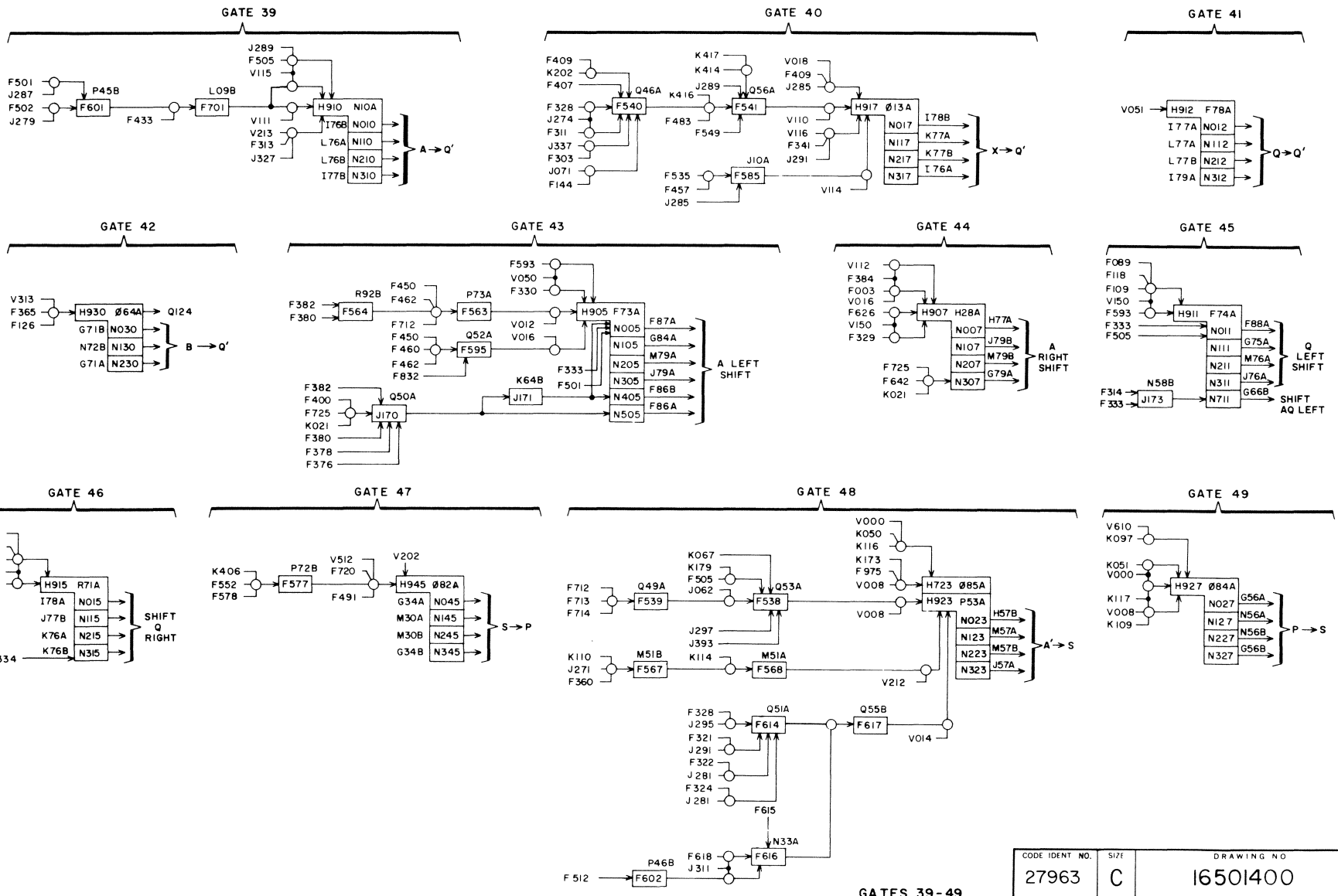


GATES 29—38

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 24

16501400 SHEET 24

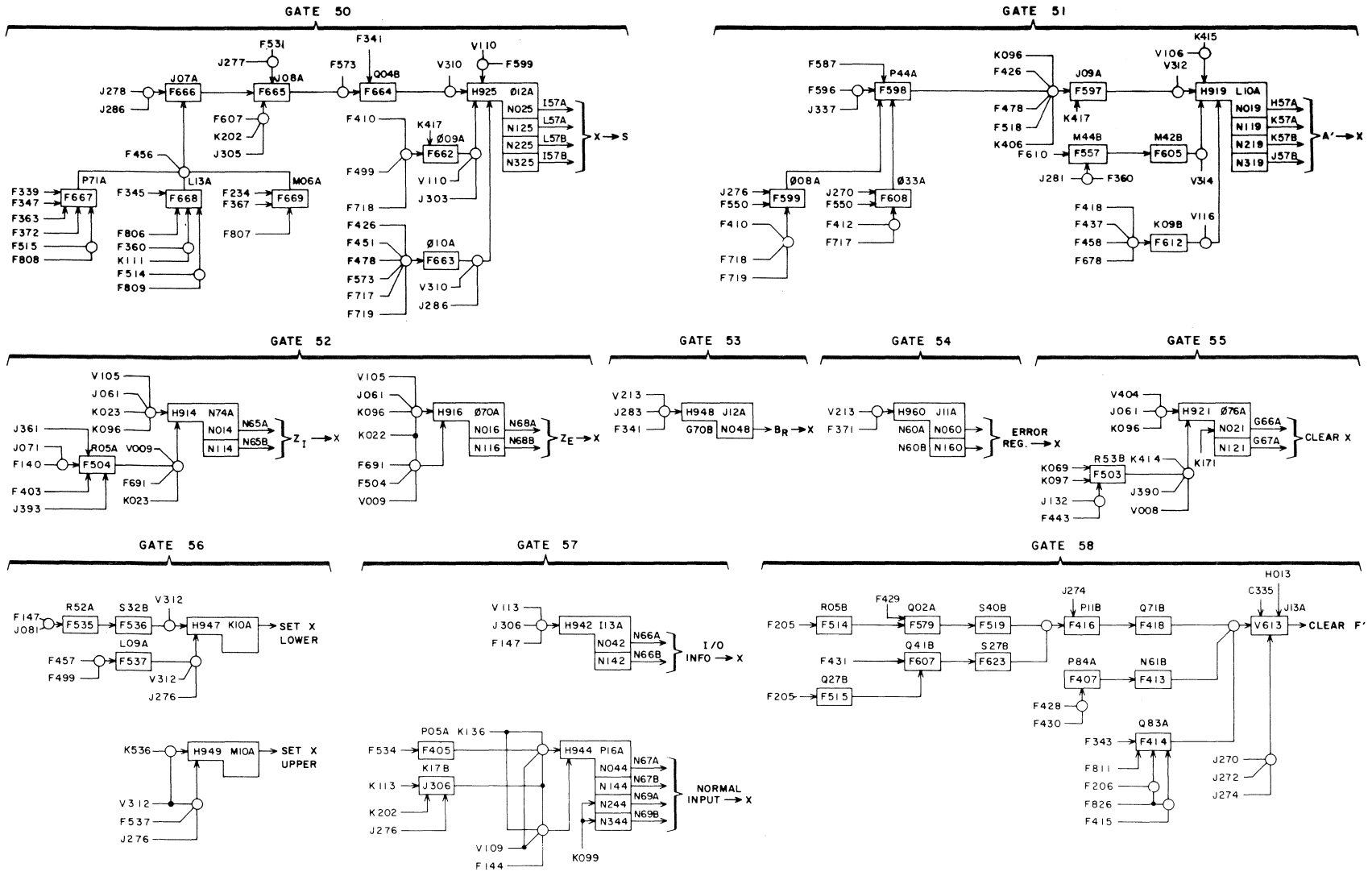
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



CODE IDENT. NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 25

16501400
SHEET 25

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

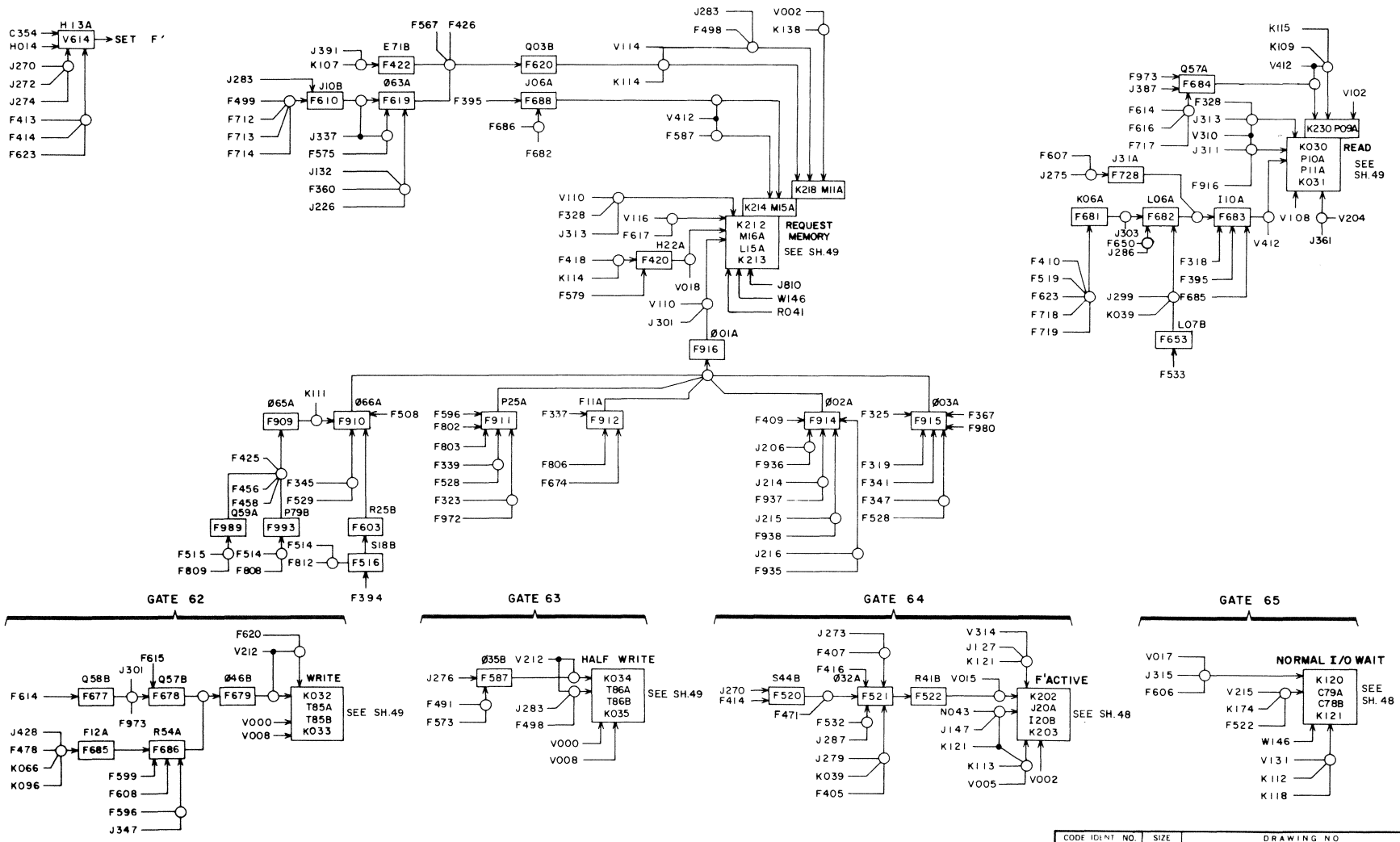


GATES 50-58

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 26

16501400 SHEET 26

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



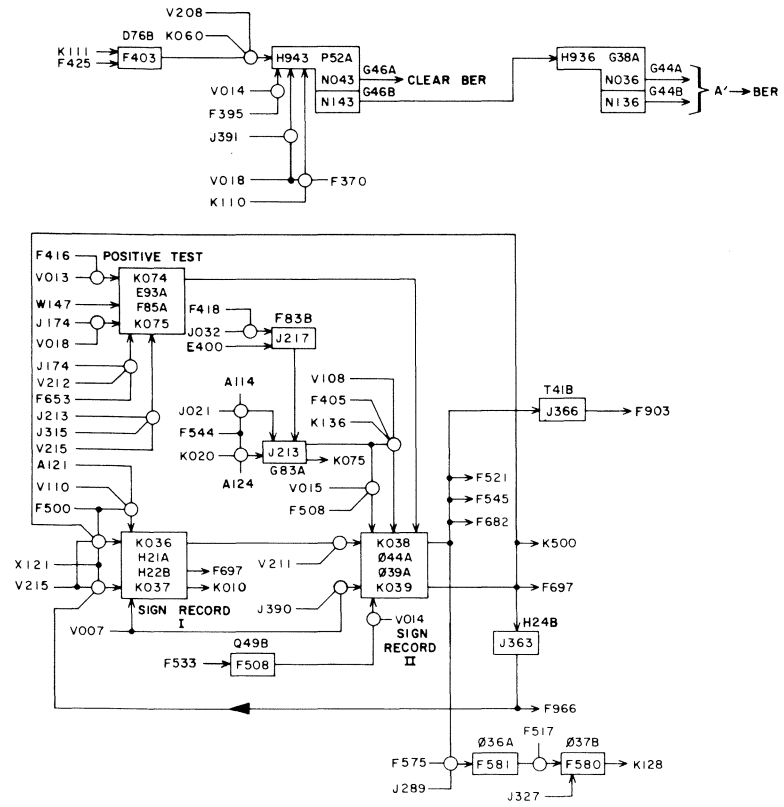
GATES 59 — 65

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 27

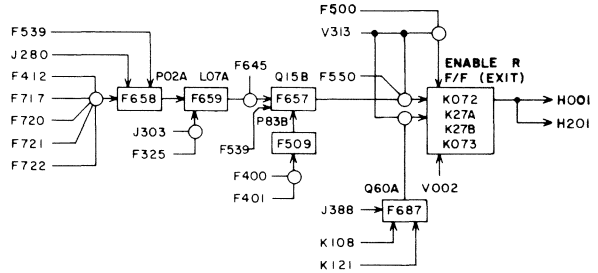
16501400
SHEET 27

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

GATE 66



GATE 67

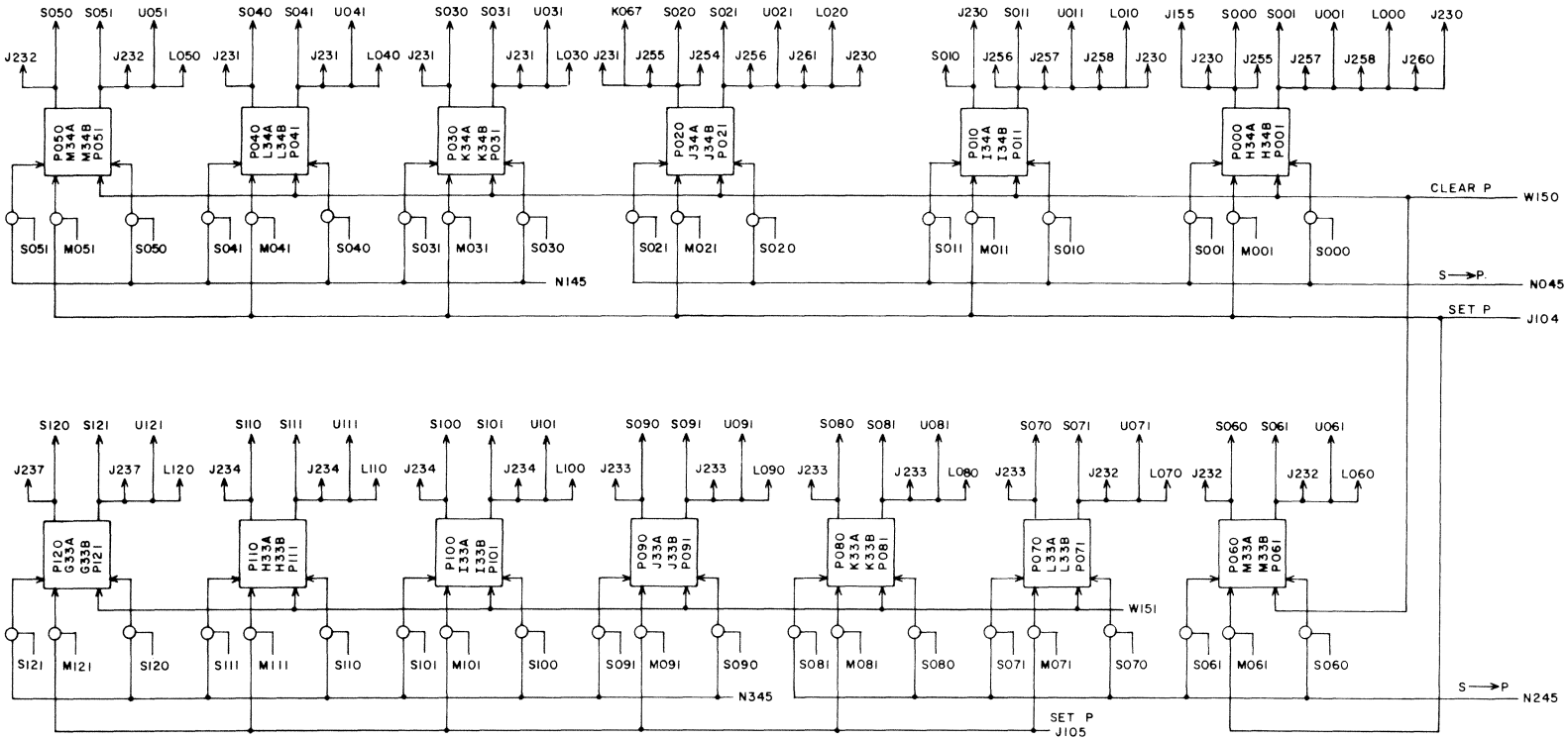


GATES 66 – 67

CODE IDENT NO.	SIZE	DRAW. NO.
27963	C	16501400
SCALE		SHEET 28

16501400
SHEET 28

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

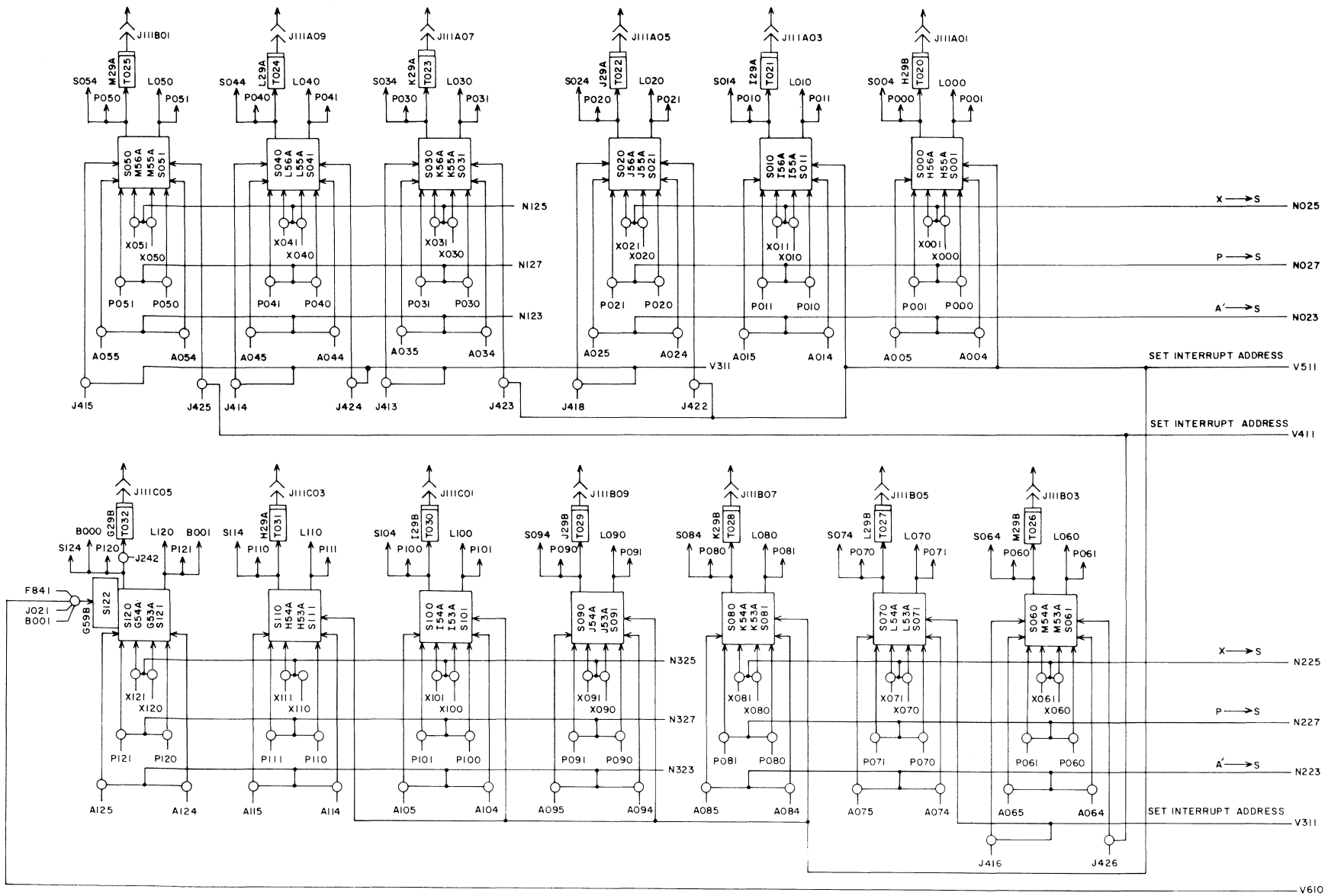


P REGISTER

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE —		SHEET 29

16501400
SHEET 29

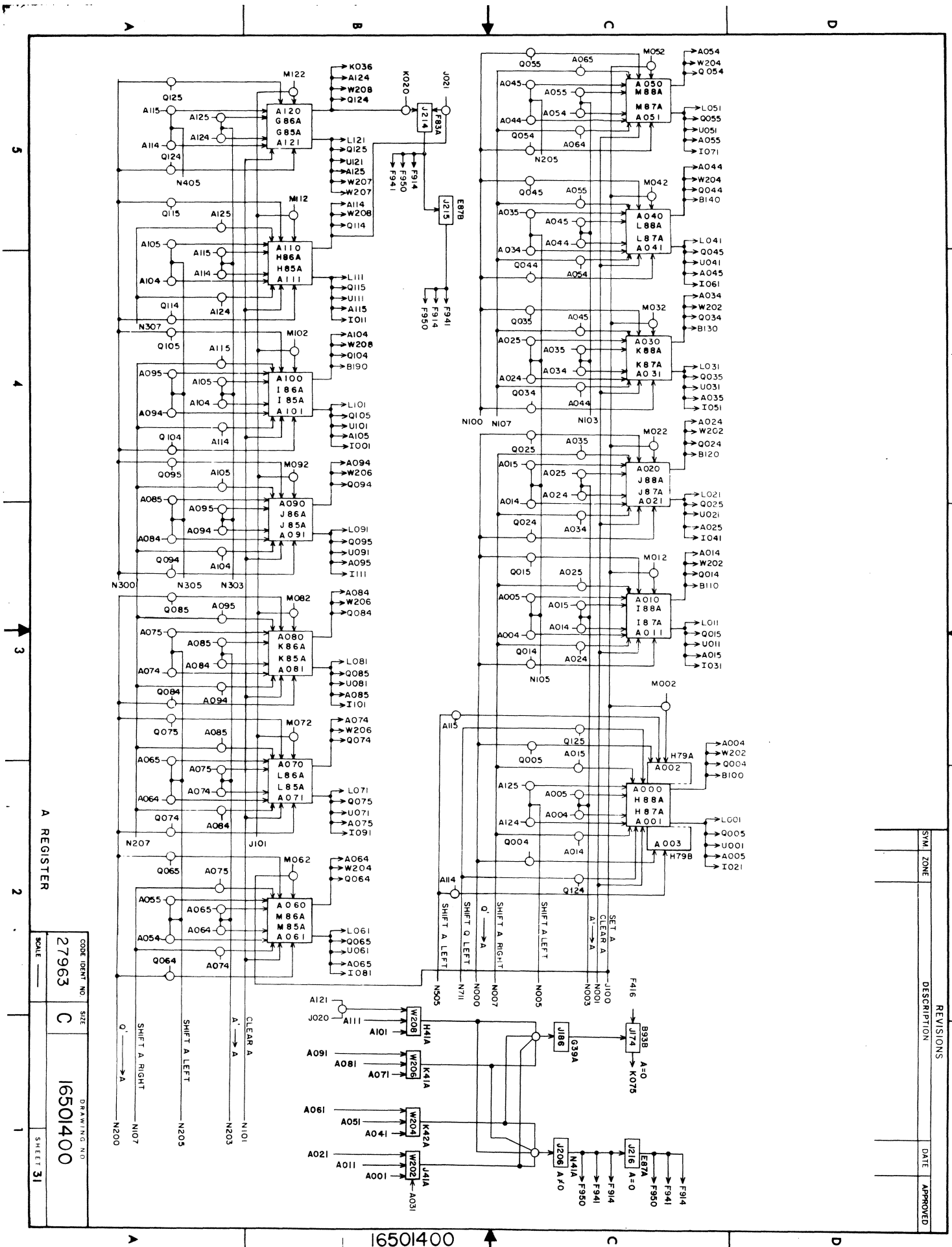
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



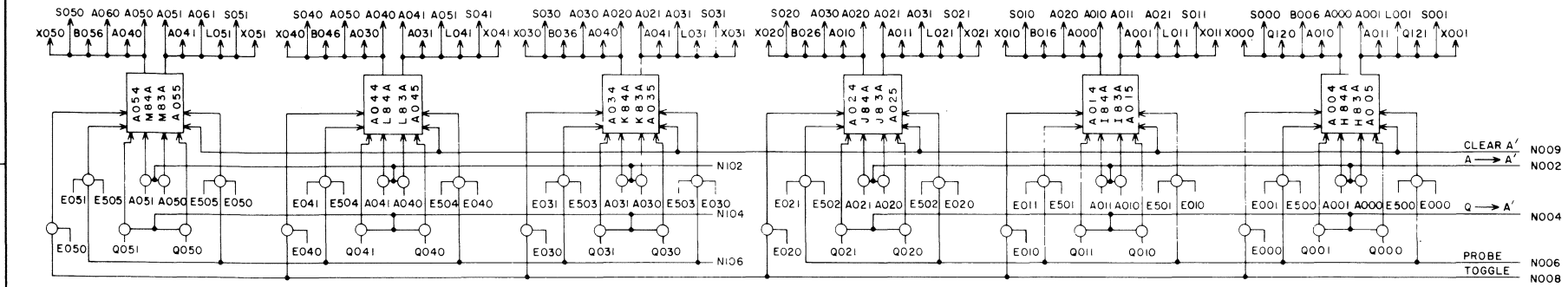
S REGISTER

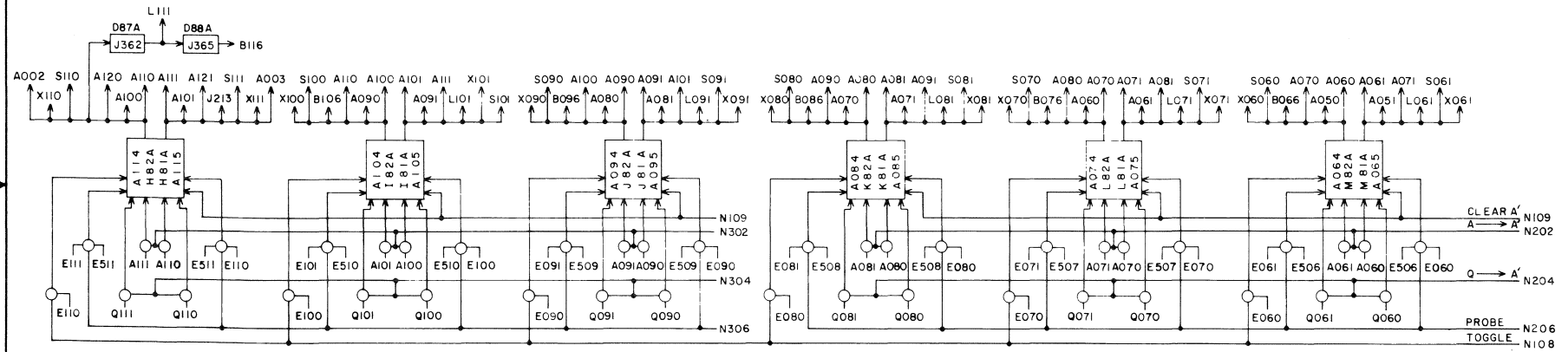
CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 30

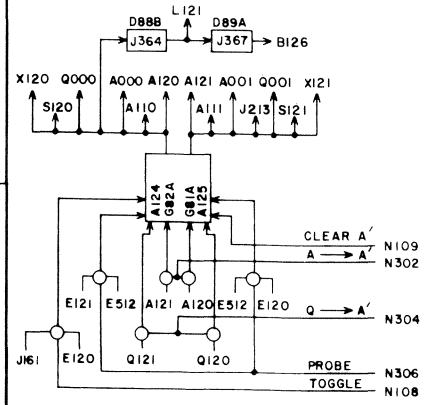
16501400
SHEET 30

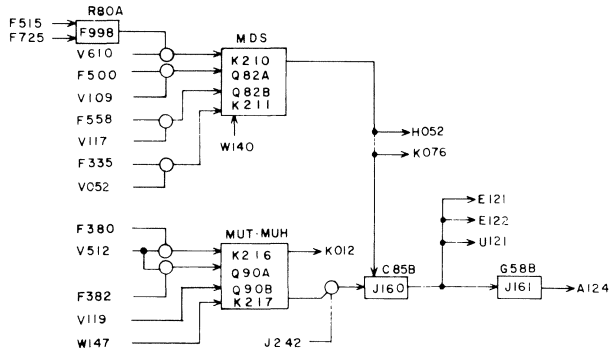

A REGISTER
A120 G86A G85A A121
A110 H86A H85A A111
A100 I86A I85A A101
A090 J86A J85A A091
A080 K86A K85A A081
A070 L86A L85A A071
A060 M86A M85A A061
A050 M88A M87A A051
A040 L88A L87A A041
A030 K88A K87A A031
A020 J88A J87A A021
A010 I88A I87A A011
A000 H88A H87A A001
A002
A003
SHIFT A LEFT
SHIFT Q LEFT
Q' → A
SHIFT A RIGHT
SHIFT A LEFT
A' → A
CLEAR A
SET A
SHIFT A RIGHT
SHIFT A LEFT
CLEAR A
Q' → A
REVISIONS
SYM.
ZONE
DESCRIPTION
DATE
APPROVED
CODE IDENT. NO. 27963
SIZE C
DRAWING NO. 16501400
SCALE —
SHEET 31
16501400
SHEET 31

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED







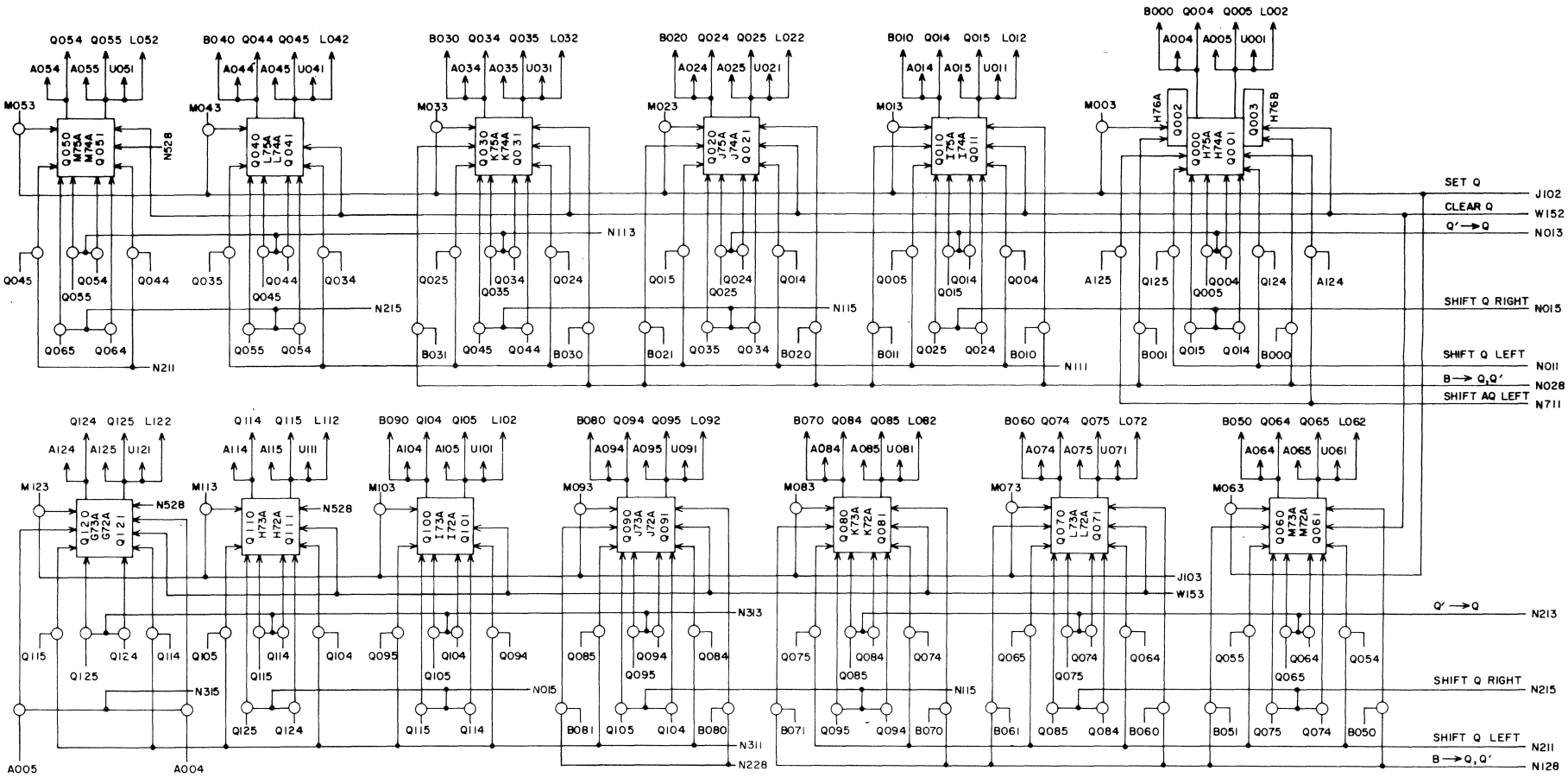


A′ REGISTER

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE —		SHEET 32

16501400
SHEET 32

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

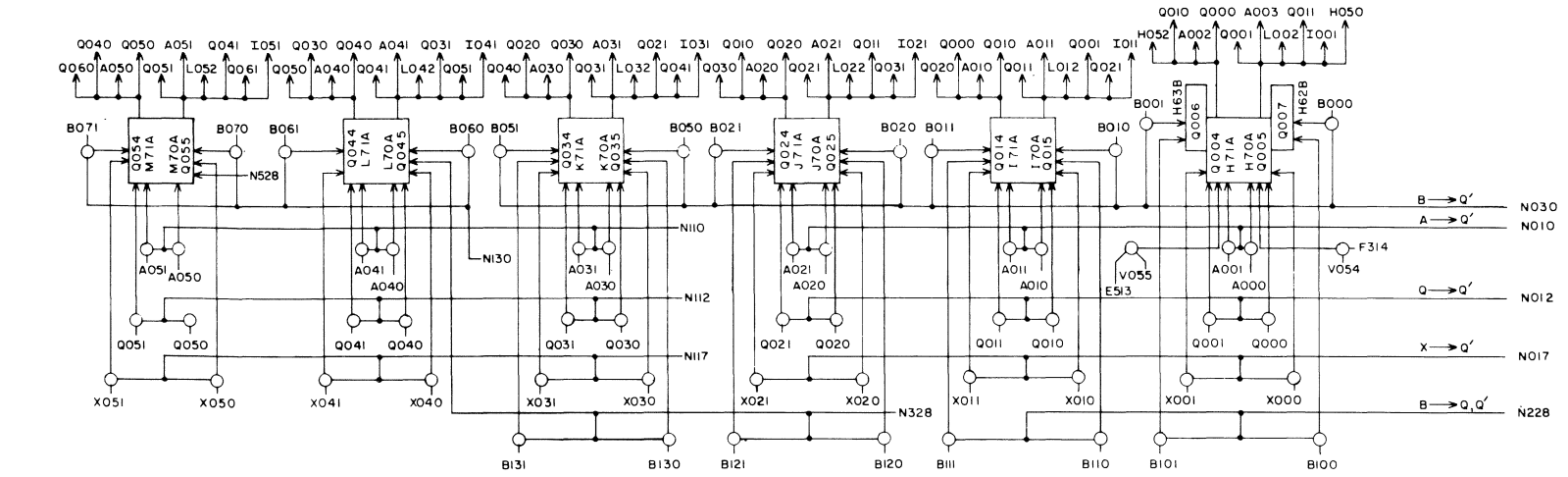


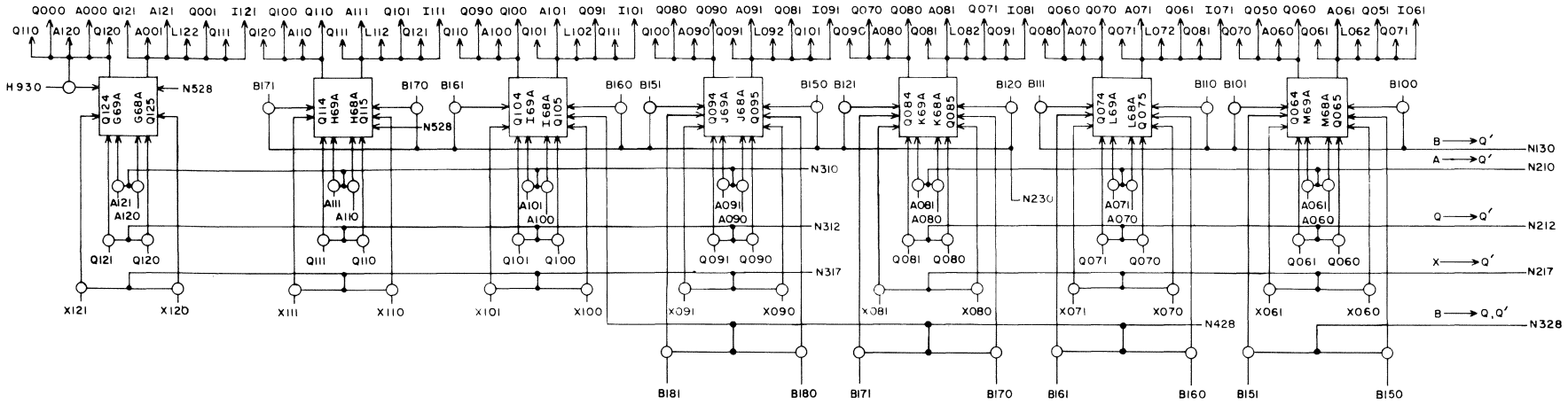
Q REGISTER

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 33

16501400
SHEET 33

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

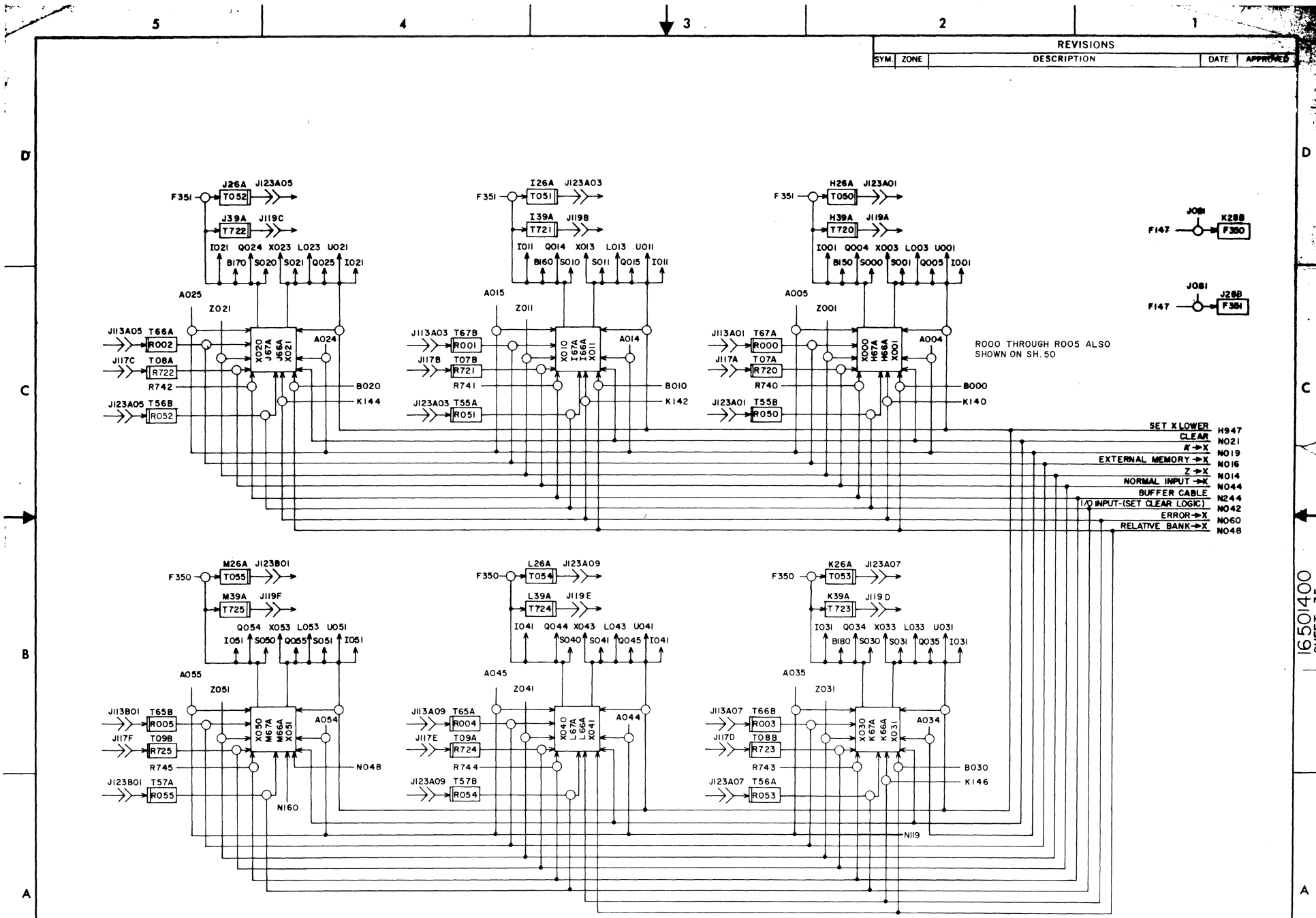




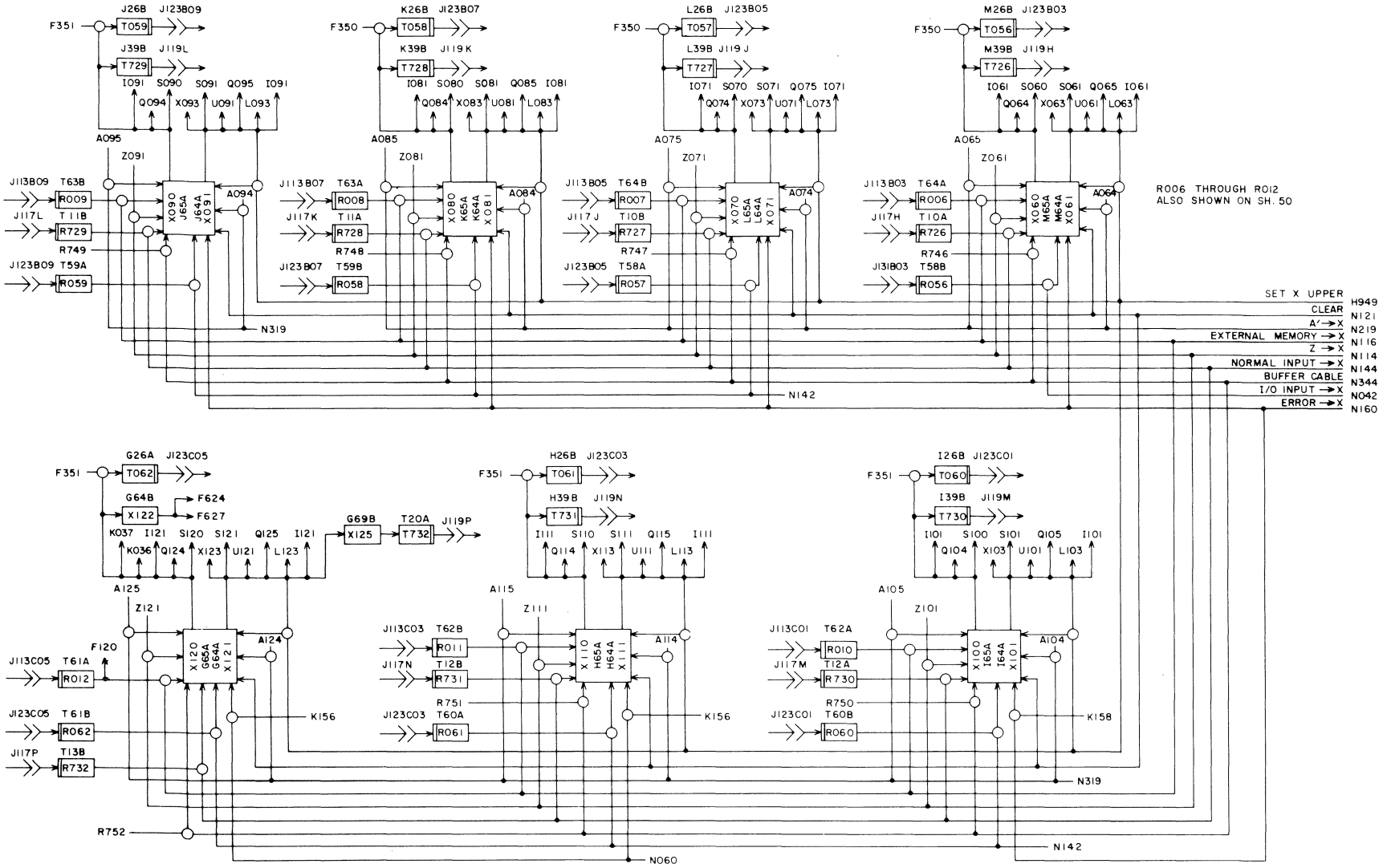
Q′ REGISTER

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 34

16501400 SHEET 34


REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
F351 J26A J123A05 T052 J39A J119C T722
I021 Q024 X023 L023 U021
B170 S020 S021 Q025 I021
A025 Z021
J113A05 T66A R002
J117C T08A R722
R742
J123A05 T56B R052
X020 J67A J66A X021
A024
B020
K144
F351 I26A J123A03 T051 I39A J119B T721
I011 Q014 X013 L013 U011
B160 S010 S011 Q015 I011
A015 Z011
J113A03 T67B R001
J117B T07B R721
R741
J123A03 T55A R051
X010 I67A I66A X011
A014
B010
K142
F351 H26A J123A01 T050 H39A J119A T720
I001 Q004 X003 L003 U001
B150 S000 S001 Q005 I001
A005 Z001
J113A01 T67A R000
J117A T07A R720
R740
J123A01 T55B R050
X000 H67A H66A X001
A004
B000
K140
ROOO THROUGH ROO5 ALSO SHOWN ON SH. 50
J08I K28B F147 F350
J08I J28B F147 F351
SET X LOWER H947
CLEAR N021
A→X N019
EXTERNAL MEMORY→X N016
Z→X N014
NORMAL INPUT→X N044
BUFFER CABLE N244
I/O INPUT-(SET CLEAR LOGIC) N042
ERROR→X N060
RELATIVE BANK→X N048
F350 M26A J123B01 T055 M39A J119F T725
Q054 X053 L053 U051
I051 S050 Q055 S051 I051
A055 Z051
J113B01 T65B R005
J117F T09B R725
R745
J123B01 T57A R055
X050 M67A M66A X051
A054
N048
N160
F350 L26A J123A09 T054 L39A J119E T724
I041 Q044 X043 L043 U041
S040 S041 Q045 I041
A045 Z041
J113A09 T65A R004
J117E T09A R724
R744
J123A09 T57B R054
X040 L67A L66A X041
A044
F350 K26A J123A07 T053 K39A J119D T723
I031 Q034 X033 L033 U031
B180 S030 S031 Q035 I031
A035 Z031
J113A07 T66B R003
J117D T08B R723
R743
J123A07 T56A R053
X030 K67A K66A X031
A034
B030
K146
N119
X REGISTER
CODE IDENT NO. 27963
SIZE C
DRAWING NO 16501400
SCALE
SHEET 35
16501400 SHEET 35

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

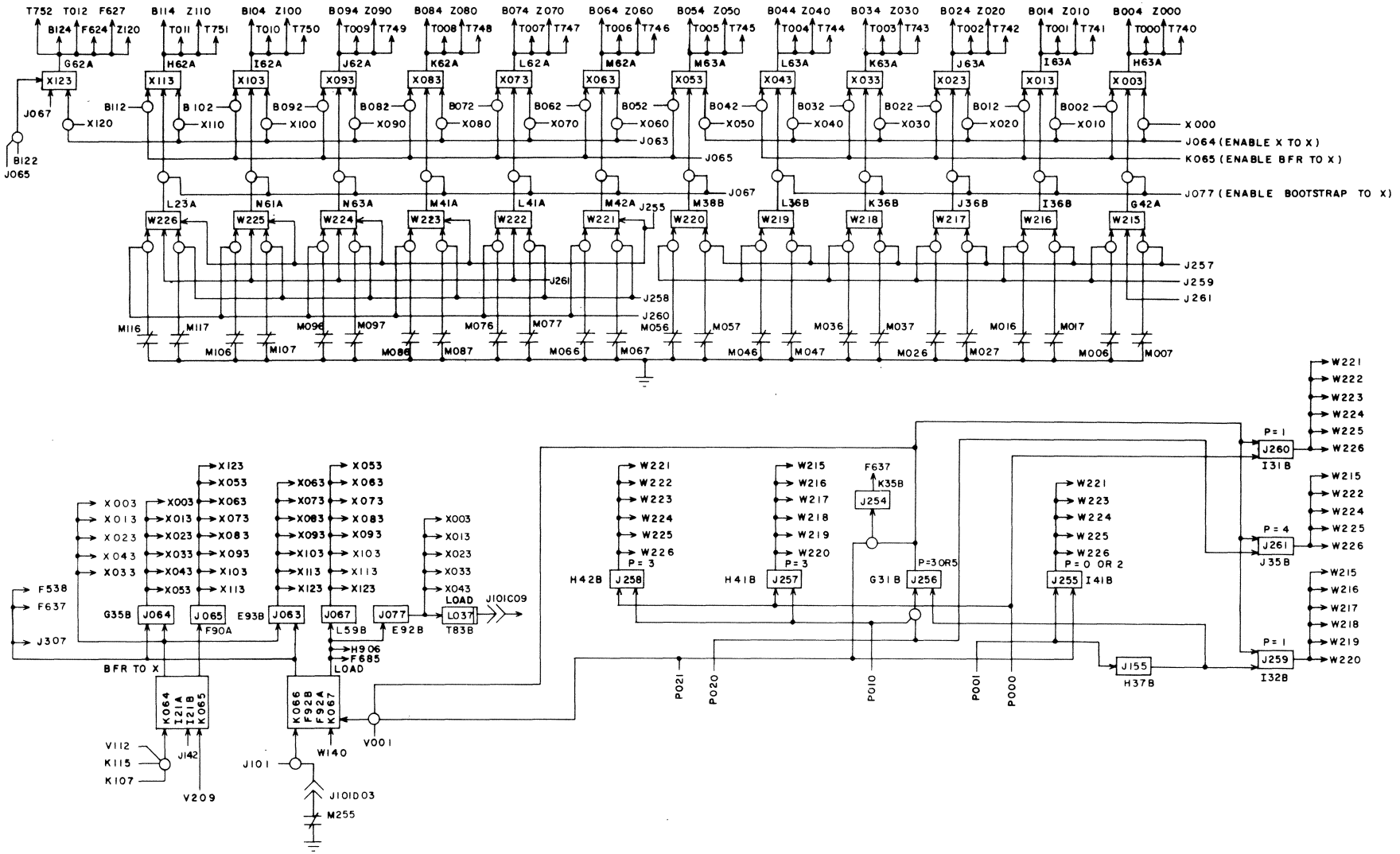


X REGISTER

16501400 SHEET 36

CODE IDENT. NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 36

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

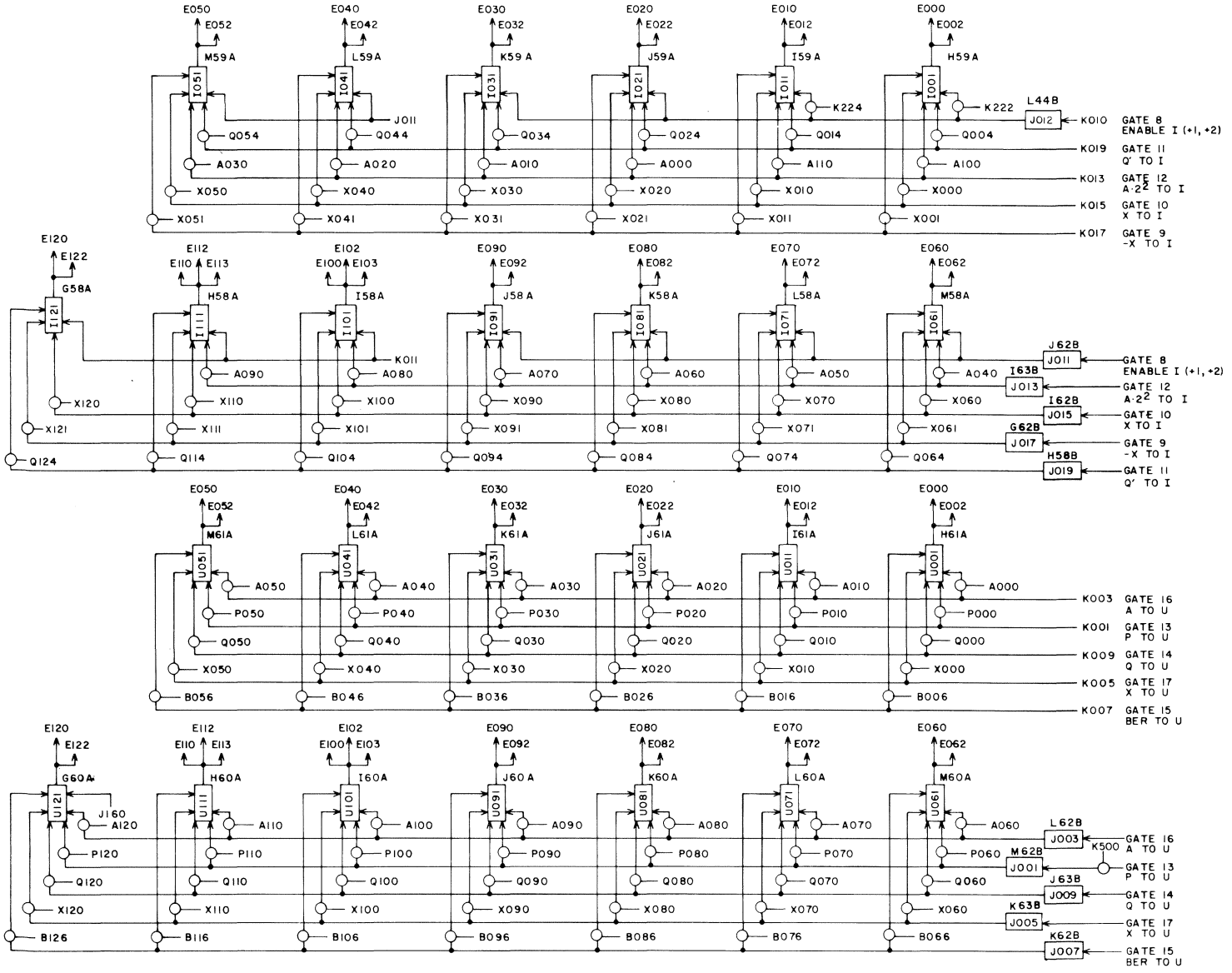


X INVERTERS

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 37

16501400
SHEET 37

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

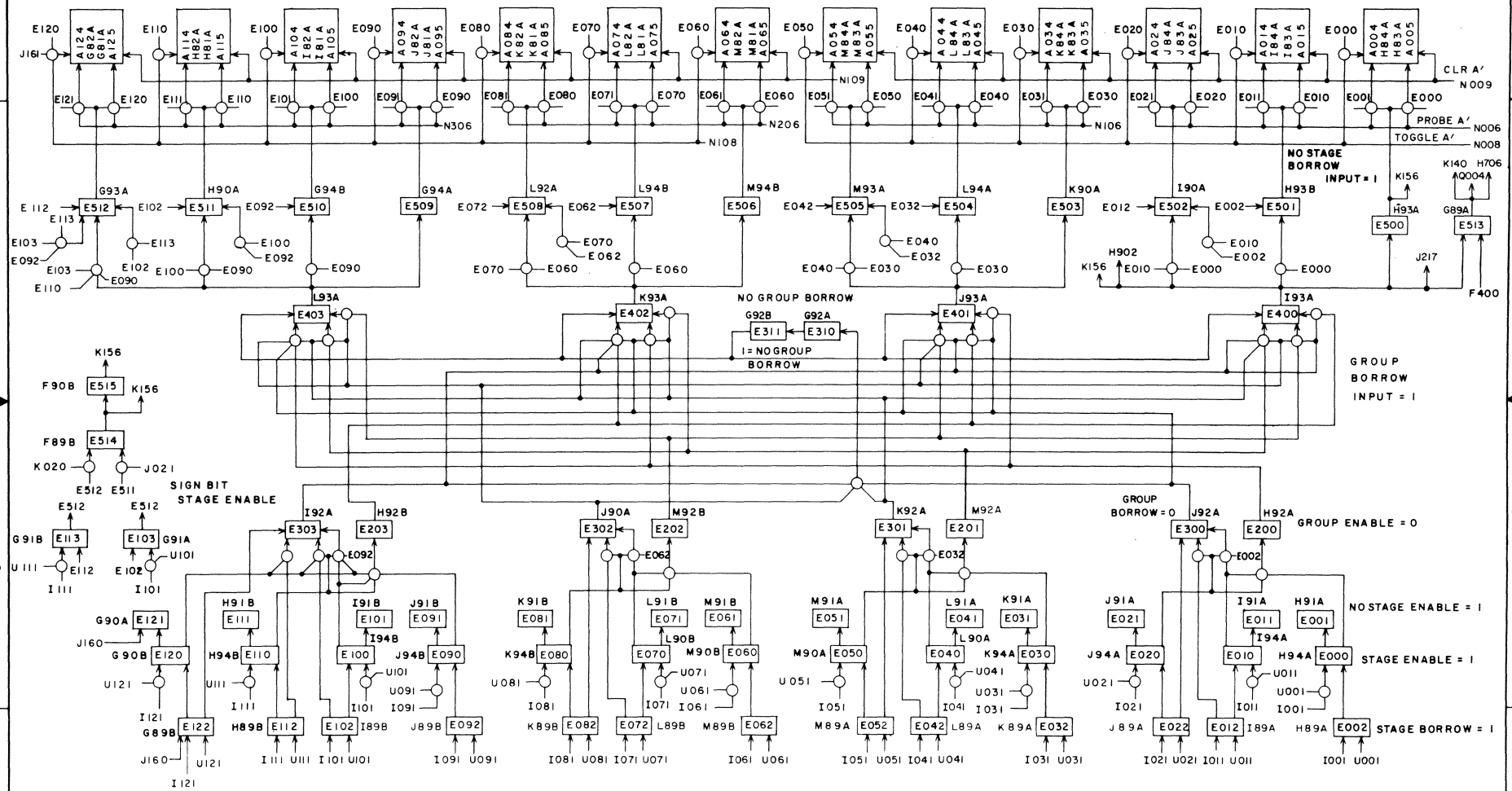


I AND U INVERTERS

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 38

16501400 SHEET 38

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

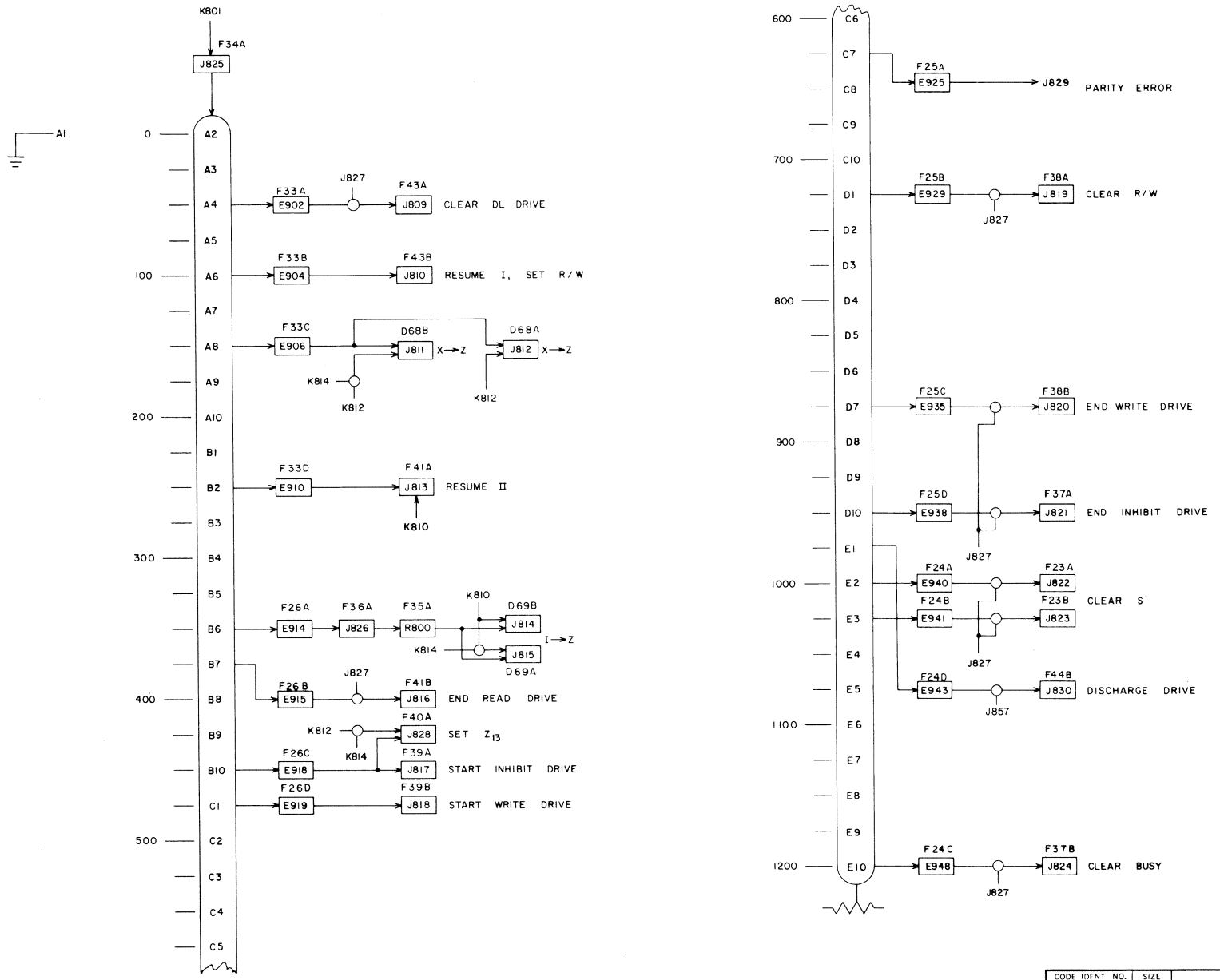


BORROW PYRAMID

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 39

16501400 SHEET 39

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB19692	11-13-68	J. S.

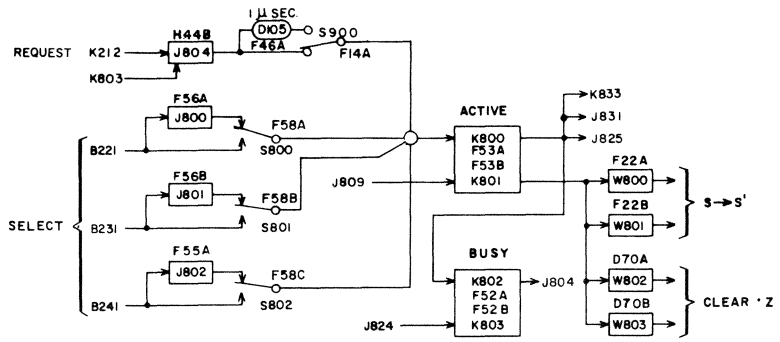


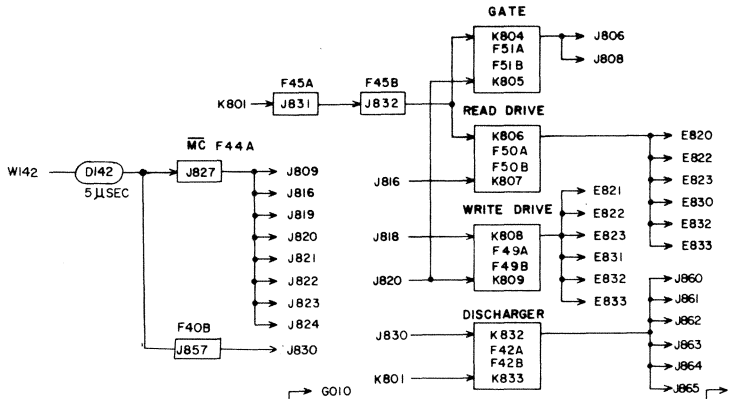
MEMORY CYCLE

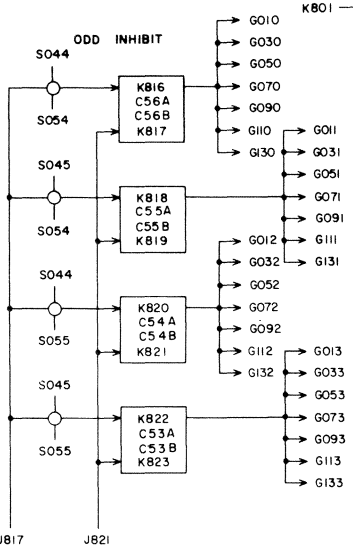
CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 40

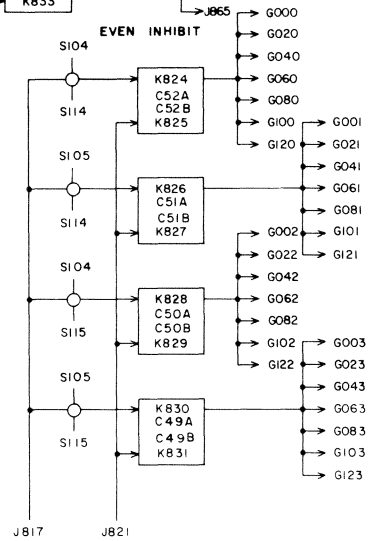
16501400
SHEET 40

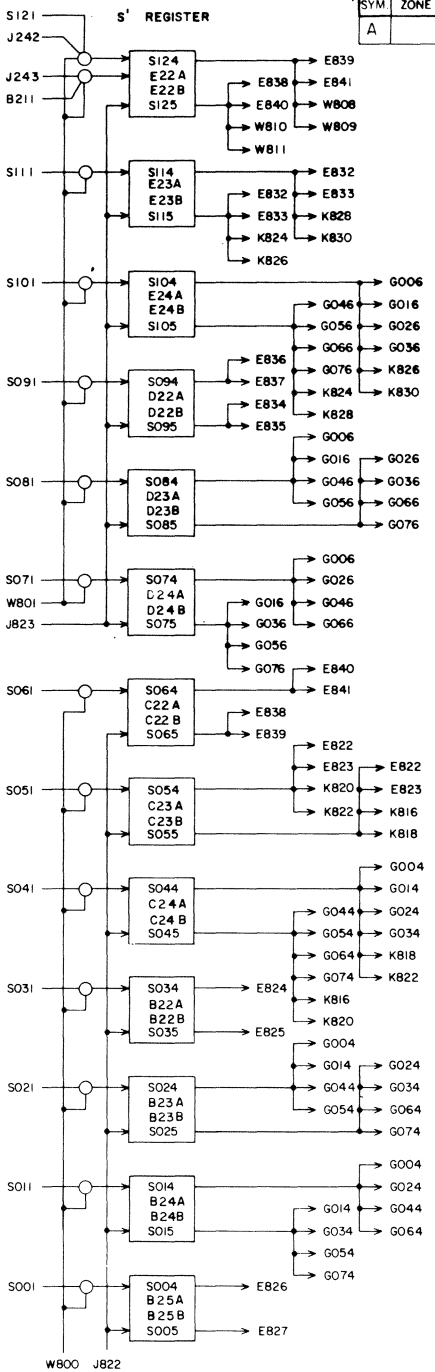
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB19692	11-13-68	

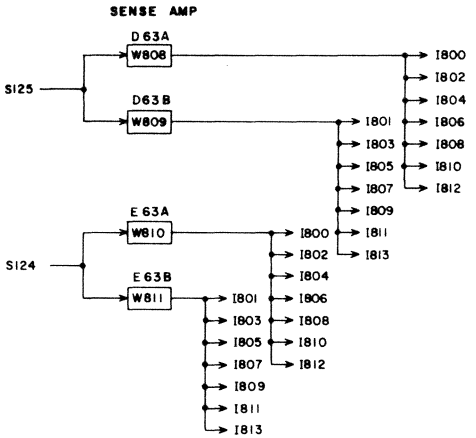


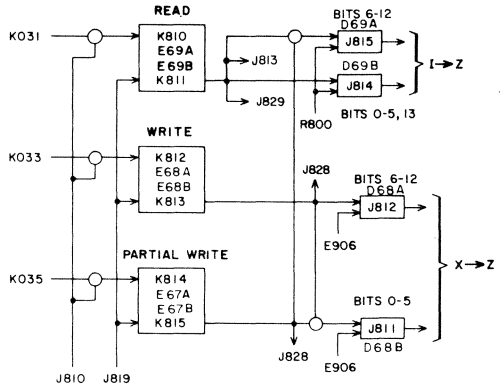








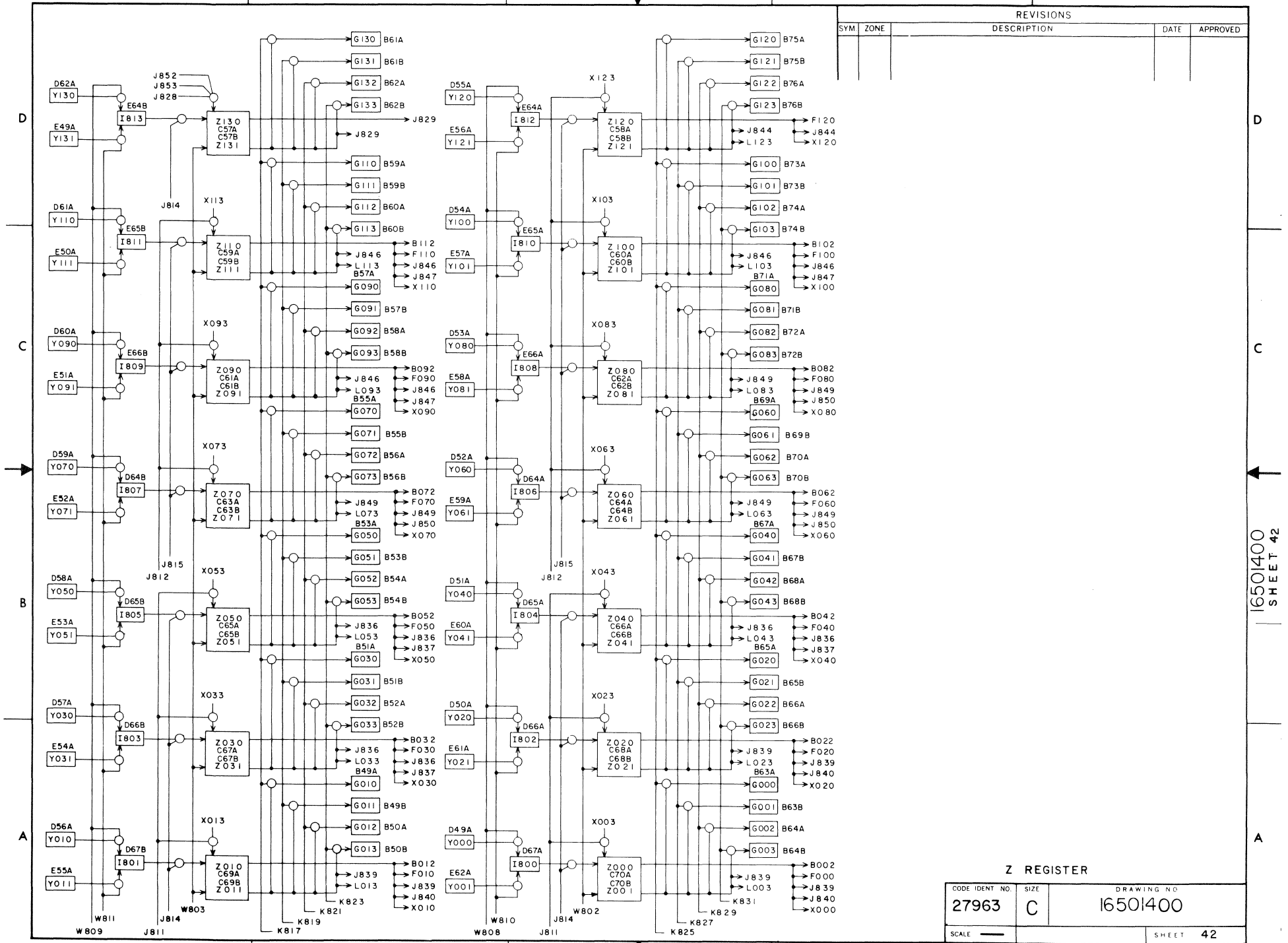




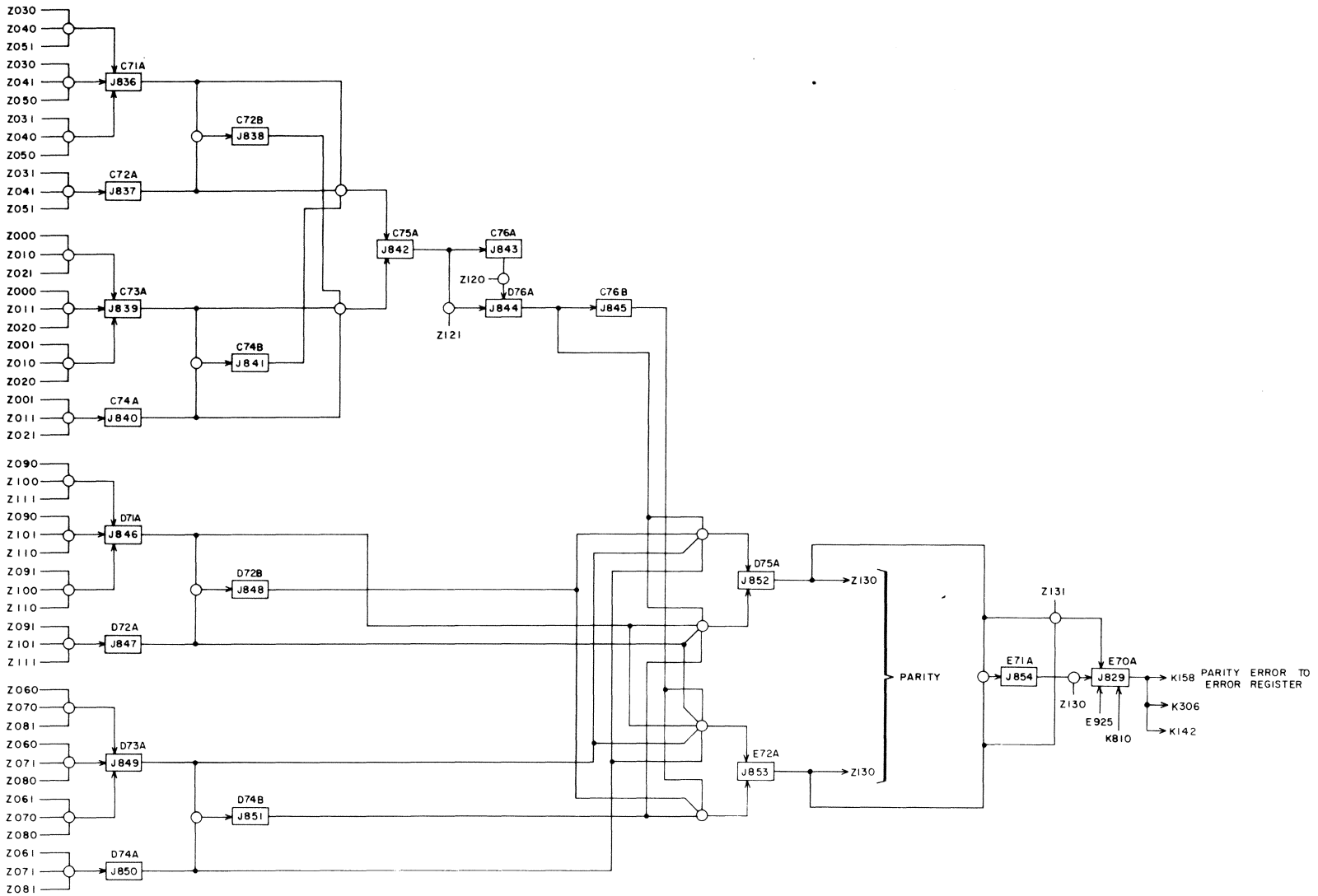
S' REGISTER AND
MEMORY CONTROL LOGIC

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 41

16501400
SHEET 41


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
Z REGISTER
CODE IDENT NO. 27963
SIZE C
DRAWING NO 16501400
SCALE
SHEET 42
16501400 SHEET 42

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

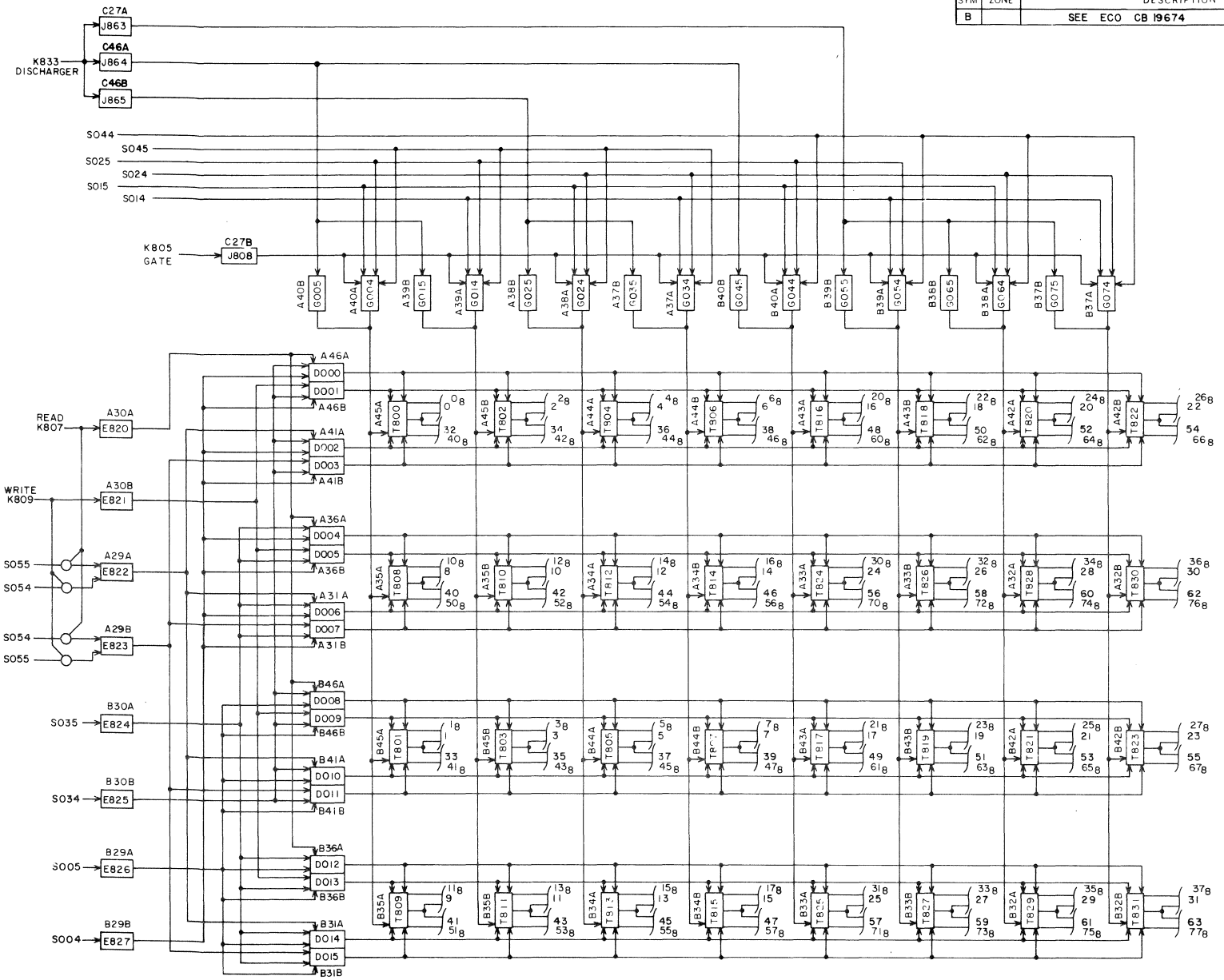


PARITY

CODE IDENT. NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 43

16501400 SHEET 43

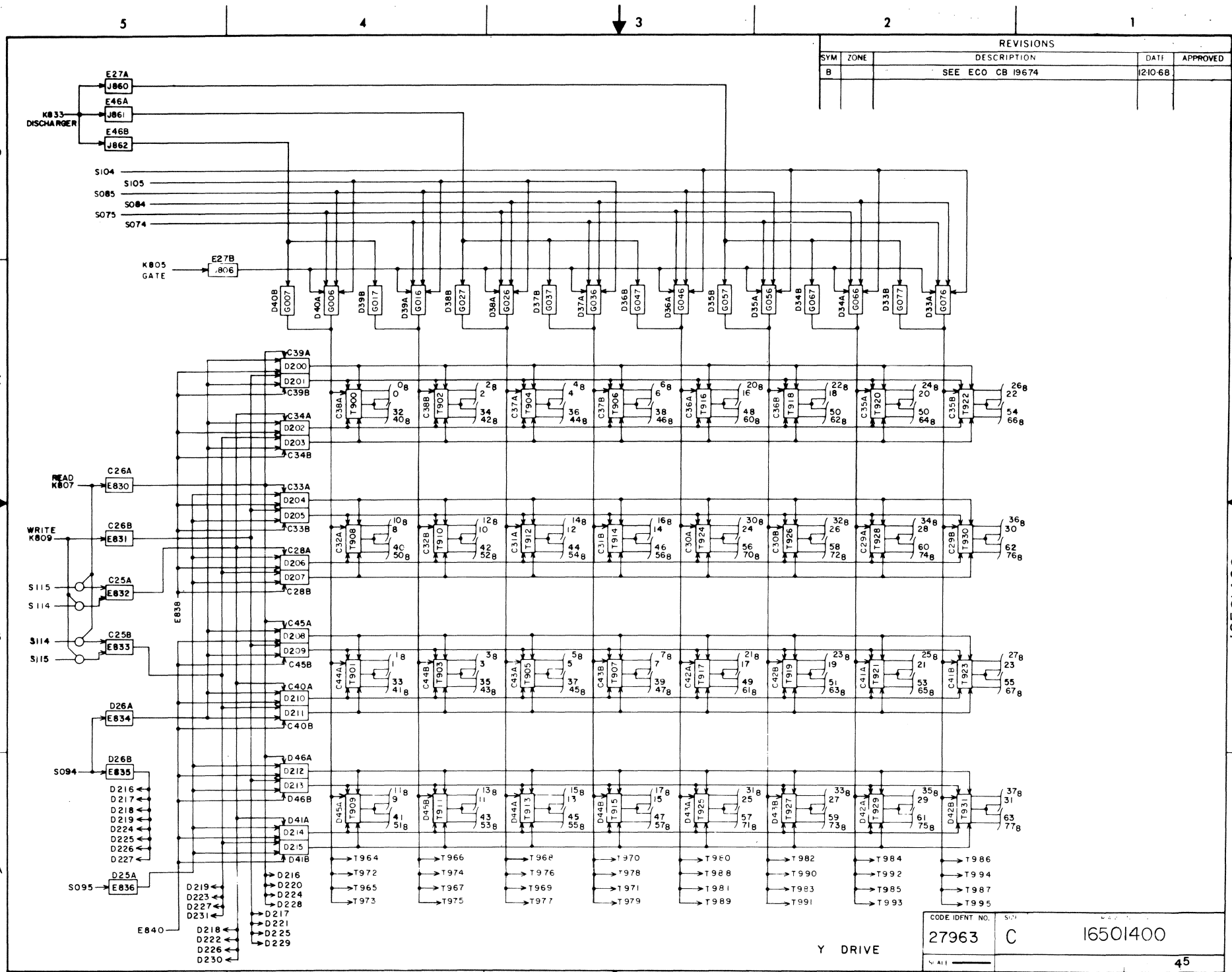
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
B		SEE ECO CB 19674	12-10-68	

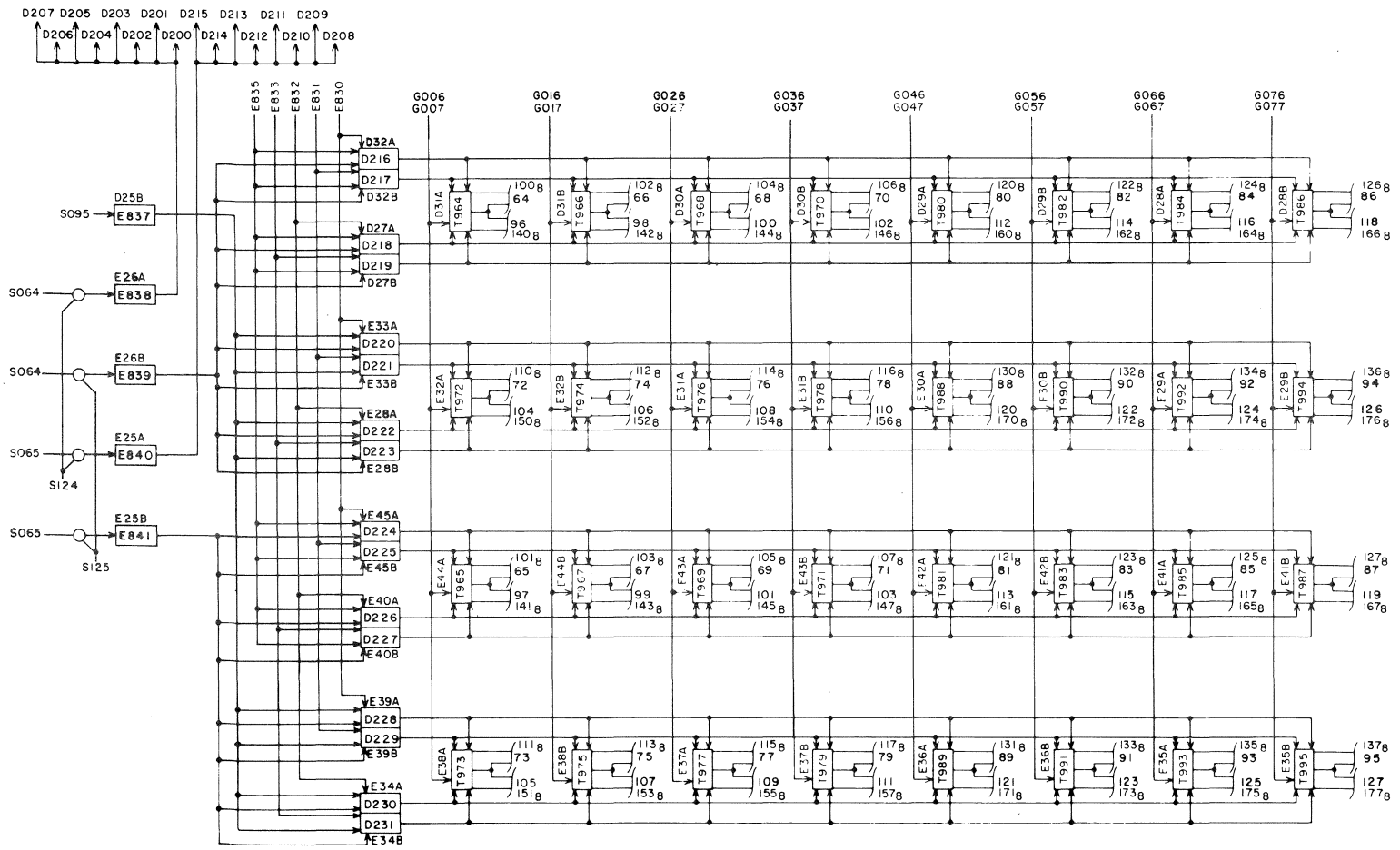


X DRIVE

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE		SHEET 44

16501400
SHEET 44


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
B | | SEE ECO CB 19674 | 12-10-68 |
E27A J860
E46A J861
E46B J862
K833 DISCHARGER
S104
S105
S085
S084
S075
S074
K805 GATE
E27B J806
D40B G007
D40A G006
D39B G017
D39A G016
D38B G027
D38A G026
D37B G037
D37A G036
D36B G047
D36A G046
D35B G057
D35A G056
D34B G067
D34A G066
D33B G077
D33A G076
C39A D200 D201 C39B
C34A D202 D203 C34B
C33A D204 D205 C33B
C28A D206 D207 C28B
C45A D208 D209 C45B
C40A D210 D211 C40B
D46A D212 D213 D46B
D41A D214 D215 D41B
READ K807
WRITE K809
C26A E830
C26B E831
C25A E832
C25B E833
D26A E834
D26B E835
D25A E836
S115
S114
S094
S095
E838
E840
D216 D217 D218 D219 D224 D225 D226 D227
D219 D223 D227 D231
D218 D222 D226 D230
D216 D220 D224 D228
D217 D221 D225 D229
C38A T900
C38B T902
C37A T904
C37B T906
C36A T916
C36B T918
C35A T920
C35B T922
C32A T908
C32B T910
C31A T912
C31B T914
C30A T924
C30B T926
C29A T928
C29B T930
C44A T901
C44B T903
C43A T905
C43B T907
C42A T917
C42B T919
C41A T921
C41B T923
D45A T909
D45B T911
D44A T913
D44B T915
D43A T925
D43B T927
D42A T929
D42B T931
T964 T972 T965 T973
T966 T974 T967 T975
T968 T976 T969 T977
T970 T978 T971 T979
T980 T988 T981 T989
T982 T990 T983 T991
T984 T992 T985 T993
T986 T994 T987 T995
Y DRIVE
CODE IDENT NO. 27963
SIZE C
16501400
SCALE
45
16501400 SHEET 45

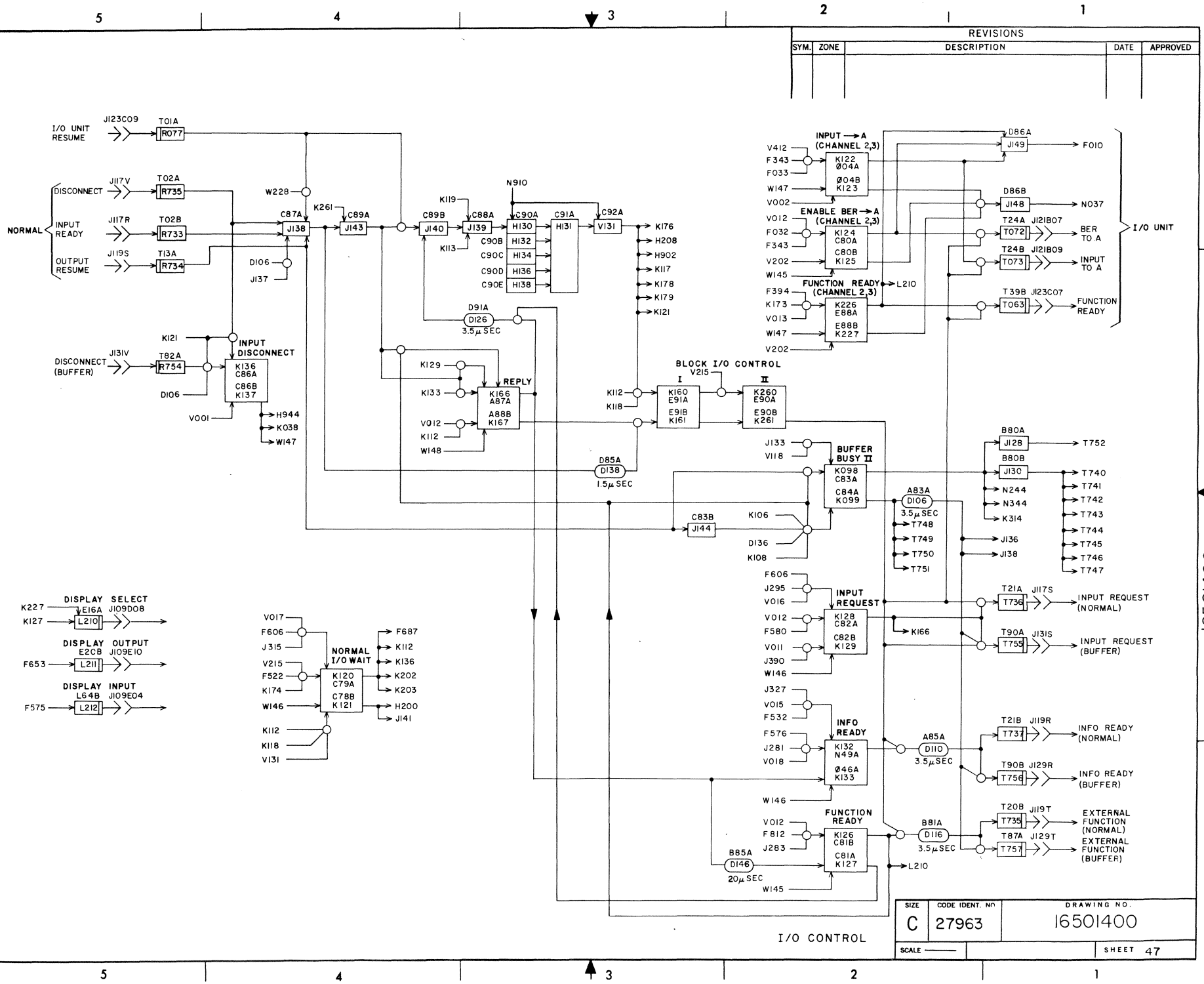


Y DRIVE

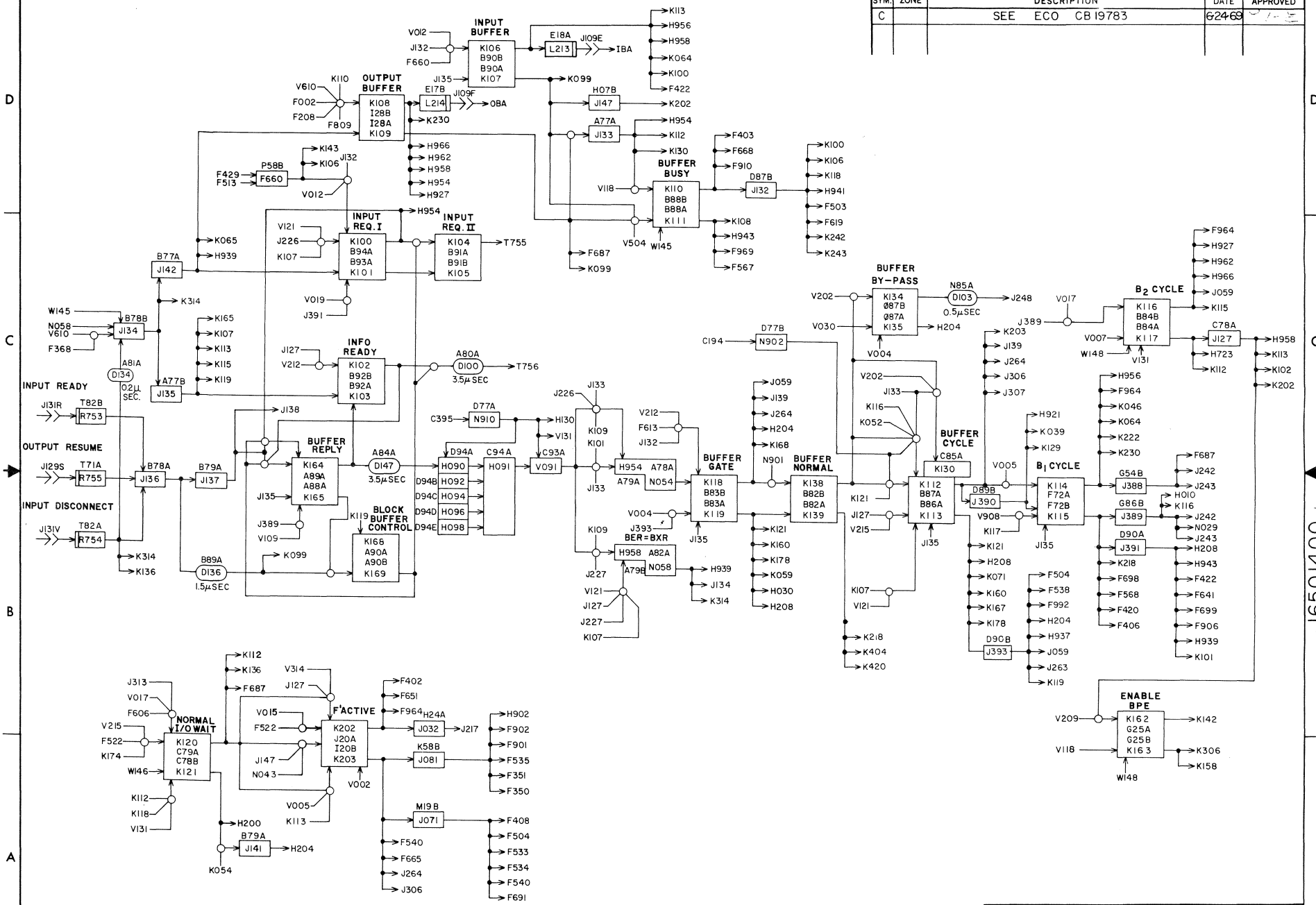
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

CODE IDENT NO.	SIZE	DRAWING
27963	C	16501400
SCALE		SHEET 46

16501400
SHEET 46


REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
I/O UNIT RESUME
NORMAL
DISCONNECT
INPUT READY
OUTPUT RESUME
INPUT DISCONNECT
DISCONNECT (BUFFER)
REPLY
BLOCK I/O CONTROL
BUFFER BUSY II
INPUT REQUEST
INFO READY
FUNCTION READY
INPUT → A (CHANNEL 2,3)
ENABLE BER → A (CHANNEL 2,3)
FUNCTION READY (CHANNEL 2,3)
I/O UNIT
DISPLAY SELECT
DISPLAY OUTPUT
DISPLAY INPUT
NORMAL I/O WAIT
I/O CONTROL
SIZE C
CODE IDENT. NO 27963
DRAWING NO. 16501400
SCALE
SHEET 47
16501400 SHEET 47

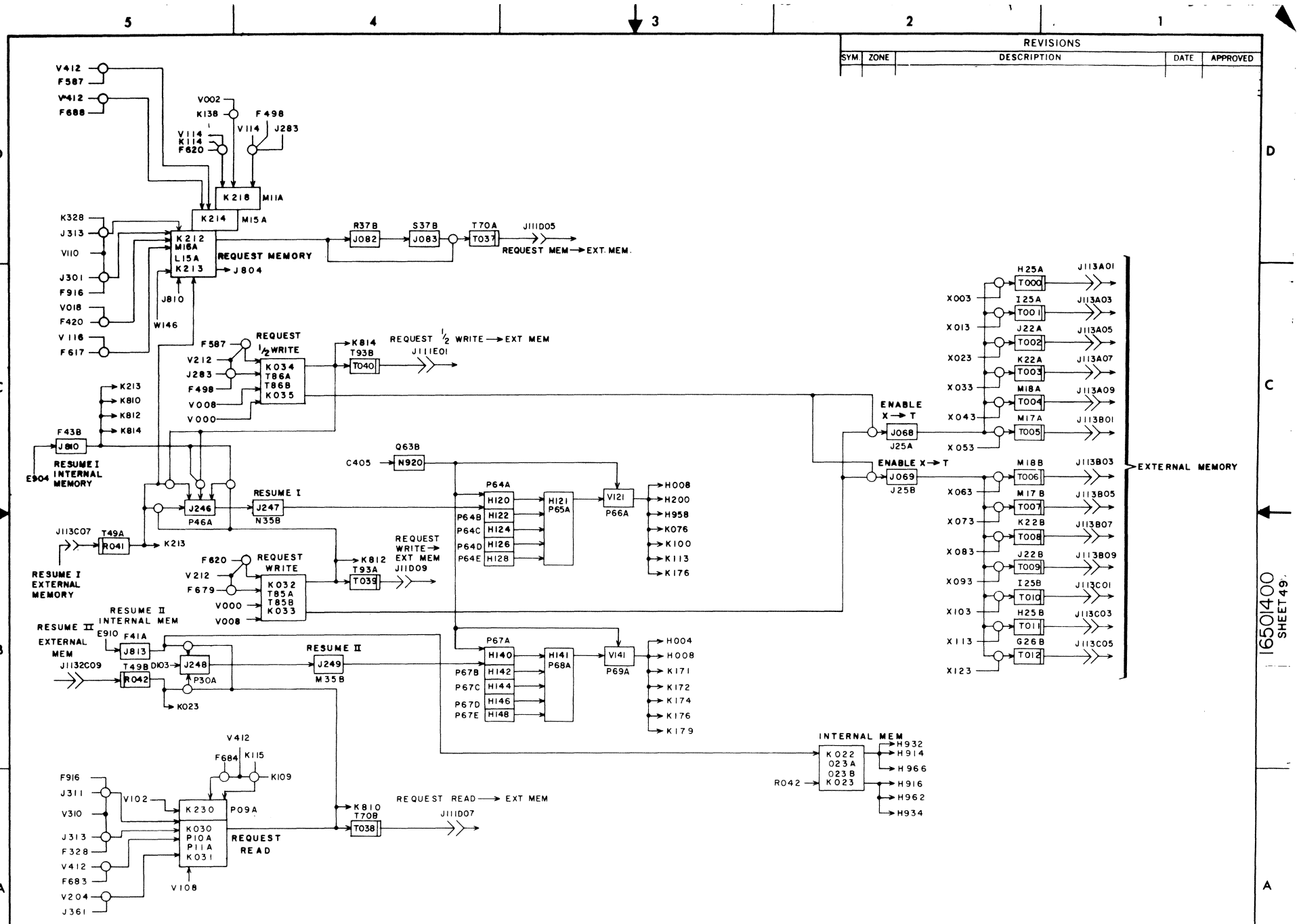
REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
C		SEE ECO CB19783	6-24-69	

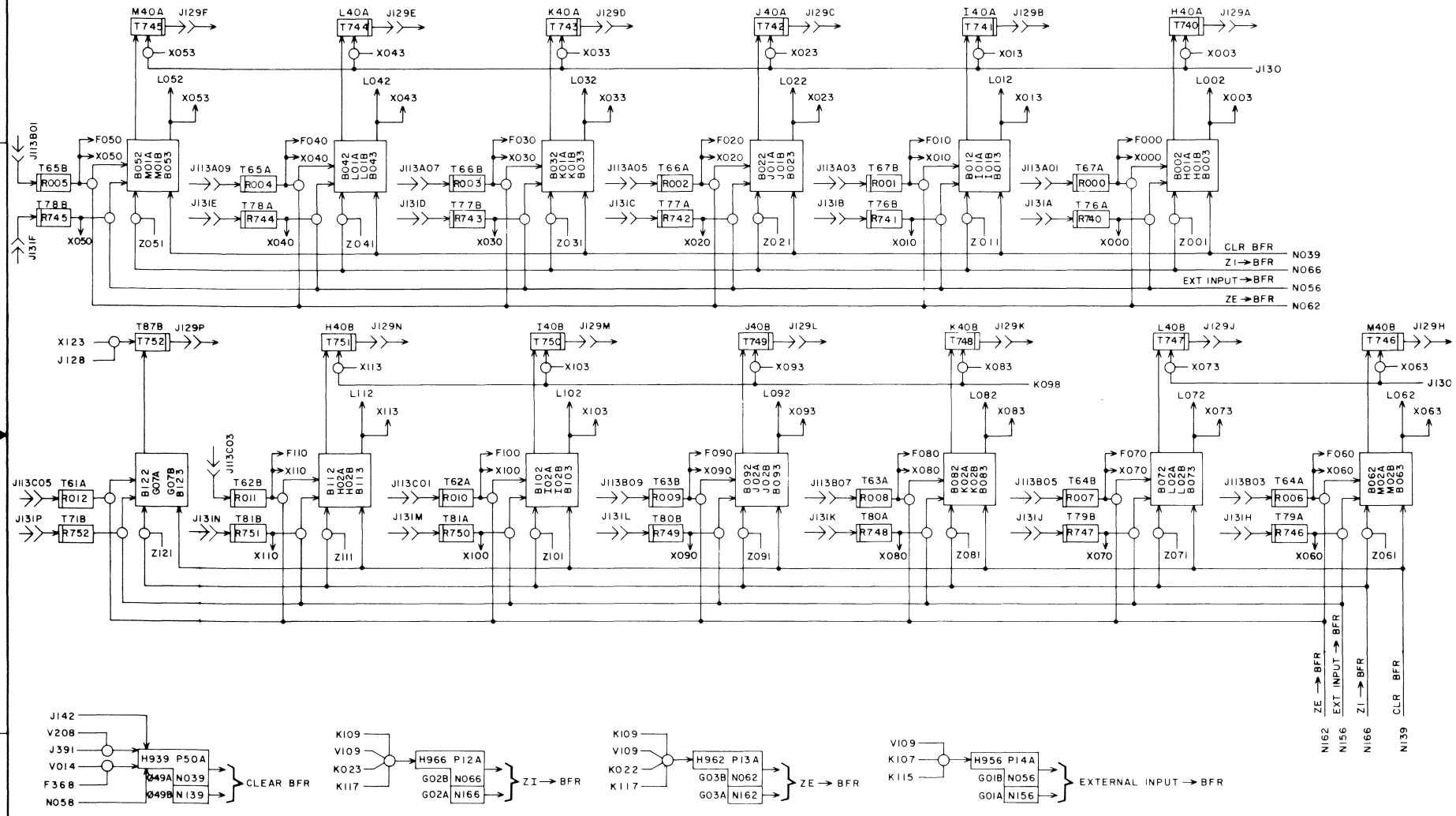


BUFFER CONTROL

SIZE	CODE IDENT. NO.	DRAWING NO.
C	27963	16501400
SCALE		SHEET 48

16501400 SHEET 48


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
REQUEST MEMORY
REQUEST MEM → EXT. MEM.
REQUEST ½ WRITE → EXT MEM
RESUME I INTERNAL MEMORY
RESUME I EXTERNAL MEMORY
RESUME II INTERNAL MEM
RESUME II EXTERNAL MEM
REQUEST WRITE → EXT MEM
REQUEST READ → EXT MEM
ENABLE X → T
ENABLE X → T
EXTERNAL MEMORY
INTERNAL MEM
EXTERNAL MEMORY CONTROL
CODE IDENT NO. 27963
SIZE C
DRAWING 16501400
SCALE
SHEET 49
16501400 SHEET 49



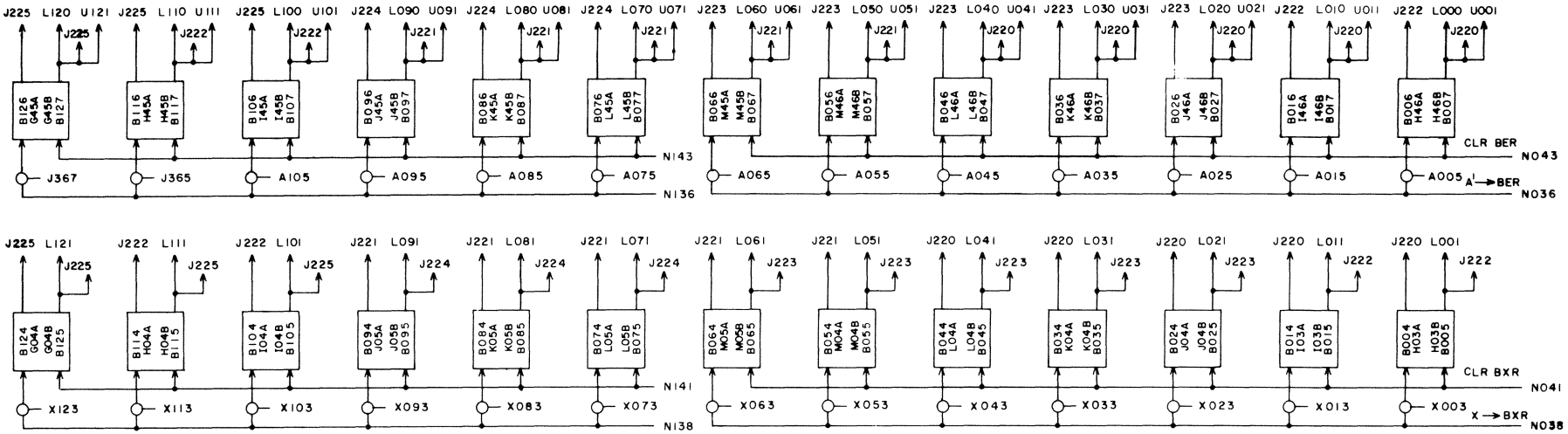
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

BFR REGISTER

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE —		SHEET 50

16501400 SHEET 50

REVISIONS				
S M	ZONE	DESCRIPTION	DATE	APPROVED



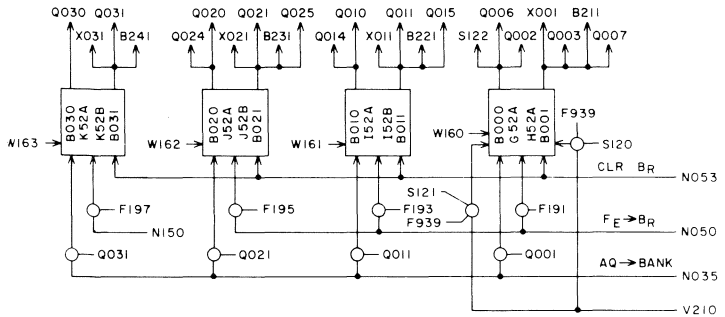
16501400
SHEET 51

BER REGISTER, BXR REGISTER, AND COMPARATOR

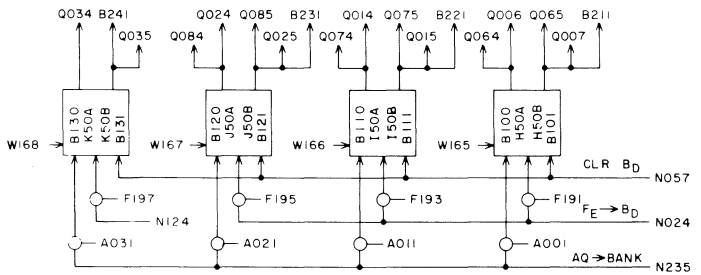
CODE IDENT NO.	SIZE	DRAWING NO.
27936	C	16501400
SCALE		SHEET 51

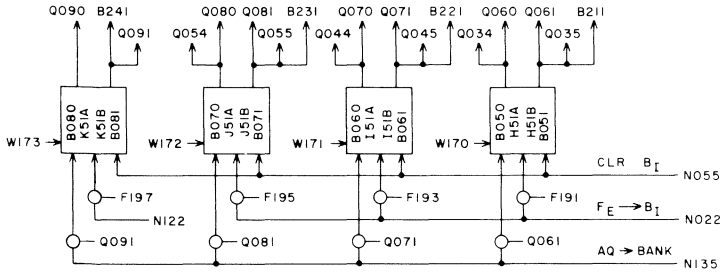
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

RELATIVE

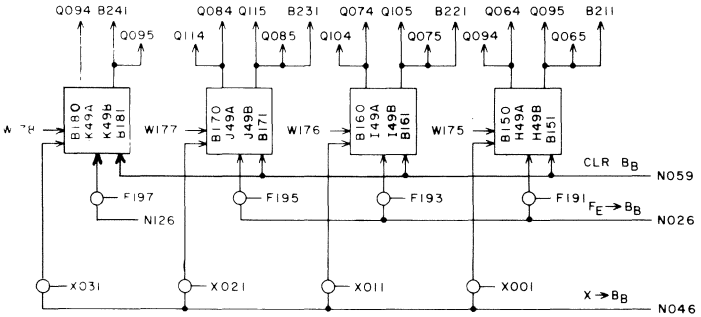


DIRECT

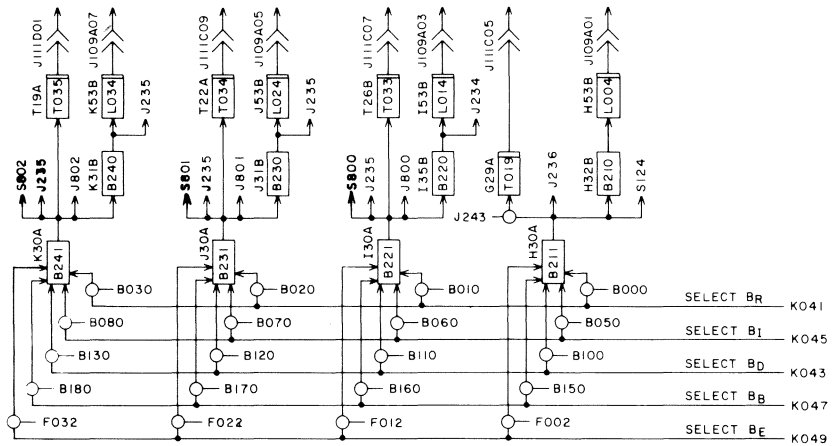




INDIRECT



BUFFER

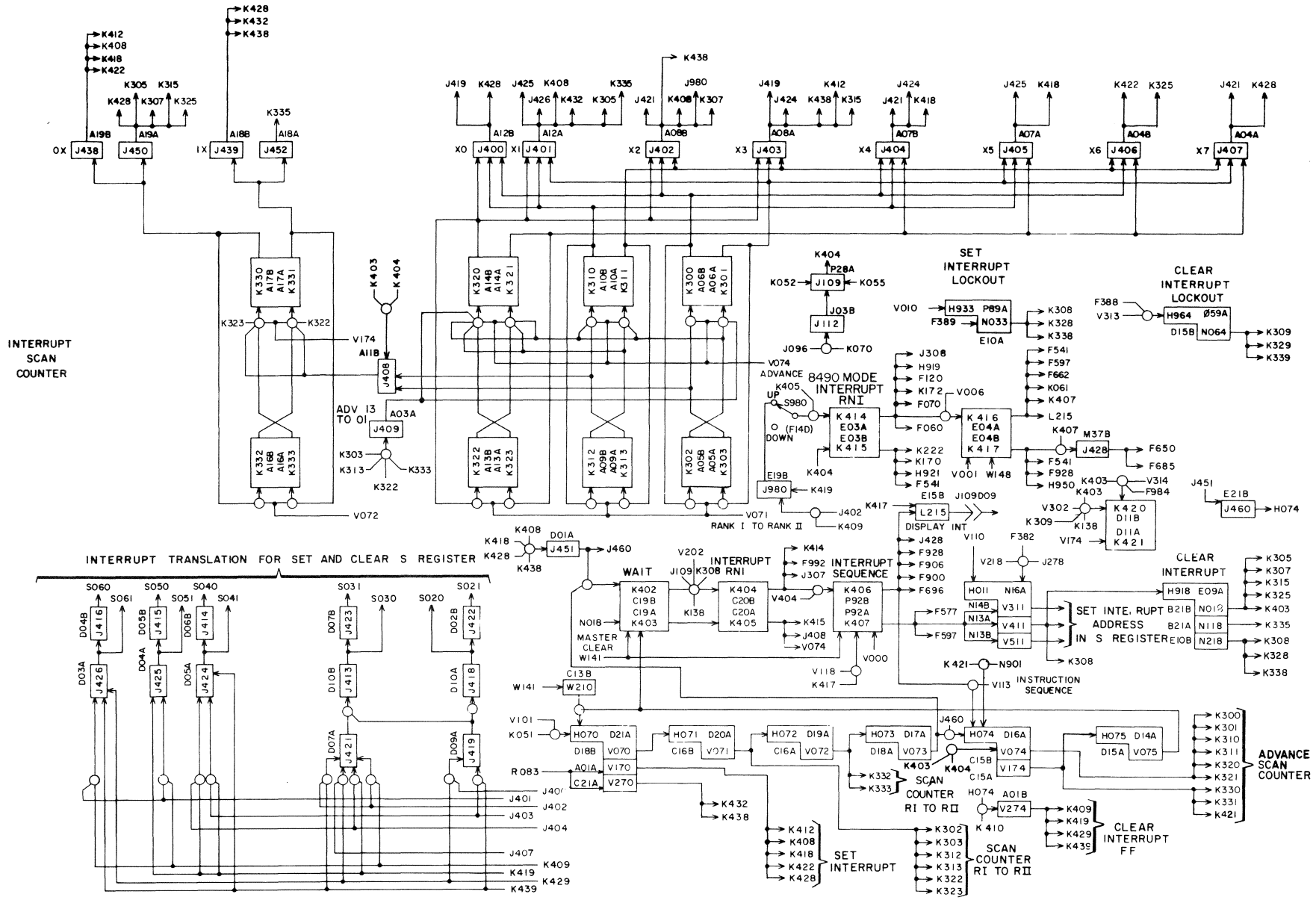


BANK CONTROL

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 52

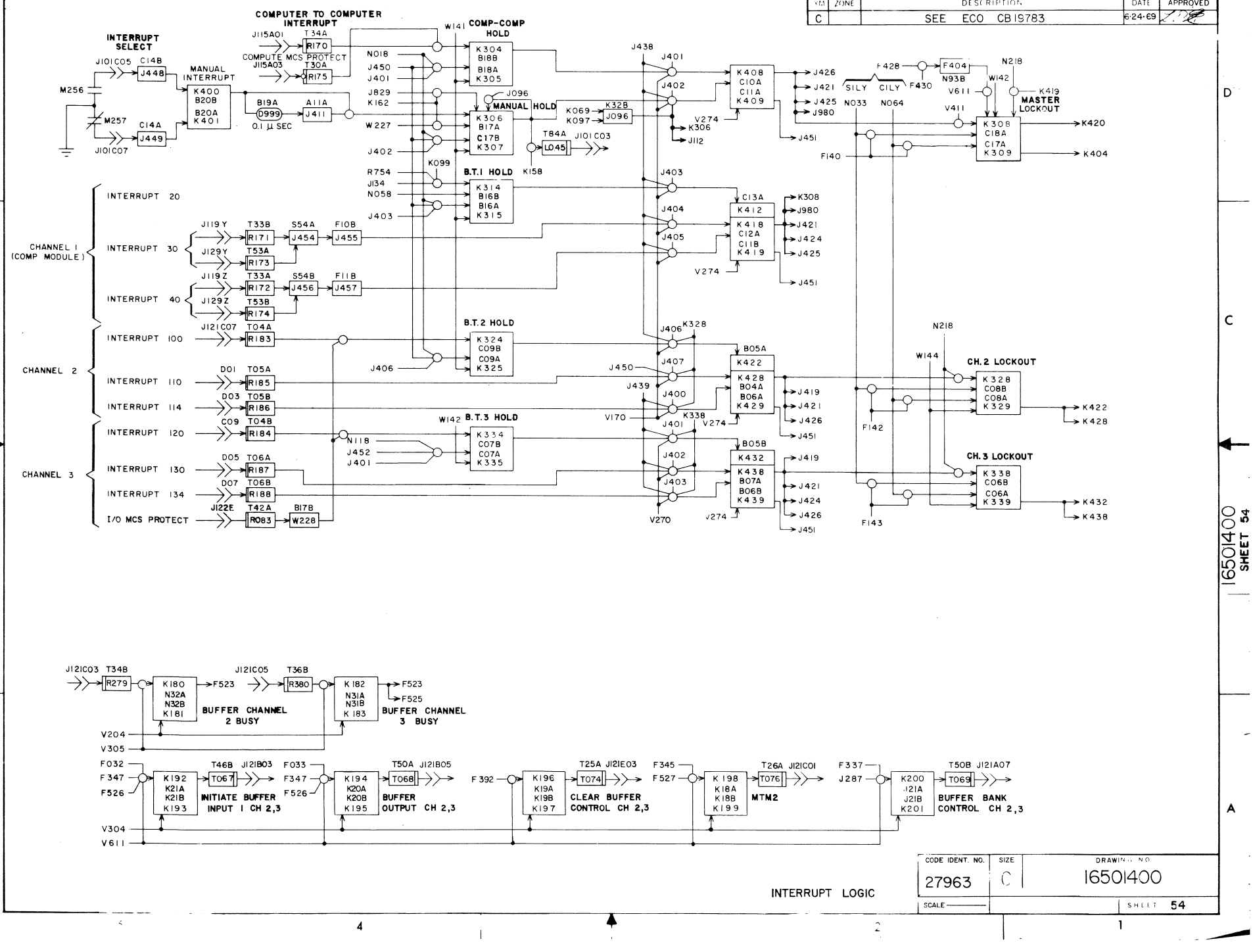
16501400 SHEET 52

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
C		SEE ECO CB19783		

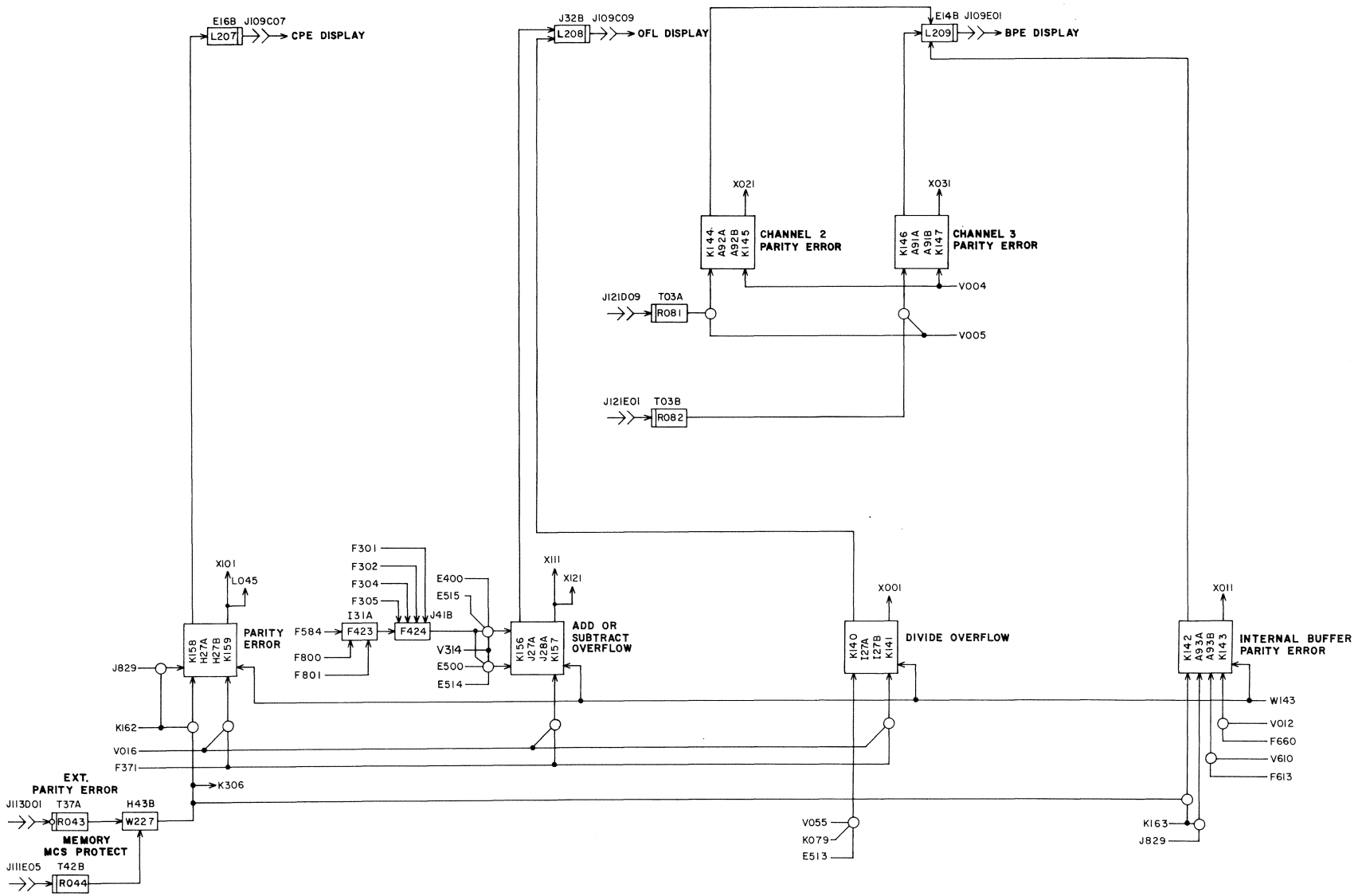


CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16501400
SCALE		SHEET 53

16501400 SHEET 53


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
C | | SEE ECO CB15783 | 6-24-69
INTERRUPT SELECT
COMPUTER TO COMPUTER INTERRUPT
COMPUTE MCS PROTECT
MANUAL INTERRUPT
0.1 μ SEC
COMP-COMP HOLD
MANUAL HOLD
B.T.1 HOLD
B.T.2 HOLD
B.T.3 HOLD
MASTER LOCKOUT
CH. 2 LOCKOUT
CH. 3 LOCKOUT
CHANNEL 1 (COMP MODULE)
CHANNEL 2
CHANNEL 3
INTERRUPT 20
INTERRUPT 30
INTERRUPT 40
INTERRUPT 100
INTERRUPT 110
INTERRUPT 114
INTERRUPT 120
INTERRUPT 130
INTERRUPT 134
I/O MCS PROTECT
BUFFER CHANNEL 2 BUSY
BUFFER CHANNEL 3 BUSY
INITIATE BUFFER INPUT I CH 2,3
BUFFER OUTPUT CH 2,3
CLEAR BUFFER CONTROL CH 2,3
MTM2
BUFFER BANK CONTROL CH 2,3
INTERRUPT LOGIC
CODE IDENT. NO. 27963
SIZE C
DRAWING NO. 16501400
SCALE
SHEET 54
16501400 SHEET 54

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
D		SEE ECO CB19782	9-29	

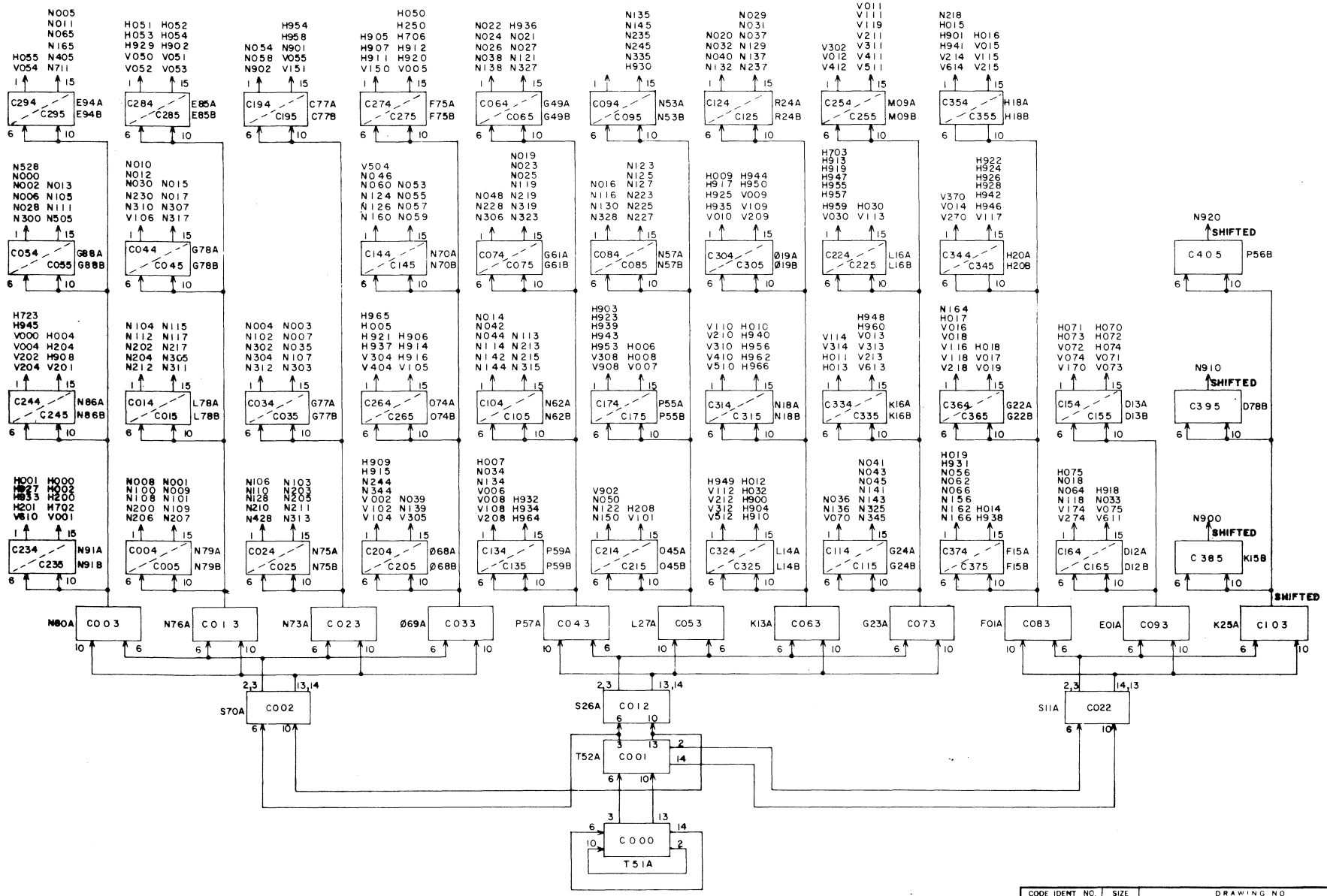


ERROR REGISTER

SIZE	CODE IDENT. NO.	DRAWING NO.
C	27963	16501400
SCALE —		SHEET 55

16501400 SHEET 55

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



MASTER CLOCK

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16501400
SCALE ——		SHEET 56

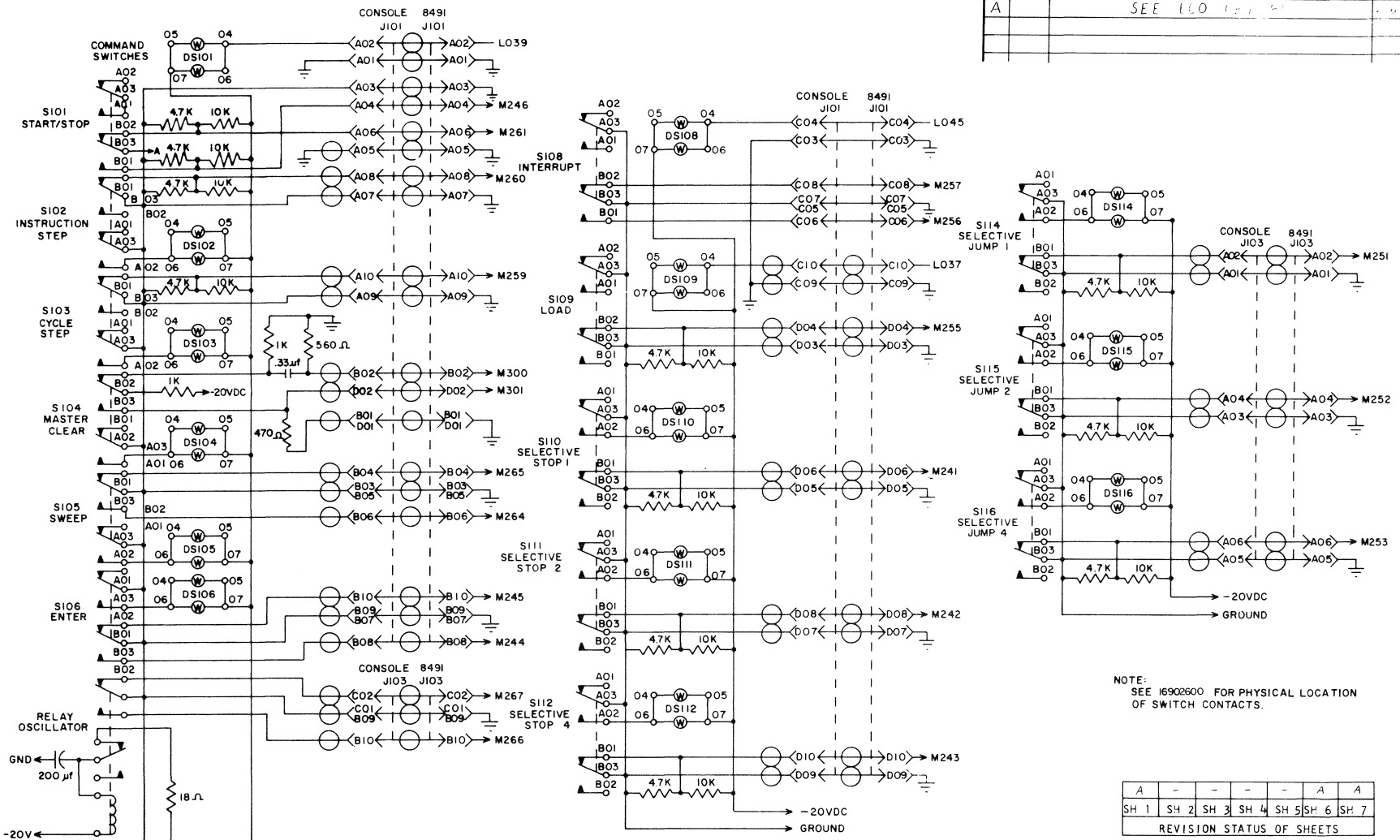
16501400 SHEET 56

SECTION 1

COMPUTE UNIT

CONSOLE SCHEMATICS

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		SEE ECO [illegible]	[illegible]	[illegible]



NOTE:
SEE 16902600 FOR PHYSICAL LOCATION OF SWITCH CONTACTS.

A	-	-	-	-	A	A
SH 1	SH 2	SH 3	SH 4	SH 5	SH 6	SH 7
REVISION STATUS OF SHEETS						

16903600 SHEET 1 OF 7

8490	
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES ON
FRACTIONS ± — DECIMALS ± — ANGLES ± —
DO NOT SCALE DRAWING
MATERIAL

CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA

CONTRACT		
APPROVED	D. C. [illegible] ET	5-5-67
ENGINEER	E. M. Noe	5-5-67
CHECKED	J. Jannigan	5-2-67
DRAWN	R. Boyle	4-10-67
APPROVED		
APPROVED		

TITLE
CONSOLE
ELECTRICAL SCHEMATIC DIAGRAM

CODE IDENT	SIZE	DRAWING NO.
09639	C	16903600
SCALE —		SHEET 1 OF 7

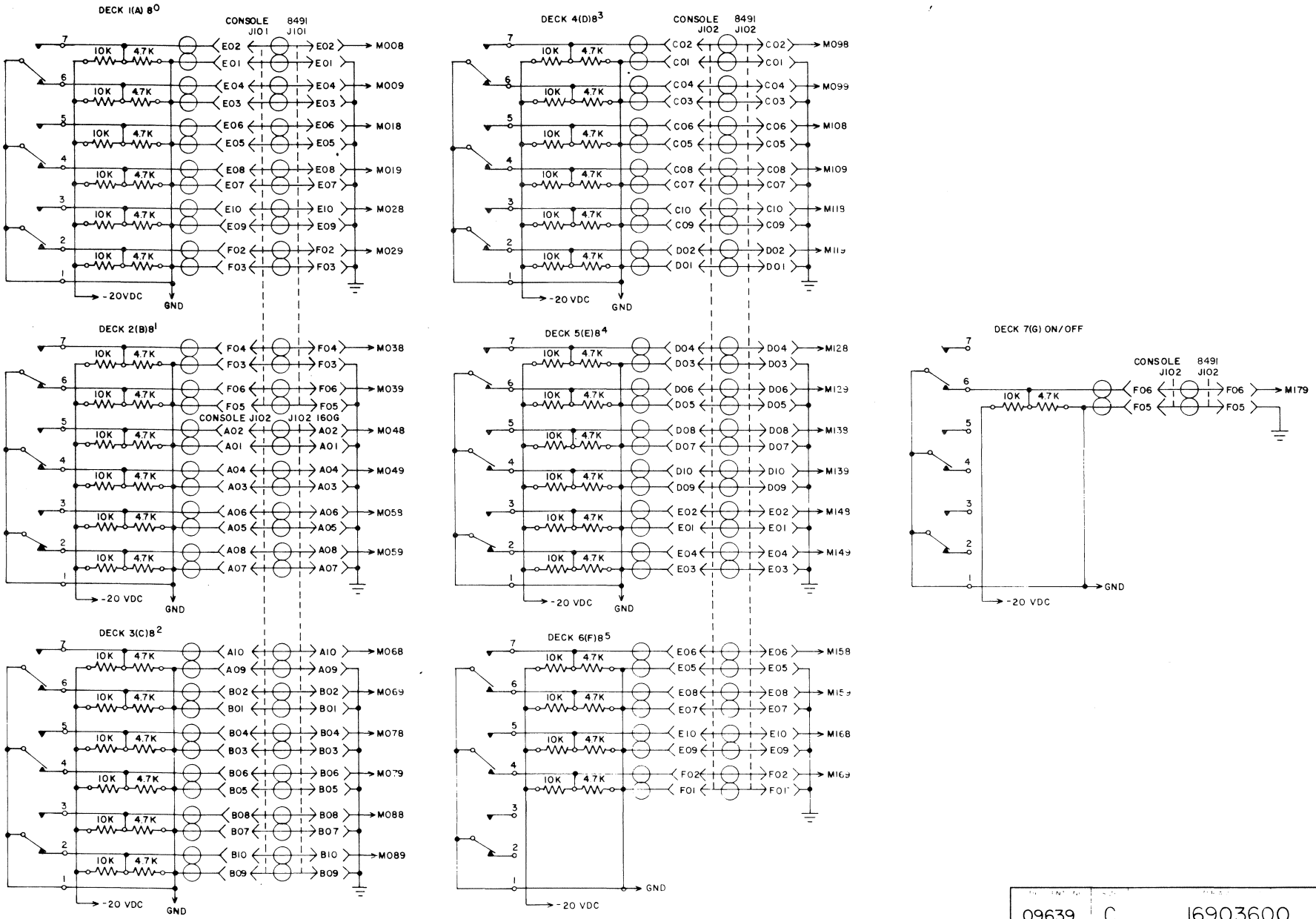
44 A 7491

NOTES:

DECKS 1 THROUGH 6 SHOWN FOR POSITION "0"
DECK 7 SHOWN FOR "OFF"

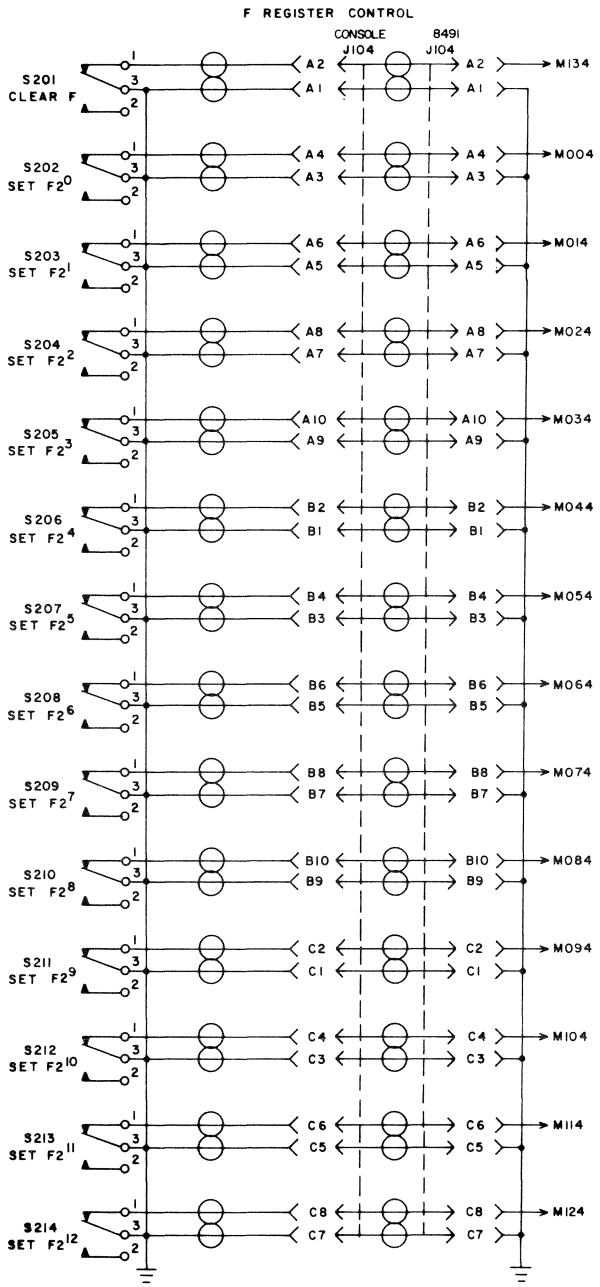
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

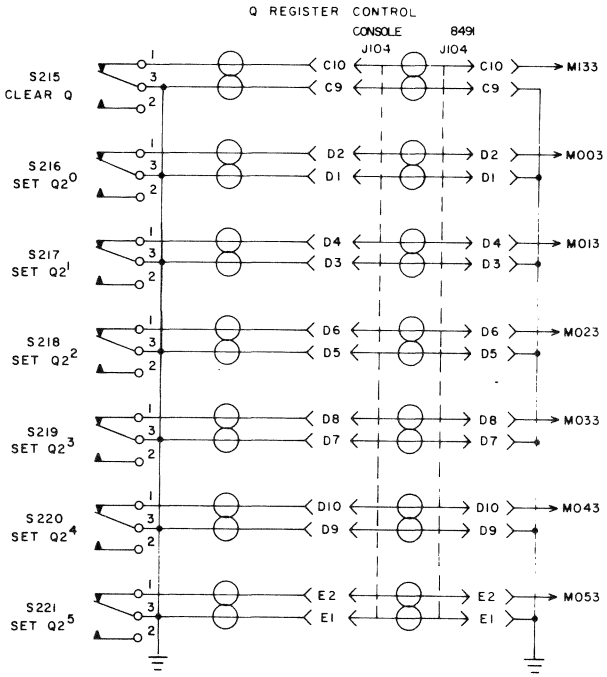
S113 BREAKPOINT SWITCH

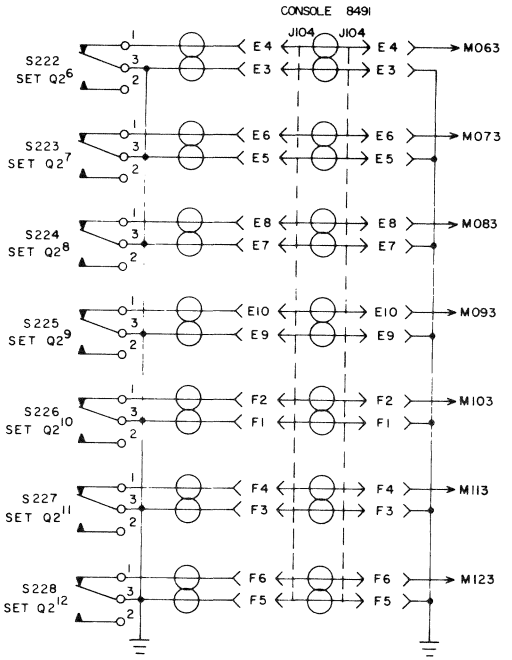


16903600
SHEET 2

09639	C	16903600	
—			2







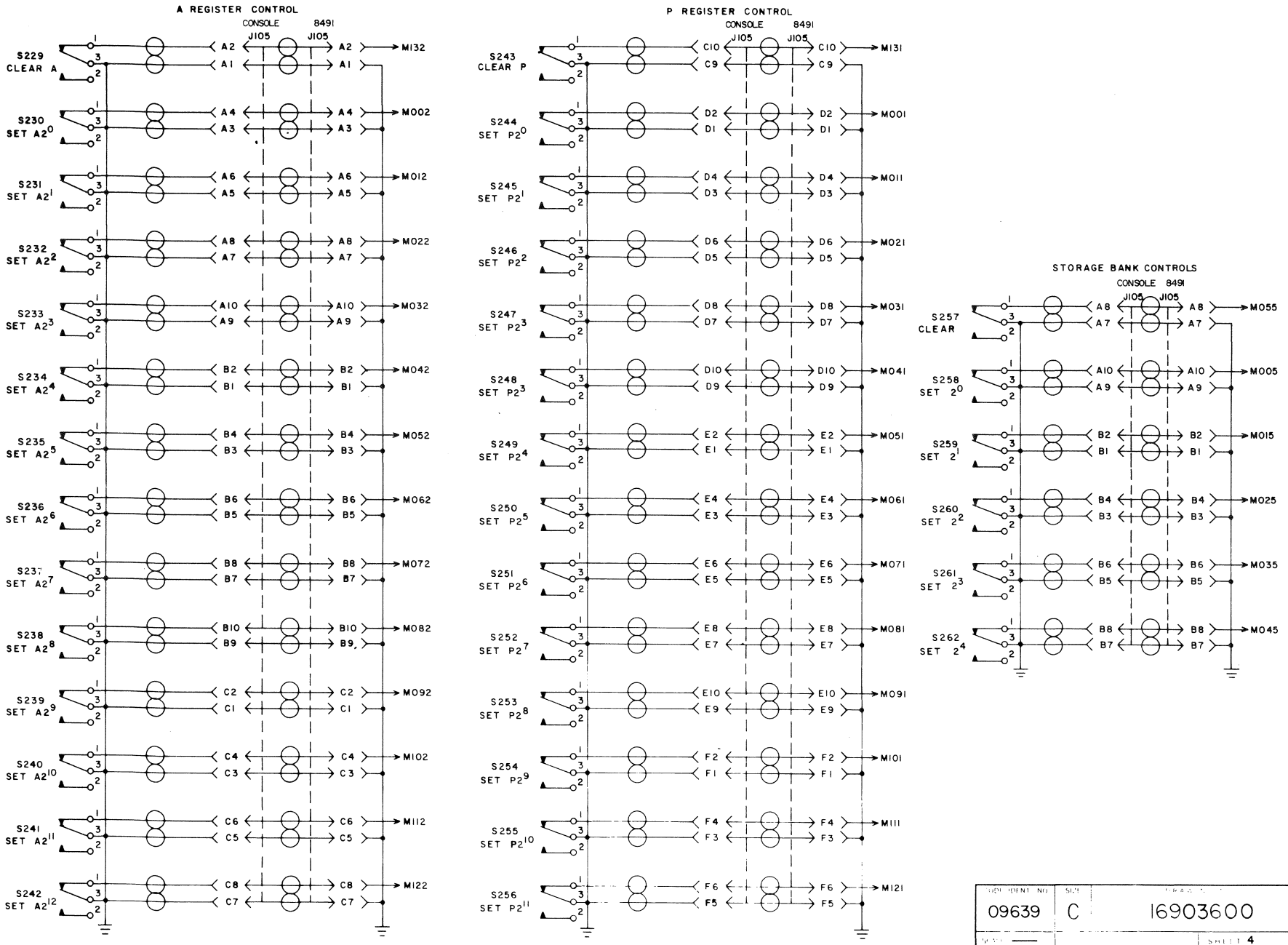
REVISIONS

SYM	ZONE	DESCRIPTION	DATE	APPROVED

16903600
SHEET 3

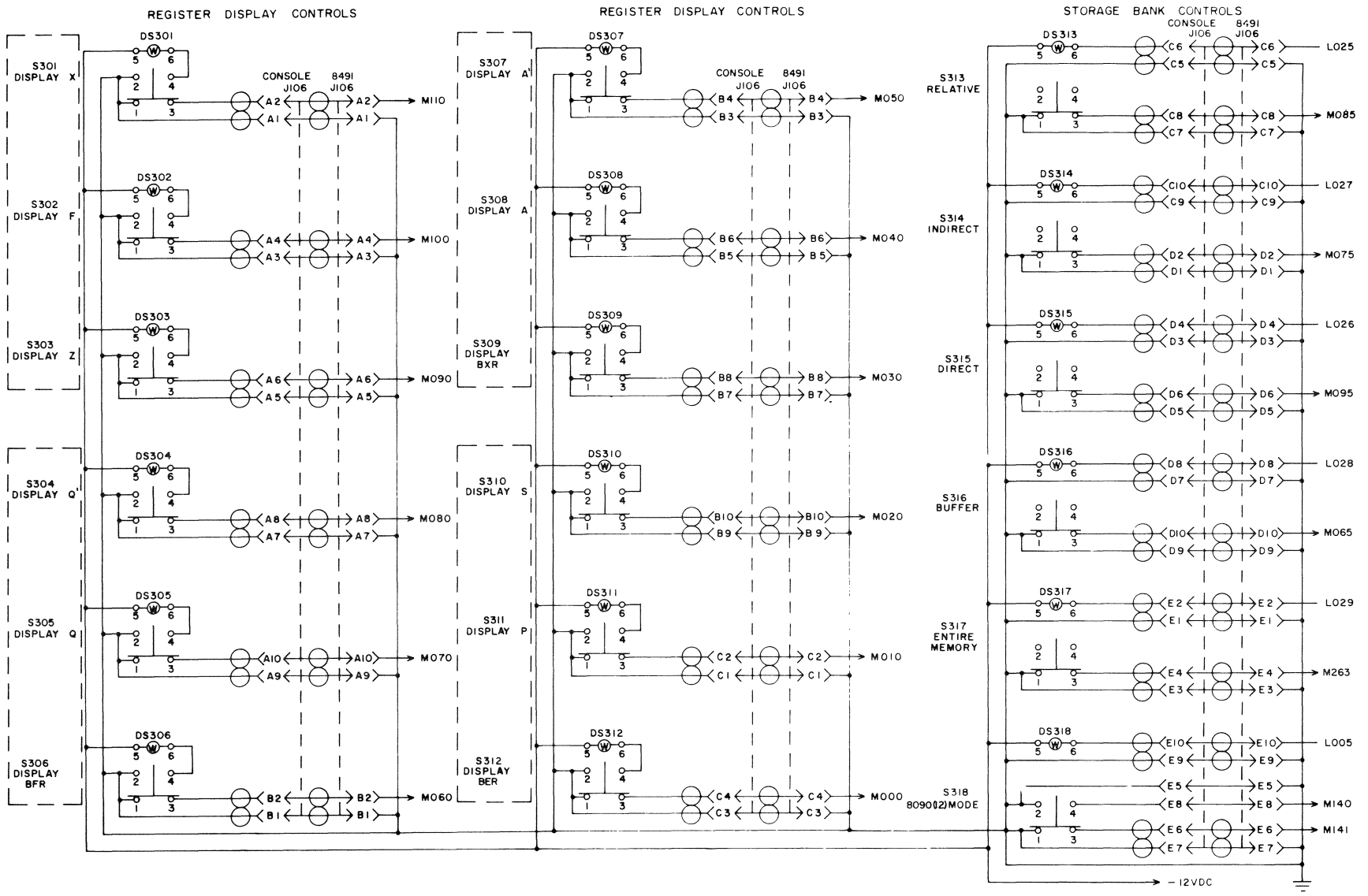
DOCUMENT NO.	SIZE	
09639	C	16903600
DATE		SHEET 3

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



DOCUMENT NO.	SIZE	DRAWING NO.
09639	C	16903600
SCALE —		SHEET 4

16903600 SHEET 4



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09639	C	16903600
SCALE		SHEET 5

16903600
SHEET 5

REVISIONS				
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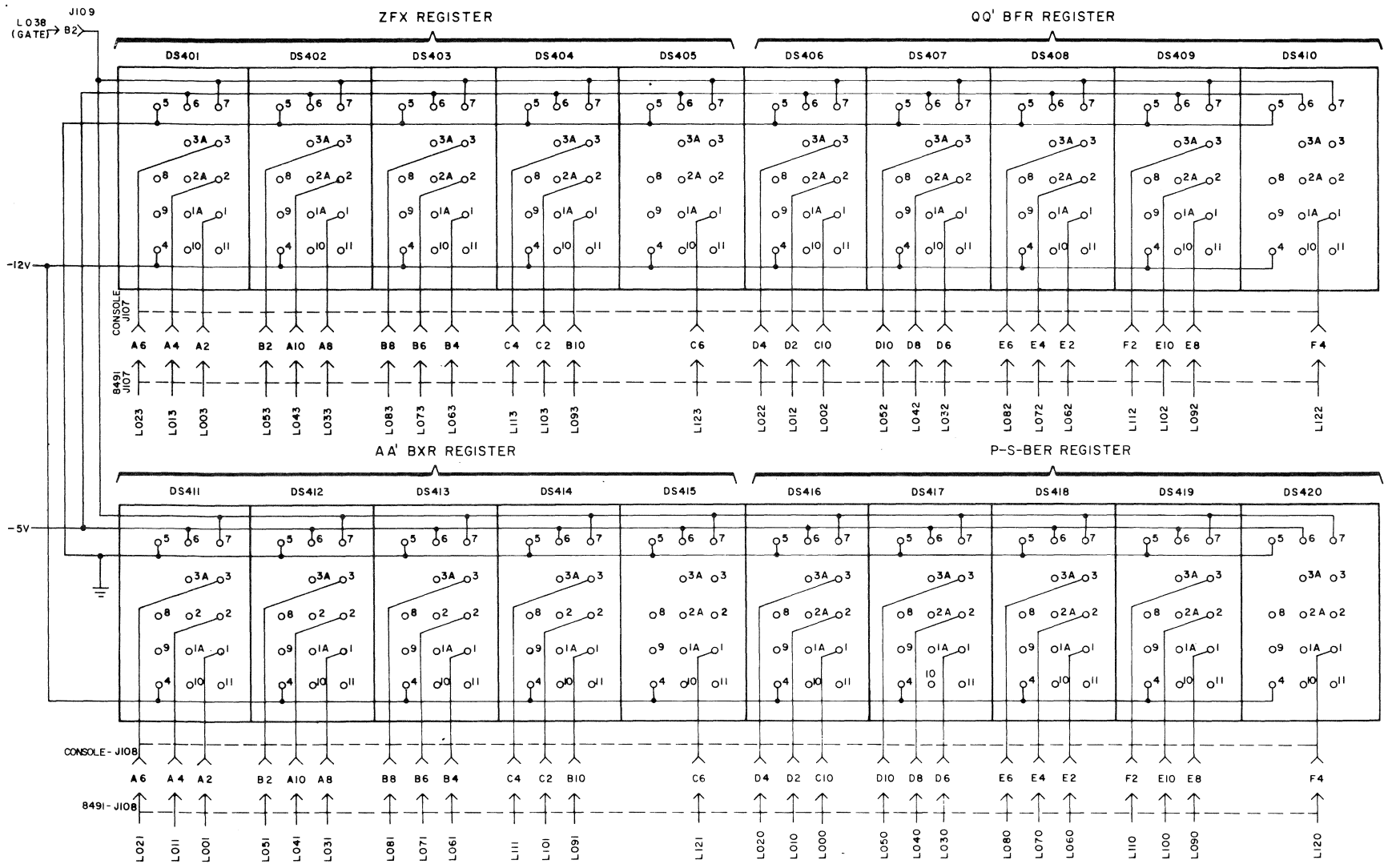

NOTE: SEE DWG. 24555600 ELECTRICAL SCHEMATIC OF LIGHT MODULES SHOWN ON THIS SHEET.

16903600 SHEET 6

CODE IDENT NO.	SIZE	DRAWING NO.
09639	C	16903600
SCALE —		SHEET 6

NOTE: FOR ELECTRICAL SCHEMATIC OF LIGHT MODULES DS421 AND DS422 SEE DWG. 24555600 FOR ELECTRICAL SCHEMATIC OF LIGHT MODULES DS423, DS424, DS425, AND DS426 SEE DWG. 11166200

REVISIONS				
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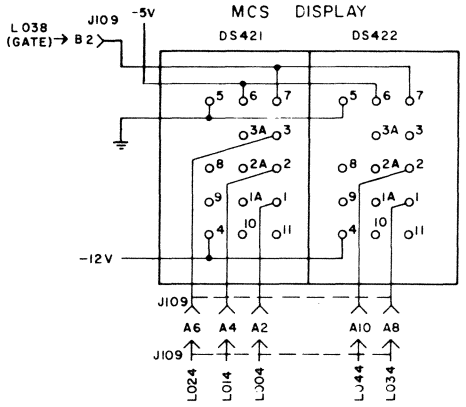
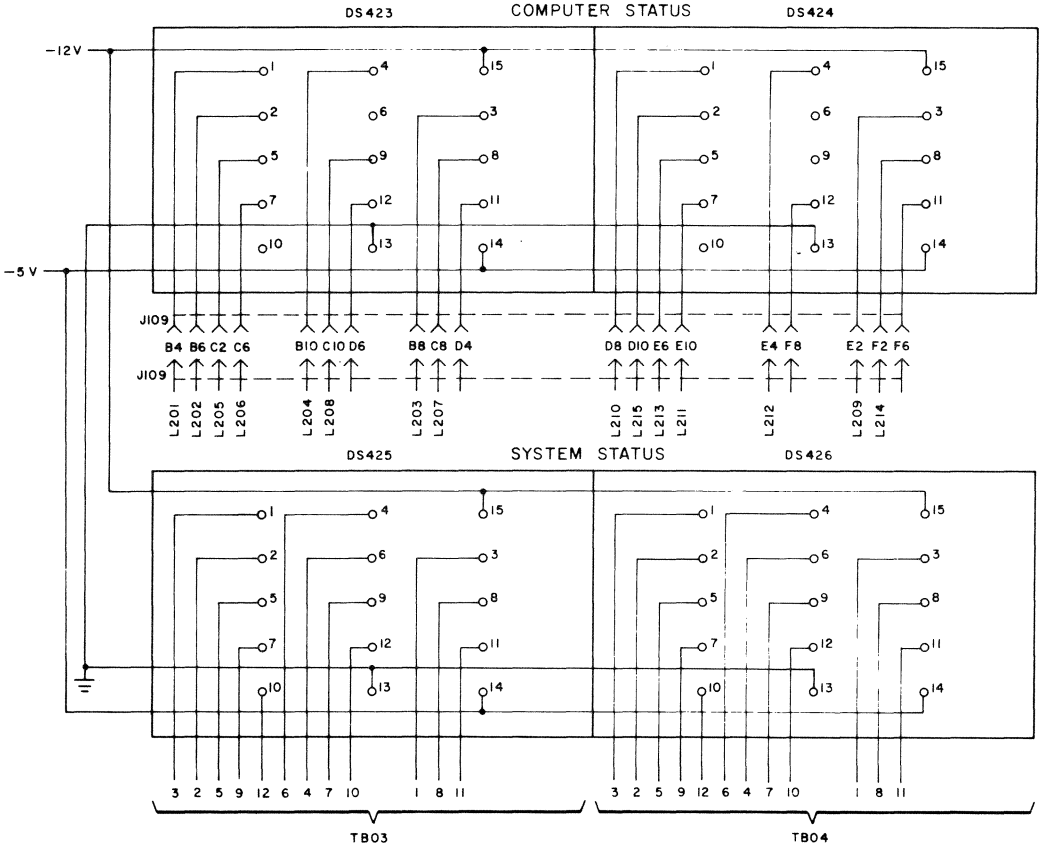




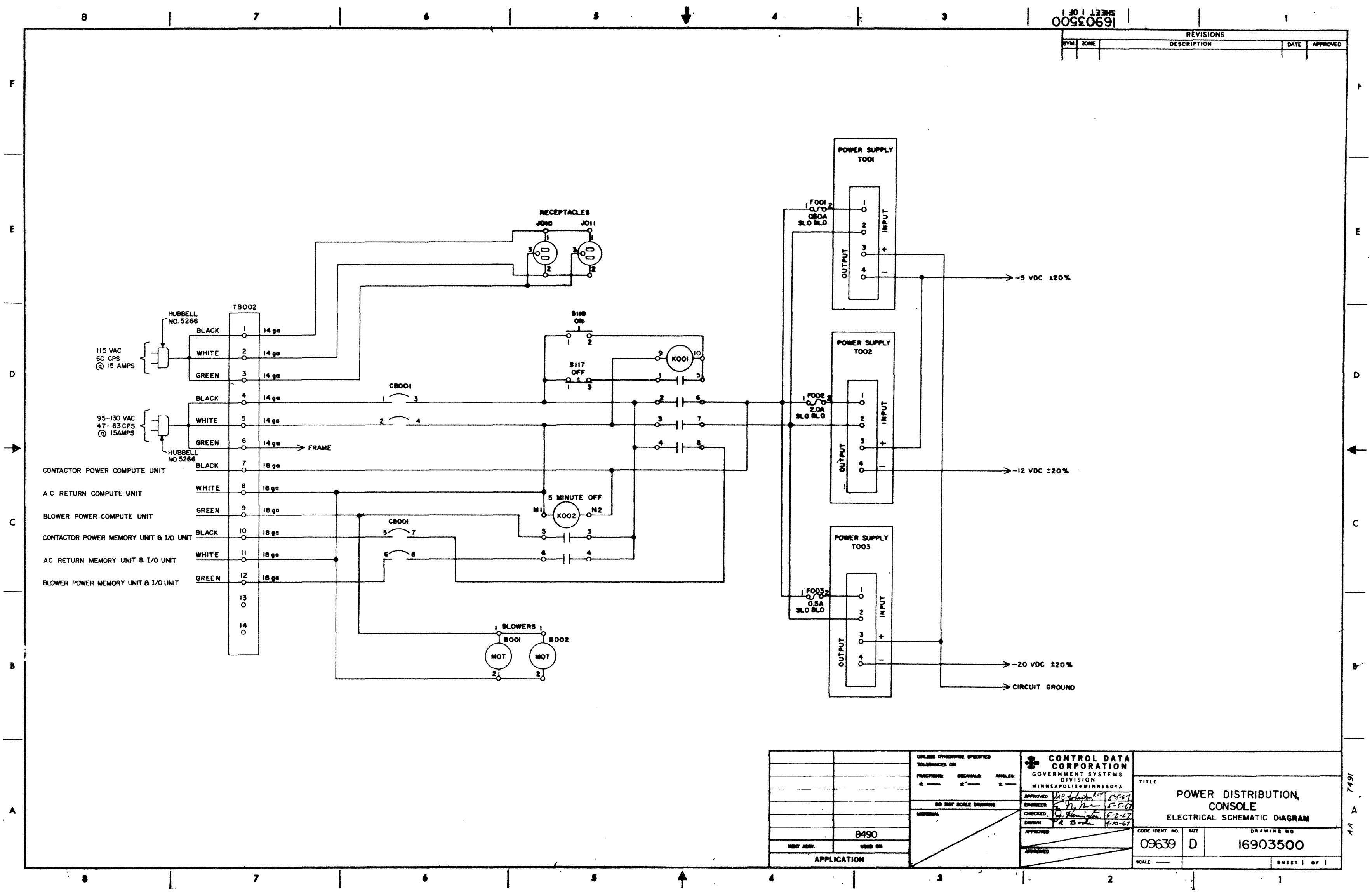
16903600
SHEET 7

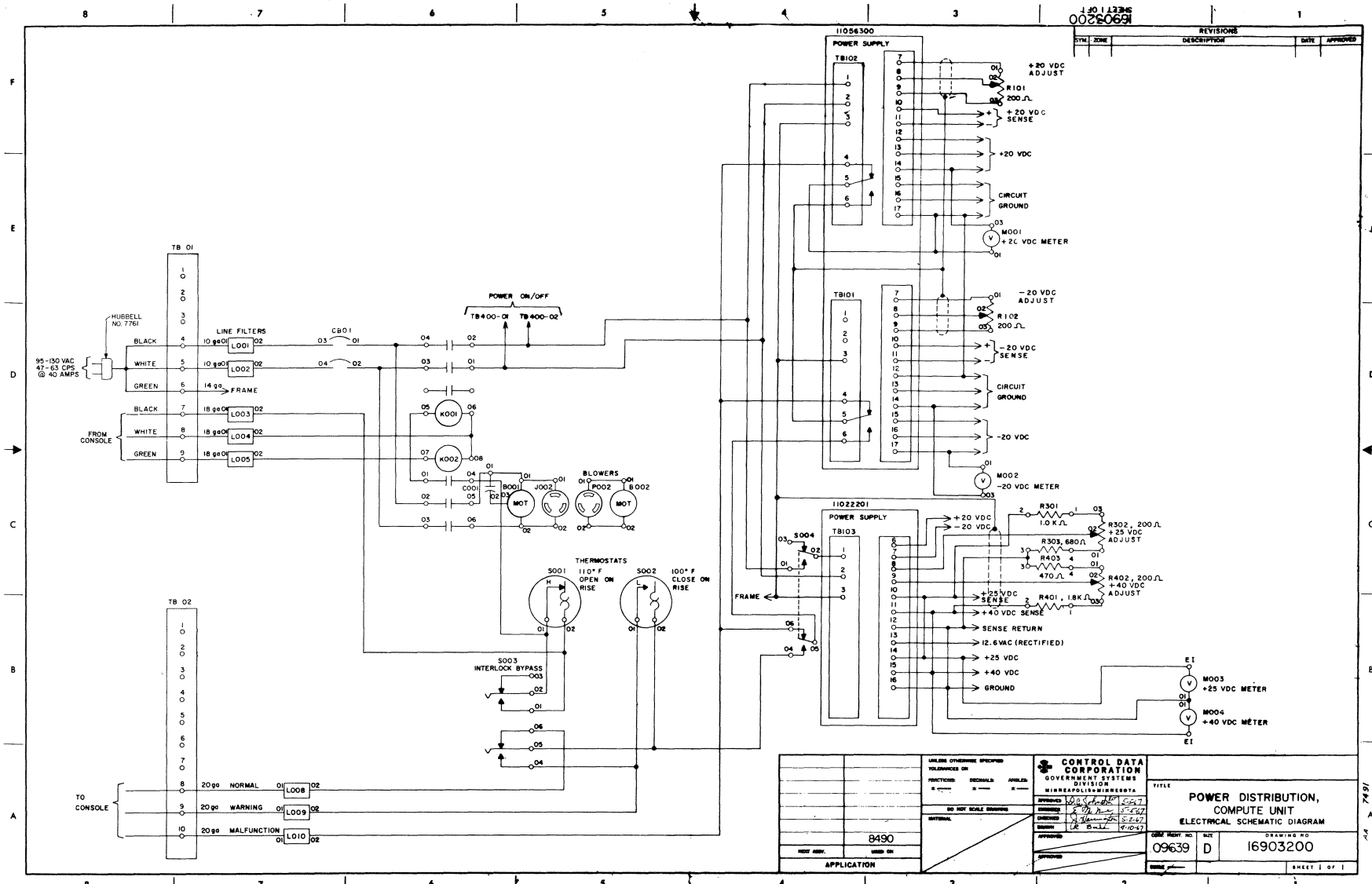
CODE IDENT. NO.	SIZE	DRAWING NO.
09639	C	16903600
SCALE ——		SHEET 7

SECTION 1

COMPUTE UNIT

POWER DISTRIBUTION AND MCS PROTECTION DRAWINGS

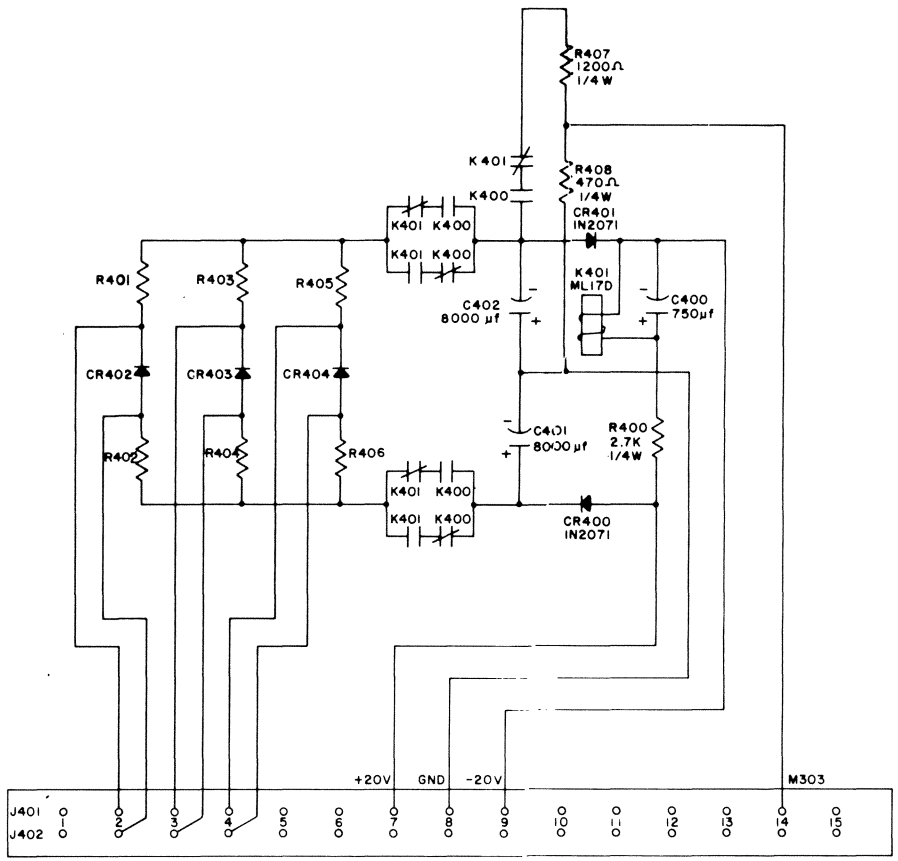

16903500 SHEET 1 OF 1
REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
RECEPTACLES
J010 J011
HUBBELL NO. 5266
TB002
115 VAC 60 CPS @ 15 AMPS
95-130 VAC 47-63 CPS @ 15AMPS
BLACK
WHITE
GREEN
14 ga
18 ga
FRAME
CONTACTOR POWER COMPUTE UNIT
A C RETURN COMPUTE UNIT
BLOWER POWER COMPUTE UNIT
CONTACTOR POWER MEMORY UNIT & I/O UNIT
AC RETURN MEMORY UNIT & I/O UNIT
BLOWER POWER MEMORY UNIT & I/O UNIT
CB001
S118 ON
S117 OFF
K001
5 MINUTE OFF
K002
M1 M2
BLOWERS
B001 B002
MOT
POWER SUPPLY T001
POWER SUPPLY T002
POWER SUPPLY T003
F001 0.50A SLO BLO
F002 2.0A SLO BLO
F003 0.5A SLO BLO
INPUT
OUTPUT
-5 VDC ±20%
-12 VDC ±20%
-20 VDC ±20%
CIRCUIT GROUND
CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA
TITLE
POWER DISTRIBUTION, CONSOLE
ELECTRICAL SCHEMATIC DIAGRAM
APPROVED 5-5-67
ENGINEER 5-5-67
CHECKED 5-2-67
DRAWN R. Boeke 4-10-67
CODE IDENT NO. 09639
SIZE D
DRAWING NO. 16903500
SHEET 1 OF 1
8490
NEXT ASSY. USED ON
APPLICATION
DO NOT SCALE DRAWING

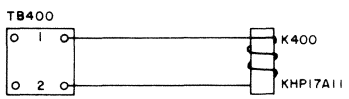

11056300
POWER SUPPLY
TB102
+20 VDC ADJUST
R101
200Ω
+20 VDC SENSE
+20 VDC
CIRCUIT GROUND
M001
+20 VDC METER
TB101
-20 VDC ADJUST
R102
200Ω
-20 VDC SENSE
CIRCUIT GROUND
-20 VDC
M002
-20 VDC METER
11022201
POWER SUPPLY
TB103
+20 VDC
-20 VDC
+25 VDC SENSE
+40 VDC SENSE
SENSE RETURN
12.6VAC (RECTIFIED)
+25 VDC
+40 VDC
GROUND
R301
1.0KΩ
R302, 200Ω
+25 VDC ADJUST
R303, 680Ω
R403
470Ω
R402, 200Ω
+40 VDC ADJUST
R401, 1.8KΩ
M003
+25 VDC METER
M004
+40 VDC METER
TB 01
HUBBELL NO. 7761
95-130 VAC 47-63 CPS @ 40 AMPS
BLACK
WHITE
GREEN
LINE FILTERS
L001
L002
FRAME
CB01
POWER ON/OFF
TB400-01
TB400-02
FROM CONSOLE
BLACK
WHITE
GREEN
K001
K002
C001
B001
J002
B002
P002
BLOWERS
MOT
TB 02
TO CONSOLE
20ga NORMAL
20ga WARNING
20ga MALFUNCTION
L008
L009
L010
S001
THERMOSTATS
110° F OPEN ON RISE
S002
100° F CLOSE ON RISE
S003
INTERLOCK BYPASS
S004
FRAME
REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA
TITLE
POWER DISTRIBUTION, COMPUTE UNIT
ELECTRICAL SCHEMATIC DIAGRAM
CODE IDENT. NO. 09639
SIZE D
DRAWING NO 16903200
SHEET 1 OF 1
8490
APPLICATION
DO NOT SCALE DRAWING

NOTES:

1. ALL DIODES ARE CONTROL DATA CORPORATION 1180200 UNLESS OTHERWISE SPECIFIED
2. ALL RESISTORS ARE 820 OHMS, 1/2 WATT, ±5% UNLESS OTHERWISE SPECIFIED

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED





		UNLESS OTHERWISE SPECIFIED TOLERANCES ON FRACTIONS ± — DECIMALS: ± — ANGLES ± —	CONTROL DATA CORPORATION GOVERNMENT SYSTEMS DIVISION MINNEAPOLIS • MINNESOTA
		DO NOT SCALE DRAWING	CONTRACT
		MATERIAL	APPROVED D.C. Zukaitis 5-2-67
			ENGINEER E.D. Nelson 5-2-67
			CHECKED J. Harrington 5-2-67
			DRAWN K. Bocka 4-10-67
			APPROVED
			APPROVED
NEXT ASSY	USED ON		
	8490		
APPLICATION			

TITLE: POWER ON/OFF, MCS PROTECTION, COMPUTE UNIT ELECTRICAL SCHEMATIC DIAGRAM

CODE IDENT NO.	SIZE	DRAWING NO.
09639	C	16902100

SCALE —— SHEET 1 OF 1

16902100 SHEET 1 OF 1

AA A 7491

SECTION 2

AUXILIARY MEMORY UNIT

THEORY OF OPERATION

SECTION 2

AUXILIARY MEMORY UNIT

GENERAL THEORY OF OPERATION

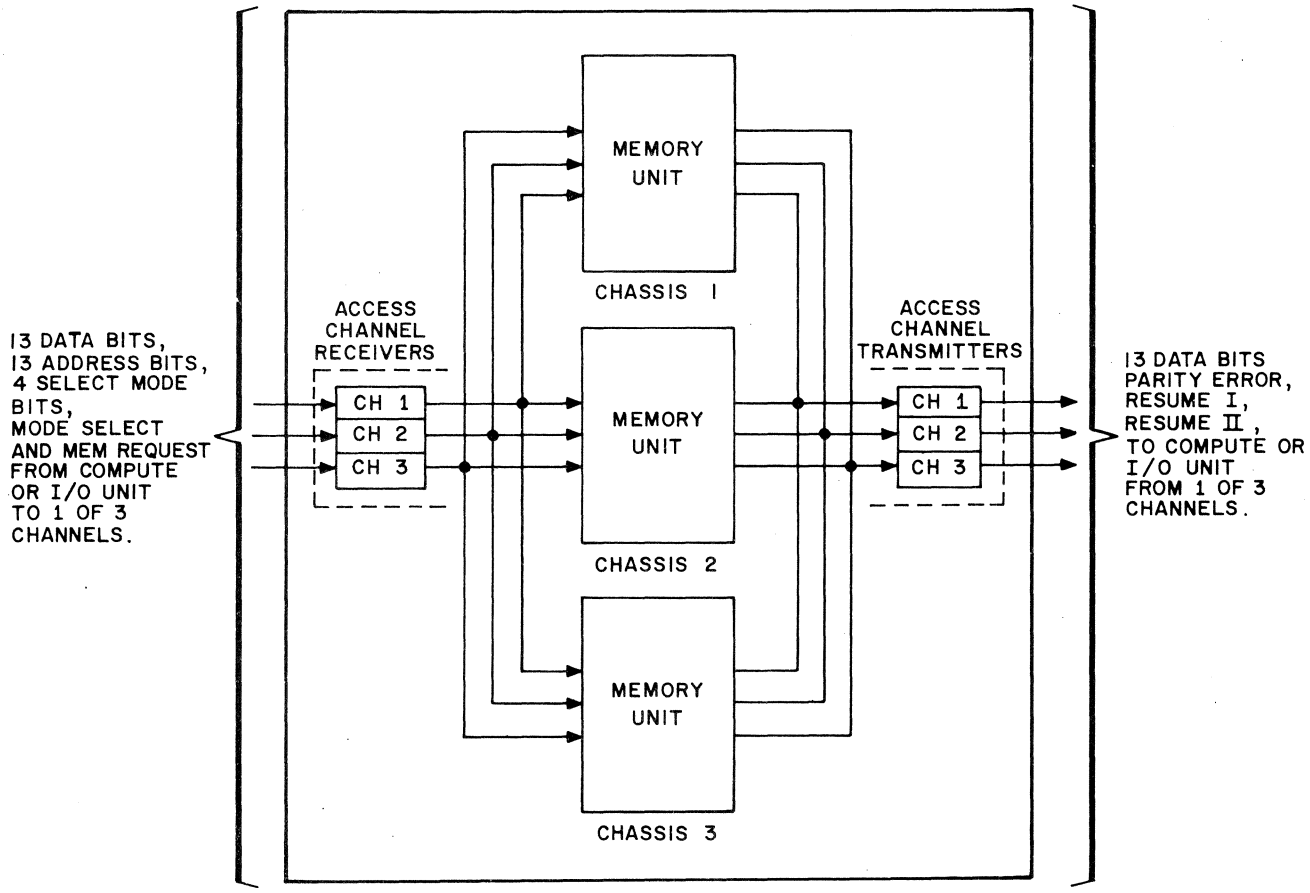
An Auxiliary Memory Unit contains from one to three memory banks dependent upon system application. A Memory Unit containing one memory bank is designated an 8492, a unit containing two memory banks is designated an 8493, and a unit containing three memory banks is designated an 8494. The 8496 and 8497 contain an I/O Unit and one and two memory banks respectively. A system using a minimum of external memory incorporates an 8492. A system using maximum external memory contains seven memory banks.

Memory banks within a unit share three access channel units to provide three channel (compute and/or I/O) access to any one Memory Unit, Figure 2-1. The access channel logic is common to three units; that is, the logic is distributed equally among the three units. In the case of one memory bank within a cabinet, the Memory Unit still receives access channel logic from each access channel unit, but the circuitry involved is at a minimum.

Each 8492 Memory Unit has a storage capacity of 8,192 14-bit words contained in two banks of 4,096 words each, Figure 2-2A. The storage function within a selected Memory Unit is controlled by a delay line for timing and a Z and S' register to directly effect a memory reference at a specific location, Figure 2-2B.

The selection of a specific bank in a Memory Unit is controlled by a Compute or I/O Unit. When a Memory Unit senses its own select code and a memory request from a Compute or I/O Unit, it performs a memory reference cycle. The time from first selection to completion of cycle requires about 1.35 microseconds. At the end of a cycle, the Memory Unit scans select codes and requests from other Compute or I/O Units in the system.

If its selection code and request for a memory reference are on the lines from other Compute or I/O Units, the Memory Unit processes each of the other references in turn before returning to the first Compute or I/O Unit for any subsequent references. This feature prevents one Compute or I/O Unit from monopolizing one Memory Unit.



NOTE:
THIS DIAGRAM IS A FUNCTIONAL ARRANGEMENT AND DOES NOT REPRESENT PHYSICAL ARRANGEMENT OF THE EQUIPMENT.

Figure 2-1. Functional Arrangement of Memory Units

The circuitry of the Compute or I/O Unit places a memory request, select code, read-write or partial-write command, and address signal on the lines of all Memory Units connected to this Compute Unit or I/O Unit. Each idle Memory Unit continuously scans its three access channels. When a Memory

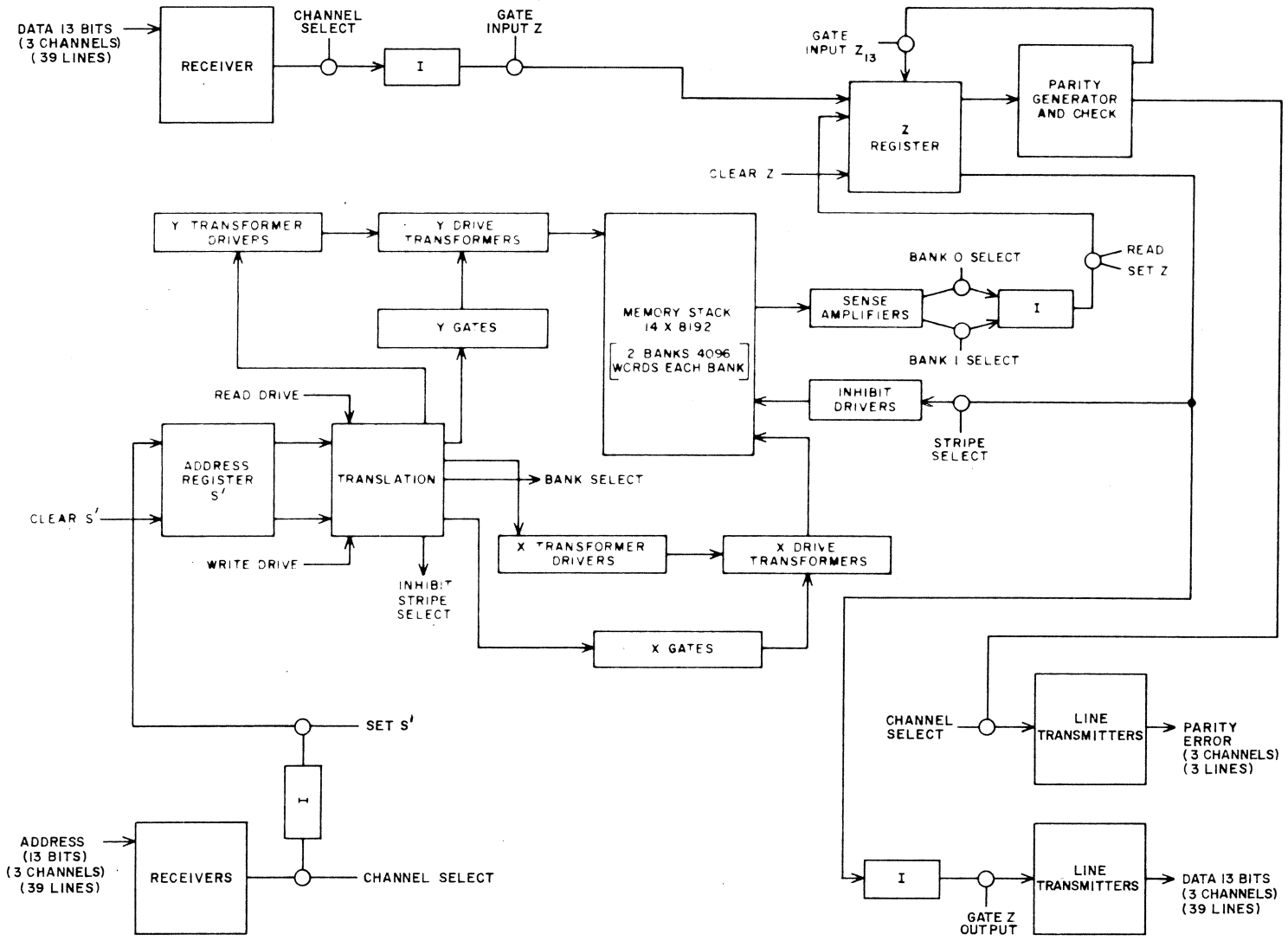


Figure 2-2A. 8492 Block Diagram (Memory)

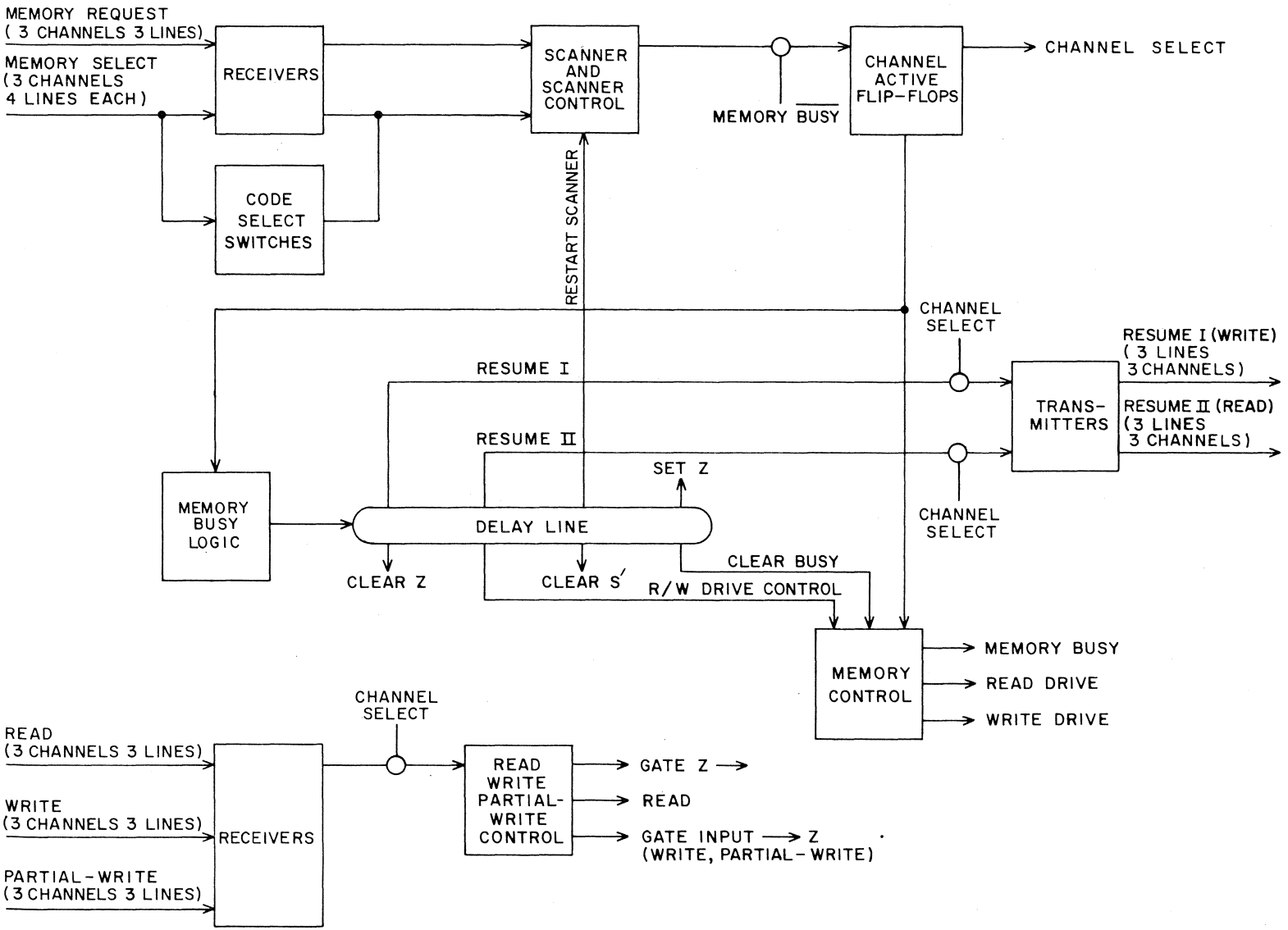


Figure 2-2B. 8492 Block Diagram (Control)

Unit senses its select code and a request on an access channel, the scanner in this Memory Unit stops. A busy flip-flop shuts out any interference from other access channels, and the read, write, or partial-write operation begins with the Compute or I/O Unit on the access channel selected by the scanner.

In the write mode, the Compute Unit or I/O Unit places data for a specific address on the interconnecting lines. When the write gate is activated, the data is transferred into the Z register of the Memory Unit that responded to the request selection at the start of the cycle.

In the read mode, the data from the memory address selected by the S' register appears on the outputs of the sense amplifiers during the read portion of the memory reference. (The sense amplifiers in the 8492 Memory Unit are identical to those in the internal memory of the 8491 Compute Unit. A functional analysis on this subject is provided in Section 1.) When the read transfer occurs, the data is transferred into the Z register of the Memory Unit. The output of the Memory Unit Z register is then gated to the Compute Unit or I/O Unit. The data word read out of memory during the read portion of the memory reference is restored in memory during the write portion of the memory reference cycle.

In the partial-write mode, both the read and write functions are used in one memory reference cycle. The upper seven bits of the 13-bit word operate in the read mode and the lower six bits of the 13-bit word operate in the write mode. The result is that the lower six bits of the word are changed in the partial-write mode while the upper seven bits are not affected.

During a program in the 8490, numerous references to various Memory Units occur. One memory is located within the Compute Unit that is performing computations. Additional external storage is provided by the 8492 Memory Units. A maximum of seven Memory Units may be used in any combination with one Compute Unit or one I/O Unit. A Memory Unit may be used by three different Compute or I/O Units.

The following control and data lines connect a Memory Unit to a Compute or I/O Unit:

Data transfer (3 channels, 13 lines each)

Bank selection and request (3 channels, 4 lines each)

Address selection (3 channels, 13 lines each)

Mode select (3 channels, 3 lines each)

Resume signals (3 channels, 2 lines each)

Master clear (3 channels, 1 line each)

Parity error (3 channels, 1 line each)

At the start of an external memory reference cycle, bank selection, memory request, mode command, address select and a data word (write operation only) are placed on the lines to the Memory Unit by the Compute or I/O Unit. The mode command for read, write, or partial-write sets the read, write, or partial-write flip-flop in the Memory Unit after that Memory Unit is selected.

DETAILED THEORY OF OPERATION

BANK AND MODE SELECTION

In the 8490 mode of operation, core storage within an Auxiliary Memory Unit is treated as one 8,192-word bank. The internal memory bank in the Compute Unit is usually designated as bank 0, and the banks in the Auxiliary Memory Units are designated with even numbers, 2 through 16_8 (2, 4, 6 through 16). In the 8090 mode, the core storage in each unit is treated as two 4,096-word banks. The internal memory in the Compute Unit is usually designated banks 0 and 1. These banks can be referenced only by the Compute Unit that contains them. The banks in the Auxiliary Memory Units are assigned unique numbers in the system (2 through 17_8 in pairs). Thus, one external memory bank would contain banks 2 and 3; another 4 and 5; etc. A number is assigned to a given unit by setting the bank selection switches in that unit. The highest order bit of the address word determines whether the odd or the even bank in a unit is referenced.

Whenever the correct select code and request appear on any of the three access channels to an idle Memory Unit, the scanner stops. The Compute or I/O Unit connected to that channel may then make one memory reference. If another Compute or I/O Unit connected to any other access channel generates a select code and request while the scanner is stopped, it could not interrupt the channel that first made the selection; but it would be selected when the scanner restarts. Since the scanner restarts from where it stopped on the last selected channel, the next-in-sequence channel would be selected.

The input circuits to the Memory Units from the selection lines consist of four receivers followed by four inverters. The inverters can be switched in or bypassed by a two-position switch associated with each inverter. The code to which a Memory Unit responds is determined by the setting of these coding switches. In one switch position, the input circuit uses a 1 to cause selection; in the other position, a 0 causes selection. Three of these switches in each of three channels are set to the select code, Figure 2-3.

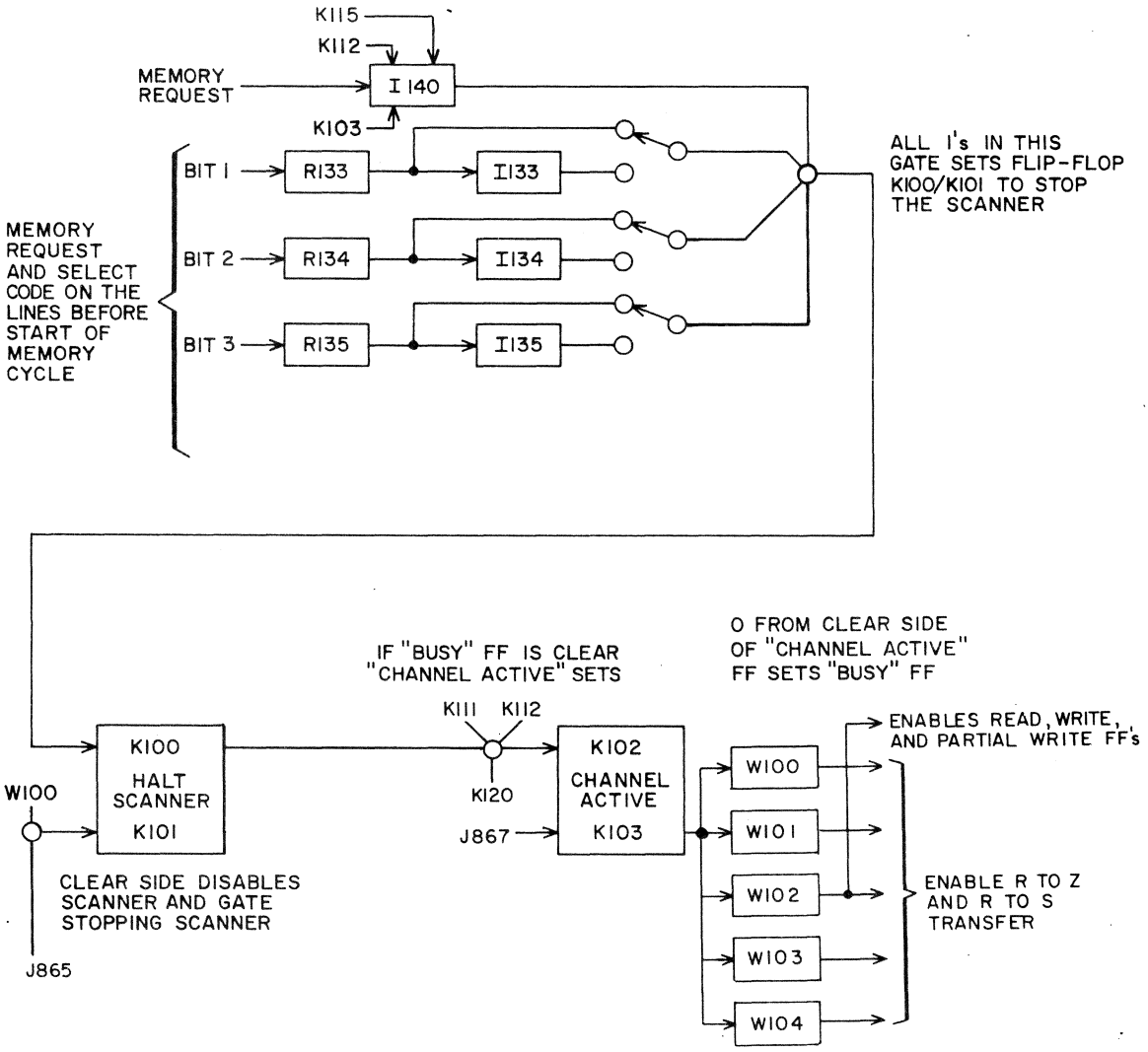
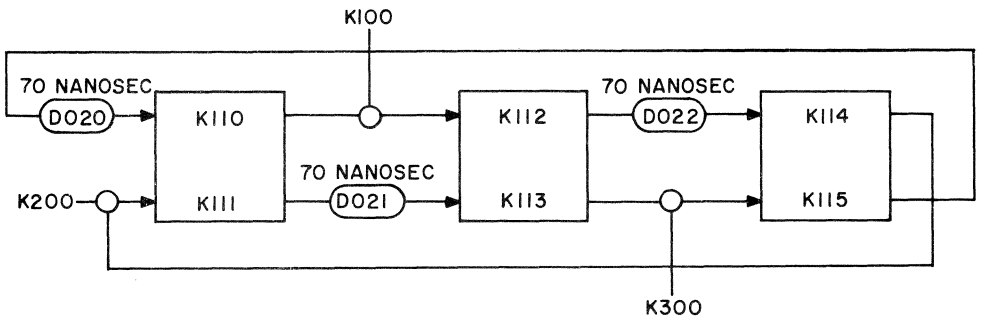


Figure 2-3. Typical Scanner Control Circuit

When the select code, request signal, and set output from the selected channel active flip-flop are received by an idle Memory Unit, the halt scanner flip-flop associated with the selected channel is set. The 0 output from the reset side of the halt scanner flip-flop blocks one of the AND gate inputs to either the set or clear side of one of the flip-flops in the scanner. Since the scanner is thereby unable to perform a set or clear function on this particular flip-flop, the scanner stops.

The scanner circuit is formed by connecting three flip-flops in a closed loop, Figure 2-4. The set output of the first flip-flop sets the second flip-flop and the set process continues sequentially until the third flip-flop is set. The set output of the third flip-flop is applied to the reset side of the first flip-flop. The reset output of the first flip-flop resets the second flip-flop and the reset process continues sequentially until the third flip-flop is reset. The reset

output of the third flip-flop sets the first flip-flop and the cycle repeats. This cycling goes on without interruption until a halt scanner flip-flop disables one of the scanner AND gates.



SCANNER SETS AND CLEARS UNINTERRUPTED UNTIL A SET OUTPUT OF A "HALT SCANNER" FF BLOCKS ONE OF THE INPUT AND GATES

Figure 2-4. Scanner Circuit

If the busy flip-flop is reset when the scanner stops, the channel active flip-flop in the selected channel is set. The 0 output of the reset side of the set channel active flip-flop is inverted and applied as a 1 to enable the input AND gates to the read, write, and partial-write flip-flops, and the S' and Z register flip-flops. The read, write, partial-write, and S' register flip-flops reset during the clear read-write and clear S' pulse at the end of the preceding cycle, and remain reset until a mode select AND gate or S' register AND gate is completed in the active channel. The Z register was reset during the clear Z pulse at the start of the current cycle.

The following discussion assumes that the write mode is to be selected in active channel 1, Figure 2-5. A 0 appears on the output of receiver R162, thereby blocking the 1 received from W102; hence a 1 appears on the output of I314. The 1 received from W102 resulted from the channel selection and setting of channel 1 channel active flip-flop. The AND gate input to K812/K813 is completed at the start of the memory cycle when the output of J811 is a 1. The reset output of K812/K813 is inverted through J815, placing an enabling 1 on the input gate for bits 6 through 12 of the Z register. This same 0 is inverted through J814, thereby placing an enabling 1 on the input gate for bits 0 through 5 of the Z register. A 1 does not appear on the output of J814 and J815 until both inputs to these inverters are 0; therefore, when a 0 from emitter-follower E904 appears at the input to these inverters, the R to Z register transfer function occurs. All Z register flip-flops that are to store 1's are set, and those that are to store 0's are not set. This write action is described under Inhibit Circuits. (The inhibit circuits in the 8492 Memory Unit are identical to those in the internal memory of the 8491 Compute Unit. A functional analysis of this subject is given in Section 1.)

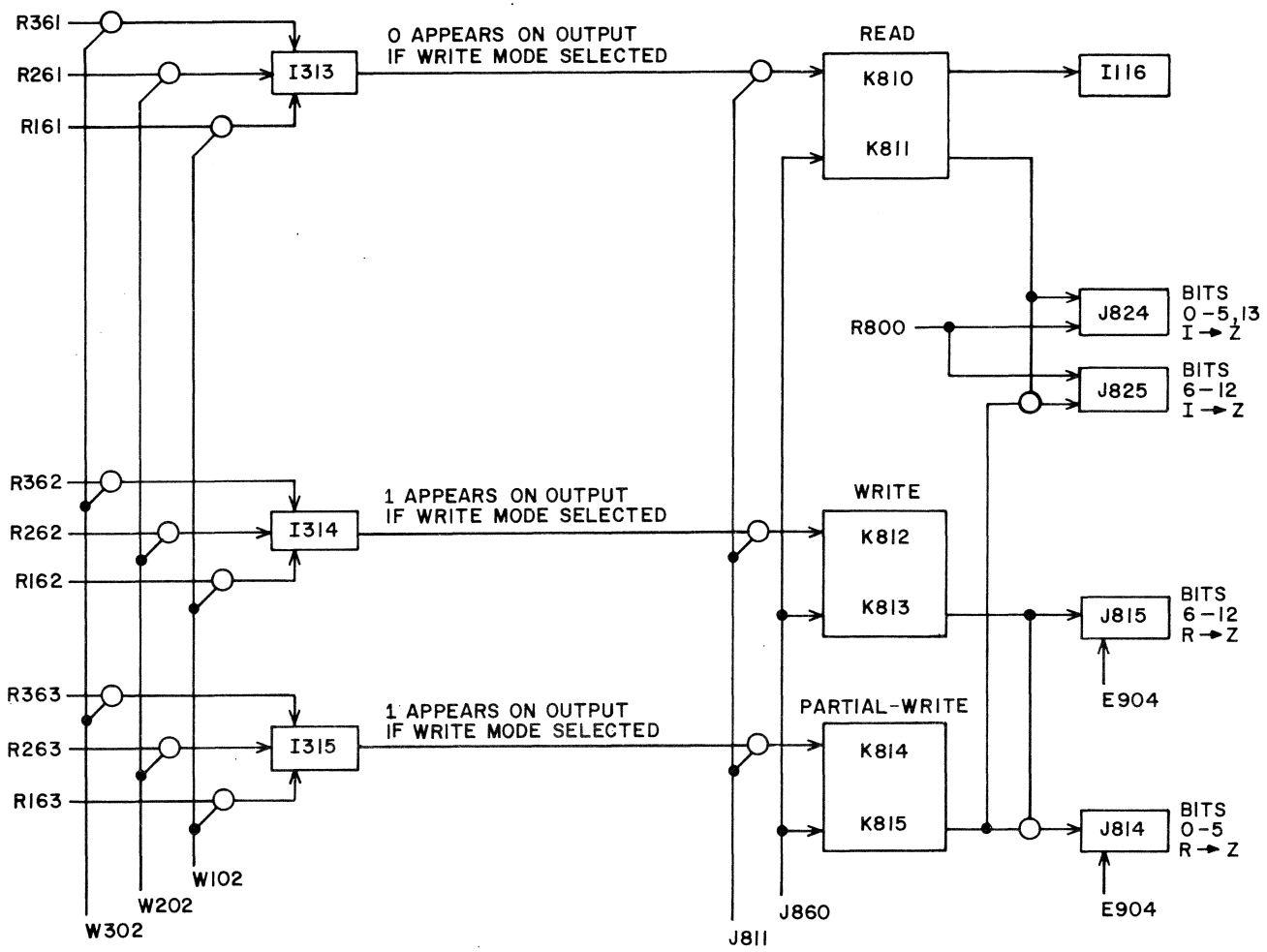
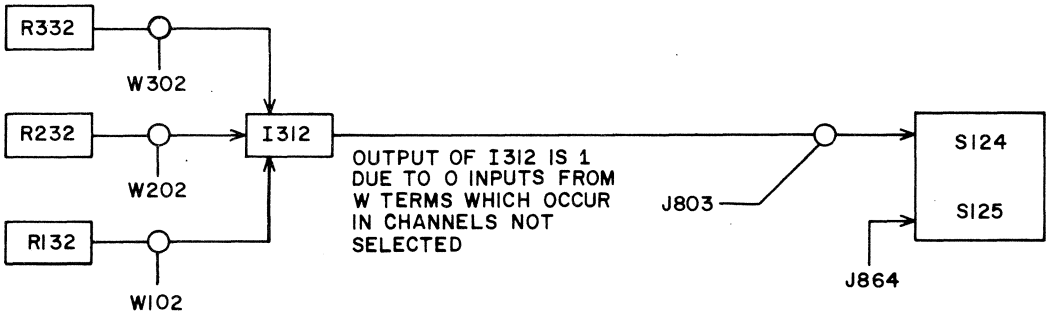


Figure 2-5. Read, Write, Partial-Write Control Logic

The 1 appearing on the output of R161 for read mode and R163 for partial-write mode combines with the 1 output of W102 to set a 0 on the output of inverters I313 and I315, respectively. This blocks the AND gate to read flip-flop K810/K811 and partial-write flip-flop K814/K815, thereby preventing these flip-flops from setting.

ADDRESS SELECTION

Since all address transfers operate in the same manner, a typical operation is described for the transfer of bit 12 from R to S' register with channel 1 selected, Figure 2-6. If bit 12 is 0, the output of R132 is a 1. When the channel active flip-flop K102/K103 sets, a 1 appears on the output of W102. The 1 output of W102 combines with the 1 output of R132 to set a 0 on the output of I312. The 0 output of I312 blocks the AND gate to S124/S125, thereby preventing this flip-flop from setting when the 1 input from J803 is received. At the end of the preceding cycle, the output of J870 is a 1 which resets the memory busy flip-flop K120/K121, Figure 2-7. The 0 output at the set side of K120/K121 enables the OR gate input at J000. The reset output of the channel 1 active flip-flop disables the AND input at J000 enabling a 1 output at J000. The 1 output at J000 is inverted by J801, causing a 1 output at J802 and J803 which enables the R to S' register transfer. The 1 output at J000 is also inverted by J800 which starts a 0 pulse down the delay line.



NOTES APPLY...
S'REGISTER TRANSFER FUNCTION WITH CHANNEL 1 SELECTED: BIT I2 IS A 0.

Figure 2-6. S' Register, Bit 12

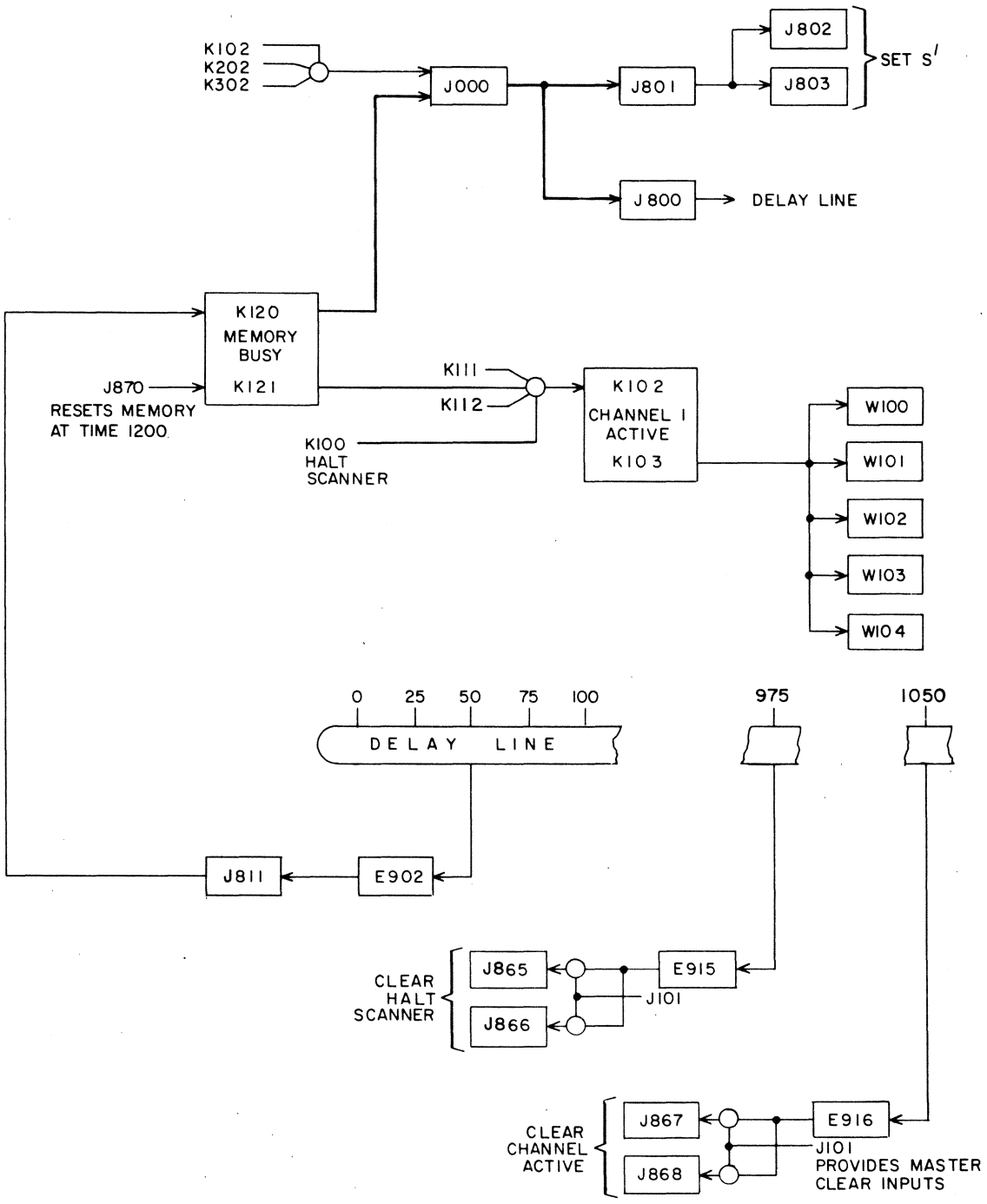


Figure 2-7. Pulse-Forming and Memory Busy Logic

The delay line is normally held at a logic 1, and when the 0 output of J800 occurs, the leading edge of this 0 pulse is started down the delay line. When the leading edge of this 0 pulse is picked off the delay line by emitter-follower E902, the 1 output of J811 sets the memory busy flip-flop K120/K121. The set output of K120/K121 sets a 1 on the input of J000, thereby causing a 0 output and setting a 1 on the output of J800. The 0 pulse is now about 50-nanoseconds wide and travels the length of the delay line in about 1200 nanoseconds.

The memory busy flip-flop K120/K121 remains set because no clear pulse has arrived to clear it, and its 0 output is applied to the AND gates of the set input side of the channel active flip-flops.

The following discussion assumes that the address in the S' register is zero. Thus, there is a 1 on the reset side of each S' register flip-flop. Since bit 12 is a 0, it operates as follows to set the memory to the even bank. The 1 output of S124/S125 remaining from the previous clear signal combines with the 1 output of S064/S065 to satisfy inverter E839. The 0 output of E839 is combined with the appropriate 0 inputs to select two transformer drivers and one gate in the even memory bank along the Y axis. The selection of the transfer driver and gate in the Y axis is accomplished in the same manner as described in the following paragraph as an example of the selection of transformer drivers and gates in the X axis.

In this example, address 0000 octal is used to select gate G004 and transformer drivers D000 and D003, as shown in Figure 2-8.

Bit 12 is used to select the odd or even bank. The remaining 12 bits, bit 11 through bit 0, are used so that the lower 6 bits select transformer drivers and gates along the X axis and the upper 6 bits select transformer drivers and gates along the Y axis. The set output of K834/K835 is inverted through the inverter E820 and applied as a 0 input to D000. The 1 output from S034/S035 is inverted through inverter E825 and applied as a 0 input to D000, D001, D002, and D003. The 1 output from S004/S005 is inverted through inverter E827 and applied as a 0 input to D000 through D003. The three coincident 0 inputs which turn on a transformer driver occur on the inputs to D000 and D003. A 1 on any input of a transformer driver does not turn on that driver. A further analysis of the action of the remaining bits shows a 1 appearing on at least one of the inputs to the remaining transformer drivers along the X axis. This prevents these transformer drivers from being turned on. A similar action occurs using appropriate logic circuitry to turn on one of the eight line driver transformers enabled by D000 and D003. The action of the gates, transformer drivers, and line driver transformers is further described under X and Y drive circuits. (The X and Y drive circuits, core arrangement, core theory, and parity logic in the 8492 Memory Unit are identical to those in the internal memory of the 8491 Compute Unit. A functional analysis of these subjects is contained in Section 1.)

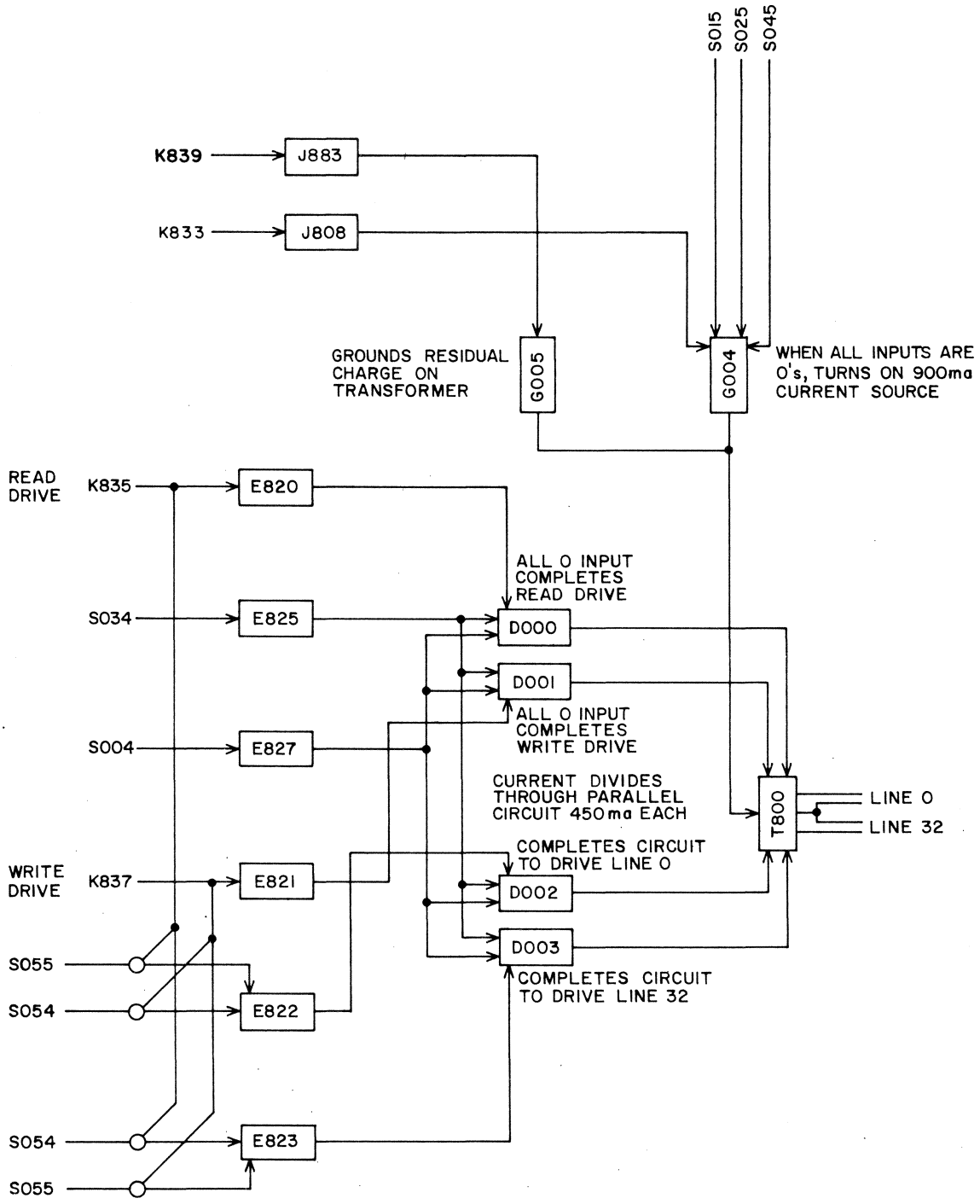


Figure 2-8. Typical Line Drive Selection Logic

MEMORY TIMING

When a memory reference to an external Memory Unit is made by a Compute or I/O Unit, the select code, memory address, mode command, FWA, LWA + 1, and memory request are originated by this Compute or I/O Unit. After memory time 0, when the delay line in the Memory Unit is active, the functions of read, write, or partial-write are controlled within the Memory Unit. The Compute Unit or I/O Unit then stays on the line until the Memory Unit completes its cycle.

Each Memory Unit contains a delay line which controls the sequence of events to read data from memory or write data into memory. The delay line in the memory section cycles through its functions in approximately 1.2 microseconds or 1200 nanoseconds.

Memory Cycle

The functions occurring during the first 200 nanoseconds of the 1.35-microsecond memory cycle are listed as minus times. At 0 time the delay line is activated. The remaining 1200 nanoseconds are listed as plus times. All times are in nanoseconds. Assume a channel 1 select code.

Time -200: The select code, memory address, mode command, and data word (assuming a write or partial-write function) are on the input data lines to the Memory Unit. At time -200 a memory request appears on the request line.

Time -198: The 1 outputs of the four inverters or three code select switches on the select-code lines plus the memory request satisfy the 4-input AND gate to one of the halt scanner flip-flops. The reset output of the halt scanner flip-flop places a blocking 0 on an AND gate to one of the flip-flops in the scanner, Figure 2-4.

Time -185: The scanner stops enabling two inputs to the AND gate of one of the channel active flip-flops. These two scanner outputs combine with the 1 output from the reset memory busy flip-flop and the 1 output from the halt scanner flip-flop to set the channel active flip-flop.

Time -40: The output of the reset side of the set channel active flip-flop is inverted and applied as a 1 to the control gate for the:

R to Z transfer of data bits

R to S' transfer of address bits

R transfer of the mode command

Transfer of data bits, parity error, resume I, and resume II to the Compute Unit

The reset output of the channel 1 active flip-flop places a disabling 0 on the AND gate input to J008.

The set output of the memory busy flip-flop enables the OR gate input to J000.

Time -30: The 1 output of J000 is inverted through J801. The 0 output of J801 is inverted through J802 and J803 to enable the AND gates to the S' register.

The 1 output of J000 also is applied to J800 to start forming a positive going pulse on the delay line, Figure 2-7.

Time -16: The 1 outputs from J802 (for the lower six bits) and J803 (for the upper seven bits) combine with the output of the I inverters following the receivers on the address lines to set the memory address in the S' register.

Time 0: The 0 pulse from J800 starts a 0 pulse down the delay line, Figure 2-9. After the leading edge of the 0 pulse on the delay line passes emitter-follower E900, a 1 appears on the output of J816. The 1 output of J816 sets the gate flip-flop K832/K833 and the read-drive flip-flop K834/K835. The 1 output from J000 resets discharger drive flip-flop K838/K839.

The set output of K832/K833 is inverted through J806 and J808 and applied to the gates in the address selection circuitry connected to the line-driver transformers. The set output of the read-drive flip-flop K834/K835 is applied to inverters E820, E822, E823, E830, E832, and E833. S' register flip-flops S044/S045, S024/S025, and S014/S015 combine with the output of J808 to satisfy the AND input of one of the gate cards in the X-drive logic. S054/S055, S034/S035, and S004/S005 are applied to the transformer drivers. The gate and transformer driver select a line-drive transformer and allow 340 milliamperes of current to flow in the energized X line. The 1 output of flip-flops S074/S075, S084/S085, and S104/S105 combine in the same manner to turn on a gate in the Y axis. Flip-flops S064/S065, S094/S095, S114/S115, and S124/S125 combine with the set output of K834/K835 to select a line in the Y axis. The Y axis selection is performed in the same manner as the X axis selection. The current is sufficient to switch a core from 1 to 0 at the intersection of the selected X and Y drive lines. The output of the discharger drive flip-flop K838/K839 places a disabling 1 on the inputs to the transformer dischargers for the X and Y drive.

Time 25: After the leading edge of the 0 pulse on the delay line reaches the input to emitter-follower E901, a 1 appears on the output of J809 and J810. The 1 output of J809 and J810 clears the Z register flip-flops in preparation for receipt of a 13-bit data word.

Mode Selection

The remaining events in a memory cycle vary depending on the mode of operation. One cycle may be either a read, write, or partial-write cycle; therefore, each mode as it occurs in a memory cycle is discussed separately.

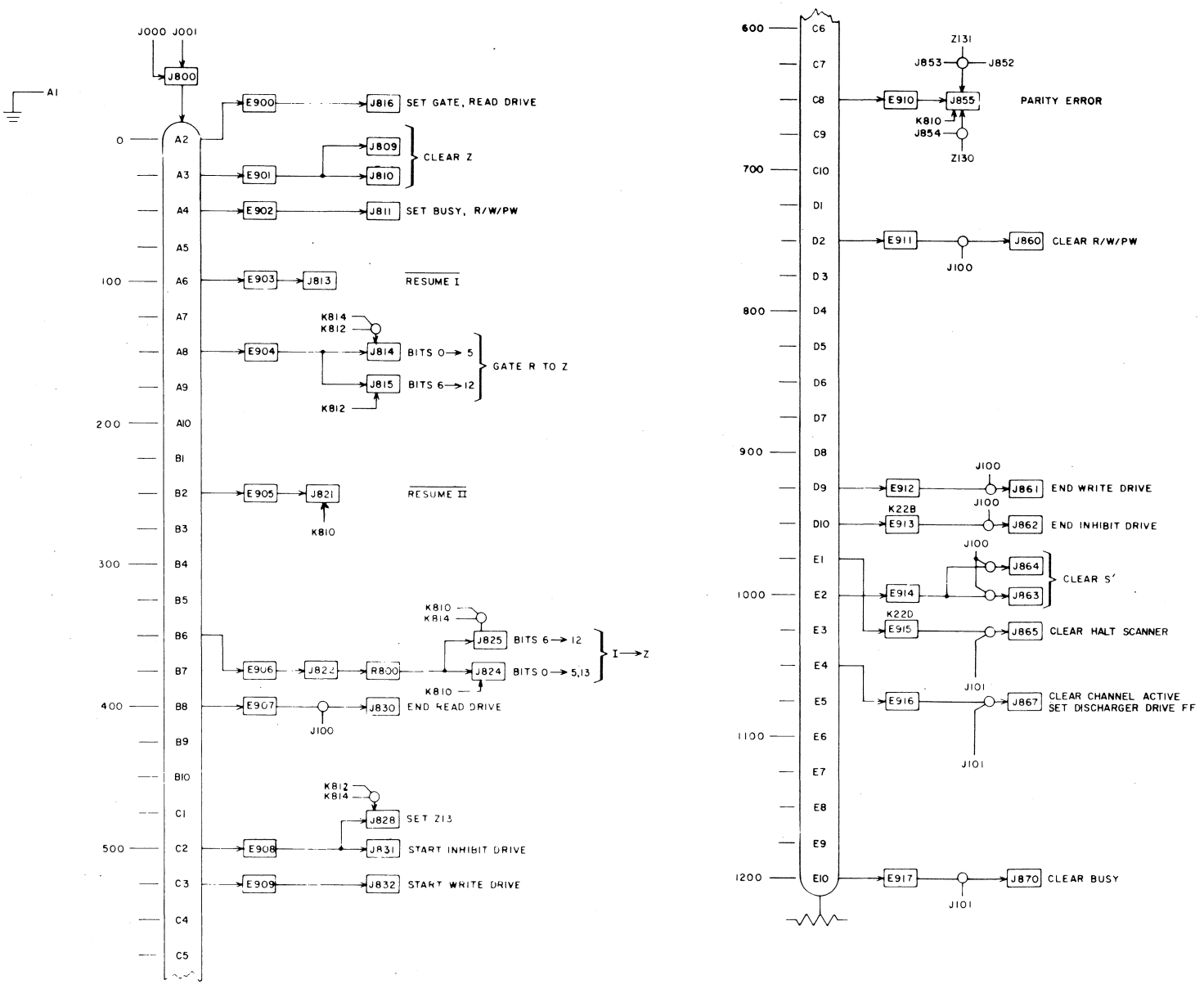


Figure 2-9. Memory Cycle

Write Mode

Time 50: After the leading edge of the 0 pulse on the delay line passes emitter-follower E902, a 1 appears on the output of J811. The 1 output of J811 is applied to set K120/K121, the memory busy flip-flop. The set output of K120/K121 causes a 0 output from J000 and J001. The 0 output of J000 and J001 enables a 1 output at J800. This returns the delay line to a logic 1. This action forms a delay line pulse approximately 50-nanoseconds wide. The 1 output of J811 also allows the read, write, or partial-write flip-flops to set.

Time 100: The leading edge of the 0 pulse on the delay line passes emitter-follower E903, producing a 1 output at J813. This 1 output at J813 is an inverted resume I signal which is applied to the AND gate inputs of transmitters T155, T255, and T355. The 1 output at J813 satisfies the AND gate to one transmitter at the selected channel. This transmits the resume I to the computer. The resume I signal indicates that the R to Z register transfer has occurred and that data may be dropped from the input lines. The signal occurs slightly before the actual R to Z register transfer; however, by the time the signal is translated by the Compute or I/O Unit, the transfer has occurred.

Time 150: The leading edge of the 0 pulse on the delay line passes emitter-follower E904. The 0 output of E904 satisfies the inputs to J814 and J815, thereby placing a 1 on their outputs. The 1 outputs of J814 and J815 allow the R to Z register transfer to occur.

Time 250: The 0 pulse on the delay line passes emitter-follower E905, causing a 1 output at J821. This 1 output is applied to the AND gate input of the resume II transmitters. The 1 output of J821 will satisfy the AND gate input to the transmitter at the selected channel of the other Memory Unit. A resume II signal appears at the selected channel to indicate that a transfer from the sense amplifier inverters to the Z register has occurred. However, since the inverters following the reset read flip-flop K810/K811 have 0 outputs, no transfer of 1's can occur and the resume II operation in write mode is equivalent to an all 0 transfer from I to the Z register.

Time 350: The 0 pulse on the delay line passes emitter-follower E906, placing a shaped 0 pulse on the output of R800. J822 and R800 shape the pulse for sense amplifier gating. The 0 output of R800 enables J824 and J825. The 1 output of the reset partial-write flip-flop K814/K815 combines with the 1 output of K810/K811 to place a blocking 1 on the input to J825. The output of J824 and J825 is 0; therefore, no I to Z transfer of 1's occurs.

Time 400: The 0 pulse on the delay passes emitter-follower E907, placing a 1 on the output of J830. The 1 output of J830 clears the read-drive flip-flop K834/K835. The set output of K834/K835 is inverted through E820, E822, E823, E830, E832, E833 to place a blocking 1 on the input to the transformer drivers along the X and Y axes. This turns off the read drive.

Time 500: The 0 pulse on the delay line passes emitter-follower E908, causing a 1 output of J831. The reset output of the write flip-flop K812/K813 combines with the 0 output of E908 to place a 1 on the output of J828. The 1 output of J831 is applied to enable the AND gate inputs to the inhibit stripe select flip-flops K816/K817 through K830/K831. This 1 combines with the set and clear outputs of S044/S045 and S054/S055 (for selection of the odd inhibit drivers) and combines with S104/S105 and S114/S115 (for selection of even inhibit drivers) to set the appropriate stripe select flip-flops. The outputs of the stripe select flip-flops combine with the reset output of Z register flip-flops to turn on the required inhibit drivers. The 1 output of J828 enables the AND gate input to parity flip-flop Z130/Z131. If parity is 1, the reset output of set flip-flop Z130/Z131 prevents a turn-on of the inhibit driver; and the core receiving a parity bit switches from 0 to 1. If parity is 0, then the core is not switched.

Time 525: The 0 pulse on the delay line passes emitter-follower E909, causing a 1 on the output of J832. The 1 output of J832 is applied to set the write-drive flip-flop K836/K837. The set output of K836/K837 is inverted and applied as 0's to turn on transformer drivers in the X and Y axes. The direction of current through the line-driver transformers, as determined by the write transformer drivers, is to switch cores from 0 to 1. Any cores that do not have an opposing inhibit current flowing through them are switched. The contents of the Z register is transferred to the memory location selected by the S' register.

Time 650: The 0 pulse on the delay line passes emitter-follower E910, placing a 0 on the input of J855. The reset output of read flip-flop K810/K811 blocks inverter J855, causing a 0 output to remain on the output of J855. The 0 output of J855 blocks the parity error transmitters so a transmission of 1 along the parity error line does not occur. The 0 output of J855 blocks the parity error transmitters at the selected channel of the other Memory Unit.

Time 750: The 0 pulse on the delay line passes emitter-follower E911, causing a 1 output of J860. The 1 output of J860 clears read flip-flop K810/K811, write flip-flop K812/K813, and partial-write flip-flop K814/K815.

Time 925: The 0 pulse on the delay line passes emitter-follower E912, causing a 1 output from J861. The 1 output of J861 clears gate flip-flop K832/K833 and write-drive flip-flop K836/K837. The reset output of K832/K833 is inverted through J806 and J808 to turn off the X and Y gates. This prevents further core switching for the remainder of the cycle. The set output of K836/K837 is inverted to block a turn-on of transformer drivers in the X and Y axes of the memory banks.

Time 950: The 0 pulse on the delay line passes emitter-follower E913, causing a 1 output of J862. The 1 output of J862 clears stripe select flip-flops K816/K817 through K830/K831. The set output of these stripe select flip-flops blocks the AND gate inputs to the inhibit generators, thereby ending the inhibit drive.

Time 1000: The 0 pulse on the delay line passes emitter-follower E914, placing a 1 on the output of J863 and J864. The 1 output of J863 and J864 clears the S' register.

Time 975: The 0 pulse on the delay line passes emitter-follower E915, placing a 1 on the output of J865. The 1 output of J865 clears the halt scanner flip-flops.

Time 1050: The 0 pulse on the delay line passes emitter-follower E916, placing a 1 on the output of J867. The 1 output of J867 clears the channel active flip-flops and the discharger drive flip-flop K838/K839. The reset output of K838/K839 is inverted through J805 and J807 and the 0 output is applied to the transformer discharger circuits. The 0 output to the discharger circuits turns them on to ground out any remnant magnetization of the line-driver transformers and thereby aids the gates to turn off.

Time 1200: The 0 pulse on the delay line passes emitter-follower E917, placing a 1 on the output of J870. The 1 output of J870 clears the memory busy flip-flop K120/K121. The set output of K120/K121 and its inverted reset output enable the AND gates to the channel active flip-flops, thereby preparing them for selection in a subsequent cycle.

Read Mode

Only those times and events that differ from the write mode are listed for the read mode. Otherwise, the time and events are the same for both modes.

Time 50: The read mode is basically the same as the write mode except the read flip-flop K810/K811 is set.

Time 150: The 1 outputs of write flip-flop K812/K813 and partial-write flip-flop K814/K815 place a blocking 1 on the inputs to J814 and J815. This prevents an R to Z register transfer and the Z register remains clear.

Time 350: The 0 pulse on the delay line passes emitter-follower E906, causing a 0 output from R800. The 0 output of R800 enables inverters J824 and J825. The reset output of the read flip-flop K810/K811 satisfies J824, placing a 1 on its output. The reset output of partial-write flip-flop K814/K815 and the reset output of K810/K811 disable the AND gate input of J825, thereby setting a 1 on the output of J825. The 1 output of J824 enables the AND gate between the sense amplifier inverters and the Z register flip-flops for bits 0 through 5 and parity bit 13. The 1 output of J825 enables the AND gate between the sense amplifier inverters and the Z register flip-flops for bits 6 through 12.

These AND gates satisfy any sense amplifier inverters having 1's on their outputs. This causes the corresponding Z register flip-flop to set. The reset outputs of the set flip-flops in the Z register are inverted and applied as 1's to the AND gate inputs of the data transmitters. Since these transmitters were enabled at time 250, a transfer of data from the Memory Unit to the selecting Compute or I/O Unit occurs.

The remainder of the memory cycle is identical to the cycle described in the write mode. The word that was destroyed when it was read out of memory is restored in its same memory location.

Partial Write

Time 100: The partial-write mode is the same as the write mode except partial-write flip-flop K814/K815 is set.

Time 150: The leading edge of the 0 pulse on the delay line passes emitter-follower E904 to place an enabling 0 on the input to J814 and J815. The reset output of K814/K815 blocks the reset output of K812/K813 to place a satisfying 0 on the inputs of J814. This sets the output of J814 to 1. The reset output of K812/K813 blocks inverter J815, thereby leaving a 0 on the output of J815. The 1 output of J814 satisfies the AND gates for a transfer of 1's from the R register input to the six lower order flip-flops in the Z register. The 0 output of J815 blocks the AND gate inputs so an R to Z register transfer of the seven upper bits does not occur.

Time 350: The 0 pulse on the delay line passes emitter-follower E906, causing a 0 on the output of R800. The 0 output of R800 enables J824 and J825. The reset output of flip-flop K810/K811 blocks the 0 input to J824 so a 0 remains on the output of J824. The reset output of the partial-write flip-flop K814/K815 blocks the AND gate input to J825. The 0 from the blocked AND gate satisfies the 0 inputs to J825 to place a 1 on the output of J825. The 1 output of J825 enables the AND gate inputs to the upper seven bits in the Z register. The upper seven bits in the selected address are gated into the Z register. The AND gates to the six lower order flip-flops of the Z register and the parity bit flip-flop are blocked by the 0 output of J824 so a sense amplifier inverter to Z transfer does not occur. The Z register now contains a word consisting of six lower bits from the Compute or I/O Unit and seven upper bits from those existing in memory.

The remainder of the cycle is the same as the write mode except at time 500 when the parity circuitry generates a parity bit corresponding to the number of 1's in the new word. The parity bit then goes into memory.

SECTION 2

AUXILIARY MEMORY UNIT

EQUIPMENT DIAGRAMS

SECTION 2

AUXILIARY MEMORY UNIT

LOGIC DIAGRAMS

- Symbol Index
- Logic Diagrams

NOTE THE CARDS IN THE UPPER CHASSIS (ROWS A THROUGH O) ARE IN LOGIC CIRCUITRY. THE CARDS IN THE LOWER CHASSIS (ROWS P THROUGH T) ARE USED FOR INTER-CHASSIS GATING.

D000	1C016A	X DRIVER ADDRESS Y-YXXOXXO R	11
D001	1C016B	X DRIVER ADDRESS Y-YXXOXXO W	11
D002	1C011A	X DRIVER ADDRESS Y-YOXOXXO R OR Y-Y1XOXXO W	11
D003	1C011B	X DRIVER ADDRESS Y-YOXOXXO W OR Y-Y1XOXXO R	11
D004	1C006A	X DRIVER ADDRESS Y-YXX1XXO R	11
D005	1C006B	X DRIVER ADDRESS Y-YXX1XXO W	11
D006	1C001A	X DRIVER ADDRESS Y-YOX1XXO R OR Y-Y1X1XXO W	11
D007	1C001B	X DRIVER ADDRESS Y-YOX1XXO W OR Y-Y1X1XXO R	11
D008	1D016A	X DRIVER ADDRESS Y-YXXOXX1 R	11
D009	1D016B	X DRIVER ADDRESS Y-YXXOXX1 W	11
D010	1D011A	X DRIVER ADDRESS Y-YOXOXX1 R OR Y-Y1XOXX1 W	11
D011	1D011B	X DRIVER ADDRESS Y-YOXOXX1 W OR Y-Y1XOXX1 R	11
D012	1D006A	X DRIVER ADDRESS Y-YXX1XX1 R	11
D013	1D006B	X DRIVER ADDRESS Y-YXX1XX1 W	11
D014	1D001A	X DRIVER ADDRESS Y-YOX1XX1 R OR Y-Y1X1XX1 W	11
D015	1D001B	X DRIVER ADDRESS Y-YOX1XX1 W OR Y-Y1XXX1 R	11
D020	1K009A	70 NANOSEC DELAY-SCANNER	4
D021	1K009C	70 NANOSEC DELAY-SCANNER	4
D022	1K009D	70 NANOSEC DELAY-SCANNER	4
D112	1N019A	MASTER CLEAR, 0.5 MICRO SEC DELAY	9
D120	1N027A	MASTER CLEAR, 5 MILLISECOND DELAY	9
D121	1N025A	MASTER CLEAR, 0.2 MICRO SEC DELAY	9
D122	1N024A	MASTER CLEAR, 1.0 MICRO SEC DELAY	9
D123	1N071A	MASTER CLEAR, 0.3 MICRO SEC DELAY	9
D200	1E013A	Y DRIVER ADDRESS OYYOYYOX-X R	12
D201	1E013B	Y DRIVER ADDRESS OYYOYYOX-X W	12
D202	1F008A	Y DRIVER ADDRESS OOYOYYOX-X W OR O1YOYYOX-X R	12
D203	1E008B	Y DRIVER ADDRESS OOYOYYOX-X R OR O1YOYYOX-X W	12
D204	1E007A	Y DRIVER ADDRESS OYY1YYOX-X R	12
D205	1F007B	Y DRIVER ADDRESS OYY1YYOX-X W	12
D206	1E002A	Y DRIVER ADDRESS OOY1YYOX-X W OR O1Y1YYOX-X R	12
D207	1E002B	Y DRIVER ADDRESS OOY1YYOX-X R OR O1Y1YYOX-X W	12
D208	1E019A	Y DRIVER ADDRESS OYYOYY1X-X R	12
D209	1E019B	Y DRIVER ADDRESS OYYOYY1X-X W	12
D210	1E014A	Y DRIVER ADDRESS OOYOYY1X-X W OR O1YOYY1X-X R	12
D211	1E014B	Y DRIVER ADDRESS OOYOYY1X-X R OR O1YOYY1X-X W	12
D212	1F020A	Y DRIVER ADDRESS OYY1YY1X-X R	12
D213	1F020B	Y DRIVER ADDRESS OYY1YY1X-X W	12
D214	1F015A	Y DRIVER ADDRESS OOY1YY1X-X W OR O1Y1YY1X-X R	12
D215	1F015B	Y DRIVER ADDRESS OOY1YY1X-X R OR O1Y1YY1X-X W	12
D216	1F006A	Y DRIVER ADDRESS 1YYOYYOX-X R	13
D217	1F006B	Y DRIVER ADDRESS 1YYOYYOX-X W	13
D218	1F001A	Y DRIVER ADDRESS 1OYOYYOX-X W OR 11YOYYOX-X R	13
D219	1F001B	Y DRIVER ADDRESS 1OYOYYOX-X R OR 11YOYYOX-X W	13
D220	1G007A	Y DRIVER ADDRESS 1YY1YYOX-X R	13
D221	1G007B	Y DRIVER ADDRESS 1YY1YYOX-X W	13
D222	1G002A	Y DRIVER ADDRESS 1OY1YYOX-X W OR 11Y1YYOX-X R	13
D223	1G002B	Y DRIVER ADDRESS 1OY1YYOX-X R OR 11Y1YYOX-X W	13
D224	1G019A	Y DRIVER ADDRESS 1YYOYY1X-X R	13
D225	1G019B	Y DRIVER ADDRESS 1YYOYY1X-X W	13
D226	1G014A	Y DRIVER ADDRESS 1OYOYY1X-X W OR 11YOYY1X-X R	13
D227	1G014B	Y DRIVER ADDRESS 1OYOYY1X-X R OR 11YOYY1X-X W	13
D228	1G013A	Y DRIVER ADDRESS 1YY1YY1X-X R	13
D229	1G013B	Y DRIVER ADDRESS 1YY1YY1X-X W	13
D230	1G008A	Y DRIVER ADDRESS 1OY1YY1X-X W OR 11Y1YY1X-X R	13
D231	1G008B	Y DRIVER ADDRESS 1OY1YY1X-X R OR 11Y1YY1X-X W	13

E820	1H001A	X DRIVER SELECTOR	11
E821	1H001B	X DRIVER SELECTOR	11
E822	1H002A	X DRIVER SELECTOR	11
E823	1H002B	X DRIVER SELECTOR	11
E824	1H003A	X DRIVER SELECTOR	11
E825	1H003B	X DRIVER SELECTOR	11
E826	1H004A	X DRIVER SELECTOR	11
E827	1H004B	X DRIVER SELECTOR	11
E830	1H005A	Y DRIVER SELECTOR	12
E831	1H005B	Y DRIVER SELECTOR	12
E832	1H006A	Y DRIVER SELECTOR	12
E833	1H006B	Y DRIVER SELECTOR	12
E834	1H007A	Y DRIVER SELECTOR	12
E835	1H007B	Y DRIVER SELECTOR	12
E836	1H008A	Y DRIVER SELECTOR	12
E837	1H008B	Y DRIVER SELECTOR	13
E838	1H009A	Y DRIVER SELECTOR	13
E839	1H009B	Y DRIVER SELECTOR	13
E840	1H010A	Y DRIVER SELECTOR	13
E841	1H010B	Y DRIVER SELECTOR	13
E900	1K019A	EMITTER FOLLOWER - TIME 0 NSEC	5
E901	1K019B	EMITTER FOLLOWER-TIME 25 NSEC	5
E902	1K019C	EMITTER FOLLOWER-TIME 50 NSEC	5
E903	1K019D	EMITTER FOLLOWER - TIME 100 NSEC	5
E904	1K020A	EMITTER FOLLOWER - TIME 150 NSEC	5
E905	1K020B	EMITTER FOLLOWER - TIME 250 NSEC	5
E906	1K020C	EMITTER FOLLOWER - TIME 350 OR 375 NSEC	5
E907	1K020D	EMITTER FOLLOWER - TIME 400 NSEC	5
E908	1K021A	EMITTER FOLLOWER - TIME 500 NSEC	5
E909	1K021B	EMITTER FOLLOWER - TIME 525 NSEC	5
E910	1K021C	EMITTER FOLLOWER - TIME 650 NSEC	5
E911	1K021D	EMITTER FOLLOWER - TIME 750 NSEC	5
E912	1K022A	EMITTER FOLLOWER - TIME 925 NSEC	5
E913	1K022B	EMITTER FOLLOWER - TIME 950 NSEC	5
E914	1K022C	EMITTER FOLLOWER - TIME 1000 NSEC	5
E915	1K022D	EMITTER FOLLOWER - TIME 975 NSEC	5
E916	1K023A	EMITTER FOLLOWER - TIME 1050 NSEC	5
E917	1K023B	EMITTER FOLLOWER - TIME 1200 NSEC	5
G000	1B001A	STRIPE 0 INHIBIT BIT 0	7
G001	1B001B	STRIPE 1 INHIBIT BIT 0	7
G002	1B008A	STRIPE 2 INHIBIT BIT 0	7
G003	1B008B	STRIPE 3 INHIBIT BIT 0	7
G004	1C010A	X GATE ADDRESS Y-YXOXOOX	11
G005	1C010B	X GATE G004 DISCHARGER	11
G006	1F014A	Y GATE ADDRESS YYOYOOYX-X	12
G007	1F014B	Y GATE G006 DISCHARGER	12
G010	1B015A	STRIPE 0 INHIBIT BIT 1	8
G011	1B015B	STRIPE 1 INHIBIT BIT 1	8
G012	1B022A	STRIPE 2 INHIBIT BIT 1	8
G013	1B022B	STRIPE 3 INHIBIT BIT 1	8
G014	1C009A	X GATE ADDRESS Y-YXOXO1X	11
G015	1C009B	X GATE G014 DISCHARGER	11
G016	1F013A	Y GATE ADDRESS YYOYO1YX-X	12
G017	1F013B	Y GATE G016 DISCHARGER	12
G020	1B002A	STRIPE 0 INHIBIT BIT 2	7
G021	1B002B	STRIPE 1 INHIBIT BIT 2	7
G022	1B009A	STRIPE 2 INHIBIT BIT 2	7
G023	1B009B	STRIPE 3 INHIBIT BIT 2	7
G024	1C008A	X GATE ADDRESS Y-YXOX1OX	11
G025	1C008B	X GATE G024 DISCHARGER	11
G026	1F012A	Y GATE ADDRESS YYOY1OYX-X	12
G027	1F012B	Y GATE G026 DISCHARGER	12

G030	1B016A	STRIPE 0 INHIBIT BIT 3	8
G031	1B016B	STRIPE 1 INHIBIT BIT 3	8
G032	1B023A	STRIPE 2 INHIBIT BIT 3	8
G033	1B023B	STRIPE 3 INHIBIT BIT 3	8
G034	1C007A	X GATE ADDRESS Y-YX0X11X	11
G035	1C007B	X GATE G034 DISCHARGER	11
G036	1F011A	Y GATE ADDRESS YY0Y11YX-X	12
G037	1F011B	Y GATE G036 DISCHARGER	12
G040	1B003A	STRIPE 0 INHIBIT BIT 4	7
G041	1B003B	STRIPE 1 INHIBIT BIT 4	7
G042	1B010A	STRIPE 2 INHIBIT BIT 4	7
G043	1B010B	STRIPE 3 INHIBIT BIT 4	7
G044	1D010A	X GATE ADDRESS Y-YX1X00X	11
G045	1D010B	X GATE G044 DISCHARGER	11
G046	1F010A	Y GATE ADDRESS YY1Y00YX-X	12
G047	1F010B	Y GATE G046 DISCHARGER	12
G050	1B017A	STRIPE 0 INHIBIT BIT 5	8
G051	1B017B	STRIPE 1 INHIBIT BIT 5	8
G052	1B024A	STRIPE 2 INHIBIT BIT 5	8
G053	1B024B	STRIPE 3 INHIBIT BIT 5	8
G054	1D009A	X GATE ADDRESS Y-YX1X01X	11
G055	1D009B	X GATE G054 DISCHARGER	11
G056	1F009A	Y GATE ADDRESS YY1Y01YX-X	12
G057	1F009B	Y GATE G056 DISCHARGER	12
G060	1B004A	STRIPE 0 INHIBIT BIT 6	7
G061	1B004B	STRIPE 1 INHIBIT BIT 6	7
G062	1B011A	STRIPE 2 INHIBIT BIT 6	7
G063	1B011B	STRIPE 3 INHIBIT BIT 6	7
G064	1D008A	X GATE ADDRESS Y-YX1X10X	11
G065	1D008B	X GATE G064 DISCHARGER	11
G066	1F008A	Y GATE ADDRESS YY1Y10YX-X	12
G067	1F008B	Y GATE G066 DISCHARGER	12
G070	1B018A	STRIPE 0 INHIBIT BIT 7	8
G071	1B018B	STRIPE 1 INHIBIT BIT 7	8
G072	1B025A	STRIPE 2 INHIBIT BIT 7	8
G073	1B025B	STRIPE 3 INHIBIT BIT 7	8
G074	1D007A	X GATE ADDRESS Y-YX1X11X	11
G075	1D007B	X GATE G074 DISCHARGER	11
G076	1F007A	Y GATE ADDRESS YY1Y11YX-X	12
G077	1F007B	Y GATE G076 DISCHARGER	12
G080	1B005A	STRIPE 0 INHIBIT BIT 8	7
G081	1B005B	STRIPE 1 INHIBIT BIT 8	7
G082	1B012A	STRIPE 2 INHIBIT BIT 8	7
G083	1B012B	STRIPE 3 INHIBIT BIT 8	7
G090	1B019A	STRIPE 0 INHIBIT BIT 9	8
G091	1B019B	STRIPE 1 INHIBIT BIT 9	8
G092	1B026A	STRIPE 2 INHIBIT BIT 9	8
G093	1B026B	STRIPE 3 INHIBIT BIT 9	8
G100	1B006A	STRIPE 0 INHIBIT BIT 10	7
G101	1B006B	STRIPE 1 INHIBIT BIT 10	7
G102	1B013A	STRIPE 2 INHIBIT BIT 10	7
G103	1B013B	STRIPE 3 INHIBIT BIT 10	7
G110	1B020A	STRIPE 0 INHIBIT BIT 11	8
G111	1B020B	STRIPE 1 INHIBIT BIT 11	8
G112	1B027A	STRIPE 2 INHIBIT BIT 11	8
G113	1B027B	STRIPE 3 INHIBIT BIT 11	8
G120	1B007A	STRIPE 0 INHIBIT BIT 12	7
G121	1B007B	STRIPE 1 INHIBIT BIT 12	7
G122	1B014A	STRIPE 2 INHIBIT BIT 12	7
G123	1B014B	STRIPE 3 INHIBIT BIT 12	7
G130	1B021A	STRIPE 0 INHIBIT BIT 13	8
G131	1B021B	STRIPE 1 INHIBIT BIT 13	8
G132	1B028A	STRIPE 2 INHIBIT BIT 13	8
G133	1B028B	STRIPE 3 INHIBIT BIT 13	8
I116	1N015A	OUTPUT GATING,CHAS 1, CHAS 2, CHAS 3	10
I120	1J003B	CHANNEL 1 ACTIVE FF OUTPUT SLAVE	4
I133	1T010A	BANK SELECT INVERTER - CHANNEL 1, BIT 1	3
I134	1T011A	BANK SELECT INVERTER - CHANNEL 1, BIT 2	3
I135	1T012A	BANK SELECT INVERTER - CHANNEL 1, BIT 3	3
I140	1L001A	REQUEST, CHANNEL 1	4
I220	1J004B	CHANNEL 2 ACTIVE FF OUTPUT SLAVE	4
I233	1R010A	BANK SELECT INVERTER - CHANNEL 2, BIT 1	3
I234	1R011A	BANK SELECT INVERTER - CHANNEL 2, BIT 2	3
I235	1R012A	BANK SELECT INVERTER - CHANNEL 2, BIT 3	3
I240	1L001B	REQUEST, CHANNEL 2	4
I300	10001A	S PRIME REGISTER INPUT INV.	6
I301	10002A	S PRIME REGISTER INPUT INV.	6
I302	10003A	S PRIME REGISTER INPUT INV.	6
I303	10004A	S PRIME REGISTER INPUT INV.	6
I304	10005A	S PRIME REGISTER INPUT INV.	6
I305	10006A	S PRIME REGISTER INPUT INV.	6
I306	10007A	S PRIME REGISTER INPUT INV.	6
I307	10008A	S PRIME REGISTER INPUT INV.	6
I308	10009A	S PRIME REGISTER INPUT INV.	6
I309	10010A	S PRIME REGISTER INPUT INV.	6
I310	10011A	S PRIME REGISTER INPUT INV.	6
I311	10012A	S PRIME REGISTER INPUT INV.	6
I312	10013A	S PRIME REGISTER INPUT INV.	6
I313	1N010A	SELECT READ INPUT INVERTER	10
I314	1N011A	SELECT WRITE INPUT INVERTER	10
I315	1N012A	PARTIAL WRITE INPUT INVERTER	10
I320	1J005B	CHANNEL 3 ACTIVE FF OUTPUT SLAVE	4
I333	1P010A	BANK SELECT INVERTER - CHANNEL 3, BIT 1	3
I334	1P011A	BANK SELECT INVERTER - CHANNEL 3, BIT 2	3
I335	1P012A	BANK SELECT INVERTER - CHANNEL 3, BIT 3	3
I340	1L002A	REQUEST, CHANNEL 3	4
I600	10016A	Z REGISTER INPUT INV.	7
I601	10017A	Z REGISTER INPUT INV.	8
I602	10018A	Z REGISTER INPUT INV.	7
I603	10019A	Z REGISTER INPUT INV.	8
I604	10020A	Z REGISTER INPUT INV.	7
I605	10021A	Z REGISTER INPUT INV.	8
I606	10022A	Z REGISTER INPUT INV.	7
I607	10023A	Z REGISTER INPUT INV.	8
I608	10024A	Z REGISTER INPUT INV.	7
I609	10025A	Z REGISTER INPUT INV.	8
I610	10026A	Z REGISTER INPUT INV.	7
I611	10027A	Z REGISTER INPUT INV.	8
I612	10028A	Z REGISTER INPUT INV.	7
I700	1G022A	SENSE AMP.INV.BIT 0	7
I701	1G022B	SENSE AMP.INV.BIT 1	8
I702	1G023A	SENSE AMP.INV.BIT 2	7
I703	1G023B	SENSE AMP.INV.BIT 3	8
I704	1G024A	SENSE AMP.INV.BIT 4	7
I705	1G024B	SENSE AMP.INV.BIT 5	8
I706	1G025A	SENSE AMP.INV.BIT 6	7
I707	1G025B	SENSE AMP.INV.BIT 7	8
I708	1G026A	SENSE AMP.INV.BIT 8	7
I709	1G026B	SENSE AMP.INV.BIT 9	8
I710	1G027A	SENSE AMP.INV.BIT 10	7
I711	1G027B	SENSE AMP.INV.BIT 11	8
I712	1G028A	SENSE AMP.INV.BIT 12	7
I713	1G028B	SENSE AMP.INV.BIT 13	8
I800	1J015A	Z REGISTER OUTPUT SLAVE, BIT 0	7

I801	1J016A	Z REGISTER OUTPUT SLAVE, BIT 1	8
I802	1J017A	Z REGISTER OUTPUT SLAVE, BIT 2	7
I803	1J018A	Z REGISTER OUTPUT SLAVE, BIT 3	8
I804	1J019A	Z REGISTER OUTPUT SLAVE, BIT 4	7
I805	1J020A	Z REGISTER OUTPUT SLAVE, BIT 5	8
I806	1J021A	Z REGISTER OUTPUT SLAVE, BIT 6	7
I807	1J022A	Z REGISTER OUTPUT SLAVE, BIT 7	8
I808	1J023A	Z REGISTER OUTPUT SLAVE, BIT 8	7
I809	1J024A	Z REGISTER OUTPUT SLAVE, BIT 9	8
I810	1J025A	Z REGISTER OUTPUT SLAVE, BIT 10	7
I811	1J026A	Z REGISTER OUTPUT SLAVE, BIT 11	8
I812	1J027A	Z REGISTER OUTPUT SLAVE, BIT 12	7
J000	1J007A	DELAY LINE PULSE SHAPER	4
J100	1N022A	MASTER CLEAR	9
J101	1N022B	MASTER CLEAR	9
J110	1J002A	SCANNER NOT HALTED	9
J112	1N018A	MASTER CLEAR, MEMORY BUSY CKT.	9
J113	1N018B	MASTER CLEAR, MEMORY BUSY CKT.	9
J114	1N020B	MASTER CLEAR, MEMORY BUSY CKT.	9
J120	1N026A	MASTER CLEAR, POWER LOSS CKT	9
J121	1N026B	MASTER CLEAR, POWER TURN-ON	9
J124	1N021A	MASTER CLEAR INPUT INV.	9
J126	1N020A	MASTER CLEAR INV	9
J800	1L017A	DELAY LINE DRIVER	5
J801	1J011A	SET S PRIME INVERTER	4
J802	1J006A	SET S PRIME	4
J803	1J008A	SET S PRIME	4
J806	1G020B	GATE FF OUTPUT SLAVE	12
J808	1D017B	GATE FF OUTPUT SLAVE	11
J809	1J020B	CLEAR Z	5
J810	1J027B	CLEAR Z	5
J811	1K017A	SET BUSY, READ/WRITE/PARTIAL WRITE FFS	5
J813	1N013A	RESUME 1 INVERTED	5
J814	1J016B	GATE R TO Z BITS 0 TO 5	5
J815	1J022B	GATE R TO Z BITS 6 TO 12	5
J816	1K017B	SET GATE, READ DRIVE	5
J821	1N014A	RESUME 2 INVERTED	5
J822	1M020A	I TO Z PULSE SHAPER	5
J824	1J015B	GATE I TO Z BITS 0 TO 5,13	5
J825	1J021B	GATE I TO Z BITS 6 TO 12	5
J828	1J026B	SET Z BIT 13	5
J830	1J017B	END READ DRIVE	5
J831	1J018B	START INHIBIT DRIVE	5
J832	1J019B	START WRITE DRIVE	5
J836	1H017A	PARITY GENERATOR	9
J837	1H018A	PARITY GENERATOR	9
J838	1H018B	PARITY GENERATOR	9
J839	1H015A	PARITY GENERATOR	9
J840	1H016A	PARITY GENERATOR	9
J841	1H016B	PARITY GENERATOR	9
J842	1H019A	PARITY GENERATOR	9
J843	1H027A	PARITY GENERATOR	9
J844	1H020A	PARITY GENERATOR	9
J845	1H020B	PARITY GENERATOR	9
J846	1H023A	PARITY GENERATOR	9
J847	1H024A	PARITY GENERATOR	9
J848	1H024B	PARITY GENERATOR	9
J849	1H021A	PARITY GENERATOR	9
J850	1H022A	PARITY GENERATOR	9
J851	1H022B	PARITY GENERATOR	9
J852	1H025A	PARITY GENERATOR	9
J853	1H026A	PARITY GENERATOR	9
J854	1H027B	PARITY GENERATOR	9
J855	1H028A	PARITY ERROR	9
J860	1J024B	CLEAR READ/WRITE/PARTIAL WRITE	5
J861	1J014A	END WRITE DRIVE	5
J862	1J014B	END INHIBIT DRIVE	5
J863	1J005A	CLEAR S PRIME	5
J864	1J009A	CLEAR S PRIME	5
J865	1M019A	CLEAR HALT SCANNER	5
J867	1J004A	CLEAR CHANNEL ACTIVE AND DISCHARGER FF	5
J870	1L016B	CLEAR BUSY	5
J880	1G020A	DISCHARGER	12
J881	1G020B	DISCHARGER	12
J882	1G020C	DISCHARGER	12
J883	1D017A	DISCHARGER	11
J884	1D017B	DISCHARGER	11
J885	1D017C	DISCHARGER	11
K100	1L004A	HALT SCANNER FF, CHANNEL 1	4
K101	1L004B	HALT SCANNER FF, CHANNEL 1	4
K102	1K002A	CHANNEL 1 ACTIVE FF	4
K103	1K002B	CHANNEL 1 ACTIVE FF	4
K110	1K006A	SCANNER	4
K111	1K006B	SCANNER	4
K112	1K007A	SCANNER	4
K113	1K007B	SCANNER	4
K114	1K008A	SCANNER	4
K115	1K008B	SCANNER	4
K120	1K016A	MEMORY BUSY FF	4
K121	1K016B	MEMORY BUSY FF	4
K200	1L005A	HALT SCANNER FF, CHANNEL 2	4
K201	1L005B	HALT SCANNER FF, CHANNEL 2	4
K202	1K003A	CHANNEL 2 ACTIVE FF	4
K203	1K003B	CHANNEL 2 ACTIVE FF	4
K300	1L006A	HALT SCANNER FF, CHANNEL 3	4
K301	1L006B	HALT SCANNER FF, CHANNEL 3	4
K302	1K004A	CHANNEL 3 ACTIVE FF	4
K303	1K004B	CHANNEL 3 ACTIVE FF	4
K810	1L026A	READ	10
K811	1L026B	READ	10
K812	1L027A	WRITE	10
K813	1L027B	WRITE	10
K814	1L028A	PARTIAL WRITE	10
K815	1L028B	PARTIAL WRITE	10
K816	1D018A	ODD INHIBIT STRIPE 0 ADDRESS Y-Y00XXXX	10
K817	1D018B	ODD INHIBIT STRIPE 0 ADDRESS Y-Y00XXXX	10
K818	1D019A	ODD INHIBIT STRIPE 1 ADDRESS Y-Y01XXXX	10
K819	1D019B	ODD INHIBIT STRIPE 1 ADDRESS Y-Y01XXXX	10
K820	1D020A	ODD INHIBIT STRIPE 2 ADDRESS Y-Y10XXXX	10
K821	1D020B	ODD INHIBIT STRIPE 2 ADDRESS Y-Y10XXXX	10
K822	1D021A	ODD INHIBIT STRIPE 3 ADDRESS Y-Y11XXXX	10
K823	1D021B	ODD INHIBIT STRIPE 3 ADDRESS Y-Y11XXXX	10
K824	1C018A	EVEN INHIBIT STRIPE 0 ADDRESS Y00YYYYX-X	10
K825	1C018B	EVEN INHIBIT STRIPE 0 ADDRESS Y00YYYYX-X	10
K826	1C019A	EVEN INHIBIT STRIPE 1 ADDRESS Y01YYYYX-X	10
K827	1C019B	EVEN INHIBIT STRIPE 1 ADDRESS Y01YYYYX-X	10
K828	1C020A	EVEN INHIBIT STRIPE 2 ADDRESS Y10YYYYX-X	10
K829	1C020B	EVEN INHIBIT STRIPE 2 ADDRESS Y10YYYYX-X	10
K830	1C021A	EVEN INHIBIT STRIPE 3 ADDRESS Y11YYYYX-X	10
K831	1C021B	EVEN INHIBIT STRIPE 3 ADDRESS Y11YYYYX-X	10
K832	1H011A	GATE	10
K833	1H011B	GATE	10
K834	1H012A	READ DRIVE	10
K835	1H012B	READ DRIVE	10

K836	1H013A	WRITE DRIVE	10
K837	1H013B	WRITE DRIVE	10
K838	1H014A	GATE DISCHARGER	10
K839	1H014B	GATE DISCHARGER	10
M100	1N028A	MASTER CLEAR POWER LOSS CKT	9
R120	1T001A	ADDRESS RECEIVER - CHANNEL 1, BIT 0	3
R121	1T001B	ADDRESS RECEIVER - CHANNEL 1, BIT 1	3
R122	1T002A	ADDRESS RECEIVER - CHANNEL 1, BIT 2	3
R123	1T002B	ADDRESS RECEIVER - CHANNEL 1, BIT 3	3
R124	1T003A	ADDRESS RECEIVER - CHANNEL 1, BIT 4	3
R125	1T003B	ADDRESS RECEIVER - CHANNEL 1, BIT 5	3
R126	1T004A	ADDRESS RECEIVER - CHANNEL 1, BIT 6	3
R127	1T004B	ADDRESS RECEIVER - CHANNEL 1, BIT 7	3
R128	1T005A	ADDRESS RECEIVER - CHANNEL 1, BIT 8	3
R129	1T005B	ADDRESS RECEIVER - CHANNEL 1, BIT 9	3
R130	1T006A	ADDRESS RECEIVER - CHANNEL 1, BIT 10	3
R131	1T006B	ADDRESS RECEIVER - CHANNEL 1, BIT 11	3
R132	1T007A	ADDRESS RECEIVER - CHANNEL 1, BIT 12	3
R133	1T008A	BANK SELECT RECEIVER - CHANNEL 1, BIT 1	3
R134	1T008B	BANK SELECT RECEIVER - CHANNEL 1, BIT 2	3
R135	1T009A	BANK SELECT RECEIVER - CHANNEL 1, BIT 3	3
R140	1T016B	DATA RECEIVER - CHANNEL 1, BIT 0	3
R141	1T017B	DATA RECEIVER - CHANNEL 1, BIT 1	3
R142	1T018B	DATA RECEIVER - CHANNEL 1, BIT 2	3
R143	1T019B	DATA RECEIVER - CHANNEL 1, BIT 3	3
R144	1T020B	DATA RECEIVER - CHANNEL 1, BIT 4	3
R145	1T021B	DATA RECEIVER - CHANNEL 1, BIT 5	3
R146	1T022B	DATA RECEIVER - CHANNEL 1, BIT 6	3
R147	1T023B	DATA RECEIVER - CHANNEL 1, BIT 7	3
R148	1T024B	DATA RECEIVER - CHANNEL 1, BIT 8	3
R149	1T025B	DATA RECEIVER - CHANNEL 1, BIT 9	3
R150	1T026B	DATA RECEIVER - CHANNEL 1, BIT 10	3
R151	1T027B	DATA RECEIVER - CHANNEL 1, BIT 11	3
R152	1T028B	DATA RECEIVER - CHANNEL 1, BIT 12	3
R160	1T007B	REQUEST MEMORY RECEIVER - CHANNEL 1	3
R161	1T013B	READ RECEIVER - CHANNAL 1	3
R162	1T014B	WRITE RECEIVER - CHANNAL 1	3
R163	1T015B	PARTIAL WRITE RECEIVER - CHANNEL 1	3
R164	**1T009B**	MASTER CLEAR RECEIVER - CHANNEL 1	3
R220	1R001A	ADDRESS RECEIVER - CHANNEL 2, BIT 0	3
R221	1R001B	ADDRESS RECEIVER - CHANNEL 2, BIT 1	3
R222	1R002A	ADDRESS RECEIVER - CHANNEL 2, BIT 2	3
R223	1R002B	ADDRESS RECEIVER - CHANNEL 2, BIT 3	3
R224	1R003A	ADDRESS RECEIVER - CHANNEL 2, BIT 4	3
R225	1R003B	ADDRESS RECEIVER - CHANNEL 2, BIT 5	3
R226	1R004A	ADDRESS RECEIVER - CHANNEL 2, BIT 6	3
R227	1R004B	ADDRESS RECEIVER - CHANNEL 2, BIT 7	3
R228	1R005A	ADDRESS RECEIVER - CHANNEL 2, BIT 8	3
R229	1R005B	ADDRESS RECEIVER - CHANNEL 2, BIT 9	3
R230	1R006A	ADDRESS RECEIVER - CHANNEL 2, BIT 10	3
R231	1R006B	ADDRESS RECEIVER - CHANNEL 2, BIT 11	3
R232	1R007A	ADDRESS RECEIVER - CHANNEL 2, BIT 12	3
R233	1R008A	BANK SELECT RECEIVER - CHANNEL 2 BIT 1	3
R234	1R008B	BANK SELECT RECEIVER - CHANNEL 2 BIT 2	3
R235	1R009A	BANK SELECT RECEIVER - CHANNEL 2 BIT 3	3
R240	1R016B	DATA RECEIVER - CHANNEL 2, BIT 0	3
R241	1R017B	DATA RECEIVER - CHANNEL 2, BIT 1	3
R242	1R018B	DATA RECEIVER - CHANNEL 2, BIT 2	3
R243	1R019B	DATA RECEIVER - CHANNEL 2, BIT 3	3
R244	1R020B	DATA RECEIVER - CHANNEL 2, BIT 4	3
R245	1R021B	DATA RECEIVER - CHANNEL 2, BIT 5	3
R246	1R022B	DATA RECEIVER - CHANNEL 2, BIT 6	3
R247	1R023B	DATA RECEIVER - CHANNEL 2, BIT 7	3
R248	1R024B	DATA RECEIVER - CHANNEL 2, BIT 8	3
R249	1R025B	DATA RECEIVER - CHANNEL 2, BIT 9	3
R250	1R026B	DATA RECEIVER - CHANNEL 2, BIT 10	3
R251	1R027B	DATA RECEIVER - CHANNEL 2, BIT 11	3
R252	1R028B	DATA RECEIVER - CHANNEL 2, BIT 12	3
R260	1R007B	REQUEST MEMORY, CHANNEL 2	3
R261	1R013B	SELECT READ, CHANNEL 2	3
R262	1R014B	WRITE RECEIVER - CHANNEL 2	3
R263	1R015B	PARTIAL WRITE RECEIVER-CHANNEL 2	3
R264	**1R009B**	MASTER CLEAR RECEIVER - CHANNEL 2	3
R320	1P001A	ADDRESS RECEIVER - CHANNEL 3, BIT 0	3
R321	1P001B	ADDRESS RECEIVER - CHANNEL 3, BIT 1	3
R322	1P002A	ADDRESS RECEIVER - CHANNEL 3, BIT 2	3
R323	1P002B	ADDRESS RECEIVER - CHANNEL 3, BIT 3	3
R324	1P003A	ADDRESS RECEIVER - CHANNEL 3, BIT 4	3
R325	1P003B	ADDRESS RECEIVER - CHANNEL 3, BIT 5	3
R326	1P004A	ADDRESS RECEIVER - CHANNEL 3, BIT 6	3
R327	1P004B	ADDRESS RECEIVER - CHANNEL 3, BIT 7	3
R328	1P005A	ADDRESS RECEIVER - CHANNEL 3, BIT 8	3
R329	1P005B	ADDRESS RECEIVER - CHANNEL 3, BIT 9	3
R330	1P006A	ADDRESS RECEIVER - CHANNEL 3, BIT 10	3
R331	1P006B	ADDRESS RECEIVER - CHANNEL 3, BIT 11	3
R332	1P007A	ADDRESS RECEIVER - CHANNEL 3, BIT 12	3
R333	1P008A	BANK SELECT RECEIVER - CHANNEL 3, BIT 1	3
R334	1P008B	BANK SELECT RECEIVER - CHANNEL 3, BIT 2	3
R335	1P009A	BANK SELECT RECEIVER - CHANNEL 3, BIT 3	3
R340	1P016B	DATA RECEIVER - CHANNEL 3, BIT 0	3
R341	1P017B	DATA RECEIVER - CHANNEL 3, BIT 1	3
R342	1P018B	DATA RECEIVER - CHANNEL 3, BIT 2	3
R343	1P019B	DATA RECEIVER - CHANNEL 3, BIT 3	3
R344	1P020B	DATA RECEIVER - CHANNEL 3, BIT 4	3
R345	1P021B	DATA RECEIVER - CHANNEL 3, BIT 5	3
R346	1P022B	DATA RECEIVER - CHANNEL 3, BIT 6	3
R347	1P023B	DATA RECEIVER - CHANNEL 3, BIT 7	3
R348	1P024B	DATA RECEIVER - CHANNEL 3, BIT 8	3
R349	1P025B	DATA RECEIVER - CHANNEL 3, BIT 9	3
R350	1P026B	DATA RECEIVER - CHANNEL 3, BIT 10	3
R351	1P027B	DATA RECEIVER - CHANNEL 3, BIT 11	3
R352	1P028B	DATA RECEIVER - CHANNEL 3, BIT 12	3
R360	1P007B	REQUEST MEMORY - CHANNEL 3	3
R361	1P013B	SELECT READ - CHANNEL 3	3
R362	1P014B	WRITE RECEIVER - CHANNEL 3	3
R363	1P015B	PARTIAL WRITE RECEIVER - CHANNEL 3	3
R364	**1P009B**	MASTER CLEAR RECEIVER - CHANNEL 3	3
R800	10014A	I TO Z PULSE SHAPER	5
S004	1I001A	S PRIME REGISTOR BIT 0	6
S005	1I001B	S PRIME REGISTOR BIT 0	6
S014	1I002A	S PRIME REGISTOR BIT 1	6
S015	1I002B	S PRIME REGISTOR BIT 1	6
S024	1I003A	S PRIME REGISTOR BIT 2	6
S025	1I003B	S PRIME REGISTOR BIT 2	6
S034	1I004A	S PRIME REGISTOR BIT 3	6
S035	1I004B	S PRIME REGISTOR BIT 3	6
S044	1I005A	S PRIME REGISTOR BIT 4	6
S045	1I005B	S PRIME REGISTOR BIT 4	6
S054	1I006A	S PRIME REGISTOR BIT 5	6
S055	1I006B	S PRIME REGISTOR BIT 5	6
S064	1I007A	S PRIME REGISTOR BIT 6	6
S065	1I007B	S PRIME REGISTOR BIT 6	6
S074	1I008A	S PRIME REGISTOR BIT 7	6
S075	1I008B	S PRIME REGISTOR BIT 7	6

S084	1I009A	S PRIME REGISTOR BIT 8	
S085	1I009B	S PRIME REGISTOR BIT 8	
S094	1I010A	S PRIME REGISTOR BIT 9	
S095	1I010B	S PRIME REGISTOR BIT 9	
S100	1M002A	BANK SELECT SW, CHANNEL 1, BIT 0	
S101	1M002B	BANK SELECT SW, CHANNEL 1, BIT 1	
S102	1M002C	BANK SELECT SW, CHANNEL 1, BIT 2	
S104	1I011A	S PRIME REGISTOR BIT 10	
S105	1I011B	S PRIME REGISTOR BIT 10	
S114	1I012A	S PRIME REGISTOR BIT 11	
S115	1I012B	S PRIME REGISTOR BIT 11	
S124	1I013A	S PRIME REGISTOR BIT 12	
S125	1I013B	S PRIME REGISTOR BIT 12	
S160	1M024A	REQUEST ENABLE SW, CHANNEL 1	
S200	1M004A	BANK SELECT SW, CHANNEL 2, BIT 0	
S201	1M004B	BANK SELECT SW, CHANNEL 2, BIT 1	
S202	1M004C	BANK SELECT SW, CHANNEL 2, BIT 2	
S260	1M024B	REQUEST ENABLE SW, CHANNEL 2	
S300	1M006A	BANK SELECT SW, CHANNEL 3, BIT 0	
S301	1M006B	BANK SELECT SW, CHANNEL 3, BIT 1	
S302	1M006C	BANK SELECT SW, CHANNEL 3, BIT 2	
S360	1M024C	REQUEST ENABLE SW, CHANNEL 3	
T140	1T016A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 0	
T141	1T017A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 1	
T142	1T018A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 2	
T143	1T019A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 3	
T144	1T020A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 4	
T145	1T021A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 5	
T146	1T022A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 6	
T147	1T023A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 7	
T148	1T024A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 8	
T149	1T025A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 9	
T150	1T026A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 10	
T151	1T027A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 11	
T152	1T028A	OUTPUT DATA TRANSMITTER - CHANNEL 1, BIT 12	
T155	1T014A	RESUME 1 TRANSMITTER - CHANNEL 1	
T156	1T015A	RESUME 2 TRANSMITTER - CHANNEL 1	
T157	1T013A	PARITY ERROR TRANSMITTER - CHANNEL 1	
T240	1R016A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 0	
T241	1R017A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 1	
T242	1R018A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 2	
T243	1R019A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 3	
T244	1R020A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 4	
T245	1R021A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 5	
T246	1R022A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 6	
T247	1R023A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 7	
T248	1R024A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 8	
T249	1R025A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 9	
T250	1R026A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 10	
T251	1R027A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 11	
T252	1R028A	OUTPUT DATA TRANSMITTER - CHANNEL 2, BIT 12	
T255	1R014A	RESUME 1 TRANSMITTER - CHANNEL 2	
T256	1R015A	RESUME 2 TRANSMITTER - CHANNEL 2	
T257	1R013A	PARITY ERROR TRANSMITTER - CHANNEL 2	
T340	1P016A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 0	
T341	1P017A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 1	
T342	1P018A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 2	
T343	1P019A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 3	
T344	1P020A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 4	
T345	1P021A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 5	
T346	1P022A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 6	
T347	1P023A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 7	
6	T348	1P024A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 8	14
6	T349	1P025A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 9	14
6	T350	1P026A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 10	14
6	T351	1P027A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 11	14
4	T352	1P028A	OUTPUT DATA TRANSMITTER - CHANNEL 3, BIT 12	14
4	T355	1P014A	RESUME 1 TRANSMITTER - CHANNEL 3	14
4	T356	1P015A	RESUME 2 TRANSMITTER - CHANNEL 3	14
6	T357	1P013A	PARITY ERROR TRANSMITTER - CHANNEL 3	14
6	T800	1C015A	XFMR, X DRIVE LINES 0,32	11
6	T801	1D015A	XFMR, X DRIVE LINES 1,33	11
6	T802	1C015B	XFMR, X DRIVE LINES 2,34	11
6	T803	1D015B	XFMR, X DRIVE LINES 3,35	11
6	T804	1C014A	XFMR, X DRIVE LINES 4,36	11
4	T805	1D014A	XFMR, X DRIVE LINES 5,37	11
4	T806	1C014B	XFMR, X DRIVE LINES 6,38	11
4	T807	1D014B	XFMR, X DRIVE LINES 7,39	11
4	T808	1C005A	XFMR, X DRIVE LINES 8,40	11
4	T809	1D005A	XFMR, X DRIVE LINES 9,41	11
4	T810	1C005B	XFMR, X DRIVE LINES 10,42	11
4	T811	1D005B	XFMR, X DRIVE LINES 11,43	11
4	T812	1C004A	XFMR, X DRIVE LINES 12,44	11
4	T813	1D004A	XFMR, X DRIVE LINES 13,45	11
14	T814	1C004B	XFMR, X DRIVE LINES 14,46	11
14	T815	1D004B	XFMR, X DRIVE LINES 15,47	11
14	T816	1C013A	XFMR, X DRIVE LINES 16,48	11
14	T817	1D013A	XFMR, X DRIVE LINES 17,49	11
14	T818	1C013B	XFMR, X DRIVE LINES 18,50	11
14	T819	1D013B	XFMR, X DRIVE LINES 19,51	11
14	T820	1C012A	XFMR, X DRIVE LINES 20,52	11
14	T821	1D012A	XFMR, X DRIVE LINES 21,53	11
14	T822	1C012B	XFMR, X DRIVE LINES 22,54	11
14	T823	1D012B	XFMR, X DRIVE LINES 23,55	11
14	T824	1C003A	XFMR, X DRIVE LINES 24,56	11
14	T825	1D003A	XFMR, X DRIVE LINES 25,57	11
14	T826	1C003B	XFMR, X DRIVE LINES 26,58	11
14	T827	1D003B	XFMR, X DRIVE LINES 27,59	11
14	T828	1C002A	XFMR, X DRIVE LINES 28,60	11
14	T829	1D002A	XFMR, X DRIVE LINES 29,61	11
14	T830	1C002B	XFMR, X DRIVE LINES 30,62	11
14	T831	1D002B	XFMR, X DRIVE LINES 31,63	11
14	T900	1E012A	XFMR, Y DRIVE LINES 0,32	12
14	T901	1E018A	XFMR, Y DRIVE LINES 1,33	12
14	T902	1E012B	XFMR, Y DRIVE LINES 2,34	12
14	T903	1E018B	XFMR, Y DRIVE LINES 3,35	12
14	T904	1E011A	XFMR, Y DRIVE LINES 4,36	12
14	T905	1E017A	XFMR, Y DRIVE LINES 5,37	12
14	T906	1E011B	XFMR, Y DRIVE LINES 6,38	12
14	T907	1E017B	XFMR, Y DRIVE LINES 7,39	12
14	T908	1E006A	XFMR, Y DRIVE LINES 8,40	12
14	T909	1F019A	XFMR, Y DRIVE LINES 9,41	12
14	T910	1E006B	XFMR, Y DRIVE LINES 10,42	12
14	T911	1F019B	XFMR, Y DRIVE LINES 11,43	12
14	T912	1E005A	XFMR, Y DRIVE LINES 12,44	12
	T913	1F018A	XFMR, Y DRIVE LINES 13,45	12
14	T914	1E005B	XFMR, Y DRIVE LINES 14,46	12
14	T915	1F018B	XFMR, Y DRIVE LINES 15,47	12
14	T916	1E010A	XFMR, Y DRIVE LINES 16,48	12
14	T917	1E016A	XFMR, Y DRIVE LINES 17,49	12
14	T918	1E010B	XFMR, Y DRIVE LINES 18,50	12
14	T919	1E016B	XFMR, Y DRIVE LINES 19,51	12
14	T920	1E009A	XFMR, Y DRIVE LINES 20,52	12
14	T921	1E015A	XFMR, Y DRIVE LINES 21,53	12

T922	1E009B	XFMR, Y DRIVE LINES 22,54	12
T923	1E015B	XFMR, Y DRIVE LINES 23,55	12
T924	1E004A	XFMR, Y DRIVE LINES 24,56	12
T925	1F017A	XFMR, Y DRIVE LINES 25,57	12
T926	1E004B	XFMR, Y DRIVE LINES 26,58	12
T927	1F017B	XFMR, Y DRIVE LINES 27,59	12
T928	1E003A	XFMR, Y DRIVE LINES 28,60	12
T929	1F016A	XFMR, Y DRIVE LINES 29,61	12
T930	1E003B	XFMR, Y DRIVE LINES 30,62	12
T931	1F016B	XFMR, Y DRIVE LINES 31,63	12
T964	1F005A	XFMR, Y DRIVE LINES 64,96	13
T965	1G018A	XFMR, Y DRIVE LINES 65,97	13
T966	1F005B	XFMR, Y DRIVE LINES 66,98	13
T967	1G018B	XFMR, Y DRIVE LINES 67,99	13
T968	1F004A	XFMR, Y DRIVE LINES 68,100	13
T969	1G017A	XFMR, Y DRIVE LINES 69,101	13
T970	1F004B	XFMR, Y DRIVE LINES 70,102	13
T971	1G017B	XFMR, Y DRIVE LINES 71,103	13
T972	1G006A	XFMR, Y DRIVE LINES 72,104	13
T973	1G012A	XFMR, Y DRIVE LINES 73,105	13
T974	1G006B	XFMR, Y DRIVE LINES 74,106	13
T975	1G012B	XFMR, Y DRIVE LINES 75,107	13
T976	1G005A	XFMR, Y DRIVE LINES 76,108	13
T977	1G011A	XFMR, Y DRIVE LINES 77,109	13
T978	1G005B	XFMR, Y DRIVE LINES 78,110	13
T979	1G011B	XFMR, Y DRIVE LINES 79,111	13
T980	1F003A	XFMR, Y DRIVE LINES 80,112	13
T981	1G016A	XFMR, Y DRIVE LINES 81,113	13
T982	1F003B	XFMR, Y DRIVE LINES 82,114	13
T983	1G016B	XFMR, Y DRIVE LINES 83,115	13
T984	1F002A	XFMR, Y DRIVE LINES 84,116	13
T985	1G015A	XFMR, Y DRIVE LINES 85,117	13
T986	1F002B	XFMR, Y DRIVE LINES 86,118	13
T987	1G015B	XFMR, Y DRIVE LINES 87,119	13
T988	1G004A	XFMR, Y DRIVE LINES 88,120	13
T989	1G010A	XFMR, Y DRIVE LINES 89,121	13
T990	1G004B	XFMR, Y DRIVE LINES 90,122	13
T991	1G010B	XFMR, Y DRIVE LINES 91,123	13
T992	1G003A	XFMR, Y DRIVE LINES 92,124	13
T993	1G009A	XFMR, Y DRIVE LINES 93,125	13
T994	1G003B	XFMR, Y DRIVE LINES 94,126	13
T995	1G009B	XFMR, Y DRIVE LINES 95,127	13
W100	10003B	ENABLE R TO S,CH 1	4
W101	10006B	ENABLE R TO S,CH 1	4
W102	10013B	INPUT ENABLE,OUTPUT GATE,CH 1	4
W103	10019B	ENABLE R TO Z, CHANNEL 1	4
W104	10025B	ENABLE R TO Z, CHANNEL 1	4
W110	1S020B	OUTPUT DATA GATE TO CHANNEL 1 FROM CHASSIS 1	14
W111	1S026B	OUTPUT DATA GATE TO CHANNEL 1 FROM CHASSIS 1	14
W112	1T010B	R1, R2, PE GATE TO CHANNEL 1 FROM CHASSIS 1	14
W120	1S021B	OUTPUT DATA GATE TO CHANNEL 1 FROM CHASSIS 2	14
W121	1S027B	OUTPUT DATA GATE TO CHANNEL 1 FROM CHASSIS 2	14
W122	1T011B	R1, R2, PE GATE TO CHANNEL 1 FROM CHASSIS 2	14
W130	1S022B	OUTPUT DATA GATE TO CHANNEL 1 FROM CHASSIS 3	14
W131	1S028B	OUTPUT DATA GATE TO CHANNEL 1 FROM CHASSIS 3	14
W132	1T012B	R1, R2, PE GATE TO CHANNEL 1 FROM CHASSIS 3	14
W200	10002B	ENABLE R TO S,CH 2	4
W201	10005B	ENABLE R TO S,CH 2	4
W202	10012B	INPUT ENABLE,OUTPUT GATE,CH 2	4
W203	10018B	ENABLE R TO Z, CHANNEL 2	4
W204	10024B	ENABLE R TO Z, CHANNEL 2	4
W210	1S020A	OUTPUT DATA GATE TO CHANNEL 2 FROM CHASSIS 1	14
W211	1S026A	OUTPUT DATA GATE TO CHANNEL 2 FROM CHASSIS 1	14
W212	1R010B	R1, R2, PE GATE TO CHANNEL 2 FROM CHASSIS 1	14
W220	1S021A	OUTPUT DATA GATE TO CHANNEL 2 FROM CHASSIS 2	14
W221	1Q027B	OUTPUT DATA GATE TO CHANNEL 2 FROM CHASSIS 2	14
W222	1R011B	R1, R2, PE GATE TO CHANNEL 2 FROM CHASSIS 2	14
W230	1Q022B	OUTPUT DATA GATE TO CHANNEL 2 FROM CHASSIS 3	14
W231	1Q028B	OUTPUT DATA GATE TO CHANNEL 2 FROM CHASSIS 3	14
W232	1R012B	R1, R2, PE GATE TO CHANNEL 2 FROM CHASSIS 3	14
W300	10001B	ENABLE R TO S,CH 3	4
W301	10004B	ENABLE R TO S,CH 3	4
W302	10011B	INPUT ENABLE,OUTPUT GATE,CH 3	4
W303	10017B	ENABLE R TO Z, CHANNEL 3	4
W304	10023B	ENABLE R TO Z, CHANNEL 3	4
W310	10020B	OUTPUT DATA GATE TO CHANNEL 3 FROM CHASSIS 1	14
W311	10026B	OUTPUT DATA GATE TO CHANNEL 3 FROM CHASSIS 1	14
W312	1P010B	R1, R2, PE GATE TO CHANNEL 3 FROM CHASSIS 1	14
W320	10021B	OUTPUT DATA GATE TO CHANNEL 3 FROM CHASSIS 2	14
W321	10027B	OUTPUT DATA GATE TO CHANNEL 3 FROM CHASSIS 2	14
W322	1P011B	R1, R2, PE GATE TO CHANNEL 3 FROM CHASSIS 2	14
W330	10022B	OUTPUT DATA GATE TO CHANNEL 3 FROM CHASSIS 3	14
W331	10028B	OUTPUT DATA GATE TO CHANNEL 3 FROM CHASSIS 3	14
W332	1P012B	R1, R2, PE GATE TO CHANNEL 3 FROM CHASSIS 3	14
W850	1F021A	ENABLE SENSE,BANK 0	10
W851	1E021B	ENABLE SENSE,BANK 0	10
W852	1F021A	ENABLE SENSE,BANK 1	10
W853	1F021B	EEABLE SENSE,BANK 1	10
Y000	1C022A	SENSE AMP BANK 0 BIT 0	7
Y001	1F022A	SENSE AMP BANK 1 BIT 0	7
Y010	1D022A	SENSE AMP BANK 0 BIT 1	8
Y011	1F022A	SENSE AMP BANK 1 BIT 1	8
Y020	1C023A	SENSE AMP BANK 0 BIT 2	7
Y021	1E023A	SENSE AMP BANK 1 BIT 2	7
Y030	1D023A	SENSE AMP BANK 0 BIT 3	8
Y031	1F023A	SENSE AMP BANK 1 BIT 3	8
Y040	1C024A	SENSE AMP BANK 0 BIT 4	7
Y041	1E024A	SENSE AMP BANK 1 BIT 4	7
Y050	1D024A	SENSE AMP BANK 0 BIT 5	8
Y051	1F024A	SENSE AMP BANK 1 BIT 5	8
Y060	1C025A	SENSE AMP BANK 0 BIT 6	7
Y061	1E025A	SENSE AMP BANK 1 BIT 6	7
Y070	1D025A	SENSE AMP BANK 0 BIT 7	8
Y071	1F025A	SENSE AMP BANK 1 BIT 7	8
Y080	1C026A	SENSE AMP BANK 0 BIT 8	7
Y081	1E026A	SENSE AMP BANK 1 BIT 8	7
Y090	1D026A	SENSE AMP BANK 0 BIT 9	8
Y091	1F026A	SENSE AMP BANK 1 BIT 9	8
Y100	1C027A	SENSE AMP BANK 0 BIT 10	7
Y101	1E027A	SENSE AMP BANK 1 BIT 10	7
Y110	1D027A	SENSE AMP BANK 0 BIT 11	8
Y111	1F027A	SENSE AMP BANK 1 BIT 11	8
Y120	1C028A	SENSE AMP BANK 0 BIT 12	7
Y121	1E028A	SENSE AMP BANK 1 BIT 12	7
Y130	1D028A	SENSE AMP BANK 0 PARITY BIT 13	8
Y131	1F028A	SENSE AMP BANK 1 PARITY BIT 13	8
Z000	1I015A	Z REGISTER BIT 0	7
Z001	1I015B	Z REGISTER BIT 0	7
Z010	1I016A	Z REGISTER BIT 1	8
Z011	1I016B	Z REGISTER BIT 1	8
Z020	1I017A	Z REGISTER BIT 2	7
Z021	1I017B	Z REGISTER BIT 2	7
Z030	1I018A	Z REGISTER BIT 3	8
Z031	1I018B	Z REGISTER BIT 3	8

Z040	1I019A	Z REGISTER BIT 4	7
Z041	1I019B	Z REGISTER BIT 4	7
Z050	1I020A	Z REGISTER BIT 5	8
Z051	1I020B	Z REGISTER BIT 5	8
Z060	1I021A	Z REGISTER BIT 6	7
Z061	1I021B	Z REGISTER BIT 6	7
Z070	1I022A	Z REGISTER BIT 7	8
Z071	1I022B	Z REGISTER BIT 7	8
Z080	1I023A	Z REGISTER BIT 8	7
Z081	1I023B	Z REGISTER BIT 8	7
Z090	1I024A	Z REGISTER BIT 9	8
Z091	1I024B	Z REGISTER BIT 9	8
Z100	1I025A	Z REGISTER BIT 10	7
Z101	1I025B	Z REGISTER BIT 10	7
Z110	1I026A	Z REGISTER BIT 11	8
Z111	1I026B	Z REGISTER BIT 11	8
Z120	1I027A	Z REGISTER BIT 12	7
Z121	1I027B	Z REGISTER BIT 12	7
Z130	1I028A	Z REGISTER PARITY BIT 13	8
Z131	1I028B	Z REGISTER PARITY BIT 13	8

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO [illegible]	11/68	[illegible]
B		SEE ECO CB [illegible]	10-69	[illegible]

NOTES:

1. INTERPRET TO ENGINEERING STANDARD 3:01.002 "PREPARATION OF LOGIC DIAGRAMS."

2. CONNECTOR NUMBERS SHOWN ARE INTERPRETED IN THE FOLLOWING MANNER:

   A. TRANSMITTER OUTPUTS AND RECEIVER INPUTS ARE TWISTED PAIR WIRES. THE SECOND WIRE OF A TWISTED PAIR IS THE NEXT HIGHER DIGIT OF THE PIN NUMBER SHOWN.

   CONNECTOR PIN NO. NO. — J003 A01 → R120

   TWO CONNECTORS ARE ASSOCIATED WITH EACH TRANSMITTER AND RECEIVER. THE SECOND CONNECTOR HAS THE SAME PIN NUMBER AS SHOWN, AND IS THE CONNECTOR NUMBER OBTAINED BY ADDING THE DIGIT 3 TO THE GIVEN CONNECTOR NUMBER. THUS THE SECOND CONNECTOR AND PIN ASSOCIATED WITH R120 IS J006 A01, EXAMPLE A.

   B. CONNECTOR PIN NO. NO. — J009 C01 → T155

3.A. THE PLACEMENT NUMBERS FOR THE R AND T TERMS LOCATED IN THE ACCESS CHANNEL GATING LOGIC ARE PRECEDED BY THE DIGIT 1, 2, OR 3. THIS DIGIT REPRESENTS THE CHASSIS NUMBER, EXAMPLE A. TERMS WHICH ARE COMMON TO ALL ACCESS CHANNELS USE THE STANDARD PLACEMENT NUMBER INTERPRETATION, EXAMPLE B.

   CHASSIS NUMBER → 1T13B

   B. D 06 A
   D: VERTICAL COORDINATE
   06: HORIZONTAL COORDINATE
   A: CARD CIRCUIT

4. △ LOGIC DESIGNATED BY THIS SYMBOL IS OMITTED IN A 8492 (3 CHANNELS)

5. △ LOGIC DESIGNATED BY THIS SYMBOL IS OMITTED IN A 8493 . (3 CHANNELS)

6. THE FOLLOWING IS A LIST OF THE SUBTITLES AND THE SHEET NO'S OF EACH:

SUBTITLE	SHEET NO.
STATUS SHEET	1
BLOCK DIAGRAM	2
INPUT GATING. CHASSIS 1	3
SCANNER & SCANNER CONTROL	4
MEMORY CYCLE	5
S' REGISTER	6
Z REGISTER EVEN BITS	7
Z REGISTER ODD BITS	8
PARITY & MASTER CLEAR LOGIC	9
MODE AND INHIBIT CONTROL	10
X DRIVE	11
Y DRIVE	12
Y DRIVE	13
OUTPUT GATING, CHASSI	14

7. LOGIC DIAGRAMS CORRESPOND TO REV. B OF DOCUMENT NUMBER 16901400 (MEMORY BANK MECHANIZED DESIGN DATA)

B	—	—	—	—	—	—	—	—	—	B	B	—	—
A	—	—	—	—	—	—	—	—	—	—	—	—	—
SH1	SH2	SH3	SH4	SH5	SH6	SH7	SH8	SH9	SH10	SH11	SH12	SH13	SH14

REVISION STATUS OF SHEETS

16901200 SHEET 1 OF 14

A AC7491

NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES ON
FRACTIONS: ± — DECIMALS: ± — ANGLES: ± —
DO NOT SCALE DRAWING
MATERIAL

CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA

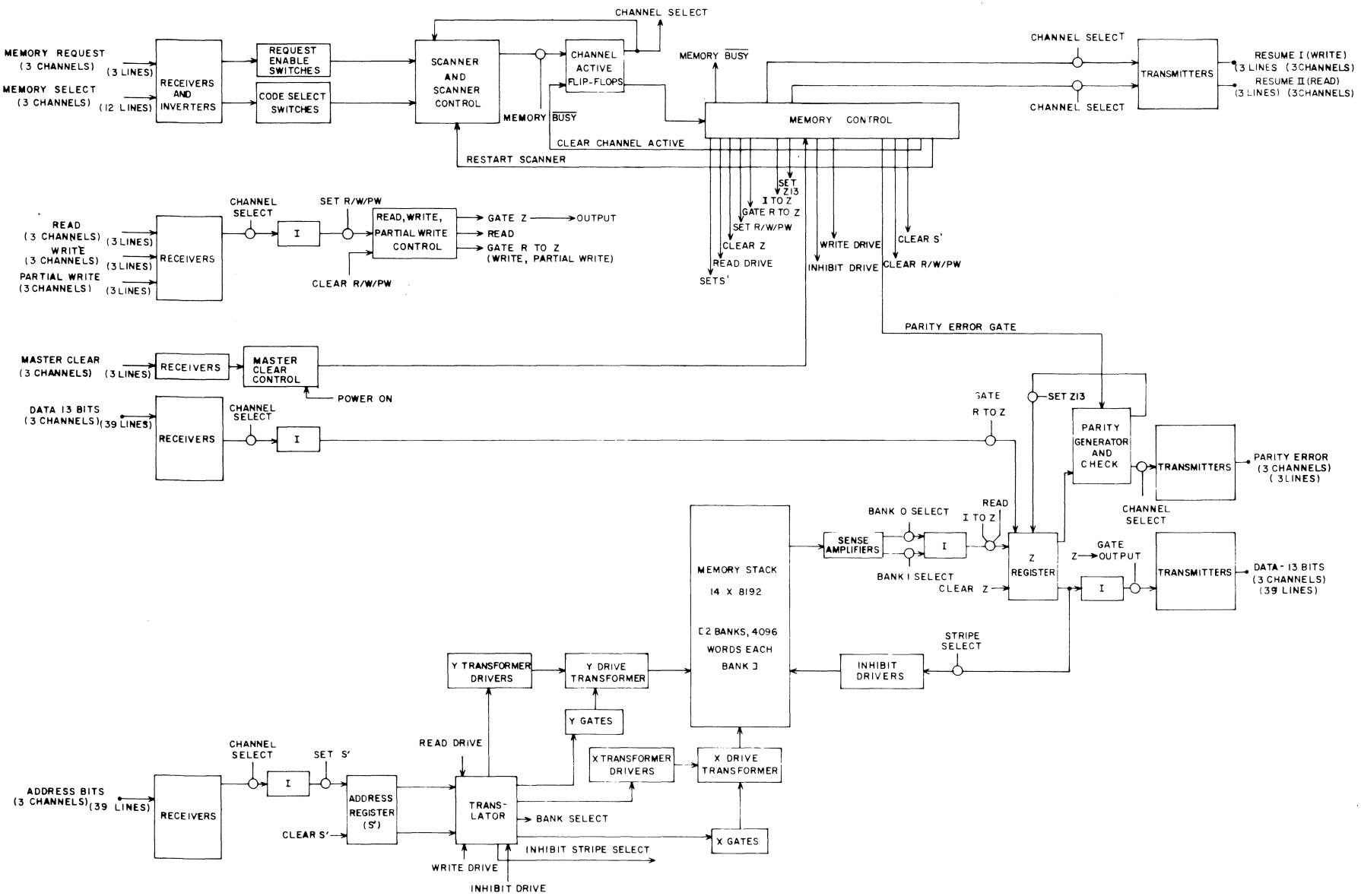
CONTRACT		
APPROVED	[signature]	5-4-67
ENGINEER	[signature]	5-4-67
CHECKED	[signature]	4-24-67
DRAWN	[signature]	2-22-67
APPROVED		
APPROVED		

TITLE
MEMORY UNIT
LOGIC DIAGRAM

SIZE	CODE IDENT NO.	DRAWING NO.
C	27963	16901200

SCALE — SHEET 1 OF 14

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

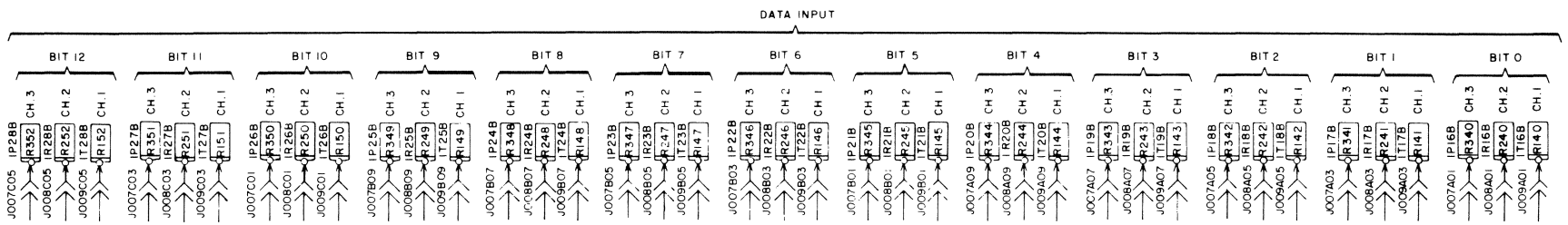


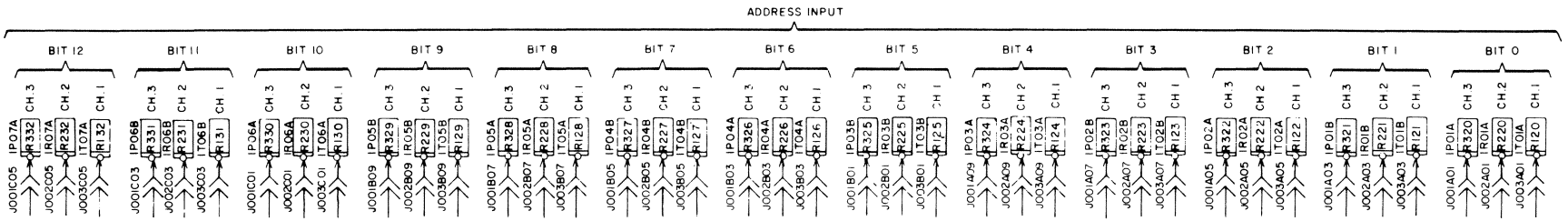
BLOCK DIAGRAM

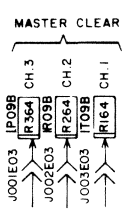
CODE IDENT NO	SIZE	DRAWING NO
27963	C	16901200
SCALE		SHEET 2

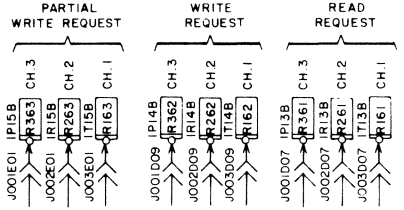
16901200 SHEET 2

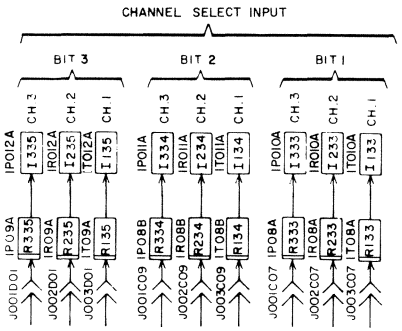
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED

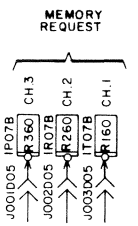










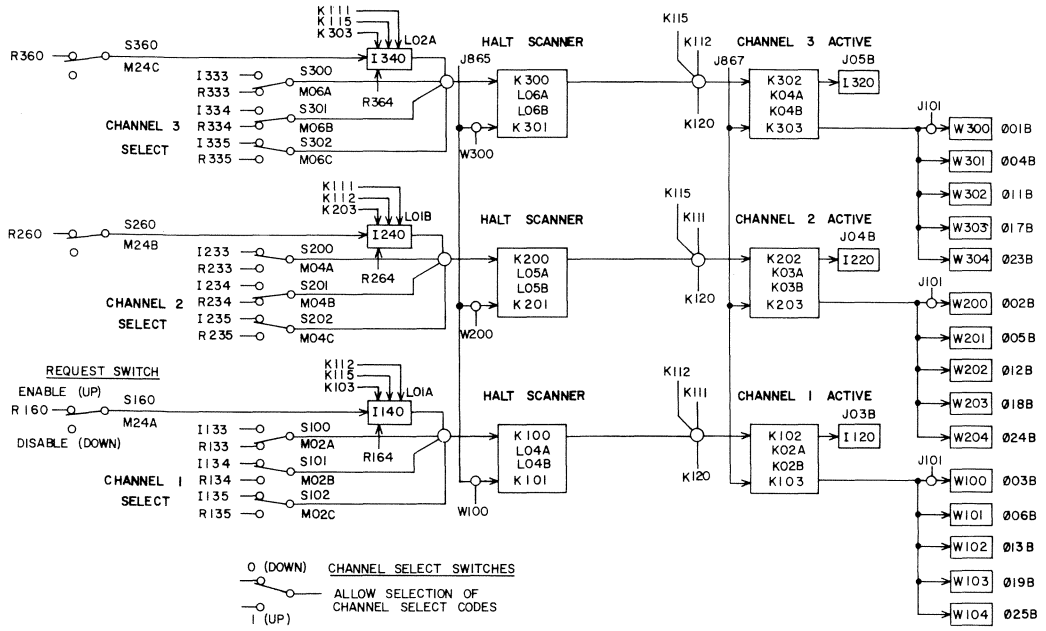


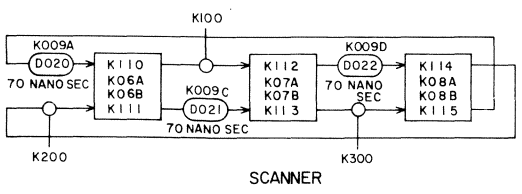
INPUT GATING CHASSIS I

CODE IDENT NO	SIZE	DRAWING NO
27963	C	16901200
SCALE		SHEET 3

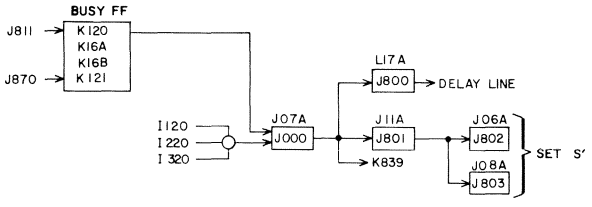
16901200 SHEET 3

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED





SCANNER



SCANNER AND SCANNER CONTROLS

SIZE	CODE IDENT. NO.	DRAWING NO.
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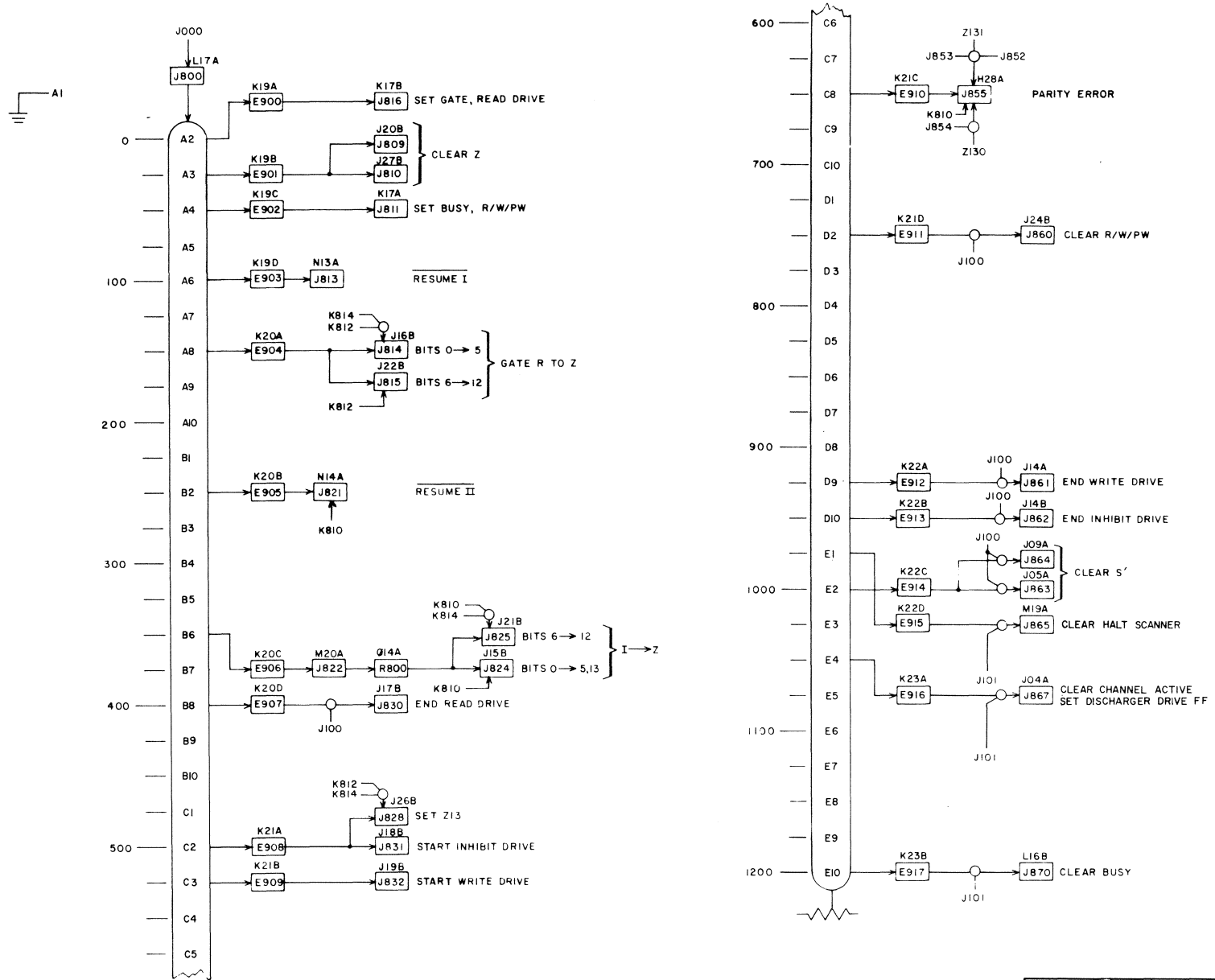
SCALE		SHEET 4

16901200 SHEET 4

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



MEMORY CYCLE

CODE IDENT. NO.	SIZE	DRAWING NO.
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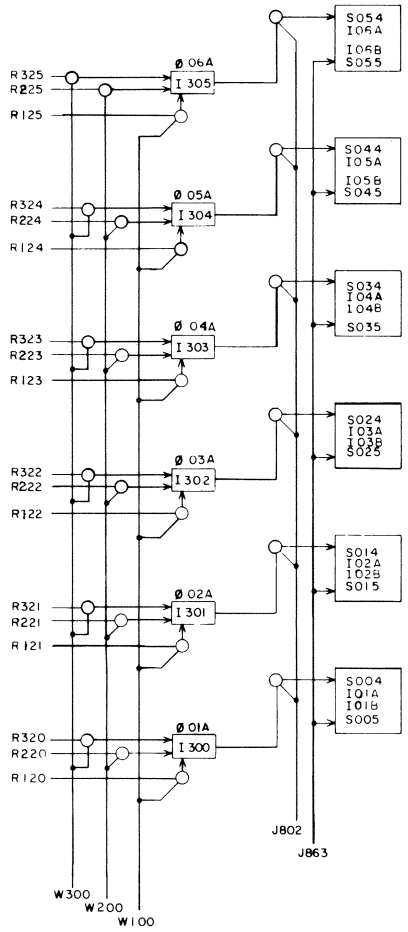
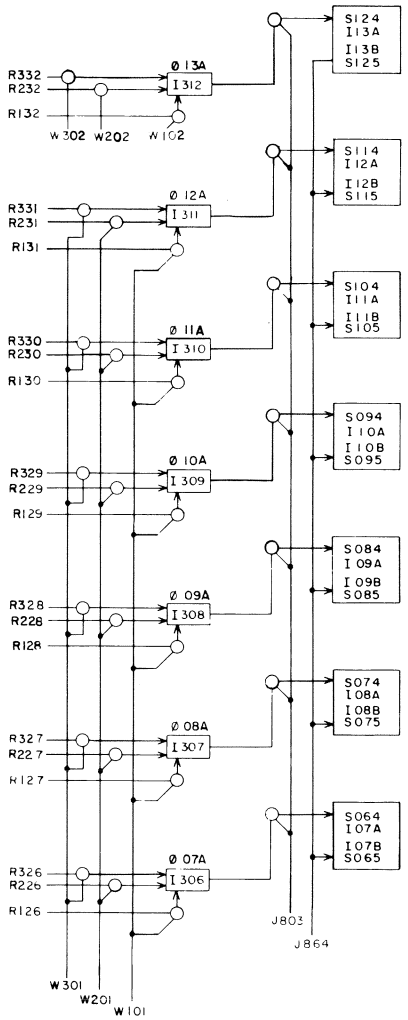
SCALE		SHEET 5

16901200
SHEET 5

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



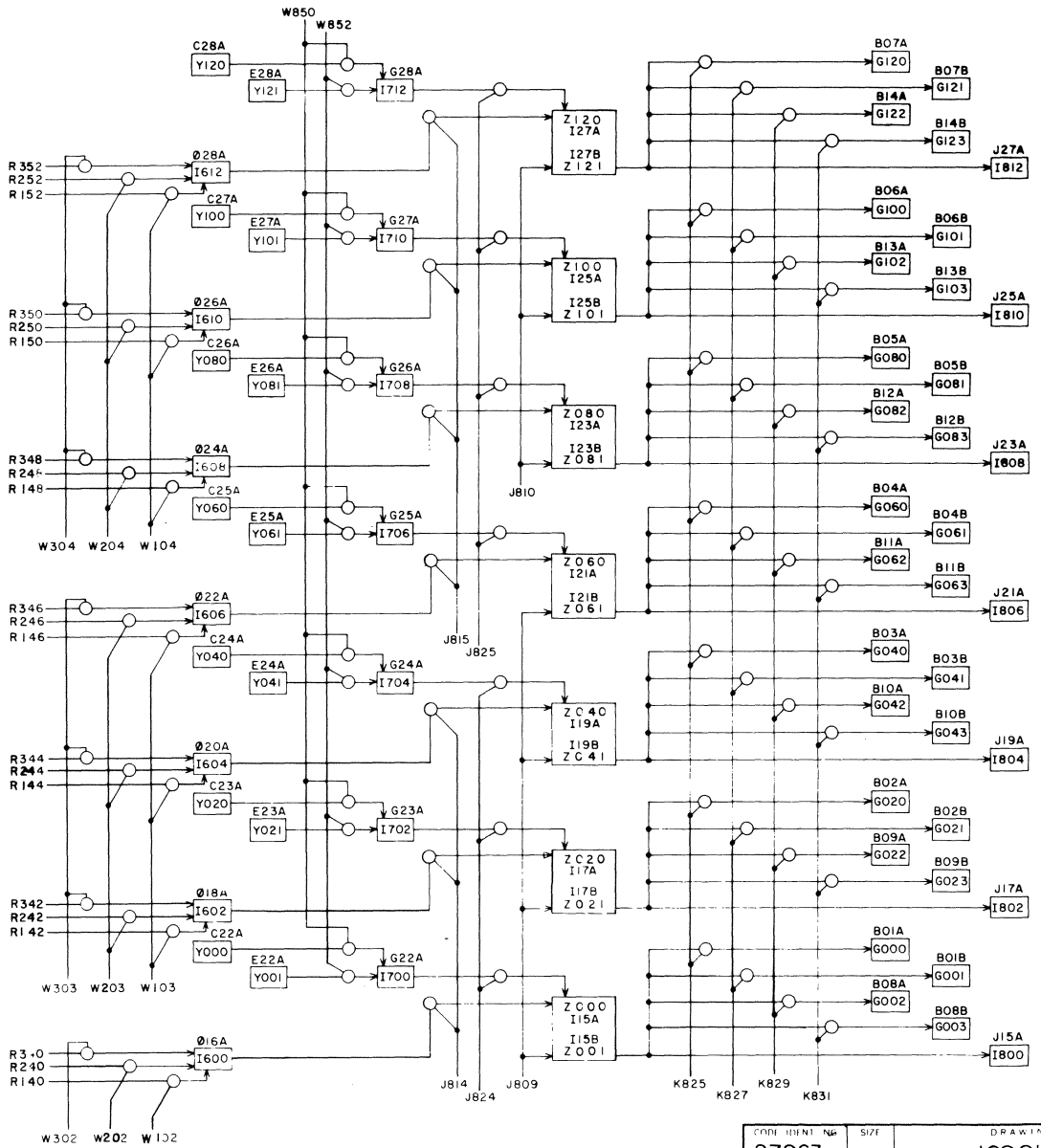


S' REGISTER

27963	C	16901200	
SCALE			6

16901200
SHEET 6

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



Z REGISTER – EVEN BITS

CODE IDENT NO	SIZE	DRAWING NO
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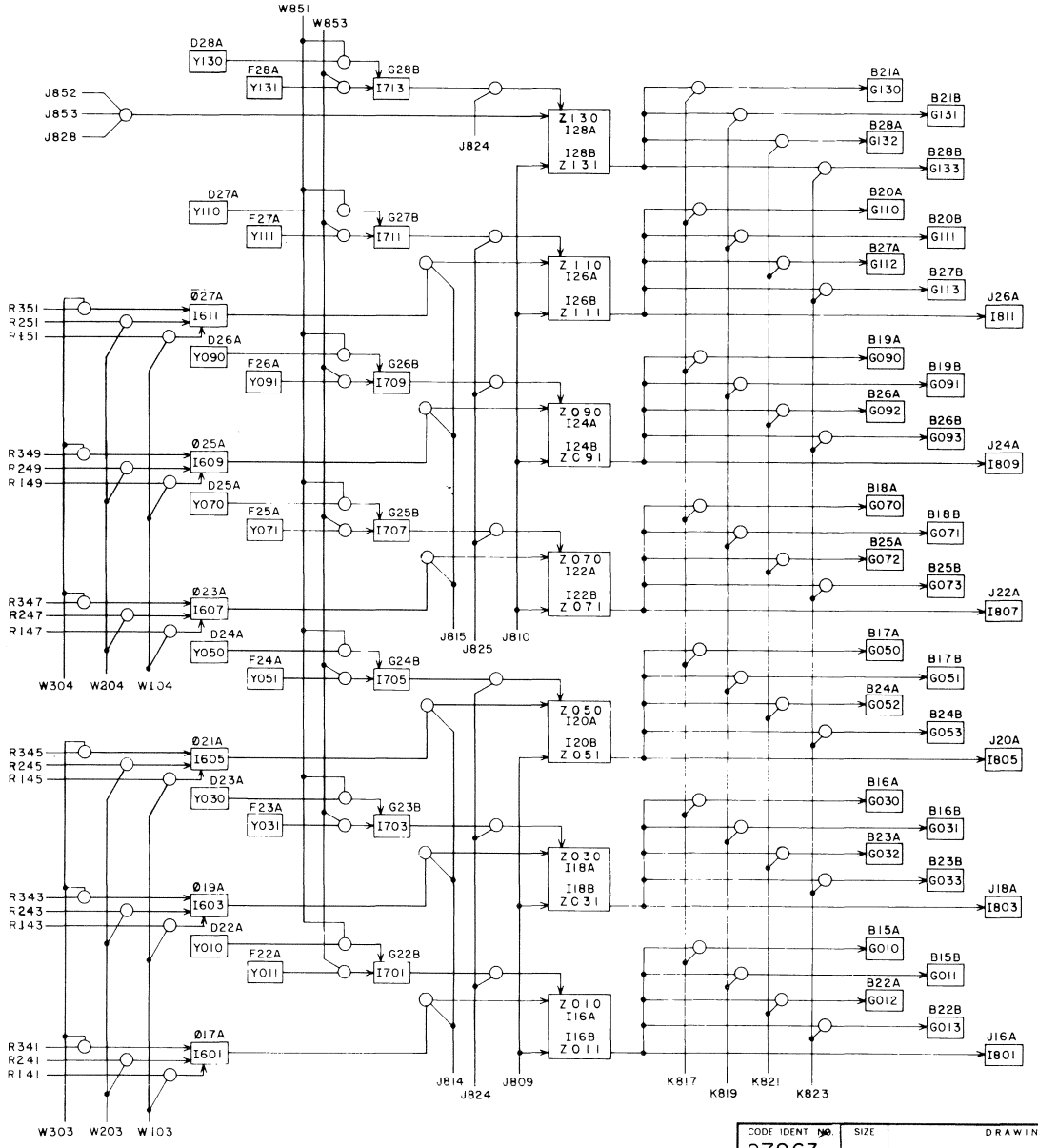
SCALE		SHEET 7

16901200
SHEET 7

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



Z REGISTER - ODD BITS

CODE IDENT NO.	SIZE	DRAWING NO
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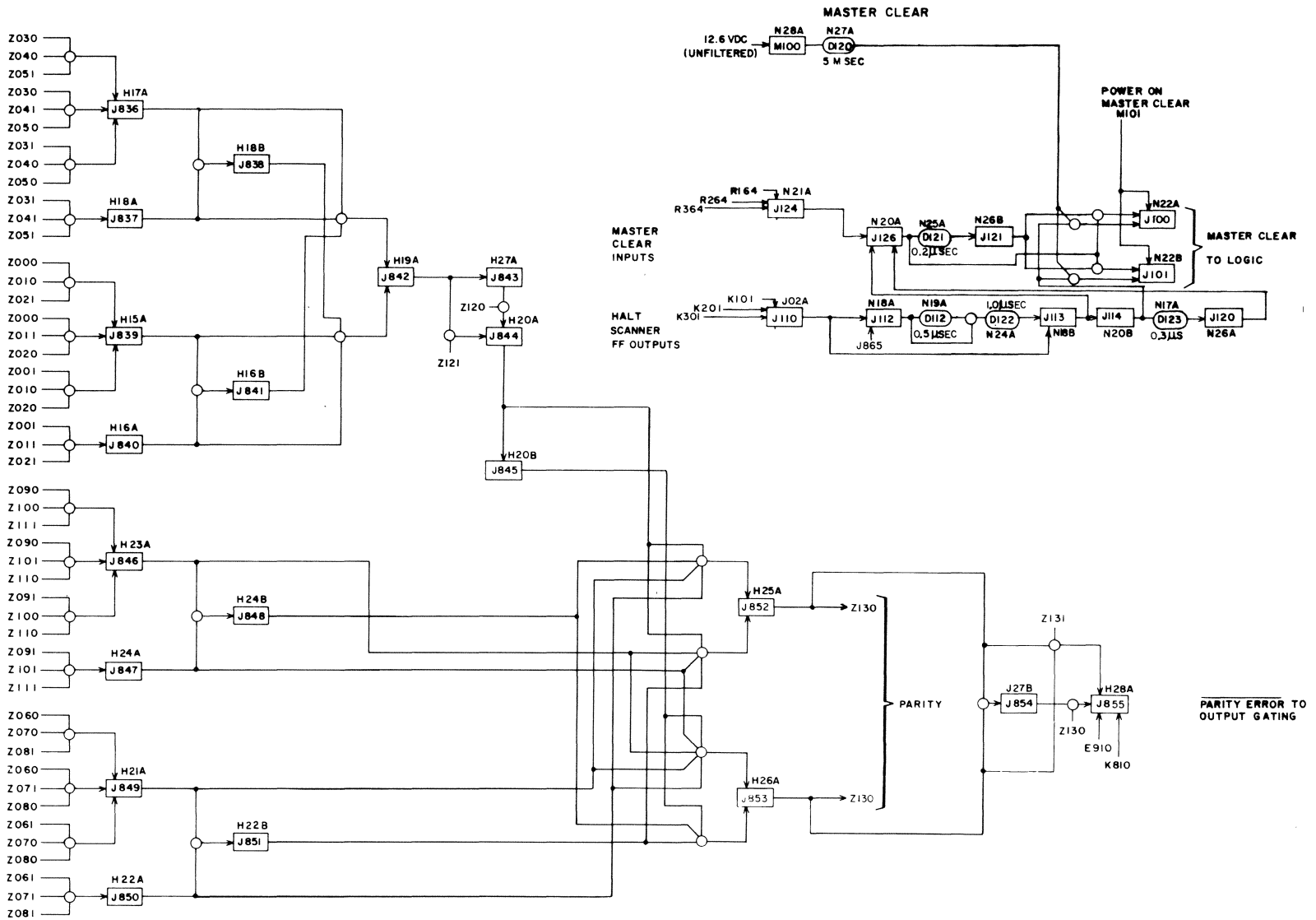
SCALE		SHEET 8

16901200 SHEET 8

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



PARITY AND MASTER CLEAR

CODE IDENT NO	SIZE	DRAWING NO
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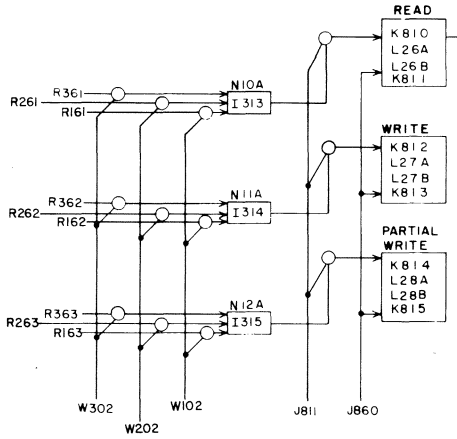
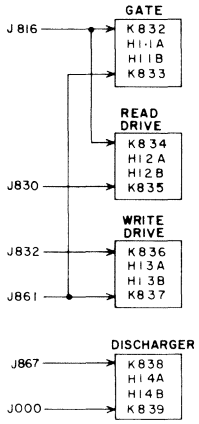
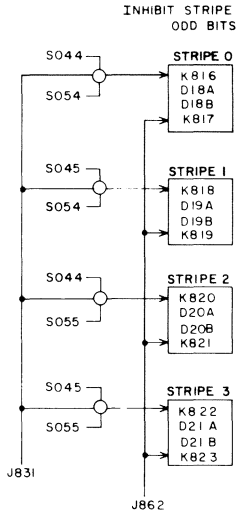
SCALE		SHEET 9

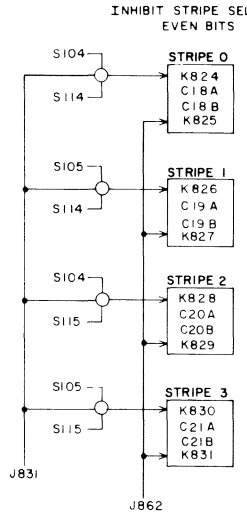
16901200 SHEET 9

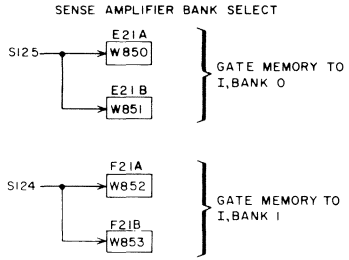
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED











16901200
SHEET 10

MODE AND INHIBIT CONTROL LOGIC

CODE IDENT NO	SIZE	DRAWING NO
27963	C	16901200
SCALE		SHEET 10

REVISIONS				
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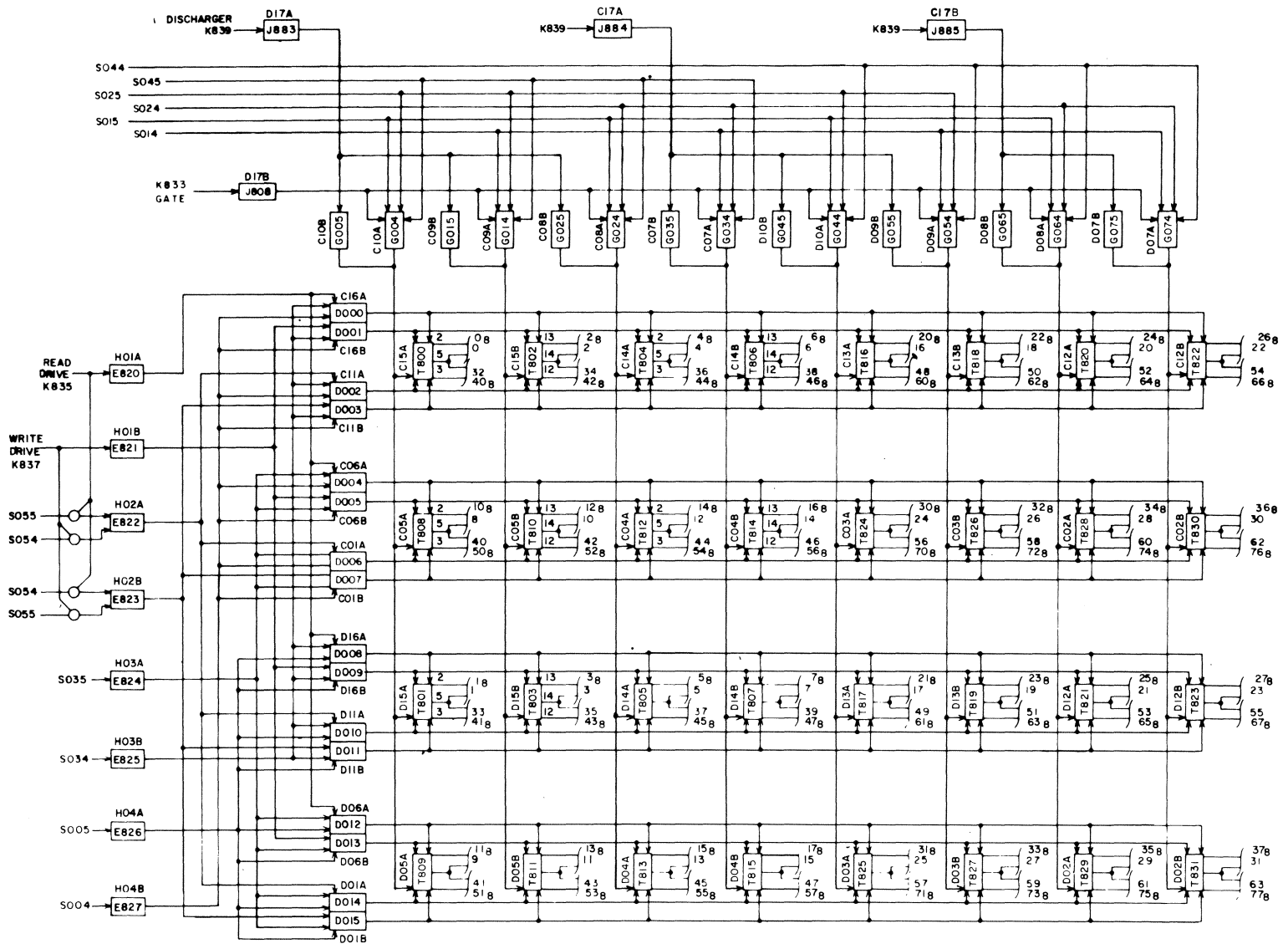

X DRIVE SELECTION

CODE IDENT NO	SIZE	DRAWING NO
27963	C	16901200
SCALE		SHEET 11

16901200 SHEET 11

REVISIONS				
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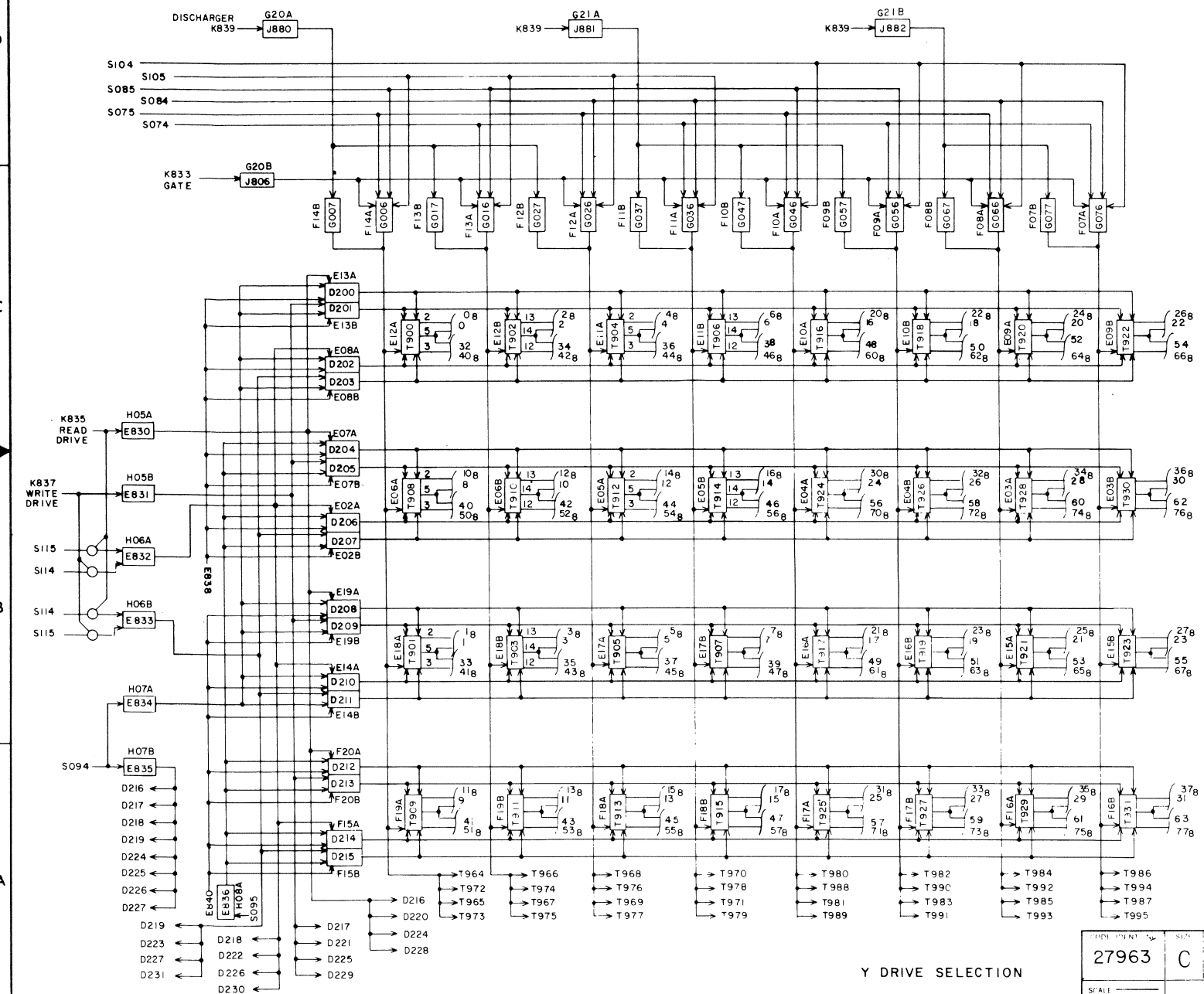

Y DRIVE SELECTION

DRAWING NO. 27963	SIZE C	16901200	
SCALE	SHEET 12		

16901200 SHEET 12

REVISIONS				
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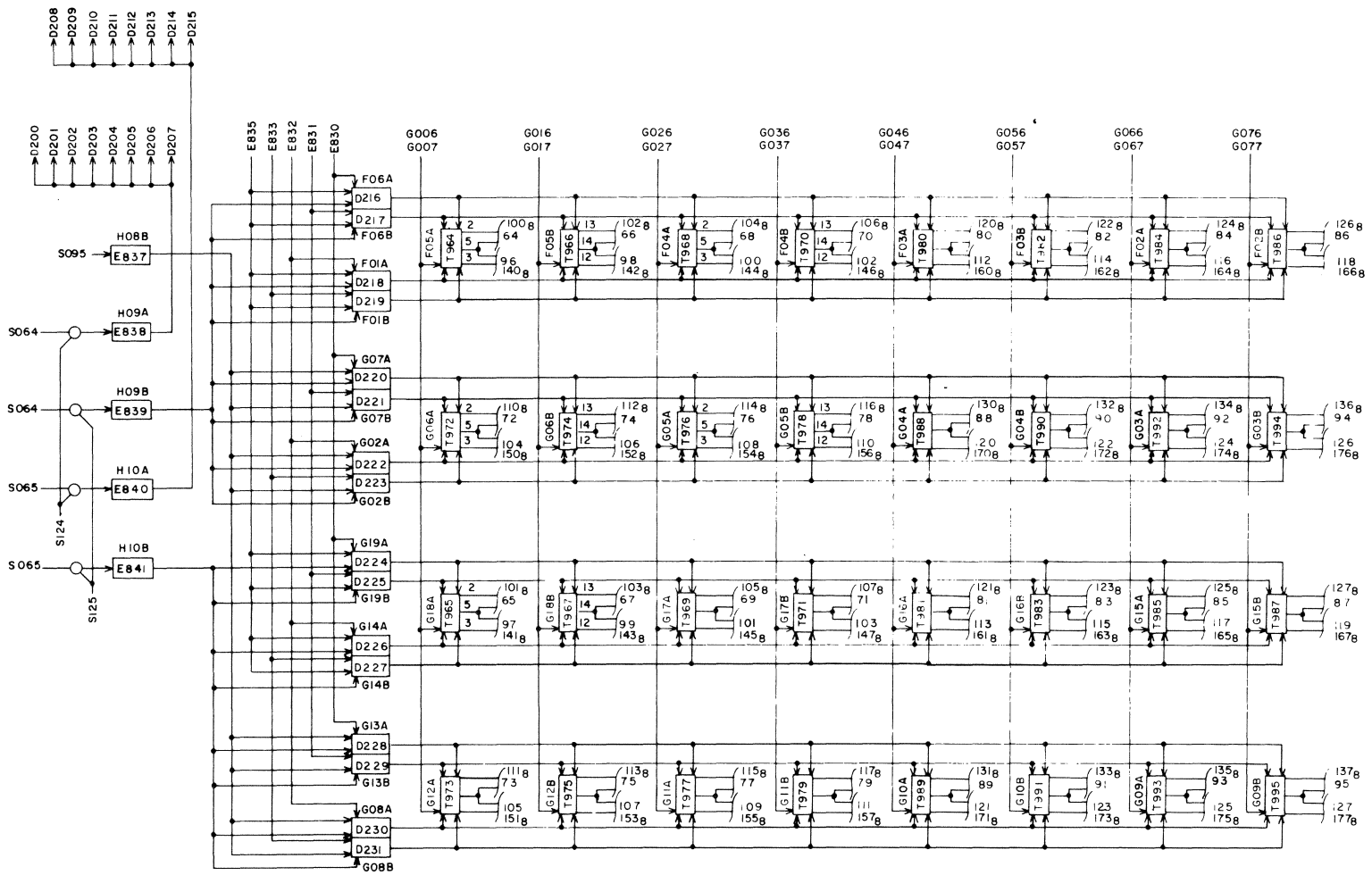
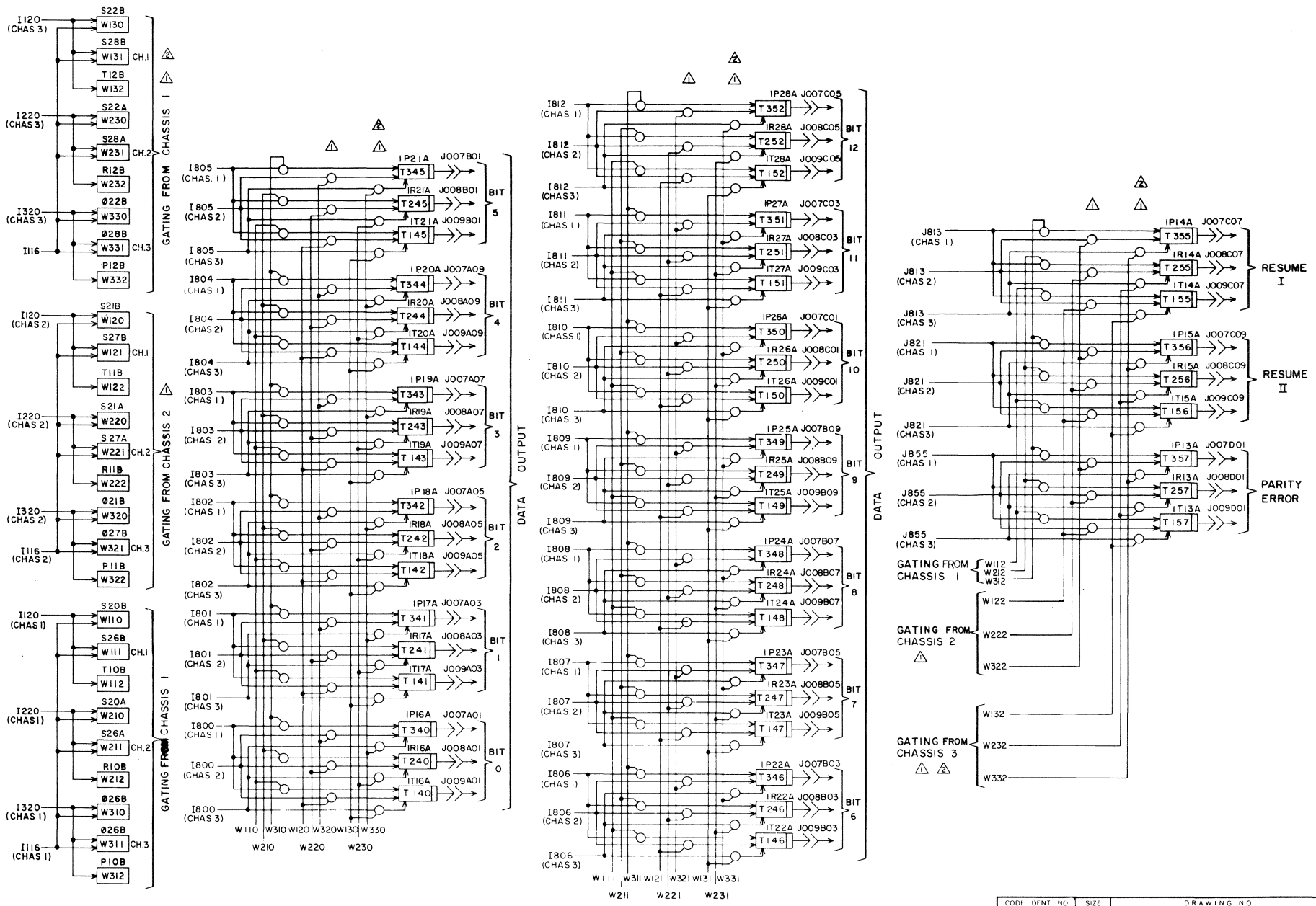


Y DRIVE SELECTION

CODE IDENT. NO.	SIZE	DRAWING NO.
27963	C	16901200
SCALE		SHEET 13

16901200
SHEET 13

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED



OUTPUT GATING CHASSIS I

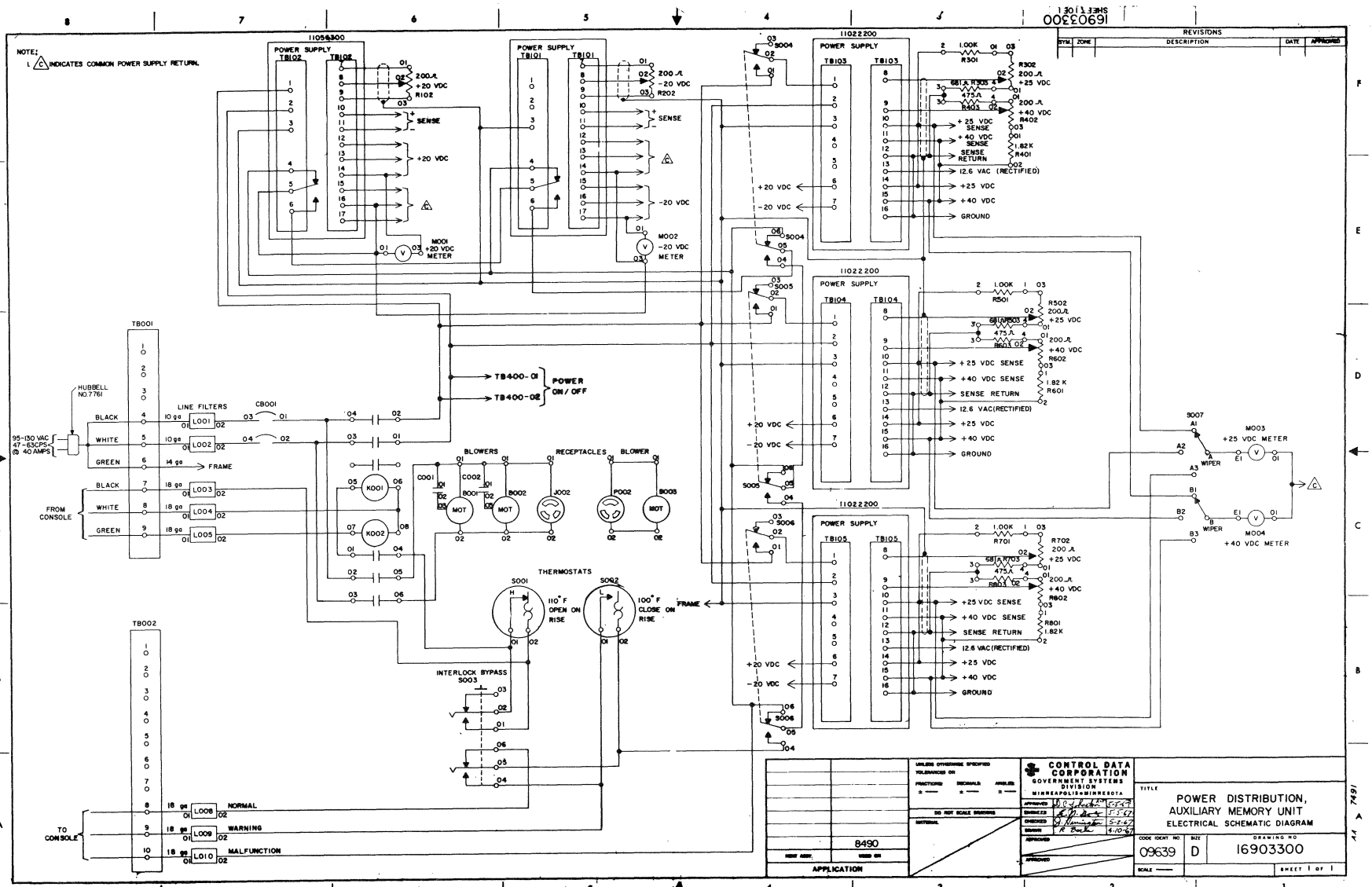
CODE IDENT NO	SIZE	DRAWING NO
27963	C	16901200
SCALE		SHEET 14

16901200 SHEET 14

SECTION 2

AUXILIARY MEMORY UNIT

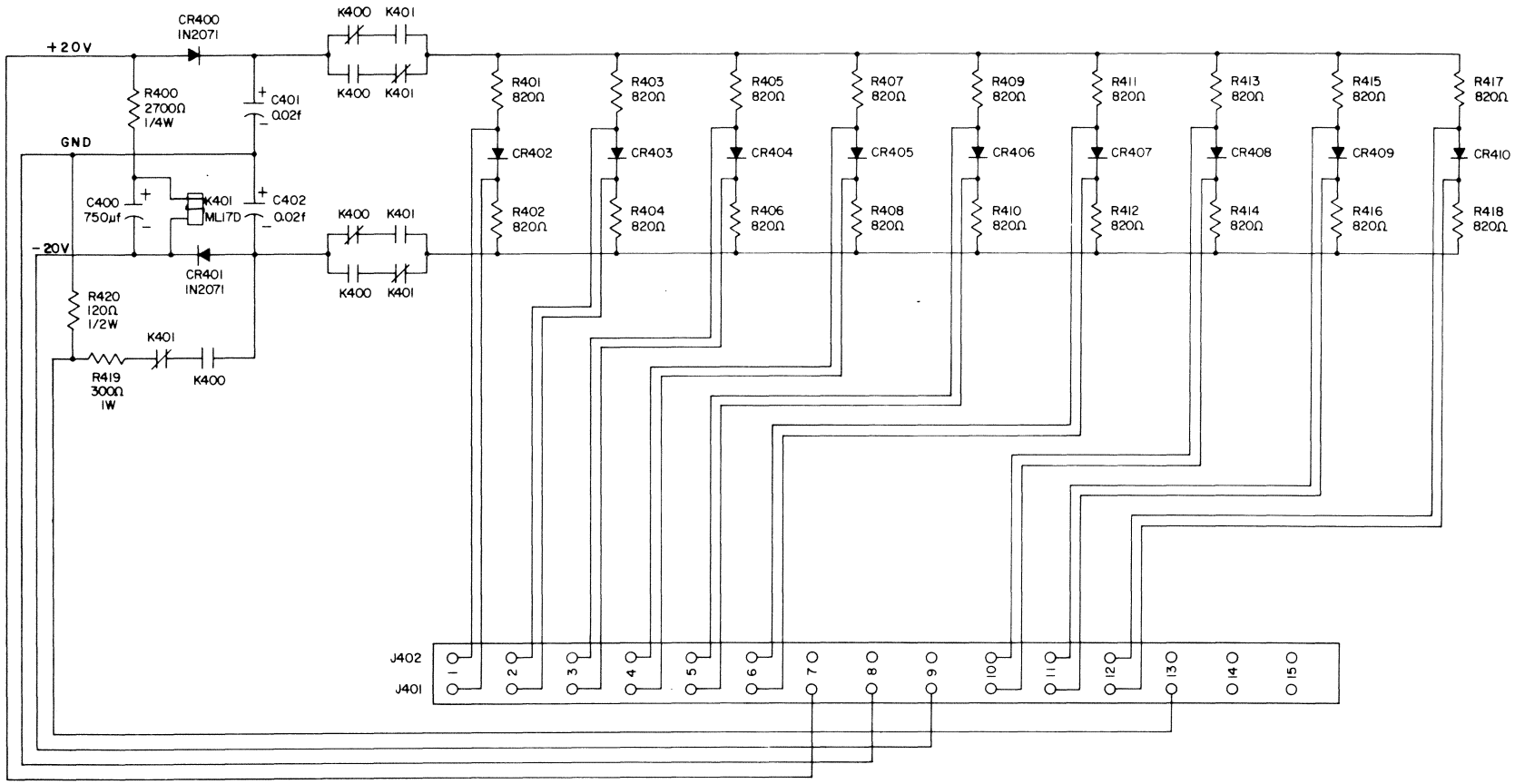
POWER DISTRIBUTION AND MCS PROTECTION DRAWINGS

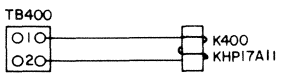

NOTE:
1. △G INDICATES COMMON POWER SUPPLY RETURN.
11054300
POWER SUPPLY TB102
TB102
200Ω +20 VDC R102
SENSE
+20 VDC
MO01 +20 VDC METER
POWER SUPPLY TB101
TB101
200Ω -20 VDC R202
SENSE
-20 VDC
MO02 -20 VDC METER
11022200
POWER SUPPLY TB103
TB103
R301 100K
R302 200Ω +25 VDC
R303 681Ω 475Ω
R402 200Ω +40 VDC
+25 VDC SENSE
+40 VDC SENSE
SENSE RETURN
R401 1.82K
12.6 VAC (RECTIFIED)
+25 VDC
+40 VDC
GROUND
+20 VDC
-20 VDC
S004
POWER SUPPLY TB104
TB104
R501 100K
R502 200Ω +25 VDC
R503 681Ω 475Ω
R602 200Ω +40 VDC
+25 VDC SENSE
+40 VDC SENSE
SENSE RETURN
R601 1.82K
12.6 VAC(RECTIFIED)
+25 VDC
+40 VDC
GROUND
+20 VDC
-20 VDC
S005
POWER SUPPLY TB105
TB105
R701 100K
R702 200Ω +25 VDC
R703 681Ω 475Ω
R802 200Ω +40 VDC
+25 VDC SENSE
+40 VDC SENSE
SENSE RETURN
R801 1.82K
12.6 VAC(RECTIFIED)
+25 VDC
+40 VDC
GROUND
+20 VDC
-20 VDC
S006
S007
MO03 +25 VDC METER
MO04 +40 VDC METER
A WIPER
B WIPER
TB001
HUBBELL NO.7761
95-130 VAC 47-63CPS @ 40 AMPS
LINE FILTERS
CB001
BLACK
WHITE
GREEN
10 ga
14 ga
18 ga
FRAME
FROM CONSOLE
L001
L002
L003
L004
L005
TB400-01
TB400-02
POWER ON / OFF
BLOWERS
RECEPTACLES
BLOWER
K001
K002
C001
C002
B001
B002
J002
P002
B003
MOT
THERMOSTATS
S001
110°F OPEN ON RISE
S002
100°F CLOSE ON RISE
INTERLOCK BYPASS S003
TB002
TO CONSOLE
L008 NORMAL
L009 WARNING
L010 MALFUNCTION
REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS 10 MINNESOTA
TITLE
POWER DISTRIBUTION, AUXILIARY MEMORY UNIT
ELECTRICAL SCHEMATIC DIAGRAM
CODE IDENT NO. 09639
SIZE D
DRAWING NO. 16903300
SCALE
SHEET 1 OF 1
NEXT ASSY. 8490
USED ON
APPLICATION
DO NOT SCALE DRAWING
MATERIAL
APPROVED
CHECKED
DRAWN
APPROVED
16903300 SHEET 1 OF 1
7491 A1

NOTES:

1. ALL DIODES CONTROL DATA CORPORATION 1180290O UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE ¼W±5% UNLESS OTHERWISE SPECIFIED.

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED





8490	
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES ON
FRACTIONS: ± —— DECIMALS: ± —— ANGLES: ± ——
DO NOT SCALE DRAWING
MATERIAL

CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA

CONTRACT		
APPROVED	[illegible]	5-5-67
ENGINEER	[illegible]	5-5-67
CHECKED	[illegible]	5-2-67
DRAWN	R Boulet	4-10-67
APPROVED		
APPROVED		

TITLE
POWER ON/OFF, MCS PROTECTION
AUXILIARY MEMORY UNIT
ELECTRICAL SCHEMATIC DIAGRAM

CODE IDENT. NO.	SIZE	DRAWING NO.
09639	C	16902200
SCALE ——		SHEET 1 OF 1

16902200

AA 7491

SECTION 3

I/O UNIT

THEORY OF OPERATION

SECTION 3

INPUT/OUTPUT UNIT

The 8495 I/O Unit provides additional data channels for the basic 8490 system. Each I/O Unit contains two buffered, bidirectional data channels designated channel 2 and channel 3. A maximum of five peripheral equipments may be connected to each data channel. The I/O Unit also has provisions for controlling memory-to-memory data transfers without intervention from the Compute Unit. However, the I/O Unit requires information from the Compute Unit to initiate I/O activity.

The basic cabinet configuration can also be altered to include an I/O Unit and one or two banks of memory. The 8496 I/O and Memory Unit contains an I/O Unit and one memory bank (8,192 storage locations); the 8497 I/O and Memory Unit contains an I/O Unit and two banks of memory (16,384 storage locations). Both of these cabinet configurations contain all the control circuitry necessary to operate the individual units.

GENERAL THEORY OF OPERATION

Figure 3-1 is a simplified, functional block diagram of an I/O Unit. This diagram presents only channel 2 and the logic which is common to both channels 2 and 3. The following descriptions consider the functional operation of an I/O Unit with respect to the various types of operations which involve this unit. All of the discussions, except memory-to-memory transfer, assume operation on channel 2, since a given operation is identical for either channel.

EXTERNAL FUNCTION

The 8490 selects an external equipment or requests its status by an external function. For equipment attached to the channels in an I/O Unit, this EF code

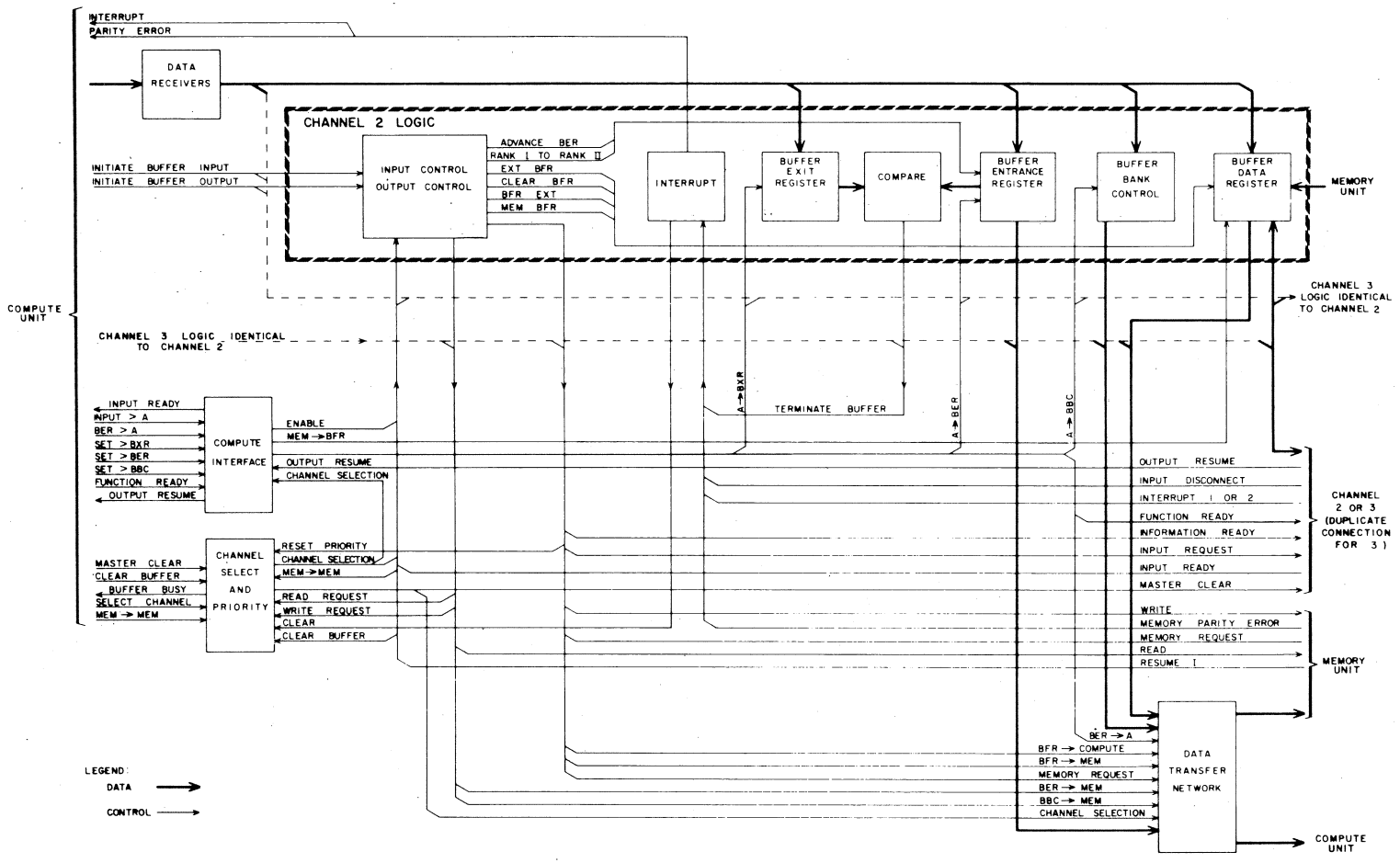


Figure 3-1. I/O Unit Simplified Functional Block Diagram

and the necessary control signals are transmitted to the I/O Unit. If the I/O Unit has been previously cleared by an internal or external control signal, the correct channel select signal enables the priority circuitry for an EF operation. When the EF code is available on the data lines from the Compute Unit, the Compute Unit transmits a function ready signal to the I/O Unit. This signal conditions the compute interface control logic to generate the signal which gates the EF code into the BFR. A signal from the compute interface control logic also enables the I/O control logic to generate the signal which gates the EF code out of the BFR onto the data lines to the external equipment. After the EF code has been sensed, the external equipment returns an output resume signal to the I/O Unit. This signal is transmitted to the Compute Unit by the I/O Unit. When the Compute Unit receives the output resume, the function ready and data signals are removed.

INPUT TO A

In response to an EF status request by the Compute Unit, the external equipment generates a status response code. An input-to-A operation is required to transmit this code from the external equipment through the channel 2 logic to the Compute Unit. Channel 2 must be selected by the channel select code from the Compute Unit. The sequence of events is initiated by an input-to-A signal from the Compute Unit. This signal causes the compute interface control logic to enable the I/O control logic. The I/O control logic sends an input request to the external equipment. This signal causes the external equipment to place the status word on the data lines and to generate an input ready signal. When this signal is received by the I/O control logic, the input request signal is removed and the data is gated into the BFR. The I/O control logic then gates the contents of the BFR onto the data lines to the Compute Unit. After the status word has been received by the Compute Unit, the input-to-A signal ceases. The removal of this signal results in the clearing of the channel 2 BFR and I/O control logic.

INTERRUPT

The I/O Unit contains separate interrupt logic for each channel. Two external interrupt lines and an input disconnect line are associated with each channel. Any of these lines may be activated by any equipment serviced by the channel. Each channel also contains provisions for a buffer termination interrupt. At the end of a buffer, as determined by the compare logic, a terminate buffer signal is sent to the interrupt logic. Whenever any interrupt is active, the correct interrupt signal is sent to the Compute Unit. This signal causes the Compute Unit to perform the routine necessary to satisfy the interrupt. Input disconnect and buffer termination signals also result in a clear signal to the channel selection and priority logic. This signal frees channel 2 for the next I/O operation involving this channel.

INPUT BUFFER

For an input buffer, the I/O Unit buffers data from an input device into a selected block of memory locations in a Memory Unit. A select channel code from the Compute Unit determines which channel will be affected by control signals from the Compute Unit. However, prior to the initiation of the input buffer, the Compute Unit sets the FWA in the BER, the LWA + 1 in the BXR, and the bank designation in the BBC for channel 2. The data for the registers and control is transmitted, one word at a time, over the data lines and placed in the proper register or control. These words control the address selection for each data word and the repetition of the buffer operation.

When an initiate buffer input signal arrives, the channel select and priority logic and the I/O control logic are conditioned for an input buffer operation. As a result of this signal, the I/O control logic sends an input request signal to the input equipment. When the input word is placed on the data lines to the BFR, the input equipment sends an input ready signal to the I/O Unit. As a result of this signal, the I/O control logic removes the input request, gates the input word into the BFR, and sends a write signal to the Memory Unit. The I/O control logic then places the contents of the BER, BBC, and BFR on the data lines to the Memory Unit and sends a memory request to the Memory Unit. This signal causes the Memory Unit to store the data word at the address specified by the contents of the BER in the bank designated by the contents of the BBC.

After the data has been stored, the Memory Unit returns a resume I signal to the I/O control logic. This logic then generates the signals necessary to increase the contents of the BER by one, clear the BFR, and generate another input request. When the next input ready signal is received by the input equipment, the preceding steps are repeated for the next input word. This process is repeated for each input word until the contents of the BER equals the contents of the BXR. When they are equal, the compare logic sends a terminate buffer signal to the interrupt logic. This logic then generates the required interrupt and clears the channel 2 control logic.

OUTPUT BUFFER

The logic of the I/O Unit is a part of the transfer of data from a selected block of memory locations in a Memory Unit to an output equipment. Channel 2, to which the output device is attached, is selected by a channel select code from the Compute Unit. Prior to the initiation of the output buffer, the Compute Unit sets the LWA + 1 in the BXR, the FWA in the BER, and the bank designation in the BBC.

When the initiate buffer output signal occurs, it conditions the channel select and priority logic and the I/O control logic. The I/O control logic then gates

the contents of the BER and BBC onto the address selection lines to the Memory Unit and generates a read signal. The I/O control logic then sends a memory request signal to the Memory Unit. This signal initiates the memory cycle which reads the contents of the location as specified by the address selection. When this data is available, a resume I signal is sent to the I/O Unit.

The receipt of the resume I signal causes the I/O control logic to remove the address selection and memory request signals from the lines; to gate the output data word from the Memory Unit onto the data lines to the output equipment; to send an information ready signal to the output equipment.

After the output equipment has processed the data word, an output resume signal is sent to the I/O Unit. This signal causes the I/O control logic to remove the output data and the information ready signal from the lines and to enter a resume cycle which clears the BFR and increases the contents of the BER by one. The next address is then gated onto the address selection lines. The buffer cycle is then repeated for the next output word. This repetition continues until the contents of BER equals the contents of the BXR, at which time a terminate buffer signal is sent to the interrupt logic. The interrupt logic then generates the correct interrupt signal and clears the channel 2 logic.

MEMORY-TO-MEMORY TRANSFER

Both channels of an I/O Unit participate in the transfer of a block of data from one memory area to another. Basically, channel 2 performs an output buffer and channel 3 performs an input buffer. However, only the BFR for channel 3 is used for both operations, so data is stored in another memory area instead of being transmitted to external equipment.

The channel 2 select code is used to enable the channel 2 priority logic. Prior to the initiation of the memory-to-memory transfer, the Compute Unit sets in the BER, BXR, and BBC the FWA, LWA + 1, and bank designation, respectively, for the memory area from which data is to be transferred. Similar data is also set in channel 3 controls for the memory data area to which data is to be transferred.

The Compute Unit then issues a memory-to-memory signal which sets a control in the priority logic. This control conditions the I/O control logic of channels 2 and 3 to perform the required operations. The memory-to-memory transfer is initiated by an IBO2 or IBO3 instruction.

The I/O control logic gates the contents of the channel 2 BER and BBC onto the address selection lines and sends a read signal to the Memory Unit.

The I/O control logic then generates a memory request which initiates the reading of the first data word at the location specified by the address selection.

When the data is available, the Memory Unit returns a resume I signal to the I/O Unit to remove the read, memory request, and address selection signals and to gate the data into the channel 3 BFR. The channel 2 I/O control logic then performs a resume cycle which increases the contents of the channel 2 BER by one.

The channel 3 I/O control logic gates a write signal and the contents of the channel 3 BER, BBC, and BFR onto the signal lines to the selected memory module. A memory request signal is then sent to the Memory Unit to initiate the storage of the data word at the location specified by the channel 3 address selection. After the data has been stored, a resume I signal is returned. This signal causes the channel 3 I/O control logic to remove all channel 3 data and control signals and to perform a resume cycle which increases the contents of the channel 3 BER by one and clears channel 3 BFR.

At the completion of the channel 2 resume cycle, the channel 2 logic begins the repetition of the memory-to-memory transfer by selecting the address of the next word. This process is performed while the channel 3 operation is being completed. The operations involving channels 2 and 3 are repeated for each word to be transferred until the contents of the channel 2 BER equals the contents of the channel 2 BXR. When these quantities are equal, the memory-to-memory transfer is terminated.

DETAILED THEORY OF OPERATION

The following paragraphs describe the logic contained in each of the blocks shown in Figure 3-1. In most cases, only channel 2 logic is discussed. It is assumed that the operation of channel 3 logic is identical.

CHANNEL SELECT AND PRIORITY

The logic in this group includes most of the circuitry which establishes initial operating conditions and which provides the control signals that condition other logic circuits to perform the required operation.

Channel Select

The channel select logic translates a select code from the Compute Unit to determine if channel 2 or channel 3 is selected. This circuitry provides the required enable signals to other portions of the logic in the I/O Unit to provide operation on the selected channel, Figure 3-2.

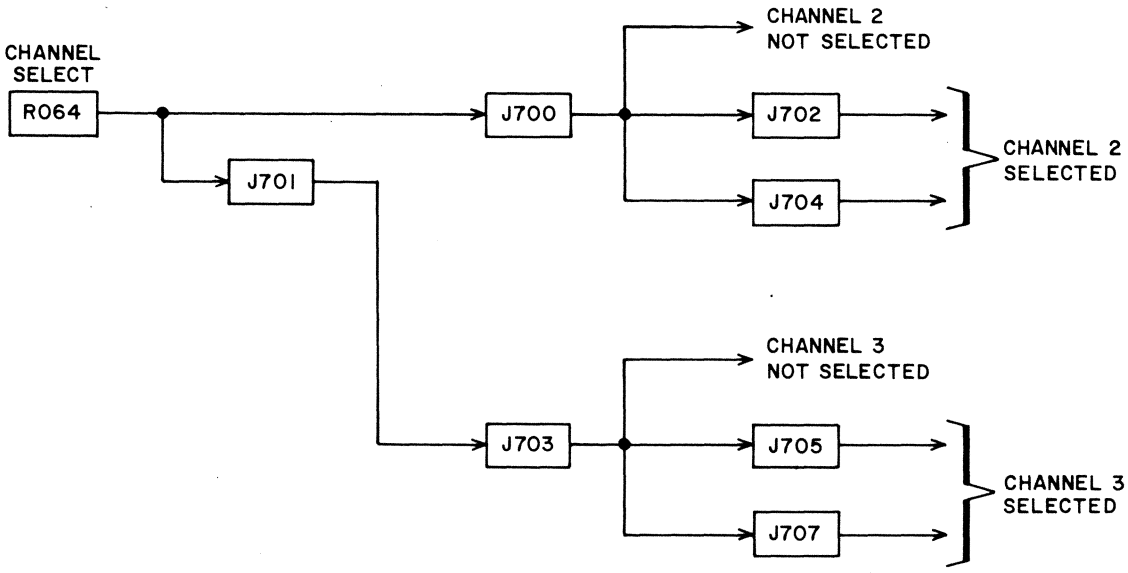


Figure 3-2. Channel Select Logic

Channel 2 Busy Logic

When channel 2 is selected, an initiate buffer input signal satisfies the AND input to the set side of K450/K451, Figure 3-3. Similarly, if channel 2 is selected, an initiate output buffer signal satisfies the AND input to the set side of K452/K453. The set outputs of these flip-flops enable the I/O control logic for their respective operations. However, these flip-flops are never set at the same time.

A reset output from each flip-flop forms an AND gate to J910. When either flip-flop is set, the AND is disabled and a 1 output occurs from J910. This 1 causes T279 to send a channel 2 busy signal to the Compute Unit. This signal prevents the Compute Unit from initiating any other operation involving channel 2 until the input or output buffer has been completed. A reset output from each flip-flop also feeds the function ready logic. One of these signals disables the function ready logic whenever channel 2 is performing as a buffer.

Clear Logic

The clear logic of channel 2 generates the signals necessary to clear the channel 2 control logic. These clear signals are necessary when a master clear or clear buffer control signal is generated by the Compute Unit or when an input disconnect or buffer termination interrupt occurs, Figure 3-4.

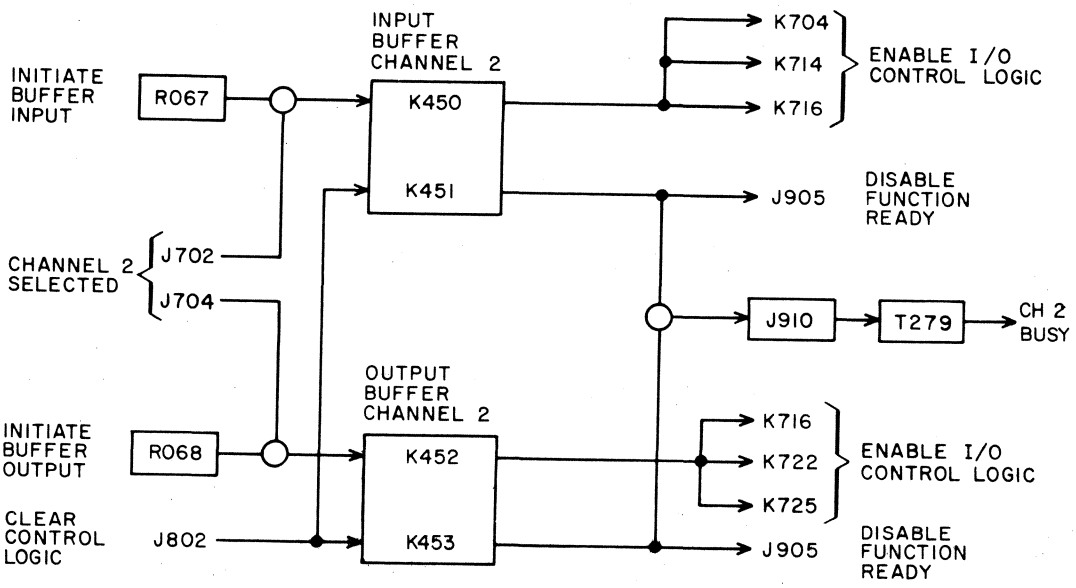


Figure 3-3. Channel 2 Busy Logic

Whenever there is a 1 input to J800, the resulting 1 outputs from J802 and J804 clear the channel 2 control logic. A master clear signal produces a 0 output from R075 and R077 which is applied to J504. This produces a 1 input to J800. J912 has a 1 output when a buffer termination interrupt occurs on channel 2. A clear buffer control signal produces a 1 from R074. If channel 2 is selected, the AND input to the set side of K472/K473 is satisfied. When resume II flip-flop resets and resume III flip-flop sets during the resume cycle, the set output of K472/K473 sets K474/K475. The set output of K474/K475 resets K472/K473 and is applied to J800. The clear signal from J802 resets K474/K475 after a 5 microsecond delay.

Priority

The priority logic enables one channel or the other to perform an input or output operation. Since both channels share the same memory lines, both cannot operate simultaneously. Figure 3-5 shows the channel 2 priority logic and a coincidence inverter. Channel 3 is identical to channel 2 except for the coincidence inverter.

When flip-flop K700/K701 is set, its reset output enables the transfer of the contents of BER and BBC to memory. The set output enables various parts of the I/O control logic for channel 2 operation.

When a channel 2 write request occurs and there is no channel 3 read or write request, a set output of K714/K715 and reset outputs of K772/K773

and K764/K765 satisfy one AND input to K700/K701. Similarly, when a channel 2 read request occurs and there is no channel 3 read or write request and data is not currently being gated from memory to BFR, a set output from K722/K723, a 1 from J946, and reset outputs from K772/K773 and K764/K765 satisfy the other AND input to K700/K701.

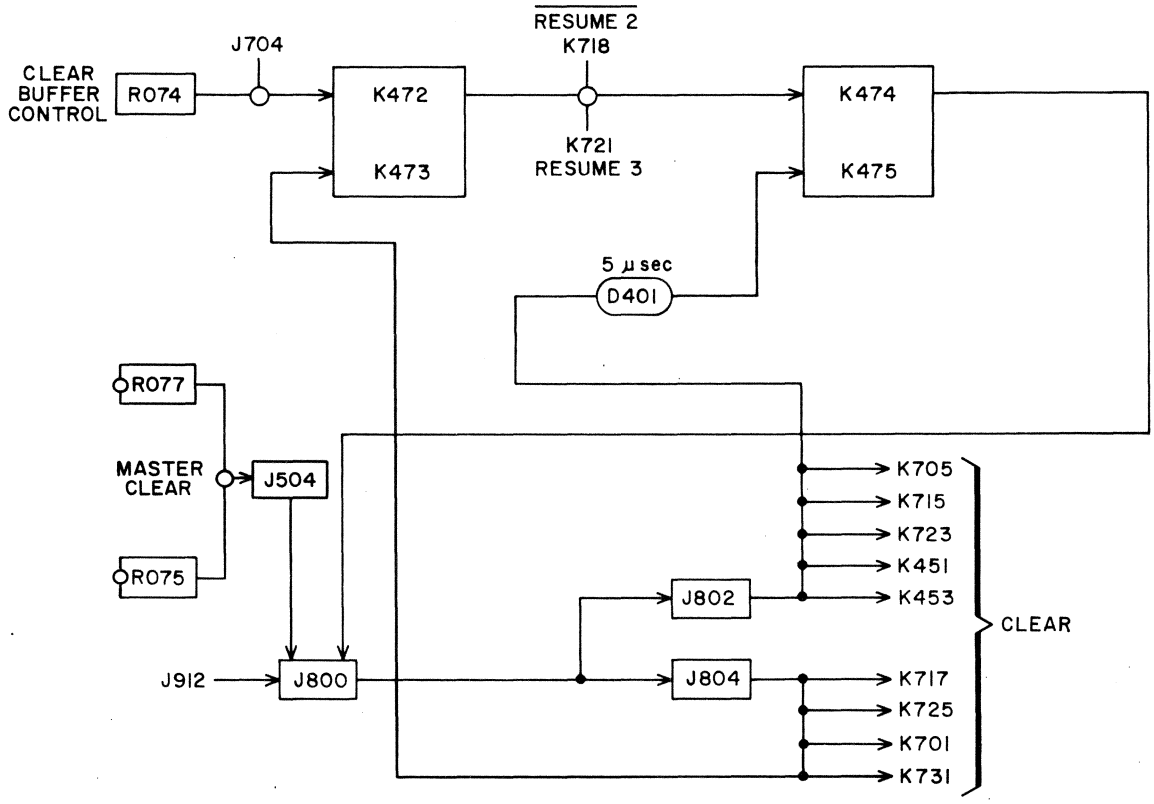


Figure 3-4. Channel 2 Clear Logic

Inverter J917 serves as a coincidence circuit if channel 2 and channel 3 priority conditions should occur simultaneously. This circuit ensures that channel 2 takes priority in such a situation. If there is a read or write request on channel 2 and a read or write request on channel 3, the two AND inputs to J917 are disabled. If neither channel 2 priority flip-flop nor channel 3 priority flip-flop is set, all inputs to J917 are 0. The resulting 1 output from J917 sets K700/K701. The channel 2 priority flip-flop is reset by any of the following conditions:

Inverter	Condition
J804	Clear channel 2 logic
J936	Channel 2 resume cycle
J947	Data from memory available for channel 2

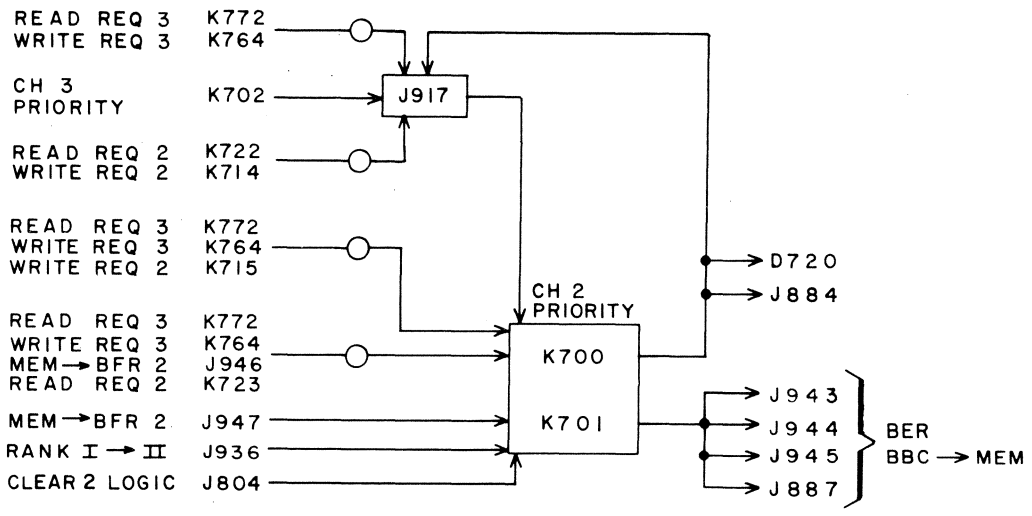


Figure 3-5. Channel 2 Priority Logic

COMPUTE INTERFACE LOGIC

Figure 3-6 shows the channel 2 compute interface logic except function ready which is described with external function logic.

Set BER, BXR, and BBC Logic

This control logic, under the direction of the Compute Unit, generates the commands necessary to enter the FWA in the BER, the LWA + 1 in the BXR, and the memory bank designation in the BBC.

When the set BBC command is generated by the Compute Unit, the output of R069 is 1. This 1 produces a 0 output from J954 and a 1 output from J966. If channel 2 is selected, the AND input to J951 is satisfied, and the set BBC channel 2 is generated. This command gates the memory bank designation from the data receivers into the BBC. The 0 output from J954 is inverted by J960. After 0.1 microsecond, a 1 output is applied to J966. As a result of this input, the output of J966 switches to a 0, which disables the AND input to J951 and removes the set BBC channel 2 command.

The operation of control logic for each of the other commands is the same. If channel 2 is selected when the command is given by the Compute Unit,

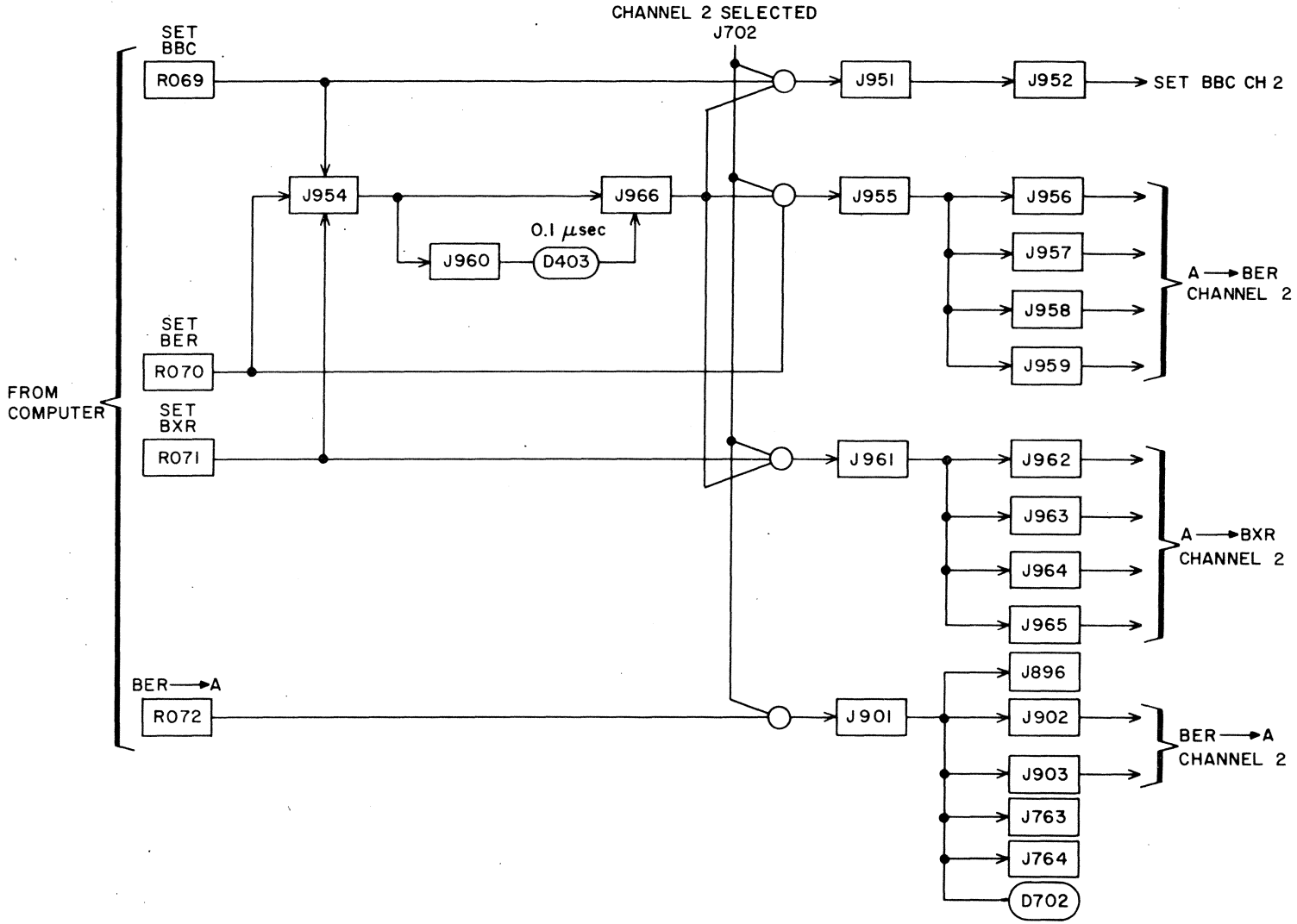


Figure 3-6. Compute Interface Logic

the appropriate command is given to perform the required gating. After 0.1 microsecond, the 1 output of D403 produces a 0 output at J966 to disable the gating command.

BER to A

When the BER to A command is generated by the Compute Unit and channel 2 is selected, the AND input to J901 is satisfied. The resultant 1 outputs from J902 and J903 gate the contents of the BER to the data transfer network. The 0 outputs from J901 gate this data onto the data lines to the Compute Unit.

BUFFER EXIT REGISTER

The BXR is a 13-stage register which holds the LWA + 1 for a buffering operation. Only one control affects the operation of the BXR. This control, A to BXR, gates the 13-bit LWA + 1 from the data receivers into the BXR. Figure 3-7 shows the lower order three stages of the BXR. The 1 outputs from J962 through J965 in the compute interface logic gate the 13-bit LWA + 1 from the data receivers into the BXR by a forced transfer. Inverters J720 through J732 invert the output of the corresponding receivers. Thus, when the output of R150 is 0, the 1 output from J720 resets K300/K301. When the output of R150 is a 1, K300/K301 is set. The only outputs from the BXR are to the logic which compares the contents of the BXR with the contents of the BER.

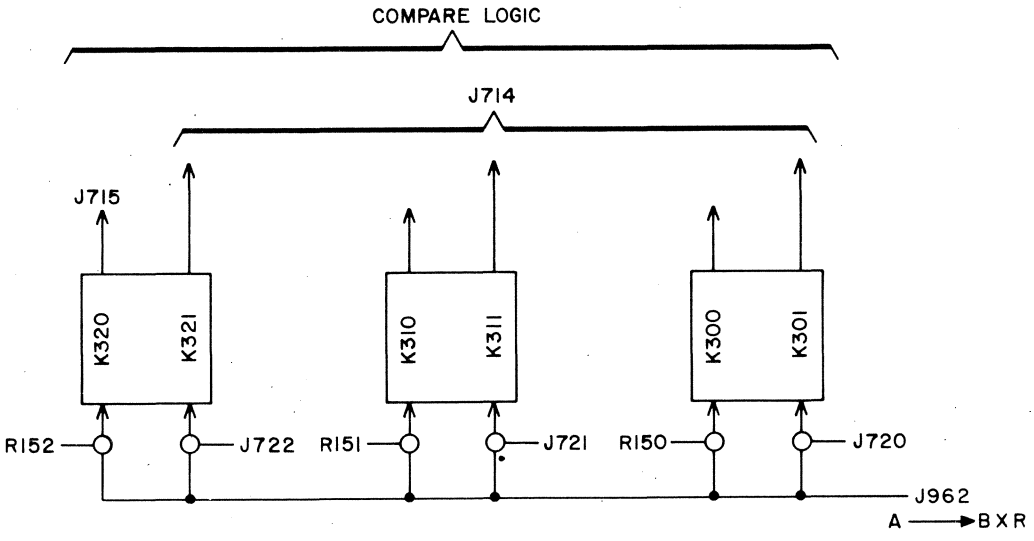


Figure 3-7. Typical Channel 2 BXR Stages

BUFFER ENTRANCE REGISTER

The BER is a 13-stage, double-ranked register which contains the current address (initially the FWA) for a buffer operation. The double-ranked feature of this register permits it to operate as an additive counter. At the completion of each buffer operation, the contents of rank I is transferred to rank II. An advance pulse complements the contents of rank II to rank I in such a manner that the current address is increased by one.

Figure 3-8 shows the lower order three stages of the BER. A 1 output from J934 enables the forced transfer of rank I to rank II. A 1 output from J938 advances the count. The lowest order stage is complemented by each advance pulse. The other stages are complemented only if all lower order stages of rank II are set. Thus, the count would advance in the following manner:

000
001
010
011
100
101
110
111

When the count reaches 111, an advance pulse is generated for the next group of three stages. The count in rank I represents the current address for a buffer operation. This address is sampled by the compare logic. The contents of the BER can be transferred through the data transfer network to the Compute Unit or to a selected Memory Unit.

BUFFER BANK CONTROL

The BBC consists of three flip-flops, Figure 3-9. The memory bank designation for a buffer is sent from the Compute Unit through the data receivers to the BBC. For each buffered word, the contents of the BBC and BER are placed on the lines to memory to select the correct address for each memory reference. The contents of the BBC remains unchanged during a buffer. It is only changed when a new bank designation is sent from the Compute Unit.

BUFFER DATA REGISTER

The BFR contains 13 stages. All buffer data which enters or leaves the I/O Unit is stored temporarily in the BFR. Figure 3-10 shows three typical stages of the BFR.

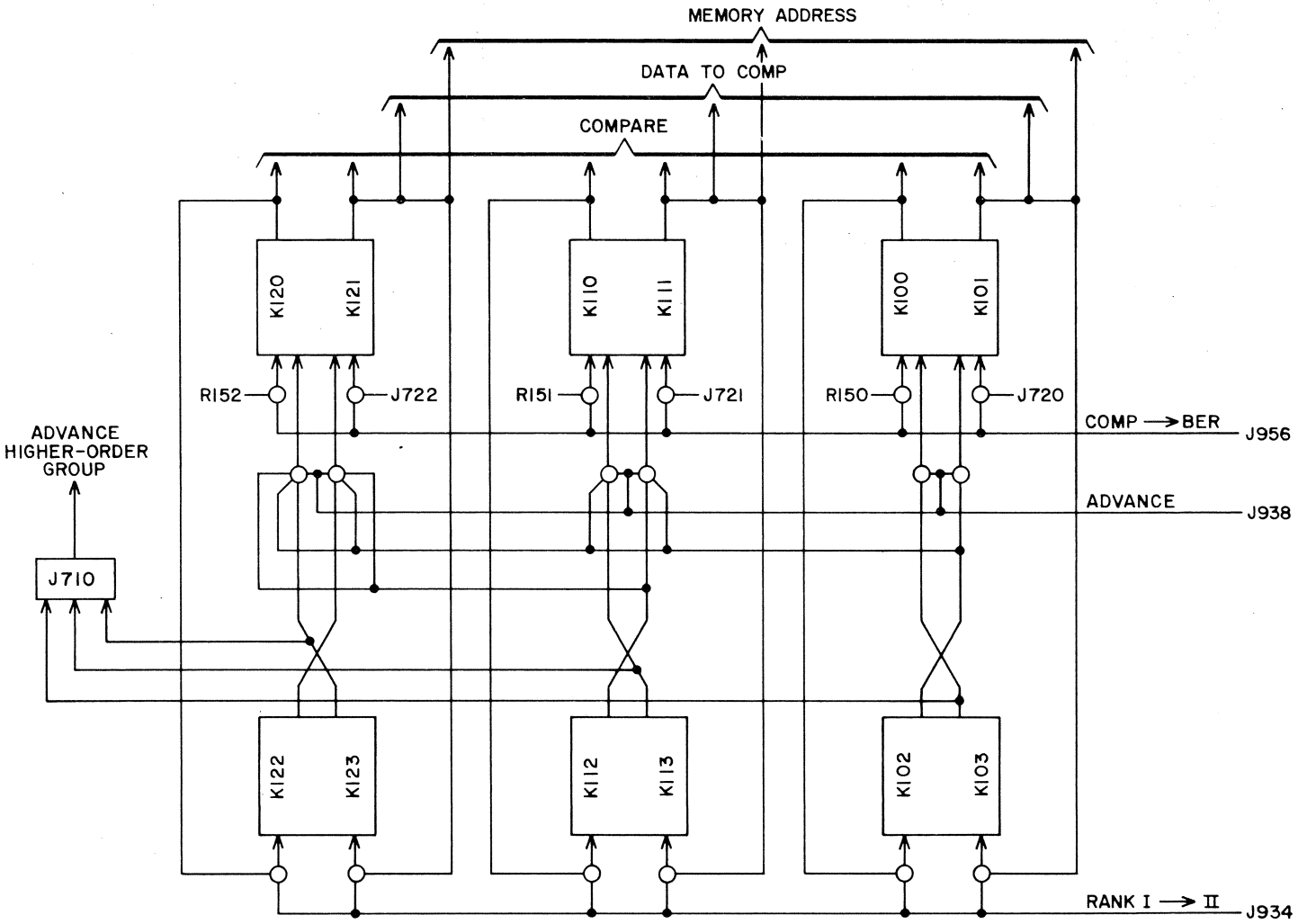


Figure 3-8. Typical Channel 2 BER Stages

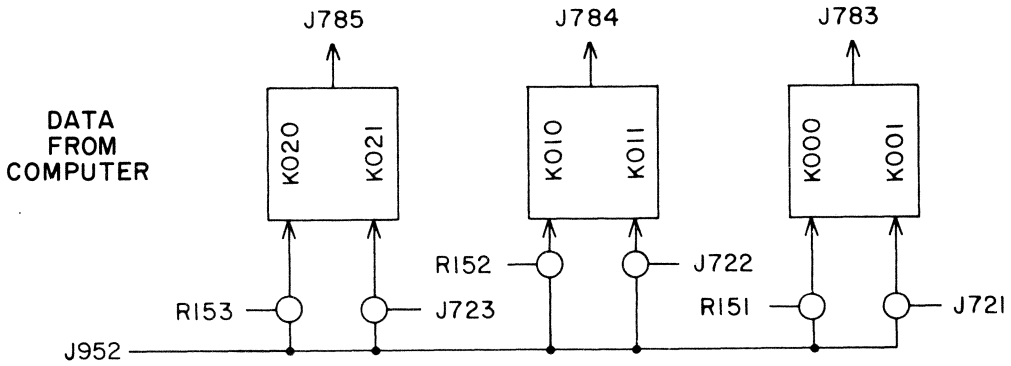


Figure 3-9. Channel 2 Buffer Bank Control

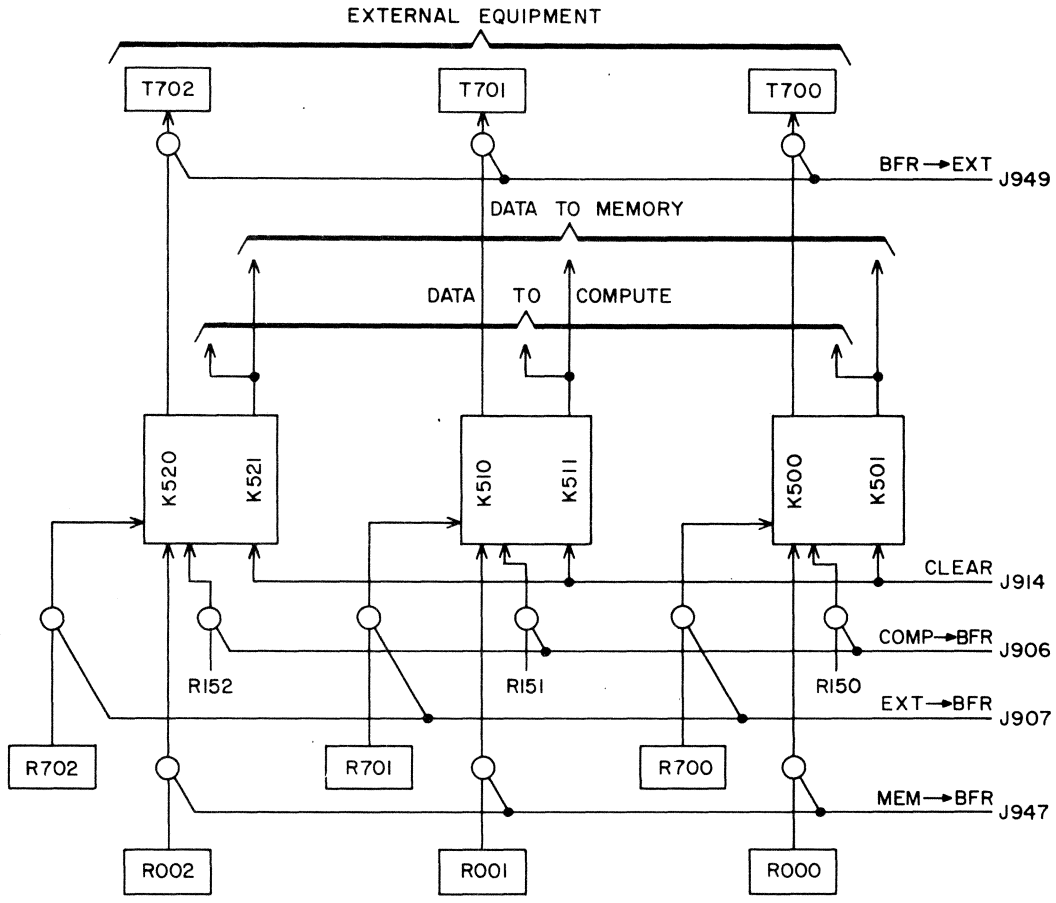


Figure 3-10. Typical Channel 2 BFR Stages

Data can enter the BFR from the Compute Unit, a Memory Unit, or an external equipment connected to channel 2, as determined by the gating signal. All data words are entered into BFR by a transfer of 1's. Similarly, with the correct gating, data can be transferred to the Compute Unit, a Memory Unit, or an external equipment. After the data word in the BFR has been transferred to the correct unit or equipment, a signal from the I/O control logic clears the BFR to receive the next data word.

DATA RECEIVERS

Thirteen receivers terminate the data lines from the Compute Unit, Figure 3-11. When a 1 is applied to a transmitter at the other end of the line, the output of the associated receivers becomes a 1. A group of 13 inverters, 1 per receiver, provides reset inputs for forced transfers. When the output of a

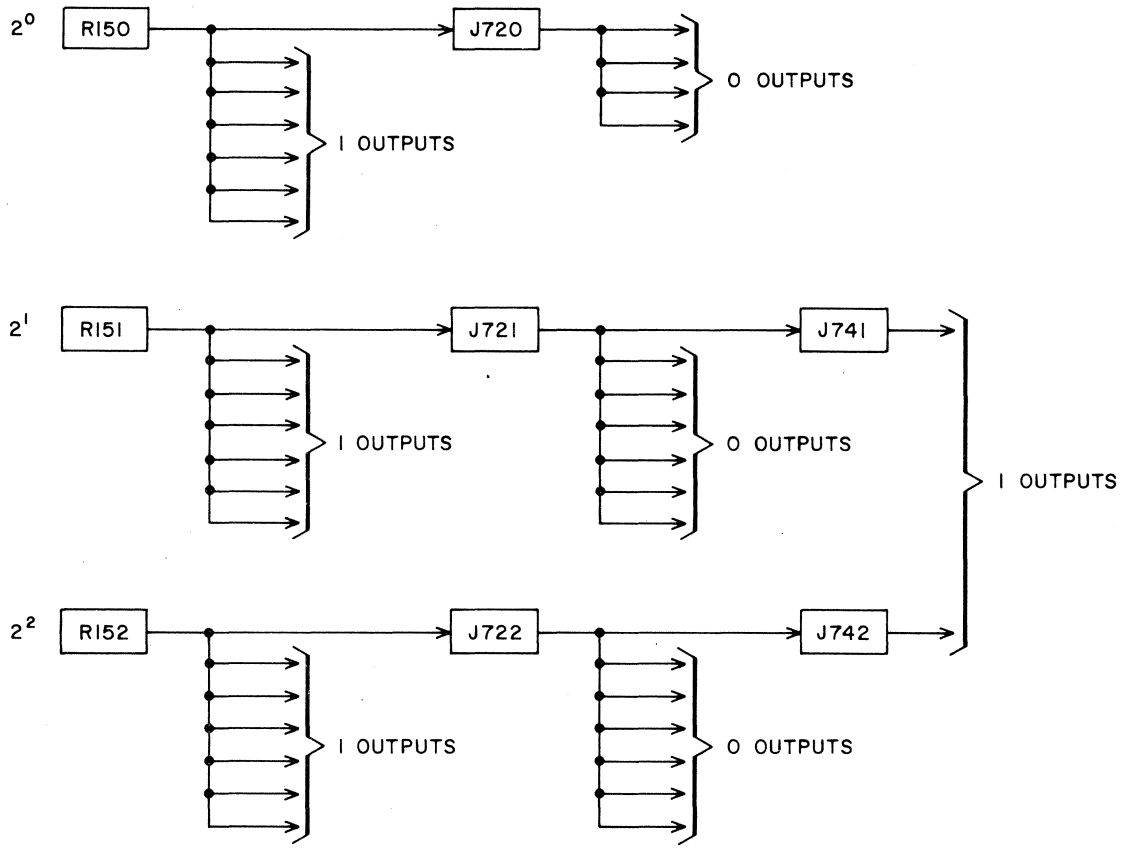


Figure 3-11. Typical Data Receivers

receiver is 0, the associated inverter has a 1 output. The data receivers and inverters are used to transfer the FWA to the BER, the LWA + 1 to the BXR, and data from the Compute Unit to the BFR. Bits 1 through 4 also transfer the bank designation to the BBC. Four inverters provide additional 1 outputs for bits 1, 2, 3, and 4. The data receivers are common to both channels 2 and 3.

DATA TRANSFER NETWORK

The data transfer network consists of the transmitters and associated inverters necessary to transfer data to the Compute and Memory Units and address selection to the Memory Unit. The data transfer network is shared by channels 2 and 3.

Data to Memory Unit

Both the channel 2 BFR and channel 3 BFR provide inputs to inverters J850 through J862, Figure 3-12. For example, J850 receives an input from the reset side of stage 00 of both BFR's. Each signal is gated by the output of an inverter in the I/O control logic for the respective channels. Thus, if the

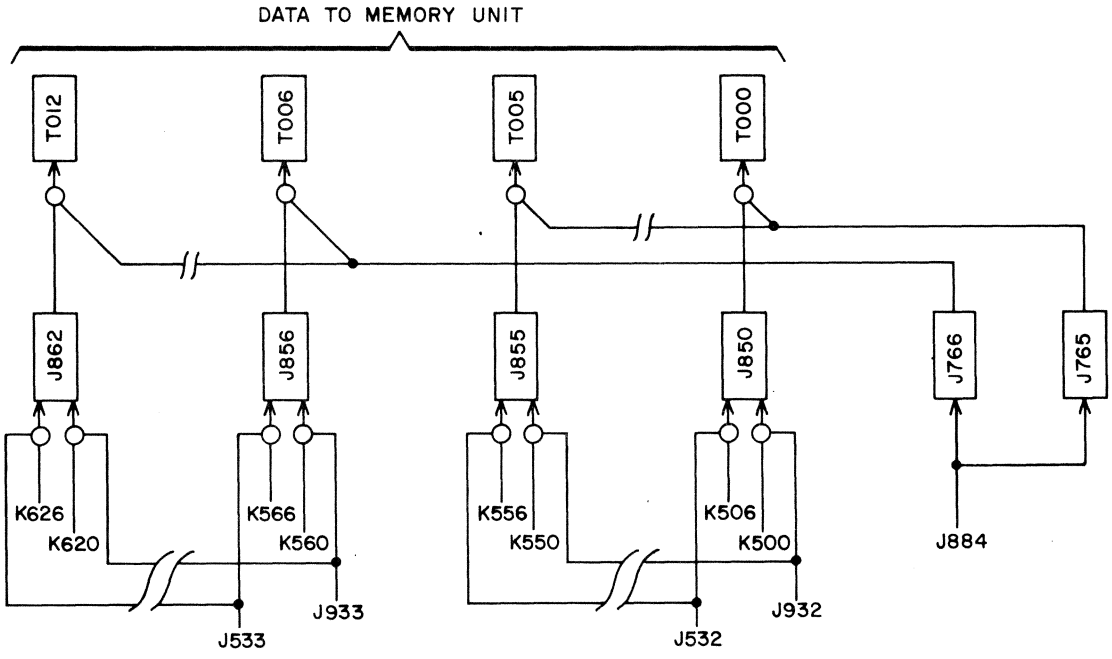


Figure 3-12. Data-to-Memory Logic

channel 2 I/O control logic generates the command BFR to memory, the 1 outputs from J932 and J933 gate the contents of channel 2 BFR into the inverters. The 1 outputs of J932 and J933 enable one AND input to each inverter and the output of a given inverter is dependent on the input from an associated stage of the BFR. Thus, if stage 00 is set, the input to J850 is a 0 and the output of J850 is a 1. If stage 00 is reset, the input to J850 is a 1 and the output of J850 is a 0. Therefore, the output of inverters J850 through J862 effectively duplicates the set output of every stage of channel 2 BFR.

When channel 2 is active, the 0 outputs from J532 and J533 disable the other AND gate to each inverter to prevent channel 3 information from entering these inverters.

When the BFR to memory command occurs for either channel, a 0 is applied at the inputs to J766 and J765. The resulting 1 outputs from these inverters gate the outputs of J850 through J862 into T000 through T012. These transmitters place the data on the data lines to the memory stack.

Bank and Address Selection

Inverters J770 through J785 and transmitters T020 through T035 transfer the bank and address selection to memory, Figure 3-13. This network is shared by channels 2 and 3. The operations of the channels are identical. When the channel 2 I/O control logic generates a BER/BBC to memory, signal 1 outputs result from J943, J944, and J945. These 1's enable the transfer of the contents of the BER and BBC to the transfer network.

For example, the 1 output of J943 enables J770 to follow the contents of stage 00 of channel 2 BFR. When stage 00 is set, the reset output provides a 0 to J770, and the output of J770 is 1. When stage 00 is reset, the reset output is 1, and the output of J770 is 0. Thus, the output of J770 duplicates the set output of stage 00. The contents of every stage of channel 2 BER and BBC is transferred to the network in this manner. The outputs from J770 through J785 are applied to T020 through T035, respectively. The transmitters then place the bank and address selection on the lines to memory. The signals on these lines select a bank in a Memory Unit and an address in that bank for the memory reference required by channel 2.

BER, BFR to Compute Unit

Inverters J750 through J762 and transmitters T150 through T162 permit the transfer to the Compute Unit of the contents of the BER or BFR in either channel, Figure 3-14. The operation is identical for both registers in both channels, except that only 12 bits are transferred from the BFR's. When the compute interface logic generates the command BER to A, J902 and J903 have 1 outputs. These 1 outputs gate the contents of the BER into the inverters. For example, when stage 00 is set, a 0 from the reset output of

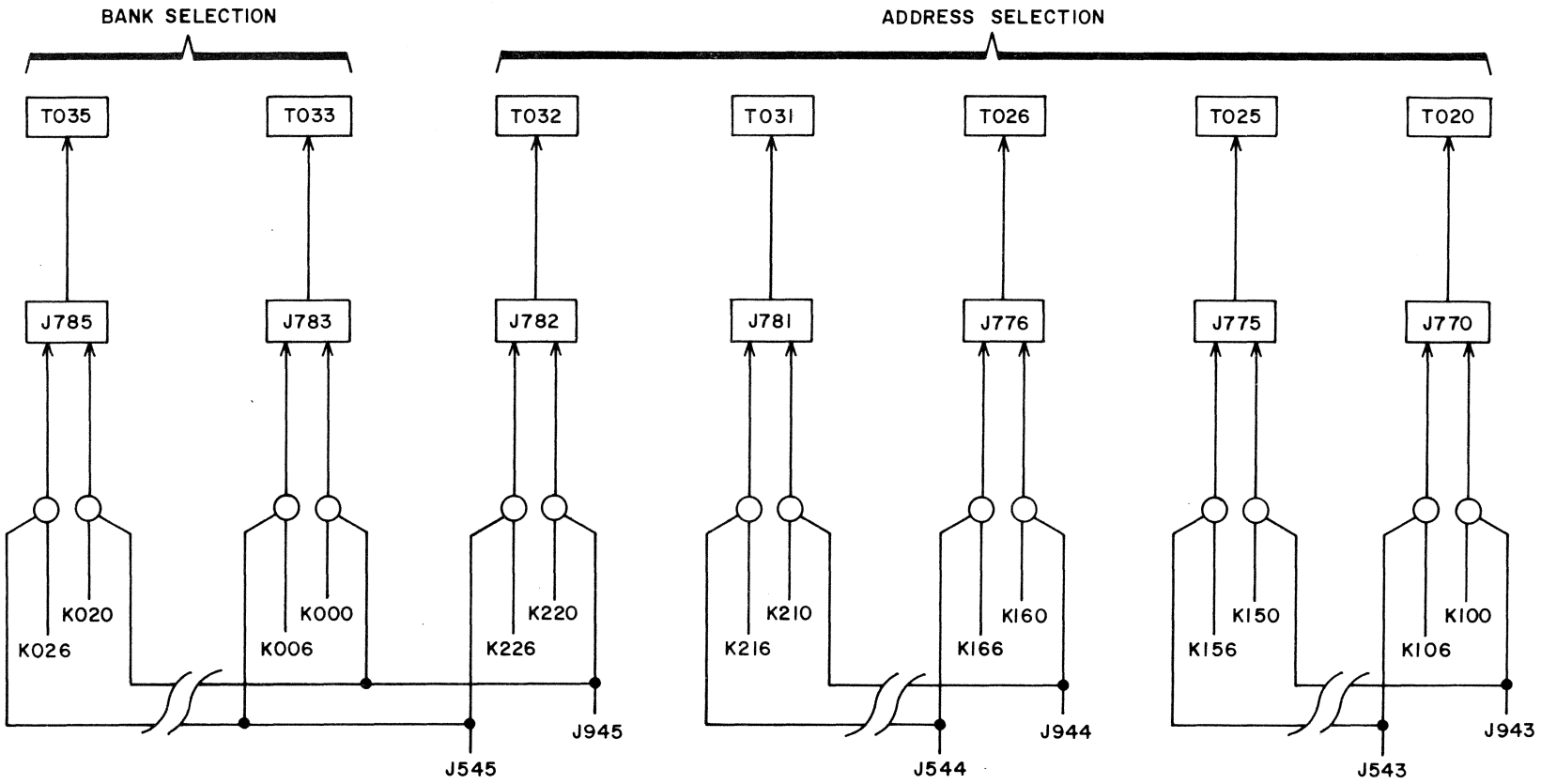


Figure 3-13. Bank and Address Selection

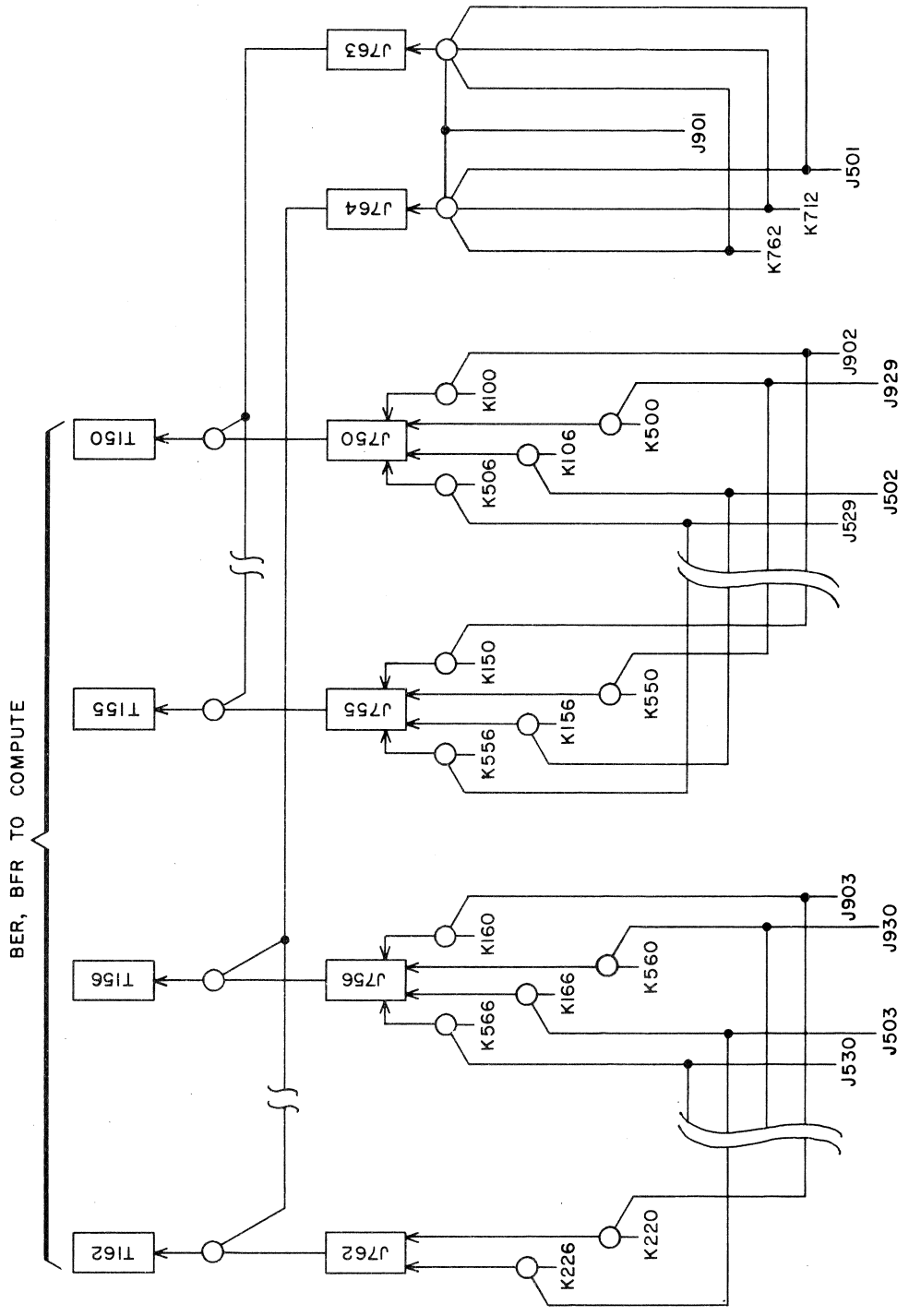


Figure 3-14. BER, BFR-to-Compute Logic

this stage disables the AND input to J750 and the output of J750 goes to 1. If stage 00 is reset, the 1 from the reset output of this stage satisfies the AND input to J750 and the output of J750 is a 0. The outputs of J750 through J762, therefore, duplicate the set outputs of the BER. When any of the conditions are present which require data to be transmitted to the Compute Unit, a 0 is applied to the AND inputs to J763 and J764. The resultant 1 outputs gate the outputs of J750 through J762 into the transmitters, which place the data on the lines to the Compute Unit.

INTERRUPT LOGIC

Basically, the interrupt logic in the I/O Unit functions as a repeater network. When an interrupt signal is generated by an external equipment on the compare logic, the interrupt logic receives this signal and transmits it to the Compute Unit, Figure 3-15.

Buffer Termination

A buffer termination interrupt occurs in two ways. An input disconnect from the equipment currently involved in a buffer operation on channel 2 produces a 1 output from R714. Because D714 delays the application of the 1 to J909, the output of J909 is still 1. Therefore, the AND input to J911 is satisfied. The 0 output from J911 is inverted to a 1 by J912 and applied to T283. A buffer termination interrupt is then sent to the Compute Unit. After 0.2 microsecond, the 1 output of J909 switches to a 0 which disables the AND input to J911 and removes the buffer termination interrupt. A buffer termination interrupt is also generated during the resume cycle for the last buffer operation. At this time, the contents of BER equals BXR and the output of J735 is 1. This 1 and the 1 from the set side of the resume III flip-flop (K721) satisfy the other AND input to J911, which results in the buffer termination interrupt. Regardless of how the interrupt is generated, a 1 output from J912 causes the clear logic to clear the buffer control logic.

Interrupts 1 and 2

The operation of interrupt 1 is identical to the operation of interrupt 2. When a given interrupt is activated by an equipment on channel 2, a 1 results from the associated receiver. This 1 is applied directly to the transmitter which sends the correct interrupt to the Compute Unit.

Parity Error

A resume signal from memory to channel 2 results in a 1 output from D722. This signal sets K730/K731. This flip-flop remains set until a similar resume signal occurs for channel 3 or the channel 2 clear logic is activated.

If a parity error occurs during a read operation on channel 2, the AND input to the set side of K726/K727 is satisfied. The set output of the flip-flop is

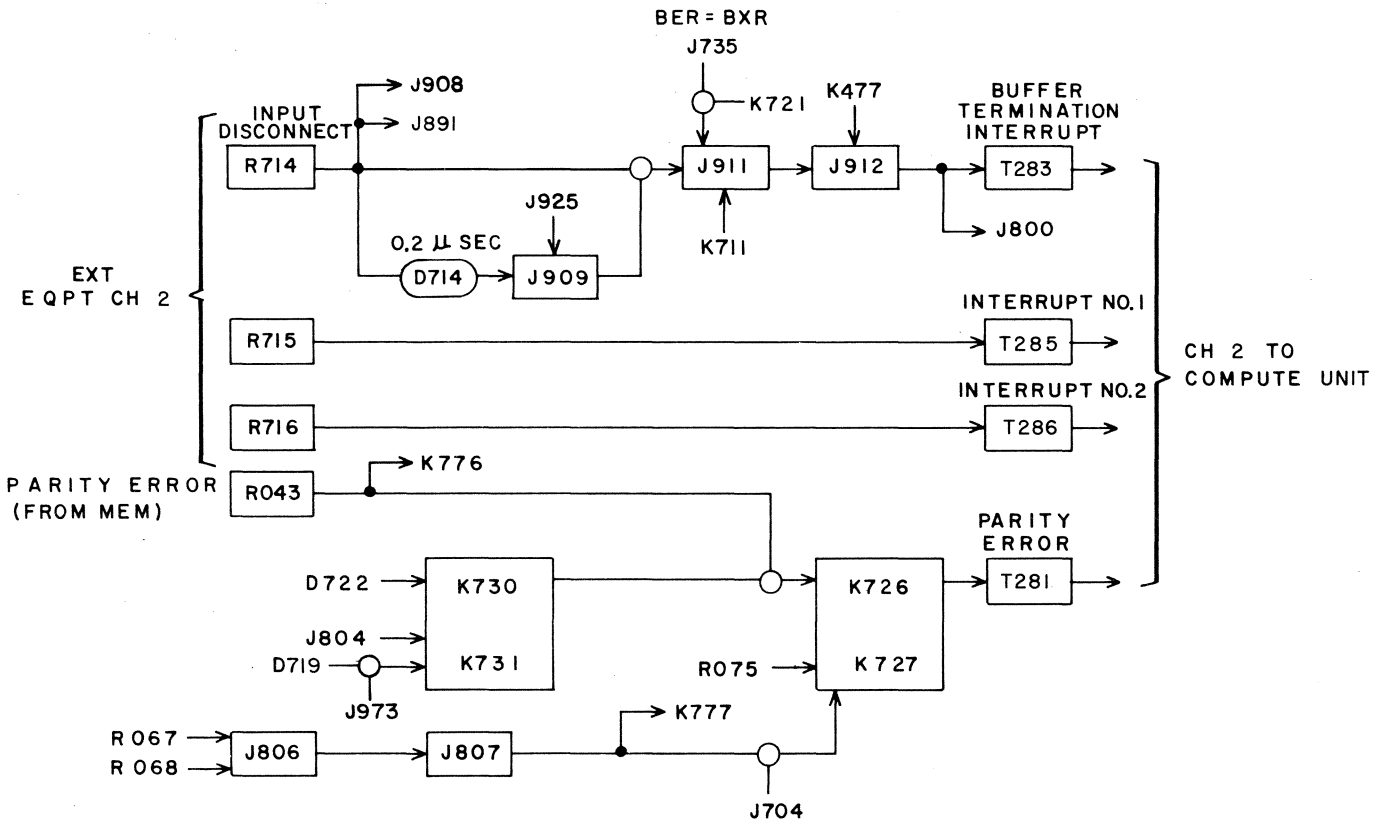


Figure 3-15. Channel 2 Interrupt Logic

applied to T281, which results in a parity error signal. This signal is removed by any of the following conditions:

1. Channel 2 is selected and a new input or output buffer is initiated.

2. A master clear occurs.

3. A channel 2 clear buffer control signal occurs.

> NOTE: The remainder of the I/O logic is discussed as it applies to a particular type of I/O operation.

EXTERNAL FUNCTION LOGIC

When the channel clear logic is activated, the 1 outputs from J802 and J804 place flip-flops K450/K451, K452/K453, and K724/K725 in the reset condition, Figure 3-16. If the external function code is to be transferred to an equipment on channel 2, the Compute Unit generates the select code for channel 2, places the EF code on the data lines, and sends a function ready signal. The resultant 1 outputs from R063 and J702 and the reset outputs from K450/K451 and K452/K453 satisfy the AND input to J905; the resultant 1 outputs from J906 and J907 gate the EF code from the data receivers into the channel 2 BFR. The 0 output from J905 also disables the AND inputs to J949 and J950. The 1 outputs from these inverters gate the EF code out of the BFR to T700 through T712, which places this code on the channel 2 external data lines.

The 1 output from J906 to T714 is delayed 0.5 microsecond. When this output switches to a 1, a function ready signal is sent to the external equipment. The function ready signal gates the EF code into an external equipment. After the code has been sensed, the external equipment sends an output resume to the channel 2 logic. Receipt of this signal causes the channel 2 logic to clear the channel 2 BFR and to transmit a resume to the Compute Unit from T077. This signal causes the Compute Unit to remove the function ready and data from the signal lines.

INPUT-TO-A LOGIC

For an input-to-A operation on channel 2, the Compute Unit generates the correct select code for channel 2 and an input-to-A signal. This signal initiates the reading of a status word from an external equipment on channel 2 and the transmission of this word through the I/O Unit to the A register in the Compute Unit. Figure 3-17 shows the channel 2 logic involved in an input-to-A operation. Normally, flip-flop K704/K705 is reset by the clear logic at the end of any operation involving channel 2. When channel 2 is

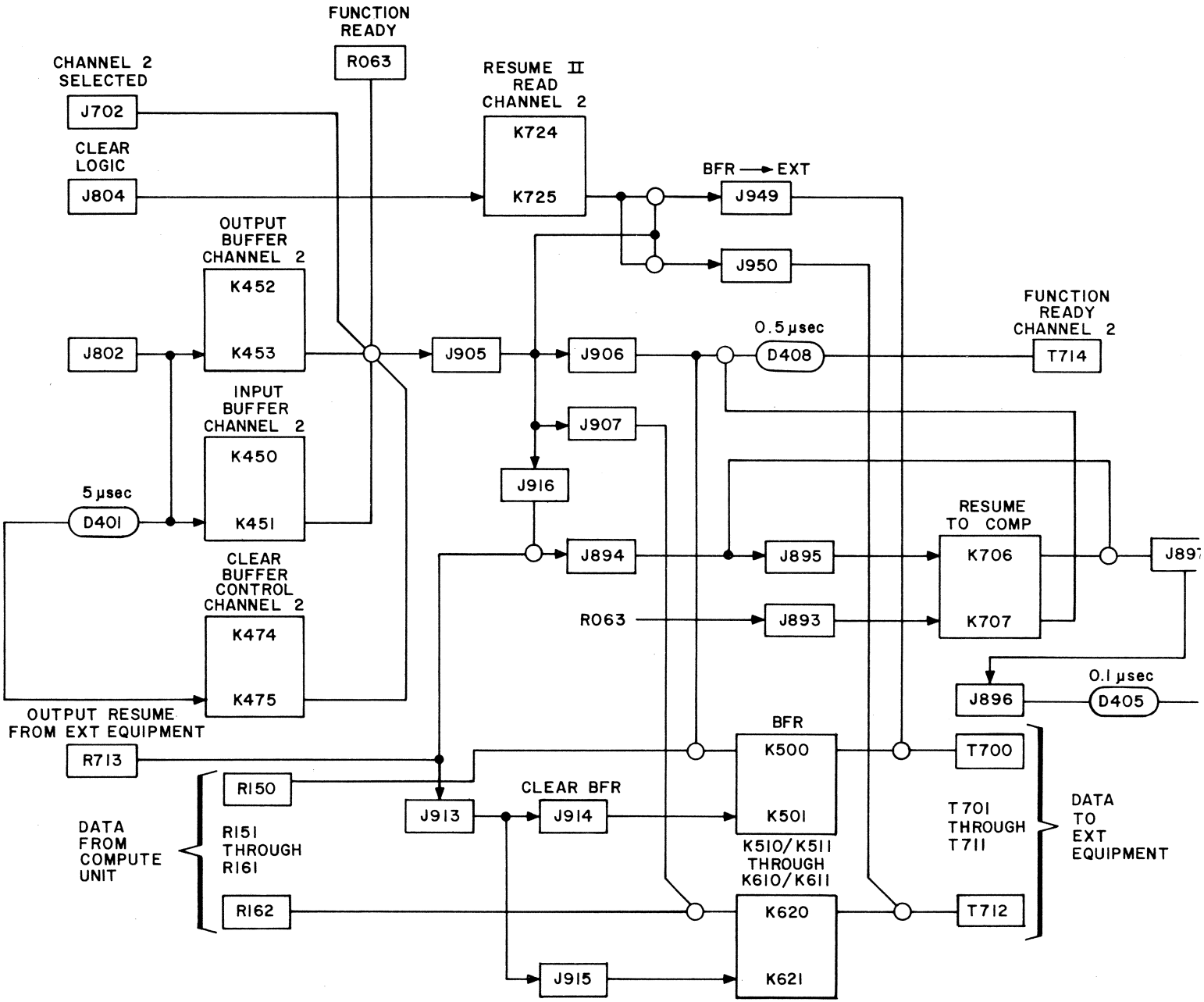


Figure 3-16. Channel 2 External Function Logic

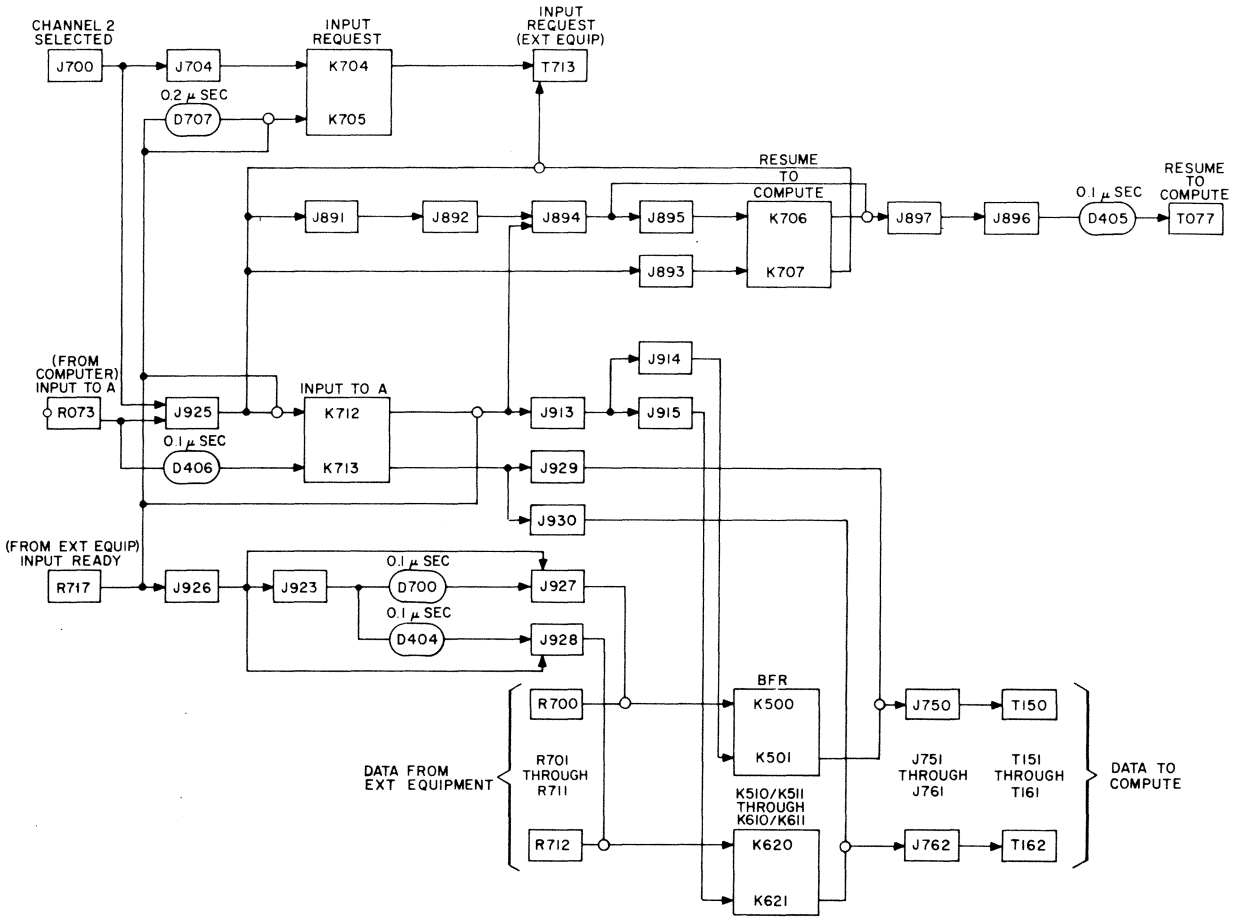


Figure 3-17. Channel 2 Input-to-A Logic

selected, a 0 output results from J700 and a 1 output results from J704. When the input-to-A signal is generated by the Compute Unit, the output of R073 is 0. The 0 outputs from J700 and R073 disable the AND inputs to J925. The output of J925 switches to 1, which causes an input request to be sent to the external equipment through T713.

When the input word is available on the data lines, the external equipment sends an input ready to the I/O Unit. The resulting 1 output from R717 combines with the 1 output from J925 to set K712/K713. Inverter J926 inverts the 1 output from R717 to a 0, which is applied to J927 and J928. The other input to these inverters is held at 0 by D700 and D404 for 0.1 microsecond. The 1 outputs from J927 and J928 gate the input word from R700 through R712 into the BFR. A reset output from K712/K713 is inverted by J929 and J930. The 1 outputs from these inverters gate the complement of the data from the BFR into inverters J750 through J762. These inverters apply the actual data word to T150 through T162 for transmission to the Compute Unit. After 0.1 microsecond, the outputs of D700 and D404 switch to a 1 and the data gate into the BFR is disabled.

When flip-flop K712/K713 was set, a set output from this flip-flop disabled the input to J894. The other input was previously disabled by the 0 output from J925 through the chain J891, J892. The resultant 1 output is ANDed with the set output of K706/K707 to produce a 1 out of J896 which is delayed 0.1 microsecond by D405 and then applied to T077. This sends a resume to the Compute Unit.

The resume signal, which occurs after the data transfer is complete, causes the Compute Unit to remove the channel selection and input-to-A signals.

When these signals are removed, the outputs of J700 and J925 go to 1. The set output of K712/K713 and the 1 output of R717 satisfy the AND input to J913. The resultant 1 outputs from J914 and J915 clear the BFR. The output of J925 goes to 0, which removes the input request. The removal of this signal, in turn, causes the external equipment to remove the input ready signal. When this signal ceases, the output of R073 goes to 1. This 1 resets K712/K713. The channel 2 input-to-A logic has now been returned to its cleared condition.

INPUT BUFFER LOGIC

Prior to the initiation of a channel 2 input buffer, the FWA is placed in the BER, the LWA + 1 in the BXR, and the memory bank designation in the BBC. When channel 2 is selected, 1 outputs result from J702 and J704, Figure 3-18. An initiate input buffer command from the Compute Unit produces a 1 output from R067. The 1 outputs from R067 and J702 satisfy the AND input to the set side of input buffer flip-flop K450/K451. Similarly, the 1 outputs from R067 and J704 combine to set input request flip-flop K704/K705.

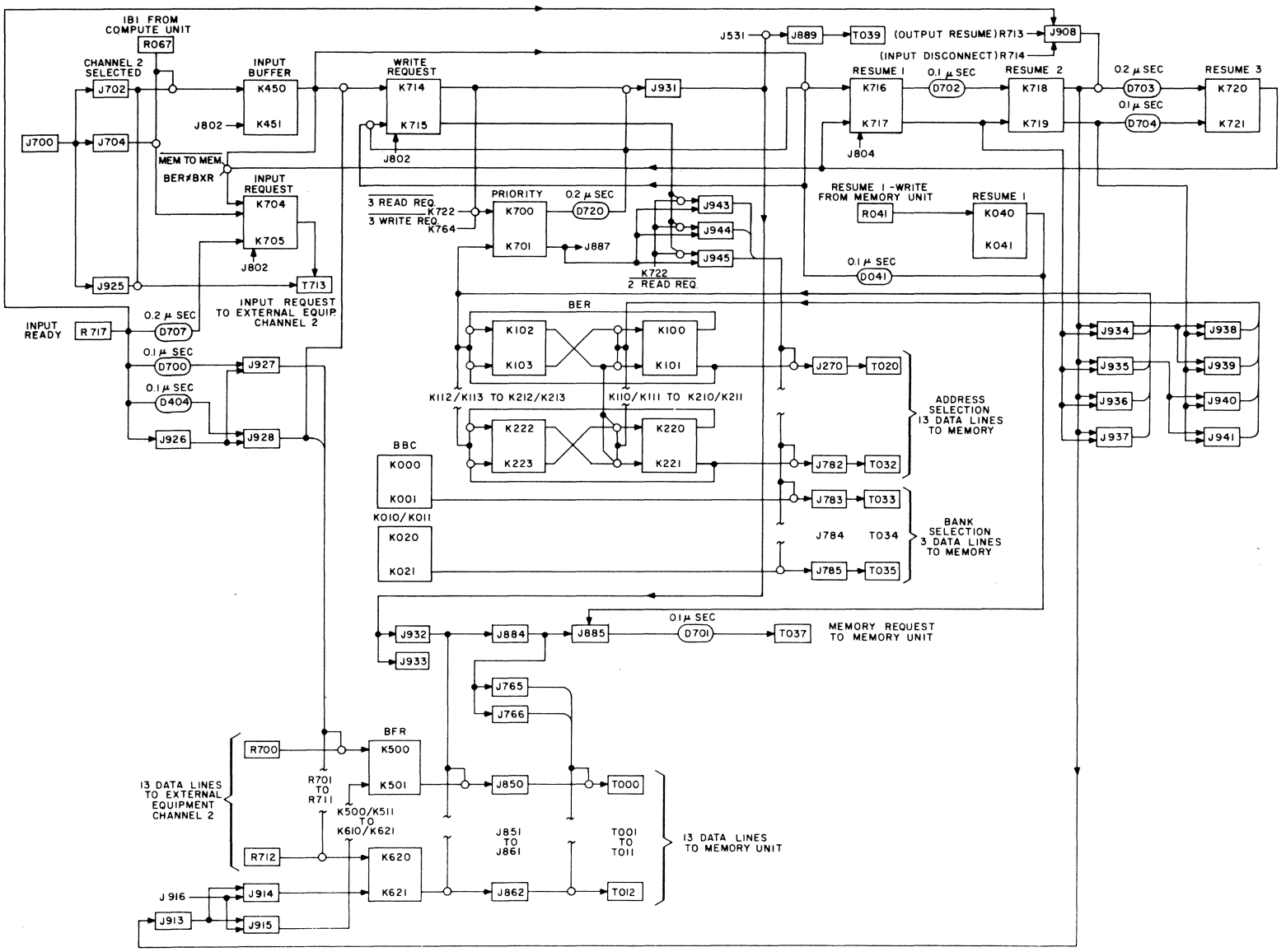


Figure 3-18. Channel 2 Input Buffer Logic

When the input request flip-flop sets, a 0 from J700 is applied to the input of J925. The resultant 1 output causes T713 to send an input request signal to the external equipment. When the input word has been placed on the data lines to channel 2, the external equipment generates an input ready. This signal produces a 1 output from R717.

A 1 output from R717 resets K704/K705, which removes the input request signal, which in turn causes the external equipment to remove the input ready signal. The 1 output from R717 produces a 0 output from J926 and 1 outputs from J927 and J928. These 1 outputs gate the input word from R700 through R712 into the lower order 12 stages of the BFR. A 1 output from J928 also combines with the set output of K450/K451 to set write request flip-flop K714/K715. After 0.1 microsecond, D700 and D404 apply the 1 output of R717 to J927 and J928, which disables the gating of data into the BFR.

If channel 3 is not involved in a read or write operation, the set output from K714/K715 is gated into the set side of priority flip-flop K700/K701. The set output of this flip-flop indicates that channel 2 has priority to use the I/O Unit memory lines.

Reset outputs from K714/K715 and K700/K701 provide 0 inputs to J943, J944, and J945. The resultant 1 outputs gate the address selection from channel 2 BER and BBC into the control lines to memory.

The set outputs from K700/K701 and K714/K715 satisfy the AND input to J931. A 0 output from J931 is inverted to a 1 by J889. This 1 causes T039 to send a write request to memory. The 0 output from J931 produces 1 outputs from J932 and J933. These 1 outputs gate the complement of the data word from the BFR into J850 through J862. The 0 output of J884 produces 1 outputs from J765 and J766. These 1 outputs gate the actual data word into T000 through T012 for transmission to memory.

A 0 output from J884 also produces a 1 output from J885. This 1 is delayed 0.1 microsecond by D701 and then applied to T037, which sends a memory request. This signal enables the selected memory bank to store the data word at the specified address.

After the Memory Unit has stored the data, a resume I signal is returned to the I/O Unit. The resultant 1 output of R041 sets the resume I flip-flop K040/K041. After 0.1 microsecond, the set output from K040/K041 combines with the set output from K700/K701 and the set output from K450/K451 to set resume I flip-flop K716/K717. Setting this flip-flop initiates the resume cycle. The set output from K040/K041 also combines with the set output from K700/K701 to reset write request flip-flop K714/K715. Resetting this flip-flop removes the address and bank selection, write request, and memory request signals from the lines to memory.

A reset output of K716/K717 produces 1 outputs from J934 through J937. These signals transfer rank I of the channel 2 BER to rank II. After a 0.1-microsecond delay, the set output of resume I flip-flop sets resume II flip-flop. A reset output from this flip-flop produces 1 outputs from J938 through J941. These 1 outputs advance the count in the BER by one. A set output from K718/K719 produces a 0 output from J913 and 1 outputs from J914 and J915. These 1 outputs clear the BFR.

If none of the signals represented by the inputs to J908 are present, the set output of K718/K719 sets resume III flip-flop after 0.2 microsecond. If the buffer is not complete, the set output of K720/K721 sets the input request flip-flop to initiate the buffering of the next input word. After the last word has been buffered, the preceding step does not occur, and the buffer is terminated. A set output of K720/K721 also resets K716/K717, which causes each of the other resume flip-flops to reset.

OUTPUT BUFFER LOGIC

Prior to an output buffer on channel 2, the Compute Unit enters the FWA, LWA + 1, and memory bank designation in the channel 2 BER, BXR, and BBC, respecitvely. The Compute Unit then selects channel 2 and generates an initiate buffer output command.

The resultant 1 outputs from J704 and R068 set channel 2 output buffer flip-flop K452/K453 and read flip-flop K722/K723, Figure 3-19. If channel 2 is not currently gating data from memory into the BFR and channel 3 is not performing a memory reference, a set output from K722/K723 sets priority flip-flop K700/K701.

Reset outputs from K722/K723 and K700/K701 produce a 1 output from J943 through J945. These 1 outputs gate the address selection and memory bank designation onto the control lines to memory. Reset outputs from the channel 2 priority and read flip-flop disable both AND inputs to J887. The resultant 1 output of J887 causes T038 to send a read signal to memory.

The set output from K700/K701 and a set output of K722/K723 satisfy the AND input to J884. The resultant 1 output of D701 is delayed 0.1 microsecond before it causes T037 to send a memory request to memory.

This signal causes the selected memory to read the contents of the specified address. In the memory cycle, a resume I signal is returned to the I/O Unit. The resultant 1 output from R041 is gated into the set side of K728/K729. After a 0.3-microsecond delay, D721 applies a 1 to J946. The resultant 1 outputs of J947 and J948 gate the data word into the BFR and reset the channel 2 read and priority flip-flops. Resetting these flip-flops causes the removal of the address and bank selection, read, and memory request signals from the lines to memory.

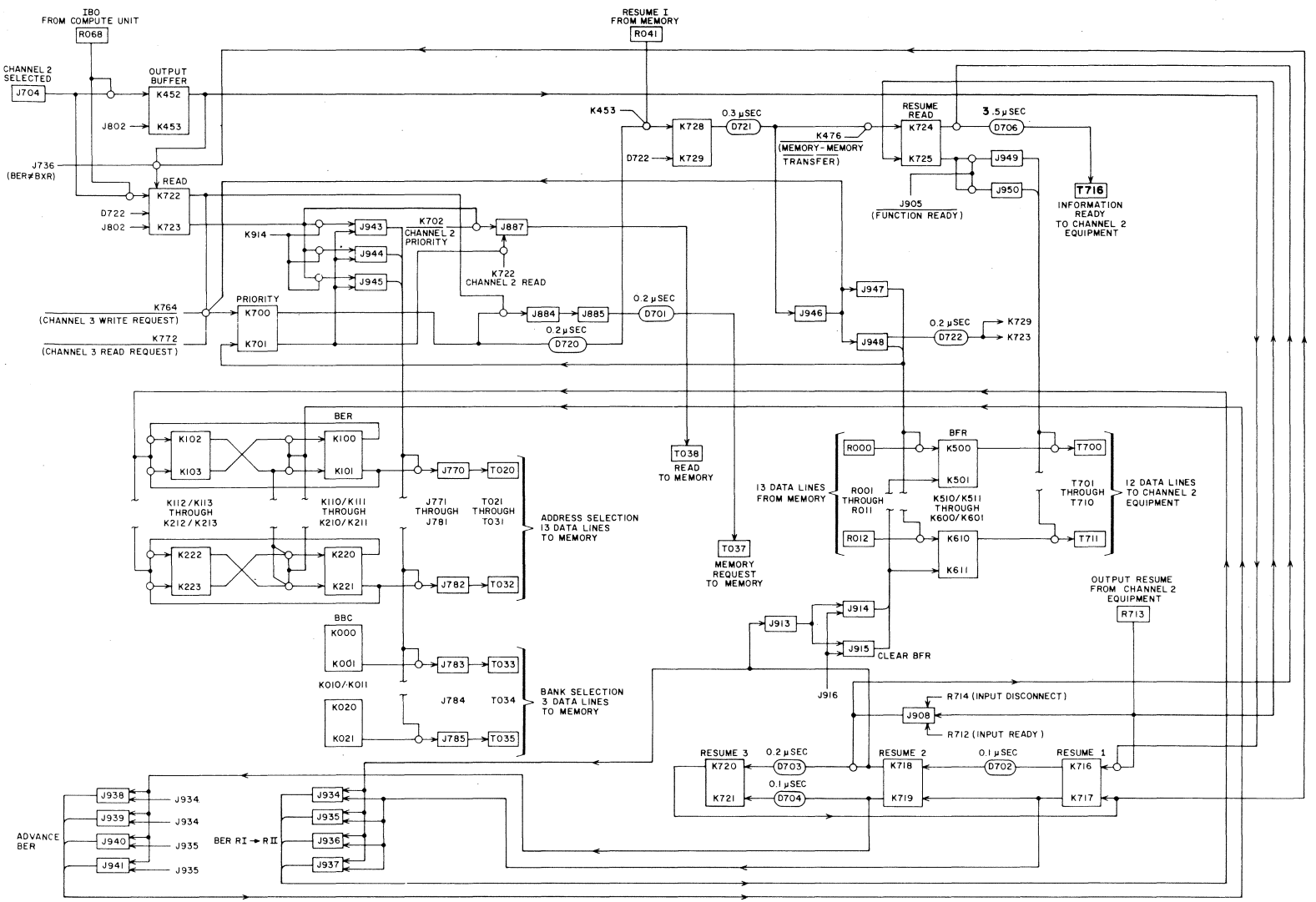


Figure 3-19. Channel 2 Output Buffer Logic

However, before the priority flip-flop resets, the 1 output from D721 sets K724/K725. A reset output of this flip-flop produces 1 outputs from J949 and J950 which gate the output word out of the BFR onto the data lines.

If there is no output resume, input ready, or input disconnect signal present, the 1 output of J908 gates the set output of K724/K725 into D706. After 3.5 microseconds, the 1 output of D706 causes T716 to send an information ready signal to the output equipment.

The information ready signal causes the output equipment to process the data word. When this operation is complete, the output equipment returns an output resume.

A 1 output of R713 and a set output from the output buffer flip-flop combine to set resume I flip-flop K716/K717. A reset output of K716/K717 is inverted by J934 through J937 to transfer rank I of the BER to rank II.

After 0.1 microsecond, the set output of resume I flip-flop sets resume II flip-flop. A reset output from the latter flip-flop is inverted by J938 through J941 to advance the count in the BER. After the output equipment removes the output resume, the set output of K718/K719 is gated into D703. After 0.2 microsecond, resume III flip-flop is set. Set outputs from this flip-flop cause the resume cycle to clear and the read flip-flop to set if the contents of BER and BXR are not equal. Setting the read flip-flop causes the buffer cycle to repeat for the next output word.

This process is repeated until the contents of the BER equals the contents of the BXR, at which time the buffer terminates.

MEMORY-TO-MEMORY TRANSFER LOGIC

Channel 2 must be selected by the Compute Unit prior to a memory-to-memory transfer. When a memory-to-memory transfer signal is generated by the Compute Unit, the 1 output from R076 sets K476/K477, Figure 3-20.

When an initiate buffer output command occurs, the 1 outputs of J972 and R068 set channel 3 input buffer flip-flop K650/K651. The 1 outputs of R068 and J704 set channel 2 output buffer flip-flop K452/K453 and channel 2 read flip-flop K722/K723. If channel 2 is not currently gating data from memory into the BFR and channel 3 is not performing a memory reference, a set output from K722/K723 sets priority flip-flop K700/K701. A reset output from K722/K723 produces 1 outputs from J943, J944, and J945. These signals gate the contents of channel 2 BER and BBC onto the data lines to memory.

Reset outputs from K700/K701 and K722/K723 disable both AND gates to J887. The resultant 1 output causes T038 to send a read signal to memory.

The set output from K700/K701 and a set output of K722/K723 satisfy the AND input to J884. The resultant 1 output from J885 is delayed by D701. After 0.2 microsecond, T037 sends a memory request to memory.

When the memory begins reading the data word at the address specified by the contents of channel 2 BER and BBC, a resume I is returned to the I/O Unit. A delayed channel 2 priority set output, the 1 output from J972, and the 1 output from R041 set K778/K779. After 0.3 microsecond, the 0 output at J546 provides 1 outputs at J547 and J548, which gates the data word from memory into the channel 3 BFR. After 0.2 microsecond the 1 output of J547 resets K778/K779.

The 1 output at R041, the set output from K452/K453, and the delayed channel 2 priority set output also combine to set K728/K729. The set output from K728/K729 resets K722/K723. After 0.3 microsecond, the 1 output from J947 resets K700/K701. After 0.2 microsecond, the 1 output from D722 resets K728/K729.

The 1 outputs from J972 and J947 set channel 3 write request flip-flop K764/K765. Since the channel 2 read and write flip-flops are reset, the set output of K764/K765 sets channel 3 priority flip-flop K702/K703.

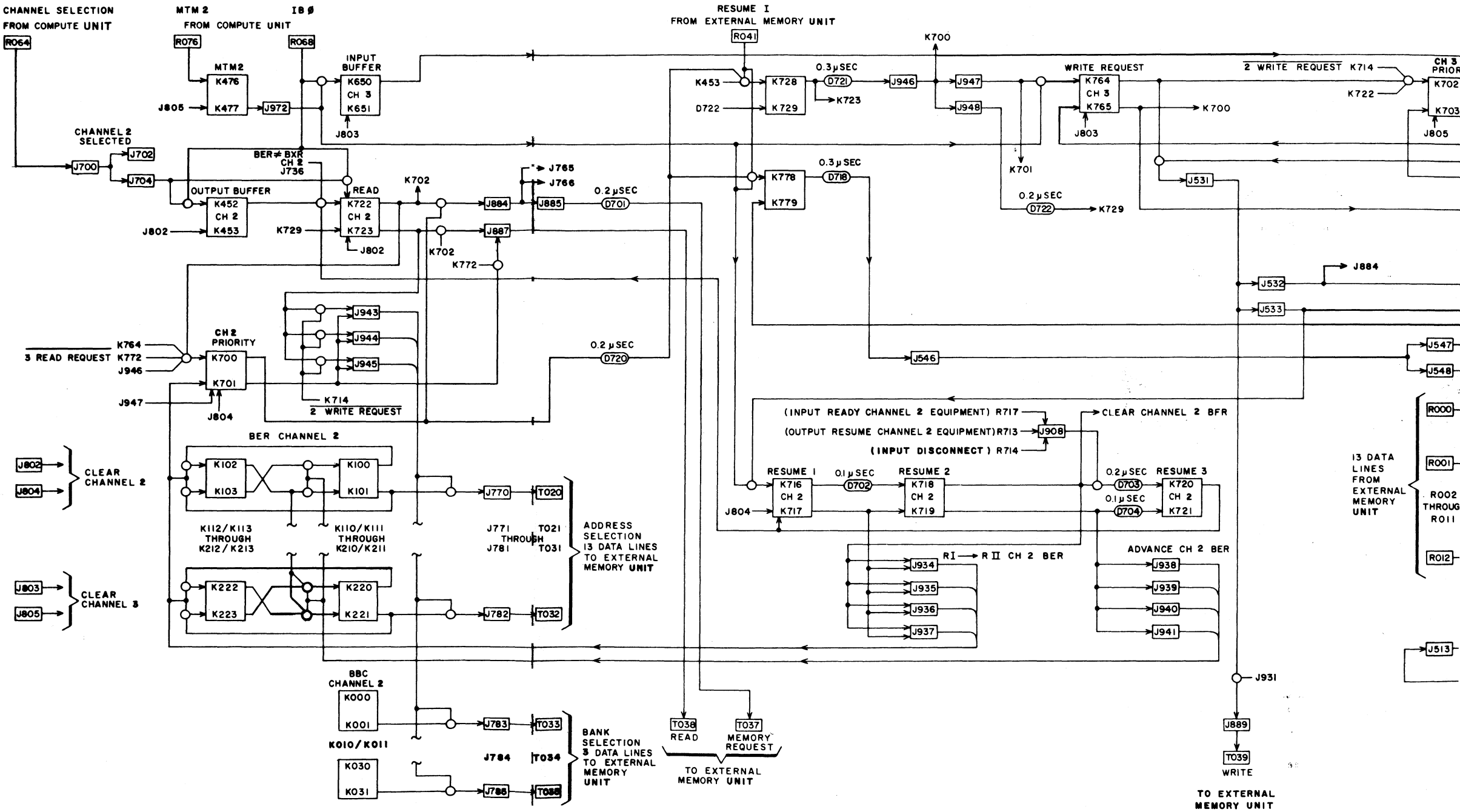
A reset output from K764/K765 produces 1 outputs from J543, J544, J545 which gate the contents of channel 3 BER and BBC onto the signal lines to memory.

After 0.2 microsecond, the set output of K702/K703, the reset output of K728/K729, and the 1 output of J946 satisfy the AND input to J531. The resultant 1 outputs from J532 and J533 gate the complement data word in the channel 3 BFR into J850 through J862. The 1 outputs of J765 and J766 gate the data onto the transmission lines to memory.

A 1 output also occurs from J889. The 1 output of J889 causes T039 to send a write signal to memory. The 1 output of J532 produces a 0 output from J884 and a 1 output from J885. After 0.1 microsecond, T037 sends a memory request to memory. This signal causes memory to store the data word at the address in the bank specified by the contents of channel 3 BER and BBC, respectively.

The 1 outputs from J533 and J972 set channel 2 resume I flip-flop. Setting this flip-flop initiates the channel 2 resume cycle, which updates the contents of the channel 2 BER and prepares for the reset work. At the end of the resume cycle, the channel 2 read flip-flop is set unless the last word has been processed. If the flip-flop sets, channel 2 begins the processing of the next word.

When the Memory Unit generates a resume I signal, the 1 output of R041 removes the memory request signal and sets resume I flip-flop K040/K041. After


CHANNEL SELECTION FROM COMPUTE UNIT
R064
MTM 2 FROM COMPUTE UNIT
R076
IB Ø
R068
MTM2
K476
K477
J805
J972
INPUT BUFFER
K650 CH 3 K651
J803
RESUME I FROM EXTERNAL MEMORY UNIT
R041
K700
K453
D722
K728
K729
0.3 µSEC
D721
K723
J946
J947
J948
WRITE REQUEST
K764 CH 3 K765
J803
K700
2 WRITE REQUEST K714
K722
CH 3 PRIOR
K702
K703
J805
K701
CHANNEL 2 SELECTED
J700
J702
J704
BER≠BXR CH 2 J736
OUTPUT BUFFER
K452 CH 2 K453
J802
READ
K722 CH 2 K723
K729
J802
K702
J884
J765
J766
J885
0.2 µSEC
D701
J887
K702
K772
K778
K779
0.3 µSEC
D718
0.2 µSEC
D722
K729
J531
J532
J884
J533
J943
J944
J945
CH 2 PRIORITY
K700
K701
K764
3 READ REQUEST K772
J946
J947
J804
K714
2 WRITE REQUEST
0.2 µSEC
D720
J546
J547
J548
R000
(INPUT READY CHANNEL 2 EQUIPMENT) R717
(OUTPUT RESUME CHANNEL 2 EQUIPMENT) R713
(INPUT DISCONNECT) R714
J908
CLEAR CHANNEL 2 BFR
BER CHANNEL 2
J802
J804
CLEAR CHANNEL 2
K102
K103
K100
K101
J770
T020
RESUME 1
K716 CH 2 K717
0.1 µSEC
D702
RESUME 2
K718 CH 2 K719
0.2 µSEC
D703
0.1 µSEC
D704
RESUME 3
K720 CH 2 K721
J804
K112/K113 THROUGH K212/K213
K110/K111 THROUGH K210/K211
J771 THROUGH J781
T021 THROUGH T031
ADDRESS SELECTION 13 DATA LINES TO EXTERNAL MEMORY UNIT
J803
J805
CLEAR CHANNEL 3
K222
K223
K220
K221
J782
T032
RI → R II CH 2 BER
J934
J935
J936
J937
ADVANCE CH 2 BER
J938
J939
J940
J941
13 DATA LINES FROM EXTERNAL MEMORY UNIT
R001
R002 THROUGH R011
R012
J513
BBC CHANNEL 2
K000
K001
K010/K011
K030
K031
J783
T033
J784
T034
J785
T035
BANK SELECTION 3 DATA LINES TO EXTERNAL MEMORY UNIT
T038
READ
T037
MEMORY REQUEST
TO EXTERNAL MEMORY UNIT
J931
J889
T039
WRITE
TO EXTERNAL MEMORY UNIT

UNIT

K700

0.3 μSEC D721 → J946 → J947 → K723

J948

K701

WRITE REQUEST K764 CH 3 K765 → K700

J803

2 WRITE REQUEST K714

K722

CH 3 PRIORITY K702 K703

J805

0.2 μSEC D717 → J887

0.3 μSEC D718

0.2 μSEC D722 → K729

J531

J532 → J884

J533

J546

J547

J548

0.2 μSEC D719

BFR CHANNEL 3 K506 K507 K516 K517 K626 K627

R000 R001 R002 THROUGH R011 R012

13 DATA LINES FROM EXTERNAL MEMORY UNIT

K526/K527 THROUGH K616/K617

J850 J851 J852 THROUGH J861 J862

T000 T001 T002 THROUGH T011 T012

13 DATA LINES TO EXTERNAL MEMORY UNIT

J513 → J514 J515

RESUME I WRITE-FROM EXTERNAL MEMORY UNIT R041

(INPUT READY CHANNEL 3 EQUIPMENT) R767

(OUTPUT RESUME CHANNEL 2 EQUIPMENT) R763

(INPUT DISCONNECT) R764

J508

RESUME I K766 CH 3 K767 ← J805

0.1 μSEC D711

RESUME 2 K768 CH 3 K769

0.2 μSEC D712

0.1 μSEC D713

RESUME 3 K770 CH 3 K771

RESUME I 0.1 μSEC D041

K040 K041

0.2 μSEC D040 → J840

R I → R II CH 3 BER

J534 J535 J536 J537

ADVANCE CH 3 BER

J538 J539 J540 J541

J765 J766 J884

J543 J544 J545

K772 3 READ REQUEST

BER CHANNEL 3

K108 K109 K106 K107

J770 → T020

K118/K119 THROUGH K218/K219

K116/K117 THROUGH K216/K217

J771 THROUGH J781 T021 THROUGH T031

ADDRESS SELECTION 13 DATA LINES TO EXTERNAL MEMORY UNIT

K228 K229 K226 K227

J782 → T032

BBC CHANNEL 3 K006 K007

K016/K017

J783 → T033

J784 T034

BANK SELECTION 3 DATA LINES TO EXTERNAL MEMORY UNIT

K026 K027

J785 → T035

UT READY CHANNEL 2 EQUIPMENT) R717

PUT RESUME CHANNEL 2 EQUIPMENT) R713

(INPUT DISCONNECT) R714

J908

→ CLEAR CHANNEL 2 BFR

I 0.1 μSEC D702 RESUME 2 K718 CH 2 K719

0.2 μSEC D703 0.1 μSEC D704 RESUME 3 K720 CH 2 K721

R I → R II CH 2 BER

J934 J935 J936 J937

ADVANCE CH 2 BER

J938 J939 J940 J941

J931

J889

T039 WRITE

TO EXTERNAL MEMORY UNIT

0.1 microsecond, the set output of K040/K041 initiates the channel 3 resume cycle which updates the contents of the channel 3 BER. The memory-to-memory transfer continues until the contents of channel 2 BER and BXR are equal. When this condition occurs, the transfer of data from one memory bank to another is complete.

SECTION 3

I/O UNIT

EQUIPMENT DIAGRAMS

SECTION 3

I/O UNIT

LOGIC DIAGRAMS

- Symbol Index
- Logic Diagrams

D040	1M004A	.2 MICRO SEC DELAY-CLEAR RES I FF	6
D041	1M003A	.1 MICRO SEC DELAY-RES I	6
D401	1K018A	5 MICRO SEC DELAY-CLR BFR CTRLS-CH 2	3
D403	1N013C	.1 MICRO SEC DELAY-REGISTER SET PULSE	5
D404	1N013D	.1 MICRO SEC DELAY-EXT EQUIP TO BFR-CH 2	6
D405	1M005A	.1 MICRO SEC DELAY-I/O UNIT RESUME TO COMPUTE	5
D406	1M005B	.1 MICRO SEC DELAY-NOT-INA2	6
D407	1N013A	.1 MICRO SEC DELAY-FUNCTION READY CONTROL-CH 2	5
D408	1N008A	.5 MICRO SEC DELAY-EXTERNAL FUNCTION READY-CH 2	5
D476	1C027A	.2 MICRO SEC DELAY-NOT-MTM2 TRANSFER	3
D593	1N001A	2 MICRO SEC DELAY-OUTPUT RESUME-CH 3	9
D600	1N026A	5 MICRO SEC DELAY-CLR BFR CTRLS-CH 3	3
D602	1N027A	.1 MICRO SEC DELAY-EXT EQUIP TO BFR-CH 3	9
D603	1M005C	.1 MICRO SEC DELAY-NOT-INA2	9
D606	1C023A	.1 MICRO SEC DELAY-FUNCTION READY CONTRL-CH 3	5
D607	10014A	3.5 MICRO SEC DELAY-EXTERNAL FUNCTION READY-CH 3	5
D700	1L007B	.1 MICRO SEC DELAY-EXT EQUIP TO BFR-CH 2	6
D701	1L018A	.1 MICRO SEC DELAY-MEMORY REQUEST	6
D702	1L007C	.1 MICRO SEC DELAY-RES FF1-CH 2	6
D703	1L006A	.2 MICRO SEC DELAY-RES FF2-CH 2	6
D704	1L007D	.1 MICRO SEC DELAY-NOT-RES FF2-CH 2	6
D705	10012A	23.5 MICRO SEC DELAY-FUNCTION READY	5
D706	1J003A	3.5 MICRO SEC DELAY-INFORMATION READY	6
D707	1K010A	.2 MICRO SEC DELAY-INPUT READY-CH 2	6
D708	1C009A	3.5 MICRO SEC DELAY-INFORMATION READY-CH 3	9
D709	1C026A	.2 MICRO SEC DELAY-INPUT READY-CH 3	9
D710	1C023B	.1 MICRO SEC DELAY-EXT EQUIP TO BFR-CH 3	9
D711	1C023C	.1 MICRO SEC DELAY-RES FF1-CH 3	9
D712	1C005A	.2 MICRO SEC DELAY-RES FF2-CH 3	9
D713	1C023D	.1 MICRO SEC DELAY-NOT-RES FF2-CH 3	9
D714	1C024A	.2 MICRO SEC DELAY-INPUT DISC PULSE-CH 2	5
D715	1C025A	.2 MICRO SEC DELAY-INPUT DISC PULSE-CH 3	5
D716	1N014A	3.5 MICRO SEC DELAY- DATA TO EXT EQUIPMENT	6
D717	1G007A	.2 MICRO SEC DELAY-CH 3 PRIORITY	3
D718	1F012A	.3 MICRO SEC DELAY-READ RESUME-CH 3	9
D719	1F013A	.2 MICRO SEC DELAY-MEM TO BFR-CH 3	9
D720	1L023A	.2 MICRO SEC DELAY-CH.2 PRIORITY	3
D721	1L024A	.3 MICRO SEC DELAY-READ RESUME-CH 2	6
D722	1L025A	.2 MICRO SEC DELAY-MEM TO BFR-CH 2	6
D809	1M005D	.1 MICRO SEC DELAY-IBI2+IB02 PULSE	6
D810	1L007A	.1 MICRO SEC DELAY-IBI2+IB02 PULSE	6
D917	10009A	3.5 MICRO SEC DELAY-INPUT READY-CH 2	6
D967	10023A	3.5 MICRO SEC DELAY-INPUT READY-CH 3	9
D993	10018A	2 MICRO SEC DELAY-OUTPUT RESUME-CH 2	6
J476	10007A	NOT-INP BFR ACTIVE CH 3 MTM2	3
J501	10021B	NOT-BFR TO A CH 3	5
J502	10020A	GATE BFR TO A CH 3	5
J503	10020B	GATE BFR TO A CH 3	5
J504	1R007A	COMPUTE OR MEMORY MASTER CLEAR	3
J505	10017B	NOT-COMPUTE TO BFR CH 3	5
J506	10016B	GATE COMPUTE DATA TO BFR CH 3	5
J507	10016A	GATE COMPUTE DATA TO BFR CH 3	5
J508	1F018B	NOT-(INP RDY+OUT RES+INP DISC)-CH 3	9
J509	1M009B	INPUT DISCONNECT CONTROL CH 3	5
J510	1M008B	CH 3 BUSY	3
J511	1M009A	BUFFER TERMINATION INTERRUPT CONTROL-CH 3	5
J512	1M015B	BUFFER TERMINATION INTERRUPT-CH 3	5
J513	1N007A	CLEAR BFR CONTROL-CH 3	9
J514	1N006A	CLEAR BFR CH 3	9
J515	1N006B	CLEAR BFR CH 3	9
J516	1M014A	FUNCTION READY CONTROL-CH 3	5
J523	10015A	EXT. EQUIP. TO BFR CONTROL-CH 3	9
J525	1C018A	INA3 CH 3 NOT BUSY	9
J526	10022A	EXT. EQUIP. TO BFR CONTROL-CH 3	9
J527	1N022A	GATE EXT. EQUIP. DATA TO BFR-CH 3	9
J528	1N022B	GATE EXT. EQUIP. DATA TO BFR-CH 3	9
J529	1F022A	GATE BFR DATA TO COMPUTE-CH 3	9
J530	1F022B	GATE BFR DATA TO COMPUTE-CH 3	9
J531	1L020A	BFR TO MEMORY CONTROL-CH 3	9
J532	1L020B	GATE BFR TO MEMORY-CH 3	9
J533	1L021A	GATE BFR TO MEMORY-CH 3	9
J534	1D025A	RANK $\bar{1}$ TO RANK 2 BFR CH 3	9
J535	1D025B	RANK $\bar{1}$ TO RANK 2 BFR CH 3	9
J536	1D026A	RANK $\bar{1}$ TO RANK 2 BFR CH 3	9
J537	1D026B	RANK $\bar{1}$ TO RANK 2 BFR CH 3	9
J538	1F027A	ADVANCE BFR CH 3	9
J539	1F027B	ADVANCE BFR CH 3	9
J540	1F026A	ADVANCE BFR CH 3	9
J541	1F026B	ADVANCE BFR CH 3	9
J543	1G026A	GATE BFR•BBC TO MEMORY-CH 3	9
J544	1G025A	GATE BFR•BBC TO MEMORY-CH 3	9
J545	1G024A	GATE BFR•BBC TO MEMORY-CH 3	9
J546	1M011A	MEMORY TO BFR CONTROL-CH 3	9
J547	10022B	GATE MEMORY TO BFR-CH 3	9
J548	10021A	GATE MEMORY TO BFR-CH 3	9
J549	1C008B	GATE BFR TO EXT. EQUIPMENT-CH 3	9
J550	1C008A	GATE BFR TO EXT. EQUIPMENT-CH 3	9
J551	1F014A	COMPUTE TO BBC CONTROL-CH 3	5
J552	1F014B	GATE COMPUTE DATA TO BBC-CH 3	5
J555	1F011A	A TO BER CONTROL-CH 3	5
J556	1F011B	GATE A TO BER-CH 3	5
J557	1F010A	GATE A TO BER-CH 3	5
J558	1F010B	GATE A TO BER-CH 3	5
J559	1K009B	GATE A TO BER-CH 3	5
J561	1F023B	A TO BXR CONTROL-CH 3	5
J562	1F023A	GATE A TO BXR-CH 3	5
J563	1F024A	GATE A TO BXR-CH 3	5
J564	1C003B	GATE A TO BXR-CH 3	5
J565	1F024B	GATE A TO BXR-CH 3	5
J593	1N002B	OUTPUT RESUME-CH 3	9
J594	1N002A	OUTPUT RESUME-CH 3	9
J610	1G009A	CH 3 BER COUNTER CARRY LOGIC	11
J611	1G010B	CH 3 BER COUNTER CARRY LOGIC	11
J612	1C002B	CH 3 BER COUNTER CARRY LOGIC	11
J613	1G009B	CH 3 BER COUNTER CARRY LOGIC	11
J614	1G011A	CH 3 BER•BXR COMPARE LOGIC	11
J615	1G012A	CH 3 BER•BXR COMPARE LOGIC	11
J616	1G016A	CH 3 BER•BXR COMPARE LOGIC	11
J617	1G014A	CH 3 BER•BXR COMPARE LOGIC	11
J618	1G015A	CH 3 BER•BXR COMPARE LOGIC	11
J619	1G013A	CH 3 BER•BXR COMPARE LOGIC	11
J635	1G004B	BER=BXR CH 3	11
J636	1G005A	BER NOT=BXR CH 3	11
J700	1M025A	NOT-CH 2 SELECTED	3
J701	1M025B	CHANNEL SELECT CODE INVERTER-BIT 0	3
J702	1M024A	CH 2 SELECTED	3
J703	1L021B	NOT-CH 3 SELECTED	3
J704	1M024B	CH 2 SELECTED	3
J705	1M022A	CH 3 SELECTED	3
J706	10005A	23.5 MICRO SEC DELAYED FUNCTION READY	5
J707	1M022B	CH 3 SELECTED	3
J710	1G018A	CH 2 BER COUNTER CARRY LOGIC	8
J711	1G010A	CH 2 BER COUNTER CARRY LOGIC	8
J712	1G027A	CH 2 BER COUNTER CARRY LOGIC	8

J713	1G018B	CH 2 BER COUNTER CARRY LOGIC	8
J714	1G019A	CH 2 BER•BXR COMPARE LOGIC	8
J715	1G020A	CH 2 BER•BXR COMPARE LOGIC	8
J716	1G021A	CH 2 BER•BXR COMPARE LOGIC	8
J717	1G017A	CH 2 BER•BXR COMPARE LOGIC	8
J718	1G022A	CH 2 BER•BXR COMPARE LOGIC	8
J719	1G013B	CH 2 BER•BXR COMPARE LOGIC	8
J720	1P027B	DATA INVERTER-DATA FROM COMPUTE-BIT 0	3
J721	1P026B	DATA INVERTER-DATA FROM COMPUTE-BIT 1	3
J722	1P025B	DATA INVERTER-DATA FROM COMPUTE-BIT 2	3
J723	1P024B	DATA INVERTER-DATA FROM COMPUTE-BIT 3	3
J724	1P023B	DATA INVERTER-DATA FROM COMPUTE-BIT 4	3
J725	1P022B	DATA INVERTER-DATA FROM COMPUTE-BIT 5	3
J726	1P021B	DATA INVERTER-DATA FROM COMPUTE-BIT 6	3
J727	1P020B	DATA INVERTER-DATA FROM COMPUTE-BIT 7	3
J728	1P019B	DATA INVERTER-DATA FROM COMPUTE-BIT 8	3
J729	1P018B	DATA INVERTER-DATA FROM COMPUTE-BIT 9	3
J730	1P017B	DATA INVERTER-DATA FROM COMPUTE-BIT 10	3
J731	1P016B	DATA INVERTER-DATA FROM COMPUTE-BIT 11	3
J732	1P015B	DATA INVERTER-DATA FROM COMPUTE-BIT 12	3
J735	1G004A	BER=BXR CH 2	8
U736	1G003A	BER NOT=BXR CH 2	8
J741	1N005A	DATA INVERTER-DATA FROM COMPUTE-BIT 1	3
J742	1N005B	DATA INVERTER-DATA FROM COMPUTE-BIT 2	3
J743	1N004A	DATA INVERTER-DATA FROM COMPUTE-BIT 3	3
J744	1N004B	DATA INVERTER-DATA FROM COMPUTE-BIT 4	3
J750	1P027A	BER,BFR DATA TO COMPUTE-BIT 0	4
J751	1P026A	BER,BFR DATA TO COMPUTE-BIT 1	4
J752	1P025A	BER,BFR DATA TO COMPUTE-BIT 2	4
J753	1P024A	BER,BFR DATA TO COMPUTE-BIT 3	4
J754	1P023A	BER,BFR DATA TO COMPUTE-BIT 4	4
J755	1P022A	BER,BFR DATA TO COMPUTE-BIT 5	4
J756	1P021A	BER,BFR DATA TO COMPUTE-BIT 6	4
J757	1P020A	BER,BFR DATA TO COMPUTE-BIT 7	4
J758	1P019A	BER,BFR DATA TO COMPUTE-BIT 8	4
J759	1P018A	BER,BFR DATA TO COMPUTE-BIT 9	4
J760	1P017A	BER,BFR DATA TO COMPUTE-BIT 10	4
J761	1P016A	BER,BFR DATA TO COMPUTE-BIT 11	4
J762	1P015A	BER,BFR DATA TO COMPUTE-BIT 12	4
J763	10011A	GATE BER,BFR TO COMPUTE-BITS 0-6	4
J764	10011B	GATE BER,BFR TO COMPUTE-BITS 7-12	4
J765	10010A	GATE DATA TO EXTERNAL MEMORY-BITS 0-6	4
J766	10010B	GATE DATA TO EXTERNAL MEMORY-BITS 7-12	4
J770	1P014A	ADDRESS TO EXTERNAL MEMORY-BIT 0	4
J771	1P014B	ADDRESS TO EXTERNAL MEMORY-BIT 1	4
J772	1P013A	ADDRESS TO EXTERNAL MEMORY-BIT 2	4
J773	1P013B	ADDRESS TO EXTERNAL MEMORY-BIT 3	4
J774	1P012A	ADDRESS TO EXTERNAL MEMORY-BIT 4	4
J775	1P012B	ADDRESS TO EXTERNAL MEMORY-BIT 5	4
J776	1P011A	ADDRESS TO EXTERNAL MEMORY-BIT 6	4
J777	1P011B	ADDRESS TO EXTERNAL MEMORY-BIT 7	4
J778	1P010A	ADDRESS TO EXTERNAL MEMORY-BIT 8	4
J779	1P010B	ADDRESS TO EXTERNAL MEMORY-BIT 9	4
J780	1P009A	ADDRESS TO EXTERNAL MEMORY-BIT 10	4
J781	1P009B	ADDRESS TO EXTERNAL MEMORY-BIT 11	4
J782	10010A	ADDRESS TO EXTERNAL MEMORY-BIT 12	4
J783	10010B	BANK SELECT TO EXTERNAL MEMORY-BIT 1	4
J784	10006A	BANK SELECT TO EXTERNAL MEMORY-BIT 2	4
J785	10006B	BANK SELECT TO EXTERNAL MEMORY-BIT 3	4
J800	10026A	NOT-MC+CBC2+CH 2 BFR TERM INT	3
J801	1N023A	NOT-MC+CBC3+CH 3 BFR TERM+MTM2 TERM	3
J802	10026B	CLEAR BUFFER CONTROLS-CH 2	3
J803	10024A	CLEAR BUFFER CONTROLS-CH 3	3
J804	10025B	CLEAR BUFFER CONTROLS-CH 2	3
J805	10024B	CLEAR BUFFER CONTROLS-CH 3	3
J806	1C020B	NOT-IBI+IBO	5
J807	1C019B	IBI+IBO	5
J808	1K004B	NOT-CRC	3
J809	1N011A	IBI (PULSED)	6
J810	1N011B	IBO (PULSED)	6
J840	1N007B	RESUME 1 CONTROL	6
J850	10005B	DATA TO EXTERNAL MEMORY-BIT 0	4
J851	10004A	DATA TO EXTERNAL MEMORY-BIT 1	4
J852	10004B	DATA TO EXTERNAL MEMORY-BIT 2	4
J853	10003A	DATA TO EXTERNAL MEMORY-BIT 3	4
J854	10003B	DATA TO EXTERNAL MEMORY-BIT 4	4
J855	10002A	DATA TO EXTERNAL MEMORY-BIT 5	4
J856	10002B	DATA TO EXTERNAL MEMORY-BIT 6	4
J857	1P004A	DATA TO EXTERNAL MEMORY-BIT 7	4
J858	1P004B	DATA TO EXTERNAL MEMORY-BIT 8	4
J859	1P003A	DATA TO EXTERNAL MEMORY-BIT 9	4
J860	1P003B	DATA TO EXTERNAL MEMORY-BIT 10	4
J861	1P002A	DATA TO EXTERNAL MEMORY-BIT 11	4
J862	1P002B	DATA TO EXTERNAL MEMORY-BIT 12	4
J884	1M006A	REQUEST MEMORY CONTROL	6
J885	1M010A	REQUEST MEMORY CONTROL	6
J887	1K011B	REQUEST READ	6
J889	1M010B	REQUEST WRITE	6
J891	1C021B	NOT-INA(2+3) DISCONNECT	5
J892	1N003B	INA(2+3) DISCONNECT	5
J893	1M017B	NOT-INA(2+3) CH NOT BUSY+FUNCTION READY	5
J894	1K009A	I/O RESUME CONTROL	5
J895	1L014B	I/O RESUME CONTROL	5
J896	1L012A	I/O RESUME TO COMPUTE	5
J897	1L012B	I/O RESUME LOGIC TO COMPUTE	5
J901	1N012A	BER TO A CONTROL-CH 2	5
J902	1N012B	GATE BER TO A-CH 2	5
J903	1N010A	GATE BER TO A-CH 2	5
J905	1N010B	NOT-COMPUTE TO BFR CH 2	5
J906	1N009A	GATE COMPUTE DATA TO BFR CH 2	5
J907	1N009B	GATE COMPUTE DATA TO BFR CH 2	5
J908	1F018A	NOT-(INP RDY-OUT RES+INP DISC)-CH 2	6
J909	1L019A	INPUT DISCONNECT CONTROL-CH 2	5
J910	1M008A	CH 2 BUSY	3
J911	1M017A	BUFFER TERMINATION INTERRUPT CONTROL-CH 2	5
J912	1M016A	BUFFER TERMINATION INTERRUPT-CH 2	5
J913	1N003A	CLEAR BFR CONTROL-CH 2	6
J914	1M016B	CLEAR BFR-CH 2	6
J915	1M015A	CLEAR BFR-CH 2	6
J916	1M014B	FUNCTION READY CONTROL-CH 2	5
J917	1L014A	CH 2 PRIORITY CONTROL	3
J923	10015B	EXT EQUIP. TO BFR CONTROL-CH 2	6
J925	1C018B	INA2 CH 2 NOT BUSY	6
J926	10007B	EXT. EQUIP. TO BFR CONTROL-CH 2	6
J927	1F006A	GATE EXT. EQUIPMENT DATA TO BFR-CH 2	6
J928	1F006B	GATE EXT. EQUIPMENT DATA TO BFR-CH 2	6
J929	1F007A	GATE BFR TO COMPUTE-CH 2	6
J930	1F007B	GATE BFR TO COMPUTE-CH 2	6
J931	1L016A	NOT-REQUEST WRITE CH 2	6
J932	1L016B	GATE BFR TO MEMORY-CH 2	6
J933	1L017A	GATE BFR TO MEMORY-CH 2	6
J934	1M020A	RANK $\overline{1}$ TO RANK 2 BER CH 2	6
J935	1M020B	RANK $\overline{1}$ TO RANK 2 BER CH 2	6
J936	1M019A	RANK $\overline{1}$ TO RANK 2 BER CH 2	6

J937	1M019B	RANK 1 TO RANK 2 BER CH 2	6
J938	1G026B	ADVANCE BER CH 2	6
J939	1G027B	ADVANCE BER CH 2	6
J940	1G025B	ADVANCE BER CH 2	6
J941	1G024B	ADVANCE BER CH 2	6
J943	1L011B	GATE BER+BBC TO MEMORY-CH 2	6
J944	1L011A	GATE BER+BBC TO MEMORY-CH 2	6
J945	1L010A	GATE BER+BBC TO MEMORY-CH 2	6
J946	1L008A	MEMORY TO BER CONTROL-CH 2	6
J947	1L008B	GATE MEMORY TO BER-CH 2	6
J948	1L010B	GATE MEMORY TO BER-CH 2	6
J949	1F004A	GATE BER TO EXT. EQUIPMENT-CH 2	6
J950	1F004B	GATE BER TO EXT. EQUIPMENT-CH 2	6
J951	10013A	COMPUTE TO BBC CONTROL-CH 2	5
J952	10013B	GATE COMPUTE DATA TO BBC-CH 2	5
J954	1P008A	NOT-SET BBC+SET BER+SET BXR	5
J955	1P007A	A TO BER CONTROL-CH 2	5
J956	1P007B	GATE A TO BER CH 2	5
J957	1P006A	GATE A TO BER CH 2	5
J958	1P006B	GATE A TO BER CH 2	5
J959	10017A	GATE A TO BER CH 2	5
J960	1P005A	SET BBC+SET BER+SET BXR	5
J961	1P005B	A TO BXR CONTROL-CH 2	5
J962	10008B	GATE A TO BXR CH 2	5
J963	10008A	GATE A TO BXR CH 2	5
J964	10011B	GATE A TO BXR CH 2	5
J965	10011A	GATE A TO BXR CH 2	5
J966	1L019B	SET BBC+SET BER+SET BXR (PULSED)	3
J972	1L017B	MTM2	5
J973	1R007B	PARITY CHECK	6
J993	10019B	OUTPUT RESUME-CH 2	6
J994	10019A	OUTPUT RESUME-CH 2	5
K000	1N017A	CH 2 BUFFER RANK CONTROL-BIT 0	5
K001	1N017B	CH 2 BUFFER RANK CONTROL-BIT 0	5
K006	1N021A	CH 3 BUFFER RANK CONTROL-BIT 0	5
K007	1N021B	CH 3 BUFFER RANK CONTROL-BIT 0	5
K010	1N016A	CH 2 BUFFER RANK CONTROL-BIT 1	5
K011	1N016B	CH 2 BUFFER RANK CONTROL-BIT 1	5
K016	1N020A	CH 3 BUFFER RANK CONTROL-BIT 1	5
K017	1N020B	CH 3 BUFFER RANK CONTROL-BIT 1	5
K020	1N015A	CH 2 BUFFER RANK CONTROL-BIT 2	5
K021	1N015B	CH 2 BUFFER RANK CONTROL-BIT 2	5
K026	1N019A	CH 3 BUFFER RANK CONTROL-BIT 2	5
K027	1N019B	CH 3 BUFFER RANK CONTROL-BIT 2	5
K040	1M002A	RESUME 1 F/F	6
K041	1M002B	RESUME 1 F/F	6
K100	1I026A	CH 2 BER-BIT 0	8
K101	1I026B	CH 2 BER-BIT 0	8
K102	1H026A	CH 2 BER RANK 2(COUNTER)-BIT 0	8
K103	1H026B	CH 2 BER RANK 2(COUNTER)-BIT 0	8
K106	1J025A	CH 3 BER-BIT 0	11
K107	1J025B	CH 3 BER-BIT 0	11
K108	1H014A	CH 3 BER RANK 2(COUNTER)-BIT 0	11
K109	1H014B	CH 3 BER RANK 2(COUNTER)-BIT 0	11
K110	1I025A	CH 2 BER-BIT 1	8
K111	1I025B	CH 2 BER-BIT 1	8
K112	1H025A	CH 2 BER RANK 2(COUNTER)-BIT 1	8
K113	1H025B	CH 2 BER RANK 2(COUNTER)-BIT 1	8
K116	1J024A	CH 3 BER-BIT 1	11
K117	1J024B	CH 3 BER-BIT 1	11
K118	1H013A	CH 3 BER RANK 2(COUNTER)-BIT 1	11
K119	1H013B	CH 3 BER RANK 2(COUNTER)-BIT 1	11
K120	1I024A	CH 2 BER-BIT 2	8
K121	1I023A	CH 2 BER-BIT 2	8
K122	1H024A	CH 2 BER RANK 2(COUNTER)-BIT 2	8
K123	1H024B	CH 2 BER RANK 2(COUNTER)-BIT 2	8
K126	1J023A	CH 3 BER-BIT 2	11
K127	1J022A	CH 3 BER-BIT 2	11
K128	1H012A	CH 3 BER RANK 2(COUNTER)-BIT 2	11
K129	1H012B	CH 3 BER RANK 2(COUNTER)-BIT 2	11
K130	1I022A	CH 2 BER-BIT 3	8
K131	1I022B	CH 2 BER-BIT 3	8
K132	1H023A	CH 2 BER RANK 2(COUNTER)-BIT 3	8
K133	1H023B	CH 2 BER RANK 2(COUNTER)-BIT 3	8
K136	1J021A	CH 3 BER-BIT 3	11
K137	1J021B	CH 3 BER-BIT 3	11
K138	1H011A	CH 3 BER RANK 2(COUNTER)-BIT 3	11
K139	1H011B	CH 3 BER RANK 2(COUNTER)-BIT 3	11
K140	1I021A	CH 2 BER-BIT 4	8
K141	1I020A	CH 2 BER-BIT 4	8
K142	1H022A	CH 2 BER RANK 2(COUNTER)-BIT 4	8
K143	1H022B	CH 2 BER RANK 2(COUNTER)-BIT 4	8
K146	1J020A	CH 3 BER-BIT 4	11
K147	1J019A	CH 3 BER-BIT 4	11
K148	1H010A	CH 3 BER RANK 2(COUNTER)-BIT 4	11
K149	1H010B	CH 3 BER RANK 2(COUNTER)-BIT 4	11
K150	1I019A	CH 2 BER-BIT 5	8
K151	1I018A	CH 2 BER-BIT 5	8
K152	1H021A	CH 2 BER RANK 2(COUNTER)-BIT 5	8
K153	1H021B	CH 2 BER RANK 2(COUNTER)-BIT 5	8
K156	1J018A	CH 3 BER-BIT 5	11
K157	1J017A	CH 3 BER-BIT 5	11
K158	1H009A	CH 3 BER RANK 2(COUNTER)-BIT 5	11
K159	1H009B	CH 3 BER RANK 2(COUNTER)-BIT 5	11
K160	1I017A	CH 2 BER-BIT 6	8
K161	1I017B	CH 2 BER-BIT 6	8
K162	1H020A	CH 2 BER RANK 2(COUNTER)-BIT 6	8
K163	1H020B	CH 2 BER RANK 2(COUNTER)-BIT 6	8
K166	1J016A	CH 3 BER-BIT 6	11
K167	1J016B	CH 3 BER-BIT 6	11
K168	1H008A	CH 3 BER RANK 2(COUNTER)-BIT 6	11
K169	1H008B	CH 3 BER RANK 2(COUNTER)-BIT 6	11
K170	1I016A	CH 2 BER-BIT 7	8
K171	1I015A	CH 2 BER-BIT 7	8
K172	1H019A	CH 2 BER RANK 2(COUNTER)-BIT 7	8
K173	1H019B	CH 2 BER RANK 2(COUNTER)-BIT 7	8
K176	1J015A	CH 3 BER-BIT 7	11
K177	1J014A	CH 3 BER-BIT 7	11
K178	1H007A	CH 3 BER RANK 2(COUNTER)-BIT 7	11
K179	1H007B	CH 3 BER RANK 2(COUNTER)-BIT 7	11
K180	1I014A	CH 2 BER-BIT 8	8
K181	1I013A	CH 2 BER-BIT 8	8
K182	1H018A	CH 2 BER RANK 2(COUNTER)-BIT 8	8
K183	1H018B	CH 2 BER RANK 2(COUNTER)-BIT 8	8
K186	1J013A	CH 3 BER-BIT 8	11
K187	1J012A	CH 3 BER-BIT 8	11
K188	1H006A	CH 3 BER RANK 2(COUNTER)-BIT 8	11
K189	1H006B	CH 3 BER RANK 2(COUNTER)-BIT 8	11
K190	1I012A	CH 2 BER-BIT 9	8
K191	1I012B	CH 2 BER-BIT 9	8
K192	1H017A	CH 2 BER RANK 2(COUNTER)-BIT 9	8
K193	1H017B	CH 2 BER RANK 2(COUNTER)-BIT 9	8
K196	1J011A	CH 3 BER-BIT 9	11
K197	1J011B	CH 3 BER-BIT 9	11

K198	1H005A	CH 3 BER RANK 2(COUNTER)-BIT 9	11
K199	1H005B	CH 3 BER RANK 2(COUNTER)-BIT 9	11
K200	1I011A	CH 2 BER-BIT 10	8
K201	1I010A	CH 2 BER-BIT 10	8
K202	1H016A	CH 2 BER RANK 2(COUNTER)-BIT 10	8
K203	1H016B	CH 2 BER RANK 2(COUNTER)-BIT 10	8
K206	1J010A	CH 3 BER-BIT 10	11
K207	1J009A	CH 3 BER-BIT 10	11
K208	1H004A	CH 3 BER RANK 2(COUNTER)-BIT 10	11
K209	1H004B	CH 3 BER RANK 2(COUNTER)-BIT 10	11
K210	1I009A	CH 2 BER-BIT 11	8
K211	1I008A	CH 2 BER-BIT 11	8
K212	1H015A	CH 2 BER RANK 2(COUNTER)-BIT 11	8
K213	1H015B	CH 2 BER RANK 2(COUNTER)-BIT 11	8
K216	1J008A	CH 3 BER-BIT 11	11
K217	1J004A	CH 3 BER-BIT 11	11
K218	1H003A	CH 3 BER RANK 2(COUNTER)-BIT 11	11
K219	1H003B	CH 3 BER RANK 2(COUNTER)-BIT 11	11
K220	1I007A	CH 2 BER-BIT 12	8
K221	1I004A	CH 2 BER-BIT 12	8
K222	1I003A	CH 2 BER RANK 2(COUNTER)-BIT 12	8
K223	1I003B	CH 2 BER RANK 2(COUNTER)-BIT 12	8
K226	1J007A	CH 3 BER-BIT 12	11
K227	1I006A	CH 3 BER-BIT 12	11
K228	1J002A	CH 3 BER RANK 2(COUNTER)-BIT 12	11
K229	1J002B	CH 3 BER RANK 2(COUNTER)-BIT 12	11
K300	1E027A	CH 2 BXR-BIT 0	8
K301	1E027B	CH 2 BXR-BIT 0	8
K306	1E014A	CH 3 BXR-BIT 0	11
K307	1E014B	CH 3 BXR-BIT 0	11
K310	1E026A	CH 2 BXR-BIT 1	8
K311	1E026B	CH 2 BXR-BIT 1	8
K316	1E013A	CH 3 BXR-BIT 1	11
K317	1E013B	CH 3 BXR-BIT 1	11
K320	1E025A	CH 2 BXR-BIT 2	8
K321	1E025B	CH 2 BXR-BIT 2	8
K326	1E012A	CH 3 BXR-BIT 2	11
K327	1E012B	CH 3 BXR-BIT 2	11
K330	1E024A	CH 2 BXR-BIT 3	8
K331	1E024B	CH 2 BXR-BIT 3	8
K336	1E011A	CH 3 BXR-BIT 3	11
K337	1E011B	CH 3 BXR-BIT 3	11
K340	1E023A	CH 2 BXR-BIT 4	8
K341	1E023B	CH 2 BXR-BIT 4	8
K346	1E010A	CH 3 BXR-BIT 4	11
K347	1E010B	CH 3 BXR-BIT 4	11
K350	1E022A	CH 2 BXR-BIT 5	8
K351	1E022B	CH 2 BXR-BIT 5	8
K356	1E009A	CH 3 BXR-BIT 5	11
K357	1E009B	CH 3 BXR-BIT 5	11
K360	1E021A	CH 2 BXR-BIT 6	8
K361	1E021B	CH 2 BXR-BIT 6	8
K366	1E008A	CH 3 BXR-BIT 6	11
K367	1E008B	CH 3 BXR-BIT 6	11
K370	1E020A	CH 2 BXR-BIT 7	8
K371	1E020B	CH 2 BXR-BIT 7	8
K376	1E007A	CH 3 BXR-BIT 7	11
K377	1E007B	CH 3 BXR-BIT 7	11
K380	1E019A	CH 2 BXR-BIT 8	8
K381	1E019B	CH 2 BXR-BIT 8	8
K386	1E006A	CH 3 BXR-BIT 8	11
K387	1E006B	CH 3 BXR-BIT 8	11

K390	1E018A	CH 2 BXR-BIT 9	8
K391	1E018B	CH 2 BXR-BIT 9	8
K396	1E005A	CH 3 BXR-BIT 9	11
K397	1E005B	CH 3 BXR-BIT 9	11
K400	1E017A	CH 2 BXR-BIT 10	8
K401	1E017B	CH 2 BXR-BIT 10	8
K406	1E004A	CH 3 BXR-BIT 10	11
K407	1E004B	CH 3 BXR-BIT 10	11
K410	1E016A	CH 2 BXR-BIT 11	8
K411	1E016B	CH 2 BXR-BIT 11	8
K416	1E003A	CH 3 BXR-BIT 11	11
K417	1E003B	CH 3 BXR-BIT 11	11
K420	1E015A	CH 2 BXR-BIT 12	8
K421	1E015B	CH 2 BXR-BIT 12	8
K426	1E002A	CH 3 BXR-BIT 12	11
K427	1E002B	CH 3 BXR-BIT 12	11
K450	1M013A	INPUT BUFFER CH 2	3
K451	1M013B	INPUT BUFFER CH 2	3
K452	1M012A	OUTPUT BUFFER CH 2	3
K453	1M012B	OUTPUT BUFFER CH 2	3
K472	1K019A	CLEAR BUFFER CONTROLS 1 CH 2	3
K473	1K019B	CLEAR BUFFER CONTROLS 1 CH 2	3
K474	1K020A	CLEAR BUFFER CONTROLS 2 CH 2	3
K475	1K020B	CLEAR BUFFER CONTROLS 2 CH 2	3
K476	1K021A	MTM2 TRANSFER	3
K477	1K021B	MTM2 TRANSFER	3
K500	1D024A	CH 2 BFR DATA REGISTER-BIT 0	7
K501	1D024B	CH 2 BFR DATA REGISTER-BIT 0	7
K506	1D012A	CH 3 BFR DATA REGISTER-BIT 0	10
K507	1D012B	CH 3 BFR DATA REGISTER-BIT 0	10
K510	1D023A	CH 2 BFR DATA REGISTER-BIT 1	7
K511	1D023B	CH 2 BFR DATA REGISTER-BIT 1	7
K516	1D011A	CH 3 BFR DATA REGISTER-BIT 1	10
K517	1D011B	CH 3 BFR DATA REGISTER-BIT 1	10
K520	1D022A	CH 2 BFR DATA REGISTER-BIT 2	7
K521	1D022B	CH 2 BFR DATA REGISTER-BIT 2	7
K526	1D010A	CH 3 BFR DATA REGISTER-BIT 2	10
K527	1D010B	CH 3 BFR DATA REGISTER-BIT 2	10
K530	1D021A	CH 2 BFR DATA REGISTER-BIT 3	7
K531	1D021B	CH 2 BFR DATA REGISTER-BIT 3	7
K536	1D009A	CH 3 BFR DATA REGISTER-BIT 3	10
K537	1D009B	CH 3 BFR DATA REGISTER-BIT 3	10
K540	1D020A	CH 2 BFR DATA REGISTER-BIT 4	7
K541	1D020B	CH 2 BFR DATA REGISTER-BIT 4	7
K546	1D008A	CH 3 BFR DATA REGISTER-BIT 4	10
K547	1D008B	CH 3 BFR DATA REGISTER-BIT 4	10
K550	1D019A	CH 2 BFR DATA REGISTER-BIT 5	7
K551	1D019B	CH 2 BFR DATA REGISTER-BIT 5	7
K556	1D007A	CH 3 BFR DATA REGISTER-BIT 5	10
K557	1D007B	CH 3 BFR DATA REGISTER-BIT 5	10
K560	1D018A	CH 2 BFR DATA REGISTER-BIT 6	7
K561	1D018B	CH 2 BFR DATA REGISTER-BIT 6	7
K566	1D006A	CH 3 BFR DATA REGISTER-BIT 6	10
K567	1D006B	CH 3 BFR DATA REGISTER-BIT 6	10
K570	1D017A	CH 2 BFR DATA REGISTER-BIT 7	7
K571	1D017B	CH 2 BFR DATA REGISTER-BIT 7	7
K576	1D005A	CH 3 BFR DATA REGISTER-BIT 7	10
K577	1D005B	CH 3 BFR DATA REGISTER-BIT 7	10
K580	1D016A	CH 2 BFR DATA REGISTER-BIT 8	7
K581	1D016B	CH 2 BFR DATA REGISTER-BIT 8	7
K586	1D004A	CH 3 BFR DATA REGISTER-BIT 8	10
K587	1D004B	CH 3 BFR DATA REGISTER-BIT 8	10

K590	1D015A	CH 2 BFR DATA REGISTER-BIT 9	7
K591	1D015B	CH 2 BFR DATA REGISTER-BIT 9	7
K596	1D003A	CH 3 BFR DATA REGISTER-BIT 9	10
K597	1D003B	CH 3 BFR DATA REGISTER-BIT 9	10
K600	1D014A	CH 2 BFR DATA REGISTER-BIT 10	7
K601	1D014B	CH 2 BFR DATA REGISTER-BIT 10	7
K606	1D002A	CH 3 BFR DATA REGISTER-BIT 10	10
K607	1D002B	CH 3 BFR DATA REGISTER-BIT 10	10
K610	1D013A	CH 2 BFR DATA REGISTER-BIT 11	7
K611	1D013B	CH 2 BFR DATA REGISTER-BIT 11	7
K616	1D001A	CH 3 BFR DATA REGISTER-BIT 11	10
K617	1D001B	CH 3 BFR DATA REGISTER-BIT 11	10
K620	1C003A	CH 2 BFR DATA REGISTER-BIT 12	7
K621	1C001A	CH 2 BFR DATA REGISTER-BIT 12	7
K626	1C002A	CH 3 BFR DATA REGISTER-BIT 12	10
K627	1C001B	CH 3 BFR DATA REGISTER-BIT 12	10
K650	1K025A	INPUT BUFFER CH 3	3
K651	1K025B	INPUT BUFFER CH 3	3
K652	1K024A	OUTPUT BUFFER CH 3	3
K653	1K024B	OUTPUT BUFFER CH 3	3
K672	1F016A	CLEAR BUFFER CONTROLS 1 CH 3	3
K673	1F016B	CLEAR BUFFER CONTROLS 1 CH 3	3
K674	1F015A	CLEAR BUFFER CONTROLS 2 CH 3	3
K675	1F015B	CLEAR BUFFER CONTROLS 2 CH 3	3
K700	1K015A	CH 2 PRIORITY	3
K701	1K014A	CH 2 PRIORITY	3
K702	1K013A	CH 3 PRIORITY	3
K703	1K014B	CH 3 PRIORITY	3
K704	1K012A	INPUT REQUEST-CH 2	6
K705	1K011A	INPUT REQUEST-CH 2	6
K706	1L013A	I/O RESUME	5
K707	1L013B	I/O RESUME	5
K710	1K008A	CH.2 TERMINATED IN MTM2 TRANSFER	3
K711	1K008B	CH.2 TERMINATED IN MTM2 TRANSFER	3
K712	1K007A	INPUT TO A-CH 2	6
K713	1K007B	INPUT TO A-CH 2	6
K714	1K006A	WRITE REQUEST-CH 2	6
K715	1K006B	WRITE REQUEST-CH 2	6
K716	1K005A	RESUME F/F 1-CH 2	6
K717	1K004A	RESUME F/F 1-CH 2	6
K718	1K003A	RESUME F/F 2-CH 2	6
K719	1K003B	RESUME F/F 2-CH 2	6
K720	1L004A	RESUME F/F 3-CH 2	6
K721	1L004B	RESUME F/F 3-CH 2	6
K722	1L003A	READ REQUEST-CH 2	6
K723	1L003B	READ REQUEST-CH 2	6
K724	1L002A	INFORMATION READY-CH 2	6
K725	1L002B	INFORMATION READY-CH 2	6
K726	1C020A	PARITY ERROR-CH 2	5
K727	1C019A	PARITY ERROR-CH 2	5
K728	1L026A	READ RESUME-CH 2	6
K729	1L026B	READ RESUME-CH 2	6
K730	1K016A	PARITY ERROR TEST-CH 2	5
K731	1K016B	PARITY ERROR TEST-CH 2	5
K754	1C022A	INPUT REQUEST-CH 3	9
K755	1C021A	INPUT REQUEST-CH 3	9
K762	1C017A	INPUT TO A-CH 3	9
K763	1C017B	INPUT TO A-CH 3	9
K764	1C016A	WRITE REQUEST-CH 3	9
K765	1C016B	WRITE REQUEST-CH 3	9
K766	1C010A	RESUME F/F 1-CH 3	9
K767	1C015B	RESUME F/F 1-CH 3	
K768	1C014A	RESUME F/F 2-CH 3	9
K769	1C014B	RESUME F/F 2-CH 3	9
K770	1C013A	RESUME F/F 3-CH 3	9
K771	1C013B	RESUME F/F 3-CH 3	9
K772	1C012A	READ REQUEST-CH 3	9
K773	1C012B	READ REQUEST-CH 3	9
K774	1C011A	INFORMATION READY-CH 3	9
K775	1C015A	INFORMATION READY-CH 3	9
K776	1N025A	PARITY ERROR-CH 3	5
K777	1O025A	PARITY ERROR-CH 3	5
K778	1F020A	READ RESUME-CH 3	9
K779	1F020B	READ RESUME-CH 3	9
K780	1K017A	PARITY ERROR TEST-CH 3	5
K781	1K017B	PARITY ERROR TEST-CH 3	5
R000	1S027A	DATA FROM MEMORY-BIT 0	7
R001	1S027B	DATA FROM MEMORY-BIT 1	7
R002	1S026A	DATA FROM MEMORY-BIT 2	7
R003	1S026B	DATA FROM MEMORY-BIT 3	7
R004	1S025A	DATA FROM MEMORY-BIT 4	7
R005	1S025B	DATA FROM MEMORY-BIT 5	7
R006	1S024A	DATA FROM MEMORY-BIT 6	7
R007	1S024B	DATA FROM MEMORY-BIT 7	7
R008	1S023A	DATA FROM MEMORY-BIT 8	7
R009	1S023B	DATA FROM MEMORY-BIT 9	7
R010	1S022A	DATA FROM MEMORY-BIT 10	7
R011	1S022B	DATA FROM MEMORY-BIT 11	7
R012	1S021B	DATA FROM MEMORY-BIT 12	7
R041	1S021A	RESUME 1	6
R043	1S020A	PARITY ERROR	5
R063	1S020B	FUNCTION READY	5
R064	1S019A	I/O CHANNEL SELECT CODE-BIT 0	3
R067	1S018B	INITIATE BUFFER INPUT	6
R068	1S017A	INITIATE BUFFER OUTPUT	6
R069	1S017B	SET BUFFER BANK CONTROL	5
R070	1S016A	SET BER	5
R071	1S016B	SET BXR	5
R072	1S015A	BER TO A	5
R073	1S015B	INA2 (INVERTED)	6
R074	1S014A	CLEAR BUFFER CONTROL	3
R075	1S014B	MASTER CLEAR FROM COMPUTE(INVERTED)	3
R076	1S013A	MTM2	3
R077	1S006A	MASTER CLEAR FROM MEMORY (INVERTED)	3
R150	1S013B	DATA FROM COMPUTE-BIT 0	3
R151	1S012A	DATA FROM COMPUTE-BIT 1	3
R152	1S012B	DATA FROM COMPUTE-BIT 2	3
R153	1S011A	DATA FROM COMPUTE-BIT 3	3
R154	1S011B	DATA FROM COMPUTE-BIT 4	3
R155	1S010A	DATA FROM COMPUTE-BIT 5	3
R156	1S010B	DATA FROM COMPUTE-BIT 6	3
R157	1S009A	DATA FROM COMPUTE-BIT 7	3
R158	1S009B	DATA FROM COMPUTE-BIT 8	3
R159	1S008A	DATA FROM COMPUTE-BIT 9	3
R160	1S008B	DATA FROM COMPUTE-BIT 10	3
R161	1S007A	DATA FROM COMPUTE-BIT 11	3
R162	1S007B	DATA FROM COMPUTE-BIT 12	3
R700	1R027A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 0	7
R701	1R027B	DATA FROM EXT. EQUIPMENT-CH 2-BIT 1	7
R702	1R026A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 2	7
R703	1R026B	DATA FROM EXT. EQUIPMENT-CH 2-BIT 3	7
R704	1R025A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 4	7
R705	1R025B	DATA FROM EXT. EQUIPMENT-CH 2-BIT 5	7
R706	1R024A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 6	7

R707	1R024B	DATA FROM EXT. EQUIPMENT-CH 2-BIT 7	7
R708	1R023A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 8	7
R709	1R023B	DATA FROM EXT. EQUIPMENT-CH 2-BIT 9	7
R710	1R022A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 10	7
R711	1R022B	DATA FROM EXT. EQUIPMENT-CH 2-BIT 11	7
R712	1R021A	DATA FROM EXT. EQUIPMENT-CH 2-BIT 12	7
R713	1R021B	OUTPUT RESUME-CH 2	6
R714	1R020A	INPUT DISCONNECT-CH 2	5
R715	1R020B	INTERRUPT 1-CH 2	5
R716	1R019A	INTERRUPT 2-CH 2	5
R717	1R010A	INPUT READY-CH 2	6
R750	1R019B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 0	10
R751	1R018A	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 1	10
R752	1R018B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 2	10
R753	1R017A	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 3	10
R754	1R017B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 4	10
R755	1R016A	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 5	10
R756	1R016B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 6	10
R757	1R015A	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 7	10
R758	1R015B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 8	10
R759	1R014A	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 9	10
R760	1R014B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 10	10
R761	1R013A	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 11	10
R762	1R013B	DATA FROM EXT. EQUIPMENT-CH 3 -BIT 12	10
R763	1R012A	OUTPUT RESUME-CH 3	9
R764	1R012B	INPUT DISCONNECT-CH 3	5
R765	1R011A	INTERRUPT 1-CH 3	5
R766	1R011B	INTERRUPT 2-CH 3	5
R767	1R010B	INPUT READY-CH.3	9
T000	1T027A	DATA TO EXTERNAL MEMORY-BIT 0	4
T001	1T027B	DATA TO EXTERNAL MEMORY-BIT 1	4
T002	1T026A	DATA TO EXTERNAL MEMORY-BIT 2	4
T003	1T026B	DATA TO EXTERNAL MEMORY-BIT 3	4
T004	1T025A	DATA TO EXTERNAL MEMORY-BIT 4	4
T005	1T025B	DATA TO EXTERNAL MEMORY-BIT 5	4
T006	1T024A	DATA TO EXTERNAL MEMORY-BIT 6	4
T007	1T024B	DATA TO EXTERNAL MEMORY-BIT 7	4
T008	1T023A	DATA TO EXTERNAL MEMORY-BIT 8	4
T009	1T023B	DATA TO EXTERNAL MEMORY-BIT 9	4
T010	1T022A	DATA TO EXTERNAL MEMORY-BIT 10	4
T011	1T022B	DATA TO EXTERNAL MEMORY-BIT 11	4
T012	1T004A	DATA TO EXTERNAL MEMORY-BIT 12	4
T020	1T021A	ADDRESS TO EXTERNAL MEMORY-BIT 0	4
T021	1T021B	ADDRESS TO EXTERNAL MEMORY-BIT 1	4
T022	1T020A	ADDRESS TO EXTERNAL MEMORY-BIT 2	4
T023	1T020B	ADDRESS TO EXTERNAL MEMORY-BIT 3	4
T024	1T019A	ADDRESS TO EXTERNAL MEMORY-BIT 4	4
T025	1T019B	ADDRESS TO EXTERNAL MEMORY-BIT 5	4
T026	1T018A	ADDRESS TO EXTERNAL MEMORY-BIT 6	4
T027	1T018B	ADDRESS TO EXTERNAL MEMORY-BIT 7	4
T028	1T017A	ADDRESS TO EXTERNAL MEMORY-BIT 8	4
T029	1T017B	ADDRESS TO EXTERNAL MEMORY-BIT 9	4
T030	1T016A	ADDRESS TO EXTERNAL MEMORY-BIT 10	4
T031	1T016B	ADDRESS TO EXTERNAL MEMORY-BIT 11	4
T032	1T015A	ADDRESS TO EXTERNAL MEMORY-BIT 12	4
T033	1T015B	BANK SELECT TO EXTERNAL MEMORY-BIT 1	4
T034	1T014A	BANK SELECT TO EXTERNAL MEMORY-BIT 2	4
T035	1T014B	BANK SELECT TO EXTERNAL MEMORY-BIT 3	4
T037	1T013B	REQUEST MEMORY	6
T038	1T012A	REQUEST READ	6
T039	1T012B	REQUEST WRITE	6
T077	1T005B	I/O RESUME TO COMPUTE	5
T150	1T011A	DATA TO COMPUTE-BIT 0	4
T151	1T011B	DATA TO COMPUTE-BIT 1	4
T152	1T010A	DATA TO COMPUTE-BIT 2	4
T153	1T010B	DATA TO COMPUTE-BIT 3	4
T154	1T009A	DATA TO COMPUTE-BIT 4	4
T155	1T009B	DATA TO COMPUTE-BIT 5	4
T156	1T008A	DATA TO COMPUTE-BIT 6	4
T157	1T008B	DATA TO COMPUTE-BIT 7	4
T158	1T007A	DATA TO COMPUTE-BIT 8	4
T159	1T007B	DATA TO COMPUTE-BIT 9	4
T160	1T006A	DATA TO COMPUTE-BIT 10	4
T161	1T006B	DATA TO COMPUTE-BIT 11	4
T162	1T005A	DATA TO COMPUTE-BIT 12	4
T279	1S001B	CH.2 BUSY TO COMPUTE	3
T280	1S002A	CH.3 BUSY TO COMPUTE	3
T281	1S002B	CH.2 PARITY ERROR TO COMPUTE	5
T282	1S003A	CH.3 PARITY ERROR TO COMPUTE	5
T283	1S003B	CH.2 BUFFER TERMINATION INTERRUPT	5
T284	1S004A	CH.3 BUFFER TERMINATION INTERRUPT	5
T285	1S004B	CH.2 INTERRUPT 1 TO COMPUTE	5
T286	1S005A	CH.2 INTERRUPT 2 TO COMPUTE	5
T287	1S005B	CH.3 INTERRUPT 1 TO COMPUTE	5
T288	1S001A	CH.3 INTERRUPT 2 TO COMPUTE	5
T700	1Q027A	CH 2 DATA TO EXT. EQUIPMENT-BIT 0	7
T701	1Q027B	CH 2 DATA TO EXT. EQUIPMENT-BIT 1	7
T702	1Q026A	CH 2 DATA TO EXT. EQUIPMENT-BIT 2	7
T703	1Q026B	CH 2 DATA TO EXT. EQUIPMENT-BIT 3	7
T704	1Q025A	CH 2 DATA TO EXT. EQUIPMENT-BIT 4	7
T705	1Q025B	CH 2 DATA TO EXT. EQUIPMENT-BIT 5	7
T706	1Q024A	CH 2 DATA TO EXT. EQUIPMENT-BIT 6	7
T707	1Q024B	CH 2 DATA TO EXT. EQUIPMENT-BIT 7	7
T708	1Q023A	CH 2 DATA TO EXT. EQUIPMENT-BIT 8	7
T709	1Q023B	CH 2 DATA TO EXT. EQUIPMENT-BIT 9	7
T710	1Q022A	CH 2 DATA TO EXT. EQUIPMENT-BIT 10	7
T711	1Q022B	CH 2 DATA TO EXT. EQUIPMENT-BIT 11	7
T712	1Q021A	CH 2 DATA TO EXT. EQUIPMENT-BIT 12	7
T713	1Q021B	INPUT REQUEST-CH 2	6
T714	1Q020A	FUNCTION READY-CH 2	5
T715	1Q020B	MASTER CLEAR-CH 2	3
T716	1Q009A	INFORMATION READY-CH 2	6
T750	1Q019A	CH 3 DATA TO EXT. EQUIPMENT-BIT 0	10
T751	1Q019B	CH 3 DATA TO EXT. EQUIPMENT-BIT 1	10
T752	1Q018A	CH 3 DATA TO EXT. EQUIPMENT-BIT 2	10
T753	1Q018B	CH 3 DATA TO EXT. EQUIPMENT-BIT 3	10
T754	1Q017A	CH 3 DATA TO EXT. EQUIPMENT-BIT 4	10
T755	1Q017B	CH 3 DATA TO EXT. EQUIPMENT-BIT 5	10
T756	1Q016A	CH 3 DATA TO EXT. EQUIPMENT-BIT 6	10
T757	1Q016B	CH 3 DATA TO EXT. EQUIPMENT-BIT 7	10
T758	1Q015A	CH 3 DATA TO EXT. EQUIPMENT-BIT 8	10
T759	1Q015B	CH 3 DATA TO EXT. EQUIPMENT-BIT 9	10
T760	1Q014A	CH 3 DATA TO EXT. EQUIPMENT-BIT 10	10
T761	1Q014B	CH 3 DATA TO EXT. EQUIPMENT-BIT 11	10
T762	1Q013A	CH 3 DATA TO EXT. EQUIPMENT-BIT 12	10
T763	1Q013B	INPUT REQUEST-CH 3	9
T764	1Q012A	FUNCTION READY-CH 3	5
T765	1Q012B	MASTER CLEAR-CH 3	3
T766	1Q009B	INFORMATION READY-CH 3	9

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB 19128	2/8/68	R. Taylor
B		REVISED SEE ECO CB 19175	2-21-68	R. Taylor

NOTES:

1. INTERPRET TO ENGINEERING STANDARD 3.01.002 "PREPARATION OF LOGIC DIAGRAMS."

2. CONNECTOR NUMBERS SHOWN ARE INTERPRETED IN THE FOLLOWING MANNER:

A. J-01 (CONNECTOR NO.) C03 (PIN NO.)

B. J-03 (CONNECTOR NO.) N (PIN NO.)

THE DASH IN THE CONNECTOR NUMBER INDICATES CHASSIS CONFIGURATION 1, 2, OR 3, DEPENDENT UPON SYSTEM APPLICATION. THE CONNECTOR NUMBER REPRESENTS EITHER THE SIGNAL INPUT OR TERMINATOR DEPENDENT UPON USE OF THE EQUIPMENT. IF THE CONNECTOR NUMBER SHOWN IS THE SIGNAL INPUT, THEN THE NEXT SEQUENTIAL CONNECTOR NUMBER IS THE TERMINATOR, OR J-02 C03, AS IN EXAMPLE A. THE 3RD DIGIT IN THE PIN DESIGNATION INDICATES AN ODD PIN NUMBER. ONE WIRE IN A TWISTED PAIR GOES TO THIS PIN. THE OTHER WIRE OF THE TWISTED PAIR GOES TO THE NEXT SEQUENTIAL PIN NUMBER, OR J-01 C04 AS IN EXAMPLE A. A PIN DESIGNATION REPRESENTING ONE WIRE IS INDICATED BY A LETTER, AS IN EXAMPLE B.

3. THE FOLLOWING IS A LIST OF THE SUBTITLES AND THE SHEET NO'S OF EACH:

4. LOGIC DIAGRAMS CORRESPOND TO REVISION B OF DOCUMENT NUMBER 16901500 (I/O UNIT MECHANIZED DESIGN DATA)

B	–	B	A	–	A	–	–	A	–	–
A	–	–	A	–	A	–	–	A	–	–
1	2	3	4	5	6	7	8	9	10	11
SHEET										
REVISION STATUS OF SHEETS										

16901100 SHEET 1 OF 11

AC A 7491

NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES ON
FRACTIONS: ± —— DECIMALS: ± —— ANGLES: ± ——
DO NOT SCALE DRAWING
MATERIAL

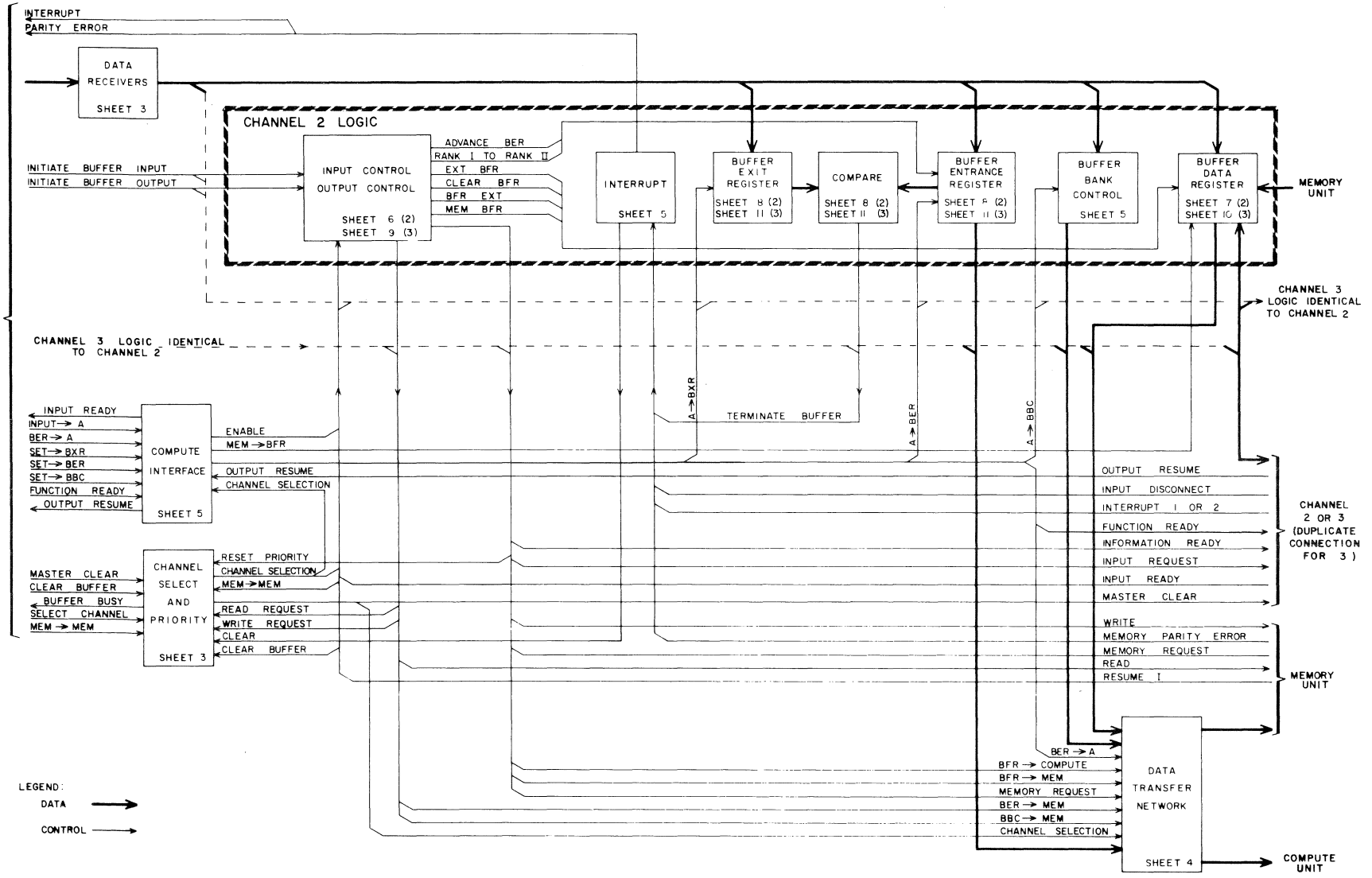
CONTROL DATA CORPORATION
GOVERNMENT SYSTEMS DIVISION
MINNEAPOLIS • MINNESOTA

CONTRACT		
APPROVED	[illegible]	5 4 67
ENGINEER	[illegible]	5-4-67
CHECKED	[illegible]	4-24-67
DRAWN	D. L. OLSON	2-22-67
APPROVED		
APPROVED		

TITLE
I/O UNIT
LOGIC DIAGRAM

SIZE	CODE IDENT. NO.	DRAWING NO.
C	27963	16901100
SCALE ——		SHEET 1 OF 11

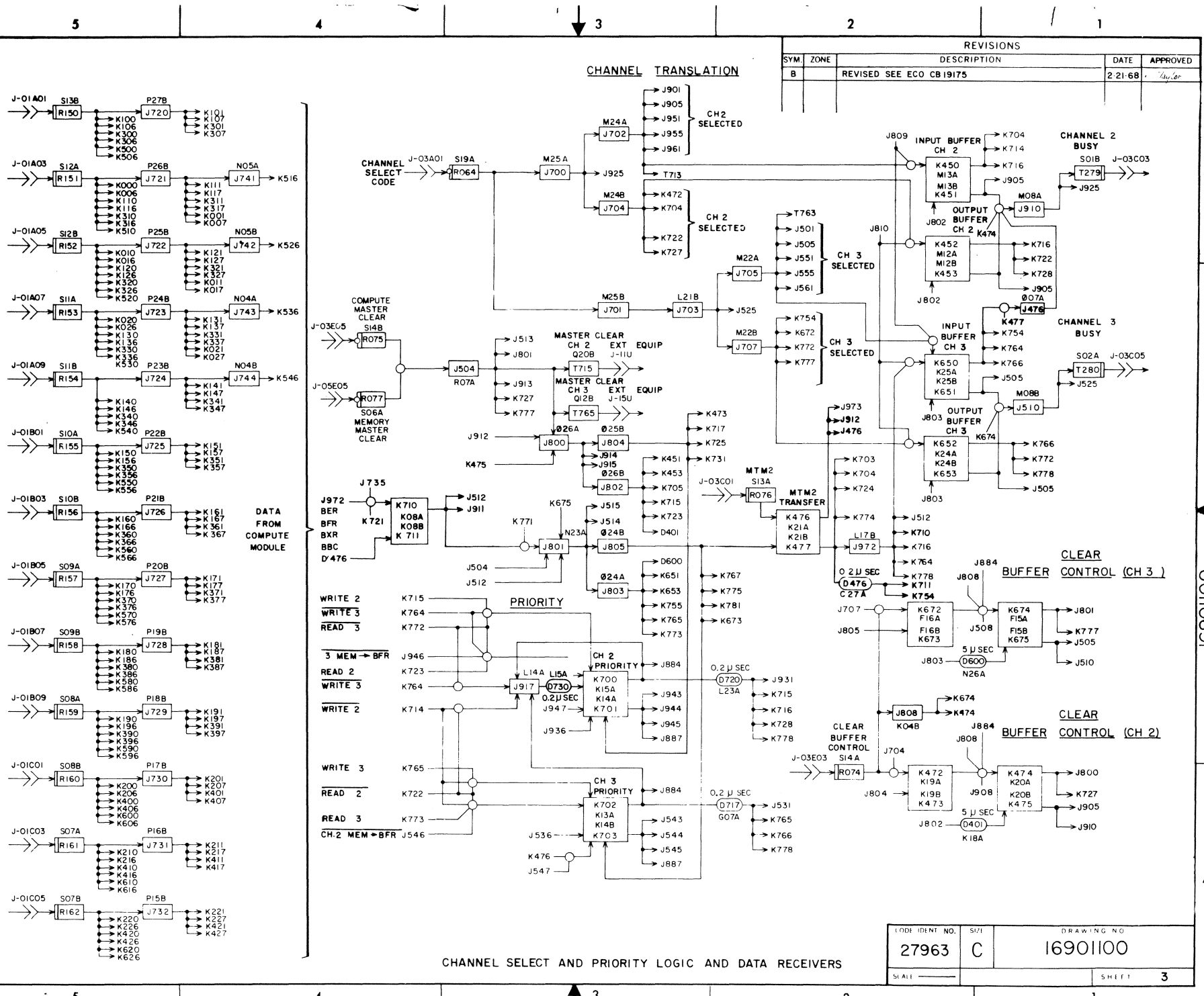
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



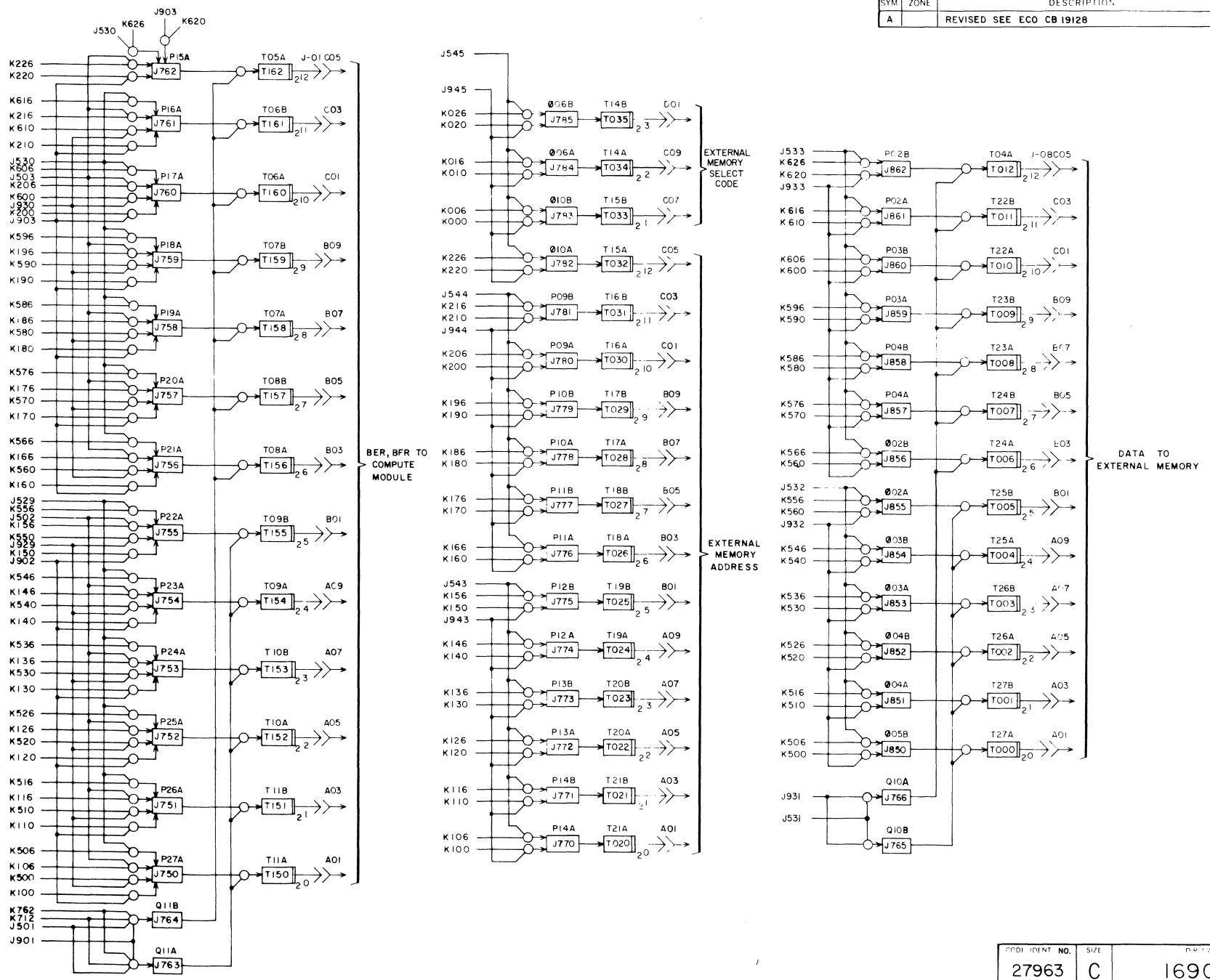
I/O UNIT BLOCK DIAGRAM

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16901100
SCALE		SHEET 2

16901100 SHEET 2


REVISIONS
SYM. | ZONE | DESCRIPTION | DATE | APPROVED
B | | REVISED SEE ECO CB19175 | 2-21-68
CHANNEL TRANSLATION
DATA FROM COMPUTE MODULE
CHANNEL SELECT CODE
CH2 SELECTED
CH 3 SELECTED
INPUT BUFFER CH 2
INPUT BUFFER CH 3
OUTPUT BUFFER CH 2
OUTPUT BUFFER CH 3
CHANNEL 2 BUSY
CHANNEL 3 BUSY
COMPUTE MASTER CLEAR
MEMORY MASTER CLEAR
MASTER CLEAR CH 2 EXT EQUIP
MASTER CLEAR CH 3 EXT EQUIP
MTM2 TRANSFER
PRIORITY
CH 2 PRIORITY
CH 3 PRIORITY
CLEAR BUFFER CONTROL (CH 3)
CLEAR BUFFER CONTROL (CH 2)
CLEAR BUFFER CONTROL
CHANNEL SELECT AND PRIORITY LOGIC AND DATA RECEIVERS
CODE IDENT NO. 27963
SIZE C
DRAWING NO 16901100
SCALE
SHEET 3
16901100 SHEET 3 OF 11

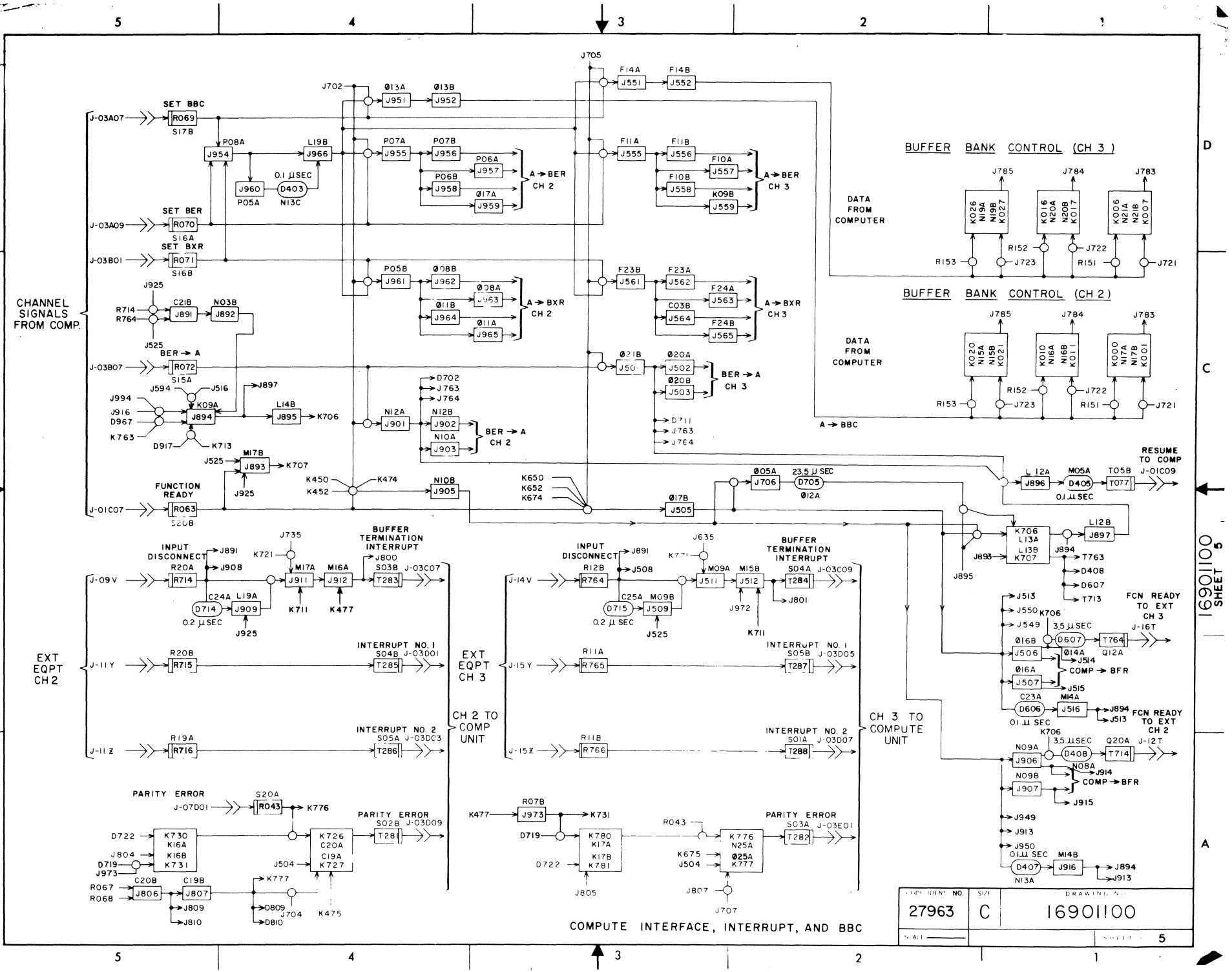
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB 19128	2/8/68	C. Taylor



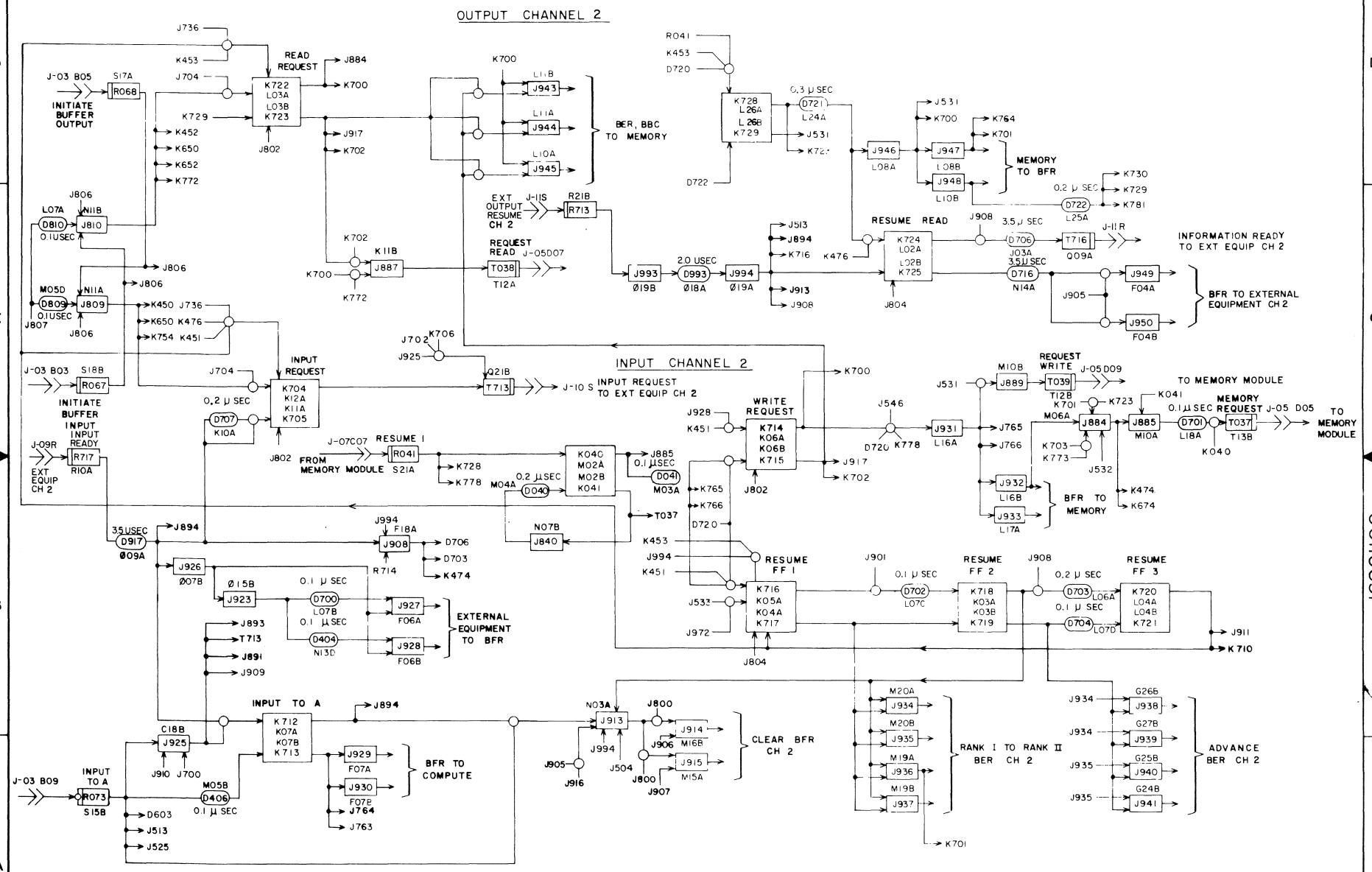
DATA TRANSFER NETWORK

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16901100
SCALE		SHEET 4

16901100 SHEET 4


CHANNEL SIGNALS FROM COMP.
SET BBC
SET BER
SET BXR
BER → A
FUNCTION READY
BUFFER BANK CONTROL (CH 3)
BUFFER BANK CONTROL (CH 2)
DATA FROM COMPUTER
A → BBC
A → BER CH 2
A → BER CH 3
A → BXR CH 2
A → BXR CH 3
BER → A CH 2
BER → A CH 3
INPUT DISCONNECT
BUFFER TERMINATION INTERRUPT
INTERRUPT NO. 1
INTERRUPT NO. 2
EXT EQPT CH 2
EXT EQPT CH 3
CH 2 TO COMP UNIT
CH 3 TO COMPUTE UNIT
PARITY ERROR
RESUME TO COMP
FCN READY TO EXT CH 3
FCN READY TO EXT CH 2
COMP → BFR
0.1 μSEC
0.2 μSEC
23.5 μSEC
3.5 μSEC
01 μ SEC
COMPUTE INTERFACE, INTERRUPT, AND BBC
DOCUMENT NO. 27963
SIZE C
DRAWING NO. 16901100
SHEET 5

REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED
A		REVISED SEE ECO CB 19128	2/8/68	K. Taylor

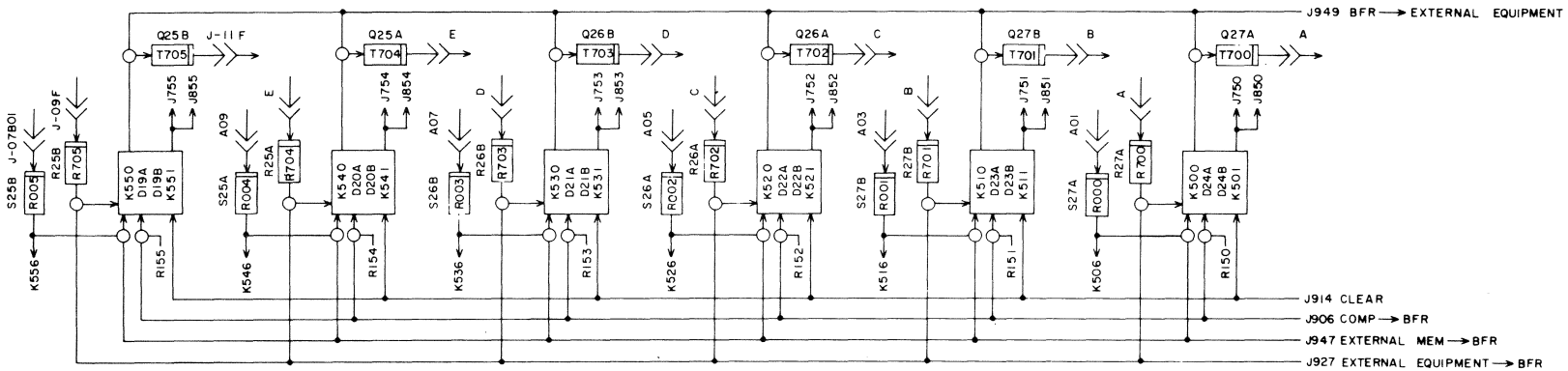


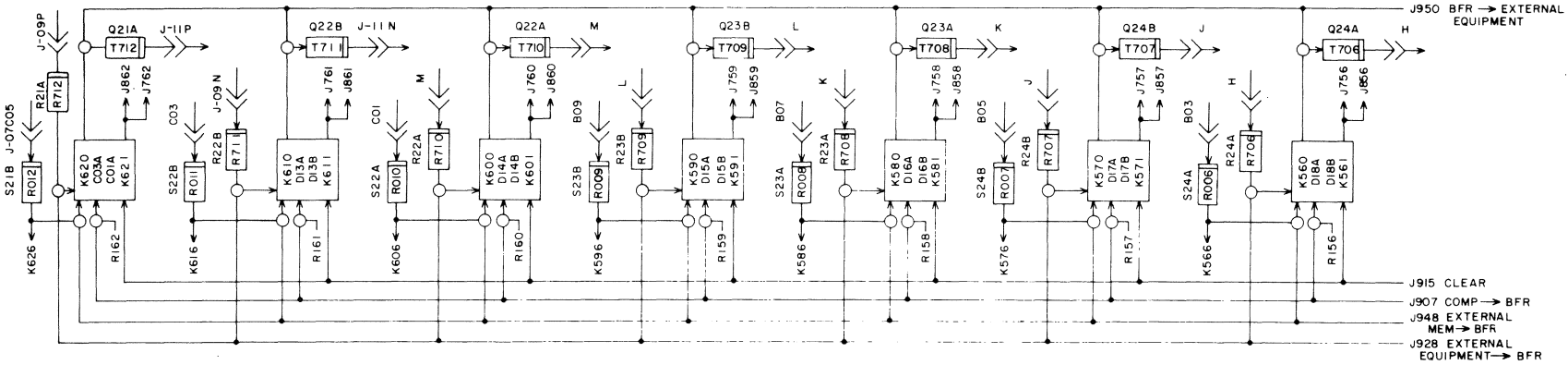
CH 2 I/O CONTROL

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16901100
SCALE		SHEET 6

16901100 SHEET 6

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

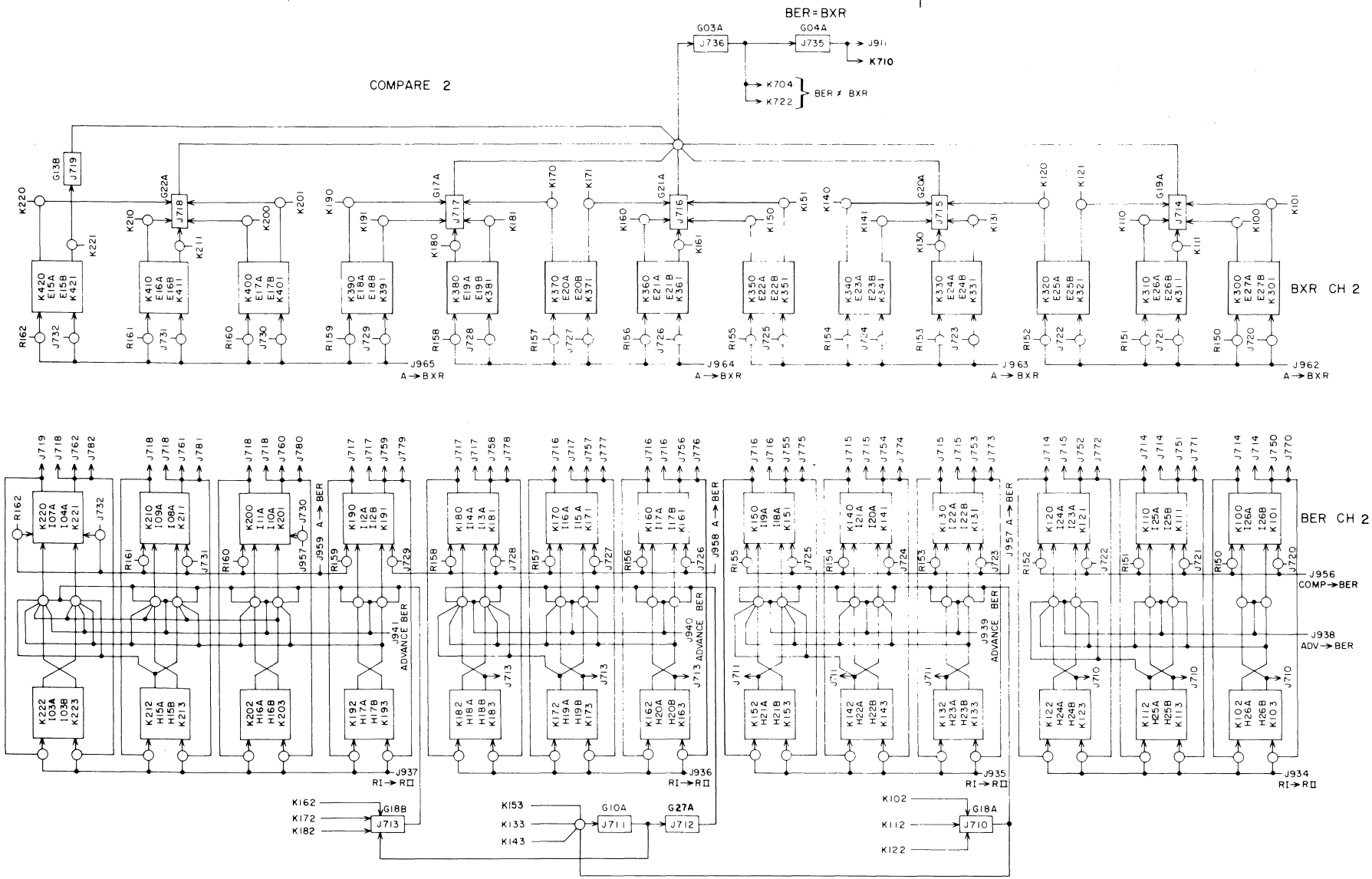




CHANNEL 2 BFR REGISTER

CODE IDENT NO.		
27963	C	16901100
		7

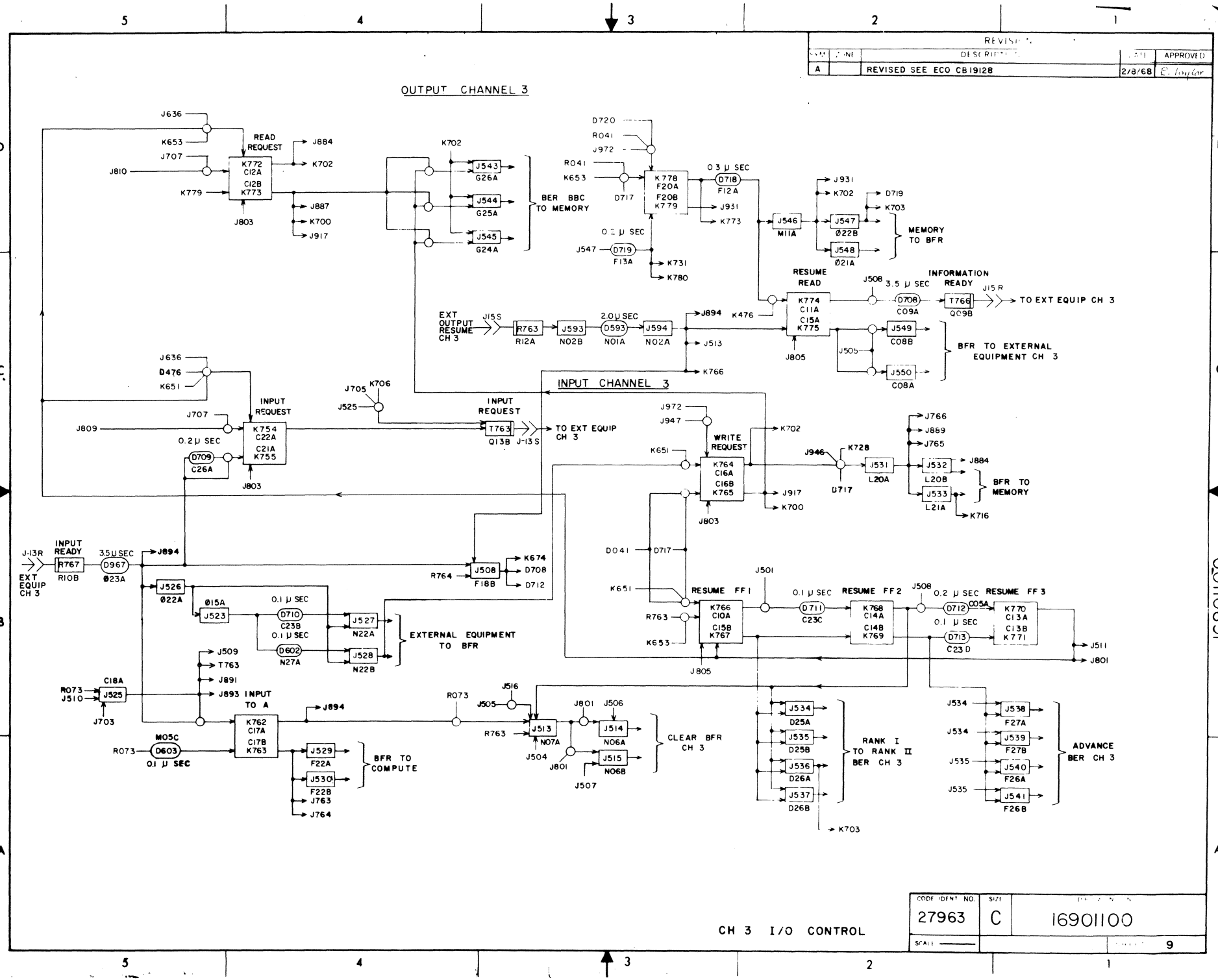
16901100 SHEET 7



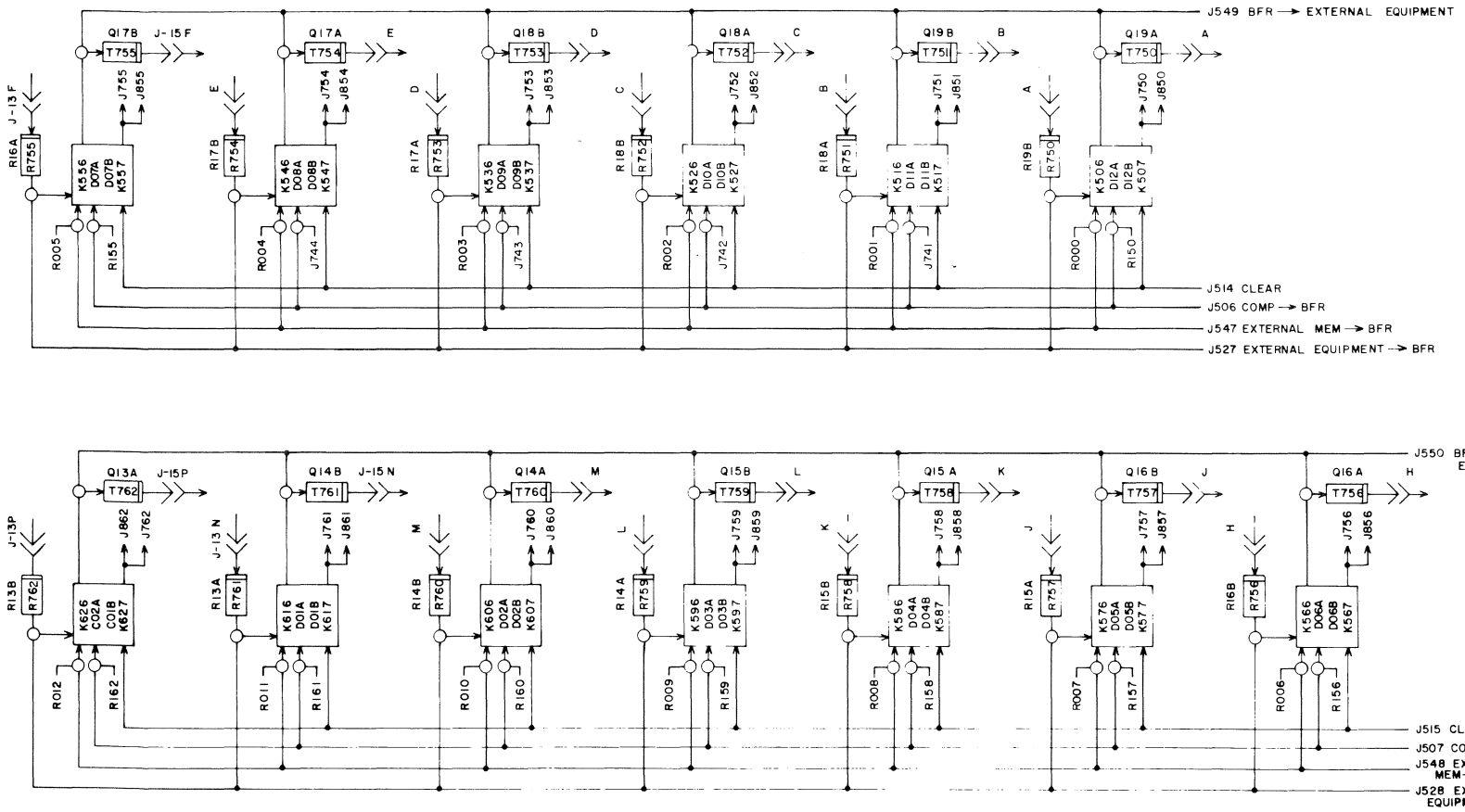
CHANNEL 2 BER, BXR, AND COMPARE

CODE IDENT NO.	SIZE	DRAWING NO.
27963	C	16901100
SCALE		SHEET 8

16901100 SHEET 8


REVISIONS
SYM | ZONE | DESCRIPTION | DATE | APPROVED
A | | REVISED SEE ECO CB19128 | 2/8/68 | E. Taylor
OUTPUT CHANNEL 3
READ REQUEST
K772 C12A C12B K773
J803
BER BBC TO MEMORY
0.3 μ SEC
0.2 μ SEC
MEMORY TO BFR
RESUME READ
INFORMATION READY
3.5 μ SEC
TO EXT EQUIP CH 3
EXT OUTPUT RESUME CH 3
2.0 μ SEC
BFR TO EXTERNAL EQUIPMENT CH 3
INPUT CHANNEL 3
INPUT REQUEST
TO EXT EQUIP CH 3
WRITE REQUEST
BFR TO MEMORY
EXT EQUIP CH 3
INPUT READY
3.5 μ SEC
EXTERNAL EQUIPMENT TO BFR
0.1 μ SEC
INPUT TO A
BFR TO COMPUTE
CLEAR BFR CH 3
RESUME FF1
RESUME FF2
RESUME FF3
RANK I TO RANK II BER CH 3
ADVANCE BER CH 3
CH 3 I/O CONTROL
CODE IDENT NO. 27963
SIZE C
DRAWING NO. 16901100
SCALE
SHEET 9
16901100 SHEET 9

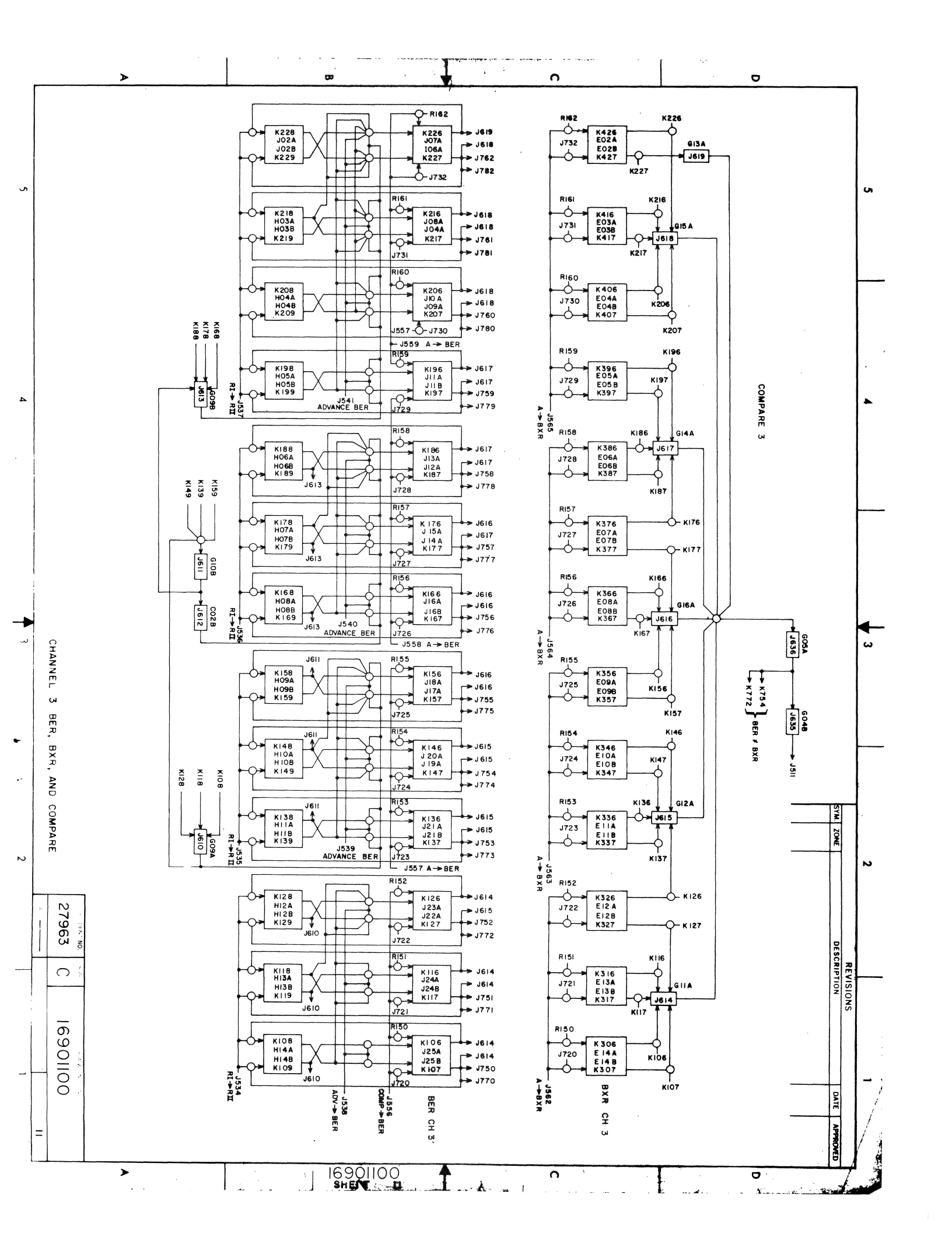
REVISIONS				
SYM	ZONE	DESCRIPTION	DATE	APPROVED



CHANNEL 3 BFR REGISTER

CODE IDENT NO.	SIZE	DRAWING NO
27963	C	16901100
SCALE		SHEET 10

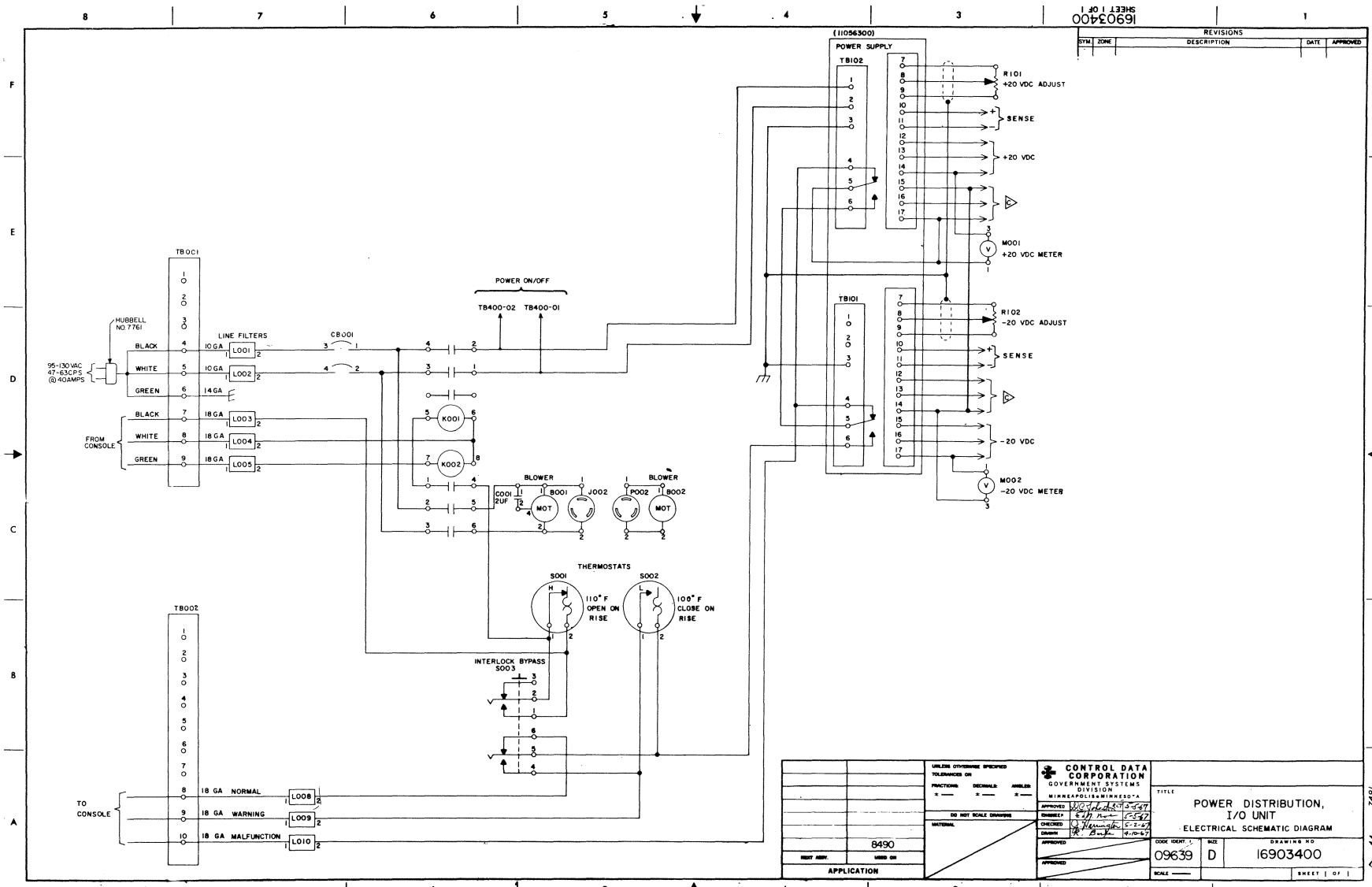
16901100 SHEET 10


CHANNEL 3 BER, BXR, AND COMPARE
COMPARE 3
BXR CH 3
BER CH 3
J537 R1 → R II
J536 R1 → R II
J535 R1 → R II
J534 R1 → R II
J538 ADV → BER
J556 COMP → BER
J559 A → BER
J558 A → BER
J557 A → BER
J541 ADVANCE BER
J540 ADVANCE BER
J539 ADVANCE BER
J565 A → BXR
J564 A → BXR
J563 A → BXR
J562 A → BXR
K754 K772 BER ≠ BXR
J511
G13A J619
G15A J618
G14A J617
G16A J616
G12A J615
G11A J614
G10B J611
G09B J613
G09A J610
G08A J636
G04B J635
C02B J612
REVISIONS
SYM.
ZONE
DESCRIPTION
DATE
APPROVED
27963
C
16901100
16901100
SHEET

SECTION 3

I/O UNIT

POWER DISTRIBUTION AND MCS PROTECTION DRAWINGS


16903400 SHEET 1 OF 1
REVISIONS
SYM. ZONE DESCRIPTION DATE APPROVED
(11056300)
POWER SUPPLY
TB102
TB101
R101
+20 VDC ADJUST
SENSE
+20 VDC
M001
+20 VDC METER
R102
-20 VDC ADJUST
-20 VDC
M002
-20 VDC METER
TB001
TB002
POWER ON/OFF
TB400-02 TB400-01
HUBBELL NO. 7761
95-130 VAC 47-63 CPS @ 40 AMPS
LINE FILTERS
CB001
BLACK
WHITE
GREEN
10 GA
14 GA
18 GA
L001
L002
L003
L004
L005
FROM CONSOLE
K001
K002
BLOWER
C001 2UF
B001
J002
P002
B002
MOT
THERMOSTATS
S001
110° F OPEN ON RISE
S002
100° F CLOSE ON RISE
INTERLOCK BYPASS S003
TO CONSOLE
18 GA NORMAL
18 GA WARNING
18 GA MALFUNCTION
L008
L009
L010
UNLESS OTHERWISE SPECIFIED TOLERANCES ON
FRACTIONS DECIMALS ANGLES
DO NOT SCALE DRAWING
MATERIAL
NEXT ASSY.
USED ON
8490
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CONTROL DATA CORPORATION
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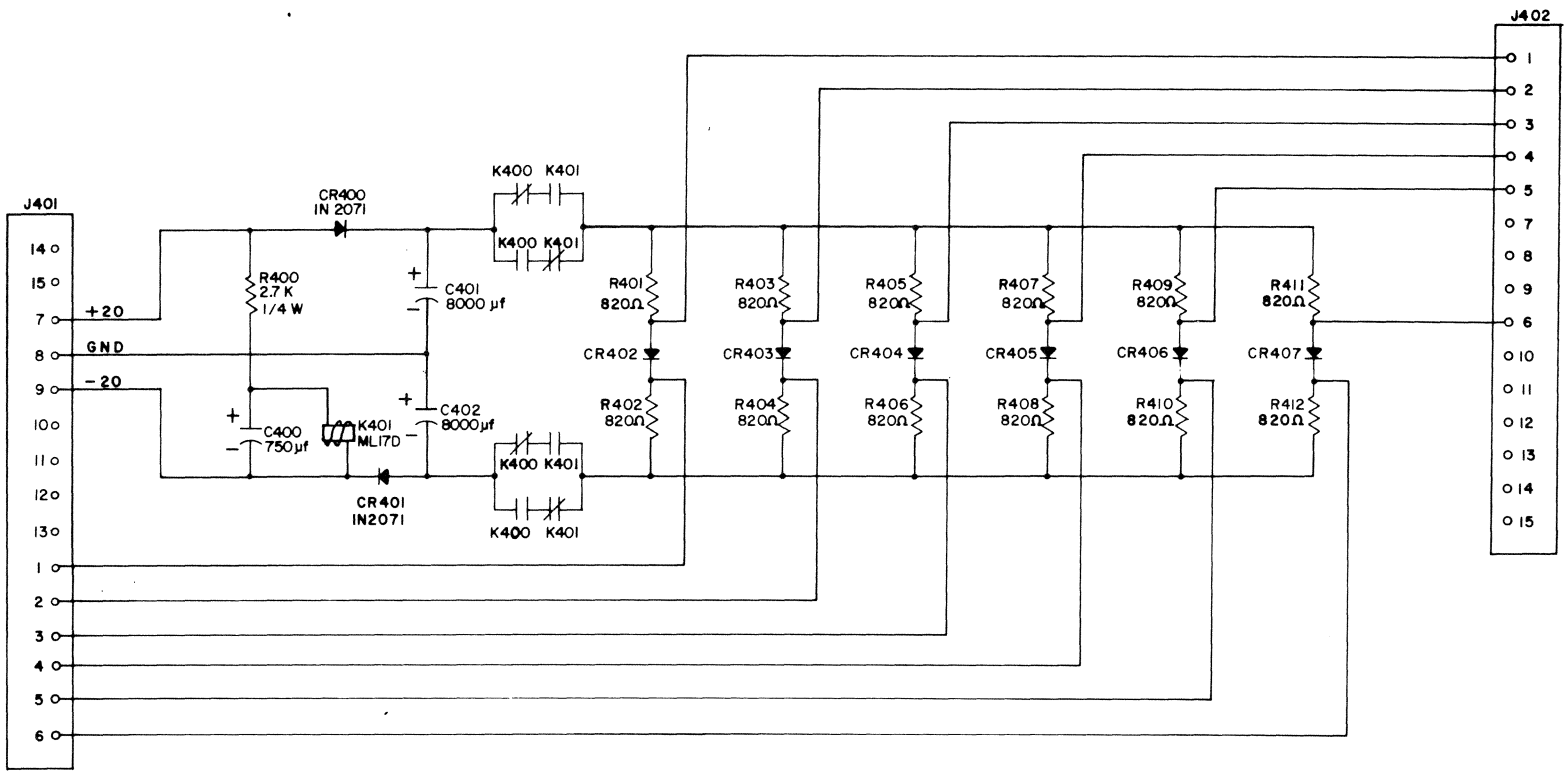
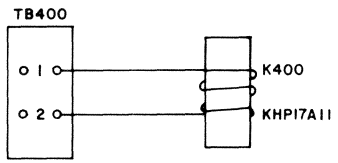
APPROVED
ENGINEER
CHECKED
DRAWN
APPROVED
APPROVED
TITLE
POWER DISTRIBUTION, I/O UNIT
ELECTRICAL SCHEMATIC DIAGRAM
CODE IDENT. NO. 09639
SIZE D
DRAWING NO 16903400
SCALE
SHEET 1 OF 1
7491 A A 0

REVISIONS				
SYM.	ZONE	DESCRIPTION	DATE	APPROVED

NOTES:
1. ALL DIODES ARE 1N2071 UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ARE 1/2 WATT ±5% UNLESS OTHERWISE SPECIFIED.





	8490
NEXT ASSY.	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED TOLERANCES ON
FRACTIONS: ± — DECIMALS: ± — ANGLES: ± —
DO NOT SCALE DRAWING
MATERIAL

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CONTRACT		
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ENGINEER	E. H. Hoe	5-5-67
CHECKED	J. Harrington	5-2-67
DRAWN	DR Bode	4-10-67
APPROVED		
APPROVED		

TITLE
POWER ON/OFF, MCS PROTECTION, I/O UNIT
ELECTRICAL SCHEMATIC DIAGRAM

CODE IDENT NO	SIZE	DRAWING NO
09639	C	16902900
SCALE NONE		SHEET 1 OF 1

16902900

AA 7491 A

CUT ALONG LINE

COMMENT SHEET

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