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CALCOMP CD14, CD14A, 1015, AND 1015A CONTROLLERS TRAINING MANUAL

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INTRODUCTION

This manual contains theory of operation information for the CD14, CD14A, 1015, and 1015A Controllers. This manual is intended to be used as a training vehicle and, subsequently, as reference data for Product Support personnel. It is presumed that the user of this manual is familiar with the contents of the Controller Maintenance Manuals as references to them are made throughout this manual. The Controller Maintenance Manuals contain the logic diagrams upon which the understanding of the theory of operation is dependent. The logic diagram references are alphanumerical characters which identify the function and the diagram within the function. For example: CI-6 identifies the sixth diagram within the channel interface (CI) function.

PURPOSE OF CONTROLLER

The controller, under the command of an IBM System 360 (Model 30 and up), controls the operation of up to eight online disk drives to provide large capacity, high speed, direct access storage. Direct access storage enables retrieval of random data records without searching a complete file of records. The controller can control eight online disk drives while performing inline diagnostics on a ninth disk drive.

The controller contains the logic and circuitry necessary to communicate with the central processing unit (CPU) channel, to accept and interpret commands from the channel, to execute these commands through direct communication with the disk drive, to control the flow of data during command execution, and to present status information to the channel at the completion of an operation.

BASIC OPERATIONS (Figure 1-1)

The CPU initiates an operation with a start I/O (SIO) instruction. The SIO instruction specifies the controller and disk drive to be used in the I/O operation and fetches a channel address word (CAW). The CAW specifies the location of the first channel command word (CCW) within the main memory. The controller decodes the command code and stores it in one register in the register function.

Seek Operation

When the command code defines a seek operation, the following actions occur: The controller selects the disk drive to be used for the operation before the seek command is issued. The selected disk drive indicates to the controller the present location (old address) of the access mechanism. The controller uses the old address and a six-byte seek address, which is received from the channel, to determine the direction and the number of cylinders the access mechanism must move. This information is sent to the disk drive and loaded into the difference counter. The control circuits in the disk drive cause the access mechanism to position the read/write heads at the desired cylinder. The disk drive then indicates to the controller that the seek operation has been completed. In turn, the controller indicates to the channel that the seek operation has been completed.

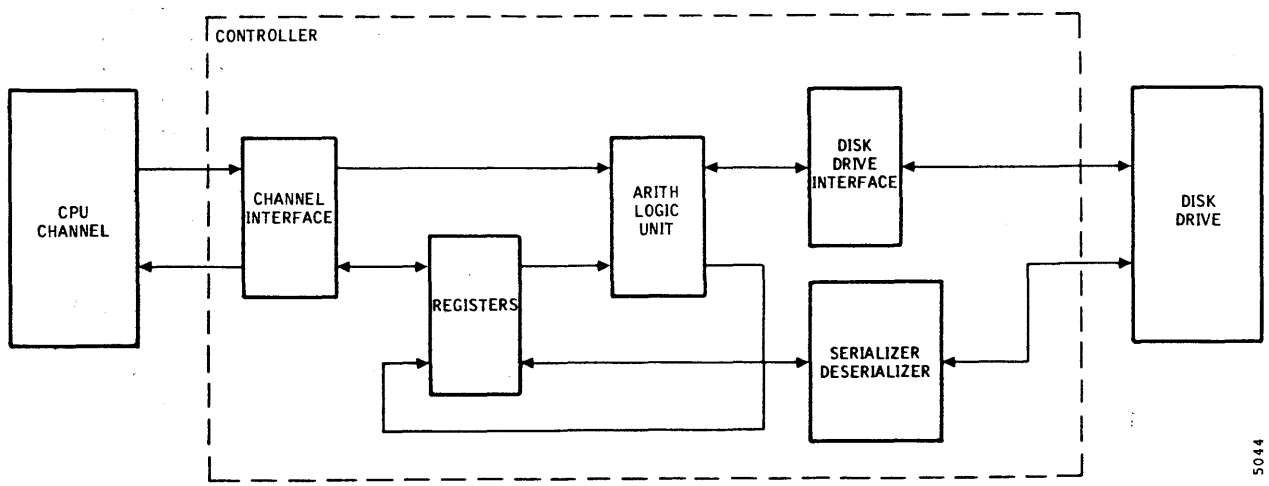


Figure 1-1. Basic Flow Diagram

Write Operation

When the command code defines a write operation, the following actions occur: Record length counters (registers in the register function) are loaded with record length information, received from the channel or derived from previous operations, for various areas of the record. The data to be written is received from the channel by the channel interface function and is routed through the arithmetic logic unit to a register in the register function. From this register, the data is sent to the serializer/deserializer function where it is serialized so that it can be routed, bit by bit, to the read/write heads in the disk drive for writing on the disk pack. As the data is being written on the disk, code check bytes are generated and are written following the data on the disk. Following the code check bytes, the address of the controller and the address of the disk drive are written and are followed by a bit count that represents the total data bits (modulo 256) in the record. The code check bytes and the bit count byte provide a parity check of the data when the data is read from the disk. Upon completion of the write operation, the controller indicates to the channel the completion of the write operation.

Read Operation

When the command code defines a read operation, the following actions occur: Record length counters (registers in the register function) are loaded with record length information, received from the channel or derived from previous operations, for various areas of the record. The selected read/write heads, properly positioned, read the data, bit by bit, from the disk. The data is routed to the serializer/deserializer function, bit by bit, where it is deserialized and accumulated in eight-bit bytes. The bytes are routed to a register in the register function. From this register, the bytes are routed through the arithmetic logic unit where parity is generated. Parity is generated on read data because it is not written on the disk, but it is required by the channel. Each byte with its associated parity bit is temporarily stored in a register in the register function. At the proper time, the byte is transferred to the channel through the channel interface function. The code check bytes, the controller and disk drive address byte, and the bit count byte are read and checked. If an error is detected, it is indicated by the controller to the channel. Upon completion of the read operation, the controller indicates to the channel the completion of the read operation.

FUNCTIONAL AREAS

The controller is functionally divided into ten areas (see block diagrams in the Maintenance Manuals):

- Channel Interface (CI)
- Register (REG)
- Timing (TIM)
- Machine Status (STAT)
- Arithmetic Logic Unit (ALU)
- Read-Only Memory (ROM)
- Serializer/Deserializer (SERDES)
- Disk Drive Interface (DDI)
- Test Select and Display (TEST)
- Power (PWR)

The channel interface function is a signal matching device which allows the controller to be attached to the CPU.

The register function contains general-purpose registers and some special-purpose registers. The microprogram of the read-only memory uses these registers to manipulate data.

The timing function provides the basic timing used in the controller and, additionally, provides various equipment resets.

The machine status function stores conditions that occur during an operation.

The arithmetic logic unit performs the functions of adding, subtracting, ORing, ANDing, and exclusive-ORing; it also generates parity.

The read-only memory contains 2,048, 48-bit words which are called microinstructions. A microprogram is a group of words that perform related functions.

The serializer/deserializer function converts parallel data to serial data when writing (sending data to a disk drive) and converts serial data to parallel data when reading (receiving data from a disk drive).

The disk drive interface function contains the data and control lines that send and receive information from the disk drive.

The test select and display function allows inline or offline testing of a disk drive and displays register contents and errors.

The power function supplies the voltages required for operating the controller and sequencing signals for applying power to the disk drives.

CHANNEL INTERFACE (Figure 1-2)

The channel interface function connects the controller to an I/O channel of the computer. The 35 lines that

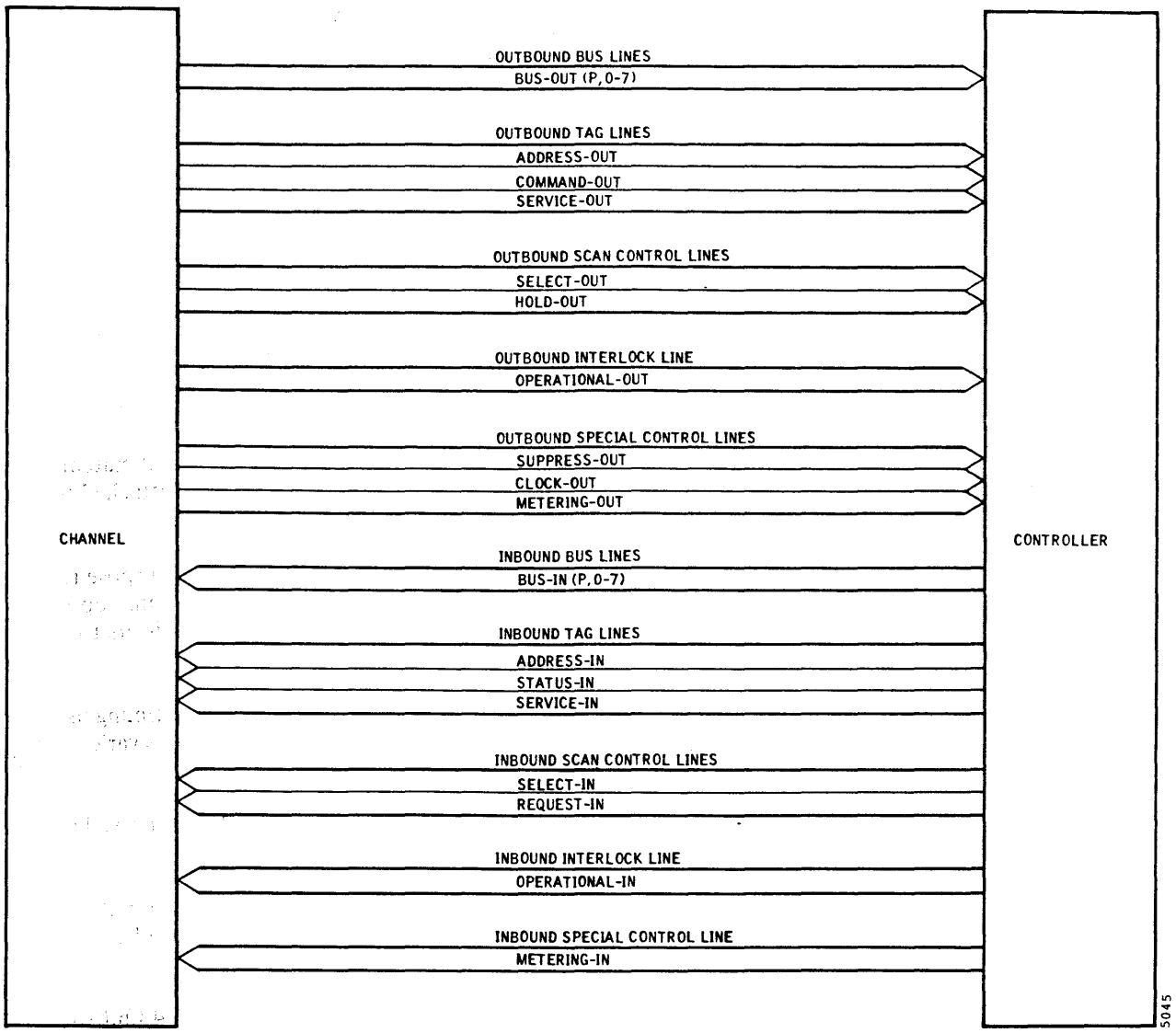


Figure 1-2. Channel Interface Lines

compose the interconnections between the controller and the channels can be separated into the following five general groups:

- Bus lines
- Tag lines
- Scan control
- Special control
- Interlock lines

Bus Lines

The bus lines consist of nine bus-in (8 bits plus parity) lines and nine bus-out (8 bits plus parity) lines that transfer data between the channel and the controller.

The type of data transferred from the channel to the controller on the bus-out lines is indicated by an associated outbound tag line. For example: if the address-out tag line is activated, the data on the bus-out lines is an address.

The type of data transferred from the controller to the channel on the bus-in lines is indicated by an associated inbound tag line. For example: if the address-in tag line is activated, the data on the bus-in lines is an address.

Tag Lines

The tag lines consist of three outbound tag lines (address-out, command-out, and service-out) and three inbound tag lines (address-in, status-in, and service-in) that identify the contents of the data on the bus-out and bus-in lines, respectively.

The address-out tag identifies the data on the bus-out lines as an address; however, for a halt I/O instruction, the address-out tag causes the controller to disconnect from the channel. The address-out tag is activated when the acquisition of a controller is desired. All controllers attached to a channel try to decode the unique address on the bus-out lines, but only one will actually decode the address. This controller, if it is not busy, will activate the operational-in interlock line when select-out is propagated to that controller.

The channel keeps the address-out tag activated until it receives operational-in, status-in, or select-in signals. When status-in is sent to the channel, it indicates that the controller is busy and cannot interrupt an operation in process. The channel, upon receiving status-in, deactivates select-out, waits for the controller to deactivate status-in, then deactivates address-out. When the channel receives select-in, it indicates that no controller has decoded the address. For a halt I/O instruction, the channel activates the select-out line, ensures that the selected controller has operational-in activated, activates the address-out tag, then deactivates select-out, and keeps the address-out tag activated until the controller deactivates the operational-in line.

The command-out tag identifies the information on the bus-out lines as a channel command (read or write). The command-out tag is activated by the channel during initial selection in reply to an address-in tag from the controller. The command on the bus-out lines identifies the operation to be performed. When the channel responds to a service-in tag with a command-out tag, the controller stops the data transfer. When the channel replies to a status-in tag with a command-out tag, the controller holds (stacks) the status data. The controller can transfer the held status data if the suppress-out control and the address-out tag are not active when the select-out scan control is activated. When the channel replies to a controller-initiated selection (address-in tag activated) with a command-out tag, the controller sends status information to the channel.

The service-out tag indicates to the controller that the channel acknowledges receipt of data on the bus-in lines or is sending data requested by the controller (service-in activated) on the bus-out lines. When the service-out tag is activated in response to a service-in tag during a write, search, or control operation, it indicates that the channel has sent the requested data on the bus-out lines. When service-out is activated in response to a service-in tag during a read or sense operation or in response to a status-in tag, it indicates to the controller that the channel acknowledges receipt of the data on the bus-in lines. The service-out tag remains activated until the service-in or status-in tag is deactivated. The service-out tag cannot be active while any other outbound tag is active.

The address-in tag notifies the channel that the information on the bus-in lines is the address of the selected controller. When the channel receives the address-in tag, it replies with a command-out tag. The address-in tag remains active until the command-out tag is activated. When address-in is activated, the command-out tag is deactivated.

The status-in tag notifies the channel that the information on the bus-in lines is status. The status-in tag remains active until the channel replies with a service-out tag to indicate receipt of the status or with a command-out tag to indicate that the status has been superseded.

The service-in tag either notifies the channel that data is on the bus-in lines during a read or sense operation or is used to request the channel to send data on the bus-out lines during a write, search, or control operation. The channel responds to a service-in tag with a service-out tag when data is received or transmitted or with a command-out tag to stop data from being transferred and end the operation.

Scan Control

The scan control lines consist of select-out, hold-out, select-in, and request-in lines. These lines are used by the channel to initiate communication with an attached controller. The controller uses the scan control lines to request service from the channel.

The select-out scan line is a series interrogation link to all controllers attached to a channel. Interrogation of controllers is in a priority sequence. The priority scheme is determined at the time of installation. Figure 1-3 shows how the priority scheme might be set up. The select-out scan line is connected serially through the controller having the highest priority, then to the next-to-the-highest priority controller, and so forth in a descending order of priority. When a controller receives a select-out signal, it either activates the operational-in line or passes the select-out signal to the next controller. When a controller passes the select-out signal, it cannot actuate its operational-in line until it receives another select-out signal. The channel holds the select-out signal active until it receives a response on either the select-in line or on the address-in tag. If each controller passes the select-out signal, it is returned to the channel on the select-in line (Figure 1-3). When a controller activates its operational-in line in response to a select-out signal, the select-out signal is neither passed to the next controller nor is it routed back to the channel on the select-in line. When the select-out/select-in loop is interrupted, the controller activates the operational-in line, then transmits an address on the bus-in lines, and activates the address-in tag. The controller keeps the operational-in line active until the operation has been completed. The channel deactivates the select-out line either after it receives the address-in tag or after the operation is complete. The controller can only deactivate the operational-in line after the channel deactivates the select-out line.

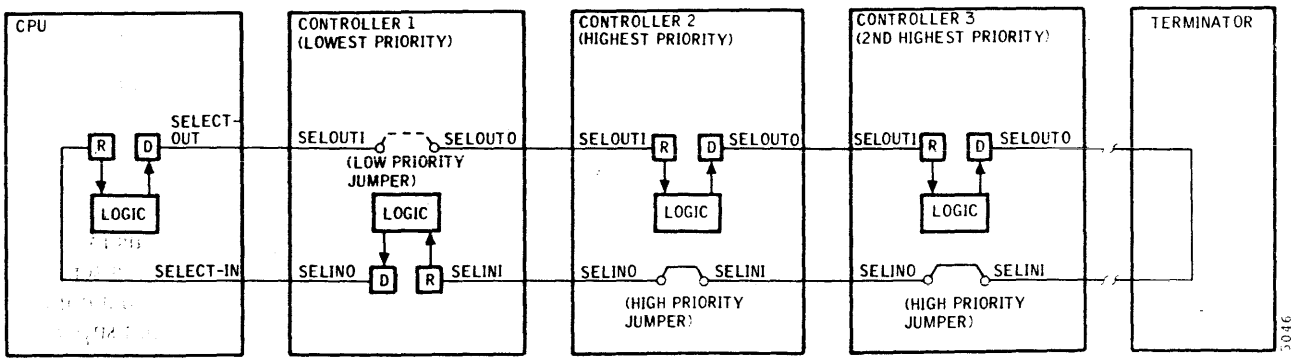


Figure 1-3. Selection Priority Connections

The select-in line is a return line to the channel for the select-out lines. As shown in Figure 1-3, the controller selection logic can be connected in either the select-out line or the select-in line, depending on its order or priority. When a select-out signal is passed to a controller that has its selection logic connected in the select-in line, the controller reacts as though the selection logic were connected in the select-out line. The controller having the lowest priority is electrically connected to the select-in line of the channel.

The hold-out scan control is used in conjunction with the select-out scan control. The hold-out line is active at all controllers simultaneously to allow the select-out signal to be relayed from controller to controller.

The request-in scan control line is activated by a controller to request service from the channel. A controller activates the request-in line to indicate to the channel that the controller will initiate a signal sequence when the next select-out signal is relayed to it. When more than one controller activates request-in, the controller with the higher priority will be serviced first.

Special Controls

The special control lines consist of clock-out, suppress-out, metering-out, and metering-in lines. The clock-out, metering-out, and metering-in controls are used by the controller to control the operation of the usage meter. The suppress-out control is used to inhibit the transfer of data or status information and to facilitate chained command operations.

The clock-out control line, when activated, indicates to all controllers that the CPU is not in a halt or wait condition. The clock-out signal designates the time at which a controller can switch between the enable and disable states. Switching between enable and disable states can take place only when the CPU is in the halt or wait condition.

The suppress-out control is used singly or in conjunction with an outbound tag to provide suppress status, suppress data, chain command, or selective reset. At the end end of an I/O operation, a controller transmits status to the channel on the bus-in lines as controlled by the status-in tag. Status indicates to the channel whether or not errors were detected during the operation and that the operation is complete. If the channel replies to the status-in signal with a command-out, the controller holds (stacks) the status data. When select-out again is activated at the controller with the stacked status, the status information will be transferred to the channel, provided that the suppress-out line is not active. If the suppress-out line is active, the controller holds the status. If the controller activates the request-in line to transfer status information to the channel and the suppress-out line is activated before the controller receives select-out, the suppress-out signal deactivates the request-in line. During a sense or seek operation, when the controller can wait for data transfer without causing an overrun condition, the suppress-out signal blocks service-out. The channel activates suppress-out before the service-in tag is deactivated to ensure that a subsequent request for data or request to transmit data is suppressed. When a chained command operation is desired, the channel activates the suppress-out line after the controller begins to transmit the ending status and before the channel activates service-out in response to status-in. When suppress-out is active at the same time as service-out and when service-out is responding to status-in, selection of that controller is maintained, and the next command from the channel is directed to that controller. When the channel activates suppress-out before deactivating operational-out and keeps suppress-out active until after operational-out is again activated, that controller is selectively reset.

The channel activates the metering-out line of all attached controllers when the CPU usage time meter is recording. All controllers that are not disabled record time on their respective meters.

The metering-in line is activated when the controller is selected by the channel and the channel activates the operational-out line. Metering-in, when active, causes the usage time meter in the CPU to record.

Interlocks

The interlock lines consist of operational-out, operational-in, and power interlock lines. The interlock lines allow only one controller to be electrically connected to the channel at a time.

The operational-out line is activated when the CPU is reset during the power-on sequence and remains on as long as the channel remains in operation. When operational-out is deactivated, the attached control units are reset. The operational-out signal is used to gate all outbound tags; therefore, when the operational-out line is deactivated, the outbound tags have no effect.

The operational-in line is activated by the controller when a select-out signal is routed to the controller. When the operational-in line is activated for a particular operation, it remains up until all information is transferred between the channel and the disk drive. The operational-in line is deactivated at the same time as or after the activation of the outbound tag associated with the transfer of the last byte of information if the select-out line is deactivated. Data on the bus-in lines and the activation of inbound tags can be enabled only when operational-in is active.

REGISTER

The register function contains 14 general-purpose registers and two specific-purpose registers. All general-purpose registers contain eight bits plus parity. Each general-purpose register is used for several different functions, and each one may or may not perform the function of its given name. The use of these registers is under the control of read-only memory (ROM) microprograms. The general-purpose registers are as follows:

- GL – Gap length register
- BY – General register
- FR – Flag register
- KL – Key length register
- DH – Data length high register
- DL – Data length low register
- OP – Operation code register
- GP – General-purpose register
- SP – Seek-in process register
- UR – Unit address register
- DR – Data read register
- DW – Data write register
- BX – Code check burst register
- CX – Code check register

All general-purpose registers have outputs to the A bus. Additionally, the BY register has an output to the B bus and to the DW register. The OP register has an additional output to the Read-Only Memory Address Register (ROMAR) where it is used in determining the Read-Only Memory (ROM) address. The UR register has an additional output (UR4 through UR7) that is used in selecting a disk drive. The DR register has two additional outputs: one to the B bus and the other to the File Data Register (FDR) in the serializer/deserializer when writing data. The DW register has an additional output that is used to put information on the bus-in lines.

The specific-purpose registers contain eight bits and no parity. The two specific-purpose registers are the following:

- DISP – Display register
- ST – Status register

During test mode (TEST/INLINE/NORMAL switch set to TEST), the contents of the DISP register will be displayed on the REGISTER indicator lamps. The content of the DISP register is the data on the ALU bus. The ST register is used by the microprogram for branching control. Each bit of the ST register may be set or reset under microprogram control to indicate conditions within the controller. The ST register receives its input from the ALU bus in test mode and is under the control of the microprogram (SS field of the ROM) during normal operation.

TIMING

The timing function contains two oscillators, a timing circuit, and reset circuits.

An 8 MHz oscillator controls the timing and reset circuits, and a 5 MHz oscillator is used by the serializer/deserializer to clock the writing of data. Data is written at a 5 MHz rate on the disk pack.

The timing circuit consists of a five-bit, free-running ring counter and gating which produces five discrete machine timing signals–T0, T1, T1.5, T2, and T3. The ring counter is clocked by the 8 MHz clock. The gating decodes the five discrete timing signals which are each 62.5 nanoseconds in duration. The spacing between T0, T1, T2, and T3 is 62.5 nanoseconds. Timing signal T1.5 is a half-step signal which occurs between T1 and T2, hence the name T1.5.

The reset circuits cause the controller to reset selectively or totally upon receiving certain signals from the channel or the test panel or upon detecting errors within the controller.

MACHINE STATUS

The machine status function indicates conditions that occur during an operation, indicates the controller address, and indicates the test requirements set in at the test panel. The machine status function consists of the error register (ER), the IS gates, and the IE register/gates. The outputs of each are entered into the A bus at specific times.

The ER register holds conditions that occur during an operation. ER0 indicates that a serial data error occurred in the serializer/deserializer during a write operation. ER1 gates an address out for testing by the microprogram. ER2 indicates a bus-out parity error. ER3 is used by the microprogram to indicate to the channel that the controller is not busy. ER4 indicates an A register parity error. ER5 is not used. ER6 indicates that channel B is selected in a two-channel controller. ER7 indicates that a halt I/O command has been sent by the channel.

The IS gates supply the controller address and information regarding the attached disk drives. IS0 through IS3 indicate the address of the controller. IS4 indicates that disk drive A (module A) has been selected for the operation to be performed. IS5 indicates that the disk drive selected for an operation is not busy, has not indicated a seek incomplete, is not at the end of a cylinder or does not indicate an unsafe condition, and is online. IS6 indicates that a request for service (gated attention) has been received from a spare disk drive. IS7 indicates that a request for service has been received from one of the eight online disk drives.

The IE register/gates indicate that the switch settings on the test panel are for an inline test of a failing disk drive. IE0 indicates that the test panel MODE SELECT switch is in the RTN (routine) or LOAD position. IE1 indicates that the MODE SELECT switch is in the LOAD, RSLT (result), or ERR (error) position. IE2 is not used; IE3 through IE5 form an inline routine code that controls the inline routine sequence. IE6 indicates command chaining. IE7 receives its input from the file tag register (FT7) which indicates module select.

ARITHMETIC LOGIC UNIT

The Arithmetic Logic Unit (ALU) function performs add, subtract, AND, OR, and exclusive-OR operations within the controller. The ALU function consists of the A register, the B register, arithmetic logic unit circuits, and control circuits.

The A register is the common entry point to the ALU circuits from the A bus. Selection of data to be entered into the A register is under the control of the SA field in the ROM.

The B register is the common entry point to the ALU circuits from the B bus. Selection of data to be entered into the B register is under the control of the SB field in the ROM. True form/complement form control of B bus data entering the B register is controlled by the SV field in the ROM.

The ALU circuits perform their arithmetic functions under control of the SC field in the ROM. The ALU circuits perform eight different operations. The output of the ALU circuits is gated out to the ALU bus.

READ-ONLY MEMORY

The Read-Only Memory (ROM) function contains fixed, predetermined information that is used to control the operation of all logic functions in the controller. The information in the ROM can only be read out. The stored information cannot be changed.

The ROM contains 2,048 48-bit words. Each word is divided into 13 fields, each having a specific function. Several of the fields are used in the ROM address to determine the next word to be read out. Refer to the following chart.

Bits	Field	Function
0	PC	Parity bit for the entire word being read
1	PA	Parity bit for the ROMAR
2-4	Spare	Not used
5	OM	When active, a word in an odd-numbered module is addressed. 1 = most significant half of quadrant; 0 = least significant half of quadrant
6-9	SL	Used to control ROMAR bit 0 for branching purposes
10-13	SH	Used to control ROMAR bit 1 for branching purposes. Also used to select a new quadrant

Bits	Field	Function
14-19	SN	Used to provide bits 2-7 of the ROMAR for the next word to be addressed in the microprogram
20-23	SS	Controls set and reset of the ST register
24-28	SD	Controls destination of the information on the D bus
29-36	SK	Provides a constant to the B register and to bits 9 and 10 of ROMAR
37-38	SB	Controls B register data source
39-41	SC	Controls carry functions and logical operation of ALU
42	SV	Sets B register to true form or complement form
43-47	SA	Used to control the A register data source

An 11-bit address register is used to address the ROM. The address is determined by different inputs to the ROM address register (ROMAR) at different times. As shown in the following chart, inputs to the ROMAR are outbound tags and controls from the channel interface function, status (ST) and operations code (OP) registers, A bus, and SN and SK fields from the ROM. Test panel inputs, START0-10, determine the address during test mode.

The ROM utilizes the current transformer principle. Ninety-six transformers are selectively linked by drive lines; however, only 48 are selected for a specific word. The ROM contains 2,048 drive lines that represent the

Input or Control	ROM Address Bits												
	10	9	8	7	6	5	4	3	2	1		0	
SL and SH Fields										SH 0 1 2 3	Branching Control	SL 0 1 2 3	Branching Control
										0 0 0 0	– – –	0 0 0 0	– – –
										0 0 0 1	SHO /	0 0 0 1	SLO /
										0 0 1 0	ST0	0 0 1 0	ST3
										0 0 1 1	OP6	0 0 1 1	ST5
										0 1 0 0	ST2	0 1 0 0	ST7
										0 1 0 1	ST4	0 1 0 1	DEQ0
										0 1 1 0	ST6	0 1 1 0	– – –
										0 1 1 1	FT5*	0 1 1 1	UMSSM
										1 0 0 0	– – –	1 0 0 0	SERVO
										1 0 0 1	CARRY	1 0 0 1	SORSP
										1 0 1 0	COMMO	1 0 1 0	SELTO
										1 0 1 1	SUPPO	1 0 1 1	OP1
										1 1 0 0	TEST*	1 1 0 0	OP3
										1 1 0 1	OP0	1 1 0 1	OP5
										1 1 1 0	OP2	1 1 1 0	ST1
										1 1 1 1	OP4	1 1 1 1	OP7
SN Field				SN0	SN1	SN2	SN3	SN4	SN5				
A BUS (when SL=6)				ABUS 7	ABUS 6	ABUS 5	ABUS 4	ABUS 3	ABUS 2	ABUS 1		ABUS 0	
OM Field			OM										
SK Field	SK5	SK6											
Test Inputs START0-10	START 10	START 9	START 8	START 7	START 6	START 5	START 4	START 3	START 2	START 1		START 0	

*Model 1015 only

2,048-word capacity of the ROM. When a specific bit of a specific word is to represent a logical one, the drive line passes through the eye of the transformer. When a specific bit of a specific word is to represent a logical zero, the drive line bypasses the respective transformer. When a current pulse is passed through the drive line, it induces a current pulse into the secondary winding (sense winding) of the transformer if the drive line passes through the eye of the transformer. The current developed in the sense winding is detected by the sense amplifier, which passes it to the sense amplifier latch associated with that bit of the word.

Parity checks are made of the ROMAR and of all sense outputs of the ROM. PA is the parity bit for the ROMAR, and PC is the parity bit for the sense outputs. If a parity error is detected, a parity error signal is sent to the test select and display function where the parity error is displayed.

SERIALIZER/DESERIALIZER

The serializer/deserializer (SERDES) is used for reading and writing data on the disk pack in the disk drive. The SERDES serializes data (changes parallel-by-byte data to serial-by-bit data) when writing on a disk pack and deserializes data (changes serial-by-bit data to parallel-by-byte data) when reading from the disk pack. Reading and writing are controlled by the microprogram.

The circuits involved in a read operation consist of the input gating, the voltage-controlled oscillator (VCO), the deserializer circuit, and the file data register (FDR). Reading of data from a selected disk drive is enabled by the read gate. Data from the disk drive is applied to the VCO which synchronizes the frequency of the read circuits with that of the incoming data. The VCO also separates the clock from the data pulses. The output of the VCO is routed to the deserializer. The deserializer consists of gates that are controlled by the phase (PH) counter. As data is applied to the deserializer gates, the PH counter gates the data into the respective bits of the FDR. When a complete byte of data is entered into the FDR, the byte is transferred from the FDR to the data read (DR) register. Data transfer continues in this manner as long as the read gate is active.

The circuits involved in a write operation consist of the FDR, serializer circuit, write clock circuit, PH counter, and output gating. Writing of data is enabled by the write gate. Data is routed to the FDR from the DR register in parallel, one byte at a time. The output of the FDR is routed to the serializer where it is gated out, one bit at a time, by the PH counter. The PH counter is clocked by alternate cycles of the 5 MHz osciliator. The write clock circuit is gated by alternate cycles of the 5 MHz oscillator, but displaced 180 degrees from those which control the PH counter that gates the output of the FDR. The gated data output of the serializer and the output of the write clock circuit are interlaced and transmitted to the selected disk drive. This interlacing of data and clock is known as double-frequency writing.

The burst check circuits are used when data is read or written in bursts; that is, data is transferred one byte after another. The circuits involved in burst checking are the burst control circuits, the burst register, the exclusive-OR circuits, and the BX and CX registers. Burst operation is enabled by the microprogram through FT register bit 4. Additionally, the microprogram sets the BX and CX registers to all ones before the burst check begins. As the burst operation begins, the first byte of data (output of FDR) is exclusively ORed with the output of the BX register (all ones) if the number of bytes in the record is even or with the output of the CX register (all ones) if the number of bytes in the record is odd. The results of the exclusive-ORing are loaded into the register that was used in the exclusive-ORing. The next byte of data is exclusive-ORed with the output of the alternate register (the register not used for the first byte). The results of this exclusive-ORing is loaded back into the register. The exclusive-ORing process continues alternating between the BX and CX registers. For read operations, the microprogram determines when a complete record has been read; at which time, the two burst check bytes at the end of the record are exclusive-ORed with the residue in the BX and CX registers. The result of the exclusive-ORing should be all zeros. For write operations, the microprogram determines when a complete record has been written; at which time, the burst check residue in the BX register is written on the disk as the first burst check byte, then the residue in the CX register is written.

Following the two burst bytes, an indicator byte and a bit count byte are written. The indicator bytes define the address of the controller and of the disk drive which were used in writing the data. The bit count byte contains the complement of the total number of data bits in the recorded field. The bit count includes the data bit counts in the sync byte, in the data field, and in the first burst byte. During a read operation, the bit count byte is checked against the number of bits counted in the sync byte, data field, and first burst byte. If the bit count does not agree, a data check error is indicated.

DISK DRIVE INTERFACE

The disk drive interface (DDI) function contains data and control circuits that connect the disk drive to the controller for reading and writing data. The circuits contained in the DDI are the File Control (FC) and File Tag (FT) registers, gating networks consisting of Module Selected (MS), Seek Complete (SC), File Status (FS), Old Address (OA), and Drive Selected (DS) gates, and a drive select error detection circuit.

The FT register identifies the type of data being sent to the disk drive from the FC register. Only FT bits 0 through 3 (tag lines) are sent to the disk drive. Only one tag line can be active at a time. FT bits 4, 6, and 7 are

used within the controller to identify various functions. FT4 indicates to the controller when to write an address mark or when to allow burst operation. FT6 indicates to the controller that the number of bytes in a record is even. FT7, when active, enables the MS gates. Inputs to the FT register are from the ROM (SN5) and the ALU bus. The input from the ALU bus determines the FT bit to be set, while the SN5 input enables all bits of the register.

The FC register transfers operating information to the disk drive under the control of the FT register. The following chart indicates the type of information transferred to the disk drive for specific tag lines.

The inputs to the FC register are from the ROM (SN5) and the ALU bus. The inputs from the ALU bus determine the FC bit to be set, while the SN5 input enables the register.

The MS gates determine the disk drive (module) to be selected by decoding bits 4 through 7 of the UR (unit address) register. The MS gates are enabled when FT7 is active.

Bus Line	Function			
FC0	Write Gate	Cylinder 128	Forward	128
FC1	Read Gate	Cylinder 64	Select Lock Reset	64
FC2	Seek Start	Cylinder 32	– – –	32
FC3	Reset Head Register	Cylinder 16	Head Address 16	16
FC4	Erase Gate	Cylinder 8	Head Address 8	8
FC5	Select Head	Cylinder 4	Head Address 4	4
FC6	Return to 000	Cylinder 2	Head Address 2	2
FC7	Head Advance	Cylinder 1	Head Address 1	1

Tag Line	Function
FT0	Control
FT1	Set Cylinder
FT2	Set Head
FT3	Set Difference

The SC gates relay gated attention (seek complete) signals from the disk drives to the A bus. In addition to the signals applied to the A bus, all gated attentions are ORed and applied to bit 7 of the Interface Status (IS) gates in the machine status function so that the microprogram can test IS7 for gated attention before testing the individual bits of the SC gates. A gated attention signal is also routed to the channel interface function where it causes the request-in scan control line to be raised if the poll enable latch (IG4) is set and the channel is not selected by another controller.

The FS gates route disk drive status from the selected drive to the A bus. The following chart identifies the status represented by each bit.

The unsafe status, the multiple module select status, and the seek incomplete status are error conditions. The end-of-cylinder status indicates that an attempt was made to advance the head advance register in the selected drive past a count of 19. The write current sense status is checked by the microprograms during a write operation to ensure that write head current is

FS Bit	Status
0	Busy
1	Online
2	Unsafe
3	Write Current Sense
4	Pack Change
5	End of Cylinder
6	Multiple Module Select
7	Seek Incomplete

flowing. The not busy, online, safe, and not-at-end-of-cylinder signals are ANDed to generate the file operable signal which is routed to IS gate bit 5. The microprogram tests IS5 to determine the operability of the selected disk drive. IF IS5 is not set, the microprogram looks at the individual signals to determine the condition that caused the disk drive to become inoperable.

The OA gates route the existing (old) cylinder address in the disk drive to the A bus for use in determining a difference count between the old cylinder address and a new cylinder address.

The drive selected logic DS gates are used in gating the read/write data between a specific disk drive and the serializer/deserializer in the controller. The microprogram can determine which drive is selected by placing the drive selected signals on the A bus.

The drive select error detection circuit determines when more than one drive responds to a drive select signal. If this occurs, a module (drive) select error is routed to bit 6 of the FS gates for the A bus and for subsequent test by the microprogram.

TEST SELECT AND DISPLAY

The test select and display function provides a means of selecting various tests and of displaying information during maintenance and troubleshooting. The test select and display function consists of three general areas: test select, register display, and error and ROMAR display.

The test select circuits contain switches that are used for entering and enabling tests of the controller or of the disk drive. When these test switches are enabled, two types of diagnostics, resident and inline, can be run. These diagnostics are part of the microprograms contained in the ROM. The resident diagnostic checks the operation of the controller; the inline diagnostic checks the operation of the spare disk drive.

The register display circuits display data contained in the register selected by the REGISTER SELECT switch. Only one register can be displayed at a time and is selected through the use of the REGISTER SELECT switch.

The error and ROMAR display circuits display errors that occur during an operation and display the ROMAR. The errors displayed are sense amplifier error, ROMAR error, data error, and machine stop. The SENSE AMP error indicator lights when a parity check of the sense amplifier outputs fails. The ADDRESS error indicator lights when a parity check of the ROMAR outputs fails. The DATA error indicator lights when a bus-out data error occurs or when a data error occurs in the ALU. The PROBE indicator lights when the address of the ROMAR matches the address set into the address stop switches. The ROMAR display circuits display the address of the ROMAR during all modes of operation.

POWER

The power function supplies the voltages required for the operation of the controller and controls the application of power to the controller and to the attached disk drives.

In normal and inline modes of operation, power turn-on and power turn-off is controlled by the CPU. In the test mode of operation, power is controlled from the controller test panel.

All dc voltages are monitored by a power monitor circuit which disables the interface between the channel and the controller and the interface between the controller and the attached disk drives if any of the monitored voltages exceed their tolerance limitations.

SECTION 2
THEORY OF OPERATION

This section contains theory of operation information for the various functional areas in the controller. The theory of operation is based on the CD14 Controller logic diagrams.

In this manual, a particular signal may be referred to as being high or low, active or inactive. High and low define the two relative voltage levels of the signal. High indicates the more positive voltage level of the signal, and low indicates the less positive voltage level. A signal and its complement are active at the same time but one is high and the other low. For example, when signal ADDCOMPA is high, it is active; the complement signal is ADDCOMPA/ and is active when it is low. The general rule for interpreting signals is as follows: If a signal is followed by a slant mark (/), it must be low to be active (e.g., ADDCOMPA/, OPINA/). If a signal is not followed by a slant mark, it must be high to be active (e.g., ADDCOMPA, OPINA).

BUS-OUT LINES (CI-1)

The bus-out lines consist of nine (eight bits plus parity) lines. For two-channel controllers, the bus-out lines are duplicated for the second channel. The bus-out lines transfer information from the channel to the attached control units (controllers) and are contained in one cable coming from the channel to the BUS INPUT connector of the first controller. The bus-out lines from the BUS INPUT connector are connected in parallel (inside the controller) to the BUS OUTPUT connector (not shown on CI-1) for "daisy-chaining" to the next controller.

The type of information transferred on the bus-out lines is indicated by an associated outbound tag line. For example, when the address-out tag line is active, the information on the bus-out lines is an address.

When the controller activates the address-out line (ADDOUTA high), selection of a controller is initiated. All attached controllers attempt to decode the address on the bus-out lines; but, since each controller has a unique address, only one can actually decode the address. The address is decoded if the content of BUSOUT0 through BUSOUT3 matches the address set into the channel A address block. (If the address of the controller is 1001, the channel address block must have jumpers for CU0, CU1/, CU2/, and CU3 in order that all high signals be applied to the ADDCOMPA gate.) If the controller that decoded the address is not busy (OPINA/ high) when the channel activates the address-out line (ADDOUTA high), an address comparison (ADDCOMPA high) is made. The ADDCOMPA signal is used to reset the propagate-select out latch (see CI-2).

The bus-out information is checked for odd parity by the parity integrated circuit (IC). The parity output of the parity IC (pin 6) must always be high when information is on the bus-out lines. This is a condition required for the ADDCOMPA gate. If parity is bad (EVENPRTY high), error register bit 2 (ER2) is set (see STAT-1), and the CHECKING DATA indicator on the test panel is lit.

CHANNEL A OUTBOUND TAG and CONTROL LINES (CI-2)

The outbound tag and control line circuits are the interface between the channel and the controller and process the incoming signals used in the operation and control of the controller and attached disk drives.

With the exception of clock-out, all channel A outbound tag and control lines are inputs on CI-2. Clock-out is an input on TIM-2.

Outbound Tags

Address-out, command-out, and service-out are the three outbound tags.

The ADDOUTA/ and ADDOUTA signals (output signals 10 and 11 respectively) are active when the channel raises the address-out tag (ADDOUTA;Q high), the channel is operational (OPOUTA;Q high), and the CHANNEL A enable switch on the controller is enabled (ENBLATH high) to indicate that the data on the bus-out lines is an address. The gated address-out signal (GTDADDOUTA/) is active when the conditions that activated the ADDOUTA gate exist while an operation is in process (CHANALTH high) to set ER7 latch (see STAT-1), indicating a Halt I/O command from the channel. When the ER7 latch is set, the command (COMMO) latch is set.

The COMDOUTA/ signal is active when the channel raises the command-out tag line (COMOUTA;Q high), the channel is operational (OPOUTA high), the CHANNEL A enable switch is enabled (ENBLATH high), and the controller has been selected (CHANALTH high) to indicate that the data on the bus-out lines is a command that specifies the operation to be performed. When COMDOUTA/ goes low, the COMMO latch is set at the following T0 time. The COMMO signal is used by the microprogram for branching.

The SERVOUTA/ signal is active when the channel raises the service-out tag (SERVOUTA;Q high), when the channel is operational (OPOUTA high), and when an operation is in process (OPINA high) to indicate that the channel has accepted the data on the bus-in lines or has placed data on the bus-out lines requested by the controller via a service-in tag. The SERVO latch is set at T1 when SERVOUTA/ is low.

Outbound Special Control Lines

Metering-out, suppress-out, and clock-out are the outbound special control lines. Clock-out is shown on TIM-2.

The OPMETA/ signal is active as long as the channel keeps the metering-out control line active (METOUTA;Q high), the controller is not disabled (ENBLALTH high), and the disk drive selected is not the spare disk drive (SSM/ high) to record CPU usage on the elapsed time meter.

The SUPPOUTA/ signal is active when the channel raises the suppress-out line and the controller is selected (CHANALTH high) to suppress data transfer, to suppress status, to indicate chain command, or to provide selective reset. The SUPPO latch is set at T1 time when SUPPOUTA/ is low and the microprogram has set the status-in latch (IG5 high).

Outbound Scan Control Lines

Select-out and hold-out are the outbound scan control lines. The hold-out line complements the select-out line by enabling the select-out logic to propagate select-out.

Hold-out (HLDOUTA) is an input to the set and reset inputs of the select-out latch. HLDOUTA high causes the select-out latch to set when the channel activates the select-out line (SELOUTI;Q high) and the channel is operable (OPOUTA high). When the channel drops the hold-out line, the select-out latch is reset. The dropping of hold-out cancels the effect of select-out in all controllers attached to the channel.

The select-out line is used in conjunction with the select-in line to connect all controllers serially into a loop so that the channel can interrogate each controller in a priority sequence. The select-in line is a return to the channel of the select-out line. As shown in Figure 1-3, a controller may be connected to either the select-out line or to the select-in line. When a controller is connected to the select-out line, it is connected for high priority; conversely, when a controller is connected to the select-in line, it is connected for low priority.

When the channel activates the select-out line (SELOUTI; Q high) of a controller connected for high priority, the jumper between E1 and E2 in the priority selection block routes the select-out signal through closed contacts of relay K1 to a channel receiver (CR-EE). Relay K1 is always energized except when the DRIVER DEGATE switch on the test panel is set to ON (SEL-REC;W high). The output of the channel receiver (SEL-OUTA) will cause the select-out latch to set if the hold-out line is active (HLDOUTA high) and the channel is operational (OPOUTA high). When a controller is connected for high priority, the select-in line (SELINIA;Q) is jumpered to the SELINOA;Q output line (E8 to E7 on the priority selection block). If the controller is connected for low priority, the select-out line (SELOUTI;Q) from the channel (or higher priority controller) is jumpered through to the SELOUTOA;Q output line. The controller connected for low priority will act upon a select-out signal that is applied through the SELINIA;Q input line in the same manner as a controller connected for high priority when the select-out signal is applied to the controller through the SELOUTIA;Q line.

The state of the propagate select-out latch determines whether the select-out signal will be passed to the next controller or will be blocked from reaching the next controller if an operation is desired of this controller. The propagate select-out latch is normally set after an operation has been completed; that is, the controller is not busy (CUBUSYA/ high), the controller has not initiated an interface signal sequence (OPINA/ high), the controller has not requested service (REQINA/ high), and the channel has not raised the address-out line (ADDOUTA/ high) and the select-out line (SELOUTA/ high). By setting the propagate select-out latch under these conditions, the select-out signal is propagated when the channel again activates the select-out line if the address on the bus-out lines is not that of this controller (PROPSELOUTA high). If the channel A interface is disabled in the controller (ENBLALTH/ high) when the channel activates the select-out line (SEL-OUTA high), PROPSELOUTA goes high. Whenever PROPSELOUTA goes high, the select-out signal (or the select-in signal when the controller is connected for low priority) is passed to the next controller through channel driver CD-R, terminals E14 and E13, and output line SELOUTOA;Q (high priority) or terminals E16 and E15 and output line SELINOA;Q (low priority).

When the channel places an address on the bus-out lines for this controller and activates the address-out tag (ADDCOMPA high) before activating the select-out line (PROPSELOUTA/ high), the propagate select-out latch is reset to inhibit the propagation of this signal. When the select-out signal is then activated, the following signals are activated: initial select A (INTALSELA/ low), addressing A (ADDRESSINGA high), and responding A (RSPNGA/ low).

The propagate select-out latch is reset if the controller is requesting service (REQINA high) when the select-out latch is reset (SELOUTA/ high). If, after the propagate select-out latch is reset, the channel initiates a selection sequence but the address does not match (ADDOUTA and ADDCOMPA/ high), the propagate select-out latch is again set.

In two-channel controllers, the propagate select-out latch is set if channel B is working with the controller when channel A initiates a polling sequence (ADDOUTA/ and SELOUTALTH high).

When the power is turned off or the controller is disabled (INTFDSBLA;W high), the select-out signal (SELOUTIA;Q) is routed directly to the SELOUTOA;Q line (high priority), and the select-in signal (SELINIA;Q) is routed directly to the SELINOA;Q line.

In two-channel controllers, the channel A latch, when set (CHANALTH signal high), indicates that the controller is working with channel A; therefore, channel B cannot work with the controller until channel A has finished. The inverse is also true. When both channels simultaneously attempt to select the controller, the channel selection circuit resolves the tie.

The channel selection circuit (see Figure 2-1) can assume three different states: channel A selected, channel B selected, or neutral. The neutral state is assumed when neither channel is selected. When the channel selection circuit is in the neutral state, the controller is selected by the first channel to complete the selection sequence. When a channel has been selected, it remains selected until the ending status is sent to the channel: at which time, it returns to the neutral position. If the second channel attempts to select the controller while the first channel is selected, the controller responds to the second channel with the short controller busy sequence.

The neutral position is assumed when the select A logic, select B logic, responding A (RSPNGA/), and responding B (RSPNGB/) are all high. Under these conditions, the CHANALTH/;A and CHANBLTH/;A signals are high, which is caused by the outputs of the two E8 gates being low. If channel A desires to select the controller, one of the select A logic inputs goes low, causing the

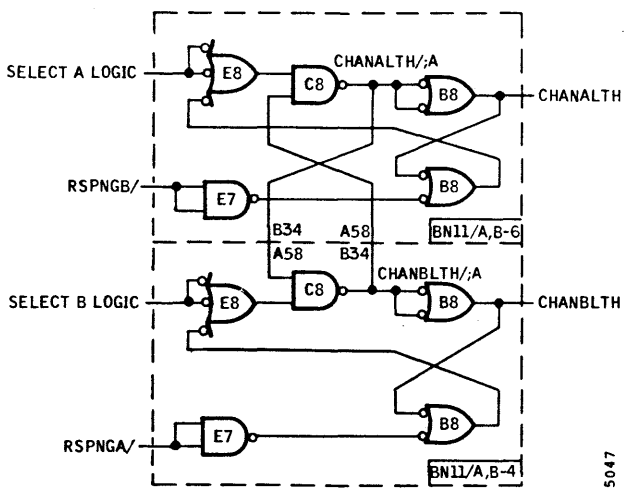


Figure 2-1. Channel Selection Circuit

CHANALTH/;A signal to go low, since the CHANBLTH/;A signal is high. With CHANALTH/;A low, CHANBLTH/;A is held high even if channel B attempts to select the controller. When the RSPNGB/ signal goes low as channel B attempts to select the controller, the B8 gate input to gate E8 goes low to further ensure that channel A remains selected. The controller will respond to channel B with the short controller busy sequence (see CI-8). The reaction described above also occurs when channel B is selected.

If both channels attempt to select the controller at the same time, the tie-breaking latch (gate C8 on each circuit board) resolves the tie by enabling one or the other channel latches.

When channel A has been selected (CHANALTH high) and the channel is operative (OPOUTA high), the channel A selected signal (ASEL) goes high to enable the metering-in line (see CI-7). During the test mode of operation (TESTSW/ low), the GATEDASEL/ signal goes low when channel A is selected (ASEL high) to inhibit resetting the channel A enable latch (see TIM-2).

Outbound Interlock Line

The outbound interlock is the operational-out line. The operational-out line (OPOUTA;Q) is active (high) as long as the channel is operable. Depending on the state of the suppress-out line, the channel may use the operational-out line to selectively reset a controller or to reset all controllers (general reset). If the channel activates the suppress-out line before deactivating the operational-out line and maintains suppress-out active until after operational-out is again activated, a selective reset will reset the controller operating with the channel at that time (see TIM-3). If the operation-out and suppress-out lines are both deactivated for 6 microseconds, all controllers not operating in the test mode will be reset.

The operational-out line (OPOUTA) is an input to all outbound tag line gating; therefore, the channel must be operational in order that the tag lines may be gated into the controller.

The command-out (COMMO), service-out (SERVO), suppress-out (SUPPO), and select-out (SELTO) latches are set by their respective channel output lines. In two-channel controllers, these latches are set by either channel. The outputs of these latches are used by the ROM for branching.

CHANNEL B OUTBOUND TAG and CONTROL LINES (CI-3)

The channel B outbound tag and control lines operate for channel B in the same manner as those for channel A (see CI-2).

The circuits shown on CI-3 are used in two-channel controllers only.

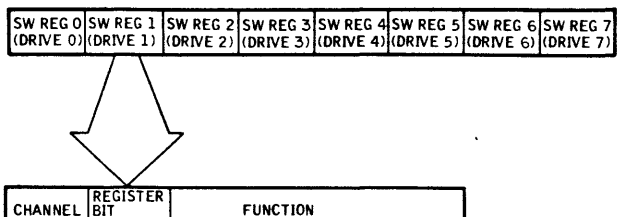
SW REGISTERS (CI-4)

The SW registers are used in two-channel controllers only.

The eight SW registers, one for each online disk drive (SW0 is associated with drive 0, SW1 with drive 1, etc.), are used by the microprogram to store the reserve status and device-end status of each disk drive for each channel (see Figure 2-2). Four bits of each SW register are associated with channel A, and the remaining four bits are associated with channel B. SW1-0 through SW1-3 are the four bits of SW register 1 (SW1) associated with channel A; SW1-4 through SW1-7 are the four bits of SW1 associated with channel B.

The input to the SW registers is from the ALU bus. The set SW register signal (SETSWREG/—SD field equals 12), when low, allows the status on the ALU bus to be entered into the SW register associated with the disk drive to be used for an operation as determined by the state of the UR register inputs (UR4 through UR7) to the decoder IC. The combination of the SETSWREG/ and the selected output of the decoder IC develops a register clock signal (CLK0 for SW register 0, CLK1 for SW register 1, etc.) that, when high, causes the contents of the ALU bus to be entered into the selected SW register.

The TAG input signal to bits 1 and 5 of the SW registers controls the method of presenting a disk drive device-end status resulting from a power-up seek or a disk pack change (not-ready-to-ready sequence). The TAG signal is developed by the TAG switch (see TEST-1). When the TAG switch is pressed (its internal indicator lit), the TAG signal is high, thus allowing ALU1/ and ALU5/ to be entered into bits 1 and 5 respectively of the selected SW register if a device-end status is indicated by the disk drive. The device-end status must be cleared by each channel before the channel can address the disk drive for a command execution. When the TAG switch is deenergized (its internal indicator not lit), the TAG signal is low, thus inhibiting ALU1/ and ALU5/ from being entered into bits 1 and 5 of the selected SW register. This allows a device-end status to be cleared by only one channel since the device-end status was not stored in bits 1 and 5 of a SW register.



CHANNEL	REGISTER BIT (SW1-X)	FUNCTION
A	0	DRIVE 1 RESERVED FOR CHANNEL A
	1	DRIVE 1 DEVICE END (POWER-UP SEEK OR PACK CHANGE) -CHANNEL A
	2	DRIVE 1 DEVICE END (SEEK COMPLETE OR BUSY) - CHANNEL A
	3	DRIVE 1 SEEK IN PROGRESS OR BUSY - CHANNEL A
B	4	DRIVE 1 RESERVED FOR CHANNEL B
	5	DRIVE 1 DEVICE END (POWER-UP SEEK OR PACK CHANGE) - CHANNEL B
	6	DRIVE 1 DEVICE END (SEEK COMPLETE OR BUSY) - CHANNEL B
	7	DRIVE 1 SEEK IN PROGRESS OR BUSY - CHANNEL B

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Figure 2-2. SW Register Bit Meaning

Bit 0 of a SW register associated with a disk drive reserved solely for channel A is set by the microprogram when channel A issues a reserve command if that disk drive is not already reserved by channel B. When channel A issues a release command, bit 0 is reset by the microprogram.

When the pack change line has been activated by a disk drive (CPC/ low—see DDI-1), bit 1 of the associated SW register is set by the microprogram to indicate that the disk drive has gone from a not-ready condition to a ready condition (either a power-up seek or a pack change). Bit 1 is reset by the microprogram when the device-end status has been accepted by channel A.

Bit 2 of an SW register is set by the microprogram when a gated attention from the associated disk drive is detected, indicating that a previously issued seek command has been completed. Bit 2 is also set when channel A attempts to select the associated disk drive reserved for channel B to indicate that the disk drive is busy. After channel B issues a release command for the disk drive, the device-end status is sent to channel A. When channel A accepts the status, bit 2 is reset.

When channel A issues a seek command for a specific disk drive, the microprogram sets bit 3 of the associated SW register when the seek-start command is sent from the controller to the disk drive. When the disk drive completes the seek, it activates the gated attention line, which, in turn, causes the request-in line to the channel to be activated so that device-end status can be presented. When the microprogram detects the gated attention, it determines whether the attention is the result of a power-up seek, pack change, or a previously issued seek command. Since bit 3 was previously set, the microprogram determines that the gated attention is the result of a previously issued seek command and sets bit 2 of the associated SW register and resets bit 3. If status is stacked by the channel, bit 2 remains set. If the channel does not stack status, bit 2 is reset.

Bits 4 through 7 provide status for channel B in the same manner as bits 0 through 3 did for channel A.

The outputs of the SW register associated with the disk drive to be used for an operation are selected (by the state of UR5 through UR7) as inputs to the A bus.

When a channel issues a general reset, that portion of the SW registers associated with the channel issuing the reset is reset (for channel A, RSTCLKA/ goes low and RSTCHANA/ goes high).

ATTENTION CONTROL (CI-5)

The attention control circuits shown on CI-5 are used in two-channel controllers only. For single-channel controllers, as indicated on CI-5, the gated attention signals (CGA0 through CGA7) are jumpered to the AT0A through AT7A and ATTCU0 through ATTCU7 lines respectively. These jumpers are on jumper module circuit board BZ12 which replaces channel D circuit board BL12 in single-channel controllers. Two BZ12 circuit boards are used to replace the two BL12 circuit boards in locations A,B-2 and A,B-3.

The attention control circuit for each of the eight associated disk drives are identical. Figure 2-3 illustrates a typical attention control circuit; that of disk drive 0.

The attention control circuits generate attention signals that are used to poll the channel to present outstanding status without a start I/O or test I/O command from the channel.

A power-up seek or a pack change at the disk drive will activate the gated attention line (CGA0 high). Since a polling interrupt sequence has not yet been initiated by the controller (IG4 low), ATTCU0 and ATTCU go high. The microprogram detects the gated attention and sets SW register bits 1 and 5, if the TAG switch is enabled (TAG signal high), and the poll enable latch (IG4 high). If disk drive 0 is not reserved for channel B (SW0-4/ high) and the controller has not selected channel B (CHANBLTH/ high), AT0A goes high to enable the request-in line (see CI-7). When the channel selects the controller, the controller sends the device-end status to channel A. When channel A acknowledges the status, the microprogram resets SW register 0, bit 1 (SW0-1 low). Channel A can now address drive 0 for command execution. Before channel B can address drive 0 for command execution, the request-in line to channel B must be activated when the controller has not selected channel A (CHANALTH/ high) and is not reserved for channel A (SW0-0/ high). After channel B selects the controller, the device-end status byte is sent to channel B. When channel B acknowledges the status, the microprogram resets SW register 0, bit 5.

When the channel issues a seek command, the controller transfers the seek-command data and a seek-start signal to disk drive 0. When the seek-start signal is sent to the disk drive, the microprogram sets bit 3 of SW0 (SW0-3/ low). Upon completing the seek, the disk drive activates the gated attention line (CGA0 high) that, in turn, activates the AT0A, ATTCU0, and ATTCU signals to indicate device-end status. When the channel accepts the status byte, the microprogram resets bit 3 of SW0.

If channel B attempts to select disk drive 0 while the drive is reserved for channel A (SW0-0/ low), the microprogram examines SW register 0 and finds bit 0 active (indicating that the drive is reserved for channel A). The microprogram causes drive busy status to be sent to the channel and causes bit 6 of SW0 to be set to indicate that the drive is busy. This does not indicate a device-end status to channel B since the drive is reserved for channel A (NR0A low). When channel A is finished with drive 0 and cancels the reservation and the controller is not selected for channel A (NR0A high), a device-end

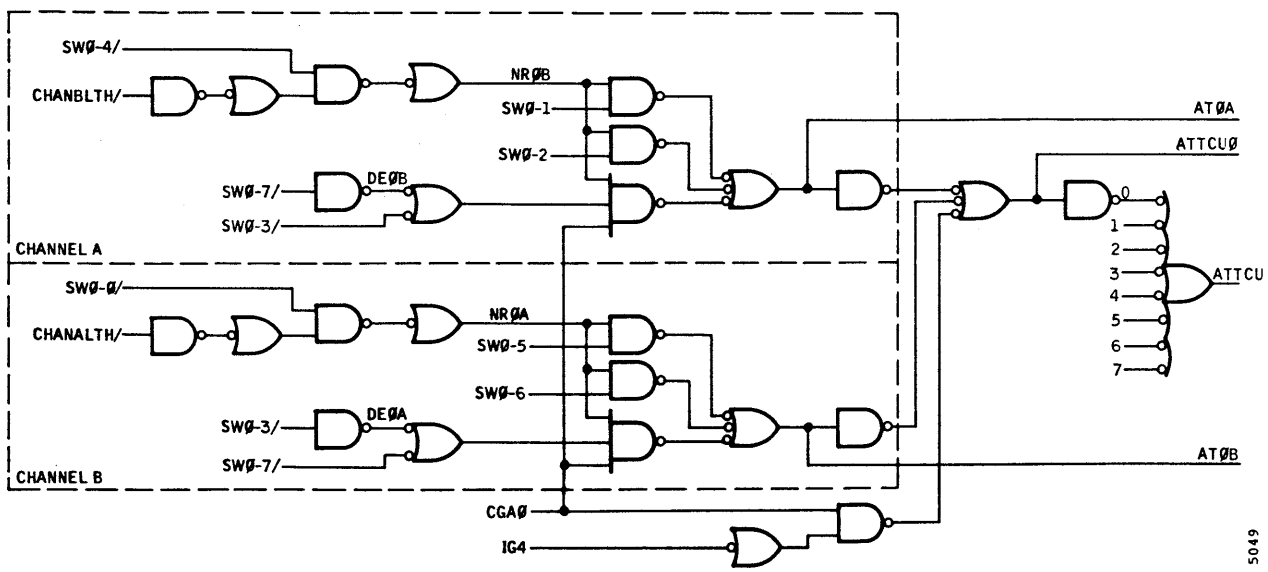


Figure 2-3. Typical Attention Control Circuit

status byte is sent to channel B. When the status byte is accepted by channel B, the microprogram resets bit 6 of SW0 (SW0-6 low). Disk Drive 0 is now available to channel B.

The attention control circuits for channel B operate in the same manner as those for channel A.

SERVICE-OUT RESPONSE (CI-6)

The service-out response (SORSP) circuits control the transfer of data between the channel and the controller for read and write operations.

Read Operation

In the channel interface, a read operation is the transfer of data from the controller to the channel (see Figure 2-4).

When a read operation is to take place, the microprogram sets IG2 and IG6 (read latch and do not suppress data, respectively). When a complete byte of data has been assembled in the DR register and is ready for transfer to the channel, the microprogram causes the contents of the DR register to be placed on the A bus (SAXDR high–SA field equals 17) with its destination as the DW register (SD field equals 18). At T3 following the transfer of the data from the DR register to the DW register, latch 1 is set. The service request latch is set at T1 following the setting of latch 1. Latch 1 is reset at T2 after the service request latch was set. Latch 2 and the SORSP latch are set at T3 after the service request latch sets. With latch 2 set and the channel not yet responding with service-out, the service-in latch is set (see CI-7). With the service-in latch set (SVCINLTH high), both the service request and latch 2 are reset at T0. When the channel responds with service-out (SERVO high), the SORSP and service-in latches reset at T1 (SVCINRST2/ low), indicating to the microprogram that the byte of data in the DW register has been accepted by the channel.

When the microprogram finds that a byte of data in the DR register is ready to be transferred to the DW register and that the byte of data in the DW register has not yet been accepted by the channel, the microprogram enables an alternate routing for the byte of data in the DR register. The microprogram issues a statement (DRBY) which transfers the contents of the DR register to the BY register. (SA equaling 17 puts the data in the DR register onto the A bus, and SD equaling 2 puts the ALU bus data into the BY register.) Latch 1 is set at T3 by SAXDR (SA equals 17), and the DRBY latch is set at T1, indicating that the data contained in the DW register was accepted by the channel; the SORSP latch and service-in latch are reset at T1. With the service-in latch reset (SVCINLTH/ high), the data contained in the BY register is transferred to the DW register (GATEBY/;1 and GATEBY/;2 low). The DRBY latch is reset at T0 after the service-in latch was reset. Since the service request latch was not reset (DRBY/ low), latch 2 is set at T1 following the reset of latch 1 and the DRBY latch to activate the service-in line. This informs the channel that another byte of data is ready for transfer.

When a read operation has been completed, the microprogram resets the read latch (IG2) and IG6.

Write Operation

In the channel interface, a write operation is the transfer of data from the channel to the controller (see Figure 2-5).

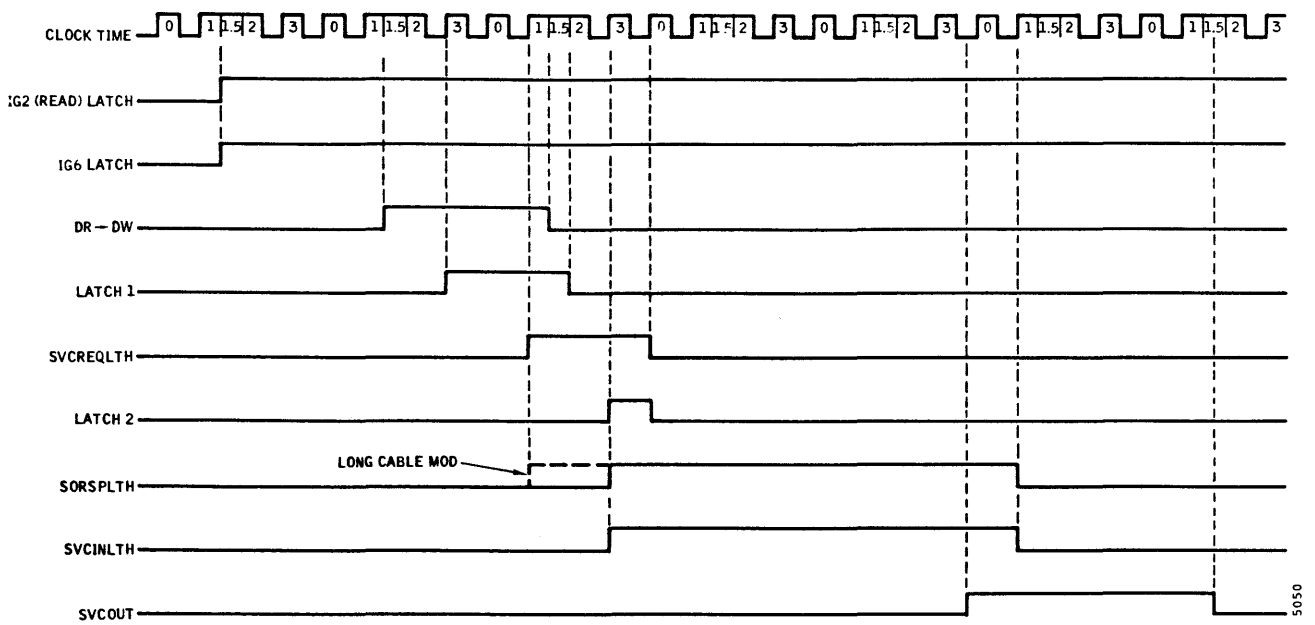


Figure 2-4. Read Operation Timing Diagram

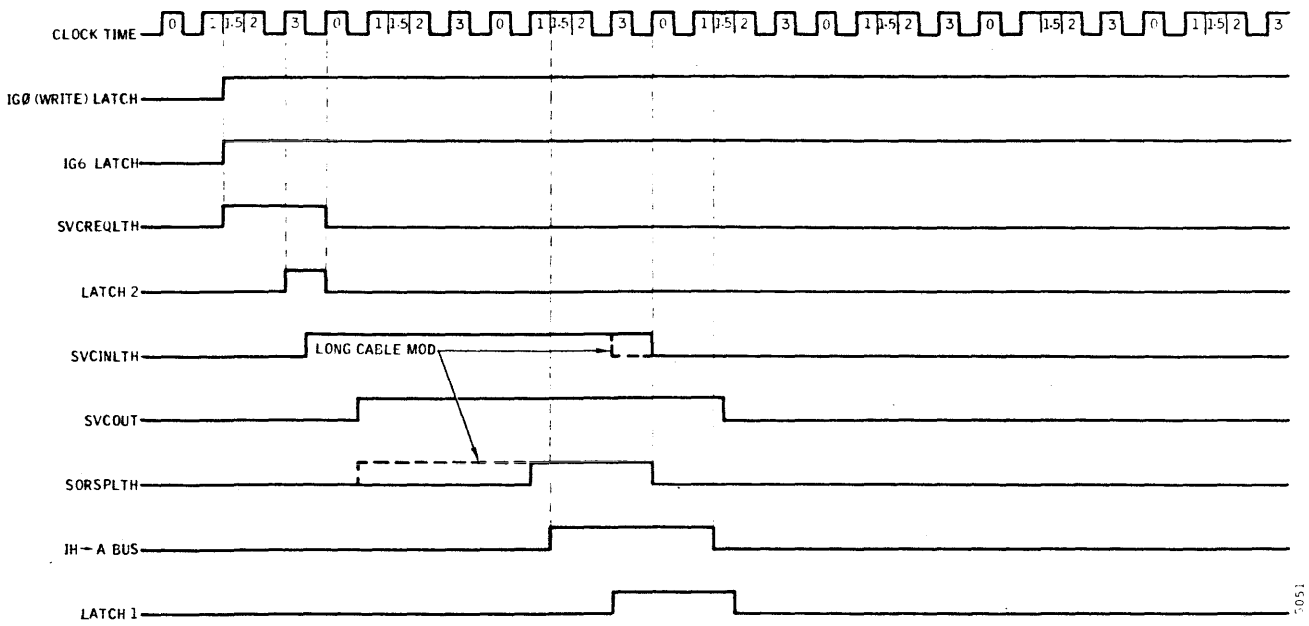


Figure 2-5. Write Operation Timing Diagram

When a write operation is to take place, the microprogram sets IG0 and IG6 (write latch and do not suppress data, respectively). With IG0 set and service-in latch reset (SVCINLTH/ high), the service request latch is set followed by latch 2 at T3. With latch 2 set and the channel not yet responding with service-out (SERVO/ high), the service-in latch is set (see CI-7) to request a byte of data from the channel. When the channel activates the service-out line (SERVO high) to indicate that a byte of data is on the bus-out lines, the SORSP latch is set at T1 (SERVO, SVCINLTH, IG2/, and T1 high). When the microprogram detects that the service-out line is active (SORSP input to ROMAR), it branches on SORSP and issues the SAXIH statement (SA equals 14) which enters the data that is on the bus-out lines into the A bus at T3. After the SAXIH statement is issued, latch 1 is set. With latch 1 set, the SORSP latch is reset at T0 (SLDR/, IG2/, LATCH1, SORSP, and T0 high). Latch 1 and the SORSP flip-flop are reset at the following T2.

When the microprogram determines that too much time is being taken by the channel to respond to a data request and that the normal routing of the bus-out data (bus-out line into the A bus then to the ALU bus and into a temporary storage register) will interfere with continuous operation, it enables an alternate routing for the bus-out data after the channel replies with service-out. The microprogram accomplishes this by issuing the SAXSL statement (SA field equals 25) and the SDXDR statement (SD field equals 17) which sets the SLDR latch at T0. When the channel responds with service-out (SERVO high), the SORSP latch is set at T1. With the SLDR and SORSP latches set, the high IHDR signal (bus-out lines transfer to DR register) enables the bus-out data to be entered into the DR register at T3 (see REG-6). The service-in latch is reset at T3 (IHDR, IG0, and T3 high). The SORSP latch is reset at T0 following the transfer of data into the DR register (SORSP high, T0 high, and IG2 low).

While the microprogram is checking the error (ER) register for any errors which might have occurred during the operation, the service request latch, latch 2, and service-in latch (see CI-7) are reset at T3 by the microprogram statement (SAXER–SA equals 21) that loads the ER register bits into the A bus.

The SORSP latch is set when the channel issues a set-file mask command. The read and write latches are not set (IG2/ and IG0/ high) when a set-file mask command is issued by the channel. The SORSP latch is set when the channel responds with service-out (SERVO, SVCINLTH, IG0/, and IG2/ high).

In controllers modified to operate with extended length bus and tab cables, the timing for setting the SORSP latch is changed. During a read operation, the SORSP latch is set as soon as the service request latch is set (if the DRBY latch is reset) and remains set when the service-in latch is reset (SVCINLTH/ goes high). In a write operation, the SORSP latch is set as soon as the channel responds with service-out (SERVO high) as long as PH27 is not low at that time. The service-in latch (see CI-7) is reset during a write operation at T3 after the microprogram allows the bus-out data to be entered into the A bus (SAXIH high).

CHANNEL A INBOUND TAG and CONTROL LINES (CI-7)

The inbound tag and control line circuits generate the various tag and control signals to identify the type of data being sent to the channel or to request service from

the channel and to provide a common data format and signal sequence.

The IG register (channel control register) is used by the microprogram to enable or disable control signals to the channel.

- IGØ (write latch) is used to enable a request for data from the channel for a write, search, or control operation.
- IG1 (operational-in) is not used; however, the equivalent gating (ALU1 and GATEIG) is incorporated in the operational-in latch reset circuit. The operational-in latch is reset when ALU1 and GATEIG are high.
- IG2 (read latch) is used by the controller to enable a request for service when a byte of data is available for transfer to the channel during read or sense operation.
- IG3 is used to initiate a polling interrupt sequence in order to present status other than device-end to the channel.
- IG4 (poll enable latch) is used to initiate a polling interrupt sequence in order to present device-end status resulting from a gated attention.
- IG5 (status-in latch) is used to enable the status-in line to the channel.
- IG6, when set, inhibits the suppression of data (when SUPOUTA is high). When IG6 is reset, data transfer to the channel is inhibited while SUPOUTA is high.
- IG7 (address-in latch) is used to activate the address-in line to the channel. IG7 is also used in the operational-in latch set logic.

Except for the select-in scan control line, all channel A inbound tag and control lines are outputs of CI-7. The select-in line is an output of CI-2.

All inbound tag and control lines are conditionally gated by the driver degate signal (DRIVDEGATE/) which is normally high. If the DRIVER DEGATE switch is set to ON, DRIVDEGATE/ goes low and inhibits the output of the inbound tag and control lines.

Inbound Tag Lines

Address-in, status-in, and service-in are the three inbound tag lines. The lines are conditioned by operational-in (OPIN), which must be high for the inbound tag lines to be activated.

The address-in tag line is activated (ADDINA;Q high) to inform the channel that the data on the bus-in lines is an address. The address-in line is activated by the microprogram when it sets the address-in latch (IG7 high) if the address-out tag is not active (ADDOUTA/ high).

The status-in tag line is activated (STATINA;Q high) to inform the channel that the data on the bus-in lines is a status byte. The status-in line is enabled when the microprogram sets the status-in latch (IG5 high). If the controller is busy when the channel addresses that controller, the controller will respond with a controller busy status byte without going through an initial selection sequence. The controller busy signal (CUBUSYA/) goes low when the channel is addressing the controller (ADDRESSINGA high) while the controller is still busy (ER7 high). In two-channel controllers, if channel A addresses the controller (ADDRESSINGA and ADDOUTA high) when the controller is selected by channel B (CHANBLTH/;A low), the CUBUSYA/ signal goes low. CUBUSYA/ low sets the CUENDA latch. When channel B disengages from the controller (CHANBLTH/ high), ER3 (see STAT-1) goes high. With ER3 high, the microprogram enables a controller-end polling interrupt. The CUBUSYA/ signal, when active, enables the bus-in parity bit, the status modifier bit (bus-in 1), and the busy bit (bus-in 3) for the controller busy status byte.

The service-in tag line is activated (SERVINA;Q high) during a read operation to identify the data on the bus-in lines as a data byte. During a write or search operation, the service-in tag line is activated to request a data byte from the channel on the bus-out lines. The service-in latch (SVCINLTH) is set during a read operation when a byte of data is ready for transfer to the channel (LATCH 2 high) if the channel has not yet responded with service out (SERVO/ high) and the controller is not suppressing data (IG6 high). During a write operation, the service-in latch is set when data is requested by the controller (LATCH 2 high) if the channel has not yet responded with service-out (SERVO/ high) and the channel is not suppressing data (SUPOUTA+B low).

Inbound Special Control Line

Metering-in is the inbound special control line.

The metering-in line is activated (METINA;Q high) when channel A is selected to operate with the controller (ASEL high) if the CHANNEL A enable switch is energized (ENBLALTH high) and the operational-in latch is set by an initial selection sequence. METINA;Q high allows the channel to record time on the meter of the processing unit.

Inbound Scan Control Lines

Select-in and request-in are the inbound scan control lines. Select-in is discussed with the select-out line in CI-2 since it provides a return path to the channel for the select-out line.

The request-in line is activated (REQINA:Q high) to request service from the channel. With the request-in line active, the controller is telling the channel that it will start a signal sequence when it receives the select-out signal. Request-in is normally activated when the PROPSELOUTA/ signal is high (usually because select-out is not active) if suppress-out is not active (SUPOUTA low), the CHANNEL A enable switch is energized (ENBLALTH high), channel B is not selected (CHANBLTH/ high), and one of the following conditions exists: (1) status other than device-end is to be sent to the channel (IG3 and ASEL high), (2) controller end status is to be sent to the channel (IG4 and CUENDA high), (3) the status-in line is active (STATINA/ low), the channel has not yet accepted the status byte (SERVOUTA/ high), and a halt I/O condition does not exist (ER7 low) when the controller sets the poll enable latch (IG4 high), or (4) a gated attention, indication device-end, is received from a disk drive (ATTENTION signal high), a halt I/O condition does not exist (ER7 low), and the controller sets IG4 (IG4 high).

In single-channel controllers, ER7 and CUENDA are not conditions for enabling the request-in line.

When an outstanding device-end status needs to be sent to the channel while the channel suppresses data (SUPOUTA high) during chained command, the microprogram may set IG6 when operational-in is not active (OPINA/ high) to enable the request-in line to be activated (INHSUPINTRP high).

Inbound Interlock Line

Operational-in is the inbound interlock line.

In order to transfer data from the controller to the channel, the operational-in line must be active (OPINA:Q high). Operational-in is a gating condition for the inbound tag lines and for the bus-in lines. This prevents erroneous data from being placed on the tag and bus-in lines when the channel is not selected by the controller.

The operational-in latch is set during an initial selection sequence (INTALSELA/ low) when this controller is selected (select-out is not propagated–PROPSELOUTA/ high) for channel A (CHANALTH/ low) and the microprogram sets the address-in latch (IG7 high) or during an initial selection sequence when a controller error (CONTERR high) is indicated. The operational-in latch is reset by the microprogram when it sets IG1 (ALU1/ low and GATEIG high) When the controller is operating in the test mode (TESTSW/ low) and the MODE SELECT switch is set to SCAN (SCANSW/ low), the operational-in latch is held reset (OPINLTHRST/ low).

In two-channel controllers, the operational-in latch is set by a channel B initial selection sequence in the same manner as for channel A.

When a halt I/O instruction is issued by the channel (ER7 high), the operational-in line is degated.

CHANNEL B INBOUND TAG and CONTROL LINES (CI-8)

The channel B inbound tag and control lines generate the various tag and control signals that identify the type of data being sent to the channel (channel B) or that request service from the channel.

The channel B inbound tag and control lines operate for channel B in the same manner as those for channel A (see CI-7).

The circuits shown on CI-8 are used in two-channel controllers only.

BUS-IN LINES (CI-9)

The bus-in lines consist of nine (eight bits plus parity) lines for each channel. For single-channel controllers, only the channel A bus-in lines are used.

All bus-in line drivers are conditionally gated by the driver degate (DRIVDEGATE/) signal which is high in normal operation. If the DRIVER DEGATE switch is set to ON, DRIVDEGATE/ goes low and inhibits the output of the bus-in lines. The gating for the bus-in lines is also conditionally gated by operational-in (OPINA). OPINA is high when data is to be transferred to the channel only after the channel has selected the controller for operation. The data on the bus-in lines is taken from the DW register and is identified by an associated inbound tag line (address-in, status-in, or service-in).

When the controller is addressed by the channel while the controller is still busy, it replies with a controller busy sequence. This sequence (CUBUSYA/ low) enables the parity bit, bits 1 and 3, and the status-in tag (see CI-7).

SD DECODE (REG-1)

The SD decode circuits, which include the status register (ST) input control logic, control the destination of the ALU bus. The value in the SD field of the ROM word determines the destination of the ALU bus.

The ST input control logic consists of the ENTERST/, SETCARRY, SETSS0-7, and SETSS8-15 signals. The SD field decode circuits include three SD group decode circuits for signals SETSD0-7, SETSD8-15, and SETSD-16-23. The ST input control logic and the SD group decode signals except for SETSD0-7 are enabled by a set enable signal (gate B5, pin 8). SETSD0-7 is enabled by a set enable SD0-7 signal (gate B5, pin 6) that is similar to the set enable signal (gate B5, pin 8). The set enable signal is high during normal or inline mode of operation (TESTSW/ high) when no ALU error exists (ALUERR low) or, if an ALU error exists, parity for the register entered into the A register is not checked (CKPRTY low) and the controller is not inhibited (INHIBITB/ high).

During the test mode of operation (TESTSW/ low), the set enable signal is high if the MODE SELECT switch is not set to SCAN (SCANSW/ high) and no ALU error exists (ALUERR low) or if an ALU error exists, parity for the register entered into the A register is not checked (CKPRTY low) and the controller is not inhibited (INHIBITB/ high). When operating in the test mode of operation (TESTSW/ low) and the MODE SELECT switch is set to SCAN (SCANSW/ low), the set enable signal is high if the SL field of the ROM word equals six (SLEQ6LTH/ low) and no ALU error exists (ALUERR low) or if an ALU error exists, parity for the register entered into the A register is not checked (CKPRTY low) and the controller is not inhibited (INHIBITB/ high).

The conditions which cause the set enable signal to go high also cause the set enable SD0-7 signal to go high but with added requirements. When the SD field is not equal to zero, the set enable SD0-7 signal goes high. When a stop command (SA equal 16) is issued by the ROM because an error is detected during test or inline mode of operation and the MODE SELECT switch is not set to ERR (ERRFZ/ high), the set enable SD0-7 signal goes high to enable the output of the ALU circuits to be entered into the display (DISP) register. When the MODE SELECT switch is set to ERR and the ROM issues a stop command because an error was detected, the two LSB's of the ROM hexadecimal address (the MSB will always be 6) for which the error occurred are entered into the DISP register and frozen there while the controller resident diagnostics are being exercised. When the MODE SELECT switch is set to ERR and the ROM issues a stop command because an error was detected while running the inline diagnostic, an error code is entered and frozen in the DISP register, and no further inline diagnostics can be run.

The set enable and set enable SD0-7 signals go high when the ENTER switch is pressed to either INNER or OUTER (ENTERINLTH/ or ENTEROUTLTH/ low). The ENTERST/ signal allows the content of the ALU bus to be entered into the status (ST) register at T1.5 during test mode of operation when the REGISTER SELECT switch is set to ST (REGSEL1 through REGSEL4 equal 14) and the ENTER switch is pressed to OUTER (ENTEROUTLTH high).

The SETCARRY signal is high when the set enable signal is high at T1.5 to set the carry latch (see ALU-1) and to set ST3 (see REG-8) if a carry out resulting from an add operation is to be stored.

The SETSS0-7/ signal is low when the set enable signal is high at T1.5 while SS0BF is low. The SETSS8-15/ signal is low when the set enable signal is high at T1.5 and SS0BF is high.

The SETSD0-7/, SETSD8-15/, and SETSD16-23/ signals are enabled by various stages of SD0 and SD1 when the set enable signal (set enable SD0-7 for SETSD0-7) is high at T1.5.

During normal and inline mode of operation, the SD field of the ROM word controls the selection of a register to which the ALU bus is routed (see Figure 2-6). During test mode, the initial selection of a register to which the ALU bus is routed is controlled by the REGISTER SELECT switch and the ENTER switch. Subsequent selection of ALU bus destination registers, after the ENTER switch is released, is under the control of the SD field. When the ENTER switch is pressed to either INNER or OUTER (ENTERINLTH/ or ENTEROUTLTH/ signal low), the SD field (SD0BF through SD4BF) is inhibited from controlling register selection; while at the same time, the switch operation allows the value of REGSEL1 through REGSEL4 to determine the register to be selected (SD1 through SD4). The SD0 output is controlled by the enter outer latch (ENTEROUTLTH) or by the enter inner latch (ENTERINLTH). When the ENTER switch is pressed to OUTER, the ENTEROUTLTH/ signal goes low, causing SD0 to go high. When the ENTER switch is pressed to INNER, the ENTERINLTH/ signal goes low, causing SD0 to go low.

Decoding of the SD field is performed by decoder ICs and decode gates. To control the enabling of the decoder ICs and decode gates, the SD0, SD0/, SD1, and SD1/ signals provide three SD group control signals: SD-equals-0-through-7 signal SETSD0-7/, SD-equals-8-through-15 signal SETSD8-15/, and SD-equals-16-through-23 signal SETSD16-23/. These three signals are individually active to enable specific decoder ICs and decode gates. The decoder ICs and decode gates are located on five circuit boards: the four ALU/register boards and the parity board. The ALU boards each contain two bits of each register and thus the decoder ICs for these two bits. Each decoder IC provides up to eight outputs; each output enables two bits of a register selected to receive the ALU bus. Combining four complementary outputs of four decoder ICs will enable all eight bits of a register (e.g., SETDR01/, SETDR23/, SETDR45/, and SETDR67/). The parity bits of some registers have unique decode gating for enabling ALU parity bit (ALUP) entry. These registers are the DR register (SETDRP/), the DW register (SETDWP/), the BX register (SETBXP/), and the CX register (SETCXP/). Unique decode gating is used to enable the entire register plus parity for the GP register (SETGP/), the SP register (SETSP/), and the UR register (SETUR/). Unique decode gating is used to enable the IE register (SETIE/) and the SW register (SETSWREG/); these registers have no parity bit.

During a write operation, an SD decode of 17 (SDXDR high) is used in the IHDR logic (bus-out input direct to DR register—see CI-6) when the microprogram determines that the channel is taking too long to respond with service-out. This bypasses the normal bus-out input to the A bus.

During a read operation, an SD decode of 2 (SDXBY high) is used in the DRBY logic (transfer the contents

FOR INTERNAL USE ONLY

WORD BIT POSITION	47 46 45 44 43	42	41 40 39	38 37	36 35 34 33 32 31 30 29	28 27 26 25 24	23 22 21 20	19 18 17 16 15 14	13 12 11 10	9 8 7 6	5	4 3 2	1	0
FIELD NAME	SA	SV	SC	SB	SK	SD	SS	SN	SH	SL	OM	SP	PA	PC
FIELD BIT POSITION	0 1 2 3 4	0	0 1 2	0 1	0 1 2 3 4 5 6 7	0 1 2 3 4	0 1 2 3	0 1 2 3 4 5	0 1 2 3	0 1 2 3	0	0 - 1 - 2	0	0
BINARY VALUE	16 8 4 2 1		4 2 1	2 1	128 64 32 16 8 4 2 1	16 8 4 2 1	8 4 2 1	32 16 8 4 2 1	8 4 2 1	8 4 2 1	-	4 - 2 - 1	-	-
FUNCTION	A REGISTER SOURCE	ALU CONTROL		B REG SOURCE	B REGISTER SOURCE & ROMAR BITS 9 & 10 SOURCE	ALU BUS DESTINATION	ST REG CONTROL	ROM NEXT ADDRESS	BRANCHING STATMENT FOR ROMAR 2ND LSB	BRANCHING STATMENT FOR ROMAR LSB		SPECIAL CONTROL		

COUNT		A REG SOURCE 0-15	A REG SOURCE 16-31	ALU CONTROL (NOTES 1 & 6)	B REG SOURCE	B REGISTER SOURCE & ROMAR BITS 9 & 10 SOURCE	ALU BUS DEST. 0-15	ALU BUS DEST. 16-31	ST REG CONTROL	ROM NEXT ADDRESS	SH	SL	OM	SPECIAL CONTROL (NOTE 9)	PA	PC
0	16	---	STOP	A+B = D	---		DISP	---			SHO/	SLO/	NOTE 3	---	NOTE 4	NOTE 5
1	17	GL*	DR	A+B+1 ⇒ D	BY		GL	DR	0 ⇒ ST4		SHO	SLO		---		
2	18	BY*	DW*	A·B ⇒ D	SK		BY	DW	0 ⇒ ST1		STO	ST3		FORCE SC		
3	19	FR*	BX	A∨B ⇒ D	DR		FR	BX	1 ⇒ ST1		OP6	ST5		CYL CLK		
4	20	KL*	CX	A+B ⇒ DC			KL	CX	0 ⇒ STO		ST2	ST7		HD CLK		
5	21	DH*	ER	A+B+1 ⇒ DC			DH	FC	1 ⇒ STO		ST4	D = 0		GP ⇒ HD		
6	22	DL*	FS	A+B+C ⇒ DC			DL	FT	0 ⇒ ST5		ST6	A ⇒ ROMAR		RTZ		
7	23	OP*	OA	A ⊕ B ⇒ D			OP	IG	1 ⇒ ST5		FT5	UMSSM (INLINE)		ENAST4		
8	24	GP*	BC	A - B ⇒ D			GP		0 ⇒ ST2		SK ⇒ ROMAR	SERVO				
9	25	SP*	DS	A - B+1 ⇒ D			SP		NOTE 2		CARRY	SORSP				
10	26	UR		A·(-B) ⇒ D			UR		0 ⇒ ST3		COMMO	SELTO				
11	27	IE		A∨(-B) ⇒ D			IE		1 ⇒ ST3		SUPPO	OP1				
12	28	SW		A - B ⇒ DC			SW	CCAR	0 ⇒ ST6		TEST	OP3				
13	29	SC		A - B+1 ⇒ DC				CHD	1 ⇒ ST6		OP0	OP5				
14	30	IH* (BUSOUT)		A - B+C ⇒ DC				CCYL	0 ⇒ ST7		OP2	ST1 (INDEX)				
15	31	IS		A ⊕ (-B) ⇒ D			SSM	CID	1 ⇒ ST7		OP4	OP7				

*REGISTERS CHECKED FOR PARITY

NOTES:

1. SYMBOLOGY:
   - + = ADD
   - - = SUBTRACT
   - · = AND
   - ∨ = OR
   - ⊕ = EXCLUSIVE-OR
   - ⇒ = SET INTO
2. 1 ⇒ ST2 IF ALU BUS IS NON-ZERO.
3. OM IS ACTIVE WHEN A WORD IN AN ODD MODULE IS ADDRESSED.
4. PA IS PARITY BIT FOR ROM ADDRESS OF THE WORD BEING READ.
5. PC IS PARITY BIT FOR ENTIRE WORD BEING READ.
6. A + B + C ⇒ D C
   - A BUS
   - B BUS
   - CARRY IN: C = VALUE OF ST3, 1 = FORCE CARRY
   - D: ALU BUS DESTINATION
   - C: STORE CARRY OUT IN ST3
7. ////////// USED ONLY IN CD14 AND 1015 TWO-CHANNEL CONTROLLERS
8. \\\\\\\\\\ USED ONLY IN 1015 AND 1015A

   (stippled) USED ONLY IN 1015A

Figure 2-6. Read-Only Memory Bit and Field Organization

of the DR register into the BY register—see CI-6) to enable the transfer of data from the DR register to the BY register when the controller is waiting for the channel to accept a byte of data from the DW register and the microprograms find another byte of data available in the DR register.

The SA0 through SA4 latches and the SB0 and SB1 latches store their respective fields of the ROM word so that they are available after the sense amplifier register (ROM-4) is reset.

The ENTER switch logic (ENTERSW high and ENTERSW/ low) causes the content of the DATA switches to be entered into the ALU during inline or test mode of operation. During inline mode of operation, a microprogram instruction (0 → GP) loads the content of the DATA switches into the GP register. The 0 → GP microinstruction is active when the SA field equals zero, the SB field equals zero, and the SD field equals eight (ALU destination is GP) while the spare disk drive is selected (UMSSM high). During test mode of operation, the ENTERSW signal goes high when the ENTER switch is pressed to INNER (ENTERINLTH/ low) or to OUTER (ENTEROUTLTH/ low).

The SB-field-equals-three signal (SBEQ3) is part of a microprogram instruction that disables the bit count advance latch in the bit count appendage circuit (SERDES-4) at the end of the cyclic code check byte.

DISP, GL, AND BY REGISTERS (REG-2)

The input data to the display (DISP), gap length (GL), and BY (general use) registers is from the ALU bus. Refer to Figure 2-6 for ALU bus destination (SD field).

The DISP register is used strictly with the REGISTER DISPLAY indicators. The DISP register displays the routine code of an inline diagnostic routine in the REGISTER DISPLAY indicators when the MODE SELECT switch is set to RTN (routine). An error code is displayed if an error occurs during ERR (error) or RSLT (result) mode.

The outputs of the GL and BY registers are routed to the A bus when they are selected. The output of the BY register may also be gated into the B bus when the SB field equals one.

FR, KL, AND DH REGISTERS (REG-3)

The input data to the flag register (FR) and to the key length (KL) and data length high (DH) registers is from the ALU bus. Refer to Figure 2-6 for ALU bus destination (SD field). The outputs of the FR, KL, and DH registers are routed to the A bus when they are selected.

DL AND OP REGISTERS (REG-4)

The input data to the data length low (DL) and operation code (OP) registers is from the ALU bus. Refer to Figure 2-6 for ALU bus destination (SD field). The outputs of the DL and OP registers are routed to the A bus when they are selected. The OP register also has outputs to the two LSBs of the ROM address register where they are used for microprogramming control.

GP, SP, AND UR REGISTERS (REG-5)

The input data to the GP (general purpose), seek-in process (SP), and unit address (UR) registers is from the ALU bus. Refer to Figure 2-6 for ALU bus destination (SD field). The outputs of the GP, SP, and UR registers are routed to the A bus where they are selected by specific microprogram instructions (SA field).

In the SP register, each bit reflects the seek status of one disk drive. Whenever a seek is initiated which requires access motion, the bit in the SP register representing the addressed disk drive is turned on. A subsequent gated attention from this disk drive causes the controller to be selected, and device-end status is presented to the channel. The microprogram senses that the gated attention was caused by a seek command because the respective bit in the SP register is high. In two-channel controllers, the SP register is not used; the SW register is used in its place.

Outputs of the UR register (UR4 through UR7) are used to select a disk drive for operation (see DDI-2). In two-channel controllers, the UR4 through UR7 outputs of the UR register are used by the SW registers (see CI-4) to determine the SW register to be used to store reserve and device-end status. There are eight SW registers, one for each disk drive.

DR AND DW REGISTERS (REG-6)

The data read (DR) register has inputs from the ALU bus, the file data register (FDR), and the bus-out lines. Transfer of data from the ALU bus to the DR register is under control of the microprogram (see SD field—Figure 2-6). Data transfer from the FDR to the DR register during a read operation is not under microprogram control, but is transferred when the FDR is full (eight bits). This transfer is controlled by the high GATEFDR signal and the low FDRXDR/ signal (see SERDES-2). The low FDRXDR/ signal also causes ST register bit 4 to be set (SETST4/ low), which, in turn, tells the microprogram of the transfer and that the DR register is full. The contents of the DR register must be transferred within 3.2 microseconds; otherwise, a new byte of data from the FDR will destroy the original byte in the DR register. Bus-out data (BUSOUTP and BUSOUT0 through BUSOUT7) is transferred to the DR register during a write operation if, while waiting for the channel to respond with a service-out, the microprogram determines that channel response is taking too long; it may enable the speed-up logic (IHDR high), which allows the bus-out data to be entered directly into the DR register rather than through the A bus. The high IHDR signal controls the entry of the bus-out data into the DR register.

The outputs of the DR register are transferred to the A bus, to the B bus, or to the FDR during a write operation. The transfer of data from the DR register to the A bus and to the B bus is under microprogram control. The transfer of data to the FDR is not under microprogram control but under control of the write gate and phase counter (see SERDES-3). When the FDR is empty, a new byte of data will be transferred from the DR register. This transfer action also causes ST4 to set, which, in turn, tells the microprogram of the transfer. If the microprogram does not cause the DR register to be loaded with a new byte of data within 3.2 microseconds, the original byte of data will again be transferred to the FDR and written on the disk pack again.

Inputs to the data write (DW) register are from the ALU bus and from the BY register. Transfer of data from the ALU bus to the DW register is under microprogram control (SD field–see Figure 2-6). Data transfer from the BY register to the DW register is also under microprogram control. If, during a read operation, the controller is waiting for the channel to accept a byte of data from the DW register and the microprogram finds another byte of data available in the DR register, it may enable the speed-up logic by supplying a microinstruction which causes the byte in the DR register to be transferred to the BY register through the A bus, the A register, and the ALU bus so that the DR register can accept another byte of data from the FDR. After the original byte of data in the DW register has been accepted by the channel, the byte that was transferred to the BY register is transferred directly to the DW register under control of the low GATEBY/ signal.

The outputs of the DW register are routed to the A bus under microprogram control and to the bus-in lines under control of the operational-in signal.

BX AND CX REGISTERS (REG-7)

The BX and CX registers are used in burst check operation. The burst check operation is performed independently of the microprogram; however, the microprogram controls the start and end of burst check operations. The microprogram sets the BX and CX registers to all ones (ALU input controlled by SETBX01/ through SETBX67/ and SETCX01/ through SETCX67/ respectively) before the start of burst check operation (BSTCHK/ high). During burst check operations, the output of the BX and CX registers alternately is exclusive-ORed with the output of the FDR (see SERDES-4). The result of the exclusive-ORing is reentered into the same register (BX or CX) under control of the SETBX/ or SETCX/ signals. Also during burst check operation, the BXTCHK/ signal is low to inhibit any entry into the BX or CX register from the ALU bus. At the end of a read operation, as determined by the microprogram, the two burst check bytes at the end of a record are exclusive-ORed with the residue in the BX and CX registers. The result of the exclusive-ORing should be all zeros. At the end of a write operation (again determined by the microprogram), the residue in the BX and CX registers is written on the disk pack (BX first) as the two burst check bytes.

ST REGISTER (REG-8)

The status (ST) register contains eight bits and is used by the microprogram for branching control. Individual bits of the ST register may be set or reset, under microprogram control, to indicate conditions within the controller. When the microprogram causes a bit to be set or reset, it may later branch to the routine determined by the condition of the status bit.

Several ST register bits have specific meanings, while the others may be used by the microprogram to indicate different meanings for different operations. ST0 is set and reset under microprogram control. ST0 is set when the SS field equals five and reset when the SS field equals four. ST1 is enabled to be set when the SS field equals three. The index pulse (CIDX high) actually causes ST1 to set. ST1 is reset when the SS field equals two. ST2 is enabled to be set when the SS field equals nine. ST2 is actually set when the ALU bus is not equal to zero. ST2 is reset when the SS field equals eight. ST3 is set under microprogram control (SS equals eleven) when a forced carry is required. ST3 is also set when a carry-out bit (COA and COB high) that results from an arithmetic add operation is to be stored (SC field equals four, five, or six). ST3 is reset by the microprogram or by a zero carry-out (COA or COB low) that results from an arithmetic add operation. ST4 is set only by serializer/deserializer operation (SETST4/ low). During a read operation, ST4 is set when a byte of data from the disk drive has been deserialized and transferred to the DR register.

During a write operation, ST4 is set when a byte of data to be written has been transferred from the DR register to the FDR for serialization. ST4 is reset by the microprogram when the SS field equals one. ST5 and ST6 are set and reset by the microprogram. ST5 is set and reset when the SS field equals seven and six respectively, and ST6 is set and reset when the SS field equals 13 and 12 respectively. ST7 is set and reset by the microprogram when the SS field equals 15 and 14 respectively. ST7 is also set by a selective reset condition (SELSET-ST7 low).

In test mode of operation, the contents of the ALU bus may be entered into the ST register when the REGISTER SELECT switch is set to ST and the ENTER switch is pressed to OUTER (ENTERST/ low). This is done to test the operation of the ST register.

TIMING COUNTER (TIM-1)

The timing counter consists of two oscillators and a five-bit, free-running counter.

The 8 MHz oscillator is crystal controlled and controls the operation of the timing counter. The output of

oscillator circuit Q4, Q5, Y2 is adjusted for symmetry by potentiometer R22. Potentiometer R22 determines the voltage level at which squaring circuit Q6 will turn on and off. The output of Q6 is applied to a gate which repowers the signal to the system logic levels.

The counter (TA through TD and TB.5) is a five-bit free-running ring counter that produces five discrete machine timing signals–T0, T1, T1.5, T2, and T3. The gating decodes the five discrete timing signals which are each 62.5 nanoseconds in duration. The spacing between T0, T1, T2, and T3 is 62.5 nanoseconds. Timing signal T1.5 is a half-step signal which occurs during the interval between T1 and T2.

CHANNEL RESET CONTROL (TIM-2)

In a two-channel controller, a general reset can be initiated by either channel at any time that the controller is not selected by the other channel. A general reset causes all reservations and status conditions stored in the controller that are related to the resetting channel to be reset. A selective reset has no effect on device reservations or status.

General Reset

The channel can cause a general reset of all online controllers by dropping operational-out and by maintaining suppress-out in a low state. In the controller, this is mechanized in the GATEGENRSTA logic. High signals OPOUTA/, SUPPOUTA/, and ENBLALTH/ cause GATEGENRSTA to go high. When GATEGENRSTA remains high for more than 4 microseconds (4 to 6 microseconds depending on the setting of pulse width adjustment potentiometer R24), pulse width one-shot Q7-Q12 will fire, causing GENRSTOSA to go high. GENRSTOSA will remain high until 600 nanoseconds after GATEGENRSTA goes low, which is caused by OPOUTA/ going low. The GENRSTOSA signal is an input to the GENRST logic. During the 600 nanoseconds after GATEGENRSTA goes low, OPOUTA will be high. With the CHANALTH signal high (CI-2), the CHANNEL A enable switch engages (ENABLEA high), GENRSTOSA high, and OPOUTA high; GENRST will go high and cause MACHRST and PROCRST signals (TIM-3) to go high, thereby providing a general reset to the controller.

GENRSTOSA also controls the following logic: RSTCLKA/, RSTCONTCHA/, RSTCHANA/, and RSTCHALTH/. RSTCLKA/ is enabled (goes low) when GENRSTOSA goes high or SETCHANRST/ goes low at T2 time. When RSTCLKA/ goes low, all SW registers (CI-4) associated with channel A are enabled for reset.

RSTCONTCHA/ is enabled (goes low) when GENRSTOSA goes high and sets the RSTCONTCHA/ latch. The low RSTCONTCHA/ signal resets the controller busy logic (CUENDA–CI-7).

RSTCHANA/ is enabled (goes high) when RSTCONTCHA/ goes low. With RSTCHANA/ high and RSTCLKA/ low, the SW registers (CI-4) associated with channel A are reset, causing all reserve status to be cancelled. RSTCHANA/ goes low (after a general reset) when the microprogram, after performing housekeeping microinstructions, activates the poll enable latch (IG4).

RSTCHALTH/ is the negated GENRSTOSA term that causes CHANALTH to set if channel B has not selected the controller (CI-2). In single-channel controllers, the RSTCHALTH/ term has no effect on CHANALTH. RSTCHALTH/ low also causes request-in (REQINA) to drop during a general reset (CI-7).

Selective Reset

Either channel can issue a selective reset by raising suppress-out and dropping operational-out. A selective reset occurs only as a result of a malfunction detected at the channel or a time-out by the channel.

Enable Latch

The enable latch for channel A operation (ENBLALTH) controls the ability of the controller to operate on commands from channel A. ENBLALTH is set when clock-out from channel A (CLKOUTA) is high, machine reset (MACHRST;1) is low, and the CHANNEL A switch on the face of the controller is energized (ENABLEA high). The only time that ENBLALTH can change state is when CLKOUTA goes low. This allows the channel to remain connected to the controller until the CPU goes to a halt or a wait condition. ENBLALTH is reset when channel A is not selected (GATEDASEL/ high), CLKOUTA is low, and the CHANNEL A switch is disengaged. ENBLALTH is also reset during the controller power-up sequence (LOGICSTART low). RC network R8, R9, and C10 in the ENBLALTH circuitry provides a time delay (approximately one millisecond) that allows the select-out relay in the channel interface (CI-2) to be energized before any outstanding status or gated attention is processed. The select-out relay is energized when INTFDSBLA;W goes low.

In single-channel controllers, the INTERFACE DISABLE indicator on the test panel is lit when ENBLALTH is reset (INTFDSBLA low). In two-channel controllers, the INTERFACE DISABLE indicator is lit only when both ENBLALTH and ENBLBLTH are reset (INTFDSBLA/ and INTFDSBLB/ low).

The general reset, selective reset, and enable latch circuits for channel B operate in a manner identical to that for channel A.

COMMON RESET CONTROL (TIM-3)

The common reset control circuits generate inhibit and reset signals.

The INHIBITA signal is activated (goes high) by many conditions. When the CHK STOP/RUN/SINGLE STEP STOP switch on the test panel is set to SINGLE STEP STOP, the INHIBITA latch is set at T1 each time the START switch is pressed during single-step test operation. During a machine reset (MACHRST;1 high), the INHIBIT latch is set. When the controller is operating in the normal or inline mode (TESTSW/ high), the INHIBITA latch is set at T3 by a sense amplifier register parity error (SARERR/ low), a read-only memory address parity error (RADERR/ low), or an A register parity error (ER4 high) when the INHIBITB latch is not set (INHIBITB/ high). When the controller is operating in the test mode and the CHK STOP/RUN/SINGLE STEP STOP switch is set to CHK STOP (CKSTPSW/ low), the INHIBITA latch is set at T3 by an A register parity error (ER4 high), a serial data parity error (ER0 high), a bus-out parity error (ER2 high), probe latch (PRBLTH/ low when test connections have been connected to the probe latch–see TEST-3), a machine stop instruction from the ROM (SA field equals 16), a sense amplifier register parity error (SARERR/ low), or a ROMAR parity error (RADERR/ low).

With the MODE SELECT switch on the test panel set to STOP while the controller is operating in the test mode (TESTSW/ low), INHIBITA latch will set at T3 when the address of the ROM matches the setting of the STOP ADDRESS switches on the test panel (STPEQ high).

The INHIBITA latch is reset in the following two ways. After a machine reset (MACHRST;1 goes high) that is caused by a general reset or a selective reset, the two latches (gates C10, C9 and C10, C10) in the INHIBITA latch reset logic are set and reset respectively. These two latches, respectively, place a high and a low signal at the input to gate C11. After MACHRST;1 goes low, the high PROCRST signal (PROCRST latch also set by a general reset or a selective reset) at T1 will set latch C10, C10. Latch C10, C10 set and latch C10, C9, which was set by MACHRST;1, will cause INHIBITA latch to reset at T2. The PROCRST latch will reset at T0 after the INHIBITA latch is reset. The second method by which the INHIBITA latch is reset is employed when the controller is in the test mode of operation. During test mode, an operation is initiated by the START switch on the test panel. When this switch is pressed, STARTSW/ goes low and resets latch C10, C9, which, in turn, sets latch C10, C10. When the START switch is released, STARTSW goes low and sets latch C10, C9. With both latches set, the INHIBITA latch is reset at T2. After the INHIBITA latch is reset (INHIBITA/ high), latch C10, C10 is reset at T0.

The INHIBITB flip-flop is clocked by T0 and follows the state of the INHIBITA latch. The INHIBITB flip-flop is used during single-step test operation to ensure that only one step in the operation occurs each time the START switch is pressed. In single-step operation, the INHIBITB flip-flop follows the INHIBITA latch by approximately 375 nanoseconds when INHIBITA sets and by approximately 250 nanoseconds when it resets.

The SETSTART/ signal is activated (goes low) only when the controller is in a stop condition (INHIBITA high) and the SET ADDRESS switch on the test panel has been pressed. When SETSTART/ is low, the ROM starts its program at the ROM address set into the START ADDRESS switches (see ROM-1).

The INDEXENBL signal goes high at T0 (both TA and OSC/ high) when the controller is not stopped (INHIBITA/ high). The INDEXENBL latch is reset at T2 (T2/ low). INDEXENBL is the initiate signal for the ROM read cycle.

The SYNCHUB signal is activated (goes low) when INDEXENBL goes high and the ROM address matches the setting of the STOP ADDRESS switch (STPEQ high).

The INHIE1/ and ERRFZ/ signals are logically identical and become active (go low) when the microprogram issues a stop instruction (SA field equals 16) and the destination of the ALU bus is the GP, SP, UR, or IE registers (SD1 high). The ERRFZ latch is reset by a machine reset when the CHECK RESET switch is pressed (CKRSTSW/ low) while the MODE SELECT switch is in the ERR position. When the MODE SELECT switch is in any position other than ERR, the ERRFZ latch has a continuous reset (ERRSW/ high).

A selective reset is issued by a channel by raising suppress-out and dropping operational-out. Only the controller presently operating with the channel is reset. The channel must activate suppress-out at least 250 nanoseconds prior to dropping operational-out and must hold suppress-out active until at least 250 nanoseconds after operational-out has been activated again. If operational-in (OPINA or OPINB) is high when suppress-out (SUPOUTA+B) is high and operational-out is low (SETSRSTA or SETRSTB high), all registers will be reset.

The channel can issue a general reset by dropping operational-out and not raising suppress-out. A general reset resets all registers and causes the microprogram to restart at address 000.

The selective reset (SELRST) or general reset (GENRST) will reset the logic in the controller (MACHRST high) when the controller is not in test mode (TESTSW/ high) or in test mode (TESTSW/ low) with the CHK STOP/ RUN/SINGLE STEP STOP switch not set to CHK STOP (CKSTPSW/ high). During the power-up sequence, the low LOGICSTART signal holds the MACHRST signal high until the power-up sequence is complete; LOGIC-START then goes high.

The SELRST/ and GENRST/ signals also cause the processor reset latch to set (PROCRST signal high). The

PROCRST signal is used in conjunction with the MACHRST signal to reset the inhibit latches.

The high SELRST and MACHRST signals cause the SELSETST7 latch to set (SELSETST7/ signal low), which, in turn, sets status register bit 7 (ST7). Setting ST7 latch inhibits the normal reset of all outstanding device-end status stored in attention latches in each disk drive.

MACHINE STATUS (STAT-1)

The machine status function supplies condition data pertaining to the operation in progress or just completed to other functions of the controller. The machine status function consists of the inline execution (IE) register/gates, the error register (ER), and interface status (IS) gates.

IE Register/Gates

When inline diagnostic routines are run in either test or inline operation, the IE register keeps track of the position within the specific inline routine. IE0 (RUTNLD high) indicates that the MODE SELECT switch is set either to RTN (RUTNSW/ low) or LOAD (LDSW/ low). IE1 (ERRLDRSLT high) indicates that the MODE SELECT switch is set to ERR (ERRSW/ low), RSLT (RSLTSW/ low), or LOAD (LDSW/ low). IE2 is not used. IE3 through IE5 form a code (345 code) that controls the sequence of operation within the inline routine. IE6 indicates routine chaining. During inline or test operations when inline diagnostic routines are to be performed, the 345 code and chaining bits are loaded when the SD field of the ROM equals 11 (SETIE/ low). The 345 code is stored in IE3 through IE6 until it is entered into the A bus prior to the next step of the routine (SA field equals 11). The 345 code is routed through the A register and gated into the OP register just prior to the start of each step in the routine. The 345 code is then decoded to determine which function is to be performed. IE7 receives its input from the file tog register (FT7–module select) and is applied directly to A bus 7 (ALU-4(2)).

ER Register

The ER register stores conditions that occur during an operation. ER0 time indicates that a serial data error has occurred in the serializer/deserializer (SERDES) during a write operation. ER0 is set by SETERR0 low when the controller is not in a halt I/O condition (ER7/ high). SETERR0/ goes low when a write data parity error occurs on a command or data byte. ER1 gates an address-out (either GTDADDOUTA or GTDADDOUTB in a two-channel controller) to the A bus for testing by the microprogram. ER2 is set when a bus-out parity error occurs. ER2 is set when EVENPRTYA (EVENPRTYA or EVENPRTYB for two-channel controllers) is high and the normal routing of the bus-out data occurs at T3 (SAXIH high–SA field of the ROM=14). ER2 is set at T2 if a bus-out parity error occurs when the speed-up logic enables the bus-out data to be entered directly into the DR register (IHDR high–SA field equals 25, SD field equals 17). The bus-out parity error is cleared (ER2 reset) either by pressing the CHECK RESET switch on the test panel (CKRSTSW/ low) or by the microprogram (OPINLTHRST/ low). ER3 is active during the short control unit busy sequence (CUENDA high). ER4 latch is set by an A register parity error (ALUERR high). Parity is checked (decode parity high) on the GL, BY, FR, KL, DH, DL, OP, GP, and SP registers, the bus-out data lines, and the DW register (SA field equals 1 through 9, 14, and 18 respectively) when in the normal mode of operation (INLINE/ high), there is no command or data bus-out parity error (ER2/ high) and there is no halt I/O condition (ER7/ high). The ER4 latch is reset in the same manner as the ER2 latch. ER5 is not used. In two-channel controllers, ER6 is active (high) when channel B is communicating with the controller (CHANBLTH/ low). ER7 latch is set by a halt I/O instruction from the channel. The halt I/O instruction causes the controller to release the channel immediately, thus stopping data transfer. The operation in progress when the halt I/O instruction was given will continue to completion. ER7 latch is set in the following manner. With an operation in progress, operational-in is up (OPINA high; OPINA or OPINB high in two-channel controllers). To initiate the halt I/O instruction, the channel drops select-out (INTALSELA/ and INTALSELB/ high) and raises address-out (ER1 high–GTDADDOUTA/ or GTDADDOUTB/ low). The combination of high operational-in, low select-out, and high address-out causes ER7 to set. ER7 latch is also set when the microprogram turns on the status-in latch (IG5 high) while operational-in is low for channels A and B (OPINA and OPINB low). When ER7 is high, the command-out latch (COMMO high–see CI-2) is forced on so that the microprogram can branch on it. This condition indicates a halt I/O to the microprogram and will reset ER7 latch by dropping operational-in (OPINLTH/ low).

IS Gates

The IS gates supply the address of the controller and information about the selected disk drive. IS0 through IS3 (CUADD0 through CUADD3) provides the mixed address of the controller (channel A is used for single-channel controllers) to the A bus (SA field of the ROM equals 15) and is placed on the bus-in lines when the address-in tag is high. IS4 through IS7 are used within the controller to identify the status of a disk drive. IS4 through IS7 are also entered into the A bus when the SA field of the ROM equals 15. IS4, when active, identifies disk drive A as being selected (CMSA high–see ALU-2(2)). IS5 (BIT50P), when active, indicates that the disk drive selected for an operation is not busy (CBSY low), has not indicated a seek incomplete (CSIN low), is not at the end of a cylinder (CEOC low) or does not indicate an unsafe condition (CUSF low), and is online (COL high). IS6, when high, indicates that a request

for service has been received from the spare disk drive (CGASM high). IS6 is applied directly from the disk drive interface function to the A bus (see ALU-2(2)). IS7, when high, indicates that a request for service has been received from one of the eight online disk drives (ATTCU high). IS7 is applied to the A bus from the disk drive interface function through the channel interface function (see ALU-2(2)).

ALU CONTROL (ALU-1)

The ALU control circuits determine the arithmetic operation to be performed by the ALU, control the A bus source for either normal or test mode of operation, and decode the SB field of the sense amplifier register (SAR) output. Refer to Figure 2-7 for ALU and ROM timing relationship.

The value contained in the SC field of the ROM word determines the operation to be performed by the ALU. The SC field defines the eight different operations that are performed by the ALU. In conjunction with the SV bit of the ROM word, 16 different operations are performed by the ALU.

As shown in Figure 2-6, an ADD operation is performed when the SC field equals 0, 1, 4, 5, or 6; an AND operation when the SC field equals 2; an OR operation when the SC field equals 3; a carry-in operation when the SC field equals 1, 5, or 6; and an exclusive-OR operation when the SC field equals 7.

The ADD;A and ADD;B signals are high when an add operation is to be performed (SC=0, 1, 4, 5, or 6). The AND/;A and AND/;B signals are low when an ANDing operation is to be performed (SC=2). The OR/ signal is low when an ORing operation is to be performed (SC=3). The AND+ADD signal is high when an ANDing or adding operation is to be performed (SC=0, 1, 2, 4, 5, or 6). The CIN and CIN/ signals are high and low respectively when a carry-in operation is to be performed (SC=1, 5, or 6). Although the carry-in latch may be set for SC counts of 2, 3, or 7, it has no meaning for these counts because the computational circuits (ALU-4(1) and ALU-4(2)) do not allow a carry-in for SC counts of 2, 3, or 7. For an SC count of 6, the value of ST3 determines whether a carry-in operation is to be performed. If ST3 is high when SC equals 6, a carry-in bit is routed to the LSB of the ALU (ALU bit 7). If ST3 is low when SC equals 6, no carry-in operation is performed. An exclusive-OR function is performed when SC equals 7. Decoding is not actually mechanized for SC equals 7; however, the absence of decoding of any other SC field allows an exclusive-OR operation.

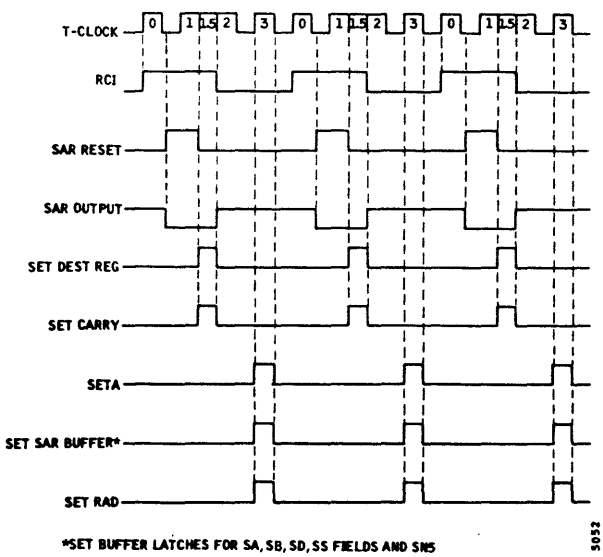


Figure 2-7. ALU Timing

When the SV bit of the ROM word is high, the B register input to the ALU is in complemented form; therefore, all arithmetic operations are performed with the complemented form of the B register output.

The ADD latch, the AND latch, the OR latch, the AND+ADD latch, and the carry-in latch are clocked when the SETA/ signal goes low. The SETA/ signal goes low at T3 when the controller is not inhibited (INHIBITB/ high) and no parity errors exist.

The DEQ0 and CARRY signals are the result of arithmetic operations that are tested by the microprogram to determine branching conditions.

The input to the A bus is normally controlled by the SA field of the ROM word. The SA gating allows the inputs to the A bus to be controlled from the test panel during the test mode of operation as well as by the ROM during the normal or inline mode of operation.

In the normal or inline mode of operation, the DISPINSW/ and DISPOUTSW/ signals are high and, thereby, inhibit the REGSEL1 through REGSEL4 signals from having any effect on the selection of register input to the A bus, but, at the same time, allow the SA0BF through SA4BF signals from the SAR to control the register entry to the A bus.

In the test mode of operation, when the DISPLAY switch on the test panel is pressed to INNER or OUTER, The REGSEL1 through REGSEL4 signals control the register selection input to the A bus. When the DISPLAY switch is pressed to INNER (DISPINSW/ low), the SA0 output will be low. The SA0 output signal will be high during test mode only when the DISPOUTSW/ signal is low, which represents an SA count of 16 through 31.

Decoding of the SB field (B bus source) of the ROM word provides three outputs: SB equals one (SBEQ1, SB equals two (SBEQ2), and SB equals three (SBEQ3).

A BUS and A REGISTER (ALU-2(1) and ALU-2(2))

The value contained in the SA field of the ROM word determines a particular input to the A bus. Figure 2-6 illustrates the A bus/A register source for each SA count. The A register is clocked by the SETA/ signal. SETA/ goes low at T3 if the controller operation is not inhibited (INHIBITB/ high) and no parity error (A register parity, SAR parity, or ROMAD parity error) is present.

Inputs to each A bus bit are multiplexed by three multiplexer integrated circuit (IC) assemblies. Selection of an input to a multiplexer IC is controlled by the selected inputs (S0 through S2) and the enable (E) input. The binary value of the S0 through S2 inputs (S2 is the MSB) determines the input to be gated through the multiplexer IC when the E input is low. For example, when SA equals 14, the BUSOUT bit is gated through the multiplexer (SA0 low, SA1 high, SA2 high, SA3 high, SA4 low). The DSBC input is applied to the A bus when SA equals 24 or 25. When SA equals 24, the bit count (BC) accumulated during a read or write operation is entered into the A bus. When SA equals 25, the disk drive that has been selected for a read or write operation is identified by entering a bit into the A bus. Disk drives B through J are identified by entering a bit into A bus 0 through A bus 7 respectively.

Register parity bits are multiplexed by three multiplexer IC assemblies in the same manner as the inputs to the A bus (see ALU-2(2)). The display parity bit (DISPP/) signal is used only during the test mode of operation. The register parity bit that is displayed on the REGISTER DISPLAY P indicator (see TEST-2) is determined by the binary value of the select and enable inputs (SA0 through SA4) to the multiplexer ICs. During the test mode of operation, the DISP1X through DISP3X signals are high for any parity bit applied to the multiplexer ICs when the DISPLAY switch is pressed to INNER or OUTER. When a parity bit is high and the above conditions are met, the DISPP/ signal is low and the REGISTER DISPLAY P indicator is lit. When the parity bit is low, the DISPP/ signal goes high and the REGISTER DISPLAY P indicator is not lit.

When the A register parity bit is to be displayed during the test mode of operation, the parity bit of the A bus input register is multiplexed through one of the three multiplexer ICs and stored in a latch if data is stored in the A register (SETA/ time). The "1" output of the latch is ANDed with DISP1X, DISP2X/, and DISP3X/ (octal count of 001). The octal count of 001 allows the A register (and the parity bit) to be displayed on the DISPLAY REGISTER indicators (see TEST-2). The "0" output of the parity latch is compared to the parity of the A register data. If the number of high bit inputs to the parity IC is even, the parity latch should be set; otherwise, an ALU parity error (ALUERR high) will be generated. Conversely, if the number of high bit inputs to the parity IC is odd, the parity latch should be reset; otherwise, an ALU parity error is generated.

B BUS and B REGISTER (ALU-3)

The value contained in the SB field of the ROM word determines a particular input to the B bus. The B bus has three input sources: BY register when SB equals one, SK field of the ROM word when SB equals two, and DR register when SB equals three. When selected, each input is routed to the B register in true form when the SV bit of the ROM word is low. When the SV bit is high, the selected input is routed to the B register in one's complement form. The one's complement output of the B register is used during a subtraction (complement + add) operation. The B register is clocked by SETA/, which is low at T3 when the controller operation is not inhibited (INHIBITB/ high) and there are no errors in A register parity, SAR parity, and ROMAR parity.

ARITHMETIC LOGIC UNIT (ALU-4(1) and ALU-4(2))

The arithmetic logic unit (ALU) performs the add, subtract, AND, OR, and exclusive-OR operations within the controller. The ALU also generates odd parity from the data that passes through it. Inputs to the ALU are from the A register, the B register, the carry-in latch, and the test panel.

As discussed in the ALU control circuit (ALU-1) description, the ALU performs the following operations: add with no carry-in and no carry-out to ST3, add with carry-in and no carry-out to ST3, add with no carry-in and carry-out to ST3, add with carry-in of the state of ST3 and carry-out, AND, OR, and exclusive-OR.

Add Operation

All add operations are basically identical; the only difference is the addition of the carry-in bit. In order to better explain the operation of the ALU, several examples of add operations are given. In these examples, one-digit numbers are used to illustrate the principle of the add operation. By using these examples, the addition of two eight-digit numbers can be followed. Figure 2-8 illustrates the interconnections between two bits of the ALU (bits 6 and 7). During the normal mode of operation, only those gates that are numbered are effectively in the circuit. These numbered gates also correspond to the numbered gates shown in Figure 2-9, which is used in conjunction with the following examples.

When the SC field of the ROM word equals 4, 5, or 6, the carry-out from the MSB (COA and COB), if any, is stored in ST3 (see REG-8) and also in the carry latch (ALU-1) where it is used by the microprogram for branching.

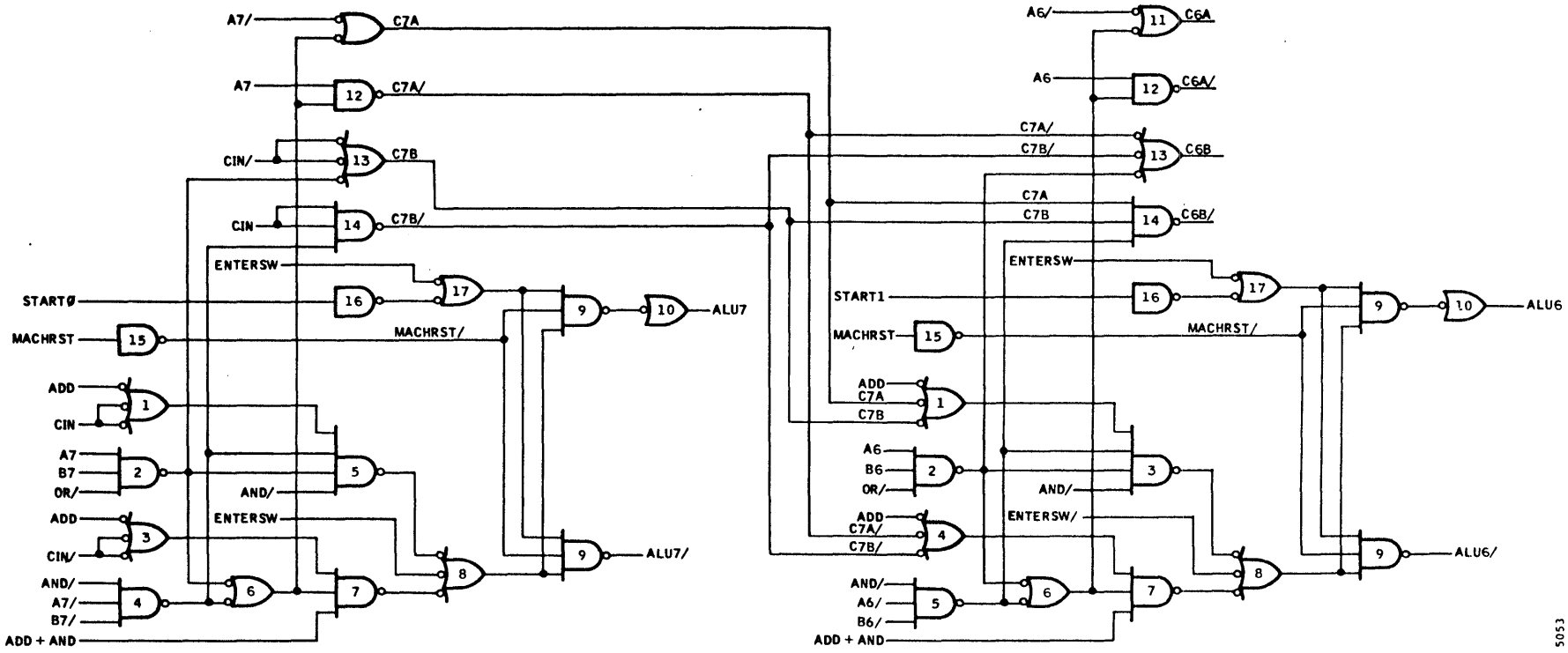


Figure 2-8. ALU Bit Interconnection

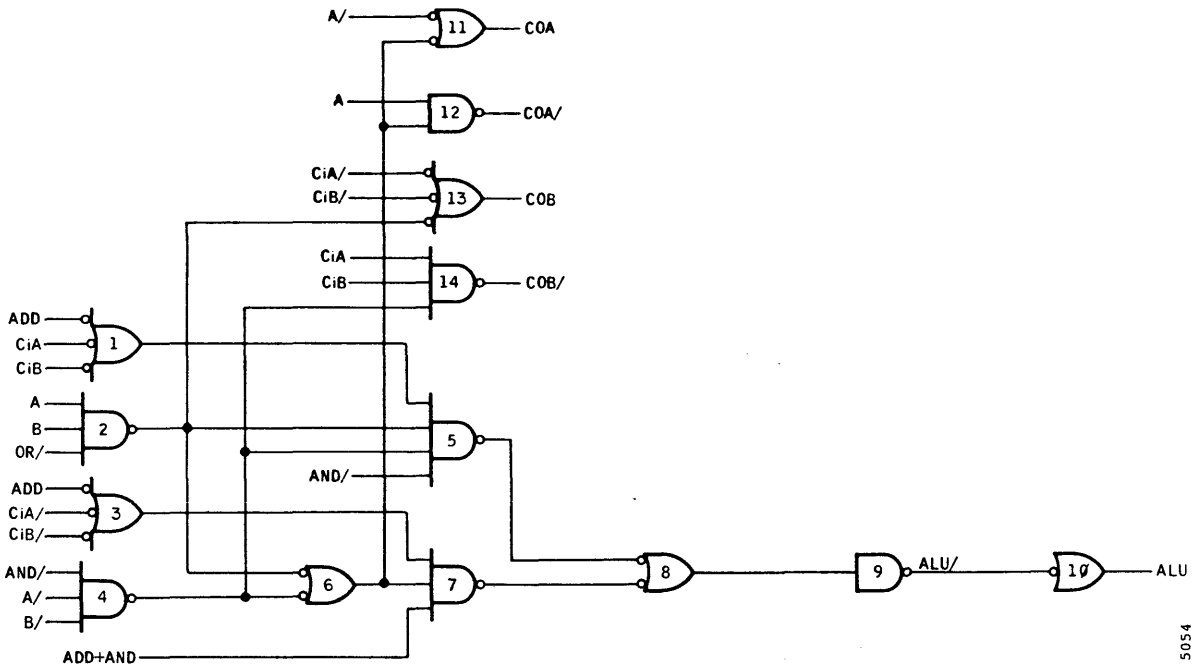


Figure 2-9. Simplified ALU Bit

- **Example 1.** Add two zeros with no carry-in.
  A = 0
  B = 0
  CIN = 0

Gate	Gate Output	Cause
1	High	CiA or CiB low (no carry-in)
2	High	A or B low
3	Low	CiA/, CiB/, and ADD high
4	Low	AND/, A/, and B/ high
5	High	Gate 4 low
6	High	Gate 4 low
7	High	Gate 3 low
8/10	Low (ALU)	Gates 5 and 7 high
9	High (ALU/)	Gate 8 low
11	High	Gate 6 low (has no effect on carry-out, as gate 13 is low)
12	High	A low
13	Low	CiA/, CiB/, and gate 2 high
14	High	CiA, CiB, or gate 4 low

- **Example 2.** Add a one and a zero with no carry-in.
  A = 1
  B = 0
  CIN = 0

Gate	Gate Output	Cause
1	High	CiA or CiB low
2	High	B low
3	Low	ADD, CiA/, and CiB/ high
4	High	A/ low
5	Low	Gates 1, 2, and 4, and AND/ high
6	Low	Gates 2 and 4 high
7	High	Gate 3 or gate 6 low
8/10	High (ALU)	Gate 5 low
9	Low (ALU/)	Gate 8 high
11	High	A/ or gate 6 low (has no effect on carry-out, as gate 13 is low)
12	High	Gate 6 low
13	Low	CiA/, CiB/, and gate 2 high
14	High	CiA or CiB low

- **Example 3.** Add two one's with no carry-in.
  A = 1
  B = 1
  CIN = 0

Gate	Gate Output	Cause
1	High	CiA or CiB low (no carry-in)
2	Low	A, B, and OR/ high
3	Low	ADD, CiA/, and CiB/ high
4	High	A/ or B/ low
5	High	Gate 2 low
6	High	Gate 2 low
7	High	Gate 3 low
8/10	Low (ALU)	Gates 5 and 7 high
9	High (ALU/)	Gate 8 low
11	High	A/ low
12	Low	A and gate 6 high (gate 12, COA, low is carry-out to next bit)
13	High	Gate 2 low
14	High	CiA or CiB high

- **Example 4.** Add two zeros with a carry-in.
  A = 0
  B = 0
  CIN = 1 (CiA and CiB are high, and CiA/ or CiB/ is low)

Gate	Gate Output	Cause
1	Low	ADD, CiA, and CiB high
2	High	A or B low
3	High	CiA/ or CiB/ low
4	Low	AND/, A/, and B/ high
5	High	Gate 1 or gate 4 low
6	High	Gate 4 low
7	Low	Gate 3, gate 6, and ADD+AND high
8/10	High (ALU)	Gate 7 low
9	Low (ALU/)	Gate 8 high
11	Low	A/ and gate 6 high
12	High	A low
13	High	CiA/ or CiB/ low
14	High	Gate 4 low

- **Example 5.** Add a one and a zero with a carry-in.
  A = 1
  B = 0
  CIN = 1 (CiA and CiB are high, and CiA/ or CiB/ is low)

Gate	Gate Output	Cause
1	Low	ADD, CiA, CiB high
2	High	B low
3	High	CiA/ or CiB/ low
4	High	A/ low
5	High	Gate 1 high
6	Low	Gates 2 and 4 high
7	High	Gate 6 low
8/10	Low (ALU)	Gates 5 and 7 high
9	High (ALU/)	Gate 8 low
11	High	A/ or gate 6 low
12	High	Gate 6 low
13	High	CiA/ or CiB/ low
14	Low	CiA, CiB, and gate 4 high (gate 14, COB, low is carry-out to next bit)

- Example 6. Add two one's with a carry in.
  A = 1
  B = 1
  CIN = 1 (CiA and CiB are high, and CiA/ or CiB/ is low)

Gate	Gate Output	Cause
1	Low	ADD, CiA, and CiB high
2	Low	A, B, and OR/ high
3	High	CiA/ or CiB/ low
4	High	A/ or B/ low
5	High	Gate 1 or gate 2 low
6	High	Gate 2 low
7	Low	Gate 3, gate 6, and ADD+AND high
8/10	High (ALU)	Gate 7 low
9	Low (ALU/)	Gate 8 high
11	High	A/ or gate 6 low
12	High	Gate 6 low
13	High	CiA/, CiB/, or gate 2 low
14	Low	CiA, CiB, and gate 4 high (gate 14, COB/, low is carry-out to next bit)

AND Operation

In an AND operation, a high output from an ALU bit is present only when both A and B inputs are high. If either or both inputs are low, the ALU output is low. The carry function is inhibited during an AND operation by the ADD signal which is low.

With the low ADD signal, the outputs of gates 1 and 3 are held high. Additionally, the outputs of gates 4 and 5 are held high by the AND/ signal, which is low during AND operation. Therefore, only gate 2 and gates 6 through 10 are effectively in the circuit during an AND operation. In an AND operation, gate 2 is the controlling gate; gates 6 through 10 merely follow the state of the gate 2 output. The ALU output is high only when a one is contained in both corresponding A and B register bits.

When ANDing two zeros, the output of gate 2 (see Figure 2-9) will be high, which is caused by the low A or B input. Likewise, when ANDing a zero and a one, the output of gate 2 will be high (A or B input low). When ANDing two ones, the output of gate 2 goes low (A, B, and OR/ high), which in turn causes the output of gate 6 to go high, the output of gate 7 to go low (gate 3 is held high by ADD input low; ADD+AND high), the output of gate 8 to go high, the output of gate 9 to go low (ALU/), and the output of gate 10 to go high (ALU).

OR Operation

In an OR operation, the ADD signal is low, thereby inhibiting the carry function. With the low ADD signal, the outputs of gates 1 and 3 are held high. The output of gate 2 is held high by the low OR/ signal (low during OR operation), and the output of gate 7 is held high by the low ADD+AND signal (low during OR operation). Therefore, only gates 4 and 5 and gates 8 through 10 are effectively in the circuit during an OR operation. The ALU output is high when a one is contained in either or both corresponding A and B register bits. In an OR operation, gate 4 is the controlling gate; gate 5 and gates 8 through 10 merely follow the state of the gate 4 output. When ORing two zeros, all inputs to gate 4 are high (AND/ is high during OR operation), causing the output of gate 4 to go low. The low output of gate 4 causes the output of gate 5 to go high (all other inputs to gate 5 are high during an OR operation). The high output of gate 5 causes the output of gate 8 to go low (the gate 7 output is high during an OR operation), the output of gate 9 (ALU/) to go high, and the output of gate 10 (ALU) to go low). In ORing a one and a zero, the output of gate 4 goes low (A/ or B/ low), the output of gate 8 goes low, and so forth. Likewise, when ORing two ones, the output of gate 4 goes low.

Exclusive-OR Operation

In an exclusive-OR operation, the ADD signal is low and, thereby, inhibits the carry function. With the ADD signal low, the outputs of gates 1 and 3 are held high. The output of gate 7 is held high by the low ADD+AND signal (low during exclusive-OR operation). Therefore, only gates 2, 4, 5, and 8 through 10 are effectively in the circuit during an exclusive-OR operation. The ALU output is high only when a one is contained in either but not both corresponding A and B register bits. In an exclusive-OR operation, gates 2 and 4 are the controlling gates and operate as OR-function gates. When exclusive-ORing two zeros, the A and B inputs to gate 2 are low, causing the output to go high; all inputs to gate 4 are high, causing the output to go low. The low output of gate 4 causes the output of gate 5 to go high, the output of gate 8 to go low, the output of gate 9 to go high (ALU/), and the output of gate 10 (ALU) to go low. When exclusive-ORing a one (A input) and a zero (B input), the low B input to gate 2 causes the output to go high; the low A/ input to gate 4 causes the output to go high. With the outputs of gates 2 and 4 high, the output of gate 5 goes low, the output of gate 8 goes low, and so forth.

When exclusive-ORing a zero (A input) and a one (B input), gates 2 and 4 react in the same manner as exclusive-ORing a one (A input) and a zero (B input). When exclusive-ORing two ones, the output of gate 4 goes low (all inputs are high) and the output of gate 4 goes high (A/ and B/ inputs low). The low output of gate 4 causes the output of gate 5 to go high, which, in turn, causes the ALU output (gate 10) to go low.

Test Mode ALU Entry (Figure 2-8)

During test or inline mode of operation, the value of the two LSB START ADDRESS switches are entered into the ALU when the ENTER switch is pressed to INNER or OUTER (test mode). When a microprogram statement (0 → GP) is present (inline mode), the value in the DATA switches (2LSB START ADDRESS switches) is loaded into the GP register through the ALU. In both cases, the ENTERSW signal goes high and the ENTERSW/ signal goes low to allow the START0 through START7 signals to be entered into the ALU. When the ENTERSW signal goes high, the state of START0 is reflected at the output of gate 17 (high if START0 is high). The ENTERSW/ signal will be low, causing the output of gate 8 to go high. With the absence of a machine reset signal (MACHRST/ high), the output of gate 9 (ALU/) goes low and the output of gate 10 (ALU) goes high. The opposite is true (gate 9 goes high and gate 10 goes low) when START0 is low.

ALU Parity Generation (ALU-4(1))

Parity is generated on all data passing through the ALU. The destination of ALU0 through ALU7 is routed to a register specified by the SD field of the ROM word (see register function). ALU parity (ALUP) is routed to most of these registers when selected. The registers for which parity is stored are GL, BY, FR, KL, DH, DL, OP, GP, SP, UR, DR, DW, BX, and CX.

READ-ONLY MEMORY ADDRESS REGISTER (ROM-11)

The read-only memory address register (ROMAD) is an 11-bit register that is used to address the 2,048 words of the ROM. During normal or inline mode of operation, inputs to the ROMAD are controlled by portions of the word just read from the ROM. During test mode of operation, inputs to the ROMAD are from the START ADDRESS switches on the test panel and from portions of the word just read from the ROM.

The input to ROMAD0 for a specific address is determined by the SL field of the ROM word. The value contained in the SL field allows a specific condition in the controller to be tested. The specific conditions tested are the odd bits of the ST and OP registers and some channel control signals.

When the value of the SL field equals six, ABUS7 through ABUS0 are entered into ROMAD bits 0 through 7 respectively.

The input to ROMAD1 for a specific address is determined by the SH field of the ROM word. The value contained in the SH field allows a specific condition in the controller to be tested. The specific conditions tested are the even bits of the ST and OP registers and some channel control signals. When the value of the SH field equals eight, SK6 and SK5 are entered into ROMAD bits 9 and 10 respectively.

Inputs to ROMAD2 through ROMAD7 are from the SN field of the ROM (SN5 through SN0, respectively). The SN field of the ROM word determines the next ROM address.

The input to ROMAD8 is the odd-module (OM) bit of the ROM word. When OM is high, an odd module in the ROM can be addressed.

During test mode of operation, the address set into the START ADDRESS switches (START0 through START10) on the test panel is clocked into the ROMAR when the controller is inhibited (INHIBITA high) and the SET ADDRESS switch on the test panel is pressed (SETSW/ low). A high INHIBITA signal and a low SETSW/ signal (see TIM-3) produce a low SET START/ signal. When the MODE SELECT switch is set to RECYC (recycle) or SCAN, the RECYCLE/ signal will go low each time the ROM address equals the address set into the STOP ADDRESS switches. Each time RECYCLE/ goes low, the ROM start address (START0 through START10) is clocked into the ROMAR.

In normal or inline mode of operation, SETRAD0-8 and SETRAD9-10 signals (see ROM-2) clock the input into the ROMAR.

The read-cycle-initiate (RCI) signals start the ROM addressing cycle. In the present ROM circuit board configuration, only RCI1 and RCI3 are used. RCI1 comprises ROMAD10/ and index enable (INDEXENBL) signals. RCI3 comprises ROMAD10 and INDEXENBL. INDEXENBL is high at T0 when the controller is not inhibited (INHIBITA/ high–see TIM-3).

The parity of the ROMAD is checked to determine whether an address error has occurred. The outputs of the ROMAR (ROMAD0 through ROMAD10) are applied to a parity circuit. The result of the parity check is latched into a flip-flop at T1. When the word specified by the address is read out, the parity result in the flip-flop is compared with PABF (address parity bit). If an odd parity is not achieved, RADERR/ goes low, thus indicating an addressing error.

RECYCLE CONTROL (ROM-2)

The recycle control circuits enable a program loop between the ROM addresses set into the START ADDRESS and STOP ADDRESS switches when the controller is operating in the test mode.

The STOP0 through STOP10 outputs of the STOP ADDRESS switches are compared with the ROMAR outputs (ROMAD0 through ROMAD10). When these signals match exactly (COMPADREQ1 and COMPADREQ2 high), the recycle latch is set at T2 if the controller is in the test mode of operation (TESTSW/ low) and the MODE SELECT switch is set to RECYC. The RECYCLE/ signal is low when the recycle latch is set and causes the ROM address set into the START ADDRESS switches to be clocked into the ROMAR (see ROM-1).

The recycle latch is also set at T2 during test mode of operation (TESTSW/ low) when the MODE SELECT switch is set to SCAN and the SL field of the ROM word is not equal to six (SLEQ6 low). With the MODE SELECT switch in the SCAN position, the storage scan test microprogram is exercised. The microprogram recycles to the home address set into the START ADDRESS switch as a result of the RECYCLE/ signal going low.

The STPEQ signal is active (goes high) when the STOP0 through STOP10 outputs of the STOP ADDRESS switches match the address in the ROMAR. The STPEQ signal is used to inhibit controller operation during the test mode of operation (TESTSW/ low) when the MODE SELECT switch is set to STOP (STOPSW/ low–see TIM-3). The STPEQ signal is also used in enabling the probe latch (TEST-3).

The SETA/ and SETRAD0-8 signals are logically identical and are activated (go low) at T3 when the controller is not inhibited (INHIBITB/ high) during normal or inline test mode (TESTSW/ high) and no errors exist (ER4 low, SARERR/ and RADERR/ high). If an A register parity error (ER4 goes high), a sense amplifier error (SARERR/ goes low), or a ROM address error (RADERR/ occurs, STPROMAD goes low and causes SETA/, SETRAD0-8/, and SETRAD9-10/ to go high. If an error occurs during test mode of operation while the CHK STOP/RUN/SINGLE STEP STOP switch is set to CHKSTOP (CHKSTPSW/ low), SETA/, SETRAD0-8, and SETRAD9-10 go high.

SETRAD9-10 is activated in the same manner as SETA/ and SETRAD0-8 with an additional requirement. SETRAD9-10 is activated when the value in the SH field of the ROM word equals eight (load SK5 and SK6 into ROMAR) or in test mode of operation when a recycle condition exists.

When the value of the SL field in the ROM word equals six (SLEQ6 high), ABUS0 through ABUS7 are loaded into the ROMAR (see ROM-1) only in the test mode of operation while the MODE SELECT switch is set to SCAN. When the value of the SL field in the ROM word does not equal six (SLEQ6/ high), SN0 through SN5 and the results of the SL and SH branch tests are loaded into the ROMAR.

READ-ONLY MEMORY (ROM-3)

The ROM is a random-access memory system that operates at a 2 MHz rate and has a total capacity of 98,034 bits of information organized as 2,048 words of 48 bits each. A single ROM access supplies the 48-bit word in parallel to the sense amplifier register (SAR).

The ROM is contained on two circuit board assemblies (some early model controllers have four ROM circuit board assemblies); each has a capacity of 1,024 words.

The two-board ROM systems presently used are of two types, and each is interchangeable with the other. They differ only in appearance and in circuit design.

Each bit of the ROMAR determines a specific portion of the ROM to be addressed. As shown in Figure 2-10, ROMAD10 (MSB) determines which ROM board is to be addressed. ROMAD9 determines the layer on the ROM board; ROMAD8 determines the module to be addressed. A module in this memory system is not a physical module, but rather a segment of the ROM equal to one-eighth of the ROM; there are 8 modules in the ROM. ROMAD 6 and 7 define a section of the ROM that is equivalent to one-fourth of a module. ROMAD6 determines the vertical (column) address of the section, and ROMAD7 determines the horizontal (row) address of the section. Within each section are 32 blocks. The block address is determined by the value of ROMAD1 through ROMAD5. ROMAD 1 and 2 determine the

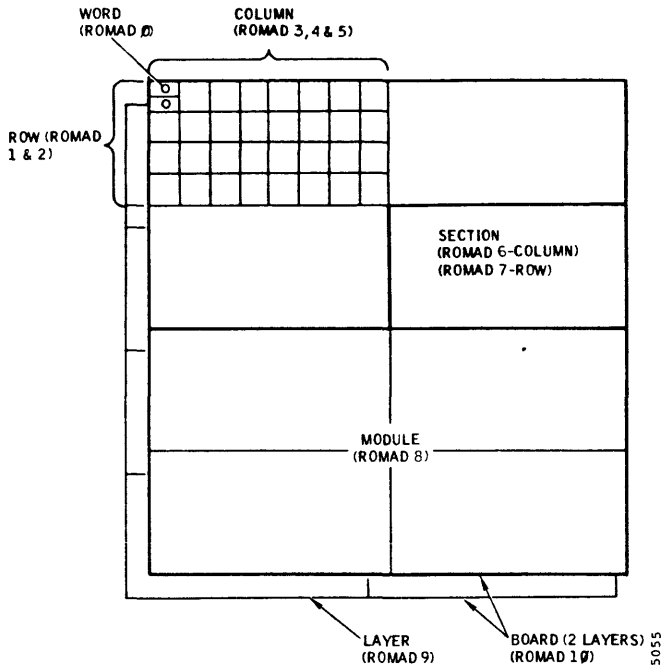


Figure 2-10. ROM Circuit Board Organization

block row address, while ROMAD3 through 5 determine the block column address. Each block contains two words. The selection of a word is determined by ROMAD0.

The RCI signal (RCI1 or RCI3, depending on which board is being addressed) initiates the memory access cycle at T0 after the ROM address (ROMAD0 through ROMAD9) has been supplied to the ROM at T3 (see Figure 2-11). The RCI signal fires the first one-shot, which, in turn, fires the second (matrix strobe) and third (drive line) one-shots. The drive line one-shot supplies the current to the two selected drive lines (selected by ROMAD1 through ROMAD9). The drive lines induce current into the secondary (sense) windings of each transformer that has a drive line passing through it. If the drive line does not pass through a transformer, no current will be induced into the sense winding. When the output of the first one-shot falls, the fourth one-shot (read sense) fires to enable ROMAD0 to select one of the two words. The selected word is supplied to the sense amplifier register (SAR).

The SAR reset signal (SARRST/) resets the SAR before the sense output of the ROM is available to the SAR.

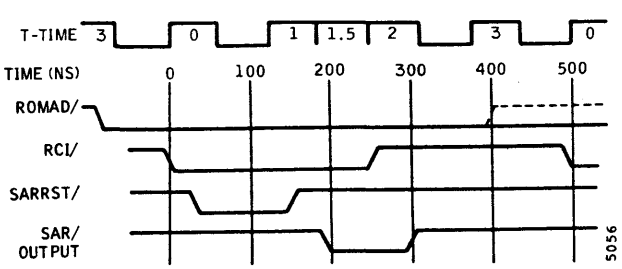


Figure 2-11. Read-Only Memory Timing Diagram

SENSE AMPLIFIER REGISTER (ROM-4(1) and ROM-4(2))

The 48-bit word output of the ROM is divided into 13 fields; each field performs a particular function during each microinstruction cycle. A description of the function of each field follows. Figure 2-6 illustrates the bit and field organization and the function of each field of the ROM.

SA Field

The value contained in the SA field (bits 43 through 47) determines the input source for the A bus (e.g., SA=17 determines that the DR register is the input source for the A bus). When operating in the test mode of operation with the CHK STOP/RUN/SINGLE STEP STOP switch set to CHK STOP, the microprogram will stop when the SA field equals 16 (see TIM-3).

SV Field

The state of the SV bit (bit 42) determines whether the B register is gated in true (SV=0) or one's complement (SV=1) form to the ALU. The SV bit is used in conjunction with the SB and SC fields.

SC Field

The value contained in the SC field (bits 39 through 41) determines the arithmetic operation that the ALU will perform. The SC field determines eight different arithmetic operations; however, in conjunction with the SV bit, 16 different arithmetic operations may be considered to be performed.

SB Field

The value contained in the SB field (bits 37 and 38) determines the input source for the B bus. The state of the SV bit determines whether the B bus source is gated into the B register in true or complement form.

SK Field

The value contained in the SK field (bits 29 through 36) is used as a constant data source by the microprogram. The SK field is an input source to the B bus when the SB field equals two. The value in SK5 and SK6 determines the ROM board and board layer that will be addressed when the SH field equals eight (load SK into ROMAR).

SD Field

The value contained in the SD field (bits 24 through 28) determines the destination of the ALU output (e.g., SD=17 places the ALU output in the DR register). It should be noted that as long as the ALU input data sources remain static, the resultant data on the ALU bus will remain static.

SS Field

The value contained in the SS field is used to control the setting and resetting of individual bits in the ST register (e.g., when SS=2, ST1 is reset and when SS=3, ST1 is set).

SN Field

The value contained in the SN field (bits 14 through 19) is used to determine the next address for the ROM. SN0 through SN5 are gated into ROMAR bits 7 through 2 respectively when the SL field does not equal six (see ROM-1). SN5 is also used to control the loading of the FC and FT registers (see DDI-3).

SH Field

The value contained in the SH field (bits 10 through 13) allows a particular controller condition to be tested. The result of the test controls the branching condition by setting or resetting ROMAR bit 1. When SH equals zero, ROMAR bit 1 is reset; when SH equals one, ROMAR bit 1 is set. When the value in the SH field equals 2 through 15, the condition to be tested, as shown on Figure 2-6, sets ROMAR bit 1 if the condition under test is on (high) or resets ROMAR bit 1 if it is off (low).

SL Field

The value contained in the SL field (bits 6 through 9) allows a particular controller condition to be tested. The result of the test controls the branching condition by setting or resetting ROMAR bit 0. When SL equals zero, ROMAR bit 0 is reset; when SL equals one, ROMAR bit 0 is set. When the value in the SL field equals 2 through 15, the condition to be tested, as shown in Figure 2-6, sets ROMAR bit 0 if the condition under test is on (high) or resets ROMAR bit 0 if it is off (low).

OM Field

The OM field (bit 5) determines whether an even or odd module is to be selected for the next address. If the OM bit is high the next module to be selected is an odd module.

PA Field

The PA bit (bit 1) is the parity bit for the ROMAR. When the number of high bits in the ROMAR is even, the PA bit must be high (odd parity); when the number of high bits is odd, the PA bit must be low.

PC Field

The PC bit (bit 0) is the parity bit for the SAR output. When the number of high SAR bits is even, the PC bit must be high; when the number of high SAR bits is odd, the PC bit must be low.

The outputs of the ROM (SAR0/ through SAR47/) are supplied to the sense amplifier register (SAR). When the controller is first powered-up or during any controller general reset, MACHRST;1 goes high. With MACHRST;1 high, all SAR latches are reset except the PC and PA latches which are set. The PC and PA latches are set to maintain correct (odd) parity. All latches including PC and PA are reset, during normal operation, just before each ROM word is read out. This is done to clear the previous word from the SAR.

SAR bits SN5, SS0 through SS3, and SD0 through SD4 have an additional latch, which is clocked by T3, to store those particular bits for a period of time after the SARRST/ signal resets the sense latch.

Parity for the SAR outputs is checked in the parity circuits (see ROM-4(2)) which comprise six parity chips. All SAR latch outputs are compared with the PC bit and should result in an odd parity indication (SARERR low). If SARERR is high, a sense amplifier parity error is indicated on the test panel (SENSE AMP indicator lit), and the controller operation is halted (see TIM-3).

READ/WRITE SELECT and PHASE LOCK (SERDES-1)

Read/Write Selection

Read and write data is transferred between the controller and the selected disk drive in serial form via a single coaxial cable. A separate read/write coaxial cable (part of the dc cable) is used to transfer data between the controller and each attached disk drive. When a disk drive is selected by the channel (through the controller) for an operation, the disk drive replies with a module select signal (individually CMSA through CMSJ). For a write operation, the module select signal from the disk drive enables the data (WRTOUT) to be transferred via the coax cable to the disk drive and to be written on the disk pack. During a read operation, the module select signal enables data from the disk drive to be routed to the phase lock circuits when the read gate (RDGATE) is high.

Phase Lock

The phase lock circuits compensate for frequency variations due to rotational rate changes in the disk drive. Variations in speed can vary ± 2 percent from the nominal rate of 2400 rpm and as much as ± 4 percent when switching from one disk drive to another.

The phase lock circuits are contained on circuit boards AT12, AT13, and AT14 located respectively in locations C-9, C-10, and C-11. The phase lock circuits basically consist of a pulse shaper, a delay line, an error detector (differential amplifier and error amplifier), a voltage-controlled oscillator (VCO), a phase control flip-flop and gating, and a decoder (window control and decode logic).

The output of the read selection circuit (RAWDATA) is routed to the pulse shaper one-shot. The pulse shaper removes pulse width variations from the RAWDATA signal so that the input to the error detector is a constant width pulse nominally 100 nanoseconds.

The delay line compensates for delays inherently generated in processing data by the error detector, VCO, and phase control circuits. The data output of the pulse shaper is routed to the error detector and to the delay line. While the data signal progresses through the delay line, the undelayed data signal is being processed by the error detector. Eleven taps on the delay line are provided for aligning the raw data (delayed) with the processed data from the phase control circuit. The output of the delay line is connected to a pulse restorer which reshapes the leading and trailing edges of the data pulses.

The error detector circuit generates an error signal that is proportional to the phase relationship of the incoming raw data (DATAOUT) to the output of the VCO. The error signal is integrated to form a time-averaged signal so that instantaneous frequency changes do not appear as a frequency error. The response time of the error detector is such that, after initial lockup, only slowly varying frequency changes caused by disk speed variations are tracked. When the phase lock circuits are locked onto the incoming raw data, the VCO signal lags the raw data by 90 degrees and the error signal is zero. The zero-set potentiometer (R17) is used to balance the error amplifier.

The output of the error amplifier is routed through frequency adjust potentiometer R23 to the 10 MHz voltage-controlled multivibrator. The frequency adjust potentiometer is used to adjust the VCO for an output of 5 MHz when the output of the error amplifier is zero volt. The 10 MHz voltage-controlled multivibrator is a free-running multivibrator whose nominal output is 10 MHz. The positive-going output of the multivibrator is used to clock the VCO flip-flop, which results in an output signal of 5 MHz from the flip-flop. A positive error signal from the error amplifier causes the multivibrator to speed up. A negative error signal causes the multivibrator to slow down. The VCO output signal is used by the phase control and decoder circuits to define the clock and data bit cell time.

The phase control circuit defines the incoming data as either a clock or data bit after the phase lock circuits have locked onto and are tracking the raw data. The phase control circuit consists of a phase control flip-flop, a clock phase gate (CLKPH/), and a data phase gate (DATAPH/). The phase control flip-flop is clocked by an output of the VCO flip-flop; therefore, its output is nominally 2.5 MHz. When the phase latch circuits have locked onto and are tracking the raw data, the phase control circuits must be orientated in the proper phase relationship to the incoming data and clock bits. This is accomplished by the phase orientation circuit when the set phase signal (SETPH/) goes low (see SERDES-2). The outputs of the phase control flip-flop (PHASELTH and PHASELTH/) are ANDed with the VCO signal to form the clock phase (CLKPH/) and data phase (DATAPH/) signals.

The decoder circuit produces separated data (SEPDATA) and separated clock (SEPCLK) signals from the delayed data (DELDATA), WINDOW, PHASELTH, and PHASELTH/ signals (see Figure 2-12). The resolution of the phase lock circuits is improved through the use of a data window which is generated from the VCO signal. The data window envelope is adjustable in width as well as in time of occurrence. The data window prevents a single data or clock bit from being decoded as both a data bit and a clock bit. When adjusting the phase lock circuits, the output of the delay line is so chosen that delayed data is centered in the PHASELTH and PHASELTH/ signals. The data window is normally adjusted for a pulse width of 200 nanoseconds minus the width of the delayed data pulse (e.g., if data width equals 80 nanoseconds, the data window is adjusted for 120 nanoseconds; 200−80=120). The data window serves as a strobe to define the sampling time for data and clock bits. The DELDATA, WINDOW, and PHASELTH or PHASELTH/ signals are ANDed to produce separate data output and clock output signals. Because of data pulse jitter or sliding, the data output and clock output signals respectively are routed to pulse shaping one-shot multivibrators which each produce a 70-nanosecond pulse.

During the period when the RDGATE signal is low, the 5 MHz oscillator signal (OSC5MHZ) is routed to the phase lock circuits to minimize drift in these circuits and to minimize the time to lock onto new data from a disk drive.

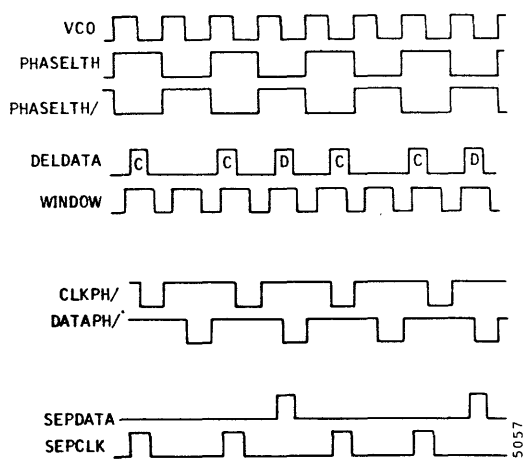


Figure 2-12. Decoder Timing

DATA CHECK (SERDES-2)

During a read operation, the data check circuits determine the beginning of the various fields recorded on a disk pack by detecting the address mark bytes preceding each field. The data check circuits also orient the phase lock circuits to the clock and data bits of the incoming data.

Phase Orientation Circuits (Figure 2-13)

When the access mechanism in the disk drive accesses a new cylinder, a different head, or a different record on the same track, the phase lock circuit may lock onto the incoming data 180 degrees out of phase: that is, it may see clock bits as data bits and data bits as clock bits. The phase orientation circuit detects this condition and generates a set phase (SETPH/) signal which reorients the phase flip-flop (SERDES-1) to coincide with the incoming data.

If the phase lock circuit latches onto the raw data 180 degrees out of phase, the following conditions will exist when reading the all-ones bytes of the track gap (also see Figure 2-14).

- The read gate (RDGATE) signal will be high.
- The RESTART signal will be high because the restart latch is reset by the high read reset (READRST) signal.
- The clock gap (CLKGAP) and data gap (DATAGAP) signals will be low because no gaps exist when reading all ones even if the phase lock circuits are 180 degrees out of phase.
- The read enable reset (RDENBLRST/) signal goes low each time that CLKPH/ goes low (READRST is high).
- Latch 1 is held set by latch 4 being in a reset state.
- Latch 2 is held reset by CLKGAP being low.
- Latch 3 is reset by the deserialize data (DESDATA/) signal being low for each data bit. Latch 3 cannot be set because latch 2 is held reset.
- Latch 4 is reset by the RDENBLRST/ signal which goes low at each CLKPH/ time.

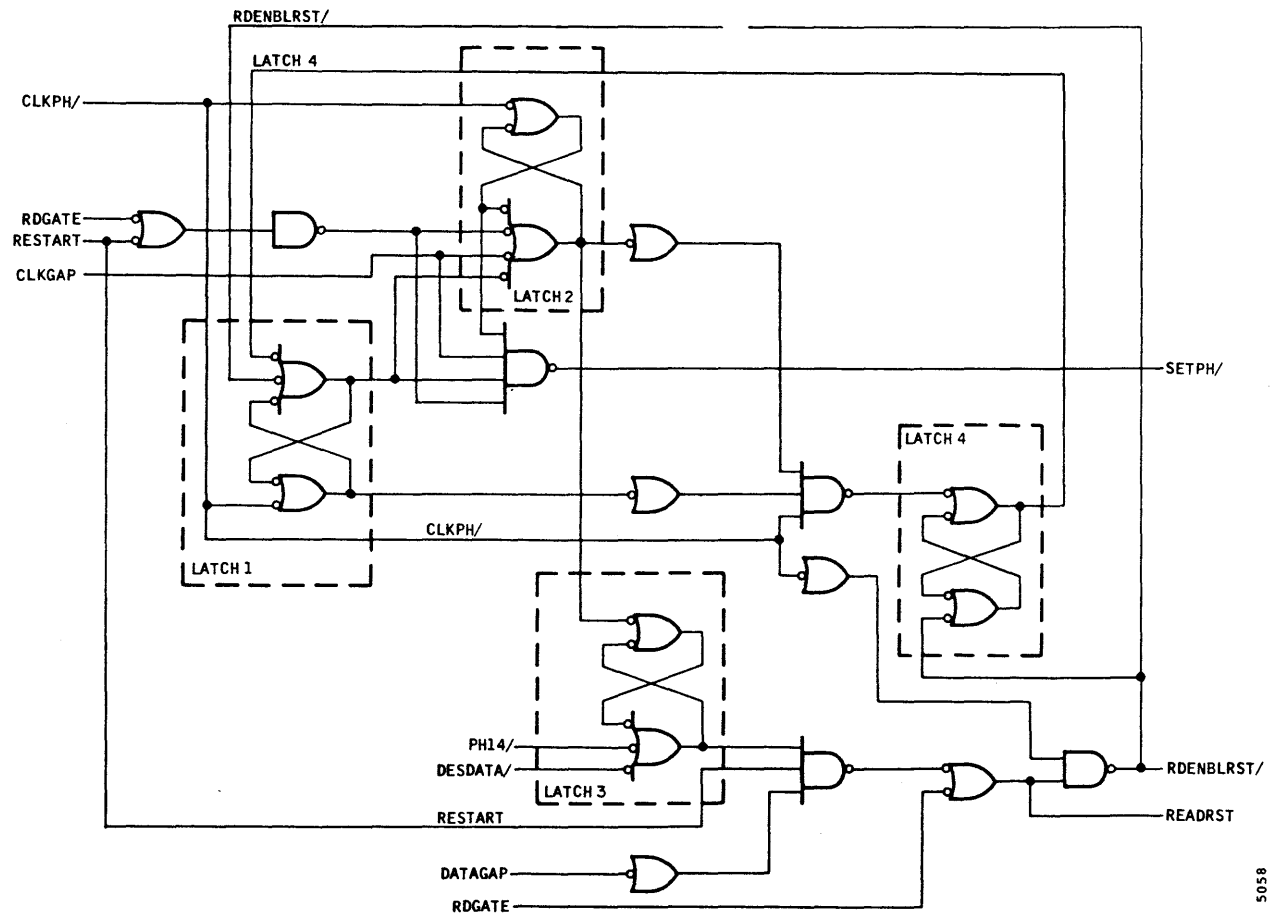


Figure 2-13. Phase Orientation Circuit

- The set phase (SETPH/) signal is held high by the CLKGAP signal which is low.

When the first byte of the four bytes of all zeros that precede the two address mark (AM) bytes is being read, a clock gap is detected (CLKGAP signal goes high) on the the second consecutive clock pulse if there is no intervening data pulse. By CLKGAP going high, the reset hold (CLKGAP low) is removed from latch 2, and, at the next clock phase time (CLKPH/ low), latch 2 is set and the SETPH/ signal goes low. The low SETPH/ signal causes the phase flip-flop to set, and, when the VCO signal goes low, an in-phase clock phase signal (CLKPH/ low) is generated. The setting of the phase flip-flop places the phase lock circuit in phase with the incoming data. Latch 3 is set at the same time that latch 2 is set. Setting latch 3 causes the READRST signal to go low and removes the reset hold from latch 4. Latch 4 is set by the CLKPH/ signal going high after latch 2 was set (latch 2 set, latch 1 set, and CLKPH/ high sets latch 4). With latch 4 set, the set hold on latch 1 is removed, and latch 1 is reset by CLKPH/ going low after latch 4 was set. Latch 2 is reset and held reset by latch 1 being reset. The SETPH/ signal goes high at the same time that latch 2 is reset.

A data gap is detected when the first missing data bit after the phase correction is detected. The high DATAGAP signal holds the READRST signal low.

When the SETPH/ signal went low, it also set phase counter (PH) bit 23. The setting of the DATAGAP latch causes the read enable (RDENABLE) to set (see SERDES-3), which allows the PH10 through PH17 and PH20 through PH27 counters to be clocked alternately by DATAPH/ and CLKPH/ respectively. When the DATAPH/ signal goes low after the DATAGAP signal goes high, PH14 latch sets, which, in turn, causes latch 3 to reset. By setting PH23 with the SETPH/ signal, the phase counter is put in step with the incoming data.

Address Mark Detection

Address marks (AM) are written before each track field as part of the gap (see Figure 2-15). The address marks are used to locate the beginning of a field for searching, writing, and reading operations. The address marks allow an operation to begin at any point on a track rather than at the index point, thus enabling faster access to data.

The AM area consists of two bytes of ones with five clock pulses missing from each byte. The AM area is preceded by a VCO area that consists of five bytes—one byte of ones immediately preceding the AM area and four bytes of zeros. Immediately following the AM area is a sync byte. The first four data bits are missing, and the last four are variable depending on which field the sync byte precedes.

The search for an address mark area first requires that the four bytes of zeros and one byte of ones be detected. During the first byte of zeros, data gap latch 1 (DG1) is set by the first clock bit (SEPCLK high) of the byte when the phase lock circuit latches in phase with the incoming data (see Figure 2-14). DG1 is set by the third clock bit of the byte after phase correction is made. When SEPCLK goes low, DG2 is set. Since there is no data bit (SEPDATA low) following the clock bit to reset DG1 and DG2, the clock gap latch is set when SEPCLK goes high for the next clock bit. With the DATAGAP signal high, the READRST and RDENBLRST/ signals are inhibited (READRST goes low and RDENBLRST/ goes high). The DATAGAP signal also causes the RDENABLE latch to set when DATAPH/ is low (see SERDES-3), thus allowing the DATAPH/ signal to step the PH10 through PH17 ring counter since the reset control for this counter was disabled when the READRST signal went low.

AM count latch 1 (AMCONT1) is clocked by the first PH10 signal after the PH10 through PH17 ring counter is enabled, which is at the beginning of the second byte of zeros. When the AMCONT1 latch is clocked, the AMCONT1 signal goes high, which, in turn, clocks the AMCONT2 latch. With both AMCONT1 and AMCONT2 signals high, the count 11 (CONT11) signal goes high. The CONT11 signal remains high until the next PH10 signal goes high, which again clocks the AMCONT1 latch to the opposite state (beginning of the third byte of zeros). Since there is no decode logic for a count of 01 (AMCONT1 reset, AMCONT2 set), no CONT signals are high during the third byte of zeros. At the beginning of the fourth byte of zeros, the AMCONT1 latch is clocked by PH10 to the opposite state (AMCONT1 signal high). With the AMCONT1 signal high, the AMCONT2 latch is clocked to the opposite state (AMCONT2 signal goes low). With the AMCONT1 signal high and the AMCONT2 signal low, the CONT10 signal goes high. At PH26 time of the fourth byte of zeros, the AM area latch is set. AT PH17 time after the AM area latch is set, the search AM (SCHAM) latch is set. Since the data good and AM good latches are not set when the AM area latch is set, the restart latch sets (RESTART signal goes low) to maintain the READRST and RDENBLRST/ signals in a disabled state. This is necessary since the DATAGAP signal, which has maintained the READRST and RDENBLRST/ signals in a disabled state since the beginning of the first byte of zeros, will go low during the byte of ones. At the beginning of the byte of zeros, the CONT10 signal goes low and the CONT00 signal goes high. At PH25 of the byte of ones, high CONT00 and AMAREA signals cause the SETAMGOOD signal to go low, which, in turn, causes the AM good and data good latches to set. The setting of the AM good and data good latches does not mean that the address marks are good, but does mean that the preamble to the two AM bytes is good.

During the two AM bytes, only the AMCONT1 and AMCONT2 flip-flops and the CONT signals change state. If a data gap occurs or a clock gap is not detected during PH22, PH23, or PH24 (AMX signal high) of either AM

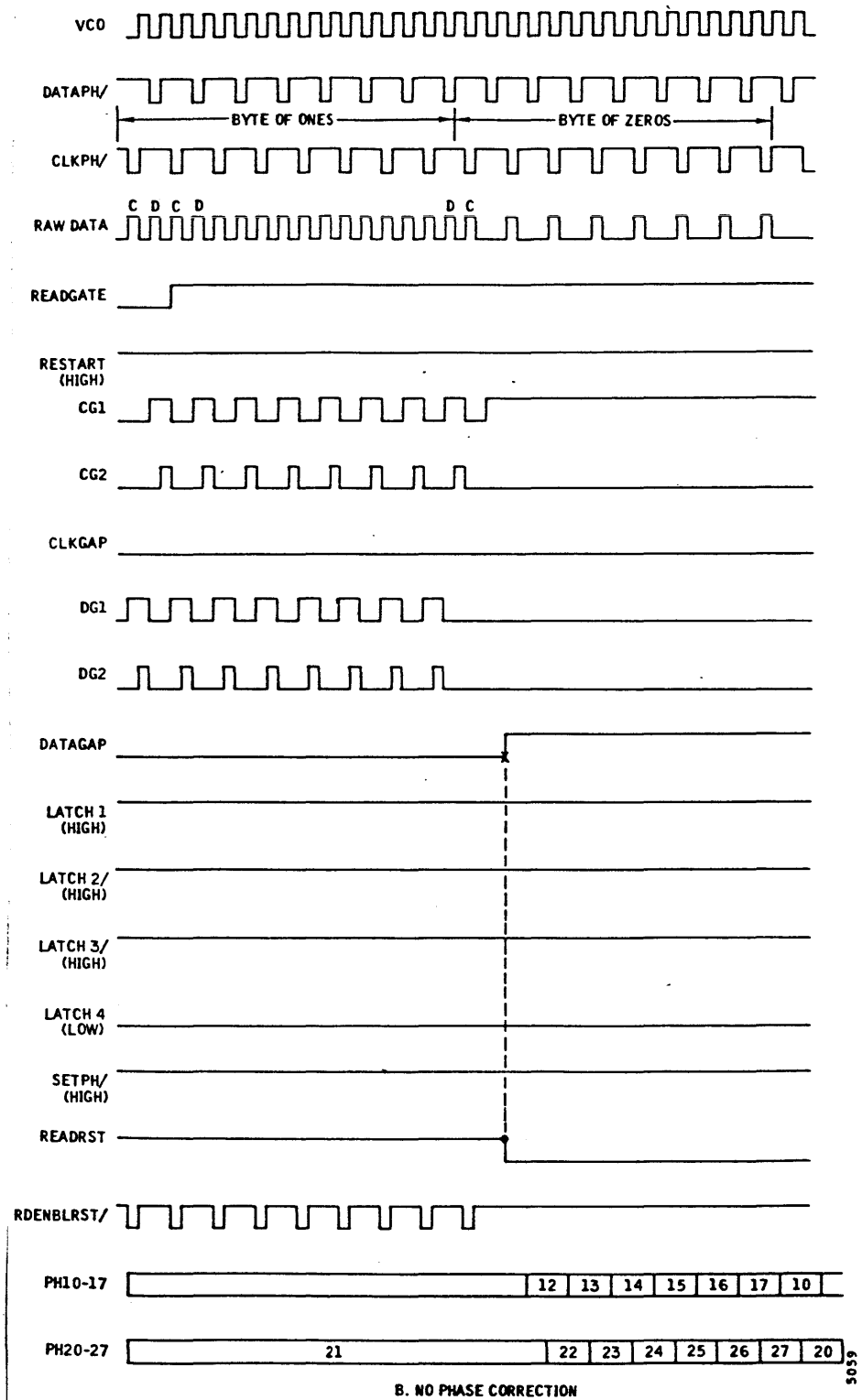
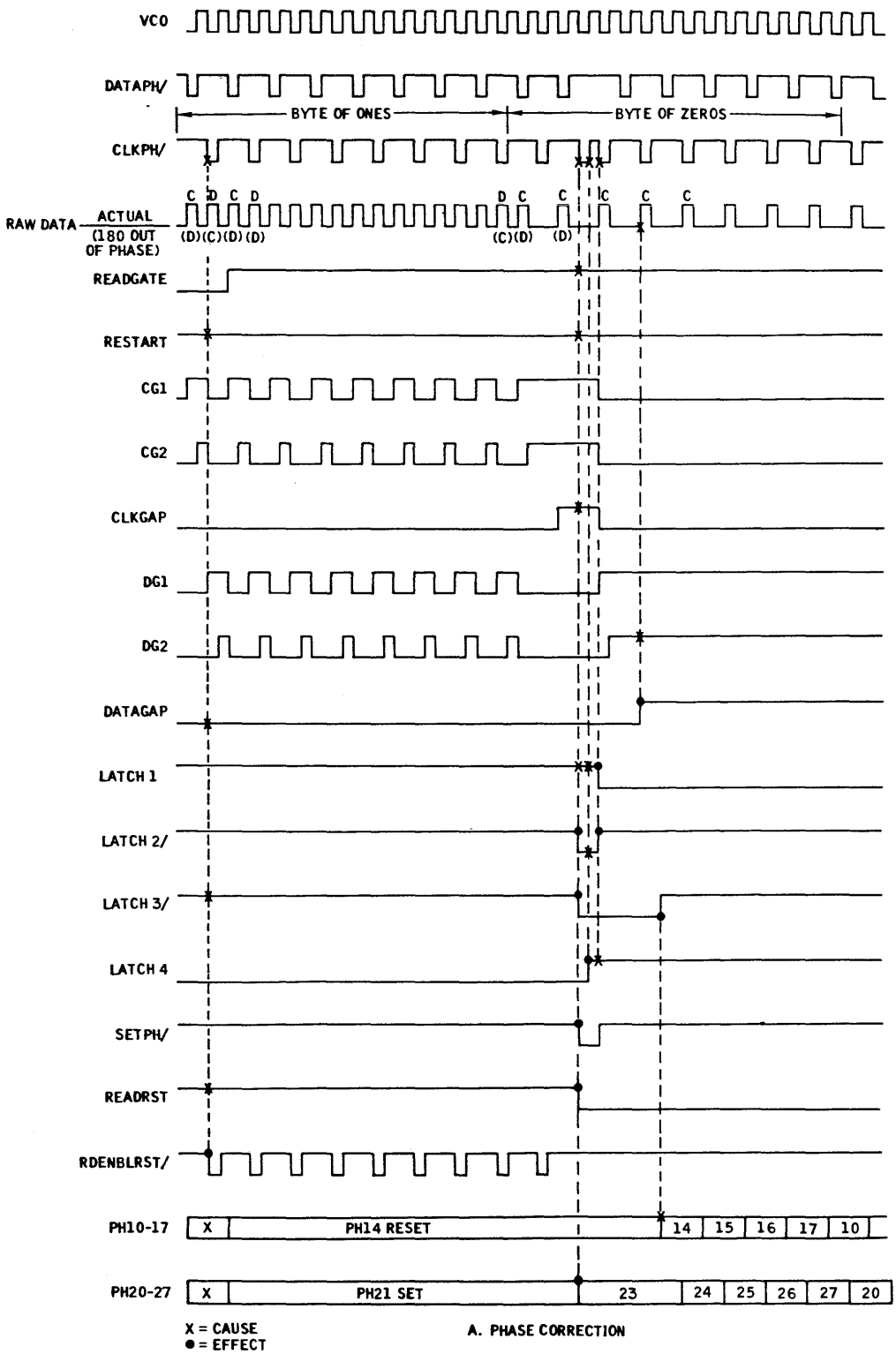


Figure 2-14. Phase Orientation Timing Diagram



A. PHASE CORRECTION

VARIABLE NUMBER OF BYTES (ALL ONES)			VCO AREA (5 BYTES)			AM AREA (2 BYTES)		SYNC AREA (1 BYTE)
ONES	ONES	ONES	ZEROS	ZEROS	ONES	ONES 5 CLOCK PULSES MISSING	ONES 5 CLOCK PULSES MISSING	SEE SYNC BYTE CONFIGURATION BELOW
11111111	11111111	11111111	00000000	00000000	11111111	11111111	11111111	

A. GAP CONFIGURATION

HA SYNC BYTE	RO COUNT SYNC BYTE	RO DATA SYNC BYTE	R_N COUNT SYNC BYTE	KEY SYNC BYTE	R_N DATA SYNC BYTE
13_{10} 00001101	11_{10} 00001011	9_{10} 00001001	14_{10} 00001110	10_{10} 00001010	9_{10} 00001001

B. SYNC BYTE CONFIGURATIONS

5060

Figure 2-15. Gap Format

byte (AMCONT2 signal high), the AM good latch is reset, which, in turn, will reset the restart latch (SCHAM, AMCONT, and AMGOOD/ high) and cause the RESTART signal to go high. If a data gap or a clock gap is detected during PH10 or PH17 when the data good latch is set, the data good latch will be reset. If the AM good and data good latches remain set through PH14 of the sync byte (CONT10 high), the check good (CHKGOOD) latch will set. At PH25 of the sync byte (CHKGOOD signal high), the SCHAM latch is reset, which, in turn, resets the AM good and data good latches. From this point on, as long as the CHKGOOD signal is high, the FDRXDR/ signal allows the accumulated deserialized data in the FDR to be transferred to the DR register at clock phase (CLKPH/ low) time of PH10.

When the FDRXDR/ signal is low (during a read operation), status register bit 4 (ST4) is set (SETST4 high), indicating to the microprogram that the DR register has been loaded with data from the FDR and is ready for transfer to the channel. ST4 is also set during a write operation when data has been transferred from the DR register to the FDR (DRXFDR/ low) for serialization to indicate to the microprogram that the DR register is ready for another byte of data.

The GATEFDR signal is high at each PH10 of a read operation (RDGATE high) to allow the output of the FDR to be available at the DR register before the FDRXDR/ signal goes low (before the CLKPH/ signal goes low).

The GATEALU signal is high to allow the ALU bus data to be entered into the DR register when a read operation is not in process (RDGATE low) and bus-out data is not being transferred into the DR register (IHDR low).

Write Address Mark

When the microprogram determines that it is time for the address mark bytes to be written, the write AM line (bit 4 of the FT register–FT4) goes high. FT4 must go high before the beginning of PH11 of the first AM byte during a write operation (WRTGATE high) in order to set the write AM latch. Before the write AM latch is set, the first clock in the first AM byte is written. After the first clock is written, the write AM latch is set and remains set until the beginning of PH16. With the write AM latch set, five clock bits (bits 2 through 6) are inhibited from being written. At the beginning of PH16, the write AM latch is reset to allow the remaining clock bits to be written in the first AM byte. The second AM byte is written in the same manner as the first AM byte.

During the writing of the second AM byte, the microprogram causes FT4 to go low. FT4 can go low at any time after the end of PH11 of the second AM byte, but it must go low before the beginning of PH25. At PH25 of the second AM byte, with FT4 low and the write AM latch set, the second AM latch is set. At PH14 of the sync byte, the read/write (R/W) data good latch is set to enable the burst check latch to set and the bit count advance latch to set.

PHASE COUNTERS AND FILE DATA REGISTER (SERDES-3)

The phase counters and the file data register (FDR) are used for both read and write operations.

Read Operation (see Figure 2-16)

A read operation is initiated by the microprogram when it causes file tag register bit 0 (FT0) and file control register bit 1 (FC1) to go high; together, these signals generate the read gate (RDGATE high). With RDGATE high, a search for an address mark (AM) is initiated (see SERDES-2).

The PH20 through PH27 counter is initialized (PH21 flip-flop set), prior to detecting the four bytes of zeros which precede the two AM bytes, by the READRST

signal and RDGATE high. PH21 is set because the read enable latch cannot be set until a data gap is detected in the first byte of all zeros. By the time a data gap is detected, PH20 time is already passed. If a phase correction is required because the phase lock circuits latch onto the incoming data 180 degrees out of phase, SETPH/ goes low and causes PH21 to reset and PH23 to set. PH23 is set when a phase correction is required, due to the time required to detect a phase error, and after the phase correction, to detect a data gap. When a data gap is detected, the read enable latch is set at data phase time (DATAPH/ low). After the read enable latch is set and during the same data phase time, the PH10 through PH17 counter is clocked one time, setting PH12 or PH14, depending on the preset conditions previously described. At the following clock phase (CLKPH/ low), the PH20 through PH27 counter is clocked one time to set PH22 or PH24, depending on the preset conditions. The PH10 through PH17 counter is clocked once each time that DATAPH/ goes low, and the PH20 through PH27 counter is clocked once each time that CLKPH/ goes low. When PH27 is set, the next DATAPH/ signal causes PH10 to set. This alternate clocking of the two counters by the DATAPH/ and CLKPH/ signals continues until the RDENBLRST/ signal goes low and resets the read enable latch.

Separated data (SEPDATA) is loaded into the FDR starting with the first byte of zeros; however, data is not transferred to the DR register until the transfer signal (FDRXDR high) enables the transfer. The first transfer is that of the sync byte at PH10 of the first data byte.

The serial SEPDATA signal is clocked into the direct set input (S) of the FDR by the PH20 through PH27 counter. When the FDR is full, its contents are transferred to the DR register at CLKPH/ time of PH10 of the following byte of data. The FDR is reset at DATAPH/ time of PH10 of the following byte of data. Since the data is transferred from the FDR and since the register is reset during PH10, data bit 0 is clocked into the parity flip-flop (data read from the disk pack contains no parity bit) at PH20 time and transferred to FDR0 at PH22 time. At PH21 time, data bit 1 is clocked into FDR1; at PH22 time, data bit 2 is clocked into FDR2; etc. Data bit 4 of the sync byte is not clocked into FRD4 (inhibited by SCHAM/ low) because the microprogram looks for a zero in that bit. A one is written in that bit to be compatible with other systems.

Write Operation (see Figure 2-17)

A write operation is started when the microprogram causes the write gate to go high (FT0 and FC0 high). The write time source (both clock and data) is the 5 MHz oscillator (see TIM-1). The 5 MHz signal (OSC5MHz) clocks a write trigger flip-flop that defines the clock time (CLKTRIG high) and the data time (DATATRIG high) Both the 5 MHz oscillator and the clock trigger flip-flop operate continuously without regard to the write gate.

The PH20 through PH27 counter is initialized by setting PH21 and resetting the rest of the flip-flops when both RDGATE and WRTGATE are low prior to the initiation of a write operation. The phase counters cannot be clocked until the write enable (WRTENABLE) latch is set. The microprogram raises the write gate in concert with the position on the disk pack where data is to be written.

The first CLKTRIG after WRTGATE goes high sets the start latch (SERCONT high). SERCONT/ goes high with the next DATATRIG and sets the write enable latch. During the same DATATRIG time after the write enable latch is set, the PH10 through PH17 counter is clocked once; PH12 is set since PH21 was previously set. When CLKTRIG is again high, the PH20 through PH27 counter is clocked once, and PH22 is set. This alternate clocking of the phase counters by DATATRIG and CLKTRIG continues until WRTGATE goes low, which resets the start and write enable latches.

The two AM bytes and the sync byte are written before any data bytes. The microprogram determines when the AM bytes are to be written and enters data (all ones) into the DR register. The contents of the DR register are transferred to the FDR during the overlapping period of PH10 and PH20 when OSC/ is high (DRXFDR/ low). DRXFDR/ also causes ST4 to set, indicating that the data has been transferred from the DR register and that the next byte of data can be placed in the DR register. As the PH20 through PH27 counter is clocked, the corresponding data bits in the FDR are gated into the WRTDATA line and then gated to the WRTOUT line by high DATATRIG, WRTGATE, and OSC/ signals. Clock bits are interspersed with the data bits by high CLKTRIG and WRITEAM/ signals. Clock bits are inhibited for bit periods that would have been clock bits 1 through 5 of both AM bytes (WRITEAM/ low).

As data passes through the ALU, parity is generated and placed in the parity bit of the DR register (DRP) and subsequently transferred to the FDR parity flip-flop. Since parity bits are not written on the disk pack, the parity bit as well as the data bit output (DATAOUT/) clock the error detect flip-flop (FF C10). When FDR0 through FDR7 contain an even number of data bits, the parity flip-flop will be set. The 0 output of the parity flip-flop will be low; therefore, it cannot clock the error detect flip-flop. However, the DATAOUT/ signal will clock (D-CLOCK) the error flip-flop an even number of times. Initially, the error detect flip-flop was set by WRTGATE low. At the end of each byte, the error detect flip-flop must end up in the set state; otherwise, a serial write data error will be indicated (SETERR0/ low) at SETST4 time (DRXFDR time). When the number of data bits in FDR0 through FDR7 is odd, the parity flip-flop will be reset.

With the parity flip-flop reset, the 0 output will clock the error detect flip-flop once at CLKTRIG time during PH11, and the DATAOUT/ signal will clock the error

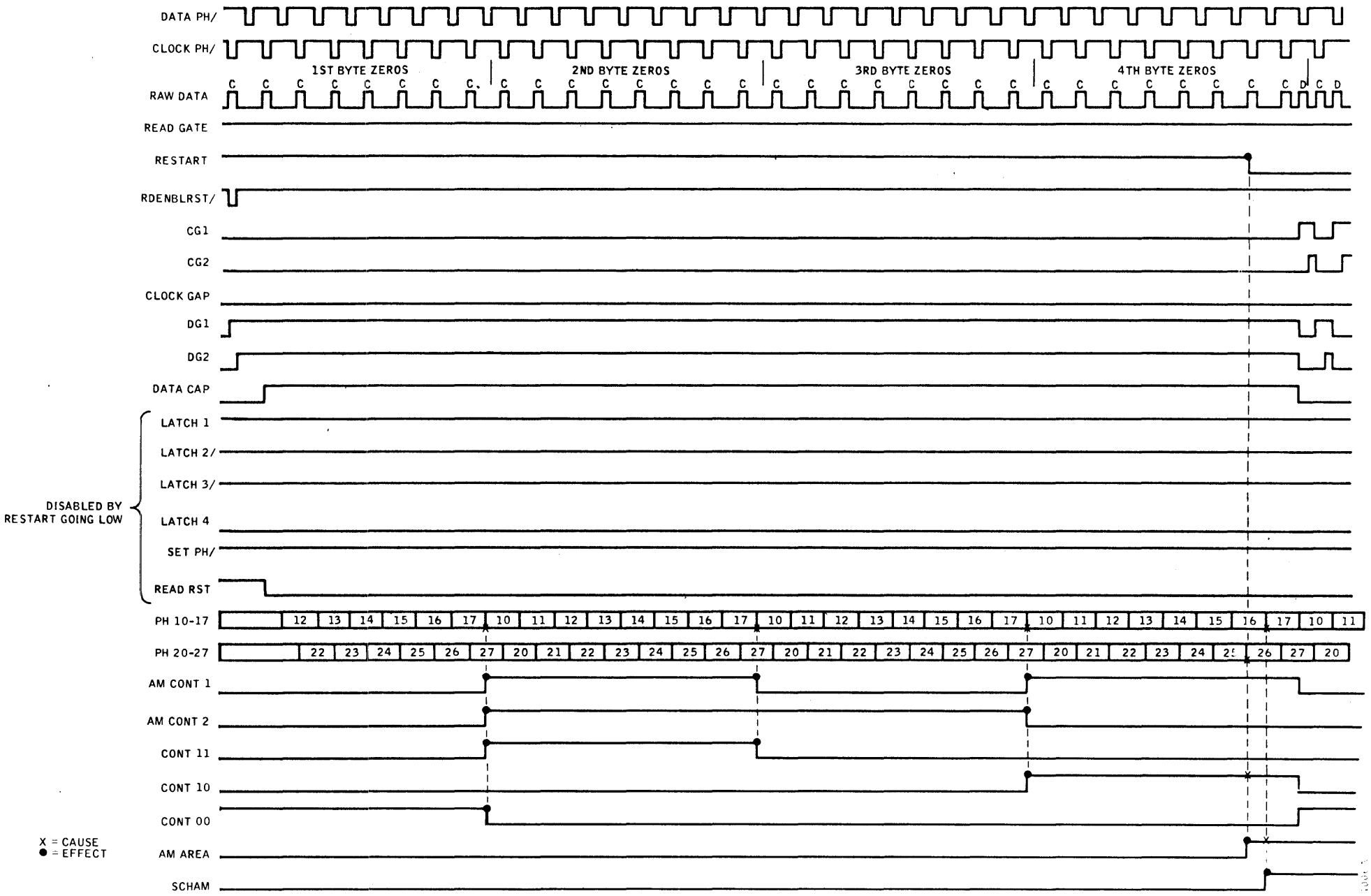


Figure 2-16. Read Timing Diagram (Sheet 1 of 2)

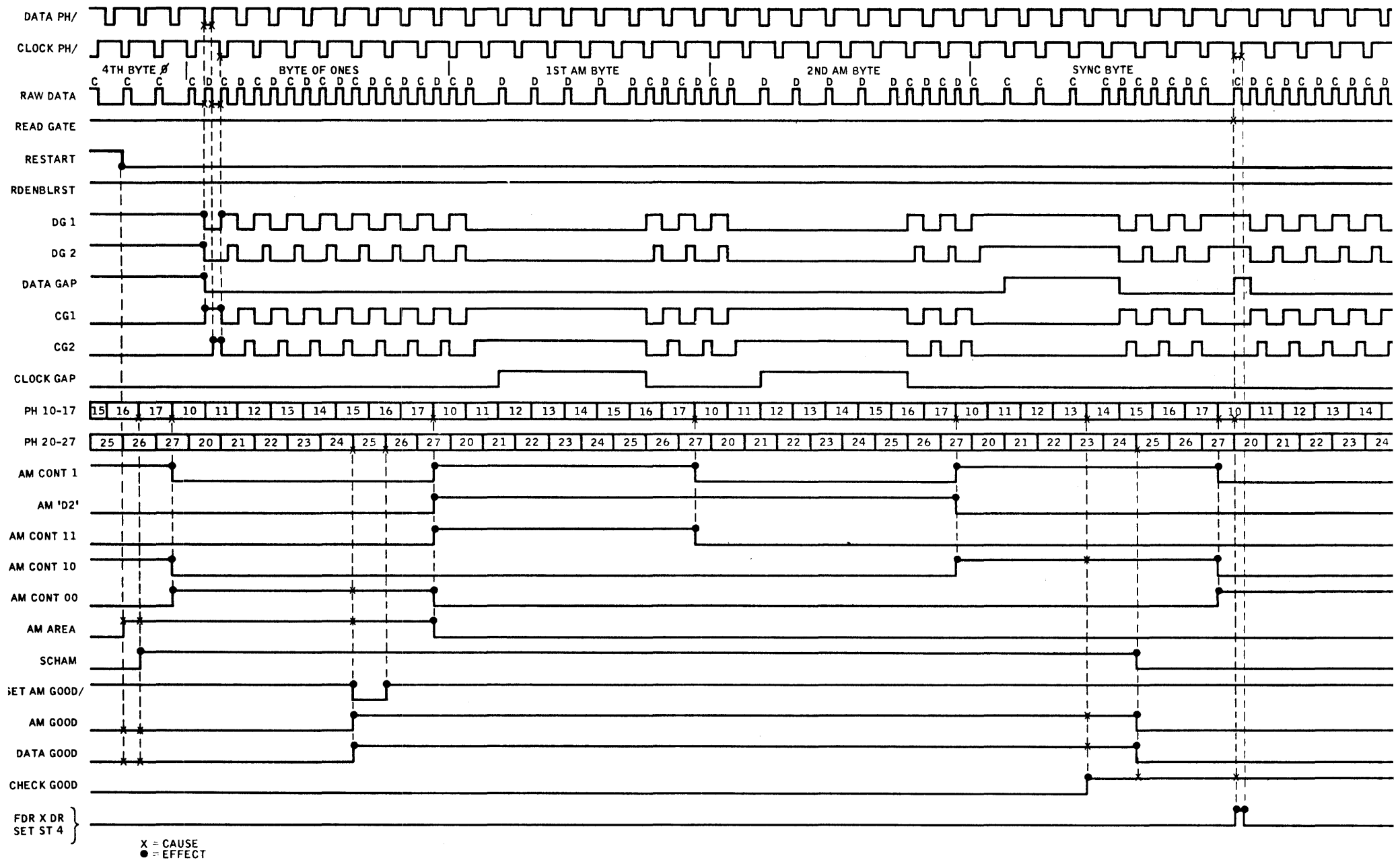


Figure 2-16. Read Timing Diagram (Sheet 2 of 2)

Figure 2-17. Write Timing Diagram (Sheet 1 of 2)

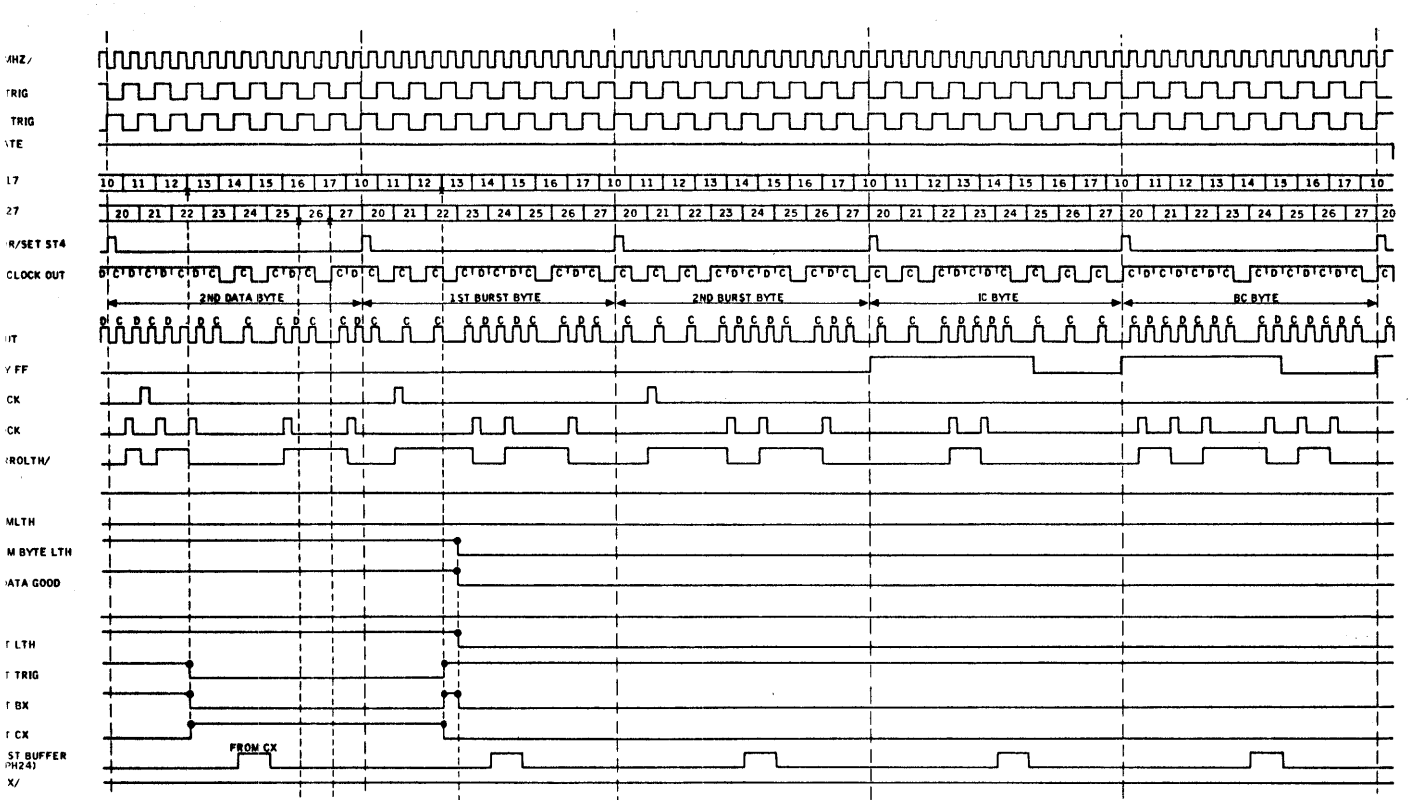


Figure 2-17. Write Timing Diagram (Sheet 2 of 2)

detect flip-flop an odd number of times. This combination of signals clocks the error detect flip-flop an even number of times.

During a write operation, the number of data bits written are counted by the modulo 256 bit counter (BC) and then written as the last bye of a record. The bit count is used as part of the error detection system. During a read operation, the number of data bits read are counted and then compared to the last byte of the record. The two should match; if not, a data check error is indicated.

BURST REGISTER AND BIT COUNTER (SERDES-4)

The burst register, burst latch, and burst trigger are used in burst check operation as are the BX and CX register (see REG-7). The bit counter counts all data bits in the sync byte, data field bytes, and first burst byte. The resultant bit count (modulo 256) is added to the data record as the last byte.

Burst Check Operation

No burst check operation takes place until the burst latch is set. During read operation, the burst latch is set at PH22 after the read data is determined to be good (R/W DATAGOOD high) and the microprogram has raised the allow-burst line (FT4 high).

The initial state of the burst trigger flip-flop determines which burst register (BX or CX) will be used first. Since the BX register must always be finished first with its burst operation at the end of a data field, the burst trigger flip-flop is initially set (R/W DATAGOOD low). This will allow the CX register to be used first (odd-length record). If the microprogram determines that the record length is even, it causes FT6 (even-length record) to go high and reset the burst trigger flip-flop after R/W DATAGOOD goes high, but before the burst latch is set at PH22 (see Figure 2-17). At the following PH13, the burst trigger is clocked to the opposite state to allow the burst operation to start with the BX register. The microprogram must initialize the BX and CX registers to all ones before the burst latch is set. The burst trigger changes state each PH13 time. The content of the BX or CX register, depending on the state of the burst trigger, is loaded into the burst buffer register at PH24 time. The output of the burst buffer register is exclusively ORed with the output of the FDR. During read operation, the result is set back into the BX or CX register (SETBX/ or SETCX/ low) at the CLKPH/ portion of PH10. During write operation, the result is set at PH26.

The microprogram determines when the complete record has been read. At this time, the first burst byte is exclusive-ORed with the residue contained in the BX register. The result should be zero; if not, a data check occurs. The second burst byte is exclusive-ORed with the residue contained in the CX register. The result should be zero; if not, a data check occurs.

During a write operation, the microprogram determines when the burst residue in the BX and CX registers is to be written. The residue in the BX register is transferred to the DR register and subsequently to the FDR. When the transfer has occurred, the residue in the CX register is then transferred to the DR register to be written as the second burst byte. When the CX register residue is transferred to the DR register, the CXXDR signal goes low, causing the second AM latch (see SERDES-2) to reset, which, in turn, resets the R/W data good latch. A low R/W DATAGOOD signal resets the burst latch.

Bit Count

Two additional bytes are written after the two burst bytes of each data field. The first byte is the indicator (IC) byte which consists of two segments: the first four bits define the controller address; the last four bits define the address of the disk drive that wrote the field. This byte is formulated by the microprogram from the wired controller address and from the disk drive address contained in the UR register.

The second byte is the bit count (BC) byte. The BC byte contains the complement of the total number of data bits contained in the sync byte, in the data field bytes, and in the first burst byte.

The BC enable latch (input latch to the BC advance latch) is set by the low R/W DATAGOOD signal with the BC advance latch reset. When the R/W DATAGOOD signal goes high at PH14 of the sync byte, the BC advance latch is set, which allows the data bits (BCCLK) to clock the bit counter. Initially, the bit counter is reset when both the RDGATE and WRTGATE are low. When several records are written consecutively, low WRITEAM/ and RDGATE signals reset the bit counter before the start of each data field. When the microprogram determines that the first burst byte has been written, the BC enable latch is reset by low CXXDR. The BC advance is then reset (SETST4 high) at PH20 of the second burst byte. After the IC byte has been transferred from the DR register to the FDR (during write operation), the microprogram issues a transfer command (SAXBC high), which causes the complement of the bit count to be routed to the DR register through the A bus, A register, and ALU bus. When it is time to write the bit count, it is transferred to the FDR. During read operation, the complement of the bit count is compared to the content of the BC byte. The result should be zero.

The high SAXSL signal allows the drive-selected signals (CMSB through CMSJ) to be entered on the A bus. Only one drive-select line may be high at any one time. Because each of the nine disk drives may be assigned any of the eight drive addresses, the microprogram statement (SAXSL) enters the drive-selected signals on the A bus

for use by the system program to identify the disk drive. This information is contained in sense byte 4. CMSA is entered on A bus bit 4 when the SA field equals 15.

DISK DRIVE INTERFACE INPUTS (DDI-1)

The disk drive interface input circuits contain the seek complete (SC) gates (CGA0 through CGA7 and CGASM), the drive-selected (DS) gates (CMSA through CMSJ), the module select error circuit, the old address (OA) gates, and the file status (FS) gates.

The SC gates relay gated attention (seek complete) signals from the disk drives to the A bus. In addition to the output of the A bus, all gated attentions are ORed (see CI-7 and CI-8) and applied to bit 7 of the interface status (IS) gates (see STAT-1) so that the microprogram can test IS7 for gated attention before testing the individual bits of the SC gates. The gated attention signals are also routed to the channel interface function (see CI-5) where they cause the request-in scan control line (see CI-7 and CI-8) to be assigned to the channel if the poll enable latch (IG4) is set and the channel is not selected for another controller.

The DS gates identify the disk drive that is selected and are used in gating the read/write data between the disk drive and the serializer/deserializer in the controller.

The drive select error detection circuit determines when more than one drive responds to a module select address. If this occurs, a module (drive) select error (MSELERR high) is routed to bit 6 of the FS gate input to the A bus for subsequent test by the microprogram.

The OA gates route the existing (old) cylinder address in the disk drive to the A bus for use in determining a difference count between the old cylinder address and a new cylinder address.

The FS gates route disk drive status from the selected drive to the A bus. The following chart identifies the status represented by each bit.

FS Bit	Status
0	Busy (CBSY)
1	Online (COL)
2	Unsafe (CUSF)
3	Write Current Sense (CWCS)
4	Pack Change (CPC)
5	End of Cylinder (CEOC)
6	Module Select Error (MSELERR)
7	Seek Incomplete (CSIN)

The unsafe status, the module select error status, and the seek incomplete status are error conditions. The end-of-cylinder status indicates that an attempt was made to advance the head advance register in the selected drive past a count of 19. The write current sense status is checked by the microprograms during a write operation to ensure that write head current is flowing. The not busy (CBSY low), online (COL high), safe (CUSF low), and not-at-end-of-cylinder (CEOC low) signals are ANDed to generate the file operable signal that is routed to IS gate bit 5 (see STAT-1). The microprogram tests IS5 (BIT50P signal—see STAT-1) to determine the operability of the selected disk drive. If IS5 is not set, the microprogram looks at the individual signals to determine the condition that caused the disk drive to become inoperable.

MODULE SELECT (DDI-2)

The module select gates (UMS0 through UMS7 and UMSSM), under control of FT7 (MOD SELECT), determine which module (disk drive) is to be selected for an operation. Only one module select line can be active (low),at any one time. The module selected is determined by decoding the four LSB bits of the unit address (UR) register.

FC AND FT REGISTERS (DDI-3)

The FT register identifies the type of data being sent to the disk drive from the FC register. Only FT bits 0 through 3 (tag lines) are sent to the disk drive, and only one tag line can be active at a time. FT bits 4, 6, and 7 are used within the controller to identify various functions. FT4 indicates to the controller when to write an address mark or when to allow burst operation. FT6 indicates to the controller that the number of bytes in a record is even. FT7, when active, enables the MS gates. Inputs to the FT register are from the ROM (SN5) and from the ALU bus. The input from the ALU bus determines the FT bit to be set, and the SN5 input enables all bits of the register.

The FC register transfers operating information to the disk drive under the control of the FT register. The following chart indicates the type of information transferred to the disk drive for specific tag lines.

The inputs to the FC register are from the ROM (SN5) and from the ALU bus. The inputs from the ALU bus determine the FC bit to be set, and the SN5 input enables the register.

When the POWER signal applied to the direct set (S) inputs of the FC and FT register bits goes low due to a voltage malfunction (see PWR-1), the two registers are reset. In these two registers, the 1 output is active when it is low.

Bus Line	Function			
FC0	Write Gate	Cylinder 128	Forward	128
FC1	Read Gate	Cylinder 64	Select Lock Reset	64
FC2	Seek Start	Cylinder 32	– – –	32
FC3	Reset Head Register	Cylinder 16	Head Address 16	16
FC4	Erase Gate	Cylinder 8	Head Address 8	8
FC5	Select Head	Cylinder 4	Head Address 4	4
FC6	Return to 000	Cylinder 2	Head Address 2	2
FC7	Head Advance	Cylinder 1	Head Address 1	1

Tag Line	Function
FT0	Control
FT1	Set Cylinder
FT2	Set Head
FT3	Set Difference (in complement form)

The block file interface signal (BLKFLINT/), when low, inhibits the FC and FT registers. If SETFC01/ through SETFC67/ or SETFT01/ through SETFT67/ go low while BLKFLINT/ is low, the respective register is reset (1 output goes high). The BLKFLINT/ signal goes low when an SAR error or ROMAR error (CONTERR high) is detected during a machine reset (MACHRST; 1 high) or when the write gate (WRTGATE high) is up as the index on the disk pack is detected (CIDX high). When an index mark is detected, the microprogram must drop the write gate so as not to write through the index portion of the disk pack.

TEST SELECT (TEST-1)

The output of the three START ADDRESS switches (S11 through S13–LSB through MSB respectively) are hexadecimally coded and provide a hexadecimal address range of 000 to 7FF which corresponds to the 2,048 different addresses contained in the ROM. The START ADDRESS switches are used during the test mode of operation (TEST/NORMAL/IN LINE switch set to TEST) to select the starting ROM address for the test to be performed. The ROM address is entered into the read-only memory address register (ROMAR) under the control of the SET ADDRESS switch. The two LSB START ADDRESS switches are also labeled as DATA switches. The START0 through START7 outputs of the DATA switches form a two-digit hexadecimal code that can be entered into any register selected by the REGISTER SELECT switch when the ENTER switch is pressed. Data entry from the DATA switches can be accomplished only during the test mode when the machine is stopped.

The output of the three STOP ADDRESS switches (S15 through S17–LSB through MSB, respectively) are hexadecimally coded and provide a hexadecimal address range of 000 through 7FF, which corresponds to the total number of addresses in the ROM. In the test mode and with the MODE SELECT switch set to RECYC, the settings of the STOP ADDRESS switches determine the ROM address at which the ROM will recycle to the ROM address set into the START ADDRESS switches. By this means, a program loop can be maintained between the start and stop ROM addresses. In the test mode and with the MODE SELECT switch set to STOP, the microprogram will be stopped at the address set into the STOP ADDRESS switches. In all modes of operation (test, normal, or inline), the exact comparison between

the ROM address and the setting of the STOP ADDRESS switches is used as a sync signal, which is accessible at the STOP ADDRESS SYNC test point (see TIM-3).

The TEST/NORMAL/IN LINE switch (S1) determines the mode of operation for the controller. In the TEST position, all test panel switches are operational. In the NORMAL position, only the CHECK RESET switch, DRIVER DEGATE switch, and the lamp test (LTTESTSW/) portion of the RESET & LAMP TEST switch are operational. In the IN LINE position, the same switches are operational as for the NORMAL position, plus the LOAD, RTN, RSLT, and ERR positions of the MODE SELECT switch.

The ENTER switch (S4) is active only during test mode while the machine is stopped to transfer data set into the DATA switches to the register selected by the REGISTER SELECT switch. The INNER and OUTER positions of the ENTER switch correspond to the inner and outer rings of the REGISTER SELECT switch dial.

The DISPLAY switch (S5) is active only during test mode while the machine is stopped to enable the display (on the REGISTER DISPLAY indicators—see TEST-2) of the contents of the register selected by the REGISTER SELECT switch. The INNER and OUTER positions of the DISPLAY switch correspond to the inner and outer rings of the REGISTER SELECT switch dial.

When the RESET & LAMP TEST switch (S6) is pressed while the controller is operating in the test mode, all registers are reset and all test panel indicators are lit. The test panel indicators remain lit until the switch is released. When the switch is pressed while the controller is operating in either the normal or inline mode of operation, only the lamp test feature (LTTESTSW/) is operational.

The SET ADDRESS switch (S7) is active only during test mode to transfer the hexadecimal ROM address, set into the START ADDRESS switches, into the ROMAR.

The START switch (S8) is active only during test mode to initiate the controller operation defined by the setting of the CHK STOP/RUN/SINGLE STEP STOP switch.

The CHK STOP/RUN/SINGLE STEP STOP switch (S9) is active only during test mode to enable the following functions: In the CHK STOP position, the controller will stop on a detected error. The ROM address of the microinstruction for which the error was detected will be displayed in the ROMAD indicators. In the RUN position, the controller runs in a normal manner as determined by the setting of the MODE SELECT switch. In the SINGLE STEP STOP position, one microinstruction is executed each time the START switch is pressed.

The CHECK RESET switch (S10) is active in all modes of operation. When this switch is pressed, any error latch that was set is reset, and the associated CHECKING indicator is turned off.

The DRIVER DEGATE switch (S19) is active in all modes of operation. When this switch is set to ON, the bus-in and tag-in lines to the channel are disabled. The SELREC output of the switch is low when the switch is not in the ON position. With SELREC low, SELREC;W is also low, which energizes one of the select-out relays in the channel interface function (see CI-2 and CI-3). The controller should be degated only when the interface is disabled.

The MODE SELECT switch (S14) is an eight-position switch that controls the testing of the controller or of the spare disk drive. When the TEST/NORMAL/IN LINE switch is set to TEST, any of the eight positions of the MODE SELECT switch may be used. When the TEST/NORMAL/IN LINE switch is set to IN LINE, only the LOAD, RTN, RSLT, or ERR positions are operable.

The CHANNEL A enable switch controls the interface between the controller and channel A. When the switch is pressed and the internal indicator is lit, the controller is enabled to communicate with the channel if the enable latch is set. When the internal indicator is not lit, the controller is effectively disconnected from the channel if the enable latch is reset.

In two-channel controllers, the CHANNEL B enable switch performs the same function for channel B as the CHANNEL A enable switch does for channel A.

In two-channel controllers, the TAG switch controls the tagging of unsolicited interrupts. The manner in which a device end, resulting from a not-ready-to-ready sequence is presented is determined by the setting of the TAG switch. When the switch is in the tagged position (internal indicator lit), device end for the not-ready-to-ready sequence is presented to both channels. After the device end is accepted, the drive can be addressed for command execution by the channel that accepted the device end. Before the other channel can address the drive for command execution, it must also receive the device end not-ready-to-ready sequence. When the switch is in the untagged position (internal indicator not lit), the device end not-ready-to-ready sequence is presented to both channels. The device end is cleared when it is accepted by either channel, and no further attempt is made to present the device end to the other channel.

The CHANNEL B and TAG switches are not part of single-channel controllers.

REGISTERS DISPLAY (TEST-2)

The register display circuits display the contents of the register selected by the REGISTER SELECT switch during test mode when the machine is stopped.

The outputs of the REGISTER SELECT switch (S18), REGSEL 1 through REGSEL 4—MSB through LSB respectively, form a hexadecimal code that corresponds basically to A bus source and ALU destination codes of the ROM (SA and SD fields, respectively). The following chart indicates the hexadecimal code generated by the REGISTER SELECT switch and the register that is selected for display on the REGISTER DISPLAY indicators.

When the DISPLAY switch is pressed to INNER (DISPINSW/low), signals DISP1X through DISP3X go high, causing the display multiplexers to select the A bus signals (ABUS0 through ABUS7) for display. Likewise, when the DISPLAY switch is pressed to OUTER (DISPOUTSW/ low), signals DISP1X through DISP3X go high for register select counts of 1 through 7 (REGSEL1 low) to select the A bus signals for display. For register select counts of 9 through E (REGSEL1 high), the register selected is determined by the octal configuration of the DISP1X (LSB) through DISP3X (MSB) inputs to the multiplexers. The display parity signal (DISPP/) is generated on ALU-2(2). The lamp test signal (LTTESTSW/), when low, tests all the indicators on the test panel.

ERROR AND ROMAR DISPLAY (TEST-3)

The error and ROMAR display function displays the present ROM address and any error that occurs during operation.

Error Display

Error or check conditions detected during operation and displayed by the CHECKING indicator consist of the following: sense amplifier error, ROM address error, probe check, data error (bus-out, ALU, or serial write data), and machine stop.

REGSEL Hexadecimal Count	Register Displayed		
	DISPLAY INNER Switch Pressed	DISPLAY OUTER Switch Pressed	DISPLAY Switch in Neutral Position
0	–	–	DISP
1	GL*	DR*	Note: DISP register is displayed when DISPLAY switch is neither in INNER nor OUTER. REGISTER SELECT switch can be in any position.
2	BY*	DW*	
3	FR*	BX*	
4	KL*	CX*	
5	DH*	ER	
6	DL*	FS	
7	OP*	OA	
8	GP*	–	
9	SP*	A	
A	UR*	B	
B	IE	ALU/	
C	SW	FC	
D	SC	FT	
E	IH*	ST	
F	IS	A BUS	

*Parity bit displayed

The SENSE AMP indicator is lit when a parity error (SARERR high) is detected in the sense amplifier register (SAR). The controller will stop operation (SARERR/ input to the inhibit circuit–TIM-3 and to the stop ROMAD circuit–ROM-2) in all modes of operation. When the controller is stopped for a sense amplifier parity error, the data word content of the SAR will be that which caused the parity error, and the ROMAR will contain the address of that data word. The SARERR latch can be reset either by a machine reset (MACHRST; 1 high) or by pressing the CHECK RESET switch (CKRSTSW/ low).

The ADDRESS indicator is lit when a parity error is detected (RADERR/ low) when the ROMAR parity and the parity bit (PABF) read from the ROM do not match (see ROM-1). The controller will stop operation in all modes of operation.

The CONTERR signal is a logical ORing of the sense amplifier error signal and the ROMAD error signal. When CONTERR is high, the interface with the disk drives is blanked and conditions the operational-in latch (see CI-2 and CI-7) so that a selective reset will be generated on the next initial selection by a channel.

The PROBE indicator is lit whenever the ROM address matches the address that is set into the STOP ADDRESS switches (STEPQ high). When jumpers are connected to any of the auxiliary inputs to the probe latch, these signals must also be high (or low for FALSESIGNAL input) for the PROBE indicator to light. When the controller is operating in the test mode and the CHK STOP/RUN/SINGLE STEP STOP switch is set to CHK STOP, the controller will stop operating when the probe latch sets (PRBLTH/ low activates the inhibit circuits–see TIM-3). The probe latch is reset by a machine reset (MACHRST; 1 high) or by pressing the CHECK RESET switch (CKRSTSW/ and RSTPROBE low).

The DATA indicator is lit when a serial data error occurs (ER0 high), when a bus-out parity error is detected on command or data bytes (ER2 high), or when an A register parity error occurs (ER4 high).

The MACHINE STOP indicator is lit whenever the controller is inhibited (INHIBITA high). When the controller is operating in the normal or inline mode and the MACHINE STOP indicator is lit, the controller will stop operating. When in the test mode, the controller will stop only if the CHK STOP/RUN/SINGLE STEP STOP switch is set to CHK STOP.

ROMAR Display

The ROMAR indicators display the hexadecimal ROM address plus parity. The parity bit (PABF) is derived from the memory data word read out for that specific ROM address.

POWER CONTROL (PWR-1)

The power control circuits control the application of power to the controller and to the attached disk drives. In the normal and inline modes of operation, power turn-on and turn-off is controlled by the CPU. In the test mode of operation, power turn-on and turn-off is controlled from the controller test panel.

Input power to the controller is 208/230 vac, 3-phase for 60 Hz machines. For 50 Hz machines, refer to the Instruction Manual for correct power hookup.

Power-Up Sequence

When the CPU is to power up the controller and attached disk drives, the MAIN POWER circuit breaker must be set to ON to apply power to the 24 vac transformer in the power supply.

Under normal conditions, the emergency-power off (EPO) control signal (24 vac) from the CPU will be present to activate EPO relay K1. In two-channel controllers, either channel can activate relay K1.

The channel initiates the power-up sequence by placing 24 vac on the power pick line. The power pick signal energizes sequence relay K2 through contacts of switch S1 on the test panel and through contacts 8 and 5 of energized relay K1. Ac power relay K3 is immediately energized and applies ac power to the power supplies and to the disk drives. When relay K2 operates, power hold relay K7 is energized by the power hold signal (24 vac) through contacts 4 and 7 of relay K2 and contacts of switch S1. With relay K7 energized, relay K2 will remain energized even though the power pick signal from the channel is removed. Relay K2 is held energized by 24 vac through contacts 8 and 5 of relay K7 and through operated contacts 8 and 5 of relay K1.

When relay K3 operated, ac power was applied to the power supplies, and the output voltages of the power supplies are applied to the power monitor circuit. If all voltages are within tolerance, the controller will immediately sequence up. A 20 ± 2-second delay circuit in the power monitor circuit is enabled if power is lost for more than two milliseconds to allow time for the disk drives to sequence down before they are enabled to again sequence up. The output of the power monitor circuit (POWER/) goes low if all input voltages are within tolerance and causes dc power-up relay K4 to energize. Relay K4 is energized by a relay driver (DCPWRUP/; W low) through contacts 9 and 6 of energized relay K7 and through contacts 7 and 4 of energized relay K1. With relay K4 energized, a controlled ground (CCNGND) signal is routed to the disk drives to initiate their turn-on sequence. Three seconds after relay K4 is energized, 3-second delay relay K5 (and relay K8 in two-channel controllers) energizes and sends a power complete (PWR COMPL) signal to the channel. Additionally, relay K5 sends a logic start signal to the

controller timing circuits, which resets the controller circuits to an initial starting point prior to commencing operation.

The power-up sequence in the test mode of operation is similar to that in the normal or inline mode of operation. In the test mode, the power-up sequence is initiated by pressing the POWER ON switch. The power hold relay is energized, which, in turn, energizes sequence relay K2 through contacts 8 and 5 of energized relay K1. The remainder of the power-up sequence is identical to that for the normal or inline mode of operation.

Power-Down Sequence

In normal or inline mode of operation, the CPU initiates the power-down sequence by dropping the power hold signal; this deenergizes power hold relay K7. When relay K7 is deenergized, dc power-up relay K4 and 3-second delay relay K5 (and K8 in two-channel controllers) deenergize. With relay K7 deenergized, sequence relay K2 will be deenergized if the read/write heads in all attached disk drives are retracted (CHEXT high). If any disk drive has its read/write heads extended (CHEXT ground), heads-extended relay K6 will be energized to keep relay K2 in the energized state. With relay K2 energized, ac power relay K3 also remains energized to supply ac power to the disk drives until all read/write heads are retracted to allow relay K6 to deenergize. With relay K6 deenergized, relays K2 and K3 also deenergize.

In the test mode of operation, the power-down sequence is initiated by pressing the POWER OFF switch on the test panel. This causes power hold relay K7 to deenergize. The remainder of the power-down sequence is identical to that for normal or inline mode of operation.

Emergency Power Down

The computer system operator initiates an emergency power down by pulling the EMERGENCY PULL control at the CPU. This causes EPO relay K1 to deenergize. With relay K1 deenergized, all relays are deenergized, thus disconnecting all power from the controller circuits and from the disk drives.

SECTION 3
MODEL 1015 DUAL DENSITY CONTROLLER

The Model 1015 Dual Density Disk Storage System comprises a 1015 Dual Density Controller and a combination of Model 215 and Model 213 Dual Density Disk Drives.

The 215 disk drive contains two spindles. Each disk pack on a 215 disk drive contains 406 cylinders (double that of a CD22). The 213 disk drive contains one spindle which is identical to a spindle in a 215. When a spindle or the 215 disk drive is mentioned, it applies to the 213 disk drive as well.

In the 1015 system, each spindle of a 215 disk drive is organized into two logical modules (one having an odd-numbered address and the other having an even-numbered address); each responds to a different module address (see Figure 3-1). The cylinder tracks of the two logical modules on one physical spindle are interleaved (that is, the odd-numbered cylinders of 406 total cylinders are associated with the odd logical module and the even-numbered cylinders are associated with the even logical module); thus each logical module contains 203 cylinders (equal to that of a CD22 spindle).

The 1015 Dual Density Controller is essentially a CD14 Controller modified to incorporate the 406-cylinder, Model 215 disk drives into the 1015 Dual Density Disk Storage System. A maximum of four online spindles (eight logical modules) and one spare spindle can be controlled by the 1015 controller.

The 1015 Dual Density Disk Storage System is plug interchangeable with the CD14/CD22 Disk Storage System and is connected to a System/360 Model 30 and up or System/370 selector channel.

PHYSICAL DIFFERENCES

The main physical difference between the 1015 controller and the CD14/CD14A Controller is the addition of an operator panel to the front of the controller (The test panel is at the back of the controller.) The operator panel contains the disk drive identification plugs. (The identification plugs in a CD14/CD22 system are located on the respective drives.) Each identification plug is double detented; that is, one detent corresponds to one of the two logical modules occupying a spindle. Eight DRIVE STATUS switches, located on the operator panel, are used to place the eight respective online logical modules either online or offline. In the CD14/CD22 system, this function was performed at each disk drive by removing (offline) or replacing (online) the identification plug. Additionally, the CHANNEL STATUS switches (Channel A and Channel B enable switches and the TAG switch) as well as the elapsed time meter are located on the operator panel. Unlike the CD14/CD14A, the CHANNEL STATUS switches on the 1015 are not lit when they are enabled.

The input/output panel differs in that only five DC CABLE connectors are provided in the 1015 controller – one for each disk drive spindle.

One new, additional B-series circuit board is used in the 1015 controller; that is the reference register circuit board located in slot A/B-1. This circuit board contains

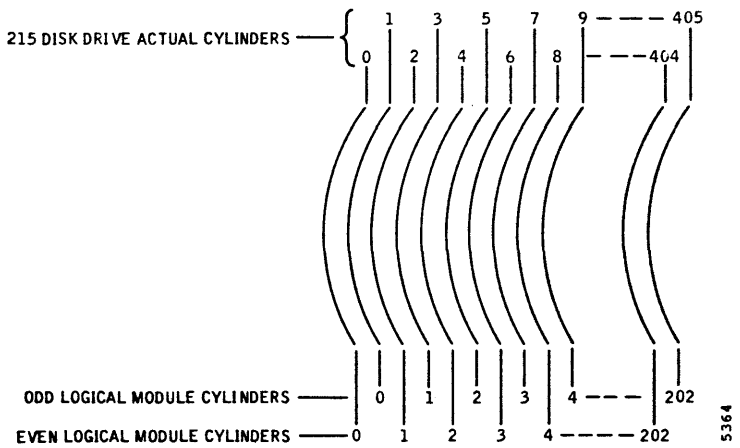


Figure 3-1. Logical Module/Actual Cylinder Representation

one 8-bit cylinder reference register and one 8-bit head reference register for each logical module. These registers store the latest issued cylinder and head addresses for each logical module.

DATA ORGANIZATION

Since the two logical modules occupying one spindle are serviced by one set of read/write heads, the organization of customer data sets is the primary consideration affecting disk drive access timing. To provide performance comparable to that of the CD14/CD22 system, the following items should be considered:

- Highly active data sets should be placed on different physical spindles to avoid head contention between the two logical modules on the same spindle.
- If two highly active data sets must be placed on the same spindle, they should be interleaved (placed on different logical modules of the same spindle) so as to occupy the same relative cylinder address.

MICROPROGRAM DIFFERENCES

The ROM contains basically the same microprograms as the ROM of the CD14 but with added features to test the additional circuitry within the 1015 controller, to perform inline diagnostic routines on the 215 disk drive, and to perform the added main line control functions required of the 1015 controller.

RESIDENT DIAGNOSTICS

The added resident diagnostic routines are divided into two groups: one that tests for the proper operation of the DRIVE STATUS switches and their associated logic, and the other that tests the head reference registers and the cylinder reference registers.

The test for the DRIVE STATUS switch operation is not chained to any resident diagnostic routine; it is a freestanding test that is initiated at memory location 773 (hex).

The head and cylinder reference registers test is chained to the resident diagnostic tests for the ALU, for the registers, for branching, and for the SW registers. This test starts at memory location 183 (hex) and ends at location 6F7 (hex).

INLINE DIAGNOSTICS

The inline diagnostic routines are performed in the same manner as they are in the CD14; however, the inline diagnostics are run over the entire 406 cylinders of the 215 disk drive. The inline diagnostic routines are run on the odd cylinders (odd logical module) when the TEST/NORMAL/IN LINE switch is set to TEST and on the even cylinders (even logical modules) when the switch is set to IN LINE.

MAIN LINE CONTROL

Since the 215 disk drive recognizes and responds to a 406-cylinder address (effective or actual address) and the operating system (CPU) uses a 203-cylinder address (reference or logical address), the 1015 controller performs the conversion. The conversion of the 203-cylinder address to a 406-cylinder address is performed by left-shifting the cylinder address (effectively doubling the address) in the controller under the control of the microprogram. If the addressed logical module is an odd module, the least significant bit of the left-shifted address (now a 9-bit address) is forced high. The most significant bit of the effective address is routed to the disk drive by FT3, which is high when the effective cylinder address is greater than 255. The reference cylinder address, of a 203-cylinder address, is stored in the cylinder reference register.

When a recalibrate command is issued, the disk drive returns to actual cylinder 0 or 1. The disk drive returns to cylinder 0 when the recalibrate command is issued to the even logical module. The disk drive returns to cylinder 1 when the command is issued to the odd logical module. When the recalibrate command (return to zero) is sent to the disk drive, the reference cylinder address and reference head address stored in the respective cylinder and head reference registers for the addressed module are reset to zero.

If the access mechanism in the disk drive misseeks by one cylinder into its companion module, a seek check is detected by sampling the least significant bit of the module ID byte. This seek check is sent to the channel.

During command decode, if a start I/O has just been issued and the command to be processed is not seek, seek cylinder, recalibrate, or read IPL, the last cylinder and head addresses stored in the respective cylinder and head reference registers for the module being addressed are reissued to the drive. If necessary, the drive access mechanism is repositioned before initial status is presented. This function is performed only during the decoding of the first command in a CCW chain.

LOGIC DIFFERENCES

The following paragraphs describe the differences between the 1015 and CD14/CD14A Controllers. The description of the differences are based on the referenced 1015 logic diagrams.

ATTENTION CONTROL (CI-5)

Each gated attention input signal (GA0 thru GA7) represents a logical module gated attention. The GA0 thru GA7 signals are derived from pack change and seek logic within the 1015 controller in conjunction with the

gated attention from the 215 disk drive (see DDI-5). In the CD14 Controller, the gated attention signals (CGA0 thru CGA7) from the disk drives (CD12 or CD22) were applied directly to the attention control circuits.

A BUS AND A REGISTER (ALU-2(1) AND ALU-2(2))

The cylinder address register inputs (CCAR0 thru CCAR7) to the A bus for *SA equals 23* in the CD14 Controller are replaced by reference address inputs (OA0 thru OA7) in the 1015 controller. The reference address may be the address of the reference cylinder, the reference head, or the cylinder address register. The selection of one of the three reference addresses is determined under microprogram control (see DDI-4).

READ-ONLY MEMORY ADDRESS REGISTER (ROM-1)

In the 1015 controller, the input to ROMAD bit 1 for *SH equals 7* is FT5. In the CD14 Controller, this input is grounded for one-channel operation, or connection to +5 STUB for two-channel operation. The FT5 (re-seek) flip-flop is set (FT5 high) by the initial command of a Chaining Command. High FT5 is used by the microprogram as a branching condition to enter the re-seek routine since the channel may have issued a seek command to the companion logical module since the last such command was issued to this logical module. Upon accomplishing the re-seek routine, FT5 is reset.

In the 1015 controller, the input to ROMAD bit 1 for *SH equals 12* is INLINESW/. In the CD14 Controller, this input is grounded. In the 1015 controller, this input determines the logical module on a physical spindle for which inline diagnostic routines will be performed. With the TEST/NORMAL/IN LINE switch set to IN LINE, INLINESW/ will be low and inline diagnostic routines will be performed on the even-numbered cylinders (even logical module). When this switch is set to TEST, INLINESW/ will be high and inline diagnostic routines will be performed on the odd-numbered cylinders (odd logical module).

READ/WRITE SELECT AND PHASE LOCK (SERDES-1)

In the 1015 controller, the read and write signals are routed between the controller and a disk drive over separate coax cables. Read signals (CRDA/;D thru CRDE/;D) are terminated in the controller, and write signals (UWRA/;D thru UWRE/;D) are terminated in the disk drives. Since only five disk drive units are connected to the 1015 controller, four unused inputs to the RAWDATA logic circuits are grounded.

BURST REGISTER AND BIT COUNTER (SERDES-4)

Since only five disk drive units (maximum) are connected to a 1015 controller as compared to nine (maximum) for a CD14 Controller, the four unused inputs to the drive selected/bit count logic (DSBC0 thru DSBC7) are grounded.

DISK DRIVE INTERFACE INPUTS (DDI-1)

The disk drive input signals to the 1015 controller are the same as those for the CD14 Controller with the following exceptions.

The gated attention signals (CGAA/;D thru CGAE/;D) from the five disk drive units are routed through identification plugs, located on the controller operator panel, where they convert drive unit gated attentions to logic module gated attentions. Each ID plug is doubled detented (i.e., two ID switches are activated when the ID plug is in place), except the one associated with the disk drive designated as the spare. The ID plug for the spare disk drive has but one detent. Upon receiving a gated attention from a disk drive, two gated attention signals are generated (one odd and one even; such as, CGA1/;D and CGA2/;D) because the gated attention signal generated by a disk drive is the logical sum of the gated attentions for the two logical modules occupying the same spindle. The logical module gated attention signals (CGA0 thru CGA7) are routed to the gated attention control circuits (see DDI-5), which determine whether the gated attentions (for both logical modules occupying the same spindle) are the result of a power-on seek or of a seek complete. If the gated attentions are the result of a power-on seek, both gated attentions are then routed to the A bus. If the gated attentions are the result of a seek complete, only the gated attention for the logical module that was previously issued a seek command is routed to the A bus. The 215 disk drive does not generate a gated attention as the result of a pack change, since the ID plugs of these disk drives are located on the 1015 controller. The generation of a pack change signal is a function of the DRIVE STATUS switches located on the operator panel (see DDI-5).

The module select error circuit in the 1015 controller operates in the same manner as in the CD14 Controller, but with only five module select inputs (CMSA thru CMSE). The remaining four inputs are grounded.

The CMSE, CID1, and CID2 signals are routed to DDI-5 for use in writing the identification on the disk pack of the disk drive unit used to write the ID byte. Signals CMSB/ ;D thru CMSD/ ;D develop a binary output (count 1 thru 3) at CID1 and CID2. CID1 is the least significant bit (LSB), CID2 is the second LSB, and CMSE is the third LSB of the ID byte.

MODULE SELECT (DDI-2)

The module select circuits operate in the same manner for the 1015 controller as they do for the CD14. However, the logical module is selected by decoding UR4 thru UR7. The double-dented ID plugs perform a wired-OR function so that when either the odd logical

module or the even logical module collocated on the spindle is selected, the respective module select signal (such as UMSA/:D) is activated. The spare module select signal (UMSSM/:D) is routed through the ID plug (single detent) associated with the drive designated as the spare.

The DRIVE STATUS switches, which are in series with the path for the logical module select signals, control the online/offline status of the disk drives. When the two DRIVE STATUS switches associated with a particular module are set to OFFLINE, that module cannot be selected by the controller. Individual logical modules may be placed offline by placing the respective DRIVE STATUS switch in the OFFLINE position.

FC AND FT REGISTERS (DDI-3)

The FC and FT registers operate basically in the same manner for the 1015 controller as they do for the CD14 Controller, except as follows.

Since the 215 disk drive requires a 406-cylinder address, a 9-bit address is required. The 215 disk drive generates its own cylinder difference count (this is done by the CD14 Controller in a CD14/CD12 or a CD14/CD22 system). Therefore, FT3 is not used as a set difference tag. Instead, FT3 is used as the MSB of the cylinder address, and FC0 thru FC7 are the second MSB thru LSB, respectively, as indicated in the following chart.

Bus Line	Function		
UB0 (FT3)	---	Cylinder 256	---
UB1 (FC0)	Write Gate	Cylinder 128	Forward
UB2 (FC1)	Read Gate	Cylinder 64	Select Lock Reset
UB3 (FC2)	Seek Start	Cylinder 32	---
UB4 (FC3)	Reset Head Register	Cylinder 16	Head 16
UB5 (FC4)	Erase Gate	Cylinder 8	Head 8
UB6 (FC5)	Select Head	Cylinder 4	Head 4
UB7 (FC6)	Return to 000	Cylinder 2	Head 2
UB8 (FC7)	Head Advance	Cylinder 1	Head 1

Tag Line	Function
UTCC (FT0)	Control
UTSC (FT1)	Set Cylinder
UTSH (FT2)	Set Head

In the 1015 controller as in the CD14 Controller, the disk drive tag lines are inhibited when the controller stops on an error. When the controller stops on an error, INHIBITA/ goes low to prevent the destruction of data on the track that is selected.

CYLINDER AND HEAD REFERENCE REGISTERS (DDI-4)

The cylinder and head reference register circuits are unique to the 1015 controller. The cylinder and head reference registers store the reference cylinder address and the reference head address that was last issued to the disk drive for each logical module.

The cylinder address reference registers are contained in four 4 x 4 register IC that form eight registers (one for each logical module) of eight bits each. The reference cylinder address (0 to 202) is stored in the reference register associated with the logical module selected at the time the actual cylinder address (0 to 405) is routed to the disk drive. The cylinder address reference registers store the eight MSB (AB0/ thru AB7/, which are FT3 and FC0 thru FC6 respectively) of the 9-bit actual cylinder address. Since the logical module cylinder address was left-shifted one bit (shifted one bit toward the MSB) to develop the 9-bit (406-cylinder) address, the eight MSB of the 9-bit actual cylinder address reflect the reference cylinder (203-cylinder) address. The ninth bit of the 9-bit address is disregarded by the cylinder address reference registers.

A 4 x 4 register IC is functionally represented in Figure 3-2. When data is to be stored in the register associated with logical module 0, the register write select logic inputs (WA and WB) are decoded (in the case of logical module 0, WA and WB are both low) to select the register for logical module 0 (CLKREG0 high). When the write gate (WG) goes low, data (ABO/ and AB3/) is entered into the register. In order to read data from the logical module 0 register, decoding of register output select logic (RA and RB) must cause

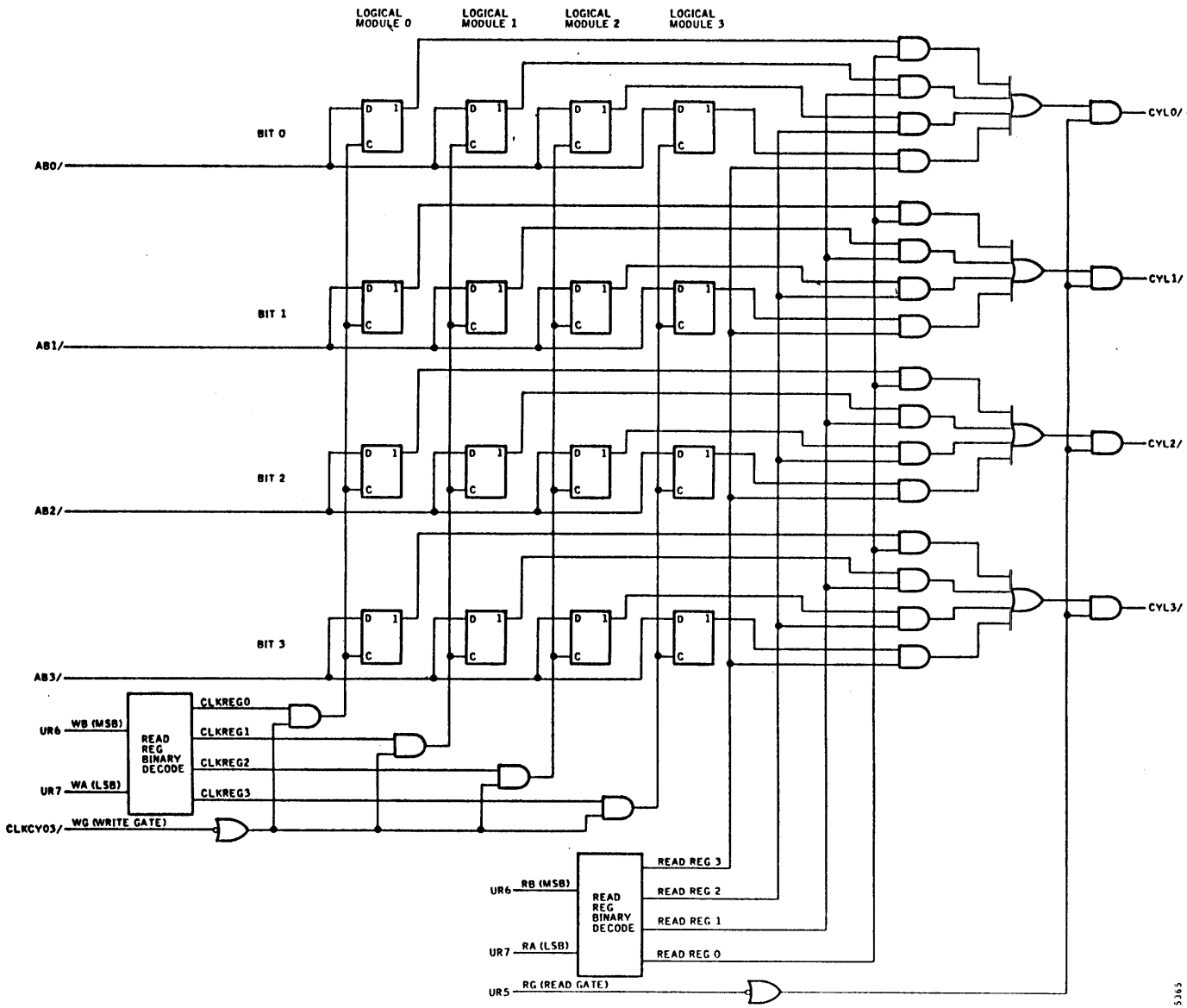


Figure 3-2. Typical 4 x 4 Register IC Functional Diagram

READREG0 to go high (RA and RB low) When the read gate (RG) goes low, data stored in the logical module 0 register is presented at the outputs (CYL0/ thru CYL3/) of the 4 x 4 register IC. The selection of other logical modules for data entry or data output is a function of the register write select logic and register read select logic respectively.

A reference cylinder address is normally entered into a logical module reference register as a function of the logical module address (binary decoding of UR5 thru UR7), the set cylinder signal (FT1 high), the module select signal (FT7 high), and the not-spare-module signal (UR4 low).

The head address reference registers are contained in four 4 x 4 register IC, that form eight registers (one for each logical module) of eight bits each. The head address stored in each of the reference registers is the actual head address for the respective logical module most recently issued (last issued) to the associated disk drive.

A head address is normally entered into a logical module reference register from the FC register through AB1/ thru AB8/ as a function of the logical module address (binary decoding of UR5 thru UR7), the set head signal (FT2 high), the module select signal (FT7 high), and the not-spare-module signal (UR4 low). Although eight bits are available for use in each head address reference register, only the five LSB are used. When a recalibrate command is issued, the control tag is activated (FT0 high) and identifies FC6 as a return-to-zero signal for the selected online logical module (FT7 high, UR4 low). The RTZ (return-to-zero) flip-flop is then set at T3, causing AB0/ thru AB8/ to go high. The high RTZ signal activates the write gate input logic for the associated cylinder and head reference group (CLKCY03/ and CLKHD03/ if the selected logical module is 0, 1, 2 or, 3 or CLKCY47/ and CLKHD47/ if the selected logical module is 4, 5, 6, or 7). In turn, the cylinder and head reference registers of the selected logical module are reset. Since the reference cylinder address and reference head address are stored in negative logic (low active), a reset causes all bits of the reference cylinder and head registers to go high. A recalibrate command is also generated by the pack change signal (CPC/ low) for a selected module.

A machine reset (MACHRST: 2 high) does not alter the content of either the cylinder address reference registers or the head address reference registers. The cylinder address register output (CCAR0 thru CCAR7), the reference head address output (HD0 thru HD7), the reference cylinder address output (CYL0 thru CYL7) of the disk drive, or the ID byte (CUADD0 thru CUADD3, CID1, CID2, and CMSE) is entered into the A bus when the SA field equals 23. In the CD14 Controller, only the cylinder address register output of the drive is entered into the A bus when *SA equals 23*. In the 1015 controller, conditions to select one of the four possible inputs for *SA equals 23* are enabled by the microprogram prior to its entry into the A bus. When the microprogram determines that the reference head address is to be entered into the A bus, it issues a destination statement of *SD equals 29*. This statement causes the CTLSD4 flip-flop to set at T1 (CTLSD4 high), which conditions the dual multiplexers to allow the reference head address to be applied to the A bus through outputs OA0 thru OA7. When the microprogram determines that the reference cylinder address is to be entered into the A bus, it issues a destination statement of *SD equals 30*, which causes the CTLSD3 flip-flop to set at T1 (CTLSD3 high). This conditions the dual multiplexers to allow the reference cylinder address to be gated through the dual multiplexers to the A bus through outputs OA0 thru OA7. Likewise, when the cylinder address register output (CCAR0 thru CCAR7) of the disk drive is to be entered into the A bus, a destination statement of *SD equals 28* is issued (CTLSD3 and CTLSD4 low) to place CCAR0 thru CCAR7 at the outputs of the dual multiplexers. When the ID byte (controller and drive address) is to be entered into the A bus, the microprogram issues a destination statement of *SA equals 31* to place the ID byte (CUADD0 thru CUADD3, CID1, CID2, and CMSE) at the outputs of the dual multiplexers. A machine reset signal (MACHRST:2) resets the CTLSD3 and CTLSD4 flip-flops which select the CCAR0 thru CCAR7 signals to be gated into the reference register outputs.

When the set seek latch signal (SETSK/) is low, the seek latch (DDI-5) for the selected module is set. SETSK/ goes low when seek start signal SKSTART/ is low (FC1 and FT7 high, and UR4 low) while recalibrate signal RECAL/ is low (FC6, FT0, and FT7 high, and UR4 low) or while the disk drive is busy (CBSY high).

GATED ATTENTION CONTROL (DDI-5)

The gated attention control circuits are unique to the 1015 controller. These circuits determine whether a gated attention from the disk drive is a result of power-up first seek or of a seek complete or the result of a logical module having been placed online (DRIVE STATUS switch for the respective logical module switched to ONLINE).

The two logical modules associated with a single spindle must have two separate addresses, one even and one odd. The combination of odd and even modules on a spindle may be of any configuration. For example, logical module 0 may have as its odd companion logical module, logical module 1, 3, 5, or 7. The determination of logical module pairing is normally made at the time of installation based on customer data organization. The pairing of odd and even logical modules is accomplished physically by interconnecting appropriate jumper blocks on the reference register circuit board. The pairing of odd and even logical modules must be

identical to the detent pairing of the identification plugs on the operator panel.

For purposes of this discussion, assume that odd logical module 1 is paired with even logical module 0 (jumpers installed on jumper block X01 between pins 1 and 16 and between pins 5 and 12). Therefore, whenever the spindle that contains logical modules 0 and 1 generates a gated attention, CGA0 and CGA1 go high (0 and 1 are detended on the associated ID plug – see DDI-1) because the gated attention from a particular spindle is the composite of gated attention for either logical module.

Each gated attention control circuit (one for each logical module) consists of a pack change (PC) latch, a seek (SK) latch, an attention (ATN) latch, and an offline (OFL) latch.

During the initial controller power-up sequence (LOGICSTART low), the pack change latch associated with any online logical module is set (DRIVE STATUS switch associated with the logical module is set to ONLINE). The PC latch for any offline logical module is held reset by the ground applied from the OFFLINE position of the associated DRIVE STATUS switch. Also, during the initial power-up sequence, all SK latches are reset by the machine reset signal (MACHRST; 2 high).

When the disk drive makes its first seek after the initial power-up sequence, gated attention for both logical modules is applied to the control circuits (CGA0 and CGA1 are high in this example. CGA0 causes offline latch OFL0 and offline latch OFL1 to set (since logical modules 0 and 1 are companion modules in this example) if the respective DRIVE STATUS switches are in the ONLINE position. The output of the offline latch (OFL0 high) and signal ONL0 high are ANDed to set the pack change latch (PC0 high), which in turn generates a gated attention to the controller circuits (GA0 high). High OFL1 and ONL1 signals are ANDed to set pack change latch PC1, which in turn generates a gated attention to the controller circuits (GA1 high). Thus, if both logical modules are online when the drive does its first seek, a gated attention is generated for both logical modules.

When a seek is issued to logical module 0, only the seek latch for that module (SK0) will be set. Seek latch SK0 is set by signal SK0.10. Signal SK0.10 is the output of a decoder and is low when the binary configuration of UR5 thru UR7 is 000 and the SETSK/ signal is low (see DDI-4). When the disk drive completes the seek, device end is sent to the controller (CGA0 and CGA1 high). The output of the seek latch (SK0 high) and CGA0 (high) are ANDed to set the ATN0 latch. Low ATN0/ generates a gated attention (GA0 high) to the central control logic of the controller. Since the seek latch for logical module 1 was not set. CGA1 has no affect on GA1.

When a logical module is switched to offline (DRIVE STATUS switch set to OFFLINE), the associated offline latch is set. When the logical module is again placed online (DRIVE STATUS switch set to ONLINE), the associated pack change latch is set, which in turn generates a gated attention.

The pack change, seek, and attention latches are reset when the controller raises the read gate (FT0 and FC1 high) for the selected module (binary configuration of UR5 thru UR7) when the SELECT signal (FT7 high and UR4 low) is high.

A pack change signal (CPC) is routed to the central control logic of the controller whenever a device end signal is generated. When a device end is generated, the controller selects the appropriate logical module (binary configuration of UR5 thru UR7) by raising the module select line (FT7 high and UR4 low generates SELECT/ low) and multiplexes the respective device end to the central control logic of the controller.

SEEK CONTROL (DDI-6)

The seek control circuits contain a busy latch for the logical module that was issued a seek and provides a busy indication to the channel for the companion logical module.

If the seek cylinder address sent by the channel is valid, the controller presents channel end (DW4 high) to the channel in a status byte (IG5 and OPINLTH high). The controller causes the selected disk drive to seek (DW5 low). Assume that logical modules 0 and 1 are paired and that a seek was issued to module 0. The module 0 busy latch sets and allows the module 0 counter to commence counting. The modulo 16 counter is clocked at a 250 Hz rate. When the counter reaches full count (64 milliseconds later), the busy latch is reset. The inhibit reset latch is set at T1 and is reset at T0 to inhibit the busy latch from being reset during the time that it is being set.

When the busy latch is set, the inhibit 1 (INH1) latch is set (BSX1 high). When the disk drive completes the seek (CGA0 and CGA1 high) and the counter times out (BSX1 low), CGA0* and CGA1* high are routed to their respective attention latches (DDI-5). Since the seek was issued only to module 0, only the module 0 seek latch (DDI-5) is set; this allows only the module 0 gated attention (GA0) to be entered onto the A-bus. If the channel had attempted to issue a seek to module 1 while the module 0 busy latch was set, the module 1 seek latch (DDI-5) would also set (drive selected busy seek – CBSYSK high). When the gated attention is received from the disk drive (CGA0 and CGA1 high), module 0 and module 1 gated attentions (GA0 and GA1 high – DDI-5) would be routed onto the A-bus and subsequently to the channel indicating device end for both modules.

HEAD ADDRESS UPDATE (DDI-7)

The head address update circuits cause the head reference address register to be updated each time the head address is updated during multitrack operation.

The head address is initially set into the head reference register when the set head tag (FT2) goes high. At this time FT0 is low allowing FC3 through FC7 to be routed through the multiplexers and clocked into the selected head reference register by FT2 (CLOCK high). The head address is also clocked into the five-bit synchronous counter. During multitrack operation, subsequent head address advances (FC7 high, FT0 low) increment the count contained in the synchronous counter and load the new head address into the head reference register.

TEST SELECT (TEST-1)

The CHANNEL STATUS switches for the 1015 controller are mounted on the operator panel. Since these switches are toggle switches, internal indicators are not used as in the CD14 Controller. Therefore, lamp drivers that are associated with the internal indicators in the CD14 are not needed in the 1015.

The INLINESW/ signal (not used in CD14) is routed to the ROM address register to define whether inline diagnostic routines are to be run on the odd or even logical module. When the TEST/NORMAL/IN LINE switch is set to IN LINE, diagnostic routines can be performed on the even logical module; when set to TEST, diagnostic routines can be performed on the odd logical module.

SECTION 4
MODEL 1015A DUAL DENSITY CONTROLLER

The 1015A Dual Density Disk Storage System comprises a 1015A Dual Density Controller and a combination of Model 215 and Model 213 Dual Density Disk Drives. Model 214 and Model 212 Single Density Disk Drives may be combined with 215 and 213 disk drives; however, the total number of spindles attached to the 1015A Controller cannot exceed nine (eight online and one spare).

The 1015A controller is essentially a 1015 controller modified to incorporate the capability of attaching a maximum of eight online spindles (16 logical modules maximum) and one spare spindle.

The 1015A Dual Density Disk Storage System is connected to a System 360, Model 30 and up, or a System 370 selector channel. Software programs need not be changed for the 1015A System.

PHYSICAL DIFFERENCES

The physical appearance of the 1015A controller is similar to that of the 1015 controller. The operator panel on the front of the 1015A controller contains nine disk drive identification plugs (one for each spindle attached to the controller) and 16 DRIVE STATUS switches, whereas the 1015 controller has five identification plugs and eight DRIVE STATUS switches.

The 1015A controller input/output panel contains nine DC CABLE connectors (one for each disk drive spindle).

The location of circuit boards in the logic and control unit differ in the 1015A from that in the 1015. Six new or additional B-series circuit boards are incorporated into the logic and control unit.

- Two additional Channel Interface D (BL14) circuit boards are added to accommodate the requirement of a total of 16 logical modules.
- Two new Reference Register (BF12) circuit boards are incorporated to store head and cylinder information for 16 logical modules.
- A new circuit board, Miscellaneous Logic I (BL15), provides control logic to the additional circuit boards.
- A new circuit board, Seek Contention Logic (BL17), eliminates seek contention problems between logical module pairs.

Five new E-series circuit boards are contained in the new E-module unit that is attached to the back of the operator panel.

- One E-series circuit board decodes the detent configuration of the ID plugs for both the even and the odd logical modules, and decodes whether the attached spindle is a 215, 214, or a spare.
- Four E-series circuit boards are used to convert physical gated attentions to logical module gated attentions and logical addresses to physical addresses, and to determine whether a companion module has previously been issued a seek.

The Model 214 Single Density Disk Drive and its single spindle version, Model 212, are very similar to the CD22 and CD22S, respectively. The 214 and 212, however, are not interchangeable with the CD22 and CD22S primarily due to different interface requirements. The 214 used with the 1015A utilizes a 75-pin interface signal connector, while the CD22 utilizes a 104-pin interface signal connector. The CD22 contains an identification plug on its operator panel. The ID plug for the 214 is located on the controller operator panel. Additionally, the 214 uses a subtractor circuit board in slot 06A while the CD22 uses a jumper module.

MICROPROGRAM DIFFERENCES

The ROM contains basically the same microprograms as the 1015 but with added features. The 1015A operates with either a 1-board or a 2-board ROM. Two-channel 1015A controllers use the same ROM as single-channel 1015A controllers. Inline routines E0 and F0 have been deleted to accommodate the additional microprogram requirements of the 1015A.

LOGIC DIFFERENCES

The arrangement of the 1015A logic diagram sheets differ in some areas from that of the 1015 due to added circuits.

The following paragraphs describe the logic differences between the 1015A and the 1015 controllers. The

description of the differences are based on the referenced 1015A logic diagrams.

SW REGISTERS (CI-4 AND CI-5)

The 1015A contains 16 SW registers, one for each online logical module. The SW registers operate in the 1015A in the same manner as they do in the 1015.

In single-channel controllers, only bits 0 through 3 of the SW register are used. These four bits of each register associated with channel A store device end information for the 16 logical modules.

ATTENTION CONTROL (CI-6 AND CI-7)

The attention control circuits operate in the same manner for the 1015A as they do for the 1015, but for 16 logical modules.

Since bits 4 through 7 of the SW register are not used in single-channel controllers (see CI-4 and CI-5), the circuit boards in slot A,B-3 and A,B-5 are replaced with jumper modules BZ15. These jumper modules supply a high (+5STUB) or low (GND) signal to inputs of the BL14 circuit boards in slots A,B-2 and A,B-4 to enable the channel A position of the attention control circuits.

ATTENTION SELECTION (CI-8)

The attention selection circuits provide any gated attention for channel A (ATTENTION A) and channel B (ATTENTION B) to the request-in logic (CI-10 and CI-11), selection of the high or low SW registers, and selection of high or low priority gated attentions.

Any gated attention signal ATTENTION A is active (high) when any logical module presents a device end for channel A. Likewise, in a two-channel controller, ATTENTION B performs the same function for channel B.

The SW register input to the A-bus is controlled by the HIGHADDR (high address) signal. When HIGHADDR is low (indicating low address selection – logical modules 0 through 7), SW0L through SW7L are routed to the A-bus. When HIGHADDR is high, SW0H through SW7H are routed to the A-bus.

In single-channel controllers, jumper modules BZ15 replace channel D circuit boards BL14 in slots A,B-3 and A,B-5. The jumper modules contain an SW register simulator for SW4L through SW7L and SW4H through SW7H to enable the SW register test portion of the resident diagnostic test to operate properly since the same read-only memory is used for both one- and two-channel controllers.

Selection of high or low priority gated attentions (ATTCU0 through ATTCU7 and ATTCU8 through ATTCU15, respectively) may be channel initiated or controller initiated. Selection of high or low priority gated attentions by the channel is initiated when either channel raises address-out and operational-out, causing ER1 to go high and setting latch 1. If UR4 is low, the high priority (low address) gated attentions will be gated through the quad-multiplexers to the A-bus. If UR4 is high, the low priority (high address) gated attentions will be gated to the A-bus.

During offline operation (when running resident diagnostic routines), DRIVDEGATE/ low sets latch 1. The state of UR4 then determines whether the high or low priority gated attentions are gated to the A-bus. Selection of high or low priority gated attentions by the controller is initiated when REQINA, REQINB, or MACHRST;2 is high, causing latch 1 to reset. If a high priority gated attention does not exist, LOWP latch will set and allow the low priority gated attentions (ATTCU8 through ATTCU15) to be routed to the A-bus if latch 1 is reset. The attention latch will set when either ATTCUHIGHP or ATTCULOWP is high. When ATTCUHIGHP and select-out (SELTO) are high, the LOWP latch resets (LOWP signal low) allowing the high priority gated attentions (ATTCU0 through ATTCU7) to be routed to the A-bus.

A BUS AND A REGISTER (ALU-2 (1) AND ALU-2 (2))

In the 1015A the ATTCU0 through ATTCU7 gated attention inputs to the A-bus for SA *equals* 13 are replaced by the ATTCU08 through ATTCU715 signals. When high priority gated attentions are to be entered into the A-bus, ATTCU08 through ATTCU715 represent ATTCU0 through ATTCU7. When low priority gated attentions are to be entered into the A-bus, ATTCU08 through ATTCU715 represent ATTCU8 through ATTCU15.

ROM ADDRESS REGISTER (ROM-1)

In the 1015A controller, the input to ROMAD bit 1 for SH *equals* 7 is FT5G. Signal FT5 is ANDed with 214SELECTED/ so that a reseek does not take place when the selected drive is a 214.

SENSE AMPLIFIER REGISTER (ROM-4 (1))

Three bits of the ROM which are spare bits in the 1015 are used as special bits (SP) in the 1015A. The three SP bits develop a number of special control terms (see DDI-12).

READ/WRITE SELECT AND PHASE LOCK (SERDES-1)

The read/write select and phase lock circuits are the same as those used in the 1015 but have additional circuits to accommodate the nine read and write coaxial lines for the nine spindles.

DISK DRIVE INPUTS (DDI-1)

The disk drive inputs in the 1015A are basically identical to those for the 1015. The main difference is the added inputs to the module select error circuit to accommodate nine spindles. Signals CID1 through CID3 develop the physical address for the ID byte in the bit count appendage to a track record.

ID PLUG DECODE (DDI-2)

The ID plug decode circuits identify the logical modules associated with each spindle; indicates whether it is a 215 disk drive, a 214 disk drive, or neither; indicates if the spindle is a spare spindle; and indicates if the selected spindle is a 214.

Three ID switches are used to identify the even logical module, three switches are used to identify the odd logical module, one switch identifies the disk drive as a 215, one switch identifies the disk drive as a 214, and one switch identifies the disk drive as the spare.

The nine decode circuits operate in an identical manner; therefore, for purposes of explanation, only the decode circuit associated with spindle E is described.

Three signals (SEE2/, SEE4/, and SEE8/) identify the address of the even logical module. When the address of the even logical module is zero, none of the ID switches (SE0-SE2) are activated. The various binary configurations of the three even ID switches define the even logical module address (that is, 0, 2, 4, 6, etc).

Three signals (SE02/, SE04/, and SE08/) identify the address of the odd logical module. When the address of the odd logical module is one, none of the ID switches (SE3-SE5) are activated. The various binary configurations of the three odd ID switches define the odd logical module address (that is, 1, 3, 5, 7, etc).

The signal DESELODDE (deselect odd module E) is active when neither a 214 nor a 215 is selected (214E/ and 215E/ high), when the spare ID plug is inserted (SPARESELCTE/ low), or when disk drive E is a 214 with an even address (214E/ and SE08/ low).

The signal DESELEVENE (deselect even module E) is active when neither a 214 nor a 215 is selected (214E/ and 215E/ high), when the spare ID plug is inserted (SPARESELCTE/ low), or when disk drive E is a 214 with and odd address (214E/ low and SE08/ high).

Whenever a gated attention is received from any disk drive identified as a spare (for example: CGAE and SPARESELCTE high), CGASM (gated attention spare module) goes high.

Whenever a 214 disk drive is selected (for example: UMSE and 214E high), signal 214 SELECTED goes high.

GATED ATTENTION (DDI-3 AND DDI-4)

The gated attention circuits convert physical module gated attentions to logical module gated attentions. For discussion purposes, assume that the disk drive connected as module C is a 215 and that the logical module pair for module C is 0 and 7. Since the even logical module is 0 (DDI-3), select signals SCE2/, SCE4/, and SCE8/ are high, thus enabling output 7 of the decoder associated with module C to become active (CGAC0/ low) when a gated attention (CGAC high) is received from the disk drive (DESELCEVENC low). Signal CGAC0/ activates CGA0 (gated attention for logical module 0). Since the odd logical module is 7 (DDI-4), select signals SC02/ and SC04/ are low, and SC08/ is high, thus enabling output 4 of the decoder associated with module C to go active (CGAC7/ low) when gated attention (CGAC high) is received from the disk drive (DESELCODDC low). Signal CGAC7/ activates CGA7 (gated attention for logical module 7).

If a 214 disk drive is connected as module C and is assigned a logical module address of 3, the decoder associated with module C for an even logical module (DDI-3) will be degated by DESELCEVENC high. The odd logical module decoder associated with module C will have output 6 active (CGAC3/ low) which in turn activates CGA3 (gated attention for logical module 3).

MODULE SELECT (DDI-5 AND DDI-6)

The module select circuits convert logical module select signals to physical module select signals. For discussion purposes, assume that the disk drive connected as module C is a 215 and the logical module pair for module C is 0 and 7. When the controller selects module 0 (UMS0/ low), UR4 through UR6 are low and EVENMODSEL/ is low (UR7 low). If the DRIVE STATUS switch for logical module 0 is in the ON LINE position, UMS0/ is routed to the multiplexers. Since logical module 0 is assigned to physical module C, the multiplexer associated with module C enables (enabled by SCE2/, SCE4/, and SCE8/ high, and DESELCEVENC low) the UMS0SW input, causing UMSCEVEN/ to go low. When the controller selects module 7 (UMS7/ low – DDI-6), UMSCODD/ goes low. When either logical module 0 or 7 is selected by the controller, physical module C is selected.

MODULE SELECT DRIVERS (DDI-7)

The module select drivers circuits combine the logical module select lines and spare module select line into a physical module select line. When either the even or odd logical module associated with a physical module is selected, the physical module select line is activated (e.g.; UMSCODD/ or UMSCEVEN/ low causes UMSC/;D to go low). Additionally, if a physical module is designated as the spare module, UMSSM/ low and SPARESELCTC high cause UMSC/;D to go low.

SEEK CONTROL (DDI-8 AND DDI-9)

The seek control circuits determine whether or not the companion of a logical module has previously been issued a seek. For purposes of discussion, assume that the disk drive connected as module C is a 215 and the logical module pair is 0 and 7. If a seek has been issued to logical module 7, signal SK7LTH/ goes low. SK7LTH/ is routed to input 4 of the SKODDC multiplexer through an inverter. Since the odd logical module address for physical module C is 7, input 4 of the multiplexer appears at the output as SKODDC/ low. Signal SKODDC/ low inhibits the gated MSB input to the module C seek decoder, thus disabling all outputs (all outputs high). Output 7 of the decoder (SKAC/) high and the other two inputs to the SKA/ gate high cause SKA/ to be low. This inhibits a gated attention for logical module 0 from being routed to the A-bus (DDI-14). If a seek had not been issued to logical module 7, signal SK7LTH/ would be high, SKODDC/ would be high, and SKAC/ and SKA/ would be low.

Similarly, if a seek had been issued to logical module 0, SKEVENC/ (DDI-9) would go low and inhibit the module C seek decoder, causing SKMC/ to go high, SKMX to go low, and SKM/ to go low. This in turn would inhibit a gated attention for logical module 7 from being routed to the A-bus (DDI-14).

The following chart indicates that the companion of the indicated logical module has previously been issued a seek when the signal is active.

Active Signal (Low)	Companion of Logical Module:
SKA/	0
SKB/	2
SKC/	4
SKD/	6
SKE/	8
SKF/	10
SKG/	12
SKH/	14
SKJ/	1
SKK/	3
SKL/	5
SKM/	7
SKN/	9
SKP/	11
SKR/	13
SKS/	15

SEEK CONTENTION (DDI-10(1) AND DDI-10(2))

The seek contention circuits set the ST4 status latch each time a byte of data is transferred during a read or write operation; when low priority gated attentions are contained in the SW register; when the companion of an addressed logical module has previously been issued a seek; or when a reserve or release command is to be executed for a two-channel controller.

The no-seek signals (NOSEEKA/-NOSEEKJ/ – DDI-10(1)) are individually active when an addressed logical module's companion module has previously been issued a seek command. The seek latches are initialized during the power-up sequence and when a machine reset occur. Assume that a stand-alone seek has been issued for the odd logical module of drive A. When the seek commences, SKSTART/ is low and UMSA is high, causing the seek latch to set and the odd/even latch to set (UR7 high). The NOSEEKA/ signal is low at this time but has no affect on the seek in progress. If a stand-alone seek is issued by the channel to the even logical module of drive A, IG7 and COMMO are high prior to the issuance of the seek to the drive. The COMMAND signal high samples the outputs of the odd/even latch to determine if a seek was issued to the companion module. Since the previous seek was for the odd module (odd/even latch set) and the present seek is for the even module (UR7/ high), the seek latch will not be reset and NOSEEKA/ will be low. NOSEEKA/ low enables ST4 to set (DDI-10(2)), allowing the microprogram to branch on this condition and causing the controller to not issue the seek to the even module. If the command for the even module was a channel command, the seek latch would be reset, allowing the seek to be issued to the even module since read or write activity would follow for the even module.

If the channel issues two seeks for the same logical module without an intervening seek for the companion logical module, the seek latch is reset. For example, the first seek sets the odd/even latch (seek for the odd module) and the seek latch. The second seek issued by the channel causes the COMMAND signal to go high when the module is selected (UMSA and UR7 high) to reset the seek latch. This in turn causes the NOSEEKA/ signal to go high and allows the controller to issue the second seek to the odd logical module.

When a byte of data has been transferred during a read or write operation, SETST4/ goes low (DDI-10(2)), causing SETST4G/ to go low.

If a released or reserve command is to be executed (OP0 high) in a two-channel controller (2CH high), SETST4G/ goes low at T1 when ST4 is to be set (SETST4LTH high).

When a no-seek condition exists (e.g., NOSEEKA/ low), SETST4G goes low at T1 if OP0 is low and ST4 is to be set (SETST4LTH high).

When gated attentions from low priority modules (8 through 15) are stored in the SW register and no high priority gated attentions exist (ATTLOWPGATE high), SETST4G/ goes low when the SA field of the ROM *equals* 13 and the SD field of the ROM *equals* 7 to transfer the gated attentions to the OP register. When ATTLOWPGATE is low, the high priority gated attentions (modules 0 through 7) are transferred to the OP register.

FILE CONTROL AND FILE TAG REGISTERS (DDI-11)

The file control (FC) and file tag (FT) registers are identical to those described in Section 2 for DDI-3.

REFERENCE REGISTERS CONTROL (DDI-12)

The reference registers control circuits control the input and output gating of the head and cylinder reference registers, and provide other control signals.

Whenever the SD field of the ROM *equals* 15, the SD=15 latch is set. At the following T0, the select spare module (SSM) latch is set. Low and high module address signals are developed from UR4/ and UR4 respectively when the spare module is not selected (SSM/ high). Even and odd module select signals are developed from the LSB of the UR register (UR7).

The SD control signals, CTLSD3 and CTLSD4, control the head and cylinder reference register, the old cylinder address, and bit count appendage inputs to the A-bus (DDI-13).

The pack change signal is active to indicate that the addressed module (either high or low address) has had its pack change latch set (DDI-14 and DDI-15). The CPCLOW/, CPCHIGH/, or ZEROHDCY/ signal causes the return-to-zero flip-flop to set.

The use of the SP (special) field of the ROM is unique to the 1015A. This field develops special control signals for the 1015A. The SP *equals* 0 and 1 decode of the SP field are not used. When SP *equals* 2, the operating system is made to think that a seek has taken place (FORCESC/ low). When SP *equals* 3, the cylinder address is clocked into the reference register (FCXCY/ low). When SP *equals* 4, the head address is clocked into the reference register (FCXHD/ low). When SP *equals* 5, the contents of the GP register are transferred to the head reference register during multiple track operation (GPXHD/ low). When SP *equals* 6, the addressed module's head and cylinder addresses in the reference registers are forced to zero (ZEROHDCY/ low). When SP *equals* 7, status latch ST4 will be set if an addressed module's companion has previously been issued a seek command, or a reserve or release command is to be executed in a two-channel controller.

UR register bits 4 and 5 are used to enable the setting of the cylinder or head reference registers as follows:

Active Control Term	Reference Register for Modules:
UR4/, UR5/	0-3
UR4/, UR5	4-7
UR4, UR5/	8-11
UR4, UR5	12-15

The SETSK signal high sets the seek latch for the selected module if the module select signal is high (FT7 high) and a recalibration (return to zero) is to be made (FC6 and FT0 high), when a seek to a new cylinder address is to be made (FT1 high), or when any disk drive is busy (CBSYA high). CBSYA is high whenever CBSY is high and address-in is sent to the channel (IG7 high) after address-out has been received from the channel (ER1 high) provided a seek complete (gated attention) is not outstanding (SW2 or SW6 high) when the controller is selected by channel A or B (CHANALTH/; A or CHANBLTH/; A low), respectively. CBSYA is inhibited (low) whenever REQINA, REQINB, or ER1 resets the 13B latch. CBSYA will remain low until IG7 goes high and the other associated conditions are met. The PCRST signal is used to reset the pack change, seek, and attention latches (DDI-14 and DDI-15).

CYLINDER AND HEAD REFERENCE REGISTERS (DDI-13)

The cylinder and head reference registers store the reference cylinder address and the reference head address that was last issued to the disk drive for each logical module. The storage of the cylinder and head addresses is accomplished in the same manner as in the 1015 but for 16 logical modules.

The normal inputs to the reference register are from the FC register and FT3. These inputs are clocked into the selected register (as determined by the state of UR4 through UR7) by either the cylinder reference clock (CYLREFCLK high for cylinder reference register) or the head reference clock (HDREFCLK high for head reference register). The FC register and FT3 input are selected when a head address is not being updated during a multitrack operation (GPXHD/ high) and a recalibrate command is not being executed (RTZ low).

During multitrack operation, the head address contained in the head reference register is updated as the head address is advanced. When a head address is to be updated, it is put on the ALU bus for entry into the GP register. When SETGP goes high, the new head address is loaded into the GP register (REG-5) and also into the head address storage latches. When the microprogram issues the load GP register into the head register command (GPXHD low), the contents of the head address

storage latches are loaded into the selected head reference register.

The control SD3 and SD4 signals (CTLSD3 and CTLSD4) control the entry onto the A-bus of the old cylinder address (CCAR), the head reference address (HD), the cylinder reference address (CYL), and the ID byte data for the bit count appendage (CUADD0 through CUADD4, CMSJ, and CID1 through CID3) in the same manner as the 1015.

When the old cylinder address for a 214 disk drive is to be entered onto the A-bus, signal 214 SELECTED goes high, allowing CCAR1 through CCAR8 to pass onto the A-bus. This is the actual cylinder address of the 214. If the old cylinder address is for a 215, signal 214 SELECTED is low, allowing CCAR0 through CCAR7 to pass onto the A-bus. This is the reference (logical) cylinder address.

GATED ATTENTION CONTROL (DDI-14 AND DDI-15)

The gated attention control circuits operate in the same manner as in the 1015. Since there are 16 logical modules in the 1015A, circuitry for the 16 logical modules is provided.

In the 1015A, the attention latch is set by an additional input, FORCESC( )/. This signal is active to make the operating system think that a seek has taken place.

APPENDIX A
DESCRIPTION OF MNEMONIC TERMS

Note: Asterisk (*) applies to 1015A only.

Signal Mnemonic	Description	Source
+5STUB	+5v pull-up signal through 1K ohm resistor	----
0 → GP	Loads the contents of the DATA switches into the GP register during inline mode of operation when spare drive is selected.	REG-1
A0-A7	A register bits 0 through 7	ALU-2(1) ALU-2(2)
ABUS0-ABUS7	A bus bits 0 through 7; input to A0 through A7 respectively.	ALU-2(1) ALU-2(2)
ADD	Defines an ADD arithmetic operation in the ALU	ALU-1
ADDCOMPA	Address Compare – Channel A. Address on bus-out lines matches controller preset channel A address.	CI-1
ADDCOMPB	Address Compare – Channel B. Address on bus-out lines matches controller preset Channel B address.	CI-1
ADDINA	Address-in Channel A. Identifies data on Channel A bus-in lines as an address.	CI-7, CI-10*
ADDINB	Address-in Channel B. Identifies data on Channel B bus-in lines as an address.	CI-8, CI-11*
ADDOUTA	Address-out Channel A. Identifies data on Channel A bus-out lines as an address.	CI-2
ADDOUTB	Address-out Channel B. Identifies data on Channel B bus-out lines as an address.	CI-3
ADDRESSINGA	Indicates that Channel A is addressing the controller.	CI-2
ADDRESSINGB	Indicates that Channel B is addressing the controller.	CI-3
ALU0-ALU7	Arithmetic logic unit bits 0 through 7. Result of arithmetic operation.	ALU-4(1) ALU-4(2)
ALUERR	ALU error. A register parity error detected during an operation.	ALU-2(2)
ALUP	ALU parity bit.	ALU-4(2)
AMAREA	Address mark area of a record on a disk pack.	SERDES-2
AMCONT1, AMCONT2	Address mark control 1 and 2. Used in the detection of recorded address marks.	SERDES-2
AMGOOD	Address mark good. Indicates that all information preceding the address mark is good.	SERDES-2
AMX	Address mark check timing	SERDES-2

Signal Mnemonic	Description	Source
AND	Defines an AND operation in the ALU.	ALU-1
AND+ADD	Defines an AND or ADD operation in the ALU.	ALU-1
ASEL	Channel A selected by the controller.	CI-2
AT0A-AT7A	Attention from disk drive 0 through 7 – Channel A.	CI-5
AT0B-AT7B	Attention from disk drive 0 through 7 – Channel B.	CI-5
ATTCU	Any attention from disk drives – Channels A and B.	CI-5
ATTCU0-ATTCU7	Attention from disk drive 0 through 7 – Channel A or Channel B.	CI-5
ATTENTION	Attention from any disk drive.	CI-7 CI-8
B0-B7	B register bits 0 through 7.	ALU-3
BBDATA0- BBDATA7	Burst buffer register data input bits 0 through 7.	SERDES-4
BCCLK	Bit count appendage clock.	SERDES-3
BCRST	Bit count reset	SERDES-4
BIT5OP	Bit 5 operable (disk drive operable)	STAT-1
BLKFLINT	Blank file interface	DDI-3, DDI-11*
BSEL	Channel B selected by the controller	CI-3
BSTCHK	Burst check	SERDES-4
BURSTBX	Burst BX register	SERDES-4
BURSTCX	Burst CX register	SERDES-4
BUSINPA	Bus-in parity bit – Channel A	CI-9, CI-12*
BUSINPB	Bus-in parity bit – Channel B	CI-9, CI-12*
BUSIN0A- BUSIN7A	Bus-in bits 0 through 7 – Channel A	CI-9, CI-12*
BUSIN0B- BUSIN7B	Bus-in bits 0 through 7 – Channel B	CI-9, CI-12*
BUSOUTP	Bus-out parity bit – Channel A or B	CI-1
BUSOUT0- BUSOUT7	Bus-out bits 0 through 7 – Channel A or B	CI-1
BUSOUTPA	Bus-out parity bit – Channel A	CI-1
BUSOUT0A- BUSOUT7A	Bus-out bits 0 through 7 – Channel A	CI-1
BUSOUTPB	Bus-out parity bit – Channel B	CI-1

Signal Mnemonic	Description	Source
BUSOUT0B- BUSOUT7B	Bus-out bits 0 through 7 – Channel B	CI-1
BXP	BX register parity bit.	REG-7
BX0-BX7	BX register bits 0 through 7	REG-7
BYP	BY register parity bit.	REG-2
BY0-BY7	BY register bits 0 through 7	REG-2
C0A, C0B	Carry-out from ALU bit 0	ALU-4(1)
C2A, C2B	Carry-out from ALU bit 2	ALU-4(1)
C4A, C4B	Carry-out from ALU bit 4	ALU-4(2)
C6A, C6B	Carry-out from ALU bit 6	ALU-4(2)
CARRY	Overflow from an arithmetic ADD operation	ALU-1
CBSY	Disk drive busy	DDI-1
CCAR0-CCAR7	Disk drive cylinder address register bits 0 through 7	DDI-1
CCNGND	Controlled ground to the disk drive	PWR-1
CEOC	Disk drive end of cylinder	DDI-1
CGA0-CGA7	Gated attention – drive 0 through 7	DDI-1
CGASM	Gated attention – spare disk drive	DDI-1
CHANALTH	Channel A latch	CI-2
CHANBLTH	Channel B latch	CI-3
CHEXT	Disk drive heads extended	PWR-1
CHKGOOD	Check good for data being read	SERDES-2
CIDX	Index	DDI-3, DDI-11*
CIN	Carry-in	ALU-1
CKPRTY	Check parity	STAT-1
CKRSTSW	Check reset switch	TEST-1
CKSTPSW	Check stop switch	TEST-1
CLK0-CLK7	Clock SW register – disk drive 0 through 7	CI-4
CLKGAP	Clock gap	SERDES-2
CLKOUTA	Clock-out – Channel A	TIM-2
CLKOUTB	Clock-out – Channel B	TIM-2

Signal Mnemonic	Description	Source
CLKPH	Clock phase	SERDES-1
CLKTRIG	Clock trigger	SERDES-3
CMSA-CMSJ	Module select – drives A through J	DDI-1
COL	Disk drive online	DDI-1
COMMO	Command-out	CI-2
COMOUTA	Command-out – Channel A	CI-2
COMOUTB	Command-out – Channel B	CI-3
COMPADREQ1, COMPADREQ2	Compare address equal – ROM address equals setting of STOP ADDRESS switches	ROM-2
CONT00-CONT11	Address mark control count 00 through 11 (binary)	SERDES-2
CONTERR	Controller error – either a sense amplifier register error or a read-only address register error.	TEST-3
CPC	Disk drive pack change	DDI-1(CD14) DDI-5(1015)
CSIN	Disk drive seek incomplete	DDI-1
CUADD0-CUADD3	Controller address bits 0 through 3	STAT-1
CUBUSYA	Controller busy – to Channel A	CI-7, CI-10*
CUBUSYB	Controller busy – to Channel B	CI-8, CI-11*
CUENDA	Controller end – Channel A. Enables polling interrupt sequence.	CI-7, CI-10*
CUENDB	Controller end – Channel B. Enables polling interrupt sequence.	CI-8, CI-11*
CUSF	Disk drive unsafe	DDI-1
CWCS	Disk drive write current sense	DDI-1
CXP	CX register parity bit	REG-7
CX0-CX7	CX register bits 0 through 7	REG-7
DATAERR	Data error caused by bus-out parity, ALU error, or serial write data error.	TEST-3
DATAGAP	Data gap	SERDES-2
DATAGOOD	Data good. Indicates information preceding AM bytes is good.	SERDES-2
DATAOUT	Data output to or from selected disk drive.	SERDES-1 SERDES-3
DATAPH	Data phase	SERDES-1

Signal Mnemonic	Description	Source
DATATRIG	Data trigger	SERDES-3
DCPWRUP	Dc power is within tolerance	PWR-1
DD00-DD50	Data delay taps – 0 to 50-nanosecond delay	SERDES-1
DE0A-DE7A	Device end – disk drive 0 through 7 to Channel A	CI-5
DE0B-DE7B	Device end – disk drive 0 through 7 to Channel B	CI-5
DGX	Data good check time	SERDES-1
DELDATA	Delayed data	SERDES-1
DEQ0	Contents of ALU bus equals zero	ALU-1
DESDATA	Deserialize data	SERDES-3
DHP	DH register parity bit	REG-3
DH0-DH7	DH register bits 0 through 7	REG-3
DISP0-DISP7	Display register bits 0 through 7	REG-2
DISP0-DISP7	REGISTER DISPLAY indicators – input bits 0 through 7	TEST-2
DISP1X-DISP3X	REGISTER DISPLAY indicators – input control	TEST-2
DISPINSW	DISPLAY INNER switch – display inner portion of REGISTER SELECT switch	TEST-1
DISPOUTSW	DISPLAY OUTER switch – display outer portion of REGISTER SELECT switch	TEST-1
DISPP	REGISTER DISPLAY indicator parity bit input	ALU-2(2)
DLP	DL register parity bit	REG-4
DL0-DL7	DL register bits 0 through 7	REG-4
DRBY	Transfer contents of DR register to BY register	CI-6, CI-9*
DR·DR	Bit count appendage reset control	SERDES-4
DRIVDEGATE	Degate channel line drivers	TEST-1
DRP	DR register parity bit	REG-6
DR0-DR7	DR register bits 0 through 7	REG-6
DRXFDR	Transfer contents of DR register into FDR	SERDES-3
DSBC0-DSBC7	Drive selected or bit count bits 0 through 7	SERDES-4
DWP	DW register parity bit	REG-6
DW0-DW7	DW register bits 0 through 7	REG-6

Signal Mnemonic	Description	Source
ENABLESWA	Enable switch – Channel A	TEST-1
ENABLESWB	Enable switch – Channel B	TEST-1
ENBLALTH	Enable Channel A latch	TIM-2
ENBLBLTH	Enable Channel B latch	TIM-2
ENTERST	Enter ALU bus into ST register during test mode of operation	REG-1
ENTERSW	Enter setting of START ADDRESS switches into the ALU bus	REG-1
ENTROUTSW	Enter data into register selected by the outer ring of the REGISTER SELECT switch	TEST-1
ENTRINSW	Enter data into register selected by the inner ring of the REGISTER SELECT switch	TEST-1
EPOCONTROLA	Emergency power off control – Channel A	PWR-1
EPOCONTROLB	Emergency power off control – Channel B	PWR-1
ER0-ER7	ER register bits 0 through 7	STAT-1
ERRFZ	Error freeze	TIM-3
ERRLDRSLT	ERR (error), LOAD, or RSLT (result) position of MODE SELECT switch	STAT-1
ERRSW	Error position of MODE SELECT switch	TEST-1
EVENPRTYA	Even parity – Channel A (parity error)	CI-1
EVENPRTYB	Even parity – Channel B (parity error)	CI-1
EXOR0-EXOR7	Exclusive-OR bits 0 through 7	SERDES-4
FC0-FC7	FC register bits 0 through 7	DDI-3, DDI-11*
FDR0-FDR7	FDR bits 0 through 7	SERDES-3
FDRXDR	Transfer content of FDR to DR register	SERDES-2
FRP	FR register parity bit	REG-3
FR0-FR7	FR register bits 0 through 7	REG-3
FT0-FT7	FT register bits 0 through 7	DDI-3, DDI-11*
GATEALU	Gate content of ALU bus into DR register	SERDES-2
GATEBY	Gate content of BY register into DW register	CI-6, CI-9*
GATEDASEL	Channel A selected by controller during test mode of operation	CI-2
GATEDBSEL	Channel B selected by controller during test mode of operation	CI-3
GATEGENRSTA	Gate general reset – Channel A	TIM-2

Signal Mnemonic	Description	Source
GATEGENRSTB	Gate general reset – Channel B	TIM-2
GATEFDR	Gate content of FDR to DR register input	SERDES-2
GATEIG	Gate ALU bus into IG register	CI-7, CI-10*
GENRST	General reset	TIM-2
GENRSTOSA	General reset one-shot – Channel A	TIM-2
GENRSTOSB	General reset one-shot – Channel B	TIM-2
GLP	GL register parity bit	REG-2
GL0-GL7	GL register bits 0 through 7	REG-2
GPP	GP register parity bit	REG-5
GP0-GP7	GP register bits 0 through 7	REG-5
GTDADDOUTA	Gated address-out – Channel A	CI-2
GTDADDOUTB	Gated address-out – Channel B	CI-3
HLDOUTA	Hold-out – Channel A	CI-2
HLDOUTB	Hold-out – Channel B	CI-3
IE3-IE6	IE register bits 3 through 6	STAT-1
IG0-IG7	IG register bits 0 through 7	CI-7
INDEXENBL	Index enable	TIM-3
IHDR	Transfer data on bus-out lines (IH) into DR register	CI-6, CI-9*
INHIBITA	Inhibit controller	TIM-3
INHIBITB	Inhibit controller – delayed	TIM-3
INHIE1	Inhibit IE bit 1	TIM-3
INLINE	Inline mode of operation	STAT-1
INLINESW	INLINE position of TEST/NORMAL/INLINE switch	TEST-1
INTALSELA	Initial selection of controller – Channel A	CI-2
INTFDSBLA	Interface disable – Channel A	TIM-2
INTALSELB	Initial selection of controller – Channel B	CI-3
INTFDSBLB	Interface disable – Channel B	TIM-2
KLP	KL register parity bit	REG-3
KL0-KL7	KL register bits 0 through 7	REG-3

Signal Mnemonic	Description	Source
LATCH1	Latch 1. Used in channel read and write operation	CI-6, CI-9*
LATCH2	Latch 2. Used in channel read and write operation	CI-6, CI-9*
LDSW	LOAD position of MODE SELECT switch	TEST-1
LOGICSTART	Logic start. Power-up sequence complete – generate machine reset.	PWR-1
LTTESTSW	Light test switch	TEST-1
MACHRST	Machine reset	TIM-3
MACHSTOP	Machine stop	TEST-3
METINA	Metering-in – Channel A	CI-7, CI-10*
METINB	Metering-in – Channel B	CI-3
METOUTA	Metering-out – Channel A	CI-2
METOUTB	Metering-out – Channel B	CI-3
MSELERR	Module select error	DDI-1
NORMALSW	NORMAL position of TEST/NORMAL/IN LINE switch	TEST-1
NR0A-NR7A	Disk drive 0 through 7 not reserved for Channel A	CI-5
NR0B-NR7B	Disk drive 0 through 7 not reserved for Channel B	CI-5
OM	Odd module (read-only memory)	ROM-4(1)
OPINA	Operational-in – Channel A	CI-7, CI-10*
OPINB	Operational-in – Channel B	CI-8, CI-11*
OPINLTH	Operational-in latch	CI-7, CI-10*
OPINLTHRST	Operational-in latch reset	CI-7, CI-10*
OPMETA	Operate meter – Channel A	CI-2
OPMETB	Operate meter – Channel B	CI-3
OPOUTA	Operational-out – Channel A	CI-2
OPOUTB	Operational-out – Channel B	CI-3
OPOUTA/DLYD	Operational-out – Channel A delayed	TIM-2
OPOUTB/DLYD	Operational-out – Channel B delayed	TIM-2
OPP	OP register parity bit	REG-4
OP0-OP7	OP register bits 0 through 7	REG-4
OPRTMTR	Operate meter	CI-2

Signal Mnemonic	Description	Source
OR	Defines an OR operation in the ALU	ALU-1
OSC	Oscillator	TIM-1
OSC5MHZ	5 megaHertz oscillator	TIM-1
OSC8MHZ	8 megaHertz oscillator	TIM-1
PA	Read-only memory address register parity bit	ROM-4(1)
PC	Read-only memory sense amplifier register parity bit	ROM-4(1)
PH10-PH17	Phase 10 through 17. Disk drive read/write time control.	SERDES-3
PH20-PH27	Phase 20 through 27. Disk drive read/write time control.	SERDES-3
PHASELTH	Phase latch	SERDES-1
POWER	Dc power within tolerance	PWR-1
POWERHOLDA	Power hold control – Channel A	PWR-1
POWERHOLDB	Power hold control – Channel B	PWR-1
POWERPICKA	Power pick – Channel A. Initiates power-up sequence from Channel A.	PWR-1
POWERPICKB	Power pick – Channel B. Initiates power-up sequence from Channel B.	PWR-1
PRBLTH	Probe latch	TEST-3
PROCRST	Processor reset	TIM-3
PROPSELOUTA	Propagate select-out – Channel A	CI-2
PROPSELOUTB	Propagate select-out – Channel B	CI-2
PWRCOMPLA	Power-up sequence complete – Channel A	PWR-1
PWRCOMPLB	Power-up sequence complete – Channel B	PWR-1
RADERR	Read-only memory address register parity error	ROM-1
RADERRL	Read-only memory address register parity error latch.	TEST-3
RADX	Partial read-only memory address register parity check	ROM-1
RAWDATA	Data from selected disk drive	SERDES-1
RCI0-RCI3	Read cycle initiate 0 through 3	ROM-1
RDENABLE	Read enable	SERDES-3
RDENBLRST	Read enable reset	SERDES-2
RDGATE	Read gate	SERDES-3

Signal Mnemonic	Description	Source
READRST	Read reset	SERDES-2
RECYCLE	Recycle the ROM address register to the setting of the START ADDRESS switches.	ROM-2
RECYSW	RECYC (recycle) position of the MODE SELECT switch.	TEST-1
REGSEL1- REGSEL4	Display register select control 1 through 4 from REGISTER SELECT switch.	TEST-2
REQINA	Request-in – Channel A	CI-7, CI-10*
REQINB	Request-in – Channel B	CI-8, CI-11*
RESTART	Restart address mark detection sequence	SERDES-2
ROMAD0- ROMAD10	Read-only memory address register bits 0 through 10.	ROM-1
RSLTSW	RSLT (result) position of MODE SELECT switch	TEST-1
RSTCHANA	Reset Channel A reserved status	TIM-2
RSTCHANB	Reset Channel B reserved status	TIM-3
RSTCLKA	Reset clock for Channel A SW registers	TIM-2
RSTCLKB	Reset clock for Channel B SW registers	TIM-3
RSTCONTCHA	Reset controller – Channel A	TIM-2
RSTCONTCHB	Reset controller – Channel B	TIM-2
RSTPROBE	Reset probe latch	TEST-1
RSTSW	Controller reset control switch (test mode only)	TEST-1
RUNSW	RUN position of MODE SELECT switch	TEST-1
RUTNLD	RTN (routine) or LOAD position of MODE SELECT switch	STAT-1
RUTNSW	RTN (routine) position of MODE SELECT switch	TEST-1
R/WDATAGOOD	Read or write data good	SERDES-2
SA0-SA4	SA field bits 0 through 4 of read-only memory	REG-1 ROM-4(2) ALU-1 CI-6, CI-9*
SAR00-SAR47	Sense amplifier register bits 0 through 47	ROM-3
SARERR	Sense amplifier register parity error	ROM-4(2)
SARERRL	Sense amplifier register parity error latch	TEST-3
SARRST	Sense amplifier register reset	ROM-3

Signal Mnemonic	Description	Source
SAXBC	Teansfer bit count (BC) to A bus	SERDES-4
SAXCX	Transfer contents of CX register to A bus	SERDES-4
SAXDR	Transfer contents of DR register to A bus	CI-6, CI-9*
SAXER	Transfer contents of ER register to A bus for error check	CI-6, CI-9*
SAXIH	Transfer contents of bus-out lines (IH) to A bus	CI-6, CI-9*
SAXSL	Transfer contents of bus-out lines to A bus	CI-6, CI-9* SERDES-4
SB0, SB1	SB field bits 0 and 1 of read-only memory	REG-1 ROM-4(2)
SBEQ1-SBEQ3	SB field of read-only memory equals 1 through 3	ALU-1 REG-1
SC0-SC2	SC field bits 0 through 2 of read-only memory	ROM-4(2)
SCANSW	SCAN position of MODE SELECT switch	TEST-1
SCHAM	Search for address mark	SERDES-2
SD0-SD4	SD field bits 0 through 4 of read-only memory	ROM-4(2) REG-1
SDXBY	Destination of ALU bus content is BY register	REG-1
SDXDR	Destination of ALU bus content is DR register	REG-1
SELOUTA	Select-out – Channel A	CI-2
SELOUTB	Select-out – Channel B	CI-3
SELREC	Select-out receive control	TEST-1
SELRST	Selective reset	TIM-3
SELSETST7	Selectively set ST7	TIM-3
SELTO	Select-out	CI-2
SEPCLK	Separated clock	SERDES-1
SEPDATA	Separated data	SERDES-1
SERCONT	Serializer control	SERDES-3
SERVINA	Service-in – Channel A	CI-7, CI-10*
SERVINB	Service-in – Channel B	CI-8, CI-11*
SERVO	Service-out	CI-2
SERVOUTA	Service-out – Channel A	CI-2

Signal Mnemonic	Destination	Source
SERVOUTB	Service-out – Channel B	CI-3
SETA	Set A register, B register, and arithmetic controls	ROM-2
SETBX	Set BX register control	SERDES-4
SETBUF	Set buffer registers	ROM-4(1) ROM-4(2)
SETCHANRST	Set channel reset latch	TIM-3
SETCX	Set CX register control	SERDES-4
SETERR0	Set ER register bit 0	SERDES-3
SETBXP	Set BX register parity bit control	REG-1
SETBX01- SETBX67	Set BX register bits 0 through 7 control	REG-1
SETBYP	Set BY register parity bit control	REG-1
SETBY01- SETBY67	Set BY register bits 0 through 7 control	REG-1
SETCARRY	Set carry latch (ST3) control	REG-1
SETCXP	Set CX register parity bit control	REG-1
SETCX01- SETCX67	Set CX register bits 0 through 7 control	REG-1
SETDHP	Set DH register parity bit control	REG-1
SETDH01- SETDH67	Set DH register bits 0 through 7 control	REG-1
SETDISP01- SETDISP67	Set display register bits 0 through 7 control	REG-1
SETDLP	Set DL register parity bit control	REG-1
SETDL01- SETDL67	Set DL register bits 0 through 7 control	REG-1
SETDR	Set DR register control	REG-6
SETDRP	Set DR register parity bit control	REG-1
SETDR01- SETDR67	Set DR register bits 0 through 7 control	REG-1
SETDWP	Set DW register parity bit control	REG-1
SETDW01- SETDW67	Set DW register bits 0 through 7 control	REG-1

Signal Mnemonic	Description	Source
SETFC01-SETFC67	Set FC register bits 0 through 7 control	REG-1
SETFRP	Set FR register parity bit control	REG-1
SETFR01-SETFR67	Set FR register bits 0 through 7 control	REG-1
SETFT01-SETFT67	Set FT register bits 0 through 7 control	REG-1
SETGLP	Set GL register parity bit control	REG-1
SETGL01-SETGL67	Set GL register bits 0 through 7 control	REG-1
SETGP	Set GP register control	REG-1
SETGRSTA	Set general reset – Channel A	TIM-2
SETGRSTB	Set general reset – Channel B	TIM-2
SETIE	Set IE register control	REG-1
SETIG01-SSTIG67	Set IG register bits 0 through 7 control	REG-1
SETKLP	Set KL register parity bit control	REG-1
SETKL01-SETKL67	Set KL register bits 0 through 7 control	REG-1
SETOPP	Set OP register parity bit control	REG-1
SETOP01-SETOP67	Set OP register bits 0 through 7 control	REG-1
SETPH	Set phase lock circuits to proper phase	SERDES-2
SETRAD0-8	Set read-only memory address register bits 0 through 8	ROM-2
SETRAD9-10	Set read-only memory address register bits 9 and 10	ROM-2
SETSD0-7	Set SD bit 0 through 7 decoder	REG-1
SETSD8-15	Set SD bit 8 through 15 decoder	REG-1
SETSD16-23	Set SD bit 16 through 23 decoder	REG-1
SETSP	Set SP register control	REG-1
SETSRSTA	Set selective reset – Channel A	TIM-2
SETSRSTB	Set selective reset– Channel B	TIM-2
SETSS0-7	Set SS bit 0 through 7 decoder	REG-1
SETSS8-15	Set SS bit 8 through 15 decoder	REG-1

Signal Mnemonic	Description	Source
SETST4	Set ST register bit 4	SERDES-4
SETSTART	Set the read-only memory address register with the contents of the START ADDRESS switches	TIM-3
SETSW	SET ADDRESS switch	TEST-1
SETSWREG	Set SW register control	REG-1
SETUR	Set UR register control	REG-1
SGLSTPSW	SINGLE STEP STOP position of CHK STOP/RUN/SINGLE STEP STOP switch	TEST-1
SH0-SH3	SH field bits 0 through 3 of read-only memory	ROM-4(1)
SHEQ8	SH field equals 8	ROM-2
SK0-SK7	SK field bits 0 through 7 of read-only memory	ROM-4(2)
SL0-SL3	SL field bits 0 through 3 of read-only memory	ROM-4(1)
SLDR	Transfer contents of bus-out lines into DR register	CI-6, CI-9*
SLEQ6	SL field equals 6	ROM-2
SN0-SN5	SN field bits 0 through 5 of read-only memory	ROM-4(1)
SORSP	Service-out responding	CI-6, CI-9*
SPARE2-SPARE4	Spare bits of read-only memory sense amplifier register (bits 2 through 4)	ROM-4(2)
SPP	SP register parity bit	REG-5
SP0-SP7	SP register bits 0 through 7	REG-5
SS0-SS3	SS field bits 0 through 3 of read-only memory	ROM-4(1)
SSM	Select spare module (drive)	DDI-2
ST0-ST7	ST register bit 0 through 7	REG-8
START0-START10	Outputs 0 through 10 of START ADDRESS switches	TEST-1
STARTSW	Start switch	TEST-1
STATINA	Status-in – Channel A	CI-7, CI-10*
STATINB	Status-in – Channel B	CI-8, CI-11*
STOP0-STOP10	Outputs 0 through 10 of STOP ADDRESS switches	TEST-1
STOPSW	STOP position of MODE SELECT switch	TEST-1
STPEQ	Stop equipment	ROM-2

Signal Mnemonic	Description	Source
SUPOUTA	Suppress-out – Channel A	CI-2
SUPOUTB	Suppress-out – Channel B	CI-3
SUPOUTA+B	Suppress-out – Channel A or B	CI-2
SUPPO	Suppress-out	CI-2
SV	SV bit of the read-only memory	ROM-4(2)
SVCINLTH	Service-in latch	CI-7, CI-10*
SVCINRST1	Service-in latch reset 1	CI-6, CI-9*
SVCINRST2	Service-in latch reset 2	CI-6, CI-9*
SVCREQ	Service request	CI-6, CI-9*
SYNCHUB	STOP ADDRESS SYNC test point signal	TIM-3
SYSSOURCEA	System voltage source – Channel A	PWR-1
SYSSOURCEB	System voltage source – Channel B	PWR-1
SW0-SW7	Multiplexed SW register bits 0 through 7	CI-4
SW0-0 – SW0-7	Disk drive 0 SW register bits 0 through 7	CI-4
SW1-0 – SW1-7	Disk drive 1 SW register bits 0 through 7	CI-4
SW2-0 – SW2-7	Disk drive 2 SW register bits 0 through 7	CI-4
SW3-0 – SW3-7	Disk drive 3 SW register bits 0 through 7	CI-4
SW4-0 – SW4-7	Disk drive 4 SW register bits 0 through 7	CI-4
SW5-0 – SW5-7	Disk drive 5 SW register bits 0 through 7	CI-4
SW6-0 – SW6-7	Disk drive 6 SW register bits 0 through 7	CI-4
SW7-0 – SW7-7	Disk drive 7 SW register bits 0 through 7	CI-4
TA-TD	Timing counter bits A through D	TIM-1
TB.5	Timing counter bit B.5 (half step between B and C)	TIM-1
TAG	TAG switch (controls unsolicited interrupts)	TEST-1
T0-T3	Timing signals 0 through 3	TIM-1
T1.5	Timing signal 1.5 (half step between 1 and 2)	TIM-1
TESTSW	TEST position of TEST/NORMAL/IN LINE switch	TEST-1
UB0-UB7	Unit bus lines 0 through 7 to disk drives (CD14)	DDI-3
UB0-UB8	Unit bus lines 0 through 8 to disk drives (1015)	DDI-3, DDI-11*
UMS0-UMS7	Unit module select – drives 0 through 7	DDI-2

Signal Mnemonic	Description	Source
UMSSM	Unit module select – spare module	DDI-2
URP	UR register parity bit	REG-5
UR0-UR7	UR register bits 0 through 7	REG-5
URWCA-URWCJ	Unit read/write coaxial cable – drives A through J (CD14 only)	SERDES-1
UTCC	Unit-Tag-Control line	DDI-3, DDI-11*
UTSC	Unit-Tag-Set cylinder	DDI-3, DDI-11*
UTSD	Unit-Tag-Set difference (CD14 only)	DDI-3, DDI-11*
UTSH	Unit-Tag-Set head	DDI-3
VCO	Voltage-controlled oscillator	SERDES-1
WRITEAM	Write address mark	SERDES-2
WRTDATA	Write data	SERDES-3
WRTENABLE	Write enable	SERDES-3
WRTGATE	Write gate	SERDES-3
WRTOUT	Write output	SERDES-3

DESCRIPTION OF MNEMONIC TERMS UNIQUE TO THE 1015 CONTROLLER

Signal Mnemonic	Description	Source
AB0-AB7	Address bus lines, AB0 thru AB7 represent FT3 and FC0 thru FC6 respectively for the reference cylinder address; AB1 thru AB8 represent FC0 thru FC7 respectively for the reference head address.	DDI-4
ATN0-ATN7	Gated attention latch signals for logical modules 0 thru 7.	DDI-5
CGAA/ ;D- CGAE/ ;D	Gated attention from disk drive units A thru E respectively.	DDI-1
CID1, CID2	The two LSB of the bit count appendage ID byte that identify physical spindle B, C, or D- used in writing the proceding record on the disk pack.	DDI-1
CLKCY03/- CLKCY47/	Reference cylinder address storage clock for logical modules 0 thru 7.	DDI-4
CLKHD03/- CLKHD47/	Reference head address storage clock for logical modules 0 thru 7.	DDI-4
CRDA-CRDE	Read data signals from disk drives A thru E respectively.	SERDES-1
CTLSD3, CTLSD4	SD field bits 3 and 4 control. Used to determine entry of CCAR, reference cylinder address, reference head address, and ID byte into the A bus.	DDI-4
CY0-CY7	Reference cylinder address register bits 0 thru 7.	DDI-4
FT3	Most significant bit of the unit bus lines (UB0).	DDI-3
GA0-GA7	Gated attention for logical modules 0 thru 7.	DDI-5
HD0-HD7	Reference head address register bits 0 thru 7.	DDI-4
OA0-OA7	Old address. Cylinder address register from the disk drive, reference head address, or reference cylinder address.	DDI-4
OFL0-OFL7	Offline signals for logical modules 0 thru 7.	DDI-5
ONL0-ONL7	Online signals for logical modules 0 thru 7.	DDI-5
PC0-PC7	Pack change for logical module 0 thru 7.	DDI-5
PCRST/	Pack change reset control.	DDI-5
PCSW0-PCSW7	Pack change switch (DRIVE STATUS switch) for logical module 0 thru 7.	DDI-5
RECAL/	Recalibrate	DDI-4
RTZ	Return to zero (recalibrate)	DDI-4
SELECT	Online logical module select.	DDI-4

Signal Mnemonic	Description	Source
SETSK	Seek latch set control	DDI-4
SK0-SK7	Seek signals for logical modules 0 thru 7 indicating that a seek has been issued to a specific logical module.	DDI-5
SKSTART	Seek start.	DDI-4
UMSA/ ;D- UMSE/ ;D	Unit module select – disk drives A thru E.	DDI-2
UWRA/ ;D- UWRE/ ;D	Write data signals from controller to disk drives A thru E.	SERDES-1

DESCRIPTION OF MNEMONIC TERMS UNIQUE TO THE 1015A CONTROLLER

Signal Mnemonic	Description	Source
AT0A-AT7A	Attention from logical modules 0 through 7 – Channel A	CI-6
AT8A-AT15A	Attention from logical modules 8 through 15 – Channel A	CI-7
AT0B-AT7B	Attention from logical modules 0 through 7 – Channel B	CI-6
AT8B-AT15B	Attention from logical modules 8 through 15 – Channel B	CI-7
ATTCU	Any logical module gated attention – Channel A and B	CI-8
ATTCU0-ATTCU7	Attention from logical modules 0 through 7 – Channel A or B	CI-6
ATTCU8-ATTCU15	Attention from logical modules 8 through 15 – Channel A or B	CI-7
ATTCUHIGHP	Any high priority logical module gated attention	CI-6
ATTCULOWP	Any low priority logical module gated attention	CI-7
ATTEN08	Any gated attention from logical modules 0 through 8	CI-8
ATTENTIONA	Attention from any logical module – Channel A	CI-8
ATTENTIONB	Attention from any logical module – Channel B	CI-8
ATTLOWPGATE	Low priority gated attention enable	CI-8
CGA0-CGA15	Gated attention – logical modules 0 through 15	DDI-3, DDI-4
CGASM	Gated attention – spare module	DDI-2
CID1-CID3	The three LSB of the bit count appendage ID byte	DDI-1
CLK0-CLK7	Clock SW register – logical modules 0 through 7	CI-4
CLK8-CLK15	Clock SW register – logical modules 8 through 15	CI-5
CPC	Pack change – any module	DDI-12
CPCHIGH	Pack change – any high addressed module	DDI-15
CPCLOW	Pack change – any low addressed module	DDI-14
CRDA-CRDJ	Read data signals from disk drives A through J	SERDES-1
CTLSD3, CTLSD4	SD field bits 3 and 4 control	DDI-12
CYLREFCLK	Cylinder reference register clock	DDI-12
DESELCEVENA-DESELCEVENJ	Deselect even logical module – disk drives A through J	DDI-2

Signal Mnemonic	Description	Source
DESELCODDA-DESELCODDJ	Deselect odd logical module -- disk drives A through J	DDI-2
EVENMODSEL	Even module select	DDI-12
FCXCY	Transfer FC register contents into cylinder reference register	DDI-12
FCXHD	Transfer FC register contents into head reference register	DDI-12
FORCESC	Force seek complete	DDI-12
GA0-GA7	Gated attention for logical modules 0 through 7	DDI-14
GA8-GA15	Gated attention for logical modules 8 through 15	DDI-15
GPXHD	Transfer GP register contents into head reference register	DDI-12
HDREFCLK	Head reference register clock	DDI-12
HIGHADDR	High address (logical modules 8 through 15)	DDI-12
LOWADDR	Low address (logical modules 0 through 7)	DDI-12
NOSEEKA-NOSEEKJ	No seek – disk drives A through J	DDI-10
OA0-OA7	Old address bits 0 through 7	DDI-13
ODDMODSEL	Odd module select	DDI-12
PCRST	Pack change reset	DDI-12
PCSW0-PCSW7	Pack change switches 0 through 7	DDI-14
PCSW8-PCSW15	Pack change switches 8 through 15	DDI-15
RECAL	Recalibrate (return to zero)	DDI-12
RTZ	Return to zero (recalibrate)	DDI-12
SAEx-SJEx	Even logical module address switches – disk drives A through J	DDI-2
SAOx-SJOx	Odd logical module address switches – disk drives A through J	DDI-2
SAXSC	Place seek complete (SC) on A-bus when SA field equals 13	DDI-10
SDXOP	Load seek complete (on A-bus) into OP register when SD field equals 7	DDI-10
SELECT	Module select	DDI-12
SETENAST4	Set enable for ST4	DDI-12
SETSK	Set seek	DDI-12
SETST4G	Set ST4 gated	DDI-10

Signal Mnemonic	Description	Source
SETST4LTH	Set ST4 latch	DDI-10
SK0LTH-SK7LTH	Seek latch for modules 0 through 7	DDI-14
SK8LTH-SK15LTH	Seek latch for modules 8 through 15	DDI-15
SKA-SKH	Seek previously issued for companion module of logical modules 0, 2, 4, 6, 8, 10, 12, and 14 respectively	DDI-8
SKEVENA-SKEVENJ	Seek issued for even logical module – disk drives A through J	DDI-9
SKJ-SKS	Seek previously issued for companion module of logical modules 1, 3, 5, 7, 9, 11, 13, and 15 respectively	DDI-9
SKODDA-SKODDJ	Seek issued for odd logical module – disk drives A through J	DDI-8
SKSTART	Seek start	DDI-12
SP0-SP2	Special field bits 0 through 2 of read-only memory	ROM-4(1)
SPARESELCTA-SPARESELCTJ	Spare module selected – disk drives A through J	DDI-2
SSM	Select spare module	DDI-12
SW0-SW7	Multiplexed SW register bits (high or low address)	CI-8
SW0H-SW7H	Multiplexed SW register bits 0 through 7 (high address)	CI-5
SW0L-SW7L	Multiplexed SW register bits 0 through 7 (low address)	CI-4
UMS0-UMS15	Unit module select – logical modules 0 through 15	DDI-5, DDI-6
UMS0SW-UMS15SW	Unit module select switches – logical modules 0 through 15	DDI-5, DDI-6
UMSA-UMSJ	Unit module select – disk drives A through J	DDI-7
UMSAEVEN-UMSJEVEN	Even logical module select – disk drives A through J	DDI-5
UMSAODD-UMSJODD	Odd logical module select – disk drives A through J	DDI-6
UMSSM	Unit module select – spare module	DDI-12
UWRA/ ;D-UWRJ/ ;D	Write data signals – controller to disk drives A through J	SERDES-1
ZEROHDCY	Set selected head and cylinder reference registers to zero	DDI-12
214A-214J	Disk drive A through J ID switches indicating 214 disk drive	DDI-2
214ASEL-214JSEL	Disk drive A through J selected is a 214	DDI-2
214 SELECTED	Selected disk drive is a 214	DDI-2
215A-215J	Disk drive A through J ID switches indicating 215 disk drive	DDI-2

APPENDIX B
REGISTER BIT MEANINGS

ER REGISTER

ER0 - Write data error
ER1 – Address-out
ER2 – Bus-out parity check
ER3 – Controller end outstanding (busy)
ER4 – ALU check
ER5 – Not used
ER6 – Channel B selected (2-channel controller only)
ER7 – Halt I/O

FT REGISTER

FT0 – Control tag
FT1 – Set cylinder address tag
FT2 – Set head tag
FT3 – Set difference tag (CD14)
FT3 – Cylinder 256 (1015)
FT4 – Address mark
FT5 – Reseek latch (1015 only)
FT6 – Burst even
FT7 – File select

FC REGISTER WITH CONTROL TAG (FT0)

FC0 – Write gate
FC1 – Read gate
FC2 – Seek start
FC3 – Head reset
FC4 – Erase gate
FC5 – Select head
FC6 – Return to 0
FC7 – Head advance

FC REGISTER WITH SET CYLINDER TAG (FT1)

FC0 – Cylinder 128
FC1 – Cylinder 64
FC2 – Cylinder 32
FC3 – Cylinder 16
FC4 – Cylinder 8
FC5 – Cylinder 4
FC6 – Cylinder 2
FC7 – Cylinder 1

FC REGISTER WITH SET SIGN AND HEAD TAG (FT2)

FC0 – Forward
FC1 – Not used
FC2 – Not used
FC3 – Head 16
FC4 – Head 8
FC5 – Head 4
FC6 – Head 2
FC7 – Head 1

FC REGISTER WITH SET DIFFERENCE TAG (FT3) (CD14 only)

FC0 – Difference Address 128
FC1 – Difference Address 64
FC2 – Difference Address 32
FC3 – Difference Address 16
FC4 – Difference Address 8
FC5 – Difference Address 4
FC6 – Difference Address 2
FC7 – Difference Address 1

The Difference Address is defined as the complement of the difference between the old address and new address.

Example: For a difference of one cylinder between old address and new address, Difference Address equals 11111110.

FS GATING

FS0 – Busy
FS1 – On line
FS2 – Unsafe
FS3 – Write current sense
FS4 – Pack change
FS5 – End of cylinder
FS6 – Multiple module select
FS7 – Seek incomplete

IE REGISTER

IE0 – Load or routine position of MODE SELECT switch
IE1 – Load, error, or result position of MODE SELECT switch
IE2 – Not used
IE3 – } These three bits form an
IE4 – } execution control code for
IE5 – } inline diagnostic routines.
IE6 – Chaining inline diagnostic routines
IE7 – Module select–FT7

IG REGISTER

IG0 – Write latch
IG1 – Reset operational-in latch
Drops operational-in to channel. Degates Status-in and Address-in
IG2 – Read latch
IG3 – Request-in (gated by not Suppress-out)
IG4 – Poll enable
Raises Request-in when attention is received from a disk drive
IG5 – Status-in

IG6 – With Operational-in high: Data transfer not suppressable
With Operational-in low: Request-in (not gated by Suppress-out)
IG7 – Address-in
Turns on Operational-in; raises Address-in when Address-out is low.

IS GATING

IS0 – MSB
IS1 –
IS2 –
IS3 – LSB
} Controller address
IS4 – Drive A selected
IS5 – File operable
IS6 – Spare drive gated attention
IS7 – Any gated attention

ST REGISTER

ST0 – Controlled by SS field of ROM
ST1 – Microprogram enables ST1 to be turned on by disk drive index signal. Turned off by microprogram, which provides index branching condition.
ST2 – Enabled by SS field. Turned on by ALU bus being non-zero (DNST21).
Turned off by microprogram SS field.
ST3 – Controlled by SS field. Also turned on and off as a result of the carry from the ALU when arithmetic statement contains a C after the destination register. ST3 is source of carry in certain arithmetic statements.
ST4 – Turned on only by serializer/deserializer.
Turned off only by SS field. In read operation, ST4=1 indicates byte has been deserialized and placed in DR register. In write operation, ST4=1 indicates byte has been taken from DR register for serializing. In a 1015A controller, ST4 is also set when low priority gated attentions are contained in the SW register, when an addressed logical module's companion module has previously been issued a seek, or when a reserve or release command is to be executed for a two-channel controller.
ST5 – Controlled by SS field.
ST6 – Controlled by SS field.
ST7 – Controlled by SS field. Also turned on by selective reset.

SW REGISTER (2-CHANNEL CONTROLLER ONLY)

SW0 – Device reserved for Channel A
SW1 – Device end – Pack change – Channel A
SW2 – Device end – Seek complete – Channel A
SW3 – Seek in progress – Channel A
SW4 – Device reserved for Channel B
SW5 – Device end – Pack change – Channel B
SW6 – Device end – Seek complete – Channel B
SW7 – Seek in progress – Channel B

APPENDIX C
MICROPROGRAM ORGANIZATION

The basic organization of the microprogram is shown in Figure C-1.

The microprogram is divided into seven basic routines; five are operational and two are diagnostic. Some operational routines are further broken down into subroutines as shown below:

Selection

- Initial Selection
- Chained Reselection

Command Decode

Initial Status Presentation

- Write Immediate
- Not Write Oriented

Command Execution

- Sense I/O
- Control Commands
- Index Processing
- Flag Byte Processing
- Load Counts
- Read or Clocking
- Search or Scan
- Write
- Gap Operation
- Check Byte Processing

End Procedure

The two diagnostic routine groups are the resident diagnostic and the inline diagnostic.

MICROPROGRAM OPERATION

The microprogram runs continuously from the time the controller power-up sequence is completed. The power-up sequence or any machine reset causes the microprogram to start (or restart) at address 000. The microprogram resets any outstanding attentions and enters the wait loop pending a command from the channel.

Initial Selection

Initial selection is initiated by the channel when the CPU issues a start I/O instruction. The start I/O instruction determines the controller and the disk drive to be used for the pending operation. When the channel raises the select-out tag line, the microprogram branches out of the wait loop and performs tests to determine the type of selection.

Channel Reselection

Entry into the chained reselection routine is from the end procedure routine when the previous operation indicates chaining. A timer controls the activation or deactivation of the write, erase, and read gates because the operation to follow must occur within a certain time to prevent running into the next area of the track. Within this routine, checks are made for index and, if detected, the microprogram exits to the end procedure routine and indicates to the channel that the selected drive is inoperable. Before the chained reselection routine exits to the command decode routine, it informs the command decode routine whether or not the selected drive is oriented for a write condition.

Command Decode

The command decode routine is entered from the initial selection or from the chained reselection routine. When the microprogram has entered the command decode routine, a command is first decoded as to type (control, search, read, write, or test and sense I/O) and then further decoded into initial program load (IPL), home address (HA), count, key, data, control, sense I/O, or test I/O. The command is also checked against the file mask to determine whether the file mask has been violated; if so, the microprogram exits to the end procedure routine. The command decode routine normally exits to the initial status presentation routine to present status to the channel.

Initial Status Presentation – Write Immediate

The write immediate subroutine presents initial status to the channel for all commands that require a write operation to begin immediately. The previous settings of the ST register bits determine whether the microprogram begins writing bytes of zeros or continues to write bytes of ones (after a formatting write, but not HA). If no errors occur, the exit is to the load counts routine.

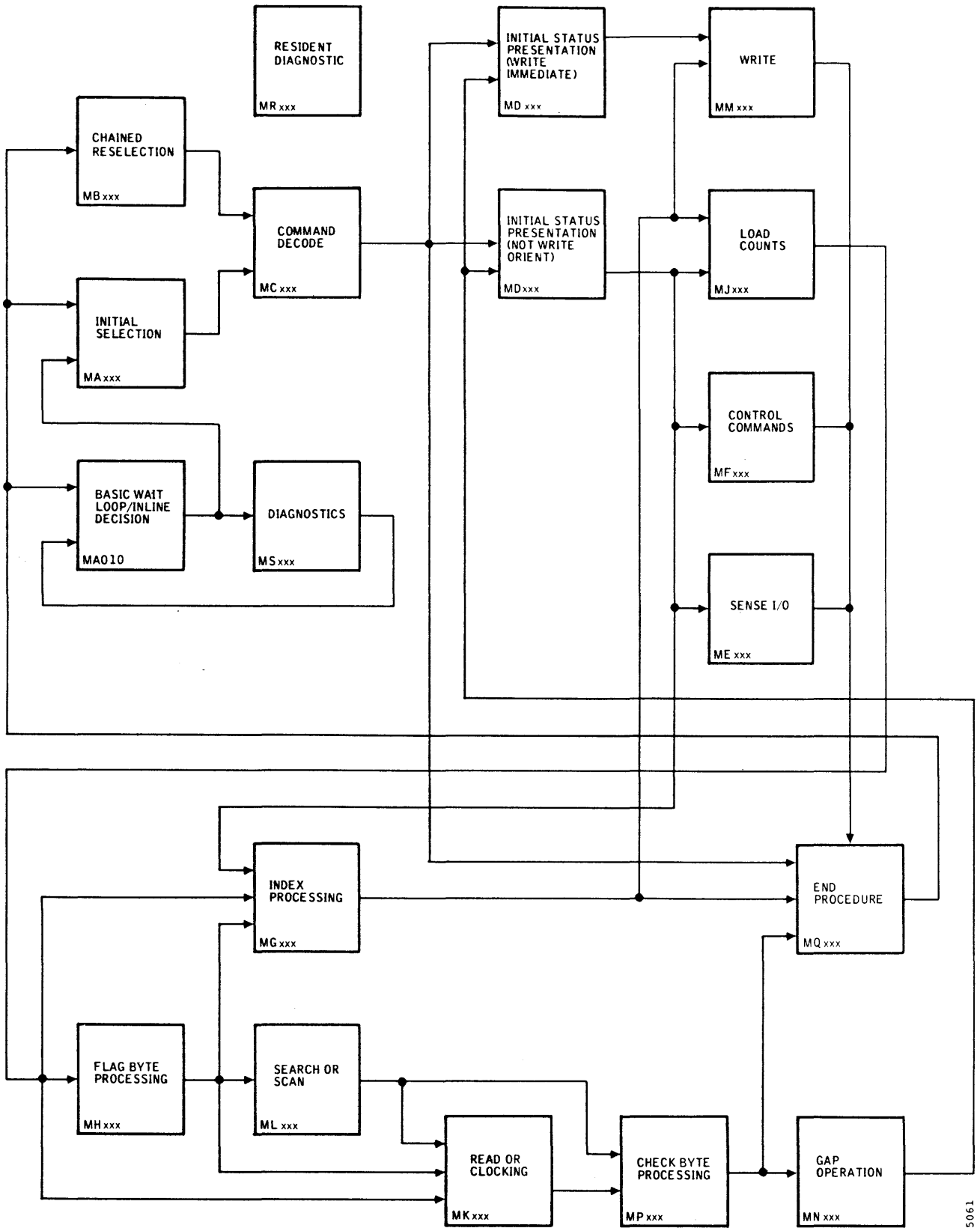


Figure C-1. Overall Microprogram Organization

Initial Status Presentation – Not Write Oriented

The not write oriented subroutine presents initial status to the channel for commands that do not require an immediate write operation.

Sense I/O

The sense I/O routine is entered from the initial status presentation (not write oriented) routine after the status byte has been accepted by the channel. If the sense information is stored, up to six bytes of information are routed to the channel. The number of bytes is dependent on the CCW count. If the sense information is not stored, the sense I/O routine transfers bytes of zeros to the channel (except bytes 3 and 4). This routine also controls the service-in/service-out communications for the transfer as well as for keeping track of the number of bytes transferred. The sense I/O routine exits to the end procedure routine.

Control Commands

The control commands routine determines the type of control command to be used. This routine checks the address data, decodes the address data, and sends it along with the proper tag line to the disk drives. This routine is also used by the set-file-mask command. File mask data is received from the channel and stored for use during seek and write commands. The control commands routine exits to the end procedure routine.

Index Processing

The index processing routine checks for missing address mark conditions, no-record-found conditions, and other timing conditions that require the index mark as a reference. When a home address is to be written, the index processing routine requests the flag byte from the channel to control the length of the home address gap. The index processing routine controls the head advance and end-of-cylinder condition during multiple track operations.

Flag Byte Processing

The flag byte processing routine checks for overflow records, missing address marks, and track condition bits. When a search home address command is to be executed, this routine stores the flag byte that is to be used in writing the flag byte in other records on the same track. The flag byte processing routine exits to the read or clocking routine or to the search or scan routine if the track condition is good; it exits to the end procedure routine if the track condition is defective.

Load Counts

The load counts routine checks the command type (CKD, KD, or D), checks the present orientation to the track, and prepares to read or clock the next field. This routine also maintains the key length and data length totals used in determining the gap length (see gap writing routine). The end-of-file, missing key area, key-length-zero, and data-length-equals-zero conditions are also checked by the load counts routine. This routine enables the controls to process these conditions in a read routine or in a search or scan routine.

Read or Clocking

The read portion of the routine gates bytes of data from the serializer/deserializer through the ALU to the channel. The clocking portion of the routine is used to clock over unwanted areas. Track orientation is updated in this routine so that proper decisions may be made in the burst byte processing routine.

Search or Scan

The search routine enables the transfer of data from the channel and from the selected disk drive. The data from the channel and that from the disk drive are compared on a byte-by-byte basis for high, low, or equal as dictated by the command. This routine sets controls which enable the setting of the status modifier. The scan routine is basically the same as the search routine except that the scan routine must inhibit comparing when a mask byte is received from the channel. The scan routine must also decrement a two-byte count since it operates on the data area as well as on count and key areas of a track.

Write

The write routine writes gaps (including address marks), receives data from the channel, and supplies data bytes to the serializer/deserializer. The write routine contains a gap-writing subroutine which controls the number of bytes written in a gap. The write routine loops within itself until the last area is written and then exits to the end procedure routine.

Gap Operation

The gap operation routine controls the turn-on of the read-gate for reading the sync byte to locate the next record.

Check Byte Processing

The check byte processing routine reads the two burst bytes, exclusively ORs the two burst bytes read from the disk with the two burst bytes generated during the read operation, and does a zero check. This routine also zero checks the bit count byte with the contents of the bit count register. If an error is found during the zero check in either of the two comparisons, the routine sets the data check error condition which is used in the sense byte.

End Procedure

Entry into the end procedure routine is from the command decode, initial status presentation, write, index processing, or check byte processing routines. Where an error has occurred or an end-of-operation is detected, entry is also made into the end procedure routines. This routine determines whether a chained or unchained end-of-operation condition exists and presents the ending status. During chained operations, the end procedure routine determines whether or not the next command will create an overrun condition. This routine also regenerates the address of the selected drive for use in the chained reselection and initial selection routines. The end procedure routine exits to the basic wait loop/inline decision loop to await the next operation.

APPENDIX D
FLOW DIAGRAMS

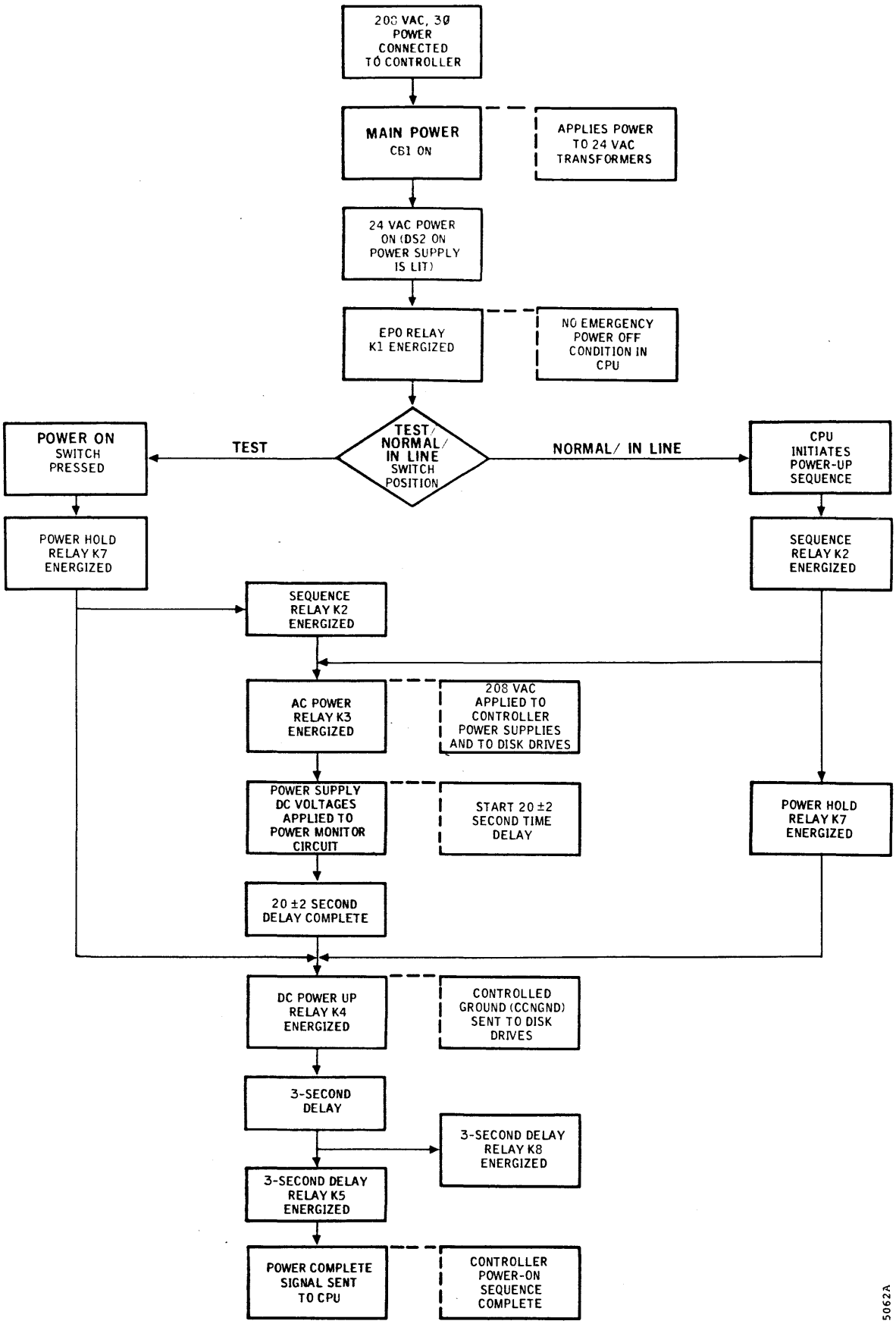


Figure D-1. Power-Up Sequence Flow Diagram

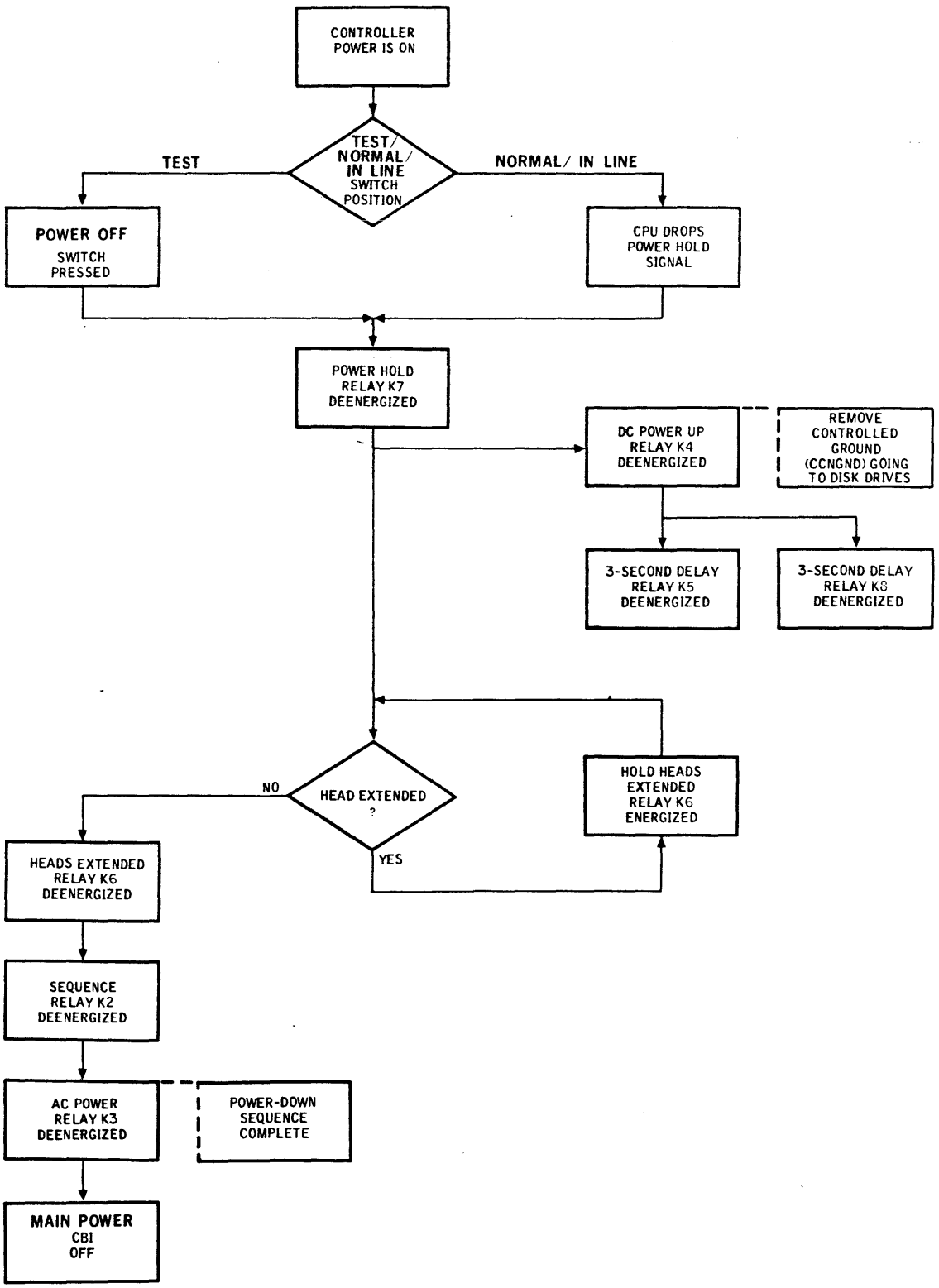


Figure D-2. Power-Down Sequence Flow Diagram

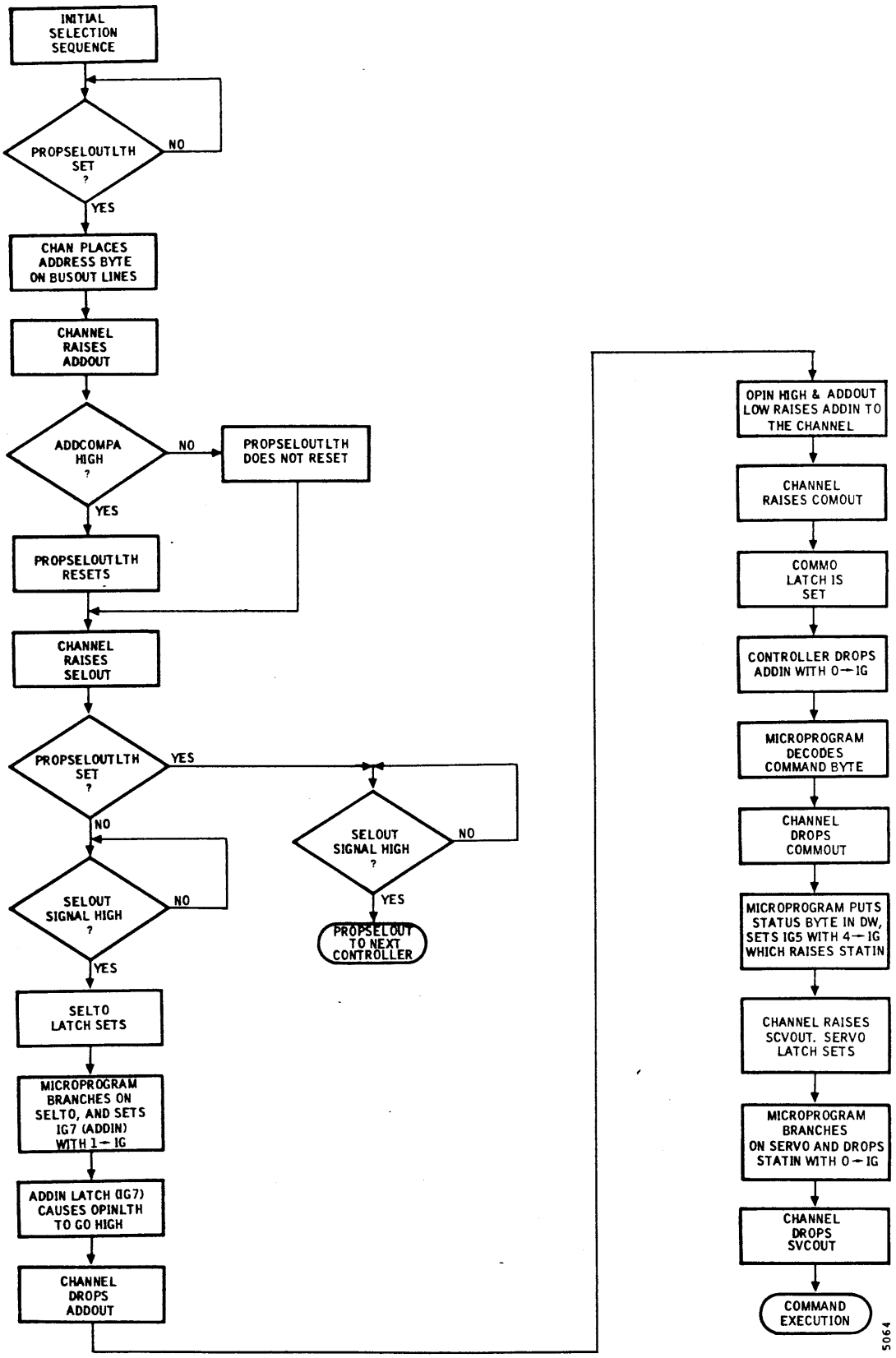


Figure D-3. Initial Selection Sequence Flow Diagram

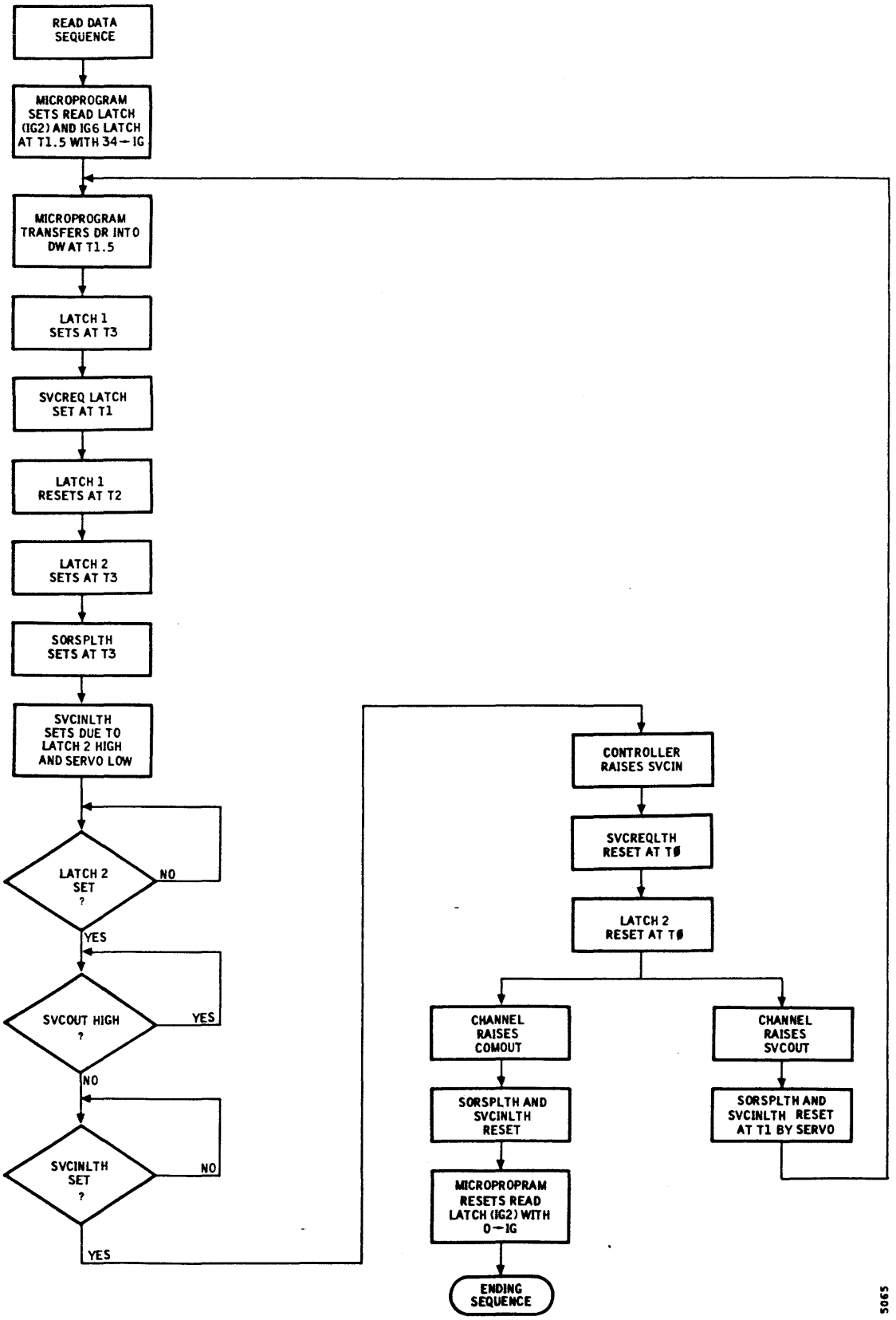


Figure D-4. Read Data Sequence Flow Diagram

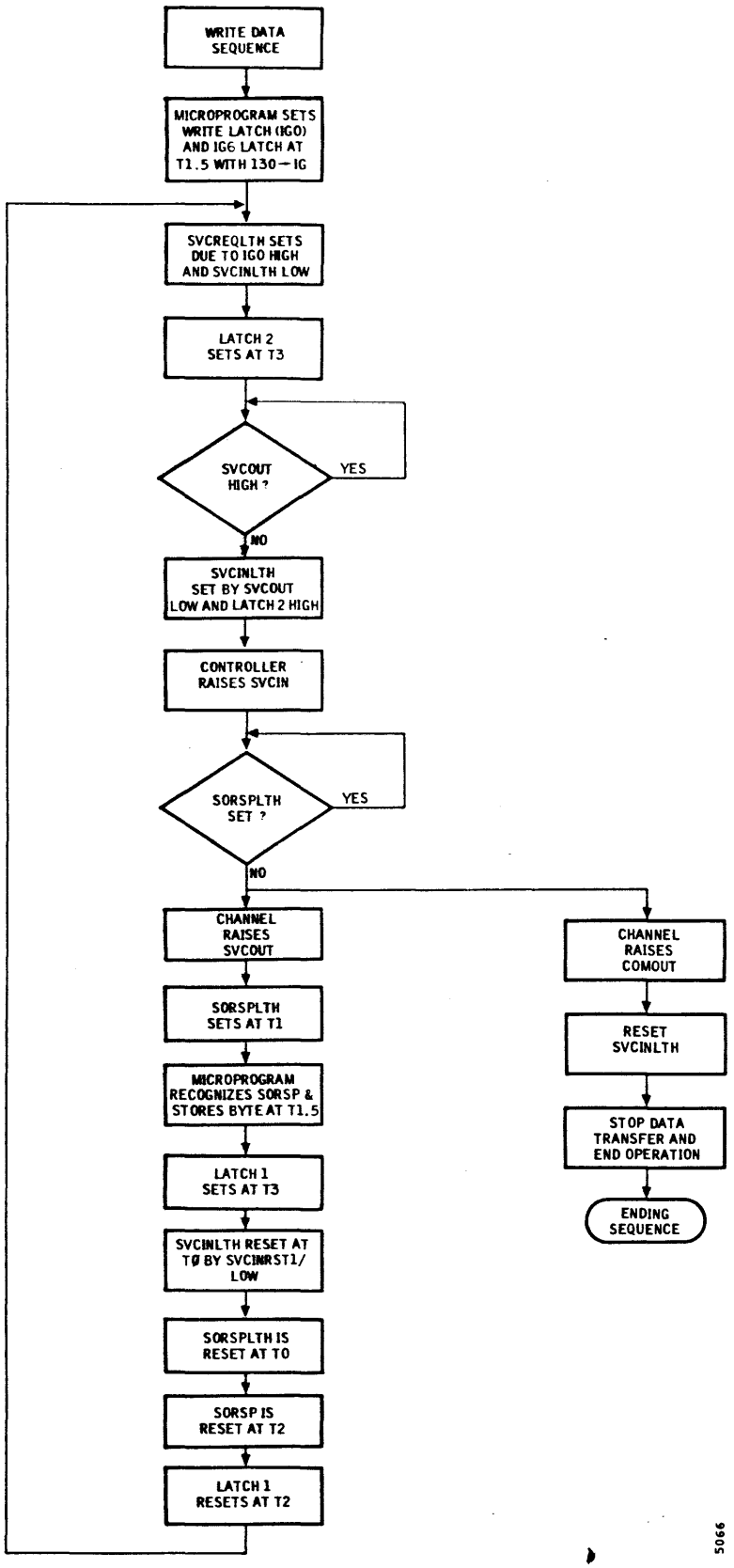


Figure D-5. Write Data Sequence Flow Diagram

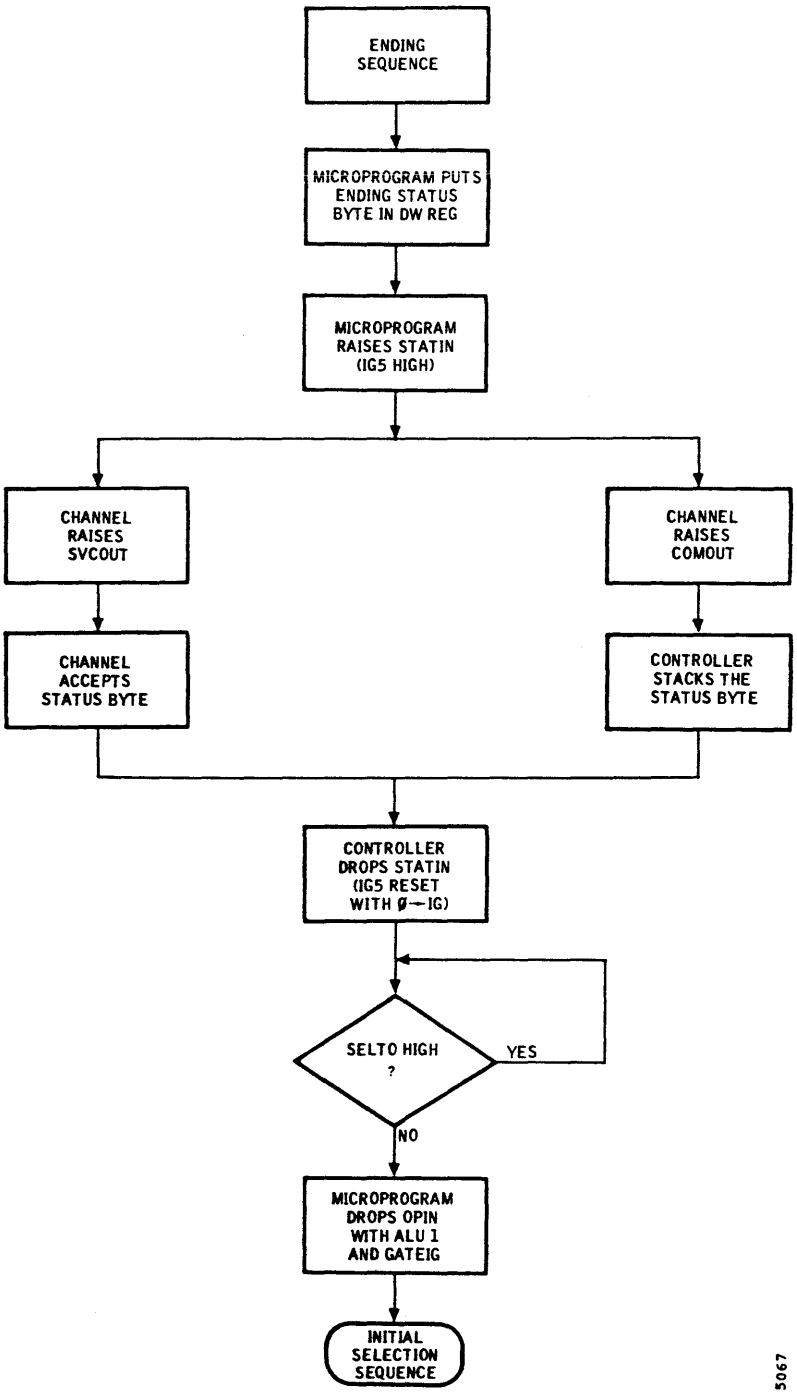


Figure D-6. Ending Sequence Flow Diagram

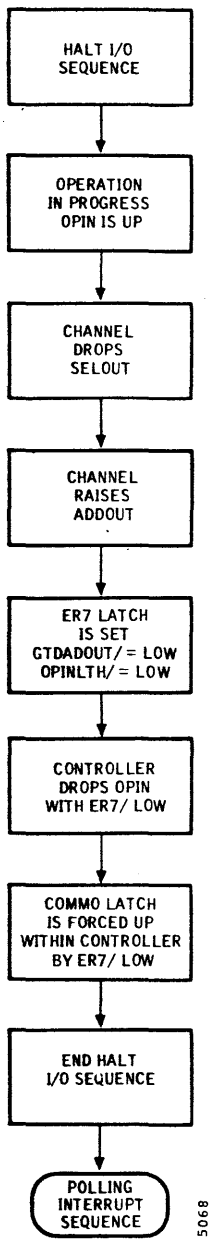


Figure D-7. Halt I/O Sequence Flow Diagram

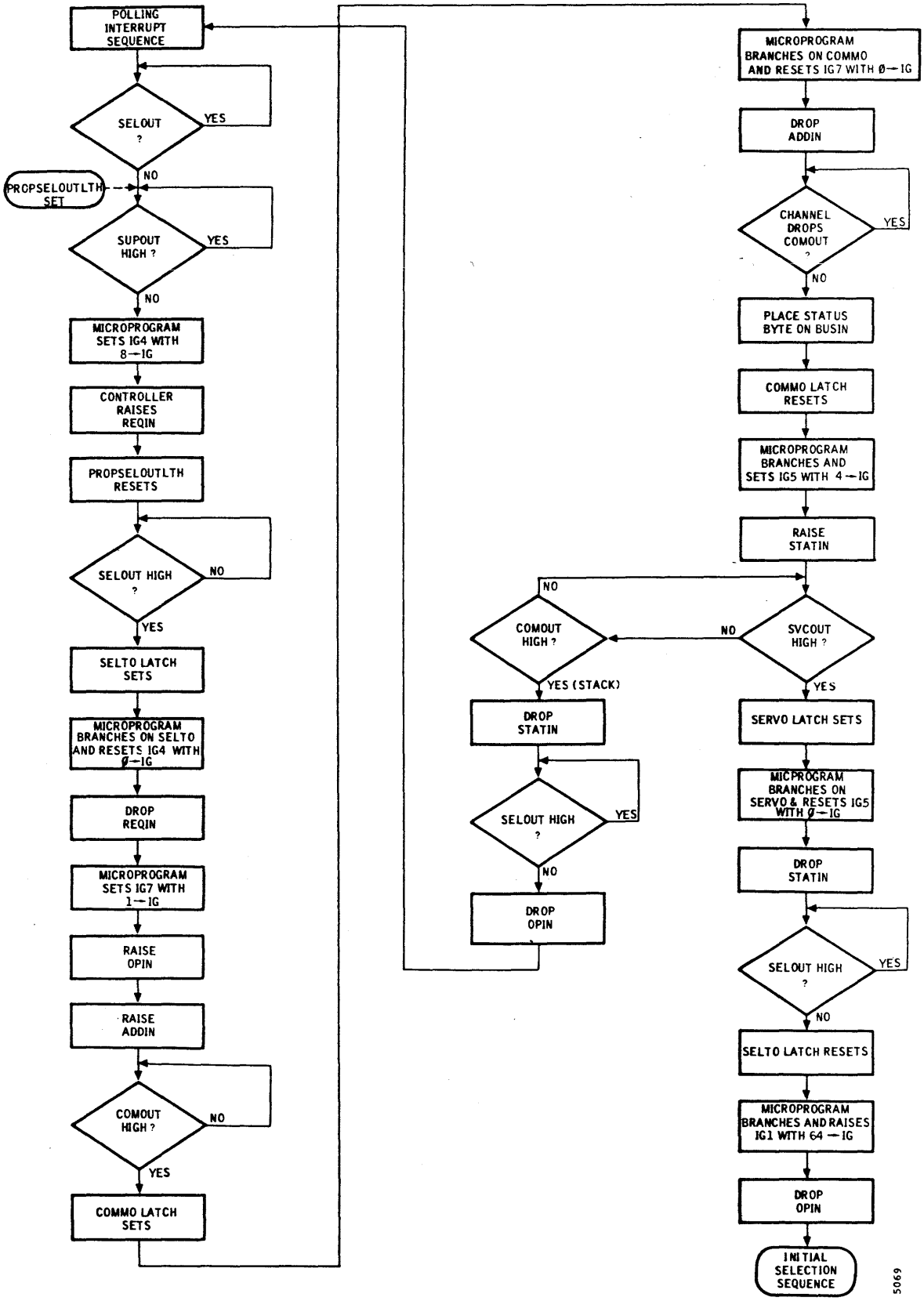


Figure D-8. Polling Interrupt Sequence Flow Diagram

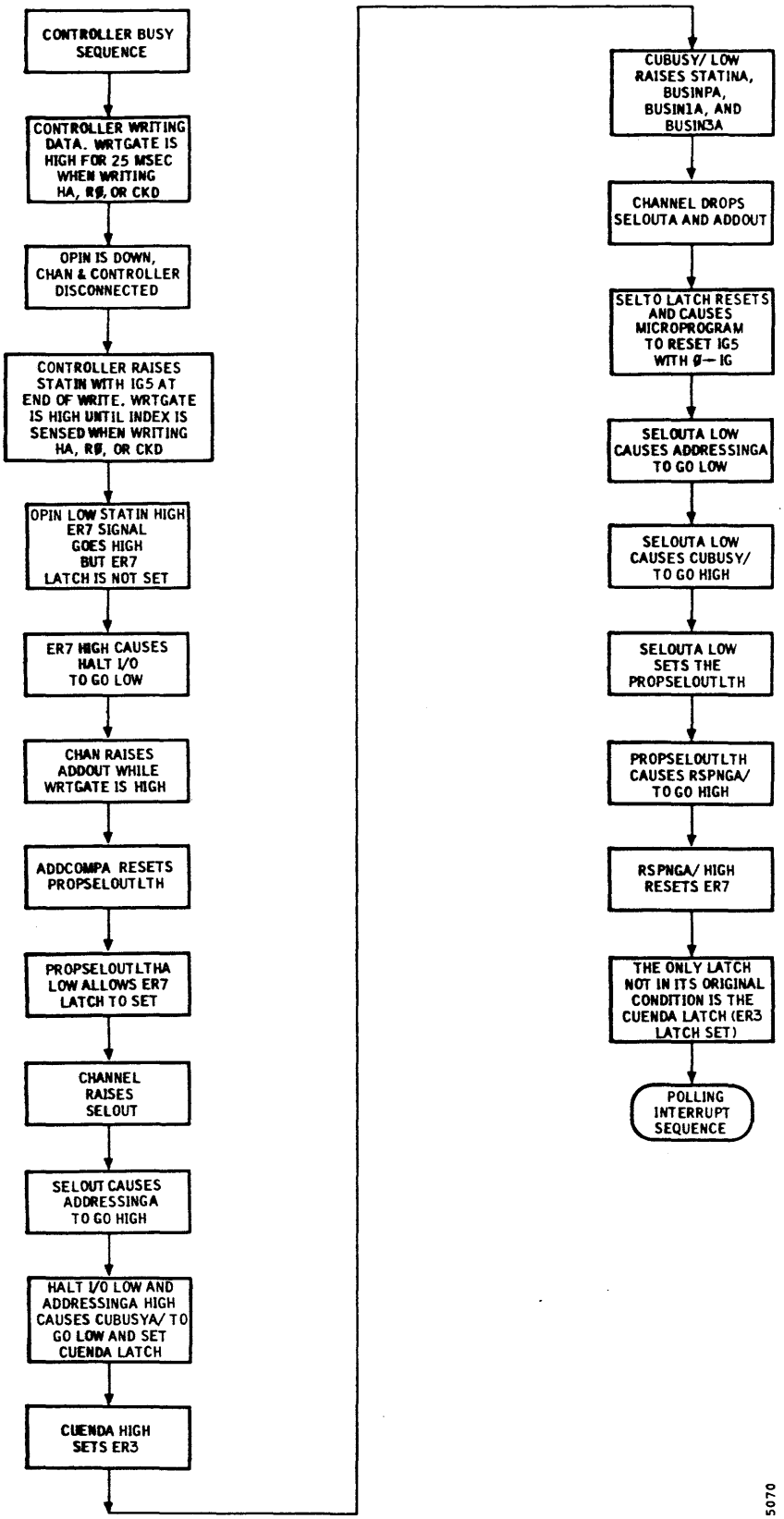


Figure D-9. Controller Busy Sequence Flow Diagram