Workstation Hardware

First Edition Revised, Update Notice 2
A-09-00066-01-A

The attached pages update: (1) edition (A-09-00016-01-A) and update notice (A-09-00058-01-A) or (2) edition (A-09-00016-01-B) of the Workstation Hardware Manual.

Insert these pages according to the collating instructions on the back of this Notice.

Updated pages are indicated by a date at the bottom of the page.

Throughout this Manual, change bars in the margins indicate technical additions and changes. Asterisks indicate deletions. Editorial changes are not identified. All changes will be incorporated into the next edition of this Manual.

Insert this page after the title page of your Manual to provide a record of this update.

Convergent Technologies

COLLATING INSTRUCTIONS

Delete	Replace With
v-x (Table of Contents)	v-x (Table of Contents)
Section 6 (6-1 to 6-8) and following three unpaginated foldouts: RAM Expansion Board (1 of 2 and 2 of 2), and Printed Circuit Assembly RAM Expansion Board	Section 6 (6-1 to 6-21)
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6. RAM EXPANSION BOARDS

OVERVIEW

The RAM Expansion Board contains the second set of dynamic RAM for a Convergent system. The Board can contain one to four banks of dynamic RAMs, each with 18 chips. There are two versions of this Board:

- o one for 16K bit chips (up to 128K bytes), and
- o one (RAM Expansion 2 Board) for 64K bit chips (up to 512K bytes).

OPERATION BY LOGIC BLOCK

RAM Array

For 16K bit RAMs, the 14 bits of addressing are multiplexed into a 7-bit row and a 7-bit column address. The chip is logically organized as a 128-square matrix of memory cells.

For 64K bit RAMs, the 16 bits of addressing are multiplexed into an 8-bit row and an 8-bit column address. The chip is logically organized as a 256-square matrix of memory cells.

The RAS- (Row Address Strobe) signal is used to latch the row address. The CAS- (Column Address Strobe) signal occurs next. It is used to latch the column address and to perform the data operation (read or write) on the addressed cell.

A write cycle is generated if the WE- pin is asserted at the leading edge of CAS-. The write data at the chip's data input pin is latched by the leading edge of CAS-.

A read cycle is generated if the WE- pin is inactive at the leading edge of CAS-, causing the data from the addressed cell to be driven on the chip's data output pin.

RAM Refresh

The RAMs are dynamic and require periodic refreshing to maintain data integrity. Whenever RAS- is asserted, all the cells on the addressed row are refreshed. For 16K bit RAMs, each cell must be refreshed every 2 ms, and for 64K bit RAMs, every 4 ms. This refreshing function is implemented using logic on the Processor and RAM Expansion Boards that generates a RAS- only refresh cycle to a row every 12.8 microseconds. The row refresh counter is incremented after every refresh cycle. Thus, for 16K bit RAMs, all 128 rows are refreshed in 1.64 ms, and, for 64K bit RAMs, 256 rows are refreshed in 3.28 ms.

Address Logic

All 72 chips in the array have the same RAS- signal. Bank selection is done by asserting one of the CAS4- - CAS7- signals. Therefore, each CAS- signal goes to 18 chips. The seven address pins, RAA0+ - RAA6+ (p2zD8) are connected in parallel to all 72 chips. On the RAM Expansion 2 Board, an additional address pin, RAA7+, is also bussed throughout the array.

The RAS- and CAS- signals are generated in the memory control section of the Processor Board. When they come onto the RAM Expansion Board, they are called RAS- (p2zA7) and CAS4- - CAS7- (p2zB8). AT 10F-11 (p2zA6), RAS- is gated so that only refreshes and accesses to the RAM Expansion Board (as opposed to the I/O Memory Board) generate the signal BRAS-. BRAS- connects to the RAS- pins of the RAMs. RFGO- indicates that a refresh is in progress, and BD2RAM- (from the Processor Board) indicates that the memory of the RAM Expansion Board is being accessed.

There are three sources for the address driven onto the RAM address lines: (1) the row address (6K(plzB6)), (2) the column address (5K(plzC6)), and, (3) the refresh row address (3K(plzD6)). The selection of which address driver is enabled

is made by the high-speed decoder consisting of 10J-3,6,8, and 11, and 10H-1 and 4 (plzC6). The RFGO- signal, when active, enables 3K and disables 5K and 6K. The COLMPX- (column multiplex) signal enables the row driver (6K) and disables the column driver (5K). COLMPX- and RFGO- come from the RAM controller on the Processor Board. RFDONE- from the Processor Board indicates that a refresh cycle has completed and causes the refresh address counters, 1K and 2K (plzD6), to increment.

Data Interface

The data input and data output pins from the RAMs are tied together, forming a bidirectional data bus (RAD0+ - RADF+) (p2zD2). Each data bus bit goes to four chips, one per bank. The parity bits, HIP+ (high-byte parity) and LOP+ (low-byte parity), are connected in the same fashion.

There are two write-enable signals, RAHIWE- (high- or odd-byte write-enable) and RALOWE- (low- or even-byte write-enable), that select writing on a byte basis. Each write-enable signal goes to one-half of the array (36 chips).

Data to and from the RAM array are buffered from the MEM bus (MEM0+ - MEMF+) by the transceivers at 9F and 9H (plzC3). The direction of the transceivers is established by the signal READ-, which is a buffered MR- (memory read) signal. The enable for the high-byte (odd) driver is HIEN- and for the low-byte (even) is LOEN-. HIEN- is asserted when the RAM Expansion RAM is addressed (BD2RAM- asserted at 10E-9 (p2zA9)) and either a read is in progress (MR- active) or the high-order byte write signal is active (RAHIWE-). LOEN- is asserted when the RAM expansion memory is addressed and either a read is in progress or the low-order byte write enable is active (RALOWE-).

Buffering For ROM Expansion Board

When a RAM Expansion Board and a ROM Expansion Board are both used on a motherboard, the ROM Expansion Board plugs into the P1 connector of the RAM Expansion Board. The address lines (LA1+ - LA10+) from the motherboard connector, J1, are buffered by chips 9A and 10A (plzB7) to become BLA1+ - BLA10+ (buffered local address) and go to P1. The data lines from the ROM Expansion Board (BMEM0+ - BMEMF+) are buffered by 9C and 10C

(plzB2) and driven onto the MEM bus (MEM0+ - MEMF+) at the J1 connector. Buffers 9C and 10C are enabled by the ROM Expansion Board decode signal from the Processor Board (PROMEXDC-).

AC CHARACTERISTICS

Refer to AC Characteristics in Chapter 4
(Processor Board)

Refer to DC Characteristics in Chapter 4
(Processor Board)

Edge-Connector Pin List

Connector J1

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	-12V
6	-12V
7	GND
8	GND
9	BD2RAM-
10	MR-
11	PROMEXDC-
12	COLMPX-
13	RFDONE-
14	RARAS-
15	GND
16	RFGO-
17	RALOWE-
18	RAHIWE-
19	CAS7-
20	CAS6-
21	CAS5-
22	CAS4-
23	HIP+
24	LOP+
25	GND
26	MEMF+
27	MEME+
28	MEMD+
29	MEMC+
30	MEMB+
31	MEMA+
32	MEM9+
33	MEM8+
34	MEM7+
35	GND
36	MEM6+
37	MEM5+
38	MEM4+
39	MEM3+
40	MEM2+
41	MEM1+
42	MEM0+
43	LA13+
44	LA12+
45	GND

Pin	Signal
46	LA11+
47	LA10+
48	LAF+
49	LAE+
50	LAD+
51	LAC+
52	LAB+
53	LAA+
54	LA9+
55	GND
56	LA8+
57	LA7+
58	LA6+
59	LA5+
60	LA4+
61	LA3+
62	LA2+
63	LA1+
64	LA0+
65	GND
66	GND
67	+12V
68	+12V
69	+12V
70	+12V
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75	
76	
77	+5V
78	+5V
79	+5V
80	+5V

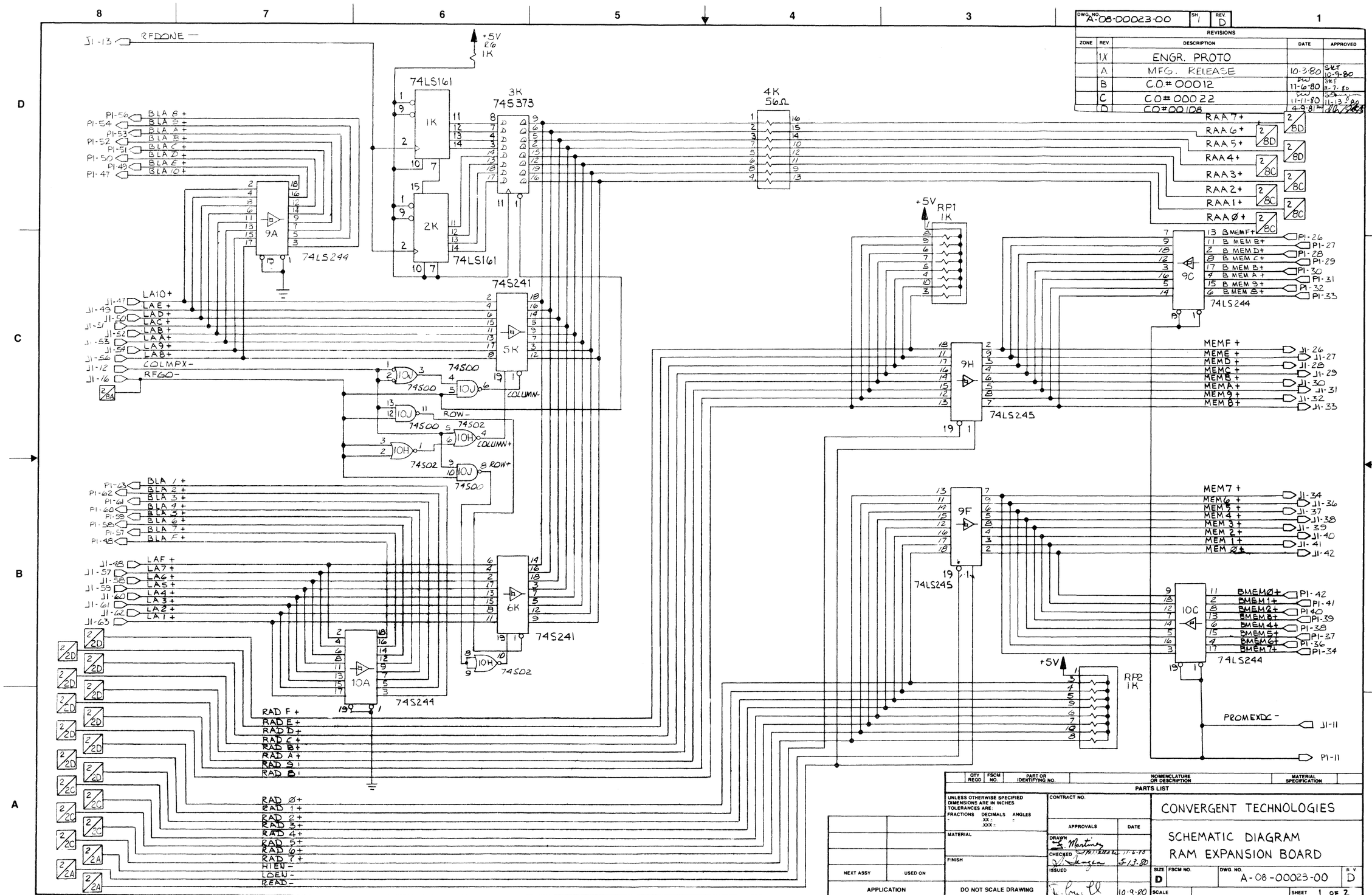

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Figure 6-1 16K RAM Expansion Board Schematic (Page 1 of 2)

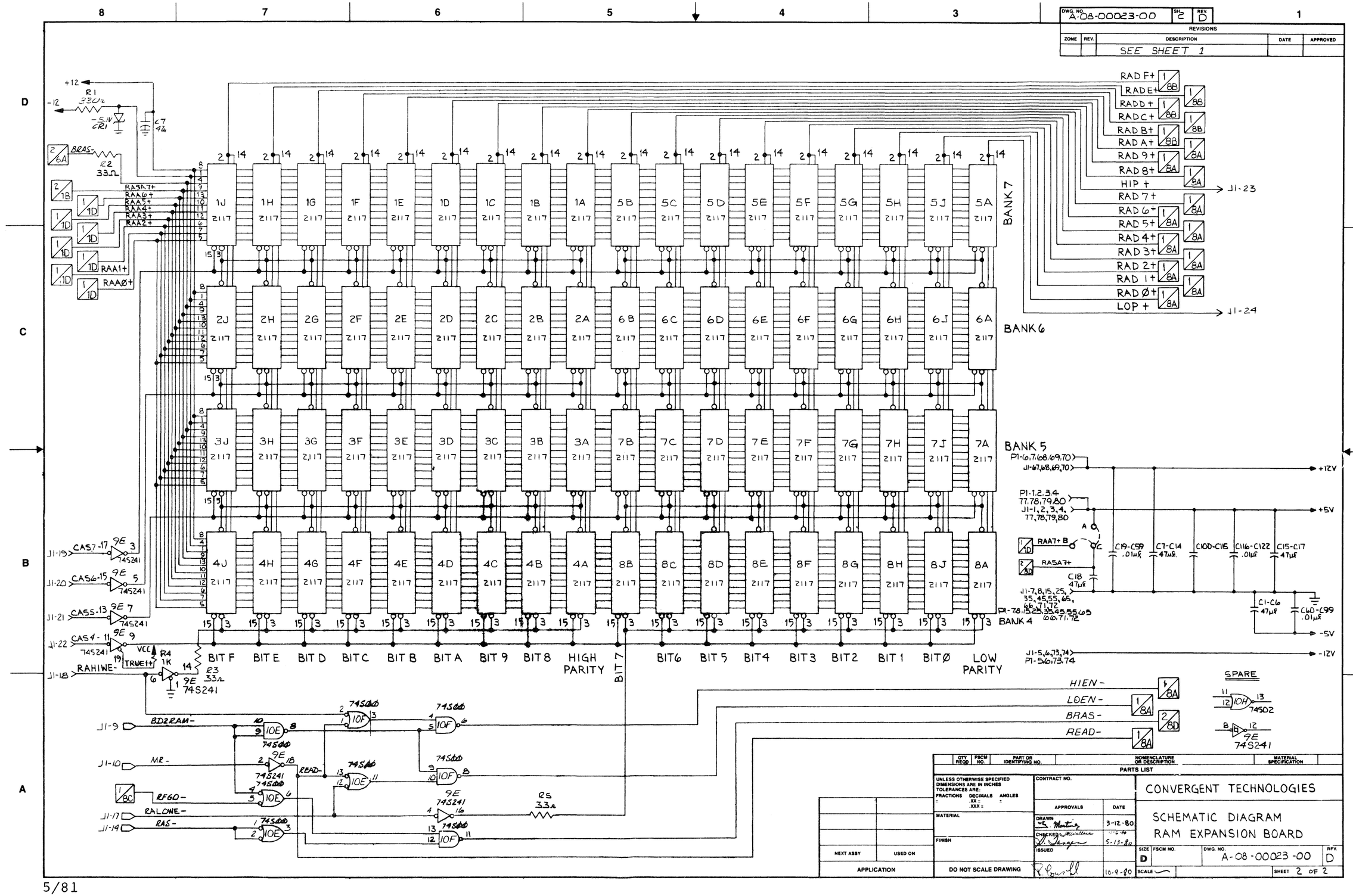

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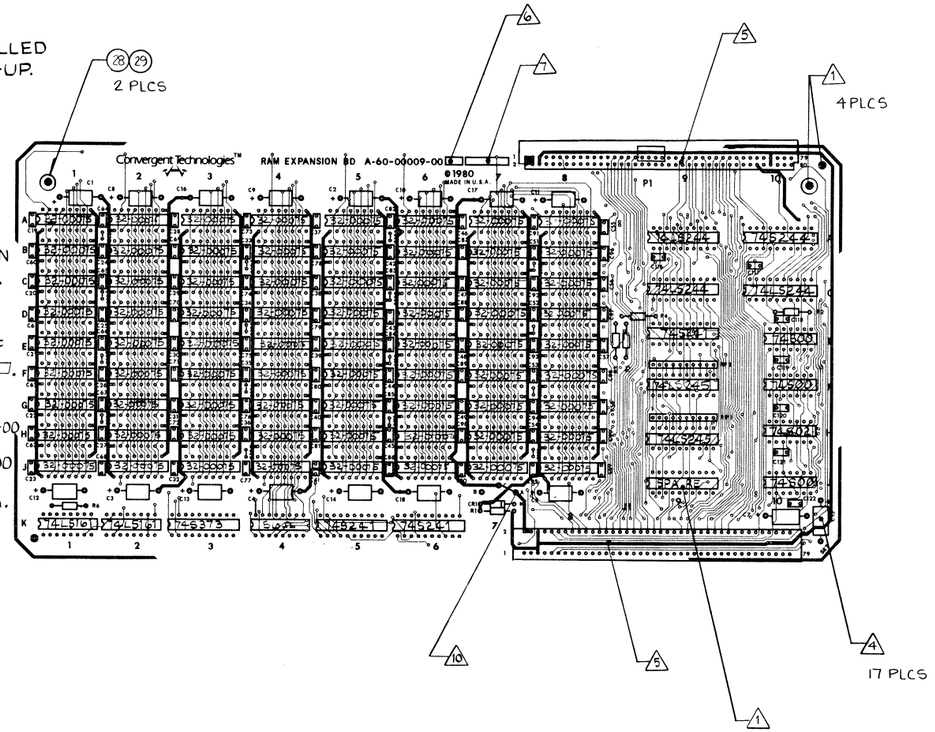
Figure 6-1 16K RAM Expansion Board Schematic (Page 2 of 2)

DWG. NO. A-60-00009-00 | SH 1 | REV. E

REVISIONS				
ZONE	REV.	DESCRIPTION	DATE	APPROVED
	A.	MFG. RELEASE	9-29-80	
	B	C.O.# 00012 - ADD SHT. 2	11-10-80	ST 11-11-80
	C	C.O.# 00022	11-11-80	ST 11-12-80
	C1	C.O.# 00035	11-26-80	ST 11-26-80
	D	C.O.# 00048	1-13-81	ST 1-13-81
	E	C.O.# 00108	4-9-81	4-13-81

NOTES:

1. MASK AREA INDICATED PRIOR TO LOADING.
2. SOCKETS TO BE INSTALLED BY SUB-CONTRACTOR. I.C. TO BE INSTALLED AT TEST.
3. MASK AREA INDICATED. COMPONENT TO BE INSTALLED AT TIME OF FINAL TOUCH-UP.
4. CONFIRM ORIENTATION.
5. USE OF SUPPORT FIXTURE REQUIRED DURING WAVE SOLDERING.
6. MARK ENGINEERING REVISION FOR THIS ASSEMBLY REV. IS D.
7. MARK APPROPRIATE DATE CODE TO SHOW DATE OF MANUFACTURE. DATE CODE IS ▭.
8. FOR COMPLETE LIST OF MATERIALS SEE A-60-00009-00
9. SCHEMATIC REF. A-08-00023-00
10. ADD CONFIGURATION JUMPER C-A.



QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN S A Wolpert	9-24-80
CHECKED	9-26-80
ISSUED	10-2-80

Convergent Technologies

PRINTED CIRCUIT ASSEMBLY
RAM EXPANSION BOARD

SIZE D | FSCM NO. | DWG. NO. A-60-00009-00 | REV. E

SCALE 1/1 | SHEET 1 OF 2

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Figure 6-2 16K RAM Expansion Board Assembly Drawing
(Page 1 of 2)

A-60-00009-00 | 2 | E

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		SEE SHEET 1		

NOTES:

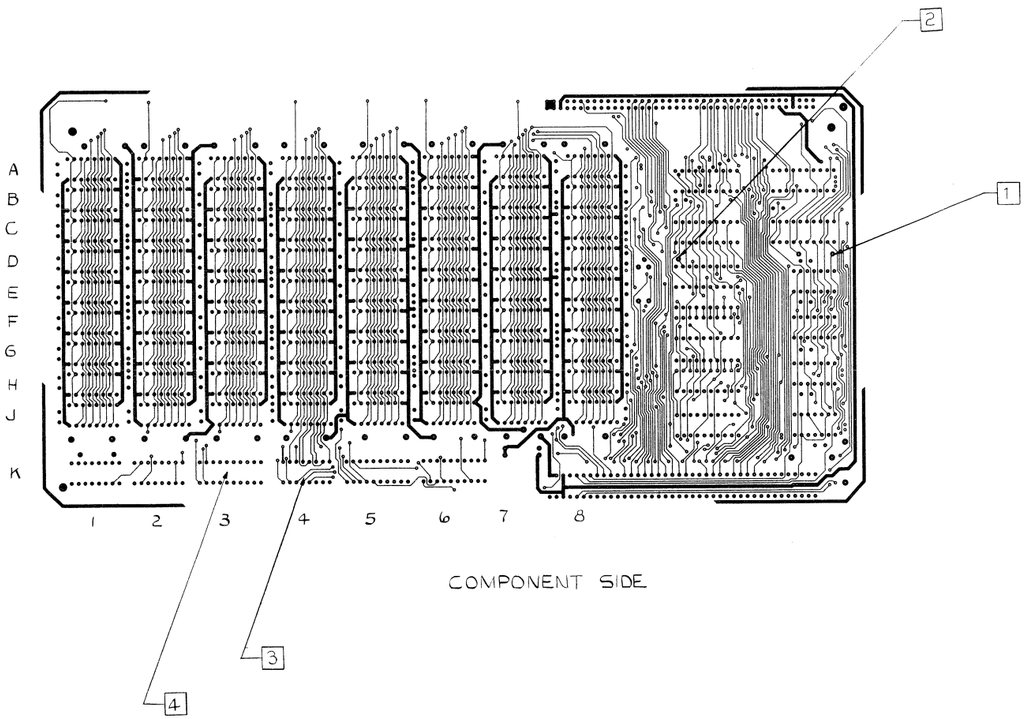
A. USE KYNAR WIRE, 30 AWG GREEN INSULATION FOR ALL JUMPERS

B. BOND JUMPERS TO PCB WITH HOT GLUE (APPROX. 1 INCH INCREMENTS.)

C. ALL JUMPERS TO BE WIRED TO THE TOPS OF IC LEGS WITH A MECHANICAL WRAP LEAD EXTENDING FROM THE MIDDLE OF THE IC LEG.

ON BOARD REVISION A:

1. REMOVE R2, 56 OHM (23-00005) AND REPLACE WITH 33 OHM (23-00002.)
2. REMOVE R4, 33 OHM (23-00002) AND REPLACE WITH 1K OHM (23-00029.)
3. REMOVE 4K, 33 OHM DIP (21-00002) AND REPLACE WITH 56 OHM DIP (21-00011)
4. REMOVE 3K, 74LS373 (32-00035) AND REPLACE WITH 74S373 (32-00060)
5. MARK ASSEMBLY REVISION D.



COMPONENT SIDE

QTY REQD	FSCM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
XX ±
XXX

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN [illegible]	11-11-80
CHECKED	
ISSUED	

NEXT ASSY | USED ON

APPLICATION

CONVERGENT TECHNOLOGIES

ASSEMBLY DRAWING-MODIFICATION

RAM EXPANSION

SIZE D | FSCM NO | DWG NO. A-60-00009-00 | REV E

SCALE 1:1 | SHEET 2 OF 2

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Figure 6-2 16K RAM Expansion Board Assembly Drawing
(Page 2 of 2)

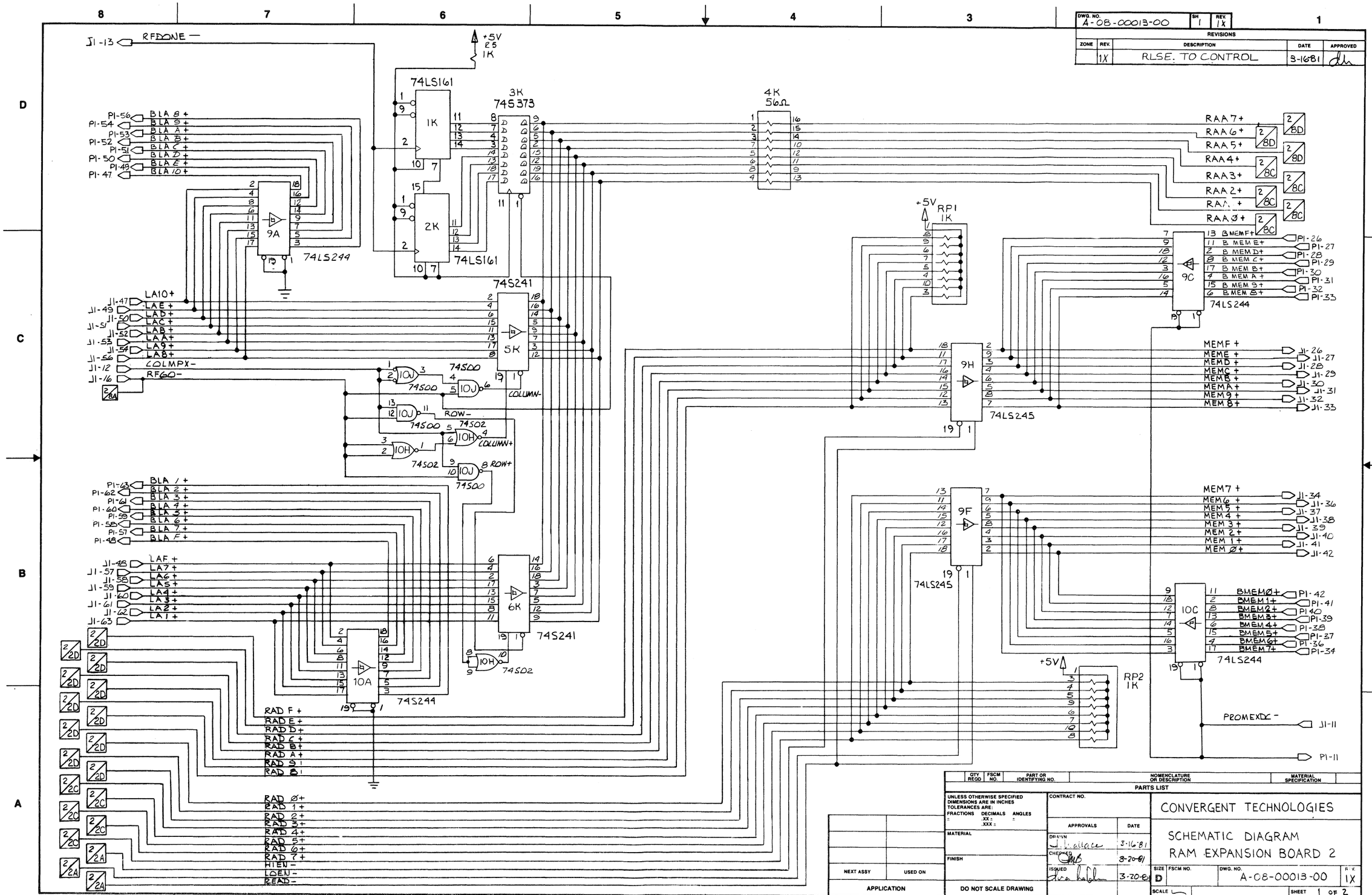

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Figure 6-3 64K RAM Expansion Board 2 Schematic
(Page 1 of 2)

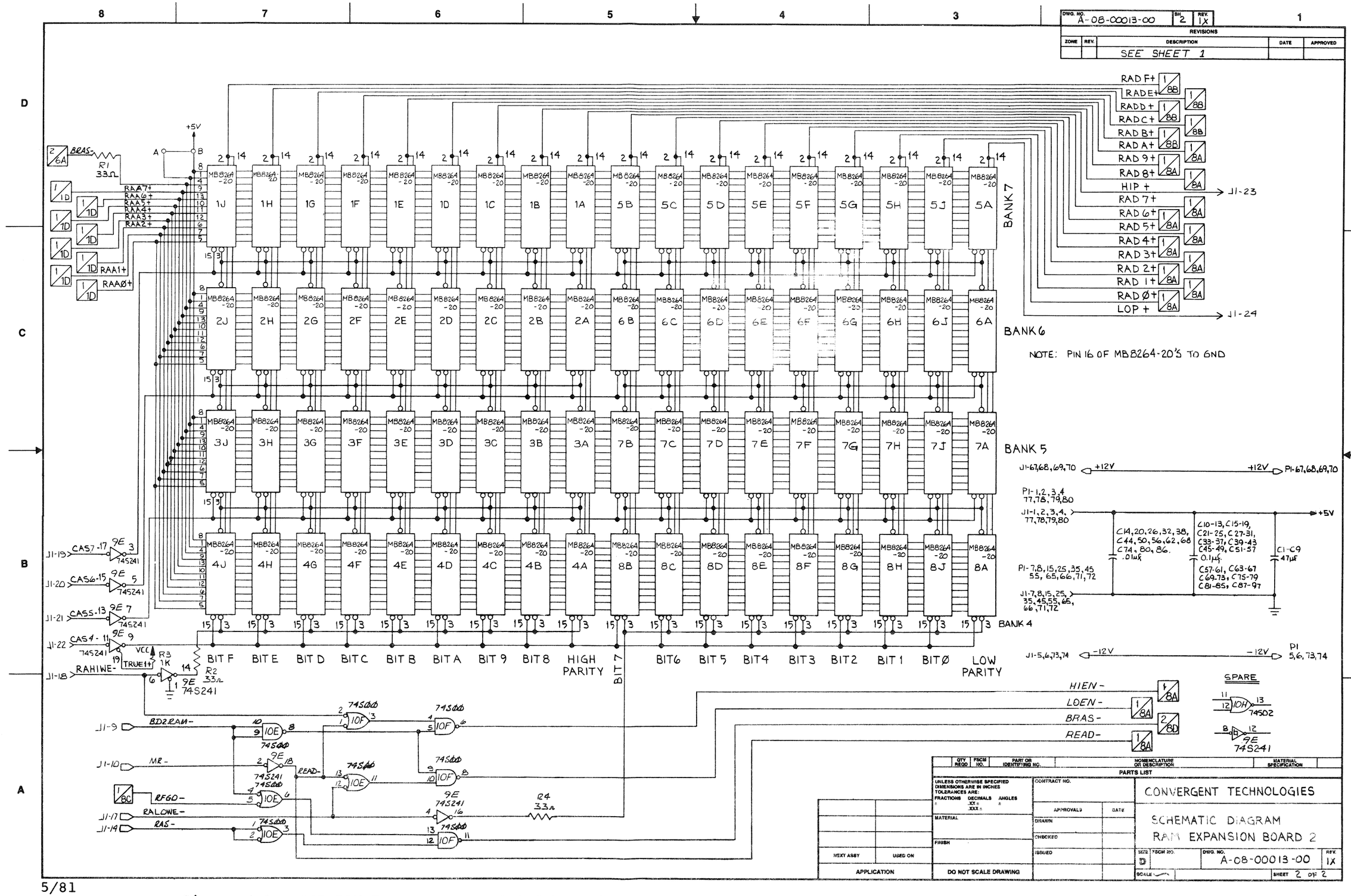

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Figure 6-3 64K RAM Expansion Board 2 Schematic
(Page 2 of 2)

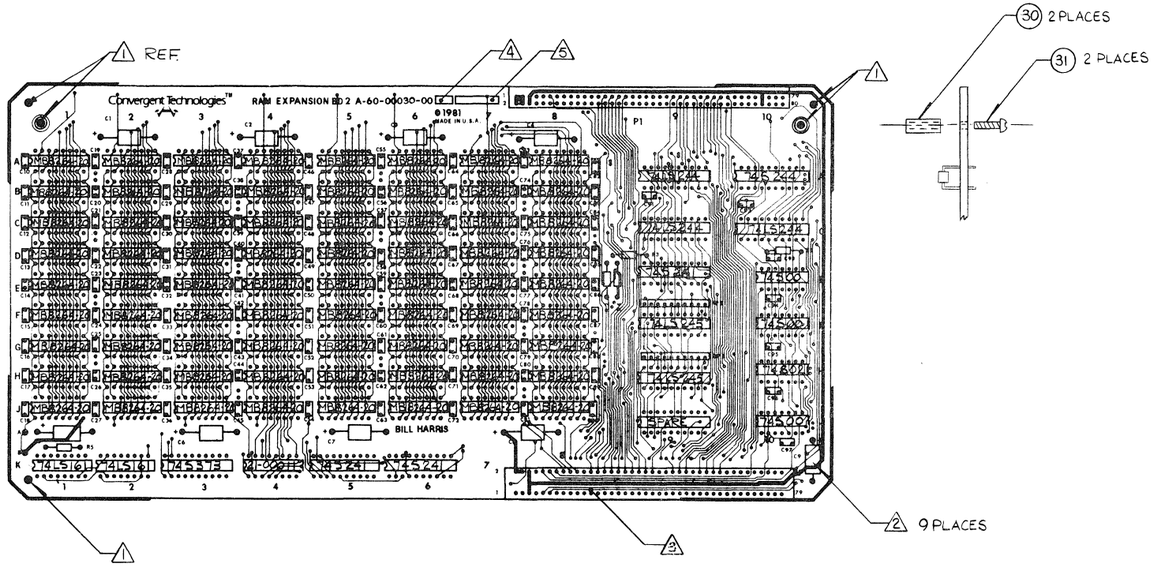
DWG. NO.	SH	REV.
A-43-00030-00	1	1X

REVISIONS

ZONE	REV.	DESCRIPTION	DATE	APPROVED
	1X	RLSE. TO CONTROL	3-18-81	

NOTES:

1. MASK AREA INDICATED PRIOR TO LOADING.
2. CONFIRM ORIENTATION.
3. USE OF SUPPORT FIXTURE REQUIRED DURING WAVE SOLDERING.
4. MARK ENGINEERING REVISION LEVEL FOR THIS ASSEMBLY
5. MARK APPROPRIATE DATE CODE TO SHOW DATE OF MANUFACTURE
6. FOR COMPLETE LIST OF MATERIALS SEE A-60-00030-01,02,03,04
7. SCHEMATIC REF. 08-00013-00



NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
	PARTS LIST	

CONTRACT NO.	CONVERGENT TECHNOLOGIES
APPROVALS / DATE	PRINTED CIRCUIT ASSEMBLY RAM EXPANSION BOARD 2
DRAWN J. Wallace 3-18-81	
CHECKED JMB 3/19/81	
ISSUED 3-20-81	SIZE D · FSCM NO. · DWG. NO. A-60-00030-00 · REV. 1X
	SCALE 1:1 · SHEET 1 OF 1

5/81

Figure 6-4 64K RAM Expansion Board 2 Assembly Drawing

13. COMMUNICATIONS I/O PROCESSOR BOARD

FUNCTIONAL DESCRIPTION AND SOFTWARE INTERFACES

The Communications I/O Processor (CommIOP) Board, an intelligent processor-based Multibus controller, expands the cluster communications capabilities of the master workstation. Each board can control two RS-422 ADCCP multidrop cluster communications lines. Much of the lower-level functions, such as polling and frame validation, are performed by local software that is down-line loaded from system memory via the Multibus. Interprocessor communication and buffer transfer between the main 8086 processor and the CommIOP is also provided by the Multibus.

Controller Processor

The CommIOP has its own Intel 8085A CPU that can execute program store out of local ROM or RAM. After a power-up or reset, the CPU goes to ROM and executes an initialization self-test followed by a bootstrap routine that down-line loads the CommIOP software from system memory to local RAM via the Multibus. Program execution then continues from local RAM.

Local Memory Space

The local memory address space is 16 bits wide or 64K bytes large. It is partitioned as shown in Figure 13-1 below.

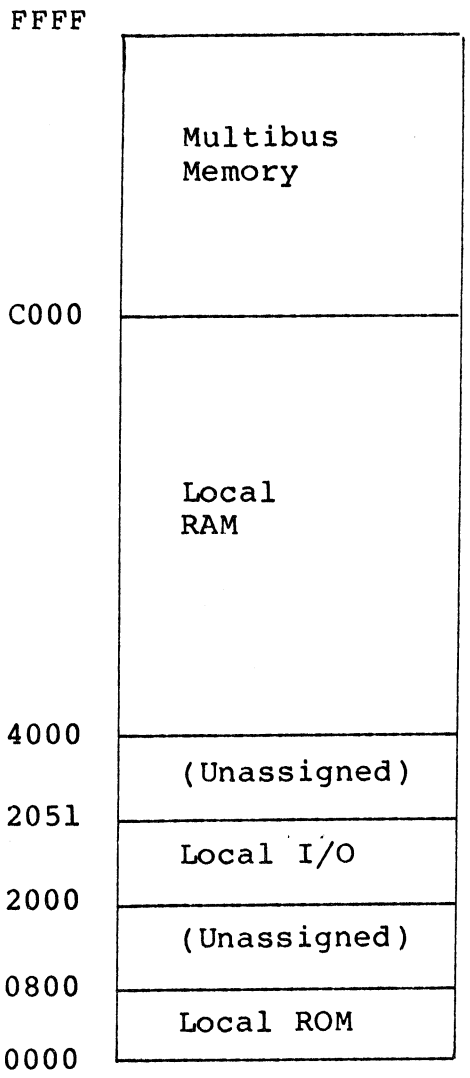


Figure 13-1. Local Memory Space

2K bytes of local ROM is addressed by hexadecimal address locations 0000 through 07FF. All local I/O is memory-mapped, starting at location 2000 and extending to 2050. Local dynamic RAM may be 16K bytes or 32K bytes large starting at 4000 and extending to 7FFF or BFFF respectively. Multibus memory is accessed through the local 16K byte window from C000 to FFFF.

Multibus Master

The CommIOP accesses main memory by becoming a Multibus master. This Multibus memory read or write occurs under local processor control. When the 8085A addresses the 16K byte memory space between C000 and FFFF, a 20-bit Multibus memory address is constructed in the following fashion: the 14 least significant bits are the least significant local address bits and the six most significant bits come from the Multibus Extended Address Register, a local on-board Read/Write register. This allows all one megabyte of Multibus memory to be accessed in 16K byte continuous segments as shown in Figure 13-2 below.

Stacker/Destacker

Data is transferred across the Multibus in words, not bytes; a stacker/destacker is implemented to convert local bytes to Multibus words and vice versa. During an even address Multibus write, the least significant byte is latched in the stacker. During an odd write, the Multibus is acquired and the entire word is written to system memory. When an even address Multibus read occurs, the Multibus is gained. The most significant byte is latched in the destacker, and the least significant byte is read by the local 8085A. During an odd address Multibus read, the most significant byte that was stored in the destacker is read by the local CPU.

Multibus Interrupts

The CommIOP may interrupt the master workstation on one of four Multibus interrupt levels: 0, 2, 5, or 6. The interrupt is enabled by a bit on the local on-board Multibus Register and the interrupt level is switch-selectable as shown in Figure 13-3.

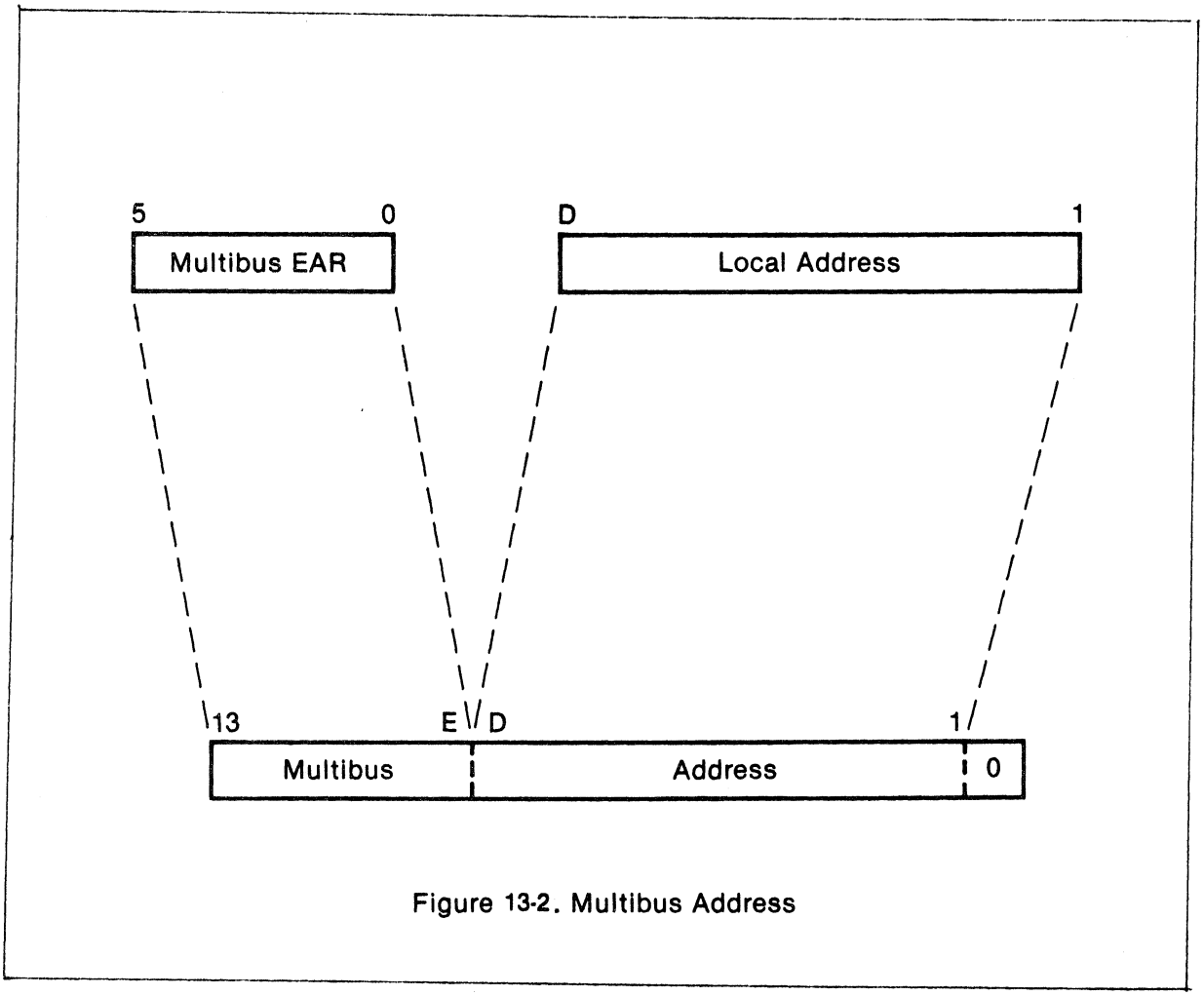


Figure 13-2. Multibus Address

Interrupt Level	Switch SW1 Bit 5	Bit 6	Bit 7	Bit 8
0	off	off	off	on
2	off	off	on	off
5	off	on	off	off
6	on	off	off	off

Figure 13-3. Multibus Interrupt Level Selection

The master workstation CPU can interrupt the CommIOP by issuing one of four Multibus output instructions whose port addresses are switch-selectable as shown in Figure 13-4 below. This allows for four CommIOPs to be installed in one workstation.

Line Interface

The CommIOP supports two independent synchronous ADCCP RS-422 multidrop cluster communications lines with one dual channel Zilog Z80A-SIO/2 USART. Each line baud rate is independent and software programmable from 18.75 bits per second to 614.4K bits per second implemented with an Intel 8253 Programmable Interval Timer. Each line can also be clocked externally; this feature is switch-selectable as shown in Figure 13-5 below.

Local DMA

Data is transferred between local RAM and each communications line via Direct Memory Access (DMA) because of the high baud rate. An Intel 8257-5 DMA controller is used for this. Two of the four DMA channels are used, one for each line.

Output Port	Switch SW1 Bit 1	Bit 2	Bit 3	Bit 4
XX40H	on	off	off	on
XX41H	off	on	off	on
XX50H	on	off	on	off
XX51H	off	on	on	off

Figure 13-4. Multibus Controller Port Selection

Channel A	Channel B	Switch SW2 Bit 1	Bit 2	Bit 3	Bit 4
Internal	Internal	off	on	on	off
Internal	External	on	off	on	off
External	Internal	off	on	off	on
External	External	on	off	off	on

Figure 13-5. Baud Rate Clock Selection

OPERATION BY LOGIC BLOCK

This section describes the hardware architecture of the CommIOP on a detailed level. A block diagram of the board is shown in Figure 13-6.

The 8085A CPU

The processor-related logic is primarily on page one of the schematic. Chip 3D (plzB7) is the 8085A itself. Pins 1 and 2 are connected to a 6.144 MHz crystal. This is twice the frequency of the internal processor clock, which is 3.072 MHz. The processor clock is output on 3D-37 and buffered by 4E-18 and 13E-18, providing both phases of the clock, PCLK+ and PCLK- respectively.

Reset on the CPU (3D-36) can be generated by two sources: a Multibus initialization (2E-10) or grounding test point 2 (2E-9). The 8085A produces a reset out signal on pin 3 which is inverted (5E-4) and used as a low-true board reset (RESET-).

The serial input data line (3D-5) is connected to a test point (TP1). This input is read after a reset by the bootstrap PROM. If this line is grounded, the CommIOP enters a diagnostic mode, continuously reading and writing to all of the master workstation's main memory. If TP1 is not grounded, the CommIOP software is down-line loaded from the master workstation and executed.

The serial output data line (3D-4) is used to flash a diagnostic indicator, CR2, which is driven by 13E-6. The state of this indicator is under program control and is used to flash various error codes during the initialization self-test.

Address generation is performed in the following fashion. The most significant byte of the 16-bit address comes directly from the 8085A (3D pins 21-28). This byte is then buffered by 7C (plzD3). The least significant byte is multiplexed on the data bus lines (3D pins 12-19). The lower address byte is selected when the address latch enable signal (ALE+) is high, and latched by 8D (plzB7) when ALE+ goes low. This byte is buffered by 8C (plzC3). The 16-bit local address bus has the mnemonics LAB0-LABF+.

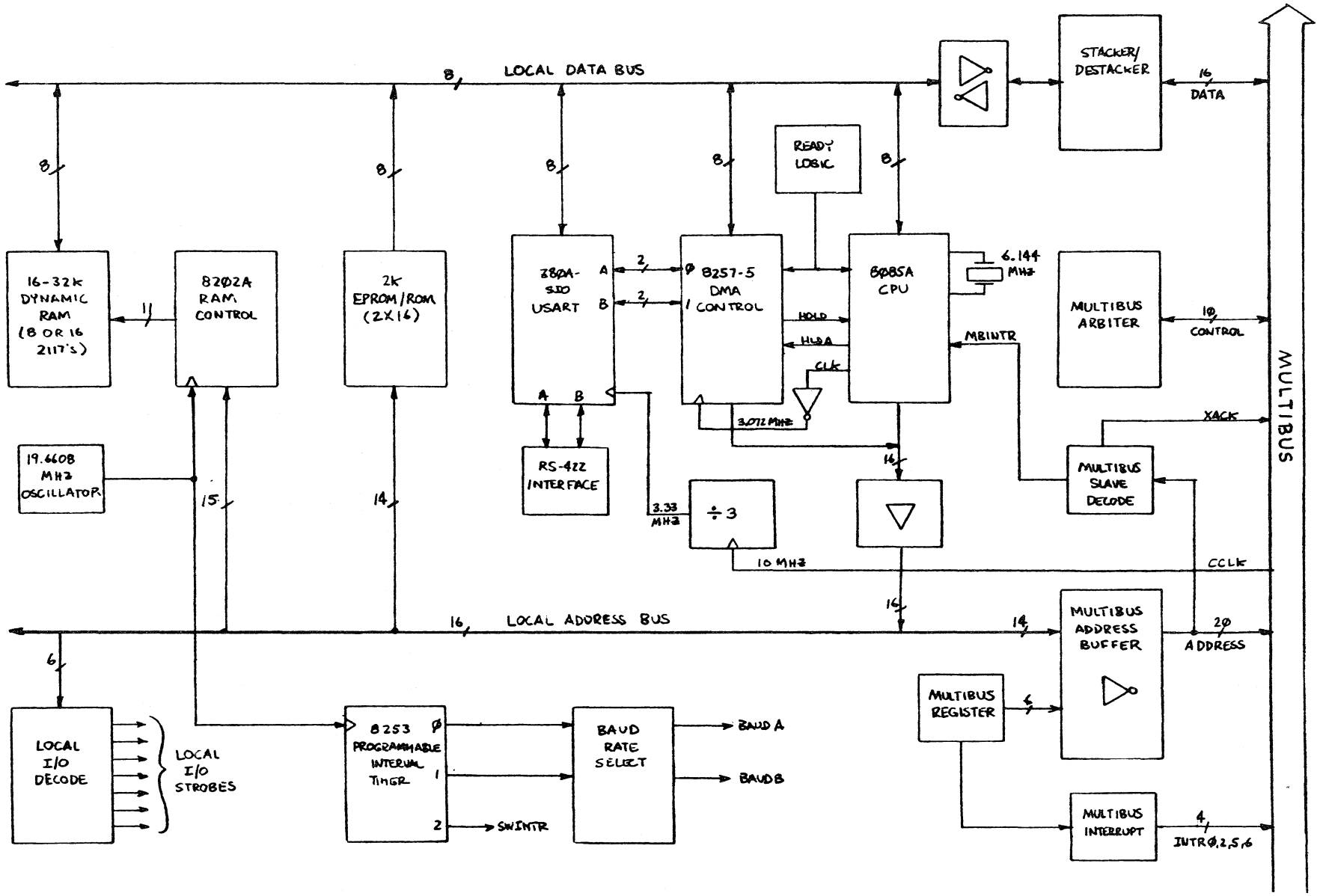


Figure 13-6. Communications I/O Processor Block Diagram

The local data bus (LDB0+ - LDB7+) is bidirectional, unbuffered, and is simply connected to the multiplexed address and data lines of the 8085A (3D pins 12-19).

The control signals, RD- (3D-32) and WR- (3D-31), are buffered by 4E-16 (p1zA5) and 4E-14 (p1zC5), respectively. Status signals S1+ (3D-33) and IO+ (3D-34) are used for decoding as described below.

The DMA handshaking signals, CPUHOLD+ (3D-39) and CPUHLDA+ (3D-38) are used in conjunction with the 8257-5 DMA controller chip. These are described below in the subsection on "Direct Memory Access."

The 8085A can be interrupted on the three maskable restart lines (RST5.5, RST6.5, RST7.5) by the software timer, the SIO USART, or the master workstation CPU via a Multibus interrupt. The details of these interrupts are listed below.

Interrupt	Priority	Source	Type Trigger
RST 7.5	1	Multibus	Rising Edge (Latched)
RST 6.5	2	SIO USART	High Level
RST 5.5	3	Software Timer	High Level

The nonmaskable trap and vectored interrupts are not used. These inputs (3D-6 and 3D-10) are grounded.

The CPURDY+ line (3D-35) determines the number of wait states to be inserted for each machine cycle. The ready logic generates this signal and is detailed in the subsection of that name below.

Local I/O

All local I/O on the CommIOP is memory-mapped. That is, memory-reference 8085A instructions perform input and output. Address decoding is performed by the decoder, 14C (p1zC3). The OR gate at 14D-3 (p1zC3) disables I/O strobe generation during DMA cycles, when CPUHLDA+ is active. The I/O selections strobes and their memory addresses, directions, and functions are listed below.

Strobe	Address	Read/Write	Function
SIOCS-	2000-2003	Read/Write	Selects SIO Chip
DMACS-	2010-2018	Read/Write	Selects DMA Chip
MBREGS-	2020	Read/Write	Selects Multibus Register
TIMERS-	2030-2036	Read/Write	Selects Timer Chip
SIOINTRCLR-	2050	Write	Clears SIO Interrupt

Direct Memory Access

Direct Memory Access (DMA) transfers data at high speed between the SIO USART chip and local RAM. An Intel 8257-5 DMA controller chip (9D) is used for this. This chip has four channels, two of which are used by the SIO. Channel 0 on the 8257-5 corresponds to Channel A on the SIO and Channel 1 to Channel B.

The DMA chip can be a local bus master or slave. The DMA chip acts as a slave when it is programmed as a standard peripheral device. The 8085A CPU generates chip select (9D-11) via local address decoding and reads or writes data from its internal registers. The addressing of these internal registers and their direction is outlined below.

Address	DMA Register	Read/Write
2010	Channel 0 Address	Read/Write
2011	Channel 0 Terminal Count	Read/Write
2012	Channel 1 Address	Read/Write
2013	Channel 1 Terminal Count	Read/Write
2018	Mode Register	Write
2018	Status Register	Read

The DMA chip is a local bus master when the DMA cycle is in progress. At this time, the 8085A CPU floats its address, data and control lines, and the DMA chip drives the address and control lines. The data bus is driven either by the RAM buffer or by the SIO depending on the direction of the transfer.

DMA transfers are initiated by the 8085A CPU enabling a specific channel and by the SIO generating a DMA request for that channel. Each DMA request from the SIO (SIORQ0- and SIORQ1-) is latched in a flip-flop, 15D-7 (p1zD5) for Channel 0 and 15D-6 (p1zD4) for Channel 1. This is done to prevent unstable request signals, because the SIO deasserts its requests during any chip select. Each DMA request is set by the request line from the SIO and cleared by the appropriate DMA acknowledge signal (DACK0- and DACK1-) or by a board reset (RESET-).

Once a DMA request line is asserted and that channel is enabled, the DMA chip generates a hold request signal, HRQ+ (9D-10). This produces the CPU hold request signal (CPUHOLD+, 3D-39). Next, the DMA chip waits for a hold acknowledge signal (9D-7) from the CPU, which means that the CPU has floated the local bus. When this occurs, priorities are internally resolved as to which of the four channels are to be serviced and the appropriate 16-bit local DMA address is presented. The least significant address byte (A0+ - A7+) comes directly from the DMA chip and is buffered by 8C (p1zC3). The most significant address byte is multiplexed on the data bus lines, latched on the falling edge of ADRSTB+ (9D-8) by the latch, 7D (p1zB4), and buffered by 7C (p1zD3). When the DMA chip controls the local address bus, it asserts its address enable signal, AEN+ (9D-9), which disables the CPU address latch, 8D, and its inversion, AEN- (13D-12), and enables the DMA address latch, 7D. The DMA acknowledge signal for the channel being serviced is also generated at this time; it chip selects the SIO.

Next, the appropriate set of control signals is generated. Since all local I/O is memory-mapped, the I/O read and write signals from the 8257-5 (9D-1 and 9D-2) are connected to the local memory read and write signals and the memory read and write signals from the 8257-5 (9D-3 and 9D-4) become the I/O read and write signals to the SIO chip. During a DMA write cycle, data is transferred from the SIO and written into RAM; WR- and IOR- are asserted. During a DMA read cycle, data is read from memory and output to the SIO; RD- and IOW- are generated.

The DMA memory cycle lasts until its ready is generated (9D-6). The DMA logic is explained in the "Ready Logic" subsection below. When the DMA

cycle ends, the DMA chip deasserts its control signals, its acknowledge signal to the SIO, its hold request signal, and its address enable signal, and floats the control and address bus.

DMA Interchange Logic

Because the Z80A-SIOA is a synchronous device and the local bus is asynchronous, certain sequences of events must be avoided for proper SIO operation. Specifically, SIO cycles cannot occur too close to each other. This is only a problem when CPU and DMA SIO cycles are consecutive. To avoid this, several flip-flops (17C, p1zD7 and 16D, and p1zD6) delay the interchange between CPU SIO and DMA SIO cycles.

Flip-flops 17C-15, 17C-7, and 17C-10 extend the hold request signal from the DMA chip (9D-10) for three processor clock periods (978 nanoseconds) to produce CPUHOLD+ (3D-39). This adds dead time between the end of a DMA SIO cycle and a possible successive CPU SIO cycle.

Flip-flops 17C-2 and 16D-9 delay the hold acknowledge signal from the CPU (3D-38) to the DMA chip (9D-7). This adds dead time between the end of a CPU SIO cycle and the beginning of a possible successive DMA SIO cycle.

Dynamic RAM

The RAM array consists of 32K bytes of 250 nanosecond 16K bit dynamic RAM chips. The lower 16K bytes (address range 4000-7FFF) are at locations 1A-8A (p2zD3); the upper 16K bytes (address range 8000-BFFF) consist of eight RAM chips at 1B-8B (p2zC3).

The RAM chips require three power voltages. Pin 8 is connected to +12v (Vdd). Bypass is provided by the two 47 microfarad capacitors (C10 and C16). Decoupling consists of eight 0.1 microfarad capacitors. Pin 9 is connected to +5v (Vcc). Decoupling is provided by eight 0.01 microfarad capacitors. Pin 1 is -5v (Vbb), which is derived from the 330 ohm resistor (R14) and the 5.1v zener diode (CR1). Bypass and decoupling are similar to that of the +12v supply.

The array has 33 ohm series terminators for all address, strobe, command and data-in lines to avoid transmission line reflections. The data-

out lines are pulled up to +5 volts with 3.3K ohm resistors (RP3).

All RAM control is performed by an Intel 8202A dynamic RAM controller chip (3C, p2zC6). All refreshing is internally generated and transparent to the CPU or DMA chip. Row and column addresses and their strobes (RAS- and CAS-) are generated with the proper timing by the 8202A as well.

Dynamic RAM Control

The 8202A initiates a memory cycle when it is chip selected (3C-33) and a read or write command (3C-32 or 3C-31) is asserted. The memory cycle corresponds to the location specified by the 15-bit address, LAB0+ - LABE+. When the memory cycle is complete, the 8202A returns two acknowledges (3C-30 and 3C-29), one of which generates a ready and a later one of which latches the data read from RAM.

Chip selection consists of simple address decoding. When the local address bus contains an address in the RAM range 4000-BFFF, MEMCY- (5E-2, p2zC6) is asserted and chip selects the 8202A.

A 19.6608 MHz oscillator (2C) is used by the 8202A for its internal timing. This clock (MEMCLK+) is connected to pin 37 on the 8202A. It is also used by flip-flops 2D-6 and 2D-8 to synchronize the read and write command input lines to the 8202A and to avoid possible metastable conditions inside the older 8202 non-"A" parts

The 8202A multiplexes 14 bits of local address into a 7-bit row address and a 7-bit column address. The row address consists of the seven least significant local address bits (LAB0+ - LAB6+) and the column address is the seven most significant bits (LAB7+ - LABD+). LABE+ (3C-24) selects which 16 kilobyte bank is accessed by selecting the appropriate row address strobe (RAS2- or RAS3-). A column address strobe (CAS-) is generated for all memory cycles. The write enable line (WE-) to the RAM is asserted only during a memory write cycle.

Dynamic RAM refresh is implemented entirely inside the 8202A. The internal refresh timer generates a refresh request approximately every 14 microseconds. During a refresh cycle, the

7-bit refresh row address is driven onto the RAM address lines and both row address strobes are pulsed, refreshing both 16K byte banks simultaneously. After the refresh cycle, the internal 7-bit refresh row address counter is incremented. All 128 rows are refreshed in approximately 1.8 milliseconds.

At the end of a memory read cycle, the memory transfer acknowledge signal, MEMACK- (3C-29), from the 8202A goes low to latch the valid data into the read data latch, 1C (p2zB5). This read data is enabled onto the local data bus when MEMCY- and RD- are both low.

ROM/EPROM

Local read-only memory bootstrap capability is provided by a 2316 ROM or 2716 EPROM at location 9C (p2zA6). These are 2K x 8-bit devices that require 11 bits of addressing (LAB0+ - LABA+). The chip is enabled (9C-18) when LABD+ - LABF+ are all low, specifying the address range, 0000-1FFF. The outputs are driven onto the local data bus when RD- (9C-20) is asserted.

Ready Logic

This logic provides the ready signals to the 8085A CPU and the 8257-5 DMA chip. During a machine or DMA cycle, the ready line is driven low to indicate that wait states must by added to the cycle. When the ready line goes high, wait states are not added and the cycle terminates.

The CPU ready signal, CPURDY+ (20E-2, p3zD3) consists of three terms: Multibus Ready (MBRDY+), CPU Memory Cycle Ready (CPUMEMRDY+), and Wait State Ready (WSRDY+). Since all three terms must be true for the CPU to become ready, the two unused ready sources are forced true by the ready logic. The three ready sources and their corresponding machine cycles are listed below.

Ready Signal	Address Range	Machine Cycle
WSRDY+	0000-3FFFF	Local I/O, including ROM
CPUMEMRDY+	4000-BFFF	Local RAM
MBRDY+	C000-FFFF	Multibus Memory

If no Multibus cycle is in progress, MBREQL+ (18C-13) is low, forcing MBRDY+ high. If a Multibus cycle is initiated, and the COMMIOP becomes a master, the Multibus command enable signal (CMDEN-, 15C-4), is asserted. MBRDY+ is held false until the slave returns a Multibus transfer acknowledge (XACK-, 15C-5).

CPU memory cycle ready (CPUMEMRDY+) is held true when no memory cycle is in progress because MEMCY+ (18C-2) is low. During a memory cycle, CPUMEMRDY+ is simply the inversion of the system acknowledge signal, SACK- (18C-1), from the 8202A RAM controller.

The wait state ready logic uses a 4-bit shift register (17E, p3zC6) to clock out a specific number of wait states during local I/O and ROM/EPROM cycles (four wait states for writes and two for reads.) This same logic also generates wait states for the SIO during DMA transfers. WSRDY+ is held true by clearing the shift register (17E-1). This occurs during CPU memory cycles when MEMCY- (15E-2) is true and CPUHLDA+ (15E-3) is true.

At the beginning of a CPU I/O cycle, ALE+ (15E-8) loads all 1's into the shift register. During an I/O read cycle, 16C-13 is high, and two processor clock cycles later 17E-14 goes low, causing WSRDY+ to be asserted. For an I/O write cycle, 17E-11 goes high four processor clocks after ALE+ occurs, causing four wait states to be generated.

The DMA ready signal, DMARDY+ (17D-6), consists of two terms: DMA memory cycle ready (DMAMEMRDY+) and wait state ready (WSRDY+). During a DMA cycle, both the memory and the SIO peripheral must become ready to complete the cycle. WSRDY+ is generated as explained above, except that ADRSTB+ (13D-5, p3zC7) from the DMA chip is delayed by one PCLK+ and initializes the wait state shift register. DMAMEMRDY+ (16D-6, p3zD4) is the system acknowledge ready (SACK-) signal from the 8202A synchronized to PCLK+ by flip-flop 16D-6.

Control Signal Logic

This miscellaneous logic at the bottom of page 3 of the schematic generates various read and write control signals. Multiplexer 15B (p3zB3) selects various control signals, depending on whether a DMA cycle is in progress (15B-1 is low). During

a CPU memory write cycle, MEMWR- (15B-9), is simply WR-; during a DMA write cycle, WR- is delayed by flip-flops 14B-8 and 14B-6 to produce MEMWR- to provide ample SIO access time. During a CPU SIO write cycle, SIOWR- (15B-12) is generated from WR-; during a DMA write cycle, SIOWR- does not occur until RAM data is valid, that is, when MEMACK- (15E-5, p3zB4) is asserted.

Multibus Stacker/Destacker

The stacker/destacker is shown at the bottom of page 4 of the schematic and consists of octal flip-flops 9E and 12E, buffers 10E and 11E, and related control logic. The Multibus data bus (DATA0+ - DATAF-) is low-true and 16 bits wide. The stacker/destacker converts this to a low-true 8-bit wide data bus (MDB0- - MDB7-). This is then inverted by the octal bidirectional inverting transceiver (11C, p4zC6) and connected to the local data bus (LDB0+ - LDB7+).

A 3-to-8 decoder (18E, p4zB7) and an octal latch (14E, p4zB6) generate the control signals for the stacker/destacker. The two most significant local address lines (LABE+ - LABF+) enable the decoder, and the least significant address line (LAB0+) and the S1+ status line from the CPU select the parity and direction of the transfer. The octal latch (14E) is clocked by NEWCY+, which occurs at the beginning of every CPU and DMA cycle.

During even Multibus reads (RDEVEN-), the least significant byte is read via buffer, 11E, and the most significant byte is stored in the octal latch, 9E. During odd Multibus reads, (RDODD-), the byte stored in 9E is read by the CPU. The CPU stores the least significant byte in the octal flip-flop stacker, 12E, during even writes (WREVEN-). During odd writes (WRODD-), both bytes (12E and 10E) are enabled onto the Multibus. A Multibus request (MBREQ+) is generated only for odd writes or even reads.

The bidirectional transceiver, 11C, is enabled during any Multibus stacker/destacker access (MBACS- is low), the direction being determined by the RD- signal.

Multibus Register

The Multibus register is an 8-bit flip-flop (13C, p4zD5) written to when MBREG5- and WR- are asserted. This register contains the six most significant Multibus address bits (MBREG0- MBREG5+) and a Multibus interrupt bit (MBREG6+). The entire register is read by enabling the buffer, 12C (p4zC5), onto the local data bus.

Multibus Address Drivers

Inverting tristate drivers, 8E, 7E, and 13E (p4zC3 and p4zD3) are enabled when theCOMMIOPbecomes Multibus master (MBMASTER-), driving 19 Multibus address lines, (ADRl- - ADRl3-) and the byte high enable line (BHEN-).

Multibus Interrupts

The Multibus register bit 6 (MBREG6+) can be programmed to generate a Multibus interrupt on levels 0, 2, 5, or 6. The enabling of interrupt levels is switch-selectable by switch SWl (p4zD3).

Local Multibus interrupts are generated by selectively decoding the eight least significant Multibus address lines (ADR0- - ADR7-) during an output command (IOWC-). This is done by the inverters, gates, and switches at p4zB2 and p4zC2. Output commands to a port in the range XX40-XX41 or XX50-XX51 cause a local interrupt. Open-collector NAND gate 19E-3 returns a transfer acknowledge signal (XACK-) to the master to terminate the output command.

Multibus Master Control

This logic is located at the top of page 5 of the schematic. It controls the acquisition of the Multibus. Flip-flop 19D-9 (p5zD6) latches the Multibus request signal for every new cycle. MBREQL+ is then synchronized to the 10 MHz Multibus clock, BCLK+, by flip-flop 20D-3, producing BREQ+ and BREQ-. BREQ- is a Multibus signal that initiates the Multibus request to the arbitration logic. The CommIOP may become Multibus master when the bus priority in signal (BPRN-) is asserted by the arbitration logic and the Multibus busy signal (BUSY-) is not asserted by any masters. NAND gate 18D-6 (p5zC5) goes

low, causing flip-flop 20B-5 to be reset on the next positive BCLK+ edge. This generates MBMASTER-, which is the address and data enable signal. The open-collector NAND gate, 19E-6, also drives BUSY- low, indicating to all other masters that the COMMIOP has acquired the Multibus. One BCLK+ later (100 nanonseconds), 20D-10 goes high generating CMDEN+ (4E-19); this drives the local command lines onto the Multibus command lines.

When the slave receives the Multibus command, it returns a transfer acknowledge signal (XACK-) to the CommIOP. This generates a ready to the 8085A CPU, which causes the local CPU cycle to terminate. When this occurs, the control line goes inactive and 20D-15 (p5zC6) goes low, causing the command to be removed from the Multibus (CMDEN+ is low). One BCLK+ later, flip-flop 20B-5 is set, disabling the address and data drivers (MBMASTER- is high).

The Multibus master control logic also generates the optional common bus request signal (CBRQ-). This signal (p5zD3) is asserted when the CommIOP has requested the Multibus (BREQ+ is high) but has not acquired it (MBMASTER- is high).

SIO Clock Generation

Flip-flops 19D-5 (p5zB4) and 19C-5 (p5zB3) divide the 10 MHz constant clock (CCLK-) from the Multibus by 3, producing a square 3.3 MHz SIO system clock (SIOCLK+). This clock is pulled up with a 300 ohm register to provide the fast rise time required by the SIO.

SIO USART

The Z80A-SIO/2 USART is used as an I/O slave peripheral as well as a DMA bus master. This chip is selected (10A-35, p6zC6) either by the CPU (SIOCS-, 14A-9) or by the DMA acknowledge signals (DACK0- and DACK1-) from the DMA chip. When the SIO is a slave, the two least significant address lines (LAB0+ - LAB1+) select the channel and control or data registers via pins 34 and 35 respectively. During a DMA cycle, the DMA acknowledge signal (DACK0- or DACK1-) forces the selection of the data register (10A-33 is low) and the channel is selected by which acknowledge is active. The internal SIO register addressing is outlined below.

CPU/DMA Cycle	Address	SIO Register Set	Read/Write
CPU	2000	Channel A Data	Read/Write
CPU	2001	Channel A Control	Read/Write
CPU	2002	Channel B Data	Read/Write
CPU	2003	Channel B Control	Read/Write
DMA (DACK0-)	----	Channel A Data	Read/Write
DMA (DACK1-)	----	Channel B Data	Read/Write

The IORQ- line (10A-36) is asserted whenever an SIO read or write occurs (SIORD- or SIOWR-).

If a read occurs, the RD- line (10A-32) also goes low. A special case exists to simulate a Z80A interrupt acknowledge to clear an SIO interrupt; both the IORQ- line and the M1- line (10A-8) must be asserted. This is generated by an output strobe (SIOINTRCLR-) from the CPU.

The transmit clocks for both channels connect to the line interface and may come from the 8253 Programmable Interval Timer or from the external receive clock lines, depending on the setting of switch SW2. The receive clocks and transmit and receive data lines connect to the line interface.

The Clear To Send (CTS-) lines are SIO outputs and enable the line transmitters. The Data Carrier Detect (DCD-) lines are SIO inputs driven by the clock detection logic. When a receive clock is detected on a line, DCD- is asserted; this enables that channel's receiver.

Programmable Interval Timer

An 8253 Programmable Interval Timer (10B, p6zB6) generates transmit clocks for both SIO channels and also provides a software timer interrupt. The timer is selected by TIMERS- (10B-21). Three 16-bit internal counters are selected by address lines LAB1+ and LAB2+, allowing for 16-bit accesses from the CPU. The addressing for the 8253 is detailed below.

Address	Timer Register	Read/Write
2030-2031	Counter 0	Read/Write
2032-2033	Counter 1	Read/Write
2034-2035	Counter 2	Read/Write
2036	Control Word	Write

Counter 0 provides the transmit clock for SIO Channel A, counter 1 generates the transmit clock

for Channel B, and counter 2 is a programmable software timer interrupt (SWINTR+).

The clock inputs for all three 8253 counters consist of a 1.23 MHz square wave (1E-11, p6z7A), which is the 19.6608 MHz MEMCLK+ divided by 16. The gate inputs are always enabled.

Clock Detection

This logic monitors both receive clock lines and generates Data Carrier Detect signals to the SIO if a clock is present. The quad flip-flop 19B (p6zB4) synchronizes both receive clocks to a 2.46 MHz clock (19B-9). This is four times the maximum baud rate (614.4 kilobits per second). If there are clock transitions, the exclusive-OR gate (17B) ouput goes low, clearing the respective counter (18A and 19A). The Data Carrier Detect signal goes low and enables the counter. The counter is continuously cleared by clock transitions until eight transmit clock periods have elapsed with no receive clock transitions. Data Carrier Detect then goes inactive and disables the counter.

Line Interface

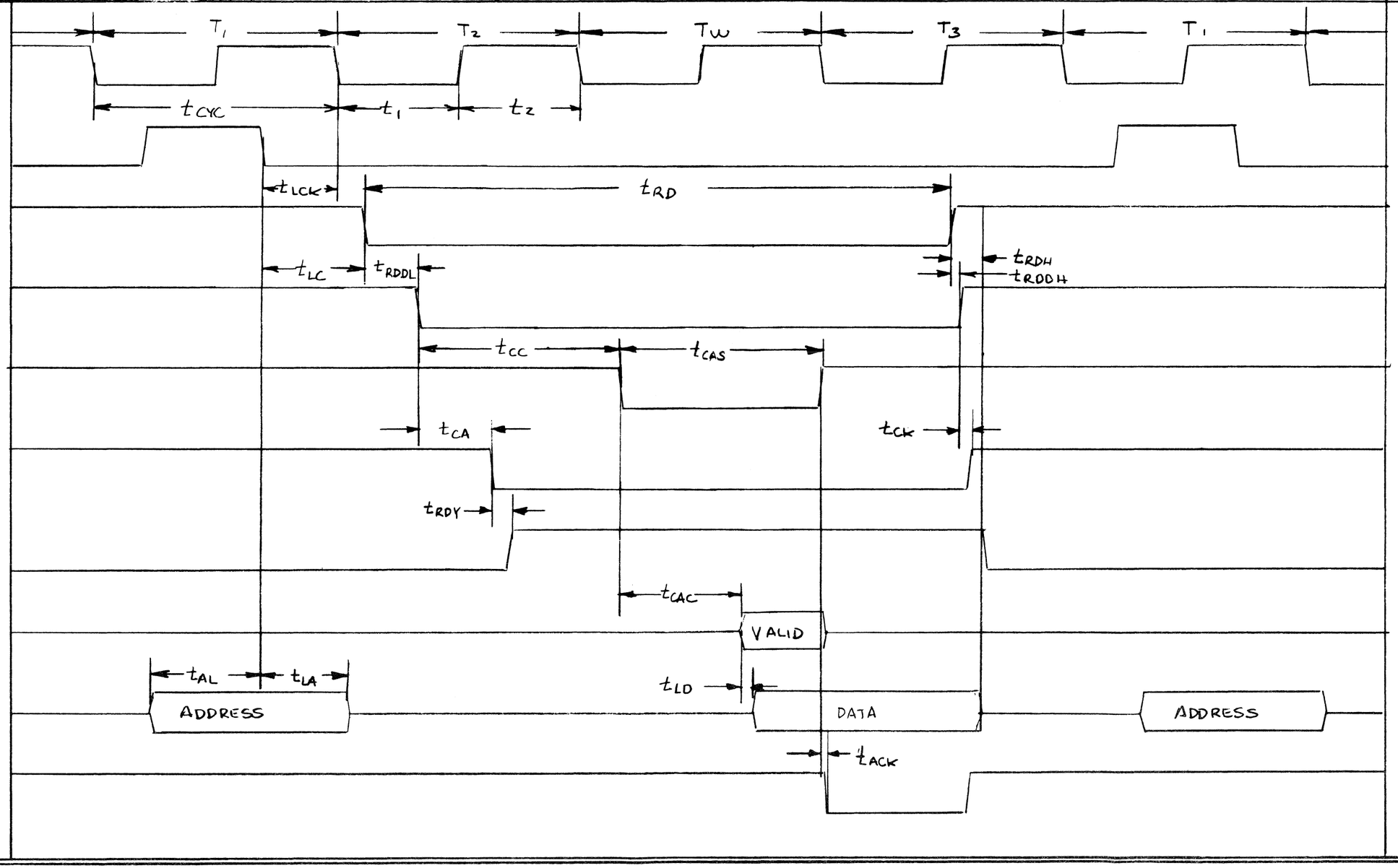
The line interface consists of two RS-422 transmitters (15A and 17A, p6zC3) and one RS-422 receiver (16A, p6zD3). Each transmitter drives the clock and data pairs for each line and is enabled by the Clear To Send signal from the respective SIO channel. The receiver is used for both channels of clock and data and is always enabled. 1K ohm series resistors provide termination for all received lines. Since the cluster communications line is half-duplex, the transmit and receive clocks and transmit and receive data RS-422 pairs are tied together on the CommIOP.

AC CHARACTERISTICS

Convergent Technologies™

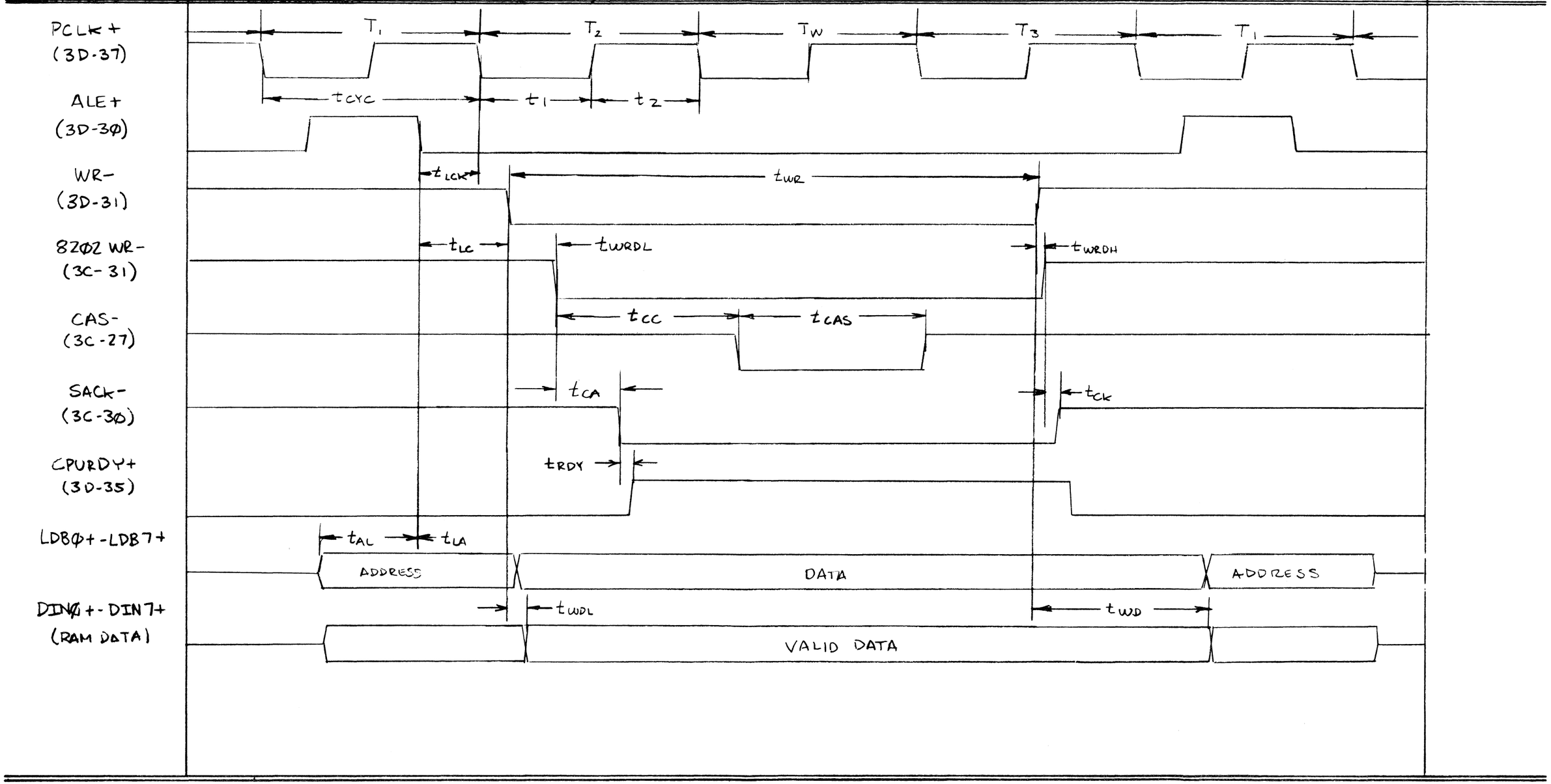
TITLE	APPROVALS	DATE	DWG NO
COMM CONTROLLER TIMING CPU MEMORY READ CYCLE	DRAWN		
	CHECKED		
APPLICATION			SHEET / REV
NEXT ASSY / USED ON	ENG		

SIGNAL	ASSUMPTION: NO REFRESH PENDING; 1 WAIT STATE	CONDITION



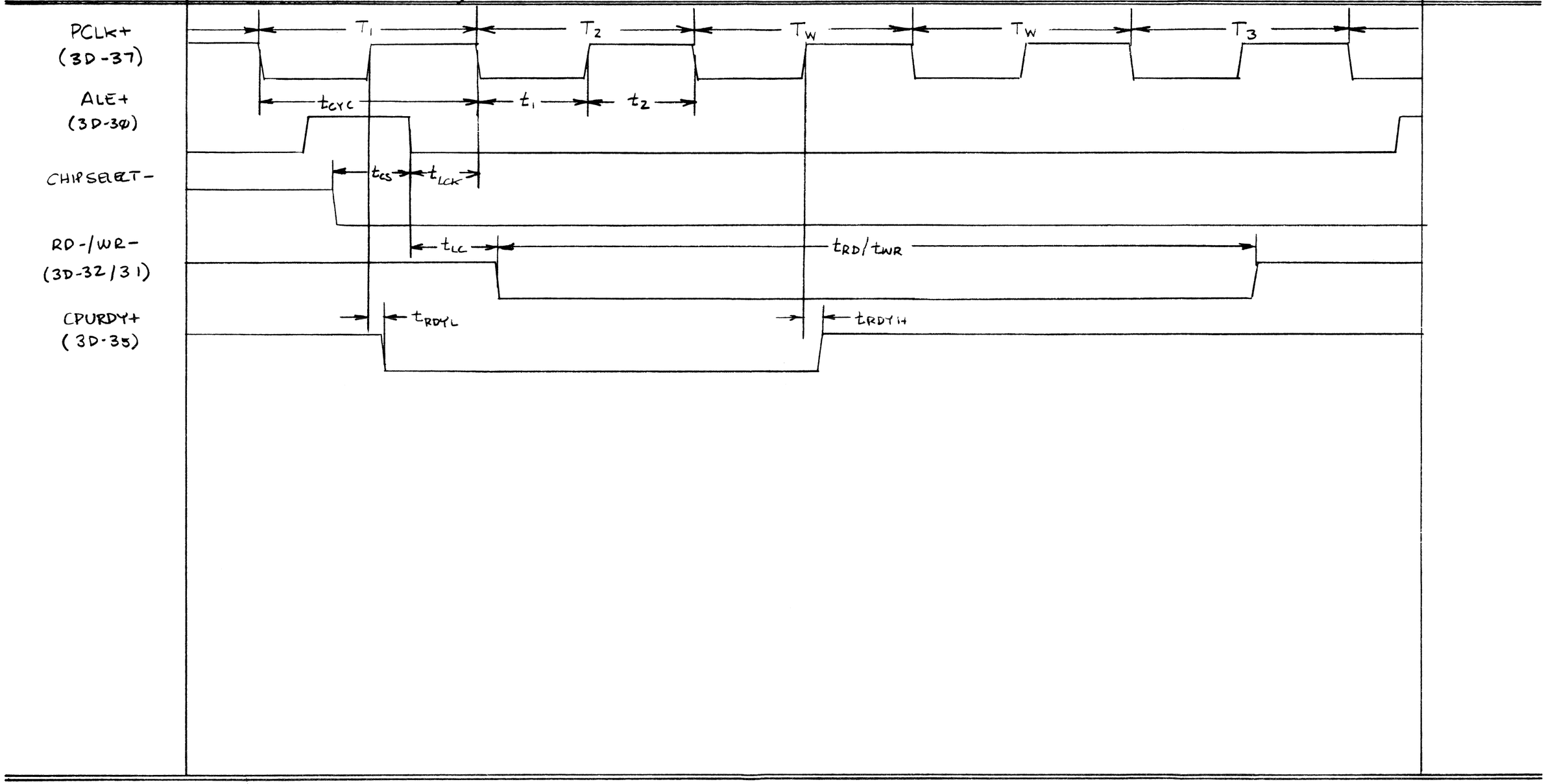
Convergent Technologies™

TITLE	APPROVALS	DATE	DWG NO
COMM CONTROLLER TIMING CPU MEMORY WRITE CYCLE	DRAWN		
	CHECKED		
APPLICATION			SHEET / REV
NEXT ASSY / USED ON	ENG		



Convergent Technologies™

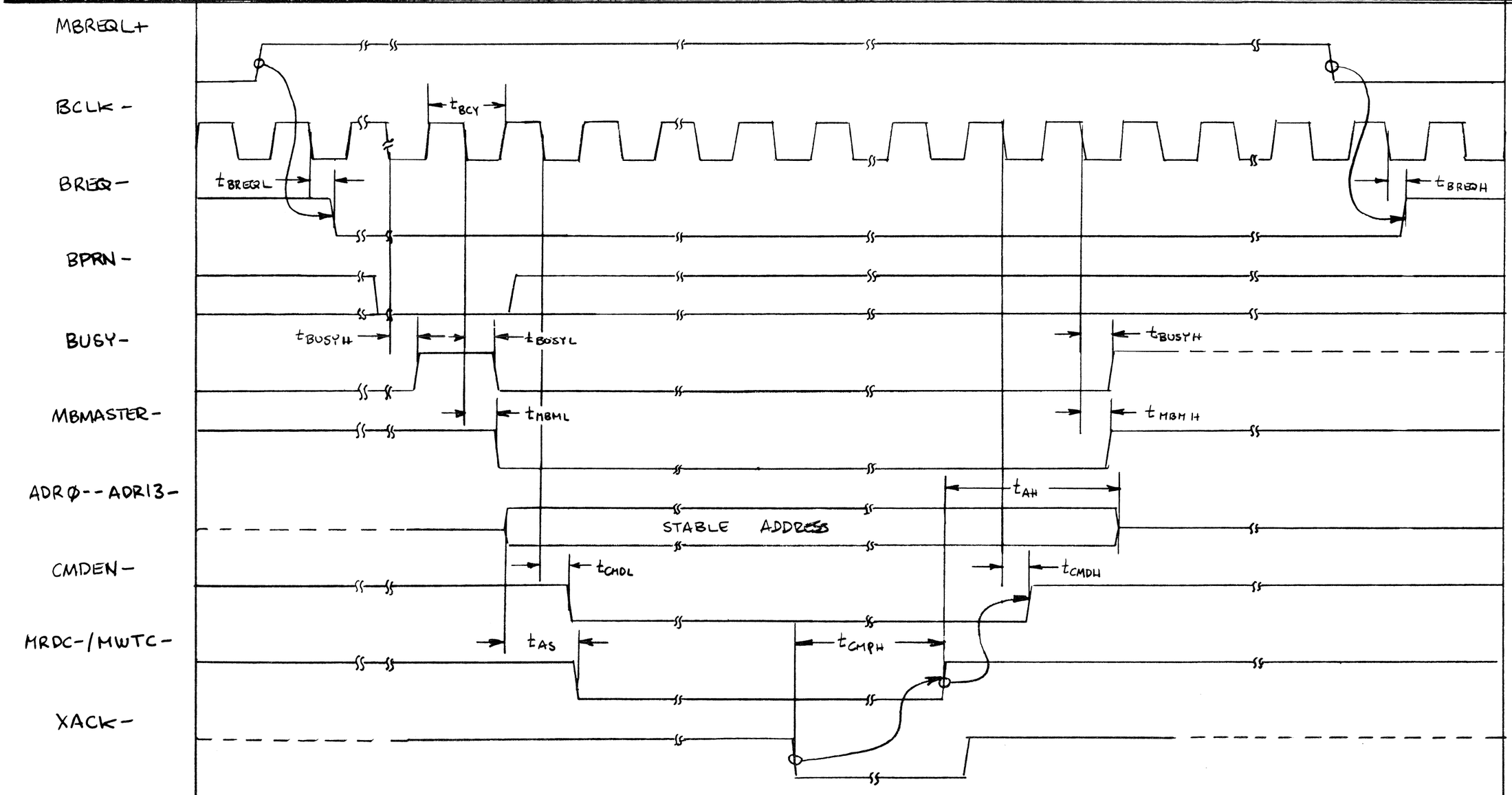
TITLE	APPROVALS	DATE	DWG NO
COMM CONTROLLER TIMING CPU IO/ROM CYCLE	DRAWN		
	CHECKED		
APPLICATION			SHEET / REV
NEXT ASSY / USED ON	ENG		



Convergent Technologies™

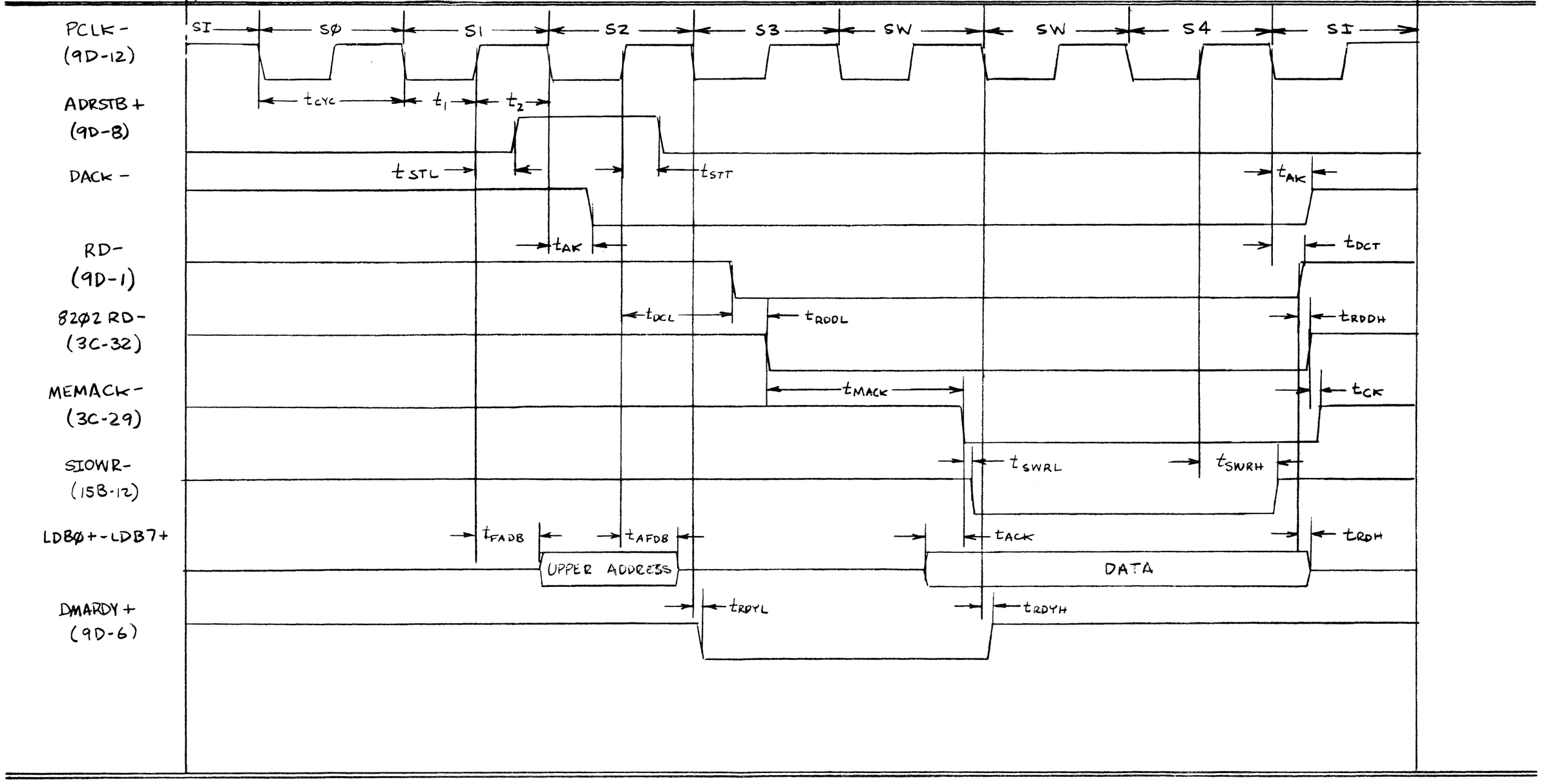
TITLE	APPROVALS	DATE	DWG NO
COMM CONTROLLER TIMING CPU MULTIBUS CYCLE	DRAWN		
APPLICATION	CHECKED		SHEET / REV
NEXT ASSY / USED ON	ENG		

SIGNAL	MULTIBUS RELEASED BY PREVIOUS MASTER	CONDITION



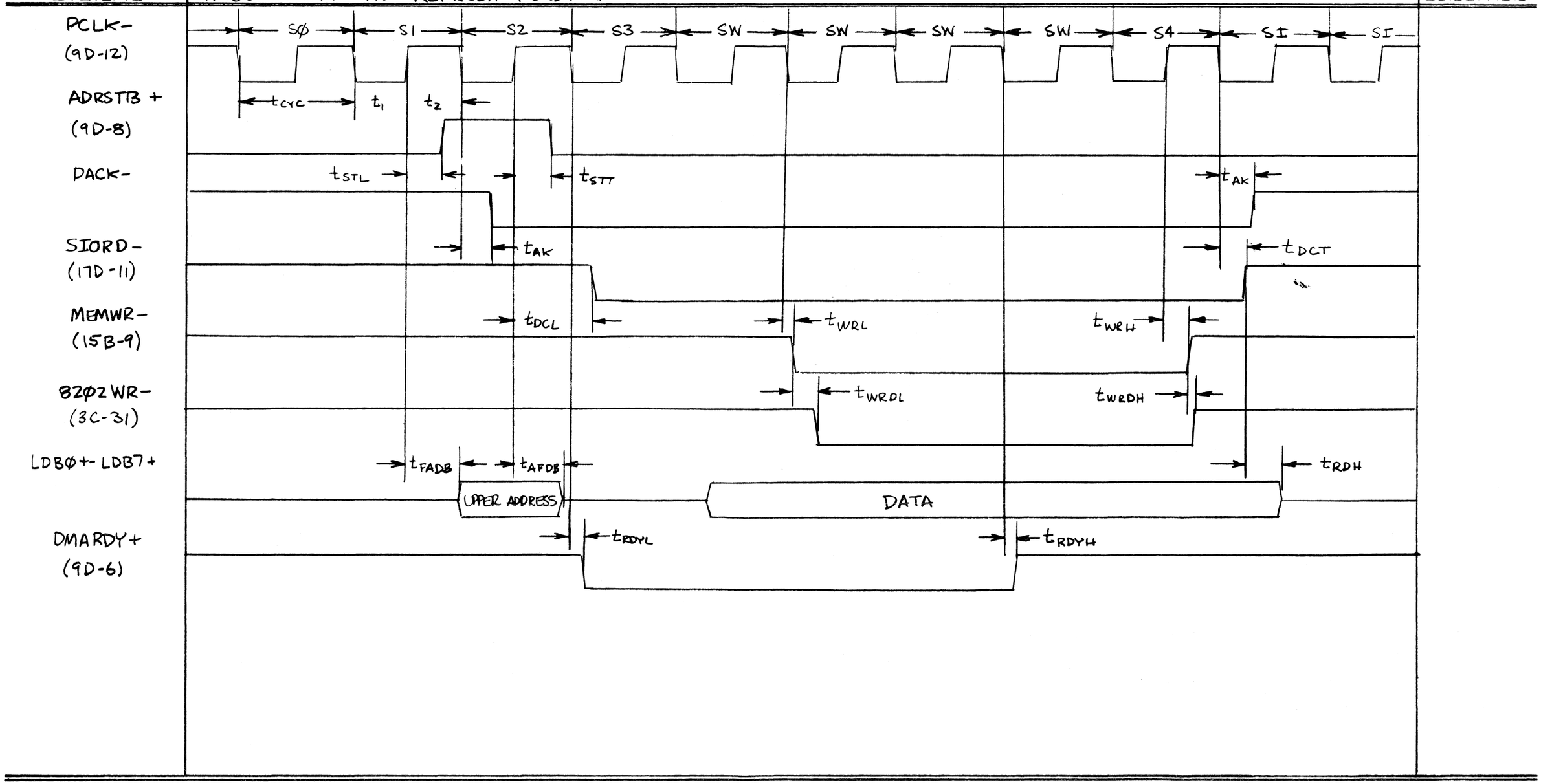
Convergent Technologies™

TITLE COMM CONTROLLER TIMING DMA READ CYCLE	APPROVALS	DATE	DWG NO
	DRAWN		
	CHECKED		
APPLICATION			SHEET / REV
NEXT ASSY / USED ON	ENG		



Convergent Technologies™

TITLE	APPROVALS	DATE	DWG NO
COMM CONTROLLER TIMING DMA WRITE CYCLE	DRAWN		
	CHECKED		
APPLICATION			SHEET / REV
NEXT ASSY / USED ON	ENG		



AC-DC CHARACTERISTICS

CPU MEMORY READ CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYC}			326		ns
t_1		83			ns
t_2		123			ns
t_{LCK}		103			ns
t_{RD}		735			ns
t_{LC}		133			ns
t_{RDDL}				91	ns
t_{RDH}				27	ns
t_{RDDH}				37	ns
t_{CC}		152		263	ns
t_{CAS}		254			ns
t_{CA}				91	ns
t_{CK}				30	ns
t_{RDY}				15	ns
t_{CAC}				165	ns
t_{AL}		118			ns
t_{LA}		103			ns
t_{LD}				13	ns
t_{ACK}				10	ns

AC-DC CHARACTERISTICS CPU MEMORY WRITE CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYC}			326		ns
t_1		83			ns
t_2		123			ns
t_{LCK}		103			ns
t_{WR}		735			ns
t_{LC}		133			ns
t_{WRDL}				109	ns
t_{WRDH}				63	ns
t_{CC}		152		263	ns
t_{CAS}		254			ns
t_{CA}				91	ns
t_{CK}				30	ns
t_{RDY}				15	ns
t_{AL}		118			ns
t_{LA}		103			ns
t_{WDL}				58	ns
t_{WD}		115			ns

AC-DC CHARACTERISTICS CPU IO/ROM CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYC}			326		ns
t_1		83			ns
t_2		123			ns
t_{CS}		25			ns
t_{LCK}		103			ns
t_{LC}		133			ns
t_{RD}		1061			ns
t_{WR}		1713			ns
t_{ROYL}				79	ns
t_{ROYH}				78	ns

AC-DC CHARACTERISTICS CPU MULTIBUS CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{BCY}			100		ns
t_{BREQL}				35	ns
t_{BREQH}				35	ns
t_{BUSYH}				48	ns
t_{BUSYL}				62	ns
t_{MBML}				40	ns
t_{MBMH}				30	ns
t_{AH}		130			ns
t_{CMDL}				40	ns
t_{CMDH}				40	ns
t_{AS}		50			ns
t_{CMPH}		436			ns

AC-DC CHARACTERISTICS DMA READ CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYC}			326		ns
t_1		123			ns
t_2		83			ns
t_{STL}				200	ns
t_{STT}				140	ns
t_{AK}				250	ns
t_{DCT}				200	ns
t_{DCL}				200	ns
t_{RDDL}				91	ns
t_{RODH}				37	ns
t_{MACK}		381		537	ns
t_{CK}				30	ns
t_{SWRL}				27	ns
t_{FADB}				300	ns
t_{AFDB}			t_{STT} + 20	170	ns
t_{ACK}		10			ns
t_{RDH}				27	ns
t_{RDYL}				89	ns
t_{RDYH}				83	ns
t_{SWRH}				227	ns

AC-DC CHARACTERISTICS DMA WRITE CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYC}			326		ns
t_1		123			ns
t_2		83			ns
t_{STL}				200	ns
t_{STT}				140	ns
t_{AK}				250	ns
t_{DCT}				215	ns
t_{DCL}				220	ns
t_{WRL}				43	ns
t_{WRH}				57	ns
t_{WRDL}				82	ns
t_{WRDH}				28	ns
t_{FADB}				300	ns
t_{AFDB}			t_{STT} + 20	170	ns
t_{RDH}				125	ns
t_{RDYL}				89	ns
t_{RDYH}				83	ns

DC CHARACTERISTICS

AC-DC CHARACTERISTICS

DC POWER REQUIREMENTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC} (+5V)				2.25	A
I_{DD} (+12V)				320	mA
I_{BB} (-12V)				21	mA

AC-DC CHARACTERISTICS DC MULTIBUS PARAMETERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DATX - I_{OL}				24	mA
DATX - I_{OH}				-2.6	mA
DATX - I_{IL}				-0.6	mA
DATX - I_{IH}				20	µA
ADRX - I_{OL}				12	mA
ADRX - I_{OH}				-12	mA
ADRX - I_{IL}				-0.8	mA
ADRX - I_{IH}				40	µA
MRDC-/MWTC- I_{OL}				64	mA
MRDC-/MWTC- I_{OH}				-15	mA
IOWC- I_{IL}				-0.4	mA
IOWC- I_{IH}				20	µA
XACK- I_{OL}				48	mA
XACK- I_{OH}				-250	µA
XACK- I_{IL}				-0.4	mA
XACK- I_{IH}				20	µA
BCLK- I_{IL}				-2	mA
BCLK- I_{IH}				50	µA
BREQ- I_{OL}				8	mA
BREQ- I_{OH}				-400	µA
BPRN- I_{IL}				-2	mA
BPRN- I_{IH}				50	µA
BUSY- I_{OL}				48	mA
BUSY- I_{OH}				-250	µA

AC-DC CHARACTERISTICS

DC MULTIBUS PARAMETERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
BUSY- I_{IL}				-0.4	mA
BUSY- I_{IH}				20	μA
CBRQ- I_{OL}				48	mA
CBRQ- I_{OH}				-250	μA
INIT- I_{IL}				-0.4	mA
INIT- I_{IH}				20	μA
CCLK- I_{IL}				-4.8	mA
CCLK- I_{IH}				140	μA
INTX- I_{OL}				48	mA
INTX- I_{OH}				-250	μA

REFERENCES

Connector Pin List

Connector P1

Pin	Signal
1	GND
2	GND
3	+5v
4	+5v
5	+5v
6	+5v
7	+12v
8	+12v
9	
10	
11	GND
12	GND
13	BCLK-
14	INIT-
15	BPRN-
16	BPRO-
17	BUSY-
18	BREQ-
19	MRDC-
20	MWTC-
21	IORC-
22	IOWC-
23	XACK-
24	
25	
26	
27	BHEN-
28	AD10-
29	CBRQ-
30	AD11-
31	CCLK-
32	AD12-
33	
34	AD13-
35	INT6-
36	
37	
38	INT5-
39	INT2-
40	
41	INT0-
42	
43	ADRE-
44	ADRF-
45	ADRC-
46	ADRD-

Pin	Signal
47	ADRA-
48	ADRB-
49	ADR8-
50	ADR9-
51	ADR6-
52	ADR7-
53	ADR4-
54	ADR5-
55	ADR2-
56	ADR3-
57	ADR0-
58	ADR1-
59	DATE-
60	DATF-
61	DATC-
62	DATD-
63	DATA-
64	DATB-
65	DAT8-
66	DAT9-
67	DAT6-
68	DAT7-
69	DAT4-
70	DAT5-
71	DAT2-
72	DAT3-
73	DAT0-
74	DAT1-
75	GND
76	GND
77	
78	
79	-12v
80	-12v
81	+5v
82	+5v
83	+5v
84	+5v
85	GND
86	GND

Connector P2

Pin	Signal
1	GND
2	GND
3	GND
4	GND
5	GND
6	CLOCK1+
7	GND
8	CLOCK1-
9	GND
10	DATA0+
11	GND
12	DATA0-
13	GND
14	DATA1-
15	GND
16	DATA1+
17	GND
18	CLOCK0+
19	GND
20	CLOCK0-

Device Pin Functions: 8085A Microprocessor

The 8085A is a complete 8-bit central processing unit (CPU). Its instruction set is completely software compatible with the 8080A microprocessor, and is designed to improve the present 8080A's performance by higher system speed. 8085A features include the following:

- o 1.3 microsecond instruction cycle,
- o on-chip clock generator (with external crystal, LC or RC network),
- o on-chip system controller; advanced cycle status information available for large system control,
- o four vectored interrupt inputs (one is nonmaskable) plus an 8080A-compatible interrupt,
- o serial in/serial out port,
- o decimal, binary, and double-precision arithmetic, and
- o direct addressing capability to 64K bytes of memory.

Signal Name	Pin Name	I/O	Function
--	VCC		+5v supply.
--	GND		Ground.
A8+ ... AF+	A8 ... A15	O	Address Bus. The most significant eight bits of the memory address or the eight bits of the I/O address, tristated during Hold and Halt modes and during RESET.
LDB0+ ... LDB7+	AD0 ... AD7	I/O	Multiplexed Address/Data Bus: Lower eight bits of the memory address (or I/O address) appear on the bus during the first clock cycle (T state) of a machine cycle. It then becomes the data bus during the second and third clock cycles.
--	ALE	O	Address Latch Enable: It occurs during the first clock state of a machine cycle and enables the address to get

			latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. The falling edge of ALE can also be used to strobe the status information. ALE is never tristated.
--	S0	O	Machine cycle status:
S1+	S1		
IO+	IO/M/		

IO/M/	S1	S0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

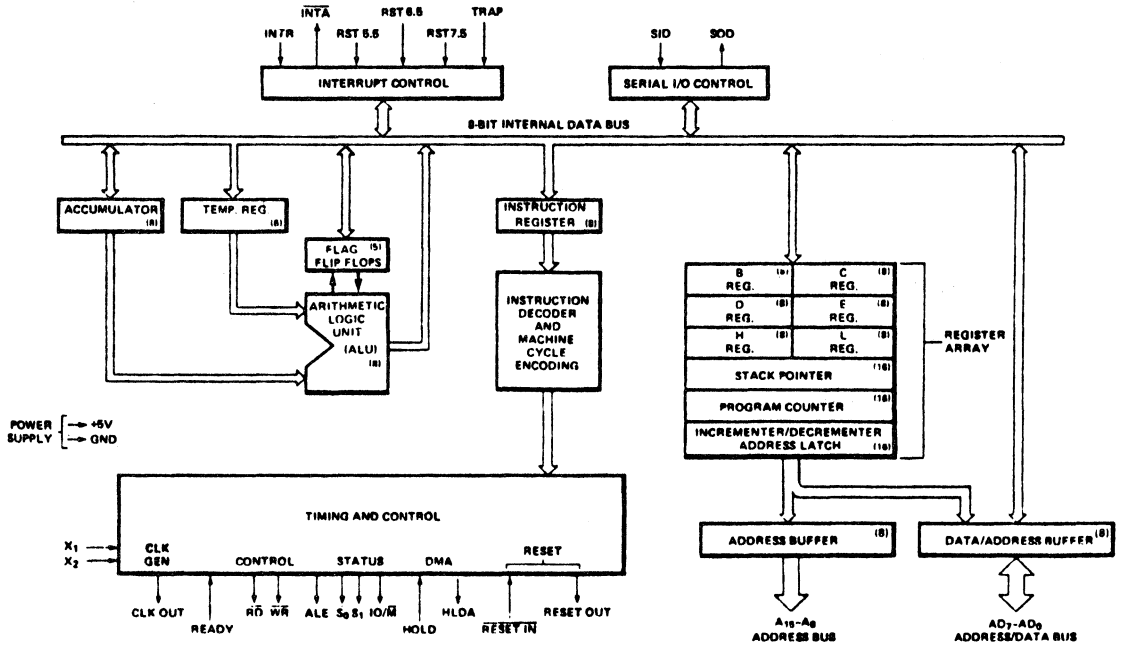
* = tristate (high impedance)
X = unspecified

S1 can be used as an advanced R/W/ status. IO/M/, S0, and S1 become valid at the beginning of a machine cycle and remain stable throughout the cycle. The falling edge of ALE may be used to latch the state of these lines.

--	RD/	O	READ control: A low level on RD/ indicates that the selected memory or I/O device is to be read and that the Data Bus is available for the data transfer. Tristated during Hold and Halt modes and during RESET.
--	WR/	O	WRITE control: A low level on WR/ indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR/. Tristated during Hold and Halt modes and during RESET.
CPURDY+	READY	I	If READY is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If READY is low, the CPU waits an integral number of clock cycles for READY to go high before completing the read or write cycle.

			READY must conform to specified setup and hold times.
CPUHOLD+	HOLD	I	HOLD indicates that another master is requesting the use of the address and data buses. The CPU, upon receiving the hold request, relinquishes the use of the bus as soon as the completion of the current bus transfer. Internal processing can continue. The processor can regain the bus only after the HOLD is removed. When the HOLD is acknowledged, the Address, Data, RD/, WR/, and IO/M/ lines are tristated.
CPUHLDA+	HLDA	O	HOLD ACKNOWLEDGE: Indicates that the CPU has received the HOLD request and that it will relinquish the bus in the next clock cycle. HLDA goes low after the Hold request is removed. The CPU takes the bus one half cycle after HLDA goes low.
--	INTR	I	INTERRUPT REQUEST: Is used as a general-purpose interrupt. It is sampled only during the next to the last clock cycle of an instruction and during Hold and Halt states. If it is active, the Program Counter (PC) is inhibited from incrementing and an INTA/ is issued. During this cycle, a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.
--	INTA/	O	INTERRUPT ACKNOWLEDGE: Is used instead of (and has the same timing as) RD/ during the Instruction cycle after an INTR is accepted. It can be used to activate the 8259 Interrupt chip or some other interrupt port.
MBINTR+ SIOINTR+ SWINTR+	RST7.5 RST6.5 RST5.5	I	RESTART INTERRUPTS: These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted. RST7.5 has the highest priority of these interrupts, RST5.5 the lowest. These interrupts have a higher priority than INTR. In addition, they

			may be individually masked out using the SIM instruction.
--	TRAP	I	Trap interrupt is a nonmaskable RESTART interrupt. It is recognized at the same time as INTR or RST5.5-7.5. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.
--	RESET IN/	I	Sets the Program Counter to 0 and resets the Interrupt Enable and HLDA flip-flops. The data and address buses and the control lines are tristated during RESET and, because of the asynchronous nature of RESET, the processor's internal registers and flags may be altered by RESET with unpredictable results. RESET IN/ is a Schmitt-triggered input, allowing connection to an R-C network for power-on RESET delay. The CPU is held in the reset condition as long as RESET IN is applied.
--	RESET OUT	O	Indicates CPU is being reset. Can be used as a system reset. The signal is synchronized to the processor clock and lasts an integral number of clock periods.
--	X1	I	X1 and X2 are connected to a crystal,
--	X2		LC, or RC network to drive the internal clock generator. X1 can be an external clock input from a logic gate. The input frequency is divided by 2 to give the processor's internal operating frequency.
--	CLK	O	Clock output for use as a system clock. The period of CLK is twice the X1, X2 input period.
--	SID	I	Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.
--	SOD	O	Serial output data line. The output SOD is set or reset as specified by the SIM instruction.



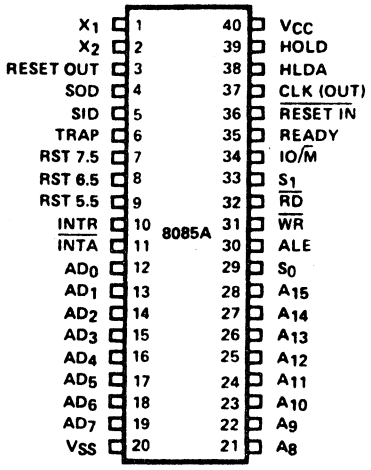


Figure 13-7. 8085A CPU

Device Pin Functions: 8257-5 DMA Controller

The 8257-5 is a four-channel Direct Memory Access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address that allows the peripheral to read or write data directly to or from memory. Acquisition of the system bus is accomplished via the CPU's hold function. The 8257-5 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete.

Signal Name	Pin Name	I/O	Function
--	VCC		+5V supply.
--	GND		Ground.
--	DRQ0 ... DRQ3	I	DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode, then DRQ0 has the highest priority and DRQ3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode), the request line is held high until the DMA acknowledge of the last cycle arrives.
DACK0- DACK1- -- --	DACK0/ DACK1/ DACK2/ DACK3/	0	DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it was selected for a DMA cycle. The DACK/ output acts as a "chip select" for the peripheral device requesting service. This line goes active (low) and inactive (high) once for each byte transferred, even if a burst of data is being transferred.

LDB0+ ... LDB7+	D0 ... D7	I/O	Data Bus Lines: These are bidirectional tristate lines. When the 8257 is being programmed by the CPU, eight bits of data for a DMA address register, a terminal count register, or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register, or the status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 outputs the most significant eight bits of the memory address (from one of the DMA address registers) to a latch via the data bus. These address bits are transferred at the beginning of the DMA cycle; the bus is then released to handle the memory data transfer during the balance of the DMA cycle.
--	IOR/	I/O	I/O Read: An active-low, bidirectional tristate line. In the "slave" mode, it is an input that allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, IOR/ is a control output that accesses data from a peripheral during the DMA write cycle.
--	IOW/	I/O	I/O Write: An active-low, bidirectional tristate line. In the "slave" mode, it is an input that allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, IOW/ is a control output that allows data to be output to a peripheral during a DMA read cycle.
PCLK-	CLK	I	Clock Input: Generally from an 8085A CLK output.
--	RESET	I	Reset: An asynchronous input (generally from an 8224 or 8085 device) that disables all DMA channels by clearing the mode register and tristates all control lines.

A0+ ... A3+	A0 ... A3	I/O	Address Lines: These least significant four address lines are bidirectional. In the "slave" mode, they are inputs that select one of the registers to be read or programmed. In the "master" mode, they are outputs that constitute the least significant four bits of the 16-bit memory address generated by the 8257.
--	CS/	I	Chip Select: An active-low input that enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, CS/ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.
A4+ ... A7+	A4 ... A7	O	Address Lines: These four address lines are tristate outputs that constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.
DMARDY+	READY	I	Ready: This asynchronous input elongates the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles. READY must conform to specified setup and hold times.
--	HRQ	O	Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ is normally applied to the HOLD input on the CPU. HRQ must conform to specified setup and hold times.
--	HLDA	I	Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.
IOR-	MEMR/	O	Memory Read: This active-low tristate output reads data from the addressed memory location during DMA Read cycles.
IOW-	MEMW/	O	Memory Write: This active-low tristate output writes data into the addressed memory location during DMA Write cycles.

ADRSTB+	ADSTB	O	Address Strobe: This output strobes the most significant byte of the memory address into a latch from the data bus.
--	AEN	O	Address Enable: This output disables (floats) the System Data Bus and the System Control Bus. It can also disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It can further isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the eight most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the four channels.
--	TC	O	Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel is automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n is the desired number of the DMA cycles.
--	MARK	O	Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisible by 128 (and the terminal

count register was loaded with n-1), does MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.

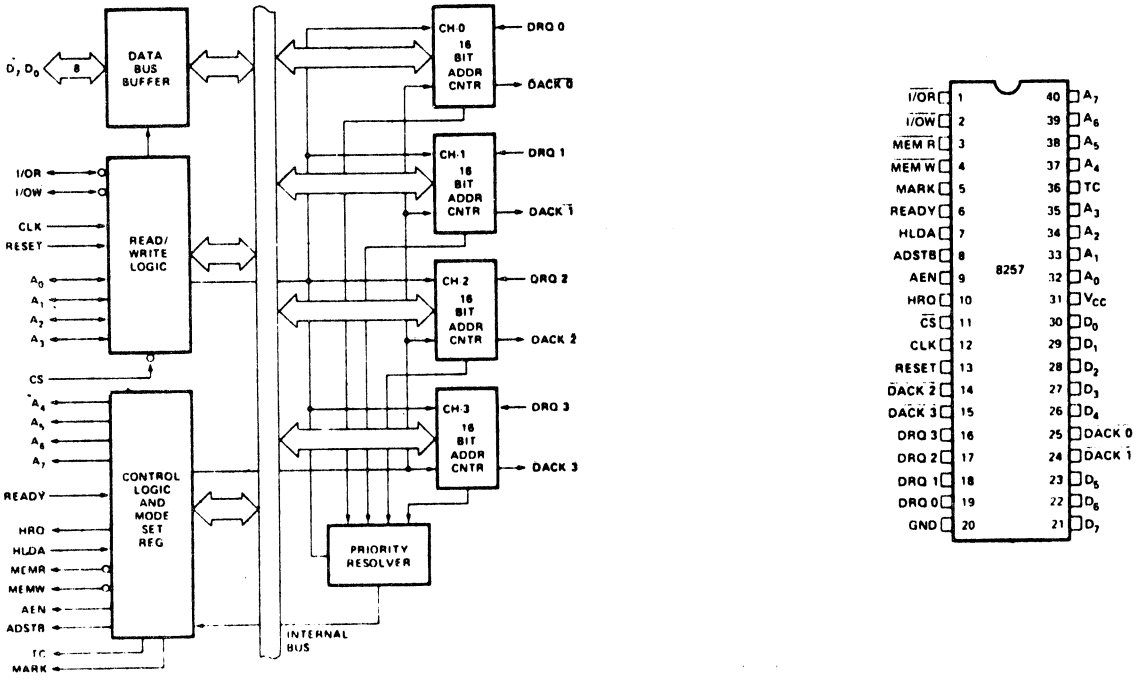


Figure 13-8. 8257-5 DMA Controller

Device Pin Functions: 8202A Dynamic RAM Controller

The 8202A is a Dynamic RAM System Controller designed to provide all signals necessary to use 2104A, 2117, or 2118 Dynamic RAMs in microcomputer systems. The 8202A provides multiplexed addresses and address strobes, as well as refresh/access arbitration. Refresh cycles can be started internally or externally.

Signal Name	Pin Name	I/O	Function
--	Vcc		+5v supply.
--	GND		Ground.
LAB0+ ... LAB6+	AL0 ... AL6	I	Low-Order Address. These address inputs generate the Row Address for the Multiplexer. If the AL6/OP3 input is pulled to +12v through a 5K ohm resistor, the 8202A configures itself for 4K RAMs. If AL6/OP3 is driven with TTL levels, the 8202A configures itself for 16K RAMs.
LAB7+ ... LABD+	AH0 ... AH6	I	High-Order Address. These address inputs generate the Column Address for the Multiplexer. If the 8202A is configured for 4K RAMs, AH6 can be used as an active high chip select for the memory controlled by 8202A. For 16K RAM operation, AH6 becomes the most significant column address bit.
--	OUT0/ ... OUT6/	O	Output of the Multiplexer. These outputs drive the addresses of the Dynamic RAM array. For 4K RAM operation, OUT6/ drives the 2104A CS/ input. (Note that the OUT/0-6 pins do not require inverters or drivers for proper operation.)
--	WE/	O	Write Enable. This output drives the Write Enable inputs of the Dynamic RAM array.
--	CAS/	O	Column Address Strobe. This output latches the Column Address into the Dynamic RAM array.

--	RAS0/ ... RAS3/	O	Row Address Strobe. These outputs latch the Row Address into the bank of of dynamic RAMs, selected by the 8202A Bank Address pins (B0, B1/OP1).
LABE+ --	B0 B1/OP1	I	Bank Address. These inputs select one of four banks of dynamic RAM via the RAS/0-3 outputs. If the B1/OP1 input is pulled to +12v through a 1K ohm resistor, the 8202A configures itself to the Advanced Read mode. This mode changes the function of the 8202A RD//S1 and REFRQ/ALE inputs and disables the RAS0/ and RAS1/ outputs.
--	RD/ S1	I	Read/S1 input. This input requests a read cycle. In normal operation, a low on this input informs the arbiter that a read cycle is requested. In the Advanced Read Mode, this input accepts the S1 status signal from the 8085A (fully decoded for a read). The trailing edge of ALE informs the arbiter that a read cycle is requested by latching S1.
--	WR/	I	Write Input. This input requests a write cycle. A low on this input informs the arbiter that a write cycle is desired.
MEMCY-	PCS/	I	Protected Chip Select. A low on this input enables the WR/ and RD//S1 inputs. PCS/ is protected against terminating a cycle in progress.
--	REFRQ/ ALE	I	Refresh Request/Address Latch Enable. During normal operation, a high on this input indicates to the arbiter that a refresh cycle is being requested. In the Advanced Read Mode, this input latches the state of the 8085 S1 signal into the RD//S1 input. If S1 is high at this time, a Read Cycle is requested. In this mode, transparent refresh is not possible.
MEMACK-	XACK/	O	Transfer Acknowledge. This output is a strobe indicating valid data during a read cycle or data written during a write cycle. XACK can latch valid data from the RAM array.

SACK-	SACK/	O	System Acknowledge. This output indicates the beginning of a memory access cycle. It can be used as an advanced transfer acknowledge to eliminate wait states. (Note: If a memory access request is made during a refresh cycle, SACK/ is delayed until XACK/ in the memory access cycle.)
--	X0/OP2	I	Crystal Inputs. These inputs permit a quartz crystal to control the frequency of the oscillator. If X0/OP2 is pulled to +12v through a 1K ohm resistor, X1/CLK becomes a TTL input for an external clock.
--	X1/CLK	I	
--	TNK		Tank. This pin is a tank circuit connection.

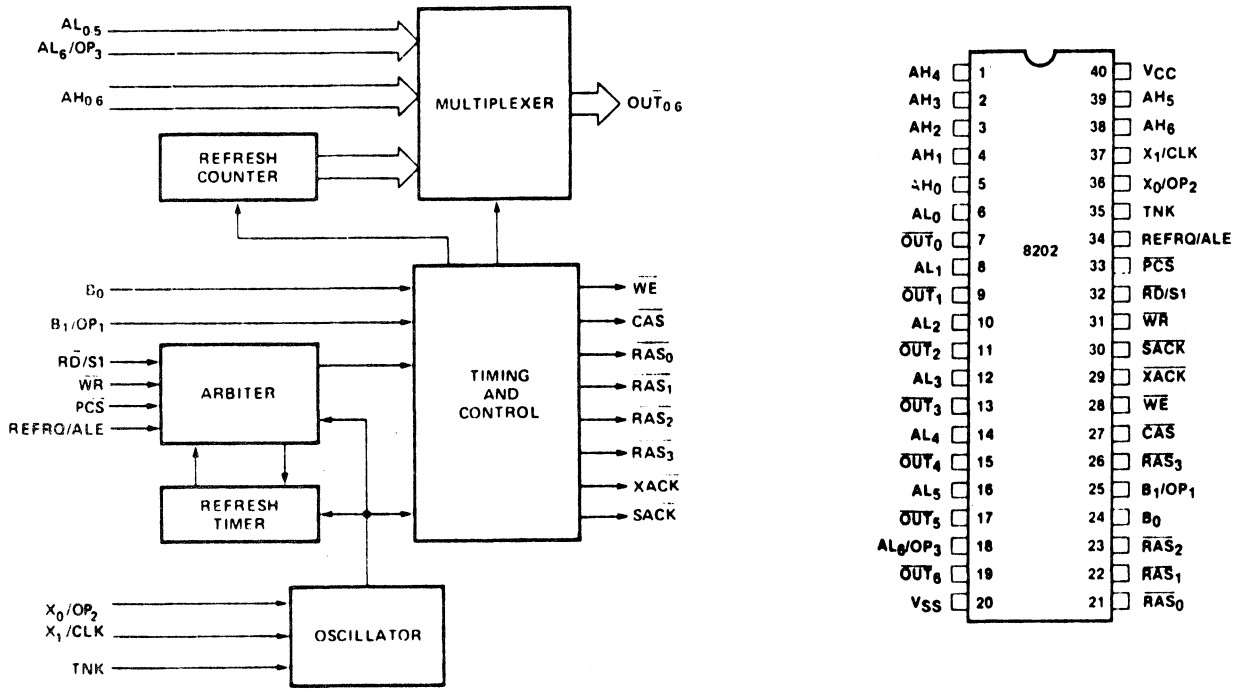


Figure 13-9. 8202A Dynamic RAM Controller

Device Pin Functions: Z80A SIO/2 Communications Controller

The Z80 SIO Serial I/O Controller is a dual-channel data communications interface. Its basic functions as a serial-to-parallel, parallel-to-serial converter/controller can be programmed by a CPU for a broad range of serial communications applications. The device supports all common asynchronous and synchronous protocols, byte- or bit-oriented, and performs all of the functions traditionally done by UARTs, USARTs and synchronous communications controllers combined, plus additional functions traditionally performed by the CPU. Some of its features are:

- Two independent full-duplex channels, with separate control and status lines for modems or other devices.
- Data rates of 0 to 800K bits/second with a 4.0 MHz clock (Z80A SIO).
- Everything necessary for complete messages in 5, 6, 7, or 8 bits/character. Includes variable stop bits and several clock-rate multipliers, break generation and detection, parity, overrun and framing error detection.
- Synchronous protocols: everything necessary for complete bit- or byte-oriented messages in 5, 6, 7, or 8 bits/character, including IBM Bisync, SDLC, HDLC, CCITT-X.25, and others. Automatic CRC generation/checking, sync character and zero insertion/deletion, abort generation/detection, and flag insertion.
- Receiver data registers quadruply buffered, transmitter registers doubly buffered.

Signal Name	Pin Name	I/O	Function
--	+5V		+5v supply.
--	GND		Ground.
--	B	I	Channel A OR B Select (input, high selects Channel B). This input defines which channel is accessed during a data transfer between the CPU and the SIO. Address bit A0 from the CPU is often used for the selection function.

--	C	I	Control or Data Select (input, high selects control). This input defines the type of information transfer performed between the CPU and the SIO. A high at this input during a CPU write to the SIO causes the information on the data bus to be interpreted as a command for the channel selected by B. A low at C means that the information on the data bus is data. Address bit A1 is often used for this function.
--	CE/	I	Chip Enable (input, active low). A low level at this input enables the SIO to accept command or data input from the CPU during a write cycle, or to transmit data to the CPU during a ready cycle.
SIOCLK+	CLK	I	System Clock (input). The SIO uses the standard Z80 System Clock to synchronize internal signals. This is a single-phase clock.
-- --	CTSA/ CTSB/	I	Clear to Send (inputs, active low). When programmed as Auto Enables, a low on these inputs enables the respective transmitter. If not programmed as auto enables, these inputs can be programmed as general-purpose inputs. Both inputs are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these inputs and interrupts the CPU on both logic level transitions. The Schmitt-trigger buffering does not guarantee a specified noise-level margin.
LDB0+ ... LDB7+	D0 ... D7	I/O	System Data Bus (bidirectional, tristate). The system data bus transfers data and commands between the CPU and the Z80 SIO. D0 is the least significant bit.
DCD0- DCD1-	DCDA/ DCDB/	I	Data Carrier Detect (inputs, active low). These pins function as receiver enables if the SIO is programmed for auto enables; otherwise they can be used as general-purpose input pins. Both pins are Schmitt-trigger buffered to accommodate slow-risetime signals. The SIO detects pulses on these

			pins and interrupts the CPU on both logic level transitions. Schmitt-trigger buffering does not guarantee a specific noise-level margin.
--	DTRA/	O	Data Terminal Ready (outputs, active
--	DTRB/		low). These outputs follow the state programmed into Z80 SIO. They can also be programmed as general-purpose outputs.
--	IEI	I	Interrupts Enable In (input, active high). This signal, with IEO, forms a priority daisy chain when there is more than one interrupt-driven device. A high on this line indicates that no other device of higher priority is being serviced by a CPU interrupt service routine.
--	IEO	O	Interrupt Enable Out (output, active high). IEO is high only if IEI is high and the CPU is not servicing an interrupt from this SIO. Thus, this signal blocks lower priority devices from interrupting while a higher priority device is being serviced by its CPU interrupt service routine.
--	INT/	O	Interrupt Request (output, open drain, active low). When the SIO is requesting an interupt, it pulls INT/ low.
--	IORQ/	I	I/O Request (output, open drain, active low). IORQ/, in conjunction with B, C, CE/ and RD/, transfers commands and data between the CPU and the SIO. When CE/ and RD/ are all active, the channel selected by B/A transfers data to the CPU (a read operation). When CE/ and IORQ/ are active, but RD/ is inactive, the channel selected by B is written to by the CPU with either data or control information as specified by C. If IORQ/ and M1/ are active simultaneously, the CPU is acknowledging an interrupt and the SIO automatically places its interrupt vector on the CPU data bus if it is the highest priority device requesting an interrupt.

--	M1/	I	Machine Cycle (input from Z80 CPU, active low). When M1/ is active and RD/ is also active, the Z80 CPU is fetching an instruction from memory; when M1/ is active while IORQ/ is active, the SIO accepts M1/ and IORQ/ as an interrupt acknowledge if the SIO is the highest priority device that has interrupted the Z80 CPU.
-- --	RxCA/ RxCB/	I	Receiver Clocks (inputs). Receive data is sampled on the rising edge of RxC/. The Receiver Clocks can be 1, 16, 32, or 64 times the data rate in asynchronous modes. Both inputs are Schmitt-trigger buffered (no noise level margin is specified).
SIORD-	RD/	I	Read Cycle Status (input from CPU, active low). If RD/ is active, a memory or I/O read operation is in progress. RD/ is used with B, CE/, and IORQ/ to transfer data from the SIO to the CPU.
-- --	RxDA RxDB	I I	Receive Data (inputs, active high). Serial data at TTL levels.
RESET-	RESET/	I	Reset (input, active low). A low RESET/ disables both receivers and transmitters, forces TxDA and TxDB marking, forces the modem controls high, and disables all interrupts. The control registers must be re-written after the SIO is reset and before data is transmitted or received.
-- --	RTSA/ RTSB/	O	Request to Send (outputs, active low). When the RTS bit in Write Register 5 is set, the RTS/ output goes low. When the RTS bit is reset in the asynchronous mode, the output goes high after the transmitter is empty. In synchronous modes, the RTS/ pin strictly follows the state of the RTS bit. Both pins can be used as general-purpose outputs.
-- --	SYNCA/ SYNCB/	I/O	Synchronization (inputs/outputs, active low). These pins can act either as inputs or outputs. In the asynchronous receive mode, they are inputs similar to CTS/ and DCD/. In

this mode, the transitions on these lines affect the state of the Sync/Hunt status bits in Read Register 0, but have no other function. In the External Sync mode, these lines also act as inputs. When external synchronization is achieved, SYNC/ must be driven low on the second rising edge of RxC/ after that rising edge of RxC/ on which the last bit of the sync character was received. In other words, after the sync pattern is detected, the external logic must wait for two full Receive Clock cycles to activate the SYNC/ input. Once SYNC/ is forced low, it should be kept low until the CPU informs the external synchronization detect logic that synchronization was lost or a new message is about to start. Character assembly begins on the rising edge of RxC/ that immediately precedes the falling edge of SYNC/ in the External Sync mode.

In the internal synchronization mode (Monosync and Bisync), these pins act as outputs that are active during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync pattern is recognized, regardless of character boundaries.

In the Z80 SIO/2 bonding option, SYNCB/ is omitted.

TxCA/ I
TxCB/

TRANSMITTER CLOCKS (inputs). TxD changes from the falling edge of TxC. In asynchronous modes, the Transmitter Clocks can be 1, 16, 32, or 64 times the data rate; however, the clock multiplier for the transmitter and the receiver must be the same. The Transmit Clock inputs are Schmitt-trigger buffered for relaxed rise- and fall-time requirements (no noise level margin is specified).

In the Z80 SIO/0 bonding option, TxCA/ is bonded together with TxCB/.

-- --	TxDA TxDB	O	TRANSMIT DATA (outputs, active high). Serial data at TTL levels.
SIORQ0- SIORQ1-	WRDYA/ WRDYB/	O	WAIT/READY A, WAIT/READY B (outputs, open drain, when programmed for Wait function; driven high and low when programmed for ready function). These dual-purpose outputs can be programmed as ready lines for a DMA controller or as Wait lines that synchronize the CPU to the SIO data rate. The reset state is open drain.

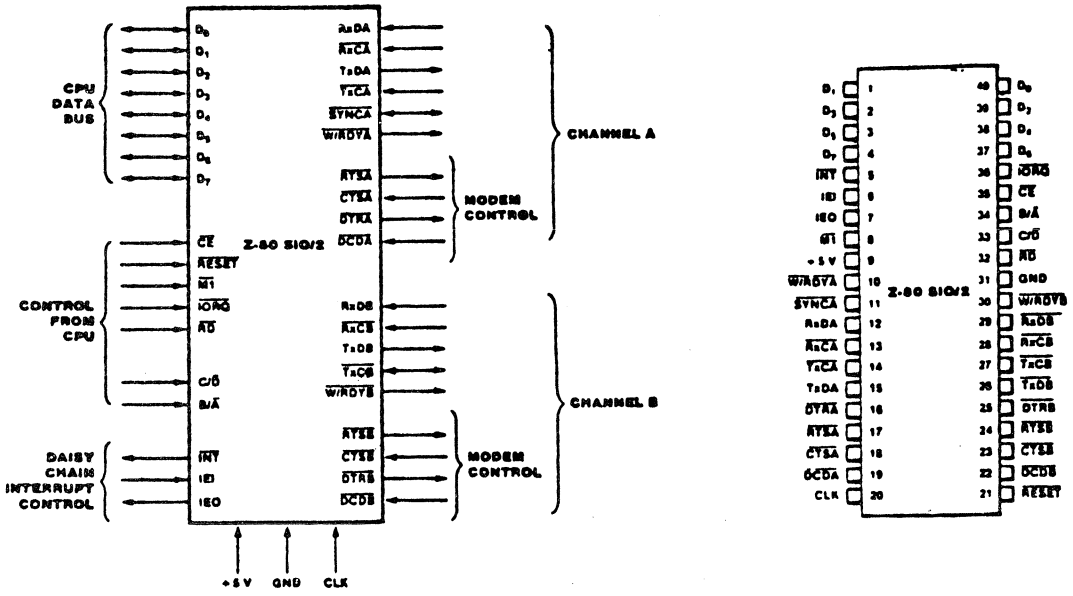


Figure 13-10. Z80A SIO/2

Device Pin Functions: 8253 Programmable Interval Timer

The 8253 Programmable Interval Timer/Counter functions as a general purpose, multitiming element that can be treated as an array of I/O ports in the system software. It is organized as three independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

Signal Name	Pin Name	I/O	Function
--	VCC		+5v supply.
--	GND		Ground.
LDB0+ ... LDB7+	D0 ... D7	I/O	Data Bus: A tristate, bidirectional, 8-bit buffer interfaces the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output CPU instructions. The Data Bus Buffer has three basic functions. 1. Programming the modes of the 8253. 2. Loading the count registers. 3. Reading the count values.
LAB1+ LAB2+	A0 A1	I	A0, A1: These inputs are normally connected to the address bus. They select one of the three counters to be operated on and address the control word register for mode selection.
TIMERS-	CS/	I	Chip Select enables the 8253. No reading or writing occurs unless the device is selected. The CS/ input has no effect upon the actual operation of the counters.
RD-	RD/	I	Read informs the 8253 that the CPU is inputting data in the form of a counters value.
WR-	WR/	I	Write informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.
1.23MHZ+ 1.23MHZ+ 1.23MHZ+	CLK0 CLK1 CLK2	I	Counter Clock Inputs provide the time base for the three independent interval counters.

--	GATE0	I	Counter Gate Inputs can enable, trig-
--	GATE1		ger or disable counters.
--	GATE2		
--	OUT0	O	Counter Outputs: In mode 0, these
--	OUT1		lines go HIGH when the programmed in-
SWINTR+	OUT2		terval has elapsed. In mode 3, they toggle at the rate programmed.

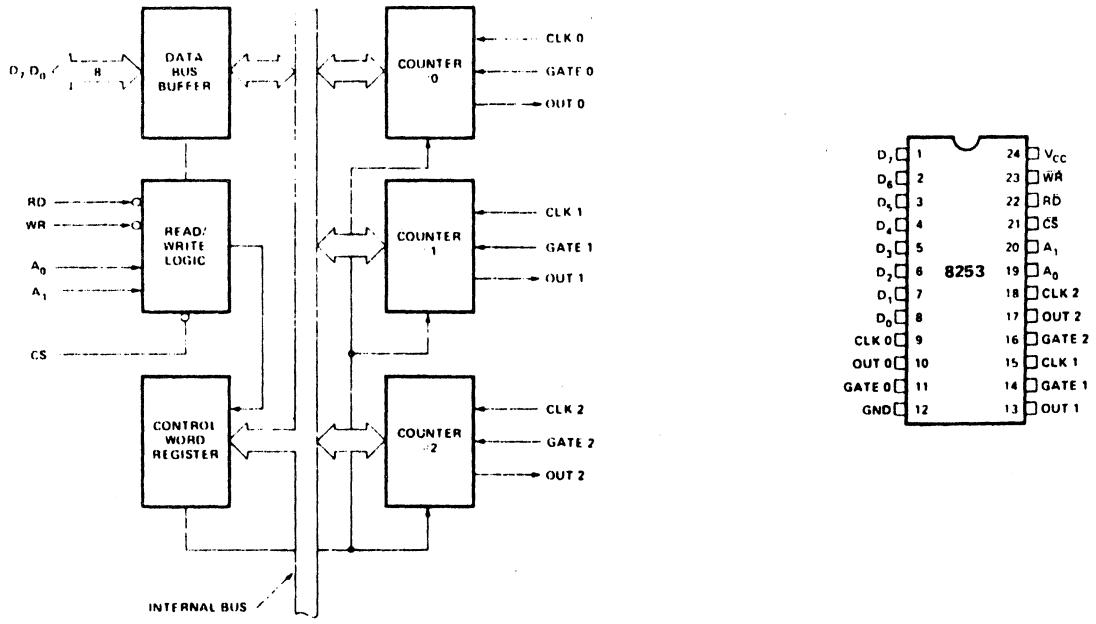


Figure 13-11. 8253 Programmable Interval Timer

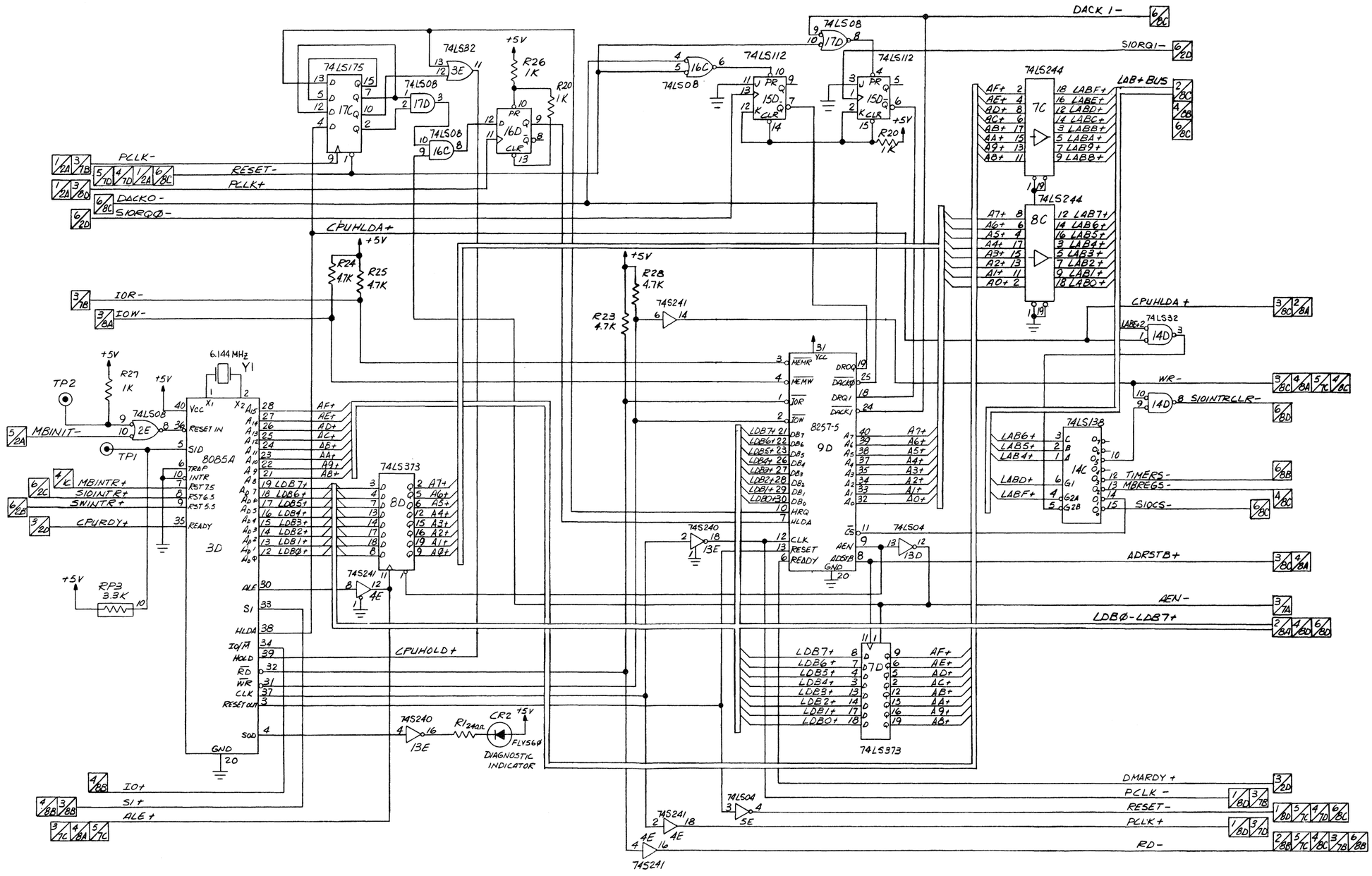


Figure 13-12 Communications I/O Processor Schematic
(Page 1 of 6)

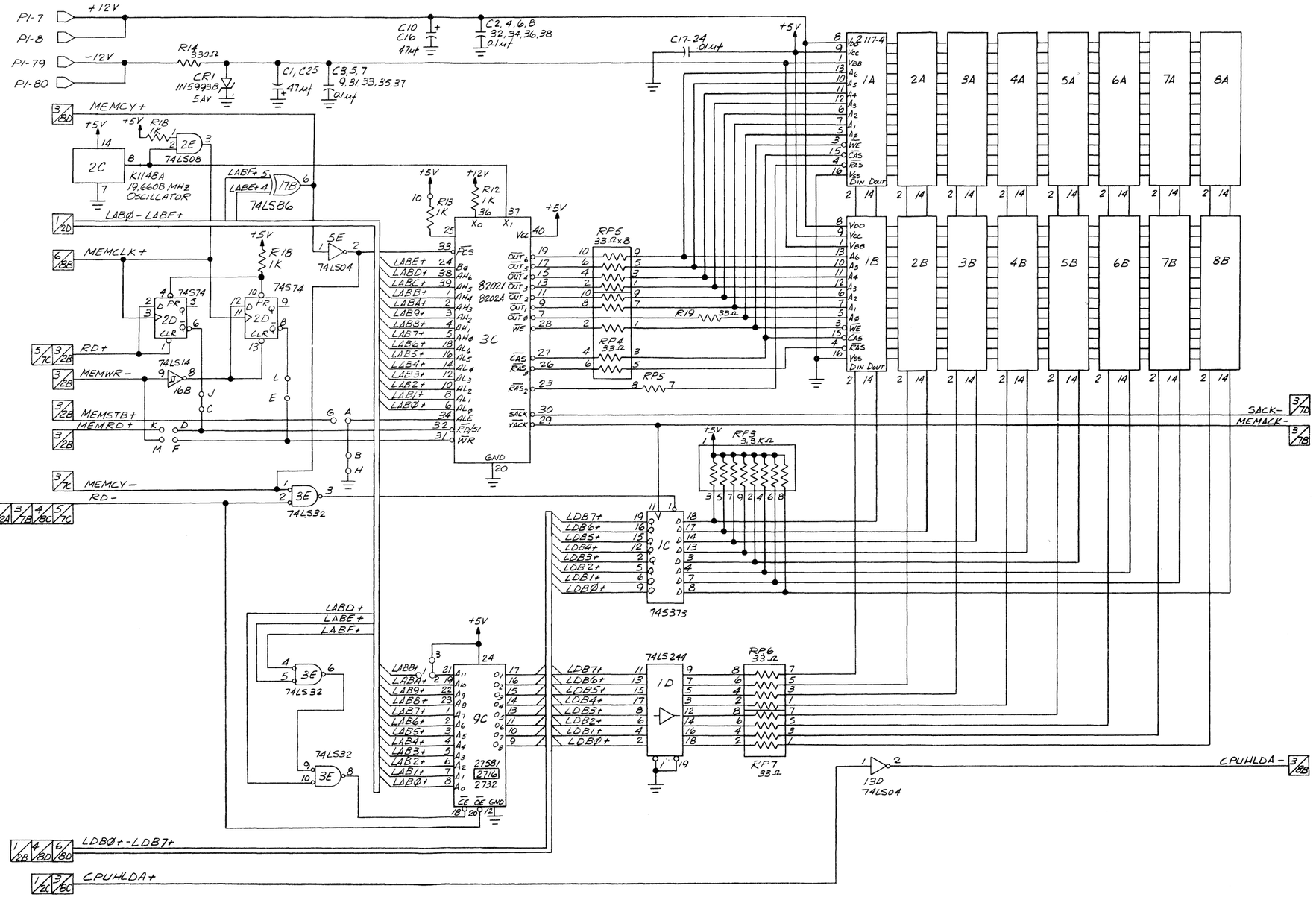
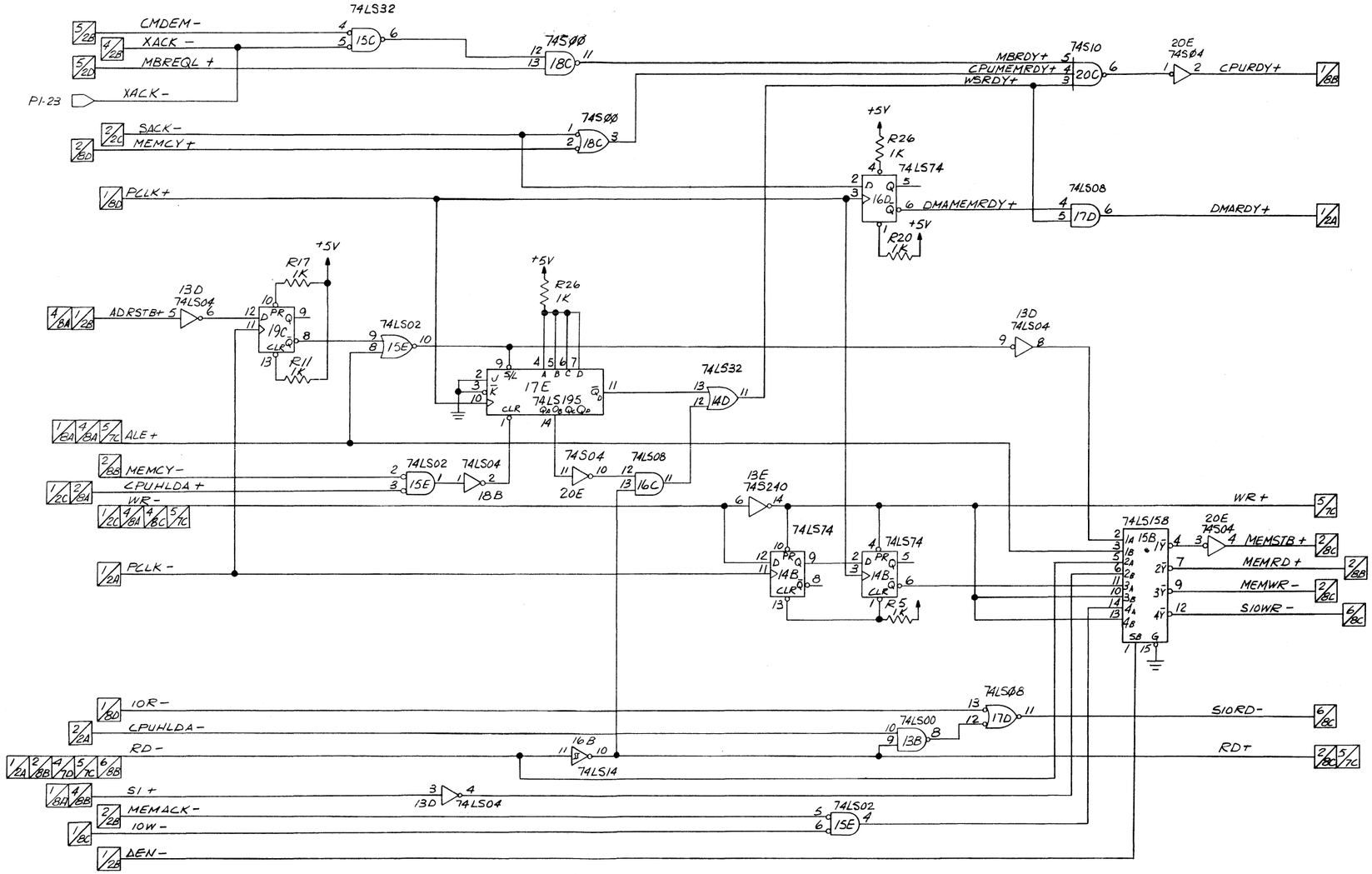


Figure 13-12 Communications I/O Processor Schematic
(Page 2 of 6)



READY AND CONTROL LOGIC

Figure 13-12 Communications I/O Processor Schematic
(Page 3 of 6)

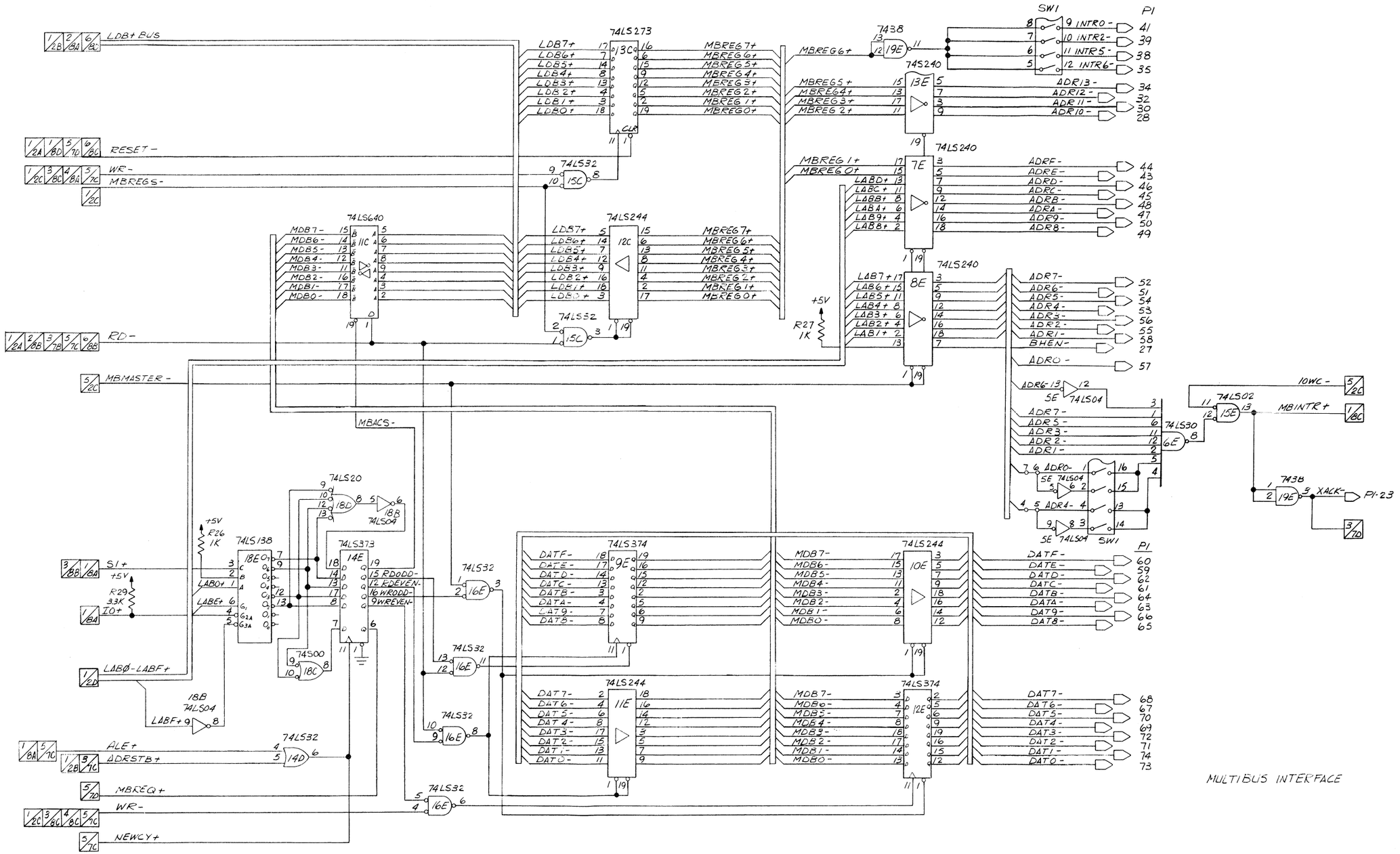
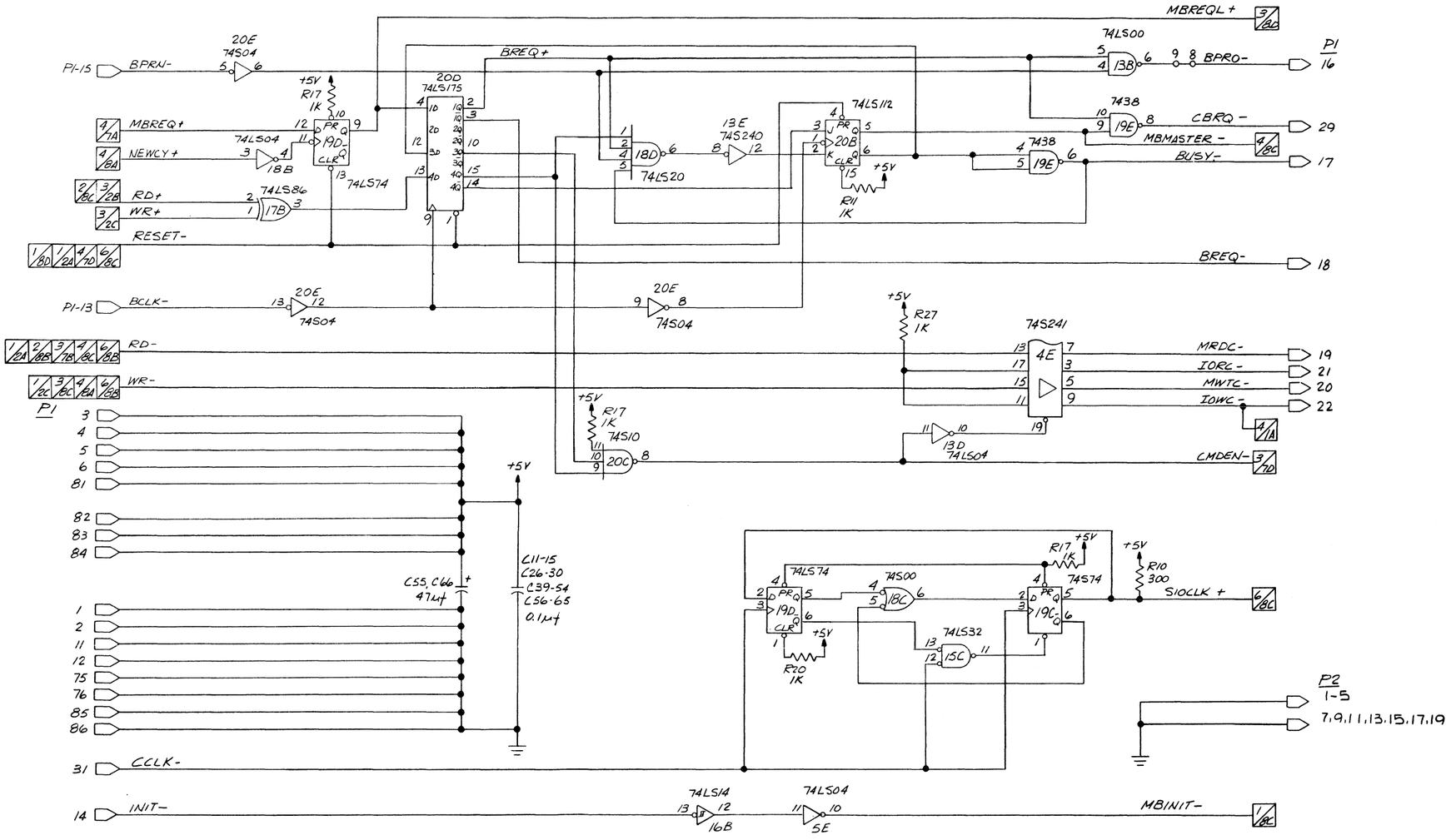


Figure 13-12 Communications I/O Processor Schematic
(Page 4 of 6)



MULTIBUS MASTER CONTROL

Figure 13-12 Communications I/O Processor Schematic
(Page 5 of 6)

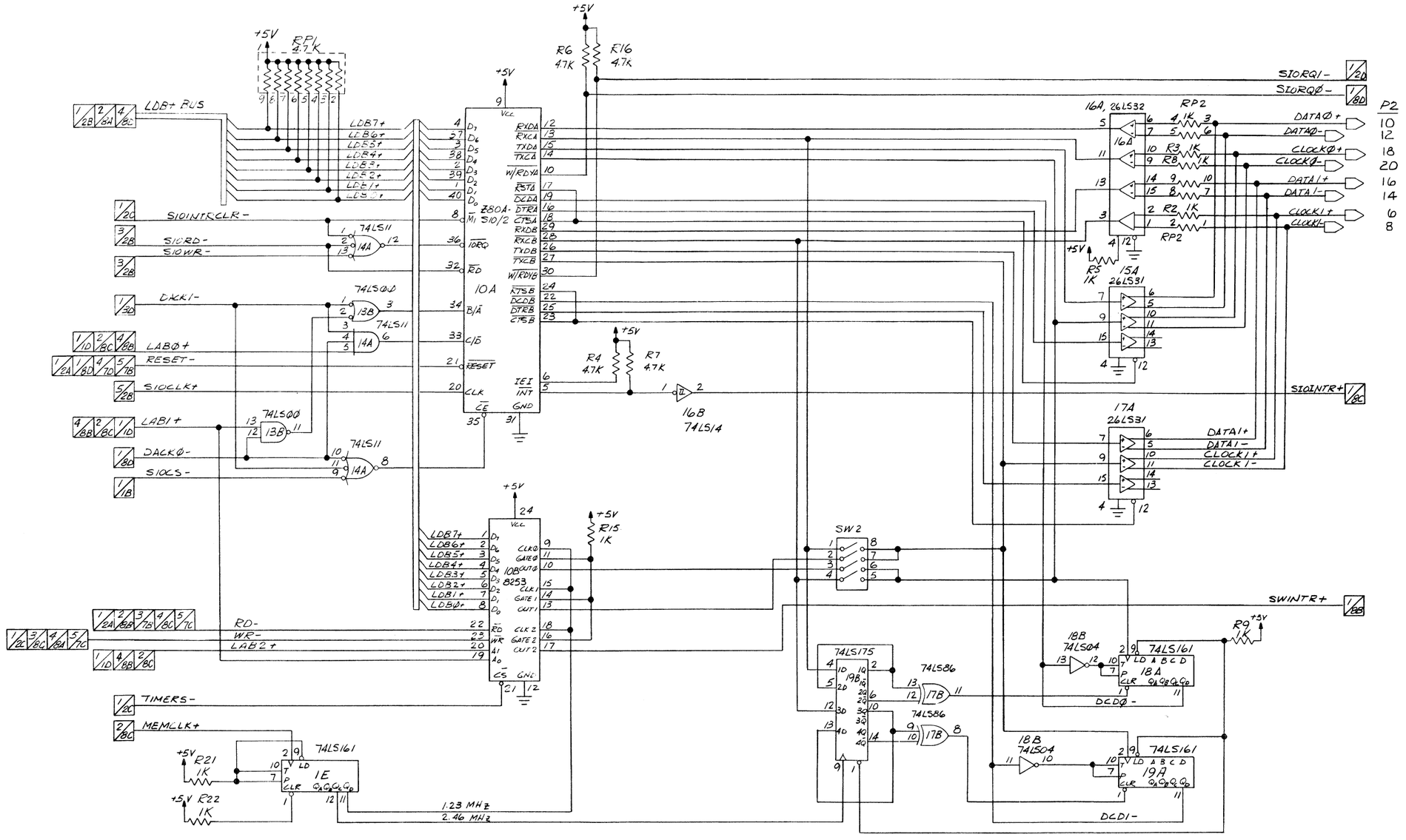


Figure 13-12 Communications I/O Processor Schematic
(Page 6 of 6)

NOTES:

1. MASK AREA INDICATED PRIOR TO LOADING.
2. SOCKETS TO BE INSTALLED BY SUB-CONTRACTOR. IC TO BE INSTALLED AT TEST.
3. MASK AREA INDICATED. COMPONENTS TO BE INSTALLED AT TIME OF FINAL TOUCH-UP.
4. COMFIRM ORIENTATION.
5. ~~USE OF SUPPORT FIXTURE REQUIRED DURING WAVE SOLDER~~.
6. MARK ENGINEERING REVISION LEVEL FOR THIS ASSEMBLY.
7. MARK APPROPRIATE DATE CODE TO SHOW DATE OF MANUFACTURE. DATE CODE IS [ ].
8. FOR COMPLETE LIST OF MATERIALS SEE A-60-00014-00.
9. SCHEMATIC REF. A-08-00004-00.

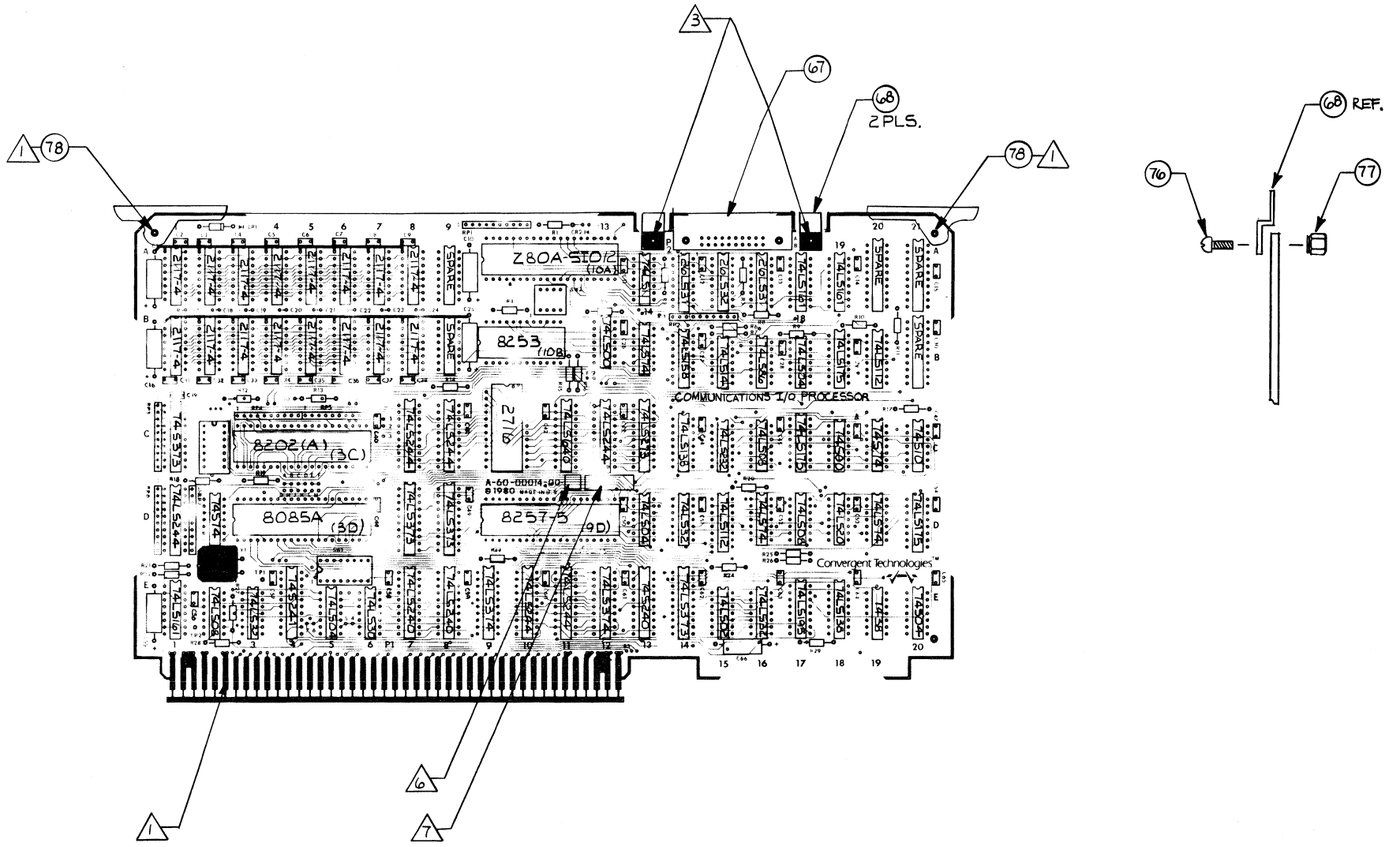


Figure 13-13 Communications I/O Processor
Printed Circuit Assembly