Convergent Technologies

UPDATE NOTICE 3
(A-09-00091-01-A)

WORKSTATION HARDWARE MANUAL

The attached pages update: (1) edition A-09-00016-01-A and Update Notices A-09-00058-01-A and A-09-00066-01-A or (2) edition A-09-00016-01-B and Update Notice A-09-00066-01-A, of the Workstation Hardware Manual.

Insert these pages according to the collating instructions on the back of this notice.

Updated pages are indicated by a date at the bottom of the page.

Throughout this Manual, change bars in the margins indicate technical additions and changes. Asterisks indicate deletions. Editorial changes are not identified. All changes will be incorporated in the next edition of this Manual.

Insert this page after the title page of your manual to provide a record of the update.

COLLATING INSTRUCTIONS

Delete	Replace With
Table of Contents (ix, x)	Table of Contents (ix, x)
10-3, 10-4 two foldouts from Section 10 (unpaginated; Video Monitor Schematic, Video Monitor Assembly Drawing)	10-3, 10-4 10-9, 10-11
Appendix C (D-1 to D-5)	Appendix C (D-1 to D-7)

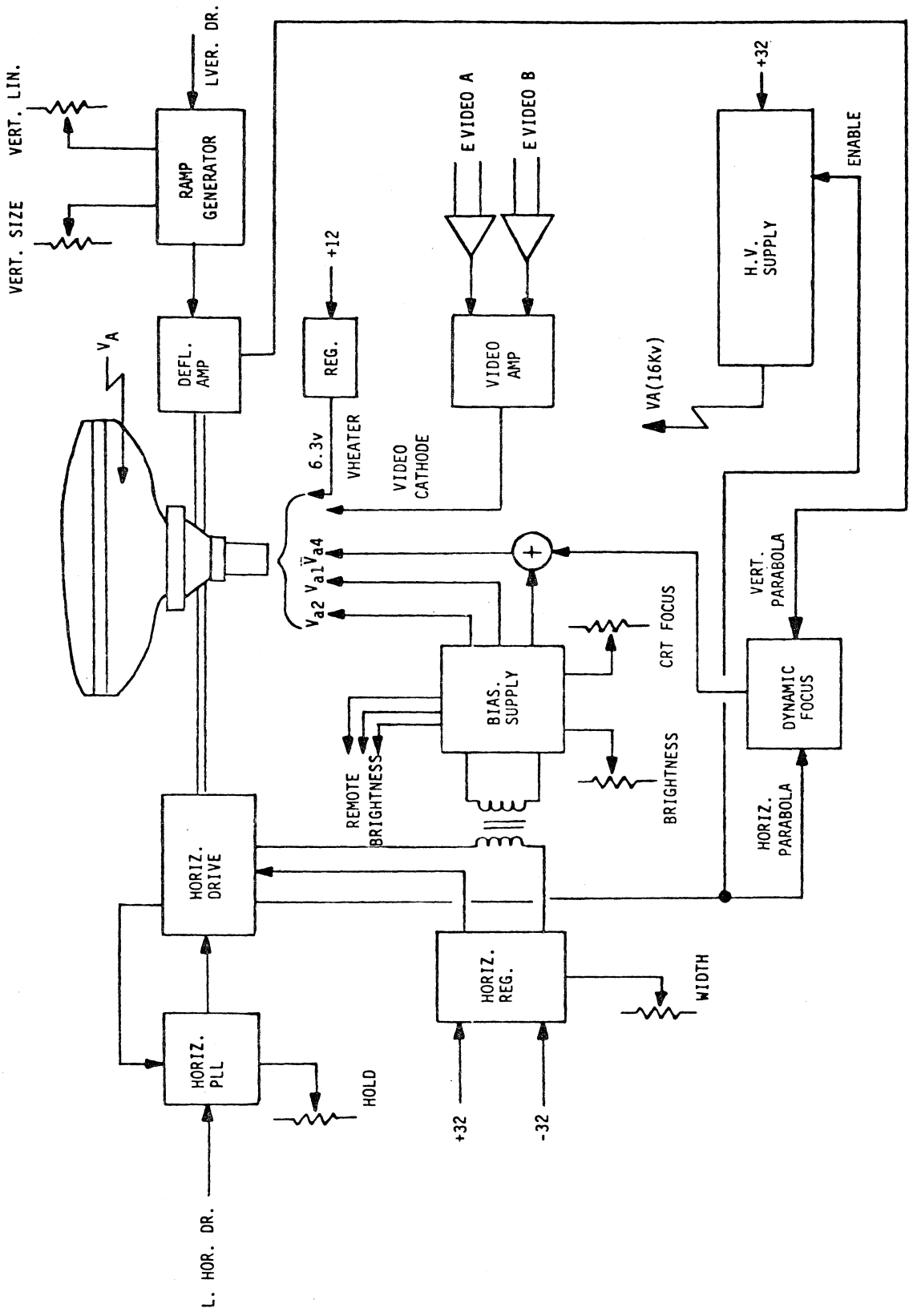

Figure 10-1. CRT-Display Block Diagram

The dynamic focus circuit is used to alter the focus voltage as a function of the position of the electron beam on the CRT face. In this way, optimum focus can be maintained, resulting in maximum resolution. The dynamic focus waveform is a composite of two parabolic waveforms. One waveform repeats at the horizontal rate (HORIZ.PARABOLA) and the other repeats at the vertical rate (VER.PARABOLA). This waveform, when summed with the D.C. focus electrode bias (adjustable by the C.FOCUS control), yields a waveform that offers maximum focus correction at the corners of the CRT raster.

Video Amplifier

EVIDEOA and EVIDEOB, the ECL signals for video display data, are converted to VIDEO, the signal which drives the cathode. The level-shifting amplifier is an emitter-coupled configuration with common-base output stage. The amplitude is 25 volts for normal data and 20 volts for half-bright data (controlled by EVIDEOB).

Power

Anode voltage for the CRT is generated by a 16-kV supply which operates from the 32 volt regulated power source. The power supply is enabled only when horizontal drive is functioning.

Another regulator provides 6.3 volts for the heater and 5 volts for the video amplifier. Power for this second regulator comes from +12V.

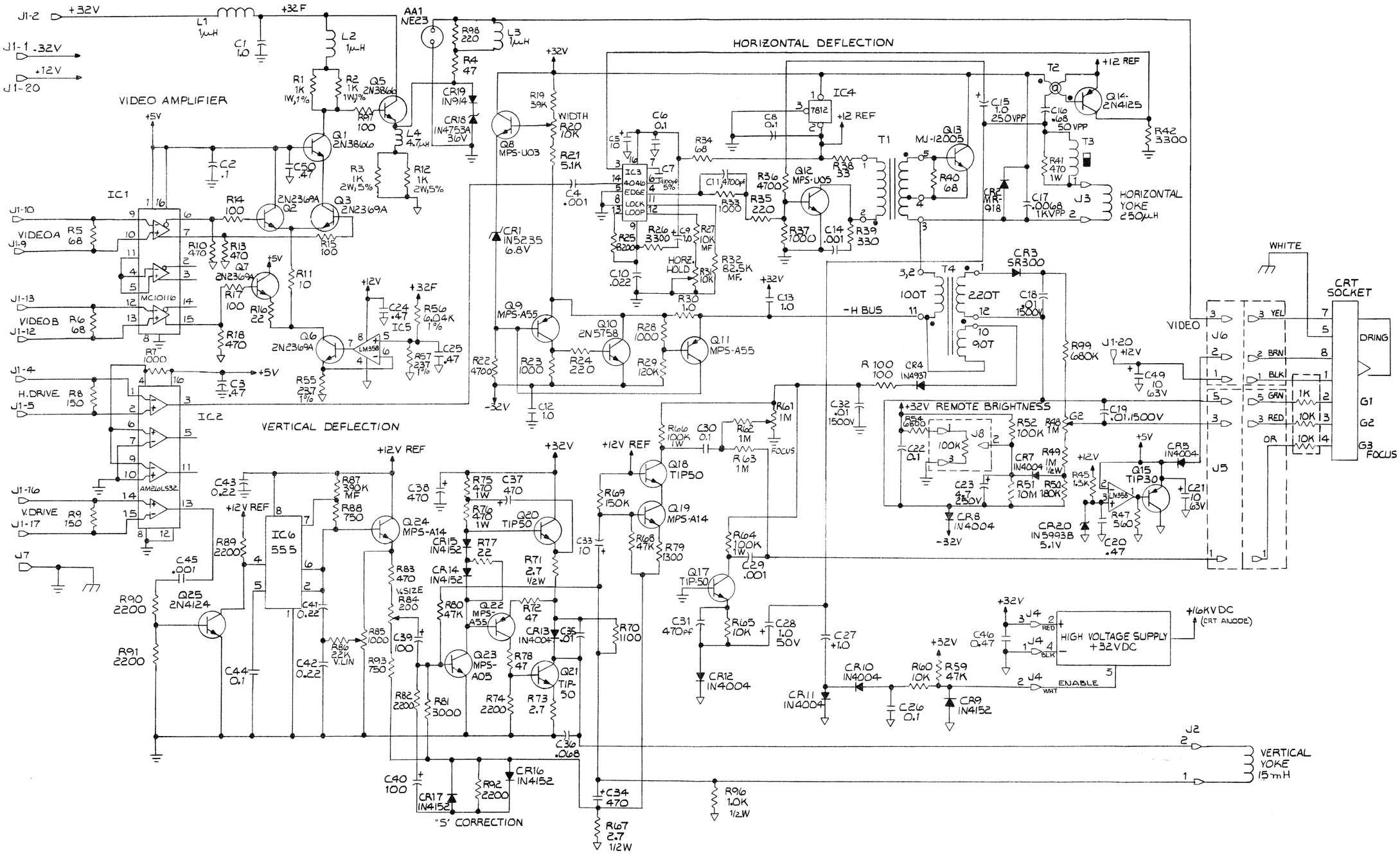

Figure 10-2. CRT-Deflection Schematic

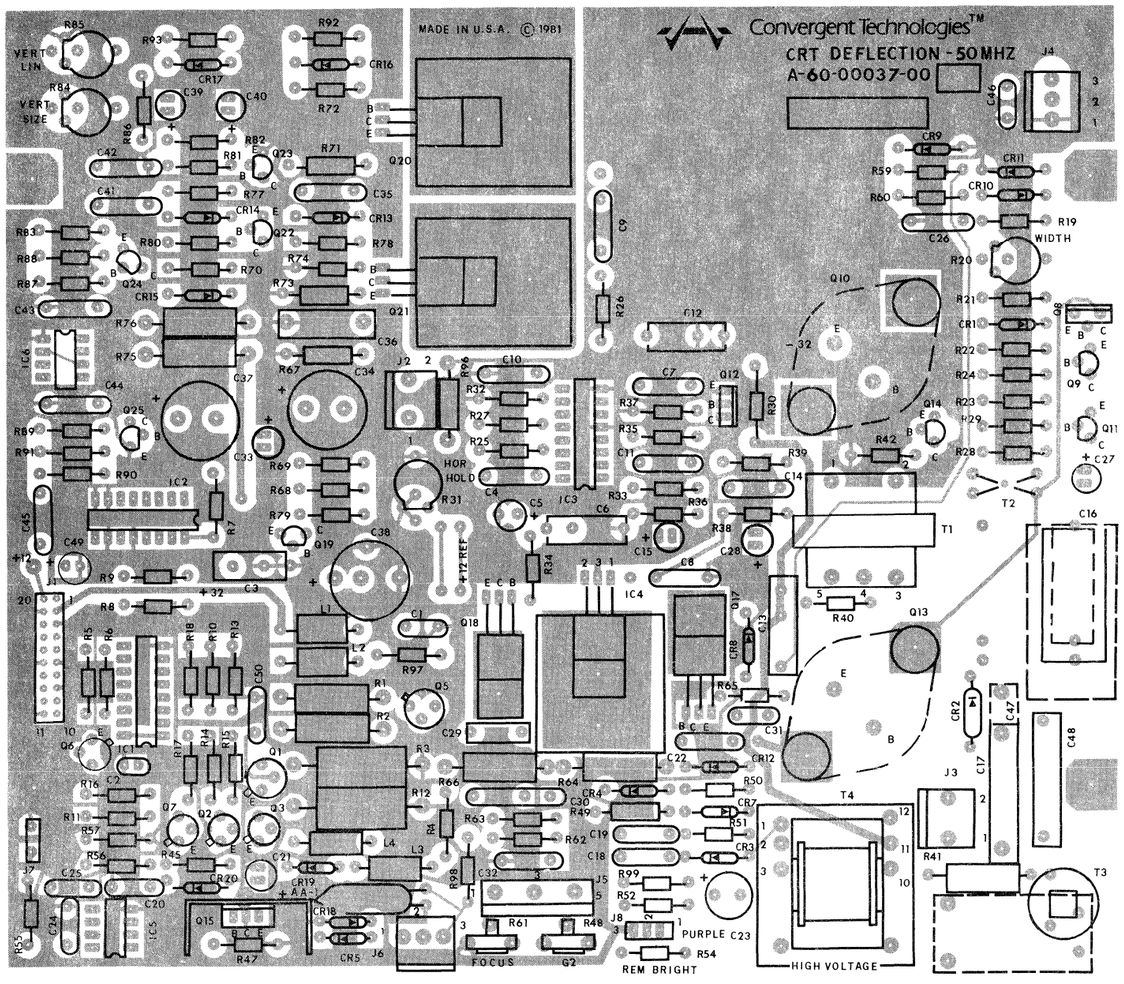

Figure 10-3. CRT-Deflection Assembly Drawing

POWER AND GROUND LOCATOR CHART					
REF. DES	TYPE	GND	+5V	+12V	-5V
IC5	LM358	4		8	
IC2	26LS32	7,10,8,12	16		
IC3	14040B	5,8			
IC6	555	1		8	
IC1	10116	8	1,16		

J1

+12V	20	1 — -32V
GND	19	2 — +32V
	18	3 — GND
V.DRIVE-	17	4 — H.DRIVE-
V.DRIVE+	16	5 — H.DRIVE+
GND	15	6 — GND
KEY	14	7 —
VIDEO B-	13	8 — GND
VIDEO B+	12	9 — VIDEO A-
GND	11	10 — VIDEO A+

REF. DESIGNATORS	
LAST USED	NOT USED
C50	
R99	
CR20	
IC6	
L4	
AA-1	
Q25	
T4	
J8	
HS4	

NOTES:

UNLESS OTHERWISE SPECIFIED:

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, 5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.

APPENDIX C

WORKSTATION SWITCH AND JUMPER SETTINGS

CPU BOARD SWITCHES

The functions of each of the switches on the CPU board are listed below.

S1

Bit	On	Off
1	4 MHz DMA	5 MHz DMA
2	no wait states	one wait state
3	not used	not used
4	5 MHz 8086	3.3 MHz 8086

S2

1	Multibus-to-CT window at 512K	no Multibus-to-CT window at 512K
2	not used	not used
3	not used	not used
4	no Multibus-to-CT window at 32K	Multibus-to-CT window at 32K

S3

1	CT-to-Multibus window at 512K	CT-to-Multibus window at 768K
2	CT-to-Multibus window at 768K	CT-to-Multibus window at 512K
3	CT generates CCLK-	external CCLK-generation
4	CT generates BCLK-	external BCLK-generation

S4

1	640K RAM total	128K RAM total 256K RAM total 384K RAM total 512K RAM total
2	128K RAM total	256K RAM total 384K RAM total 512K RAM total 640K RAM total
3	128K RAM total 256K RAM total 512K RAM total	384K RAM total 640K RAM total

Bit	On	Off
4	128K RAM total 256K RAM total 384K RAM total	512K RAM total 640K RAM total

S5

1	2732 PROMs	2716 PROMs
2	2716 PROMs	2732 PROMs
3	not used	not used
4	not used	not used

S6

1	no PROM board	PROM board
2	PROM board	no PROM board
3	no CT-to-Multibus access	CT-to-Multibus access enabled
4	CBRQ- always asserted	CBRQ- from Multibus master

CPU BOARD JUMPERS

For workstations without 8087 coprocessors, a jumper from TP6 to ground must be installed. If an 8087 is used, there must be no jumper installed.

I/O-MEMORY BOARD SWITCHES

The functions of each of the switches on the I/O-Memory board are listed below.

S1

Bit	On	Off
1	Channel A external transmit clock	Channel A internal transmit clock
2	Channel A external receive clock	Channel A internal receive clock
3	Channel A internal transmit clock	Channel A external transmit clock
4	Channel A internal receive clock	Channel A external receive clock
5	Channel B external transmit clock	Channel B internal transmit clock
6	Channel B external receive clock	Channel B internal receive clock
7	Channel B internal transmit clock	Channel B external transmit clock
8	Channel B internal receive clock	Channel B external receive clock

S2

ID switch: For workstations with serial number A-8131A-0400 or lower, see the "Bootstrap ROM" section in the second edition (A-09-00014-02-A) of the System Programmer's Guide. For workstations with serial number A-8131B-0400 or higher, see the Release Notice for Common Boot ROM Firmware (A-09-00065-01-A).

S3

Bit	On	Off
1	internal carrier detect	external carrier detect
2	external carrier detect	internal carrier detect
3	not used	not used
4	not used	not used

I/O-MEMORY BOARD JUMPERS

For Channel A RS-232 operation, jumper plugs must be installed in JP2 and JP4 and not in JP1 and JP3.

For Channel A RS-422 operation, jumper plugs must be installed in JP1 and JP3 and not in JP2 and JP4.

I/O-Memory board jumper E-F must be installed for 16K RAM chip operation.

RAM EXPANSION BOARD JUMPERS

If a 128K RAM Expansion Board is included, jumper A-C must be installed for 16K RAM operation.

MOTHERBOARD JUMPERS

A jumper plug must be installed in motherboard location U3 for cluster communications operation. This connects the 9-pin cluster communications connectors and protection diodes to Channel A. For workstations with a switch in U3, all 8 bits must be on.

For noncluster Channel A use, there must be no jumper plug in location U3, or if there is a switch, all 8 bits must be off.

FACTORY CONFIGURATION 1

The following configuration constitutes a dual RS-232 workstation. It is the Convergent factory setting for workstations with the following serial numbers:

8034A-00051 - 8034A-00093
8034A-00096 - 8034A-00099
8034A-00102 - 8034A-00106
8034A-00110 - 8106A-00122

CPU

bit	S1	S2	S3	S4	S5	S6
1	on	off	on	*	off	off
2	on	off	off	*	on	on
3	off	off	on	*	off	off
4	on	on	on	*	off	on

* See switch S4 on p. D-1 for the settings for different memory boards

I/O Memory

bit	S1	S2	S3
1	off	on	off
2	off	on	on
3	on	on	off
4	on	on	off
5	off	on	
6	off	on	
7	on	on	
8	on	on	

CPU jumper TP6 to ground is installed.

I/O-Memory jumper E-F is installed.

I/O-Memory jumper plugs JP2 and JP4 are installed; JP1 and JP3 are not installed.

RAM expansion jumper A-C is installed.

Motherboard jumper plug is not installed in U3.

FACTORY CONFIGURATION 2

The following configuration constitutes a Channel A cluster RS-422 and Channel B RS-232 workstation with 2716 bootstrap ROMs. It is the Convergent factory setting for workstations with the following serial numbers:

8034A-00094 - 8034A-00095
8034A-00100 - 8034A-00101
8034A-00107 - 8034A-00109
8106A-00123 - 8131A-00399

	CPU					
bit	S1	S2	S3	S4	S5	S6
1	on	off	on	*	off	off
2	on	off	off	*	on	on
3	off	off	on	*	off	off
4	on	on	on	*	off	on

* See switch S4 on p. D-1 for the settings for different memory boards.

	I/O Memory			
bit	S1	S2		S3
		Master	Cluster Workstation	
1	off	on	on	on
2	on	on	on	off
3	off	on	off	off
4	on	on	on	off
5	off	on	on	
6	off	on	on	
7	on	on	on	
8	on	on	off	

CPU jumper TP6 to ground is installed.

I/O-Memory jumper E-F is installed.

I/O-Memory jumper plugs JP1 and JP3 are installed; JP2 and JP4 are not installed.

RAM expansion jumper A-C is installed.

Bits 1-8 of motherboard switch U3 are On.

FACTORY CONFIGURATION 3

The following configuration constitutes a Channel A cluster RS-422 and Channel B RS-232 workstation with 2732 bootstrap ROMs. It is the Convergent factory setting for workstations with the following serial numbers:

8131B-00400 and up.

	CPU					
bit	S1	S2	S3	S4	S5	S6
1	on	off	on	*	on	off
2	on	off	off	*	off	on
3	off	off	on	*	off	off
4	on	on	on	*	off	on

* See switch S4 on p. D-1 for the settings for different memory boards.

	I/O Memory		
bit	S1	S2	S3
1	off	off	on
2	on	on	off
3	off	off	off
4	on	off	off
5	off	on	
6	off	on	
7	on	on	
8	on	off	

CPU jumper TP6 to ground is installed.

I/O-Memory jumper E-F is installed.

I/O-Memory jumper plugs JP1 and JP3 are installed; JP2 and JP4 are not installed.

RAM expansion jumper A-C is installed.

Bits 1-8 of motherboard switch U3 are On.