AWS-220, -230, -240 Hardware Manual

Volume 2

Convergent Technologies

AWS-220, -230, -240 HARDWARE MANUAL

Volume 2

Specifications Subject to Change.

First Edition (April, 1982) A-09-00112-01-A

CONTENTS: VOLUME 2

LIST OF FIGURES

LIST OF TABLES

CONTENTS: VOLUME 1

CONTENTS: VOLUME 1

LIST OF FIGURES

LIST OF TABLES

4 EXTERNAL INTERFACES

INTRODUCTION

This section discusses specific hardware or software interface characteristics of the keyboard, printer, and RS-232-C communications interfaces used on the AWS-220, -230, and -240.

The discussion of each major interface includes a description of the signals, software and hardware information, cabling diagrams, and electrical characteristics.

Some of the information contained in this section, along with more detailed discussions of the external interface logic, is also contained in the "Architecture" and "Theory of Operation" sections.

KEYBOARD INTERFACE

The interface used for communications between each of the AWS-220, -230, and -240 workstations and its keyboard is bidirectional, asynchronous, and serial, operating at a rate of about 1200 baud. Transmission to the keyboard is used for lighting keyboard LEDs and for diagnostic commands. Transmission from the keyboard indicates keyboard status and is also used for diagnostic tests. A reset line is included in the interface, which is activated by either a power-up or manual reset. Power supplied to the keyboard from the workstation's power supply is +5 V dc.

Interface Signals

The following signals are used with the keyboard interface:

Signal	Meaning
KBDO-	Asynchronous serial output data from the workstation to the keyboard. A TTL high signal indicates a 0 data bit or start bit; a TTL low signal indicates no data, a stop bit, or a 1 data bit.
KBDI-	Asynchronous serial input data to the workstation from the keyboard. A TTL high signal indicates a 0 data bit or start bit; a TTL low signal indicates no data, a stop bit, or a 1 data bit.
INIT-	A reset signal to the keyboard. INIT- is issued from the workstation upon either a power-up or manual reset.
VCC+	+5 V dc power to the keyboard from the workstation.

Data is transmitted on the KBDO- and KBDI- lines in standard asynchronous data communications bit protocol. When data transmission is not in progress, KBDO- and KBDI- are both low. At the beginning of a byte transfer, KBDO- or KBDI- is set high for a single bit interval (the start

bit) before sending eight bits of data, low-order bit first. After the eight data bits are transmitted, KBDO- or KBDI- is set low for at least one bit interval (the stop bit) before another byte is sent.

Software Interface

Software communicates with the keyboard through one channel of an NEC 7201 on the 8088 or 8086 CPU Board. Complete programming information for the 7201 is given in the "Architecture" section under "Keyboard and Keyboard Communications."

Interrupts

The keyboard interface can be serviced by software status polling or by interrupts. If interrupts are used, the interrupt vector is issued through the 7201 on the CPU Board.

Byte Protocol

A general summary of the byte protocol for the keyboard software is as follows.

- When a key changes state (up or down) the present keyboard status, a list of all keys currently down, is sent from the keyboard.
- If no keys are down (when the last key is released), a special code (C0h) is sent to the 7201 to indicate that all keys are up.

This protocol is extremely flexible since it allows any type of chording that the system software can provide. In particular, it allows any key, or combination of keys, to be shifted to alter the meaning of the key or keys. The keys labled SHIFT on the AWS-220, -230, or -240 keyboard have no special meaning within the keyboard; they are decoded like any other keys. The keys on the keyboard are assigned as follows:

Keyboard Code (hexadecimal)	Key
00	HELP
01	up arrow
02	MARK
03	BOUND
04	FINISH
05	PREV PAGE
06	1/2
07	CANCEL
08	BACKSPACE
09	TAB
0A	RETURN
0B	down arrow
0C	NEXT PAGE
0D	NEXT
0E	left arrow
0F	right arrow
10	(SH-L')
11	SCROLL UP
12	MOVE
13	SCROLL DOWN
14	COPY
15	f1
16	f2
17	f3
18	f4
19	f5
1A	f6
1B	GO
1C	f7
1D	f8
1E	f9
1F	f10
20	space
21	number 9
22	(SH-R')
23	(0')
24	(NEXT')
25	unused code
26	unused code
27	' (single quote)
28	unused code
29	unused code
2A	unused code
2B	= (equals sign)
2C	, (comma)
2D	- (hyphen)
2E	. (period)
2F	/
30...39	numbers 0...9
3A	unused code

Keyboard Code (hexadecimal)	Key
3B	;
3C	unused code
3D	unused code
3E	unused code
3F	invalid code
40	indicates last key released; always has high bit on (that is, 0C0h)
41	number 6
42	number -
43	ACTION
44	OVERTYPE
46	number 2
47	number 3
48	left SHIFT
49	right SHIFT
4E...5A	unused codes
5B	[
5C	number 7
5D	]
5E	^ (caret)
5F	unused code
60	number 1
61...7A	a...z
7B	number 4
7C	number 8
7D	number 5
7E	unused code
7F	DELETE

The LEDs on the keyboard are assigned as follows:

LED	Key	Legend
LED0	17	f10
LED1	16	f9
LED2	15	f8
LED3	10	f3
LED4	9	f2
LED5	8	f1
LED6	63	LOCK
LED7	62	OVERTYPE

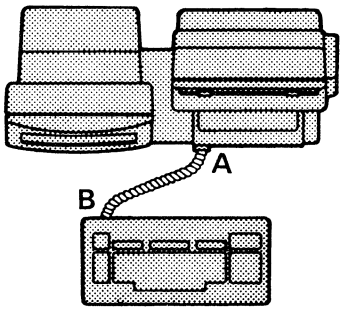
Cabling

This subsection details the assembly of cables for the keyboard interface.

Assembly: Keyboard Cable

Function: Connects keyboard to mainframe of the workstation

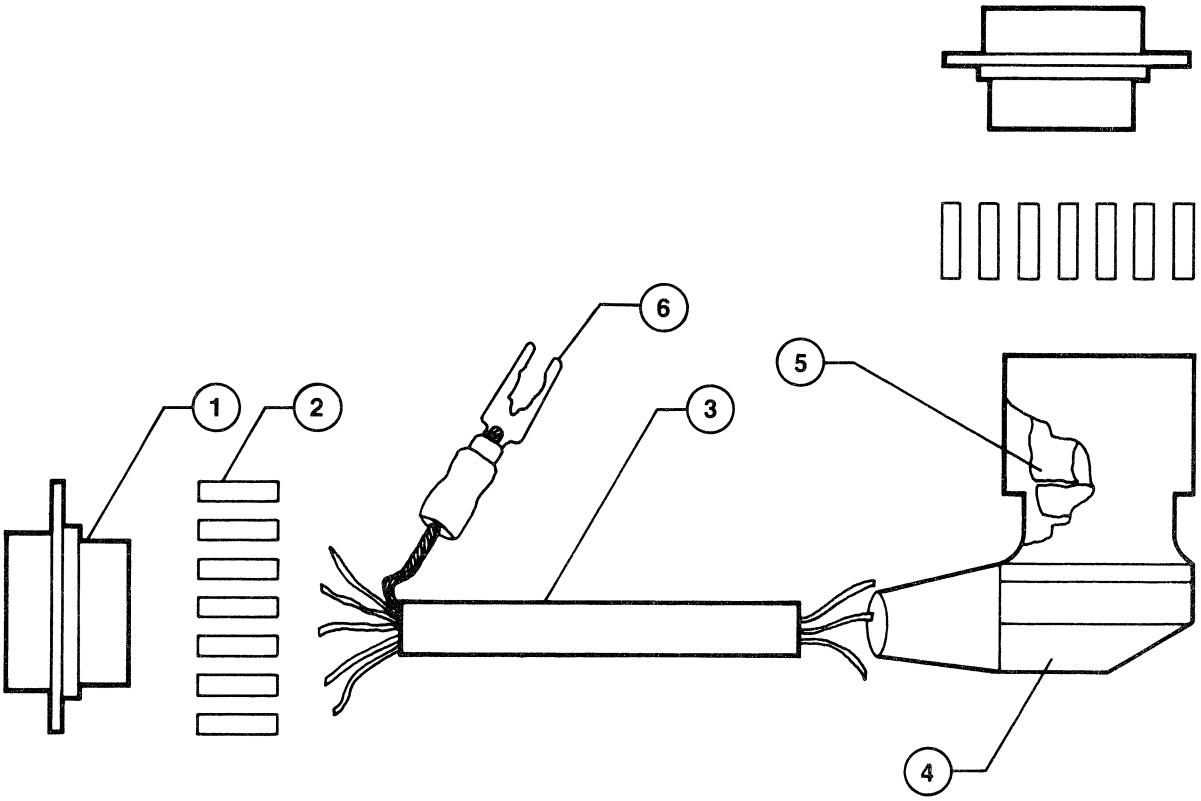
Connection:



Pinouts:

A Workstation	B Keyboard	Assignments
1	1	KBDI-
2	2	Ground
3	3	KBDO-
4	4	Ground
5	5	INIT-
6	6	VCC+
7	7	VCC+
8	8	Ground
9	9	Ground

Construction:



Item	Quan.	Description
1.	2	9-Pin D-type plug housing (male). Use Amphenol #17-91090-18 or equivalent.
2.	18	Crimp pin contacts. Use Amphenol #17-1392-04-150 or equivalent
3.	1 ft (0.3 m)	9-conductor shielded cable. Use Belden #YH9457 or equivalent.
4.	2	Molded PVC backshell. Use Belden #EX-80CON-019 or equivalent.
5.	as req.	Copper tape. Use 3M #1425.
6.	1	Spring spade terminal. Use Amp #52453-1.

Note: The minimum length of this cable is 1 ft (0.30 m); the maximum length is 5 ft (1.5 m).

The power supply for the AWS-220, -230, and -240 can supply 0.7 A at +5 V dc to the keyboard. Be sure, when making cables, that all the conductors in the keyboard cable are large enough to provide the proper power supply level required by the keyboard.

DC Characteristics

Signal	Driver	Voh/Vol	Ioh/Iol
KBD0-	74LS240	2.4/0.5	3.0 ma/24 ma
INIT-	74LS240	2.4/0.5	3.0 ma/24 ma

Signal	Driver	Voh/Vol	Ioh/Iol
KBDI-	74LS240	2.0/0.8	0.02 ma/0.20 ma

AC Characteristics

Signal	Baud Rate
KBDO-	1200 + or - 1%
KBDI-	1200 + or - 5%

RS-232-C COMMUNICATIONS INTERFACE

The AWS-220, -230, and -240 workstations provide two programmable RS-232-C communications ports, which are similar in operation to the Channel B port on the IWS workstation. An NEC 7201 (Intel 8274) Multi-Protocol Serial Controller (MPSC) is used to control the two ports and provides bit synchronous, byte synchronous, or asyncronous communications at baud rates of from 50 to 19.2 kilobaud. The RS-232-C communicaitons ports are interrupt-controlled through the 8259A on the FDC or HDC Board.

The RS-232-C communications ports operate as Data Terminal Equipment (DTE) as specified in the EIA RS-232-C Standard, published by the Electronic Industries Association. Both of the RS-232-C communications ports can be directly connected to Data Communications Equipment (DCE) or, with a crossed cable, to other types of Data Terminal Equipment. Cabling information is given below.

Interface Signals

The following signals are supported by the two RS-232-C communications ports:

Name (and Direction)	EIA Designation	Pin Number/Meaning
Transmit Data (out)	BA	Pin 2. Data transmitted to the DCE. This signal is held high if data is not being transmitted.
Secondary Transmit Data (out)	SBA	Pin 14. Same as Transmit Data but for the secondary channel.
Request to Send (out)	CA	Pin 4. A transition from 0 to 1 tells the DCE to enter the transmit mode. The DCE responds by activating its Clear to Send line.

Name (and Direction)	EIA Designation	Pin Number/Meaning
Data Terminal Ready (out)	CD	Pin 20. Indicates to the DCE that the communications port is on line and ready to operate.
Receive Data (in)	BB	Pin 3. Data received by the DTE. This signal is held in a binary one condition if data is not being received.
Secondary Receive Data (in)	SBB	Pin 16. Same as Receive Data but for the secondary channel.
Clear to Send (in)	CB	Pin 5. Indicates to the communications port that the DCE is ready to transmit data.
Data Set Ready (in)	CC	Pin 6. Indicates to the communications port that the DCE is online and ready to operate.
Carrier Detect (in)	CF	Pin 8. Indicates to the communications port that a signal is being received.
Ring Indicator (in)	CE	Pin 22. Indicates to the communications channel that a ringing signal is being received.
External Transmit Clock (in)	DB	Pin 15. Transmit clock from DCE.
External Receive Clock (in)	DD	Pin 17. Receive clock from DCE.

The Secondary Transmit Data and Secondary Receive Data lines are not controlled by the 8274.

Instead, these lines are controlled by the CPU when it writes data to Port A4h, the Extended Control Register.

Software Interface

Software communicates with either of the RS-232-C communications ports through the following input/output ports:

Port	Device	Read	Write
A8h	7201	Port A data	Port A data
A9h	7201	Port A status	Port A command
AAh	7201	Port B data	Port B data
ABh	7201	Port B status	Port B command
ADh	8253	Port B baud rate	Port B baud rate
AEh	8253	Port A baud rate	Port A baud rate
AFh	8253	8253 mode	---
A4h	General	Extended communication status	Extended control

Ports A8h and AAh

Ports A8h and AAh are the Data Registers for RS-232-C Ports A and B, respectively. Ports A8h and AAh can be read from or written to when the RS-232-C Port is receiving or transmitting data, respectively.

Register AL Bit (CPU)	Read Information
0-7	Receive data bits 0-7.

Register AL Bit (CPU)	Write Information
0-7	Transmit data bits 0-7.

Ports A9h and ABh

Each of the two RS-232-C communications ports has a set of three status (read) registers and eight

command (write) registers. The CPU transfers information to and from these registers by input/output Ports A9h (for RS-232-C Port A) and ABh for RS-232-C Port B). Since the 7201 uses the 8259A to send an interrupt vector to the CPU, Port ABh Write Register 2 of the 7201 is not used. The Pointer Register bits at Write Register 0 for both Ports A9h and ABh selects which read or write register is accessed when Ports A9h and ABh are used. When either a manual or power-up reset occurs, the Pointer Register is set to 0. Any read or write to Ports A9h and ABh then accesses Read Register 0 or Write Register 0, respectively and are programmed when Write Register 0 is written to. The Pointer Register bits are reset to 0 after any command or status access is made to a read or write register other than 0.

For example, to access Read Register 2, a 2 is written as the Pointer Register code to Write Register 0. The next read accesses Read Register 2. The hierarchy of registers in the 7201 is shown in Figure 2-4 in the "Architecture" section, above. The format of the registers is given in the "Architecture" section under "Cluster Communications."

Ports ADh, AEh, and AFh

Ports ADh, AEh, and AFh, used for setting the baud rate for RS-232-C Channels A and B and the counter mode, are described in the "Architecture" section under "8253 Counter Timer" above.

Port A4h

Port A4h, the extended control and status port, is used to provide several communications signals not directly supported by the 7201.

EXTENDED COMMUNICATIONS CONTROL REGISTER

Register AL Bit (CPU)	Write Information
0	Secondary Transmit (Channel B)
1	Secondary Transmit (Channel A)
2-3	Unused by RS-232-C communications channels. These bits can be 1 or 0.
4	RS-232-C Channel B synchronous (external clocking)
5	RS-232-C Channel A synchronous (external clocking)
6	Unused
7	Unused by RS-232-C communications channels. This bit can be 1 or 0.

EXTENDED COMMUNICATIONS STATUS REGISTER

Register AL Bit (CPU)	Read Information
0	Secondary Receive Data (Channel B)
1	Data Set Ready (Channel B)
2	Ring Indicator (Channel B)
3	Secondary Transmit Data (Channel B)
4	Secondary Receive Data (Channel A)
5	Data Set Ready (Channel A)
6	Ring Indicator (Channel A)
7	Secondary Transmit Data (Channel A)

Interrupts

When one of the RS-232-C communications channels interrupts the CPU, it does so through the Intel 8259A Interrupt Controller on the FDC or HDC Board. The INT- (Interrupt) line of the 7201 is sent through an inverter to the 8259A as INT3+. When an interrupt is requested, the 8259A asserts its INT- line to the CPU to request service. The CPU acknowledges the interrupt with two INTA- pulses. When the first INTA- pulse occurs, the 8259A resolves the priority of the interrupt from the RS-232-C communications channels and four other interrupt sources. When the second INTA- pulse occurs, the 8259A sends a unique interrupt vector to the CPU for the RS-232-C channel. After receiving the interrupt vector, the CPU jumps to a service routine for the interrupting device.

Cabling

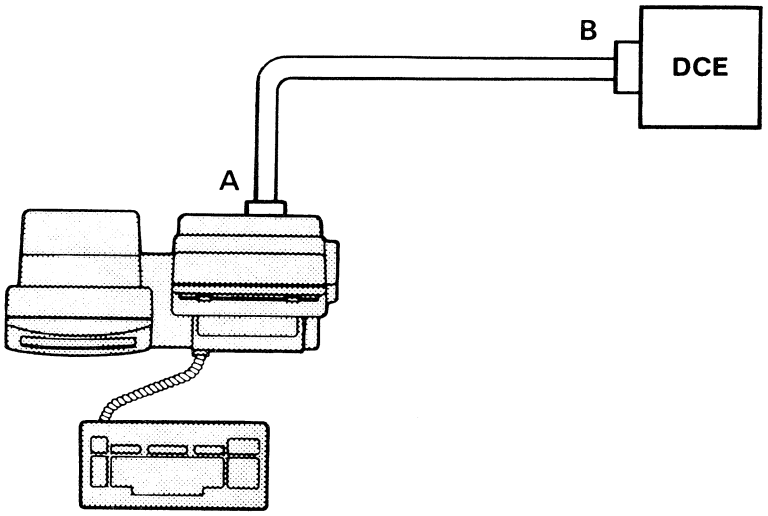
There are two types of RS-232-C cables that can be connected to either RS-232-C communications channel: straight, and crossed. A straight cable is used to connect Data Terminal Equipment (DTE), such as a workstation to Data Communications Equipment (DCE), such as a modem.

A crossed cable connects two DTEs, such as a workstation and a terminal. The control and data lines are crossed so that a null modem is presented to each of the DTEs. The cabling details are shown below.

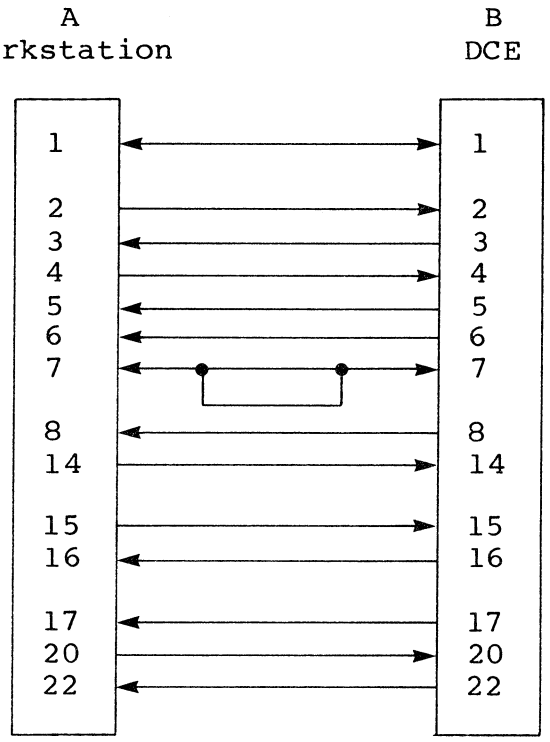
Assembly: Straight Cable for RS-232-C Communications

Function: Connects workstation to Data Communications Equipment (DCE).

Connection:



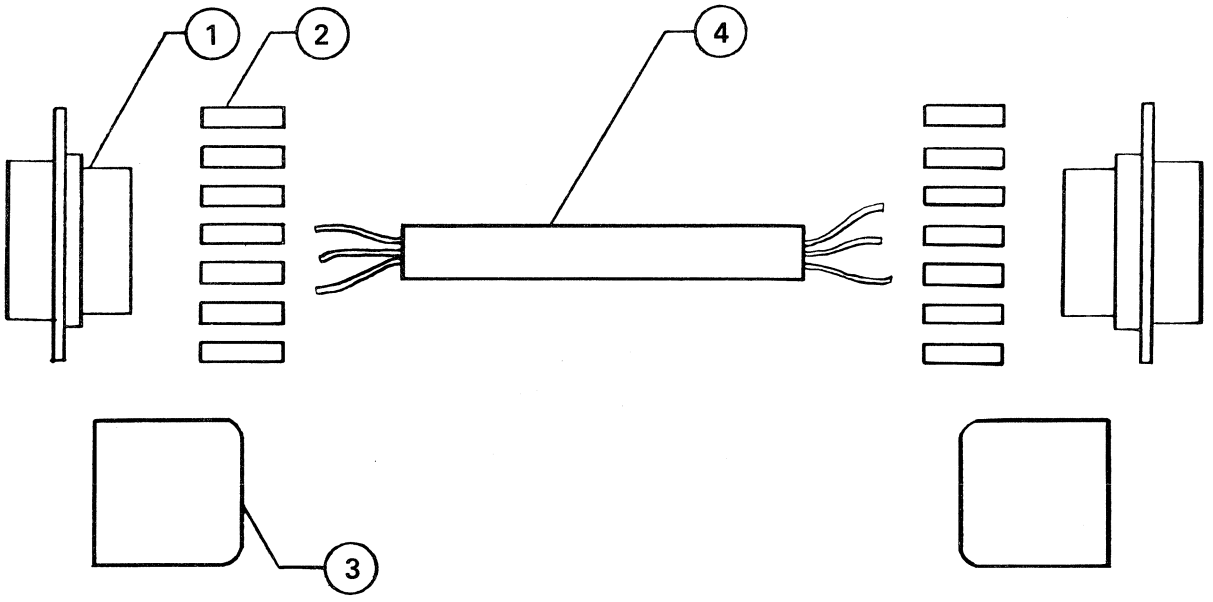
Pinouts:



Assignments

1	Protective Ground (shield)
2	Transmit Data
3	Receive Data
4	Request To Send
5	Clear To Send
6	Data Set Ready
7	Signal Ground (Spare Conductor)
8	Carrier Detect
14	Secondary Transmit Data
15	Transmit Clock
16	Secondary Receive Data
17	Receive Clock
20	Data Terminal Ready
22	Ring Indicator

Construction:



Item	Quan.	Description
1.	2	25-Pin D-type plug assemblies (male). Use Amp #205208-1 or equivalent.
2.	30	Connector contacts. Use Amp #66507-3 or equivalent.
3.	2	Connector shell and strain reliefs Use Amp #207908-7 or equivalent.
4.	25 ft (7.62 m)	15-conductor shielded cable. Use Belden #9541 or equivalent.

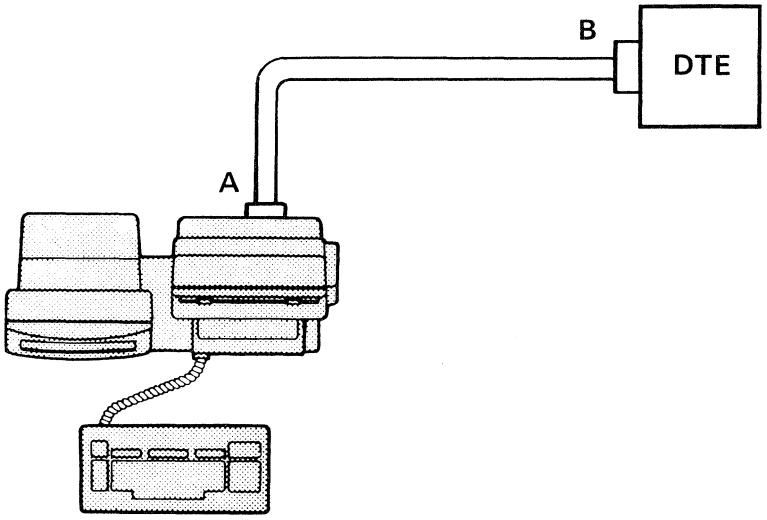
Pin 1 must be attached to the shield drain wire at both ends. Also, the additional conductor in this cable must be terminated to signal ground (pin 7) at both ends.

Note: The minimum length of this cable is 25 ft (7.62 m); the maximum length is 50 ft (15.2 m).

Assembly: Crossed Cable for RS-232-C Communications

Function: Connects workstation to Data Terminal Equipment (DTE)

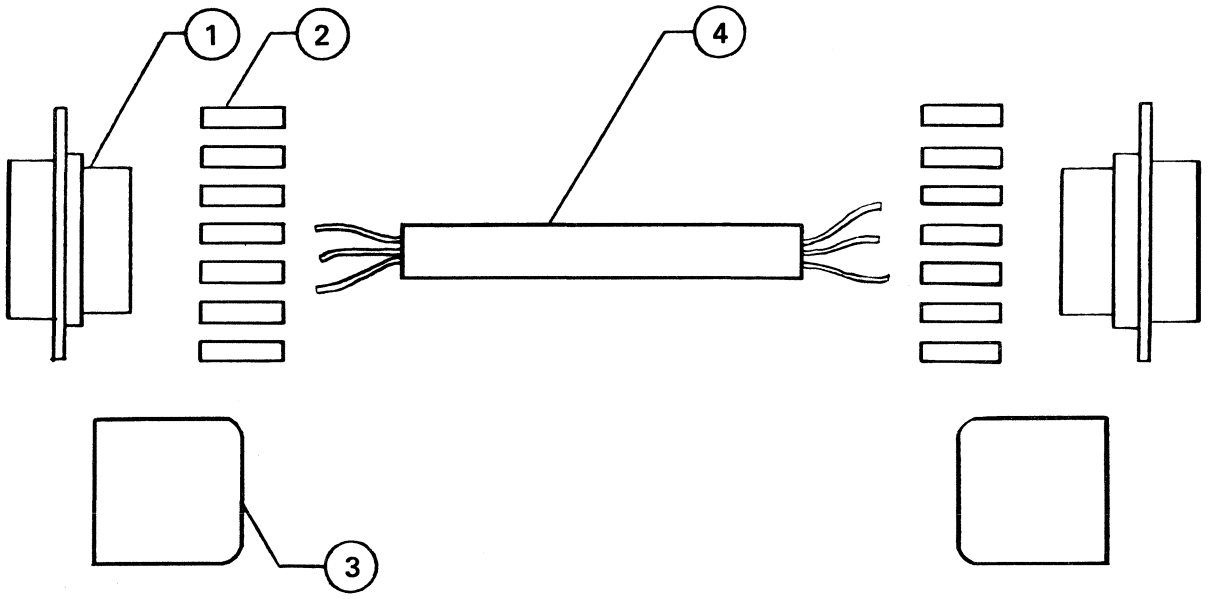
Connection:



Pinouts:

Assignments	A Workstation	B DTE	Assignments
Protective Ground (shield)	1	1	Protective Ground (sheild)
Transmit Data	2	3	Receive Data
Receive Data	3	2	Transmit Data
Request To Send	4	4	Request to Send
Clear To Send	5	5	Clear to Send
Signal Ground	7	7	Signal Ground
Data Set Ready	6	6	Data Set Ready
Carrier Detect	8	8	Carrier Detect
Data Terminal Ready	20	20	Data Terminal Ready

Construction:



Item	Quan.	Description
1.	2	25-pin D-type plug assemblies (male). Use Amp #205208-1 or equivalent.
2.	18	Connector contacts. Use Amp #66507-3 or equivalent.
3.	2	Connector shell and strain reliefs. Use Amp #207908-7 or equivalent.
4.	25-ft (7.62 m)	3-conductor shielded cable. Use Belden #9533 or equivalent.

Pin 1 must be connected to the shield drain wire at both ends.

Note: The minimum length of this cable is 25 ft (7.62 m); the maximum length is 50 ft (15.2 m).

PRINTER INTERFACE

The parallel printer interface on the AWS-220, -230, or -240 provides a Centronics-compatible interface to parallel-interface printers. For connection to serial printers, one of the two RS-232-C communications channels can be used.

Interface Signals

The printer interface supports the following signals:

Name	Meaning
LPT0+-LPT7+	Eight bits of data sent from the workstation to the printer. Generally, only seven bits are used.
STROBE-	A handshake line from the workstation to the printer. A low STROBE- signal indicates that data is present on the LPT0+-LPT7+ lines and should be accepted by the printer.
LPTACK-	An acknowledge signal from the printer to the workstation indicating that a character has been accepted and that another one can be sent.
LPTBUSY+	A status line to the workstation indicating that the printer cannot currently accept data. Generally, this signal goes high only when the printer is making some other type of mechanical motion.
NOPAPER+	A status line to the workstation indicating that the printer is out of paper.
LPTSELECT+	A status line to the workstation indicating that the printer is selected, has paper, and is ready to print.

The signals LPTBUSY+, NOPAPER+, and LPTSELECT+ are status bits only; they have no other effects on the printer interface hardware. These bits are sent to an input port and are handled exclusively by software.

The signal LPTACK- is not directly readable by software and has direct hardware effects (see "Printer Logic" below).

The signal STROBE- is generated by the workstation hardware whenever a program sends data to the printer data port.

Software Interface

Software communicates with the parallel printer interface through the Printer Control and Status Port B0h.

An output instruction from the CPU to Port B0h causes eight bits of data on the LPT0+-LPT7+ lines to go to the printer. It also generates a STROBE- signal, which causes the printer to accept the data. In addition, the BUFBUSY+ flip-flop is set in the hardware and remains set until the printer generates the LPTACK- strobe, which resets BUFBUSY+. BUFBUSY+ can be sensed either by an interrupt or by a program reading Port B0h.

An input instruction to Port B0h sends four bits of status information to the CPU. The status bits sent to the CPU are:

Register AL Bit (CPU)	Read Information
0	LPTBUSY+ (Line Printer Busy). If 1, the printer is either printing or making some other type of mechanical motion.
1	SELECT+ (Printer Selected). If 1, the printer is online and ready to receive data.
2	BUFBUSY+ (Buffer Busy). If 1, this line indicates that the printer has not yet acknowledged a character. If 0, The printer is waiting for another character to be sent.

Register AL Bit (CPU)	Read Information
3	NOPAPER+ (No Paper). If 1, the printer is out of paper.
4-7	Unused

Interrupts

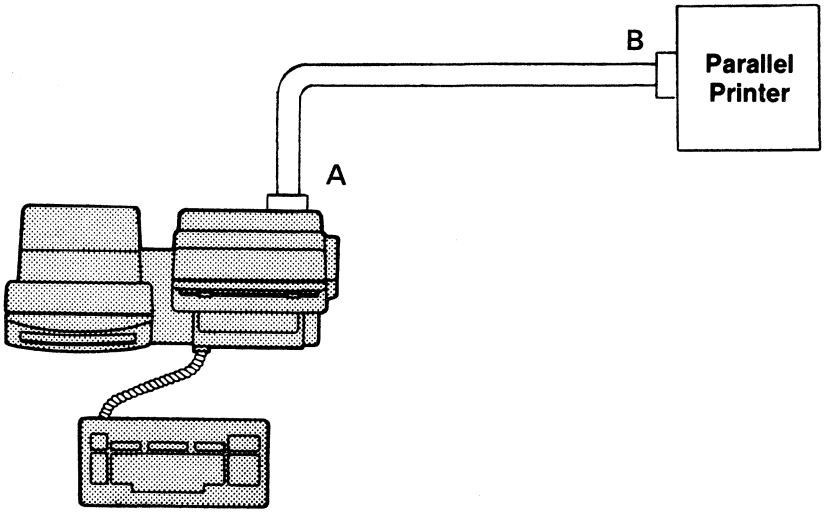
In the AWS-220, -230, and -240, the BUFBUSY+ flip-flop is directly connected to interrupt level 4 of the 8259A interrupt controller. The interrupt can be masked within the 8259A. When BUFBUSY+ is not set, the printer interface requests an interrupt. Generally, the printer drive program determines when mechanical motion is taking place and allows interrupts from the printer via the 8259A mask.

Cabling

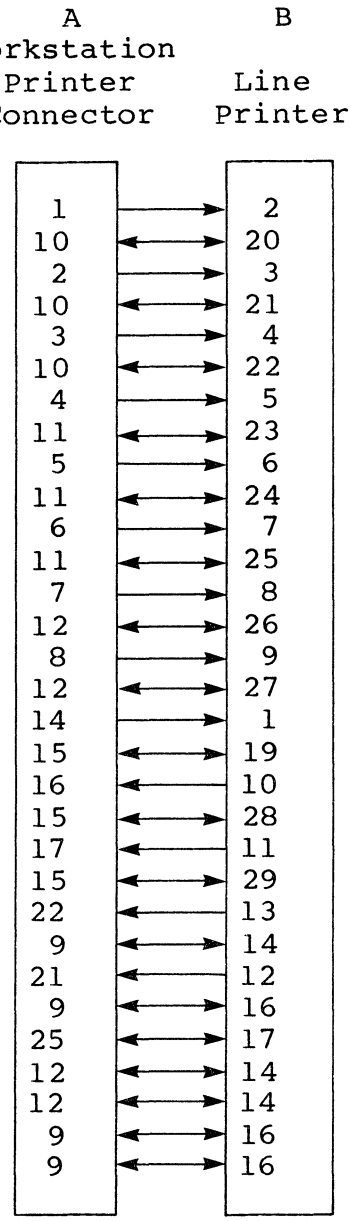
Assembly: Parallel Printer Interface Cable

Function: Connects workstation to Centronics-interface line printer

Connection:

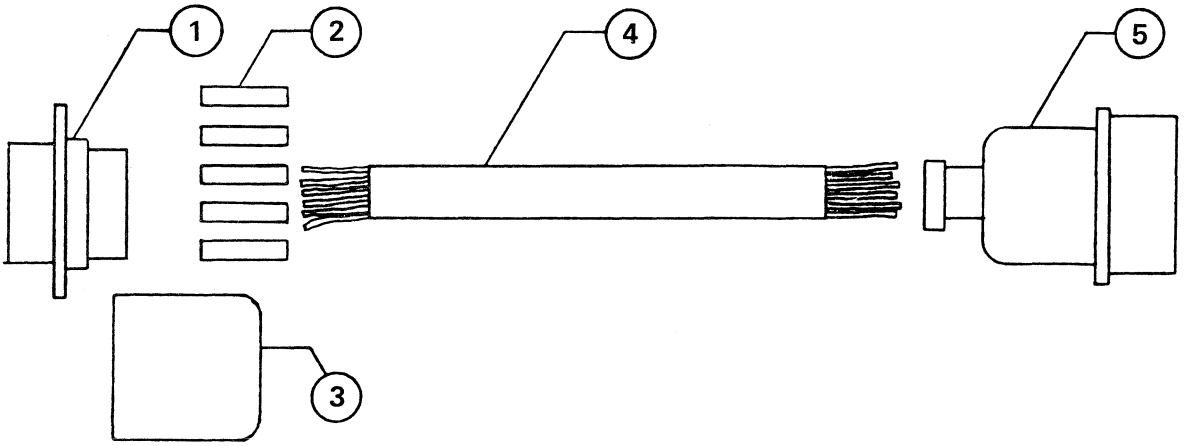


Pinouts:



Assignment
LPTØ+
GND
LPT1+
GND
LPT2+
GND
LPT3+
GND
LPT4+
GND
LPT5+
GND
LPT6+
GND
LPT7+
GND
STROBE-
GND
LPTACK-
GND
LPTBUSY+
GND
LPTSELECT+
GND
NOPAPER+
GND
CHASSIS GND (shield)
GND (spare conductor)
GND (spare conductor)
GND (spare conductor)
GND (spare conductor)

Construction:



Item	Quan.	Description
1.	1	25-pin D-type plug assembly (male). Use Amp #205208-1 or equivalent.
2.	25	Connector contacts. Use Amp #66507-3 or equivalent.
3.	1	Connector shell and strain relief. Use Amp #207908-7 or equivalent
4.	10-ft (3.0 m)	(or 30-conductor) twisted pair shielded cable. Use Belden #9515 or equivalent
5.	1	36-pin "Blue Ribbon" type connector assembly (male). Use Amphenol #57-30360 or equivalent.

The chassis ground must be connected to the shield drain wire at both ends.

A twisted pair consists of a signal and a ground, that is, DATAØ+ (workstation pin 1) and ground (workstation pin 10).

All four unused conductors must be connected to a ground at both ends.

The vinyl insulation must be stripped back at the 36-pin printer connector so that the metal strain relief clamps down on the conducting shield.

Note: This cable must be 10 ft (3.0 m) minimum. Longer lengths must be approved by the printer manufacturer.

DC Characteristics

Signal	Driver	Voh/Vol	Ioh/Iol
LPT0+-LPT7+	74LS373	2.4/0.5	2.6 mA/24 mA
STROBE-	74LS244	2.4/0.5	3.0 mA/24 mA

Signal	Receiver	Vih/Vil	Iih/Iil
LPTBUSY+	74LS244	2/0.8	0.02 mA/4.8 mA *
LPTSELECT+	74LS244	2/0.8	0.02 mA/4.8 mA *
NOPAPER+	74LS244	2/0.8	0.02 mA/4.8 mA *
LPTACK+	7414	2/0.6	0.04 mA/5.8 mA *

* Includes a 1-kilohm pullup resistor

AC Characteristics

Also see the timing diagram, Figure 4-1, below.

Parameter	Term	Time
T_{DS}	Data setup time to STROBE-	1.0 μs min
T_{SW}	Strobe width	1.5 μs min 1.7 μs max
T_{DH}	Data hold time after STROBE-	5.0 μs min
T_{AW}	Acknowledge width	0.1 μs min

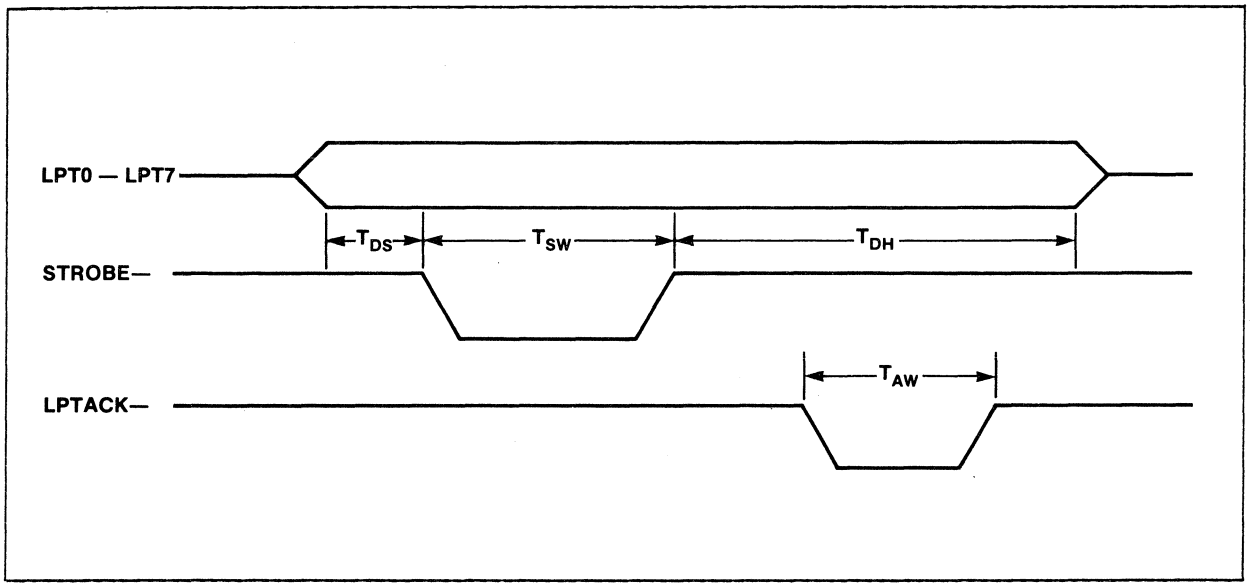


Figure 4-1. Keyboard Timing Diagram.

APPENDIX A: 8086/8088 INSTRUCTION SET

Control Transfer

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
CALL = Call:			
Direct within segment	1 1 1 0 1 0 0 0	disp-low	disp-high
Indirect within segment	1 1 1 1 1 1 1 1	mod 0 1 0 r/m	
Direct intersegment	1 0 0 1 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 0 1 1 r/m	
JMP = Unconditional Jump:			
Direct within segment	1 1 1 0 1 0 0 1	disp-low	disp-high
Direct within segment-short	1 1 1 0 1 0 1 1	disp	
Indirect within segment	1 1 1 1 1 1 1 1	mod 1 0 0 r/m	
Direct intersegment	1 1 1 0 1 0 1 0	offset-low	offset-high
		seg-low	seg-high
Indirect intersegment	1 1 1 1 1 1 1 1	mod 1 0 1 r/m	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1		
Within seg adding immed to SP	1 1 0 0 0 0 1 0	data-low	data-high
Intersegment	1 1 0 0 1 0 1 1		
Intersegment, adding immediate to SP	1 1 0 0 1 0 1 0	data-low	data-high
JE/JZ=Jump on equal/zero	0 1 1 1 0 1 0 0	disp	
JL/JNGE=Jump on less/not greater or equal	0 1 1 1 1 1 0 0	disp	
JLE/JNG=Jump on less or equal/not greater	0 1 1 1 1 1 1 0	disp	
JB/JNAE=Jump on below/not above or equal	0 1 1 1 0 0 1 0	disp	
JBE/JNA=Jump on below or equal/ not above	0 1 1 1 0 1 1 0	disp	
JP/JPE=Jump on parity/parity even	0 1 1 1 1 0 1 0	disp	
JO=Jump on overflow	0 1 1 1 0 0 0 0	disp	
JS=Jump on sign	0 1 1 1 1 0 0 0	disp	
JNE/JNZ=Jump on not equal/not zero	0 1 1 1 0 1 0 1	disp	
JNL/JGE=Jump on not less/greater or equal	0 1 1 1 1 1 0 1	disp	
JNLE/JG=Jump on not less or equal/ greater	0 1 1 1 1 1 1 1	disp	

	7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
JNB/JAE Jump on not below/above or equal	0 1 1 1 0 0 1 1	disp
JNBE/JA Jump on not below or equal/above	0 1 1 1 0 1 1 1	disp
JNP/JPO Jump on not par/par odd	0 1 1 1 1 0 1 1	disp
JNO Jump on not overflow	0 1 1 1 0 0 0 1	disp
JNS Jump on not sign	0 1 1 1 1 0 0 1	disp
LOOP Loop CX times	1 1 1 0 0 0 1 0	disp
LOOPZ/LOOPE Loop while zero/equal	1 1 1 0 0 0 0 1	disp
LOOPNZ/LOOPNE Loop while not zero/equal	1 1 1 0 0 0 0 0	disp
JCXZ Jump on CX zero	1 1 1 0 0 0 1 1	disp
INT Interrupt		
Type specified	1 1 0 0 1 1 0 1	type
Type 3	1 1 0 0 1 1 0 0	
INTO Interrupt on overflow	1 1 0 0 1 1 1 0	
IRET Interrupt return	1 1 0 0 1 1 1 1	

Process Control

CLC Clear carry	1 1 1 1 1 0 0 0
CMC Complement carry	1 1 1 1 0 1 0 1
STC Set carry	1 1 1 1 1 0 0 1
CLD Clear direction	1 1 1 1 1 1 0 0
STD Set direction	1 1 1 1 1 1 0 1
CLI Clear interrupt	1 1 1 1 1 0 1 0
STI Set interrupt	1 1 1 1 1 0 1 1
HLT Halt	1 1 1 1 0 1 0 0
WAIT Wait	1 0 0 1 1 0 1 1
ESC Escape (to external device)	1 1 0 1 1 x x x mod x x x r/m
LOCK Bus lock prefix	1 1 1 1 0 0 0 0

Footnotes:

AL = 8-bit accumulator
AX = 16-bit accumulator
CX = Count register
DS = Data segment
ES = Extra segment
Above/below refers to unsigned value.
Greater = more positive;
Less = less positive (more negative) signed values
if d = 1 then "to" reg; if d = 0 then "from" reg
if w = 1 then word instruction; if w = 0 then byte instruction

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0* disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP
DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

if s w = 01 then 16 bits of immediate data form the operand
if s w = 11 then an immediate data byte is sign extended to form the 16-bit operand.
if v = 0 then "count" = 1, if v = 1 then "count" in (CL)
x = don't care
z is used for string primitives for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

0 0 1 reg 1 1 0

REG is assigned according to the following table

16-Bit (w = 1)	8-Bit (w = 0)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X:X:(OF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

Data Transfer

MOV = **Move:**	76543210	76543210	76543210	76543210
Register/memory to/from register	100010dw	mod reg r/m		
Immediate to register/memory	1100011w	mod 000 r/m	data	data if w = 1
Immediate to register	1011w reg	data	data if w = 1	
Memory to accumulator	1010000w	addr low	addr high	
Accumulator to memory	1010001w	addr low	addr high	
Register/memory to segment register	10001110	mod 0 reg r/m		
Segment register to register/memory	10001100	mod 0 reg r/m		

PUSH = **Push:**		
Register/memory	11111111	mod 110 r/m
Register	01010 reg	
Segment register	000 reg 110	

POP = **Pop:**		
Register/memory	10001111	mod 000 r/m
Register	01011 reg	
Segment register	000 reg 111	

XCHG = **Exchange:**		
Register/memory with register	1000011w	mod reg r/m
Register with accumulator	10010 reg	

IN = Input from		
Fixed port	1110010w	port
Variable port	1110110w	

OUT = Output to		
Fixed port	1110011w	port
Variable port	1110111w	

XLAT = Translate byte to AL	11010111	
LEA = Load EA to register	10001101	mod reg r/m
LDS = Load pointer to DS	11000101	mod reg r/m
LES = Load pointer to ES	11000100	mod reg r/m
LAHF = Load AH with flags	10011111	
SAHF = Store AH into flags	10011110	
PUSHF = Push flags	10011100	
POPF = Pop flags	10011101	

Arithmetic

ADD = **Add:**				
Reg./memory with register to either	000000dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 000 r/m	data	data if s w = 01
Immediate to accumulator	0000010w	data	data if w = 1	

ADC = **Add with carry:**				
Reg./memory with register to either	000100dw	mod reg r/m		
Immediate to register/memory	100000sw	mod 010 r/m	data	data if s w = 01
Immediate to accumulator	0001010w	data	data if w = 1	

INC = **Increment:**		
Register/memory	1111111w	mod 000 r/m
Register	01000 reg	
AAA = ASCII adjust for add	00110111	
BAA = Decimal adjust for add	00100111	

SUB = **Subtract:**				
Reg./memory and register to either	001010dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 101 r/m	data	data if s w = 01
Immediate from accumulator	0010110w	data	data if w = 1	

SBB = **Subtract with borrow**				
Reg./memory and register to either	000110dw	mod reg r/m		
Immediate from register/memory	100000sw	mod 011 r/m	data	data if s w = 01
Immediate from accumulator	0001110w	data	data if w = 1	

DEC = **Decrement:**	76543210	76543210	76543210	76543210
Register/memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG Change sign	1111011w	mod 011 r/m		

CMP = **Compare:**				
Register/memory and register	001110dw	mod reg r/m		
Immediate with register/memory	100000sw	mod 111 r/m	data	data if s w = 01
Immediate with accumulator	0011110w	data	data if w = 1	
AAS ASCII adjust for subtract	00111111			
DAS Decimal adjust for subtract	00101111			
MUL Multiply (unsigned)	1111011w	mod 100 r/m		
IMUL Integer multiply (signed)	1111011w	mod 101 r/m		
AAM ASCII adjust for multiply	11010100	00001010		
DIV Divide (unsigned)	1111011w	mod 110 r/m		
IDIV Integer divide (signed)	1111011w	mod 111 r/m		
AAD ASCII adjust for divide	11010101	00001010		
CBW Convert byte to word	10011000			
CWD Convert word to double word	10011001			

Logic

NOT Invert	1111011w	mod 010 r/m		
SHL/SAL Shift logical/arithmetic left	110100vw	mod 100 r/m		
SHR Shift logical right	110100vw	mod 101 r/m		
SAR Shift arithmetic right	110100vw	mod 111 r/m		
ROL Rotate left	110100vw	mod 000 r/m		
ROR Rotate right	110100vw	mod 001 r/m		
RCL Rotate through carry flag left	110100vw	mod 010 r/m		
RCR Rotate through carry right	110100vw	mod 011 r/m		

AND = **And**				
Reg./memory and register to either	001000dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 100 r/m	data	data if w = 1
Immediate to accumulator	0010010w	data	data if w = 1	

TEST = **And function to flags, no result:**				
Register/memory and register	1000010w	mod reg r/m		
Immediate data and register/memory	1111011w	mod 000 r/m	data	data if w = 1
Immediate data and accumulator	1010100w	data	data if w = 1	

OR = **Or**				
Reg./memory and register to either	000010dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 001 r/m	data	data if w = 1
Immediate to accumulator	0000110w	data	data if w = 1	

XOR = **Exclusive or:**				
Reg./memory and register to either	001100dw	mod reg r/m		
Immediate to register/memory	1000000w	mod 110 r/m	data	data if w = 1
Immediate to accumulator	0011010w	data	data if w = 1	

String Manipulation

REP = Repeat	1111001z
MOVS = Move byte/word	1010010w
CMPS = Compare byte/word	1010011w
SCAS = Scan byte/word	1010111w
LODS = Load byte/wd to AL/AX	1010110w
STOS = Stor byte/wd from AL/A	1010101w

APPENDIX B: CLUSTER CABLING AND INTERCONNECTIONS

This Appendix details the components necessary to connect the AWS-220, -230, and -240 workstations to a master workstation and to other cluster workstations. Certain assemblies are not manufactured by Convergent Technologies; they are shown only to provide the user with information about their construction.

Cabling information for the parallel printer interface, the keyboard, and the RS-232-C Channels A and B is given in the "External Interfaces" section, above.

CLUSTER COMMUNICATIONS CABLES

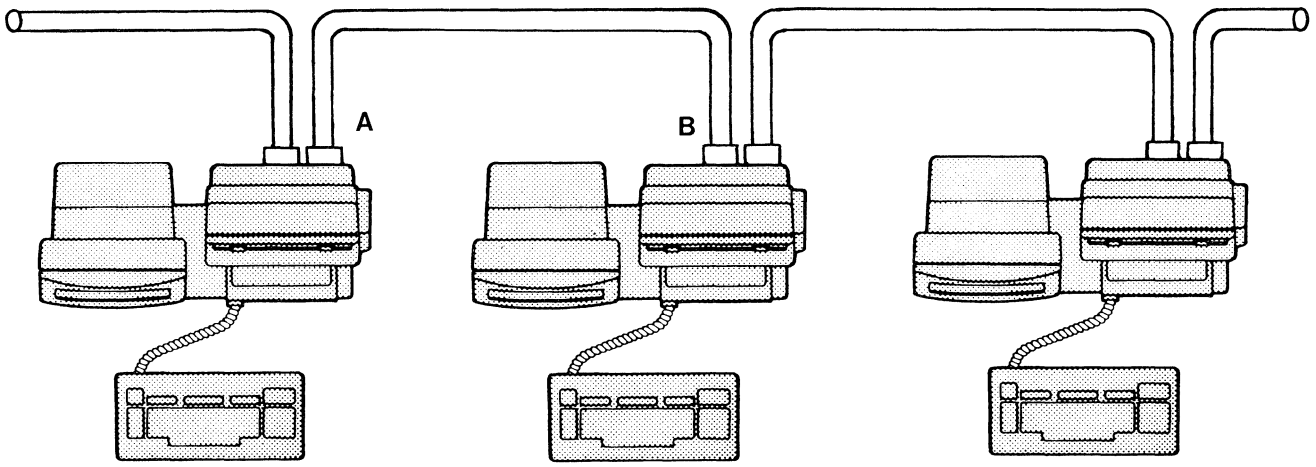
Communications between an AWS-220, -230, and -240 and a master workstation pass through communications cables. The cables are linked in a daisy-chain configuration by two connectors marked "Cluster Communications" on the back panel of each workstation. The cluster workstations at the ends of the daisy chain have a special terminator plugged into the unused cluster communications jack. The details of the cabling and termination are shown below.

Assembly: Cluster Communications Cable

Convergent Part Number: 61-00027

Function: Connects workstations to the cluster communications line

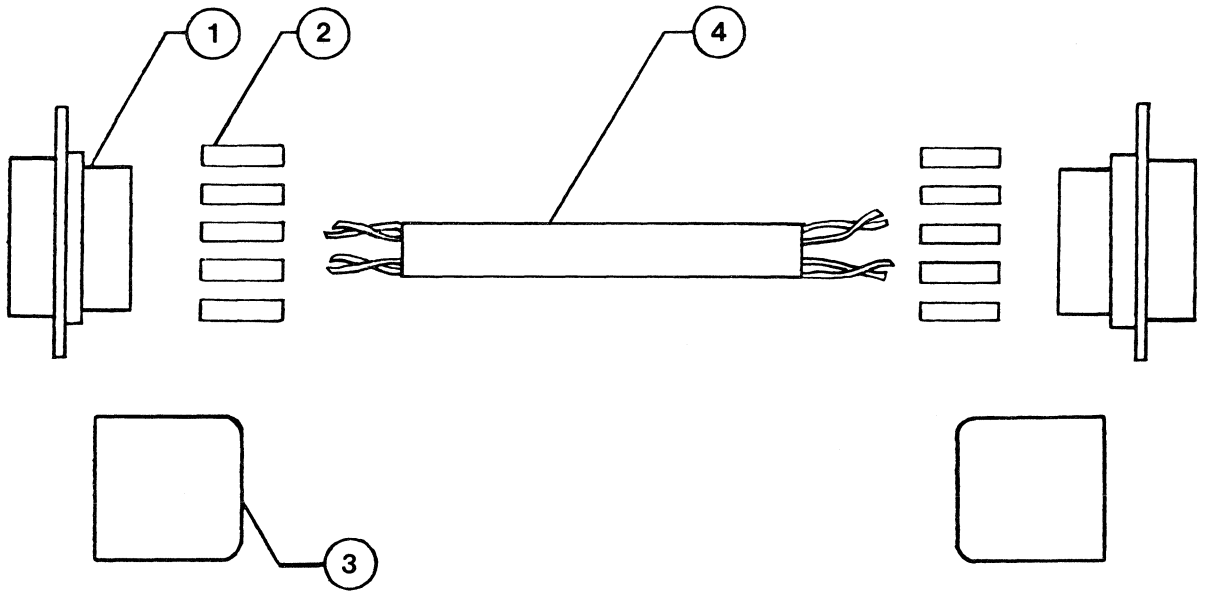
Connection:



Pinouts:

A		B	Assignments
1	↔	1	GND (shield)
2		2	no connection
3		3	no connection
4		4	no connection
5		5	no connection
6	↔	6	CLK+
7	↔	7	CLK-
8	↔	8	DATA+
9	↔	9	DATA-

Construction:



Item	Quan.	Description
1.	2	9-pin D-type plug assemblies (male). Use Amp #205204-1 or equivalent.
2.	10	Connector contacts. Use Amp #66507-3 or equivalent.
3.	2	Connector shell/strain reliefs. Use Amp #207908-1 or equivalent.
4.	50 ft (15.2 m)	4-conductor twisted pair shielded cable. Use Belden #9502 or equivalent.

Pin 1 must be connected to the shield wire at both ends.

Pins 6 and 7 are a twisted pair; pins 8 and 9 are a twisted pair.

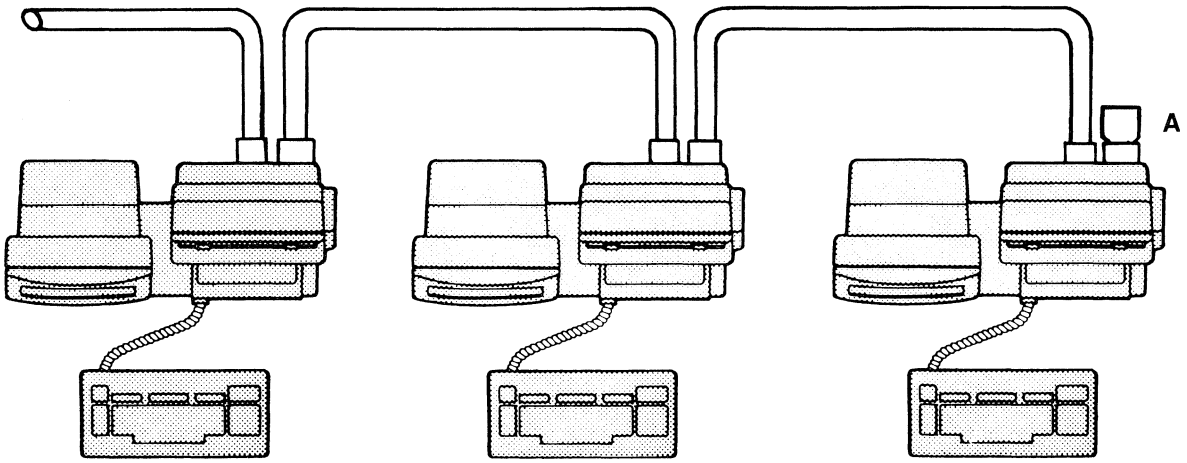
Notes: The maximum total length of a cluster communications line is 1,200 ft (366 m). The minimum cable length between workstations is 25 ft (7.62 m).

Assembly: Cluster Communications Terminator

Convergent
Part Number: 61-00029

Function: Terminates cluster communications line

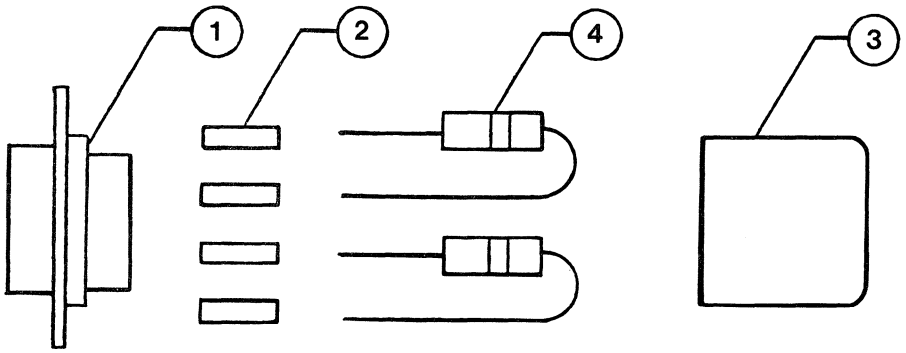
Connection:



Pinouts:

A	Assignments
1	no connection
2	no connection
3	no connection
4	no connection
5	no connection
6	CLK+ 240 Ohms 1/4 W (to pin 7)
7	CLK-
8	DATA+ 240 Ohms 1/4 W (to pin 9)
9	DATA-

Construction:



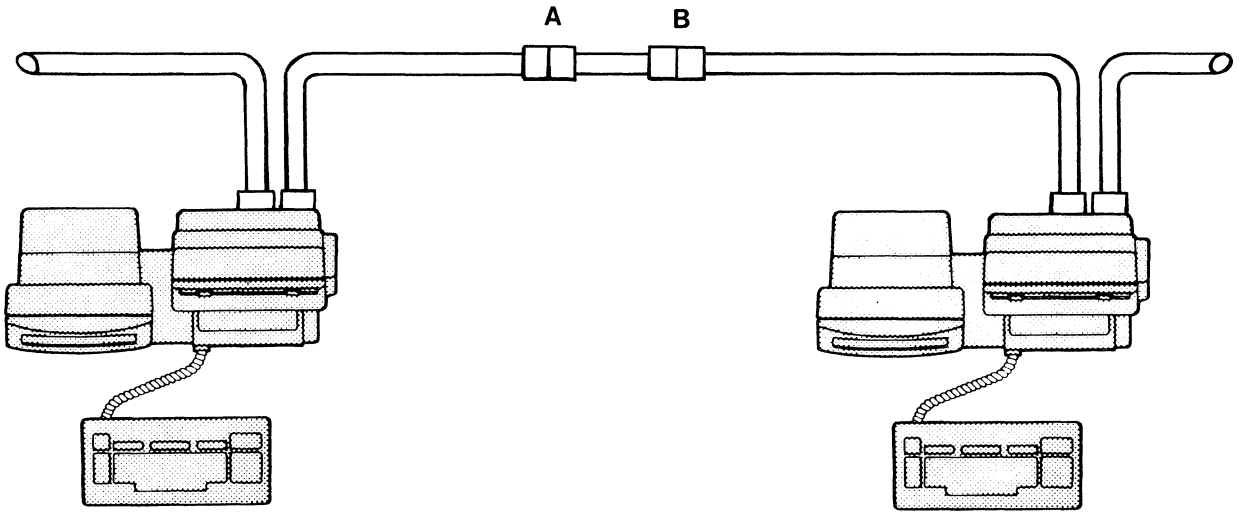
Item	Quan.	Description
1.	1	9-pin D-type plug assembly (male). Use Amp #205204-1 or equivalent.
2.	4	Connector contacts. Use Amp #66507-3 or equivalent.
3.	1	Connector shell. Use Amp #207908-1 or equivalent.
4.	2	240-ohm 1/4-W resistors

Note: A terminator must be installed at each end of the cluster communications line.

Assembly: Cluster Communications Cable Splice

Function: Joins two cluster communications cables

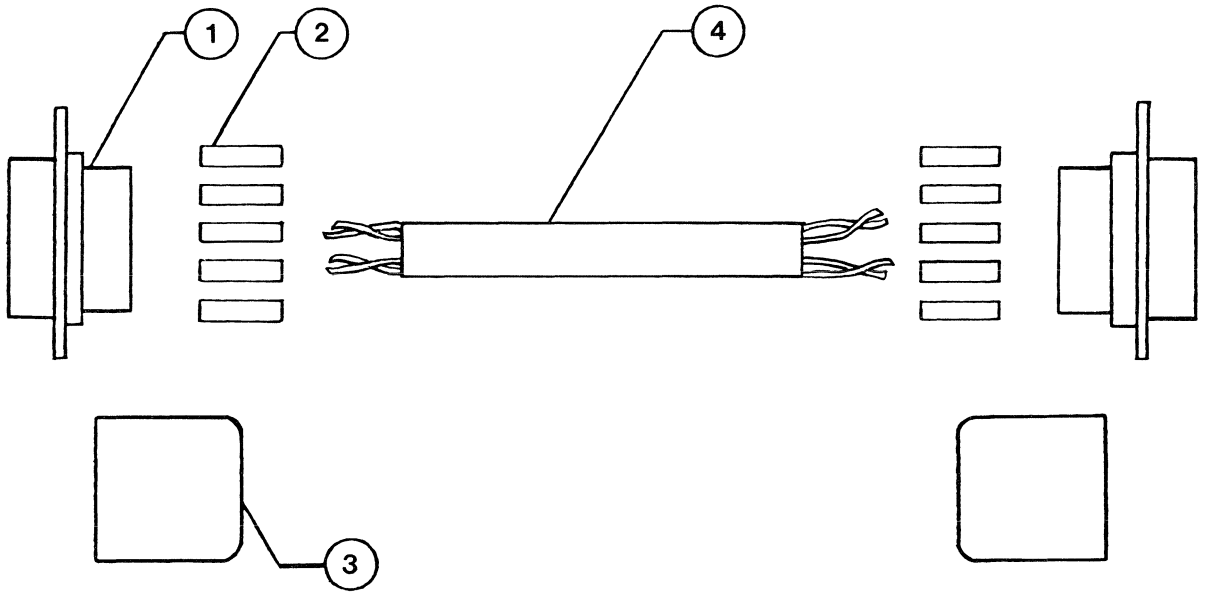
Connection:



Pinouts:

A	B	Assignments
1	1	GND (shield)
2	2	no connection
3	3	no connection
4	4	no connection
5	5	no connection
6	6	CLK+
7	7	CLK-
8	8	DATA+
9	9	DATA-

Construction:



Item	Quan.	Description
1.	2	9-pin D-type receptacle assemblies (female). Use Amp #205203-1 or equivalent.
2.	10	Connector contacts. Use Amp #66505-9 or equivalent.
3.	2	Connector shell/strain reliefs. Use Amp #207908-1 or equivalent.
4.	0.5 ft (0.15 m)	4-conductor twisted pair shielded cable. Use Belden #9502 or equivalent.

Pin 1 must be connected to the shield drain wire at both ends.

Pins 6 and 7 are a twisted pair; pins 8 and 9 are a twisted pair.

Note: The maximum total length of a cluster communications line is 1,200 ft (366 m).

APPENDIX C: WORKSTATION SPECIFICATIONS

ELECTRONIC

Memory Capacity

RAM

Available configurations provide 128, 256, 348, or 512 kilobytes.

ROM

CPU Board:	4 kilobytes
FDC or HDC Board:	4 kilobytes

Mass Storage

5 1/4-in floppy disk drive (single-sided)

Unformatted:	500 kilobytes
Formatted:	315 kilobytes

5 1/4-in floppy disk drive (double-sided)

Unformatted:	1 megabyte
Formatted:	630 kilobytes

5 1/4-in hard disk drive

Unformatted:	6.38 megabytes (minimum)
Formatted:	5.00 megabytes (minimum)

Processor Speed

8088 CPU Board:	5 MHz with one wait state for a memory fetch
8086 CPU Board:	8 MHz with no wait state for a memory fetch

Serial Input/Output Rate

Cluster communications

307 kilobaud

RS-232-C communications

External clock:	110 to 19.2 kilobaud
Internal clock:	50 to 19.2 kilobaud

Parallel Output Rate

19.6k characters per second

Memory Refresh Rate

78 kHz

Mass Storage Timing

Floppy disk drive

Transfer rate:	16k words/sec
Access time (average):	158 ms
Access time (track to track):	6 ms
Settling time:	15 ms
Motor Start time:	200 ms

Hard disk drive

Transfer rate:	312k words per/sec
Access time (average):	95 ms
Access time (track to track):	3 ms

SAFETY AND ENVIRONMENTAL

Safety

UL 478 (EDP) and 114 (office equipment)

CSA 154 (EDP) and 143 (office equipment)

VDE 0806, Parts 1 and 2 (available at extra cost)

BSI BS 3861, Parts 1, 2, and 3 (available at extra cost)

EMI

US FCC Rules and Regulations, Part 15, Subpart J, Class A

VDE 0871, Level A (available at extra cost)

ESD

5,000 V:	no observable effect
15,000 V:	no operator-perceived errors

	25,000 V:	no permanent damage

Altitude

Operating:	6,000 ft ASL
Nonoperating:	12,000 ft ASL

Acoustic Noise Level

NR40

Temperature and Humidity

System

	Operating:	+32 - 104° F (0 - 40° C)
	Nonoperating:	-40 - 167° F (-40 - 75° C)

Media

	Operating:	+50 - 104° F (+10 - 40° C)
	Nonoperating:	- 7 - 116.6° F (-22 - 47° C)

System

Humidity:	5 - 95% noncondensing

Media

Humidity:	20 - 80% noncondensing

PHYSICAL

Workstation

Height

13.75 in (34.92 cm)

Length

30.00 in (76.20 cm)

Depth

12.00 in (30.48 cm)

Weight

AWS-220:	48 lb	(21.82 kg)
AWS-230:	52 lb	(23.64 kg)
AWS-240:	53 lb	(24.10 kg)

Keyboard

Height:	2.40 in (6.09 cm)
Length:	18.00 in (45.72 cm)
Depth:	8.50 in (21.59 cm)
Weight:	5.00 lb (2.27 kg)

Cable Lengths

AC line
10 ft

Keyboard to workstation

coiled:	14 in
extended:	5 ft

Maximum cluster length
1,200 ft

ELECTRICAL

AC Power Frequency

47 to 440 Hz

AC Voltage

85 to 130 V rms
or
180 to 260 V rms

AC Power Requirements

Maximum:	105 Vrms
Floppy disk drive:	1.25 A
Floppy and hard disk drive:	2.00 A

APPENDIX D: ENHANCED VIDEO FEATURES

While the Intel 8275 is the basic controlling element for the video display control logic, several of its features are not used by Convergent software. These features include special control characters, different font shapes, different DMA timings, different blink rates, etc.

INITIALIZATION PARAMETERS

When the 8275 is issued a Reset command, it is programmed with a set of initialization parameters that control all video display functions until the next Reset command. The frequency of video display refresh is a function of several of these parameters, and changing the frequency from the standard 60 Hz by altering a parameter can have undesirable effects.

For example, if the frequency is not exactly 60 Hz, the video display has a wavy look. If it is slower than about 50 Hz, the video display has a noticeable flicker. Also, if the horizontal sweep and vertical refresh frequencies are too far from the nominal values, the CRT Deflection Board cannot operate correctly and the video display loses synchronization.

The formulas for determining the proper horizontal and vertical frequencies are shown below.

The horizontal sweep frequency formula is:

$$Fh = Fp / Wc / (H + 3 + (2 \times Z))$$

where:

Fh	is the horizontal sweep frequency,
Fp	is the pixel frequency (17.82 MHz),
Wc	is the horizontal pixels per character (9), and
H, Z	are the 8275 initialization parameters.

The vertical refresh frequency formula is:

Fv = Fh / (L + 1) / (R + 1 V)

where:

Fv	is the vertical sweep frequency,
Fp	is the pixel frequency (17.82 MHz), and
L, R, V	are the 8275 initialization parameters.

The initialization parameters H, Z, L, R, and V can be reprogrammed as long as Fv remains at the line frequency. If Fv is not exactly equal to the line frequency, the video display operates subject to the problems described above. The complete set of the initialization parameters, including those described in the previous examples, are listed in Table D-1 below.

ROW 29

There are normally 29 rows displayed on the video display (even though the CTOS Operating System fills row 29 with blanks). To ensure continuous synchronization of the video display to the DMA controller, a special control character (F3h) is inserted in character positions 79 and 80 of row 29. The F3h character appears as a visible blank. Therefore, at least the first 78 characters of row 29 can be used.

If the F3h character is not inserted in the video map, row 29 can be 80 characters. However, if a DMA underrun occurs, the video display will not be synchronized and the character that should appear in row 1 column 1 of the video display appears at some other video display position. (DMA underrun can be caused by too many field attributes on a row in the invisible attribute mode.) This condition remains until the next Reset command.

Table D-1. 8275 Initialization Parameters. (Page 1 of 2)

Parameter	Values Range	Values Normal	Meaning
H	0-79	79	One less than the number of characters per row. Each row can contain from 1 to 80 characters.
Z	0-15	10	2 + (Z x 2) is the number of character counts per horizontal retrace. If a smaller Z is used, the video display is shifted to the left. Similarly, a larger Z moves the video display to the right.
L	0-15	10	One less than the number of raster lines per character. If L is not 10, the font ROM may need to be changed to fill the new character cell. The font ROM can be programmed with a character cell up to 16 raster lines high (9 by 16). The underline is fixed on raster line 9.
R	0-28	28	One less than the number of displayable rows on the video display.
V	0-3	1	The number of row intervals for vertical retrace, (where one row interval equals 11 horizontal sweeps of the video display). If V is greater than 1,there are (V - 1) blank rows at the top of the video display.
S	0-1	0	Nonspaced rows. When set to 1, the 8275 double-spaces rows; that is, every other character row on the video display is blank. DMA is not requested for the blank rows.

Table D-1. 8275 Initialization Parameters. (Page 2 of 2)

Parameter	Values Range	Values Normal	Meaning
U	0-15	7	One less than the raster line number that the 8275 assumes the underline is on. Since the 8275 underline is not used, U only affects the result of the special graphic characters, C0h-EFh. If U is greater than 7, the top and bottom raster lines of all characters are made blank.
M	0-1	0	Nonoffset line numbers. The raster line counter, which addresses the font ROM, counts from 0 to the value of L above. When L is 1, the raster line counter starts with L during the top line of the character cell, followed by 0 to (L - 1).
F	0-1	0	Transparent attributes. When F is 0, field attribute characters use no space on the video display, and there is a limit of 16 field attribute characters per row. When F is 1, there is no limit to the number of field attribute characters, but each field attribute character is displayed as a visible space.
C	0-3	0	Blinking underline cursor. If C is 2, the cursor does not blink. If C is 1 or 3, no cursor appears.

SPECIAL GRAPHIC CHARACTERS

There are 11 characters that, when placed in the video map, activate external signals on the 8275. One of these signals, VSP (Video Suppress), causes the video display to go blank. The other three signals, LTEN, LA0, and LA1 are not used. The manufacturer of the 8275 intended these 11 characters for line graphics, and the underline for a continuous horizontal bar. When the signals VSP, LTEN, LA0, and LA1+ are active, therefore, depends on when the raster line specified by the parameter U is displayed. In addition, when CC0 (Character Code bit 0) from the 8275 is 1, the character is displayed as half-bright. CC1 (Character Code bit 1) causes the character to blink. The characters are listed in Table D-2 below.

Table D-2. Special Graphic Character Effects.

Graphic Character	Externally Active Signals			
	LA1	LA0	VSP	LTEN
C0h - C3h	At line U	At > line U	At < line U	No
C4h - C7h	At line U	At > or = U	At < line U	No
C8h - CBh	At line U	At < line U	At > line U	No
CCh - CFh	At line U	At < or = U	At > line U	No
D0h - D3h	No	At > line U	At < line U	At line U
D4h - D7h	At line U	At all lines	No	No
D8h - DBh	At line U	At < or > U	No	No
DCh - DFh	No	No	At > line U	At line U
E0h - E3h	No	No	At < or > U	At line U
E4h - E7h	No	At all lines	No	No
E8h - EBh	No	At < or > U	No	At line U

Notes: > = line numbers greater than
< = line numbers less than

When a special graphic character is displayed, the font ROM is generating the character that corresponds to the character code of the special graphic character with the high-order bit 0. That is, if character code C1 is used, the font ROM is attempting to display an A (ASCII code 41h), and VSP blanks everything above raster line U.

An example of the use of special graphic characters is the use of character E0h instead of blank (20h) in rows that are to be word-underlined. Word-underlining breaks the underline between words without requiring field attribute characters.

CONTROL CHARACTERS

Control characters F0h-F3h in the video map are used for special control features of the 8275. The control characters appear on the video display as blanks, even in reverse video fields. The F0h-F3h control characters are described in the "Architecture" section under "Video Display Control."

OTHER COMMANDS

The 8275 in the AWS-220, -230, and -240 uses seven commands: Reset (described above in "Initialization Parameters"), Start Display, Stop Display, Load Cursor, Enable Interrupt, Disable Interrupt, and Preset Counters.

Start Display

This command causes the video display and DMA requests to begin, and the Interrupt Enable and Video Enable status flags to be set. The Start Display command has two parameters, S and B, which can be altered to change the DMA load. They are used as listed below.

	Values		
Parameter	Range	Normal	Meaning
S	0-7	1	(8 x S) - 1 is the number of character clocks between video DMA requests.
B	0-3	3	2 raised to the B power is the number of characters read in each DMA burst.

Stop Display

This command stops the video display. The Start Video command must be given to start the video display again.

Load Cursor

When the 8088 writes a Load Cursor command to the 8275, the cursor is positioned on the video display according to the next two bytes sent from the 8088. The first byte is the character position in the row; the second byte is the row number on the video display.

Enable and Disable Interrupt

Although the interrupt line of the 8275 is not used, the Enable and Disable Interrupt commands can be used with the 8275 status reads to determine when the last row of the video display is being displayed. These commands can also be used to measure speed or frequency (where the event happens at a 60 Hz rate), or to find a convenient time to change the video map or the DMA address and/or count of the video map. The Enable and Disable Interrupt commands are not used with the CTOS Operating System.

Preset Counters

This command causes the 8275 timing to be reinitialized. The Preset Counters command can be used for synchronizing the video display to the DMA buffer or to any other event. This command is not used with the CTOS Operating System.

STATUS INFORMATION

8275 Status

The 8275 status register can be read to gain information about the state of the video display control logic. The status bits are:

Status Bit	Meaning
IE	Interrupt Enable. This is set to 1 by the Enable Interrupt command or Start Display command. This is reset by the Disable Interrupt or Reset command. See the Enable/Disable Interrupt commands description.
IR	Interrupt Request. This is set to 1 during the video display of the last row of the frame. See the Enable/Disable Interrupt command description.
LP	Light Pen Active. Not used.
IC	Improper Command. This is set to 1 if an invalid command/parameter string is sent to the 8275.
VE	Video Enabled. This is set to 1 by the Start Display command and reset by the Stop Display or Reset command.
DU	DMA Underrun. This is set to 1 if a hardware or software failure causes the 8275 to underrun, that is, the DMA could not get data when it needed it. This can be used to determine when video display resynchronization is required in lieu of the F3h characters.
FO	FIFO Overrun. This is set to 1 if too many field attributes are in a row in the "invisible attribute mode."

8257 Status

Input Port 8h contains two bits corresponding to the 8257.

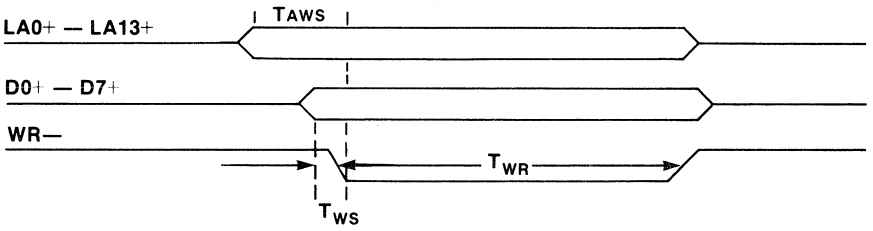
Bit	Meaning
3	Update Status. This is set to 1 when the last character of the DMA video map is read. It is reset by reading the status.

Bit	Meaning
4	Update Flag. This is set to 1 to indicate that the DMA update address and count Ports 6h and 7h are loaded but not used. Software can use this information to merge different video maps since ports 6h and 7h are the address and count values used for the next video display of the frame.

DMA PORTS

Ports 4h and 5h contain the current address and count values for the video display. Reading these Ports is valuable for synchronizing software to refresh the video display. For instance, if a row is to be altered to contain too many field attributes for a short time, the address port can be read to determine whether video DMA is about to use that row in the video map.

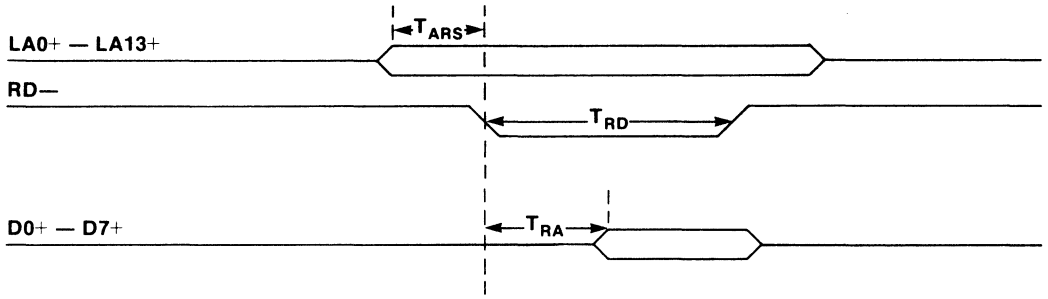
APPENDIX E: EXPANSION INTERFACE TIMING DIAGRAMS



AC Characteristics

Symbol	Parameter	Typ	Unit
T_{WS}	Write Data Setup	0	ns
T_{WR}	Write Width	550	ns
T_{AWS}	Address to Write Setup	200	ns

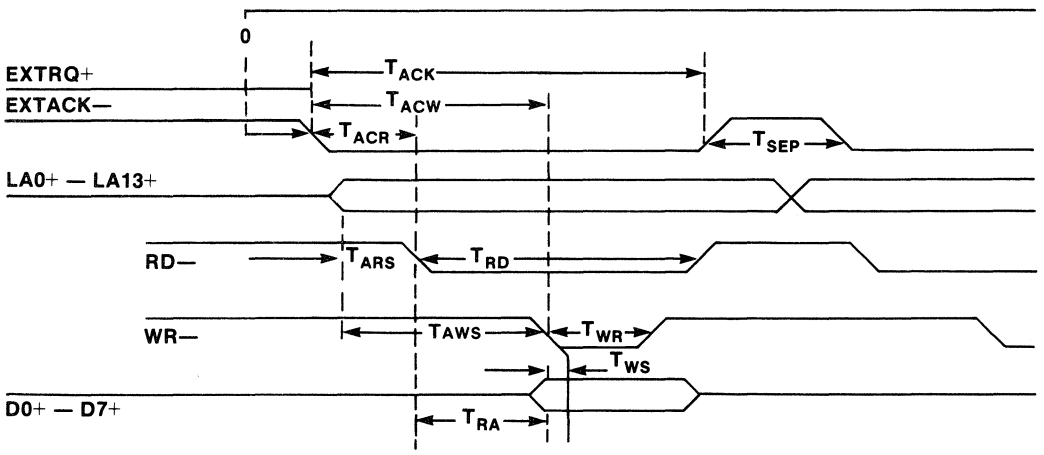
Figure E-1. Expansion Interface Non-DMA Write (8088).



AC Characteristics

Symbol	Parameter	Typ	Unit
T_{ARS}	Address to Read Setup	250	ns
T_{RD}	Read Width	550	ns
T_{RA} (Memory Read Access Performance)	Read Access	390	ns
T_{RA} (Memory Read Access CPU Requirement)	Read Access	370	ns

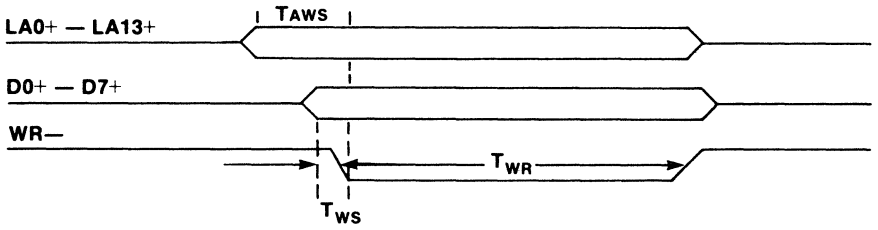
Figure E-2. Expansion Interface Non-DMA Read (8088).



AC Characteristics

Symbol	Parameter	Typ	Unit
T_{ACW}	Acknowledge Setup to Write	550	ns
T_{ACR}	Acknowledge Setup to Read	150	ns
T_{ARS}	Address Setup to Read	100	ns
T_{RD}	Read Width	1000	ns
T_{WR}	Write Width	400	ns
T_{AWS}	Address Setup to Write	500	ns
T_{WS} (Memory Read Performance)	Write Data Setup	30	ns
T_{WS} (Memory Write Requirement)	Write Data Requirement	-50	ns
T_{RA}	Memory Read Access	370	ns
T_{SEP}	Acknowledge Separation	400	ns
T_{ACK}	Acknowledge Width	1200	ns

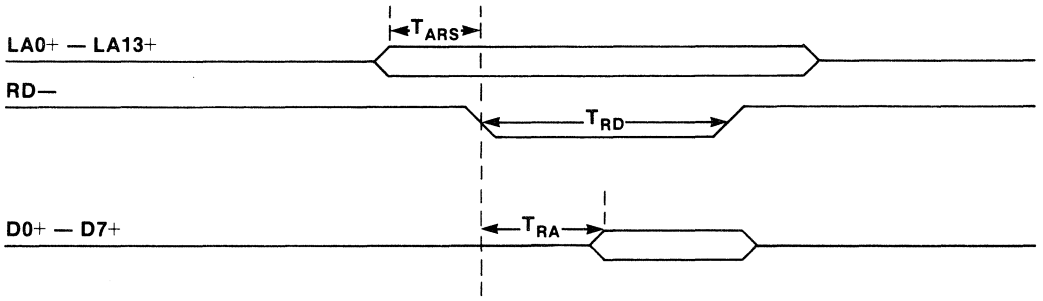
Figure E-3. Expansion Interface DMA Mode (8088).



AC Characteristics

Symbol	Parameter	Typ	Unit
T_{WS}	Write Data Setup	0	ns
T_{WR}	Write Width	1000	ns
T_{AWS}	Address to Write Setup	100	ns

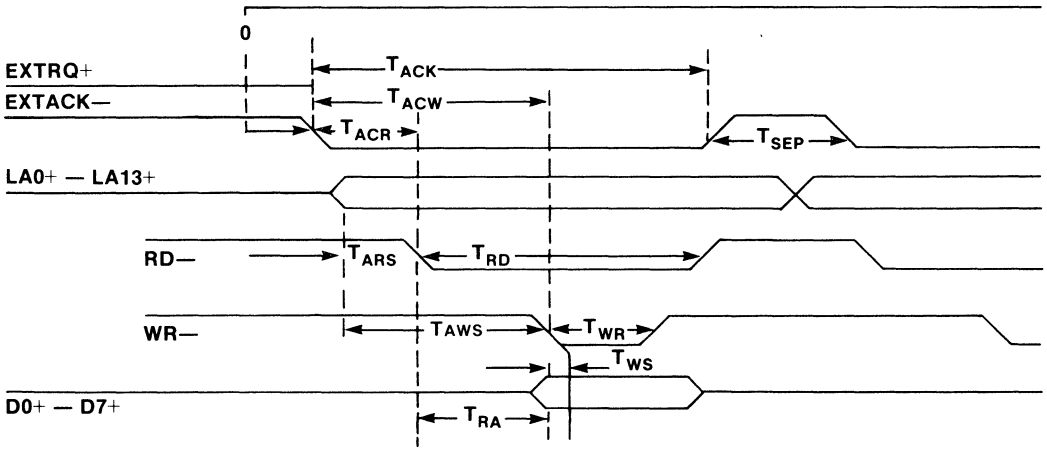
Figure E-4. Expansion Interface Non-DMA Write (8086).



AC Characteristics

Symbol	Parameter	Typ	Unit
T_{ARS}	Address to Read Setup	100	ns
T_{RD}	Read Width	1000	ns
T_{RA} (Max. I/O Read Access CPU Requirement)	Read Access	900	ns

Figure E-5. Expansion Interface Non-DMA Read (8086).



AC Characteristics

Symbol	Parameter	Typ	Unit
T_{ACW}	Acknowledge Setup to Write	500	ns
T_{ACR}	Acknowledge Setup to Read	150	ns
T_{ARS}	Address Setup to Read	200	ns
T_{RD}	Read Width	800	ns
T_{WR}	Write Width	330	ns
T_{AWS}	Address Setup to Write	500	ns
T_{WS}	I/O Write Data Setup	300	ns
T_{WS} (Memory Write Requirement)	Write Data Requirement	-30	ns
T_{RA}	Memory Read Access	250	ns
T_{SEP}	Acknowledge Separation	330	ns
T_{ACK}	Acknowledge Width	600	ns

Figure E-6. Expansion Interface DMA Mode (8086).

APPENDIX F: SIGNAL GLOSSARY

Signal Name	Figure/Page	Description
A0+-A7+	3-3/3 3-31/4	Address 0-7. RAM array address lines.
ACK-	3-25/4 3-31/8	Character Acknowledge. From line printer.
AD0+-AD13+	3-3/2 3-14/2	Address and Data 0-13. Address and data lines to and from the CPU.
ADRIS-	3-3/2 3-14/2 3-25/2 3-31/7	Address Disable. Used by FDC or HDC when the four high-order address bits of a DMA buffer are supplied.
ADSTB+	3-3/2	Address Strobe. Used by 8257 on the CPU Board to clock the address latch.
AEN+	3-3/2 3-14/2	Address Enable. Used by 8257 to enable the address drivers.
ALTFONT+	3-3/5 3-14/6	Alternate Font. Asserted by the video display control logic to access the upper half of the font ROM address space.
ASYNC-	3-14/2	Ready Syncronization Select. Ready synchronization selector for 8284(A).
BA0+-BA7+	3-14/4	Buffered Memory Address. Buffered address lines to the upper half of the RAM array.
BD0+-BD7+	3-25/2 3-31/6	Buffered Data Bus 0-7. Data bus for the FDC and HDC Boards to and from the CPU Board.
BDATA0+-BDATAF+	3-3/3 3-14/3	Buffered RAM Data. Data to RAM array and parity checker.

Signal Name	Figure/Page	Description
BHE-	3-14/2	Bus High Enable. From CPU for bus control.
BRD-	3-25/2 3-31/6	Buffered Read Strobe. From CPU Board to FDC or HDC Board.
BRESET-	3-25/2 3-31/6	Buffered Reset. From CPU Board RESET-.
BWR-	3-25/2 3-31/6	Buffered Write Strobe. From CPU Board to FDC or HDC Board.
C1CLK+	3-25/4 3-31/8	Counter 1 Clock. Counter 1 clock output from the 8253 counter/timer to the RS-232-C communications logic.
C2CLK+	3-25/4 3-31/8	Counter 2 Clock. Counter 2 clock output from the 8253 counter/timer to the RS-232-C communications logic.
CAS+	3-3/3 3-14/4	Column Address Strobe.
CAS+	3-25/2 3-31/6	Cascade. Output from the 8259A interrupt controller.
CCLK+	3-3/5 3-14/6	Character Clock. Character clock for the video display control logic.
CH0ACK-	3-14/2	Channel 0 DMA Acknowledge.
CLAMP-	3-25/6 3-31/4	Clamp. Used by the disk controller to make the VFO start in phase with the incoming data stream.
CLRZ-	3-31/4	Clear Zero Detector. From the HDC Board address mark detector.
COLMPX-	3-3/3 3-14/4	Column Multiplex. RAM column multiplex strobe.

Signal Name	Figure/Page	Description
COMMACK-	3-3/2 3-14/2	Communications DMA Acknowledge. DMA acknowledge from the 7201 on the CPU Board.
COMMRQ+	3-3/2 3-14/2	Communications DMA Request. DMA request from the 7201 on the CPU Board.
CPUDIS-	3-14/6	CPU Disable. Sent from an advanced video board to disable parts of the video display control logic.
CRCRST+	3-31/5	CRC Reset. Used by 8X300 to reset the CRC generator.
CRCTIME+	3-31/5	CRC Time. Used by the 8X300 during CRC generation.
CYC+	3-3/3 3-14/4	Cycle. Indicates the start of a normal memory read or write cycle.
D0+-D7+	3-3/2 3-14/2	Data Bus Lines 0-7.
DATA0+-DATA7+	3-3/3 3-14/3	RAM Data 0-7. Data lines to and from the RAM array.
DCDA+	3-3/4 3-14/5	Carrier Detect Channel A. Clock detection input to 7201 from the cluster communications line.
DCDB+	3-3/4 3-14/5	Carrier Detect Channel B. Input to 7201 from 8253 counter/timer.
DEN-	3-3/2 3-14/2	Data Bus Enable. From CPU to enable data buffer.
DESTACK+	3-14/2	Destack. Destacking signal used during ROM read cycle.

Signal Name	Figure/Page	Description
DISPARDC-	3-3/2 3-14/3	Disable Parity Detection. Used to disable parity logic.
DMACK-	3-25/5 3-31/6	DMA Acknowledge. DMA acknowledge signal from 8257 to disk controller.
DMAEN+ and -	3-3/2 3-14/2	DMA Enable. Used by 8257 to enable address, data, and control components.
DMARQ+	3-31/2	DMA Request. To CPU Board.
DREQ+	3-25/5	DMA Request. Delayed DMA data request.
DRIVED-	3-25/2 3-31/6	Drive Data Bus. Used to set the direction of the data bus transceivers.
DRQ+	3-25/5	Data Request. Output from 8272 to request DMA data.
DT-/R+	3-14/2	Data Transmit/Receive. CPU data input or outputs selector used to control bus transceivers.
DWAIT-	3-14/4	DMA Wait Request. Wait request output from an advanced video board.
ECRCS-	3-25/2 3-31/6	Extended Control Register Chip Select.
ENPARDC-	3-3/2 3-14/3	Enable Parity Detection. Used to enable parity detection. Active when the CPU reads Port F0h.
EPCLK+	3-14/6	External Pixel Clock/ From an advanced video board.
ERLYMR+	3-14/2	Early Memory Write. Early memory write strobe from CPU outputs.

Signal Name	Figure/Page	Description
EXD0+-EXD7+	3-14/2	Expansion Data Bus 0-7. To and from the FDC or HDC Board.
EXP1DC-	3-3/2 3-14/2 3-25/2 3-31/6	Expansion 1 Decode. Enables input/output devices on the FDC or HDC Board.
EXP2DC-	3-3/2 3-14/2 3-25/2 3-31/6	Expansion 2 Decode. Enables input/output devices on the FDC or HDC Board.
EXTRQ-	3-25/2 3-31/6	External DMA Request. DMA request from FDC or HDC Board to the 8257 on the CPU Board.
FRZ+	3-25/2 3-31/6	Freeze. Used to make sure that DRIVED- is low only during the second INTA- pulse in an interrupt acknowledge cycle.
GPA0+	3-3/5 3-14/6	General Purpose Attribute 1. Selects alternate font in the video display control logic. An advanced video board can use this signal for a different attribute.
GPA1+	3-3/5 3-14/6	General Purpose Attribute 1. Selects reverse video in the video display control logic. An advanced video board can use this signal for a different attribute.
HALFBRIGHT+ and -	3-3/5 3-14/6 3-37/1	Half-bright. Half-intensity video output from the video display control logic.
HDSEL0--HDSEL2-	3-31/3	Head Select 0-2. Read/write head select lines to the hard disk drives.

Signal Name	Figure/Page	Description
HLDA+	3-3/2 3-14/2	Hold Acknowledge. Output from CPU to 8257 to indicate that the 8257 can take control of the address, data, and control lines on the CPU Board.
HORDR+ and -	3-3/5 3-14/6 3-37	Horizontal Drive. Differential horizontal drive signal from the video display control logic.
HRQ+	3-3/2 3-14/2	Hold Request. Hold input to the CPU from the 8257.
HRTC+	3-3/5 3-14/6 3-37/1	Horizontal Retrace. Video horizontal retrace output from the 8275.
INDEX-	3-25/5 3-31/3	Index. Index mark signal from disk drive.
INT+	3-25/2 3-31/6	Interrupt. Interrupt output fro the 8259A.
INT1+-INT6+	3-25/2 3-31/6	Interrupt 1-6. Interrupt inputs to the 8259A from the FDC or HDC Board input/output devices.
INTA-	3-3/2 3-14/2 3-25/2 3-31/6	Interrupt Acknowledge. Output from CPU to acknowledge an interrupt from an input/output device.
INTR+	3-3/2 3-14/2 3-25/2 3-31/6	Interrupt Request. Interrupt request input to the CPU from input/ output devices.
IO+	3-3/2 3-14/2	Input/Output. Output from CPU. Indicates that an input/output operation is in progress.
IORD-	3-3/2 3-14/2	Input/Output Read. Read strobe from the 8257.

Signal Name	Figure/Page	Description
IOWR-	3-3/2 3-14/2	Input/Output Write. Write strobe from the 8257.
IPI-	3-3/4 3-14/5 3-25/2 3-31/6	Interrupt Pending In. Interrupt pending input to the CPU Board 7201.
IV0+-IV7+	3-31/2	Instruction/Vector 0-7. From and to the 8X300.
LA0+-LA13+	3-3/2 3-14/2 3-25/2 3-31/6	Line Address 0-13. Address bus (LA0+-LA4+ on FDC or HDC Board).
LB-	3-31/2	Left Bank. Selects data buffer on left bank of 8X300 IV bus.
LPT0+-LPT7+	3-25/4 3-31/8	Line Printer Data 0-7. Data output to line printer.
LPTBUSY+	3-25/4 3-31/8	Line Printer Busy. Status line from line printer.
LPTCS-	3-25/4 3-31/8	Line Printer Chip Select. Used to select the line printer interface.
M+/IO-	3-14/2	Memory or Input/Output Decode. Output from the CPU during a memory or input/output operation.
MA0+-MA7+	3-3/3 3-14/4	Memory Address 0-7. RAM array address lines.
MCLK-	3-31/2	Master Clock. Clock output from 8X300.
MEMOK+	3-3/3 3-14/4	Memory OK. Indicates that a normal memory cycle is complete or will complete shortly.
MEMR-	3-3/2 3-14/4	Memory Write. Memory write strobe from the 8257.

Signal Name	Figure/Page	Description
MEMW-	3-3/2 3-14/2	Memory Write. Memory write strobe from the 8257.
MOT0+-MOT1+	3-25/3	Motor 0-1. Used to select floppy disk drive motor on FDC Board.
MR-	3-3/2 3-14/2	Memory Read. Buffered memory read strobe from CPU or 8257.
MRDY+	3-3/3 3-14/4	Memory Ready. Ready signal to 8257.
MW-	3-3/2 3-14/2	Memory Write. Buffered memory write strobe from CPU or 8257.
NMI+	3-3/2 3-14/2	Nonmaskable Interrupt. Input to CPU from parity logic.
NOPAPER+	3-25/4 3-31/8	No Paper. Status bit from line printer.
NORMCYC+ and -	3-3/3 3-14/4	Normal Cycle. Indicates that a normal memory cycle (nonrefresh) is in progress.
NORMRDY-	3-3/3 3-14/4	Normal Cycle Ready. From memory logic to indicate that a normal cycle is complete.
ONBDINT+	3-3/4 3-14/5 3-25/2 3-31/6	On-Board Interrupt. Output from 7201 on CPU Board. Indicates that an interrupt from an input/output device on the CPU Board has occurred.
PBHE-	3-14/2	Processor Bus High Enable. See BHE- above.
PCLOCK+	3-3/2 3-14/2	Processor Clock. A 5 MHz (8088) or 8 MHz (8086) clock to the CPU and memory logic.

Signal Name	Figure/Page	Description
POWERFAIL-	3-31/6	Power Failure. To 8X330 floppy disk controller.
RAMCYC-	3-3/3 3-14/4	RAM Cycle. Indicates that a RAM memory cycle is in progress.
RAMMR-	3-3/3 3-14/4	RAM Memory Read. Indicates a RAM memory read cycle.
RAS-	3-3/3 3-14/4	Row Address Strobe. Memory row address strobe.
RB-	3-31/2	Right Bank. Selects input/output devices on right bank of 8X300 IV bus.
RDDAT+	3-31/3	Read Data. From HDC Board data separator.
RDDAT+ and -	3-25/6	Read Data. Read data input to (RDDAT-) and output from (RDDAT+) the floppy data separator.
RDDLY1+	3-31/4	Read Delay. To HDC Board address mark detector.
RDW+	3-25/6	Read Window. Data read window generated by the FDC Board data separater.
READY+	3-3/3 3-14/2	Ready. Ready signal from the memory logic.
READY-	3-25/5 3-31/3	Drive Ready. Input to disk drive controller.
RES-	3-3/2 3-14/2	Reset In. Reset Switch input to 8284(A) clock generator. Use to generate RESET+.
RESET+	3-3/2 3-14/2	General Purpose System Reset. Master reset signal for the CPU Board.

Signal Name	Figure/Page	Description
RFADR-	3-3/3 3-14/4	Refresh Address. Sets the refresh address in the RAM array.
RFRAS-	3-3/3 3-14/4	Refresh Row Address Strobe. Row address strobe for refresh cycle.
RFRDY-	3-3/3 3-14/4	Refresh Ready. Indicates that a RAM refresh cycle is complete.
ROMSUP-	3-3/3 3-14/3 3-25/4 3-31/8	ROM Suppress. Used by the FDC or HDC Board to suppress the CPU Board ROM.
ROWMUX-	3-3/3 3-14/4	Row Multiplex. RAM row multiplex strobe.
RST-	3-31/2	Reset. 8X300 reset.
RXCA+ and -	3-3/4 3-14/5	Receive Clock Channel A. Differential inputs to the 7201 on the CPU Board for cluster communications clock.
RXDA+ and -	3-3/4 3-14/5	Receive Data Channel A. Differential inputs to the 7201 on the CPU Board for cluster communications data.
SC+	3-31/2	Select Command. Command strobe from 8X300.
SELECT+	3-25/4 3-31/8	Line Printer Selected. Status line from line printer.
SKCOMP-	3-31/3	Seek Complete. From floppy disk drives on HDC Board.
STACKEN-	3-14/2	Stack Enable. Used during a ROM read cycle to stack two bytes for the CPU to read.

Signal Name	Figure/Page	Description
STROBE-	3-25/4 3-31/8	Character Strobe. To line printer.
TC+	3-3/2 3-14/2 3-25/2 3-31/6	Terminal Count. Terminal DMA address count from the 8257 to the disk controller.
TMRD-	3-14/5	Timer Read. Delayed 8253 read strobe from the CPU.
TMWR-	3-14/5	Timer Write Delayed 8253 write strobe from the CPU.
VCO	3-25/5	Voltage-Controlled Oscillator. Output from 8272 on the FDC Board.
VIDACK-	3-3/2 3-14/2	Video DMA Acknowledge. Output from 8257 to acknowledge a video DMA request.
VIDRQ+	3-3/5 3-14/6	Video DMA Request. DMA request from video display control logic to 8257.
VRTC+	3-3/5 3-14/6	Vertical Retrace. Video vertical retrace output of the 8275.
VSP+	3-3/5 3-14/6	Video Suppress. Video blanking output from the 8275.
WAIT1+-WAIT2+	3-3/3	Memory Wait 1 and 2. Indicates 1 or 2 wait states for a memory cycle.
WC+	3-31/2	Write Command Strobe. From 8X300.
WE0- and WE1-	3-3/3 3-14/3	Write Enable 0 and 1. Write enable signals to the RAM array.
WMF	3-31/5	Write MFM Data. Write data to Hard disk drive.
WOSC+ and -	3-31/5	Write Oscillator. For hard disk write circuits.

Signal Name	Figure/Page	Description
WRDATA-	3-31/3	Write Data. From 8X300 floppy controller to disk drive.
WRPROT-	3-31/3	Write Protect. From disk drive to 8X330.
WRTOP+	3-31/2	Write Operation. From 8X330 to indicate a write operation.

APPENDIX G: FLOPPY DISK DRIVE MANUFACTURER'S MANUAL

Shugart, Model SA410/460

Shugart

475 Oakmead Parkway, Sunnyvale, CA 94086 Telephone: (408) 733-0100

PUBLICATION CHANGE NOTICE

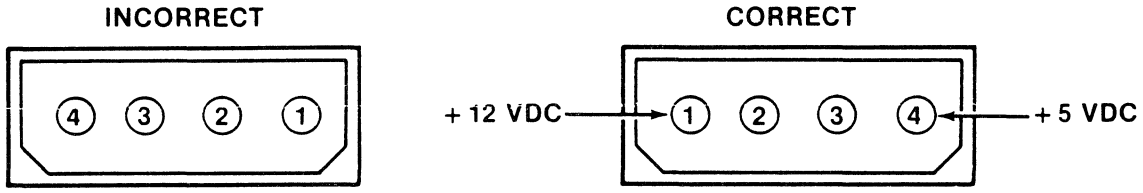
PN: 39024-0 + -1 **Product:** SA410/460 **Date:** 10-29-81 **Errata: #** 1

Pub. Date: 9/80 & 6/81 **Pub. Type:** OEM

Subject: J2 pin designations

Figure 20 (page 20, P/N 39024-0 and page 18, P/N 39024-1) shows pin numbers in reverse order. Make ink corrections to the figures as follows:

Page 20, P/N 39024-0



Page 18, P/N 39024-1

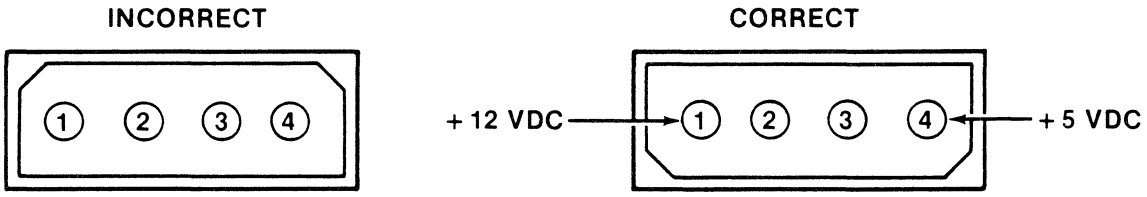


TABLE OF CONTENTS

TABLE OF CONTENTS (CON'T)

LIST OF ILLUSTRATIONS

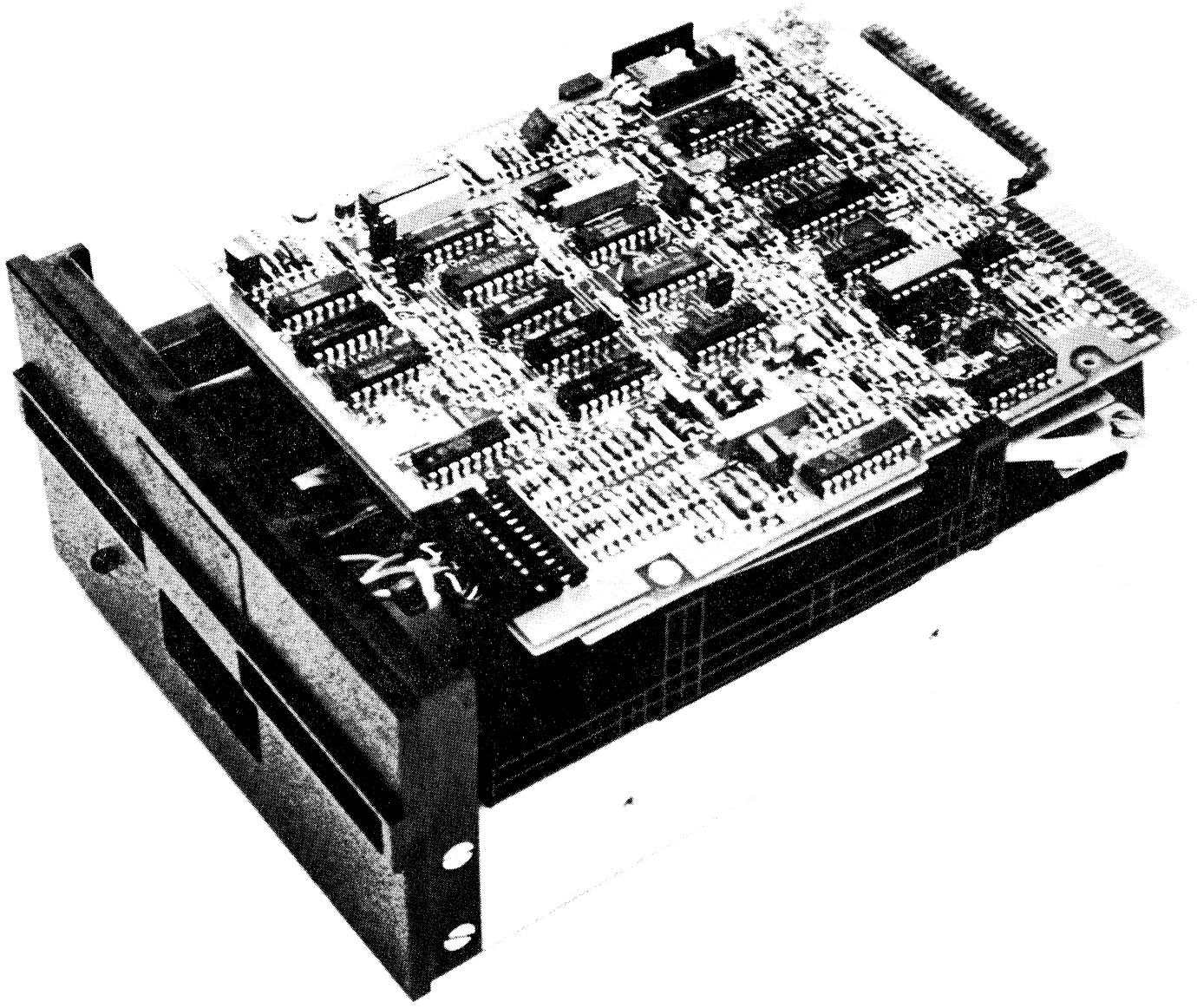


FIGURE 1. SA410/460 96 TPI MINIFLOPPYS

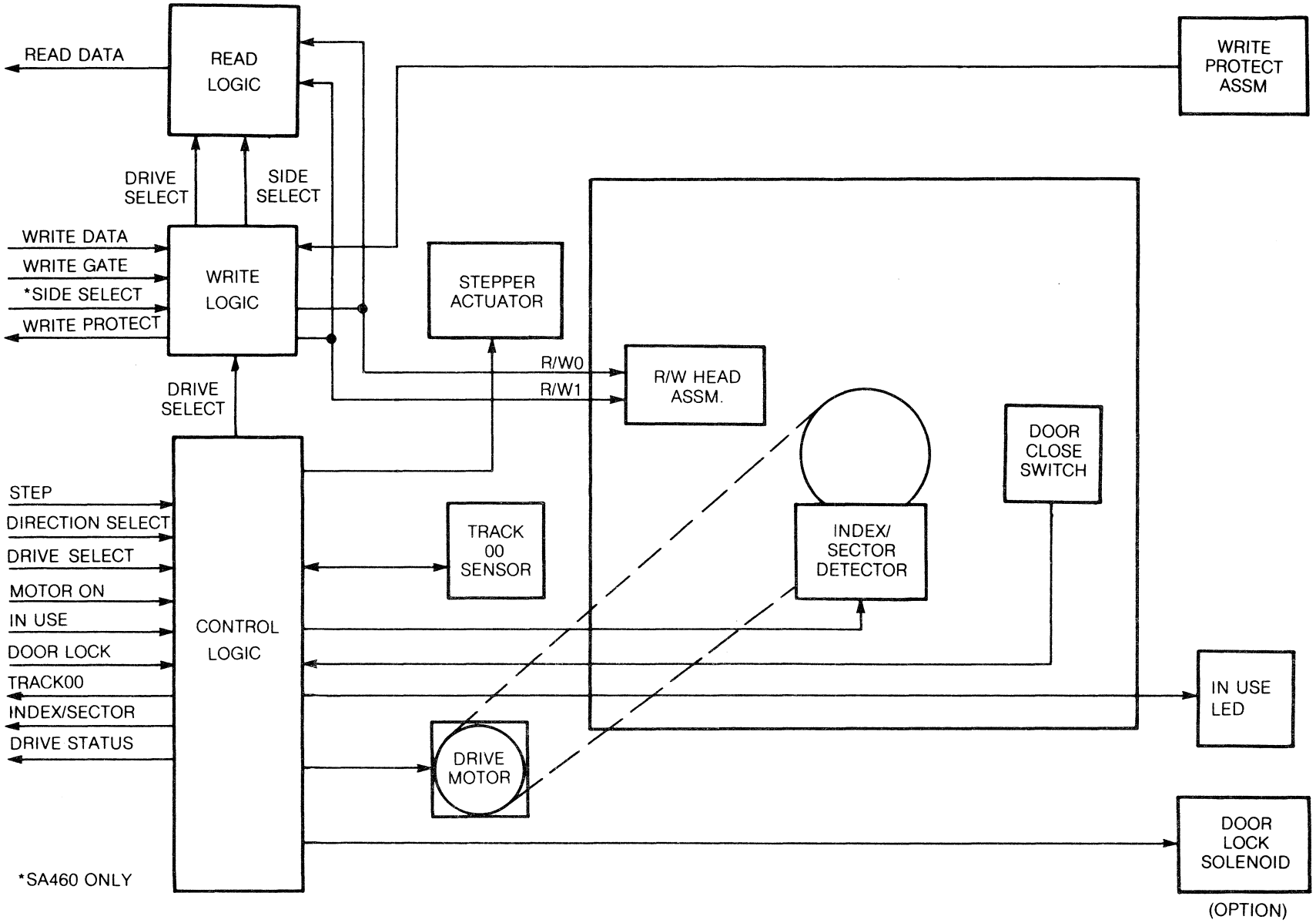


FIGURE 2. SA410/460 FUNCTIONAL DIAGRAM

1.0 INTRODUCTION

1.1 General Description

The compact SA410 single-sided and SA460 double-sided, 96 TPI, Minifloppy™ disk drives offer a reliable, low cost, high performance solution for OEM data storage applications which require maximum capacity in a Minifloppy. The SA410/460 Minifloppy drives are less than one-half the size of Shugart's standard SA801 floppy disk drive, fit comfortably in the space allocated for most tape cassette units, and offer up to one megabyte of unformatted capacity.

SA410/460 Minifloppy drives have these standard features: compact size - just 3.25" high × 5.75" wide × 8.25" deep, and weight of three pounds; low heat dissipation; positive media insertion to keep door from closing on media; rapid start DC drive motor with precision servo speed control and integral tachometer; direct drive stepping motor actuator with precise HeliCam™ V-groove lead screw; ball bearing anti-backlash followers; read/write head assembly; internal write protect circuitry; activity light, and solid die cast chassis.

The SA410 and SA460 are your best choices for word processing systems, microprocessor based systems, 'intelligent' calculators, program storage, personal computer systems and other applications where low cost higher capacity random access data storage is required. The SA410/460 offers the most cost effective data storage of any flexible media disk drive.

Key Features

- 96 Track per inch
- Precise HeliCam™ Actuator
- 0.5/1 MByte (unformatted) capacity
- SA400/450 I/O compatibility
- Same compact size and weight as the SA400/450 - similar to most tape cassette units
- 125/250 Kbits/second transfer rate
- Single and double density capability
- Low heat dissipation
- Positive media insertion to avoid media damage
- Rapid start DC drive motor (eliminates AC requirements)
- Shugart Bi-Compliant™ read/write head assembly on SA460
- Write protect circuitry
- Activity light
- Door Lock Solenoid
- Drive Status

1.2 Specification Summary

1.2.1 Performance Specifications

	SA410	**SA460**
Capacity	Single/Double Density	Single/Double Density
Unformatted		
Per Disk	250/500 KBytes	0.5/1 MByte
Per Surface	250/500 KBytes	250/500 KBytes
Per Track	3.1/6.2 KBytes	3.1/6.2 KBytes
Formatted (10 Sector/Track)		
Per Disk	204.8/409.6 KBytes	409.6/819.2 KBytes
Per Surface	204.8/409.6 KBytes	204.8/409.6 KBytes
Per Track	256/512 KBytes	256/512 KBytes
Transfer Rate	125/250 Kbits/sec	125/250 Kbits/sec
Latency (avg.)	100 msec	100 msec
Access Time (w/o settling)		
Track to Track	6 msec	6 msec
Side to Side	--	0.2 msec
Average	158 msec	158 msec

	SA410	SA460
Settling Time	15 msec	15 msec
Motor Start Time	200 msec	200 msec

1.2.2 Functional Specifications

Rotational Speed	300 rpm	300 rpm
Recording Density (inside track)	2788/5576 bpi	2961/5922 bpi
Flux Density	5576 fci	5922 fci
Track Density	96 tpi	96 tpi
Tracks	80	80
Index	1	1
Encoding Method	FM/MFM	FM/MFM
Media Requirements		
soft sectored	SA114	SA164
16 sectors hard sectored	SA115	SA165
10 sectors hard sectored	SA117	SA167

Industry standard flexible diskette
Oxide on 0.003 in. (0.08mm) Mylar
5.25 in. (133.4mm) square jacket

1.2.3 Physical Specifications

Environmental Limits	*Operating*	*Shipping*
Ambient Temperature =	40°F to 115°F (4.4°C to 46.1°C)	-40° to 144°F (-40°C to 62°C)
Relative Humidity =	20% to 80%	1% to 95%
Maximum Wet Bulb =	78°F (25.6°C)	no condensation

Storage
-8°F to 117°F (-22°C to 47°C)
1% to 95%
no condensation

DC Voltage Requirements
+12V ± 5% @ 1.3A typical, 2.2A MAX
+ 5V ± 5% @ 0.5A typical, 0.7A MAX

Mechanical Dimensions (exclusive of front panel)
Width = 5.75 in. (146.1mm)
Height = 3.25 in. (82.6mm)
Depth = 8.25 in. (205mm)
Weight = 3 lbs. 3 ozs. (1.44 Kg) Nominal)

Power Dissipation =
18.2 watts (62.1 BTU/Hr) Continuous (typical)
14.6 watts (49.8 BTU/Hr) Standby (typical)

1.2.4 Reliability Specifications

MTBF: 8000 POH under typical usage*
*Assumes the duty cycle of the drive spindle motor to be 25%
PM: Not required
MTTR: 30 minutes
Component Life: 5 years

Error Rates:
Soft Read Errors: 1 per 10^9 bits read
Hard Read Errors: 1 per 10^{12} bits read
Seek Errors: 1 per 10^6 seeks

Media Life:
Passes per Track: 3.0×10^6
Insertions: 30,000 +

2.0 FUNCTIONAL CHARACTERISTICS

The SA410/460 Minifloppy disk drives consist of:

1. Read/Write and Control Electronics
2. Drive Mechanism
3. Precision Track Positioning Mechanism
4. Read/Write Head(s)

2.1 Electronics

The electronics are packaged on one PCB which contains:

1. Index Detector Circuits
2. Head Position Actuator Driver
3. Read/Write Amplifier and Transition Detector
4. Write Protect
5. Drive Select Circuits
6. Spindle Motor Control

The Head Positioning Actuator moves the read/write head(s) to the desired track on the diskette. The head(s) are loaded onto the diskette when the door is closed.

2.2 Drive Mechanism

The DC drive motor under servo speed control (using an integral tachometer) rotates the spindle at 300 rpm through a belt-drive system. An expandable collet/spindle assembly provides precision media positioning to ensure data interchange. A mechanical interlock prevents door closure without proper media insertion, thus eliminating media damage.

2.3 Positioning Mechanism

The read/write head assembly is accurately positioned through the use of a precision HeliCam V-groove lead screw with a ball follower which is attached to the head carriage assembly. Precise track location is accomplished as the lead screw is rotated in discrete increments by a stepping motor.

2.4 Read/Write Head(s)

The glass bonded ceramic and ferrite read/write head(s) contain tunnel erase elements to provide erased areas between data tracks. Thus normal interchange tolerances between media and drives will not degrade the signal to noise ratio and diskette interchangeability is insured.

The read/write head(s) are mounted on a carriage which is located on precision carriage ways. The diskette is held in a plane perpendicular to the read/write head(s) by a platen located on the base casting. This precise registration assures perfect compliance with the read/write head(s). The read/write head(s) is in direct contact with the diskette. The head surfaces have been designed to obtain maximum signal transfer to and from the magnetic surface of the diskette with minimum head/diskette wear.

2.5 Recording Formats

The format of the data recorded on the diskette is totally a function of the host system, and can be designed around the users application to take maximum advantage of the total available bits that can be written on any one track.

For a detailed discussion of the various recording formats refer to Section 7.0.

3.0 FUNCTIONAL OPERATIONS

3.1 Power Sequencing

Applying DC power to the SA410 or SA460 can be done in any sequence; however, during power up, the WRITE GATE line must be held inactive or at a high level. After application of DC power, a 100 ms delay should be introduced before any operation is performed. Also, after powering on, initial position of the read/write heads with respect to the data tracks on the media is indeterminant. In order to assure proper positioning of the read/write heads after power on, a Step Out operation should be performed until the Track 00 line becomes active (Recalibrate).

3.2 Drive Selection

Drive selection occurs when a drive's DRIVE SELECT line is activated. Only the drive with this line active will respond to input lines or gate output lines. Under normal operation, the DRIVE SELECT line enables the input and output lines and lights the Activity LED on the front of the drive.

3.3 Motor On

In order for the host system to read or write data the DC drive motor must be turned on. This may be accomplished by activating the line MOTOR ON. A 200 ms delay must be introduced after activating this line to allow the motor to come up to speed before reading or writing can be accomplished.

The motor must be turned off by the host system by deactivating the MOTOR ON line. This should be done if the drive has not received a new command within two (2) seconds (10 revolutions of diskette) after completing the execution of a command. This will insure maximum motor and media life. **Note:** All motors in a daisy chain configuration are turned on with MOTOR ON. Reference sections 4.1.1.2 and 4.1.1.3.

3.4 Track Accessing

Seeking the read/write heads from one track to another is accomplished by:

a. Activating DRIVE SELECT line.

b. Selecting desired direction utilizing DIRECTION SELECT line.

c. WRITE GATE being inactive.

d. Pulsing the STEP line.

Multiple track accessing is accomplished by repeated pulsing of the STEP line until the desired track has been reached. Each pulse on the STEP line will cause the read/write heads to move one track either in or out depending on the DIRECTION SELECT line. Head movement is initiated on the trailing edge of the STEP pulse.

3.4.1 Step Out

With the DIRECTION SELECT line at a plus logic level (2.5V to 5.25V) a pulse on the STEP line will cause the read/write heads to move one track away from the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in Figure 3.

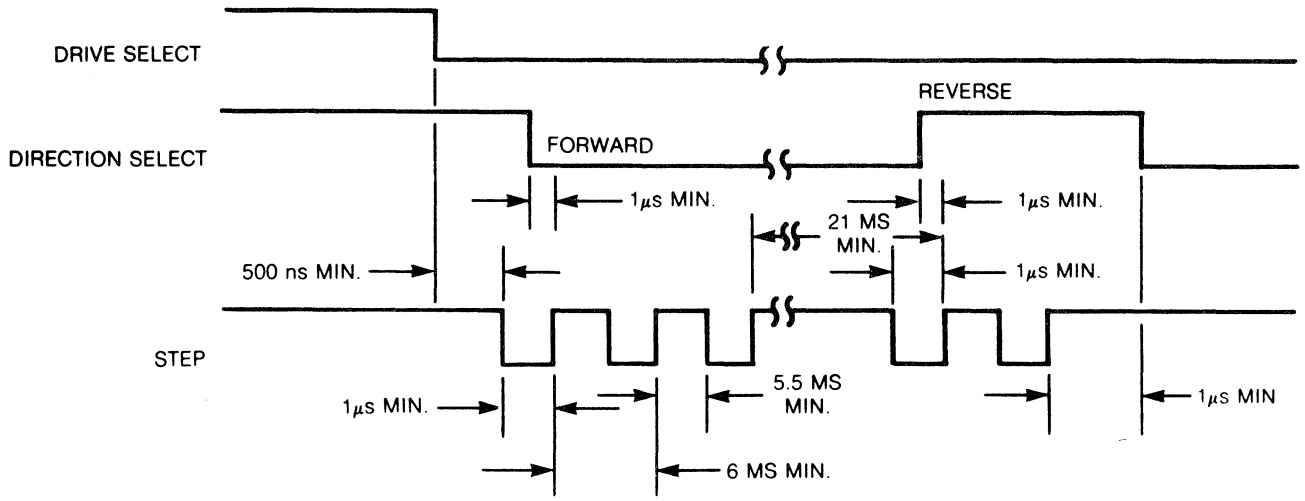


FIGURE 3. TRACK ACCESS TIMING

3.4.2 Step In

With the DIRECTION SELECT line at minus logic level (0V to .4V), a pulse on the STEP line will cause the read/write heads to move one track closer to the center of the disk. The pulse(s) applied to the STEP line must have the timing characteristics shown in Figure 3.

3.5 Side Selection (SA460 only)

Head Selection is controlled via the I/O signal line designated SIDE SELECT. A plus logic level on the SIDE SELECT line selects the read/write head on the side 0 surface of the diskette. A minus logic level selects the side 1 read/write head. When switching from one side to the other. A 200μs delay is required after SIDE SELECT changes state before a read or write operation can be initiated. Side select should not change state for a minimum of 1.1 msec after write gate is terminated. Figure 4 shows the use of SIDE SELECT prior to a read operation.

3.6 Read Operation

Reading data from the SA410/460 minifloppy drive is accomplished by:

a. Activating DRIVE SELECT line.

b. Selecting Head (SA460 only).

c. WRITE GATE being inactive.

The timing relationships required to initiate a read sequence are shown in Figure 4. These timing specifications are required in order to guarantee that the read/write heads position has stabilized prior to reading.

The timing of Read Data (FM) is shown in Figure 5.

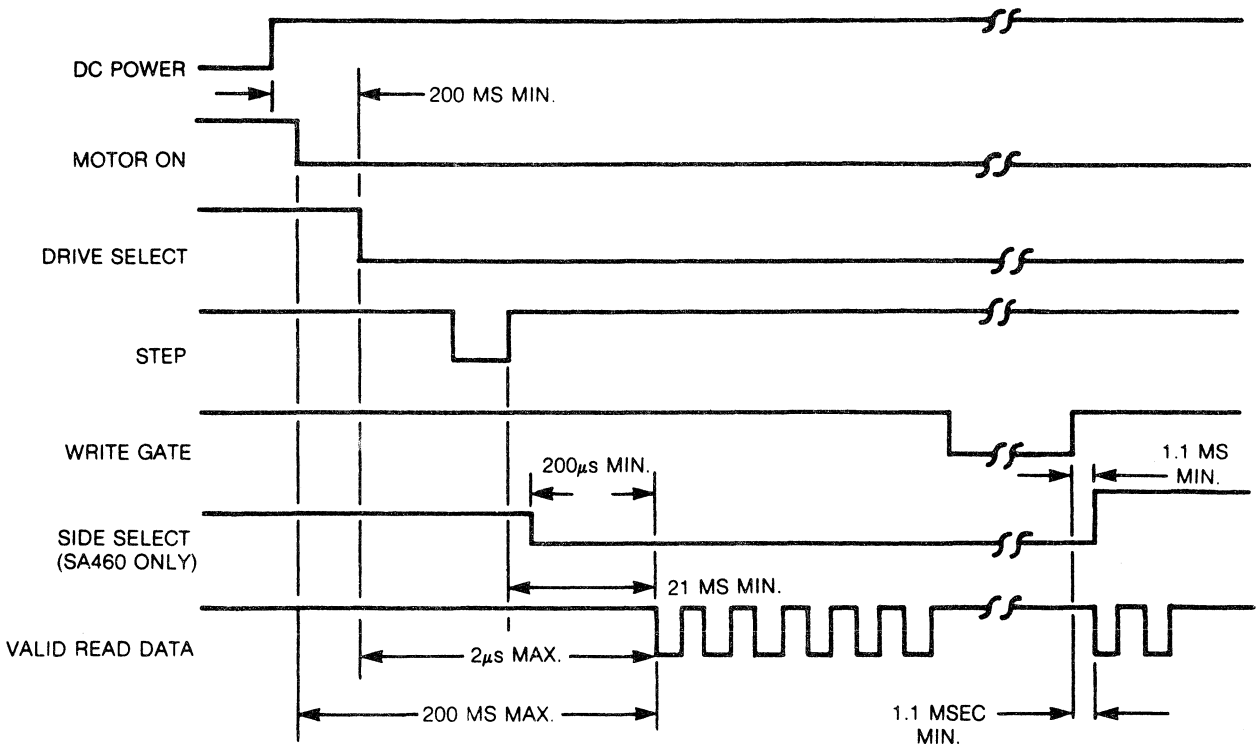
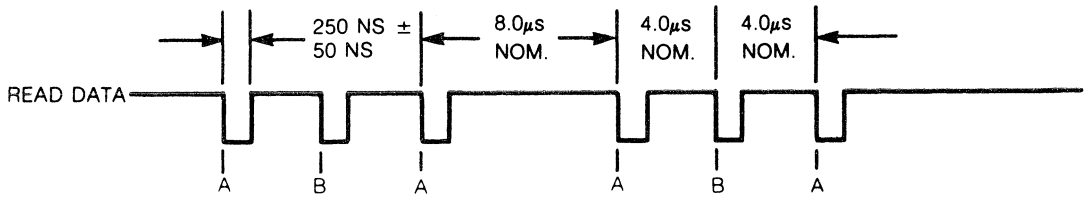


FIGURE 4. READ INITIATE TIMING



A = LEADING EDGE OF BIT MAY BE ± 800 ns FROM ITS NOMINAL POSITION
B = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION

FIGURE 5. READ DATA TIMING (FM)

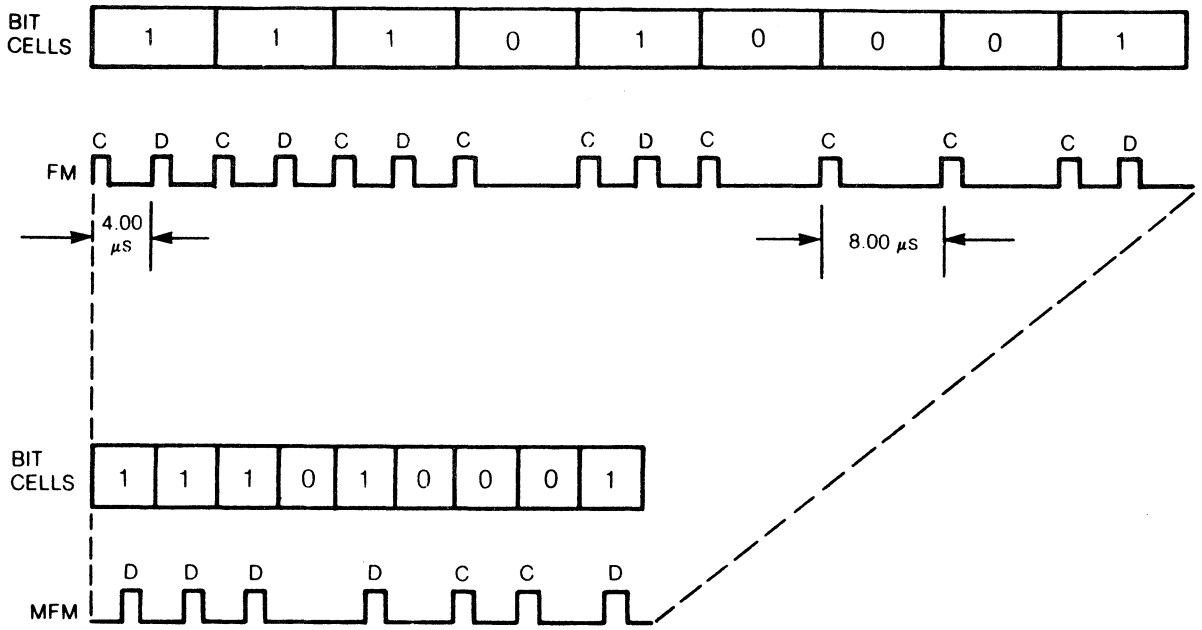


FIGURE 6. FM AND MFM CODE COMPARISONS

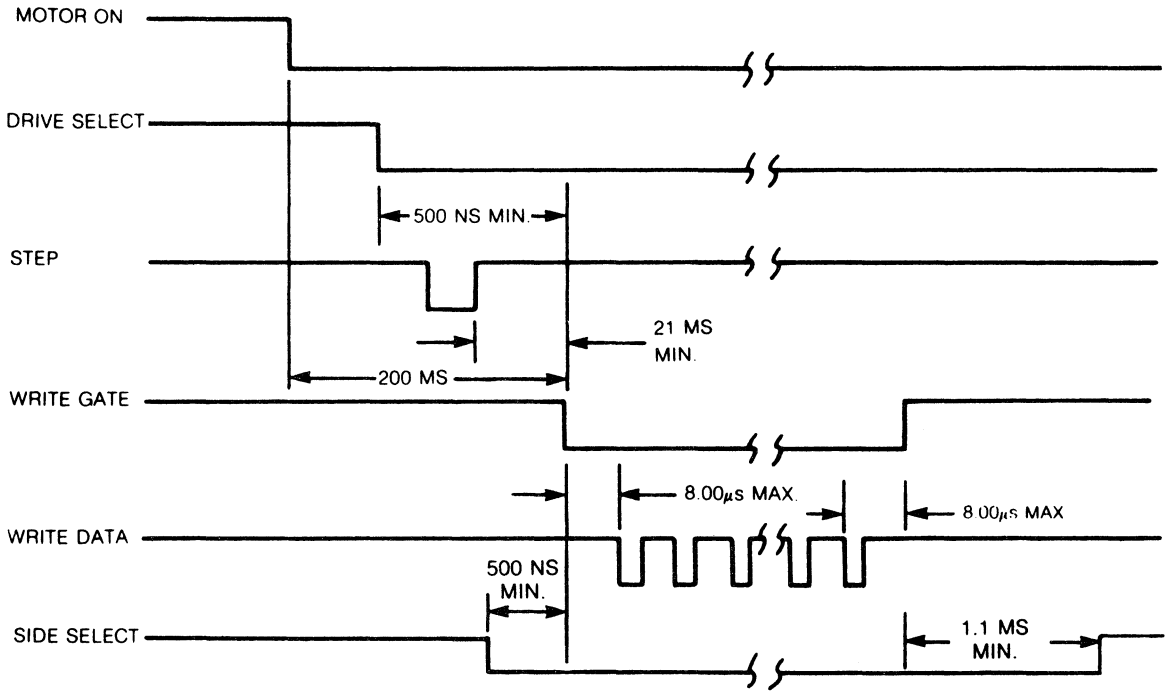


FIGURE 7. WRITE INITIATE TIMING

The encoding scheme of the recorded data can be either FM or MFM. FM encoding rules specify a clock bit at the start of every bit cell (Refer to Figure 6). MFM encoding rules allow clock bits to be omitted from some bit cells, with the following prerequisites:

The clock bit is omitted from the current bit cell if either the preceding bit cell or the current bit cell contains a data bit. See Figure 6.

In the above mentioned encoding schemes, clock bits are written at the start of their respective bits cells and data bits at the centers of their bit cells.

3.7 Write Operation

Writing data to the SA410/460 is accomplished by:

a. Activating the DRIVE SELECT line.

b. Selecting Head (SA460 only).

c. Activating the WRITE GATE line.

d. Pulsing the WRITE DATA line with the data to be written.

The timing relationships required to initiate a Write Data sequence are shown in Figure 7. These timing specifications are required in order to guarantee that the read/write head's position has stabilized prior to writing. Drive select, or side select (SA460), may not change nor a step command be issued for a minimum of 1.1 msec after write gate is returned to an inactive state (refer to paragraph 4.1.1.7).

The timing specifications for the Write Data pulses are shown in Figure 8.

Write data encoding can be FM or MFM. The write data should be precompensated 100 ns on all tracks to counter the effects of bit shift. The direction of compensation required for any given bit in the data stream depends on the pattern it forms with nearby bits.

3.8 Sequence of Events

The timing diagram shown in Figure 9 shows the necessary sequence of events with associated timing restrictions for proper operation.

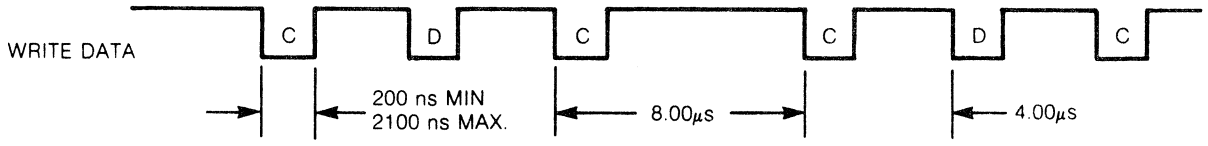


FIGURE 8. WRITE DATA TIMING (FM)

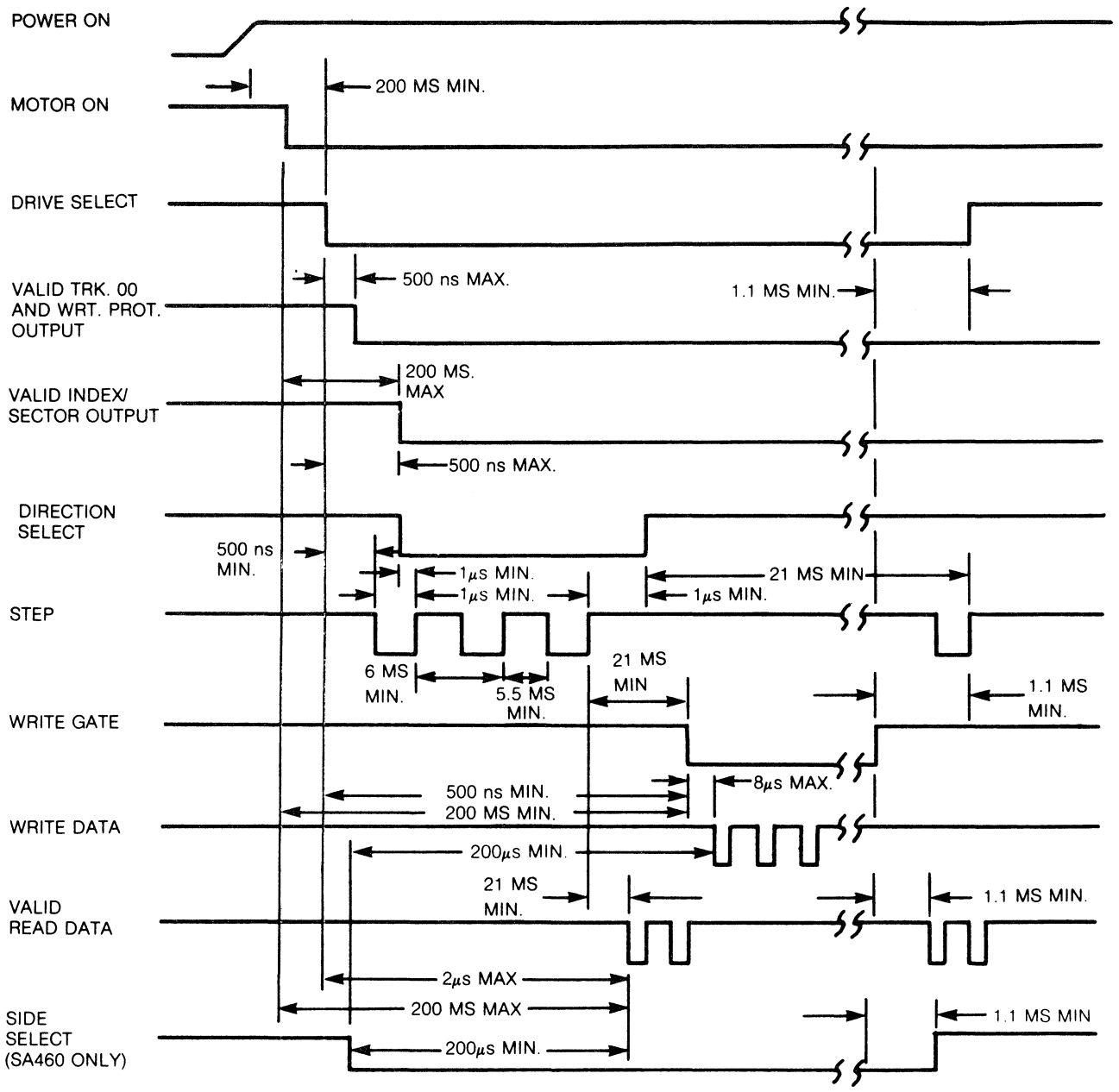


FIGURE 9. GENERAL CONTROL AND DATA TIMING REQUIREMENTS

4.0 ELECTRICAL INTERFACE

The interface of the SA410/460 minidiskette drives can be divided into two categories:

1. Signal

2. Power

The following sections provide the electrical definition for each line.

Refer to figure 10 for all interface connections.

Refer to section 8.0 for description of options.

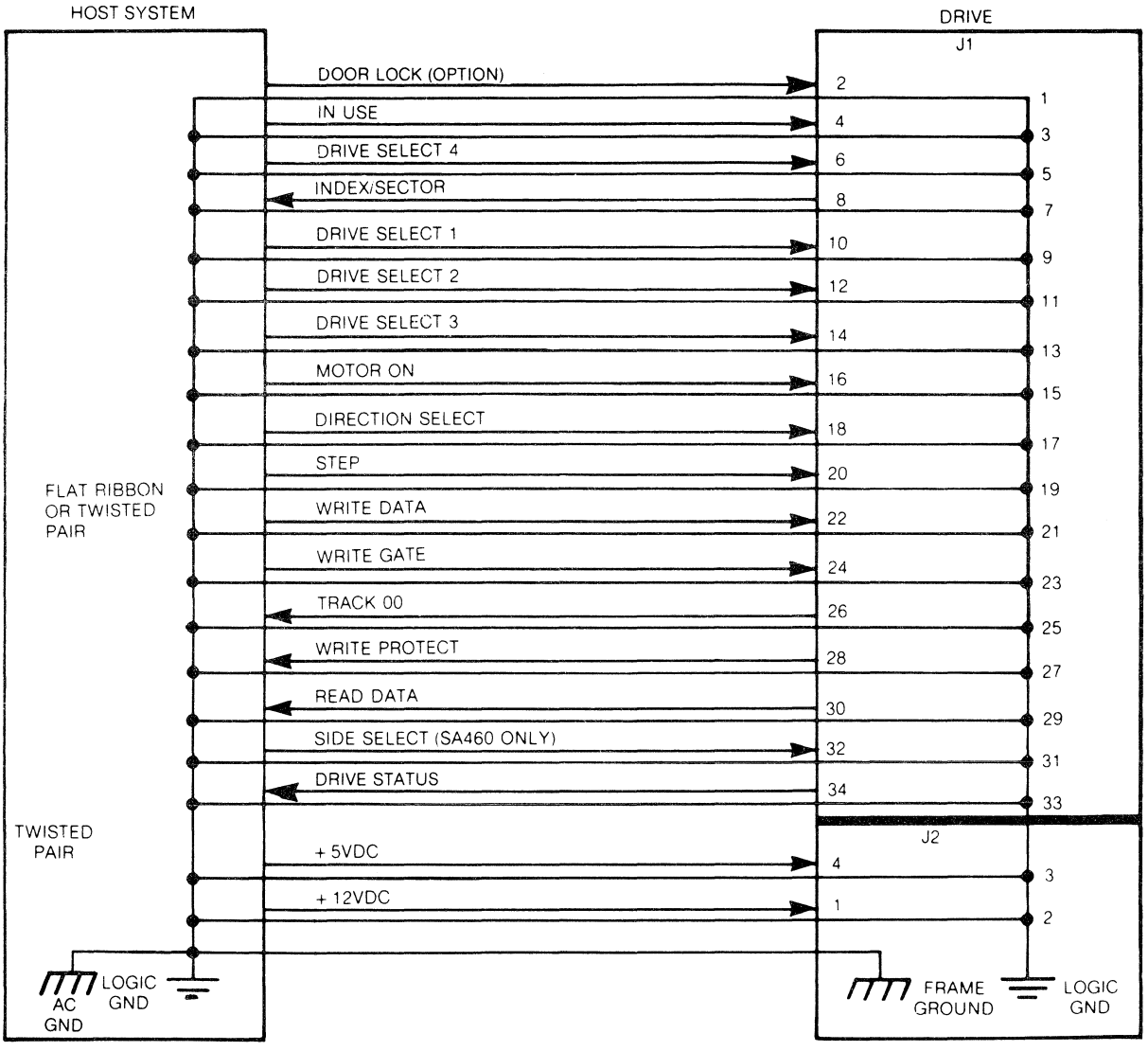


FIGURE 10. INTERFACE CONNECTIONS

4.1 Signal Interface

The signal interface consists of two categories:

1. Control

2. Data Transfer

All lines in the signal interface are digital in nature and either provide signals to the drive (input), or provide signals to the host (output), via interface connector P1/J1.

4.1.1 Input Lines

The input signals are of 3 types, those intended to be multiplexed in a multiple drive system, those which will perform the multiplexing and those signals which are not multiplexed and affect all the drives in a daisy chain system.

The input signals to be multiplexed are:

1. DIRECTION SELECT

2. STEP

3. WRITE DATA

4. WRITE GATE

5. SIDE SELECT (SA460 only)

The input signals which are intended to do the multiplexing are:

1. DRIVE SELECT 1

2. DRIVE SELECT 2

3. DRIVE SELECT 3

4. DRIVE SELECT 4

The signals which are not multiplexed are IN USE and MOTOR ON.

The input lines have the following electrical specifications Refer to Figure 11 for the recommended circuit.

True = Logical zero = Vin 0.0V to +.04V @ 40 ma (max)

False = Logical one = Vin + 2.5V to +5.25V @ 250μa (open)

Input impedance = 220/330ohms

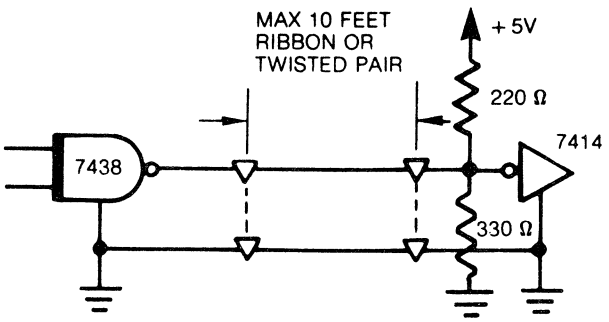


FIGURE 11. INTERFACE SIGNAL DRIVER/RECEIVER

4.1.1.1 Input Line Terminations

The SA410/460 has been provided with the capability of terminating the eight input lines listed below.

1. MOTOR ON
2. DIRECTION SELECT
3. STEP
4. WRITE DATA
5. WRITE GATE
6. SIDE SELECT (SA460 only)
7. DOOR LOCK
8. IN USE

These lines are terminated through a 220/330 ohm resistor pack installed in a dip socket.

In a single drive system this resistor pack should be kept in place to provide the proper terminations.

In a multiple drive system only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. External terminations may also be used, then the user must provide the terminations beyond the last drive and each of the eight lines must be terminated to +5VDC through a 220/330 ohm 1/4 watt resistor.

4.1.1.2 DRIVE SELECT 1-4

The SA460 or SA410 is configured to operate with up to four drives in a multiplexed multiple drive system.

SINGLE DRIVE SYSTEM (MX shorting plug installed)

With the MS shorting plug installed, DRIVE SELECT when activated to a logical zero level will turn the motor on. With MX shorted, the I/O lines are always enabled.

MULTIPLE DRIVE SYSTEM (MX shorting plug not installed)

Four separate input lines (DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 and DRIVE SELECT 4) are provided so that up to four drives in a multiplexed system may have separate input pins. Only the drive with its unique DRIVE SELECT line active will turn its motor on, allow the drive to respond to multiplexed input lines and enable the outputs to drive their respective signal lines. A logic zero on the interface selects a unique drive select line for a drive.

4.1.1.3 MOTOR ON

This input, when activated to a logical zero level, will turn on the drive motor allowing reading or writing on the drive. A 0.2 second delay after activating this line must be allowed before reading or writing. This line should be deactivated, for maximum motor life, if no commands have been issued to the drives within two seconds nominal (10 revolutions of the media) after completion of a previous command. This time may be varied by the host system to maximize system through-put and motor life depending on application.

As discussed in section 4.1.1.2, when MS is shorted the motor will turn on when the DRIVE SELECT line is activated or if the MOTOR ON line is activated. A user selectable option is available where by the motor will turn on only when the MOTOR ON line is activated.

4.1.1.4 Direction Select

This interface line defines direction of motion the read/write heads will take when the STEP line is pulsed. An open circuit or logical one defines the direction as "out" and if a pulse is applied to the STEP line the read/write heads will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in" and if a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

4.1.1.5 Step

This interface line is a control signal which causes the read/write heads to move with the direction of motion as defined by the DIRECTION SELECT line. This signal must be a logical zero going pulse with a minium pulse width of 1μs and a logical one for 5.5 ms minimum between adjacent pulses. Each subsequent pulse must be delayed by 6 ms minimum from the preceeding pulse.

The access motion is initiated on each logical zero to logical one transition, or the trailing edge of the signal pulse. Any change in the DIRECTION SELECT line must be made at least 1μs before the trailing edge of the STEP pulse. the DIRECTION SELECT logic level must be maintained 1μs after trailing edge of STEP pulse. Refer to Figure 12 for these timings.

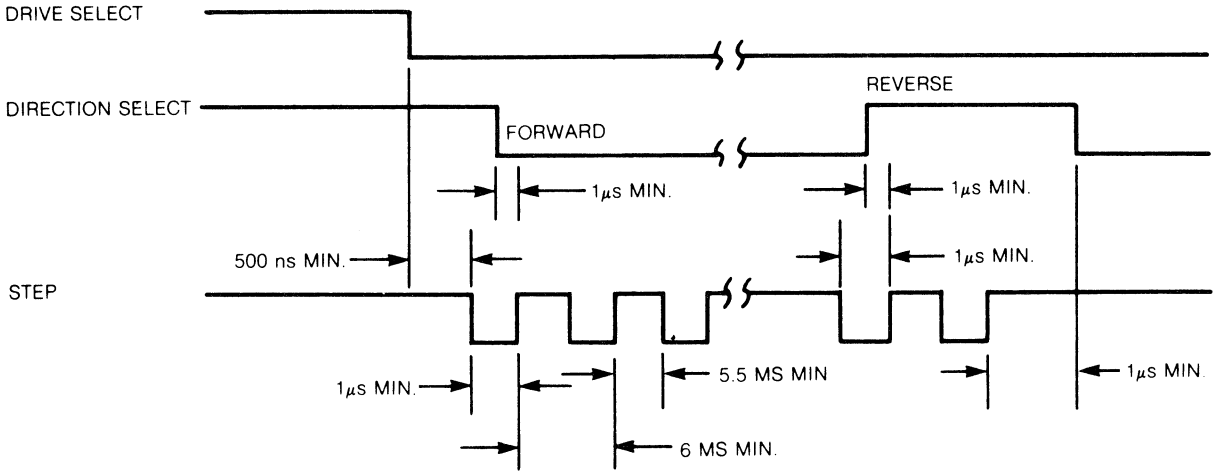


FIGURE 12. STEP TIMING

4.1.1.6 Write Gate

The active state of this signal, or logical zero, enables Write Data to be written on the diskette. The inactive state or logical one, enables the read data logic and stepper logic. Refer to Figure 7 for timings.

4.1.1.7 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level, will cause the current through the read/write heads to be reversed thereby writing a data bit. This line is enabled by Write Gate being active. Write Data must be inactive during a read operation. Refer to Figure 13 for timings.

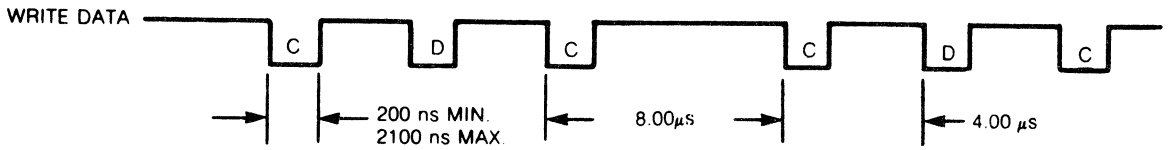


FIGURE 13. WRITE DATA TIMING (FM ENCODING)

4.1.1.8 Side Select (SA460 only)

This signal defines which side of a two-sided diskette is to be written to or read from. A logical one selects the side 0 head. When switching from one side to the other a 200 μs delay is required before a read operation can be initiated. A delay of 1.1 ms is required after a write operation before changing the state of side select.

4.1.1.9 In Use

Normally, the activity LED on the selected drive will turn on when the corresponding DRIVE SELECT signal is active. The IN USE input can alternately activate the LED on all the drives in a daisy chain or separately in a radial configuration.

4.1.2 Output Lines

The output control lines have the following electrical specifications. Refer to Figure 11 for the recommended circuit.

True = Logical zero = Vout + 0.0V to + 0.4V @ 40 ma (max)

False = Logical one = Vout + 2.5V (open collector @ 250μa max)

4.1.2.1 Track 00

The active or logical zero state of this interface signal indicates when the drive's read/write heads are positioned at track zero (the outermost track) and the stepper is locked on track. This signal is at a logical one level, or inactive state, when the drive's read/write heads are not at track zero. When the drive's read/write heads are at track zero and an additional step out pulse is issued to the drive, a mechanical stop will keep the read/write heads at track zero.

4.1.2.2 Index/Sector

This interface signal is provided by the drive each time an index or sector hole is sensed at the Index/Sector photo detector. Normally, this signal is at a logical one level and makes the transition to the logical zero level each time a hole is sensed.

When using media Soft Sectored, there will be one pulse on this interface signal per revolution of the diskette (200 ms). This pulse indicates the physical beginning of a track. Refer to Figure 14.

When using the Index/Sector signal, look for an edge or transition rather than a level for determining its status. With no diskette inserted, this signal remains active or at a logical zero level which is an erroneous status.

4.1.2.3 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. Refer to Figure 17 for the timing and bit shift tolerance within normal media variations.

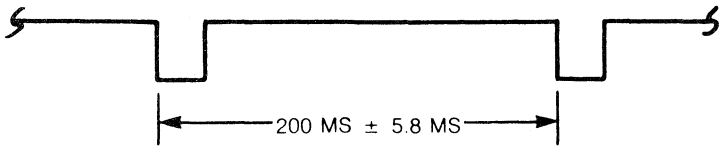


FIGURE 14. INDEX TIMING (SOFT SECTORED MEDIA)

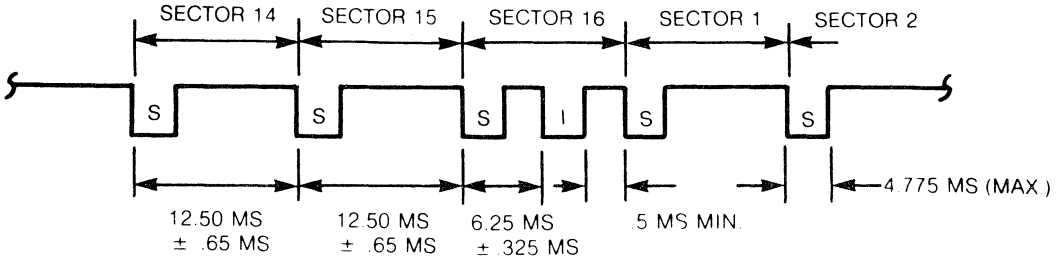


FIGURE 15. INDEX/SECTOR TIMING (SA115 OR SA165 MEDIA)

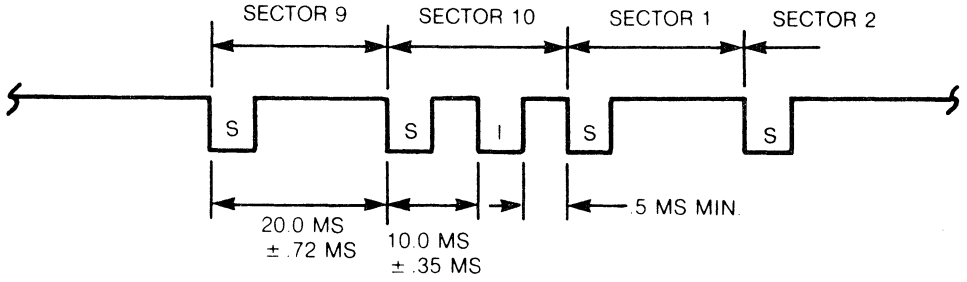
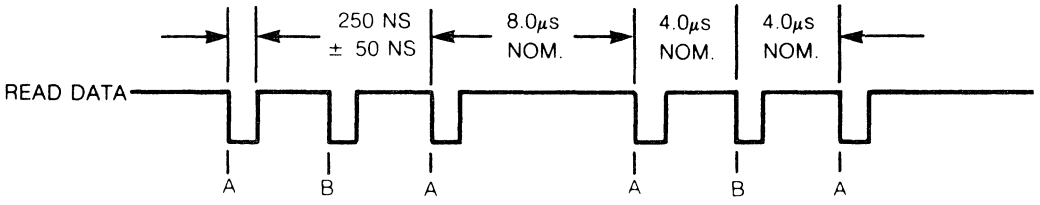


FIGURE 16. INDEX/SECTOR TIMING (SA117 OR SA167 MEDIA)



A = LEADING EDGE OF BIT MAY BE ± 800 ns FROM ITS NOMINAL POSITION
B = LEADING EDGE OF BIT MAY BE ± 400 ns FROM ITS NOMINAL POSITION

FIGURE 17. READ DATA TIMING (FM)

4.1.2.4 Write Protect

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected with label over notch. The drive will inhibit writing with a protected diskette installed in addition to notifying the interface (refer to paragraph 8.5).

4.1.2.5 Drive Status (Refer to Paragraph 8.4)

4.2 Power Interface

The SA410 or SA460 requires only DC power for operation. DC power to the drive is provided via P2/J2 located on the component side of the PCB near the spindle drive motor. The two DC voltages, their specifications and their P2/J2 pin designators are outlined in table 1. The specifications outlined on current requirements are for one drive. For multiple drive systems the current requirements are a multiple of the maximum current times the number of drives in the system.

P2 PIN	DC VOLTAGE	TOLERANCE		MAX RIPPLE (p to p)
1	+ 12VDC	± 0.6VDC	2.20 A MAX. 1.3 A TYP.	100 mV max allowable
2	+ 12 Return			
3	+ 5 Return			
4	+ 5VDC	± 0.25	.70A MAX .50A TYP.	

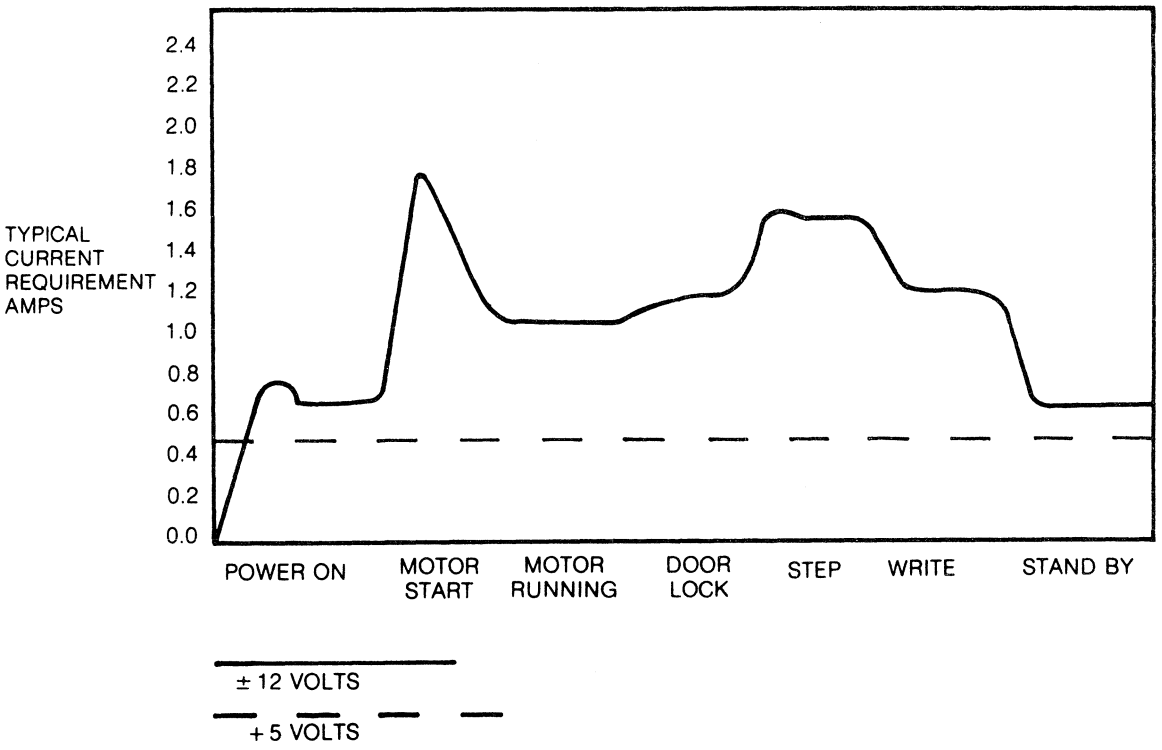


TABLE 1. DC POWER REQUIREMENTS

4.2.1 Frame Ground

It is important that the drive be frame grounded to the host system AC or frame ground. Failure to do so may result in drive noise susceptibility.

5.0 PHYSICAL INTERFACE

The electrical interface between the SA410 or SA460 and the host system is via two connectors. The first connector, J1, provides the signal interface and the second connector, J2, provides the DC power.

This section describes the physical connectors used on the drive and recommended connectors to be used with them. Refer to Figure 18 for connector locations.

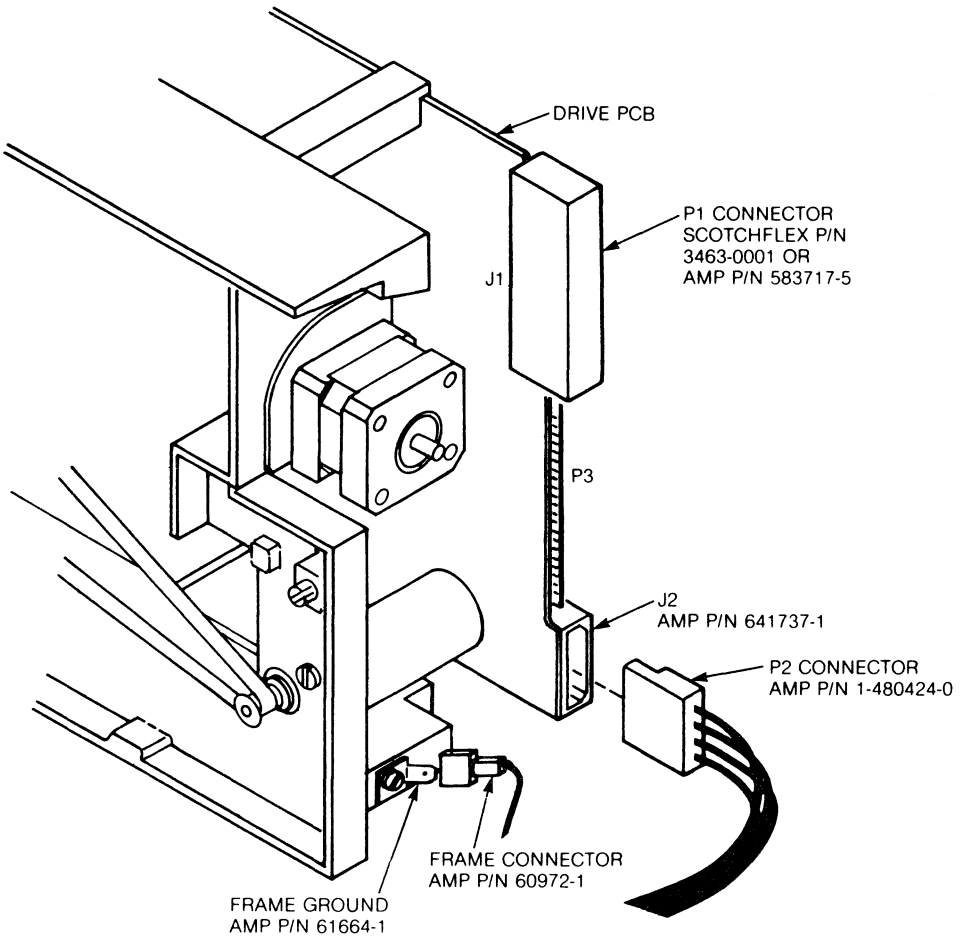


FIGURE 18. INTERFACE CONNECTORS-PHYSICAL LOCATIONS

5.1 J1/P1 Connector

Connection to J1 is through a 34 pin PCB edge connector. The dimensions for this connector are shown in Figure 19. The pins are numbered 1 through 34 with the even numbered pins on the component side of the PCB and the odd numbered pins on the non-component side. Pin 2 is located on the end of the PCB connector closest to the corner and is labeled 2. A key slot is provided between pins 4 and 6 for optional connector keying.

The recommended connectors for P1 are shown in Figure 18.

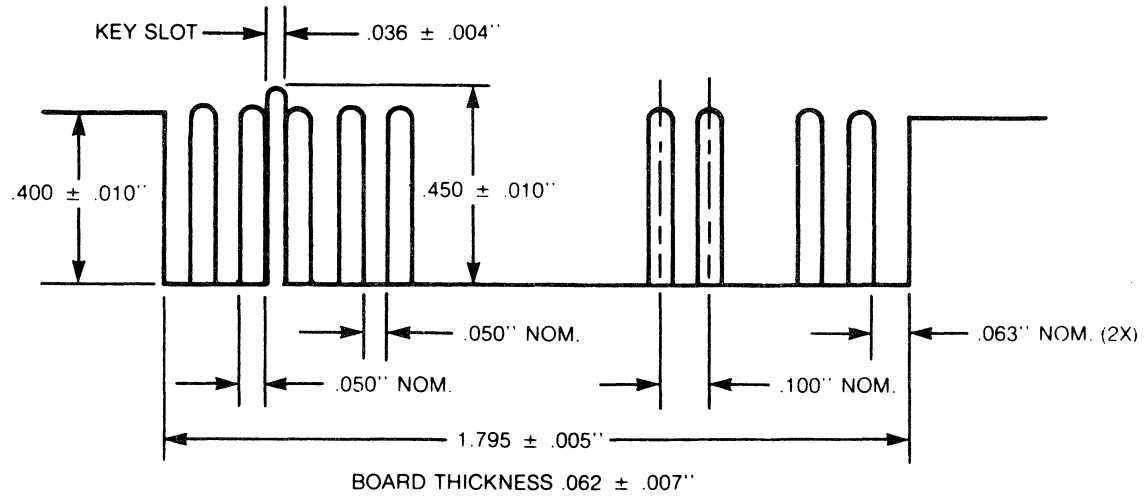


FIGURE 19. J1 CONNECTOR DIMENSIONS

5.2 J2/P2 Connector

The DC power connector, J2, is mounted on the component side of the PCB and is located near the spindle drive motor. J2 is a 4 pin AMP Mate-N-Lok connector P/N 641737-1. The recommended mating connector (P2) is AMP P/N 1-480424-0 utilizing AMP pins P/N 61473-1. J2, pin 1, is labeled on the component side of the PCB. Wire used should be #18 AWG. Figure 20 illustrates J2 connector as seen on PCB from the rear of the drive.

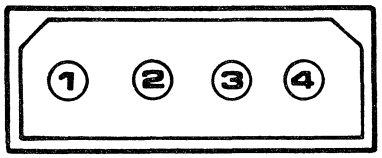


FIGURE 20. J2 CONNECTOR

5.3 Frame Grounding

The drive must be frame grounded to the host system to insure proper operation. If the frame of the drive is not fastened directly to the frame of the host system with a good AC ground, a wire from the system AC frame ground must be connected to the drive. For this purpose, a faston tab is provided on the drive where a faston connector can be attached or soldered. The tab is AMP P/N 61664-1 and its mating connector is AMP P/N 60972-1.

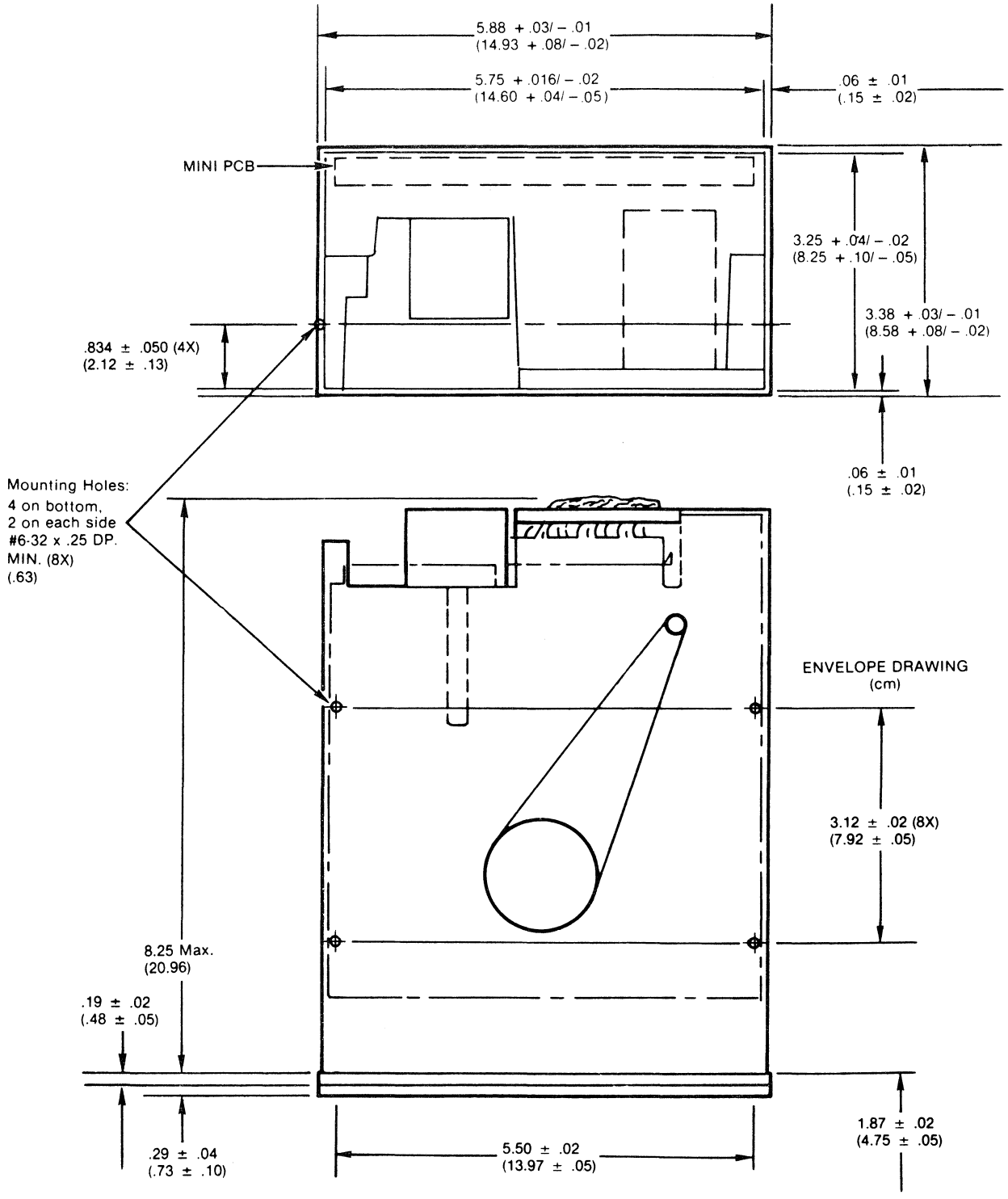


FIGURE 21. PHYSICAL DIMENSIONS

6.0 DRIVE PHYSICAL SPECIFICATIONS

This section contains the mechanical dimensions and mounting recommendations for the SA410 or SA460.

6.1 Mechanical Dimensions

Refer to Figure 21 for dimensions of the SA410/460.

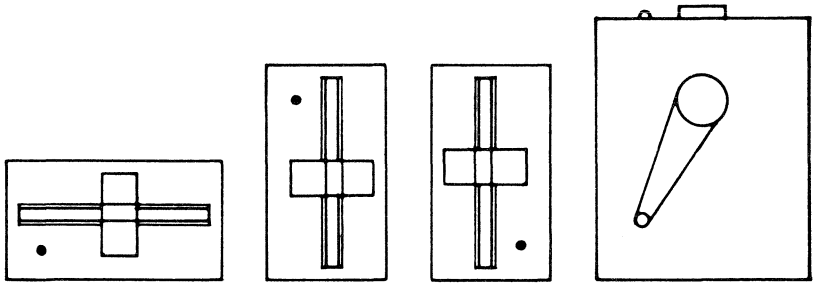
6.2 Mounting

As shipped from the factory, the drive is capable of being mounted in one of the following positions:

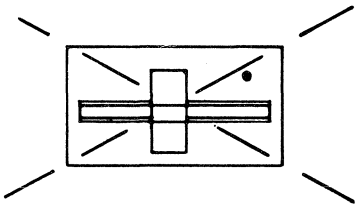
1. Top Loading -mounted upright.

2. Front Loading -mounted vertical with door opening left or right.

   -mounted horizontal with PCB up. DO NOT HORIZONTAL MOUNT WITH PCB DOWN.



RECOMMENDED



NOT RECOMMENDED

FIGURE 22. RECOMMENDED MOUNTING

7.0 RECORDING FORMAT

7.1 General

The format of the data recorded on the diskette is totally a function of the host system. As discussed in Section 3.6, data can be recorded on the diskette using FM or MFM encoding. In these encoding techniques, clock bits are written at the start of their respective bit cells and data bits at the centers of their bit cells.

7.2 Byte

A Byte, when referring to serial data (being written onto or read from the disk drive), is defined as eight (8) consecutive bit cells. The most significant bit cell is defined as bit cell 0 and the least significant bit cell is defined as bit cell 7. When reference is made to a specific data bit (i.e., data bit 3), it is with respect to the corresponding bit cell (bit cell 3).

During a write operation, bit cell 0 of each byte is transferred to the disk drive first with bit cell 7 being transferred last. Correspondingly, the most significant byte of data is transferred to the disk first and the least significant byte is transferred last.

When data is being read back from the drive, bit cell 0 of each byte will be transferred first with bit cell 7 last. As with reading, the most significant byte will be transferred first from the drive to the user.

Figure 23 illustrates the relationship of the bits within a byte and Figure 24 illustrates the relationship of the bytes for read and write data.

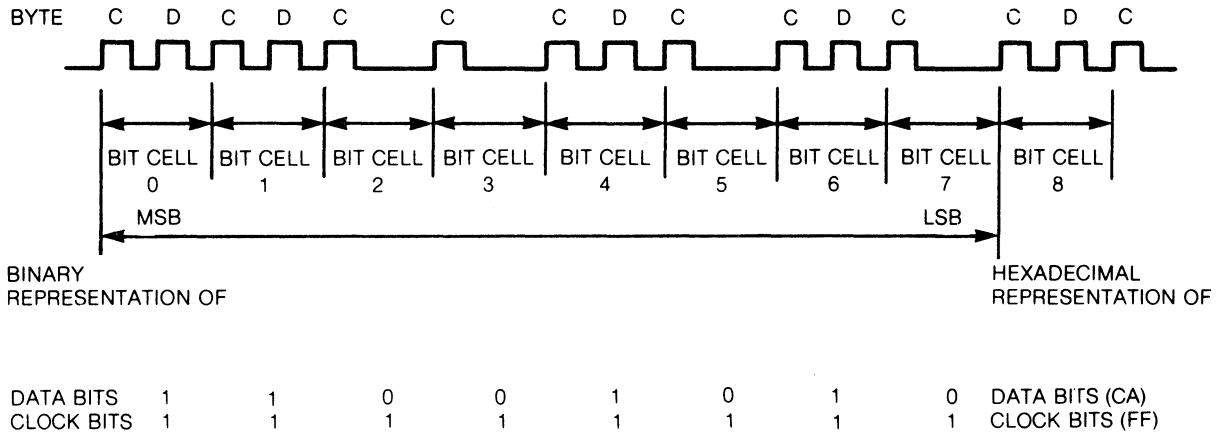


FIGURE 23. BYTE (FM ENCODING)

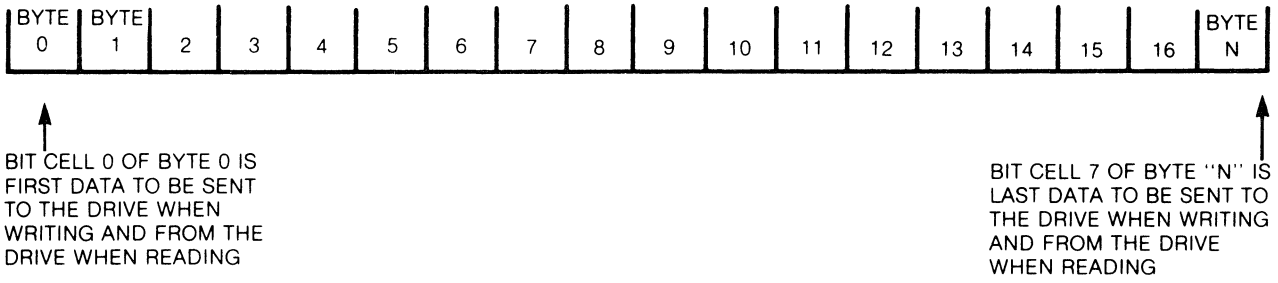


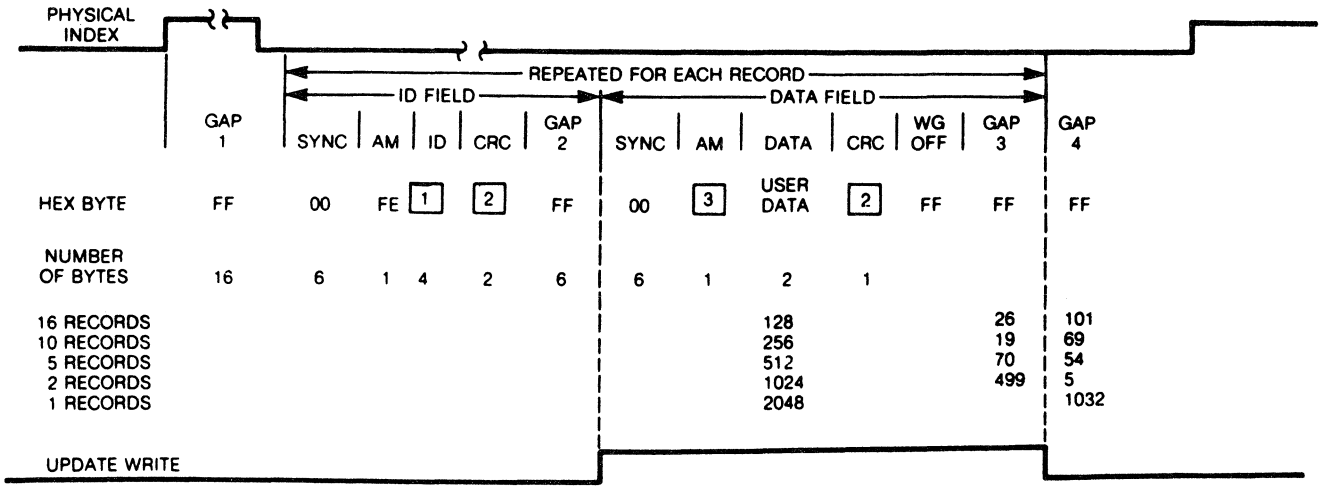
FIGURE 24. DATA BYTES

7.3 Formats

Tracks may be formatted in numerous ways and is dependent on the using system. The SA410 or SA460 can use either hard or soft sectored formats.

7.3.1 Soft Sectored Recording Format

In this format, the using system may record one long record or several smaller records. Each track is started by physical index pulse and then each record is preceded by a unique recorded identifier. This type of recording is called soft sectoring. Figure 25 illustrates the recommended single density (FM) formats. Figures 26 shows the recommended double density (MFM) formats.

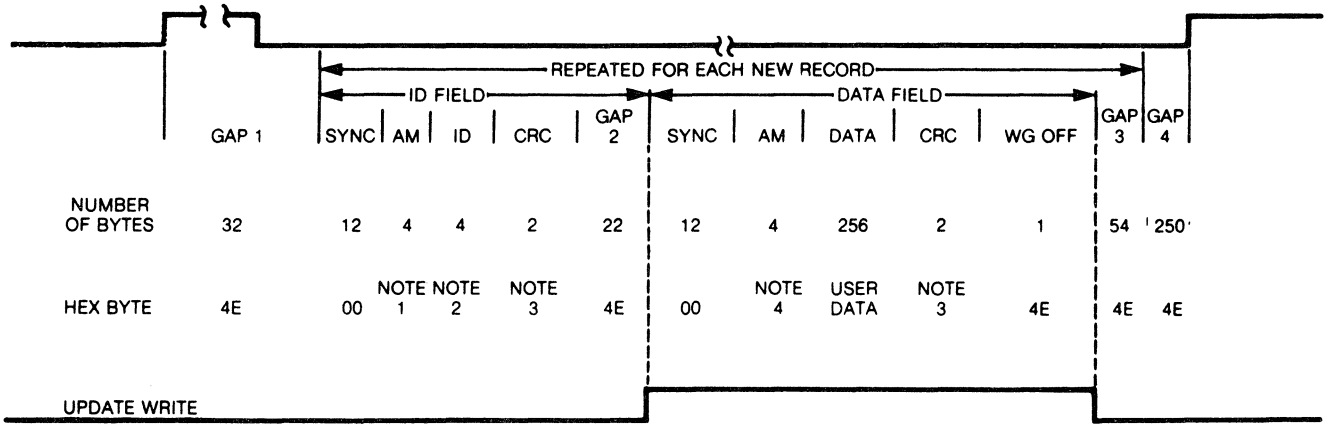


NOTES: 1. Track Number, Head Number, Sector Number, Sector Length.

2. IBM or Equivalent CRC Generator.

3. FB for Data or F8 for Deleted Data.

FIGURE 25. RECOMMENDED SOFT SECTOR SINGLE DENSITY (FM) (EVEN BOUNDARIES)



NOTES: 1. First three bytes are Hex A1 with missing Clock Transitions between bits 4 and 5. Last byte is Hex FE.

2. Track Number, Head Number, Sector Number, Sector Length (Hex 01).

3. IBM or Equivalent CRC Generator.

4. Same as Note 1, except last byte = Hex FB.

FIGURE 26. MFM RECOMMENDED FORMAT - 256 BYTES/16 RECORDS PER TRACK (IBM TYPE)

7.3.1.1 Track Layout

Index is the physical detector indicating one revolution of the media and is used to initiate format operations, generate the Ready signal in the storage device, insure one complete revolution of the media has been searched, and for a deselect storage device signal after a certain number of revolutions.

Gap 1-**G1** is from the physical index mark to the ID field address mark sync and allows for physical index variation, speed variation and interchange between storage devices.

ID Field-**Sync** is a fixed number of bytes for Separator synchronization prior to AM. Includes a minimum of two bytes plus worst case Separator sync up requirements.
ID Pre Address Mark (MFM)-Three bytes of A1 with unique clock bits not written per encode rules.
ID Address Mark (FM)-is a unique byte to identify the ID field and not written per the encode rules.
ID Address Mark (MFM)-is one byte of FE and it is written per the encode rules.
ID-if a four byte address containing track number, head number, record number, and record length.
CRC-is two bytes for cyclic redundancy check.

Gap 2-**Gap** from ID CRC to data AM sync and allows for speed variation, oscillator variation and erase core clearance of ID CRC bytes prior to write gate turn on for an update write.

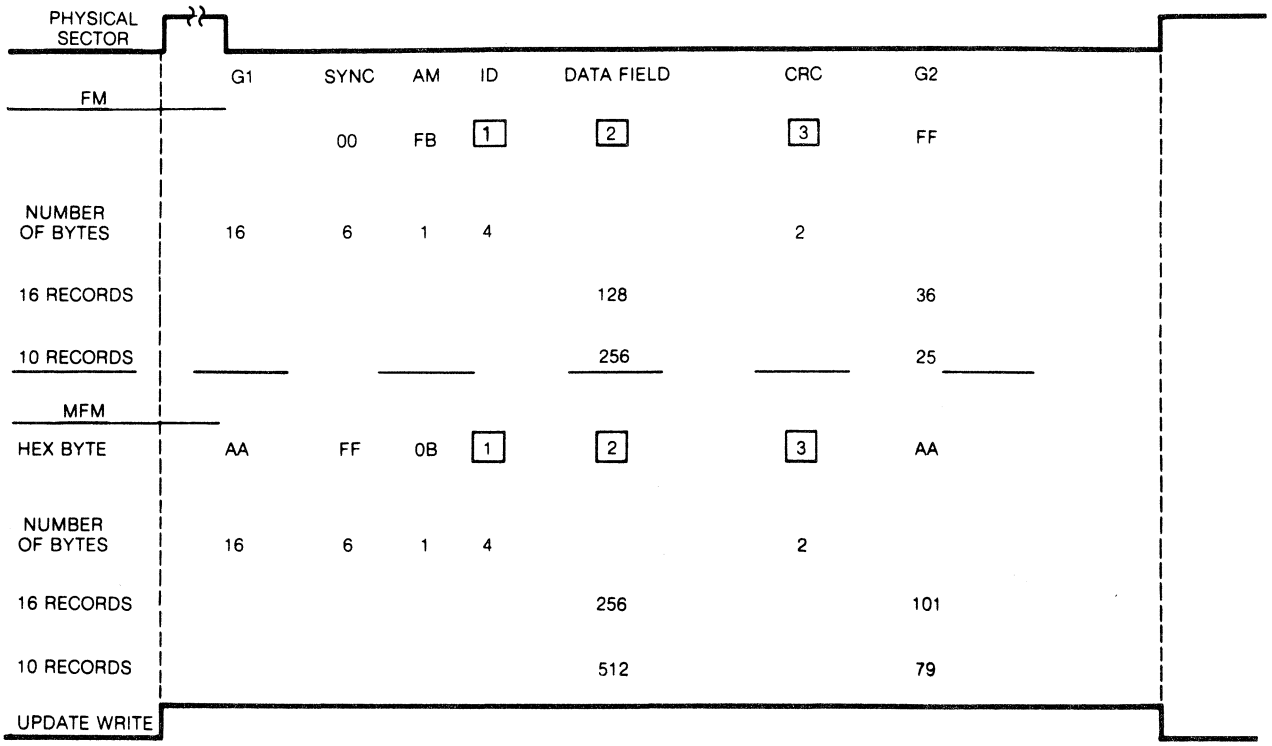
Data Field-**Sync** is a fixed number of bytes for Separator synchroniztion prior to the AM. Includes a minimum of two bytes plus worst case separator sync up requirements.
Pre Data Address Mark (MFM)-Three bytes of A1 with unique clock bits not written per the encode rules.
Data Address Mark(FM)-is a unique byte to identify the Data Field and it is not written per the encode rules.
Data Address Mark (MFM)-is one byte of FB or F8 and it is written per the encode rules.
Data-is the area for user data.
CRC-is two bytes for cyclic redundancy check.
WG OFF (Write Gate Off)-is one byte to allow for Write Gate turn off after an update write.

Gap 3-**Gap** from WG OFF to next ID AM sync and allows for erase core to clear the Data Field CRC bytes, speed and write oscillator variation, read preamplifier recovery time and system turn around time to read the following ID Field.

Gap 4-**G4** is the last gap prior to physical index and allows for speed and write oscillator variation during a format write and physical index variation.

7.3.1.2 Hard Sectored Recording Format

In this format, the using system may record up to 16 or 10 sectors (records) per track. Each track is started by a physical index pulse and each sector is started by a physical sector pulse. This type of recording is called hard sectoring. Figure 27 illustrates the hard sectored formats. All drive tolerances have been taken into account in developing these formats.



NOTES: 1. Track Number, Head Number, Record Number, Record Length.

2. User Data.

3. Generated by CRC Generator (IBM or Equivalent).

FIGURE 27. RECOMMENDED HARD SECTOR FM AND MFM FORMATS

8.0 CUSTOMER INSTALLABLE OPTIONS

The SA410/460 can be modified by the user to function differently than the standard method. These modifications can be implemented by adding or deleting connections. Options can be selected by use of a shorting plug or a cut trace. This section discusses examples of midifications and how to install them. The examples are:

1. DRIVE SELECT, MOTOR ON and IN USE
2. DOOR LOCK from IN USE or DRIVE SELECT
3. SIDE SELECT, using DIRECTION SELECT
4. DRIVE STATUS
5. WRITE PROTECT

TRACE DESIGNATOR	DESCRIPTION	SHIPPED FROM FACTORY	
		OPEN	SHORT
U3	Terminations for Multiplexed Standard Inputs		plugged
DS1	DRIVE SELECT 1 input line		plugged
DS2,3,4	DRIVE SELECT 2,3,4 input lines	X	
MX	DRIVE SELECT Enabled Single Drive System	X	
MS	MOTOR ON From DRIVE SELECT	X	
SS	Standard SIDE SELECT		plugged
SD	SIDE SELECT Option using DIRECTION SELECT	X	
DD	DOOR DISTURB		plugged
DO	DOOR OPEN		
RI	READY INDEX		plugged
RD	READY DOOR		
DA	DOOR LOCK From DRIVE SELECT	X	

TABLE 2. CUSTOMER CUT/ADD TRACE OPTIONS

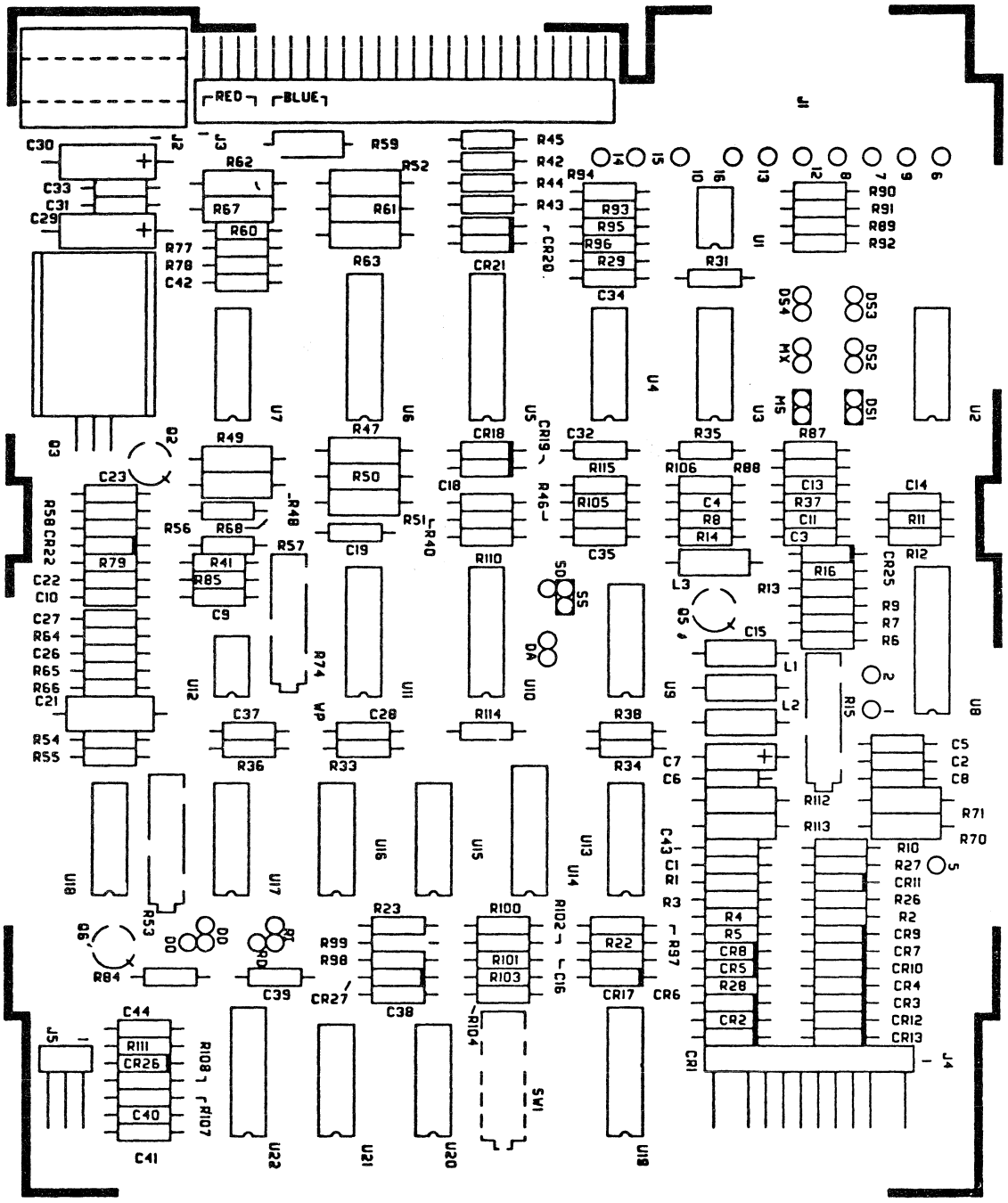


FIGURE 28 COMPONENT LOCATIONS

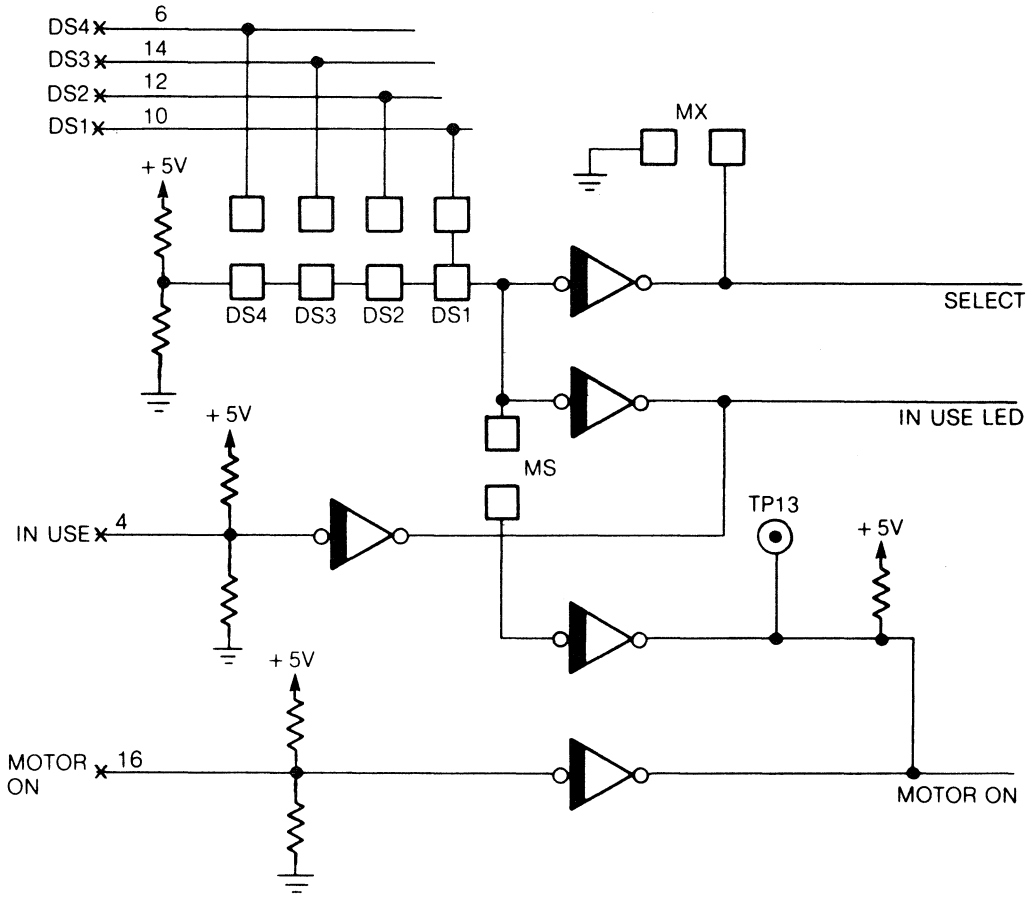


FIGURE 29. DRIVE SELECT, MOTOR ON AND IN USE

8.1 Drive Select

The DRIVE SELECT Jumper (DS1,2,3,4) as the drive is shipped is in position DS1. The SA410/460 is configured to operate alone in a single drive system. It can be easily modified to operate with other drives in a daisy chained, multiplexed multiple drive system. This is done by selecting specific drive address and jumpering the appropriate DRIVE SELECT line.

The MX option is used for single drive systems. By shorting MX the I/O lines are always enabled.

The MS option allows the motor to be enabled from DRIVE SELECT.

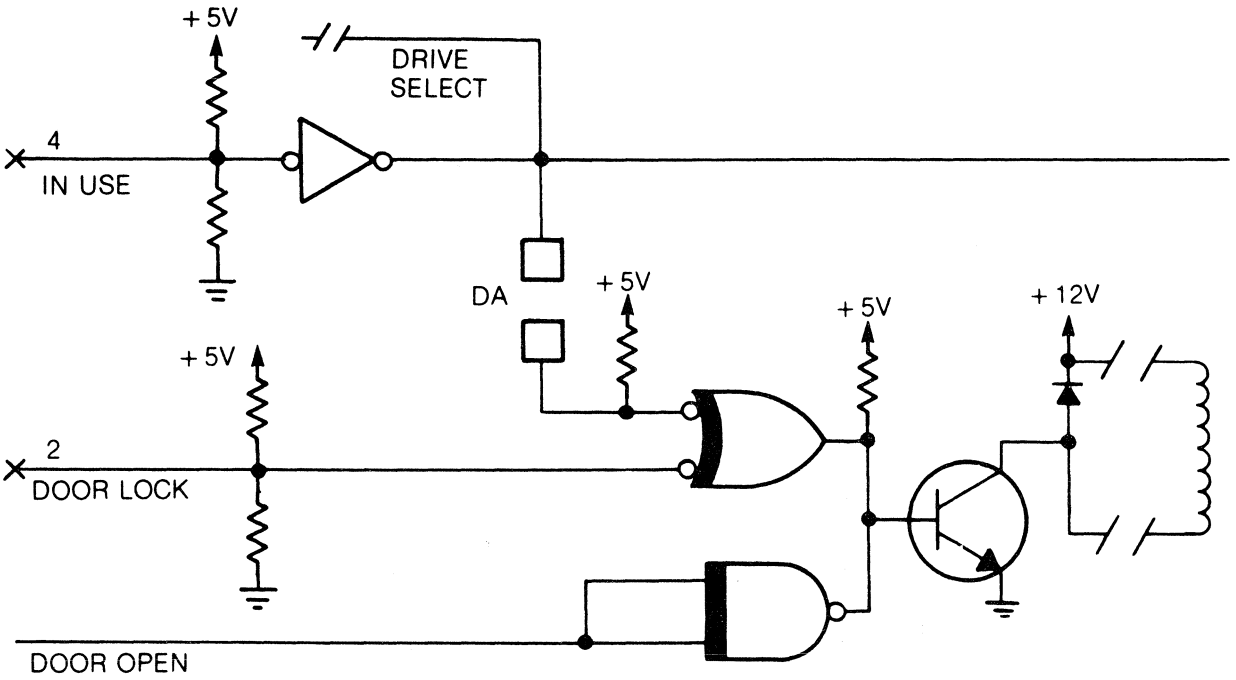


FIGURE 30. DOOR LOCK FROM IN USE OR DRIVE SELECT

8.2 The Door Lock Solenoid (Option)

The Door Lock Solenoid can be activated by the interface line provided on PIN 2.

The DA option allows the Door Lock Solenoid to be activated when the IN USE or DRIVE SELECT Signal has been asserted to a logic zero.

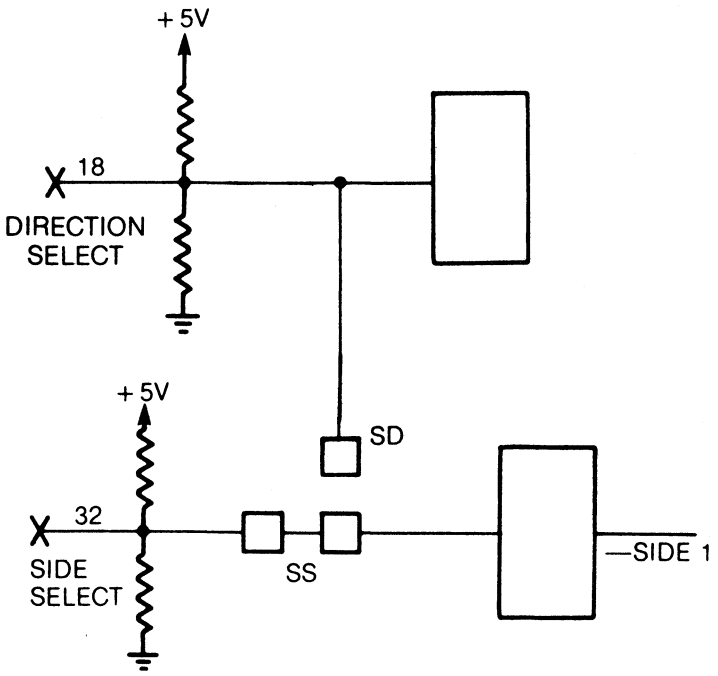


FIGURE 31. SIDE SELECT, USING DIRECTION SELECT

8.3 Side Select

The SIDE SELECT function can be controlled via the DIRECTION SELECT line, if desired. With this option, the DIRECTION SELECT line controls the direction of head motion during stepping operations and controls side (head) selection during read/write operations. To implement this option, simply move jumper SS to location SD.

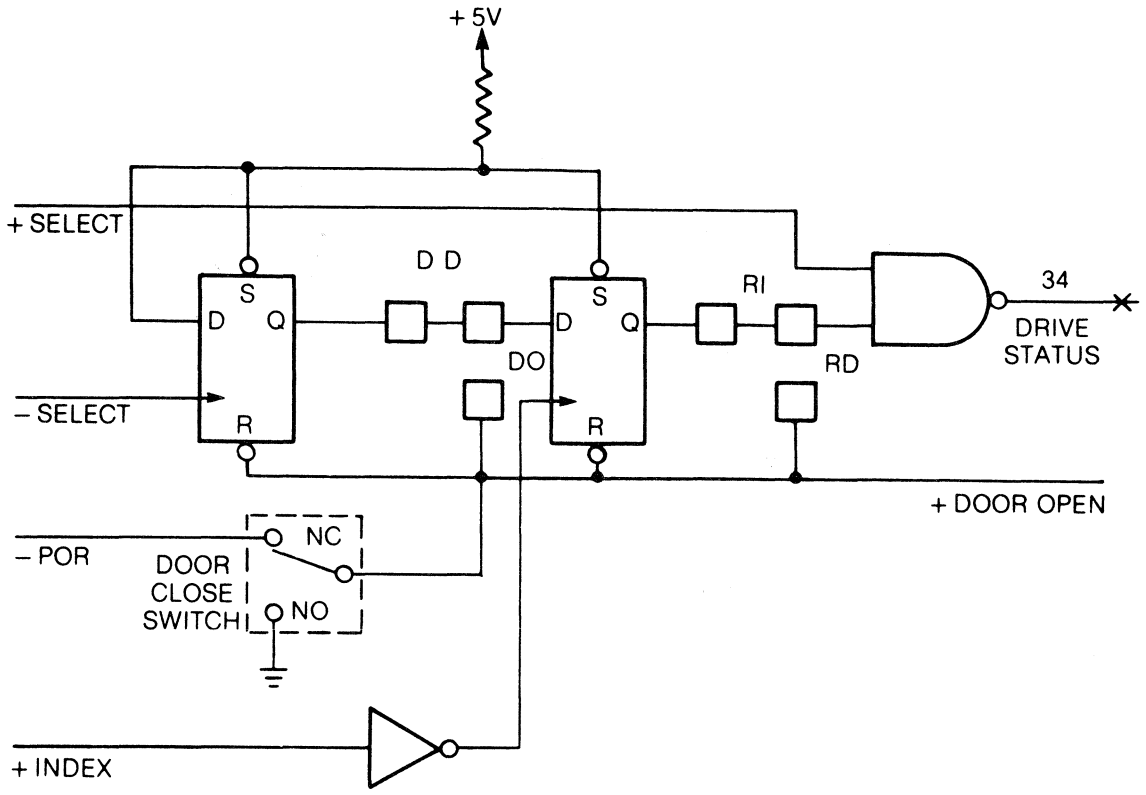


FIGURE 32. DRIVE STATUS

8.4 Drive Status

This interface signal gives the user an indication that a diskette is inserted correctly in the drive and the door is closed. The DRIVE STATUS signal is active, at a logic zero level, when the following conditions are met:

(a) the door is closed
(b) the door has not been opened since the drive was last deselected; and
(c) an INDEX/SECTOR pulse has been sensed since the previous conditions were met.

If the DRIVE STATUS signal is inactive, the user may deselect and then select the drive to test DRIVE STATUS again: if the door had previously been disturbed (condition (b) was not met) but is now closed, DRIVE STATUS WILL ACTIVATE upon sensing an INDEX/SECTOR pulse.

Condition (b) may optionally be eliminated by cutting trace DD and shorting trace DO. Conditions (b) and (c) may optionally be eliminated by cutting trace RI and shorting trace RD. One of these two options must be implemented if MX is shorted (see Figure 29), since condition (b) will not be met.

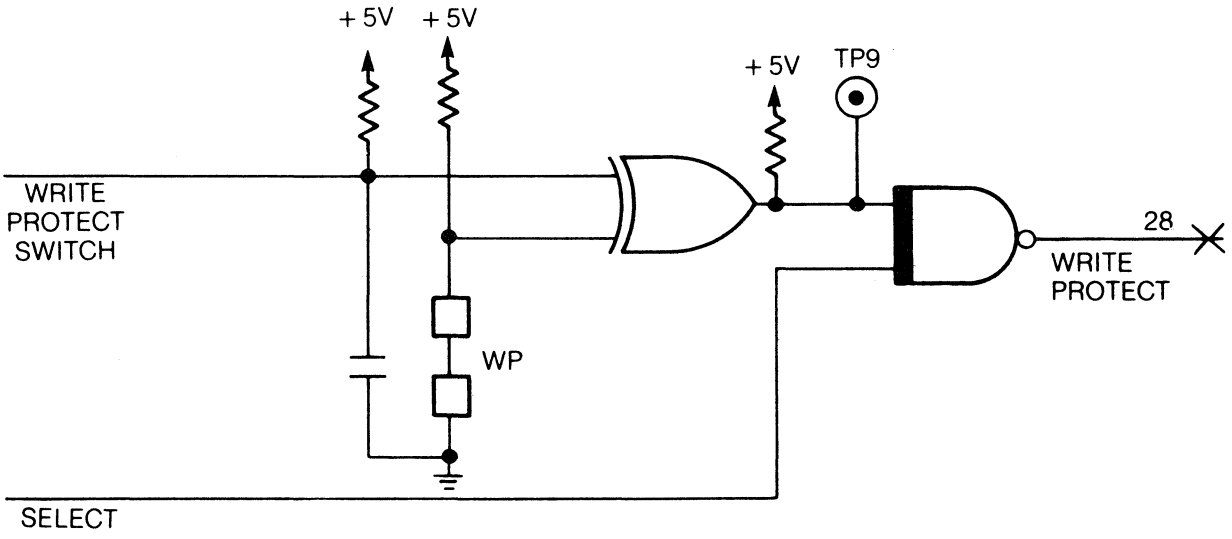


FIGURE 33. WRITE PROTECT

8.5 Write Protect

This interface signal is provided by the drive to give the user an indication when a Write Protected Diskette is installed. The signal is logical zero level when it is protected with label over notch. Under normal operation, the drive will inhibit writing with a protected diskette installed in addition to notifying the interface. If the "WP" trace is cut, writing to the diskette is inhibited unless a label is installed over the notch.

9.0 OPERATION PROCEDURES

The SA410 or SA460 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following section is a guide for the handling procedures on the minidiskette and minifloppy drive.

9.1 Minidiskette Loading

To load the diskette, open the door on the front panel, insert the diskette with label towards the door handle and close handle. A mechanical interlock prevents door closure without proper media insertion, thus eliminating media damage.

9.2 Minidiskette Handling

To protect the diskette, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

1. Return the diskette to its storage envelope whenever it is removed from drive.
2. Do not bend or fold the diskette.
3. Store diskettes not for immediate use in their box.
4. Keep diskettes away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on the disk.
5. Replace storage envelopes when they become worn, cracked or distorted. Envelopes are designed to protect the disk.
6. Place I.D. labels in the correct location, never use them in layers.
7. Do not write on the plastic jacket with a lead pencil or ball point pen. Use a felt tip pen.
8. Do not use erasers.
9. Heat and contamination from a carelessly dropped ash can damage the disk.
10. Do not expose diskette to heat or sunlight.

10.0 INSTALLATION OF PACKAGING MATERIALS

All 410's and 460's shipped from the factory and regional depots are equipped with carriage stops and door retainers. The carriage stop is designed to prevent head carriage movement while the drive is in transit. The door retainer eliminates the possibility of breakage resulting from the door opening during shipment.

Upon receipt of the drive, the door retainer and carriage stop should be removed and retained. They must be reinstalled prior to any further shipment of the drive.

To prepare a drive for shipment:

A. Locate the head carriage at Track 00.

B. Insert the carriage stop as you would a diskette, with the tab under the head carriage (see Figure 34).

C. Install the door retainer by sliding the center section (with the tabs nearest the PCB), into the door pin slots and bending the tabs down over the hub frame (see Figure 35).

D. Place the drive in its packing container (see Figure 36 and 37).

Failure to follow this procedure may result in damage to the drive.

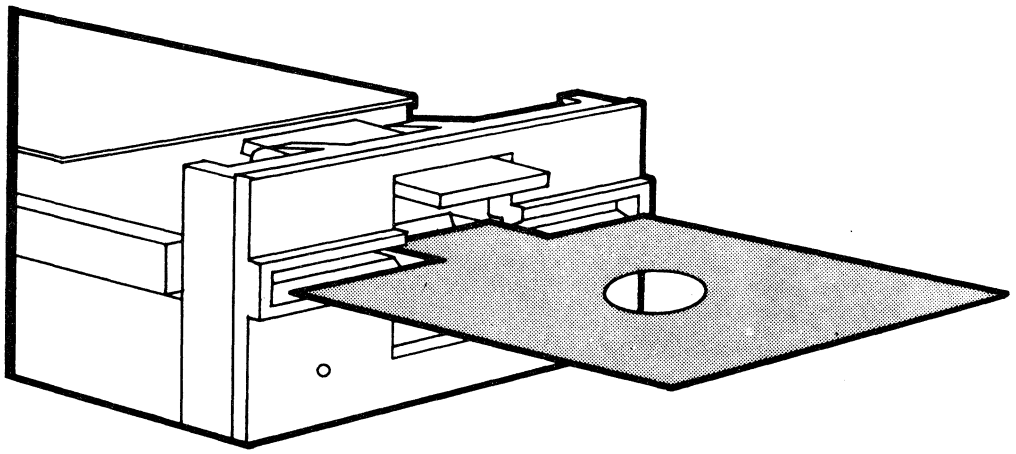


FIGURE 34. CARRIAGE STOP

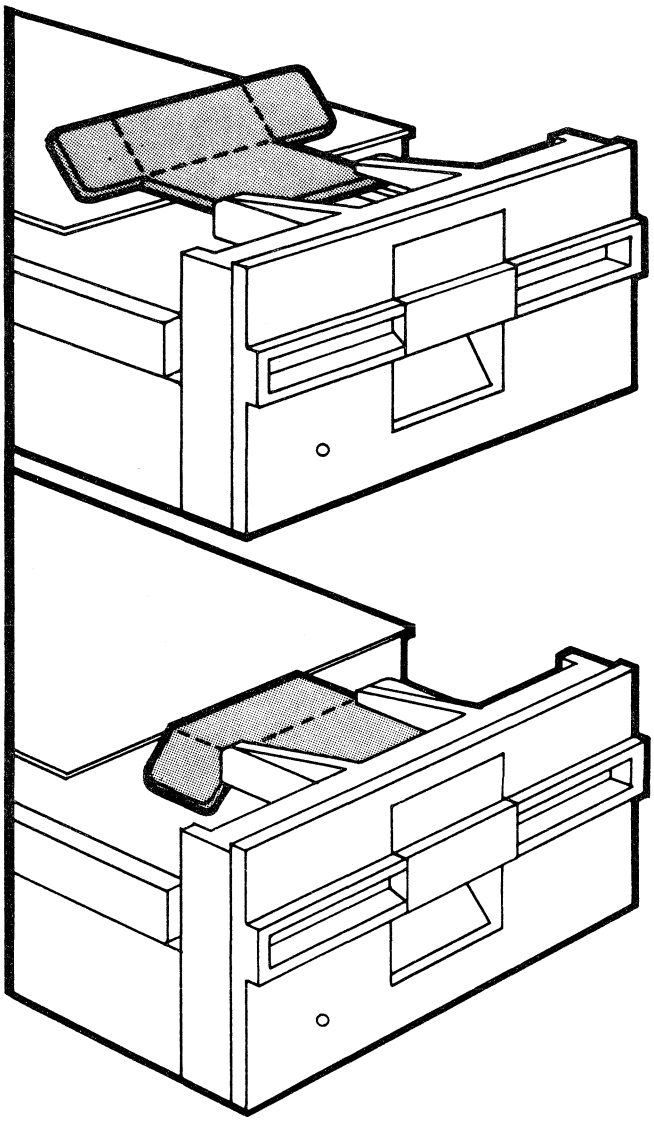


FIGURE 35. DOOR RETAINER

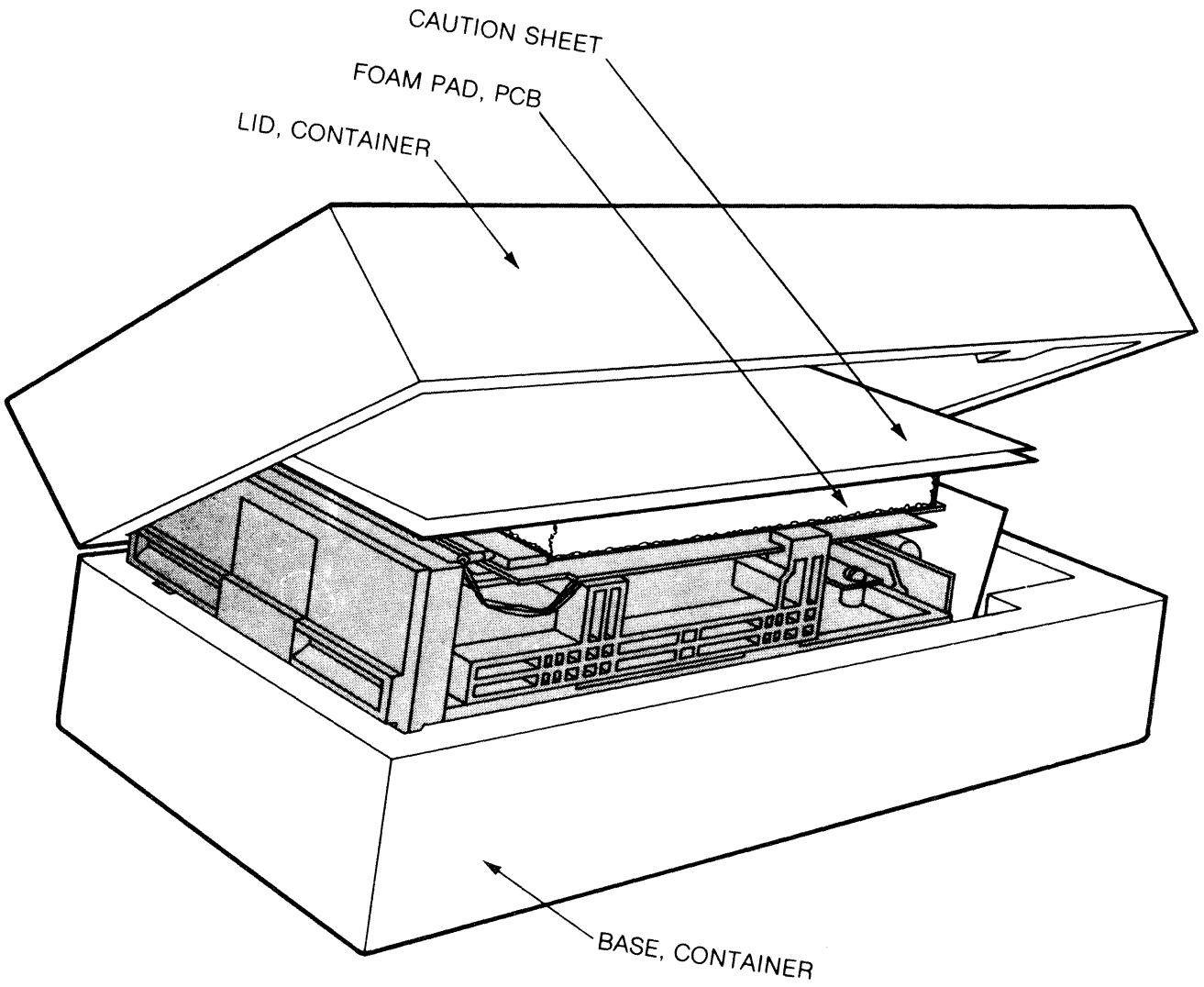


FIGURE 36. DRIVE CONTAINER

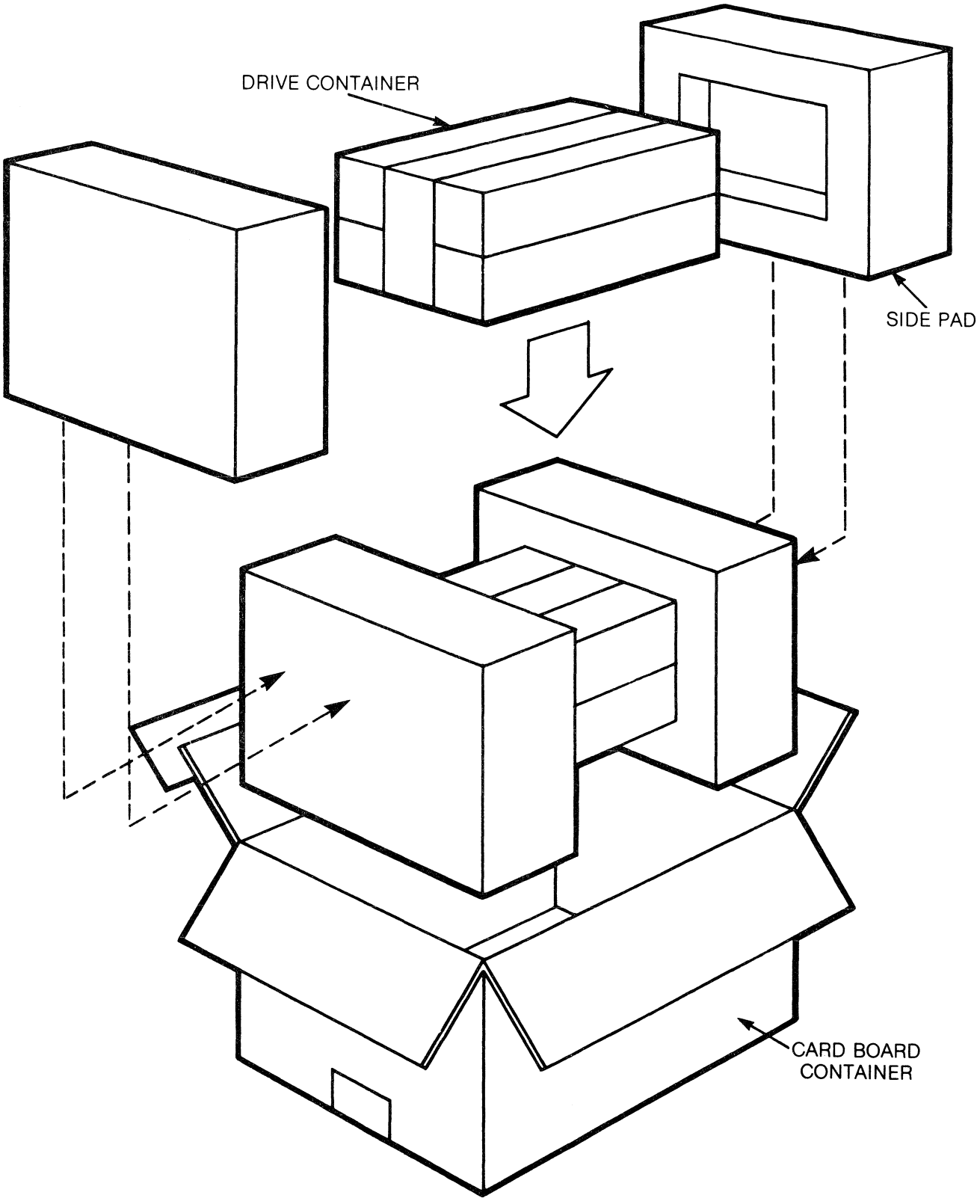


FIGURE 37. SHIPPING CONTAINER

APPENDIX H: FLOPPY DISK DRIVE MANUFACTURER'S MANUAL

Magnetic Peripherals, Inc., Model 9409T

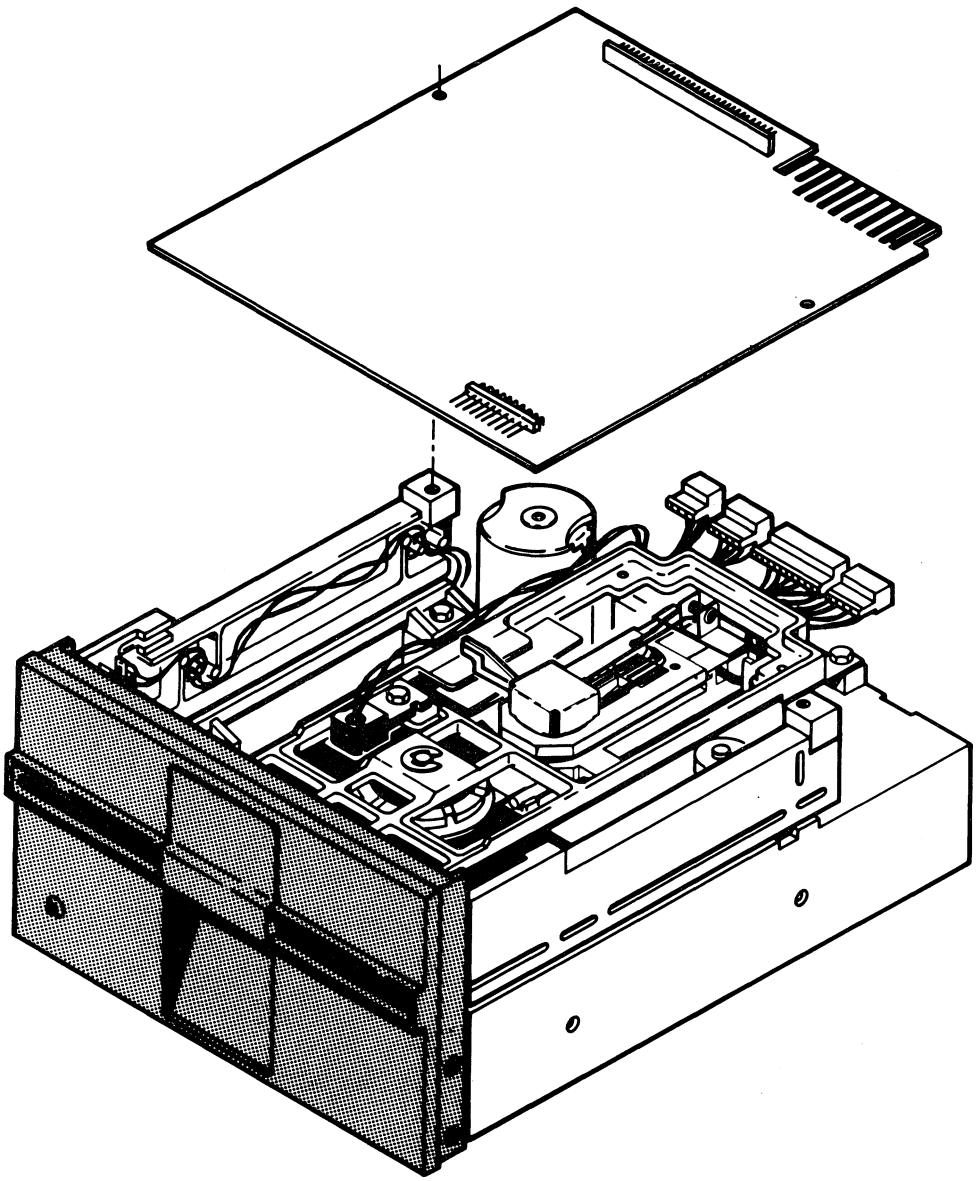
TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The 9409T is a 96 TPI double-sided 5.25-inch flexible disk drive (FDD) which features one megabyte capacity. The 9409T utilizes standard 96 TPI double-sided 5.25-inch flexible media in either single density (FM) or double density (MFM) recording. Device applications include small computer systems, intelligent data terminals, and home computers. The 9409T is illustrated in Figure 1.



GG138a

Figure 1. 9409T Flexible Disk Drive

The 9409T contains control and read/write electronics and a band stepper track accessing positioner capable of reading or writing 96 tracks per inch. The 9409T incorporates tunnel erase heads which provide maximum signal to noise ratio.

The interface signals and timings, power requirements, mechanical dimensions, and mounting requirements are industry-compatible.

Index pulses are produced by a photoelectric sensing assembly mounted within the 9409T. Track-to-track accessing and positioning are accomplished with a DC-powered, +12-volt stepper motor.

Figure 2 illustrates standard diskette insertion.

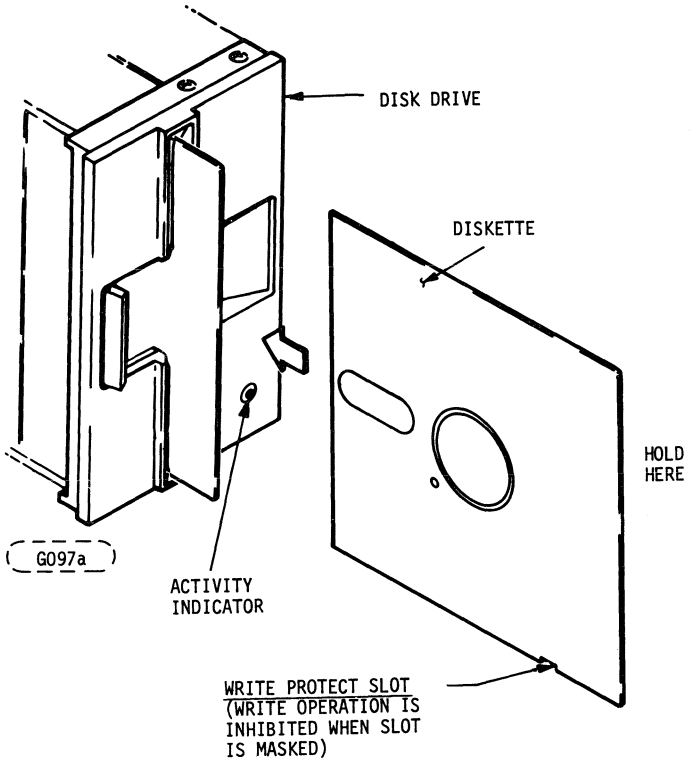


Figure 2. Diskette Insertion

2.0 APPLICABLE DOCUMENTS

2.1 STANDARDS

The Model 9409T FDD has been designed as a system peripheral to the highest standards of design and construction. The drive, however, must depend upon its host equipment to receive adequate power and environment in order to provide optimum performance and compliance with applicable industry and governmental regulations. Special attention must be given in the areas of safety, power distribution, grounding, shielding, audible noise control, and temperature regulation of the device to ensure specified performance and compliance with all applicable regulations.

The 9409T is a component, and, as such, is not subject to standards imposed by FCC Docket 20780/FCC 80-148 Part 15 governing EMI of computing devices.

2.2 DOCUMENTATION

The following documents and specifications provide detailed theory of operation, maintenance procedures, and media format considerations. These documents are not included with each unit, but must be ordered separately.

- Model 9409T FDD Hardware Maintenance Manual
- Alignment Diskette Specification (Double-Sided Operation)
- Double-Sided Diskette Specification (5.25-Inch Double Density)
- Application Note, PLO and Write Precompensation for 5.25-Inch Flexible Disk Drives, 77653447
- Application Note, 5.25-Inch FDD Format Considerations and Controller Compatibilities, 75897469

3.0 FEATURES

3.1 STANDARD FEATURES

The 9409T FDD has the following standard features:

- Double-Sided 96 TPI 5.25-Inch Media Capability
- Single-Density (FM) and Double-Density (MFM) Encoding
- Industry-Compatible Interface
- Industry-Compatible Mounting Configurations
- Only Two DC Power Voltages Required (+5 V and +12 V)
- Write Protect Indication
- Activity Indicator
- Long-Life Ceramic Read/Write Heads
- Band Stepper Motor
- Hard or Soft Sector Formatting
- Head Select
- Drive Select
- Track-Zero Detection
- Index Detection
- Step/Direction Control for Track-to-Track Access
- Black Finish

3.2 OPTIONAL FEATURES

- Door Open Option
- Head Load Solenoid Option

4.0 PERFORMANCE SPECIFICATIONS

Capacity	Single Density	Double Density
Unformatted		
Per Disk	500.0 kbytes	1.0 Mbyte
Per Surface	250.0 kbytes	500.0 kbytes
Per Track	3.125 kbytes	6.250 kbytes
Formatted (16 Sectors, 128/256 Bytes)*		
Per Disk	327.68 kbytes	655.36 kbytes
Per Surface	163.84 kbytes	327.68 kbytes
Per Track	2048 bytes	4096 bytes
Code	FM	MFM
Transfer Rate	125 kbits/s	250 kbits/s
Latency (Average)	100 ms	100 ms
Seek Time		
Track-to-Track	5 ms	5 ms
Average	132 ms	132 ms
Settle Time	15 ms	15 ms
Head-Load Time	0 (or 50 ms optional**)	0 (or 50 ms optional**)
Side-Select Time	200 µs***	200 µs***
Write Precompensation	0	250 ns (trk 43-79)

* Assumes tunnel erase heads.

** 50 ms with Head-Load Solenoid option.

*** Assumes motor on, drive selected, head loaded, and erase turn-off delay completed from any previous write operation.

4.1 DEFINITIONS

4.1.1 Latency

Latency is the time required for the read/write head to reach a particular area on a track after positioning is completed. For a rotational/spindle speed of 300 revolutions per minute, the 9409T has an average latency of 100 ms.

4.1.2 Seek/Settle Time

The seek/settle time is the time required by the read/write head to move from track to track plus the time needed for the head to stabilize on track prior to data transfer. Seek/settle time for the 9409T is 20 milliseconds: 5 milliseconds for a single track access and 15 milliseconds for head settling time.

4.1.3 Head-Load Time

Head-load time is defined as the time from initial activation of the head-load function until valid data transfer between the drive and controller can be assured. The 9409T requires no head load time. However, a head load solenoid is optional and can be supplied to customers on request. With the optional head-load solenoid, the amount of head-load time required by the 9409T is 50 milliseconds.

4.1.4 Read Stabilization

Upon conclusion of a write operation, a minimum delay time of 1 millisecond is required before valid read data can be assured. Time is required to allow for completing the erase function. Time necessary to allow for the read circuit to stabilize after switching from one head to the other is 200 microseconds.

5.0 FUNCTIONAL SPECIFICATIONS

	Single Density	Double Density
Encoding Method	FM	MFM
Rotational Speed	300 r/min	300 r/min
Recording Density (Track 79, Side 1)	2961 bpi	5922 bpi
Flux Reversal Density (Track 79, Side 1)	5922 FRI	5922 FRI
Track Density	96 TPI	96 TPI
Tracks Per Surface	80	80
Heads	2	2
Inside Recorded Radius (Side 0)	1.437 in (36.49 mm)	1.437 in (36.49 mm)
Outside Recorded Radius (Side 0)	2.250 in (57.15 mm)	2.250 in (57.15 mm)
Inside Recorded Radius (Side 1)	1.344 in (34.14 mm)	1.344 in (34.14 mm)
Outside Recorded Radius (Side 1)	2.167 in (55.04 mm)	2.167 in (55.04 mm)
Motor Start Time	150 ms (typical)	150 ms (typical)

6.0 RELIABILITY SPECIFICATIONS

The following reliability specifications assume correct host/drive operational interface has been implemented, including all interface timings, power supply voltages, environmental conditions, and application of recommended data-recovery techniques. (PLO and Write Precompensation Application Note

is available upon request.) The following MTBF assumes spindle drive motor duty cycle is 25% of power-on hours.

Error Rates	
Soft Read Errors	$\leq$1 per 10^9 bits read
Hard Read Errors	$\leq$1 per 10^{12} bits read
Seek Errors	$\leq$1 per 10^6 seeks
MTBF	$\geq$8000 Power-On Hours, Typical Usage
MTTR	0.5 Hour
Service Life	5 Years
Preventive Maintenance	None Required

6.1 MEAN TIME BETWEEN FAILURES (MTBF)

The following equation defines MTBF:

$$\text{MTBF} = \frac{\text{Power On Hours}}{\text{Number of Equipment Failures}}$$

Power On Hours are defined as the total time which the drive has AC and DC power applied, less maintenance time.

Equipment Failures are defined as any substandard performance of the drive because of equipment malfunction, excluding stoppages or substandard performance caused by operator error, adverse environment, power failure, controller failure, cable failure, or other failure not caused by the drive. In order to calculate a meaningful MTBF, all sites in which the drive is utilized is included and total power on hours should exceed 10,000 hours.

6.2 MEAN TIME TO REPAIR (MTTR)

Mean Time to Repair (MTTR) is defined as the average time required for an adequately trained and competent service technician to diagnose and correct a malfunction on site. MTTR for the 9409T is 30 minutes and does not include travel time nor time when the drive is not released to the service technician.

6.3 SERVICE LIFE

The 9409T has a useful service life of five years or 31,200 hours, whichever occurs first, before requiring factory overhaul. Repair or replacement of field replaceable parts is permitted during the lifetime of the drive.

7.0 PHYSICAL/ELECTRICAL SPECIFICATIONS

7.1 DC POWER REQUIREMENTS

DC power requirements are as shown in Table 1.

Table 1. DC Power Requirements

CONDITIONS	NOMINAL VOLTAGE		
	+5 V	+12 V	
		WITH HEAD LOAD SOLENOID	WITHOUT HEAD LOAD SOLENOID
Tolerance	±0.25 V	±0.6 V	±0.6 V
Ripple (Peak-to-Peak)	≤50 mV	≤100 mV	≤100 mV
Seeking Current:			
Typical:	0.5 A	0.9 A	0.75 A
Maximum Surge on Motor Start **	*0.7 A	*1.8 A	*1.65 A

* Specified current requirements are on a per-drive basis. Current requirement increases by a factor equal to the number of driver per power supply. For example, two drives per supply would require +12 V at 3.6 A and +5 V at 1.4 A.
**Typical surge duration is less than 200 milliseconds.

7.2 POWER DISSIPATION

With Head Load Solenoid	Without Head Load Solenoid
26.4 watts (maximum)*	24.5 watts (maximum)*
13.3 watts (nominal)	11.6 watts (nominal)

7.3 INRUSH CURRENT

Inrush current is dependent upon the power source as well as the 9409T. Primary considerations are host power supply source impedance(s), host-to-9409T power line resistance and inductance, and 9409T capacitance load presented by the filter capacitors. Schematically, this may be represented as shown in Figure 3.

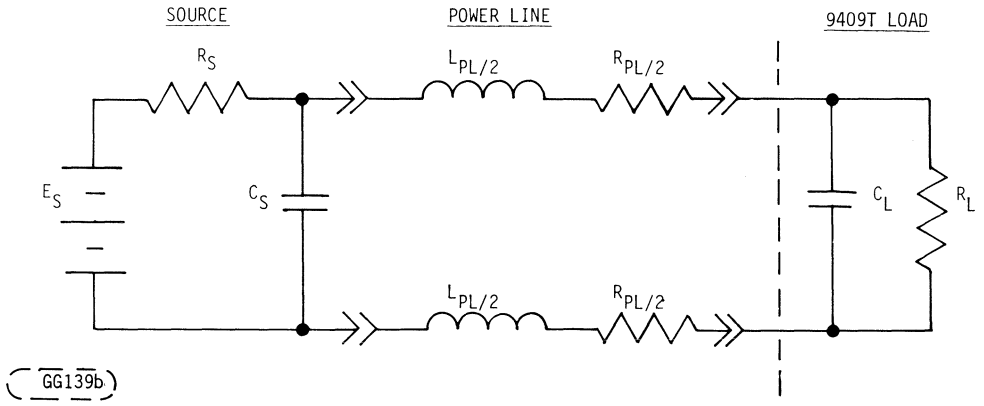


Figure 3. Inrush Current

Nominal equivalent loads for the 9409T are as follows:

	+12 V	+5 V
C_L	22 microfarads	39 microfarads
R_L	13 ohms	10 ohms

* Maximum power dissipation is calculated using maximum current surge and upper tolerance on power supply voltage rating. The peak value is typically 100 ms after motor start and has a duration less than 200 ms.

7.4 ENVIRONMENTAL LIMITS

Temperature and humidity specifications preclude condensation on any drive part. The 9409T is intended for use with host systems which operate in computer room and office environments. Altitude and barometric pressure specifications are referenced to a standard day at 58.7°F (14.8°C).

	Operating	Shipping and Storage
Ambient Temperature	40° to 115°F (4.4° to 46.1°C)	-40° to 144°F (-40° to 62.2°C)
Temperature Gradient	18°F/hr (-7.7°C/hr)	36°F/hr (20°C/hr)
Relative Humidity	20% to 80%	0 to 95%
Maximum Wet Bulb Temperature	79°F (26.1°C)	No condensation
Altitude (Sea Level Reference)	-983 to +9850 feet (-300 to +3002 meters)	-983 to +9850 feet (-300 to +3002 meters)
Barometric Pressure		
in of HG	30.9 to 22.2	30.9 to 18.8
mm of HG	784.9 to 563.6	784.9 to 476.9
psi	15.18 to 10.9	15.18 to 9.22

7.5 MECHANICAL SPECIFICATIONS

Following are mechanical specifications for the 9409T. Refer to Figure 4 for detailed mounting dimensions.

Height:	3.38 inches	85.8 millimeters
Width:	5.88 inches	149.4 millimeters
Depth:	8.29 inches	210.6 millimeters
Weight:	3.2 pounds	1.45 kilograms

WT: 3.2 lbs. (1.45 kg)

MOUNTING HOLES: FOUR ON BOTTOM, TWO EACH SIDE; #6-32 X 0.31 in. (7.9 mm) DEPTH

PACKAGE DIMENSION		
	INCHES	MILLIMETERS
A	8.00 MAX	203.2 MAX
B	5.75 +0.00 -0.02	146 +0.00 -0.5
C	0.29 ±0.02	7.4 ±0.5
D	1.87 ±0.02	47.5 ±0.5
E	3.12 ±0.02	79.2 ±0.5
F	5.88 ±0.01	149.4 ±0.3
G	3.38 ±0.01	85.9 ±0.3
H	0.06 ±0.01	1.5 ±0.3
I	5.50 ±0.02	140 ±0.5
J	0.86 ±0.02	21.8 ±0.5
K	1.50 ±0.01	38.1 ±0.5
L	1.41 ±0.01	35.8 ±0.5

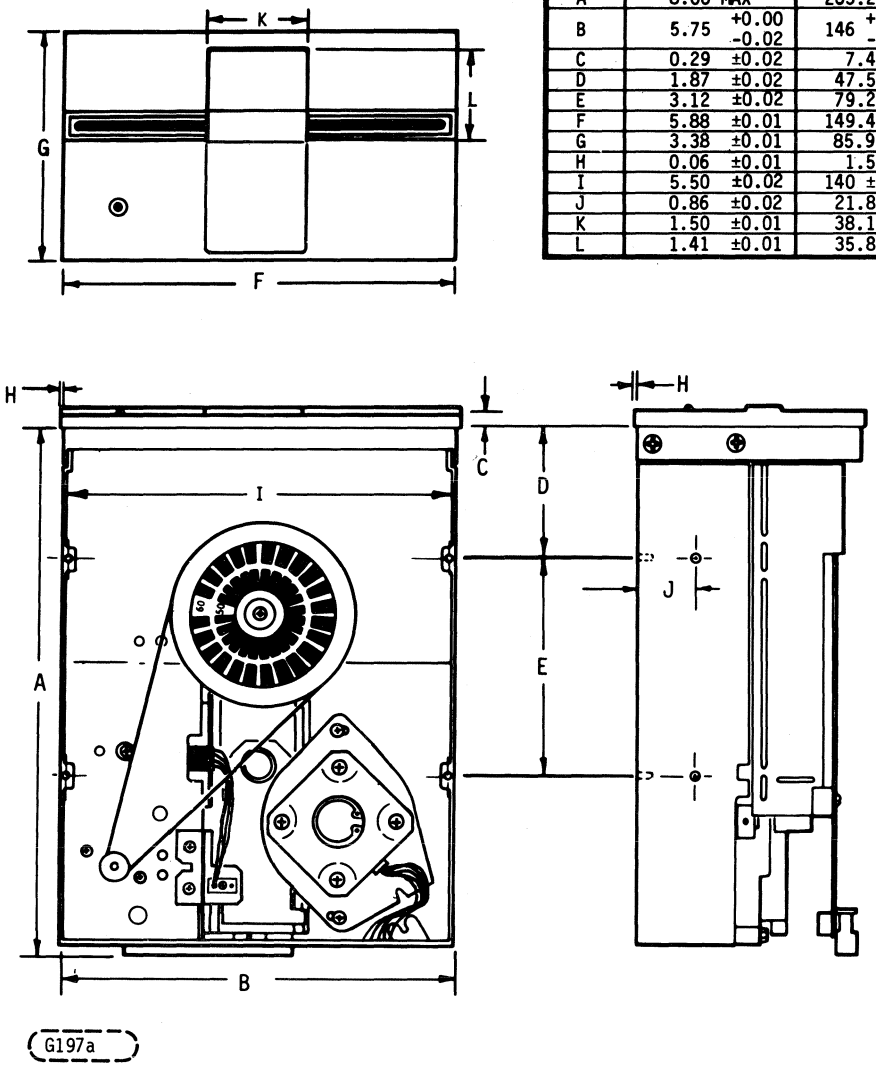


Figure 4. Dimensions of 9409T FDD

7.5.1 Drive Orientation

The 9409T can be mounted in any of the following loading positions:

- horizontal with the access door opening upward and PCB facing upward.
- vertical with the access door opening to the left or right.
- upright with the front panel at the top.

The drive should not be mounted with the PCB facing downward.

8.0 RECORDING CHARACTERISTICS/FORMAT

Capacity is determined by customer-selected data format and coding techniques.

8.1 ENCODING METHODS

Data can be recorded in either FM or MFM encoding. The format of the data recorded is a function of the host system.

8.1.1 Single-Density Recording

Double-frequency modulation (FM) recording is recommended for use in the single-density mode. FM recording is self-clocking and provides synchronization for data separation utilizing simple one-shot techniques. However, use of a phase-lock oscillator (PLO)* instead of a simple one-shot system will increase operating margins and result in greater data reliability with more tolerance for media imperfections.

---

* PLO and Write Precompensation Application Note is available on request.

8.1.2 Double-Density Recording

Modified frequency modulation (MFM) recording doubles the data storage capacity. Since the MFM coding technique is not self-clocking, it is necessary to use a PLO to generate a synchronized clock from the data stream. If both single- and double-density systems are being used, the same PLO serves both applications. Improved window margins will result if precompensation is used during writing in order to limit the effective peak shift in the read-back signal. Only inner tracks, i.e., tracks 40 to 50, starting and running through track 79 need be precomped. A PLO and Write Precompensation Application Note is available upon request.

8.1.2.1 Write Precompensation

Write precompensation is required to decrease the effect of bit shift on the reduced bit cell and recovery window timing of MFM data. The window is defined as being the total time allowed for the bit to appear and be recognized. The data recovery window of MFM is two microseconds as opposed to the FM window of four microseconds. The amount of recommended write precompensation for maximum window margin is 250 nanoseconds, early or late, in relation to nominal. Refer to Figure 5.

Write precompensation should be applied to tracks, 43 through 79, on both sides of the diskette. Switching in write precompensation by the controller is required. Precomp should begin at any track between tracks 40 and 50.

Write precompensation is applied to data patterns that will result in a large amount of bit shift. The controller precompensation circuit looks at three bits on each side of a reference bit and determines whether or not to shift.

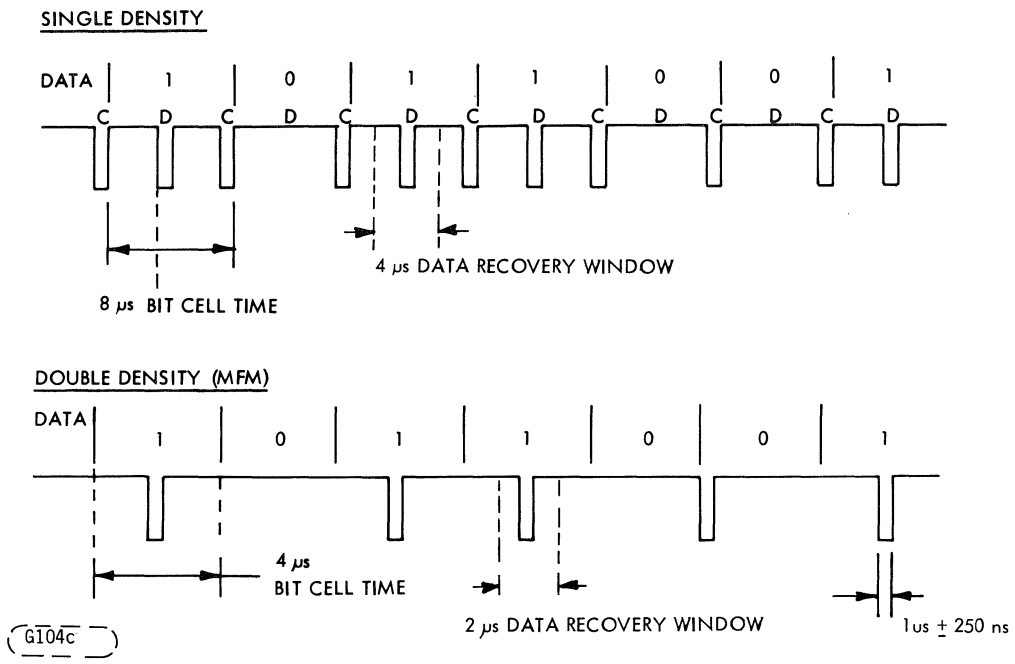


Figure 5. Nominal Data Timing

The following MFM patterns are compensated (bit-shifted) in the direction of the arrow.

LATE	EARLY
X 0 1 1 →	X 1 1 0 ←
1 0 0 0 →	0 0 0 1 ←

X = Don't Care

The following is an explanation of the MFM write precompensation algorithm.

When a data pattern of 011 is written on the disk, the first 1 is shifted toward the 0 (data bit cell with or without flux transition). Write precompensation shifts this 1 in the opposite direction the amount of the expected shift. In the case

of the 1000 pattern, the second 0 (clock bit) shifts toward the first 0 (data bit cell with no flux transition) and this clock bit is compensated late towards the third 0 (clock bit). With pattern 110, the second 1 shifts toward the 0 (bit cell with no transition) so this 1 data bit is compensated early towards the first 1 data bit. In the last pattern, 0001, the third 0 (clock bit) is shifted towards the 1 (data bit) due to the nominal 6 microseconds between these two bits. Thus, the third 0 (clock bit) is compensated early towards the second 0 to counteract shifting towards the 1.

8.2 FORMAT CONSIDERATIONS

Design of the 9409T allows for data recording using either hard or soft sector formats. The following operational tolerances should be considered when selecting a particular format for the system. For additional information, consult the Application Note, 5.25-Inch FDD Format Considerations and Controller Compatibilities.

8.2.1 Index Tolerance

8.2.1.1 Post-Index (Gap No. 1)

Before initial recording of data upon a selected track, a minimum gap time of 1 millisecond is required to allow for drive-to-drive and adjustment tolerances. This is the gap (Gap 1) from the edge of the index pulse to the beginning sync field for the ID field address mark. This gap allows for variations in Index pulse width, speed variations, and interchange tolerances between drives.

8.2.1.2 Pre-Index (Gap No. 4)

The Pre-Index Gap No. 4 is required to compensate for maximum speed variations between drives. Physically, the gap is the space between the last sector and beginning of the index pulse. Its minimum length is 7.2 milliseconds in the recommended formats.

8.2.2 Inter-Record Tolerance

8.2.2.1 Pre-Address (Gap No. 3)

The Pre-address length is a minimum of 1.64 milliseconds, but varies with sector size for 128-byte sector lengths. The pre-address gap timing is Gap No. 3 and is based on the tunnel-erase structure of the read/write head and maximum erase-circuit turn-off delay.

8.2.2.2 Pre-Data (Gap No. 4)

Pre-data gap is Gap No. 2 and has a minimum timing requirement of 489 microseconds. Gap timing is determined by the erase turn-on circuit tolerance and the tunnel-erase structure of the read/write head.

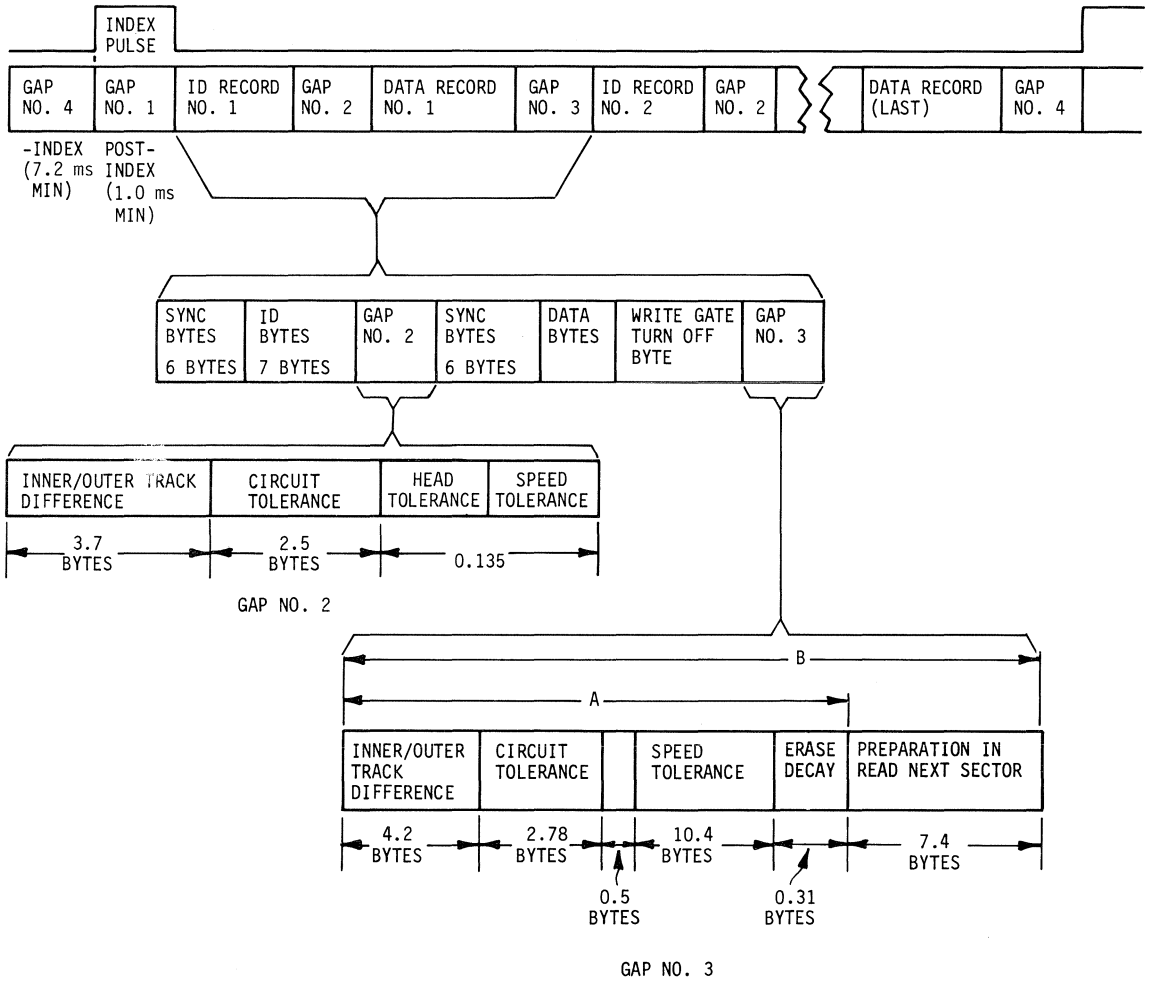
8.2.3 Soft-Sector Formatting

For system use of soft-sector formatting, Figure 6 provides several recommended timing tolerances for individual gaps positioned within the format. For sector formats utilizing MFM recording, Figure 7 presents the minimum gap for timing tolerances required for this recording scheme.

8.2.4 Hard-Sector Formatting

Hard-sector formats use sector holes in the diskette to separate the track into sectors. The mechanical and electrical parameters of flexible disk drives and media require the format to consist of three parts: Preamble, User Data, and Postamble.

The Preamble consists of a defined number of gap bytes that are written starting at the beginning of the sector pulse. The Preamble length is defined so that under worst-case conditions User Data will not be lost due to sector pulse jitter or erase delays.



A - 18.2 BYTES - TO PREVENT DATA LOSS UNDER WORST-CASE CONDITIONS.

B - 25.6 BYTES - GUARANTEES CONSECUTIVE SECTOR OPERATION UNDER WORST CASE CONDITIONS.

ZZ102b

Figure 6. Minimum Requirements for Single-Density Soft-Sector Format (Part 1)

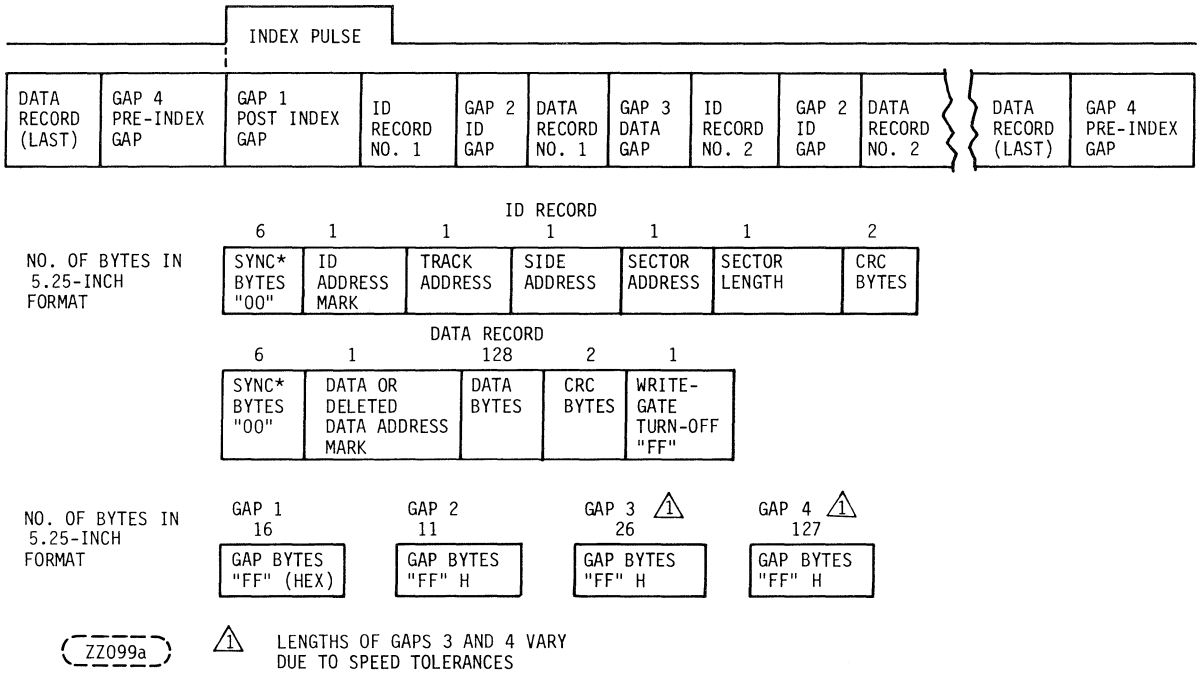
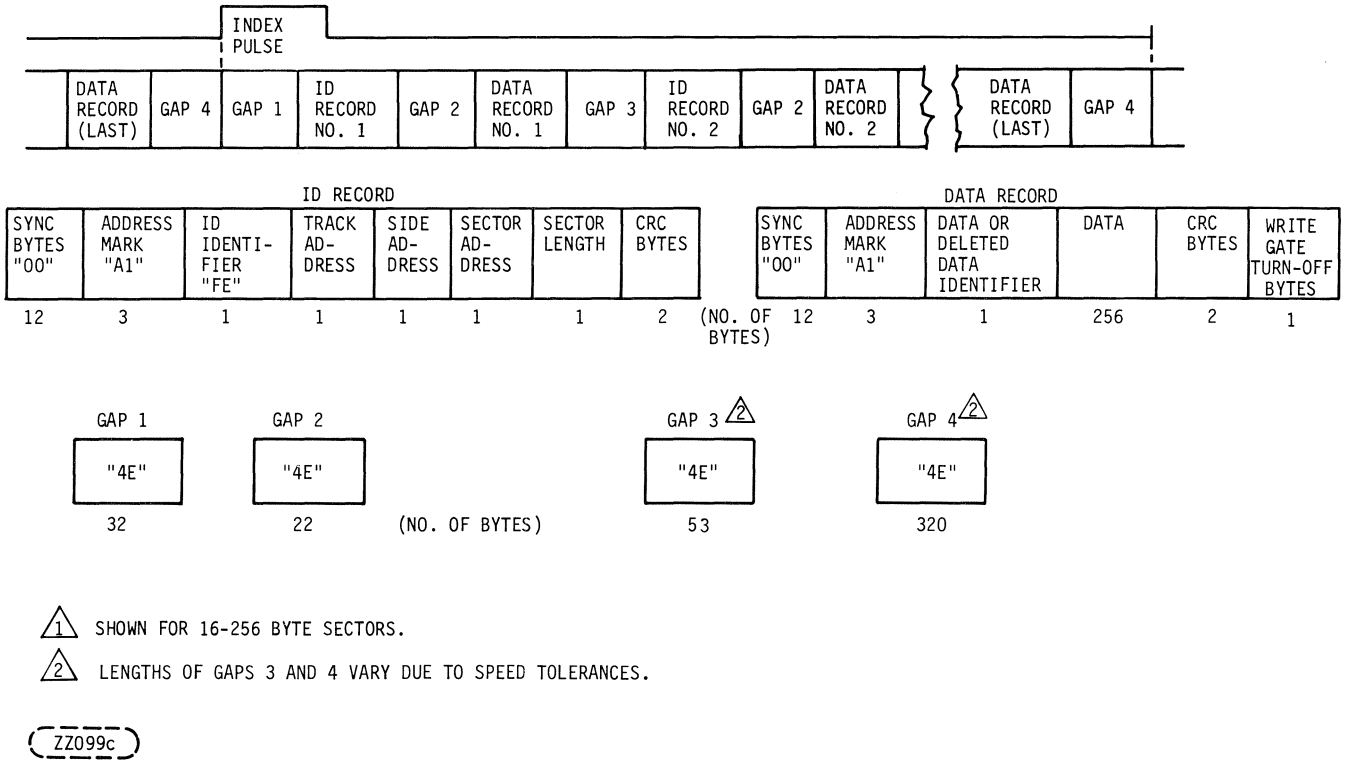


Figure 6. Minimum Requirements for Single-Density Soft-Sector Format (Part 2)

User Data consists of data, sync bytes, ID bytes, and CRC bytes used by the particular format. User Data and the Preamble are both written each time a sector is updated.

A buffer zone, or Postamble, is required at the end of a sector between the User Data and the earliest sector pulse.

Recommended minimum Preamble and Postamble gaps are given in Table 2 and illustrated in Figure 8.



1 SHOWN FOR 16-256 BYTE SECTORS.

2 LENGTHS OF GAPS 3 AND 4 VARY DUE TO SPEED TOLERANCES.

ZZ099c

Figure 7. Recommended Double-Density Format

Table 2. Recommended Preamble/Postamble Gap

POSTAMBLE		BLANK (NO CHARACTER WRITTEN)	ZEROES (CHARACTER WRITTEN)
16 Sectors Per Track	Minimum Preamble	8 bytes	24 bytes
	Maximum User Data	156 bytes	148 bytes
	Minimum Postamble	22 bytes	15 bytes
10 Sectors Per Track	Minimum Preamble	8 bytes	23 bytes
	Maximum User Data	269 bytes	261 bytes
	Minimum Postamble	27 bytes	19 bytes

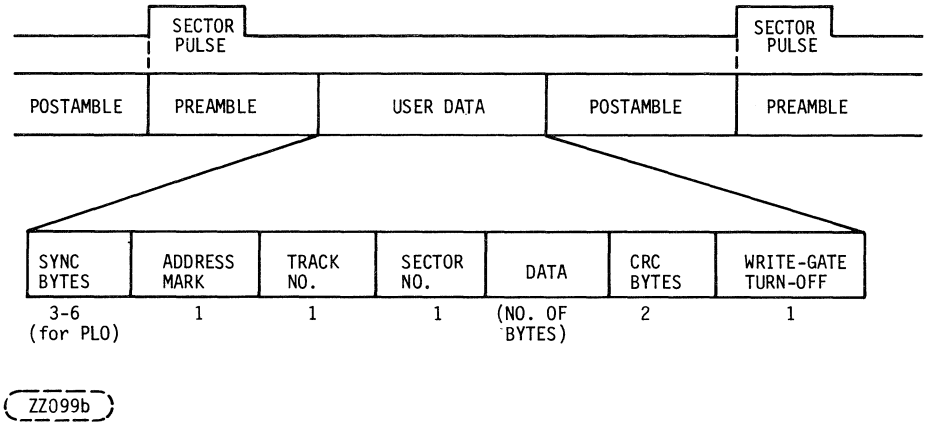


Figure 8. Recommended Hard Sector Format

As shown in Table 2, there are two ways to configure the Postamble Field: Blank and Zeroes.

1. Blank (No Character Written) - the controller can turn off Write Data at the end of the User Data field and leave the Postamble as an empty or blank field.

2. Zeroes (Character Written) - the Write Gate can turn off Write Data at the beginning of the next sector pulse. When doing this, the controller must write gap characters; that is, all zeroes in the Postamble field.

The Write Gate Turn-Off at the end of the User Data field is recommended because it allows the use of a larger User Data field. The values given for maximum User Data field guarantee maximum recovery for read-after-write operation under worst-case conditions.

9.0 INSTALLATION INFORMATION

9.1 ELECTRICAL INTERFACE

The electrical interface between the 9409T and host system consists of two primary connectors. The I/O signal connector J1 contains all interface signals transmitted to and from the drive. Connector J2 supplies DC power to the 9409T. AC power is not applicable to this device. A separate frame ground connection is available at the rear of the unit.

See Figure 9 for interface connections and Figure 10 for connector locations.

9.2 POWER CONNECTOR

DC power is provided to the 9409T by the host system through connector J2, which is mounted on the non-component side of the printed circuit board near the spindle drive motor. Refer to Figure 10 for connector location and Table 3 for pin assignments. Table 4 lists the recommended mating connector for J2.

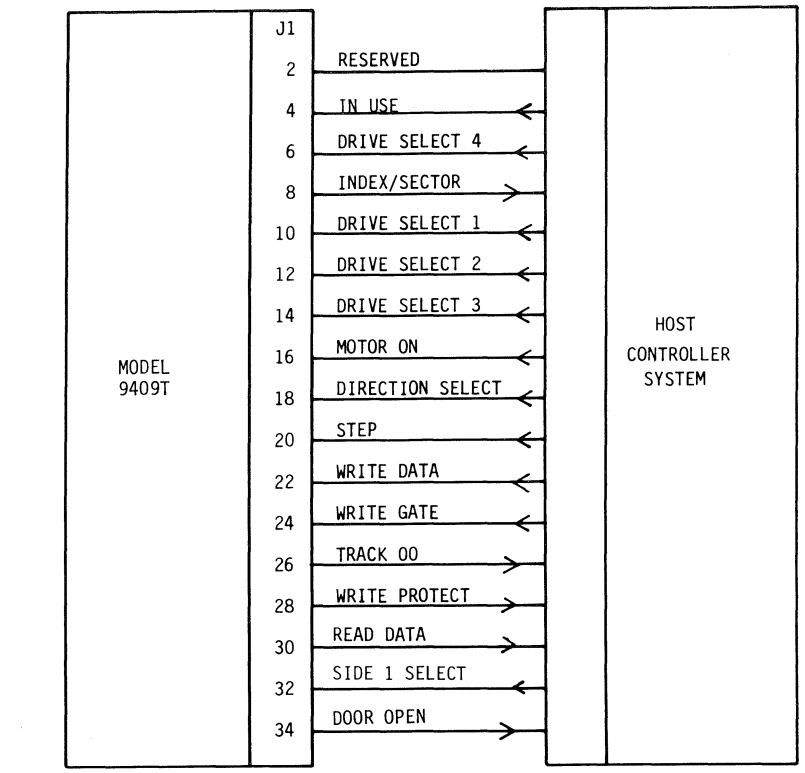


Figure 9. Interface Connections

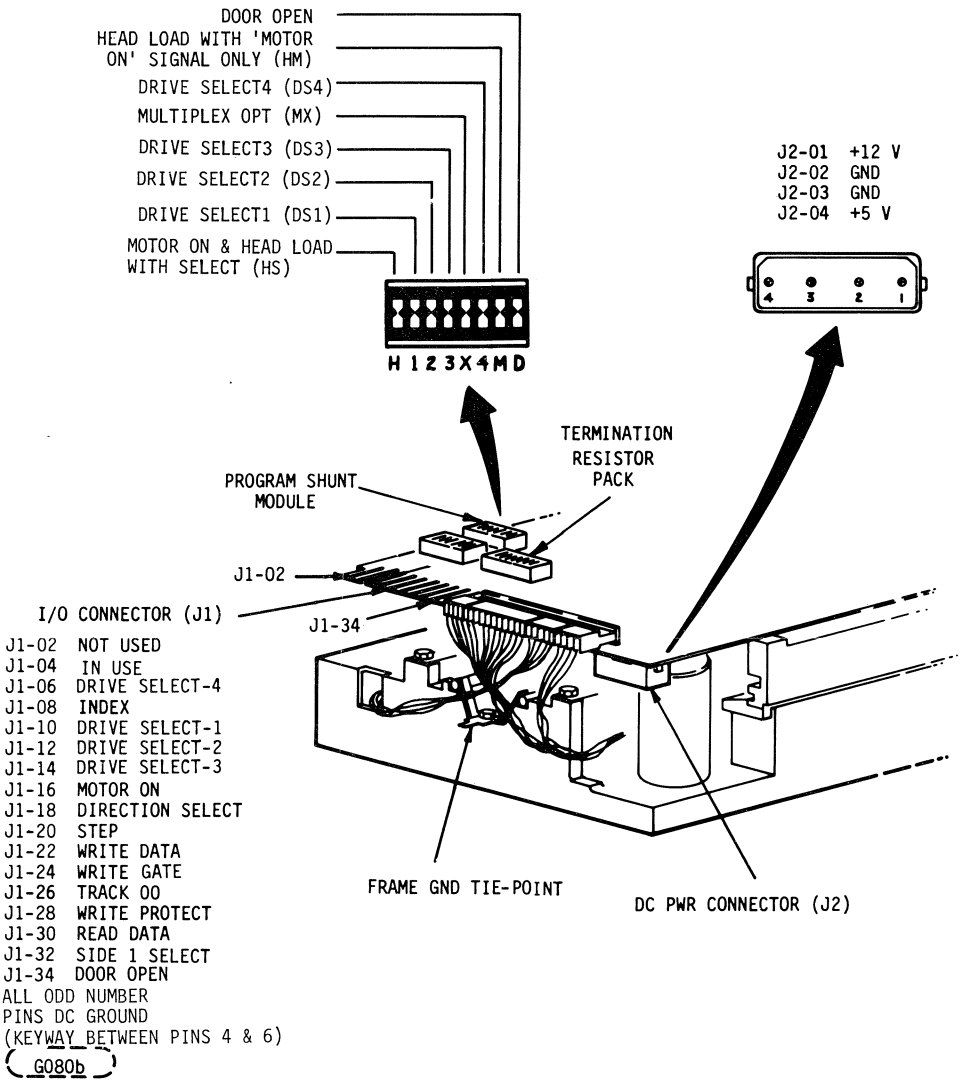


Figure 10. Input/Output (J1), DC Power (J2), Terminator, and Programmable Shunt Module Location/Description

Table 3. DC Interface

POWER LINE DESIGNATION	PIN NUMBER
+12 Volts	J2-01
+12 Volts Return	J2-02
+5 Volts Return	J2-03
+5 Volts	J2-04

Listed in Table 4 is connector information for J2/P2.

Table 4. J2/P2

TYPE OF CABLE	CONNECTOR	CONTACTS
18 AWG	J2, 4-Pin AMP Mate-N-Lok 350211-1 P2, AMP 1-480424-0	AMP 61473-1

9.3 I/O CONNECTOR

The I/O connector J2 is a 34-pin PCB edge connector. Its location is shown in Figure 10. The dimensions for J1 are shown in Figure 11. The pins are numbered 1 through 34, with the even-numbered pins appearing on the component side of the PCB and odd-numbered pins on the non-component side. A key slot is provided between pins 4 and 6 for optional connector keying.

The maximum I/O cable length between the host controller and the 9409T (or last FDD in a daisy chain configuration) should be no greater than 10 feet (3.048 meters). Refer to Section 9.5 for more detailed information.

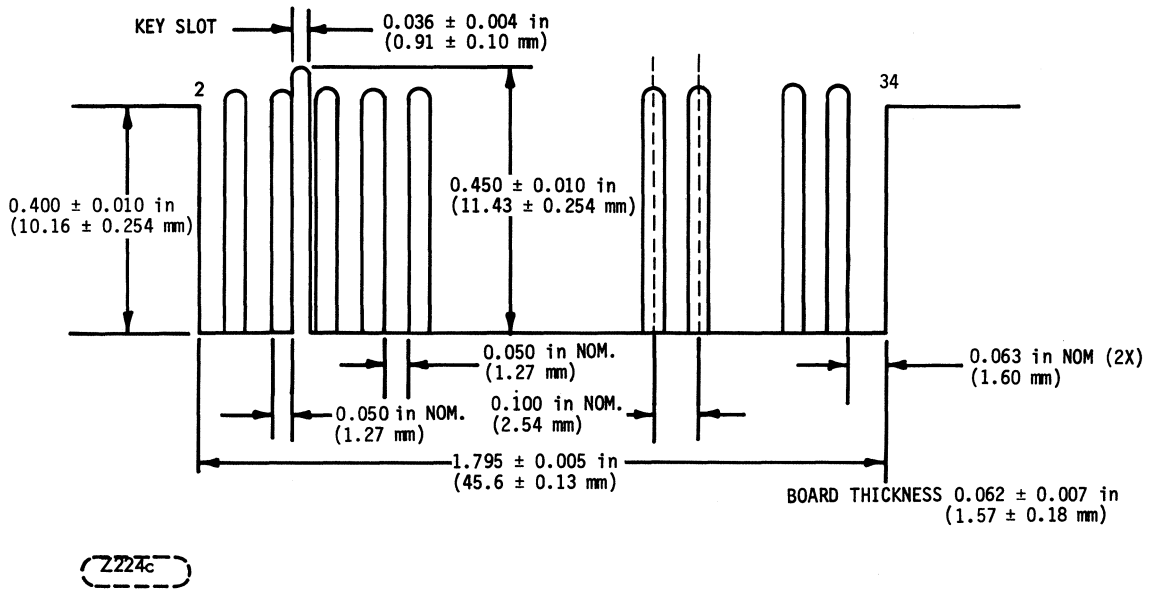


Figure 11. I/O Connector (J1) Dimensions

The recommended mating connector for J1 and type of cable are shown in Table 5.

Table 5. J1/P1

TYPE OF CABLE	CONNECTOR	CONTACTS
Twisted Pair, 26 AWG	AMP 583717-5	AMP 1-583616-4
Flat Cable	3M Scotchflex 3463-0001	---
---	AMP Keying Pin 583274-2	---

9.4 GROUNDING REQUIREMENTS

To ensure optimum performance and noise immunity, the 9409T must be frame grounded to the host equipment AC ground. A Faston tab has been provided on the rear of the casting where its mating Faston connector can be attached or soldered. The tab is AMP part number 61664-1 and its mating connector is AMP part number 60972-1. Figure 10 shows the ground point.

9.5 CONFIGURATIONS

9.5.1 Daisy-Chain Configuration

A daisy-chain configuration incorporates interfacing of the disk drives on a common I/O cable. Only the FDD which is selected by the host system has its control and data signals enabled through this common interface. The program shunt module shown in Figure 10 allows creation of each individual drive-selection address for each drive in the daisy-chain. Four drive selection addresses are made available by the program shunt module for interfacing up to four drives in a daisy chain configuration (shown in Figure 12).

Refer to section 12.0 for descriptions of drive selection and head load options.

Termination in a daisy chain configuration is described in paragraph 9.6.3.

9.5.2 Radial Configuration

In a radial configuration the disk drives do not share the same I/O cable. Each drive is interfaced to its own I/O cable which, in turn, allows interfacing of more than four drives and a variety of system operational techniques. Drive-selection addressing must be accommodated at the program shunt module to allow activation of I/O signals.

Refer to section 12.0 for descriptions of drive select and head load options.

A radial configuration is shown in Figure 12 and termination is described in paragraph 9.6.2.

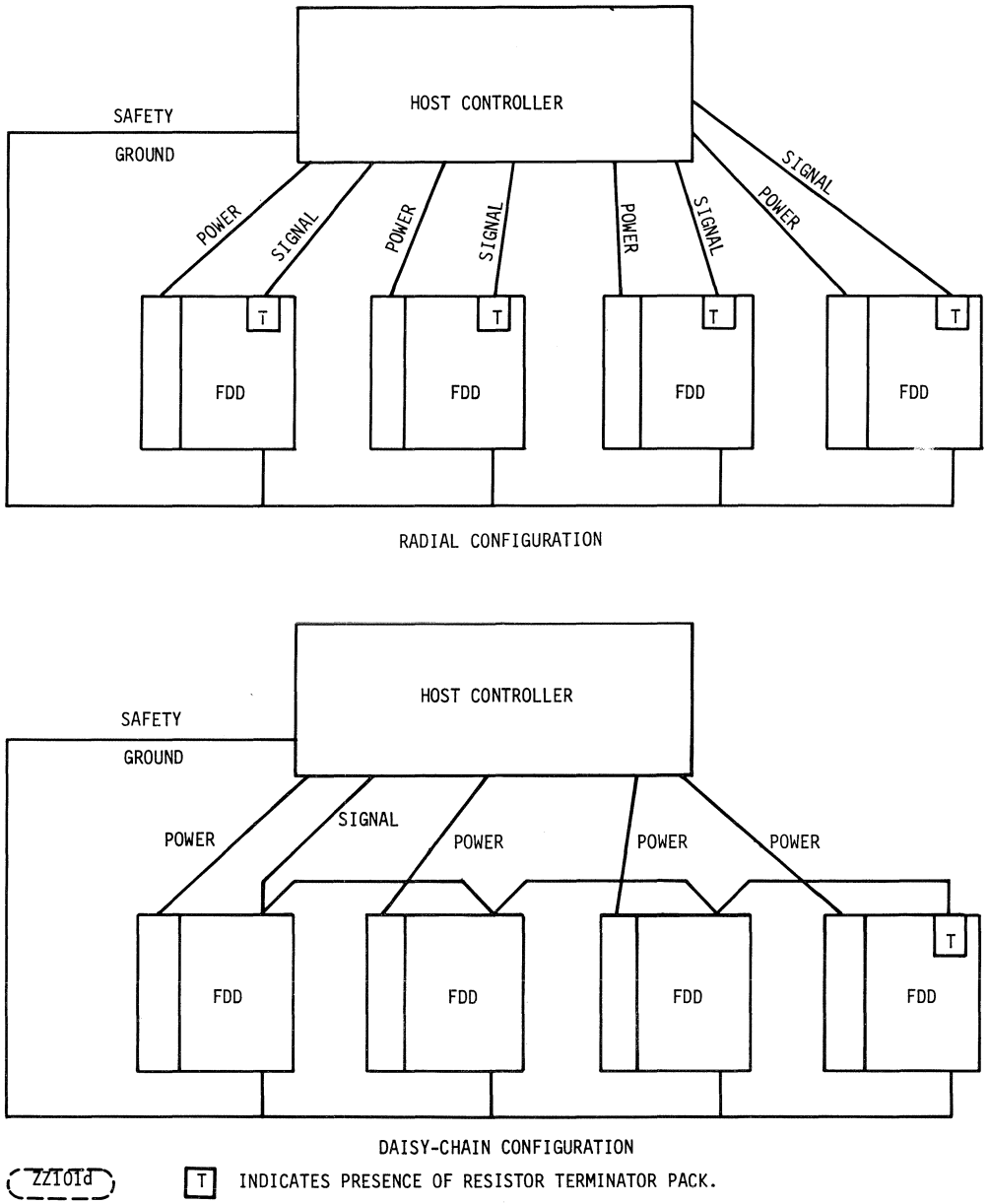


Figure 12. FDD System Connection Configurations

9.6 INTERFACE TERMINATIONS

Figure 13 provides a logical representation of the interface line termination used for the 9409T.

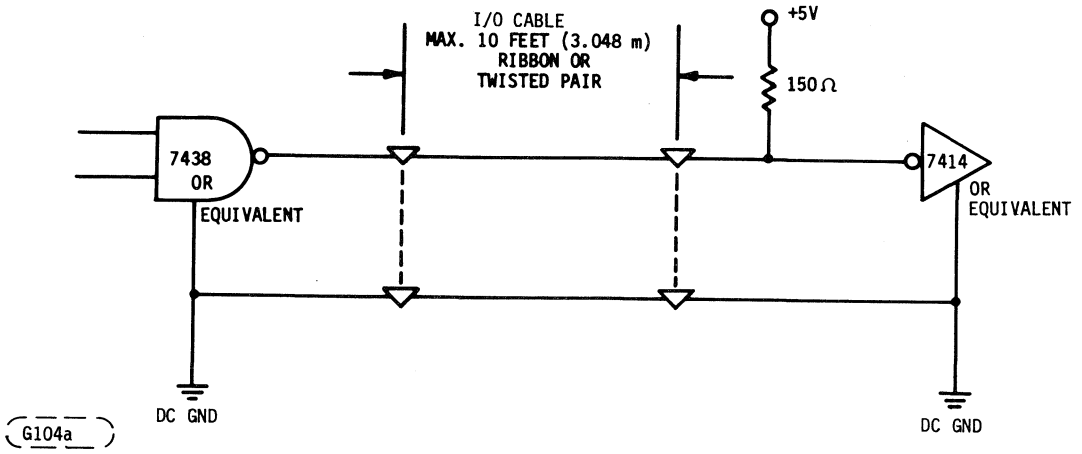


Figure 13. Interface Terminations

9.6.1 Areas of Termination

Termination for each input line is accommodated by a 150-ohm resistor pack installed in a DIP socket located on the PCB of the 9409T (Figure 10).

9.6.2 Termination in a Radial Configuration

In a single drive or radial configuration, the resistor pack must be kept in place on each PCB to provide the proper terminations.

9.6.3 Termination in a Daisy Chain Configuration

In a daisy chain configuration, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed.

9.6.4 External Terminations

For configurations requiring external termination, the user must terminate each input line to +5 V dc through a 150-ohm, 1/4-watt resistor.

10.0 ERROR RECOVERY

Seek errors will rarely occur unless the stepping rate is exceeded. In the event of a seek error, recalibration of track location can be achieved by repetitive step-out commands until a Track 00 signal is received.

To guard against degradation from imperfections in the media, no more than four attempts to write a record should be attempted when read-after-write errors are encountered. If a record cannot be successfully written within four attempts, it is recommended that the sector or track be labeled defective and an alternate sector or track assigned. If more than two defective tracks are encountered, it is recommended that the diskette be replaced.

In the event of a read error, up to 10 attempts should be made to recover with reread operations. If after 10 attempts the data has not been recovered, step the head several tracks away and then reposition to recover the data. Unloading the head when data transfers are not imminent will increase the data reliability and extend diskette life.

11.0 INTERFACE SIGNAL DESCRIPTION

11.1 ACTIVE/INACTIVE LOGIC SIGNALS

Signal State	Logic Level	Voltage
Inactive (False)	High	+2.5 V to +5.25 V
Active (True)	Low	0.0 V to +0.4 V

11.2 INPUT/OUTPUT SIGNALS

11.2.1 Drive Select

Drive Select (J1-6, -10, -12, -14) activates the internal circuitry of a selected drive. Activating this line to a logic low (active) level will condition the drive's input and output lines. All input and output lines are gated with Drive Select with the exception of Motor On (J1-16) and In Use (J1-4).

After the activation of the Drive Select line, a minimum time delay is required before the start of any write or read operation. (See Figures 21 and 22.) Table 6 includes these minimum time delays which are dependent on the drive shunt configuration.

Table 6. Minimum Time Delays

MODE OF OPERATION	TIME TO VALID READ DATA
Motor up to speed and head loaded (with or without head load option).	2 milliseconds
Optional head load.	50 milliseconds
Motor on when drive selected.	150 milliseconds typical

The operation of the Drive Select lines and selection of a designated drive is controlled through the programmable shunt position DS1, DS2, DS3, and DS4. Refer to section 12.0 for further information.

11.2.2 Motor On

The Motor On circuit can be configured to operate in any of the three different ways described below.

1. If shunt HM is shorted and HS is open, the drive motor will turn on and the head will load when a logic low is applied to the Motor On line (J1-16). There is a 150-millisecond delay from active Motor On until there is valid read data.

    a. The advantage of this configuration is that after initial motor up-to-speed delay, the drive can be selected (Drive Select line active) and there is a maximum of 150 milliseconds (typical) before valid read data. (Motor must be turned on for this to be valid; with or without the head load option.)

    b. The disadvantage of this configuration is that with the motor turned on and the head loaded at all times, there is increased wear to the drive motor, media, and heads.

2. If shunt HS is shorted and HM is open, the drive motor will turn on when a logic low is applied to any of the Drive Select lines (J1-6, -10, -12, or -14). This configuration uses the Drive Select line to start the motor and load the heads. The minimum delay from drive selection to valid read data is now 150 milliseconds (typical) due to the delay for motor start time.

    a. The advantage of this configuration is reduced motor, media, and head wear because motor, media, and heads are only used when needed (selected).

b. The disadvantage of this configuration is that the maximum time from drive selection to valid read data is 150 milliseconds.

3. Same shunt configuration as case 2; that is, HS shorted and HM open. However, the Motor On line, rather than the Drive Select line, is used to start the motor. In this case, if the head load option is used, the head is loaded when the drive is selected and a 50-millisecond delay is required before there is valid read data. If the head load option is not used, there is valid read data 2 microseconds after drive selection. (The above two timing intervals assume that motor-up-to-speed delay has been met.)

   a. The advantage of this configuration is that it can be used to obtain the maximum drive-to-drive access time in a daisy chain (assuming that the head load option is not used).

   b. The disadvantage of using the Motor On line to turn on the drive motor is that all drives in a daisy chain configuration turn on the motor when a low level is applied to Motor On.

11.2.3 Direction Select

Direction Select (J1-18) transfers a control signal to determine the direction the read/write head will move when the Step line is pulsed.

A logic high defines the direction as "out," and if a pulse is applied to the Step line, the read/write head will move away from the center of the diskette. Conversely, if this input is a logic low level, the direction of motion is defined as "in," and if a pulse is applied to the Step line, the read/write head will move toward the center of the diskette. Refer to Figure 14 for timing details.

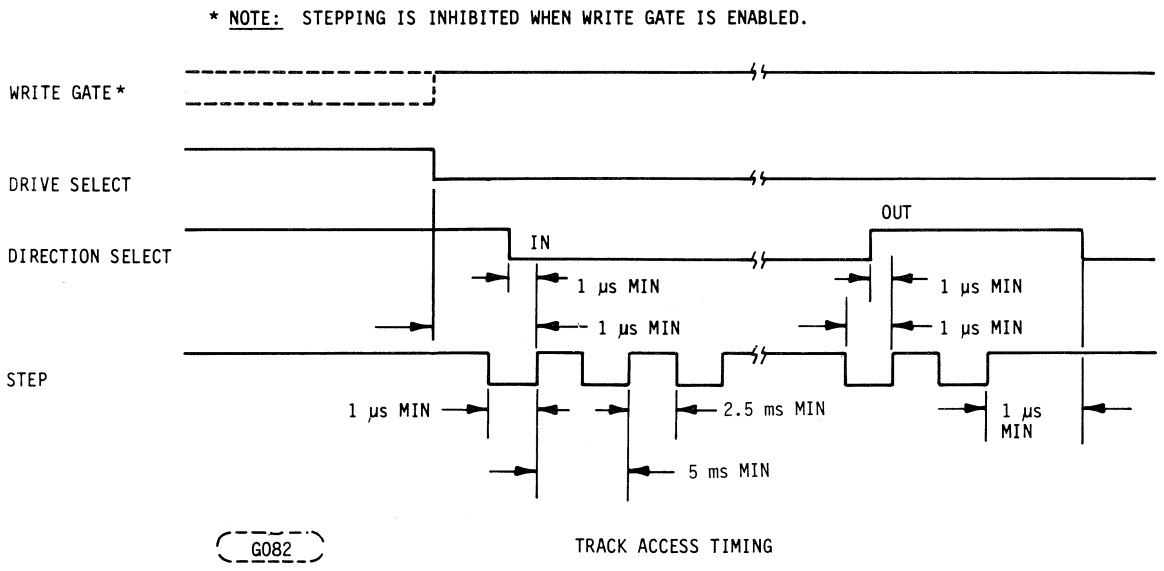


Figure 14. Track Access Timing

11.2.4 Step

Step (J1-20) pulses are control signals which cause the read/write head to move in a direction determined by the condition of the Direction Select line.

Access motion is initiated on each logic low-to-high transition, or on the trailing edge of each signal pulse. Any change in the Direction Select line must be made at least 1 microsecond before the trailing edge of the Step pulse. A requirement exists for the Direction Select logic level to be maintained 1 microsecond after the trailing edge of the Step pulse.

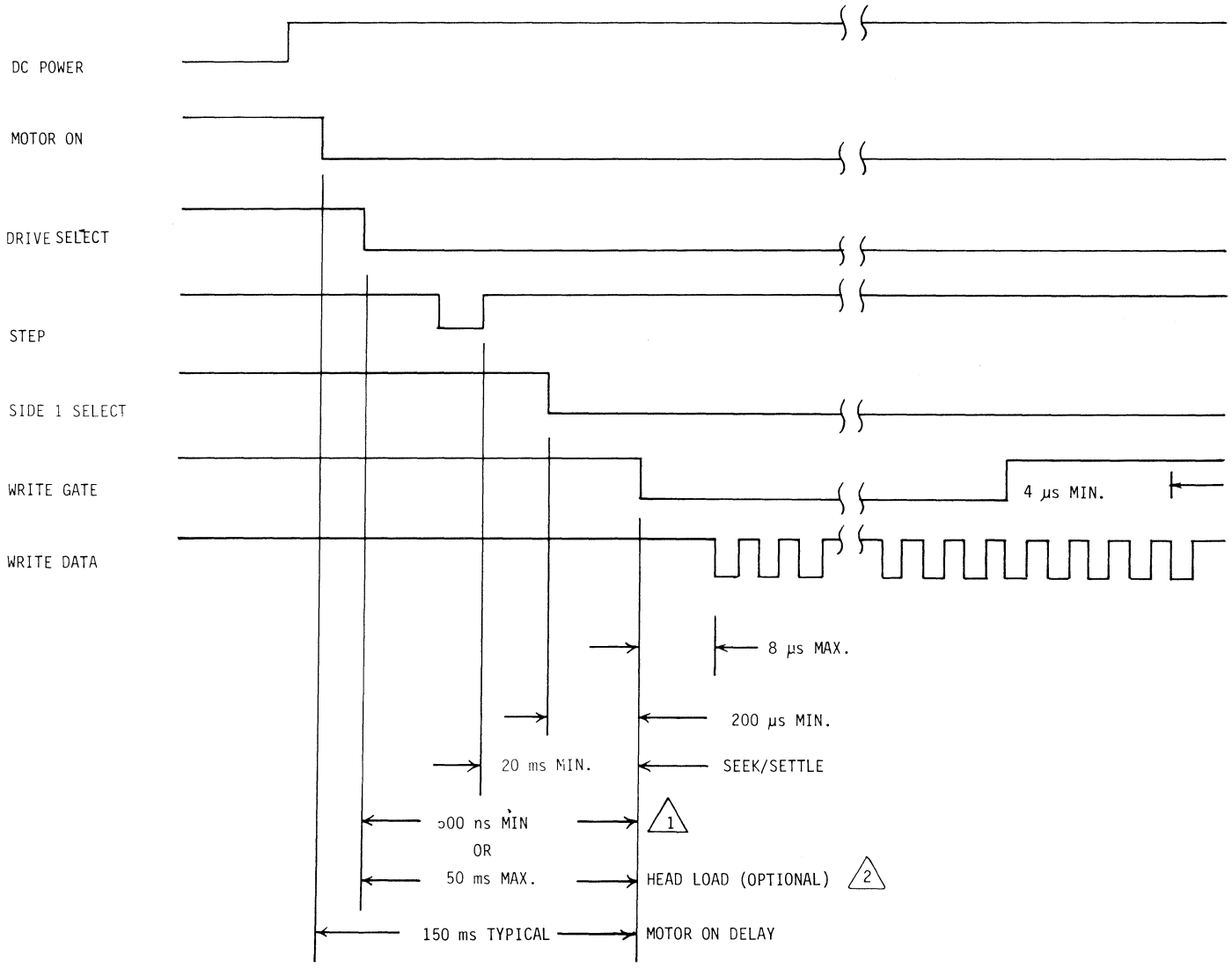
Activation of the Write Gate line while using a write-protected diskette will not inhibit movement of the read/write head during transmission of Step pulses.

Refer to Figure 14 for timing details.

11.2.5 Write Gate

The active state of Write Gate (J1-24), or logic low, enables Write Data to be written on the diskette. The inactive state, or logic high, enables the Read Data logic and Step logic.

A maximum delay time of 8 microseconds is allowed between the switching sequence of the Write Gate line and the leading edge of the first data pulse to be recorded. Figure 15 illustrates this sequence of events.



1 ASSUMES HEAD IS LOADED AND MOTOR IS UP TO SPEED WHEN DRIVE IS SELECTED.

GG142a 2 IF HEAD LOAD SOLENOID IS NOT USED, 500 ns MINIMUM.

Figure 15. Write Initiate Timing

11.2.6 Write Data

Write Data (J1-22) provides data to be written on the diskette. Each pulse transition from a logic high to a logic low level, as clocked through a D flip-flop within the logic circuitry, will cause current through the read/write head to reverse, creating a data bit.

Signals transmitted on the Write Data line are transmitted in the form of clock/data composite pulses. The recommended pulse width for both data bit and clock pulse is 200 nanoseconds (minimum) and 2.1 microseconds (maximum). Generation of data on the media is possible only during activation of the Write Gate to a logic low level. Figure 16 illustrates these timing sequences. Refer to paragraph 8.1.2.1 for recommended write precompensation.

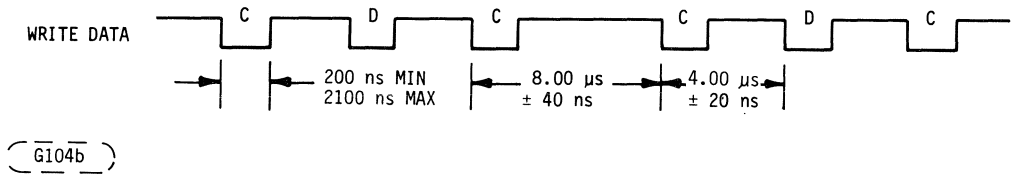


Figure 16. Write Data Timing (FM)

11.2.7 Read/Write Operations

At the conclusion of a write or read operation, there are a number of timing considerations which must be observed.

1. After any write operation, there is a 1-millisecond minimum time delay to allow for the erase turn-off delay required with the tunnel erase head. Interface signals which must

remain in a stable state during this delay are: a) Drive Select, b) Head Load, c) Motor On, d) Side 1 Select, and e) Step. This can be considered as write operation-to-read-operation time.

2. If a side change occurs at the termination of a write operation, the side change delay of 200 microseconds plus the 1-millisecond erase turn-off delay is required; that is, a total of 1200 microseconds. This is write-to-read time including a side change.

3. In going from a read operation to a read operation including a side change, only the side change delay of 200 microseconds must be observed.

Refer to Figure 17 for detailed timing.

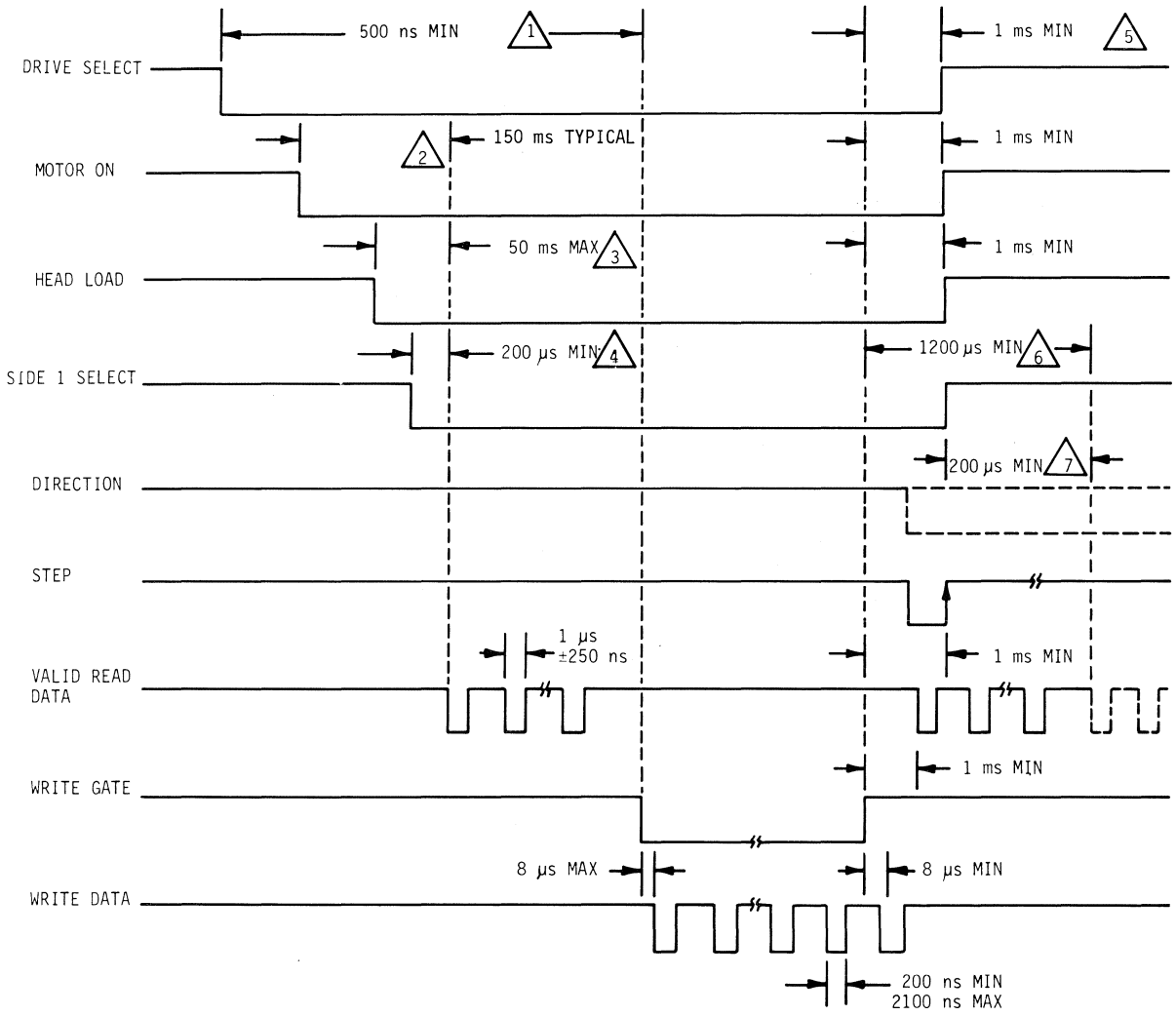
11.2.8 Track 00

The active or logic low state of the Track 00 signal (J1-26) indicates the read/write head is positioned at track 00.

This signal is at a logic high level (inactive state) when the read/write head is not at track 00.

When the read/write head is at track 00, and an additional step-out pulse is issued to the drive, motion is inhibited and the Track 00 signal will remain active (logic low).

A step-out sequence is recommended on a power-up sequence or a restore function to recalibrate for track 00 position.



1. ASSUMES MOTOR ON AND HEAD LOADED.
2. ASSUMES NO HEAD LOAD SOLENOID.
3. ASSUMES MOTOR UP TO SPEED. (50 ms IF HEAD LOAD OPTION USED.)
4. ASSUMES MOTOR UP TO SPEED AND HEAD LOADED.
5. THE 1 ms IS THE ERASE TURN-OFF DELAY REQUIRED FOR TUNNEL ERASE HEADS.
6. THE 1200 µs IS THE ERASE TURN-OFF DELAY PLUS SIDE CHANGE DELAY.
7. THE 200 µs IS REQUIRED FOR A CHANGE IN SIDE CHANGE.

GG143a

Figure 17. Read/Write Operations

11.2.9 Index/Sector

The Index/Sector signal (J1-8) is detected and transmitted to the controller each time an index or sector hole is sensed by the index/sector photocell detector.

The signal generated is a 0.5 millisecond (minimum) pulse which indicates the presence of an Index or Sector hole during its transition from a logical one to a logical zero level as shown in Figure 18.

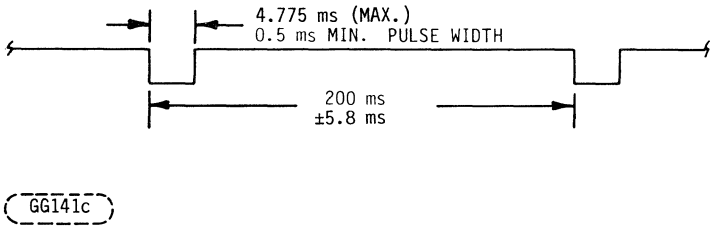


Figure 18. Index Timing (Soft-Sector Media)

Using soft-sectored media, a single pulse will be generated per revolution of the diskette, every 200 ±5.8 milliseconds, indicating the physical beginning of a track.

Using hard-sectored media (16 or 10 sectors), 17 or 11 pulses, respectively, will be generated per revolution. Figures 19 and 20 provide an illustration of index/sector timings for 16 and 10 sector applications.

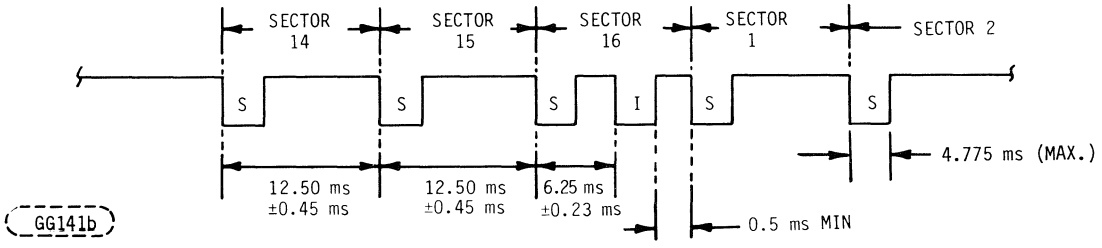


Figure 19. Index/Sector Timing (16 Hard-Sector Media)

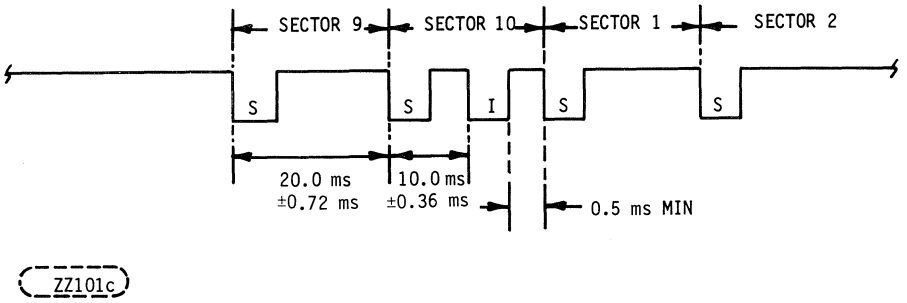


Figure 20. Index/Sector Timing (10 Hard-Sector Media)

11.2.10 Read Data

Read Data (J1-30) provides a transmission of composite clock and data pulses of 1 microsecond, ±250 nanoseconds, to indicate the presence of either a clock or data pulse by means of a logic high-to-low transition. Figures 21 and 22 provide references for timing and bit shift tolerance within normal media variations.

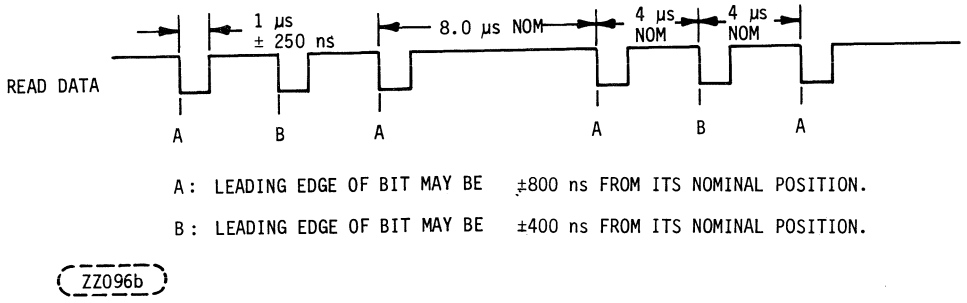


Figure 21. Read Signal Timing

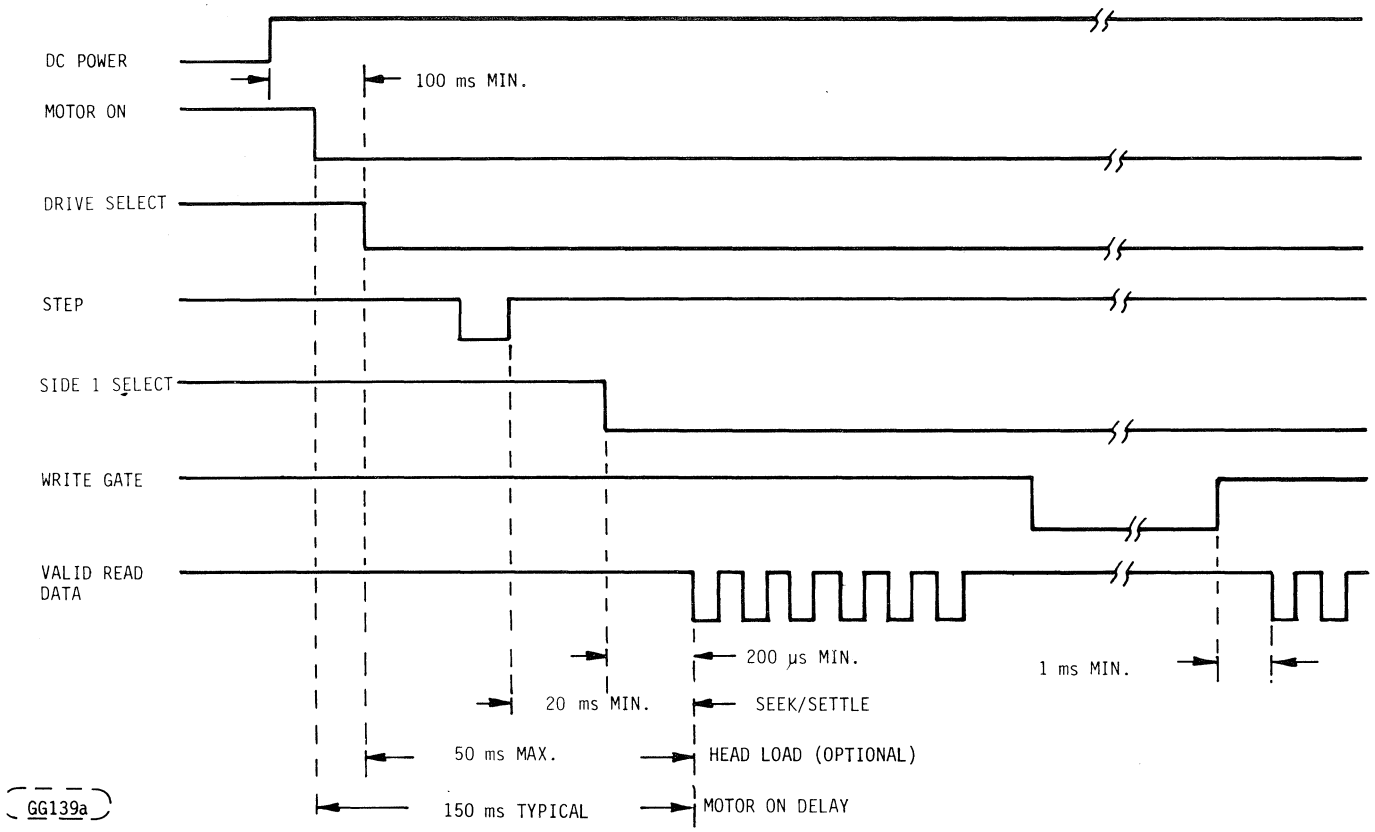


Figure 22. Read Initiate Timing

11.2.11 Write Protect

Write Protect (J1-28) notifies the user that a write protected diskette (i.e., when the write protect slot on the diskette is masked) is installed in the drive. The normal configuration is that a logic low level will appear on the interface line J1-28 indicating that the diskette is write protected and writing will be inhibited.

If it is necessary to invert this output signal so that an unmasked slot gives a write protect indication and inhibits writing, the user must move the black wire on the write protect

switch to the unused switch pin (the one closest to the PWA). This gives write protect indication to the I/O and inhibits writing on a diskette with an unmasked slot.

11.2.12 Side 1 Select

Side 1 Select (J1-32) defines which side of a two-sided diskette is used for reading and writing.

A logic high selects side 0, the lower surface; a logic low selects side 1, the upper surface. When the selected diskette side is changed, a delay of 200 microseconds is required before any read or write operation is initiated (assuming that drive is selected, motor is on, and head is loaded).

11.2.13 In Use

In Use (J1-4) allows for the activation of the activity LED independent of Drive Select. When a logic low is applied to In Use the activity LED is turned on whether or not the drive is selected. In daisy-chain operation, all drives would have the activity LED illuminated if In Use is active.

11.2.14 Door Open (Optional Feature)

Door Open (J1-34) indicates that the door is open. By cutting the program shunt module, DO, the user can enable a latch circuit which will monitor and store any door-disturbed status while the drive is not selected. This signal will be active when the drive is selected. Unless the door remains open, the latch is cleared when the Drive Select signal is removed.

If the shunt is not cut, the door open status is always active to the interface. The status is not latched (stored) but changes with each door opening. The drive is shipped with shunt DO not cut (shorted).

12.0 CUSTOMER SELECTABLE OPTIONS

The 9409T contains a 16-pin program shunt module mounted on the PCB (Figure 23) which allows the drive to be selected to operate in a single drive system or a multiplexed drive system.

As shipped from the factory, each shunt position is shorted. Drive selection is accomplished by cutting selected shunt positions.

Head Load and Door Open are optional features which can be supplied on request.

The program shunt module is Amp part number 435704-8. The shunt positions can be cut using an Amp cutting tool (1-435830-1). The shunt is installed in a DIP socket and, at the customer's option, can be replaced by a DIP switch (Amp 435626-5).

Table 7 provides a listing of optional configurations which can be utilized by the customer.

12.1 MULTIPLEX OPTION

The 9409T is shipped from the factory configured to operate in a single drive system. To activate the multiplex option, cut MX (5-10) position of the programmable shunt. This will allow the multiplexing of I/O lines. For single drive applications, shorting MX will cause a constant enable on the I/O signal lines whenever the drive is powered on.

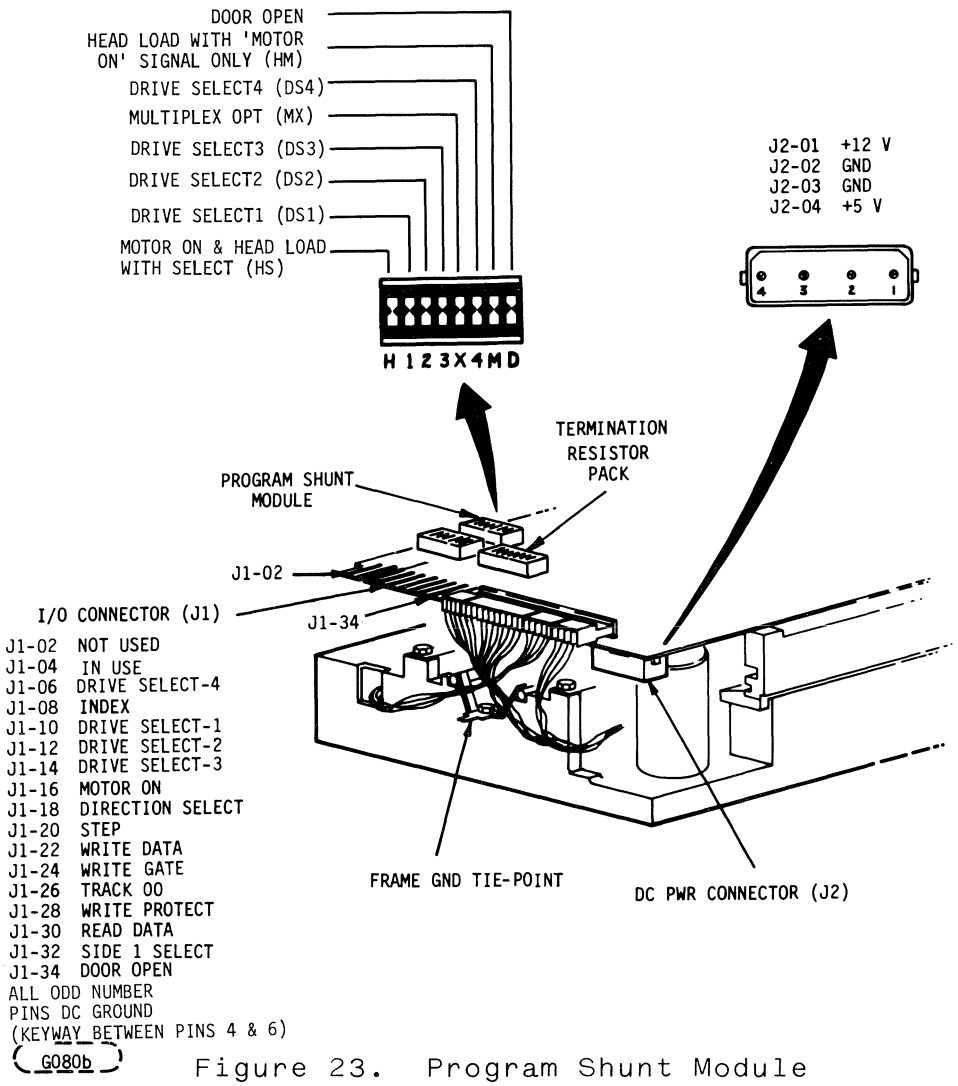


Figure 23. Program Shunt Module

12.2 DRIVE SELECT OPTIONS (1, 2, 3, 4)

The 9409T utilizes four input lines for designation of a particular drive. With MX (5-10) cut, positions DS1 through DS4 are used to select the Drive Select line which will activate the unique drive. Only the drive with its Drive Select line activated will respond to the input lines, gate the output lines, and turn on the indicator located on the front panel. (Exception: the In Use line will turn on the indicator independent of all other lines.) For example, in designating a drive as Drive 1, the user must cut Drive Select shunts DS2,

DS3, DS4 (pins 3-12, 4-11, and 6-9, respectively) and leave DS1 (pins 2-13) shorted. Refer to Figure 24 for Drive Select shunt configurations.

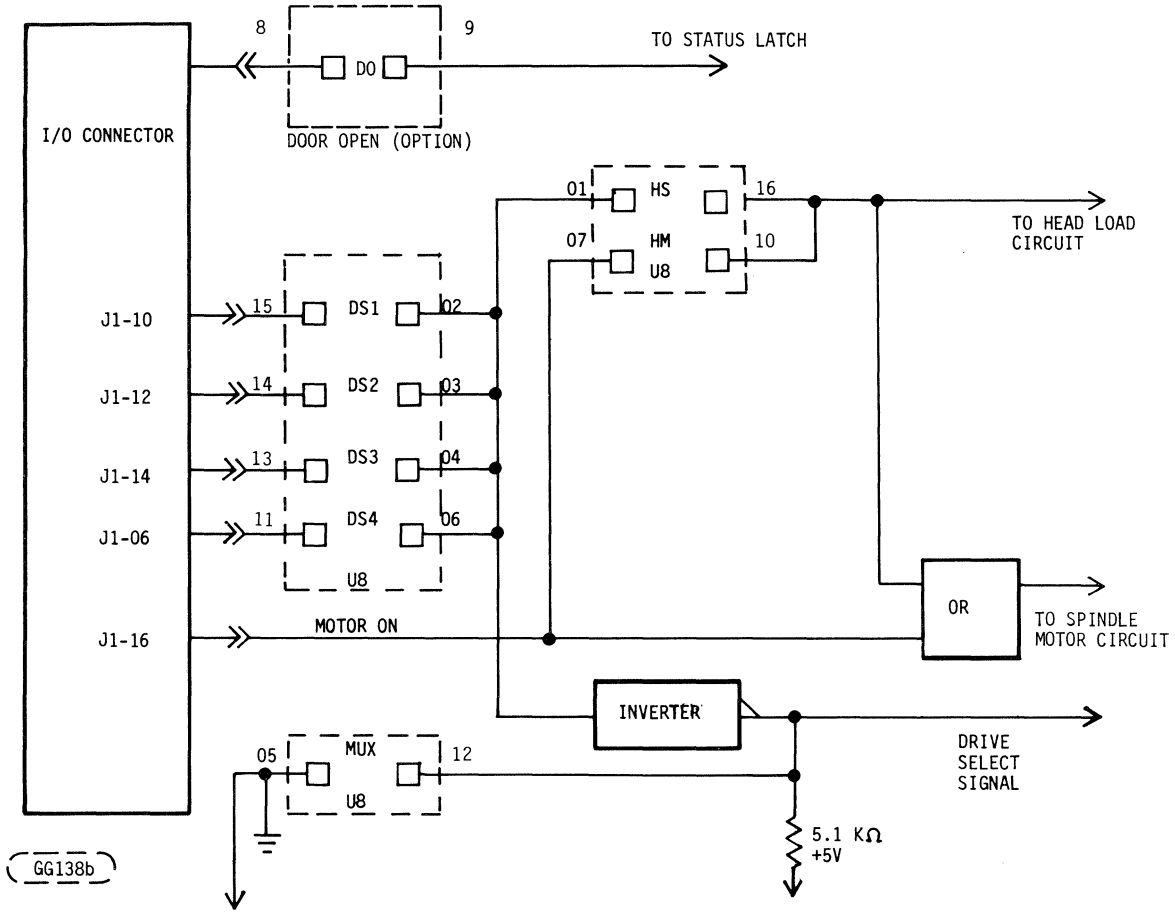


Figure 24. Drive Select Shunt Configuration

12.3 HEAD LOAD WITH MOTOR ON

With HM (7-8) shorted and HS (1-14) open*, the read/write head will load against the media when the Motor On line is activated to a logic low.

12.4 HEAD LOAD WITH DRIVE SELECT

With HS (1-4) shorted and HM (7-8) open*, the head load solenoid will energize with Drive Select activated and load the read/write head.

12.5 DOOR OPEN (Optional Feature)

Door Open indicates that the door is open. By cutting the programmable shunt module, DO, the user can enable a latch circuit which will monitor and store any door-disturbed status while the drive is not selected. This signal will be active when the drive is selected. Unless the door remains open, the latch is cleared when the Drive Select signal is removed.

If the shunt is not cut, the door open status is always active to the interface. The status is not latched (stored) but changes with each door opening. The drive is shipped with shunt DO not cut (shorted).

---

*It is an invalid configuration to have both HS (1-14) and HM (7-8) shorted. In such a configuration, input current to Motor On and/or Drive Select may damage drivers on the host.

12.6 HEAD LOAD SOLENOID (Optional Feature)

In most applications, a head load/unload solenoid is not required. It is optional and can be supplied to customers on request. The head load solenoid option is recommended to extend media life and in all applications where it is impractical to turn the spindle motor off when the drive is not selected.

When this option is present (HS shorted, HM open), the solenoid may be activated and the heads loaded against the media when the drive is selected. With HM shorted and HS open, the solenoid will load when the Motor On line is activated to a logical 0 level. All read and write operations must be delayed for 50 milliseconds from the time of solenoid activation to permit the head to properly position itself against the media.

If the head-load solenoid is not used, the heads are loaded onto the media at all times. The drive spindle motor should be shut off when the file is not being accessed. This reduces media and drive motor wear.

Table 7. Customer Option Configurations

MX	HS	HM	DS1	DS2	DS3	DS4	NOTES
X	O	O	X	X	X	X	Invalid configuration. Head will not load and motor will not start.
O	O	S	S O O O	O S O O	O O S O	O O O S	• Read/write head is loaded and motor is turned on with a low level on Motor On. • Activity indicator activated (if In Use remains at a high level) and drive is selected by a low level on Drive Select.
O	S	O	S O O O	O S O O	O O S O	O O O S	• Read/write head is loaded, motor is turned on (if Motor On remains at a high level). • Activity indicator is activated (if In Use remains at a high level), and drive is selected by a low level on Drive Select.
S	O	S	S O O O	O S O O	O O S O	O O O S	• Drive is always selected. • Activity indicator is activated (if In Use remains at a high level) by a low level on Drive Select. • Heads load and motor is turned on with a low level on Motor On.
S	S	O	S O O O	O S O O	O O S O	O O O S	• Drive is always selected. • Read/write head is loaded, motor is turned on (if Motor On remains at a high level), and activity indicator is activated by a low level on Drive Select (if In Use line is held high).
X	S	S	X	X	X	X	Invalid configuration. Input current to Motor On and/or Drive Select may damage drivers on host.
S = SHORT				O = OPEN			X = DON'T CARE
The Door Open option is included on the 16-pin programmable shunt at pins 8 and 9. With DO open, the user enables a latch circuit which monitors and stores any door-disturbed status while the drive is not selected. This signal will be active when the drive is selected. Unless the door remains open, the latch is cleared when the Drive Select signal is removed.							

APPENDIX I: HARD DISK DRIVE MANUFACTURER'S MANUAL

Seagate Technology, Model ST 506/412

TABLE OF CONTENTS

Figures

Tables

1.0 Introduction

1.1 General Description:

The ST-506/412 disc drive is a random access storage device utilizing two non-removable 5¼ inch discs as storage media. Each disc surface employs one movable head to service 153/306 data tracks. The total formatted capacity of the four heads and surfaces is 5/10 megabytes (32 sectors per track, 256 bytes per sector, 612/1224 tracks).

Low cost and unit reliability are achieved through the use of a band actuator and open loop stepper head positioning mechanism. The inherent simplicity of mechanical construction and electronic controls allows maintenance free operation throughout the life of the drive. Both elecronic PCB's are mounted outside the head disc assembly, allowing field serviceability.

Mechanical and contamination protection for the heads, actuator, and discs is provided by an impact resistant aluminum enclosure. A self-contained recirculating system supplies clean air through a 0.3 micron filter. A second port in the filter assembly allows pressure equalization with ambient air without chance of contamination. A patented spindle pump assures adequate air flow and uniform temperature distribution throughout the head and disc area. Thermal isolation of the stepper and spindle motor assemblies from the disc enclosure results in a very low temperature rise within the enclosure. This provides significantly greater off track margin and the ability to immediately perform read and write operations after power up with no thermal stabilization delay.

The ST-506/412 electrical interface is similar to Shugart Associates' SA1000 family of 8 inch fixed disc drives. ST-506/412 *size* and *mounting* are identical to the industry standard minifloppy disc drives, and they use the same DC voltages and connector. No AC power is required.

Key Features:

- ★ Storage Capacity of 6.38/12.76 megabytes unformatted, 5.0/10.0 megabytes formatted as shipped.
- ★ Same physical size and mounting as the minifloppy.
- ★ Same DC voltages as the minifloppy.
- ★ Band actuator and stepper motor head positioning.
- ★ 5.0 megabit/second transfer rate.
- ★ Simple floppy-like interface.
- ★ Same track capacity as a double density 8 inch floppy.

1.2 Specification Summary:

1.2.1 Physical Specifications:

Environmental Limits:

Ambient Temperature
Operating: 40° to 122°F (4° to 50°C)
Non-Operating: —14° to 140°F (—10° to 60°C)

Max Temperature Gradient
Operating: 18°F/hr. (10°C)
Non-operating: Below Condensation

Relative Humidity: 8 to 80% non-condensing

Maximum Elevation
Operating: 10,000 ft.
Non-operating: —1000 to 12,000 ft.

Shock
Operating: 10G's
Non-operating: 40G's (on box side frames)

DC Power Requirements
+12V ±5%, 1.8A typical, 4.5A maximum (at power on)
+5V ±5%, .7A typical, 1.0A maximum
+12V/+5V Maximum Ripple = 50mV P-P

Mechanical Dimensions:

Height	3.25 inches
Width	5.75 inches
Depth	8.00 inches
Weight	4.6 lbs. (2.1 kg)
Shipping Weight	7.0 lbs. (3.2 kg)

Heat Dissipation
25 watts typical
29 watts maximum

1.2.2 Reliability Specifications:

MTBF	11,000 POH, typical usage
PM	Not Required
MTTR	30 minutes
Component Design Life	5 years

Error Rates:

Soft read errors	1 per 10^{10} bits read
Hard read errors*	1 per 10^{12} bits read
Seek errors	1 per 10^{6} seek

* Not recoverable within 16 retries

1.2.3 Performance Specifications:

	ST-506	ST-412
Capacity		
Unformatted		
Per Drive	6.38 Megabytes	12.76 Megabytes
Per Surface	1.59 Megabytes	3.19 Megabytes
Per Track	10416 Bytes	10416 Bytes
Formatted		
Per Drive	5.0 Megabytes	10.0 Megabytes
Per Surface	1.25 Megabytes	2.5 Megabytes
Per Track	8192 Bytes	8192 Bytes
Per Sector	256 Bytes	256 Bytes
Sectors Per Track	32	32
Transfer Rate	5.0 Mbits/sec	5.0Mbits/sec
Access Time		
Track to Track	3ms	3ms
Average*	85ms	85ms
Maximum*	205ms	205ms
Setting Time	15ms	15ms
Average Latency	8.33ms	

*using fast seek algorithm (including setting)

1.2.4 Functional Specifications:

Rotational speed	3600 rpm ±1%	3600 rpm ±1%
Recording density	7690 bpi max	9074 bpi max
Flux density	7690 fci	9074 fci
Track density	255 tpi	345 tpi
Cylinders	153	306
Tracks	612	1224
R/W Heads	4	4
Discs	2	2

2.0 Functional Characteristics

2.1 General Operation:

The ST-506/412 disc drive consists of read/write and control electronics, read/write heads, track positioning actuator, media, and air filtration system. The components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the desired track.
3. Read and write data.
4. Provide a contamination free environment.

2.2 Read/Write and Control Electronics

Electronics are packaged on two printed circuit boards. The primary board to which power, control and data signals are connected includes:

1. Index detection circuit.
2. Head position/actuator circuit.
3. Read/write circuits.
4. Drive up to speed circuit.
5. Head select circuit.
6. Write fault detection circuit.
7. Step motor drive circuit.
8. Drive select circuit.
9. Track zero detector circuit.

The second PCB, mounted to the sideframe under the primary board derives its power from the primary board and provides power and speed control to the spindle drive motor.

2.3 Drive Mechanism

A brushless DC drive motor rotates the spindle at 3600 rpm. The spindle is driven directly with no belt or pulley being used. The motor is thermally isolated from the head/disc assembly to minimize temperature rise in the sealed chamber containing the heads and discs. The motor and spindle are dynamically balanced to insure a low vibration level. A brake is used to quickly stop the spindle motor when power is removed. The head/disc assembly is shock mounted to minimize transmission of vibration through the chassis or frame.

2.4 Air Filtration System (Figures 1A & 1B)

The discs and read/write heads are fully enclosed in a module using an integral recirculation air system and absolute filter to maintain a clean environment. Integral to the filter is a port which also permits ambient pressure equalization without contaminate entry.

2.5 Positioning Mechanism (Figure 2)

The read/write heads are mounted on a ball bearing supported carriage which is positioned by a band actuator connected to the stepper motor shaft. The stepper motor is thermally isolated from the head/disc assembly to minimize temperature rise in the sealed chamber.

FIGURE 1A

AIR FILTRATION SYSTEM

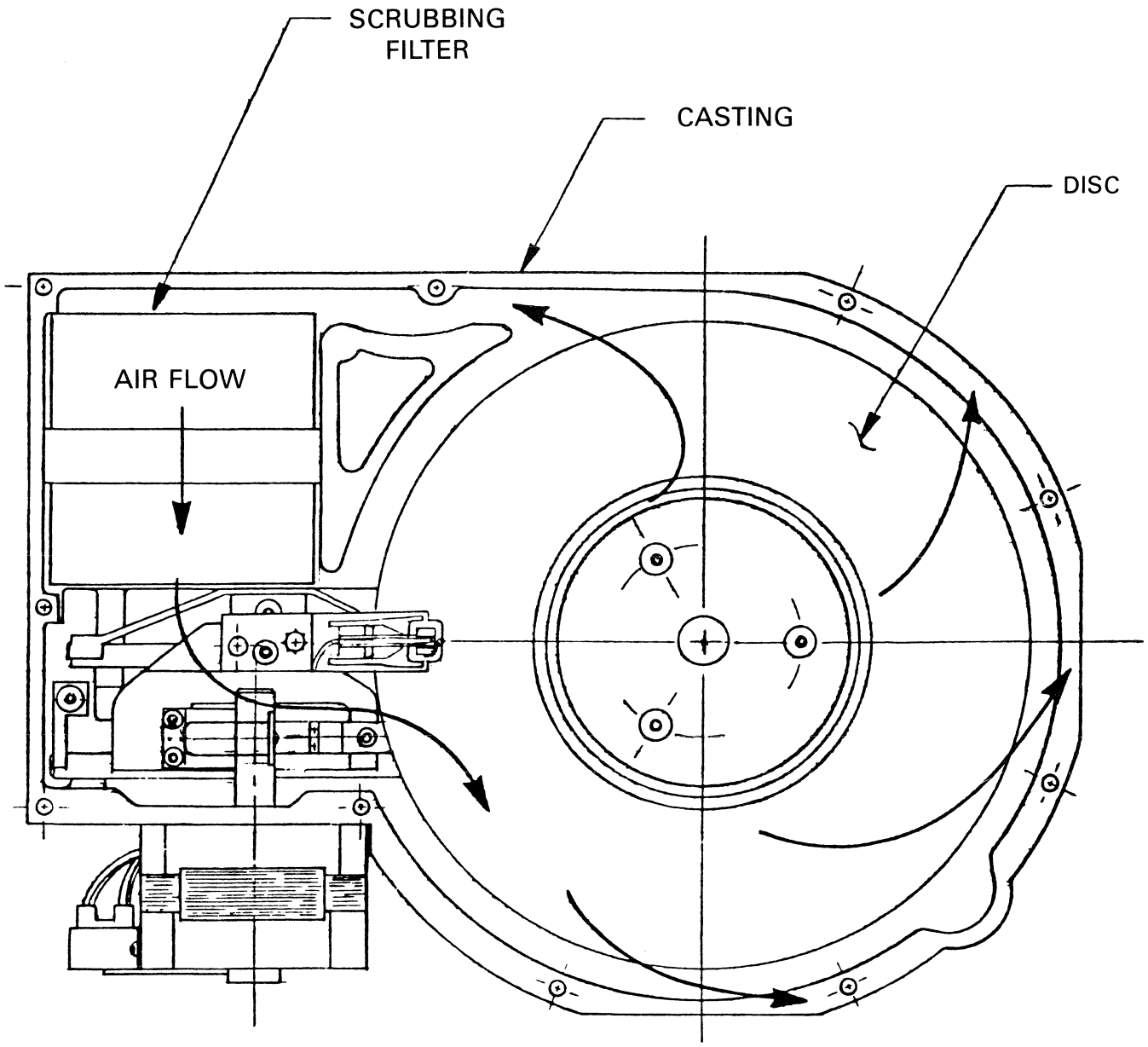


FIGURE 1B

AIR FILTRATION SYSTEM

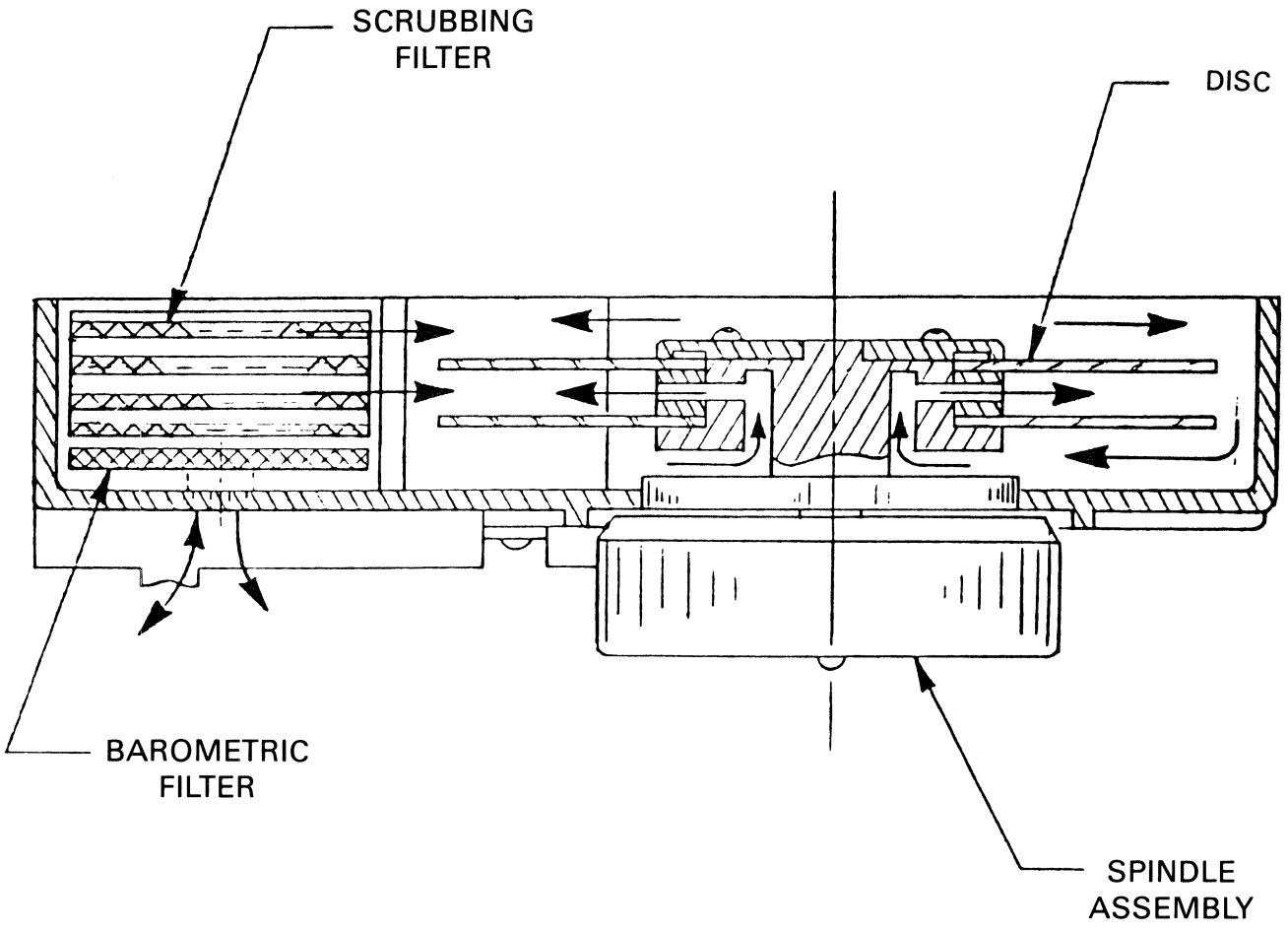
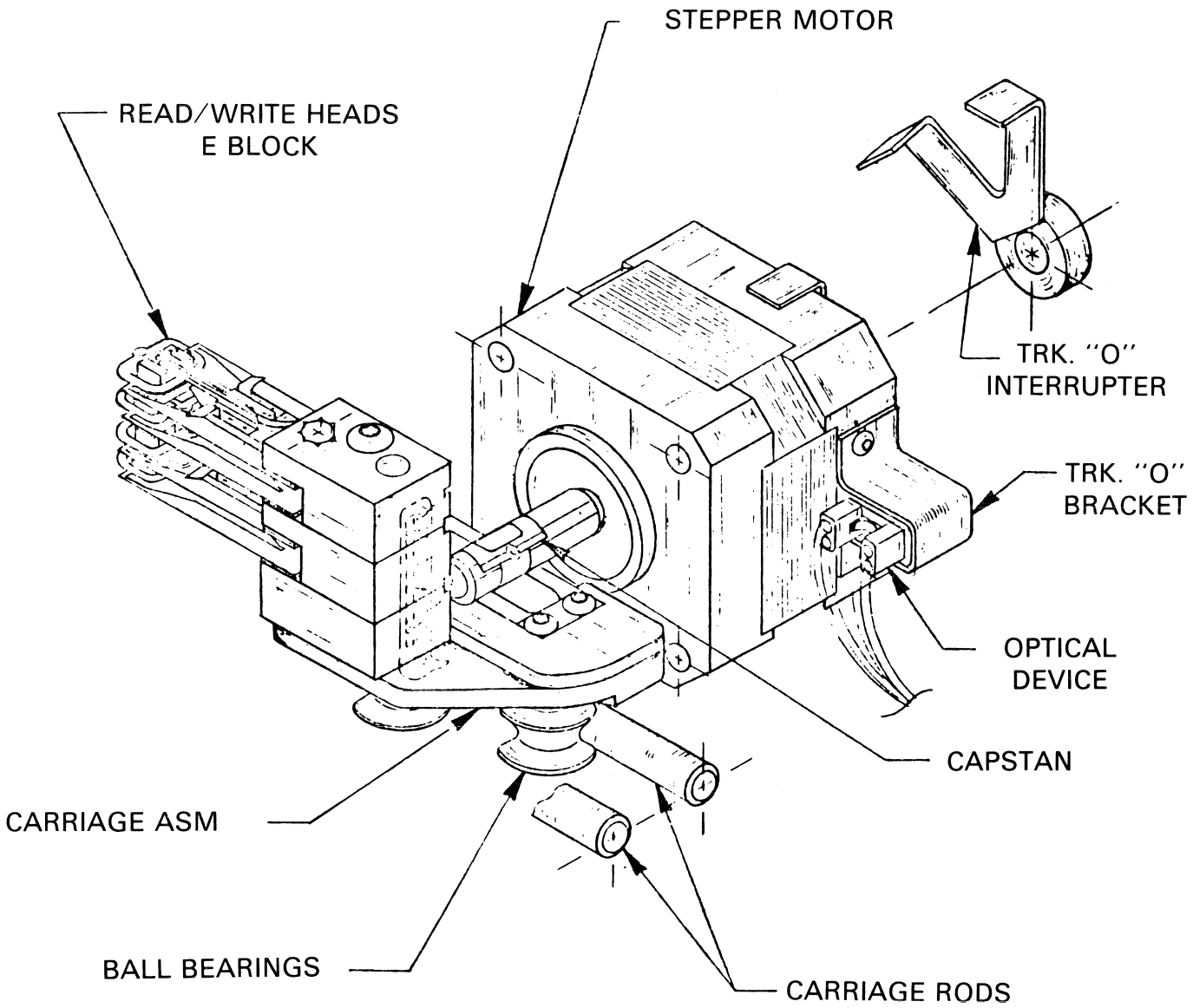


FIGURE 2

POSITIONING MECHANISM



2.6 Read/Write Heads and Discs

The recording media consists of a lubricated thin magnetic oxide coating on a 130 mm diameter aluminum substrate. This coating formulation, together with the low load force/low mass flying heads, permits reliable contact start/stop operation.

Data on each of the four disc surfaces is read by one read/write head, each of which accesses 153/306 tracks.

3.0 Functional Operations

3.1 Power Sequencing (Figure 3)

Plus 5 and +12 volts may be applied in any order; however, +12 volts must be applied to start the spindle drive motor. A speed sense circuit counts 512 disc revolutions before recalibrating the heads to track 0 (See section 4.5.2 for exception). For this recalibration to occur, the step input signal must be inactive. TRACK Ø, SEEK COMPLETE and READY signals on the interface will become true sequentially. The drive will not perform read, write or seek functions until READY becomes true.

3.2 Drive Selection

Drive selection occurs when one of the DRIVE SELECT lines is activated. Only the selected drive will respond to the input signals, and only that drive's output signals are then gated to the controller interface (See section 4.5.1 for exception).

3.3 Track Accessing

Read/write head positioning is accomplished by:

a) Deactivating Write Gate.

b) Activating the appropriate Drive Select line.

c) Being in the READY condition with SEEK COMPLETE true.

d) Selecting the appropriate direction.

e) Pulsing the Step line.

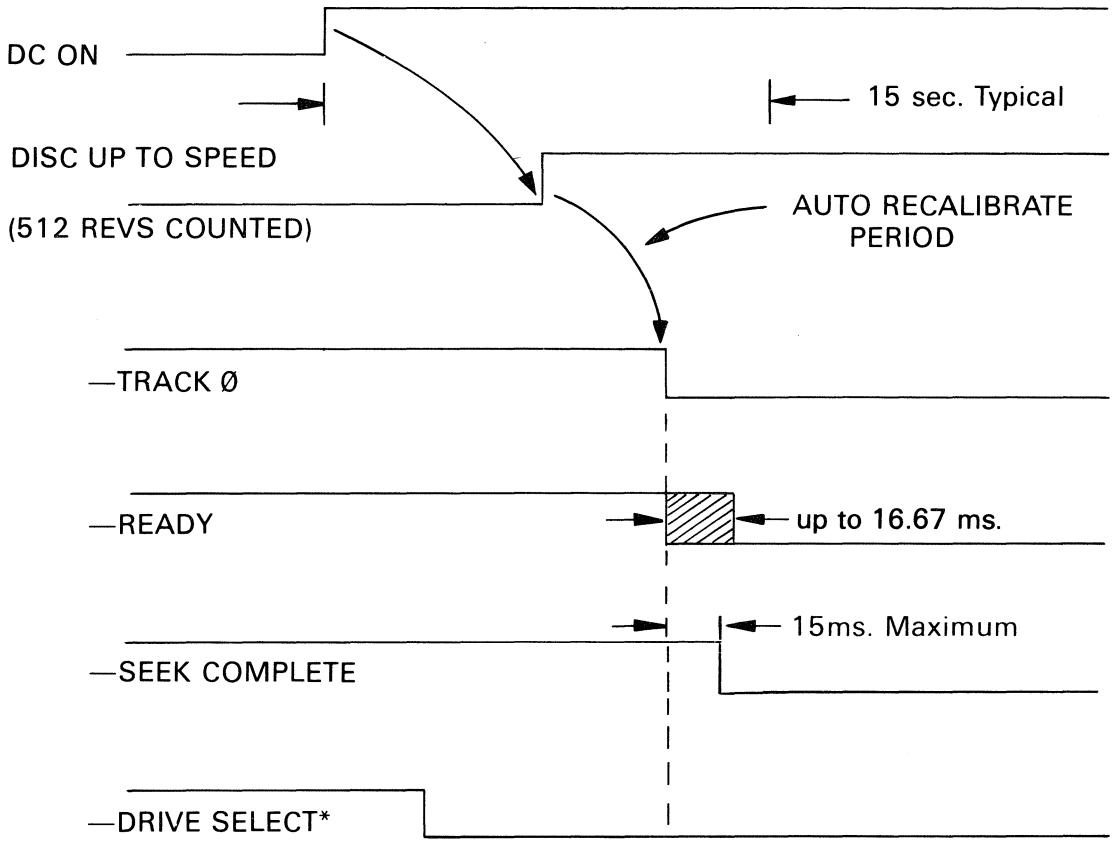
Each step pulse will cause the heads to move either 1 track in or 1 track out depending on the level of the Direction line. A low level on the Direction line will cause a seek inward toward the spindle; a high, outward toward track Ø.

3.4 Head Selection

Any of the 4 heads can be selected by placing the head's binary address on the two Head Select lines.

FIGURE 3

POWER UP SEQUENCE



(*GATES READY, TK Ø, SEEK COMPLETE)

3.5 Read Operation

Reading data from the disc is accomplished by:

a) Deactivating the Write Gate line.

b) Activating the appropriate Drive Select line.

c) Assuring the drive is Ready.

d) Selecting the appropriate head.

3.6 Write Operation

Writing data onto the disc is accomplished by:

a) Activating the appropriate Drive Select line.

b) Assuring that the drive is Ready.

c) Selecting the proper head.

d) Insuring no Write Fault conditions exist.

e) Activating Write Gate and placing data on the Write Data line.

4.0 Electrical Interface

The interface to the ST-506/412 can be divided into three catagories, each of which is physically separated.

1. Control signals.
2. Data signals.
3. DC power.

All control lines are digital in nature (open collector TTL) and either provide signals to the drive (input) or signals to the host (output) via interface connection J1/P1. The data transfer signals are differential in nature and provide data either to (write) or from (read) the drive via J2/P2 (Defined by EIA RS-422).

Table I through III and Figures 4 through 6 show connector pin assignments and interconnection of cabling between the host controller and drives.

TABLE I

J1/P1—CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	—REDUCED WRITE CURRENT
3	4	RESERVED (Head 2^2 in future products)
5	6	—WRITE GATE
7	8	—SEEK COMPLETE
9	10	—TRACK Ø
11	12	—WRITE FAULT
13	14	—HEAD SELECT 2^0
15	16	RESERVED (TO J2 PIN 7)
17	18	—HEAD SELECT 21
19	20	—INDEX
21	22	—READY
23	24	—STEP
25	26	—DRIVE SELECT 1
27	28	—DRIVE SELECT 2
29	30	—DRIVE SELECT 3
31	32	—DRIVE SELECT 4
33	34	—DIRECTION IN

TABLE II

J2/P2—CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	— DRIVE SELECTED
4	3	RESERVED
6	5	RESERVED
8	7	RESERVED (TO J1 PIN 16)
	9, 10	RESERVED
12	11	GND
	13	+ MFM WRITE DATA
	14	— MFM WRITE DATA
16	15	GND
	17	+ MFM READ DATA
	18	— MFM READ DATA
20	19	GND

TABLE III

J3/P3—DC CONNECTOR PIN ASSIGNMENTS

VOLTAGE		GROUND	
PIN 1	+12 VOLTS DC	PIN 2	+12 VOLT RETURN
PIN 4	+5 VOLTS DC	PIN 3	+5 VOLT RETURN

FIGURE 4

CONTROL SIGNALS

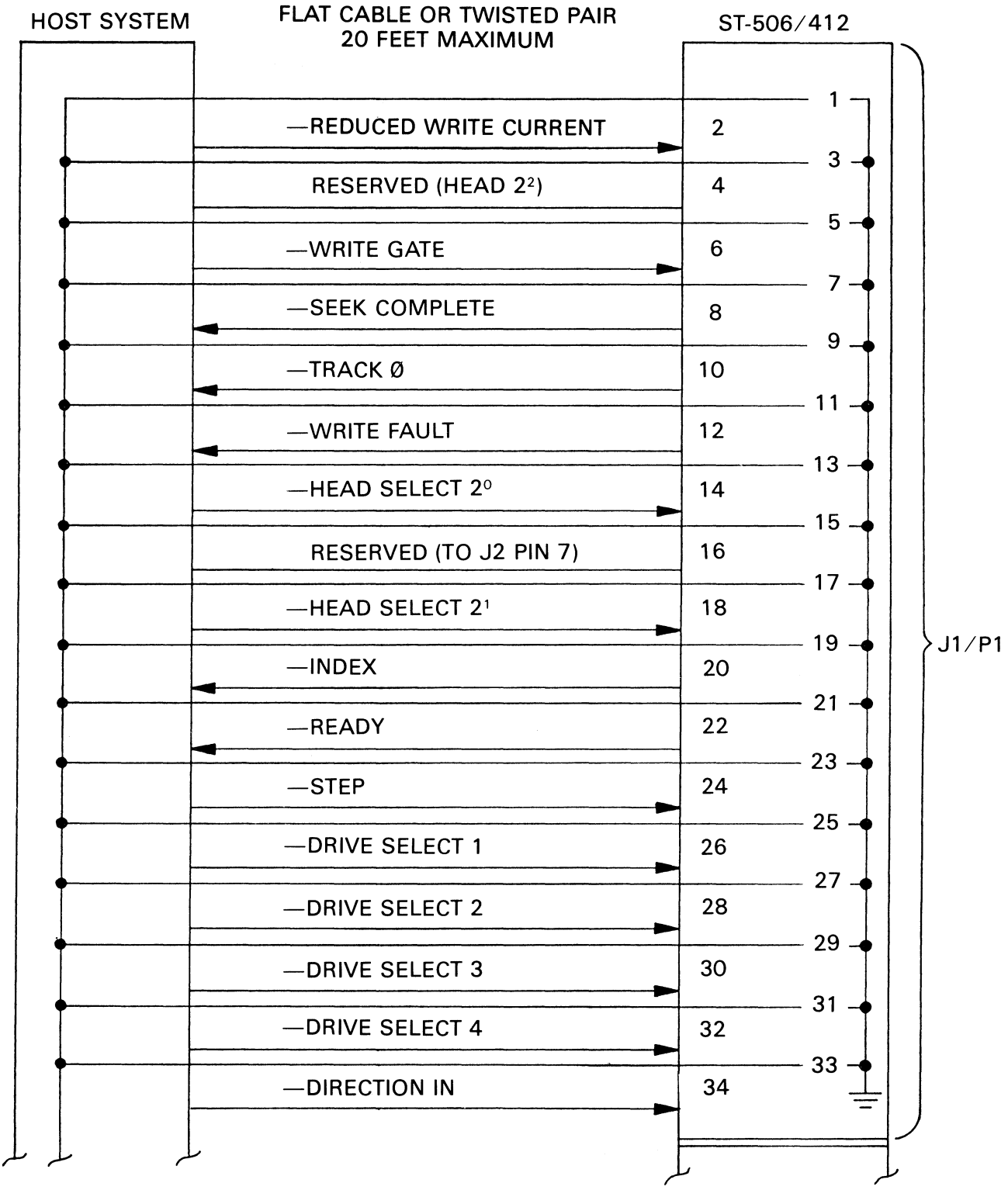


FIGURE 5

DATA SIGNALS

FLAT CABLE OR TWISTED PAIR
20 FEET MAXIMUM

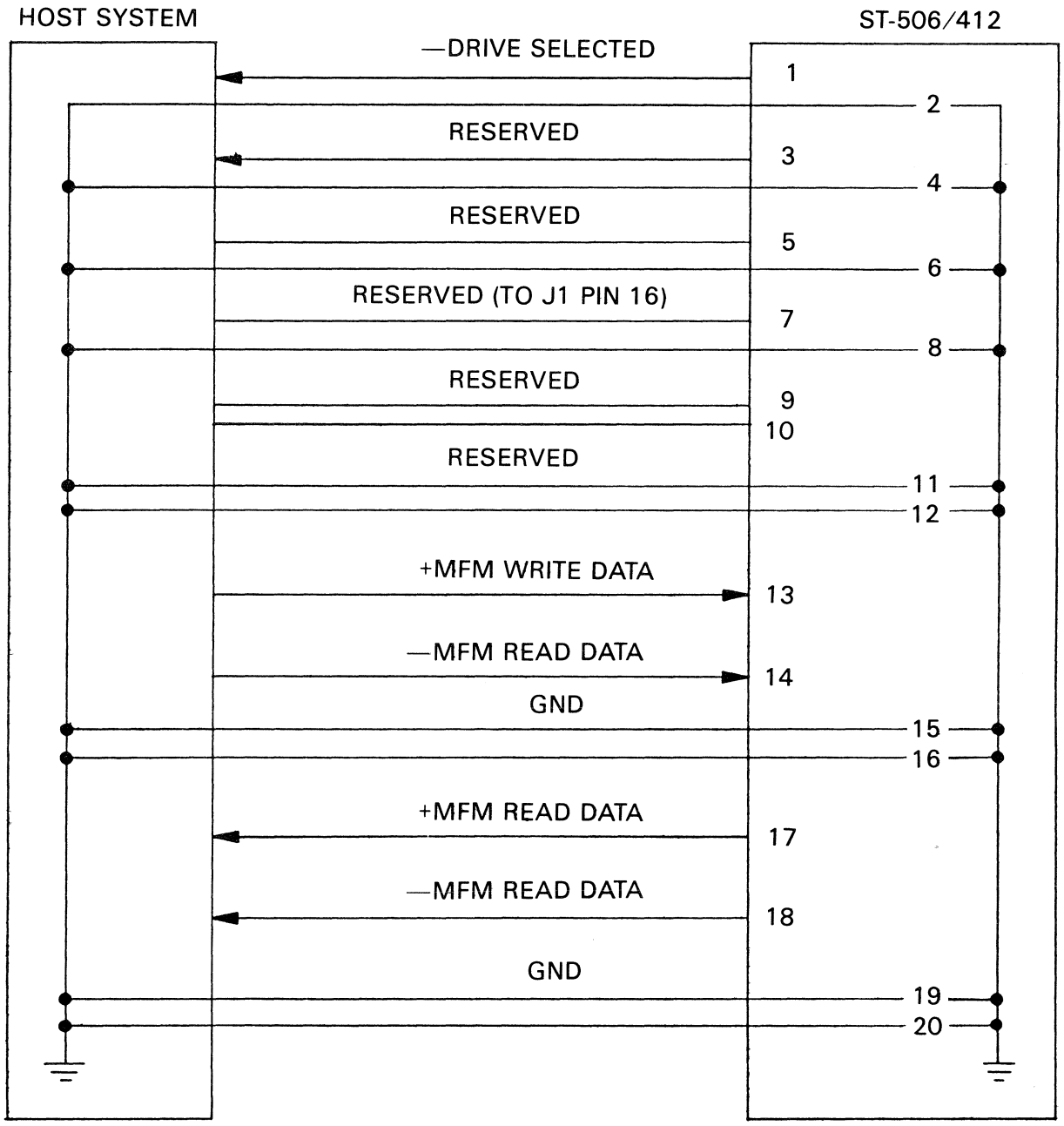
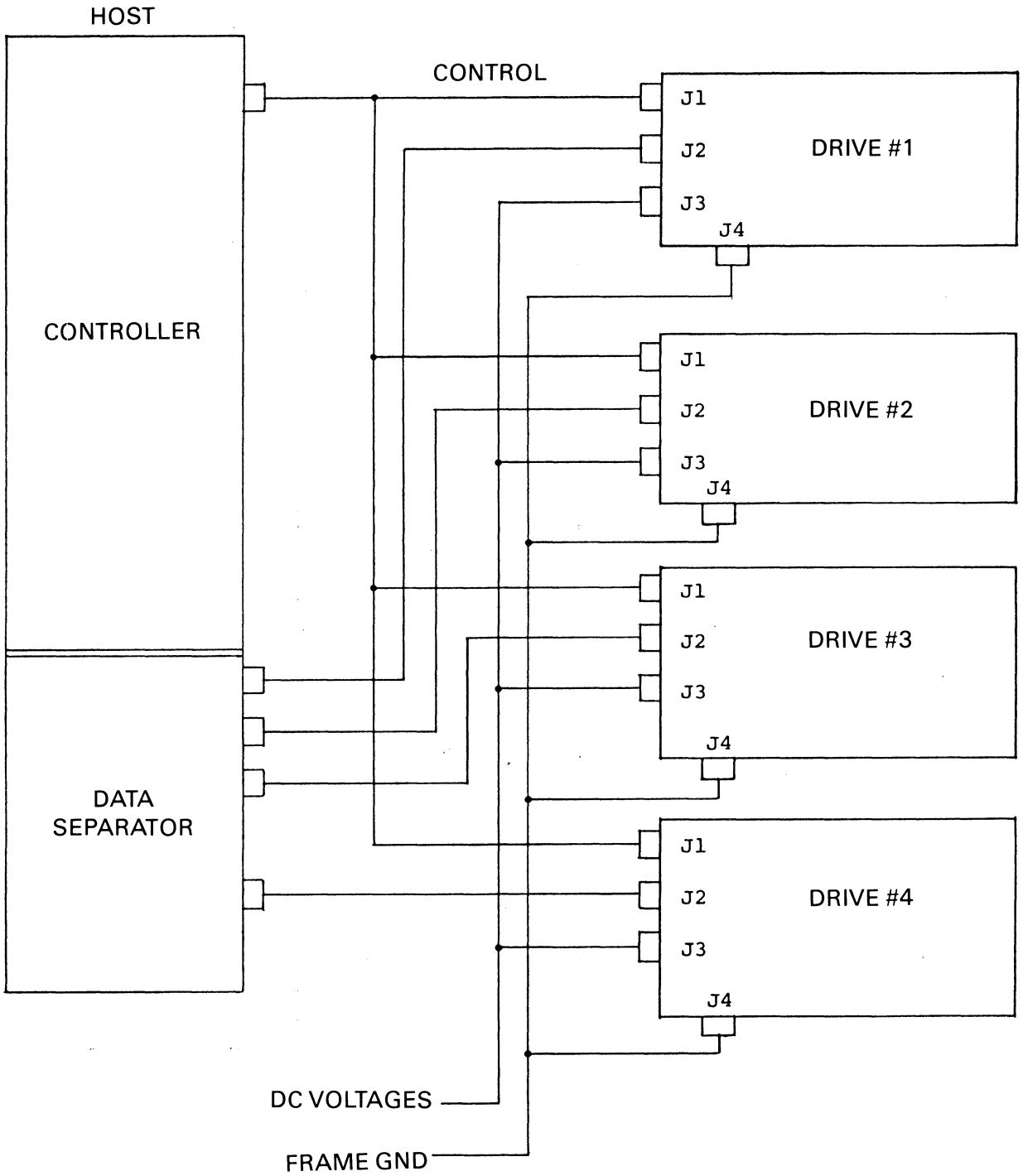


FIGURE 6
TYPICAL CONNECTION, 4 DRIVE SYSTEM



4.1 Control Input Lines

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are REDUCED WRITE CURRENT, WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, STEP and DIRECTION IN. The signal to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3 or DRIVE SELECT 4.

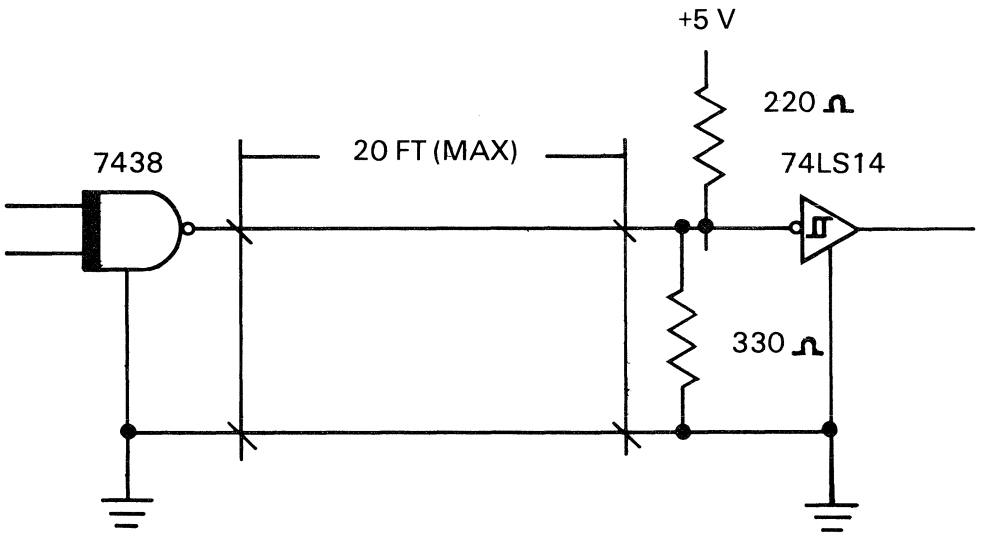
The input lines have the following electrical specifications. Refer to Figure 7 for the recommended circuit.

TRUE: 0.0VDC to 0.4VDC @ I = —40 mA (MAX)

FALSE: 2.5VDC to 5.25VDC @ 1=+250 uA (OPEN COLLECTION)

FIGURE 7

CONTROL SIGNALS DRIVER/RECEIVER COMBINATION



4.1. Reduced Write Current (Not used on 412)

This line, when active together with WRITE GATE, causes the write circuitry to write on the disc with a lower write current. It is required that this line to be set true when writing is to be performed on cylinders 128 /NA* through 152, and set false when writing is to be performed on cylinders 0 through 127/NA*.

A 220/330 ohm resistor pack allows for line termination.

4.1.2 Write Gate

The active state of this signal, or low level, enables write data to be written on the disc. The inactive state of this signal, or high level, enables data to be transferred from the drive.

A 220/330 ohm resistor pack allows for line termination.

4.1.3 Head Select 2^0 and 2^1

These two lines allow selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant line. Heads are numbered Ø through 3. When both HEAD SELECT lines are high (inactive), head 0will be selected.

A 220/330 ohm resistor pack allows for line termination.

4.1.4 Direction In

This signal defines direction of motion of the R/W head when the STEP line is pulsed. An open circuit or high level defines the direction as "out" and if a pulse is applied to the STEP line, the R/W heads will move away from the center of the disc. If this line is a low level, the direction of motion is defined as "in" and the R/W heads will move toward the center of the disc. Change in direction must meet the requirement shown in Figure 8.

A 220/330 ohm resistor pack allows for line termination.

Note: Direction must not change during step time.

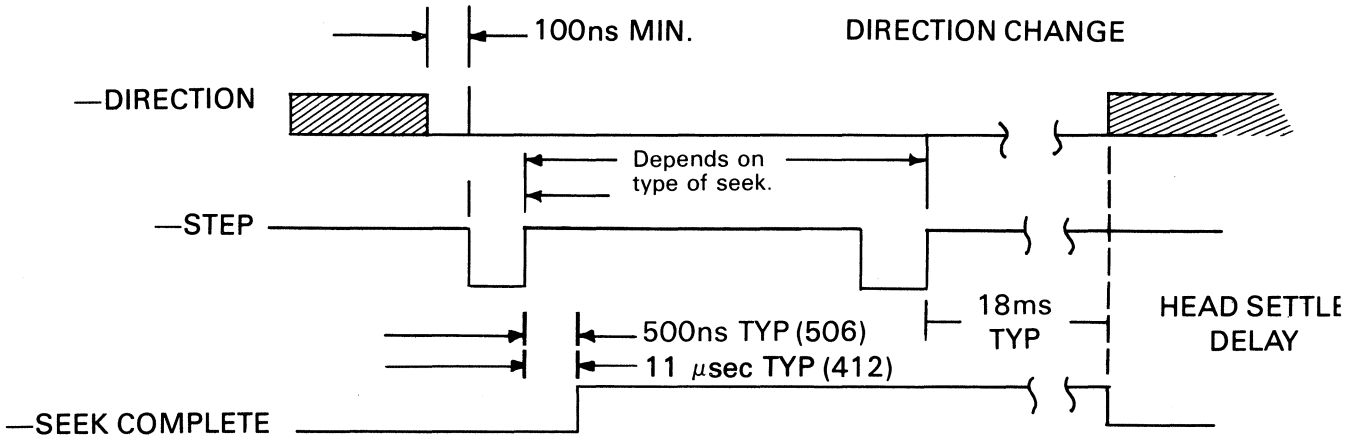
4.1.5 Step

This interface line is a control signal which causes the R/W head to move in the direction of motion defined by the DIRECTION IN line.

The access motion is intiatied at the low to high level transition or trailing edge of the signal pulse. Any change in the DIRECTION line must be made at least 100ns before the leading edge of the step pulse (refer Figure 8A for general timing requirements).

A 220/330 resistor pack allows for line termination.

FIGURE 8A
SEEK TIMING GENERAL

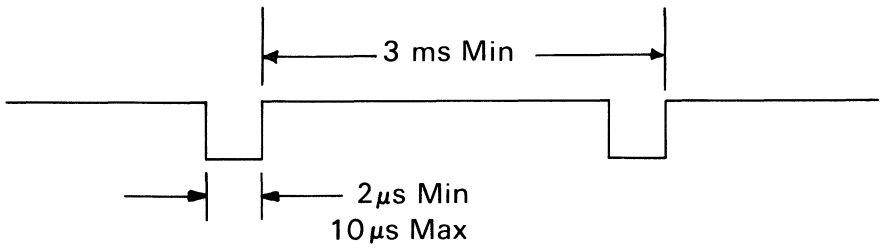


*Change in direction can not be made prior to seek complete.

Slow Seek (506 and 412)

The R/W head will move at the rate of the incoming step pulses. The minimum time between successive steps is 3.0ms. The minimum pulse width is 2.0 usec. See Figures 8A and 8B for step timing.

FIGURE 8B
SLOW SEEK STEP PULSE TIMING

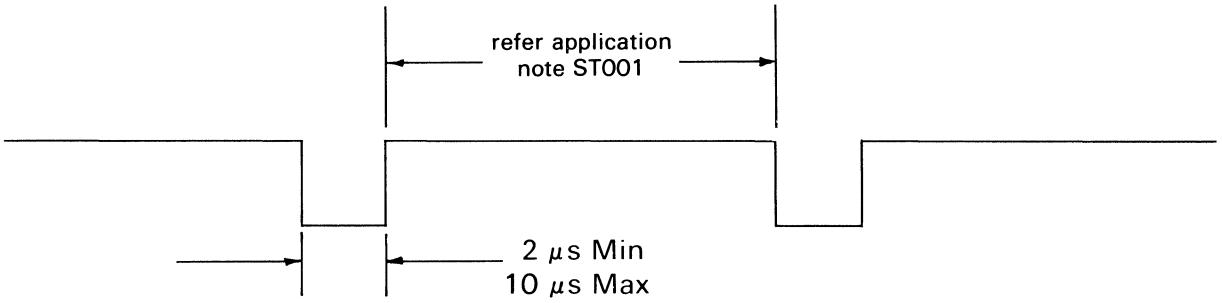


Algorithm Driven Seek (Not supported on 412)

In order to better utilize the stepper motor's speed characteristics, the controller can issue step pulses at a rate faster than 3ms. This algorithm accelerates the motor to its maximum speed, steps it slightly less than the desired distance, and then decelerates it prior to arriving on the specified track. Employing this algorithm allows access time to be reduced considerably while maintaining a 15ms setting time. For more information consult Seagate Application Note ST001.

FIGURE 8C

ALGORITHM DRIVEN SEEK

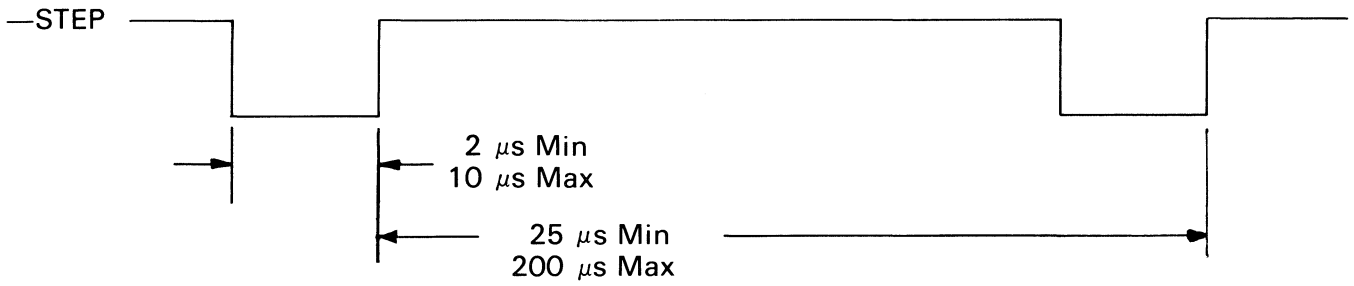


Buffered Seek (ST-412only)

Microprocessor utilization on the ST412 adds the capability of capturing and storing up to 305 step pulses. The controller may burst pulses to the 512 and they will be accepted until 1) time after last pulse exceeds 200 usec or 2) 305 step pulses are received. At the occurrence of either of these conditions, the ST412 microprocessor will stop accepting step pulses from the controller and will begin issuing them to the stepper motor. Depending on the length of seek, the microprocessor will select the optimum algorithm. Any pulses issued at a rate between 200 usec and 3 msec may be lost (refer Figures 8A & 8D).

FIGURE 8D

BUFFERED SEEK



4.1.6 DRIVE SELECT 1—4 (Figure 13)

DRIVE SELECT, when a low level, connects the drive interface to the control lines. Cutting the appropriate shunts at IC position 6B (6E on 412) will determine which select line on the interface will activate that drive. The following table indicates which DRIVE SELECT shunts must be cut.

DRIVE SELECT	CUT SHUNTS
DS 1	10-7, 11-6, and 12-5
DS 2	9-8, 11-6, and 12-5
DS 3	9-8, 10-7, and 12-5
DS 4	9-8, 10-7, and 11-6

4.2 CONTROL OUTPUT LINES

The output control signals are driven with an open collector ouput stage capable of sinking a maximum of 48mA at low level or true state with maximum voltage of 0.4V measured at the driver. When the line driver is in the high level or false state, the driver transistor is off and the collector leakage current is a maximum of 250uA.

All J1 ouput lines are enabled by their respective DRIVE SELECT line.

Figure 7 shows the recommended circuit.

4.2.1 SEEK COMPLETE

This line will go to a low level or true state when the R/W heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when seek complete is false.

SEEK COMPLETE will go false in three cases:

1) A recalibration sequence is initiated (by drive logic), at power on, if the R/W heads are not over track zero.

2) 500ns (typical) after the leading edge of a step pulse or series of step pulses.

3) If +5 volts or +12 volts are lost momentarily but restored.

4.2.2 TRACK Ø

This interface signal indicates a low level or true state only when the drive's R/W heads are positioned at cylinder zero (the outermost data track).

4.2.3 WRITE FAULT

This signal is used to indicate a condition exists at the drive that may cause improper writing on the disc. When this line is a low level or true, further writing and stepping is inhibited at the drive until the condition is corrected. Write fault cannot be reset via the interface.

Note: controller should edge detect this signal.

There are three conditions detected:

a) Write current in a head without WRITE GATE active or no write current with WRITE GATE active and DRIVE SELECTED.

b) Multiple heads selected, no head selected, or improperly selected.

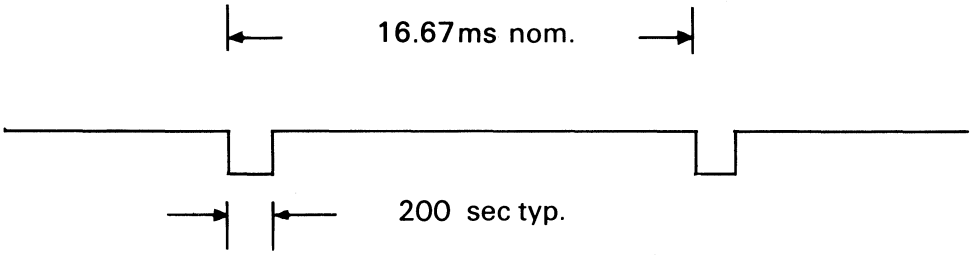
c) DC voltages are grossly out of tolerance.

4.2.4 INDEX (Figure 9)

This interface signal is provided by the drive once each revolution (16.67ms nom.) to indicate the beginning of a track. Normally, this signal is a high level and makes the transition to a low level to indicate INDEX. Only the transition from high to low is valid.

FIGURE 9

INDEX TIMING



4.2.5 READY

This interface signal when true together with SEEK COMPLETE, indicates that the drive is ready to read, write or seek, and that the I/O signals are valid. When this line is false, all writing and seeking is inhibited.

The typical time after power on for READY to be true is 15 seconds.

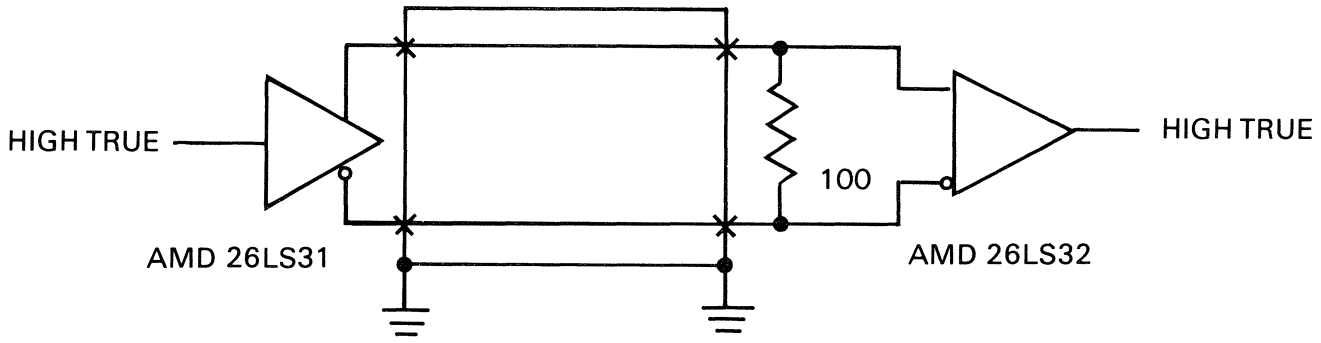
4.3 DATA TRANSFER LINES

All lines associated with the transfer of data between the drive and the host system are differential in nature and may not be multiplexed. These lines are provided at the J2/P2 connectors on all drives.

Two pair of balanced signals are used for the transfer of data: WRITE DATA and READ DATA. Figure 10 illustrates the driver/receiver combination used in the drive for data transfer signals.

FIGURE 10

DATA LINE DRIVER/RECEIVER COMBINATION



Z =105

FLAT RIBBON OR TWISTED PAIR
MAXIMUM 20 FEET

NOTE: ANY EIA RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE.

4.3.1 MFM WRITE DATA

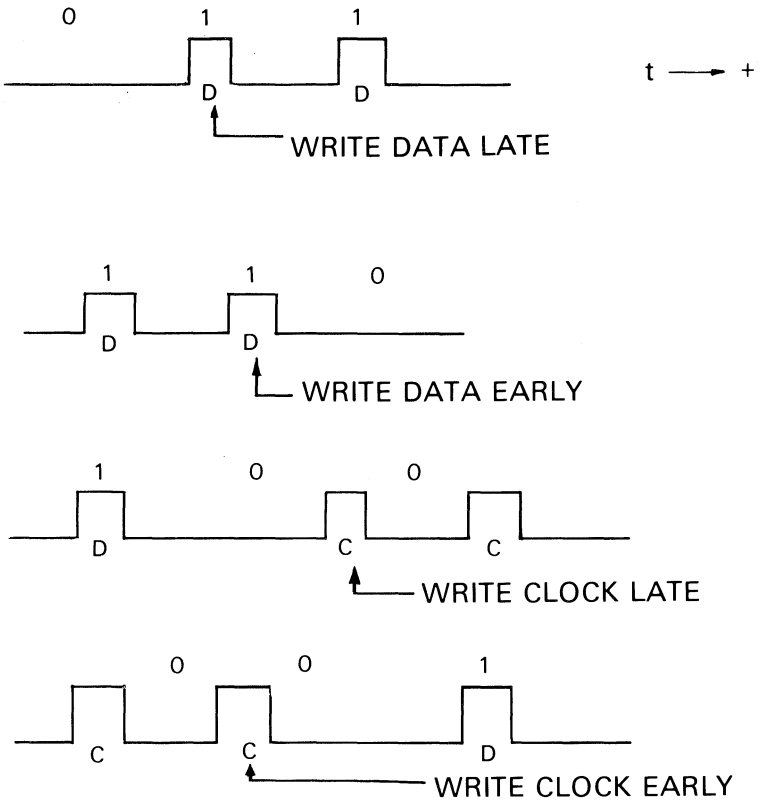
This is a differential pair that defines the transitions to be written on the track. The transition of +MFM WRITE DATA line going more positive than the —MFM WRITE DATA will cause a flux reversal on the track provided WRITE GATE is active. This signal must be driven to an inactive state (+MFM WRITE DATA more negative than —MFM WRITE DATA) by the host system when in a read mode.

To insure data integrity at the error rate specified when using an ST506, the write data presented by the host must be pre-compensated on tracks 128/128* through 152/306.

The optimum amount of pre-compensation is 12ns for both early and late written bits. Figure 11 shows the bit patterns to be compensated. All other patterns are written "on time."

FIGURE 11

WRITE PRECOMPENSATION PATTERNS



Writing should occur out of a shift register which is used to observe the pattern. "On time" represents a nominal delay. Early and late represent less and more delay respectively.

4.3.2 MFM READ DATA

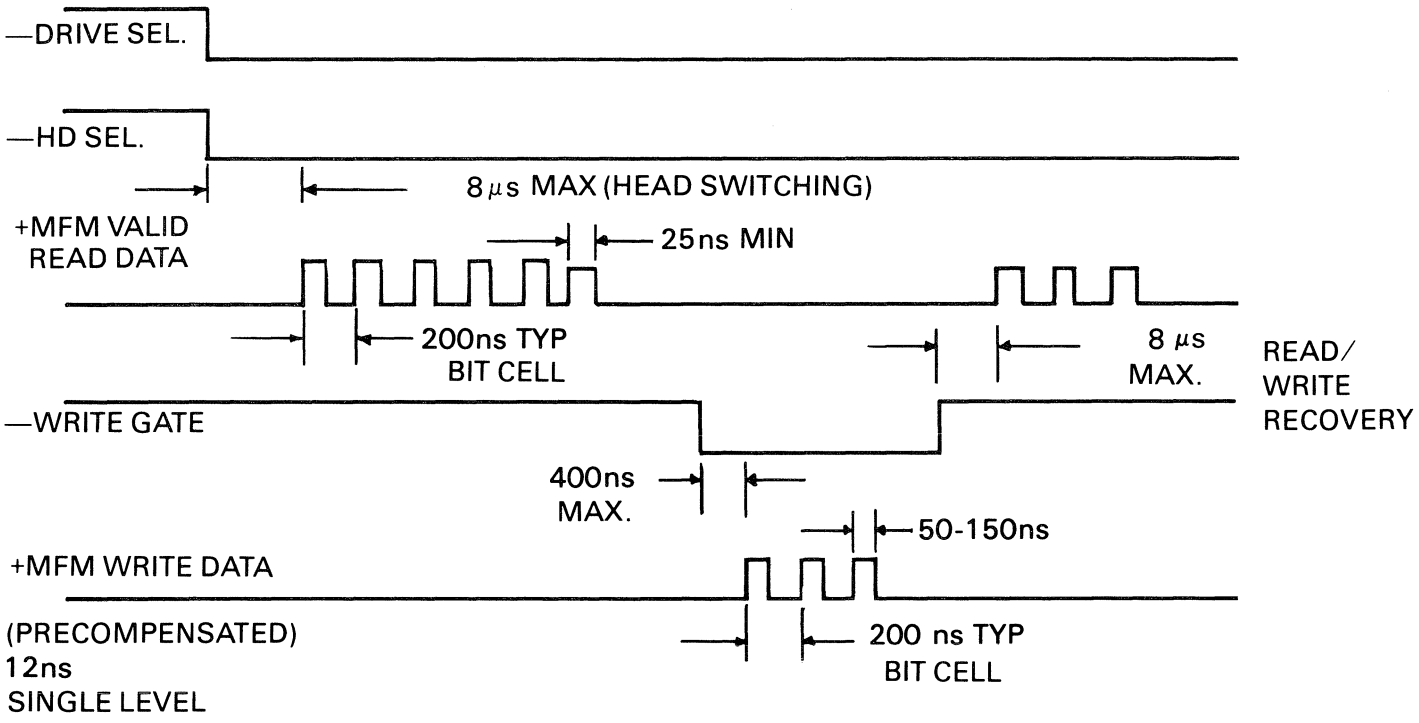
The data recovered by reading a pre-recorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM READ DATA line going more positive than the —MFM READ DATA line represents a flux reversal on the track of the selected head.

4.3.3 READ/WRITE TIMING

The timing diagram as shown in Figure 12 depicts the necessary sequence of events (with associated timing restrictions) for proper read/write operation of the drive.

FIGURE 12

READ/WRITE DATA TIMINGS



4.4 DRIVE SELECTED

A status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED line is driven by a TTL open collector driver as shown in Figure 7. This signal will go active only when the drive is programmed as drive x (x= 1,2,3, or 4) by cutting the shunt on the drive. The DRIVE SELECT X line at J1/P1 is activated by the host system.

4.5 CUSTOMER OPTIONS (Figure 13)

Three optional features which are implemented via a shunt block at IC position 6B (6E on the 412) on the main printed circuit board are available for customer reconfiguration of the drive functions.

4.5.1 "R" (Radial) Option

As shipped, the 14 pin shunt block (16 pin socket) is plugged in pins 2-15, leaving pins 1 and 16 open. This results in a daisy chain operation. Outputs are not active until the drive is selected. Moving the shunt block one position, to use pins 1 and 16, results in radial operation. In this case, all output signals are active, even if the drive is not selected. However, in this case, the front panel LED will not be on. Drive Select must be active to light the LED.

4.5.2 "D" (Defeat Recal) Operation

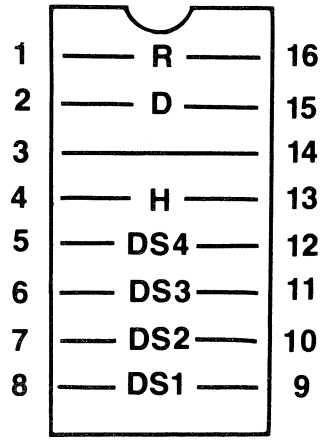
As shipped, the "D" shunt, pins 2-15, is shorted. In this case, whenever a power up sequence is performed, the heads will automatically be repositioned to track Ø. Cutting the shunt D will defeat the automatic recal operation, allowing the drive to become "Ready" earlier. However, during power up, the stepper circuitry will always put phase "A" active. Thus, there is no guarantee that the drive heads will be positioned at the same cylinder as existed when the drive was powered down. It will start at the same track only if the track corresponded to one which utilizes phase A. When using this option, issuing a Read ID command would allow determination of the active address, and could be used to initialize a present track address register.

4.5.3 "H" (Half Step) Option

As shipped, the "H" shunt, pins 4-13, is shorted. In this case step pulses are applied to the interface at an interval of 3 milliseconds as shown in Figure 8A. Cutting shunt "H" allows a significant decrease in access time when used in conjunction with a simple software algorithm supplied by the user (refer Figure 8C). For detailed implementation information, contact the factory for a copy of Application Note ST-ØØ1 (ST Part Number 36001-001).

FIGURE 13

OPTION SHUNT BLOCK



DS1, DS2, DS3, DS4 = Drive Selected

H = Half Step Option

D = Defeat Auto Recal

R = Radial Connection

Note: Jumper shorted is active condition for DS1, DS2, DS3, DS4, and R.
Jumper open is active condition for H and D.

5.0 Physical Interface:

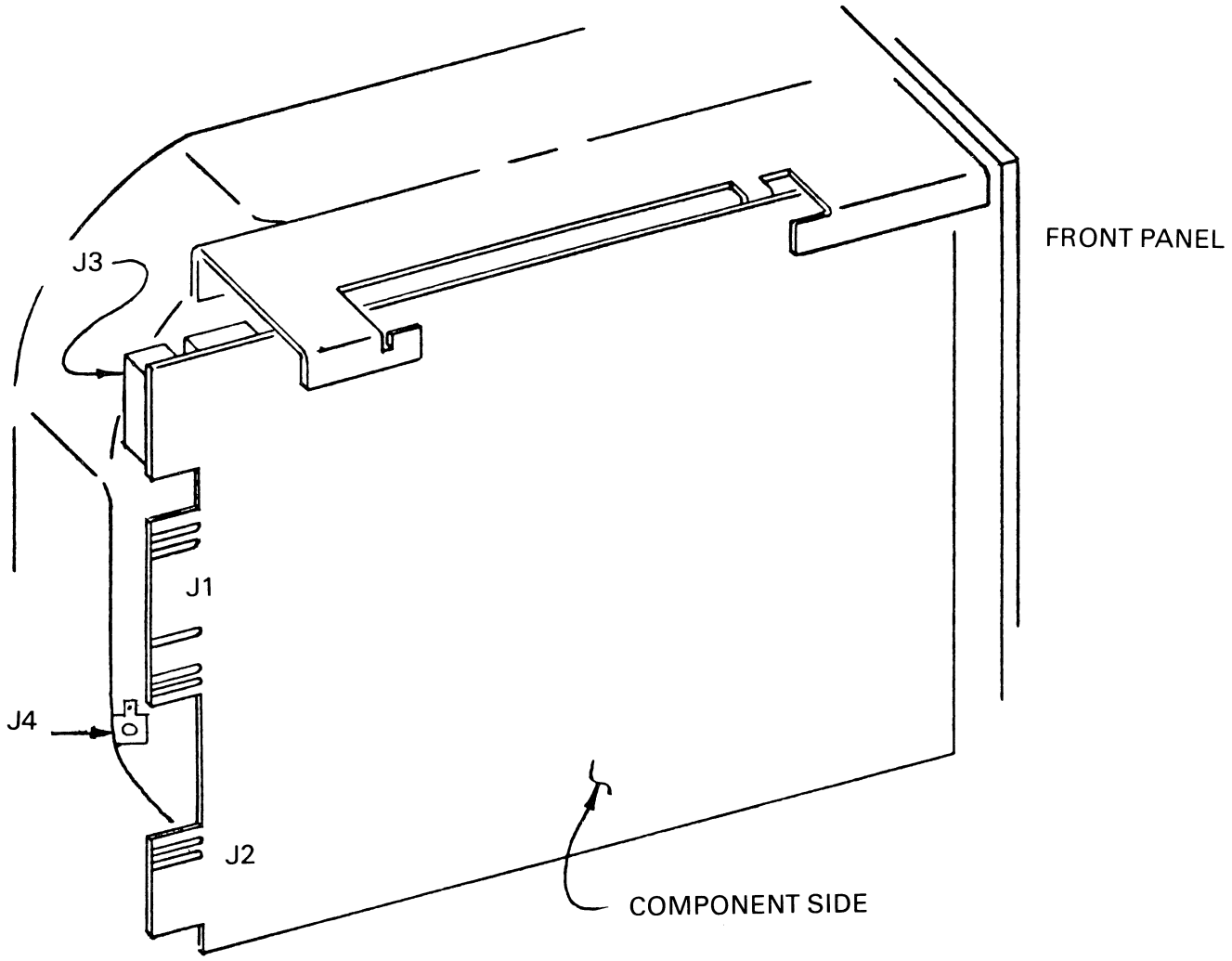
The electrical interface between the ST506/412. and the host controller is via four connectors:

1. J1 - Control signals (multiplexed)
2. J2 - Read/write signals (radial)
3. J3 - DC power input
4. J4 - Frame ground

Refer to Figure 14 for connector locations.

FIGURE 14

INTERFACE CONNECTOR PHYSICAL LOCATIONS



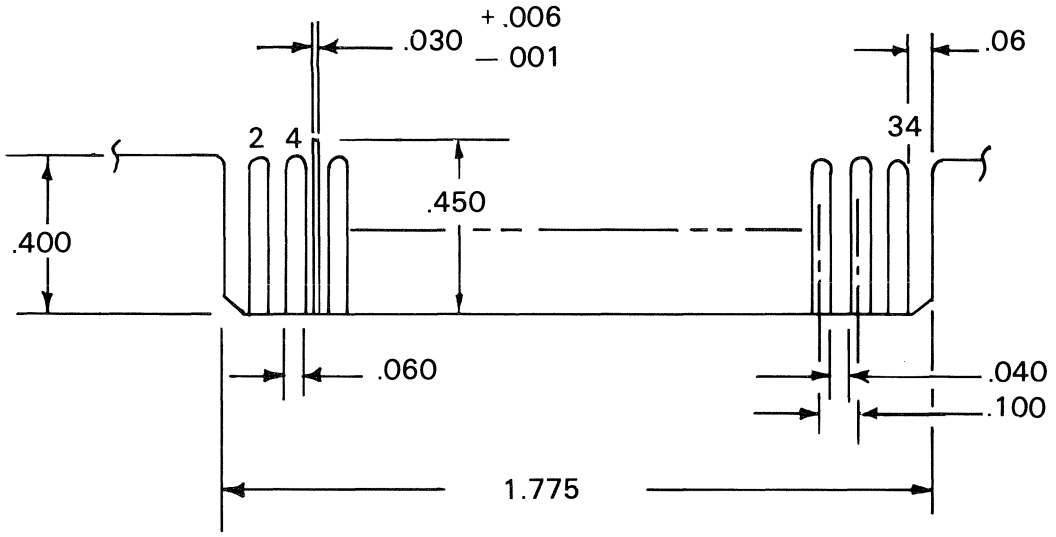
5.1 J1/P1 Connector—Control Signals

Connection of J1 is through a 34 pin edge connector. The dimensions for this connector are shown in Figure 15. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the DC Power connector J3/P3 and is labelled. The recommended mating connector for P1 is AMP ribbon connector P/N88373-3 or Molex 15-35-1341. All odd pins are ground.

A key slot is provided between pins 4 and 6.

FIGURE 15

J1 CONNECTOR DIMENSIONS



Unless noted, .xx = ±.030, .xxx = ±.010

BOARD THICKNESS
.062 + .007

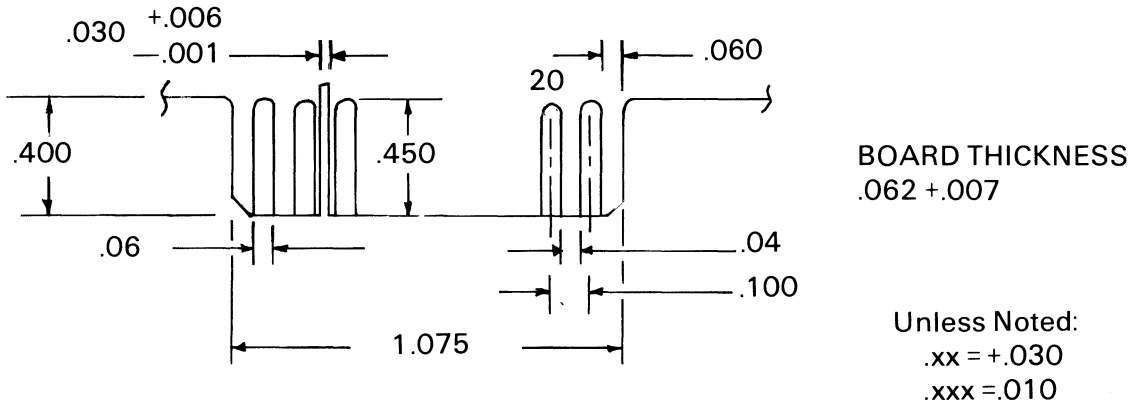
5.2 J2/P2 Connector—Data Signal

Connection to J2 is through a 20 pin edge connector. The dimensions for the connector are shown in Figure 16. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6, or Molex P/N 15-35-1201.

A key slot is provided between pins 4 and 6.

FIGURE 16

J2 CONNECTOR DIMENSIONS

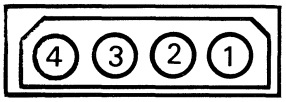


5.3 J3/P3 Connector—DC Power

DC power connector (J3) is a 4 pin AMP Mate-N-Lok connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-408424-0 utilizing AMP pins P/N 350078-4 (Strip) or P/N 61173-4 (Loose Piece). J3 pins are numbered as shown in Figure 17.

FIGURE 17

J3 CONNECTOR—DRIVE PCB SOLDER SIDE



Current requirements and connector pin numbers are shown in Table IV.

TABLE IV

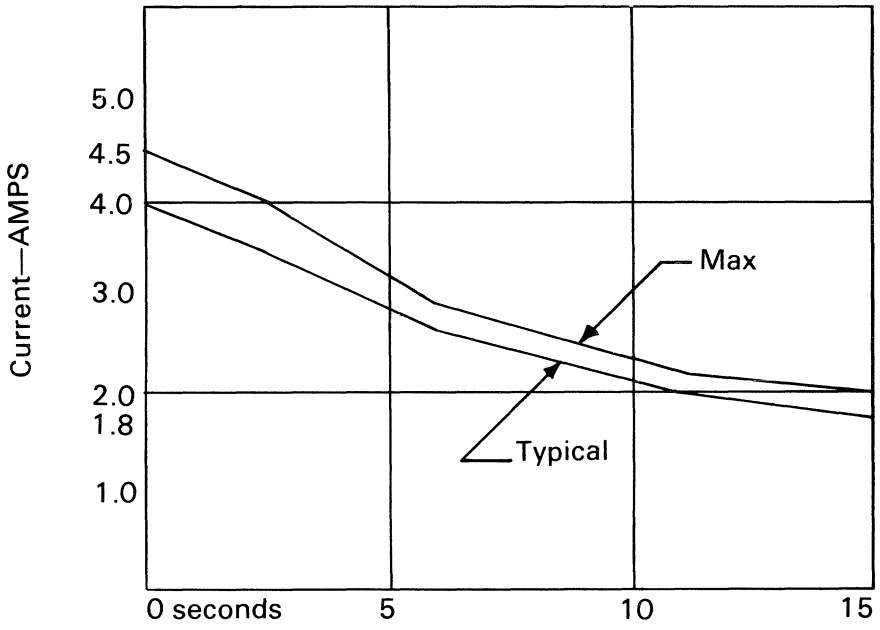
DC POWER REQUIREMENTS

J3 Connector	Current AMPS	
	Max	Typ
Pin 4 +5 Volts DC ± 5% Pin 3 +5 Volt Return	1.0	0.7
Pin 1 +12 Volts DC ± 5%* Pin 2 +12 Volt Return	4.5**	1.8

* ±10% at power on or seeking, ±5% for reading or writing.
** Occurs only during power up, per curve below.

TABLE V

MOTOR START CURRENT REQUIREMENTS



+12V current power up cycle

5.4 J4/P4 Frame Ground Connector

Faston AMP P/N 61761-2

Recommended mating connector AMP 62187-1

If used, the hole in J4 will accomodate a wire size of 18 AWG max.

6.0 Physical Specifications

This section describes the mechanical dimensions and mounting recommendations for the ST-506/412

6.1 Mounting Orientation

Recommended orientation is either vertical on either side or horizontal with PCB down. The only prohibited orientation is horizontal with PCB up. *In the final mounting configuration, insure that operation of the four shock mounting screws should not protrude inside the frame more than .09 inches.*

6.2 Mounting Holes

Eight mounting holes, four on the bottom and two on each side are provided for mounting the drive in an enclosure. The size and location of these holes, shown in Figure 18, are identical to the industry standard minifloppy drive.

6.3 Physical Dimensions

Overall height/width/depth and other key dimensions are shown in Figures 18 and 19. As in the case of the mounting holes, the dimensions are identical to the minifloppy, allowing a direct physical replacement.

6.4 Shipping Requirement

For shipping the heads are positioned over track 140/280 and are held to approximately that position by an edge rubber placed on the top cover. By securing the heads in this manner, there is enough free travel to insure that the heads do not absorb the total shock of any impact, while preventing them from hitting the crash stops. The edge rubber should be removed for use and is not necessary when the drive is shipped mounted in a system. No other precautions are required when shipping the drive.

FIGURE 18

MOUNTING PHYSICAL DIMENSIONS

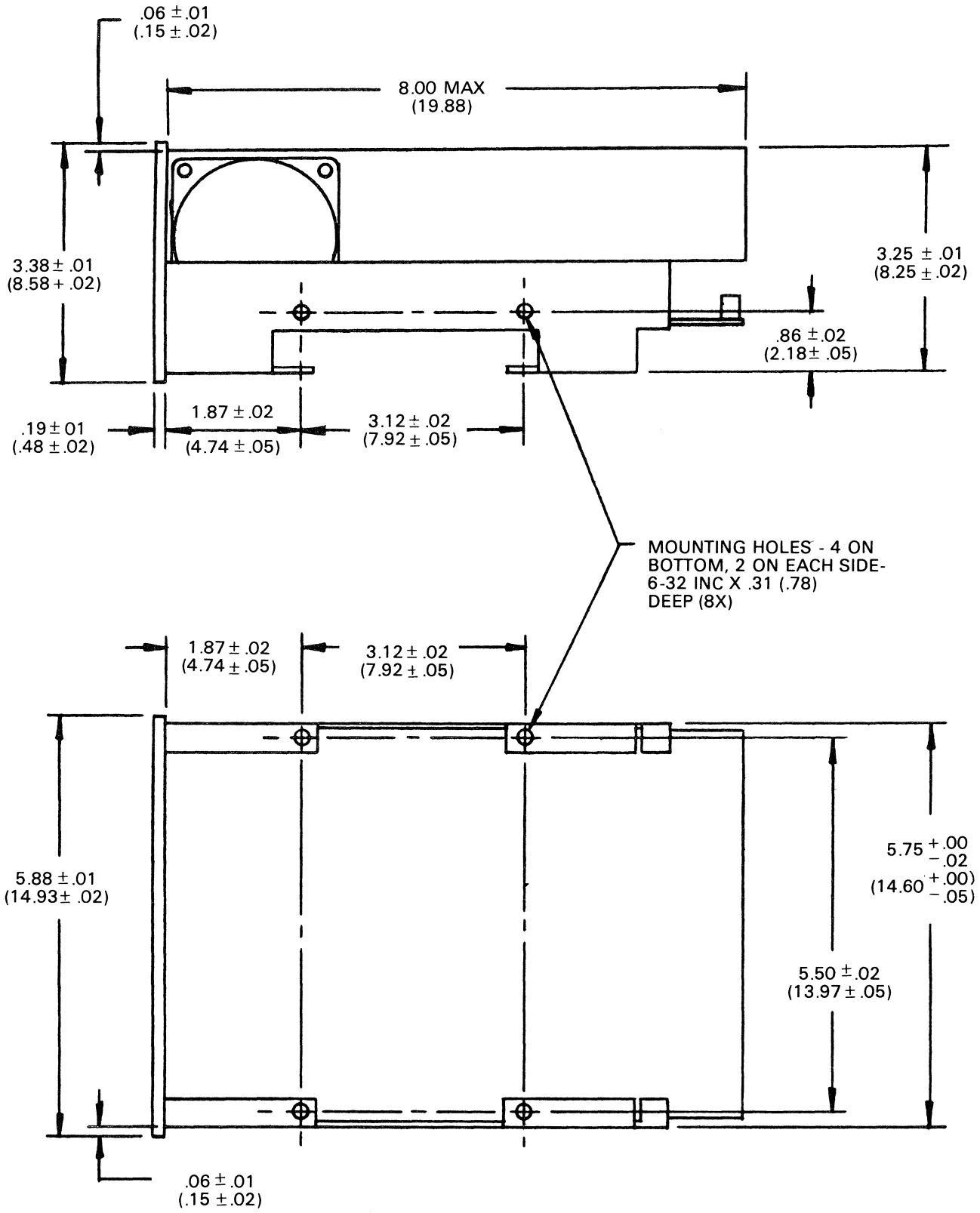
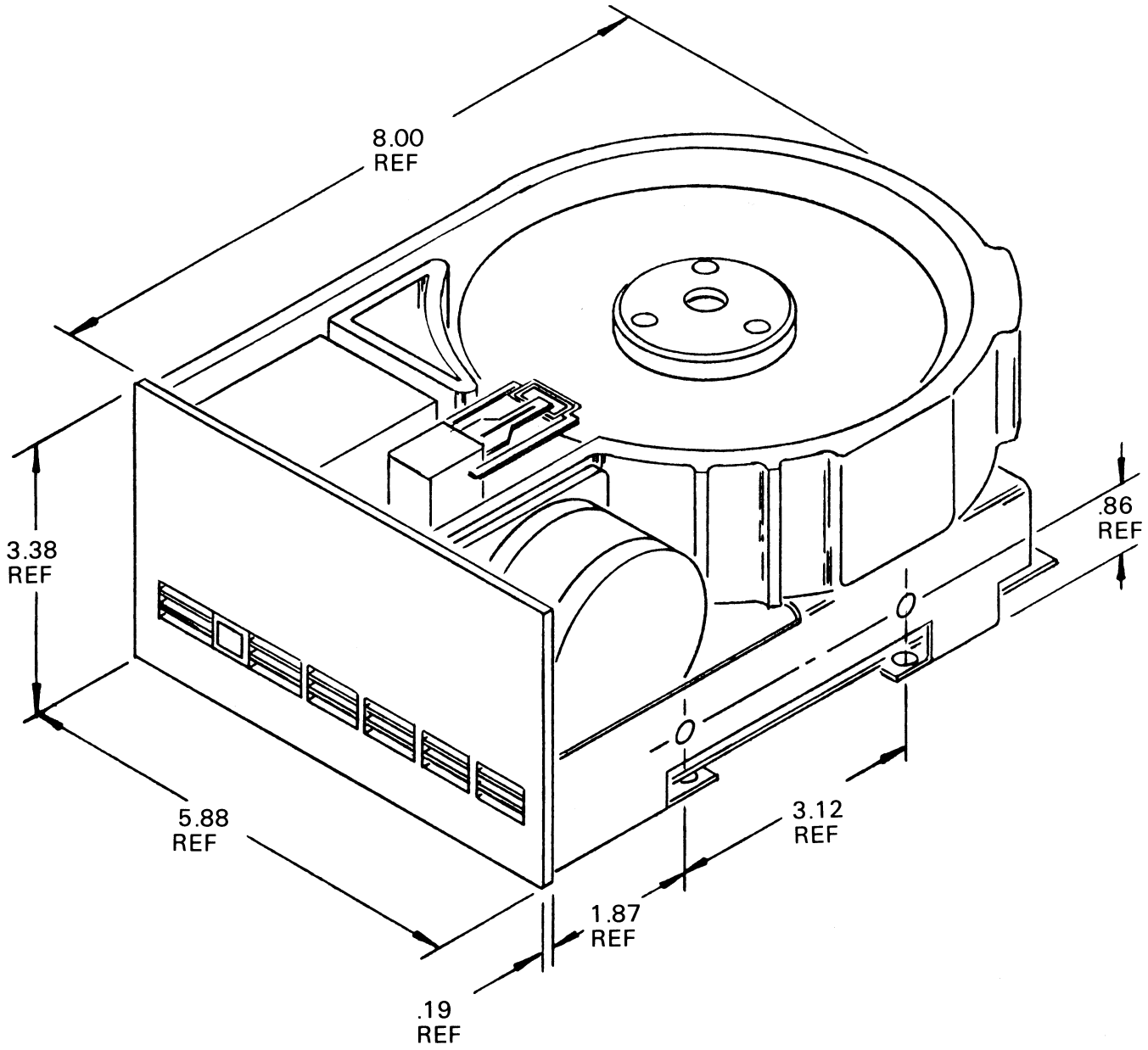


FIGURE 19

OVERALL PHYSICAL DIMENSIONS



7.0 Track Format

The purpose of a format is to organize a data track into smaller sequentially numbered blocks of data called sectors. The format is a soft sectored type which means that the beginning of each sector is defined by a prewritten identification (ID) field which contains the physical sector address plus cylinder and head information. The ID field is then followed by a user supplied data field.

The format is a slightly modified version of the IBM System 34 double density format which is commonly used on floppy disc drives. The encoding method is Modified Frequency Modulation (MFM).

Figure 20 shows the track format as shipped. 8192 bytes are available on each track, based on 32 sectors, each having 256 bytes of user data.

The beginnings of both the ID field and the data field are flagged by unique characters called address marks. An address mark is two bytes in length. The first byte is an "A1" data pattern. This is followed by either an "FE" pattern for an ID address mark, or an "F8" pattern for the data address mark.

The "A1" pattern is made unique by violating the encoding rules of MFM by omitting one clock bit. This makes the address mark pattern unique to any other serial bit combination that could occur on the track. See Figure 21 depiction of the "A1" byte. Each ID and data field is followed by a 16 bit cyclic redundancy check (CRC) character used for a particular data pattern.

Surrounding the ID and data fields are gaps to establish physical and timing relationships between these fields.

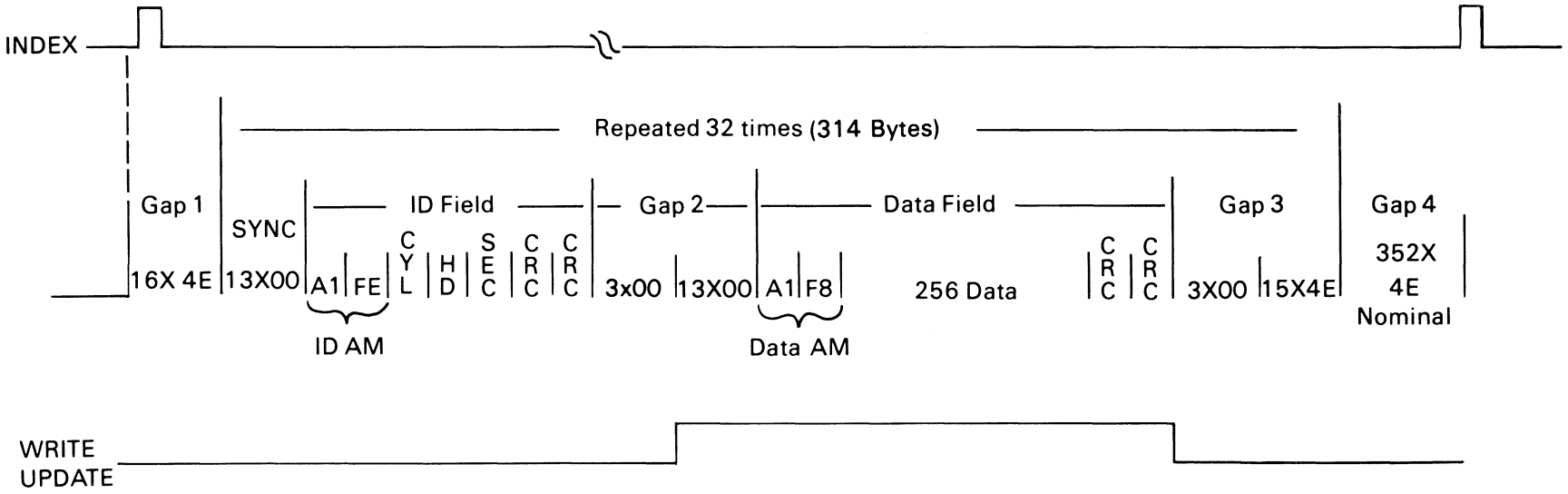
7.1 Gap 1

Gap 1 is to provide for variations in Index detection. As shipped, gap 1 is 16 bytes long, but must be at least 12 bytes. Gap 1 is immediately followed by a sync field preceding the first ID field.

7.2 Gap 2

Gap 2 follows the CRC bytes of the ID field, and continues to the data field address mark. It provides a known area for the data field write splice to occur. The latter portion of this gap serves as the sync up area for the data field AM. As shipped gap 2 is 16 bytes. Minimum length required is determined by the "lock up" performance of the phase-lock-loop in the data separator, which is part of the host control unit.

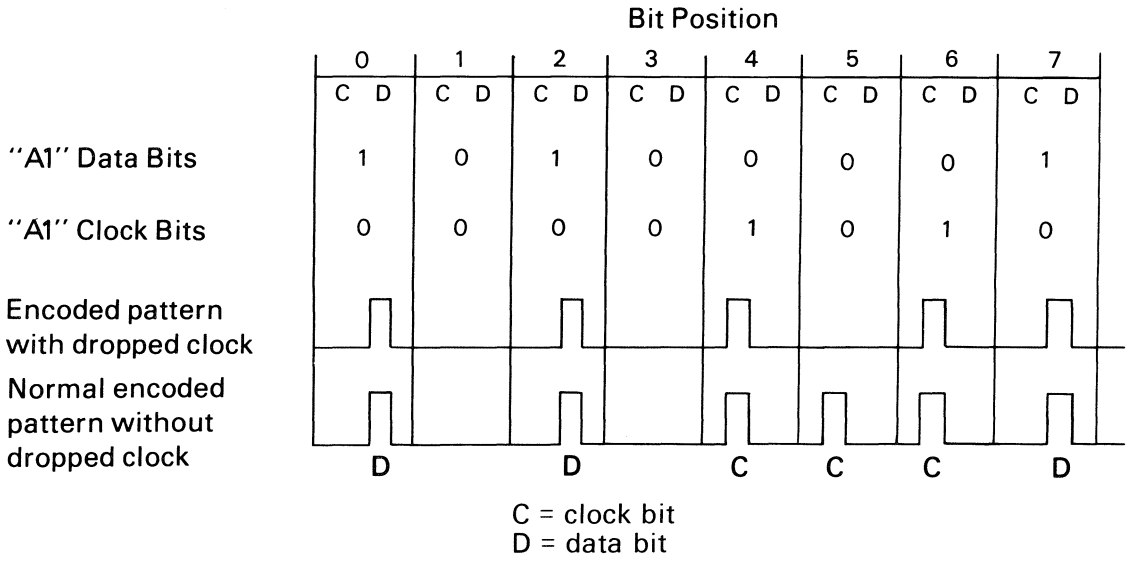
FIGURE 20
TRACK FORMAT AS SHIPPED



NOTES:

1. Nominal Track Capacity = 10416 Bytes
2. Total Data Bytes/Track = 256 x 32 = 8,192
3. Sector interleave factor is 4. Sequential ID Fields are sector numbered 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26,...etc.
4. Data Fields contain the bit pattern 0000 as shipped
5. CRC Fire Code $=x^{16}+x^{12}+x^{5}+1$
6. Bit 7 of Head Byte ID Field equals 1 in a defective sector (Cylinder Ø is error free)
7. Bit 5 of Head Byte reserved for numbering cylinders greater than 256
8. Bit 6 of Head Byte reserved for numbering cylinders greater than 512

FIGURE 21
"A1" ADDRESS MARK BYTE



C = clock bit
D = data bit

7.3 Gap 3

Gap 3 following each data field allows for the spindle speed variations. This allows for the situation where a track has been formatted while the disc is running faster than nominal, then write updated with the disc running slower than normal. Without this gap, or if it is too small, the sync bytes or ID field of the next field of the next field could be over written. As shipped, the gap allows a ±3% speed variation (actual drive spec is ±1%). Minimum gap is 8 bytes for a 256 byte record size.

7.4 Gap 4

Gap 4 is a speed tolerance buffer for the entire track, which is applicable in full track formatting operations to avoid overflow into the index area. The format operation which writes ID fields begins with the first encountered index and continues to the next index. The actual bytes in Gap 4 depends on the exact rotating speed during the format operation.

7.5 Sector Interleaving

As shipped, the track format uses an interleave factor of 4. That is sequentially sectored ID numbers are 0, 8, 16, 24, 1, 9, 17, 25, 2, 10, 18, 26, etc. This allows sufficient system turnaround time to process multiple sectors during a single revolution, thus enhancing through-put of typical file read/write operations.

7.6 Defective Sector Flags

As shipped, any sector which is considered marginal for data recording or which has a permanent defect, will be indicated by the presence of a 1 in bit position 7 of the head byte in the ID field.

In addition, a printout will be provided with each drive which lists the location of these same defects in terms of head number, cyclinder number, sector and byte.

No units will be shipped to customers if surface analysis identifies more than 3 hard errors per surface, or 8 total errors per drive. Additionally no errors will be present on cylinder Ø

Testing for defects involves an analysis of the total media surface under marginalized test conditions.

APPENDIX J: HARD DISK DRIVE MANUFACTURER'S MANUAL

Computer Memories, Inc., Model CM 5000

TABLE OF CONTENTS

TABLE OF CONTENTS (cont.)

1.0 Introduction

1.1 General Description:

The CM 5000 Series of 5¼" Winchester Disk Drives are intended for mini- and microcomputer applications which require high speed random access disk storage at low cost. The units incorporate one, two, or three platters and utilize a Winchester-type head/media technology similar to that used in IBM-3350 type disk drives. Each platter has two data surfaces. Each data surface employs one movable head to service 256 data tracks.

The unit outline dimensions are identical to the envelope of industry-standard minifloppy disk drives and the unit requires only DC voltages for operation. These voltages are compatible with those used by industry-standard minifloppy disk drives.

Each unit consists of a drive mechanics assembly and a PCBA package which provides an industry-standard 5¼" Winchester interface for attachment to a formatter/controller. The interface allows up to 4 drive units to be daisy chained to a single formatter/controller. All electronic components are located outside the head/disk assembly for ease of field serviceability.

Mechanical and contamination protection for the heads, actuator and disks are provided by an impact resistant aluminum enclosure. A self contained recirculating system supplies clean air through a 0.3 micron filter. A breather filter allows pressure equalization with ambient air without chance of contamination.

Key Features:

- Storage capacities of 5.33, 10.67, or 16 Mbytes unformatted.
- Winchester design reliability.
- Same physical size and mounting as standard minifloppies.
- Same DC voltages as minifloppies.
- No AC voltage requirement.
- Swing-arm and metal band positioner.
- 4.34 or 5.0 Megabit/second transfer rate
- Brushless DC spindle motor
- Electronic damping.
- No hysteresis positioning.
- Step-pulse buffer and velocity ramp profile
- Off-track positioning capability (optional)

1.2 Summary of Specifications:

1.2.1 Physical Specifications:

Environmental Limits:

Ambient Temperature:

Operating = 50 °F to 115 °F (10 °C to 46 °C)
Non-operating = – 40 °F to 140 °F (-40 °C to 60 °)

Temperature Gradient:

Operating = 18 °F/hr (10 °C/hr)
Non-operating = Below that which can cause condensation

Max. Wet Bulb = 78 °F (25.6 °C)

Elevation:

Operating = – 100 to 6000 ft (-30 to 1828 meters)
Non-operating = -1000 to 12,000 ft. (-3095 to 3656 meters)

Vibration:

Operating = 1g
Non-operating = 20g

Shock:

Operating = 5g
Non-operating = 20g

Ambient Magnetic Field TBD gauss

EMI Susceptability TBD mv/meter

DC Voltage Requirement:

+ 12 VDC ± 10% 2.0A typical (3.5A starting),
0.5V peak-to-peak maximum ripple

+ 5 VDC ± 5% 0.9A typical (1.0A max.),
50mV peak-to-peak maximum ripple

Heat Dissipation = 100BTU/hr (29 watts)

Mechanical Dimensions:

Height = 3.25 inch (82.6 mm)
Width = 5.75 inch (146.1 mm)
Depth = 8.00 inch (203 mm)
Weight = less than 5 lbs.

Media:

Oxide coated disks (IBM 3350 technology)
Outside diameter: 130 mm
Inside diameter: 40 mm
Thickness: 0.075 inch

1.2.2 Performance Specifications:

Capacity	CM5205	CM5410	CM5616
Unformatted			
Per Drive	5.33 Mbytes	10.67 Mbytes	16.0 Mbytes
Per Surface	2.67 Mbytes	2.67 Mbytes	2.67 Mbytes
Per Track	10416 Bytes	10416 Bytes	10416 Bytes
Formatted			
Per Drive	4.2 Mbytes	8.4 Mbytes	12.6 Mbytes
Per Surface	2.1 Mbytes	2.1 Mbytes	2.1 Mbytes
Per Track	8.2 Kbytes	8.2 Kbytes	8.2 Kbytes
Per Sector	256 Bytes	256 Bytes	256 Bytes
Sectors/Track	32	32	32
Transfer Rate	5.0 or 4.34 Mbits/sec	5.0 or 4.34 Mbits/sec	5.0 or 4.34 Mbits/sec
Average Latency	8.33 or 9.6 msec	8.33 or 9.6 msec	8.33 or 9.6 msec
Access Time (includes settling time)			
Track-to-track	20 msec	20 msec	20 msec
Average	105 msec	105 msec	105 msec
Maximum	240 msec	240 msec	240 msec

1.2.3 Functional Specifications:

	CM5205	CM5410	CM5616
Rotational Speed	3600 or 3125 rpm	3600 or 3125 rpm	3600 or 3125 rpm
Speed Variation	±.1%	±.1%	±.1%
Recording Density	8650 bpi	8650 bpi	8650 bpi
Flux Density	8650 fci	8650 fci	8650 fci
Track Density	345 tpi	345 tpi	345 tpi
Cylinders	256	256	256
Tracks	512	1024	1536
R/W Heads	2	4	6
Disks	1	2	3
Index	1	1	1
Encoding Method	MFM	MFM	MFM

1.2.4 Reliability Specifications

MTBF:	8000 power-on hours
PM:	None required
MTTR:	30 minutes
Component Life:	5 years

Error rates:

Soft read errors =	1 per 10^{10} bits read
Head read errors =	1 per 10^{12} bits read
Seek errors =	1 per 10^{6} seeks

Defects:

No greater than 8 defects/surface. Defects* shall be no larger than 16 bits. Track 000 on each surface shall be defect-free.

*Defect is defined as an area during which the signal amplitude could fall below 55% of track average amplitude or pulses which are greater than 140% of track average amplitude.

2.0 Functional Characteristics

2.1 General Description:

The CM5000 5¼" Winchester disk drive consists of Read/Write and control electronics, read/write heads, track positioning mechanism, media, and air filtration system. These components perform the following functions:

1. Interpret and generate control signals.
2. Position the heads over the desired track.
3. Read and write data.
4. Provide a contamination free environment.

2.2 Read/Write and Control Electronics

Electronics are packaged on two printed circuit boards. The primary board to which power, control and data signals are connected includes:

1. Index detection circuit
2. Head position/actuator drivers
3. Read/Write circuits
4. Head select circuit
5. Step motor drive circuit
6. Drive select circuit
7. Track 000 detector circuit

The primary board also includes a microprocessor which performs the following functions:

1. Controls both the spindle and stepper motor
    a. Spindle speed controlled to .1%
    b. Controls motor braking
    c. Controls start-up current
    d. Senses motor failures, power losses, etc.
    e. Reduces power in stepper motor
    f. Provides ramp-up and ramp-down function
2. Electronic damping
3. Track position count
4. Reduces write current
5. Prevents over-travel
6. Restores head to Track 000 on power-up.
7. Monitors write fault condtions
8. Gives fault indication
9. Controls all internal timing
10. Generates seek complete

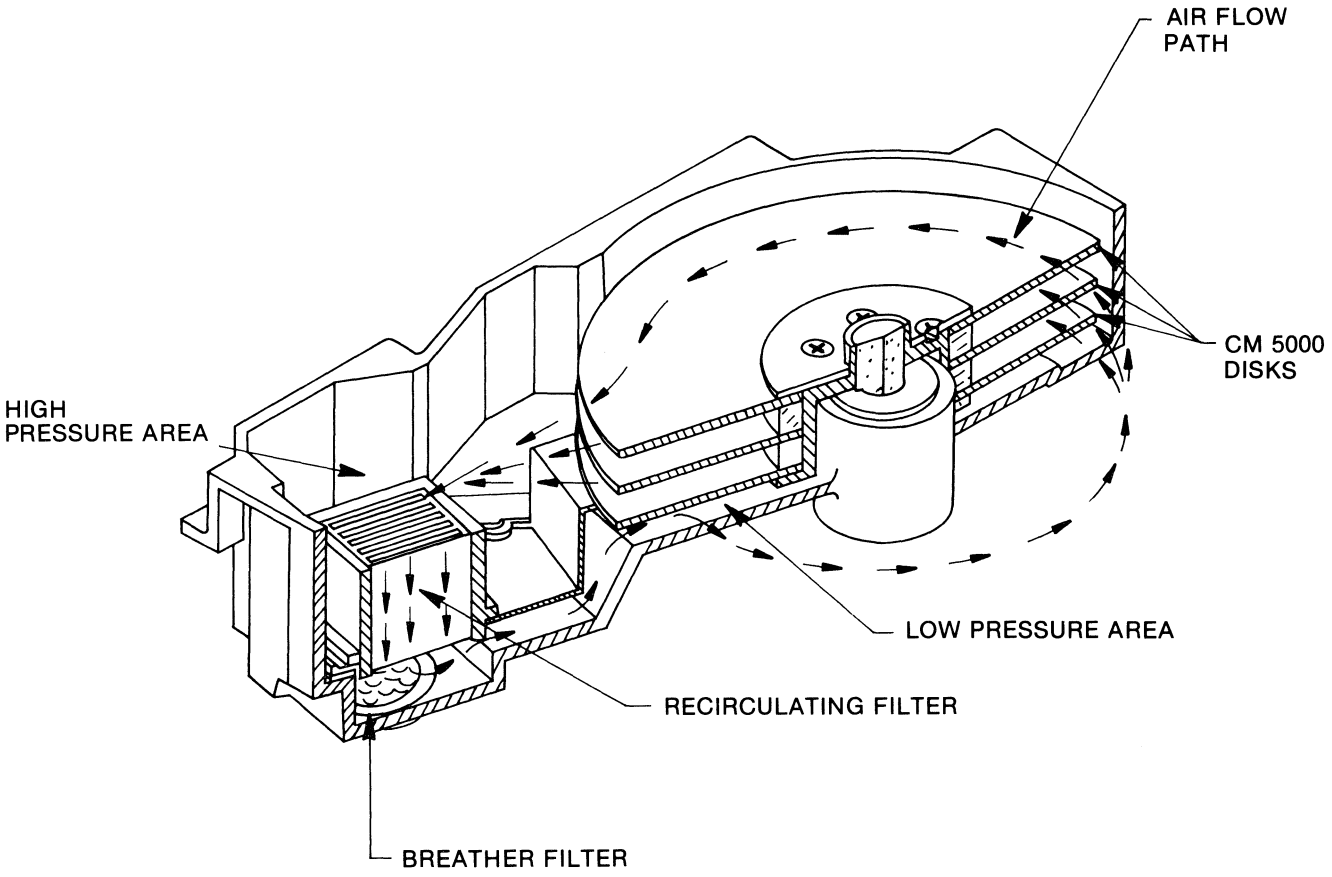
The second printed circuit board derives its power from the primary board and provides power to the spindle drive motor.

2.3 Drive Mechanism

A die cast base houses the recording heads, disks, and the head positioning mechanism as well as the spindle drive motor. Rotational drive for the disks is provided by a direct coupled brushless DC motor. No electronic parts are within the sealed area and electrical connections are made between the recording heads within this area and the electronics via a flexible circuit cable.

2.4 Air Filtration System (Figure 1)

The disks and read/write heads are fully enclosed in a module using an integral recirculation air system with an absolute recirculating filter which maintains a clean environment. A separate absolute breather filter permits pressure equalization with the ambient air without contamination.



CM 5000 AIR CIRCULATION SYSTEM

FIGURE 1.

2.5 Positioning Mechanism (Figure 2)

The positioner is a swing arm mechanism supported on two preloaded ball bearings. The system is designed to accept between 2 and 6 heads depending on the model number. The swing arm is connected via a connecting arm to a metal band/stepping motor actuator system. Each 0.9 degrees rotation of the high precision stepping motor moves the recording heads one track in discrete increments.

2.6 Read/Write Heads and Disks

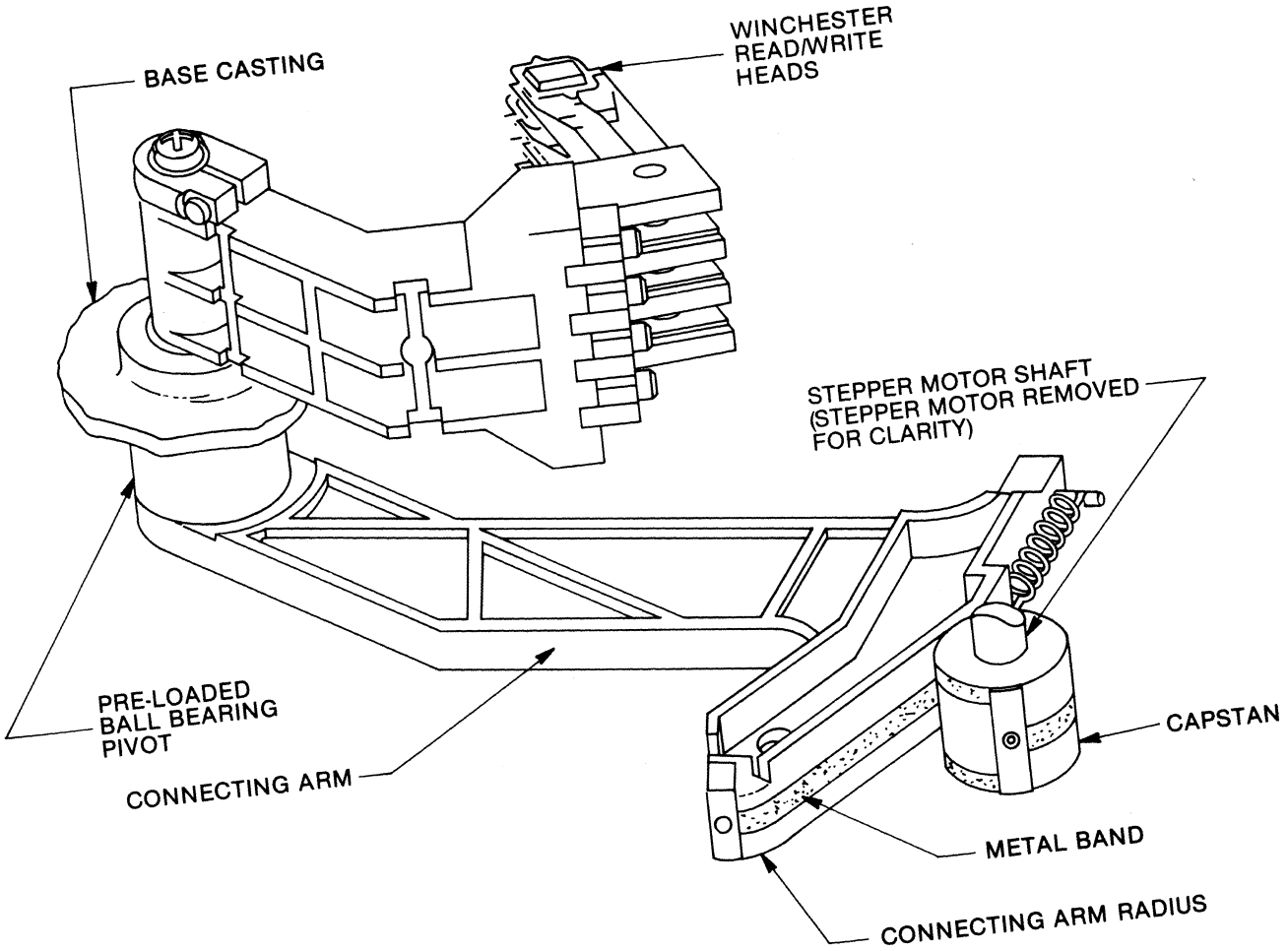
The recording media consists of a lubricated thin magnetic oxide coating on a 130mm outside diameter aluminum substrate. This coating formulation, together with the low load force/low mass Winchester type flying heads, permit reliable contact start/stop operation.

Data on each disk surface is read by one read/write head which accesses 256 tracks. The drive is available in three basic configurations:

one disk with two read/write heads (CM5205)
two disks with four read/write heads (CM5410)
three disks with six read/write heads (CM5616)

2.7 Read/Write Head Landing Zone

to be added.....



CM 5000 POSITIONING SYSTEM
FIGURE 2.

3.0 Functional Operations

3.1 Power Sequencing

The DC voltages, +5v and +12v, may be applied in any order. When the voltages are applied to the drive and the power sense circuit determines that all voltages are within limits, the initial load sequence occurs. This sequence consists of running the spindle up to operating speed and positioning the heads over Cylinder 000.

3.2 Drive Selection

Drive selection occurs when one of the drive select lines are activated. Only the drive appropriately jumpered will respond to the input signals, and that drive's output signals are then gated to the controller.

3.3 Track Accessing

Read/Write head positioning is accomplished by:

a) Deactivating Write Gate
b) Activating the appropriate Drive Select Line.
c) Being in the Ready condition with seek complete true.
d) Selecting the appropriate direction.
e) Pulsing the Step line.

Each step pulse will cause the heads to move either one track in or one track out depending on the status of the Direction Line. A true on the Direction line will cause a seek inward toward the spindle; a false outward toward track 000. Step pulses may be issued to the drive at a rate as fast as 200ms between pulses. The drive will automatically ramp up to as fast as 0.7 msec between tracks before ramping down and settling on the track. Seek complete will go true when the R/W heads have settled on the final track at the end of a seek.

3.4 Head Selection

Any of the 6 possible heads can be selected by placing that head's binary address on the three Head Select lines.

3.5 Read Operation

Reading data from the disk is accomplished by:

a) Deactivating the Write Gate line.
b) Activating the appropriate Drive Select line.
c) Assuring the drive is Ready.
d) Selecting the appropriate head.

3.6 Write Operation

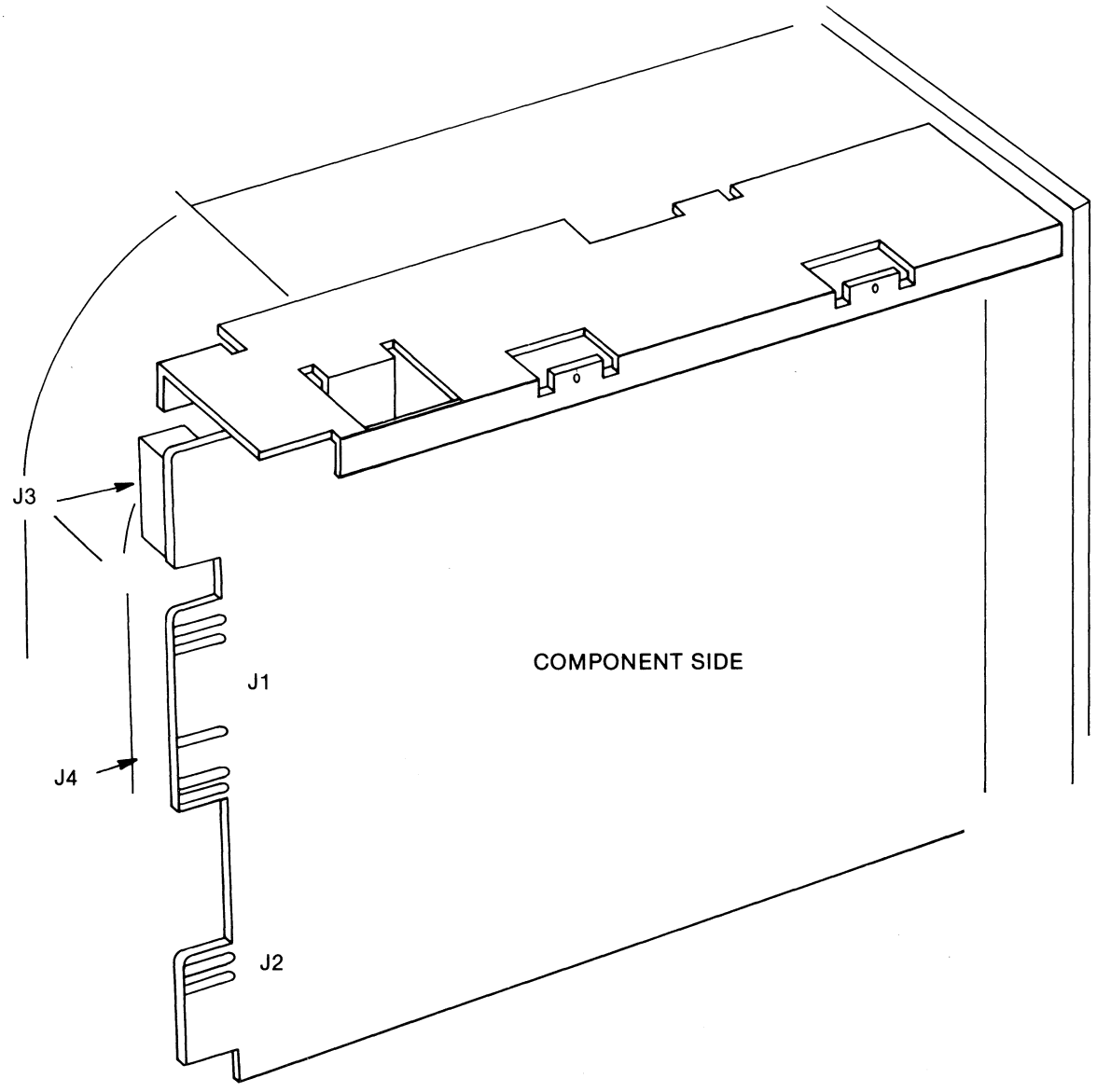
Writing data onto the disk is accomplished by:

a) Activating the appropriate Drive Select line.
b) Assuring that the drive is Ready.
c) Selecting the proper head.
d) Insuring no write fault conditions exist.
e) Activating Write Gate and placing data on the Write Data line.

4.0 Electrical Interface

4.1 Physical Interface

The interface of the drive can be divided into three categories: Control, Signal and DC power. Table I, II and III define the pin assignments for these interface lines. Tables IV and V show the recommended cable type, and the grounding configuration at the drive and at the host systems. Figure 3 indicates the physical location of the connectors. Figure 4 indicates a typical connection for a four drive system.



INTERFACE CONNECTOR PHYSICAL LOCATION

FIGURE 3.

TABLE I J1/P1 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	– OFFTRACK (OPTION)
3	4	– HEAD SELECT 2^2
5	6	– WRITE GATE
7	8	– SEEK COMPLETE
9	10	– TRACK 000
11	12	– WRITE FAULT
13	14	– HEAD SELECT 2^0
15	16	RESERVED (TO J2 PIN 7)
17	18	– HEAD SELECT 2^1
19	20	– INDEX
21	22	– READY
23	24	– STEP
25	26	– DRIVE SELECT 1
27	28	– DRIVE SELECT 2
29	30	– DRIVE SELECT 3
31	32	– DRIVE SELECT 4
33	34	– DIRECTION IN

TABLE II J2/P2 CONNECTOR PIN ASSIGNMENT

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	– DRIVE SELECTED
4	3	RESERVED
6	5	SPARE
8	7	RESERVED (TO J1 PIN 16)
10	9	SPARE
12	11	GND
	13	+ MFM WRITE DATA
	14	– MFM WRITE DATA
16	15	GND
	17	+ MFM READ DATA
	18	– MFM READ DATA
20	19	GND

TABLE III P3 — DC CONNECTOR PIN ASSIGNMENTS

VOLTAGE	GROUND
PIN 1 + 12 VOLTS DC	PIN 2 + 12 VOLT RETURN
PIN 4 + 5 VOLTS DC	PIN 3 + 5 VOLT RETURN

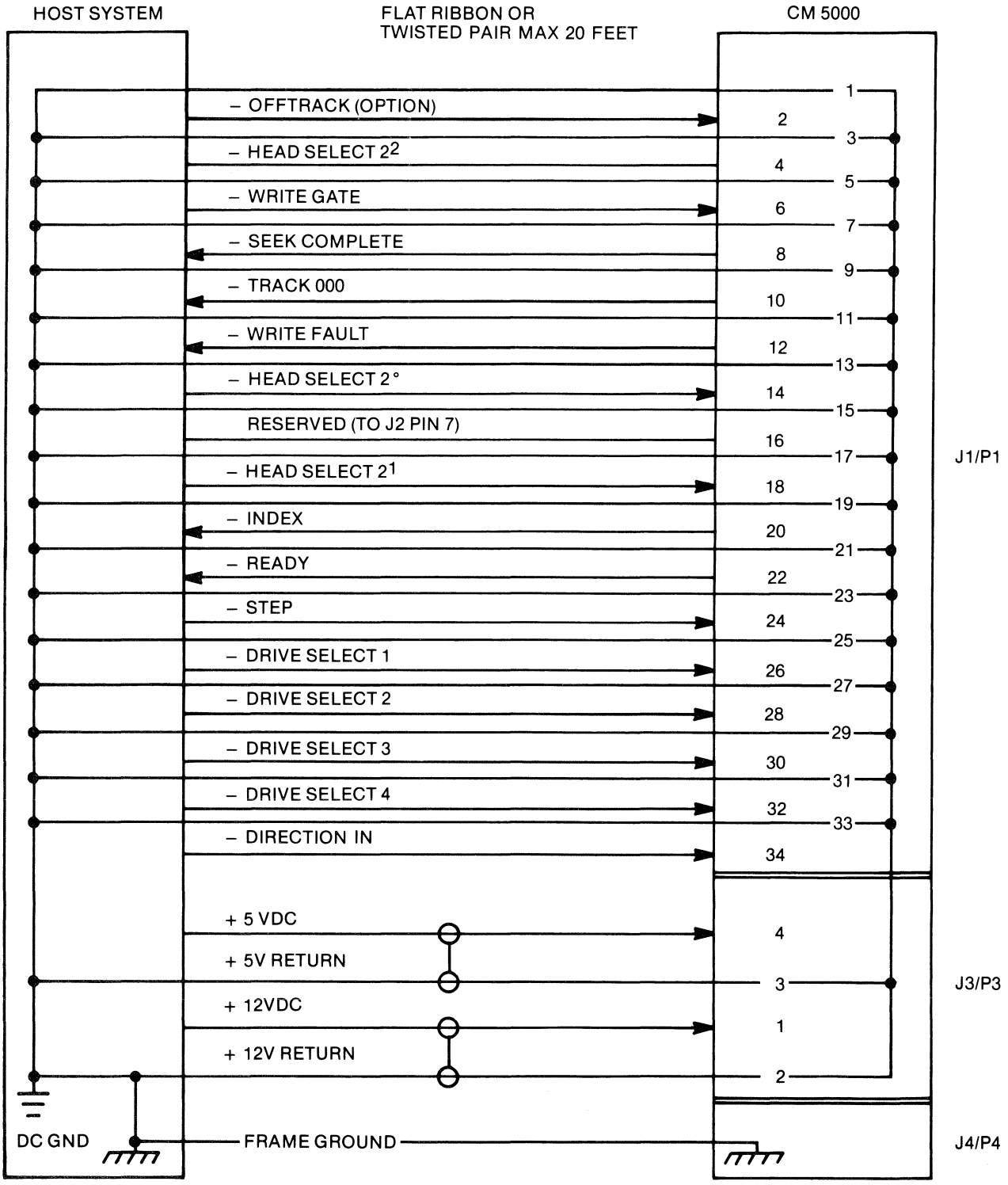


TABLE IV SINGLE DRIVE SYSTEM J2/P2 NOT SHOWN

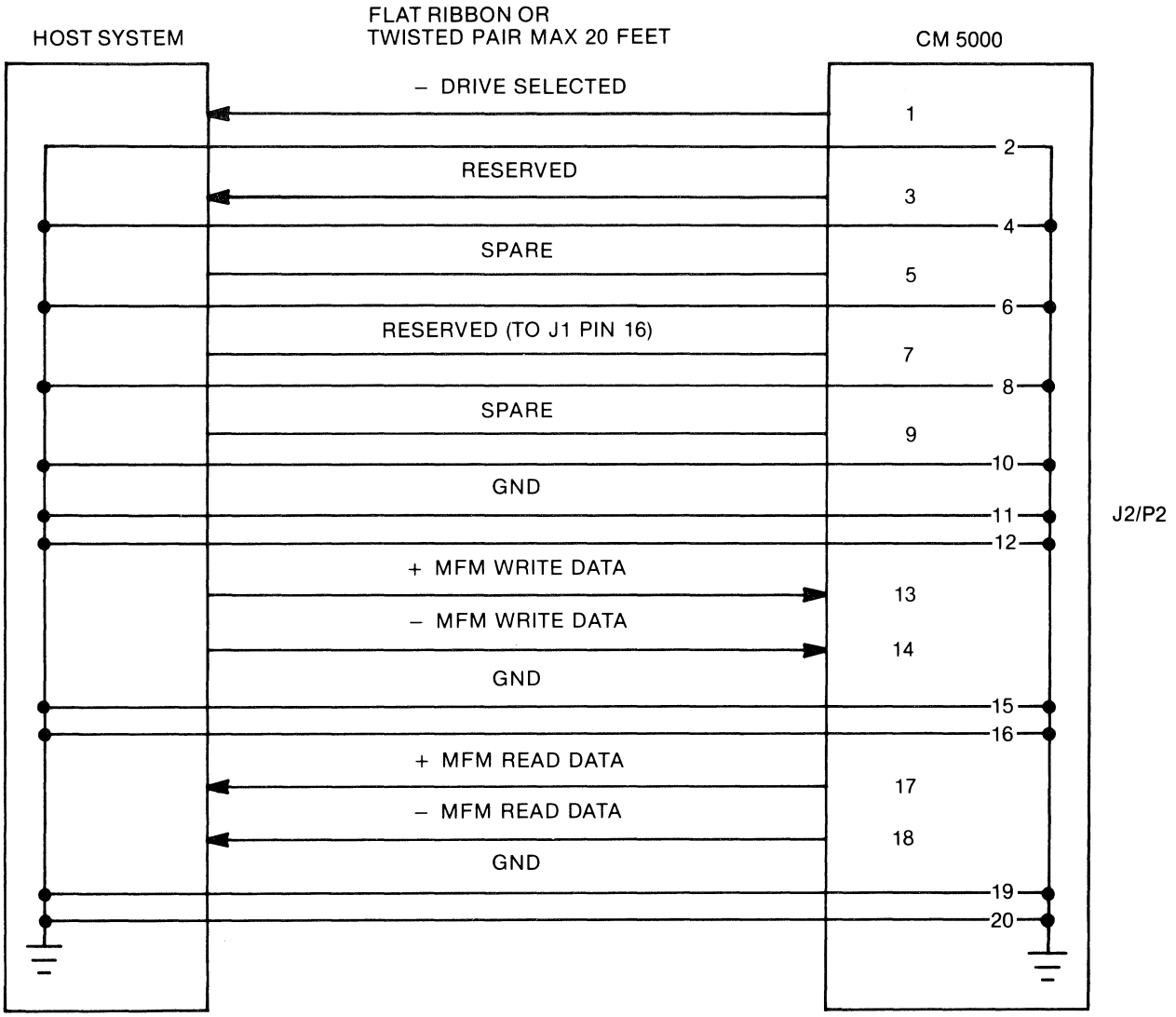


TABLE V SINGLE DRIVE SYSTEM J2/P2

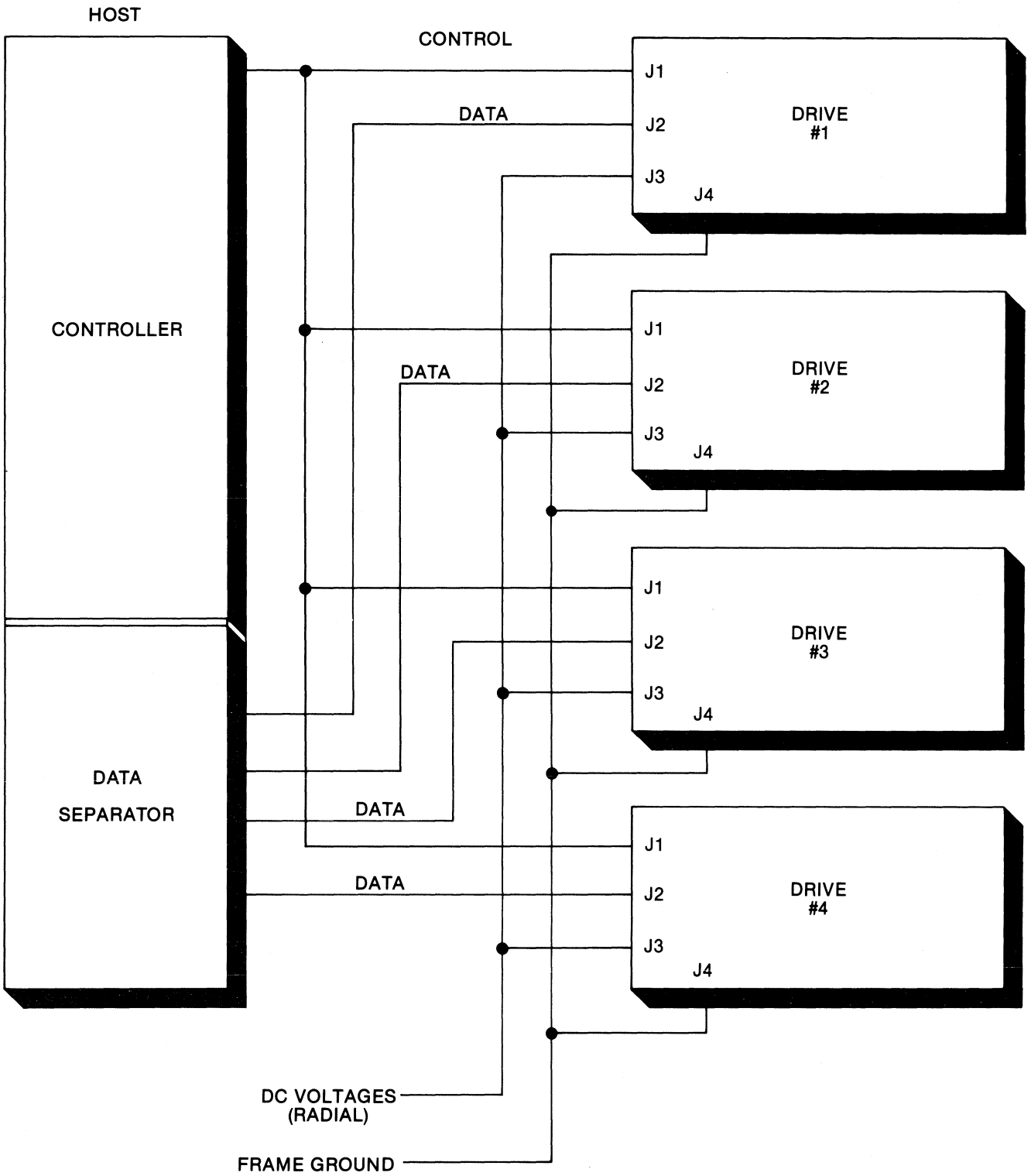


FIGURE 4.

Computer Memories Hard Disk Drive J-21

4.1.1 J1/P1 CONNECTOR

Connection to J1 is via a 34 pin PCB edge connector. The dimensions for this connector are shown in Figure 5. The pins are numbered 1 through 34 with the even pins located on the component side of the PCB. Pin 2 is located on the end of the PCB connector closest to the DC power connector J3/P3. A key slot is provided between pins 4 and 6. The recommended mating connector for P1 is AMP ribbon connector PIN 88373-3.

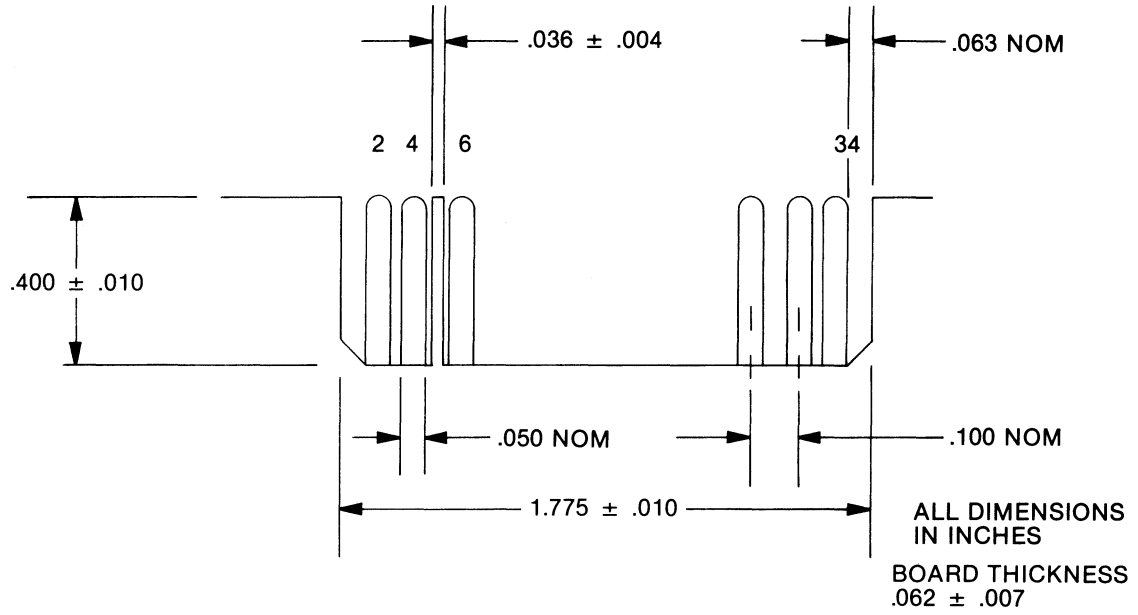


FIGURE 5. J1 CONNECTOR DIMENSIONS

4.1.2 J2/P2 CONNECTOR

Connection to J2 is via a 20 pin PCB edge connector. The dimensions for the connector are shown in figure 6. The pins are numbered 1 through 20 with the even pins located on the component side of the PCB. The recommended mating connector for P2 is AMP ribbon connector P/N 88373-6. A key slot is provided between pins 4 and 6.

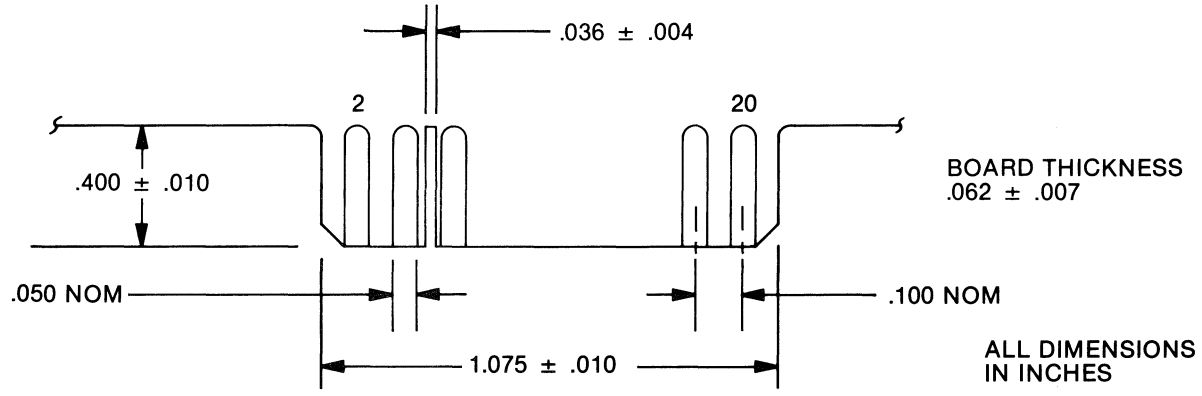


FIGURE 6. CONNECTOR DIMENSIONS

4.1.3 J3/P3 CONNECTOR

The DC Power connector (J3), Figure 7, is a 4 pin AMP MATE-N-LOK connector P/N 350211-1 mounted on the solder side of the PCB. The recommended mating connector (P3) is AMP P/N 1-480424-0 utilizing AMP pins P/N 350078-4.

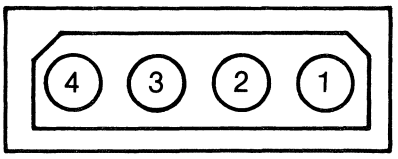


FIGURE 7 J3 CONNECTOR (DRIVE PCB SOLDER SIDE).

The required voltages and current levels on connector J3/P3 are shown below.

DC VOLTAGE	CURRENT	
	MAX.	TYP.
+12 ± 1.2V 0.5 V P-P Max. Ripple	3.5A (Start current)	2.0A
+5 ± 0.25V 50mV P-P Max. Ripple	1.0A	0.9A

4.1.4 J4/P4 FRAME GROUND CONNECTOR

FASTON AMP P/N 62275-1

4.2 Interface Lines and Pin Assignments

4.2.1 CONTROL INPUT LINES

The control input signals are of two types: those to be multiplexed in a multiple drive system and those intended to do the multiplexing. The control input signals to be multiplexed are OFFTRACK (OPTION), WRITE GATE, HEAD SELECT 2^0, HEAD SELECT 2^1, HEAD SELECT 2^2, STEP and DIRECTION IN. The signal to do the multiplexing is DRIVE SELECT 1, DRIVE SELECT 2, DRIVE SELECT 3, or DRIVE SELECT 4.

The input lines have the following electrical specifications. Refer to figure 8 for the recommended circuit.

TRUE: 0.0VDC to 0.4 VDC @ I = – 40 mA (max)

FALSE: 2.5VDC to 5.25 VDC @ I = OmA (Open)

Each control input line is terminated by a 220/330 resistor pack as shown in figure 5.

4.2.1.1 DRIVE SELECT 1, 2, 3, AND 4.

The Drive Select lines, when true, enable the input lines of the correspondingly programmed drive(s). Only one Drive Select line should be true at any time.

4.2.1.2 HEAD SELECT 2^0, 2^1, AND 2^2

These lines provide for the selection of each individual read/write head in a binary coded sequence. HEAD SELECT 2^0 is the least significant address line. Heads are numbered 0 and 1 on the CM 5205; 0 through 3 on the CM 5410 and 0 through 5 on the CM 5616.

4.2.1.3 WRITE GATE

The active (true) state of this signal enables write data to be written on the selected disk of the selected drive provided that READY and SEEK COMPLETE are true, the head is not OFFSET and no WRITE FAULT exists on the selected drive. The inactive state of WRITE GATE permits the STEP pulses to step the R/W actuator on the selected and READY drive or it enables data to be transferred from that drive if SEEK COMPLETE is true.

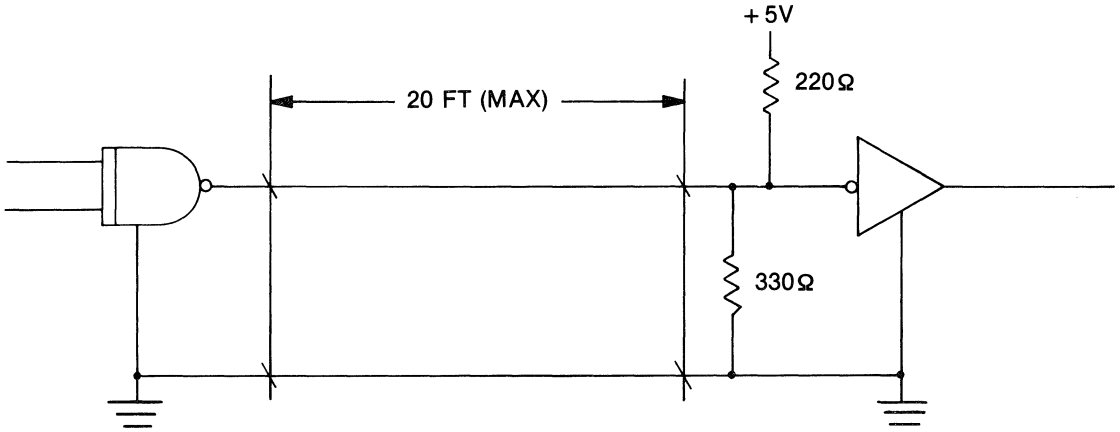


FIGURE 8. CONTROL SIGNAL DRIVER/RECEIVER COMBINATION

4.2.1.4 STEP

This is a control signal which causes the R/W head to move in the direction of motion defined by the DIRECTION IN line. In the normal seeking mode the head moves one track for each STEP pulse. Optionally if OFFTRACK is true then the STEP and DIRECTION IN signals are used to move the head approximately one sixth of a track from its nominal position. See section 4.2.1.6 OFFTRACK for further details on this option.

Motion is initiated by the leading edge (i.e. false to true) of the STEP pulse. Any change in the DIRECTION line must be made at least 100nS before the leading edge of the STEP pulse.

STEP pulses may be issued at any interval as low as 200 uS. The minimum pulse width is 1.0uS.

See figure 9 for STEP pulse timing.

In a restore (recalibration) operation the minimum interval between successive STEP pulses should be 3.0mS.

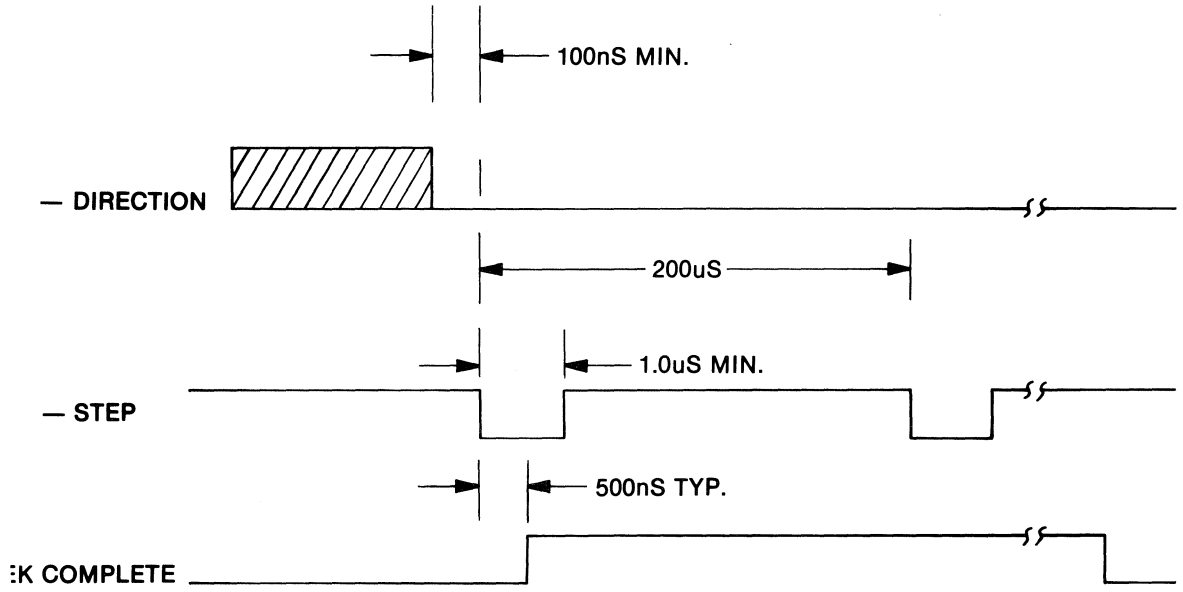


FIGURE 9. STEP PULSE TIMING

4.2.1.5 DIRECTION IN

This signal defines the direction of motion of the R/W head when the STEP line is pulsed. When the signal is false the direction is defined as "out" and a STEP pulse causes the R/W heads to move away from the center of the disk. .When this line is true the direction is defined as "in" and the heads will move toward the center of the disk. The tracks are numbered 000 through 255 and track 000 is the outermost track. If an attempt is made to seek out beyond track 000 or in beyond track 255 the actuator will stop when one of these extremes is reached.

Once a move has been initiated no attempt should be made to reverse the direction of seeking while the SEEK COMPLETE Line is false.

4.2.1.6 OFFTRACK

The true state of this signal in conjunction with a STEP pulse will cause the R/W heads to move from their nominal track position by approximately one tenth of a track in the direction defined by the DIRECTION IN line. The actuator will only move by one such increment on a given side of nominal, an attempt to go further offtrack will be ignored. The actuator may be restored to its nominal position by means of a single STEP pulse with the OFFTRACK line true and the DIRECTION IN line set to the opposite sense to that when the offtrack condition was introduced. The normal stepping mode is resumed whenever STEP pulses are issued with the OFFTRACK Line false, regardless of the starting condition of the actuator, i.e. the actuator will now seek to the nominal position of the newly addressed track.

Writing is inhibited in the OFFTRACK condition and any attempt to write will generate a WRITE FAULT response.

Figure 10 shows offtrack mode timing.

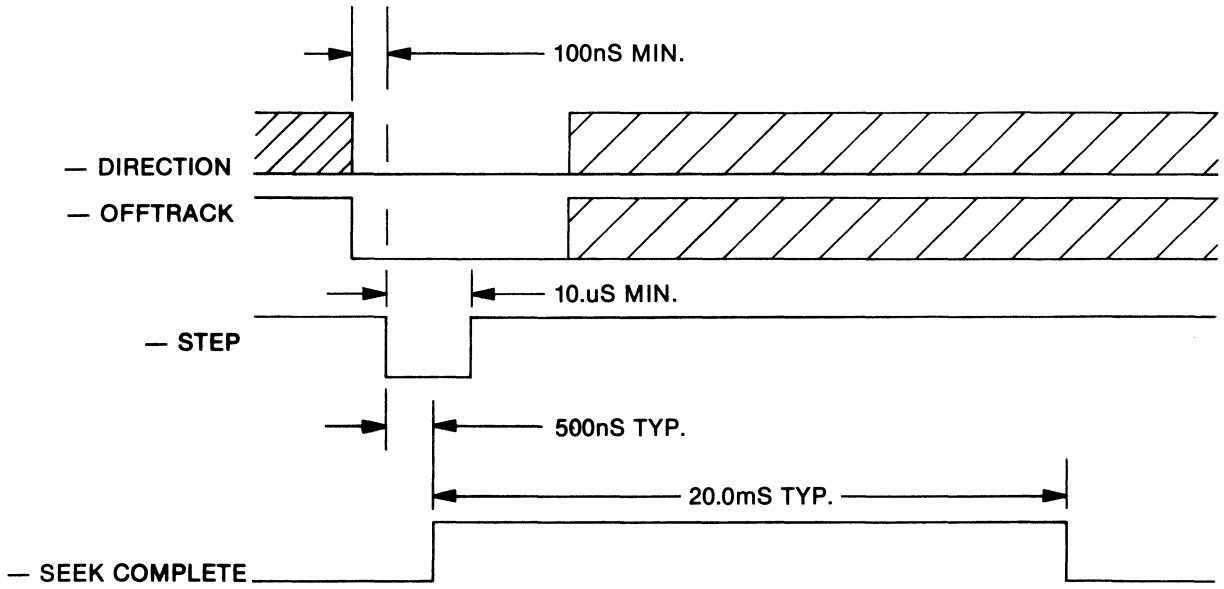


FIGURE 10. OFFTRACK MODE TIMING

4.2.2 Control Output Lines

The output control lines are driven with an open collector output stage capable of sinking a maximum of 40mA at the true or active state with a maximum voltage of 0.4V measured at the driver. In the false or inactive state the output transistor is off and the maximum collector cutoff current is 250uA.

The output control lines are enabled by the programmed DRIVE SELECT Line.

The recommended circuit is shown in figure 8.

4.2.2.1 SEEK COMPLETE

This line will go true when the R/W heads have settled on the final track at the end of a seek. If the OFFTRACK option is used it will also go true when the heads have settled following any of these incremental moves.

The SEEK COMPLETE Line will go false at the following times:

a) During the power on sequence while the drive logic is in the process of restoring the R/W heads to track 000.
b) Approximately 500nS after the leading edge of the first in any series of STEP pulses.

The minimum duration which this line will remain in the false state is approximately 20.0mS.

Writing is inhibited when SEEK COMPLETE is false. Any attempt to write during this period will generate a WRITE FAULT. When false SEEK COMPLETE also inhibits the transmission of MFM READ DATA.

No attempt should be made to reserve the direction of stepping when SEEK COMPLETE is false.

4.2.2.2 TRACK 000

The true state of this line is generated when the R/W heads are on their last step approaching track 000, i.e., when they are moving from track 001 to track 000. It remains true as long as the heads are positioned at track 000. Track 000 is the outermost track.

4.2.2.3 WRITE FAULT

This signal is used to indicate that a condition exists in the drive which causes improper writing on the disk(s). When this line is true, further writing is inhibited at the drive until the condition is corrected.

The following conditions are detected:

a) Write current in a head without WRITE GATE active.
b) No write current in a head with WRITE GATE active and DRIVE SELECTED.
c) WRITE GATE active when the heads are set in an offtrack position and the drive is selected.
d) The DC voltages are grossly out of tolerance.

WRITE FAULT may be cleared by de-selecting the drive for a period exceeding 50μsecs, otherwise the condition will automatically clear 2 msecs after the conditions generating the fault have been removed.

Writing is inhibited internally during seeking or if WRITE GATE is true at the time of SEEK COMPLETE going true.

4.2.2.4 INDEX

The leading edge (i.e. false to true) of this pulse indicates the beginning of each track. The pulse occurs once per revolution of the disk (16.67 mS nom.).

4.2.2.5 READY

When the READY line is true together with SEEK COMPLETE the drive is ready to seek or read and if in addition the heads are not offtrack it is also ready to write. When this line is false the I/O signals are not valid, also, writing, seeking and the transmission of read data are inhibited.

At power on the READY line goes true when the DC voltages are within tolerance, the disks are rotating at the correct speed and the heads are positioned at track 000.

The READY Line will go false when the DC voltages are out of tolerance and/or the disks fail to maintain regulated speed.

4.3 DATA TRANSFER LINES

The data transfer lines are provided at the J2/P2 connector. They are differential in nature and may not be multiplexed.

Two pairs of balanced signals are used for the transfer of data, one pair each for MFM WRITE DATA and MFM READ DATA. Figure 11 illustrates the driver/receiver combination used in the CM 5000 drive for data transfer signals.

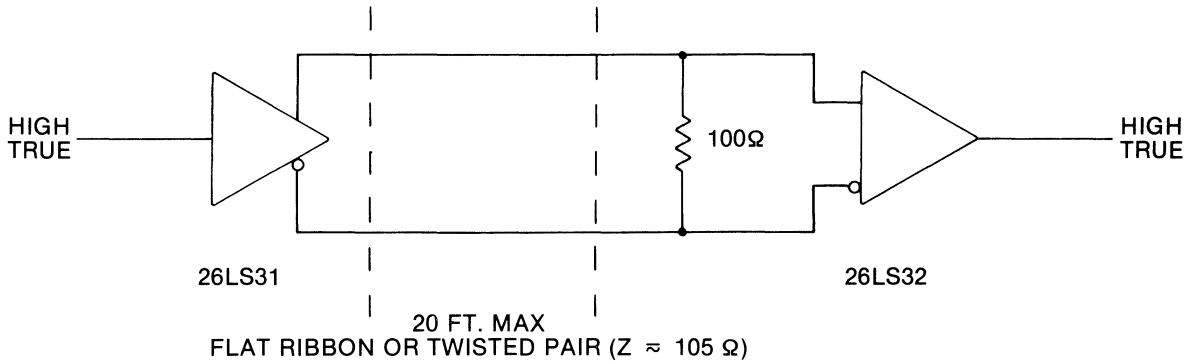


FIGURE 11. DATA LINE DRIVER/RECEIVER

4.3.1 MFM WRITE DATA

This is a differential pair that defines the transitions to be written on the track. When WRITE GATE is active the transition of the signal + MFM WRITE DATA going more positive than — MFM WRITE DATA causes a flux reversal to be recorded on the track. When WRITE GATE is inactive the host system must hold + MFM WRITE DATA more negative than — MFM WRITE DATA.

The standard MFM write data transmission rate is 5.000 Mbits/sec. Optionally, the drive may be provided with transfer rate of 4.34 Mbits/sec. The write data timing is shown in figure 12. The actual occurence of the flux reversals may differ due to write precompensation.

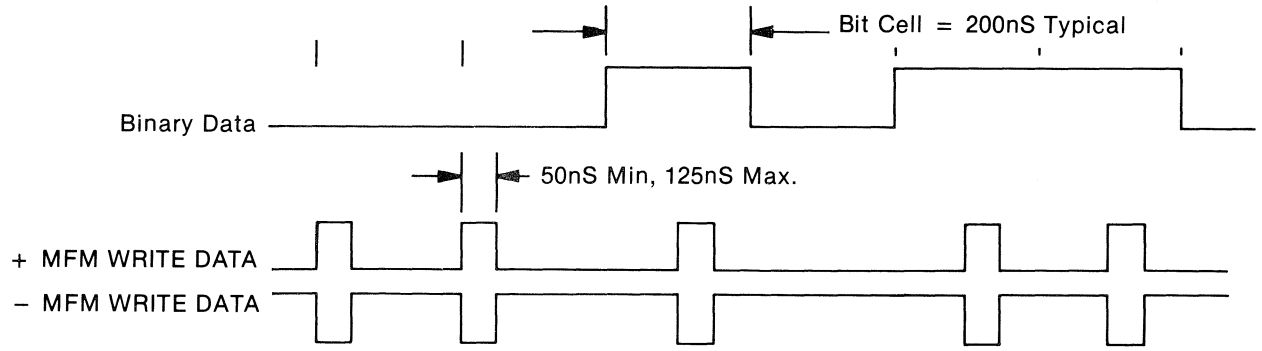


FIGURE 12. MFM WRITE DATA TIMING.

4.3.2 MFM READ DATA

Data recovered from a pre-recorded track is transmitted to the host system via a differential pair of MFM READ DATA lines. The transition of the +MFM READ DATA line going more positive than the –MFM READ DATA line represents a flux reversal on the track of the selected head.

Read data is suppressed during writing and seeking operations and also when the drive is not selected. Following a write operation and/or a HEAD SELECT change the read data will not be valid for a period of up to 20uS. If the drive is already selected at the end of a seek operation, read data will appear immediately upon SEEK COMPLETE. When the drive has been de-selected, read data will not re-appear for a period of up to 100uS after it is reselected.

Typical MFM read data timing is shown in figure 13.

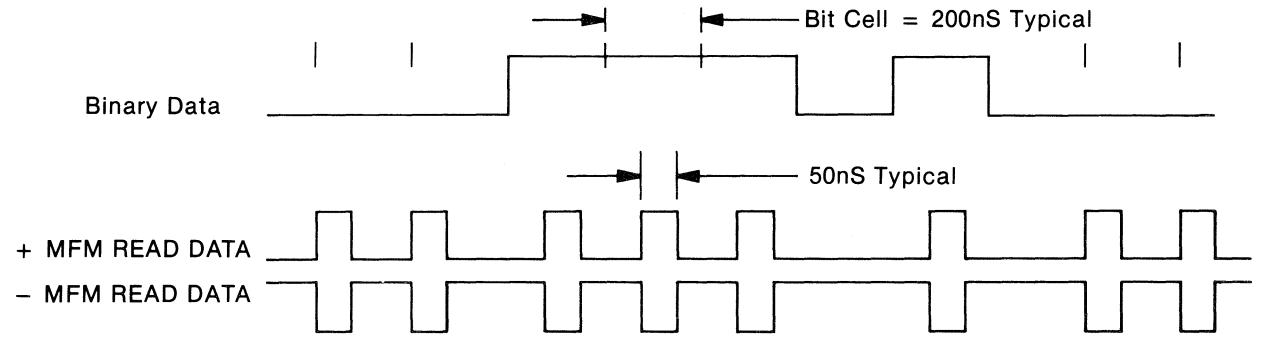


FIGURE 13. MFM READ DATA TIMING.

4.3.3 DRIVE SELECTED

This status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The DRIVE SELECTED Line is driven by a TTL open collector driver as shown in figure 8. When the appropriate DRIVE SELECT line at J1/P1 is activated by the host system this signal will go active on the correspondingly programmed drive.

4.4 GENERAL TIMING REQUIREMENTS

Figure 14 is a timing diagram showing the necessary sequence of events and associated timing restrictions for proper operation of the drive.

Note that an automatic recalibration to track zero occurs at DC power on. At DC power off the disks are brought to a complete stop in approximately 20Secs.

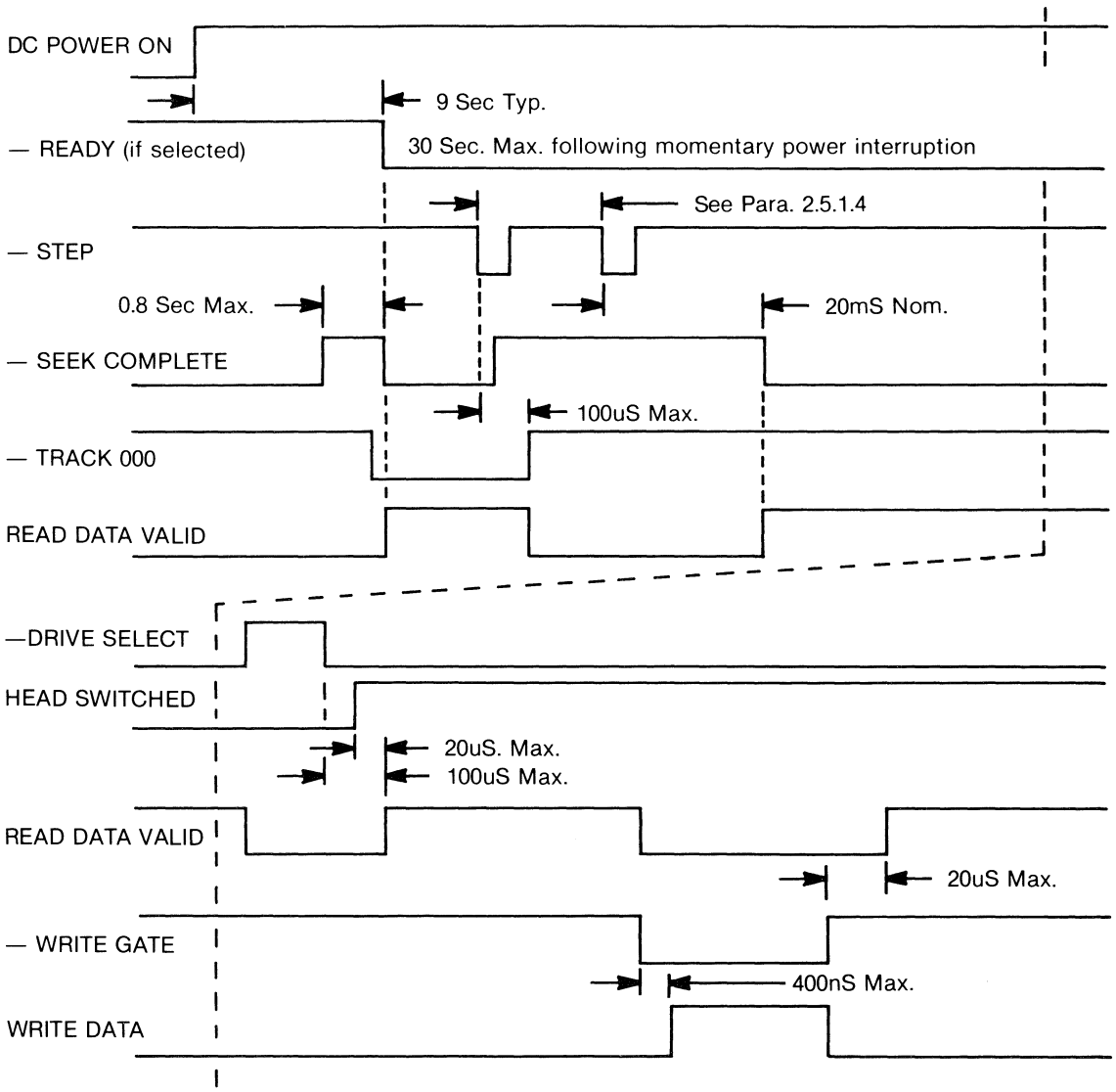


FIGURE 14. GENERAL TIMING REQUIREMENTS.

5.0 Physical Specifications

This section describes the mechanical and mounting recommendations for the CM 5000.

5.1 Mounting Orientation

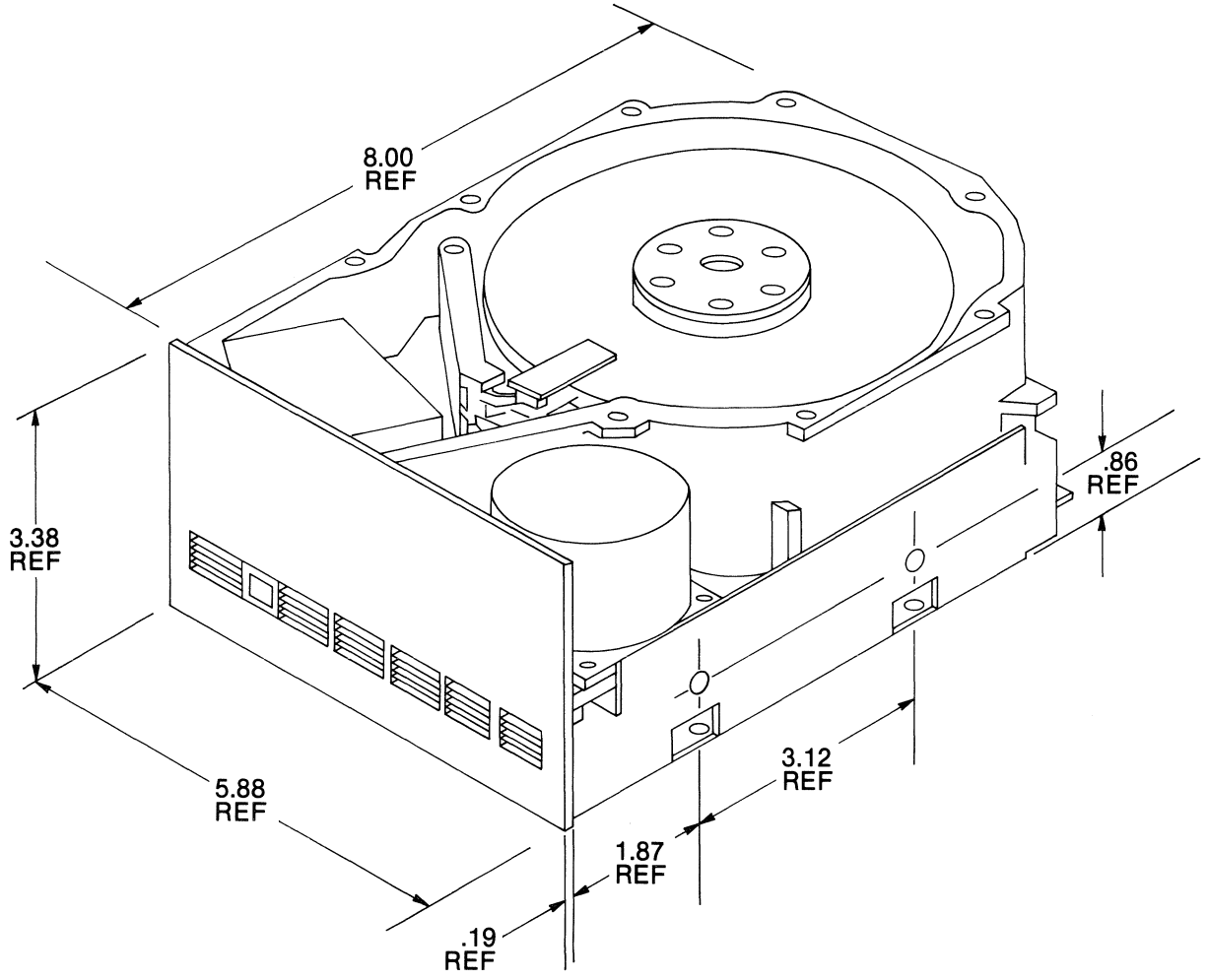
The CM 5000 may be mounted in any orientation. In the final mounting configuration, insure that operation of the four shock mounts which isolate the base casting from the frame is not restricted.

5.2 Mounting Holes

Eight mounting holes, four on bottom and two on each side are provided for mounting the drive into an enclosure. The size and location of these holes, shown in Figure 15, are identical to industry standard minifloppy drives.

5.3 Physical Dimensions

Overall height/width/depth and other key dimensions are shown in Figures 15 and 16.



CM500 MECHANICAL OUTLINE
GENERAL PERSPECTIVE.

FIGURE 15.

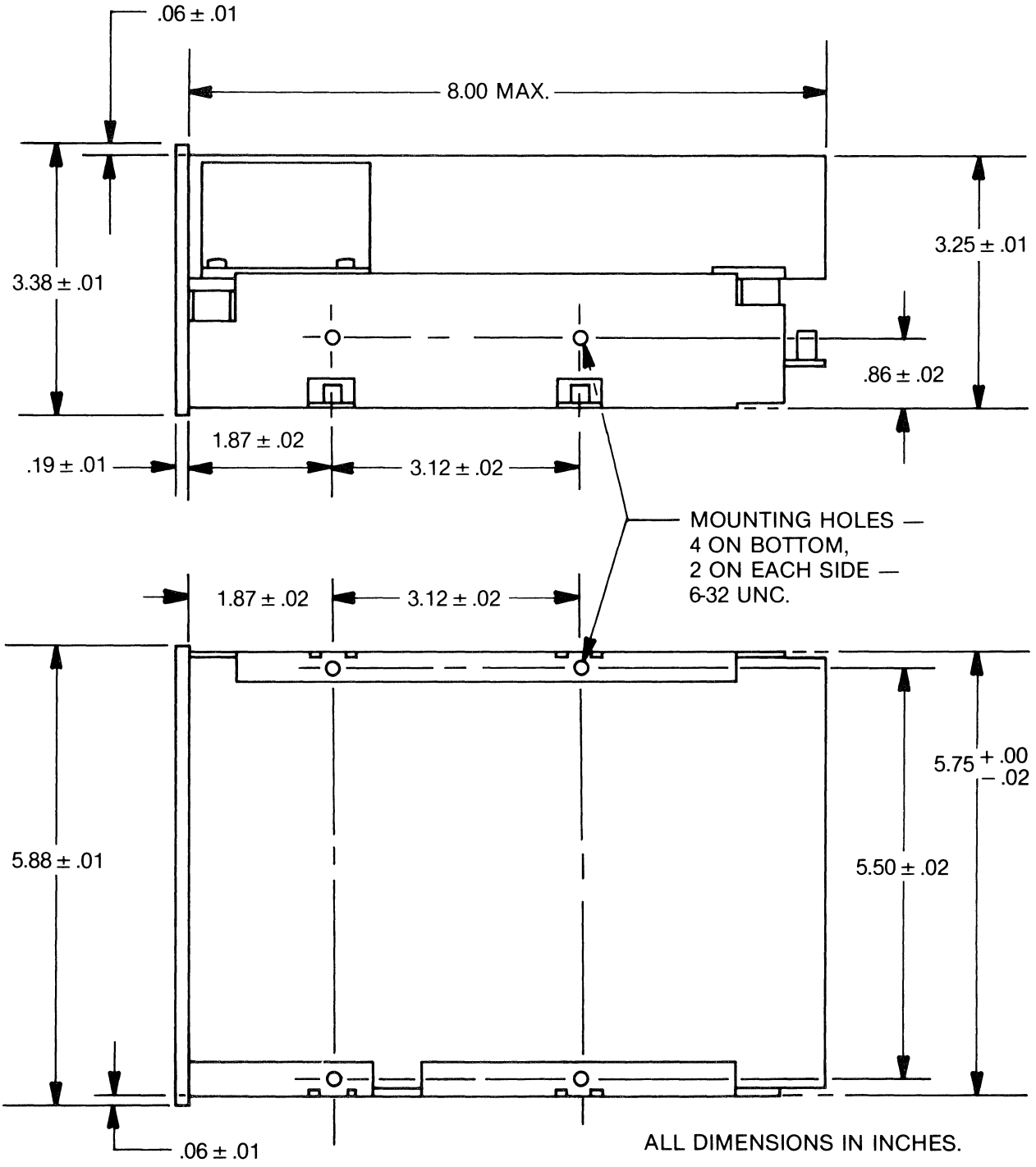


FIGURE 16. CM5000 MECHANICAL OUTLINE
BOTTOM AND SIDE VIEWS.

6.0 Media Defect and Errors

Any defects on the media surface will be identified on a defect map provided with each drive. This defect map will indicate the Head number, Track number, and number of bytes from index for each defect. The maximum number of defects/surface is eight (8) with track 000 certified to be defect-free on each surface. Each defect shall be no longer than 16 bits (a defect is defined as an area during which the signal amplitude could fall below 55% of track average amplitude or pulses which are greater than 140% of track average amplitude)

7.0 CM 5000 Track Format

to be added . . . .

8.0 CM 5000 Jumper Options

All jumper options are shown in Figure 17 and Table VI.

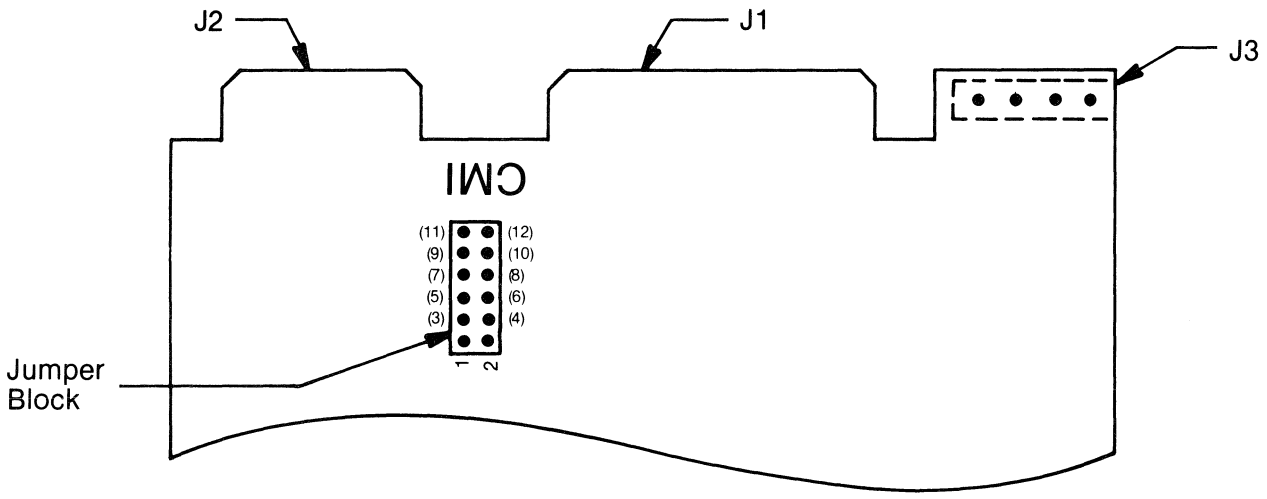


FIGURE 17

Function	Jumper Block Pin Numbers
Drive Select 0	1, 2
Drive Select 1	3, 4
Drive Select 2	5, 6
Drive Select 3	7, 8
Off-track Positioning (Option)	9, 10
Reserved	11, 12

TABLE VI

9.0 Schmetic Diagrams

The CM 5000 contains two PC Boards:

a) Main Control Board, and

b) Motor Control Board.

The schematic diagrams for the Main Control Board are shown in Drawings no 200210 (3 sheets). The schematic diagram for the Motor Control Board is shown in Drawing 200213.

The component locations for the two boards is shown in drawings 200317 and 200319.

10.0 Test Points

to be added.....

GLOSSARY

7201 MPSC. (NEC 7201 Multi-Protocol Serial Controller) The 7201 is a two-channel device used on the CPU Board for cluster and keyboard communications. See the 1981 Catalog published by NEC Microcomputers, Inc.

8086 Microprocessor. The Intel 8086 is a 16-bit microprocessor operating at 8.0 MHz on the 8086 CPU Board. The 8086 is software-compatible with Intel 8088 microprocessors. See the Component Data Catalog published by the Intel Corporation.

8088 Microprocessor. The 8088 is the workstation microprocessor on the 8088 CPU Board. The 8088 is software-compatible with the Intel 8086 family of microprocessors. The 8088 has an 8-bit data bus and requires two memory cycles to read or write a 16-bit word. See the Component Data Catalog published by the Intel Corporation.

8253 Counter/Timer. The 8253 is a three-channel programmable counter/timer chip manufactured by the Intel Corporation. The 8253 is used in the AWS-220, -230, and -240 to generate speaker tones, programmable interrupts, and the clock for cluster communications. See the Component Data Catalog published by the Intel Corporation.

8257 DMA Controller. See DMA and the Component Data Catalog published by the Intel Corporation.

8259A Interrupt Controller. The 8259A handles various peripheral interrupt devices on the FDC and HDC Boards. When one of devices needs to interrupt the CPU, the 8259A interrupts on the peripheral's behalf. During the interrupt acknowledge cycle from the CPU, the 8259A resolves the priority of other interrupting devices on the board and issues an interrupt vector to the CPU. Any interrupt input to the 8259A can be masked by software. See the Component Data Catalog, published by the Intel Corporation.

8272 Floppy Disk Controller. The 8272 is a floppy disk controller manufactured by the Intel Corporation. It contains much of the circuitry necessary to implement the floppy disk controller on the FDC Board for the AWS-220 and AWS-230 workstations. The 8272 on the FDC Board always

uses DMA Channel 0 to transfer data to and from the RAM array during a read or write operation. See the Component Data Catalog, published by the Intel Corporation.

8275 CRT Controller. The Intel 8275 CRT Controller is used as the controller for the video display control logic. The 8275 controls raster and cursor timing, row buffering, and special video attrubute decoding. The 8275 uses DMA Channels 2 and 3 to receive data from the RAM array. See the Component Data Catalog, published by the Intel Corporation.

8X36 Bidirectional Input/Output Ports. The HDC Board uses three 8X36 bidirectional input/output ports as status, command, and data ports, respectively, for the hard disk controller. The 8X36s receive data from the 8X300 microcontroller and send data to the 8X300 on the IV bus. See the 8X300 Design Guide, published by the Signetics Corporation.

8X300 Microcontroller. The Signetics 8X300 controls all of the floppy and hard disk fuctions on the HDC Board. The 8X300 operates from a microprogram stored in two on-board ROMs and communicates with its peripheral devices through the IV bus. Instructions from the CPU Board are sent through an 8X320 bus interface register array. See the 8X300 Design Guide, published by the Signetics Corporation.

8X320 Bus Interface Register Array. The Signetics 8X320 bus interface register array contains sixteen 16-bit registers for interfacing the 8X300 microcontroller to the HDC Board bus interface. See the 8X300 Design Guide, published by the Signetics Corporation.

8X330 Floppy Disk Controller. The Signetics 8X330 floppy disk controller contains all the circuitry necessary to control the floppy disk drive on the AWS-240. The 8X330 is controlled by the 8X300 microcontroller. See the 8X300 Design Guide, published by the Signetics Corporat-on.

AWS-220, -230, and -240. The AWS-220, -230, and -240 are hardware configurations in which the processor electronics, keyboard, and CRT monitor are all placed on the user's desktop. The AWS-220, -230, and -240 workstations each contain an 8086 or 8088 microprocessor and their own mass

storage peripherals. See the "Overview" section above.

Bootstrap ROM. The 4-kilobyte bootstrap ROM runs simple diagnostic tests and loads the CTOS System Image into the RAM array for the workstation upon either a manual or power-up reset.

Buffer. A buffer is an amplifying signal driver, not necessarily with memory capability. Buffers that provide temporary storage for data are called "storage buffers."

Bus. A bus is a collection of signal lines used by more than one device. In general, three types of buses make up a bus set (which is also referred to as a bus): the address bus, the data bus, and the control bus.

Bus Master. See Master.

Byte. A byte is 8 bits. Also see High-Order Byte and Low-Order Byte.

Character Cell. A character cell is the pixel matrix on the video display within which each character is formed. The workstation uses a 9-by-11-pixel matrix as a character cell. Also see Pixel.

Clear. A register is cleared when a logical 0 or series of 0s is written to that register. Also see Reset and Set.

Cluster Communications Logic. The cluster communications logic on the CPU Board allows the AWS-220, -230, and -240 to communicate with a master workstation on an RS-422, half-duplex communications channel at a transmission rate of 307 kilobaud. Channel A of the 7201, in conjunction with the 8257, is used for cluster communications

Cluster Configuration. A cluster is a hardware configuration in which cluster workstations are linked in a daisy chain to a master workstation.

CPU. The CPU used in the AWS-220, -230, and -240 is either an 8086 or an 8088 microprocessor located on the CPU Board.

CPU Board. The CPU Board used in the AWS-220, -230, and -240 contains all memory, along with

all microprocessor, communications, and video display control logic.

Direct Memory Access Logic. See DMA.

DMA. (Direct Memory Access) DMA allows a peripheral device to transfer data to or from memory without using the CPU. Three DMA channels are used in the AWS-220, -230, and -240, for cluster communications, video display refresh, and the FDC or HDC Board.

DMA Address. When the DMA channel is initialized for a transfer, the DMA address is the initial address in memory of the transfer. If the DMA address is read for status at any time, it is the current memory address of the transfer.

DMA Count. When the DMA channel is initialized for a transfer, the DMA count is the number of bytes to be transferred in the operation. If the DMA count is read for status at any time, it is the number of bytes remaining to be transferred.

Driver. See Buffer.

Execution Speed. The execution speed is the basic speed of the CPU, which is 5 MHz with one wait state for the 8088 and 8 MHz without wait states for the 8086. Also see Memory Cycle Time.

Expansion Interface. The expansion interface extends all signals necessary to operate the FDC or HDC Boards in the AWS-220, -230, and -240 workstations.

Font ROM. The font ROM is associated with the video display control logic on the CPU Board. It is used to store the 256 normal and line-drawing characters.

Half-Bit Shift. Half-bit shift is a video attribute that delays the illumination of a pixel row in a character cell by one-half pixel clock period to give smoother characters.

High-Order Byte. The high-order byte is the most significant byte in a word (bits 8h to Fh). The high-order byte is also called the odd byte since it always has an odd address in memory.

Interrupt Logic. The interrupt logic is used to interrupt the CPU. Interrupts are handled

internally by the 7201. The only noncommunications interrupt source is Counter 2 of the 8253, which is used to generate general purpose interrupts for software.

Invisible Attribute Mode. The invisible attribute mode allows the video attribute characters stored in the video map to remain invisible on the video display. See Video Map and Video Attribute Characters.

IV Bus. The IV (Instruction Vector) bus is the bus for the 8X300 microcontroller on the HDC Board. The 8X300 uses the IV bus to transfer data from and to peripheral devices, such as the 8X320 bus interface register array, the 8X330 floppy disk controller, and the three 8X36 bidirectional input/output ports on the HDC Board.

Keyboard Interface Logic. The keyboard interface logic on the CPU Board contains a serial communications channel and clock for communications with the keyboard's 8048 single-chip microcomputer.

LA Bus. See Line Address Bus.

Line Address Bus. The line address bus is a 20-bit bus on the CPU Board consisting of signal lines LA0+-LA13+.

Low-Order Byte. The low-order byte is the least significant byte in a word (bits 0h to 7h). The low-order byte is also called the even byte since it always has an even address in memory.

Manual Reset. A manual reset is a system reset brought about by the user pressing the reset button on the rear panel of the AWS-220, -230, or -240. Also see Reset.

Master. A master is a device that controls the data and address buses. The two bus masters in the workstations are the 8088 or 8086, and the 8257.

Master Workstation. A master workstation is used in a cluster configuration to control access to shared resources.

Memory Cycle Time. The memory read or write cycle time is 1 μs, which is the time to read or write 1 byte with one wait state in the cycle.

MFM. MFM (Modified Frequency Modulation) is a data encoding scheme used on the AWS-220 and AWS-230 FDC Board to store double-density data on a floppy disk. The basic rules for MFM encoding are as follows. Write data bits are at the center of a bit cell and write clock bits are at the beginning of a bit cell if: (1) there is no data bit written in the previous bit cell, and (2) there will be no data bit written in the current cell. See 8X330 Floppy Disk Controller, published by the Signetics Corporation.

Minimum Mode (8086 or 8088). The 8086 or 8088 used in the AWS-220, -230, and -240 is wired to operate in the minimum mode, which makes the microprocessor's control lines perform in a manner similar to those of an Intel 8085.

MPSC. Multi-Protocol Serial Controller. See 7201.

Multidrop. Multidrop is a data communications technique in which several devices share the same signal lines.

Nonmaskable Interrupt. A nonmaskable interrupt is caused by a parity error. When it occurs, the CPU branches to the address contained in locations 8h, 9h, Ah, and Bh, which is the address of a recovery software routine.

Parity Bit. A parity bit is stored along with every data byte in memory as a ninth bit. The AWS-220, -230, and -240 use an even parity error checking system. When a byte with an odd number of 1 bits is stored in a memory location, a 1 is stored as the parity bit. Accordingly, when a byte is stored with an even number of 1 bits, a 0 is stored as the parity bit.

Parity Error Register. The parity error register is the 20-bit register at Ports E0h, E4h, and E8h on the CPU Board. This register latches the address at which a RAM parity error occurred and indicates whether DMA was active at the time of the error.

Pipelining. Pipelining is a technique for increasing the available access time by

synchronizing information to and from a logic element. An example of pipelining is when an address into a memory is synchronized with the time requirement for the data out of memory.

Pixel. A pixel is the smallest addressable picture element on the video display. The AWS-220, -230, and -240 use a 9-by-11-pixel matrix to form a character. Also see Character Cell.

Port. A port is an input/output address, usually containing (if a status port) or requiring (if a command port) specific data, such as the DMA Control/Status Register at Port 8h. A port can allow access to several registers (see Register).

Power-up Reset. A power-up reset is an automatic system reset ocurring when the power is turned on. Also see Reset.

RAM. (Random Access Memory) The RAM in the AWS-220, 230, and -240 is made up of 64-kilobit (kb) dynamic RAM chips. Up to eight banks of nine 64-kb RAMs can be installed on the CPU Board for a total RAM capacity of 512 kilobytes.

Register. A register is a temporary memory location for data, such as Register AL of the 8088 or 8086.

Reset. A reset can be either a system reset, as defined by the reset pin functions of the various chips connected to the system reset function, or a software register reset, equivalent to a clear. Also see Power-up Reset and Manual Reset.

ROM. (Read Only Memory) A ROM refers to either a ROM or PROM (Programmable ROM). Several ROMs are used in the AWS-220, -230, and -240 workstations for the font ROM, and for bootstrap ROMs on the CPU and FDC or HDC Boards.

Set. To set is to write a logical 1 or series of 1s to a register. Also see Clear.

Storage Buffer. A storage buffer is a buffer with storage, such as a flip-flop, latch, or register.

Video Attribute Character. A video attribute character specifies certain visual qualities of the video display characters, such as underline, reverse video, or blinking.

Video Display Control Logic. The video display control logic on the CPU Board controls video generation.

Video Map. The video map is the area in the workstation's RAM array where video display information is stored and refreshed.

Wait State. A wait state is a temporary suspension of an input/output or memory cycle. It is used when an input/output or memory device operates at a speed slower than that of the CPU. Wait states are generated for every input/output or memory cycle the 8088 CPU performs. Wait states are not added to 8086 RAM read or write cycles.

Word. A word is 16 bits or 2 bytes.

USER'S COMMENT SHEET

AWS-220, -230, -240 Hardware Manual
EW-220 Volume 2: A-09-00112-01-A

We welcome your comments and suggestions. They help us improve our manuals. Please give specific page and paragraph references whenever possible.

Does this manual provide the information you need? Is it at the right level? What other types of manuals are needed?

Is this manual written clearly? What is unclear?

Is the format of this manual convenient in arrangement, in size?

Is this manual accurate? What is inaccurate?

Name_____ Date_____
Title_____ Phone_____
Company Name/Department_____
Address_____
City_____ State_____ Zip Code_____

☐ Please check here if you'd like a reply.

Thank you.
All comments become the property of Convergent Technologies, Inc.

Seal or tape for mailing - do not use staples

fold

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 1309 SANTA CLARA, CA.

POSTAGE WILL BE PAID BY -

Convergent Technologies™
2500 Augustine Drive
Santa Clara, Ca. 95051

ATTN: TECHNICAL PUBLICATIONS

fold

cut along here

USER'S COMMENT SHEET

AWS-220, -230, -240 Hardware Manual
EW-220 Volume 2: A-09-00112-01-A

We welcome your comments and suggestions. They help us improve our manuals. Please give specific page and paragraph references whenever possible.

Does this manual provide the information you need? Is it at the right level? What other types of manuals are needed?

Is this manual written clearly? What is unclear?

Is the format of this manual convenient in arrangement, in size?

Is this manual accurate? What is inaccurate?

Name_____ Date_____
Title_____ Phone_____
Company Name/Department_____
Address_____
City_____ State_____ Zip Code_____

☐ Please check here if you'd like a reply.

Thank you.
All comments become the property of Convergent Technologies, Inc.

Seal or tape for mailing - do not use staples

fold

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 1309 SANTA CLARA, CA.

POSTAGE WILL BE PAID BY -

Convergent Technologies™
2500 Augustine Drive
Santa Clara, Ca. 95051

ATTN: TECHNICAL PUBLICATIONS

fold

cut along here

USER'S COMMENT SHEET

AWS-220, -230, -240 Hardware Manual
EW-220 Volume 2: A-09-00112-01-A

We welcome your comments and suggestions. They help us improve our manuals. Please give specific page and paragraph references whenever possible.

Does this manual provide the information you need? Is it at the right level? What other types of manuals are needed?

Is this manual written clearly? What is unclear?

Is the format of this manual convenient in arrangement, in size?

Is this manual accurate? What is inaccurate?

Name_____ Date_____
Title_____ Phone_____
Company Name/Department_____
Address_____
City_____ State_____ Zip Code_____

☐ Please check here if you'd like a reply.

Thank you.
All comments become the property of Convergent Technologies, Inc.

Seal or tape for mailing - do not use staples

fold

NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES

BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 1309 SANTA CLARA, CA.

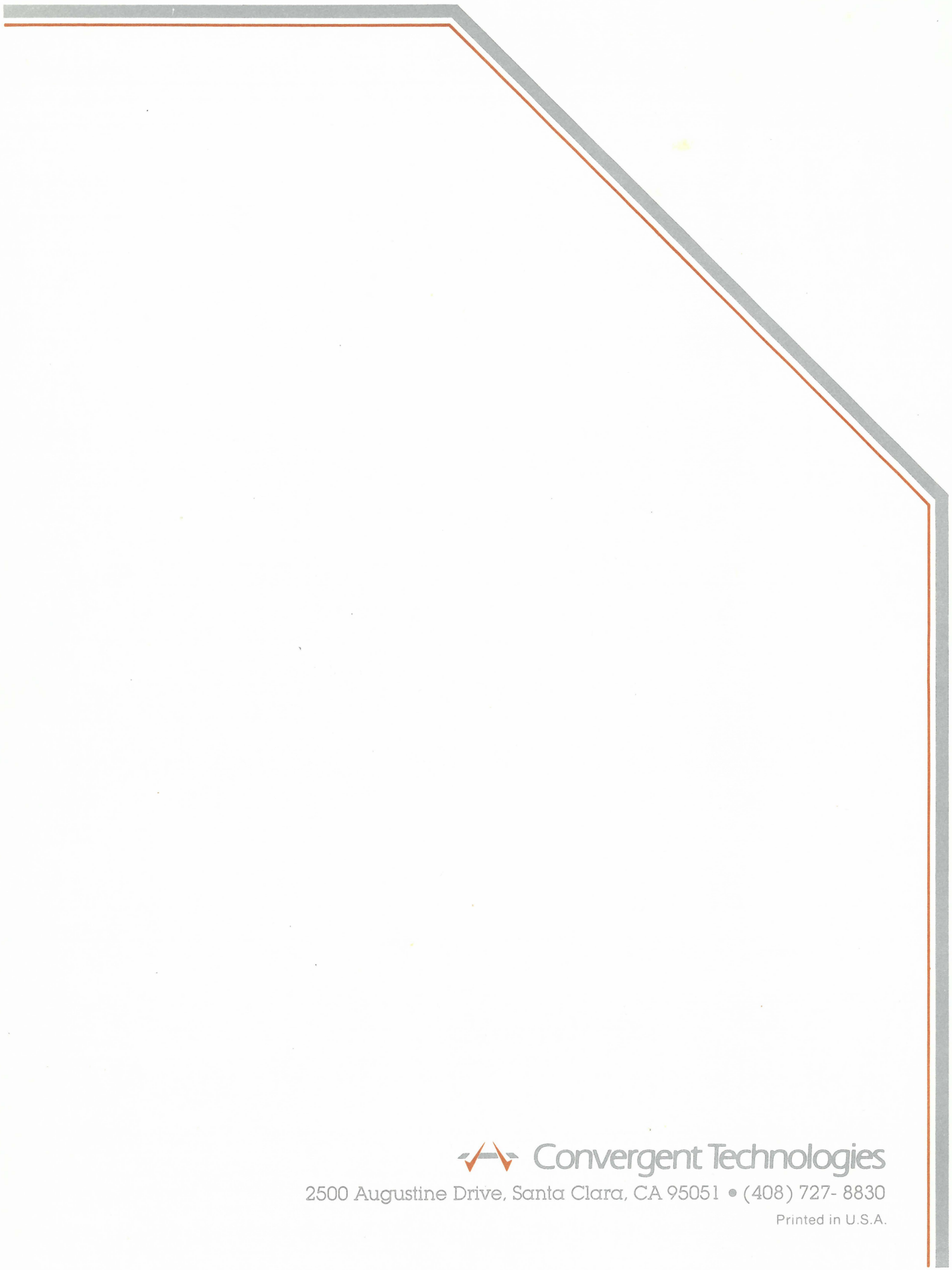
POSTAGE WILL BE PAID BY -

Convergent Technologies™
2500 Augustine Drive
Santa Clara, Ca. 95051

ATTN: TECHNICAL PUBLICATIONS

fold

cut along here



Convergent Technologies
2500 Augustine Drive, Santa Clara, CA 95051 • (408) 727- 8830
Printed in U.S.A.