FLOPPY/HARD DISK MANUAL

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This manual is one of a set that documents the Convergent™ Family of Information Processing Systems. The set can be grouped as follows:

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This section outlines the contents of these manuals.

INTRODUCTORY

The Installation Guide describes the procedure for unpacking, cabling, and powering up a system.

The Operator's Guide addresses the needs of the average user for operating instructions. It describes the workstation switches and controls, keyboard function, and floppy disk handling.

The Executive Manual describes the command interpreter, the program that first interacts with the user when the system is turned on. It describes available commands and discusses command execution, file management, program invocation, and system management. It also addresses status inquiry, volume management, the printer spooler, and execution of batch jobs. This manual now incorporates the System Utilities and Batch Manuals.

The Context Manager Manual describes and teaches the use of the Context Manager, which allows the user to run applications concurrently and interchange them on the screen almost instantly.

The Status Codes Manual contains complete listings of all status codes, bootstrap ROM error codes, and CTOS initialization codes. The codes are listed numerically along with any message and an explanation.

The NGEN Installation Guide describes the procedure for unpacking, assembling, cabling, and powering up an NGEN workstation.

The NGEN Operator's Guide is a link between the operator, the NGEN workstation, and the workstation's documentation. The Operator's Guide describes the operator controls and the use of the floppy disk drives, as well as how to verify that the workstation is operational and how to use software release notices.

HARDWARE

NGEN

The Processor Manual: Model CP-001 describes the Processor Module, which houses the Processor board, Memory board, I/O board, Video/Keyboard board, and Motherboard. It details the architecture and theory of operations of the printed circuit boards, external interfaces, and the Memory Expansion Cartridge, as well as the X-Bus specifications.

The Dual Floppy Disk Manual and the Floppy/Hard Disk Manual describe the architecture and theory of operation for the NGEN modules. They discuss the respective disk drives and controllers, and contain the applicable OEM disk drive manuals.

The Diagnostics Manual describes the diagnostics available for the NGEN workstation. It discusses the Processor Module's bootstrap ROM program and error codes, and individual software diagnostics for modules in the workstation.

The Keyboard Manual describes the theory of operation for the NGEN keyboard.

The Power System Manual describes the operation and connections for the 36-Volt Power Supply and the dc/dc converters used with the NGEN workstation.

The Monochrome Monitor Manual: Model VM-001 describes the operation and connections of the 12-inch Monochrome Monitor used with the NGEN workstation.

The Color Monitor Manual describes the operation and connections of the 15-inch Color Monitor used with the NGEN workstation.

IWS

The Workstation Hardware Manual describes the mainframe, keyboard, and video display for the IWS family of workstations. It specifies system architecture, printed circuit boards (Motherboard, Processor, I/O Memory, Multiline Communications Processor, Video Control, Graphics Control Board, ROM and RAM Expansions), keyboard, video monitor, Multibus interface, communications interfaces, power supply, and environmental characteristics of the workstation.

The Peripherals Hardware Manual describes the non-SMD single-board Mass Storage Subsystem (MSS) and Mass Storage Expansion (MSX) disk subsystems for the IWS family of workstations. It contains descriptions of the disk controller Motherboard, the two controller boards for floppy and Winchester disks, power supplies, disk drives, and environmental characteristics.

The IWS Peripherals Hardware Manual (SMD Version) describes the SMD MSS and MSX disk subsystems having one controller board.

AWS

The AWS-210 Hardware Manual describes the mainframe, keyboard, and video display of the AWS-210 workstation. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, and CPU), keyboard, video monitor, expansion interface, cluster communications interface, power supply, and environmental characteristics of the workstation.

The AWS-220, -230, -240 Hardware Manual describes the mainframe, keyboard, disk controllers, and video display of the AWS-220, -230, and -240 workstations. It specifies architecture, theory of operation of the printed circuit boards (Motherboard, Deflection, 8088 CPU, 8086 CPU, Floppy Disk Controller, and Hard Disk Controller), keyboard, video monitor, cluster communications interface, external interfaces, power supply, and environmental characteristics of the workstation.

The AWS Color Workstation Hardware Manual describes the mainframe, keyboard, and color video display of the AWS Color Workstation. This manual reports the architecture and theory of operation of the printed circuit boards (Motherboard, Graphics Control Board, Hard Disk Controller, Color Video, Color Deflection, and CPU), keyboard, color monitor, peripheral interfaces, cluster communications interface, power supply, and environmental characteristics of the workstation. This manual also contains four OEM disk drive manuals and a summary of adjustments for the color monitor.

OPERATING SYSTEM

The CTOS™ Operating System Manual describes the operating system. It specifies services for managing processes, messages, memory, exchanges, tasks, video, disk, keyboard, printer, timer, communications, and files. In particular, it specifies the standard file access methods: SAM, the sequential access method; RSAM, the record sequential access method; and DAM, the direct access method.

The System Programmer's Guide addresses the needs of the system programmer or system manager for detailed information on operating system structure and system operation. It describes (1) cluster architecture and operation, (2) procedures for building a customized operating system, and (3) diagnostics.

GUEST OPERATING SYSTEMS

The CP/M-86™ and MS™-DOS Manuals describe the single-user operating systems originally designed for the 8086-based personal computer systems.

The GW™-BASIC Manuals describe the version of BASIC that runs on the MS™-DOS operating system.

The XENIX™ Manuals describe the 16-bit adaptation of the UNIX system, including the XENIX environment for software development and text processing.

PROGRAMMING LANGUAGES

The COBOL, FORTRAN, FORTRAN-86, BASIC (Interpreter), BASIC Compiler, PASCAL, and Assembly Language Manuals describe the system's programming languages. Each manual specifies both the language itself and also operating instructions for that language.

The Pascal Manual is supplemented by a popular text, Pascal User Manual and Report.

The Assembly Language Manual is supplemented by a text, the Central Processing Unit, which describes the main processor, the 8086. It specifies the machine architecture, instruction set, and programming at the symbolic instruction level.

PROGRAM DEVELOPMENT TOOLS

The COBOL Animator describes the COBOL Animator, a debugger that allows the user to interact directly with the COBOL source code during program execution.

The Editor Manual describes the text editor.

The Debugger Manual describes the Debugger, which is designed for use at the symbolic instruction level. It can be used in debugging FORTRAN, Pascal, and assembly-language programs. (COBOL and BASIC, in contrast, are more conveniently debugged using special facilities described in their respective manuals.)

The Linker/Librarian Manual describes the Linker, which links together separately compiled object files, and the Librarian, which builds and manages libraries of object modules.

DATA MANAGEMENT FACILITIES

The CT-DBMS™ Manual describes Convergent's data base management system (CT-DBMS), which consists of (1) a data manipulation language for accessing and manipulating the data base and (2) utilities for administering the data base activities such as maintenance, backup and recovery, and status reporting.

The ISAM Manual describes both the single- and the multiuser indexed sequential access method. It specifies the procedural interfaces (and how to call them from various languages) and the utilities.

The Forms Manual describes the Forms facility that includes (1) the Forms Editor, which is used to interactively design and edit forms, and (2) the Forms run time, which is called from an application program to display forms and accept user input.

The Sort/Merge Manual describes (1) the Sort and Merge utilities that run as a subsystem invoked at the Executive command level, and (2) the Sort/Merge object modules that can be called from an application program.

TEXT MANAGEMENT FACILITIES

The Word Processing User's Guide introduces the Word Processor to the first-time user. It provides step-by-step lessons that describe basic word processing operations. The lessons show how to execute operations and apply them to sample text.

The Word Processing Reference Manual is a reference tool for users already familiar with the Word Processor. It describes the Word Processor keyboard and screen; basic, advanced, and programmer-specific operations; list processing; printer and print wheel configurations; and hardware considerations.

The Word Processing Quick Reference provides a concise summary of all word processing operations and briefly describes the keyboard and commands.

APPLICATIONS FACILITIES

The Project Planner schedules and analyzes tasks, milestones, and the allocation of resources in a project. By means of diagrams and several kinds of bar charts, Project Planner presents time and resource allocation results and shows the occurrence of project milestones. The Project Planner Manual explains the use of the program and also serves as a reference once the user is familiar with it.

The CT-MAIL™ User's Reference Manual introduces the first-time user to the CT-MAIL electronic mail system. It provides step-by-step instructions for using the basic CT-MAIL operations to create, send, and receive mail.

The CT-MAIL™ Administrator's Reference Manual provides the System Administrator with instructions for installing, configuring, and maintaining the CT-MAIL electronic mail system; setting up communication lines; creating and maintaining mail centers; adding mail users; creating distribution lists; and troubleshooting.

Multiplan is a financial modeling package designed for business planning, analysis, budgeting, and forecasting.

The Business Graphics User's Guide introduces Business Graphics to the first-time user. It provides step-by-step lessons that describe basic Business Graphics operations. The lessons show how to execute operations and apply them to sample charts.

The Business Graphics Reference Manual is a reference tool for users already familiar with Business Graphics. It describes the Business Graphics keyboard and screen; box and arrow cursor movement; obtaining information from Multiplan; operations; and plotter configurations.

The Graphics Programmer's Guide is a reference for applications and systems programmers. It describes the graphics library procedures that can be called from application systems to generate graphic representations of data, and it includes a section on accessing Business Graphics from an application system.

The Font Designer Manual describes the interactive utility for designing new fonts (character sets) for the video display.

COMMUNICATIONS

The Asynchronous Terminal Emulator Manual describes the asynchronous terminal emulator.

The 3270 Terminal Emulator Manual describes the 3270 emulator package.

The 2780/3780 RJE Terminal Emulator Manual describes the 2780/3780 emulator package.

The SNA Network Gateway Manual describes the SNA Network Gateway, which supports data communications over an SNA network. The SNA Network Gateway comprises the Transport Service and Status Monitor. The Transport Service allows a Convergent workstation to function as cluster controller and forms the foundation for Convergent SNA products.

The SNA 3270 Emulator Manual describes the SNA 3270 emulator package. The SNA 3270 emulator provides CRT and printer subsystems in addition to a Virtual Terminal Interface for use in application programs.

The X.25 Network Gateway Manual describes the X.25 Network Gateway, which supports CCITT Recommendation X.25 communications over a public data network. There are three levels of access to the network: packet, X.25 sequential access method,

and the Multimode Terminal Emulator X.25 communications option.

The Multimode Terminal Emulator User's Guide introduces the Multimode Terminal Emulator to the first-time user. It describes the MTE video display, keyboard, display memory, and advanced operations for the X.25 communications option.

The Multimode Terminal Emulator Reference Manual is a reference tool for sophisticated users of the Multimode Terminal Emulator. It describes the MTE escape sequences and field verification program.

REFERENCES

The boards that make up the Floppy/Hard Disk Module are heavily dependent upon programmable large-scale integration (LSI) circuitry to perform their functions. Since hardware functions and software interfaces of the LSI circuitry are only summarized in this manual, users can find additional information in the following manufacturers' literature:

- Intel Component Data Catalog
- Intel Microprocessor and Peripheral Handbook
- Western Digital Corp. WD1Ø1Ø Winchester Disk Controller data sheet
- Western Digital Corp. WD279X-Ø2 Floppy Disk Formatter/Controller Family data sheet
- Western Digital Corp. 1983 Components Handbook

CONVENTIONS

NUMBERS

Numbers used in this manual are written in decimal unless suffixed with "h" for hexadecimal. For example, 1Øh = 16 and ØFFh = 255.

SIGNAL NAMES

Signal names used in this manual are suffixed with plus (+) and minus (-) to distinguish active-high from active-low, respectively. An example of a RD (Read) signal is as follows:

Signal Name	Logical State	Voltage Level
RD-	Ø (active)	Low
	1 (inactive)	High
RD+	Ø (inactive)	Low
	1 (active)	High

1 OVERVIEW

INTRODUCTION TO THE WORKSTATION

The workstation is composed of modules that provide data storage and processing functions. Depending on its configuration, the workstation will run application software as a standalone workstation, as a master workstation providing facilities for several cluster workstations, or as a cluster workstation.

In its most basic form, a workstation with Processor Module, Keyboard, and Monitor can run a software application as a cluster workstation. This configuration uses disk space on a cluster master to call up software applications and files. If disk storage is added, a workstation can store its own software applications and files. In this configuration, the workstation operates either as a standalone or provides disk storage services to cluster workstations as a cluster master.

Other modules, such as different or additional displays, processors, storage modules, communications modules, or keyboards, can be added to (or easily removed from) the workstation as processing needs change.

Since the workstation is modular, separate manuals provide details about logic, operation, and interface for the various modules of the system. The "Guide to Technical Documentation" in the front of this manual provides the complete list of manuals.

An explanation of the system capabilities and the system bus, designated as the X-Bus, is found in the Processor Manual for the system.

In this manual, the term "X-Bus master" is used to denote any device or module capable of accessing control of the X-Bus data, address, and control lines.

In sections describing the assignment of I/O base addresses, the term "Processor Module" is used. The Processor Module, itself an X-Bus master, is the only X-Bus master capable of assigning I/O base addresses to X-Bus modules during power-up reset, manual reset, or under software control.

INTRODUCTION TO THE MANUAL

This manual is written for the engineer who tests or services the Floppy/Hard Disk Module electronics or who writes or modifies system software for use with the workstation. This manual does not, however, support modifications to existing hardware. The manual is divided into the following sections:

- Overview
- Architecture
- Theory of Operation
- Hard Disk Expansion

The "Overview" describes the capabilities of the Floppy/Hard Disk Module, as well as the major components that make up the Floppy/Hard Disk Module.

The second section, "Architecture," covers the floppy/hard disk controllers in terms of their applicable software interface to hardware components. Applicable command and status registers for the controllers, as well as other components, are defined. In addition, the X-Bus identification scheme is summarized.

Section 3, "Theory of Operation" details the component-level circuit descriptions of the Floppy/Hard Disk Module. In addition, an interconnect wire list is provided.

The subsection "Hard Disk Expansion," provides an interconnection wire list for a Hard Disk Expansion Module. In addition, module specifications and OEM manuals are provided in appendixes.

GENERAL DESCRIPTION

The Floppy/Hard Disk Module, shown in Figure 1-1, consists of a single modular assembly and contains the circuitry necessary to provide 630K bytes of storage in one half-height 5.25-in. floppy disk drive and 5 or 10M bytes of storage in one half-height 5.25-in. hard disk drive.

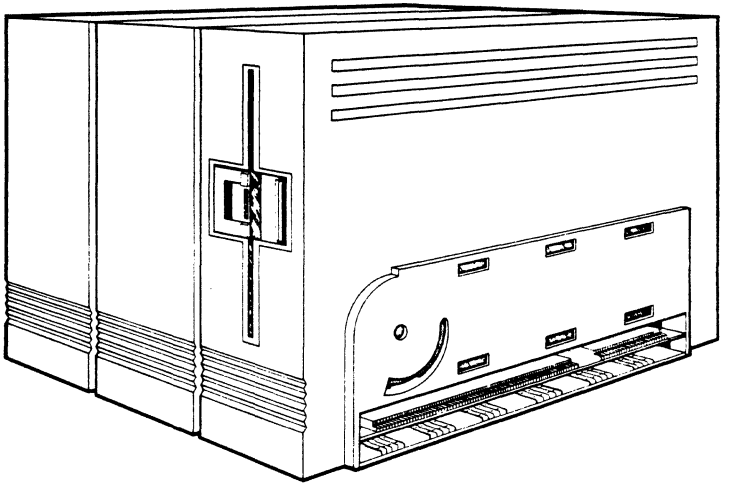


Figure 1-1. Floppy/Hard Disk Module.

The Floppy/Hard Disk Module is connected through the X-Bus to a controlling module called an X-Bus master. For detailed information about the X-Bus, refer to the Processor Manual for the system.

FLOPPY DISK

The floppy disk drive stores 630K bytes of information using double-sided media qualified for double-density storage of data. The drive uses the Modified Frequency Modulation (MFM) form of data encoding. A manufacturer's manual for the floppy disk drive is included in Appendix B.

The floppy disk circuitry uses a 40-pin Western Digital WD2797-02 floppy disk formatter/controller, which contains most of the logic necessary to control the floppy disk drive, including a phase-locked loop data separator, write precompensation circuitry, and cyclic redundancy checking (CRC) circuitry. In addition, an 8253 programmable interval timer supplements the WD2797-02.

HARD DISK

The hard disk drive stores 5M or 10M bytes of information using Winchester technology. The drive uses the MFM form of data encoding.

The hard disk circuitry uses a 40-pin Western Digital WD1010 Winchester disk controller, which is used with an external 8K byte RAM data buffer. In addition, one 6331-1 PROM, two 8253 programmable interval timer chips, two 16L8 programmable array logic (PAL) chips, and phase-locked loop data separator circuitry supplement the WD1010.

MAJOR COMPONENTS

The major components of the Floppy/Hard Disk Module include the following:

- the enclosure, which houses the drives, controllers, and X-Bus interface
- the motherboard, which lies against the bottom of the enclosure
- the Controller board, which is mounted vertically along the left side of the enclosure
- two dc/dc power converters that plug into the motherboard, one supplying +12 Vdc and one supplying +5 Vdc
- one half-height floppy disk drive mounted vertically in the enclosure
- one half-height hard disk drive mounted vertically in the enclosure

Major components used for floppy disk control logic, which are resident on the Controller board, include the following:

- one WD2797-Ø2 floppy disk formatter/controller
- one programmable interval timer (also used for the hard disk drive)

Major components used for hard disk control logic are resident on the Controller board and include the following:

- one WD1Ø1Ø Winchester disk controller
- two 8253 programmable interval timers (one of which is also used for the floppy disk controller)
- one 6331-1 PROM
- two PAL chips
- four 2K by 8 bits (2K-byte) RAM chips
- one 4K by 8 bits (4K-byte) 2732 EPROM
- one MC4Ø44 phase-frequency detector
- one 74S124 voltage-controlled oscillator

2 ARCHITECTURE

INTRODUCTION

This section provides information for the systems programmer who needs to understand the Floppy/Hard Disk Module hardware at a functional block level and who must program the large-scale integration (LSI) devices within the Floppy/Hard Disk Module.

A functional logic block diagram is shown in Figure 2-1. Each block is described in this section in relation to the programmable LSI device or devices performing the applicable function in the workstation. Each subsection describes the nature of the function and how it is implemented. In addition, specific status and command registers are examined.

The following subjects are detailed:

- X-Bus interface
- floppy disk controller
- floppy disk command and status registers
- floppy disk formatting
- hard disk controller
- hard disk command and status registers
- hard disk formatting
- programmable array logic
- module base input/output (I/O) addressing
- module I/O address summary

X-BUS INTERFACE

The I/O ports on the Floppy/Hard Disk Module are partially defined by the module base I/O address issued by the Processor Module. For example, the floppy disk Data register resides at port XXØ6h, where XX is the module address and Ø6h is the register address. Upon either a power-up or manual reset, the bootstrap ROM program in the Processor Module assigns a unique address to each module that is physically attached to the X-Bus. The operating system also has the ability to change module addresses at any time. Procedures used to change the module address through the operating system are included in the "Module Base I/O Address Summary" subsection at the end of this section. In addition, a summary of I/O register addresses used with the Floppy/Hard Disk Module is provided in the "Module I/O Address Summary" subsection.

MODULE IDENTIFICATION

A power-up, manual reset, or any I/O operation to port ØF98Øh resets all X-Bus modules, except the Processor Module. Only the module immediately to the right of the Processor Module is enabled. This module identifies itself by placing a type/state word on the data bus when port Ø is read by the Processor Module. (To reset the X-Bus modules via port ØF98Øh, see the "Panel Debugger" subsection, below.)

The Processor Module writes to port Ø a base I/O address that corresponds to a register in the module (for example, the Floppy/Hard Disk Module) and defines the range of I/O addresses reserved for its use. Writing to port Ø also causes the module to reenable the X-Bus connection to the next module and to ignore subsequent reads and writes to and from port Ø. This allows the Processor Module to repeat the process for each module, beginning at the module adjacent to the Processor Module and repeating the process for each module to the right.

A ready time-out, signaled by a nonmaskable interrupt (NMI) when accessing port Ø, signifies that no additional modules are available.

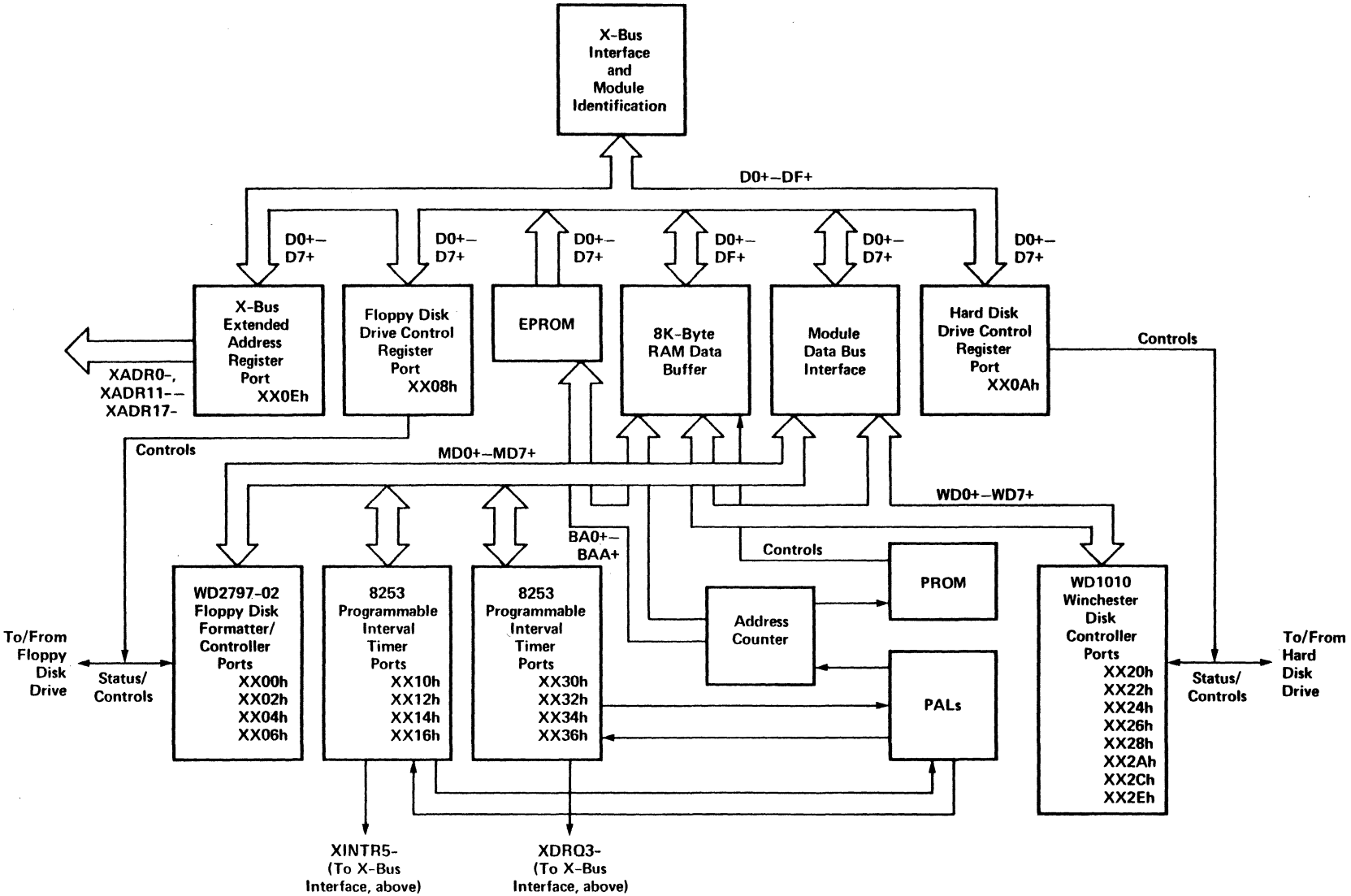


Figure 2-1. Floppy/Hard Disk Module Functional Logic Block Diagram.

IMPLEMENTATION

The module identification scheme is implemented by hardware as follows:

- All modules on the X-Bus are assigned an input signal line (XPIN) and are required to generate an output signal line (XPOUT). The input signal will always enter a module on the module's left side, and the output signal will always exit the module on the module's right side.

- During power up, all modules reset an internal flip-flop to drive XPOUT low.

- The XPIN line of the module closest to the Processor Module is controlled by the Processor Module; when XPIN is low, the I/O register clears.

- When a module's XPIN is high and its XPOUT is low, the base I/O address is zero.

- The Processor Module reads port Ø to identify the peripheral (in this case, the Floppy/Hard Disk Module) and then writes a byte to the low-order eight bits of the data bus, which become the high-order eight bits of the device's I/O address range (256-byte ports or 128-word ports). This write also enables the XPOUT line in the module, which allows the next module on the right to undergo the same operation.

So that 8-bit devices are not required to scan the high-order byte of a port, the base I/O address is written to the low-order byte of port Ø. This corresponds to the high-order byte of the 16-bit base address, and defines a range of up to 256 port addresses reserved for that module's use.

The Processor Module is always referred to as module Ø, and the first module to the right of the Processor Module is referred to as module 1, and so on. The bootstrap ROM always writes this module number to the low byte of port Ø when it performs the identification polling sequence. Therefore, the module to the right of the Processor Module uses I/O ports Ø1ØØh through Ø1FFh, the next module to the right uses ports Ø2ØØh through Ø2FFh, and so on, depending on how

many modules are used. The bootstrap ROM also builds an array of the module type/state words returned by each module and stores this table in memory for the system.

FLOPPY DISK CONTROLLER

The Western Digital WD2797-Ø2 floppy disk formatter/controller performs the following four basic types of disk commands:

- Control commands (Type 1 commands) include movement of the read/write head to a specified track on the floppy disk (seeks), track jumping (steps), and track Ø recalibration or restoration. Control commands never involve a data transfer.

- Read/write commands (Type 2 and Type 3 commands) include sector or entire track data transfers. The controller can also read the identification information from a floppy disk sector.

- The Force Interrupt command (Type 4 command) is issued by the X-Bus master to terminate a multiple-sector read/write command or to ensure controller operation after a control operation.

For control and read/write commands, the X-Bus master addresses the WD2797-Ø2 through the X-Bus address bus and then issues the command to the WD2797-Ø2 on the XDATØ- through XDAT7- (X-Bus Data Bus) lines. Depending on the command, other registers, such as the Track register and the Sector register, may be loaded with the appropriate information. Immediately after the WD2797-Ø2 receives the command, it sets the Busy (controller busy) bit in the Status register (that is, bit Ø at port XXØØh) and executes the command. With the exception of the Force Interrupt command (below), the X-Bus master should not attempt to write to any register in the WD2797-Ø2 when the Busy bit is set. When a command is finished, the WD2797-Ø2 interrupts the X-Bus master, using the XINTR5- (X-Bus Interrupt, Priority 5) line.

When the Read Sector command is issued, the WD2797-Ø2 begins reading the specified sector and assembles the first byte read in the Data register. Simultaneously, the WD2797-Ø2 sets the DRQ+ (Data Request) bit in the Status register (that is, bit 1 at port XXØØh) and also sends DRQ+ back to the X-Bus master as XDRQ4- (X-Bus Data Request, Priority 4). The X-Bus master reads the WD2797-Ø2 Data register at address XXØ6h for the

byte. The WD2797-Ø2 continues to assemble bytes in the Data register and requests service from the X-Bus master. When the last byte is read from the Data register in the WD2797-Ø2, the 8253 programmable interval timer circuit sets the XINTR5- line to the X-Bus master. The X-Bus master responds with a Force Interrupt command to the WD2797-Ø2 to stop execution of the read command.

A Write Sector command executes in the same manner.

Under software control, two counters of the 8253 supplement the operation of the WD2797-Ø2 when a read or write command is issued. During such commands, the WD2797-Ø2 cannot terminate the command and request an X-Bus interrupt until it senses that five index marks have been detected. It takes about 1ØØØ milliseconds for the floppy disk to make five revolutions, and the 8253 issues the interrupt as soon as counters Ø and 1 time out.

Before loading the command in the WD2797-Ø2, the X-Bus master loads two counters in the 8253. Counter Ø is loaded with the total byte count, minus 2, of the transfer and is clocked every time the X-Bus master addresses the Data register. Counter 1 is loaded with a number to count an interval of about 14Ø microseconds so the WD2797-Ø2 can compute the two CRC bytes in case a read error has occurred in the last sector. Counter 1 is clocked by a 1-MHz oscillator. The logic is arranged so that both counters must time out before an interrupt request is issued to the X-Bus master.

When the X-Bus master senses the interrupt after a multiple-sector read operation, it sends the Force Interrupt command to the WD2797-Ø2. This command, which can be loaded into the WD2797-Ø2 Command register at any time, terminates any command in progress. Several flag bits in the Force Interrupt command byte can be set to specify the WD2797-Ø2 command interrupt conditions. (See the subsection, "Floppy Disk Drive Command and Status Registers," below.)

FLOPPY DISK DRIVE COMMAND AND STATUS REGISTERS

The Command and Status registers that affect the floppy disk formatter/controller in the Floppy/Hard Disk Module are as follows:

Address (h)	Function	Access
XX00	Status register	R
XX00	Command register	W
XX02	Track register	R/W
XX04	Sector register	R/W
XX06	Data register	R/W
XX08	Floppy Disk Drive Control register	W
XX10	Read counter 0	R
XX10	Load counter 0	W
XX12	Read counter 1	R
XX12	Load counter 1	W
XX16	8253 Mode Control word (also used for hard disk control)	W

STATUS AND COMMAND REGISTERS (PORT XX00h)

The read-only Status and write-only Command registers for the WD2797-02 can be accessed at port XX00h. The WD2797-02 accepts, one at a time, a total of 11 commands. (See Tables 2-1 and 2-2.) Command words should only be loaded into port XX00h when bit 0 of the Status register, the Busy bit, is 0. (See Table 2-3.) The only exception is the Force Interrupt command, which can be loaded into the Command register at any time. When one of these 11 commands is being executed, the Busy bit in the Status register is set. When a command is completed, an interrupt to the X-Bus master is generated, and the Busy bit is reset. The Status register indicates whether the just-completed command encountered an error or was fault-free. The Status register bits are summarized in Table 2-3.

Table 2-1. Floppy Disk Controller Command Summary.

Type	Command*	7	6	5	4	3	2	1	Ø
1	Restore	Ø	Ø	Ø	Ø	H	V	R1	RØ
1	Seek	Ø	Ø	Ø	1	H	V	R1	RØ
1	Step	Ø	Ø	1	T	H	V	R1	RØ
1	Step-In	Ø	1	Ø	T	H	V	R1	RØ
1	Step-Out	Ø	1	1	T	H	V	R1	RØ
2	Read Sector	1	Ø	Ø	M	L	E	U	Ø
2	Write Sector	1	Ø	1	M	L	E	U	AØ
3	Read Address	1	1	Ø	Ø	Ø	E	U	Ø
3	Read Track	1	1	1	Ø	Ø	E	U	Ø
3	Write Track	1	1	1	1	Ø	E	U	Ø
4	Force Interrupt	1	1	Ø	1	I3	I2	I1	IØ

*Refer to Table 2-2 for a description of the command parameters in this table

Table 2-2. Floppy Disk Controller Flag Summary. (Page 1 of 2)

Command Type	Flag/Description	Suggested Value
1	R1, RØ = Stepping motor rate	RØ and R1 = Ø
1	V = Track number verify flag Ø = No verify 1 = Verify on destination track	V = Ø
1	H = Head load flag Ø = Unload head at beginning 1 = Load head at beginning	H = Ø
1	T = Track update flag Ø = No update 1 = Update track register	T = 1
2	L = Sector length flag Ø = 256, 512, 1024, and 128 for LSB's sector length in ID fields ØØ, Ø1, 1Ø, and 11, respectively 1 = 128, 256, 512, and 1024 for LSB's sector length in ID fields ØØ, Ø1, 1Ø, and 11, respectively	L = 1
2	M = Multiple record flag Ø = Single record 1 = Multiple records	command dependent

Table 2-2. Floppy Disk Controller Flag Summary. (Page 2 of 2)

Command Type	Flag/Description	Suggested Value
2, 3	AØ = Data address mark Ø = FBh (DAM) 1 = F8h (deleted DAM)	AØ = Ø
2, 3	U = Update SSO Ø = Update SSO to Ø 1 = Update SSO to 1	command dependent
2, 3	E = 15 millisecond delay Ø = No 15 millisecond delay 1 = 15 millisecond delay (30 millisecond for 1 MHz)	E = 1
4	IX = Interrupt condition flags IØ = 1 Not ready to ready transition I1 = 1 Ready to not ready transition I2 = 1 Index pulse I3 = 1 Immediate interrupt, requires reset I3- IØ = Ø Terminate with no interrupt (INTRQ)	command dependent

Table 2-3. Status Register Summary. (Page 1 of 3)

Summary of Commands

Bit	All Type I Commands	Read Address	Read Sector	Read Track	Write Sector	Write Track
Ø	Busy	Busy	Busy	Busy	Busy	Busy
1	Index Pulse	DRQ	DRQ	DRQ	DRQ	DRQ
2	Track ØØ	Lost Data	Lost Data	Lost Data	Lost Data	Lost Data
3	CRC Error	CRC Error	CRC Error	Ø	CRC Error	Ø
4	Seek Error	RNF	RNF	Ø	RNF	Ø
5	Head Loaded	Ø	Record Type	Ø	Ø	Ø
6	Write Protect	Ø	Ø	Ø	Write Protect	Write Protect
7	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready	Not Ready

Table 2-3. Status Register Summary. (Page 2 of 3)

Status for Type 1 Commands

Data Bit	Function
Ø	Busy: When set, indicates that a command is in progress; when reset, indicates that no command is in progress
1	Index: When set, indicates that an index mark is detected from the floppy disk drive; this bit is an inverted copy of the IP- (Index Pulse) input
2	Track ØØ: When set, indicates that the read/write head is positioned over track ØØ; this bit is an inverted copy of the TRØØ- (Track ØØ) input
3	CRC Error: When set, indicates that a CRC error was encountered in an ID field
4	Seek Error: When set, indicates that the desired track was not verified; reset to Ø when updated.
5	Head Loaded: When set, indicates the head is loaded and engaged; this bit is a logical AND of the HLD+ (Head Load) and HLT+ (Head Load Time) signals
6	Protected: When set, indicates write protect is activated; this bit is an inverted copy of the WRPT- (Write Protect) input
7	Not Ready: When set, indicates the drive is not ready; this bit is an inverted copy of the Ready input and is logically ORed with MR- (Master Reset)

Table 2-3. Status Register Summary. (Page 3 of 3)

Status for Type 2 and 3 Commands

Data Bit	Function
Ø	Busy: When set, indicates that a command is under execution; when reset, no command is under execution
1	Data Request: Copies the DRQ+ output; when set, indicates that the Data register is full on a Read operation or that the Data register is empty on a Write operation (reset to Ø when updated)
2	Lost Data: When set, indicates that the X-Bus master did not respond to DRQ (Data Request) in one byte interval (reset to Ø when updated)
3	CRC Error: If bit 4 is set, an error was found in one or more ID fields; otherwise, indicates error in data field (reset to Ø when updated)
4	Record Not Found: When set, indicates that the desired track, sector, or side was not found (reset to Ø when updated)
5	Record Type: On a Read Record command, indicates the record-type code from the data field address mark (1 = deleted data mark; a Ø = data mark); on any write command, this bit is forced to Ø
6	Write Protect: Not used on Read Record or Read Track commands; on any write command, indicates that the floppy disk is write-protected (reset to Ø when updated)
7	Not Ready: When set, indicates that the drive is not ready; when reset, indicates that the drive is ready; this bit is an inverted copy of the Ready input and is ORed with MR- (Master Reset); the Type 2 and 3 commands do not execute unless the drive is ready

Commands are divided into four types. For the command bytes and their corresponding flag explanations, see Tables 2-1 and 2-2, respectively. For additional information, see the Western Digital Corp. 1983 Components Handbook.

TRACK REGISTER (PORT XXØ2h)

This 8-bit read/write register contains the track number of the current read/write head position. During a seek or read/write operation, this register holds the current track number and is increased each time the read/write head is stepped in toward the center of the floppy disk or decreased each time the read/write head is stepped out toward the edge of the floppy disk. The contents of the Track register are compared with the recorded track number in the floppy disk's track identification field during disk read, write, and verify operations. The Track register should not be loaded when the WD2797-Ø2 Status register Busy bit (bit Ø) is set.

SECTOR REGISTER (PORT XXØ4h)

This 8-bit read/write register contains the address of the desired sector position. The content of this register is compared with the recorded sector number in the identification field during read or write operations. The Sector register should not be loaded when the WD2797-Ø2 Status register Busy bit (bit Ø) is set.

DATA REGISTER (PORT XXØ6h)

This 8-bit register holds a byte of data during read or write operations. During read operations, the assembled data byte is tranferred in parallel to this register from the internal Data Shift register of the WD2797-Ø2. During disk write operations, information is transferred in parallel from this register to the internal Data Shift register. During a seek command, the Data register holds the address of the desired track position.

FLOPPY DISK DRIVE CONTROL REGISTER (PORT XXØ8h)

Data bit functions of this write register are as follows:

Data Bit	Function
Ø	If set, enables floppy disk drive and associated light; if reset, disables floppy disk drive and associated light
1	Unused
2	If set, turns on floppy disk drive motor; if reset, turns off floppy disk drive motor
3, 4	Unused
5	If set, selects side 1; if reset, selects side Ø
6	If set, selects 2-MHz clock for seek operations; if reset, selects 1-MHz clock for read and write operations
7	WD2797-Ø2 Reset: Reset to Ø initializes all internal logic of the WD2797-Ø2 and disables the WD2797-Ø2

COUNTER Ø (PORT XX1Øh)

After the 8253 Mode Control word is written, two bytes are written into this register. Counter Ø is clocked every time the X-Bus master addresses the WD2797-Ø2 Data register. Counter Ø is loaded with two bytes to indicate the actual number of bytes to be transferred, minus 2, during the read or write operation. If, for example, a transfer involves 16 sectors of 256 bytes each, the hexadecimal equivalent of 4Ø94 (ØFFEh) is loaded into this register as follows:

1. Write FEh to port XX1Øh (least significant byte).

2. Write ØFh to port XX1Øh (most significant byte).

COUNTER 1 REGISTER (PORT XX12h)

After the 8253 Mode Control word is written, two divisor bytes are written into this Counter register. The counter divides a 1-MHz input clock by the number selected by the divisor bytes. This counter is programmed to time out about 14Ø microseconds after the data transfer to give the WD2797-Ø2 enough time to compute the two CRC bytes in case of a read error. If, for example, a 14Ø-microsecond timeout interval occurs, the hexadecimal equivalent of 14Ø (ØØ8Ch) is loaded into this register as follows:

1. Write 8Ch to port XX12h (least significant byte of the count).

2. Write ØØ to port XX12h (most significant byte of the count).

MODE CONTROL REGISTER (PORT XX16h)

This write-only register holds the Mode Control word for the two counters (that is, counters Ø and 1) used in the 8253 programmable interval timer for floppy disk control. Data bit functions are as follows:

Data Bit	Function
Ø	If set to 1, the counter counts in binary-coded decimal; if reset to Ø, the counter counts in binary
1 - 3	Mode control (must be reset to Ø)
4, 5	Read/load (see below)
6, 7	Select counter (see below)

Read/Load Bits

5	4	Mode Selected
Ø	Ø	Counter latching operation
Ø	1	Read/load least significant byte only
1	Ø	Read/load most significant byte only
1	1	Read/load least significant byte first, then most significant byte

Select Counter Bits

7	6	Counter Selected
Ø	Ø	Ø
Ø	1	1
1	Ø	Not used for floppy (used for hard disk drive)
1	1	Unused

FLOPPY DISK FORMATTING

When the WD2797-Ø2 formats a track on the floppy disk drive, the data for the formatting operation must be stored in the X-Bus master's memory. Formatting the floppy track is accomplished by positioning the read/write head over the desired track and issuing a Write Track command.

Upon receipt of the Write Track command, the read/write head is loaded, and the Busy bit (bit Ø) is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt to the X-Bus master is asserted. The Data Request line is activated immediately upon receipt of the command, but writing does not start until after the first byte is loaded into the Data register. If the Data register has not been loaded by the time the index pulse is encountered, the operation is terminated (making the device Not Busy), the Lost Data status bit (bit 2) is set, and the interrupt is asserted. If the operation starts, (that is, a first byte is written but a succeeding byte is not present in the Data register when needed), a byte of zeros is substituted.

This sequence continues from one index mark to the next. Normally, the data pattern appearing in the Data register is written on the disk with a normal clock pattern. If, however, the WD2797-Ø2 detects a data pattern of F5h through FEh in the Data register, the WD2797-Ø2 interprets this pattern as data address marks with missing clocks or CRC generation. As a consequence, F5h through FEh should not appear in the gap, data fields, or ID fields.

The CRC generator is initialized when any data byte from F8h to FEh is about to be transferred from the Data register to the internal Data Shift register or by receipt of F5h. An F7h pattern transferred from the Data register to the Data Shift register generates two CRC characters in MFM. CRCs must be generated by an F7h pattern.

The formatting values in hexadecimal for a floppy disk with 16 sectors of 256 bytes each are listed in Table 2-4. A drawing of the same floppy disk format is shown in Figure 2-2.

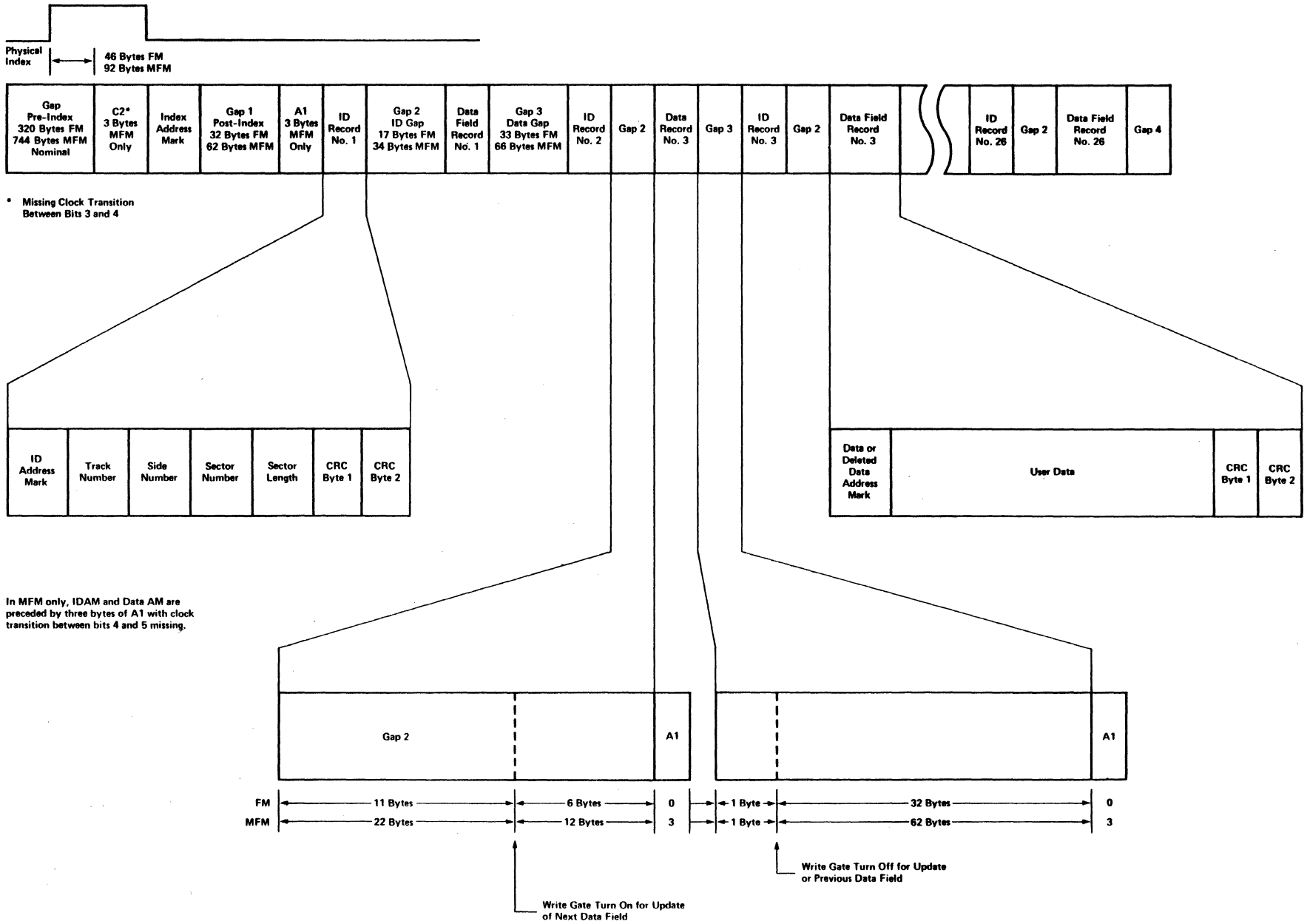


Figure 2-2. Floppy Disk Track Format.

Table 2-4. Floppy Disk Formatting Values.

Number of Bytes	Value of Byte Written (h)
80	4E
12	00
3	F6 (writes C2)
1	FC (index mark)
50	4E
Write the following values once for every sector on the floppy disk:	
12	00
3	F5 (writes A1)
1	FE (ID address mark)
1	Track number (0 through 4C)
1	Side number (0 or 1)
1	Sector number (1 through 10h)
1	01 (sector length)
1	F7 (2 CRCs written)
22	4E
12	00
3	F5 (writes A1)
1	FB (data address mark)
256	Data
1	F7 (2 CRCs written)
54	4E
Continue writing 4Eh until the WD2797-02 interrupts (approximately 598 bytes).	
598	4E

HARD DISK CONTROLLER

A disk operation begins when the X-Bus master writes task information into the Task File registers of the WD1Ø1Ø Winchester disk controller. The task information includes the disk cylinder number, head number, sector number, drive number, track number for start of write precompensation, sector size, and the number of sectors to be transferred. After the task information has been written, the X-Bus master writes the command into the Command register. During a Write Sector command, the X-Bus master reads the status of the WD1Ø1Ø to inspect the buffer data request flag, and then writes data into the RAM data buffer.

When the RAM data buffer is full, the BRDY+ (Buffer Ready) input of the WD1Ø1Ø is activated. Then, the WD1Ø1Ø de-asserts the BDRQ+ (Buffer Data Request) line and asserts BCS- (Buffer Chip Select).

The buffered data is transferred to the hard disk, and the RAM data buffer becomes empty.

HARD DISK DRIVE COMMAND AND STATUS REGISTERS

TASK FILE REGISTERS (PORTS XX2Øh THROUGH XX2Eh)

Before any of the commands or status information can be executed, a set of registers, collectively referred to as the Task File registers, must be set up.

The Task File registers for the hard disk controller in the Floppy/Hard Disk Module are as follows:

Address (h)	Function	Access
XX2Ø	Data register	R/W
XX22	Error register	R
XX22	Write Precompensation Cylinder register	W
XX24	Sector Count register	R/W
XX26	Sector Number register	R/W
XX28	Cylinder Number Low register	R/W
XX2A	Cylinder Number High register	R/W
XX2C	Sector/Drive/Head register	R/W
XX2E	Status register	R
XX2E	Command register	W

DATA REGISTER (PORT XX2Øh)

This read/write register holds a byte of data during read or write operations.

ERROR REGISTER (PORT XX22h)

Positive-true data bit functions of this read register are as follows:

Data Bit	Function
Ø	Data Address Mark Not Found: Data field address mark not found during a read; the data address mark should be found within 15 bytes after the ID field (see Figure 2-3, "Hard Disk Track Format," below)
1	TKØØØ Error: Occurs when track Ø is not found in a Restore command after 1Ø24 stepping pulses
2	Aborted Command: Set upon the following conditions (after command has started): o drive not ready o write fault o seek complete not active within 16 index pulses o illegal command code
3	Reserved; reset to Ø
4	ID Not Found: Occurs when cylinder, head, sector, or size parameters cannot be found after 16 index pulses have been encountered
5	Reserved; reset to Ø

6	Data Field CRC: Error detected in the data field; the sector can be reread to attempt recovery from a soft error (the data contained in the buffer can be read, but contains errors)
7	Bad Block: A bad block address mark has been detected during read or write attempt

WRITE PRECOMPENSATION CYLINDER REGISTER (PORT XX22h)

Data bits Ø through 7 of this write register indicate the cylinder number; the write current is reduced and write data is precompensated.

The value loaded into this register is internally multiplied by 4 to specify the actual cylinder where reduced write current (RWC) is asserted. For example, a value of Ø1h will cause RWC to activate on cylinder 4, and Ø2h will cause RWC to activate on cylinder 8. Switching points, therefore, are Ø, 4, 8, up to 1Ø2Ø. The RWC will be asserted when the current cylinder is equal to a greater value than the value in this register. For example, if a drive requires precompensation on cylinder 128 (8Øh) and above, this register should be loaded with 32 (2Øh).

SECTOR COUNT REGISTER (PORT XX24h)

Data bits Ø through 7 of this read/write register indicate the number of sectors to transfer during a disk read/write operation, or the number of sectors per track during a disk format operation.

SECTOR NUMBER REGISTER (PORT XX26h)

Data bits Ø through 7 of this read/write register indicate the sector address during read/write operations.

CYLINDER NUMBER LOW REGISTER (PORT XX28h)

Data bits Ø through 7 of this read/write register indicate the low byte of the cylinder that is being read from or written to.

CYLINDER NUMBER HIGH REGISTER (PORT XX2Ah)

Data bits Ø through 7 of this read/write register indicate the high byte of the cylinder that is being read from or written to.

SECTOR/DRIVE/HEAD REGISTER (PORT XX2Ch)

Data Bit	Function
Ø - 2	Head Number
3, 4	Drive Number
5, 6	Sector Size (see below)
7	Sector Extension: Reset to use CRC

Sector Size Bits

6 5	Data Field (in bytes)*
Ø Ø	256
Ø 1	512
1 Ø	1Ø24
1 1	128

*CTOS standard software uses 512K bytes

STATUS REGISTER (PORT XX2Eh)

Positive-true data bit functions of this read register are as follows:

Data Bit	Function
Ø	Error: Indicates that a bit in the Error register has been set
1	Command in Progress: Indicates that a command is in progress
2	Reserved; reset to Ø
3	Data Request: Reflects the BDRQ+ line; when active, a buffer data transfer is desired (Data request flag is used for programmed I/O while BDRQ+ is used for DMA-controlled I/O)
4	Seek Complete: Reflects Seek Complete (SC+) line
5	Write Fault: Reflects the Write Fault (WF+) line; an interrupt is generated when set
6	Drive Ready: Reflects the Drive Ready (DRDY+) line; after an error interrupt, DRDY+ waits until the Status register is read; an interrupt is generated when reset
7	Busy: Active when the WD1Ø1Ø is accessing the disk; activated by writing into the Command register, and deactivated at the end of all commands except Read Sector (deactivation occurs when a sector of data has been transferred to the RAM data buffer after the Read Sector Command)

COMMAND REGISTER (PORT XX2Eh)

Bytes of this write register can be configured for one of the following:

Command	Data Bits 7	6	5	4	3	2	1	Ø
Restore*	Ø	Ø	Ø	1	T3	T2	T1	TØ
Seek*	Ø	1	1	1	T3	T2	T1	TØ
Read Sector**	Ø	Ø	1	Ø	D	M	Ø	Ø
Write Sector**	Ø	Ø	1	1	Ø	M	Ø	Ø
Scan ID	Ø	1	Ø	Ø	Ø	Ø	Ø	Ø
Write Format	Ø	1	Ø	1	Ø	Ø	Ø	Ø

*Step Time

T3	T2	T1	TØ	For 5-MHz Write Clock
Ø	Ø	Ø	Ø	35 microseconds
Ø	Ø	Ø	1	Ø.5 milliseconds
Ø	Ø	1	Ø	1.Ø milliseconds
Ø	Ø	1	1	1.5 milliseconds
1	1	1	1	7.5 milliseconds

**I/O Type and Sector Read or Write

D	Function
Ø	Programmed I/O
1	Direct memory access

M	Function
Ø	Single-sector read or write
1	Multiple-sector read or write

CONTROL REGISTERS (PORTS XXØAh THROUGH XX36h)

In addition to the Task File registers, the following registers are used for hard disk drive control in the Floppy/Hard Disk Module:

Address (h)	Function	Access
XXØA	Hard Disk Drive Control register	W
XXØE	X-Bus Extended Address register	W
XX14	Read counter 2 (located on 8253 used for floppy drive control)	R
XX14	Load counter 2 (located on 8253 used for floppy drive control)	W
XX16	8253 mode control (also used for floppy drive control)	W
XX3Ø	Read counter Ø	R
XX3Ø	Load counter Ø	W
XX32	Read counter 1	R
XX32	Load counter 1	W
XX34	Read counter 2	R
XX34	Load counter 2	W
XX36	8253 mode control	W

HARD DISK DRIVE CONTROL REGISTER (PORT XXØAh)

Positive-true data bit functions of this write register are as follows:

Data Bit	Function
Ø	Drive Select Ø: Selects the Floppy/Hard Disk Module hard disk drive
1	Drive Select 1: Selects the Expansion Module hard disk drive (if applicable)
2	Boot Select: Allows the ROM on the Controller board to be transferred to X-Bus master memory via DMA
3 - 5	Head Select /Expansion Head Select: Value selects either hard disk head or Expansion Module hard disk head (depending on data bits Ø and 1)
6	Hard Disk Write: Must be set if a hard disk write operation is to be performed
7	WD1Ø1Ø Reset: Reset to Ø initializes all internal logic of the WD1Ø1Ø and disables the WD1Ø1Ø

X-BUS EXTENDED ADDRESS REGISTER (PORT XXØEh)

Positive-true data bit functions of this write register are as follows:

Data Bit	Function
Ø	X-Bus address line 11h
1	X-Bus address line 12h
2	X-Bus address line 13h
3	X-Bus address line 14h
4	X-Bus address line 15h
5	X-Bus address line 16h
6	X-Bus address line 17h
7	Disable Read/Write: If set, disables X-Bus master I/O read and write signals to the WD1Ø1Ø, allowing the WD1Ø1Ø a dedicated bus to the RAM data buffer

During DMA transfers, X-Bus address line ØØh (that is, XADRØ-) is issued, since the Extended Address Register cannot cross 64K-word boundaries.

COUNTER 2 REGISTER (PORT XX14h)

This counter is used to count the total number of words for internal use by the controller.

After the 8253 Mode Control word of ØBØh is written to port XX16h, this counter is loaded with two bytes that represent the total transfer count in words, minus two.

If, for example, 1Ø24 words (2Ø48 bytes) are to be transferred, this counter is loaded with 1Ø24 minus 2, or 1Ø22 (that is, Ø3FEh) as follows:

1. Write FEh to port XX14h (least significant byte).

2. Write Ø3h to port XX14h (most significant byte).

MODE CONTROL REGISTER (PORT XX16h)

This write-only register holds the Mode Control word for counter 2 used in the 8253 programmable interval timer for hard disk control. Bit functions are as follows:

Data Bit	Function
Ø	If set to 1, the counter counts in binary-coded decimal; if reset to Ø, the counter counts in binary
1 - 3	Mode control (must be reset to Ø)
4, 5	Read/load (see below)
6, 7	Select counter (see below)

Read/Load Bits

5	4	Mode Selected
Ø	Ø	Counter latching operation
Ø	1	Read/load least significant byte only
1	Ø	Read/load most significant byte only
1	1	Read/load least significant byte first, then most significant byte

Select Counter Bits

7	6	Counter Selected
Ø	Ø	Not used for hard disk (used for floppy disk)
Ø	1	Not used for hard disk (used for floppy disk)
1	Ø	2
1	1	Unused

COUNTER Ø (PORT XX3Øh)

This counter is used to count the total number of words to be transferred.

After the 8253 Mode Control word of 3Øh is written to port XX36h, this counter is loaded with two bytes that represent the total transfer count in words, minus one.

If, for example, 1Ø24 words (2Ø48 bytes) are to be transferred, this counter is loaded with 1Ø24 minus 1, or 1Ø23 (that is, Ø3FFh) as follows:

1. Write FFh to port XX3Øh (least significant byte).

2. Write Ø3h to port XX3Øh (most significant byte).

COUNTER 1 (PORT XX32h)

This counter is used to count the number of words transferred in one DMA burst.

After the 8253 Mode Control word of 72h is written to port XX36h, this counter is loaded with two bytes that represent the DMA burst size in words.

If, for example, a burst size of four words is used, this counter is loaded as follows:

1. Write Ø4h to port XX32h (least significant byte).

2. Write ØØh to port XX32h (most significant byte).

COUNTER 2 REGISTER (PORT XX34)

This counter is used to control the time elapsed after one DMA burst.

After the 8253 Mode Control word of B2h is written to port XX36h, this counter is loaded with two bytes that represent the time elapsed after one DMA burst.

If, for example, a 2.5 microsecond interval is used, this counter is loaded as follows:

1. Write 05h to port XX34h (least significant byte).

2. Write 00h to port XX34h (most significant byte).

MODE CONTROL REGISTER (PORT XX36h)

This write-only register holds the Mode Control word for counters Ø, 1, and 2 used in the 8253 programmable interval timer for hard disk control. Bit functions are as follows:

Data Bit	Function
Ø	If set to 1, the counter counts in binary-coded decimal; if reset to Ø, the counter counts in binary
1 - 3	Mode control (see below)
4, 5	Read/load (see below)
6, 7	Select counter (see below)

Mode Control Bits

3	2	1	Mode
Ø	Ø	Ø	Interrupt on terminal count
Ø	Ø	1	Programmable one-shot
X	1	Ø	Unused
X	1	1	Unused
1	Ø	Ø	Unused
1	Ø	1	Unused

Read/Load Bits

5	4	Mode Selected
Ø	Ø	Counter latching operation
Ø	1	Read/load least significant byte only
1	Ø	Read/load most significant byte only
1	1	Read/load least significant byte first, then most significant byte

Select Counter Bits

7	6	Counter Selected
Ø	Ø	Ø
Ø	1	1
1	Ø	2
1	1	Unused

HARD DISK FORMATTING

The Write Format command in the Command register (port XX2Eh) is used to format one track using the Task File registers and the sector buffer. During the Write Format command, the sector buffer is used for additional parameter information instead of sector data. The content of the sector buffer for a 32-sector track format with an interleave factor of 2 is shown in Table 2-5.

Each sector requires a two-byte sequence. The first byte designates whether a bad block mark is to be recorded in the sector's ID field. An Øh is normal; an 8Øh indicates a bad block mark for that sector. In Table 2-5, sector Ø4 will receive a bad block mark.

The second byte indicates the logical sector number to be recorded. Using this scheme, sectors may be recorded using any interleave factor desired. The remaining memory in the sector buffer may be filled with any value; its purpose is only to generate a BRDY (Buffer Ready) to inform the WD1Ø1Ø to begin formatting the track.

An implied seek is also in effect during this command if the cylinder registers differ from the internal cylinder position. The Sector Count register is used to hold the total number of sectors to be formatted (where FFh equals 255 sectors). The Sector Number register holds the number of bytes to be used for gap 1 and gap 3. (A bit pattern of 4Eh is used.)

The data field is loaded with ØFFh, and CRC is automatically generated and appended unless the extension bit is set in the Sector/Drive/Head register.

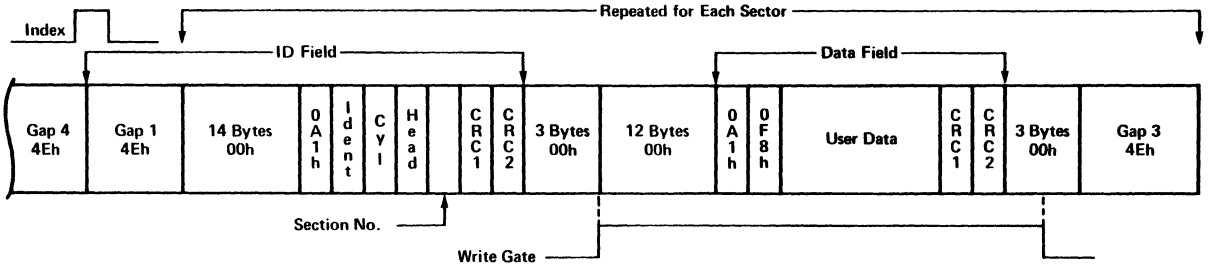
After the last sector is written, the controller backfills the track with 4Eh bits. When an index pulse that follows the last sector written is encountered, the format operation is terminated.

As with other commands, a write fault or not ready condition will terminate the command.

The hard disk track format is shown in Figure 2-3.

Table 2-5. Sample Sector Buffer.

Address (h)	Data Ø	1	2	3	4	5	6	7
ØØ	ØØ	ØØ	ØØ	1Ø	ØØ	Ø1	ØØ	11
Ø8	ØØ	Ø2	ØØ	12	ØØ	Ø3	ØØ	13
1Ø	8Ø	Ø4	ØØ	14	ØØ	Ø5	ØØ	15
18	ØØ	Ø6	ØØ	16	ØØ	Ø7	ØØ	17
2Ø	ØØ	Ø8	ØØ	18	ØØ	Ø9	ØØ	19
28	ØØ	ØA	ØØ	1A	ØØ	ØB	ØØ	1B
3Ø	ØØ	ØC	ØØ	1C	ØØ	ØD	ØØ	1D
38	ØØ	ØE	ØØ	1E	ØØ	ØF	ØØ	1F
4Ø	FF	FF	FF	FF	FF	FF	FF	FF
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
FØ	FF	FF	FF	FF	FF	FF	FF	FF



NOTE: GAP 1/3 length determined by Sector Number register contents during formatting

ID FIELD
- ØA1h = ØA1h with ØAh clock
- IDENT = MSB of cylinder number
  - ØFE = Ø to 255 cylinders
  - ØFF = 256 to 511 cylinders
  - ØFC = 512 to 767 cylinders
  - ØFD = 768 to 1Ø23 cylinders
- HEAD = Bits Ø, 1, and 2: Head number
  - Bits 5 and 6: Sector size
  - Bit 7: Bad block mark
- SEC# = Logical sector number

DATA FIELD
- ØA1h = ØA1h with ØAh clock
- ØF8h = Data addres mark; normal clock
- USER = Data field 128 to 1Ø24 bytes*

*No CRC, but seven additional bytes written at end of data field if EXT bit in Sector/Drive/Head register is set to 1

Figure 2-3. Hard Disk Track Format.

PROGRAMMABLE ARRAY LOGIC

Two 16L8 programmable array logic (PAL) chips are used in the Floppy/Hard Disk Module to generate control signals. Programming examples are provided in Figures 2-4 and 2-5 for integrated circuit (IC) designations 7E and 13E, respectively. (See the schematic diagram shown in Figure 3-2, page 5, in Section 3, "Theory of Operation," for IC designation of the PALs.)

```
/XMEMRD /XDACK3 /IORD WDIORDWR ODD BCS BOOTEN END WWRITE GND
/RST START BDRQ /DISBL /CNTRINC ADRINC DMACLK END2 /8253CLK VCC

IF (VCC) /DMACLK = /XDACK3 + /XMEMRD * /IORD
IF (VCC) CNTRINC = DMACLK + BCS * WDIORDWR
;
;          ADRINC = DMACLK + BCS * WDIORDWR * ODD
;
IF (VCC) /ADRINC = /DMACLK * /BCS + /DMACLK * /WDIORDWR
                   + /DMACLK * /ODD
IF (VCC) 8253CLK = BCS * WDIORDWR * ODD
;
IF (VCC) DISBL   = END * BOOTEN + RST
;
;           START = /END * ( BOOTEN + BDRQ * END2 * /WWRITE
;                   + BDRQ * /END2 * WWRITE )
;
IF (VCC) /START  = END + /BDRQ * /BOOTEN + /BOOTEN * /END2 *
                   /WWRITE + /BOOTEN * END2 * WWRITE
```

Figure 2-4. 16L8 PAL Program for Integrated Circuit 7E.

```
BDRQ /LD4 END2 2Q WWRITE END A1 A2 /2797CS GND
/8253CS /MDEN NC IORDWR /BCR START /W8253EN /DM BRDY VCC
;
; BRDY SIGNALS WD1010 THAT BUFFER IS READY FOR DATA TRANSFER
;          BRDY = BDRQ * END + BDRQ * /WWRITE * /END2
;
IF (VCC) /BRDY = /BDRQ + WWRITE * /END + END2 * /END
;
; DM PROVIDES THE CLOCK TO THE 8253 FLOPPY TIMER COUNTER 0
;          DURING FLOPPY DATA DMA TRANSFER
;
IF (VCC) DM    = 2797CS * A1 * A2 * IORDWR
;
; MDEN ENABLES THE DATA BUS TRANSCEIVER OF THE WD2797
;          FLOPPY CONTROLLER AND THE 8253 TIMERS
;
IF (VCC) MDEN  = 2797CS + 8253CS + W8253EN
;
; BCR RESETS THE 8K BYTES DATA BUFFER BEFORE AND AFTER THE
;          DMA CYCLE
;
IF (VCC) BCR = START * /2Q + /START * 2Q + LD4
```

Figure 2-5. 16L8 PAL Program for Integrated Circuit 13E.

MODULE BASE I/O ADDRESS SUMMARY

As described in the "X-Bus Interface" subsection, above, during power-up or push-button reset, the Processor Module assigns a base address to each module connected to it on the X-Bus. The first module to the right of the processor is assigned a base I/O address of Ø1XXh, the second module to the right of the Processor Module is assigned a base I/O address of Ø2XXh, and so on.

The base I/O address of any module except the Processor Module can be programmed to be any number from Ø1XXh to FFXXh (in 1XXh address increments). Two facilities are available for changing the base address of the modules: the Panel Debugger routine in the Processor Module's bootstrap ROM program and the software Debugger.

Using either debugger, each module on the X-Bus must first be reset to clear the addresses previously set by the Processor Module. Also, each module on the X-Bus must be assigned a new base address number.

PANEL DEBUGGER

To change the base I/O address using the Panel Debugger routine, proceed as follows:

1. Simultaneously press the RESET button on the back of the workstation and the space bar on the keyboard.

2. To bring up the Panel Debugger routine, press P.

3. To reset the X-Bus, type "ØF98ØO=n" at the "+" prompt (n can be any number) and then press <Return>. (Note that the letter "O" is the character preceding the equal sign.)

4. To select the first module to the right of the Processor Module, type "ØI". Port Ø returns an identification number for the module (for example, 1Ø7Øh is a number assigned to the Floppy/Hard Disk Module).

5. Type the desired base address for the module, for example, "ØO=1", and then press <Return>. This causes Ø1XXh to be output to port Ø. In

this example, the base address assigned to the first module is "1" or Ø1XXh. If this module is the Floppy/Hard Disk Module, the floppy drive Status register is at address Ø1ØØh and the floppy drive Data register is at Ø1Ø6h. The LED in front of the module lights to show that it is selected.

Repeat steps 4 and 5 for every module in the system, assigning a different base I/O address to each module. (For further information about the Panel Debugger routine, see the Diagnostics Manual.)

SOFTWARE DEBUGGER

To change the base I/O address using the software Debugger, proceed as follows:

1. Enter the debugger by simultaneously pressing the ACTION and A keys.

2. To reset the X-Bus, type "ØF98ØO" at the "!" prompt, and press the right arrow key. Enter a number from Ø to 9. (Note that the letter "O" is the last character in ØF98ØO.)

3. To select the first module to the right of the Processor Module, type "ØI" and the right arrow key. Port Ø returns an identification number for the module (1Ø7Øh is a number assigned to the Floppy/Hard Disk Module).

4. Type "ØO" and press the right arrow key. Then enter the desired base address for the module, 1 to FF. For example, if "FF" is typed, FFXXh is output to port Ø. In this case, the base address assigned to the first module is "FF" or FFXXh. If this module is the Floppy/Hard Disk Module, the floppy drive Status register is at address FFØØh and the floppy drive Data register is at FFØ6h.

Repeat steps 3 and 4 for every module in the system, assigning a different base address to each module. (For further information about the software Debugger, see the Debugger Manual.)

MODULE I/O ADDRESS SUMMARY

A summary of the I/O ports defined for the Floppy/Hard Disk Module is provided in Table 2-6. Port number, associated logic, input information, and output information are listed.

Table 2-6. I/O Address Summary. (Page 1 of 2)

Port No. (h)	Associated Logic	Read	Write
XX00	WD2797-02	Status register	Command register
XX02	WD2797-02	Track register	Track register
XX04	WD2797-02	Sector register	Sector register
XX06	WD2797-02	Data register	Data register
XX08	Floppy disk drive	-	Control register
XX0A	Hard disk drive	-	Control register
XX0E	X-Bus addressing	-	Extended Address register
XX10	Floppy disk 8253	Read counter 0	Load counter 0
XX12	Floppy disk 8253	Read counter 1	Load counter 1
XX14	Hard disk 8253	Read counter 2	Load counter 2
XX16	Floppy/hard disk 8253	-	Mode control

Table 2-6. I/O Address Summary. (Page 2 of 2)

Port No. (h)	Associated Logic	Read	Write
XX2Ø	WD1Ø1Ø	Data register	Data register
XX22	WD1Ø1Ø	Error register	Write Pre-compensation Cylinder register
XX24	WD1Ø1Ø	Sector Count register	Sector Count register
XX26	WD1Ø1Ø	Sector Number register	Sector Number register
XX28	WD1Ø1Ø	Cylinder Number Low register	Cylinder Number Low register
XX2A	WD1Ø1Ø	Cylinder Number High register	Cylinder Number High register
XX2C	WD1Ø1Ø	Sector/ Drive/Head register	Sector/ Drive/Head register
XX2E	WD1Ø1Ø	Status register	Command register
XX3Ø	Hard disk 8253	Read counter Ø	Load counter Ø
XX32	Hard disk 8253	Read counter 1	Load counter 1
XX34	Hard disk 8253	Read counter 2	Load counter 2
XX36	Hard disk 8253	-	Mode control

3 THEORY OF OPERATION

INTRODUCTION

This section, which provides detailed component-level descriptions of the hardware incorporated in the Floppy/Hard Disk Module, is directed to the engineer who needs to understand the Floppy/Hard Disk Module at the component level. Each functional block shown throughout this section is described in relation to the logic that performs the function. In addition, schematic drawings are provided in Figure 3-1 to supplement the text.

CIRCUIT DESCRIPTIONS

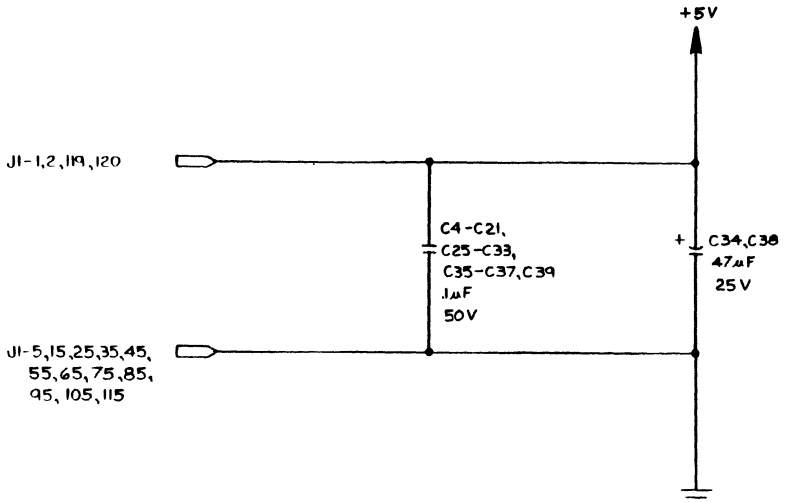
Detailed component-level circuit descriptions are given for the following:

- X-Bus module identification
- local module data bus interface
- transfer acknowledge generation
- Floppy/Hard Disk Module device decoding
- floppy disk drive controller logic
- hard disk drive controller logic
- disable read/write
- hard disk drive boot ROM
- hard disk drive controller RAM data buffer
- RAM chip selection and addressing
- RAM data direction
- direct memory access transfers
- state sequencer
- hard disk drive read/write circuitry
- 8253 programmable interval timers
- power supplies

PWR & GND LOCATER CHART			
REF. DES	TYPE.	+5V	GND

SPARE GATES		
TYPE	REF. DES.	QTY.
74LS244	10F	2
74LS74	9B	1
7474	1F	1
74LS125	1C	1
745124	1B	1
74586	4A	1

REFERENCE DESIGNATION	
LAST USED	NOT USED
C40	
RP4	
R19	
J1	
L1	



NOTES: UNLESS OTHERWISE SPECIFIED.

1. RESISTANCE VALUES ARE IN OHMS, 1/4W, ±5%.
2. CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL DEVICES ARE STANDARD 7&14, 10&20, 12&24, 14&28; PWR & GND CONNECTIONS.

Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 1 of 7)

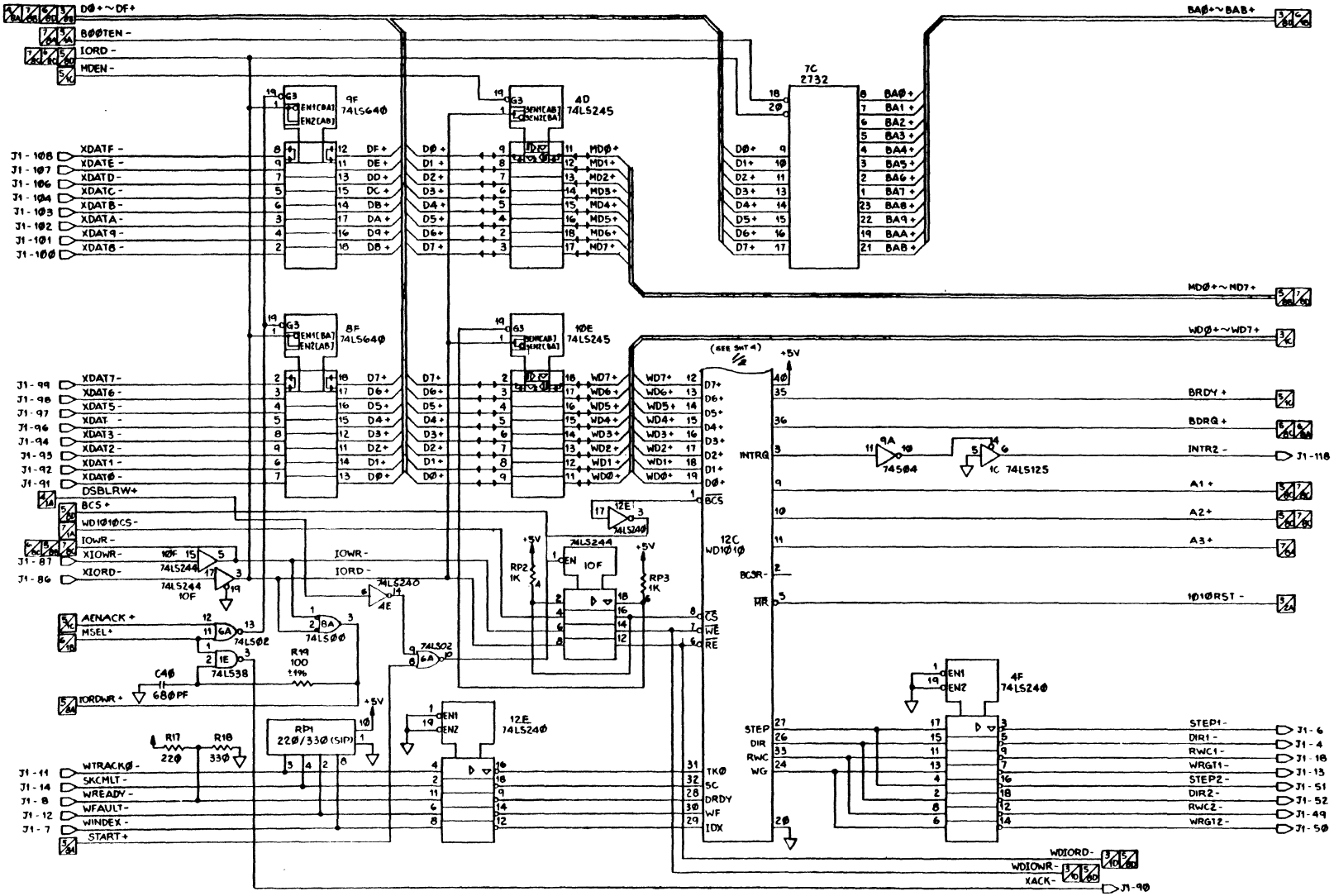


Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 2 of 7)

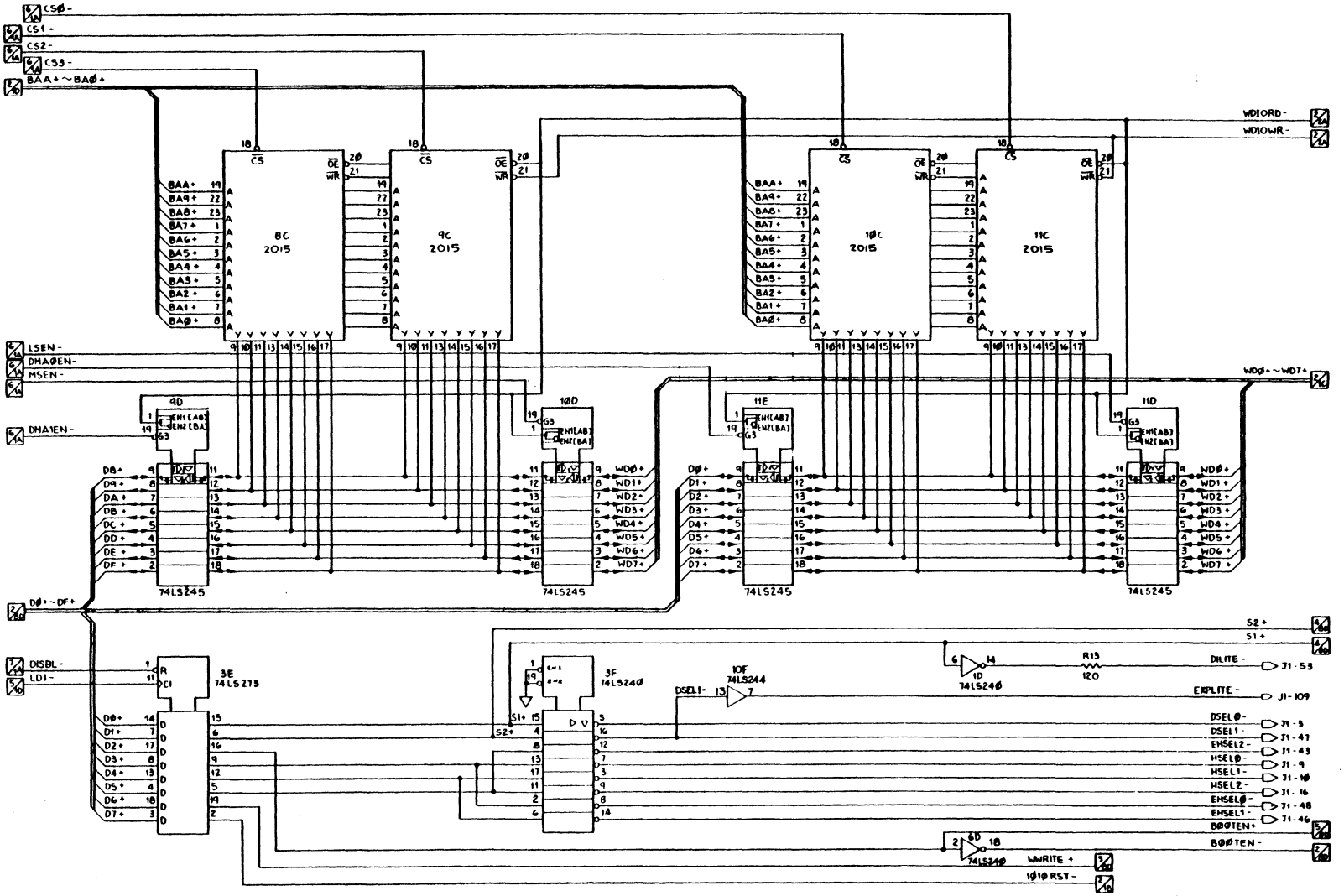


Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 3 of 7)

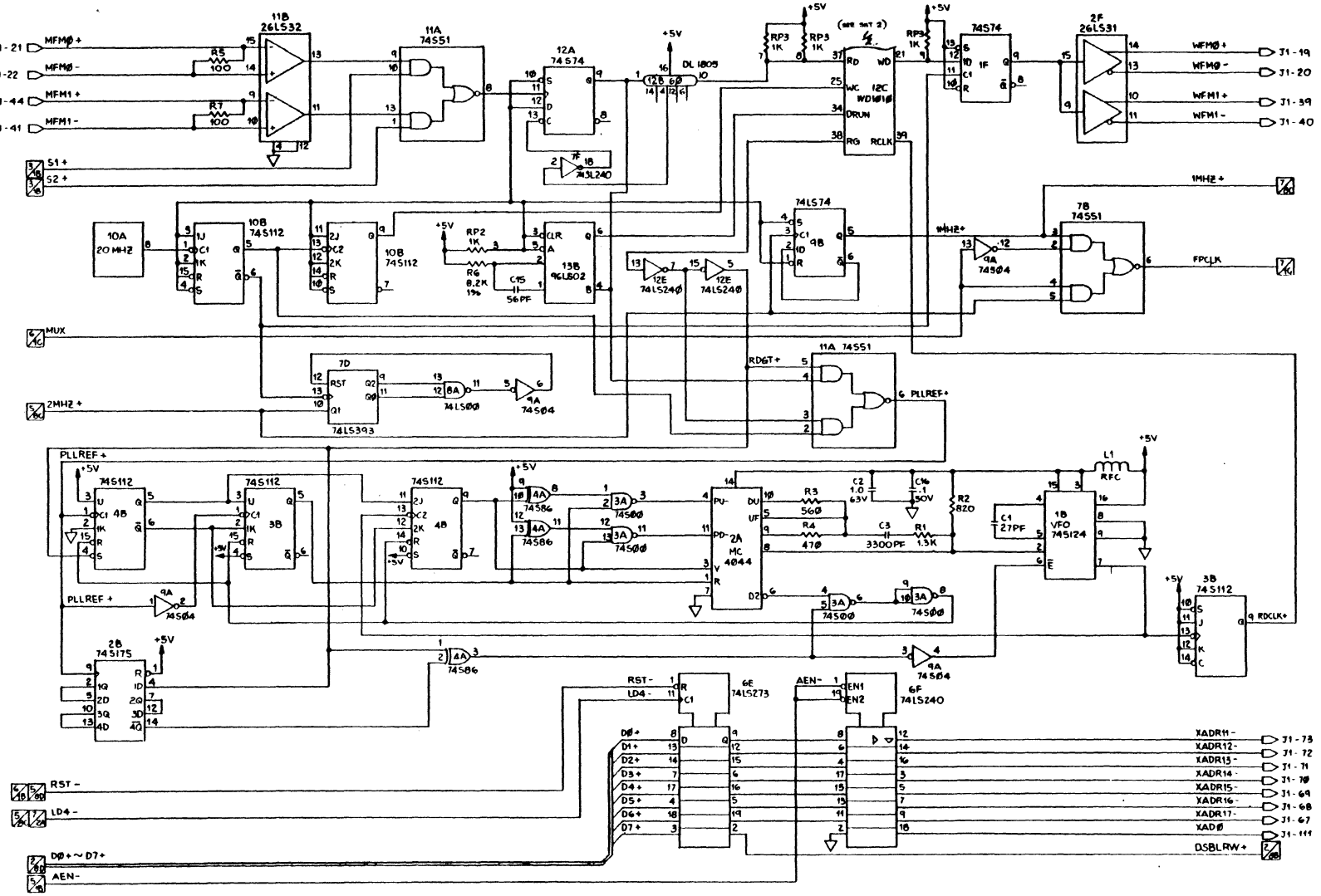


Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 4 of 7)

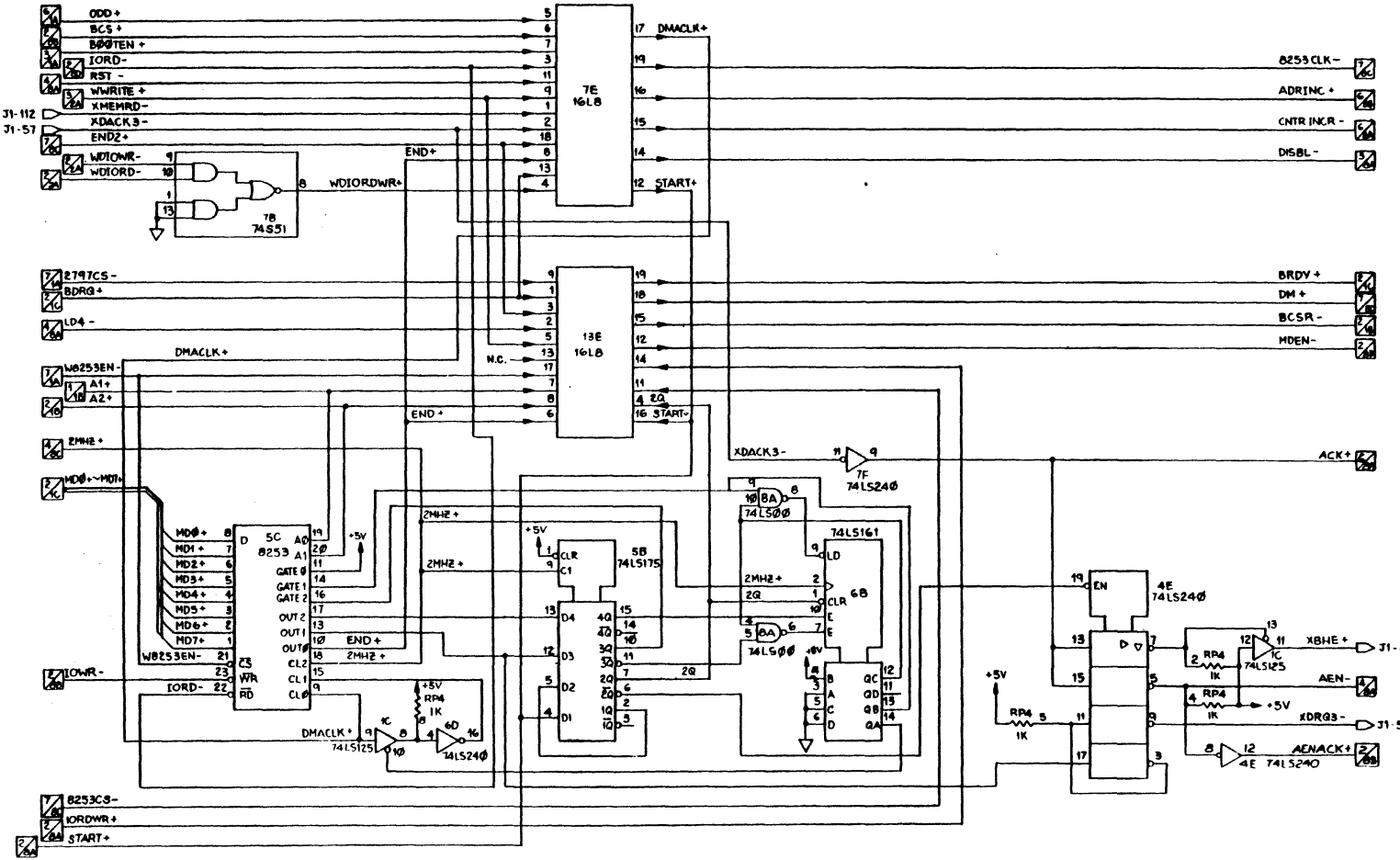


Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 5 of 7)

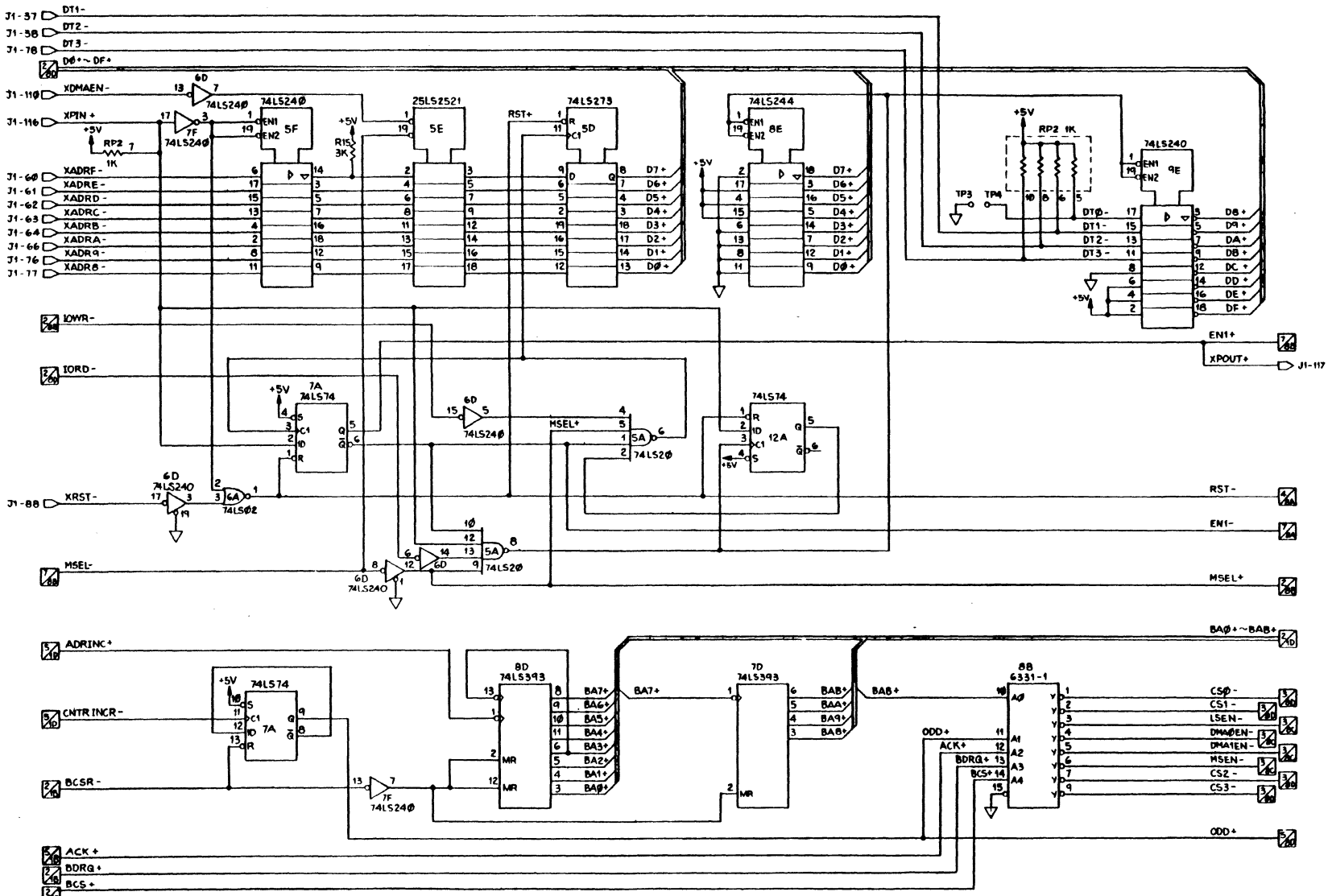


Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 6 of 7)

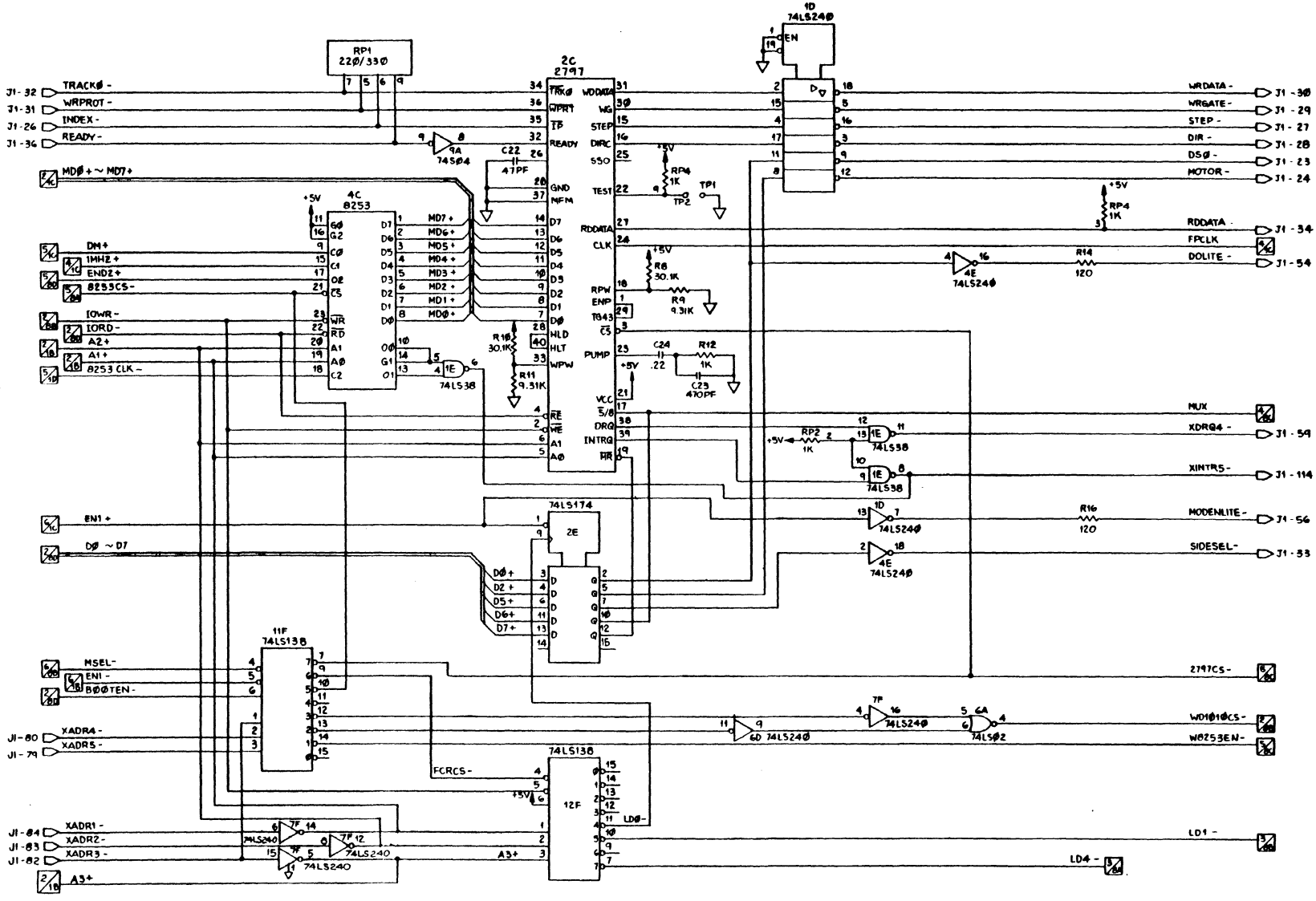


Figure 3-1. Floppy/Hard Disk Module Schematic Diagram. (Page 7 of 7)

X-BUS MODULE IDENTIFICATION

The Processor Module communicates with the Floppy/Hard Disk Module through the X-Bus interface as shown in Figure 3-1, page 6. Base addresses for the various I/O ports and registers are assigned by the Processor Module when a power-up reset or a manual (push-button) reset occurs on the X-Bus as XRST- (X-Bus Reset), or when XPIN+ (X-Bus Priority In) is reset low, signifying that activity on the X-Bus for the Floppy/Hard Disk Module has been suspended.

XRST-, connecting from J1, pin 88, is inverted at 6D (pin 3) and driven to NOR gate 6A (pin 3). A low XPIN+ connecting from J1, pin 116, is inverted at 7F (pin 3) before connecting at NOR gate 6A (pin 2). In either case (that is, a reset or low X-Bus Priority In), a high signal at pin 3 or 2 forces a low signal at pin 1 of 6A, to clear D flip-flop 7A at pin 1 and clear I/O Address register 5D at pin 1.

When 7A is reset, a high signal is generated from pin 6 as the complement of EN1- (Enable). In addition, XPOUT+ (X-Bus Priority Out) is forced low at pin 5 of 7A, which causes all X-Bus activity for modules farther down the X-Bus (that is, to the right of the Floppy/Hard Disk Module) to be suspended via connector J1, pin 117.

XPIN+ then becomes high to signify that the Processor Module wishes to identify the Floppy/Hard Disk Module (that is, assign the module a base I/O address).

The Processor Module reads I/O address ØØ from XADR8- through XADRF- (X-Bus Address Lines 8 through Fh) via connector J1, pins 6Ø through 64, 66, 76, and 77. The high eight address bits (XADR8- through XADRF-), which represent port ØØ, are buffered and inverted at 5F to the A-side inputs of comparator 5E. (Note that XPIN+ is inverted at 7F, pin 3, enabling 5F.) Since I/O Address register 5D was previously cleared at pin 1, the B-side inputs of comparator 5E also connect to eight low bits, and therefore compare as equal with the A-side inputs, signaling MSEL- (Module Select) from pin 19 of 5E.

During XIORD- (X-Bus I/O Read), shown in Figure 3-1, page 2, IORD- (I/O Read) is generated at buffer

10F (pin 3) via pin 86 of connector J1. As shown in Figure 3-1, page 6, IORD- is inverted at 6D (pin 14) and NANDed at gate 5A (pin 13) with the high signal from pin 6 of 7A, and with XPIN+ and MSEL+ (pins 10, 12, and 9, respectively). A low signal is, therefore, generated from 5A (pin 8), to enable buffers 8E and 9E (pins 1 and 19).

Note that any time the Floppy/Hard Disk Module is selected (signified by MSEL+, as shown in Figure 3-1, page 2) and either XIORD- or XIOWR- is pulsed (via connector J1, pin 86 or 87), XACK- is generated via connector J1, pin 90. XIORD- or XIOWR- is buffered at 10F (pin 17 or 15, respectively), generating IORD- or IOWR- at pin 3 or 5, respectively. Either IORD- or IOWR- forces NAND gate 8A to generate a high signal (pin 3), which is NANDed at gate 1E with MSEL+ at pins 2 and 1, respectively. This forces XACK- at pin 3, which is generated back to the Processor Module.

In summary, when a power-up or manual reset occurs, or when activity on the X-Bus for the Floppy/Hard Disk Module has been suspended, and the Processor Module issues an IORD- command to port 00, signified by four high signals at the input of NAND gate 5A (pins 10, 12, 13, and 9) shown in Figure 3-1, page 6, a low signal is generated (pin 8), enabling hard-wired buffers 8E and 9E, signifying that an I/O read of port 00 has occurred, causing the Floppy/Hard Disk Module to output its assigned identifier number.

Since 8E and 9E are hard-wired, low-order data lines D0+ through D7+ (Local Data Lines 0 thorugh 7) are assigned identifying bits (that is, an identifying code) of 70h, and high-order data lines D8+ through DF+ are assigned identifying bits of 10h. Therefore, 1070h represents the Floppy/Hard Disk Module.

Note that input signals at pins 11, 13, 15, and 17 of 9E are pulled high by 1-kilohm resistors at RP2. Future expansions connecting to DT0- through DT3- (Drive Type 0 Through 3), however, will vary the identifying code between 10h and 1Fh. Therefore, future identifying codes may range from 1070h through 1F70h.

Local module data lines D0+ through DF+ are interfaced to XDAT0- through XDATF- (X-Bus Data Lines 0 through F) via data transceivers 8F and 9F

(shown in Figure 3-1, page 2), which are enabled at pin 19 when MSEL+ forces a low signal at NOR gate 6A (pin 13). Since XIORD- is active at 8F and 9F (pin 1), data is directed from DØ+ through DF+ to XDATØ- through XDATF-.

In summary, during the I/O read of port ØØ, the Floppy/Hard Disk Module identifier, 1Ø7Øh, is generated to the Processor Module via the X-Bus data lines.

Once the Processor Module receives the 1Ø7Øh Floppy/Hard Disk Module identifier, it writes the base I/O address for the module into I/O Address register 5D (shown in Figure 3-1, page 6). This I/O address defines the range of I/O ports reserved for the Floppy/Hard Disk Module. The Processor Module issues an I/O address via low-order data lines DØ+ through D7+, and that becomes the high-order eight bits of the 256 I/O address range, for example, ØlXXh or Ø2XXh, depending upon the physical location of the Floppy/Hard Disk Module. During the identification polling sequence, the module adjacent to the Processor Module uses I/O ports Ø1ØØh through Ø1FFh, the next module uses Ø2ØØh through Ø2FFh, and so on. The module identifier is stored in a memory table for use by the system. (See Section 2, "Architecture.")

When the Processor Module writes the base I/O address to the Floppy/Hard Disk Module, IOWR- is inverted at 6D (pin 5) and driven to NAND gate 5A (pin 4). A low signal is generated from 5A (pin 6), clocking I/O Address register 5D (pin 11), which is loaded with the base I/O address sent by the Processor Module.

Note that the following conditions are input at 5A during an I/O write to load 5D:

- MSEL+ (pin 5)
- High signal (pin 1) generating from 7A (pin 6) as a result of the reset or suspended activity of the Floppy/Hard Disk Module
- High signal at pin 2, generating from pin 5 of D flip-flop 12A. During the IORD- cycle, 12A is clocked at pin 3 to generate a high signal at pin 5 (resulting from XPIN+ at pin 2), This high signal connects at 5A (pin 2).

Since the inputs at 5D consist of the module base I/O address, the outputs of 5D do not compare with the outputs of 5F at comparator 5E. Therefore, a high signal is generated from 5E (pin 19). Simultaneously, D flip-flop 7A is clocked (pin 3), and a low signal is generated at pin 6. This low signal forces NAND gate 5A high at pin 8, disabling module identifier buffers 8E and 9E (pins 1 and 19).

In addition, just as with XIORD-, XACK- is pulsed from pin 3 of NAND gate 1E (shown in Figure 3-1, page 2).

As shown in Figure 3-1, page 6, once flip-flop 7A is set and XPOUT+ is generated from pin 5, the low signal at pin 6 of 7A disables the gates at 5A at pins 1Ø and 1, and only the address written into I/O Address register 5D causes the module to respond to an I/O read or write operation from the X-Bus master. A high signal is generated from pin 5 of 7A as EN1+. As shown in Figure 3-1, page 7, EN1+ is inverted at gate 1D (pin 7) and driven as MODENLITE- (Module Enable Light) via connector J1, pin 56, indicating that the module has been identified.

To summarize, input/output reads or writes to addressable devices within the Floppy/Hard Disk Module, such as the WD2797-Ø2, WD1Ø1Ø, or one of the 8253 programmable interval timers, are performed when the Processor Module places a base address for the Floppy/Hard Disk Module (such as ØlXX, Ø2XX, and so on) on the XADR8- through XADRF- lines and the address for the register within the device (such as XXØl, XXØ2, and so on) on the XADRl- through XADR5- address lines. Next, data is placed on the XDATØ- through XDAT7- data lines while either XIORD- or XIOWR- is asserted.

Note in Figure 3-1, page 6, that XDMAEN- (X-Bus Direct Memory Access Enable), which indicates that a DMA cycle is in progress, causes comparator 5E to become disabled at pin 1. During a DMA cycle, the XADR8- through XADRF- lines may contain memory address data not to be mistaken for a module base I/O address.

LOCAL MODULE DATA BUS INTERFACE

X-BUS DATA INTERFACE

Transceivers 8F and 9F (shown in Figure 3-1, page 2) are used as the interface between local module data lines DØ+ through DF+ and X-Bus data lines XDATØ- through XDATF- (from connector J1, pins 91 through 94, 96 through 1Ø4, and 1Ø6 through 1Ø8). The low-order data byte is connected to 8F, and the high-order data byte is connected to 9F.

Both transceivers enable when either ACK+ (Acknowledge) or MSEL+ are active at NOR gate 6A (pin 12 or 11, respectively). ACK+, which signifies an I/O read or I/O write, is generated when the X-Bus master issues XDACK3- (X-Bus DMA Acknowledge, Priority 3) via connector J1, pin 57 (as shown in Figure 3-1, page 5). XDACK3- is inverted at 7F (pin 9) and driven as ACK+. MSEL+, which signifies that the Floppy/Hard Disk Module has been selected, is generated when pin 19 of comparator 5E (shown in Figure 3-1, page 6) becomes active-low. This low signal is inverted at 6D (pin 12) as MSEL+. (See the "X-Bus Module Identification" subsection, above.)

In summary, when either ACK+ or MSEL+ (shown in Figure 3-1, page 2) is active at NOR gate 6A, a low signal is generated from pin 13, enabling 8F and 9F at pin 19.

During an X-Bus master I/O read cycle, XIORD- (via connector J1, pin 86) directs local module data lines DØ+ through DF+ to X-Bus data lines XDATØ- through XDATF-. During an X-Bus master I/O write cycle, XIORD- becomes inactive, and data is directed from XDATØ- through XDATF- to DØ+ through DF+.

FLOPPY DISK CONTROLLER DATA INTERFACE

Transceiver 4D (shown in Figure 3-1, page 2) is used as the interface between local module data lines DØ+ through D7+ and local floppy disk data lines MDØ+ through MD7+ (Floppy Data Lines Ø through 7). Transceiver 4D is enabled at pin 19 when Programmable Array Logic (PAL) chip 13E (Figure 3-1, page 5) issues MDEN- (Floppy Data Enable) from pin 12.

MDEN- is active when any of the following conditions are met at 13E:

- 2797CS- is active at pin 9
- 8253CS- is active at pin 11
- W8253EN- is active at pin 17

2797CS-, 8253CS-, and W8253EN- are generated from 1-of-8 decoder 11F as described in the "Floppy/Hard Disk Module Device Decoding" subsection, below.

During an I/O read cycle, IORD-, which connects at pin 1 of 4D, directs local floppy disk data lines MDØ+ through MD7+ to local module data lines DØ+ through D7+. During an I/O write cycle, IORD- becomes inactive, and data is directed from DØ+ through D7+ to MDØ+ through MD7+.

HARD DISK CONTROLLER DATA INTERFACE

Transceiver 1ØE (shown in Figure 3-1, page 2) is used as the interface between local module data lines DØ+ through D7+ and local hard disk data lines WDØ+ through WD7+ (Winchester Data Lines Ø through 7). Transceiver 1ØE is enabled at pin 19 when WD1Ø1ØCS- is generated from 1-of-8 decoder 11F at pin 12 or 13 (see Figure 3-1, page 7, and the "Floppy/Hard Disk Module Device Decoding" subsection), and when either of the following occurs:

- START+ is active at PAL 7E (pin 12), shown in Figure 3-1, page 5, which indicates that a DMA cycle is in progress.
- DSBLRW+ (Disable Read/Write) is not asserted from the X-Bus master via X-Bus Extended Address register 6E (pin 2) shown in Figure 3-1, page 4. (See the "Hard Disk Drive Controller Logic" subsection, below.)

As shown in Figure 3-1, page 2, either of these conditions causes NOR gate 6A to generate a low signal from pin 1Ø, enabling the tristate buffer 1ØF at pin 1. When enabled, WD1Ø1ØCS- (which was issued to enable the WD1Ø1Ø) is generated from pin 16, which loops back to pin 2 and, consequently, is driven from pin 18 to 1ØE (pin 19).

During an I/O read cycle, IORD-, which connects at pin 1 of 1ØE, directs local hard disk data lines WDØ+ through WD7+ to local module data lines DØ+ through D7+. During an I/O write cycle, IORD- becomes inactive, and data is directed from DØ+ through D7+ to WDØ+ through WD7+.

TRANSFER ACKNOWLEDGE GENERATION

During an I/O read or I/O write cycle, IORD- or IOWR- forces NAND gate 8A (pin 3) high as IORDWR+ (I/O Read or Write) as shown in Figure 3-1, page 2. IORDWR+ is NANDed with MSEL+ (signifying that the Floppy/Hard Disk Module has been selected) at gate 1E (pin 2 and 1, respectively) to generate XACK- (Transfer Acknowledge) back to the X-Bus master via connector J1, pin 90.

FLOPPY/HARD DISK MODULE DEVICE DECODING

As shown in Figure 3-1, page 7, 1-of-8 decoder 11F decodes X-Bus address lines XADR3- through XADR5- to generate appropriate read/write commands. Decoder 11F is enabled at pins 4, 5, and 6 when the following conditions are met:

- The Floppy/Hard Disk Module has been selected, signified by MSEL- at pin 4.
- Neither a power-up reset nor a manual reset has been performed, signified by EN1- at pin 5.
- The bootstrap ROM routine is not in progress, signified by an inactive BOOTEN- (Boot Enable) at pin 6.

X-Bus address lines XADR3- through XADR5-, which connect at connector J1, pins 82, 80, and 79, drive 11F (pins 1, 2, and 3, respectively) to output the following:

XADR5-	XADR4-	XADR3-	Port* (h)	Pin	Signal	Function
Ø	Ø	Ø	XX38-XX3F	15	N/A	Unused
Ø	Ø	1	XX3Ø-XX37	14	W8253EN-	Enables 8253, which is used in conjunction with WD1Ø1Ø
Ø	1	Ø	XX28-XX2F	13	WD1Ø1ØCS-	Enables WD1Ø1Ø and associated transceivers
Ø	1	1	XX2Ø-XX27	12	WD1Ø1ØCS-	Enables WD1Ø1Ø and associated transceivers
1	Ø	Ø	XX18-XX1F	11	N/A	Unused
1	Ø	1	XX1Ø-XX17	1Ø	8253CS-	Enables 8253, which is used in conjunction with WD2797-Ø2
1	1	Ø	XXØ8-XXØF	9	FCRCS-	Enables decoder 12F during I/O write cycle (see below)
1	1	1	XXØØ-XXØ7	7	2797CS-	Enables WD2797-Ø2

*XX represents the base I/O address

As shown above, 1-of-8 decoder 12F is enabled when the following conditions are met:

- o XADR3- is low
- o XADR4- and XADR5- are high
- o an I/O write cycle is in progress

In other words, when 11F issues FCRCS- (Floppy Controller Register Chip Select), which represents addresses XX08h through XX0Fh, during an IOWR- cycle, 12F enables at pins 4, 5, and 6. (Note that the pin 6 enable of 12F is strapped to +5 V.)

X-Bus address lines XADR1- through XADR3-, which connect at connector J1, pins 84, 83, and 82, drive 12F (pins 1, 2, and 3, respectively) to output the following:

XADR3-	XADR2-	XADR1-	Port* (h)	Pin	Signal	Function
0	0	0	XX0E	7	LD4-	Used to clock X-Bus Address Control register 6E
0	0	1	XX0C	9	N/A	Unused
0	1	0	XX0A	10	LD1-	Used to clock Hard Disk Drive Control register 3E
0	1	1	XX08	11	LD0-	Used to clock Floppy Disk Drive Control register 2E

*XX represents the base I/O address

FLOPPY DISK DRIVE CONTROLLER LOGIC

INTRODUCTION

The WD2797-Ø2 floppy disk formatter/controller (2C), shown in Figure 3-1, page 7, provides most of the circuitry necessary to control the floppy disk drive, including a phase-locked loop data separator, write precompensation circuitry, address mark generation and detection circuitry, and CRC circuitry. The WD2797-Ø2 clock can operate at 1 MHz during read or write operations, or at 2 MHz to enable track seeks at 3 milliseconds per track. A functional block diagram of the floppy disk drive controller logic is provided in Figure 3-2. The pin assignments and functions for 2C are listed in Table 3-1.

Table 3-1. WD2797-Ø2 Floppy Disk Formatter/Controller Pin Assignments and Functions. (Page 1 of 5)

Pin	Function
1	**Enable Write Precompensation (ENP+).** When high, enables write precompensation to be performed on the write data output; tied to pin 29, TG43+ (Track Greater Than 43).
2	**Write Enable (WE-).** When low, causes data on the DØ+ through D7+ data lines to be written into a register previously selected with the AØ+ and A1+ lines; CS- (pin 3) must be low.
3	**Chip Select (CS-).** When low, selects the WD2797-Ø2 and allows X-Bus communication with it.
4	**Read Enable (RE-).** When low, causes data to be read from a register previously selected with the AØ+ and A1+ lines and placed on the DØ+ through D7+ data lines; CS- (pin 3) must be low.
5, 6	**Register Selection Lines (AØ+, A1+).** Used to select the register to receive or transmit data on the DØ+ through D7+ data lines under control of the RE- and WE- strobes as follows:

A1+	AØ+	RE-	WE-
Ø	Ø	Status	Command
Ø	1	Track	Track
1	Ø	Sector	Sector
1	1	Data	Data

Table 3-1. WD2797-Ø2 Floppy Disk Formatter/Controller Pin Assignments and Functions. (Page 2 of 5)

Pin	Function
7 - 14	**Data Line Ø Through Data Line 7 (DØ+ - D7+).** Bidirectional data lines used to transfer commands, status information, and data between the X-Bus and the WD2797-Ø2.
15	**Step (STEP+).** Output that pulses once for every track that the drive read/write head will cross.
16	**Direction (DIRC+).** When high, the read/write head is stepping in (toward the spindle); when low, the read/write head is stepping out (toward the edge of the floppy disk).
17	**Size Select (5-/8+).** Input must be low to select 5.25-in. floppy disk drive and 1-MHz clock during read/write oeprations. During seek operations, this line is high to select 2-MHz clock.
18	**Read Pulse Width (RPW+).** Input connected to external resistors to control the phase comparator within the data separator of the WD2797-Ø2.
19	**Master Reset (MR-).** When low, the WD2797-Ø2 resets and loads Ø3h into the Command register. The Not Ready bit (bit 7) of the Status register is also reset. When it becomes high, a restore command executes, regardless of the state of the Ready signal from the floppy disk drive. In addition, Ølh is loaded into the Sector register.

Table 3-1. WD2797-Ø2 Floppy Disk Formatter/Controller Pin Assignments and Functions. (Page 3 of 5)

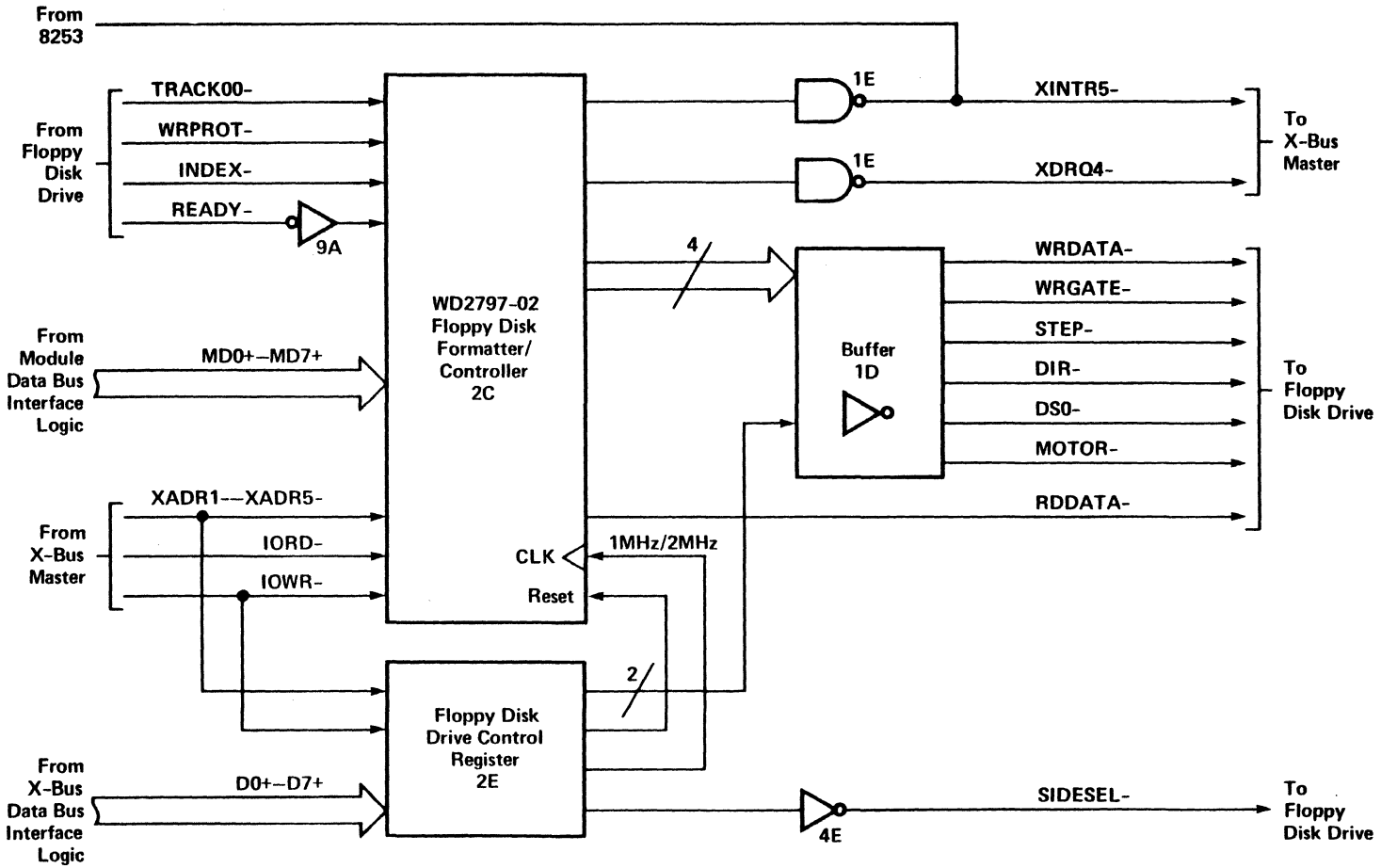
Pin	Function
2Ø	**Ground (GND).**
21	**Power (VCC).** Strapped to +5 V.
22	**Test (TEST-).** When low, enables internal signals to appear on selected pins of the WD2797-Ø2. (TEST- can be used to verify that the RPW+ resistors R8 and R9, and the WPW+ resistors R1Ø and R11 are correct.)
23	**Pump (PUMP+).** High-impedance output signal, which is forced high or low to increase or decrease the voltage-controlled oscillator (VCO) frequency.
24	**Clock (CLK+).** Input that supplies the clock for the internal circuitry of the WD2797-Ø2. The frequency of CLK+ is 1 MHz during read or write commands and 2 MHz during seeks.
25	**Side Select Output (SSØ+).** Not used.
26	**Voltage-Controlled Oscillator (VCO).** Input that is connected to capacitor C22 to adjust the center frequency of the VCO.
27	**Read Data (RDDATA-).** Data input signal from the floppy disk drive. The input is a negative pulse for each recorded flux transition.
28	**Head Load (HLD+).** Output that controls loading of the read/write head against the floppy disk media; connected to the HLT+ input (pin 4Ø).

Table 3-1. WD2797-Ø2 Floppy Disk Formatter/Controller Pin Assignments and Functions. (Page 4 of 5)

Pin	Function
29	**Track Greater than 43 (TG43+).** Output that informs the floppy disk drive when the read/write head is positioned between tracks 44 through 76; valid only during a read or write command.
3Ø	**Write Gate (WG+).** Output that is valid before data is written on the floppy disk.
31	**Write Data (WRDATA+).** Output that issues a 25Ø-nsec (MFM) pulse for each flux transition written on the floppy disk; contains the unique address marks as well as data and clocks for the floppy disk drive.
32	**Ready (READY+).** Input that indicates floppy disk drive readiness; sampled for a high state before read or write commands are performed. If low, the read or write command is not performed, and an interrupt is generated. Type 1 commands are performed regardless of the state of READY+. (See Section 2, "Architecture.") The READY+ input appears in inverted format as Status register bit 7.
33	**Write Precompensation Width (WPW+).** External resistors tied to this input control the amount of delay in the write precompensation mode.
34	**Track ØØ (TRØØ-).** Input from the floppy disk drive, indicating that the read/write head is over track ØØ.

Table 3-1. WD2797-Ø2 Floppy Disk Formatter/Controller Pin Assignments and Functions. (Page 5 of 5)

Pin	Function
35	**Index Pulse (IP-).** Input from the floppy disk drive, indicating that the index hole on the floppy disk has been encountered.
36	**Write Protect (WPRT+).** Input sampled whenever a write command is received by the WD2797-Ø2 A low at this input terminates the write command and sets the write-protect bit in the Status register. (See Section 2, "Architecture.")
37	**Double Density (MFM+).** Input tied to ground, selecting double density (MFM) encoding of data.
38	**Data Request (DRQ+).** Output indicating that the Data register of the WD2797-Ø2 contains asembled data in read operations, or the Data register is empty in write operations. This signal is reset when serviced by the Processor Module through reading or loading of the Data register. (See Section 2, "Architecture.")
39	**Interrupt Request (INTRQ+).** Output that is set at the completion of any command and is reset when the Status register is read from or the Command register is written to. (See Section 2, "Architecture.")
4Ø	**Head Load Timing (HLT+).** Connected to the HLD+ output (pin 28) of 2C to control the head load timing.



3-2. Floppy Disk Controller Logic Functional Block Diagram.

GENERAL OPERATION

As shown in Figure 3-1, page 7, the WD2797-Ø2 formatter/controller, shown as 2C, is enabled at pin 3 when 11F generates 2797CS- from pin 7, signifying addresses XXØØh through XXØ7h. (See "Floppy/Hard Disk Module Device Decoding," above.) When 2C is selected, the X-Bus master can select one of several registers by using XADR1- and XADR2- X-Bus address lines and can read from, or write to, the selected register by using the XDATØ- through XDAT7- lines to transfer data. (See "X-Bus Data Interface," above.) XADR1- is inverted at pin 14 of 7F before generating to 2C (pin 5) as AØ+. XADR2- is inverted at 7F (pin 12) before generating to 2C (pin 6) as A1+.

Read operations are indicated when XIORD- generates through pin 3 of buffer 1ØF (Figure 3-1, page 2) to the RE- (Read Enable) input of 2C at pin 4, shown in Figure 3-1, page 7. Similarly, write operations are indicated when XIOWR- generates through pin 5 of 1ØF (Figure 3-1, page 2) to the WE- (Write Enable) input of 2C at pin 2. Internal registers of 2C are listed below with their addresses in the module relative to the module base I/O address, XXh:

A1+	AØ+	Read Register (RE-)	Write Register (WE-)
Ø	Ø	Status (XXØØh)	Command (XXØØh)
Ø	1	Track (XXØ2h)	Track (XXØ2h)
1	Ø	Sector (XXØ4h)	Sector (XXØ4h)
1	1	Data (XXØ6h)	Data (XXØ6h)

When the X-Bus master performs a read or write operation to the floppy disk drive, it writes data into the WD2797-Ø2 (2C) Sector and Track registers and then writes the command byte into the Command register. If a read operation is commanded, 2C assembles a serial byte from the floppy disk drive, loads it into the Data register, and sets the DRQ+ (DMA Request) line at pin 38 high (as shown in Figure 3-1, page 7). DRQ+ is inverted at NAND gate 1E and sent to the X-Bus master to request service as XDRQ4- (X-Bus DMA Request, Priority 4) via connector J1, pin 59. The X-Bus master reads the Data register at address XXØ6h

for the byte. This continues for all bytes requested in the command. When the command has been completed, 2C interrupts the X-Bus master through its INTRQ+ (Interrupt Request) line at pin 39. INTRQ+ is inverted at pin 8 of NAND gate 1E and sent to the X-Bus master as XINTR5- (X-Bus Interrupt, Priority 5) via connector J1, pin 114, to request a new command sequence. Finally, as shown in Figure 3-1, page 6, the X-Bus master sets XDMAEN- high again, to signify that a DMA cycle is not in progress.

A write to the floppy disk drive occurs in the same manner, except that DRQ+ is set when 2C requires a byte from the X-Bus master. Again, 2C requires a byte from the X-Bus master when it has completed the command.

FLOPPY DISK DRIVE CLOCK LOGIC

Data bit 6 of the Floppy Disk Drive Control register (2E in Figure 3-1, page 7), controls the frequency of the 1- or 2-MHz clock used to control operations of the WD2797-Ø2 shown as 2C. If data bit 6 is set, MUX- (Multiplex) becomes high before it is multiplexed at 7B (Figure 3-1, page 4) to produce a 2-MHz FPCLK- (Floppy Clock) at pin 6. If data bit 6 is reset, MUX- is inverted at pin 12 of 9A before it is multiplexed at 7B to produce a 1-MHz FPCLK- at pin 6. FPCLK- is generated to pin 24 of 2C as shown in Figure 3-1, page 7.

Note in Figure 3-1, page 4, that the 2-MHZ+ pulse is generated by 4-bit binary counter 7D (pin 1Ø). Counter 7D is clocked by a 1Ø-MHz pulse (pin 13), which originated at 2Ø-MHz oscillator 1ØA. The 2-MHz pulse is divided by two at D flip-flop 9B (pin 5), generating 1MHZ+.

FLOPPY DISK DRIVE INTERFACE LOGIC

The interface between the WD2797-Ø2 formatter/controller and the floppy disk drive consists of a Floppy Disk Drive Control register for drive selection, motor control, and clock pulses, and of one buffer for data and control signals.

Control Signals

The following signals shown in Figure 3-1, page 7, are buffered and inverted at 1D directly from the WD2797-Ø2 (2C):

Signal	1D Pin	J1 Connector Pin	Function
WRDATA-	18	3Ø	Write Data: 25Ø-nsec pulse for each flux transition written on the floppy disk
WRGATE-	5	29	Write Gate: When low, allows data to be written
STEP-	16	27	Step Pulse: Pulse for every track that the drive read/write head will cross
DIR-	3	28	Step Direction: When high, signifies read/write head stepping in toward spindle; when low, signifies read/write head stepping out

The following control signals originate from Floppy Disk Drive Control register 2E during read/write operations from or to port XXØ8h:

Signal	Data Bit	2E Pin	J1 Connector Pin	Function
DSO-	Ø	2	23	Drive Select Ø: Signal from the X-Bus master that selects floppy disk drive; also enables floppy disk drive light via connector J1, pin 54, as DØLITE- (Drive Ø Light)
MOTOR-	2	5	24	Drive Motor On: Signal from the X-Bus master that turns on the floppy disk drive motor
SIDESEL-	5	7	33	Side Select: If set, side 1 will be used for operation; if reset, side Ø will be used for operation
MUX-	6	1Ø	N/A	Multiplex: Used by the floppy disk formatter/ controller to select 2-MHz clock during seek operations and 1-MHz clocks during read and write operations (see "Floppy Disk Clock Logic," above)

Note that signals from pin 12 of 2E (data bit 7) control the master reset of 2C (pin 19), and that pin 15 of 2E is unused.

Status Signals

The following status signals, which originate at the floppy disk drive, connect to the WD2797-Ø2 (2C) as follows:

Signal	J1 Connector Pin	2C Pin	Function
TRACKØ-	32	34	Track Ø Detected: Indicates that the read/write head is over track ØØ
WRPROT-	31	36	Floppy Write Protected: Pulse during a write command (low signal) terminates write command and sets write-protect bit in the internal Status register
INDEX-	26	35	Index Mark Detected: Indicates that index hole on the floppy disk has been encountered
READY-	36	32	Drive Ready: Indicates whether floppy disk drive is ready (high pulse at pin 32 indicates a read or write command; low pulse indicates read or write command is not performed)

HARD DISK DRIVE CONTROLLER LOGIC

INTRODUCTION

The hard disk drive controller circuitry in the Floppy/Hard Disk Module is built around the WD1Ø1Ø Winchester disk controller (12C) shown in Figure 3-1, page 2, which provides the following:

- multiple sector read/write commands
- CRC generation/verification circuitry
- data rates up to 5M bits per second (bps)
- automatic restore on seek errors

A functional block diagram of the hard disk drive controller logic is provided in Figure 3-3. The pin assignments and functions of 12C are listed in Table 3-2.

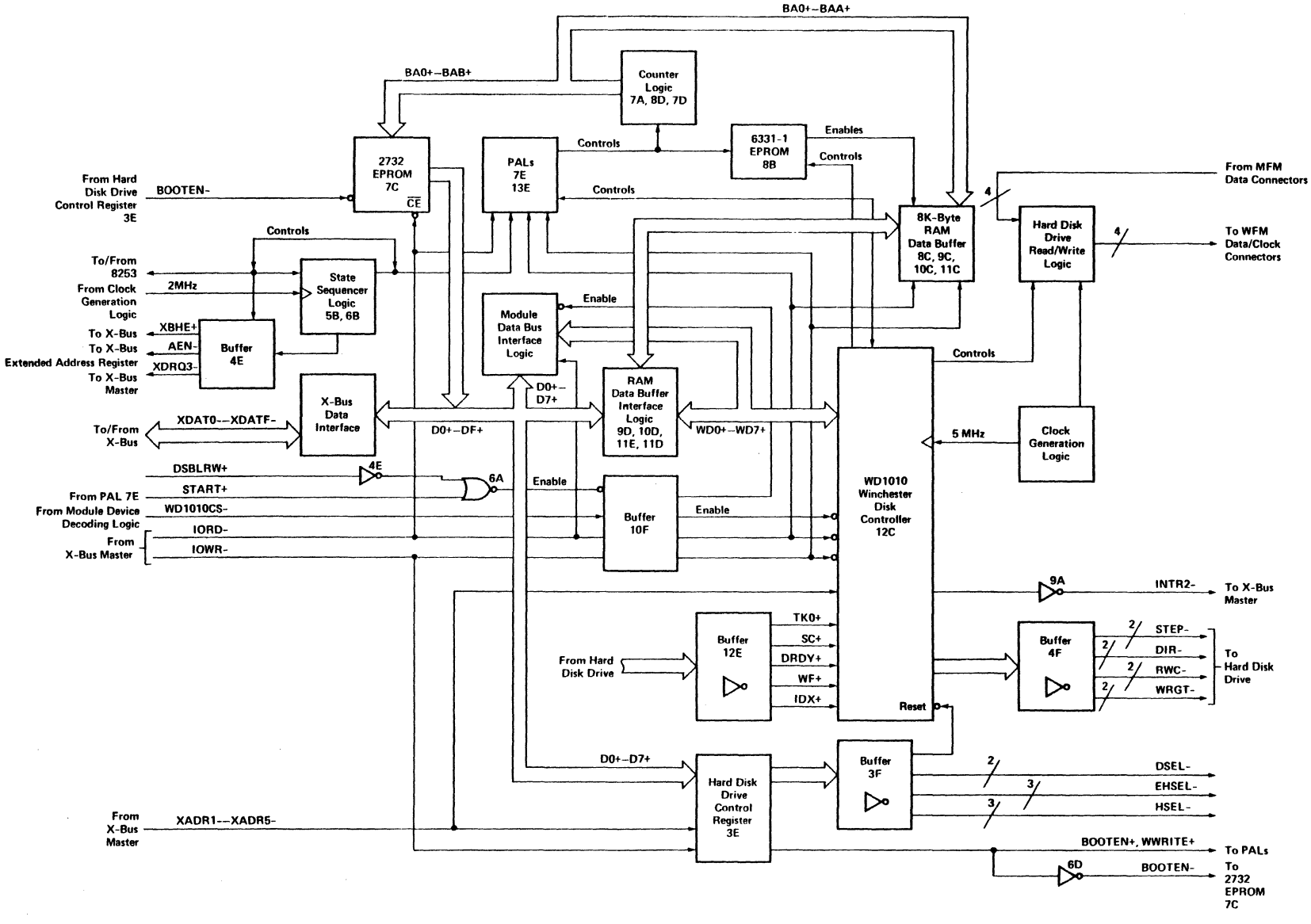


Figure 3-3. Hard Disk Controller Logic Functional Block Diagram.

Table 3-2. WD1Ø1Ø Winchester Disk Controller Pin Assignments and Functions. (Page 1 of 3)

Pin	Function
1	**Buffer Chip Select (BCS-).** Active-low output used for selecting external RAM data buffer.
2	Unused.
3	**Interrupt Request (INTRQ+).** Output that is set high at the completion of any command.
4	Must be an open circuit.
5	**Master Reset (MR-).** Input used to intialize all internal logic.
6	**Read Enable (RE-).** Bidirectional line used as an input for reading the Task registers and an output when 12C reads the RAM data buffer; tristate.
7	**Write Enable (WE-).** Bidirectional line used as an input for writing into the Task registers and as an output when 12C writes to the RAM data buffer; tristate.
8	**Chip Select (CS-).** Used to enable 12C.
9 - 11	**Address Lines (AØ+ Through A2+).** Used to select the internal register to transmit/receive data on the DØ+ through D7+ data bus.
12 - 19	**Data Bus (DØ+ Through D7+).** Bidirectional bus used to transfer commands, status information, and data.
2Ø	Ground.

Table 3-2. WD1Ø1Ø Winchester Disk Controller Pin Assignments and Functions. (Page 2 of 3)

Pin	Function
21	**Write Data (WD+).** Output that contains the MFM clock and data pulses to be written on the disk.
22, 23	Unused.
24	**Write Gate (WG+).** Output set high before a write is performed on the disk.
25	**Write Clock (WC+).** 5-MHz clock input used to derive internal write timing.
26	**DIR+ (Direction).** Output that determines the direction of the stepping motor.
27	**Step Pulse (STEP+).** Output pulses used for the stepping motor.
28	**Drive Ready (DRDY+).** Input that must be high to allow the execution of commands.
29	**Index Pulse (IDX+).** Input that informs 12C when the index hole has been encountered.
3Ø	**Write Fault (WF+).** Error input to 12C that indicates a fault condition at the drive.
31	**Track ØØØ (TKØ+).** Input that indicates the read/write heads are positioned over the outermost cylinder.
32	**Seek Complete (SC+).** Input that informs 12C when head settling time has expired.

Table 3-2. WD1Ø1Ø Winchester Disk Controller Pin Assignments and Functions. (Page 3 of 3)

Pin	Function
33	**Reduced Write Current (RWC+).** Programmed output used to reduce write current on a selected starting cylinder.
34	**Data Run (DRUN+).** Input that informs 12C when a string of 1s or Øs has been detected.
35	**Buffer Ready (BRDY+).** Input that informs 12C that the sector RAM data buffer is full or empty.
36	**Buffer Data Request (BDRQ+).** Output set to initiate data transfers to/from the sector RAM data buffer.
37	**Read Data (RD+).** Input from the hard disk drive; consists of both MFM clocks and data pulses.
38	**Read Gate (RG+).** Output set high when data is being inspected from the hard disk.
39	**Read Clock (RCLK+).** Square-wave clock input derived from the external data recovery circuits.
4Ø	**Power (+5 V).** Power supply input.

GENERAL OPERATION

The WD1Ø1Ø (12C) controls the hard disk drives in both the Floppy/Hard Disk Module and the Hard Disk Expansion Module.

The X-Bus master selects 12C via 1-of-8 decoder 11F (Figure 3-1, page 7) as described in the "Floppy/Hard Disk Module Device Decoding"

subsection, above. A low signal at pin 12 of 11F (representing addresses XX20h through XX27h) is inverted at pin 16 of 7F and NORed at gate 6A to generate WD1Ø1ØCS- at pin 4. Note that a low signal at pin 13 of 11F (representing addresses XX28h through XX2Fh) is inverted at pin 9 of 6D and also forces NOR gate 6A (pin 4) low as WD1Ø1ØCS-.

As shown in Figure 3-1, page 2, WD1Ø1ØCS- is buffered at tristate buffer 1ØF, which is enabled at pin 1.

A disk operation begins when the X-Bus master writes task information into the Task registers of 12C. (See Section 2, "Architecture," for task information.) After the task information has been written, the X-Bus master writes the command into the Command register. During a write sector command, the X-Bus master can then read the status of 12C to inspect the buffer data request flag, and write data into the RAM data buffer. (See the "Hard Disk Drive Controller RAM Data Buffer" subsection, below.)

When the RAM data buffer becomes full, it activates the BRDY+ (Buffer Ready) input of 12C. Then, 12C de-asserts the BDRQ+ (Buffer Data Request) line and asserts BCS- (Buffer Chip Select) allowing 12C to have a direct bus to the RAM data buffer, which is isolated from the X-Bus read/write control lines. The X-Bus data bus cannot access 12C (because of tristate buffer 1ØF). When the buffered data is transferred to the hard disk, and the RAM data buffer is empty, START+ enables tristate buffer 1ØF, thereby reconnecting the two buses. The X-Bus can then read or write status/commands from or to 12C.

DISABLE READ/WRITE

The X-Bus master uses DSBLRW+ (Disable Read/Write) to disable the X-Bus read/write control lines to 12C so that these lines do not interfere with the read/write signals of 12C, which are used for incrementing the RAM data buffer. (See the "RAM Chip Selection and Addressing" subsection, below.)

As shown in Figure 3-1, page 4, the X-Bus master sets data bit 7 of X-Bus Extended Address register 6E (port XXØEh) to generate DSBLRW+ from pin 2.

As shown in Figure 3-1, page 2, DSBLRW+ is inverted at pin 14 of 4E and NORed with an inactive START+ at gate 6A (pins 9 and 8, respectively), generating a high signal at pin 10, which disables buffer 10F at pin 1. (An inactive START+ signifies that a DMA cycle is not in progress.)

HARD DISK DRIVE CLOCK LOGIC

As shown in Figure 3-1, page 4, the reference clock for the hard disk drive read and write circuitry is a 20-MHz crystal oscillator, 10A. It clocks J-K flip-flop 10B (pin 1) to generate a 10-MHz frequency at pin 5. This 10-MHz signal is used at multiplexer 11A (pin 2) as a 10-MHz phase-locked loop reference when RG+ (Read Gate) at pin 38 of the WD1010 (12C) is not asserted. (See the "Hard Disk Drive Read/Write Circuitry" subsection, below.)

In addition, this 10-MHz frequency is divided by two at J-K flip-flop 10B (pin 9) as a 5-MHz pulse, which is used to derive internal write timing at 12C (pin 25).

A 10-MHz signal is also generated from pin 6 of 10B to pin 11 of D flip-flop 1F for use with the MFM clock/data output to driver 2F.

Four-bit binary counter 7D is used to divide the 10-MHz signal down to a 2-MHz pulse at pin 10. This 2-MHz pulse clocks counter 2 of 8253 programmable interval timer 5C (shown in Figure 3-1, page 5), which is used to count the time elapsed after one DMA burst. In addition, 2MHZ+ is used to clock the state sequencer chips 5B and 6B. (See the "State Sequencer" subsection, below.)

HARD DISK DRIVE INTERFACE LOGIC

The applicable hard disk drive is selected when the X-Bus master writes to port XX0Ah as described in the "Floppy/Hard Disk Drive Module Device Decoding" subsection. As shown in Figure 3-1, page 7, LD1- (Load 1) is generated from pin 10 of 1-of-8 decoder 12F when the X-Bus master writes to address XX0Ah. LD1- clocks Hard Disk Drive Control register 3E at pin 11 (See Figure 3-1,

page 3), to generate signals through buffer 3F, which is enabled at pins 1 and 19. Note that 3F inverts the signals connecting from 3E.

Control Signals

The control data bits written to 3E and the corresponding output functions at connector J1 are as follows:

Data Bit	Signal	J1 Connector Pin	Function
Ø	DSELØ-	3	Drive Select Ø: Signal from the X-Bus master that selects the Floppy/Hard Disk Module hard disk drive
1	DSEL1-	47	Drive Select 1: Signal from the X-Bus master that selects the Expansion Module hard disk drive
3	HSELØ-/ EHSELØ-	9 48	Head Select Ø/ Expansion Head Select Ø: Signal from the X-Bus master that selects either Floppy/Hard Disk Module hard disk head Ø or Expansion Module hard disk head Ø (depending on data bits Ø and 1)
4	HSEL1-/ EHSEL1-	1Ø 46	Head Select 1/ Expansion Head Select 1: Signal from the X-Bus master that selects either Floppy/Hard Disk Module hard disk head 1 or Expansion Module hard disk head 1 (depending on data bits Ø and 1)

Data Bit	Signal	J1 Connector Pin	Function
5	HSEL2-/ EHSEL2-	16 47	Head Select 2/ Expansion Head Select 2: Signal from the X-Bus master that selects either Floppy/Hard Disk Module hard disk head 2 or Expansion Module hard disk head 2 (depending on data bits Ø and 1)

Data bits written to 3E to perform other functions are as follows:

Data Bit	Signal	Function
2	BOOTEN-/ BOOTEN+	Used to enable boot ROM
6	WWRITE+	Used to activate BRDY+ input to the WD1Ø1Ø, indicating a hard disk write operation is in progress
7	1Ø1ØRST-	Initializes all internal logic of the WD1Ø1Ø

The Hard Disk Drive Control register is disabled via DISBL- (Disable), which is generated from PAL 7E at pin 14, shown in Figure 3-1, page 5. (See the "Programmable Array Logic" subsection in Section 2, "Architecture," for programming information on 7E.)

Stepping Signals (Status)

To perform stepping, the Command register of the WD1010, shown as 12C in Figure 3-1, page 2, is loaded from the X-Bus master. Then 12C reads the status lines from the hard disk drive via buffer 12E as follows:

Signal	J1 Connector Pin	12C Pin	Function
WTRACK0-	11	31	Winchester Track 0: Indicates read/write heads are positioned over the outermost cylinder
SKCMLT-	14	32	Seek Complete: Indicates when head settling time has expired
WREADY-	8	28	Winchester Drive Ready: Allows the execution of commands
WFAULT-	12	30	Write Fault: Indicates a faulty head
WINDEX-	7	29	Winchester Index Pulse: Indicates that the index magnet has been encountered

Stepping Signals (Controls)

After reading the status lines,/ the WD1010 issues the following signals through buffer 4F (which inverts the signals) to the J1 connector, which connects to the selected hard disk drive:

Signal	12C Pin	J1 Connector Pin	Function
STEP+	27	6, 51	STEP1-/STEP2-: Steps the motor of the selected hard disk drive
DIR+	26	4, 52	DIR1-/DIR2-: Determines direction of the selected stepping motor
RWC+	33	18, 49	RWC1-/RWC2-: Reduces write current on the selected starting cylinder
WG+	24	13, 50	WRGT1-/WRGT2-: Becomes high before a write is performed on the selected hard disk

When SKCMLT- (Seek Complete) indicates the completion of a seek, 12C issues INTRQ+ (Interrupt Request) at pin 3. INTRQ+ inverts at pin 10 of 9A, to enable 1C at pin 4. Pin 5 of 1C is tied to ground, forcing INTR2- (Interrupt Request, Priority 2) at pin 6. INTR2- connects to the X-Bus master processor via connector J1, pin 118.

HARD DISK DRIVE BOOT ROM

As shown in Figure 3-1, page 2, 4K-byte EPROM 7C contains the necessary information for the X-Bus master to boot from the hard disk drive.

The X-Bus master accesses 7C by setting data bit 2 of Hard Disk Drive Control register 3E (port XXØAh) shown in Figure 3-1, page 3. BOOTEN+ (Boot Enable) is inverted as BOOTEN- at pin 18 of 6D and driven to pin 18 of 7C, shown in Figure 3-1, page 2, enabling 7C.

During a DMA cycle, the X-Bus master issues an IORD- to pin 2Ø of 7C, enabling the output of DØ+ through D7+.

In addition, BOOTEN+ is generated to PAL 7E at pin 7 (Figure 3-1, page 5), and IORD- is generated to 7E (pin 3), causing 7E to generate ADRINC+ (Address Increment), which causes address counters 8D and 7D to increment (Figure 3-1, page 6). Buffered address lines BAØ+ through BAB+ are generated to 7C (Figure 3-1, page 2).

HARD DISK DRIVE CONTROLLER RAM DATA BUFFER

The RAM data buffer consists of four blocks of 2K by 8 bits (2K bytes) of static RAM, totaling 8K bytes. As shown in Figure 3-1, page 3, and Figure 3-4, two blocks consist of even-numbered low-order bytes (11C and 1ØC), and two blocks consist of odd-numbered high-order bytes (9C and 8C). Power feeds into the RAM chips at pin 24, and each chip is grounded at pin 12.

Buffered address lines BAØ+ through BAA+ are input at pins 1 through 8 and 19, 22, and 23. (See the "RAM Chip Selection and Addressing" subsection, below.) Data input/output lines are connected to pins 9 through 11 and 13 through 17. Either the X-Bus master or the WD1Ø1Ø pulses pin 21 as WDIOWR- to enable a write or pin 2Ø as WDIORD- to enable a read. The chip selects (pin 18) are controlled by 6331-1 PROM 8B, shown in Figure 3-1, page 6. (See Table 3-3 for the input and output functions of 8B.)

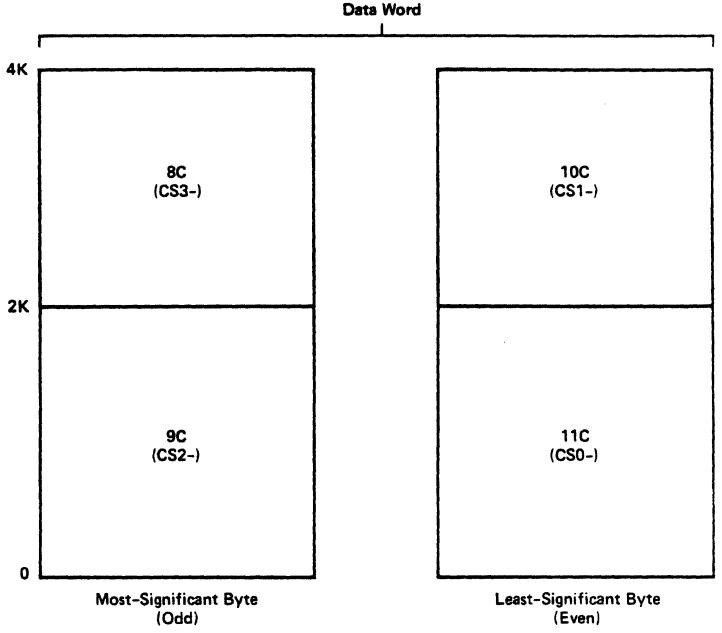


Figure 3-4. RAM Data Buffer Map.

Table 3-3. 6331-1 PROM Firmware Routine.

Pin Name		A4	A3	A2	A1	A0	08	07	06	05	04	03	02	01	
Pin No.		14	13	12	11	10	9	7	6	5	4	3	2	1	
Signal Name		BCS+	BDRQ+	ACK+	MS+	BAB+	CS3-	CS2-	MSEN-	DMA1EN-	DMA0EN-	LSEN-	CS1-	CS0-	
Adrs	00	0	0	0	0	0	1	1	1	1	1	1	1	1	FF
	01	0	0	0	0	1	1	1	1	1	1	1	1	1	FF
	02	0	0	0	1	0	1	1	1	1	1	1	1	1	FF
	03	0	0	0	1	1	1	1	1	1	1	1	1	1	FF
	04	0	0	1	0	0	1	1	1	1	1	1	1	1	FF
	05	0	0	1	0	1	1	1	1	1	1	1	1	1	FF
	06	0	0	1	1	0	1	1	1	1	1	1	1	1	FF
	07	0	0	1	1	1	1	1	1	1	1	1	1	1	FF
	08	0	1	0	0	0	1	1	1	1	1	1	1	1	FF
	09	0	1	0	0	1	1	1	1	1	1	1	1	1	FF
	0A	0	1	0	1	0	1	1	1	1	1	1	1	1	FF
	0B	0	1	0	1	1	1	1	1	1	1	1	1	1	FF
	0C	0	1	1	0	0	1	0	1	0	0	1	1	0	A6
	0D	0	1	1	0	1	0	1	1	0	0	1	0	1	65
	0E	0	1	1	1	0	1	0	1	0	0	1	1	0	A6
	0F	0	1	1	1	1	0	1	1	0	0	1	0	1	65
	10	1	0	0	0	0	1	1	1	1	1	0	1	0	FA
	11	1	0	0	0	1	1	1	1	1	1	0	0	1	F9
	12	1	0	0	1	0	1	0	0	1	1	1	1	1	9F
	13	1	0	0	1	1	0	1	0	1	1	1	1	1	5F
	14	1	0	1	0	0	1	1	1	1	1	1	1	1	FF
	15	1	0	1	0	1	1	1	1	1	1	1	1	1	FF
	16	1	0	1	1	0	1	1	1	1	1	1	1	1	FF
	17	1	0	1	1	1	1	1	1	1	1	1	1	1	FF
	18	1	1	0	0	0	1	1	1	1	1	1	1	1	FF
	19	1	1	0	0	1	1	1	1	1	1	1	1	1	FF
	1A	1	1	0	1	0	1	1	1	1	1	1	1	1	FF
	1B	1	1	0	1	1	1	1	1	1	1	1	1	1	FF
	1C	1	1	1	0	0	1	1	1	1	1	1	1	1	FF
	1D	1	1	1	0	1	1	1	1	1	1	1	1	1	FF
	1E	1	1	1	1	0	1	1	1	1	1	1	1	1	FF
	1F	1	1	1	1	1	1	1	1	1	1	1	1	1	FF

BCS+ = Buffer Chip Select from 12C
BDRQ+ = Buffer Data Request from 12C
ACK+ = DMA Request Acknowledged from the X-Bus master
MS+ = Odd byte of a word selected
BAB+ = Most significant bit of the RAM data buffer address counter

CS3- = Upper 2K buffer chip odd byte select
CS2- = Lower 2K buffer chip odd byte select
MSEN- = 12C to odd buffer data path enable
DMA1EN- = X-Bus master DMA to buffer data path enable
DMA0EN- = X-Bus master DMA to buffer data path enable
LSEN- = 12C to even buffer data path enable
CS1- = Upper 2K buffer chip even byte select
CS0- = Lower 2K buffer chip even byte select

RAM CHIP SELECTION AND ADDRESSING

When the WD1Ø1Ø (12C) is reading from or writing to the RAM data buffer, BCS- (Buffer Chip Select) is inverted at pin 3 of 12E (Figure 3-1, page 2) and driven as BCS+ to pin 14 of 8B (Figure 3-1, page 6). This causes 8B to generate CSØ- (Chip Select Ø) from pin 1. As shown in Figure 3-1, page 3, CSØ- enables RAM data buffer 11C at pin 18, which represents the least-significant, or even, data byte. In addition, 8B (Figure 3-1, page 6) generates LSEN- (Least Significant Byte Enable) from pin 3, enabling transceiver 11D at pin 19 (Figure 3-1, pge 3), which allows WDØ+ through WD7+ data transfers.

Before the next byte is generated, CNTRINCR- (Counter Increment) is issued from PAL 7E (pin 15), shown in Figure 3-1, page 5. (See the "Programmable Array Logic" subsection in Section 2, "Architecture," for programming information of PAL 7E.) CNTRINCR- clocks D flip-flop 7A (Figure 3-1, page 6), which acts as a state machine to generate two states for even and odd bytes. ODD+ (Odd Byte) is generated from 7A (pin 9) to 8B (pin 11), causing 8B to issue CS2- from pin 7. As shown in Figure 3-1, page 3, CS2- enables RAM data buffer 9C (pin 18), which represents the most-significant (odd) byte. In addition, 8B (Figure 3-1, page 6) generates MSEN- (Most Significant Byte Enable) from pin 6, enabling transceiver 1ØD at pin 19 (Figure 3-1, page 3), which also allows WDØ+ through WD7+ data transfers.

During a write to the RAM data buffer, this sequence occurs for each data word until RAM data buffer chips 11C and 9C become full (that is, contain 2K words). Four-bit binary counters 8D and 7D shown in Figure 3-1, page 6, are used to detect the 2K-word limit. Every word causes 8D to increment by one count via ADRINC+, which is generated by PAL 7E at pin 16 (Figure 3-1, page 5). (See the "Programmable Array Logic" subsection in Section 2, "Architecture," for programming information of PAL 7E.) When a 2K count is reached, represented by BAB+ at pin 6 of 7D, BAB+ is generated to pin 1Ø of 8B, causing 8B to issue CS1- from pin 2, representing the least-significant byte, and then CS3- from pin 9, representing the most-significant byte, in the same manner as described for CSØ- and CS2-, above. This allows for data words between 2K and 4K.

Note in Table 3-3 that the WD1Ø1Ø (12C) issues BDRQ+ (Buffer Data Request) from pin 36 (Figure 3-1, page 2) to pin 13 of 8B (Figure 3-1, page 6) to initiate the 8-bit data transfers to or from the RAM data buffer. In addition, ACK+ is issued as an acknowledge from the X-Bus master via connector J1, pin 57, shown in Figure 3-1, page 5, as XDACK3-.

As shown in Figure 3-1, page 6, BDRQ+ and ACK+ are used at 8B when the X-Bus master transfers data to or from the RAM data buffer, since the X-Bus master transfers 2-byte data words (that is, 16 bits). An X-Bus master data transfer causes 8B to issue either DMAØEN- (DMA Ø Enable) from pin 4 or DMA1EN- (DMA 1 Enable) from pin 5. DMAØEN- enables transceiver 11E (pin 19) to transfer the least-significant data byte (DØ+ through D7+). DMA1EN- enables transceiver 9D (pin 19) to transfer the most-significant data byte (D8+ through DF+).

RAM DATA DIRECTION

When reading data, WDIORD- (at pin 1 of each transceiver shown in Figure 3-1, page 3) causes the following, depending upon the enables at pin 19:

- 10D and 11D direct hard disk controller data lines WD0+ through WD7+ to the RAM data buffers (since WD1010 actually reading from the hard disk and writing to the RAM data buffers).
- 9D directs data from the RAM data buffer lines to local data lines D8+ through DF+.
- 11E directs data from the RAM data buffer lines to local data lines D0+ through D7+.

When writing data, WDIORD- becomes inactive at pin 1 of each transceiver to cause the following, depending upon the enables at pin 19:

- 10D and 11D data from the RAM data buffer lines to hard disk controller data lines WD0+ through WD7+ (since the WD1010 is actually reading from the RAM data buffers and writing to the hard disk).
- 9D directs local data lines D8+ through DF+ to RAM data lines.
- 11E directs local data lines D0+ through D7+ to RAM data lines.

DIRECT MEMORY ACCESS TRANSFERS

The 8253 programmable interval timer (5C) shown in Figure 3-1, page 5, is used to determine DMA transfer word counts.

Counter Ø is used to count the number of words being transferred to the X-Bus master. Counter Ø will interrupt on the last count by issuing END+ from pin 1Ø of 5C, signaling the DMA counter to start. Counters 1 and 2 are used as pulses for DMA. Counter 1 contains the number of words required for the DMA count (that is, burst size), and counter 2 is used as a time delay before the next DMA pulse to avoid bus contention. (See the "8253 Programmable Interval Timers" subsection, below, for 8253 operation, and the "State Sequencer" subsection, below, for states of the DMA transfers.)

For proper read/write sector and format timing, see the following:

- Figure 3-5, "Read/Write Sector Timing Diagram"
- Figure 3-6, "Single Sector Read Timing Diagram"
- Figure 3-7, "Single Sector Write Timing Diagram"

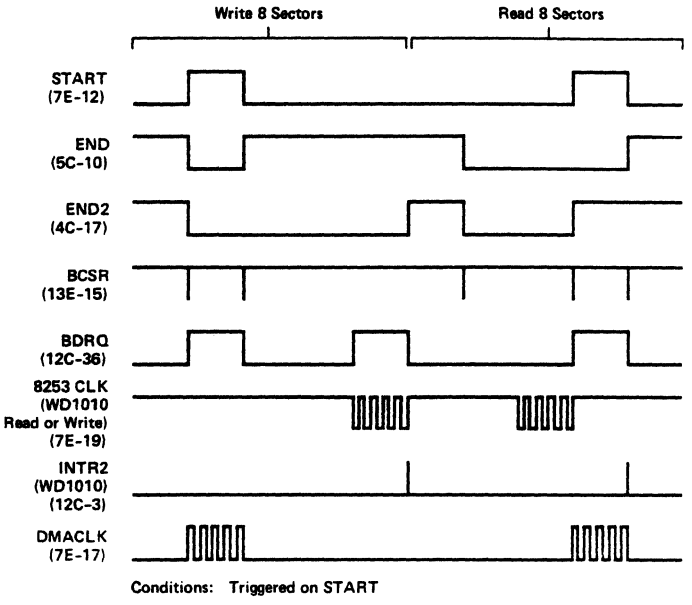
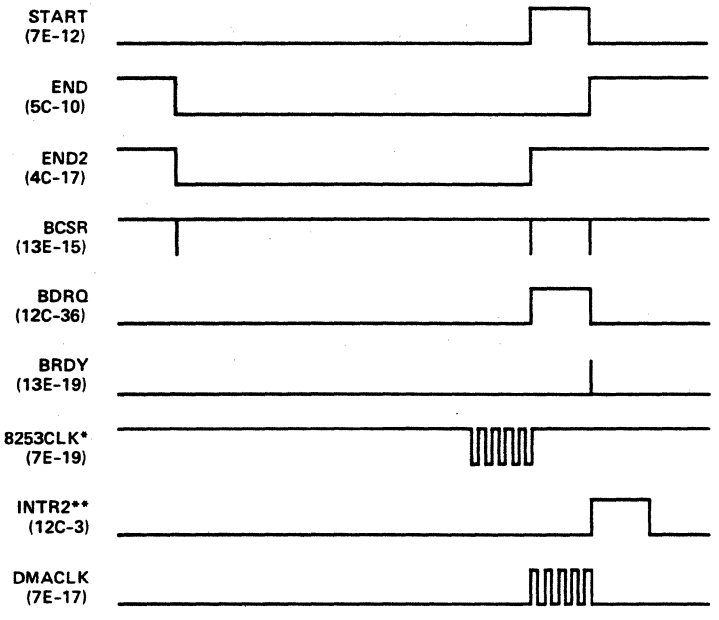


Figure 3-5. Read/Write Sector Timing Diagram.



Conditions: * Triggered on END = 0 and END2 = 1
** Triggered on START = 1

Figure 3-6. Single Sector Read Timing Diagram.

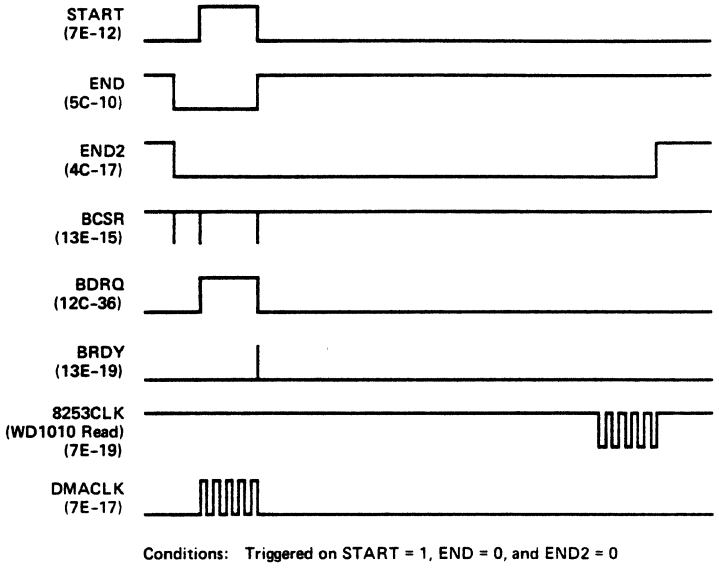


Figure 3-7. Single Sector Write Timing Diagram.

Clocks Ø and 1 are driven by DMACLK+ (DMA Clock) and its complement, which are generated from PAL 7E (pin 17). (See the "Programmable Array Logic" subsection in Section 2, "Architecture," for programming information on PAL 7E.) When START+ becomes high, signifying a DMA request to the X-Bus master, 5C issues a low signal (pin 13), which is inverted at 4E (pin 3) and again at 4E (pin 9), generating XDRQ3- (X-Bus DMA Request, Priority 3) via connector J1, pin 58. (See the "State Sequencer" subsection, below, for the operation of 5C.) Note that START+ from PAL 7E (pin 12) is generated to register 5B (pin 4), forcing a high output at pin 2 of 5B. This high signal loops back to pin 5 of 5B during the next 2MHZ+ transition at pin 9, generating a low signal at pin 6 that enables 4E (pin 19).

The X-Bus master responds with XDACK3- (X-Bus DMA Acknowledge, Priority 3) via connector J1, pin 57, as shown in Figure 3-1, page 5. XDACK3- is inverted at 7F (pin 9) as ACK+ (Acknowledge). (See the "State Sequencer" subsection, below, for state information.) ACK+ is inverted at pin 5 of 4E and driven as AEN- (Address Enable). As shown in Figure 3-1, page 4, AEN- enables buffer 6F at pins 1 and 19, which generates XADRØ- and XADR11- through XADR17- to connector J1, pins 111 and 67 through 73. Note that address lines XADR11- through XADR17- are controlled by data bits DØ+ through D6+ at X-Bus Extended Address register 6E. See the "X-Bus Extended Address Register (Port XXØEh)" in Section 2, "Architecture," for data bit functions.

Note that XBHE+ (X-Bus High Enable) is generated from buffer pin 11 of 1C to connector J1, pin 89 (Figure 3-1, page 5).

STATE SEQUENCER

The state sequencer circuitry shown in Figure 3-1, page 5, is used for DMA transfer operations between the RAM data buffer and the X-Bus master. A 2-MHz signal clocks counter 2 in the 8253 (5C) at pin 18, shift register 5B at pin 9, and state machine 6B at pin 2. See the "Hard Disk Drive Clock Logic" subsection, above, for the 2-MHz clock generation. Timing of the state sequencer is provided in Figure 3-8.

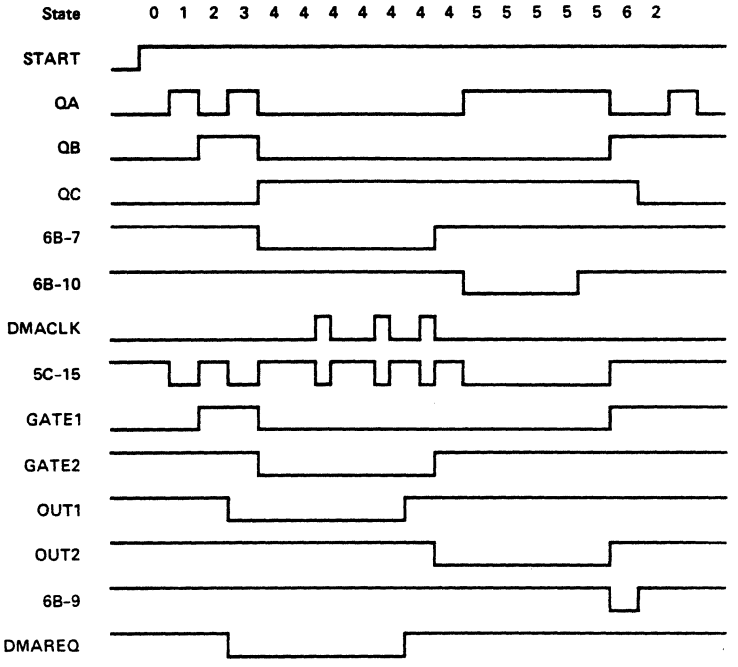


Figure 3-8. State Sequencer Timing.

The start of a DMA cycle, which is represented by START+ from pin 12 of PAL 7E, occurs during any of the following conditions:

- during a read of the boot ROM

- after the WD1010 finishes a read operation from the hard disk

- before the WD1010 performs a write operation to the hard disk

The X-Bus master loads counter 0 of programmable interval timer 5C with the total number of words that have to be transferred. Counter 1 specifies the number of transfers in one DMA burst, and counter 2 is used as a delay before another DMA transfer.

START+ initiates the DMA transfer at pin 4 of shift register 5B. Note that the outputs of state machine 6B are all low at this time (that is, state 0). Therefore, a low signal is generated from pin 14 of 6B, enabling buffer 1C at pin 10. An inactive DMACLK+, therefore, is inverted at 6D (pin 16), forcing a high signal at the counter 1 input of 5C (pin 15).

On the next 2-MHz clock, a high signal is generated from pin 14 of 6B, disabling buffer 1C at pin 10. A 1-kilohm resistor (RP4) causes 6D to generate a low signal from pin 16.

During state 2, a high signal is again generated from 6D (pin 16), forcing pin 15 of 5C high. In addition, a high signal is generated from pin 13 of 6B, which loads into gate 1 of 5C at pin 14.

The purpose of states 1 and 2 described above is to set up the output for counter 1. At the start of state 3, 5C generates a low pulse from pin 13 to pin 12 of 5B, and to pin 17 of 4E. Inverter 4E, therefore, generates a high signal (pin 3), which inverts again at pin 9 of 4E. As a result, XDRQ3- is generated to the X-Bus master via connector J1, pin 58.

In response, the X-Bus master generates XDACK3- back via connector J1, pin 57. Then, DMACLK+ is generated during state 4 from 7E (pin 17), clocking 5C at pin 15. After three words are read by the X-Bus master (signified by three DMACLK+ pulses as shown in Figure 3-8), the counter 1 output at pin 13 of 5C becomes high.

Note from Figure 3-8 that QC of 6B becomes high at the start of state 4. This signal is NANDed at gate 8A with a high signal caused by the low

signal output of counter 1 (pin 13 of 5C). Therefore, a low signal is generated from 8A at pin 6, which inhibits 6B (pin 7) from counting.

After three DMACLK+ pulses, the counter 1 output of 5C (pin 13) becomes high, forcing the output of 8A (pin 6) high and enabling 6B at pin 7, which initiates state 5.

At the start of state 5, the counter 2 output of 5C at pin 17, which determines the timeout before another DMA transfer, becomes low and inhibits 6B from counting. (Note that the gate of counter 2 is controlled by the counter 1 output as shown in Figure 3-8.) After the specified timeout, a high signal is generated from 5C at pin 17, enabling 6B at pin 1Ø.

During state 6, a high signal is generated from pin 13 of 6B, which is NANDed with a high signal generating from 6B (pin 12) at gate 8A, forcing a low signal from pin 8 that loads 6B (pin 9). The cycle then repeats itself beginning at state 2.

At the end of state 6, a low signal is generated from 6B (pin 12) that inverts at NAND gate 8A (pin 6) enabling 6B at pin 7. In addition, this low signal disables gate 8A at pin 8.

HARD DISK DRIVE READ/WRITE CIRCUITRY

READ

MFM Data

During a read, differential data from the selected hard disk drive (MFMØ+ and MFMØ-, or MFM1+ and MFM1-, connecting at connector J1, pins 21 and 22, or 44 and 41, respectively) is driven to RS-422 receiver 11B at pins 15 and 14, or 9 and 1Ø. (See Figure 3-1, page 4.)

Multiplexer 11A determines from which drive the data is connecting via select lines S1+ or S2+. When either S1+ or S2+ is high at Hard Disk Drive Control register 3E (Figure 3-1, page 3), a high signal at pin 1Ø or 1 of 11A (Figure 3-1, page 4) forces a low signal at pin 8, clocking pulse-width shaper flip-flop 12A at pin 11. Since pin 12 of 12A is connected to +5 V through 1-kilohm resistor RP2, a high signal is generated from pin 9 through delay line 12B. After 4Ø nsec, a high signal is inverted at gate 7F (pin 18), to clear 12A at pin 13. This allows a 5Ø-nsec pulse width signal at pin 9.

After 1ØØ nsec, a high signal generates to the WD1Ø1Ø (12C) at pin 37.

The 5Ø-nsec pulse width from pin 9 of 12A triggers one-shot 13B at pin 4. The RC network consisting of R6 and C15 creates a 23Ø-nsec pulse width. A string of low bits (Ø's) or high bits (1's) constantly retriggers 13B, causing a high signal at pin 6 that informs 12C at pin 34 that a string of unchanging bits is generating from the selected hard disk drive.

When the string terminates, 13B times out and issues a low signal at pin 6 to notify 12C at pin 34 that the string has ceased.

When 12C detects a data string, it issues a high signal from pin 38 as RG+ (Read Gate). RG+ is inverted at pins 7 and 5 of 12E as RDGT+ (Read Gate), which generates to multiplexer 11A (pin 5) and its complement, which generates to multiplexer 11A (pin 3). When RG+ is asserted from 12C, therefore, 11A is tied to MFM data generating from 12A (pin 9).

Note that when 12C is not reading data from the selected hard disk drive (that is, the valid data string is not detected), RG+ is not asserted, and the phase-detection circuitry described below is locked to a reference by the 10-MHz reference clock. The reference clock generates from J-K flip-flop 10B at pin 5, as a result of the 20-MHz oscillator at 10A.

Phase-Detection Circuitry

PLLREF+ (Phase-Locked Loop Reference) is generated from 11A (pin 6) to phase-detector enable flip-flop 4B (pin 1) and phase-comparison flip-flop 3B (pin 1), which detect either the MFM data reference or the 10-MHz clock reference.

Since pin 3 of phase-detector enable flip-flop 4B is strapped to +5 V, a high signal is generated from pin 5 to set (enable) phase-comparison flip-flops 3B and 4B at pins 3 and 11, respectively, and open a phase-comparison window. Flip-flops 3B and 4B should be clocked simultaneously. If an error exists between the frequency of the MFM data and voltage-controlled oscillator (VCO) output from 1B (pin 7), one of the phase-comparison flip-flops will be clocked before the other. For example, if the VCO is running too fast, a high signal from 1B (pin 7) clocks 4B (pin 13) before 3B (pin 1) is clocked by MFM data. In this case, 4B will generate a high signal from pin 9, and 3B will generate a low signal from pin 5.

The high signal from 4B (pin 9) forces exclusive OR gate 4A (pin 8) low, which causes NAND gate 3A to output a high signal at pin 3. Simultaneously, the low signal from 3B (pin 5) forces exclusive OR gate 4A (pin 11) high. This high signal is NANDed at gate 3A with the high signal that was propagated by 4B (pin 9) to output a low signal at pin 11.

Since pins 4 and 11 inputs of phase-frequency detector 2A are active-low, the low signal from 3A (pin 11) causes 2A to pump down (pin 11). Therefore, a low signal is generated from pin 8 to oscillator 1B (pin 2), causing the output frequency of 1B (pin 7) to run slow.

When the MFM data clocks 3B at pin 1, a high signal is generated from pin 5 to 2A at pin 1.

When both pins 3 and 1 of 2A become high, a low signal is generated from pin 6, which forces 3A (pin 8) low, resetting phase-detector enable flip-flop 4B, and phase-comparison flip-flops 3B and 4B and, therefore, closing the phase-comparison window.

When 1B is running slow, the MFM data will clock 3B at pin 1 before 4B (pin 13) is clocked by the output of 1B (pin 7). Therefore, a high signal is generated from 3B at pin 5, forcing the input of 2A at pin 11 high to inhibit 2A from pumping down. In addition, the low signal from 4B at pin 9 forces the input of 2A at pin 4 low, enabling 2A to pump up.

In summary, when the phase is different at pins 1 and 3 of phase-frequency detector 2A (that is, between the reference voltage from pin 5 of 3B and the variable oscillator output from pin 9 of 4B), 2A pumps up or down to control the frequency of 1B at pin 2. When pin 4 of 2A is low and pin 11 of 2A is high, the frequency increases at pin 8. When pin 11 of 2A is low and pin 4 of 2A is high, the frequency decreases at pin 8. When pin 2 of 1B becomes high, the output frequency increases; when pin 2 becomes low, the output frequency decreases.

The output of 1B at pin 7 clocks J-K flip-flop 3B at pin 13, to generate RDCLK+ (Read Clock) at pin 9. RDCLK+ connects to pin 39 of the WD1010 (12C). When a string of 0s or 1s is detected, the phase-locked loop is clocked to MFM data, the RDCLK+ becomes high, and 12C anticipates a string of 0s or 1s and searches the ID field. Then 12C starts loading the RAM data buffer.

Phase Synchronization

Shift-register 2B is used to start the phase-locked loop circuitry at the same phase as the incoming MFM data. MFM data, which is represented as PLLREF+, clocks 2B at pin 9. After four clock cycles, a low signal is generated from pin 14 and exclusive ORed at gate 4A with RDGT+ (pins 2 and 1, respectively). This causes a high signal to generate at pin 3, which is inverted at pin 4 of 9A, enabling 1B (pin 6).

Note that before RDGT+ is propagated through 2B, a high signal is generated from pin 14, causing gate 4A to produce a low signal that is inverted at pin 4 of 9A, disabling 1B at pin 6.

WRITE

When the WD1010 (12C) writes data, it issues WD+ (Write Data) at pin 21 (Figure 3-1, page 4). The data is clocked by the 10-MHz clock generated from J-K flip-flop 10B at pin 6 as a result of 20-MHz oscillator 10A. The MFM clock and data pulses are driven at 2F as WFM0+ and WFM0-, or WFM1+ and WFM1- to the selected hard disk drive (via connector J1, pins 19 and 20, or 39 and 40).

FLOPPY DISK OPERATION

If WD2797-Ø2 formatter/controller 2C (shown in Figure 3-1, page 7) is prompted to perform a read operation on a nonexistent floppy disk sector, such as sector 17 on a 16-sector floppy disk, or if it is asked to read an entire track of data, 2C makes a futile search for the missing sector before issuing an interrupt request to the X-Bus master. Since this operation takes five revolutions of the floppy disk media (or about 1ØØØ milliseconds), the 8253 programmable interval timer (4C) is used to terminate the read or write command after the last byte is read. This also gives 2C enough time to compute the two CRC bytes if a read error has occurred.

The total number of bytes to be transferred is loaded into 4C. When the read or write operation is complete, 4C interrupts the X-Bus master. The X-Bus master, in turn, issues a Force Interrupt command to 2C to terminate the search.

A functional block diagram of the programmable interval timer logic is shown in Figure 3-9. Programming requirements for 4C are described in Section 2, "Architecture."

The pin assignments and functions of 4C are provided in Table 3-4.

As shown in Figure 3-1, page 7, the 8253 programmable interval timer 4C is selected when 1-of-8 decoder 11F issues 8253CS- at pin 1Ø, as described in the "Floppy/Hard Disk Module Device Decoding" subsection, above. When selected, the X-Bus master writes to several registers in 4C (using the XIOWR- strobe) to set the timing mode (always equal to Ø, Interrupt on Terminal Count) and to specify the number of bytes in counter Ø to be transferred.

The X-Bus master can select one of several registers by using XADR1- and XADR2- X-Bus address lines, and can read from or write to the selected register by using the XDATØ- through XDAT7- lines. (See the "X-Bus Data Interface" subsection, above.) XADR1- is inverted at 7F (pin 14) before generating to the AØ+ input of 4C (pin 19). XADR2- is inverted at 7F (pin 12) before generating to the A1+ input of 4C (pin 2Ø).

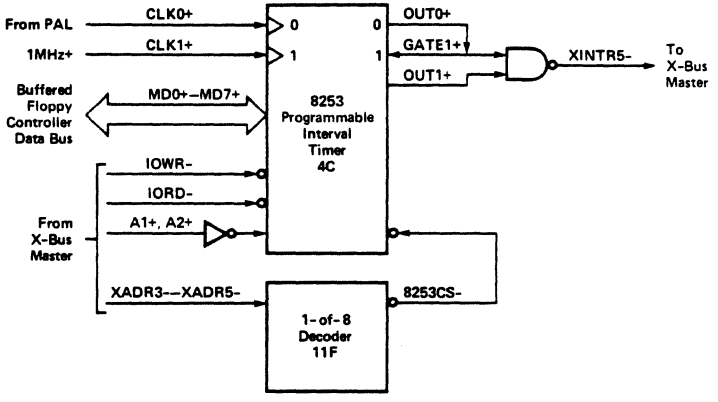


Figure 3-9. Floppy Disk Controller Programmable Interval Timer Logic Functional Block Diagram.

Table 3-4. 8253 Programmable Interval Timer 4C Pin Assignments and Functions. (Page 1 of 2)

Pin	Function
1 - 8	**Data Bus Lines (DØ+ through D7+).** Bidirectional interface to system data bus.
9	**Clock Ø (CØ+).** Clock input (from PAL 13E) of counter Ø.
1Ø	**Output Ø (OØ+).** Used for interrupt timeout; tied to G1+ input (pin 14).
11	**Gate Ø (GØ+).** Gate input of counter Ø; strapped to +5 V.
12	Ground.
13	**Output 1 (O1+).** Used for interrupt timeout.
14	**Gate 1 (G1+).** Gate input of counter 1; tied to OØ+ (pin 1Ø).
15	**Clock 1 (C1+).** 1-MHz clock input of counter 1.
16	**Gate 2 (G2+).** Gate input of counter 2; strapped to +5 V.

Table 3-4. 8253 Programmable Interval Timer 4C Pin Assignments and Functions. (Page 2 of 2)

Pin	Function
17	**Output 2 (O2+).** Signal to PALs; used to tabulate the total number of words for internal use by 12C.
18	**Clock 2 (C2+).** Clock input from PAL used to reset counter 2.
19, 2Ø	**Address Lines (AØ+ and Al+).** Used to select one of the three counters or the Control Word register for read or write operations; connected to X-Bus address lines XADR1- and XADR2-.
21	**Chip Select (CS-).** Enables 4C when 11F issues 8253CS- from pin 1Ø as described in the "Floppy/Hard Disk Module Device Decoding" subsection.
22	**Read (RD-).** Signifies I/O read operation.
23	**Write (WR-).** Signifies I/O write operation.
24	Power (+5 V).

Read operations are indicated when XIORD- generates through pin 3 of buffer 10F (Figure 3-1, page 2) to the RD- (Read) input of 4C (pin 22) shown in Figure 3-1, page 7. Similarly, write operations are indicated when XIOWR- generates through pin 5 of 10F to the WR- (Write) input of 4C at pin 23. Internal registers of 4C are listed below with their addresses in the module relative to the module base I/O address (XXh):

A2+	A1+	Read Register (RD-)	Write Register (WR-)
0	0	Read counter 0 (XX10h)	Load counter 0 (XX10h)
0	1	Read counter 1 (XX12h)	Load counter 1 (XX12h)
1	0	Read counter 2 (XX14h)	Load counter 2 (XX14h)
1	1	-	Mode word (XX16h)

Counters 0 and 1 are used for the interrupt function. Counter 0 is loaded with the total byte count of the read operation. Counter 1 is loaded with a fixed time interval to time out (about 40 microseconds), which allows 2C to compute the two CRC bytes at the last sector of the transfer if a read error has occurred. If counter 1 is not used, a race condition can occur if the X-Bus master issues a Force Interrupt command to 2C before it actually finishes with the CRC bytes. Therefore, both counters time out before an interrupt is sent to the X-Bus master.

When counter 0 times out, its output becomes high at pin 10 and generates to enable gate 1 at pin 14. Then, counter 1 outputs a high signal at pin 13. The high signals from both counters are generated to NAND gate 1E (pins 5 and 4, respectively) to assert XINTR5- to the X-Bus master via connector J1, pin 114.

Counter 0 is clocked by DM+ (DMA), once for every byte transferred by 2C, at pin 9 of 4C, indicating that the Data register in 2C is being accessed. Counter 1 is clocked at pin 15 by the 1-MHz output at pin 5 of divide-by-two flip-flop 9B shown in Figure 3-1, page 4.

Note that counter 2 is not used by the floppy controller; counter 2C is used by the hard disk controller, as described below in the "Hard Disk Operation" subsection.

HARD DISK OPERATION

The hard disk controller 12C uses both 8253 programmable interval timers resident to the Floppy/Hard Disk Module (that is, 4C and 5C). Counter 2 of 4C is used to tabulate the total number of words for internal use by 12C (since 12C does not support multiple-sector transfers). All counters of 5C are used for DMA transfers.

A functional block diagram of the programmable interval timer logic used by the hard disk controller is shown in Figure 3-1Ø. Programming requirements for 4C and 5C are described in Section 2, "Architecture." In addition, timing diagrams are provided in Figures 3-5 through 3-7.

The pin assignments and functions of 4C are provided in Table 3-4. The pin assignments and functions of 5C are provided in Table 3-5.

As shown in Figure 3-1, page 7, 5C is selected when 1-of-8 decoder 11F (Figure 3-1, page 7) issues W8253EN- (pin 1Ø) as described in the "Floppy/Hard Disk Module Device Decoding" subsection, above. When selected, the X-Bus master writes to several registers in 5C (using the XIOWR- strobe shown in Figure 3-1, page 2) to set the timing mode.

As shown in Figure 3-1, page 2, the X-Bus master can select one of several registers by using XADR1- and XADR2- X-Bus address lines, and can read from or write to the selected register. (See "X-Bus Data Interface," above.) XADR1- is inverted at 7F (pin 14) before generating to 5C as A1+. XADR2- is inverted at 7F (pin 12) before generating to 4C as A2+. As shown in Figure 3-1, page 5, A1+ connects to the AØ+ input of 5C (pin 19), and A2+ connects to the A1+ input of 5C (pin 2Ø).

Table 3-5. 8253 Programmable Interval Timer 5C Pin Assignments and Functions. (Page 1 of 2)

Pin	Function
1 - 8	**Data Bus Lines (DØ+ through D7+).** Bidirectional interface to hard disk controller data bus (MDØ+ through MD7+).
9	**Clock Ø (CLØ+).** DMA clock input (from PAL 7E) of counter Ø.
1Ø	**Output Ø (OUTØ+).** Used to terminate cycle; connected to PALs 7E and 13E.
11	**Gate Ø (GATEØ+).** Gate input of counter Ø; strapped to +5 V.
12	Ground.
13	**Output 1 (OUT1+).** Used to indicate the number of words for the DMA count.
14	**Gate 1 (GATE1+).** Gate input of counter 1; controlled by state machine 6B.
15	**Clock 1 (CL1+).** DMA clock input (from PAL 7E); controlled by state machine 6B.
16	**Gate 2 (GATE2+).** Gate input of counter 2; controlled by the output of counter 1 via register 5B.

Table 3-5. 8253 Programmable Interval Timer 5C Pin Assignments and Functions. (Page 2 of 2)

Pin	Function
17	**Output 2 (OUT2+).** Used to determine the timeout between DMA transfers.
18	**Clock 2 (CL2+).** 2-MHz clock input.
19, 20	**Address Lines (A0+ and A1+).** Used to select one of the three counters or the Control Word register for read or write operations; connected to X-Bus address lines XADR1- and XADR2-.
21	**Chip Select (CS-).** Enables 5C when 11F (Figure 3-1, page 7) issues W8253EN- from pin 14 as described in the "Floppy/Hard Disk Module Device Decoding" subsection.
22	**Read (RD-).** Signifies that the 80186 CPU is inputting values for the counters.
23	**Write (WR-).** Signifies that the 80186 CPU is outputting mode information or loading counters.
24	Power (+5 V).

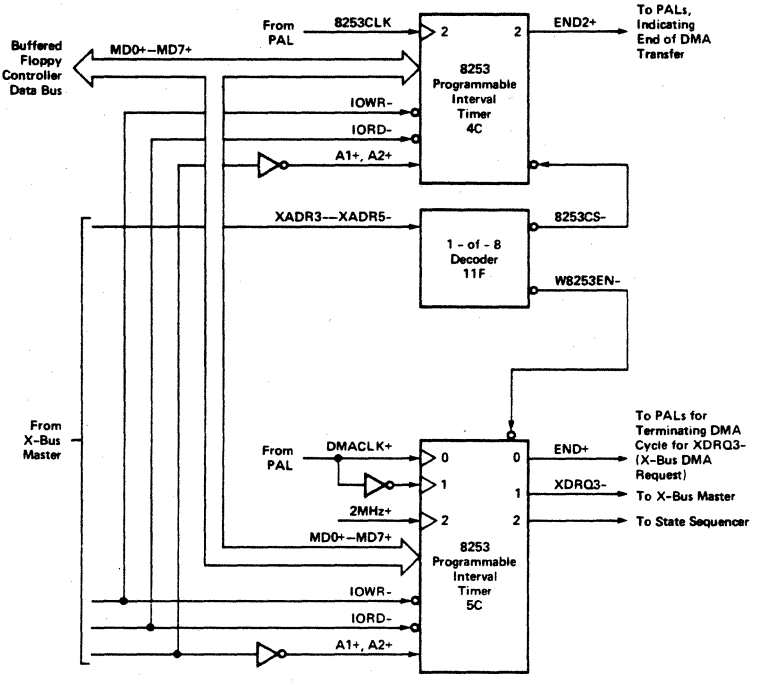


Figure 3-1Ø. Hard Disk Controller Programmable Interval Timer Logic Functional Block Diagram.

Read operations are indicated when XIORD- generates through pin 3 of buffer 1ØF (Figure 3-1, page 2) to the RD- (Read) input of 5C (pin 22) shown in Figure 3-1, page 5. Similarly, write operations are indicated when XIOWR- generates through pin 5 of 1ØF to the WR- (Write) input of 5C at pin 23.

Internal registers of 5C are listed below with their addresses in the module relative to the module base I/O address (XXh):

A2+	A1+	Read Register (RD-)	Write Register (WR-)
Ø	Ø	Read counter Ø (XX3Øh)	Load counter Ø (XX3Øh)
Ø	1	Read counter 1 (XX32h)	Load counter 1 (XX32h)
1	Ø	Read counter 2 (XX34h)	Load counter 2 (XX34h)
1	1	--	Mode word (XX36h)

When the X-Bus master loads a command in controller 12C, the following times are set in counters Ø, 1, and 2 of 8253 5C:

- word count (counter Ø)
- DMA burst count (counter 1)
- DMA delay count (counter 2)

In addition, counter 2 of 8253 4C shown in Figure 3-1, page 7, is set to provide internal timing for 12C.

After the mode control is loaded, END+ and END2+ become low. Then, 12C accesses the ID field, reads the content from the hard disk, and loads the content into the RAM data buffer. During this time, the inactive END2+ counts. At the end of the count, END2+ becomes high, signifying that 12C has written data into the RAM data buffer. PAL 7E then resets counter 2 of 4C (pin 18) by issuing 8253CLK- from pin 19. 7E then generates a START+ signal from pin 12 to allow the DMA transfer.

Refer to the "State Sequencer" subsection, above, for state information.

POWER SUPPLIES

Two standard dc/dc power converters are used in the Floppy/Hard Disk Module. One supplies +12 Vdc for the drives while the other supplies +5 Vdc for the drives and controller circuitry. For more information, refer to the Power System Manual.

FLOPPY/HARD DISK INTERCONNECT WIRE LIST

Signal	XBUS IN (P1)	XBUS OUT (J1)	CNT-RLR (P9)	FLOPPY (P5)	HARD (P3)	HARD FAN (P10)	(P6)	J2	J3
XPWREN-*	5	5							
XDACK3-	6	6	57						
XDRQ3-	7	7	58						
XDACK2-	8	8							
XDRQ2-	9	9							
XDACK1-	10	10							
XDRQ1-	12	12							
XDRQ4-	13	13	59						
XADRF-	14	14	60						
XADRE-	15	15	61						
XADRD-	16	16	62						
XADRC-	18	18	63						
XADRB-	19	19	64						
XADRA-	20	20	66						
XADR17-	21	21	67						
XADR16-	22	22	68						
XADR15-	24	24	69						
XADR14-	25	25	70						
XADR13-	26	26	71						
XADR12-	27	27	72						
XADR11-	28	28	73						
XADR10-	30	30	74						

*Also connects to pin 15 of P7 and P8

Signal	XBUS IN (P1)	XBUS OUT (J1)	CNT-RLR (P9)	FLOPPY (P5)	HARD (P3)	HARD (P10)	FAN (P6)	J2	J3
XADR9-	31	31	76						
XADR8-	32	32	77						
XADR7-	33	33							
XADR6-	34	34	79						
XADR5-	36	36	80						
XADR4-	37	37	81						
XADR3-	38	38	82						
XADR2-	39	39	83						
XADR1-	40	40	84						
XADR0-	42	42	111						
XPIN+	44		116						
XPOUT+		44	117						
X33KHZSYNC+*	46	46							
XINTR5-	48	48	114						
XINTR3-	49	49	113						
XINTR4-	50	50							
XINTR2-	51	51	118						
XINTR1-	52	52							
XINTR0-	54	54							
XMODE3-	55	55							
XMEMRD-	57	57	112						
XMEMWR-	58	58							
XDMAEN-	60	60	110						

*Also connects to pin 14 of P7 and P8

Signal	XBUS IN (P1)	XBUS OUT (J1)	CNT-RLR (P9)	FLOPPY (P5)	HARD (P3)	HARD (P10)	FAN (P6)	J2	J3
XMODE2-	61	61							
XDATF-	62	62	108						
XDATE-	63	63	107						
XDATD-	64	64	106						
XDATC-	66	66	104						
XDATB-	67	67	103						
XDATA-	68	68	102						
XDAT9-	69	69	101						
XDAT8-	70	70	100						
XDAT7-	72	72	99						
XDAT6-	73	73	98						
XDAT5-	74	74	97						
XDAT4-	75	75	96						
XDAT3-	76	76	94						
XDAT2-	78	78	93						
XDAT1-	79	79	92						
XDAT0-	80	80	91						
XSPKR-	81	81							
XACK-	82	82	90						
XLOCK-	84	84							
XBHE-	85	85	89						
XRESET-	86	86	88						
XIOWR-	91	91	87						
XIORD-	92	92	86						

Signal	XBUS IN (P1)	XBUS OUT (J1)	CNTRLR (P9)	FLOPPY (P5)	HARD (P3)	HARD (P10)	FAN (P6)	J2	J3
XPCLK+	93	93							
XDCLK-	95	95							
STEP1-			6		24				
DIR1-			4		34				
RWC1-			18		2				
WRGT1-			13		6				
STEP2-			51						5
DIR2-			52						6
RWC2-			49						7
WRGT2-			50						8
DSEL0-			3		26				
DSEL1-			47						10
HSEL0-			9		14				
HSEL1-			10		18				
HSEL2-			16		4				
EHSEL0-			48						11
EHSEL1-			46						12
EHSEL2-			43						13
MFM0+			21			17			
MFM0-			22			18			
MFM1+			44						14
MFM1-			41						16
SEL0-			17			1			
SEL1-			42						17

Signal	XBUS IN (P1)	XBUS OUT (J1)	CNTRLR (P9)	FLOPPY (P5)	HARD (P3)	HARD (P10)	FAN (P6)	J2	J3
WFMØ+			19			13			
WFMØ-			20			14			
WFM1+			39						18
WFM1-			40						19
DT1-			37						20
DT2-			38						22
TRACKØ-			32	26					
WRPROT-			31	28					
INDEX-			26	8					
READY-			36	34					
WRDATA-			30	22					
WRGATE-			29	24					
STEP-			27	20					
DIRECTION-			28	18					
RDDATA-			34	30					
DSØ-			23	10					
SIDESEL-			33	32					
MOTORØ-			24	16					
WTRACKØ-			11		10				25
WFAULT-			12		12				26
SKCOMPL-			14		8				28
WINDEX-			7		20				23
WREADY-			8		22				24
DT3-			78						27
EXPLITE-			109						30

HARD DISK EXPANSION

A Hard Disk Expansion Module can be connected to the right side of the Floppy/Hard Disk Module (looking from the front). See the Installation Guide for details.

A hard disk expansion interconnect wire list is provided below.

HARD DISK EXPANSION INTERCONNECT WIRE LIST

Signal	XBUS IN (P1)	XBUS OUT (J2)	WINCH EXP BUS (P5)	WINCH (P3)	WINCH (P10)	POWER BRICK (P8)
XPWREN-	5	5				15
XDACK3-	6	6				
XDRQ3-	7	7				
XDACK2-	8	8				
XDRQ2-	9	9				
XDACK1-	10	10				
XDRQ1-	12	12				
XDRQ4-	13	13				
XADRF-	14	14				
XADRE-	15	15				
XADRD-	16	16				
XADRC-	18	18				
XADRB-	19	19				
XADRA-	20	20				
XADR17-	21	21				
XADR16-	22	22				
XADR15-	24	24				
XADR14-	25	25				
XADR13-	26	26				
XADR12-	27	27				
XADR11-	28	28				
XADR10-	30	30				
XADR9-	31	31				

Signal	XBUS IN (P1)	XBUS OUT (J2)	WINCH EXP BUS (P5)	WINCH (P3)	WINCH (P1Ø)	POWER BRICK (P8)
XADR8-	32	32				
XADR7-	33	33				
XADR6-	34	34				
XADR5-	36	36				
XADR4-	37	37				
XADR3-	38	38				
XADR2-	39	39				
XADR1-	4Ø	4Ø				
XADRØ-	42	42				
XPIN+	44					
XPOUT+		44				
X33KHZSYNC+*	46	46				14
XINTR5-	48	48				
XINTR3-	49	49				
XINTR4-	5Ø	5Ø				
XINTR2-	51	51				
XINTR1-	52	52				
XINTRØ-	54	54				
XMODE3-	55	55				
XMEMRD-	57	57				
XMEMWR-	58	58				
XDMAEN-	6Ø	6Ø				
XMODE2-	61	61				
XDATF-	62	62				

Signal	XBUS IN (P1)	XBUS OUT (J2)	WINCH EXP BUS (P5)	WINCH (P3)	WINCH (P10)	POWER BRICK (P8)
XDATE-	63	63				
XDATD-	64	64				
XDATC-	66	66				
XDATB-	67	67				
XDATA-	68	68				
XDAT9-	69	69				
XDAT8-	70	70				
XDAT7-	72	72				
XDAT6-	73	73				
XDAT5-	74	74				
XDAT4-	75	75				
XDAT3-	76	76				
XDAT2-	78	78				
XDAT1-	79	79				
XDAT0-	80	80				
XSPKR-	81	81				
XACK-	82	82				
XLOCK-	84	84				
XBHE-	85	85				
XRESET-	86	86				
XIOWR-	91	91				
XIORD-	92	92				
XPCLK+	93	93				
XDCLK-	95	95				

Signal	XBUS IN (P1)	XBUS OUT (J2)	WINCH EXP BUS (P5)	WINCH (P3)	WINCH (P10)	POWER BRICK (P8)
STEP2-			5	24		
DIR2-			6	34		
RWC2-			7	2		
WRGT2-			8	6		
DSEL1-			10	26		
EHSEL0-			11	14		
EHSEL1-			12	18		
EHSEL2-			13	4		
MFM1+			14		17	
MFM1-			16		18	
SEL1-			17		1	
WFM1+			18		13	
WFM1-			19		14	
DT1-			20			
DT2-			22			
WTRACK0-			25	10		
WFAULT-			26	12		
SKCOMPL-			28	8		
WINDEX-			23	20		
WREADY-			24	22		
DT3-			27			
ELITE-			30			

APPENDIX A: FLOPPY/HARD DISK MODULE SPECIFICATION

ELECTRONIC

MASS STORAGE

Capacity

5.25-in. floppy disk drive

Unformatted: 1M byte
Formatted: 630K bytes

Hard disk drive

Unformatted: 12M bytes
Formatted: 10M bytes

Controller

Western Digital WD2797-02 Formatter/Controller

Western Digital WD1010 Winchester Disk Controller

POWER REQUIREMENTS

Consumption

36 Vdc 6 power units (80 W)

ENVIRONMENTAL

TEMPERATURE

Operating: 0 degrees C to 40 degrees C
(32 degrees F to 104 degrees F)

Storage: -40 degrees C to 75 degrees C
(-40 degrees F to 167 degrees F)

HUMIDITY

Operating: 20% to 80% noncondensing

Storage: 8% to 90% noncondensing

APPENDIX B: MITSUBISHI MINI FLEXIBLE-DISK DRIVE —M4852/M4853-SPECIFICATIONS

MITSUBISHI MINI FLEXIBLE-DISK DRIVE M4852/M4853 (1.0MB HALF HEIGHT)

Specifications

MITSUBISHI ELECTRIC CORPORATION

3.1.3 USER CHANGEABLE OPTIONS

Non-standard modes of operation are available to the customer by using option plugs, and some PCB cut and/or jumpers. When using a plug, installing the option plug on a pair of square pins is a "short" condition, and removing it is an "open". A trace or a soldered wire jumper between two pads is a "short", and none is a "open".

The specific options are explained below.

3.1.3.1 DS0 TO DS3

When two or more FDDs are connected to the system, jumper one of the four choices to allow the drive to be enabled when the particular select line is taken to a logical "0" condition.

Only one drive per system may be designated for each drive number. In other words, there can only be one drive "0", etc., in a system.

3.1.3.2 MX

If only one FDD is in a system, this option may be used to constantly select the drive. It causes to drive to ignore the status of the "DS" lines.

This jumper must be removed in multi-drive systems.

3.1.3.2 HS

This plug is installed to cause the heads to load when the drive is selected by DS0 through DS3. This occurs after the drive is "ready". Do not install HM or HC with this option.

3.1.3.3 HM

This plug is installed to cause the heads to load when the motor on line (P1-16) is brought to a logical "0" level. This occurs after the drive is "ready". Do not install HS or HC with this option.

3.1.3.4 HC

This plug is installed to cause a constant head load condition which occurs after the drive is ready to allow for proper seating of the floppy disk. Do not install HS or HM with this option.

3.1.3.5 MM

This plug is installed to cause the spindle motor to turn on and rotate the disk with the input of a logical "0" on the motor on line, P1-16.

3.1.3.6 MS

This plug is installed to cause the spindle motor to turn on and rotate the disk when the drive is selected by applying a logical "0" on one of the drive select lines, DS0 through DS3.

3.1.3.7 H-1

Installing the "H" jumper in position 1 routes whatever type of "ready" signal is selected to be outputed from the drive to the head load circuit ready qualification input.

3.1.3.8 H-2

Installing the "H" jumper in position 2 routes the "current status" ready signal to the head load circuit ready qualification input.

3.1.3.9 H-3

Installing the "H" jumper in position 3 routes the "held status" ready signal to the head load circuit ready qualification input.

3.1.3.10 R-2

Installing the "R" jumper in position 2 enables a "current status" ready output from the drive. The output goes to a logical "0" when the floppy disk is rotating at proper speed.

3.1.3.11 R-3

Installing the "R" jumper in position 3 enables a "held status" ready output from the drive. The output will be a logical "0' when a disk is inserted and correctly clamped in the drive. (Index pulses were detected correctly).

3.1.3.12 R-4

This option must not be used at this time.

3.1.3.13 MC

Cutting this PCB trace causes the spindle motor to run whenever a floppy disk is inserted in the drive.

3.1.3.14 RD-RS

This option is associated with "R-4", and therefore has no significance at this time.

3.1.3.15 DI

Cutting this PCB trace disables the in-use input to the drive (P1-4). This means that the only time the front panel LED will be lit will be when the drive is selected. The MX option cannot be used in conjunction with this modification; the in use LED will never be illuminated if it is.

3.1.3.16 WRITE PROTECT INVERSION

The option pads between IC's M1 and L1 are used to invert the logic of the write protect slot on the floppy disk. The trace from the center pad to the in-board pad must be cut, and the center pad must be jumped to the out-board pad to enable this option.

3.1.3.17 INPUT TERMINATIONS

All seven input lines to the drive are terminated (See section 3.1.1). The jumper plug located between IC's C5 and D5 should be removed on drives in multi-drive systems, with the exception of the drive the furthest electrical distance from the controller.

NAME	LOCATION	DESCRIPTION	TYPE CONNECTION	FACTORY SHIPMENT	
				Open	Short
DS0	6B	Drive Address 0	Plug		X
DS1	6B	" " 1	"	X	
DS2	6B	" " 2	"	X	
DS3	6B	" " 3	"	X	
MX	6B	Continues Drive Select	"	X	
HS	6B	Head Load W/Drive Select	"		X
HM	6B	" " W/Motor On	"	X	
HC	6B	" " Constantly	"	X	
MM	5E	Motor On-Motor On Input	"		X
MS	5E	Motor On-Drive Select	"	X	
H1	2L	Head Load-Drive Ready	"		X
H2	2L	Head Load-Current Status	"	X	
H3	2L	Head Load-Held Status	"	X	
R2	2L	Ready Output-Current Status	"		X
R3	2L	Ready Output-Held Status	"	X	
R4	2L	Not Used-Leave Open	"	X	
MC	2E	Motor Constantly On	Trace		X
RD	2K	Not Used-Leave Open	"	X	
RS	2K	Not Used-Leave Shorted	"		X
DI	6B	Disable In Use Input	"		X
-	2M	Write Protect Inversion	"	Note 1	Note 1
	6B	Input Terminations	Plug		7

Note 1: See Section 3.1.3.16 for description of this unmarked option.

4.7 DISK INSERTION

The sequence of events that occur with disk insertion are:

1) The user inserts the disk into the drive until an audible "click" is heard. This indicates that the drive ejection mechanism has received the disk.

2) When the disk is fully inserted into the drive a mechanical switch is accuated, and the spindle motor starts to rotate.

3) The user clamps the disk on to the rotating spindle using the bridge handle. The handle is moved until an audible click is heard.

4) The disk starts to rotate, and the index sensor begins to detect pulses of light from the index LED.

5) Two index pulses are detected in a minimum period of time, which switches the "current ready" and "held ready" logic to a true state. If the disk is not properly seated, this will not occur because the index hole in the disk will never allow light to strike the presise location required to activate the photo-transistor that is the index pulse sensor. The spindle motor is turned off.

6) Option jumper H-3 (or in some cases H-1) may be used to load the head on to the disk at this time. This is desirable if the user wishes to eliminate the head load and settling times associated with motor start/stop operation.

4.8 DISK REMOVAL

To remove the disk from the drive the user depresses the front panel door flop, which releases the bridge handle. The ejector mechanism then transports the disk out of the drive into the users fingers.

This action also resets the "held ready" status to a false condition, which can be detected by having the system controller poll the drive for its status (if the R-3 option is used).

CONTENTS

CHAPTER 1 INTRODUCTION

The Mitsubishi M4852/M4853 Flexible Disk Drives are high-performance, double-side, double bit and double track density flexible disk drive using a standard 5.25-inch diskette, that provides maximum customer satisfaction even to those who demand high reliability and long service life.

- Main Features -

- o **Model M4852 is the standard size, and Model M4853 is half as high (41 mm) as the standard size.**
- o **Model M4853 includes a diskette ejector for easy diskette removal.**
- o **A new circular gimbal spring in the read/write head suspension mechanism greatly improves medium tracking performance.**
- o **The steel band drive system for positioning achieves the best inter-track access time in its class: just 3 ms.**
- o **The maintenance-free, DC, brushless, direct-drive motor obviates the belt replacement necessary for conventional counterparts.**
- o **Stable media interchangeability, wide off-track window time margin, and excellent performance are maintained over wide ambient temperature and relative humidity ranges.**
- o **The high-torque spindle motor permits control by switching on and off either the motor (starting time 250 ms) or the head load magnet (loading time less than 50 ms).**

1.1 General Description

- o The M4853 Flexible Disk Drive is a twin-head, double-sided magnetic disk drive with a formatted memory capacity of more than 635 kilobytes for double-density recordings.
- o The M4853 reads and writes 5.25-inch, double-sided diskettes in double-density format.
- o The M4853 employs the unique Mitsubishi circular gimbal spring for holding and loading the magnetic heads to assure soft, steady contact with the medium. This means excellent read/write operation and a long service life for the medium. One of the outstanding features of this mechanism is reduction of the effects of jacket deformation and thickness variations, thereby stabilizing read/write performance and dispensing with the need for selecting products of a specific manufacturer.

1.2 Specifications

1.2.1 Performance specifications (Table 1-1)

Table 1-1 Performance Specifications

	Double Density
Memory capacity	
Unformatted	
Disk	1000 kilobytes
Per surface	500 kilobytes
Per track	6.25 kilobytes
Formatted	256 bytes/sector
Disk	655.4 kilobytes (including spare tracks)
Per surface	327.7 kilobytes (including spare tracks)
Per track	4096 bytes = 256 bytes x 16 sectors
Transfer rate	250 kilobits/second
Average latency time	100 ms
Access time	
Track to track	3 ms
Average	94 ms (including 3 ms step time and settling time)
Settling time	15 ms
Head loading time	50 ms
Motor starting time	250 ms

1.2.2 Functional specifications (Table 1-2)

Table 1-2 Functional Specifications

	Double Density
Recording density	5922, bits per inch
Magnetic flux inversion density	5922 FCI
Encoding method	MFM
Track density	96 tracks per inch
Number of cylinders	80
Number of tracks	160
Number of heads	2
Rotation speed	300 rpm
Rotation period	200 ms
Index	1
Media	Double-sided 96 TPI, standard 5.25-inches diskette

1.2.3 Physical Specifications (Table 1-3)

Table 1-3 Physical Specifications

DC power requirements	
+5 V	+5 V ± 5%, 0.5 A typical
+12 V	+12 V ± 5%, 0.7 A typical (Seeking)
Operating environmental conditions	
Ambient temperature	5°C to 43°C (41°F to 109.4°F)
Relative humidity	20% to 80% (Maximum wet bulb temperature: 29°C (85°F))

Table 1-3 (cont.)

Non-operating environmental conditions	
Ambient temperature	-20°C to 51°C (-4°F to 125°F)
Relative humidity	5% to 95%
Heat dissipation	11.4 Watts Continuous seek (typical)
	9 Watts Standby (typical)
	5.6 Watts Motor off (typical)
Physical dimensions	(Except for front panel)
	Model M4852 Model M4853
Height	82.6 mm (3.25 in) 41 mm (1.62 in)
Width	146 mm (5.75 in) 146 mm (5.75 in)
Depth	203.2 mm (8 in) 203.2 mm (8 in)
Front panel dimensions	
Model M4852	85.8 x 149.3 mm (3.38 x 5.88 in)
Model M4853	42 x 148.0 mm (1.65 x 5.83 in)
Weight	1.3 kg (2.9 lbs)

1.2.4 Reliability specifications (Table 1-4)

Table 1-4 Reliability Specifications

MTBF	10,000 POH or more
MTTR	30 minutes
Unit life	5 years or 20,000 energized hours, whichever comes first
Media life	
Insertion	3×10^4 or more
Rotational life	3.5×10^6 pass/track or more
Tap-tap	10^5 on the same spot of a track
Error rate	
Soft read error	10^{-9} bit
Hard read error	10^{-12} bit
Seek error	10^{-6} seek

CHAPTER 2 OPERATION OF MAJOR COMPONENTS

2.1 System Operation

The M4852/M4853 Flexible Disk Drive consists of a medium rotating mechanism, two read/write heads, an actuator to position the read/write heads on tracks, a solenoid to load the read/write heads on the medium, and electronic circuits to read and write data, and to drive these components.

The rotation mechanism clamps the medium inserted into the drive to the spindle, which is directly coupled to the DC brushless direct-drive motor, and rotates it at 300 rpm. The positioning actuator moves the read/write head over the desired track of the medium. Then, the head loading solenoid loads the read/write head on the medium to read or write data.

2.2 Electronic Circuits

The electronic circuits to drive the individual mechanisms of the M4852/M4853 are located on a single printed-circuit board, which consists of the following circuits:

- o Line driver and receiver that exchange signals with the host system
- o Drive selection circuit
- o Index detection circuit
- o Head positioning actuator drive circuit
- o Head loading solenoid drive circuit
- o Read/write circuit
- o Write protect circuit
- o Track 00 detection circuit
- o Drive ready detection circuit
- o Head selection circuit
- o In use and panel indicator LED drive circuit

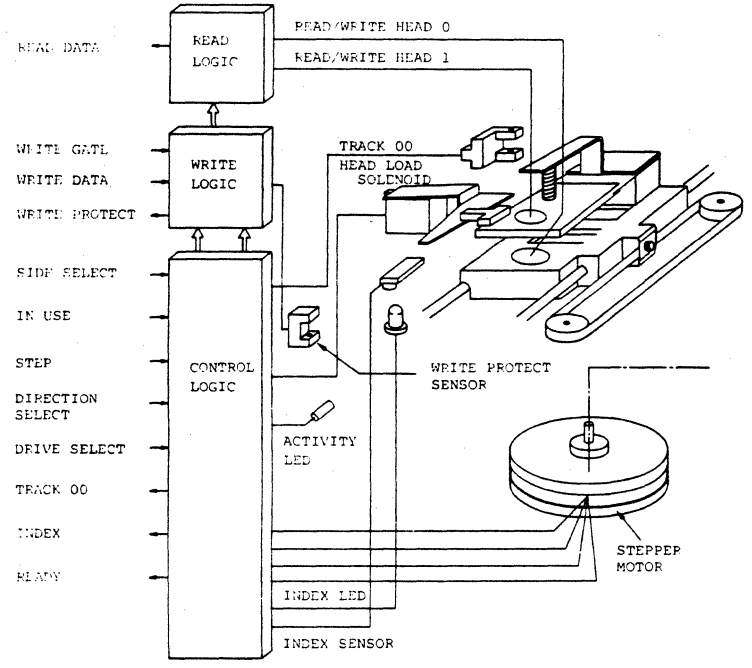


Fig. 2-1 M4853 Functional View

2.3 Rotation Mechanism

The diskette rotation mechanism uses the DC brushless direct-drive motor to directly rotate the spindle at 300 rpm.

2.4 Positioning Mechanism

The positioning mechanism positions the read/write heads as described below.

The head carriage assembly is fastened to the steel band secured around the capstan of a two-phase hybrid stepping motor; a 1.8° turn of the stepping motor moves the read/write head one track in the designated direction, thus positioning the read/write head.

This drive system is temperature compensated to minimize read/write head deviations from the disk tracks caused by ambient temperature change.

2.5 Read/Write Heads

The read/write heads are MnZn magnetic ferrite.

Each read/write head has three ferrite head cores, consisting read/write core and erase cores on both sides of the read/write core to erase the space between tracks (tunnel erase).

The two read/write heads, which are located face-to-face with a disk between them, are mounted on compliant, circular gimbal springs so that the heads track the disk with good contact to enable maximum reproduction of the signals from the disk. The high surface tracking ability of the circular gimbal keeps the disk free of stress, and thus improves diskette life.

CHAPTER 3 ELECTRICAL INTERFACE

There are two kinds of electrical interfaces: Signal interface and DC power interface.

The signal interface sends and receives control signals and read/write data between the M4853 and the host system via the J1/P1 connector.

The DC power interface drives the spindle drive motor of the M4853, and supplies power to the electronic circuits and the stepping motor which drives the read/write head positioning mechanism via the J2/P2 connector.

The signals and pin arrangement of these two types of interfaces are shown in Tables 3-1 and 3-2.

Table 3-1 DC Power Connector Pin Arrangement (J2/P2)

Source voltage	Pin number	Remarks
+12 V DC	1	
+12 V DC return	2	
+5 V DC return	3	
+5 V DC	4	

Table 3-2 Signal Connector Pin Arrangement (J1/P1)

Signal	Signal Pin Number	Ground Return Pin Number
SPARE	2	1
IN USE	4	3
DRIVE SELECT 3	6	5
INDEX	8	7
DRIVE SELECT 0	10	9
DRIVE SELECT 1	12	11
DRIVE SELECT 2	14	13
MOTOR ON	16	15
DIRECTION SELECT	18	17
STEP	20	19
WRITE DATA	22	21
WRITE GATE	24	23
TRACK 00	26	25
WRITE PROTECT	28	27
READ DATA	30	29
SIDE ONE SELECT	32	31
READY	34	33

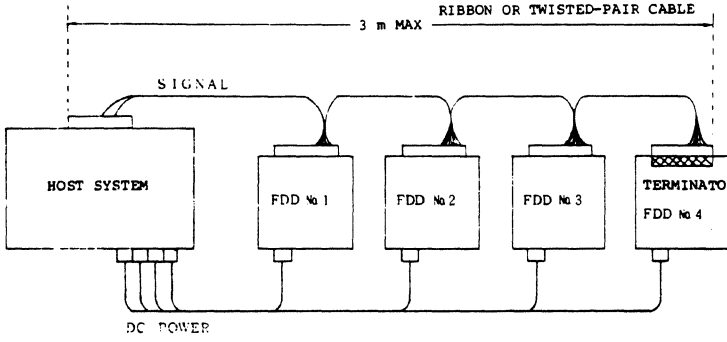


Fig. 3-1 Cabling Method (Sketch)

3.1.2 Line driver and line receiver

The recommended interface line driver and line receiver circuits for the host system and the drives are shown in Fig. 3-2.

It is suggested that a Schmitt trigger circuit with a hysteresis characteristic at the switching level be used for the line receiver to improve the noise resistance of the interface lines.

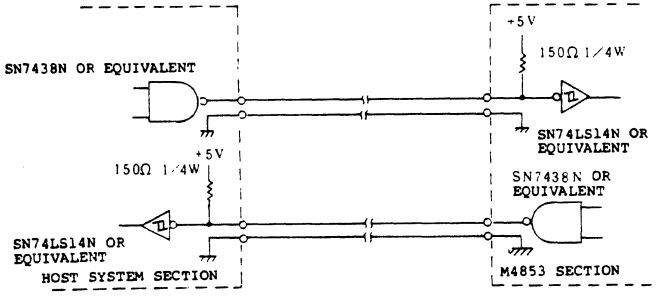


Fig. 3-2 Recommended Line Driver and Line Receiver Circuits

3.1 Signal Interface

The signal interface is classified into control signals and data signals. These interface signal lines are all at TTL levels. The meanings and characteristics of the signal levels are as follows:

- o True = Logical "0" = VL 0 V to +0.4 V
  Iin 40 mA maximum
- o False = Logical "1" = VH +2.5 V to +5.25 V
  Iin 0 mA
- o Input impedance = 150 Ohms

3.1.1 Cabling method and input line termination

The M4853 uses a daisy chain system of cable connections. A single ribbon cable or twisted-pair cable may be fitted with multiple connectors to permit connection of up to four drives.

The connected drives are multiplex-controlled by drive select lines, and any one of the drives can be accessed.

The cabling method and input line termination are shown in Fig. 3-1. A maximum of seven input signal lines, plus the drive select lines, may be terminated at the M4852/M4853. Proper operation of the drives requires termination at or near the drive connected to the end of the interface cable farthest from the host system.

The M4852 has detachable resistor modules and M4853 has jumper plug terminators mounted on the printed-circuit board to terminate these input signal lines.

When a drive is shipped from the factory, its terminators are installed on the printed-circuit board.

Keep the terminators connected in the drive that is connected to the end of the interface cable, and disconnect the terminators in all the other drives.

3.1.3 Jumpers

The jumpers on the printed-circuit board are used to set conditions for drive selection and head loading.

The uses of the individual jumper pins are as follows:

(1) MX

Jumper these pins when connecting only one FDD to the system.

The single drive then is always selected, permitting transmission and reception of input and output signals regardless of the conditions of drive select 0 to drive select 3.

Open these pins when connecting two or more FDDs.

(2) DS0 to DS3

When two or more FDDs are connected to the system, jumper one of DS0 to DS3 so that only the drive whose select line corresponds to the jumpered pin is selected by a logical "0" to permit transmission and reception of input and output signals.

For example, if DS0 is jumpered, its drive is selected when drive select 0 is at logical "0."

(3) HS and HM

These jumpers are used for setting head loading conditions.

If HS is jumpered, the heads are loaded by drive selection.

If HM is jumpered, the heads are loaded by turning the motor on.

Do not jumper HS and HM concurrently.

DS0 and HS are jumpered before shipment of the product from the factory. If different modes are desired, change the settings.

3.1.4 Input signal lines

The M4852/M4853 has 11 input signal lines. Input signals can be classified into two types: One is multiplexed in a multi-drive system; and the other performs a multiplex operation.

The multiplexing signals are as follows:

- o Drive select 0
- o Drive select 1
- o Drive select 2
- o Drive select 3

(1) Drive select 0 to drive select 3

When these drive select lines are at logical "0" level, a multiplexed I/O lines become active to enable read/write operation. These four separate input signal lines, drive select 0 to drive select 3, are provided for connecting four drives to one system and mutually multiplexing them. Jumper pins DS0, DS1, DS2, and DS3 on the printed-circuit board are used to select drives to be made active, corresponding to drive select lines.

DS0 is shorted before shipment from the factory, so this setting must be changed when establishing other select lines.

(2) Side one select

This interface line is used to select which of the two sides of the diskette should be read or written. When this line is at logical "1," the Side 0 head is selected; or when it is at logical "0," the Side 1 head is selected. If the polarity of the side one select signal is reversed, delay read/write operation by more than 100 μs before execution.

Upon completion of a write operation, reverse the polarity of the side one select signal after a delay of 1000 μs. The heads are tunnel erase type, with a physical core gap deviation between the read/write head and the erase heads so with no delay, non-erased areas would be generated on the diskette due to a timing difference between the write data area and the erase area during write operation. This is prevented by delaying the erase current cutoff time of a few hundred microseconds within the M4852/M4853. Therefore, the head select must not be reversed during this delay time. Also, the track access action must not be permitted for 1000 μs.

(3) Direction select

This interface line controls the direction. (inward or outward) in which the read/write head should be moved when a step signal pulse is applied.

If the signal is at logical "1," the read/write head moves from the center of the diskette outward; if it is at logical "0," the head moves inward.

(4) Step

This interface line is a pulse signal for moving the read/write head in the direction defined by the direction select line. The read/write head moves by one track each time a signal pulse is applied to the step line. The step line is normally logical "1," and the step operation starts with the trailing edge of a negative-going pulse (reversal from logical "0" to logical "1").

The direction select line must be reversed more than 1 μs before the trailing edge of the step pulse.

(5) Write gate

When this interface line goes to logical "0," the write driver becomes active and the data given to the write data line is written on the selected side of the diskette. When the interface line goes to logical "1," the write driver becomes inactive to enable the read data logic. The verified read data is obtained 1000 μs (maximum) after the write driver becomes inactive. Refer to CHAPTER 4 for the timing.

(6) Write data

Data to be written on the diskette is sent to this interface line.

This line is normally at logical "1," and reverses the write current at the leading edge of a negative-going data pulse (reversal from logical "1" to logical "0") to write data bits.

This line is enabled when the write gate is at logical "0," Fig. 3-3 shows the write data timing.

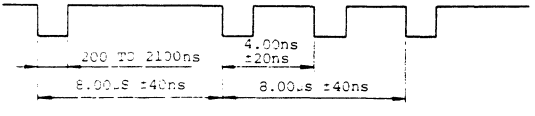


Fig. 3-3 Write Data Timing (FM Encoding)

(7) In use

An LED indicator on the front panel lights when this interface line goes to logical "0." The LED is also lit by the drive select.

(8) Motor on

This interface line starts the spindle motor when it goes to logical "0." The write gate does not go to logical "0" until more than 250 ms after the motor-on line goes logical "0."

The motor-on line goes logical "1" to stop the motor and keep it off while the drive is out of operation, thus prolonging motor life.

3.1.5 Output signal lines

The M4853 has five standard output signal lines.

(1) Index

This interface line is normally logical "1" but sends a logical "0" output pulse 4 ms wide each time the diskette makes one revolution (200 ms period).

This signal signifies the start of a track on the rotating diskette. The index signal timing is shown in Fig. 3-4.

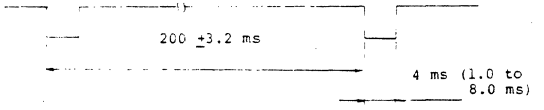


Fig. 3-4 Index Timing

(2) Track 00

When this interface line is at logical "0," it indicates that the read/write head of the selected drive is positioned on track 00. If the output of the selected drive is at logical "1," it indicates that the read/write head is positioned on a track other than track 00.

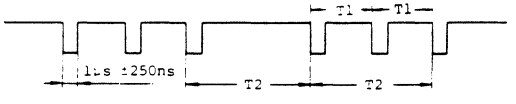
(3) Ready

This interface line is logical "1" when the door is open or no diskette is in the drive. The line goes logical "0" (ready) if an index pulse is detected twice or more when the index hole is correctly detected, and the DC power (+5 V and +12 V) supplied after a diskette is inserted into the drive and the door is closed.

(4) Read data

This interface line reads the data stored on the diskette with the read/write heads, and outputs raw data (combined clock and data signals) converted into pulse signals by an electronic circuit.

The read data line is normally logical "1" but it sends a logical "0" (negative-going) output pulse during a read operation. Fig. 3-5 shows allowable limits on timing variations with the usual diskette and bit shifts.



T_1 = 4.00 µs ±800 ns (Jitter due to rotation variation excluded)

T_2 = 8.00 µs ±1.6 µs (Jitter due to rotation variation excluded)

Fig. 3-5 Read Data Timing (FM Encoding)

(5) Write protect

This interface signal notifies the host system of the insertion of a diskette with a write protect notch into the drive. The signal goes to logical "0" when a write-protected diskette is inserted into the drive. When the signal is at logical "0," write on the diskette is inhibited even if the write gate line becomes active.

3.2 Power Interface

The M4852/M4853 requires two types of DC power supplies.

One is +12 V DC, which drives the drive motor to rotate the diskette. It is supplied to the stepping motor and the read/write circuit. The other is +5 V DC, which is used for the logic circuit and the read/write circuit.

NOTE

The index LED is driven by the +12 V DC.

3.2.1 DC power

DC power is supplied via connector J2/P2 on the back of the printed-circuit board. The specifications of the two DC voltages are shown in Table 3-3. The pin arrangement of connector J2/P2 is shown in Table 3-1.

Table 3-3 DC Power Specifications

DC voltage	Voltage variation	Current	Maximum ripple voltage (peak-to-peak)
+5 V DC	±0.25 V (±5%)	1.0 A maximum 0.5 A typical	50 mV
+12 V DC	±0.6 V (±5%)	1.00 A maximum 0.7 A typical at seek	100 mV

CHAPTER 4 FUNCTIONAL OPERATION

4.1 Power On Sequencing

No read/write operation may be performed during the period of 200 ms or more from the start of DC power supply until the control signal stabilizes and the drive is ready.

The read/write head may have been positioned on an incorrect track after switching the DC power on, so before starting a read/write operation, be sure to perform the step out operation until a track 00 signal is output to the interface line, and thus correctly position the read/write head.

4.2 Drive Selection

The M4852/M4853 daisy chain cabling system permits connection of multiple drives to a single cable.

These drives are selected when the drive select lines on the drive side become active. Only the drive whose drive select line is active sends and receives signals to and from the host system. The select lines on the drive must have different numbers if two or more drives are connected. If the same number is assigned, an operation error occurs due to interference among the interface output signals of the drives themselves.

4.3 Positioning Operation

The seek operation which moves the read/write head to the desired track selects a direction, inward or outward, depending on the polarity of the direction select signal, and moves the head by the step signal. If access to a track two or more tracks away is required, step pulses are continuously sent until the head moves to the desired track.

Head movement starts with the trailing edge of the step pulse. Fig. 4-1 Shows the operation timing.

4.4 Side One Selection

The read/write heads located on both sides of the diskette are selected by the side one select signal. When the side one select line is high, the Side 0 head is selected. When it is low, the Side 1 head is selected.

4.5 Read Operation

The required timing for read operations is shown in Figs. 4-1 and 3-5. These timing specifications are necessary for accurate read operation.

Two modes of encoding, FM and MFM, are used for the data stored on media. FM is used for single-density read, and MFM for double-density read.

A comparison of the FM and MFM encoding modes is shown in Fig. 4-2.

4.6 Write Operation

The requiring timing for write operation is shown in Fig. 3-3.

These timing specifications must be strictly observed to ensure an accurate write operation.

Write data can be encoded by either FM or MFM. The M4852/M4853 has good contact stability of the read/write heads on the medium and employs high-performance read/write heads, so no precompensation is necessary for correcting the big shift effect when writing data in the MFM mode (double density).

In case of applying write precompensation, smaller compensation is recommended such as 7.5% or smaller.

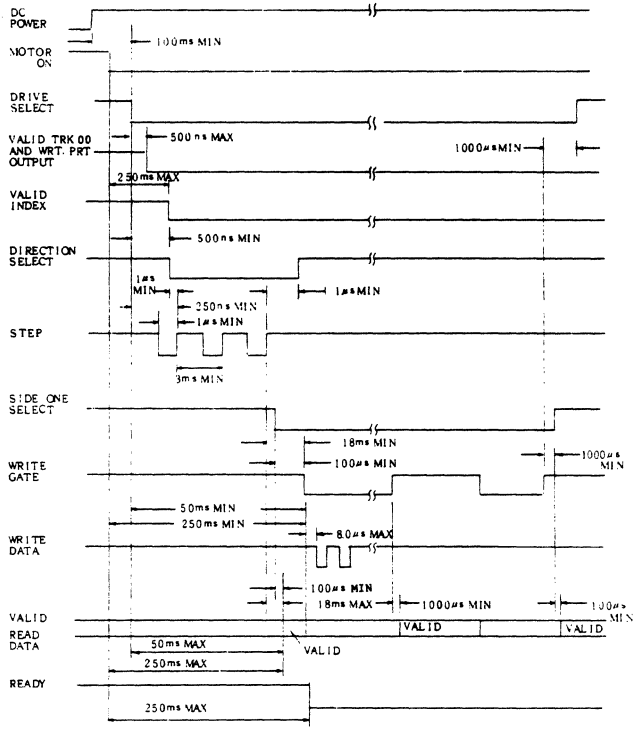


Fig. 4-1 Control and Data Timing

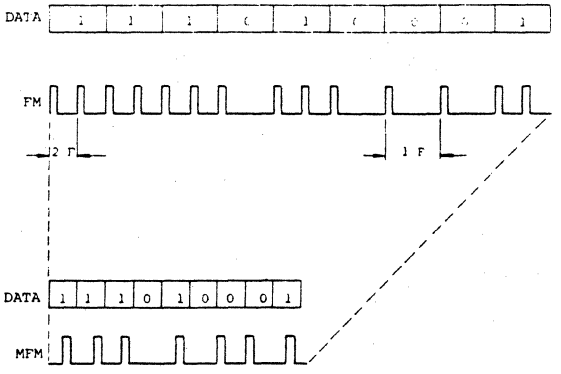


Fig. 4-2 Comparison of FM and MFM Encoding Systems

CHAPTER 5 PHYSICAL INTERFACE

Electronic interfaces between the M4852/M4853 and the host system are accomplished with three connectors. Connector J1 is for the signal interfaces, connector J2 for the DC power supplies, and connector J5 for frame grounding. The connectors used for the M4852/M4853, and recommended mating connectors are described below.

5.1 Signal Connectors

J1 is a card-edge type, 34-pin (for both sides, or 17 pins for a single side) connector with even-numbered pins (2, 4, to 34) on the parts side and odd-numbered pins (1, 3, to 33) on the soldered side.

A key slot is provided between pins 4 and 6 for the polarity reversal prevention.

The dimensions of J1 are shown in Fig. 5-1.

Recommended P1 connectors that mate with J1 are shown in Tables 5-1 and 5-2.

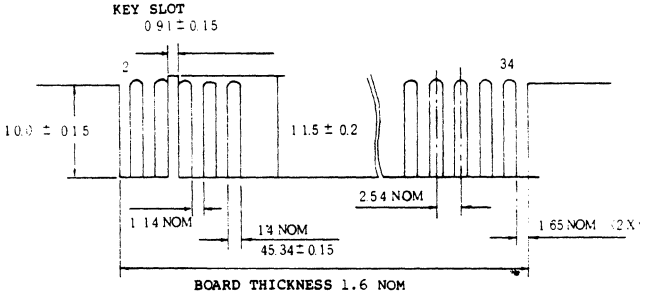


Fig. 5-1 Connector J1 Dimensions (mm) and Pin Numbers

Table 5-1 Connectors for Twisted-Pair Cable (P1)

Parts	Crimp Type	Solder Type
	AMP P/N	AMP P/N
Housing	583717-5	583717-5
Contact	1-583616-1	583854-3
Polarity key	583274-1	583274-1
Crimping tool	90268-1	
Extraction tool	91073-1	91073-1
Twisted-pair cable (3 m max.)	AWG 26	AWG 26

Table 5-2 Connector for Flat Cable (P1)

Parts		3M P/N
Connector		3463-0001
Polarity key		3439-0000
Crimping tools	Press	3440
	Locator press	3443-11
	Platen	3442-3
Flat cable (3 m max.)		3365/34

5.2 DC Power Connector (J2/P2)

J2 is a four-pin DC power connector made by AMP, located on the back of the printed-circuit board. Pin 4 on connector J2 is located closest to J1/P1; the arrangement of the pins as viewed from the side is shown in Fig. 5-2. Pin numbers are shown on the parts side.

The connectors on the drive side and cable side are shown in Table 5-3.

Table 5-3 DC Power Connectors

Parts	P2 (Cable Side)	J2 (Drive Side)
	AMP P/N	AMP P/N
Housing	1-480424-0	172349-1
Contact (4 pins)	60619-1	-
Crimp tool	90124-2	-
Extraction tool	1-305183-2	-
Cable (3 m max.)	AWG 18	-

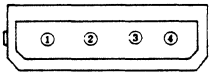


Fig. 5-2 Connector J2

5.3 Frame Ground Connector (J5/P5)

FASTON Terminal	Crimp Terminal
AMP P/N 60920-1	AMP P/N 60972-1

5.4 Interface Connector Physical Location

Fig. 5-3 shows the physical locations of the interface connectors used for the M4853.

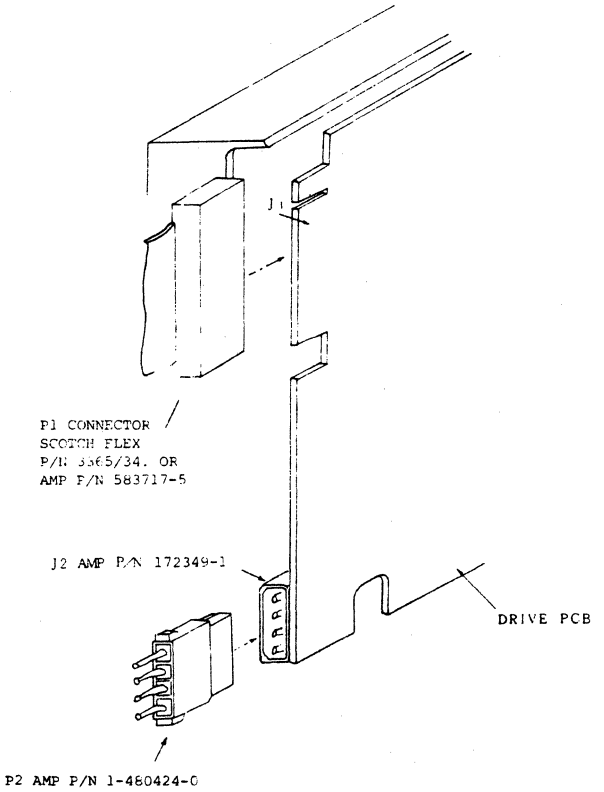


Fig. 5-3 Connector Location Diagram (Rear View)

CHAPTER 6 DRIVE PHYSICAL SPECIFICATIONS

6.1 Installation Direction

Install the M4852/M4853 disk drive in the directions shown in Fig. 6-1.

The slant mount should be within 10 degrees.

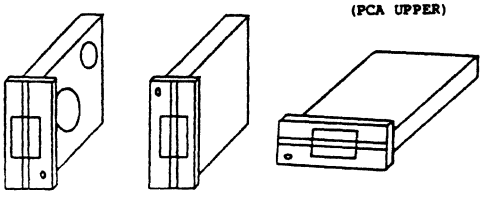


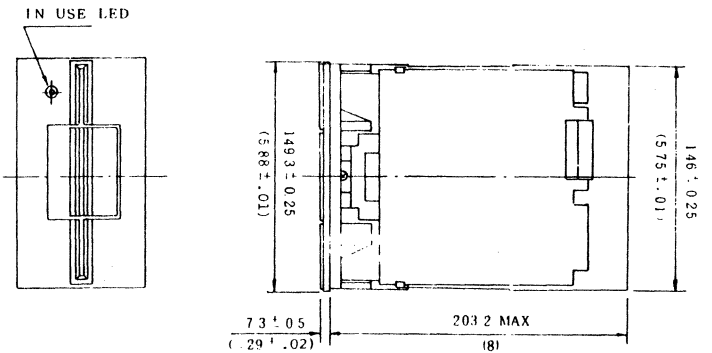
Fig. 6-1 Disk Drive Installation Directions

6.2 Dimensions of M4852

See Fig. 6-2.

6.3 Dimensions of M4853

See Fig. 6-3.



Note: All dimensions are in mm
dimensions in ( ) are in
inches

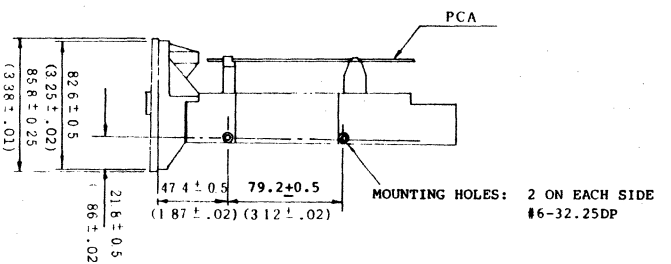
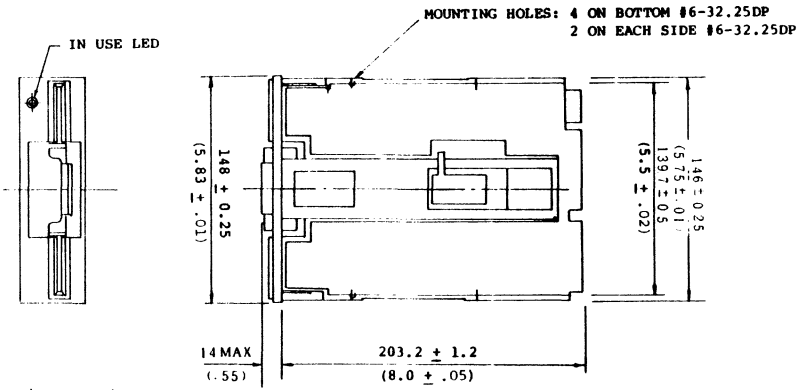


Fig. 6-2 Dimensions of M4852



Note: All dimensions are in mm
dimensions in ( ) are in inches

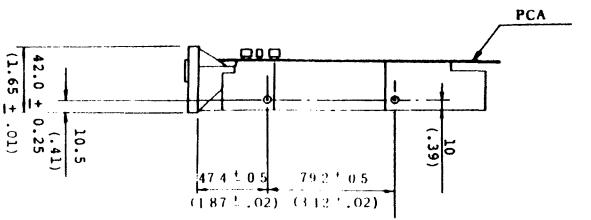


Fig. 6-3 Dimensions of M4853

CHAPTER 7 ERROR DETECTION AND CORRECTION

This chapter describes the general cause analysis and corrective procedures to be followed in the event that data errors occur.

7.1 Write Errors

If an error occurs during a write operation, it can be detected by performing a read operation on the diskette rotation immediately following the write operation. This is generally called a write check, which is an effective means of preventing write errors. It is recommended, therefore, that a write check be made without fail.

If a write error occurs, repeat the write operation and conduct a write check. If data cannot be correctly written even after the write operation is repeated about ten times, perform a read operation on another track to determine whether the data can be read correctly. If so, a specific track of the diskette is defective. If data cannot be correctly read on the other track, the drive is assumed to have some trouble. If the diskette is defective, replace it.

7.2 Read Errors

Most data errors that occur are soft errors. If a read error occurs, repeat the read operation to recover the data.

The following are possible main causes of soft errors:

- Dust is caught between the read/write head and diskette causing a temporary fault in head contact. Such dust is generally removed by the self-cleaning wiper of the jacket, and the data is recovered by the next re-read operation. If read/write is continued for a long time in a very dusty environment, however, hard errors can result from a damaged diskette surface.

- Random electrical noise ranging in time from a few microseconds to a few milliseconds can also cause read errors. Spike noise generated by a switching regulator, particularly one that has short switching intervals, deteriorates the signal-to-noise ratio, and increases the number of re-read operations for data recovery. It is necessary, therefore, to make an adequate check on the noise levels of the DC power supplies to the drive and frame grounding.

- Written data or diskettes may have so small a defect as cannot be detected by a data check during write operation.

- Fingerprints or other foreign matter on a written diskette can also cause a temporary error. If foreign matters is left on a

written diskette for a long time, it can adhere to the diskette, possibly causing a hard error.

It is recommended that the following read operations be performed to correct these soft errors:

- Step 1: Repeat the read operation about ten times until the data is recovered.
- Step 2: If the data cannot be recovered by Step 1, move the head to other track, the opposite direction of the previous track position before the designated track, and then return the head to the original position.
- Step 3: Repeat an operation similar to Step 1.
- Step 4: If the data cannot be recovered, take the error as a hard error.

CHAPTER 8 RESHIPMENT PRECAUTIONS

When reshipping the drive, make sure the protection sheet for transportation is in place in the drive, and close the door.

MITSUBISHI ELECTRIC CORPORATION
HEAD OFFICE MITSUBISHI DENKI BLDG MARUNOUCHI TOKYO 100 TELEX J24532 CABLE MELCO TOKYO

MITSUBISHI ELECTRONICS AMERICA, INC.
USA OFFICE 991 KNOX STREET TORRANCE CA 90502 TEL (213) 515-3993 TELEX 664787 MELA TRNC

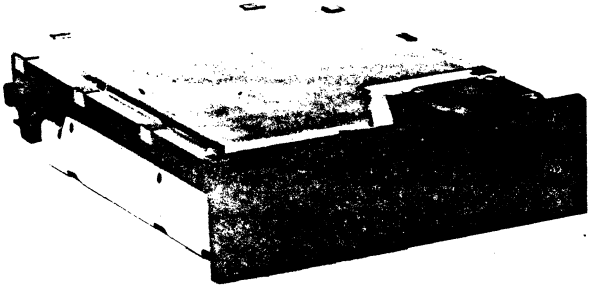
*SJ2-G3375B-1st Edition June 1982
*SJ2-3375C-2nd Edition March 1983
8303-700 A.S.K. 58-586

APPENDIX C: TANDON RIGID DISK DRIVES —TM251, TM252

Tandon

TM251, TM252

RIGID DISK DRIVES



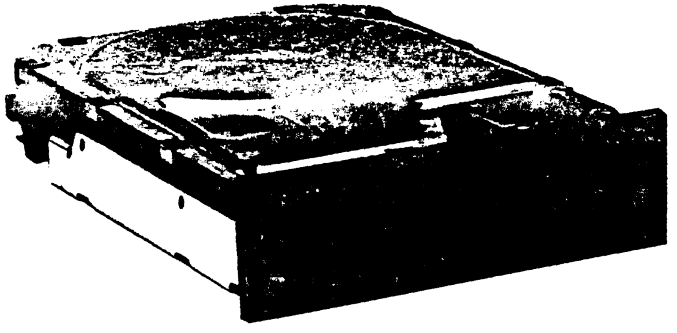
PRODUCT SPECIFICATION AND USER'S MANUAL

NOTICE

This document is intended to provide the user with detailed information adequate for the efficient installation, operation, and service of the equipment involved.

However, while every effort has been made to keep the information contained herein current and accurate as of the date of publication, no guarantee is given or implied as to its accuracy.

TM251, TM252
345 TRACKS PER INCH
PRODUCT SPECIFICATION AND USER'S MANUAL



Tandon CORPORATION
20320 PRAIRIE STREET
CHATSWORTH, CALIFORNIA 91311

CONTENTS

ILLUSTRATIONS

FIGURES

TABLES

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

This manual provides useful information to assist the customer when incorporating the Tandon rigid disk drive into a system.

Tandon Corporation's TM250 series of drives are full feature, one-half height, 5-1/4-inch, rigid disk drives. They are compact data storage devices that contain one or more 130-millimeter plated aluminum platters within a sealed housing.

The TM250 series includes Model Numbers TM251 and TM252, which have one or two recording platters, and use two or four recording heads, respectively.

1.1 SCOPE OF THE DOCUMENT

Section 1 of this manual contains a general description of the disk drives. Section 2 contains the product specifications. Section 3 provides information on operation of the drives.

1.2 PURPOSE OF THE DRIVE

The 5-1/4-inch disk drive is a rotating disk memory device designed for random access data storage and retrieval. Typical applications include word processing systems, entry level microprocessor systems, intelligent calculators, program storage, small business computer systems, and any application in which low cost, random access data storage is required.

1.3 MAJOR FEATURES

MICROPROCESSOR CONTROL

The TM250 series of drives feature an onboard microprocessor. The microprocessor provides five major functions:

1. Self-calibration on power-up.
2. Buffered seek timing for improved access times.
3. Improved positioning with reduced hysteresis.
4. Write current switching for optimal recording quality.
5. Power and track fault detection.

DAISY CHAIN CAPABILITY

The drive provides the address selection and gating functions necessary to daisy chain a maximum of four units at the user's option. The last drive on the daisy chain terminates the interface. The terminations are accomplished by a resistor array plugged into a DIP socket.

INDUSTRY STANDARD INTERFACE COMPATIBILITY

The drive is compatible with controllers that use an industry standard interface.

AIR FILTRATION

A self-contained, recirculating air filtration system supplies clean air through a 0.3-micron filter. A secondary absolute filter is provided to allow pressure equalization with the ambient atmosphere without contamination. The entire head-disk-actuator compartment is maintained at a slightly positive pressure to further ensure an ultraclean environment.

COMPACT SIZE

The reduced height of the drive occupies only one-half the mounting space required for a conventional drive.

1.4 FUNCTIONAL DESCRIPTION

The drives are fully self-contained, and require no operator intervention during normal operation. During the power-up sequence, the spindle motor reaches 3,600 RPM, and the positioning mechanism recalibrates the recording heads to Track 0. At this time, a Ready signal on the interface indicates the drive is ready for operation.

The head is positioned over the desired track by means of a four-phase stepper motor/band assembly and its associated electronics. This positioner uses a one-step rotation to cause a one-track radial movement. Subsequently, the recording heads can be positioned over the desired cylinders, and the data can be read or written from the appropriate track by selecting the desired head.

Typically, the drive uses MFM write and read data recording methods. Data recovery electronics include a low-level read amplifier, differentiator, a zero-crossover detector, and digitizing circuits. No data encoding or decoding feature is provided on the drives.

The drives have the following sensor systems:

1. An optical Track 0 switch senses when the Head Carriage Assembly is positioned at Track 0.
2. An index sensor, which consists of a magnetic pick-up and index hole positioned to provide an analog signal when an index hole is detected.

1.5 PHYSICAL DESCRIPTION

A representative drive is shown in Figure 1-1. The drives contain 130 millimeter storage media that rotate at 3,600 RPM, using a direct drive, brushless D. C. motor. The recording is accomplished by non-contact standard recording heads that are moved by a precision split band positioning device and stepper motor.

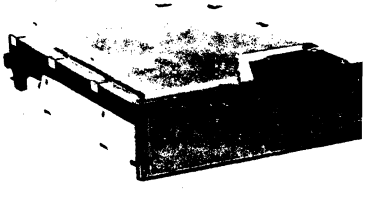


FIGURE 1-1
DISK DRIVE

The Head Disk Assembly is enclosed in a sealed cast aluminum housing, which includes an air filtration system to ensure a contamination-free environment. The housing is shock mounted to a metal frame that has the front panel attached, and threaded holes on the sides and bottom for mounting the drive onto a chassis.

In addition, the drive includes the read/write and control electronics, servo spindle control electronics, and an index sensor.

SECTION 2

PRODUCT SPECIFICATIONS

INTRODUCTION

This section contains the mechanical and operational, reliability and environmental specifications for the TM251 and TM252 disk drives.

2.1 MECHANICAL SPECIFICATIONS

The mechanical and physical dimensions are contained in Figure 2-1.

2.2 ELECTRICAL AND OPERATIONAL SPECIFICATIONS

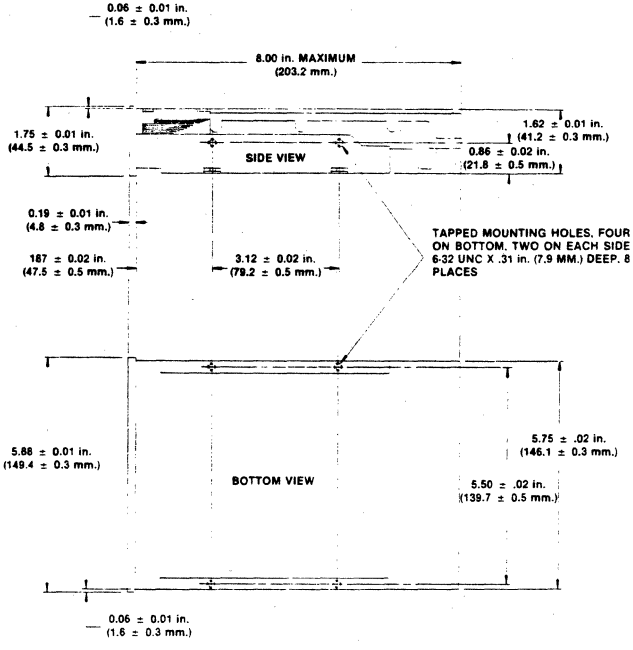
The electrical and operational specifications are contained in Table 2-1. Typical starting current requirements at nominal voltage are contained in Figure 2-2.

2.3 RELIABILITY SPECIFICTIONS

The reliability specifications are contained in Table 2-2.

2.4 ENVIRONMENTAL SPECIFICATIONS

The environmental specifications are contained in Table 2-3.



NOTE: WEIGHT IS 1.47 KILOGRAMS, 3.25 POUNDS MAXIMUM.

FIGURE 2-1
DISK DRIVE OUTLINE DRAWING

TABLE 2-1
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Media	Lubricated, 130 millimeter, plated aluminum disk
Tracks Per Inch	345 TPI
Spacing, track to track	2.9 milinches
Number Of Cylinders	306 cylinders
Number Of Tracks	
TM251	612 tracks
TM252	1,224 tracks
Disk Speed	3,600 RPM ± 1 percent
Average Latency	8.33 milliseconds
Start Time	15 seconds maximum
Stop Time	15 seconds maximum
Seek Time, track to track	3 milliseconds
Head Settling Time, last track accessed	15 milliseconds
Average Access Time, including head settling time, 3 millisecond step rate	321 milliseconds
Average Access Time Using Buffered Seek, including head settling time	85 milliseconds
Transfer Rate	5 megabits per second

TABLE 2-1 (CONTINUED)
ELECTRICAL AND OPERATIONAL SPECIFICATIONS

Maximum Flux Reversal Density	9090 FRPI
Unformatted Capacity Per Drive	
TM251	6.38 megabytes
TM252	12.76 megabytes
Unformatted Capacity Per Surface	3.19 megabytes
Unformatted Capacity Per Track	10.4 kilobytes

POWER REQUIREMENTS

+ 12 volts D. C. ± 10 percent, 1.2 amperes typical, 3.6 amperes maximum during motor start-up, not to exceed 12 seconds, 2 amperes maximum running, with no more that 50 millivolts Periodic and Random Deviation (PARD).

+ 5 volts D. C. ± 5 percent, 0.7 amperes typical, 1.2 amperes maximum running, with no more than 50 millivolts PARD.

There are no restrictions in sequencing power supplies on or off.

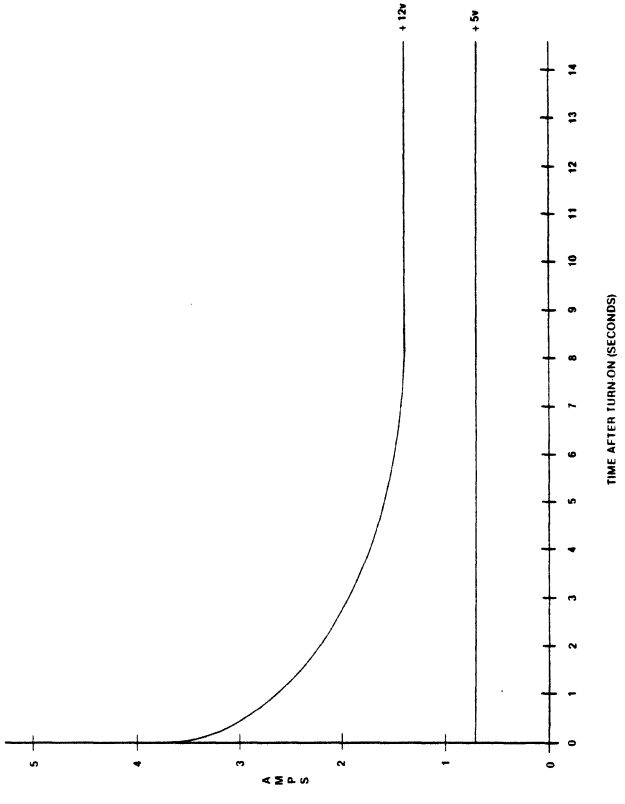


FIGURE 2-2
TYPICAL STARTING CURRENTS

TABLE 2-2
RELIABILITY SPECIFICATIONS

SOFT AND HARD READ ERROR RATES, EXCLUSIVE OF MEDIA DEFECTS

For data that has been verified previously as error free, and when used in conjunction with a data separator and phase lock loop of good design, the recoverable (soft) read error rate for any subsequent read operation shall not exceed one error in 1×10^{10} bits transferred. A recoverable read error is an error that may be corrected within five attempts to reread the data.

The nonrecoverable (hard) read error rates shall not exceed one error in 1×10^{12} bits transferred. A nonrecoverable read error is an error that may not be corrected within five attempts to reread data, providing that the writing of the data previously has been verified as correct. The seek error rate is not to exceed one error in 1×10^{6} seeks.

MEDIA DEFECTS

Any defects on the media surface will be identified on a defect map provided with each drive. This defect map will indicate the head number, track number, and number of bytes from index for each defect. Each defect shall be no longer than 16 bytes. Cylinders 000 and 001 are guaranteed error free.

The map is offered as a guide only. The number of defects and their location can change due to customer system variations such as data separators.

Mean Time Between Failures	11,000 power on hours
Mean Time To Repair	30 minutes
Component Design Life	5 years
Preventative Maintenance	Not required

TABLE 2-3
ENVIRONMENTAL SPECIFICATIONS

Ambient Temperature	
Operating	4°C to 50°C, 39°F to 122°F
Nonoperating	−40°C to 60°C, −40°F to 140°F
Temperature Gradient	
Operating	10°C per hour, 18°F per hour
Nonoperating	Below that causing condensation
Relative Humidity	8-to-80 percent, noncondensing
Relative Humidity Gradient	
Operating	20 percent per hour
Nonoperating	Below that causing condensation
Maximum Wet Bulb Temperature	26°C, 78.8°F, without condensation
Elevation	
Operating	Density Altitude: −457 to 2,972 meters, −1,500 to 9,750 feet
Nonoperating	Sea level to 3,650 meters, Sea level to 12,000 feet

SECTION 3

OPERATION

INTRODUCTION

This section contains information pertinent to the handling, inspection, installation, and operation of the TM250 series of drives.

3.1 UNPACKING THE DRIVE

Each drive is shipped in a protective container which, when bulk packaged, minimizes the possibility of damage during shipment.

The following procedure is recommended for unpacking the drive.

1. Place the shipping container on a flat work surface.
2. Visually examine the shipping container for damage.
3. Cut the tape on the shipping container.
4. Remove the foam lid and pads from the shipping container.
5. Remove the inner container.
6. Remove the drive from the inner container.
7. Place the drive on a foam lined surface.
8. Notify the carrier immediately if any damage is found.

CAUTION

Do not manually rotate the stepper motor or spindle motor. Damage to the heads and disk may result.

NOTE

The inside chamber of the drive is a sealed compartment that must not be opened.

When returning the drive to the service center, be sure to use prior steps in reverse order, and ensure the foam stiffeners are in the proper location, with the cardboard dividers properly in place between the drives (see Figure 3-1).

3.2 PREINSTALLATION CHECKOUT

Before applying power to the drive, inspect for the following:

1. Ensure the front panel is secure.
2. Ensure the circuit board is secure.
3. Ensure the connectors are firmly seated.
4. Ensure there is no debris or foreign material between the frame and the head/disk casting.
5. Ensure the head/disk housing can move freely on the shock mounts of the frame.
6. Ensure the termination resistor pack and jumper blocks are firmly seated and in the correct configuration.

3.3 MOUNTING THE DRIVE

The drive can be mounted in any vertical or horizontal plane. Eight 6-32 tapped holes are provided for mounting: two on each side and four on the bottom of the frame (see Figure 2-1). The drive

is manufactured with some critical internal alignments that must be maintained. Hence, it is important the mounting hardware does not introduce significant stress on the drive.

Any mounting scheme in which the drive is part of the structural integrity of the enclosure is not permitted. Mounting schemes should allow for adjustable brackets or incorporate resilient members to accommodate tolerances.

DUST COVER

The design of an enclosure should incorporate a means to prevent contamination from loose items, e. g., dust, lint, and paper chad since the drive does not have a dust cover.

FREE AIR FLOW

When the drive is mounted so the components have access to the free flow of air, normal convection cooling allows operation over the specified temperature range (see Table 2-3).

CONFINED ENVIRONMENT

When the drive is mounted in a confined environment, air flow must be provided to maintain specified air temperatures in the vicinity of the motors and the circuit boards.

3.4 INTERFACE CONNECTORS

The electrical interface between the drive and the host system is via three connectors. J1 provides control signals for the drive (see Figure 3-2). J2 provides for the radial connection of read/write data signals (see Figure 3-3). J3 provides for D. C. power (see Figure 3-4).

Table 3-1 contains interface lines. The interface description of the connectors, and the location of each, is contained in this section.

J1/P1 CONNECTOR

Connection to J1 is through a thirty-four-pin connector. Figure 3-2 contains the dimensions of this connector. The pins are numbered 1 through 34. The recommended mating connector for P1 is AMP connector P/N 499496-9.

J2/P2 CONNECTOR

Connection to J2 is through a 20-pin connector. Figure 3-3 contains the dimensions of this connector. The recommended mating connector for P-2 is AMP connector P/N 499497-4.

J3/P3 CONNECTOR

D. C. power connector J3 is a four-pin AMP Mate-N-Lok connector, P/N 350211-1, mounted on the component side of the circuit board. The recommended mating connector, P3, is AMP P/N 1-480424-0, utilizing AMP pins P/N 60619-4. J3 pins are labeled on the J3 connector (see Figure 3-4). J3 cabling must be 18 AWG, minimum.

FRAME GROUND CONNECTOR

The frame ground connector is Faston AMP P/N 61761-2. The recommended mating connector is AMP P/N 62187-1. To realize error rates (see Table 2-2), it must be connected directly to the centrally located system ground via an 18 AWG, minimum, cable.

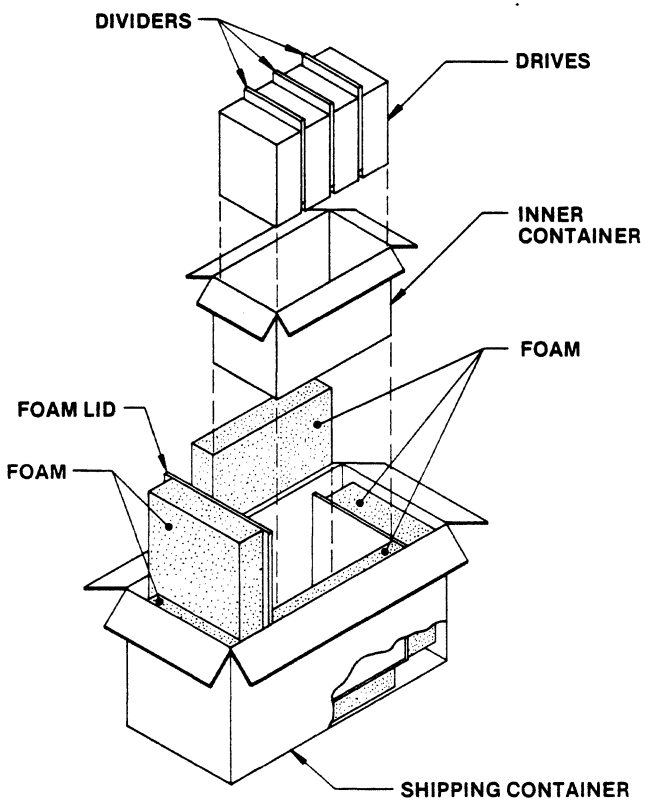


FIGURE 3-1
MULTIPACK SHIPPING CONTAINER

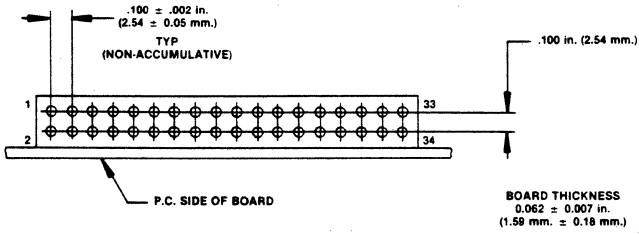


FIGURE 3-2
J1 EDGE CONNECTOR DIMENSIONS

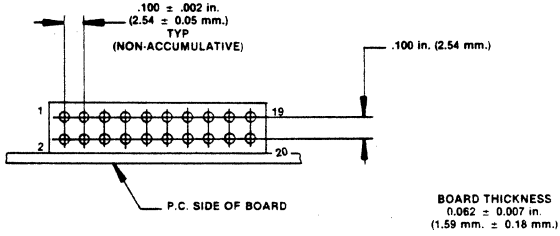


FIGURE 3-3
J2 EDGE CONNECTOR DIMENSIONS

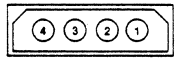


FIGURE 3-4
J3 POWER CONNECTOR

TABLE 3-1
DRIVE INTERFACE SIGNALS AND PIN ASSIGNMENTS

Connector	Interface Pin Number: Signal	Ground	Signal Type	I/O	Name of Signal
P1	2	(1)	S	I	Spare
↑	4	(3)	S	I	Spare
	6	(5)	S	I	Write Gate
	8	(7)	S	O	Seek Complete
	10	(9)	S	O	Track 0
34-Pin	12	(11)	S	O	Fault
Ribbon	14	(13)	S	I	Head Select 2^0
Daisy	16	(15)	—	—	Reserved (To J2- 7)
Chain	18	(17)	S	I	Head Select 2^1
|	20	(19)	S	O	Index
|	22	(21)	S	O	Ready
|	24	(23)	S	I	Step
|	26	(25)	S	I	Drive Select 0
|	28	(27)	S	I	Drive Select 1
|	30	(29)	S	I	Drive Select 2
↓	32	(31)	S	I	Drive Select 3
P1	34	(33)	S	I	Direction In
P2	1	(2)	S	O	Drive Select
↑	3	(4)	S	—	Spare
|	5	(6)	—	—	Reserved
|	7	(8)	—	—	Reserved (To J1- 16)
20-Pin	9	(10)	—	—	Spare
Ribbon	11	(12)	—	—	Ground
Radial	13	—	D	I	+ Write Data
|	14	—	D	I	- Write Data
|	15	(16)	—	—	Ground
|	17	—	D	O	+ Read Data
↓	18	—	D	O	- Read Data
P2	19	(20)	—	—	Ground
P3	1			—	+ 12 volts D. C. In
Radial	2			—	+ 12 volts D. C. Return
Radial	3			—	+ 5 volts D. C. Return
P3	4			—	+ 5 volts D. C. In

NOTES:
S = Single Ended
D = Differential
I = Drive Input
O = Drive Output

3.5 INTERFACE LINE DESCRIPTIONS

The interface for the TM250 series drive is available in one configuration. It is compatible with industry standard drives. Compatibility is defined as using the same pin assignment where the signal and function are common. Table 3-1 contains pin assignments.

The interface may be connected in the radial or daisy chain configuration (see Figures 3-5 and 3-6).

INPUT CONTROL SIGNALS

The input control signals are of two kinds: those to be multiplexed in a multiple drive system and those that do the multiplexing. The input control signals to be multiplexed are: Reduced Write Current, Write Gate, Head Select Line 2^0, Head Select Line 2^1, Step, and Direction In. The multiplexing signal is Drive Select 0, Drive Select 1, Drive Select 2 or Drive Select 3.

The input signals have the following electrical specifications, as measured at the drive. Figure 3-7 illustrates the recommended circuit.

True: 0.0 volt D. C. to 0.4 volt D. C. at I = – 40 milliamperes, maximum

False: 2.5 volts D. C. to 5.25 volts D. C. at I_I = 250 microamperes, maximum (open)

All input signals share a 220/330 ohm resistor pack for line termination. Only the last drive in the chain should have the resistor pack installed.

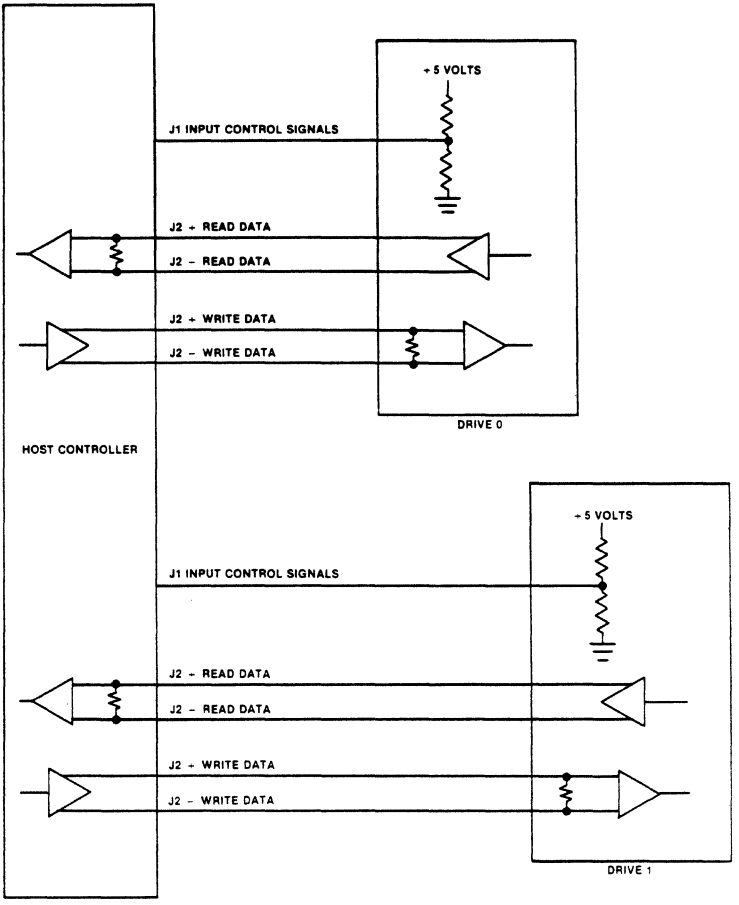


FIGURE 3-5
RADIAL CONFIGURATION

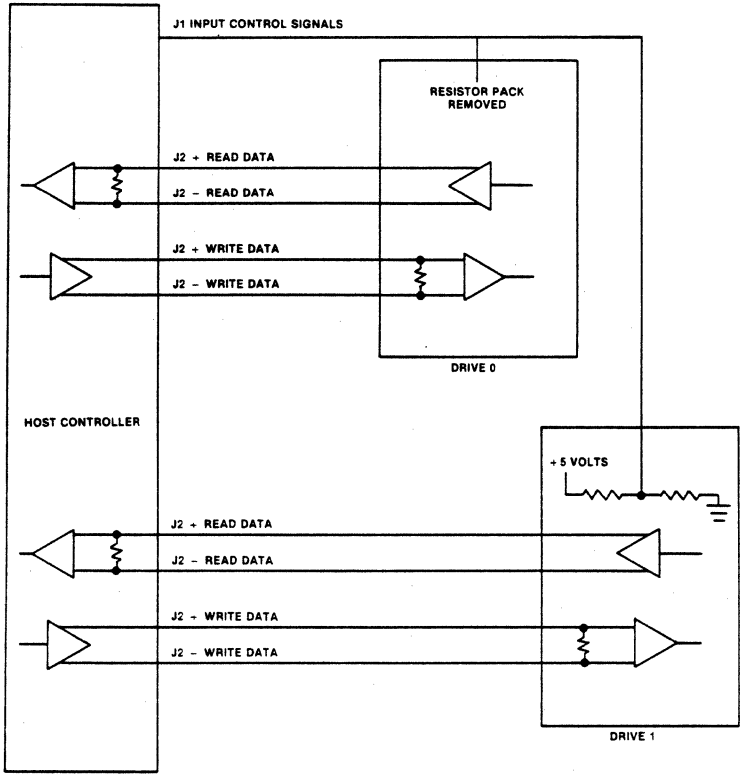


FIGURE 3-6
DAISY CHAIN CONTROL LINES

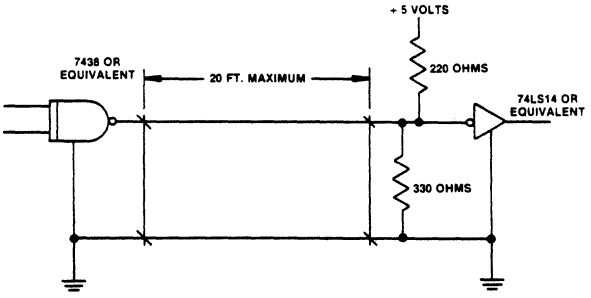


FIGURE 3-7
CONTROL SIGNAL/DRIVER RECEIVER CIRCUIT COMBINATION

WRITE GATE

The active state of this signal or logical zero level enables write data to be written on the disk. The inactive state of this signal enables the data to be transferred from the drive. In addition, the inactive state enables the step pulse to step the read/write actuator.

HEAD SELECT LINES 2^0 AND 2^1

These two lines provide for the selection of each read/write head in a binary coded sequence. Head Select Line 2^1 is the least significant line. The heads are numbered 0 through 3. When all Head Select lines are false, Head 0 is selected. Table 3-2 describes which head is selected for the head select lines.

Head recovery time (head-to-head select, write-to-read recovery, or read-to-write recovery) is 2.4 microseconds, maximum.

STEP

This interface line is a control signal that causes the read/write heads to move with the direction of motion defined by the Direction In line.

The access motion is initiated at the logical true-to-logical false transition or the trailing edge of this signal pulse. Any change in the Direction In line must be made at least 100 nanoseconds before the true-to-false edge of the step pulse. The quiescent state of this line should be held logically false.

The read/write head moves at the rate of the incoming step pulses. The minimum time between successive steps is three milliseconds, except during execution of a buffered seek. The minimum pulse width is one microsecond. Figure 3-8 illustrates the step timing.

TABLE 3-2
HEAD SELECT LINES

Head Select Line 2^1	Head Select Line 2^0	Head Selected
1	1	0
1	0	1
0	1	2
0	0	3

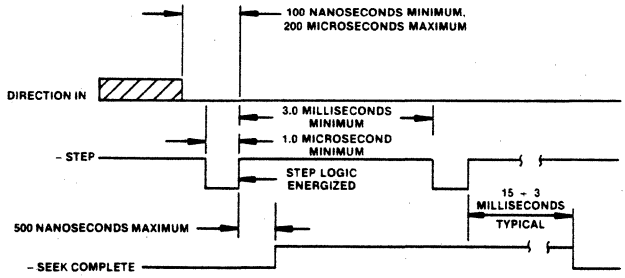


FIGURE 3-8
STEP MODE TIMING

BUFFERED SEEK

The buffered seek uses an onboard microprocessor that calculates the most efficient seek algorithm for the user. The user need only issue step pulses in accordance with the timing shown (see Figure 3-9). Step pulses are issued in a 1:1 ratio to the cylinders moved. If more pulses are issued than there are cylinders left to move, the heads soft stop at the last cylinder.

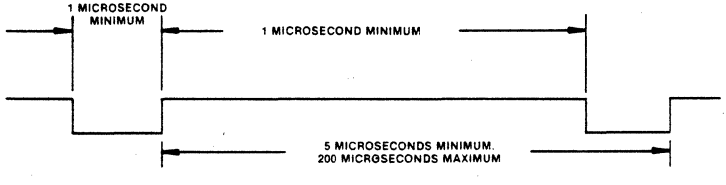


FIGURE 3-9
BUFFERED SEEK STEP PULSES

DIRECTION IN

This signal defines the direction of motion of the read/write head when the Step line is pulsed. An open circuit or logical false defines the direction as "out". If a pulse is applied to the Step line, the read/write heads move away from the center of the disk. If this line is true, the direction is defined as "in", and the read/write heads move in toward the center of the disk.

Seek Complete must be true prior to changing directions and the application of additional step pulses.

REDUCED WRITE CURRENT

The Reduced Write Current input line is terminated, but is not used in the TM250 series drives. The microprocessor automatically switches write current.

DRIVE SELECT 0 THROUGH DRIVE SELECT 3

These control signals enable the selected drive's input receivers and output drivers. When logically false, the output drivers are open circuits and the input receivers do not acknowledge signals presented to them.

Selecting the appropriate jumper block at W9 through W12 determines which select line activates the drive.

NOTE

Only one drive may be selected at a time.

OUTPUT CONTROL SIGNALS

The output control signals are driven with an open collector output stage capable of sinking a maximum of 40 milliamperes in a true state, with a maximum voltage of 0.4 volt measured at the driver. When the line driver is in the false state, the driver transistor is off, and the collector cutoff is a maximum of 250 microamperes.

All J1 output lines are enabled by the respective Drive Select lines.

SEEK COMPLETE

The Seek Complete signal goes true when the read/write heads have settled on the final track at the end of a seek. Reading or writing should not be attempted when Seek Complete is false.

Seek Complete goes false:

1. When a recalibration sequence is initiated by the microprocessor at power on because the read/write heads are not over Track 0.

2. 500 nanoseconds, maximum, after the trailing edge of a step pulse or a series of step pulses.

3. When power is momentarily lost, Seek Complete is false when power is restored and remains false until an automatic recalibration is completed.

TRACK 0

The Track 0 signal indicates a true state only when the drive's read/write heads are positioned at Track 0, the outermost data track.

FAULT

The Fault signal is used to indicate a condition exists in the drive that could cause improper writing on the disk. When this line is true, further writing is inhibited, as are other drive functions, until the condition is corrected.

This condition is caused by either the + 12 volt or + 5 volt supply dropping below the specified limits, and on power up until a successful recalibration sequence is completed.

INDEX

The Index signal is provided once each revolution, 16.7 milliseconds nominal, to indicate the beginning of the track. Normally, this signal is false and makes the transition to true to indicate Index. Only the transition from logical false to logical true is valid.

READY

When true, the Ready signal, together with Seek Complete, indicates that the drive is ready to read, write or seek, and the I/O signals are valid. When this line is false, all controller-initiated functions are inhibited.

The typical time after power on for Ready to be true is fifteen seconds. Track 0, Seek Complete, and Ready come true sequentially during power on.

SELECT STATUS

A Status line is provided at the J2/P2 connector to inform the host system of the selection status of the drive.

The Drive Selected line is driven by a TTL open collector drive (see Figure 3-7). This signal goes active only when the drive is programmed as Drive X, X = 0, 1, 2, or 3, by programming the shunt on the drive, and the Drive Select X line at J1/P1 is activated by the host system.

DATA TRANSFER SIGNALS

All lines associated with the transfer of data between the drive and the host system are differential in nature and may be multiplexed. These lines are provided at the J2/P2 connector on all drives.

Signal level are defined by RS-422A.

Two pairs of balanced lines are used for the transfer of data: MFM Write Data and MFM Read Data. Figure 3-10 illustrates the driver/receiver combination used with the drive for data transfer signals.

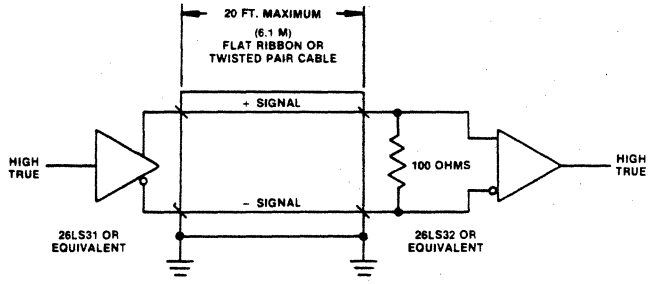


FIGURE 3-10
DATA TRANSFER LINE DRIVER RECEIVER

MFM WRITE DATA

This is a differential pair of lines that define the flux transition to be written on the track. The transition of the +MFM Write Data line going more positive than the −MFM Write Data line causes a flux reversal on the track if Write Gate is active. This signal must be driven to an inactive state, +MFM Write Data more negative than −MFM Write Data, by the host system when in a read mode.

The delay from the leading edge of Write Gate to the Write Data pulse is 400 nanoseconds, maximum.

Host controllers may implement write precompensation circuits that recognize worst case patterns and adjust the write data waveform. Although a value cannot be specified for write precompensation, Tandon suggests a value of 12 nanoseconds for systems using MFM double density recording format.

MFM READ DATA

The data recovered by reading a prerecorded track is transmitted to the host system via the differential pair of MFM Read Data lines. The transition of the +MFM Read Data line going more positive than the -MFM Read Data line represents a flux reversal on the track of the selected head.

3.6 DRIVE ADDRESS AND OPTION SELECTION

The drive address and option selection is determined by the programmable jumper blocks located on the logic circuit board. If jumper configurations are changed, power should be cycled off and on, so that the microprocessor can recognize the new configuration.

The option programming guide is contained in Table 3-3.

3.7 SHIPPING PACK AND HANDLING

Figures 3-11 through 3-13 provide basic information on recommended design guidelines for packaging systems.

From various drop tests conducted, it has been established that drives subjected to shock loads in excess of twenty G's may be damaged and consequently not meet published performance specifications for data reliability, margins, and function.

In order to avoid media or head damage, it is recommended that:

1. Drive mounting designs incorporate some type of shock dampening consideration.

2. Shipping cartons protect the drive within the system to withstand twenty G's.

3. Individual drives are handled carefully, e.g., receiving and in-process personnel are property trained, surface mats are used on working surfaces to prevent the possibility of "handling shock," and padding is placed on racks and carts.

Please emphasize the critical aspects of handling these drives to all concerned people. In addition, Tandon provides technical assistance on packing and handling to customers upon request.

TABLE 3-3
OPTION PROGRAMMING GUIDE

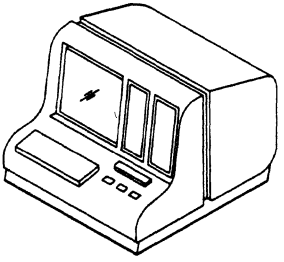
Option Jumper	Function	Factory Programmed, Not User Accessible	Usage
W1	Track Fault	O	Install for excess track fault.
W2	Test	O	Install for unit self-test.
W3	Disable Limit	O	Install to disable soft limits.
W4	Spin Select	O	Install for spin select.
W5	Tracks	O	Not used.
W13	Future Option	O	Install for backlash.
W14	Future Option	I	Install for no backlash.

Option Jumper	Function	Factory Programmed, User Accessible	Usage
W15	Drive Select	I	Omit W15 for drive-to-controller lines, enabled when drive not selected.
W16	Index	I	Omit W16 for index-to-controller line, enabled when drive not selected.
RTW7	Read Terminator	I	Install only at the end drive for daisy chain data. Install in all drives for radial data.
WTW8	Write Terminator	I	
S4W9	Drive Select 4	O	Install one of four plugs only. Plug corresponds to drive address.
3W10	Drive Select 3	O	
2W11	Drive Select 2	O	
1W12	Drive Select 1	I	
U23	Terminator Pack	I	Install at the end drive only for daisy chain control lines.

NOTES:

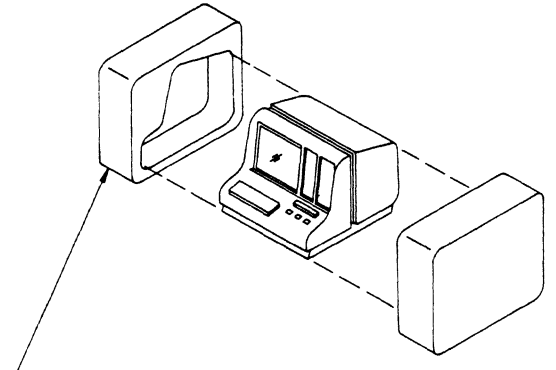
O = Omit
I = Install

STEP A.



ENCLOSE UNIT IN POLY BAG TO AVOID SURFACE SCRATCHES AND OTHER DAMAGE.

STEP B.



MOLD POLYURETHANE "CLAMSHELL" TO "CUBE" UNIT.

FIGURE 3-11
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 1

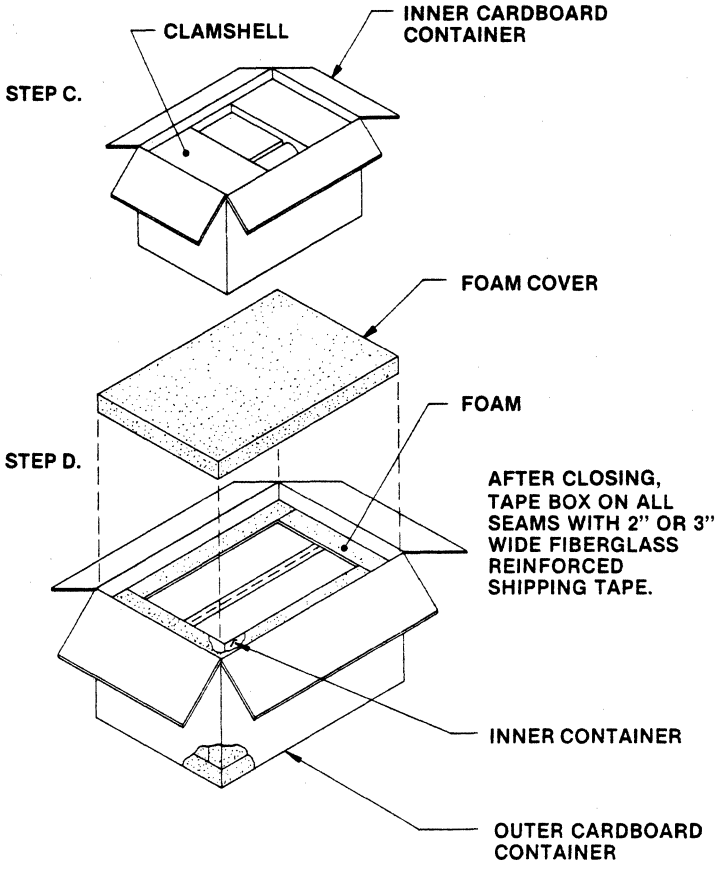


FIGURE 3-11 (CONTINUED)
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 1

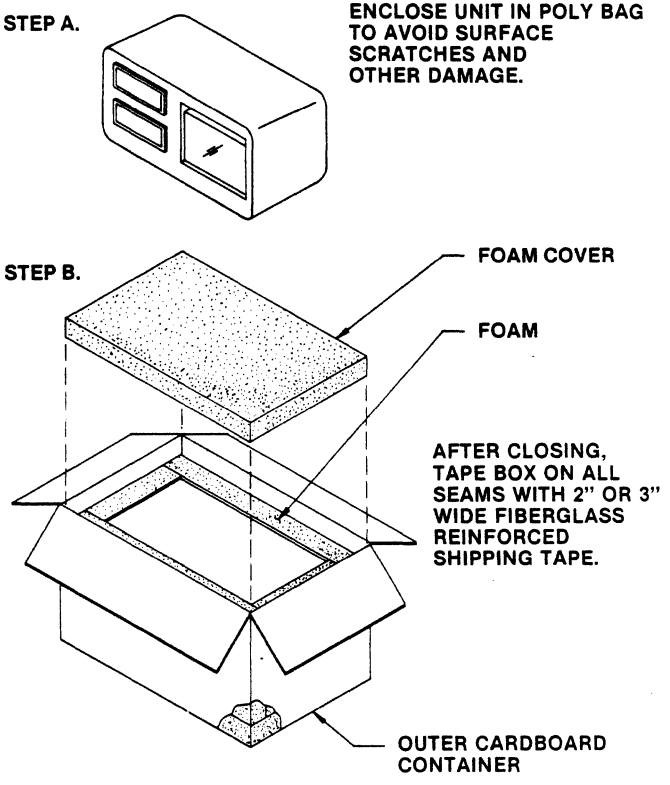
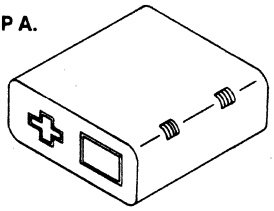


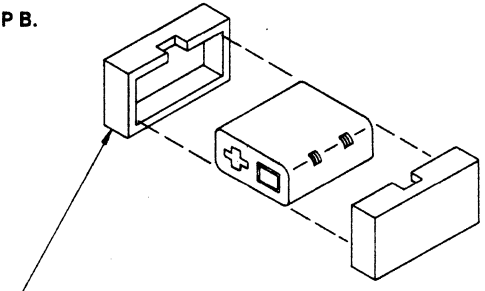
FIGURE 3-12
RECOMMENDED SHIPPING PACK DESIGN.
CONFIGURATION 2

STEP A.



ENCLOSE UNIT IN POLY BAG TO AVOID SURFACE SCRATCHES AND OTHER DAMAGE.

STEP B.



MOLD POLYURETHANE "CLAMSHELL" TO "CUBE" UNIT.

FIGURE 3-13
RECOMMENDED SHIPPING PACK DESIGN, CONFIGURATION 3

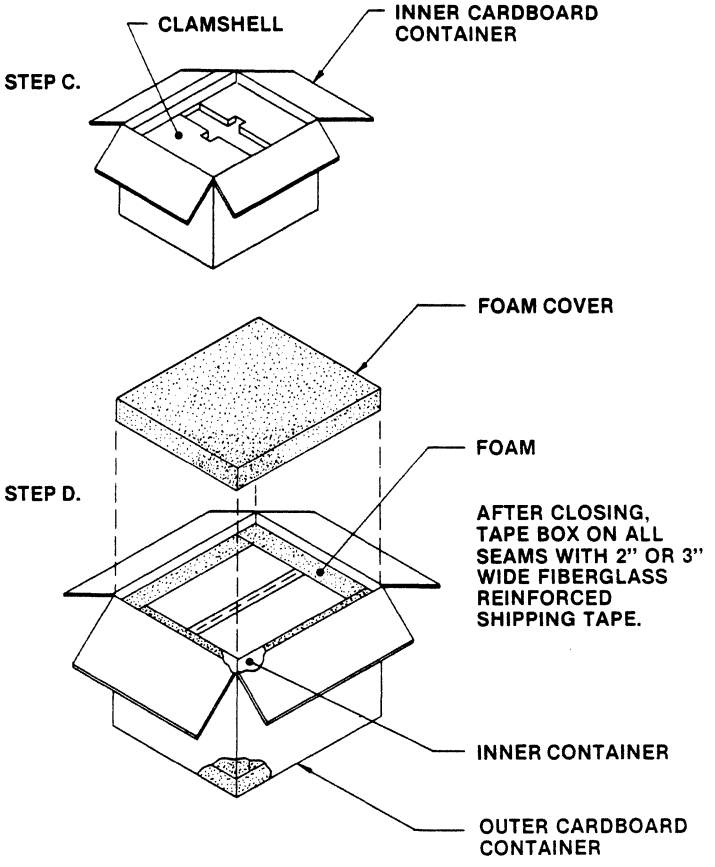
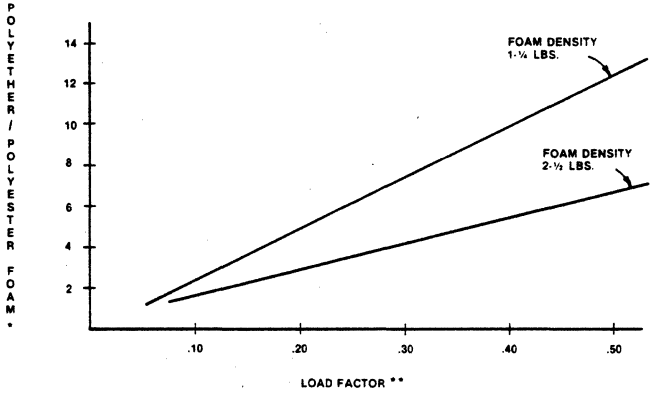


FIGURE 3-13 (CONTINUED)
RECOMMENDED SHIPPING PACK DESIGN,
CONFIGURATION 3



NOTES

THE GRAPH GIVES FOAM THICKNESSES TO SATISFY 10 G MINIMUM SHOCK LOADS ON STANDARD 30-INCH DROP TEST. HENCE, ALL PACKAGE DESIGNS SHOULD BE TESTED TO VERIFY THEIR ULTIMATE PERFORMANCE.

* THICKNESS IS IN INCHES.

** THE LOAD FACTOR IS IN LBS. PER SQ. INCH.
THE FORMULA IS: LOAD FACTOR = $\frac{\text{UNIT'S WEIGHT (LBS.)}}{\text{SMALLEST SIDE OF UNIT (SQ. INCHES)}}$

FIGURE 3-14
LOAD GRAPH

Tandon
CORPORATE OFFICES
20320 PRAIRIE STREET
CHATSWORTH, CA 91311

TEL. NO.: (213) 993-6644
TELEX NO.: 194794
TWX NO.: 910-494-1721

P/N 179050-001A (T5008A 5-83)

PRINTED IN U.S.A.

2732 EPROM. (Erasable programmable read-only memory). The 2732 EPROM contains the necessary information for the X-Bus master to boot from the hard disk drive.

6331-1 PROM. Programmable read-only memory. The 6331-1 PROM contains information that controls access to the RAM data buffer.

8253 programmable interval timer. The 8253 is a three-channel programmable counter/timer chip manufactured by Intel. Two 8253s are used in the Floppy/Hard Disk Module for interrupt control and DMA transfers. See the Intel Microprocessor and Peripheral Handbook.

Active X-Bus module. An active X-Bus module is a module that, having become the system bus master, can drive all commands and address signals of the X-Bus.

Buffer. A buffer is an amplifying signal driver, not necessarily with memory capability. Buffers that provide temporary storage for data are called "storage buffers."

Bus. A bus is a signal line or a set of lines used by an interface system to connect a number of devices and to transfer information. In general, three types of buses make up a bus set (which is also referred to as a bus): the address bus, the data bus, and the control bus. Also see X-Bus.

Bus cycle. A bus cycle is the process whereby digital signals effect the transfer of data bytes or words across the interface by means of an interlocked sequence of control signals. Interlocked denotes a fixed sequence of events in which one event must occur before the next event can occur.

Bus master. See Master.

Byte. A byte is a group of eight adjacent bits operated on as a unit. Also see High-order byte and Low-order byte.

Clock cycle. A clock cycle is a signal wave form used to achieve synchronization of the timing of switching circuits and memory.

Cluster configuration. A cluster is a hardware configuration in which cluster workstations are linked in a daisy chain to a master workstation.

Compatibility. Compatibility is the degree to which modules can be interconnected and used without modification.

Direct memory access logic. See DMA.

DMA. (Direct memory access) DMA allows a peripheral device to transfer data to or from memory without using the CPU via a DMA controller in the Processor Module.

DMA address. When the DMA channel is initialized for a transfer, the DMA address is the initial address in memory of the transfer. If the DMA address is read for status at any time, it is the current memory address of the transfer.

Driver. See Buffer.

Flip-flop. A flip-flop is a digital circuit that can be in either of two states, depending upon the input received and which state it was in when the input was received.

Handshake A handshake is a process whereby control signals are exchanged between the CPU and a device or devices.

High-order byte. The high-order byte is the most significant byte in a word (bits 8h to Fh). The high-order byte is also called the odd byte, since it always has an odd address in memory.

High state. The high state is the more positive voltage level used to represent one of two logical binary states (using positive logic).

Identification polling sequence. The identification polling sequence is a routine in the bootstrap ROM used to identify modules connected to the X-Bus.

Input/output pins. Input/output pins are the pins of a chip through which signals are input or output.

Interface. An interface is a shared boundary between two systems, or between parts of two systems, through which information is conveyed.

Interrupt logic. Interrupt logic interrupts the CPU so it can service an I/O or peripheral device.

Local address bus. A local address bus is an address bus that is local to the Floppy/Hard Disk Module.

Low-order byte. The low-order byte is the least significant byte in a word (bits Øh to 7h). The low-order byte is also called the even byte since is always has an even address in memory.

Low state. The low state is the more negative voltage level used to represent one of two binary states (using positive logic).

Manual reset. A manual reset is a system reset brought about when the user presses the reset button on the rear of the Processor Module. Also see Reset.

Master. In the master-slave concept, the master is a module that controls the data and address buses. The master acquires the bus (or X-Bus) through bus exchange logic, and then generates command signals, address signals, and memory or I/O addresses.

Master workstation. The master workstation runs applications and provides resources to individual cluster workstations.

MFM. See Modified frequency modulation.

Modified frequency modulation (MFM). MFM is an encoding scheme used in the Floppy/Hard Disk Module to store double-density data.

Motherboard. The motherboard interfaces to all boards and power supplies.

NMI. See Nonmaskable interrupt.

Nonmaskable interrupt (NMI). During the X-Bus module identification polling sequence, a nonmaskable interrupt signals a ready timeout to signify that no additional modules are connected to the X-Bus.

PAL. See Programmable array logic.

Passive X-Bus module. A passive X-Bus module is a module that cannot become the X-bus master because

it is not able to drive the bus command signals of the X-Bus.

Peripheral device. An electromechanical unit, such as a keyboard, CRT, disk drive, or printer that can be connected to the workstation.

Port. A port is an input/output address, usually containing (if a status port) or requiring (if a command port) specific data, such as the Floppy Disk Drive Command/Status register at port XXØØh (where XX signifies the module base I/O address). A port can allow access to several registers. See Register.

Power-up reset. A power-up reset is an automatic system reset occurring when the power is turned on. Also see Reset.

Programmable array logic (PAL). Two 16L8 PAL chips generate control signals for the floppy and hard disk drives.

RAM (Random access memory.) The RAM in the Floppy/Hard Disk Module is made up of four blocks of 2K by 8 bits (2K bytes) of static RAM, totaling 8K bytes.

RAM data buffer. See RAM.

Register. A register is a temporary memory location for data.

Reset. A reset can be either a system reset, as defined by the reset pin functions of the various chips connected to the system reset function, or a software register reset, equivalent to a clear. Also see Power-up reset and Manual reset.

Set. To set is to write a logical 1 or series of 1's to a register.

Signal. A signal is the physical representation of logic.

Signal level. The signal level is the relative magnitude of a signal when compared to an arbitrary reference.

Signal line. A signal line is one of a set of signal conductors in an interface system used to transfer messages among interconnected modules.

Signal parameters. Signal parameters are the element of an electrical quantity whose values or sequence of values convey information.

State sequencer. State sequencer circuitry in the Floppy/Hard Disk Module controls DMA transfer operations between the RAM data buffer and the X-Bus master.

Storage buffer. A storage buffer is a buffer with storage, such as a flip-flop, latch, or register.

System. A system is a set of interconnected elements that achieve a given objective through the performance of a specified function.

Tristate buffers. A tristate buffer is a buffer that has these logic output states: Ø, 1, and the high impedance state.

Wait state. A wait state is a temporary suspension of an I/O or memory cycle. It is used when an I/O or memory device operates at a speed slower than that of the CPU.

WD1Ø1Ø. The Western Digital WD1Ø1Ø Winchester disk controller controls hard disk drive circuitry. See the Western Digital Corp. WD1Ø1Ø Winchester Disk Controller data sheet.

WD2797-Ø2. The Western Digital WD2797-Ø2 floppy disk formatter/controller contains most of the circuitry necessary in the Floppy/Hard Disk Module to control the floppy disk drive. See the Western Digital Corp. WD279X-Ø2 Floppy Disk Formatter/Controller Family data sheet.

Word. A word is 16 bits or two bytes.

Workstation master. A workstation master is a master module within a workstation. Also, see Master.

X-Bus. X-Bus is a standard asynchronous system bus that allows for total configurability and interconnection of the workstation modules. The X-Bus supports two independent address spaces: memory and I/O. The X-Bus structure is built upon the master-slave concept, thereby allowing modules of different speeds to interface.

X-Bus master. Module that controls the X-Bus.

Floppy/Hard Disk Manual

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