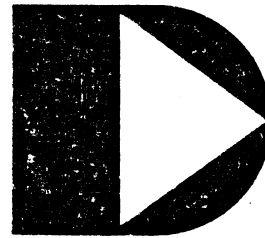


DATAPOINT 1800

FIRST LEVEL MAINTENANCE MANUAL

DATAPOINT CORPORATION



The leader in dispersed data processing™

Manual No. 75217-00

July, 1978

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SECTION I
EQUIPMENT DESCRIPTION

1.1 GENERAL

The Datapoint 1800 System is a stand alone processor/diskette system. The 1800 processor contains a CRT, removable keyboard, 8 bit control processor, 64K of memory (4K of ROM, 56K of user RAM, and 4K of system RAM); SDLC, BISYNC, GENSYNC, and ASYNC communication ports. Additional memory expansion modules of 32K may be added to a maximum of 124K of RAM memory. The 1800 keyboard is removable and can be located up to one meter from the processor unit. The 1800 processor has a 6600 compatible I/O bus. This can be used with standard Datapoint 6600 peripheral equipment that does not require power through the I/O bus.

The Datapoint 1800 System also includes the 1842 Dual Diskette Drive. The 1800 processor controls the diskette drive through a specialized bus called a "micro bus". The diskette drive can be operated (under program control) in either single density or double density recording mode, and can be used to make density conversions between the two modes. Storage capacity for the diskette drive is either 0.5 megabyte or 1.0 megabyte depending on the recording density. Up to four drives may be connected to the 1800 processor for a maximum on-line storage capacity of four megabytes.

The standard nominal primary power is 115 VAC, 60 Hz. Power input circuits are field changeable for operation with primary power of 88 to 264 VAC at frequencies of 50 or 60 Hz.

NOTE

This manual covers only the 1800 processor. For information on the 1842 Dual Diskette Drive, refer to First Level Maintenance Manual No. 75218.

1.2 EQUIPMENT SUPPLIED

The Datapoint 1800 Processor is shipped with the 1800 System with one each of the following equipment:

- a. 1800 Processor.
- b. 1842 Dual Diskette Drive.
- c. Micro Bus I/O Cable.
- d. Micro Bus Terminator.

Table 1-1 shows the equipment supplied by model and part number. Table 1-1 is for general information only. Current shipping lists take precedence in specifying the equipment supplied.

TABLE 1-1

EQUIPMENT SUPPLIED		
<u>MODEL NUMBER</u>	<u>DESCRIPTION</u>	<u>PART NUMBER</u>
1800	Processor with Keyboard	11-0522-001
1821	Processor, 32K Memory	10-1402-001
1822	Processor, 64K Memory	-003
1823	Processor, 96K Memory	-004
1824	Processor, 124K Memory	— -005
1842	Dual Diskette Drive	11-0525-001
	Micro bus I/O Cable	10-1147-XXX
	Cable, 7 in. (used with extension drive)	-001
	Cable, 36 in.	-002
	Micro bus Terminator	10-1145-001

1.3 PHYSICAL DESCRIPTION

The 1800 Processor (Figures 1-1 and 1-2) consists of two major assemblies: the processor itself and the keyboard. The keyboard can be attached to the processor or located up to one meter away from the processor. The processor and keyboard are modular in design and are each enclosed in a molded, top removable housing. Electronic components and circuitry are on printed wiring boards. Equipment specifications for the 1800 processor is given in Table 1-2.

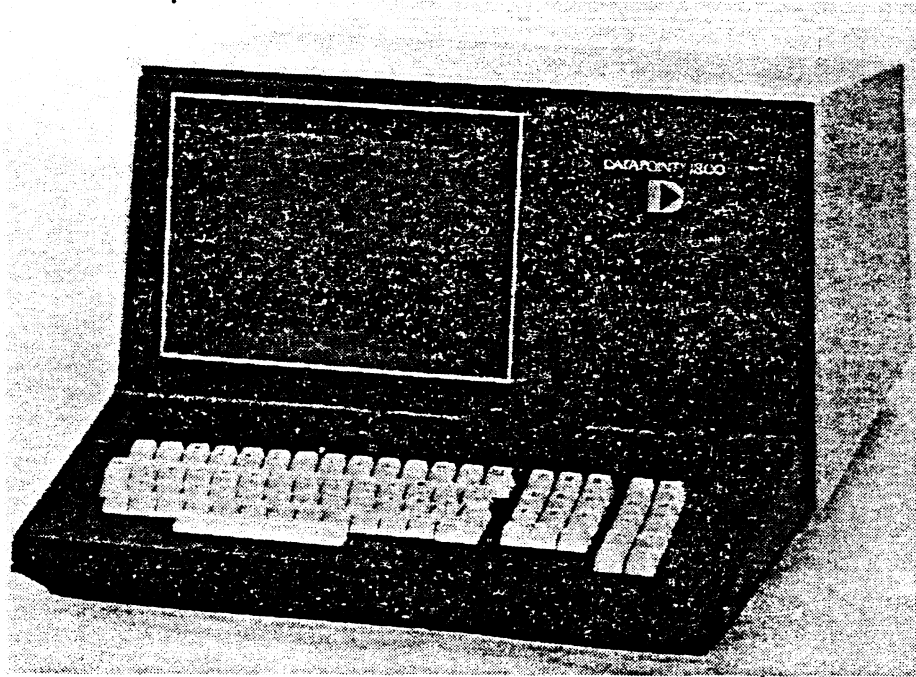


Figure 1-1. 1800 Processor - Keyboard Attached

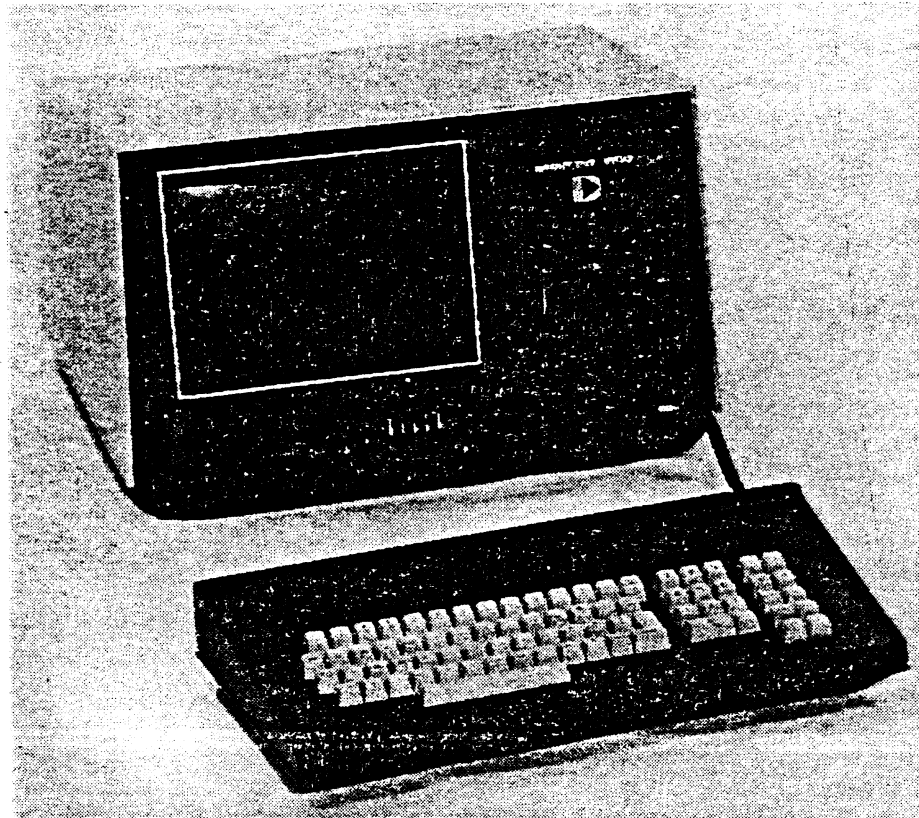


Figure 1-2. 1800 Processor - Keyboard Detached

TABLE 1-2

EQUIPMENT SPECIFICATIONS FOR
1800 PROCESSOR

DIMENSIONS

Width	52.0 cm	20.0 in.
Height	31.5 cm	12.4 in.
Depth	58.0 cm	22.7 in.
Weight	24.5 kg	54.0 lbs.

POWER

Input (nominal)	115/230 VAC, 50/60 $\pm$ 1 Hz
Optional Input (jumper selected)	88 thru 132 VAC 174 thru 264 VAC
Consumption	150 watts

ENVIRONMENT

Temperature	10 to 38 degrees C 50 to 100 degrees F
Humidity	20 to 90 percent non-condensing

CHARACTERISTICS

Display Size	5.5 X 8.4 inches
Active Display Size	5 X 7.9 inches
Characters per line	80
Number of Lines	24
Characters Displayable	1920
Intensity	Adjustable
Brightness	35 ft. lamberts
Contrast Ratio	12:1
CRT Phosphor	P31
Character Size	0.071 X 0.146 inches
Deflection Type	Magnetic
Deflection Method	Raster Scan
Character Code	ASCII
Type of Memories	MOS RAM and ROM
Memory Size (ROM)	8192 words
Memory Size (user, RAM)	Up to 124K words in four 32K word steps
Display Refresh Rate	60/50 frames/sec (power line frequency)

TABLE 1-2 (Cont)

Character Set	128 characters (Loadable)
Character Format	5 X 7 dot matrix
Cursor	Non-Destructive Blinking
Spot Diameter	0.01 inch
Repeatability	0.01 inch
Screen Refresh Memory	Processor RAM memory thru DMA
Video Capability	Normal, Inverse, Blinking
Word/Byte Length	8 bits

<u>SERIAL COMM MODULE</u>	
Modes	SDLC, BISYNC, GENSYNC, ASYNC
Data Clock	Internal or External
Data Rates (internal clock)	300, 600, 1200, 2400, 4800, 9600 Baud
Data Rates (external clock)	Up to 9600 Baud
Word Length	8 bits
Order of Bit Transmission	First: A0, LAST: A7
Error Detection	Automatic CRC generation and checking
CRC Polynomial	$X^{16} + X^{12} + X^5 + 1$
Frame Character	01111110 (Octal 176)
NRZ/NRZI	Jumper Selected

1.4 FUNCTIONAL DESCRIPTION

1.4.1 FUNCTIONAL COMPONENTS

Functional items or circuits of major importance in the processor are as follows:

- a. Keyboard, keyboard PWA, and direct buffer PWA.
- b. Display assembly including CRT, deflection raster scan PWA, and flyback transformer.
- c. Logic circuits on Processor-Emulation and Display-I/O PWA's including the 1800 control processor, emulation logic (to build 6600 instructions for 6600 I/O, display logic, 6600 I/O logic, 1800 micro bus logic, and serial communications logic.

d. Main memory including up to four 32K RAM PWA's and one 8K ROM PWA.

e. Power Supply.

1.4.1.1 CONTROLS AND INDICATORS

The only operator control, other than the keyboard, is the power ON-OFF switch located on the right side of the base plate.

There are two indicators on the 1800 processor. The first, an indicator on the RH end of the keyboard, is powered by +5VDC from the power supply and if lit, indicates that the power supply is on. The second indicator is a LED and is located at the right end of connector J7 on the display-I/O board. It indicates that fuse F1 is blown. Fuse F1 is a two ampere fuse in the +5 volt power line of the 6600 I/O bus. For the LED to light, the fuse must be blown. Fuse F1 is located at the rear of connector J5 on the display-I/O board.

There are four LED indicators on the Power Supply Control Board. They are termed LV, OV, IL, and CB for Low Voltage, Overvoltage, Current Limit, and Crowbar. The LV LED indicates that the power supply was shut off because the AC line voltage fell below either 90VAC RMS or 180VAC RMS. The OV LED indicates that the power supply was shut off because the AC line voltage rose above either 140VAC RMS or 280VAC RMS. The IL LED indicates that the power supply was shut off because of a continuous overload or short circuit condition on any output. The CB LED indicates that the power supply was shut off because the +5VDC output voltage exceeded the safe voltage limit for the logic circuits (+7 VDC maximum).

1.4.2 PROCESSOR FUNCTION

The control processor forms the central hub of the 1800 unit with all data transfers occurring through the control processor. The control processor communicates to the other modules that comprise an 1800 unit through high speed input and output ports. In addition to its task of supporting the keyboard, display, serial communications and 6600 I/O modules, the control processor also emulates the 6600 USER MODE instructions.

The memory module contains random access memory (RAM) for program and data storage and read only memory (ROM) for system functions such as initialization, keyboard, display, and communications subroutines.

The keyboard module provides one of the two operator interfaces of an 1800 unit. The control processor performs key scanning and code conversion. The keyboard only provides data to the control processor and all keyboard transfers must pass through the control processor. The control processor then provides the interface to the user level program in the form of status and keyboard data bytes in memory. The keyboard has ten function keys available for program use. The keyboard is detachable and can be located up to one meter from the processor.

The display module is the other operator interface in an 1800 unit. The display is controlled by the control processor and is refreshed from the processor memory. The display module has a loadable character set and provides for inverted video on a character by character basis under processor control. The control processor provides "pointers" to the beginning of each line as the display requires them and a DMA channel transfers the information from the processor memory to a line buffer. This transfer operation also performs memory refresh for dynamic memories.

The serial communications module provides the serial communications channel of an 1800 using the SDLC, BISYNC, GENSYNC, or ASYNC disciplines. The module contains a minimum of components due to the control processor performing all data operations down to the bit level. The maximum rate of the communications module is 9600 baud and is selected by jumpers. The communications module is not restricted to the modes provided but can be reprogrammed with new firmware to allow any discipline.

To allow the 1800 unit to interface with other Datapoint peripherals, a 6600 type parallel I/O interface module is provided. This module is controlled by the control processor and allows the 1800 unit to interface with standard Datapoint peripherals (printers, etc.). The 6600 interface module provides the normal "A bus" functions and generates the external commands used in the standard Datapoint Processor line. The 6600 I/O bus does not provide operating power for peripherals. Standard 6600 I/O parity checking is used.

The address register is used to assign a unique address to each 1800 unit in a system for identification purposes. This address is determined by a set of eight DIP switches located inside the 1800 unit. The address set by the switches is then read in by the control processor through an input port and made available to the system program.

1.4.2.1 KEYBOARD

The detachable keyboard has 76 key positions including a basic 55 key alphanumeric group, an eleven key numeric group, and a ten key system control group (functional keys). The keyboard uses a capacitively coupled key closure to initiate the generation of character codes. Character generation occurs only with the downward movement of the key. The multi-key rollover ensures that a character is encoded only once and does not prevent other keys from being encoded. Transfer of characters from the keyboard is under processor control. Characters are generated in ASCII code. The character code resides in the ROM memory which allows for special code sets. The ten function keys are on the right side of the keyboard. Five of the function keys are reserved for the functions INTERRUPT, RESTART, ATTENTION, KEYBOARD, and DISPLAY. To protect against accidental restarts it is necessary to depress both the RESTART and INTERRUPT keys to cause a restart. The order of depression is not significant as the restart occurs when either key is released.

1.4.2.1.1 KEYBOARD CONTROL PROCESSOR INTERFACE

The control processor communicates to the keyboard module through several control/status bytes in system RAM. The control/status bytes are:

<u>Location</u>	<u>Description</u>
0167550	KBS2
0167551	KBS1
0167552	Keyboard data
0167553	Frame Counter

- a. KBS1 - KBS1 is one of the keyboard status bytes. This byte contains status information about the function switches on the keyboard. When a key is depressed the corresponding status bit is a one. The function keys will also provide a read ready and a key code to allow them to be used as coded control keys.

Bit Definitions:

- 0 - Display key
- 1 - Keyboard key
- 2 - Keyboard Char ready
- 3 - Reserved (0)
- 4 - Reserved (0)
- 5 - Reserved (0)
- 6 - Reserved (0)
- 7 - Reserved (0)

- b. KBS2 - The second keyboard status byte indicates the condition of keyboard switches F1 through F5. The corresponding status bit will be a one when the switch is depressed and will remain a one until the switch is released.

Bit Definitions:

- 0 - F5
- 1 - F4
- 2 - F3
- 3 - F2
- 4 - F1
- 5 - Restart key
- 6 - Attention key
- 7 - Interrupt key

- c. Keyboard Data - This byte carries the keyboard data from the keyboard to the control processor.
- d. Frame Counter - The frame counter is incremented once at the end of each frame (50 or 60 Hz) and is used for timing the cursor blink rate.

1.4.2.1.2 KEYBOARD CONTROL PROCESSOR INTERFACE OPERATION

The keyboard KEYSTROBE signal is sent to the control processor input port. This allows the control processor to determine how long a key is held down. This is necessary to emulate the function of the keyboard and display keys. The control processor provides the scanning signals by loading an output port (Figure 1-3) and observes the condition of KEY STROBE and STROBE. When the control processor detects a STROBE it indicates that a new key closure has been detected and the control processor will read in the key code on the keyboard input port. For function keys the control processor will detect the KEY STROBE signal and by knowing the scan code that was loaded it can determine which key is depressed. The control processor will then load the appropriate bit in the keyboard status byte.

The keyboard is interfaced to the control processor through logic that generates the necessary timing signals to allow the keyboard to function.

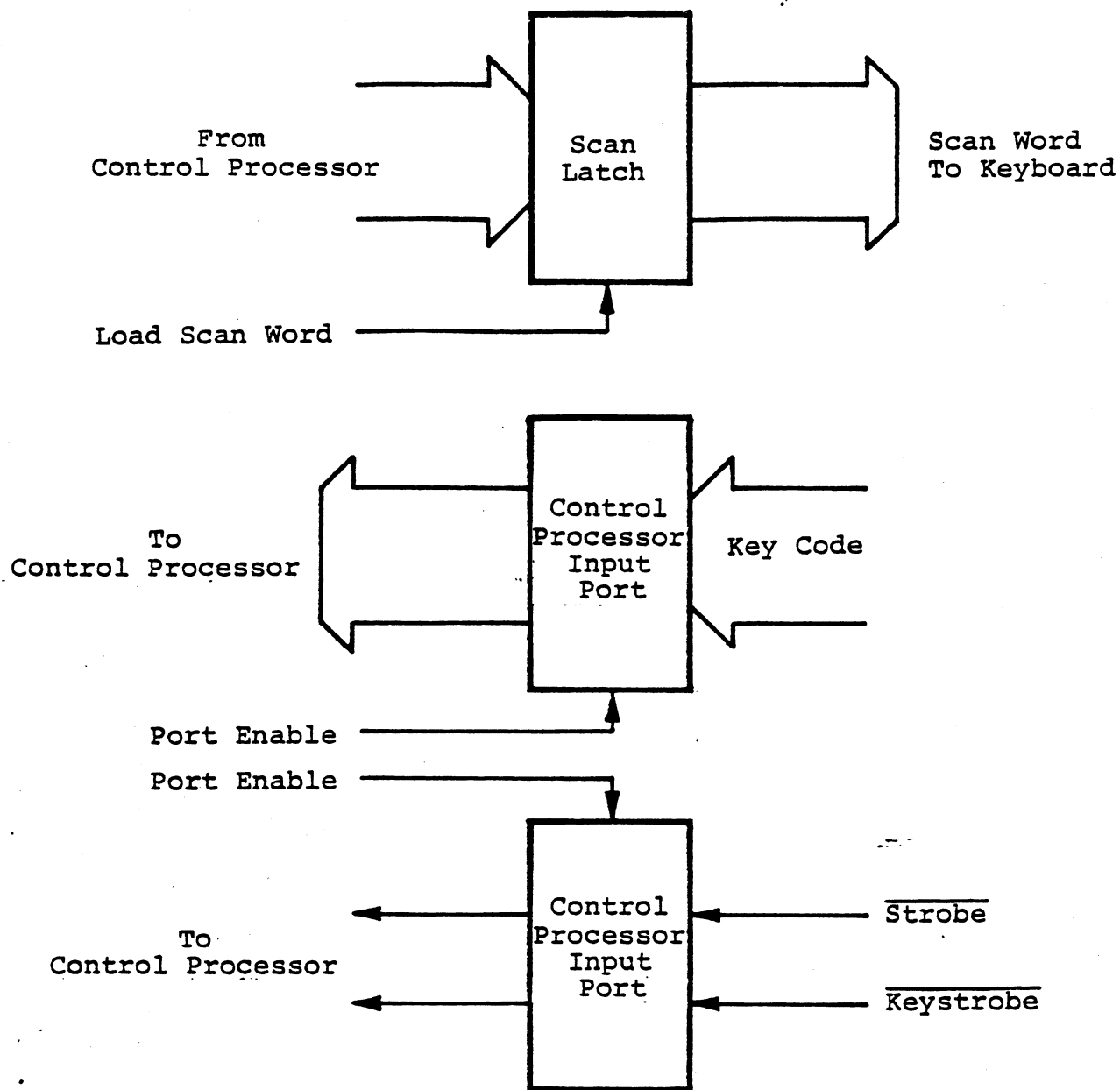


Figure 1-3. 1800 Keyboard Control Processor Interface

1.4.2.2 DISPLAY

The 1800 display is a magnetically deflected raster scan CRT display. It provides for the display of 1920 characters organized in 24 lines of 80 characters each. The display is refreshed (at 60/50 frames per second, power line synchronized) from the processor memory through a DMA channel under control processor control. The display character generator is loadable allowing any character set desired to be displayed without special ROM tooling. The display also incorporates an inverse video feature that allows characters to be displayed as dark dots on a light background on a character by character basis (Figure 1-4). This function is under program control.

1.4.2.2.1 DISPLAY CONTROL PROCESSOR INTERFACE

The control processor communicates to the display by providing a list of pointers to the data it desires to display on the screen. The list of screen pointers is stored in memory in locations 0167554 through 0167637 and are defined as follows:

<u>Location</u>	<u>Definition</u>
0167554,55	Top Null Line
0167556,57	Display Line 0
0167560,61	Display Line 1
0167562-633	Display Lines 2-22
0167634,35	Display Line 23
0167636,37	Bottom Null Line

These locations all contain two byte pointers to the first character in memory to be displayed in the first position of the respective line. The contents of the following 79 locations in memory will be displayed as the rest of each line. The pointers must specify memory locations that have existing physical memory (the display pointers are sector and based) and the display pointer should not cause the display DMA to cross a sector boundary.

The character set is loaded by the LDCF (LOAD CHARACTER FONT) instruction that is new for the 1800 processor. This instruction allows the character font for each ASCII code to be loaded from memory.

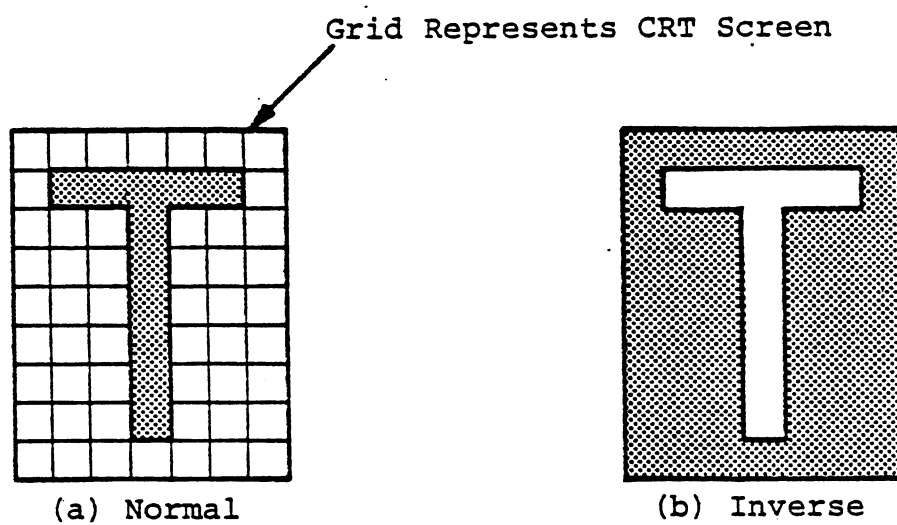


Figure 1-4. 1800 Processor Inverse Video Presentation

The inverse video feature is controlled by the MSB of each character to be displayed. If the MSB of the character as read out of memory by the DMA is a zero, the character is displayed normally. If the MSB is a one the character is displayed as dark dots against a light background.

The blinking cursor is implemented by using an unused character code to form a solid character, then blinking the solid character at the cursor position at the cursor blink rate.

1.4.2.2.2 DISPLAY CONTROL PROCESSOR INTERFACE OPERATION

The interface to the deflection system is through the standard Molex connectors for both signals and power.

The 1800 unit obtains its display data from the processor memory through a DMA channel. Each time a new line is required for the display (every 10 scans) a new line flag is sent to the control processor. When the control processor recognizes this flag it loads the display line starting address latch with the address of the data in the processor main memory it wishes to display on the next line. This address is routed through the sector table and then loaded into the DMA counter. The DMA logic then cycle steals memory during the retrace intervals (approximately 11 microseconds) and loads up the next line of data into half of the line buffer until 128 (only 80 are used) characters have been loaded (128 reads are performed to allow for refreshing 32K RAMS). The line buffer is organized as two buffers of 80 characters each, one for the line currently being displayed and one for the next line being loaded. At the completion of each frame the display logic sets a bottom line flag to the processor to indicate the next line loaded will be the bottom line (scanning is left to right, bottom to top). This is required to allow the control processor to maintain frame sync.

The inverse video function is obtained by selectively complementing the video information to the video amplifier. The most significant bit of each character is used to indicate the video polarity, a zero for normal and a one for inverted video.

When the character set is loaded, the display is stopped during the loading of the character font RAM. This allows circuitry that is used for the display to serve "double duty" and perform some of the loading functions. Simplified and detailed block diagrams of the display logic on the display-I/O board are shown in Figures 1-5 and 1-6.

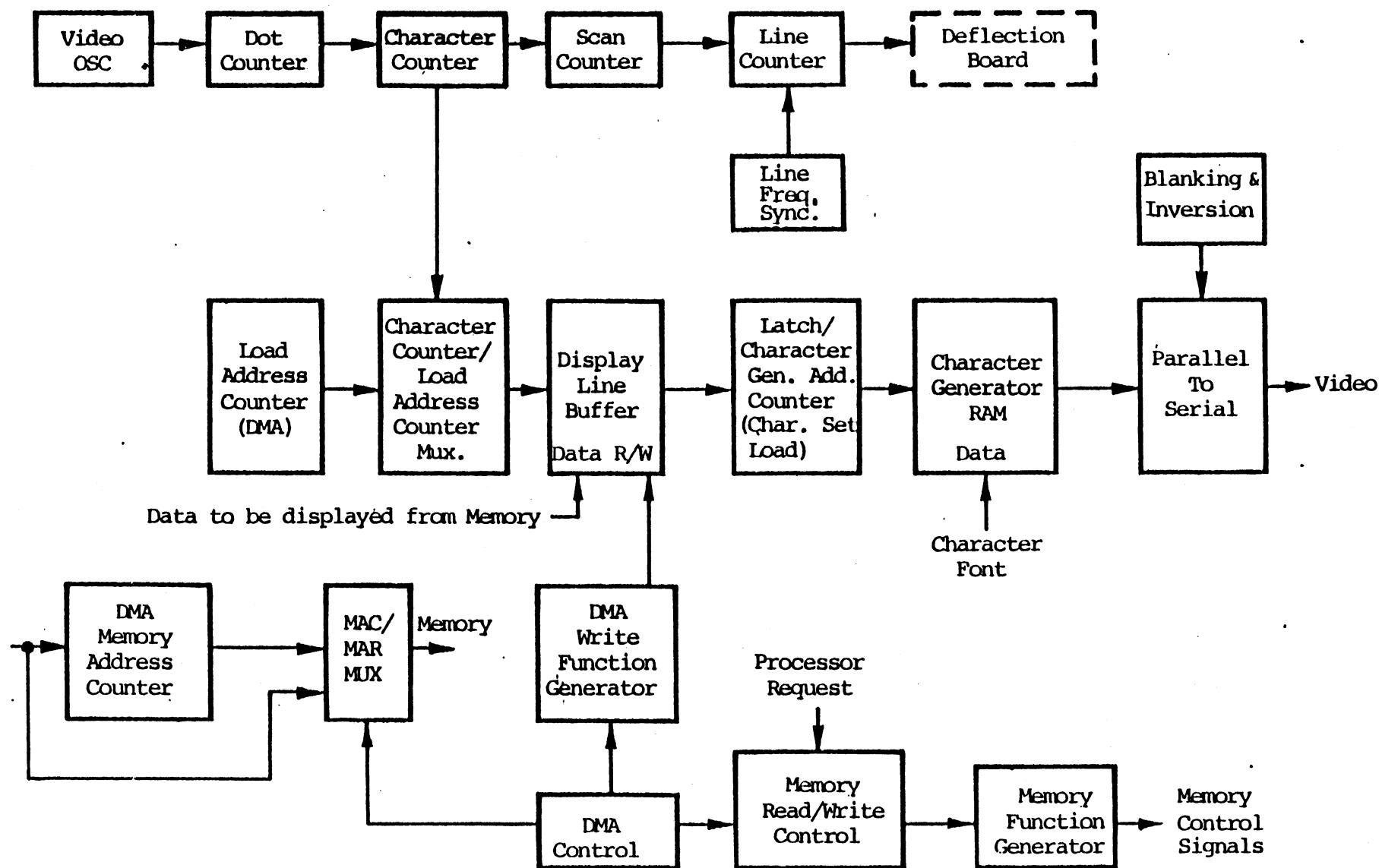


Figure 1-5. 1800 Processor Display Logic (Display-I/O Board)

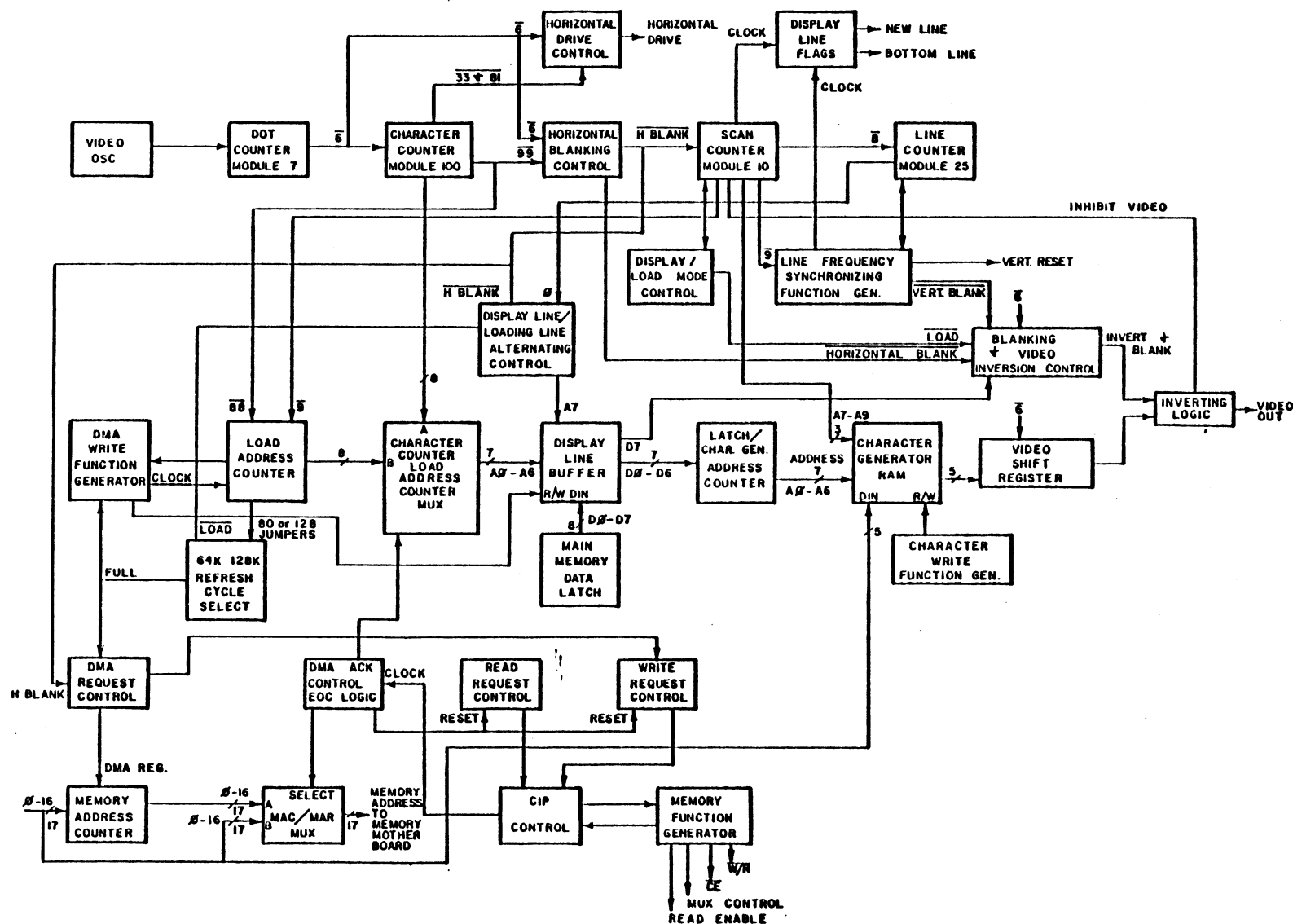


Figure 1-6. 1800 Processor Display (Display-I/O Board)

1.4.2.2.3 DEFLECTION RASTER SCAN

The deflection raster scan board contains the circuits necessary to process all signals required by the CRT. The horizontal circuit in conjunction with the flyback transformer, generates horizontal scan for the CRT raster, and produces 12,000 volts for the CRT anode. The horizontal circuit also provides adjustments for horizontal linearity and width of the CRT raster, and adjustments for focus and brightness of the CRT itself. The vertical circuit generates and provides for size adjustment of the vertical scan for the CRT raster. The deflection raster scan board contains an amplifier to process the video signal to the CRT, and a feed-through for filament voltage to the CRT. The horizontal drive, vertical reset, and video signals all come from the display I/O board. Figure 1-7 shows a block diagram of the deflection raster scan board. The flyback transformer shown in the figure is not mounted on the board.

1.4.2.3 SERIAL COMMUNICATIONS MODULE

The serial communications module is self contained within the 1800 processor and allows for communication under SDLC, BISYNC, GENSYNC, and ASYNC disciplines. The module is fully buffered with a 128 character buffer on transmit and receive and can operate full duplex with internal or external clock up to 9600 baud. The module provides for automatic testing of clear to send. The error checking division is provided on both transmit and receive when needed and on transmit the bytes are automatically inserted in the data block. The communications module performs bit assembly on the incoming serial data stream allowing it to operate with any discipline by changing the microcode.

The module also provides for control of an ACU unit for dialing. Serial interface bus pin assignments are given in Table 1-3.

1.4.2.3.1 SERIAL COMMUNICATIONS MODULE CONTROL PROCESSOR INTERFACE

The macro-program communicates to the communications module through status and control bytes located in system ram, and special communication instructions. A complete description of the status and control bytes and communications instructions are given in the 1800 Processor Reference Manual.

1-17

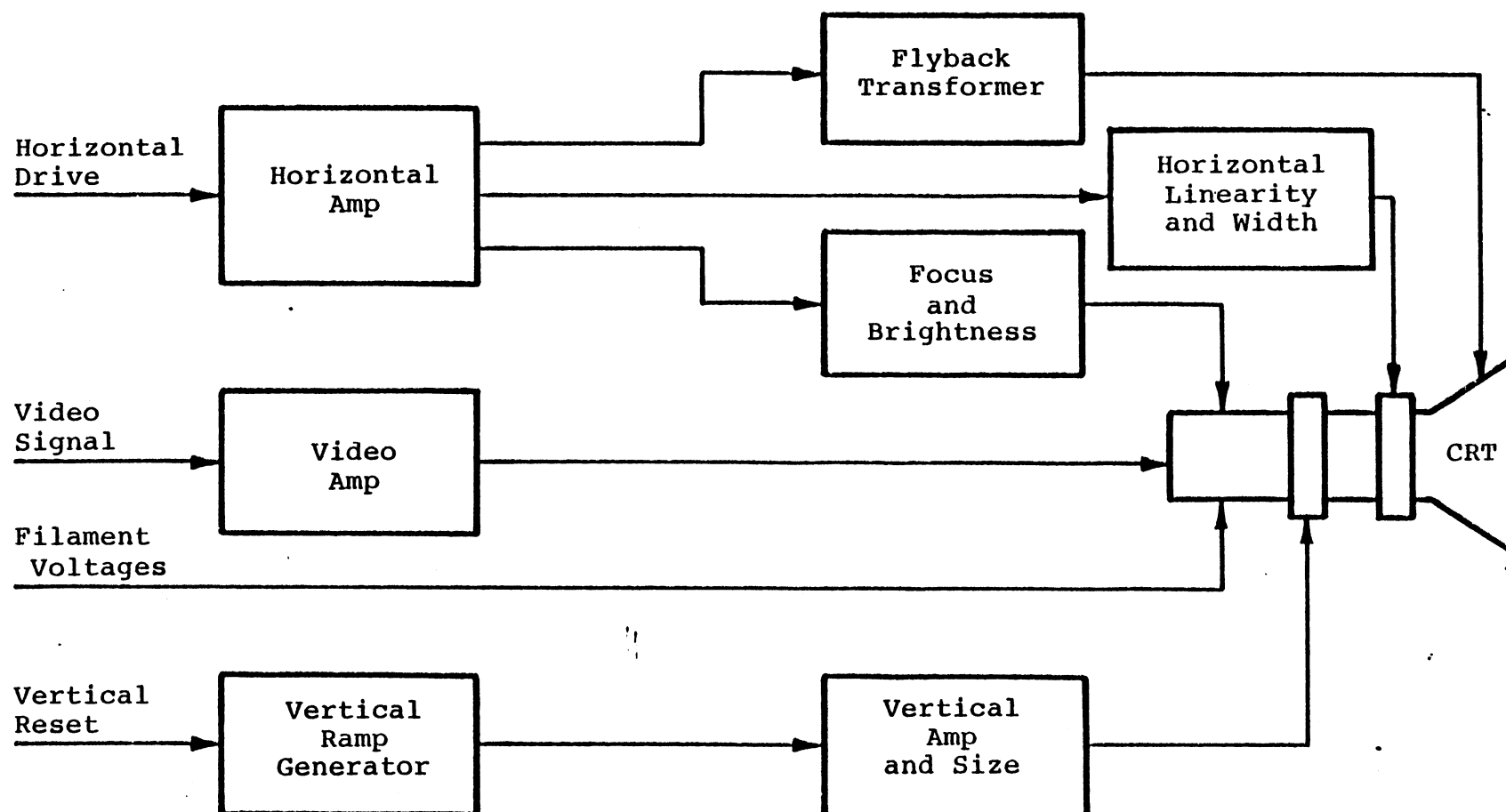


Figure 1-7. Deflection Raster Scan Board (A4)

TABLE 1-3

SERIAL INTERFACE BUS PIN ASSIGNMENTS

EIA CKT DESCRIPTION		SOFTWARE	PIN
AA	PROTECTIVE GROUND		1,37
AB	SIGNAL GROUND		7,27,33,36
BA	TRANSMITTED DATA		2
BB	RECEIVED DATA		3
CA	REQUEST TO SEND	SIMODOUT BIT 0	4
CB	CLEAR TO SEND	SIMODIN BIT 3	5
CC	DATA SET READY	SIMODOUT BIT 4	6
CD	DATA TERMINAL READY	SIMODIN BIT 1	20
CE	RING INDICATOR	SIMODIN BIT 6	22
CF	RECEIVED LINE SIGNAL DETECTOR	SIMODIN BIT 5	8
CG **	SIGNAL QUALITY DETECTOR	SIACUIN BIT 3	21
CH/CI	RATE SELECT/NEW SYNC	SIMODOUT BIT 4	23
DA	TRANSMIT CLOCK FROM DTE		24
DB	TRANSMIT CLOCK FROM DCE		15
DD	RECEIVE CLOCK TO DTE		17
CRO *	CALL REQUEST	SIACUOUT BIT 5	19
PWI	ACU POWER INDICATION	SIACUIN BIT 7	28
DLO	DATA LINE OCCUPIED	SIACUIN BIT 1	13
COS	CALL ORIGATION STATUS	SIACUIN BIT 2	16
ACR *	ABANDON CALL AND RETRY	SIACUIN BIT 7	11
NB1 *	DIGIT 1	SIACUOUT BIT 0	29
NB2 *	DIGIT 2	SIACUOUT BIT 1	30
NB4 *	DIGIT 4	SIACUOUT BIT 2	31
NB8 *	DIGIT 8	SIACUOUT BIT 3	32
PND *	PRESENT NEXT DIGIT	SIACUIN BIT 0	12
DPR *	DIGIT PRESENT	SIACUOUT BIT 4	14
SBA **	SECONDARY TRANSMITTED DATA	SIACUOUT BIT 4	14
SBB **	SECONDARY RECEIVED DATA	SIACUIN BIT 2	16
SCA **	SECONDARY REQUEST TO SEND	SIACUOUT BIT 5	19
SCB **	SECONDARY CLEAR TO SEND	SIACUIN BIT 1	13
SCF **	SECONDARY RECEIVED LINE SIGNAL DETECTOR	SIACUIN BIT 3	12
	INTERNAL RECEIVE CLOCK GENERATOR		34
	INTERNAL TRANSMIT CLOCK GENERATOR		35

* ACU USAGE

** SUPPLEMENTARY MODEM USAGE

1.4.2.3.2 SERIAL COMMUNICATIONS MODULE CONTROL PROCESSOR INTERFACE OPERATION

The communications module takes full advantage of the control capabilities of the control processor. The module itself consists of the rate generator, data receivers and drivers, modem control drivers and receivers, and the interface to the control processor. The control processor does the bit assembly, CRC generation and checking, parallel to serial conversion, zero deletion (SDLC) and insertion, control character detection, and buffer control.

The receiver section contains a rate generator that provides bit rate clocks for data sampling and also provides bit resync. The data sampler sets a flag to the control processor for each sample to indicate a bit is available. The control processor then inputs the data bit through an input port and operates on it and successive bits to accumulate data bytes to load into the receive buffer.

The transmit section contains an identical rate generator that sets a flag each bit time. When the control processor recognizes this flag it loads a single data bit into the output buffer. This bit then goes through a "clean up" flip-flop to eliminate jitter. The control processor repeats this eight times for each character and then reads another byte from the transmit buffer if one is available and the process repeats until the buffer is empty.

The modem control section consists of a four bit latch that the control processor loads with the data word that it reads from the MODCTL byte in memory. This latch then connects to a group of drivers that connect to the external modem.

The control lines from the modem (clear to send etc.) go through line receivers and then appear at input ports to the control processor. The control processor can then read in the modem status on these lines under macro-instruction control.

1.4.2.4 CONTROL PROCESSOR

The central part of the 1800 processor is the control processor logic on the processor-emulation board. All processor data transfers pass through the control processor. The processor supports and communicates to the other 1800 modules through high speed input and output ports. In addition to supporting the keyboard, display, serial communications module, and I/O bus, the processor emulates the 6600 USER MODE instructions. It performs this emulation by "building" complex 6600 instructions from many simpler control processor instructions.

1.4.2.4.1 MACRO INSTRUCTION SET

The macro level processor executes all the USER MODE instructions from the Datapoint 6600 plus the normal I/O instructions (except to keyboard, CRT, and tape deck). The instruction set for the 1800 processor is presented in the 1800 Reference Manual.

In the 1800 there is a significant increase in the quantity of user information (registers, stack, etc.) that is stored in system RAM. To make dealing with this information in system RAM easier there have been several instructions created that allow moving this data around or from registers to memory and back. Some of these are simply modified 6600 instructions (such as Betal) and some are new (System Move). The new instructions that have been implemented in the 1800 are presented in the 1800 Reference Manual.

1.4.2.4.2 MACRO LEVEL INTERRUPTS

Certain fault conditions in the hardware and other software operations will cause interrupts to occur. These interrupts cause calls to the interrupt vectors located in system RAM. The interrupt vectors consist of jump pairs that can be overstored by the user program to change the action taken in response to the interrupt.

The interrupt vector locations are:

0167400	Memory Parity Fault
0167406	Input parity error
0167414	Output parity error
0167422	Write violation
0167430	Access violation
0167436	Instruction violation
0167444	One millisecond
0167452	System call
0167460	Break Point
0167466	Unimplemented instr.
0167474	Sector Table Parity
	Special Vector Entries
0167502	Wait called by disk drivers
0167505	Wait called by display drivers
0167510	Beep Audio Channel Entry
0167516	Click Audio Channel Entry
0167524-36	Reserved

There is also a fail-safe interrupt that causes the equivalent of a power on reset to the processor if macro instruction execution is stopped for more than 30 ms. This is to prevent the machine from "hanging" if macro execution stops because of an external transient or temporary malfunction. This fail-safe also sets a status bit to the processor to differentiate it from a normal power on reset.

1.4.2.4.3 CONTROL PROCESSOR ORGANIZATION

The 1800 processor uses a fast control processor to perform control of CRT, Keyboard, communications module, and emulate the macro processor. Figure 1-8 shows a simplified block diagram of the control processor. Some of the characteristics of this control processor are:

- a. High speed - 100 nanosecond macro instruction rates.
- b. Pipelined instruction execution.
- c. 4K micro program addressing space.
- d. 16 bit Micro Instruction word.
- e. 8 bit data word.
- f. 32 general purpose registers + temporary register.
- g. 6 arithmetic/logical operations and increment operations.
- h. Conditional branching.
- i. Subroutine capability.

The micro program is stored in the 4K 16 bit words of ROM. This contains the emulation micro program and the micro program necessary to perform the basic levels of control for the screen, keyboard, SDLC and I/O modules. The speed of this ROM determines the maximum speed of the control processor, therefore the ROM must have an access time of less than 80 nanoseconds. The individual ROM chips are 4K ROMS organized 512 X 8. These ROMS have interchangeable PROM equivalents.

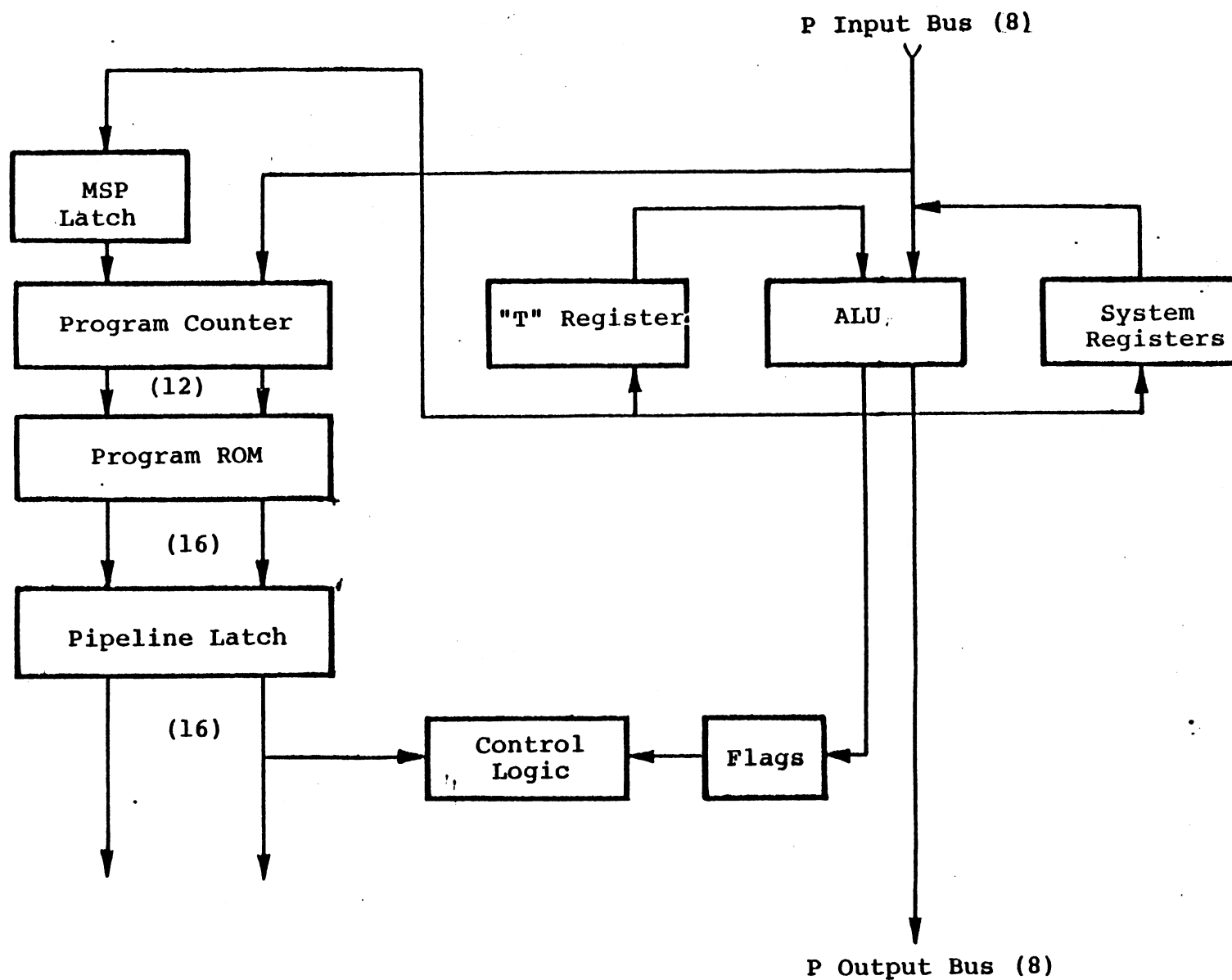


Figure 1-8. Control Processor Block Diagram

-In order to emulate the Datapoint 6600 USER MODE instruction set at a reasonable speed, a number of data storage/operator units are provided for the control processor as input and output ports (Figure 1-9). These emulation aids serve to enhance the speed of emulation by performing special functions or preventing the control processor from requiring reads from slower RAM memory when frequently used information is needed for a macro instruction.

The Emulation Support logic consists of:

- a. 8 User Registers.
- b. 8 System Registers.
- c. 4 User Flags.
- d. Memory Address Register.
- e. Base Register and Adder.
- f. Sector Table.
- g. Implicit Register.
- h. I Register.
- i. I-Decode ROMS.

Detailed block diagrams of the processor-emulation circuitry are shown in Figures 1-10 and 1-11.

1.4.2.5 MEMORY

The 1800 can address up to 128K bytes of addressable memory. This memory is organized in 9 bit words (8 data + parity) and is composed of N channel MOS random access memory and MOS ROM. Due to the dynamic nature of the RAM used it is necessary to periodically "refresh" the data in memory. This is performed automatically in the 1800 unit during the DMA cycles for the display. The display utilizes approximately 15 percent of the available memory cycles for the DMA operation required to refresh the screen. The parity track allows for automatic detection of memory errors to prevent inadvertant operation with faulty memory. The memory parity is even to prevent reads from empty card positions causing a parity fault.

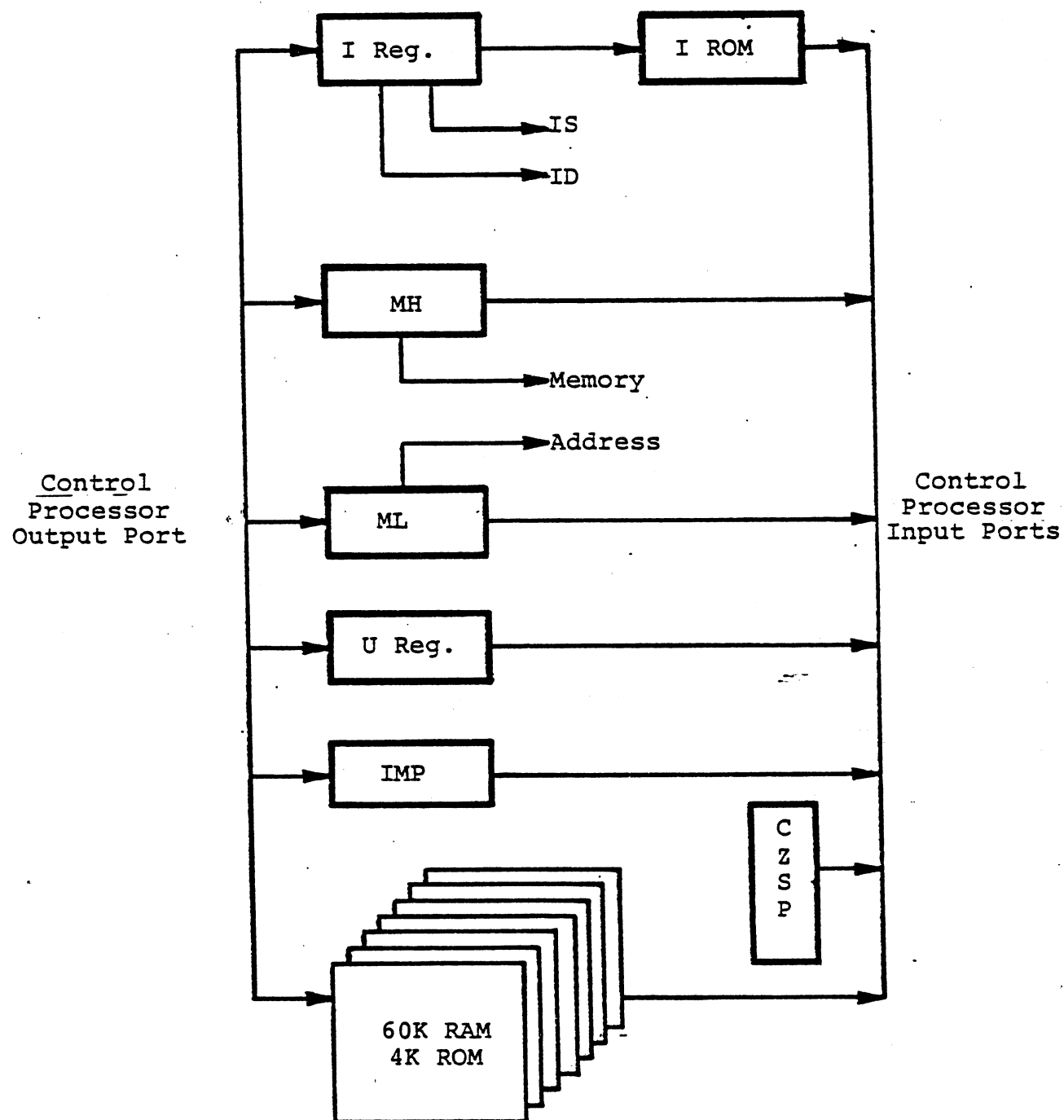
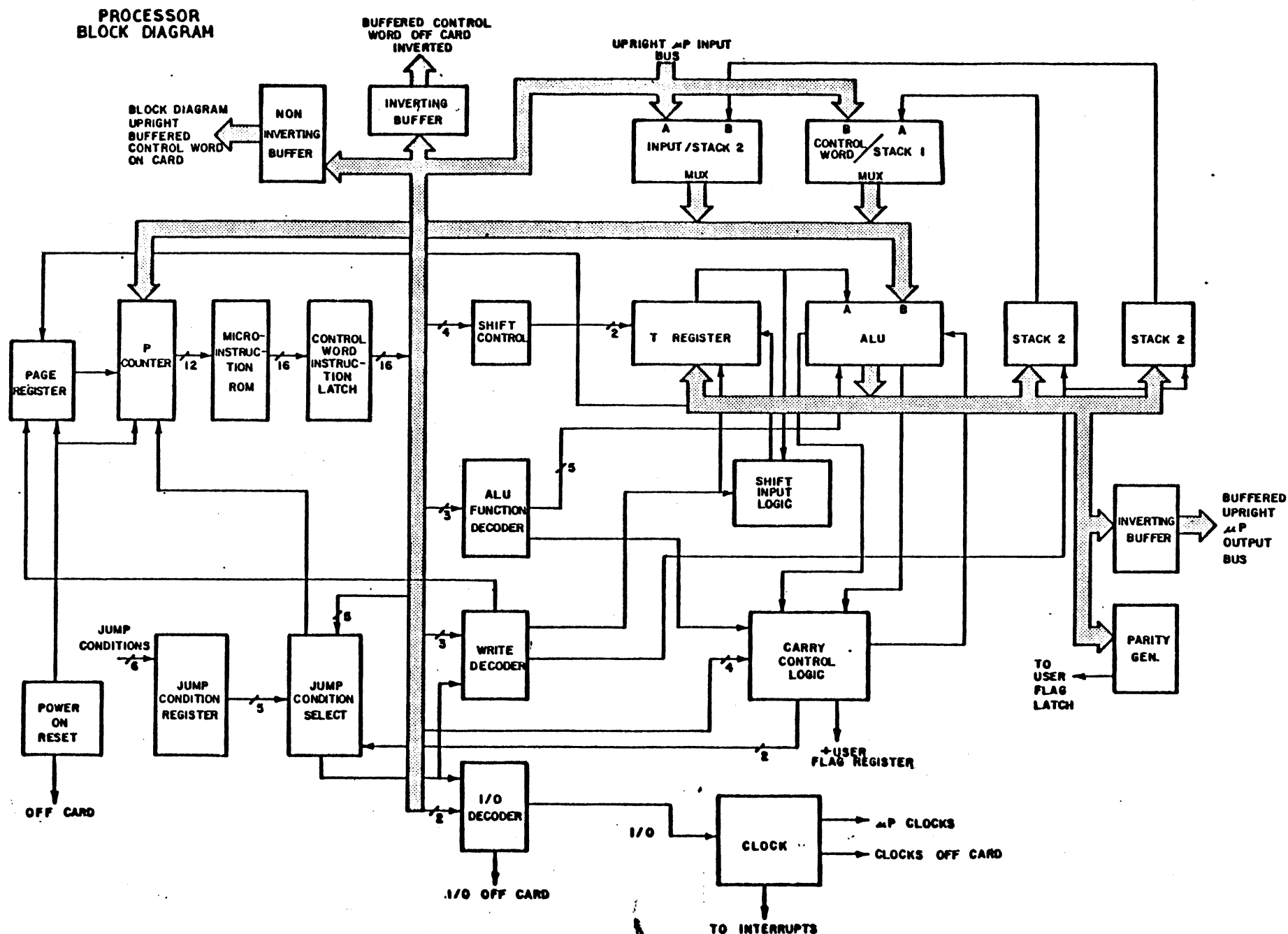


Figure 1-9. Control Processor Emulation Support



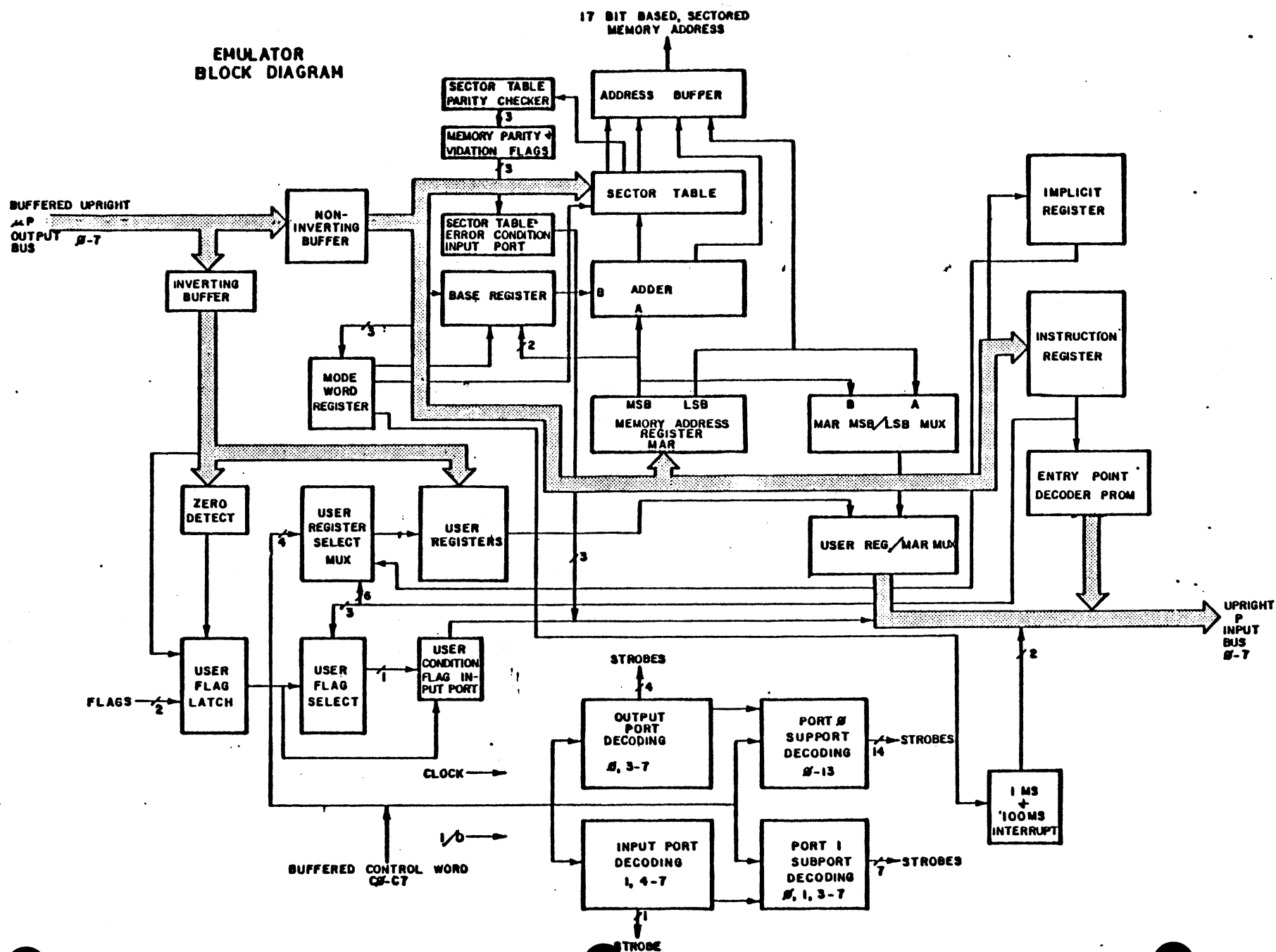


Figure 1-11. 1800 Processor, Emulation Circuitry (Processor-Emulation Board)

The 1800 memory consists of up to 124K of RAM in four cards (32K per card), and 8K of ROM in one card. The 1800 processor must have for proper operation, the following minimum number of cards installed.

<u>MEMORY CARD</u>	<u>LOCATION</u>
ROM	J7 (next to CRT).
RAM	J8

1.4.2.5.1 RAM MEMORY

The 1800 processor contains provisions for four RAM memory boards in card slots J8 through J11. Each board contains 32K bytes of 9 bits each. The ninth bit is used for parity checking. Each board is physically arranged in 2 rows of 9 bits. Each row contains 16,384 bytes. See Figure 1-12 and 1-13. For processors with less than 124K of RAM memory, the RAM boards are located as follows:

<u>USER MEMORY SIZE</u>	<u>MEMORY LOCATION</u>
32K	J8
64K	J8, J9
96K	J8, J9, J10
124K	J8 thru J11

The system RAM is physically located on the RAM card in J8 of the memory motherboard. System RAM is used to store interrupt vectors, screen data, and macro-interface bytes.

1.4.2.5.2 ROM MEMORY

The ROM card provides up to 8K of mask ROM and/or 4K of PROM. This ROM is used for initialization, debug program, keyboard and display handlers, and serial communications programs. This card contains four 2K X 8 ROM integrated circuits that have access and cycle time compatible with the RAM cards. There are also provisions for up to 8, 4K PROMS for "soft ROM" that can be strapped to occupy the same address space as the ROMS would for testing. The amount of ROM available to the system is determined by straps on the ROM card and the ROM addressing space can "overlap" some of the RAM space. The ROM is utilized in 4K increments. The ROM card generates an artificial parity bit to pacify the processor. The block diagram of the ROM board is shown in Figure 1-14. The ROM board is physically located in J7 on the memory motherboard.

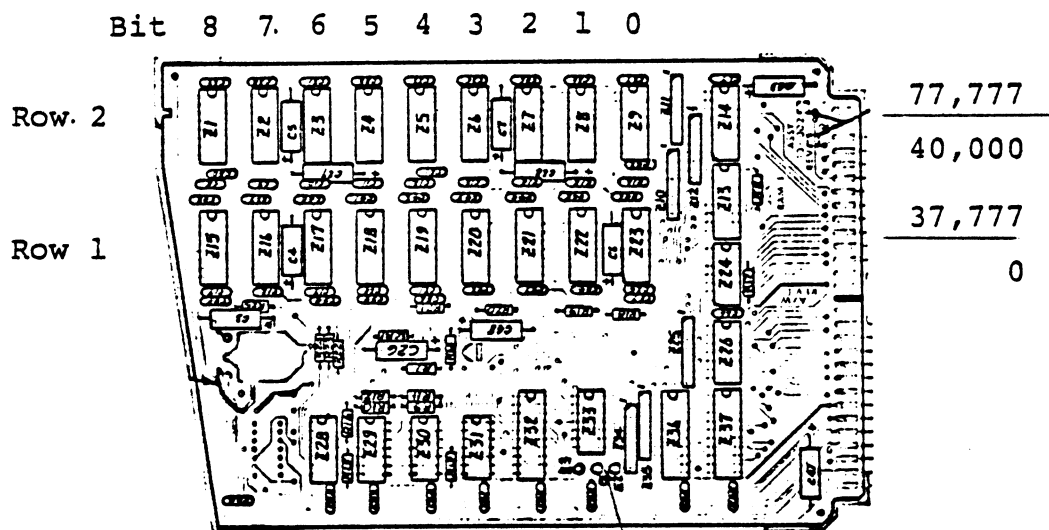


Figure 1-12. Physical RAM Memory Location

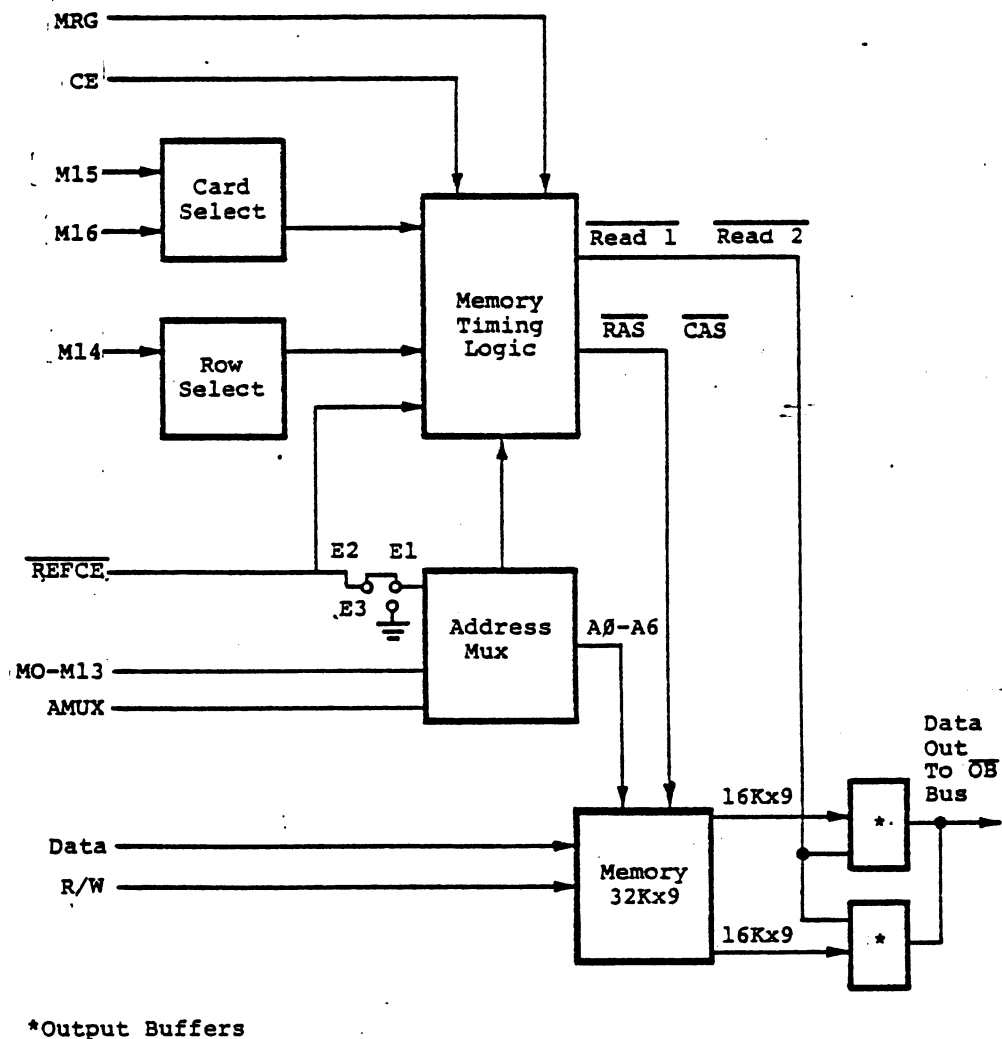


Figure 1-13. 32K RAM Memory

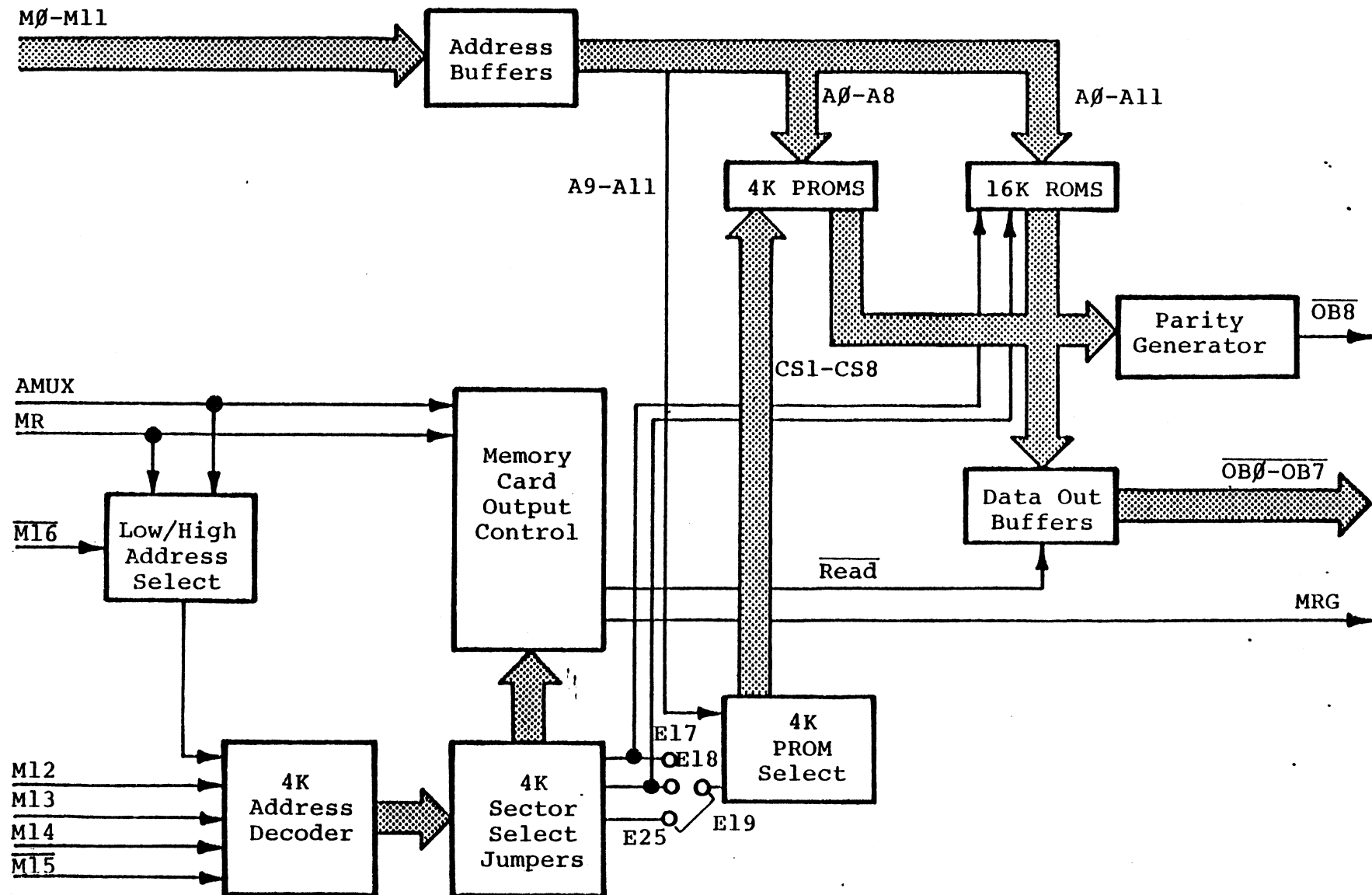


Figure 1-14. 8K ROM Memory Board

The routines contained in the ROM memory are as follows:

- a. Initialization
- b. Character set load
- c. Diskette boot
- d. Diskette drivers
- e. Display and keyboard drivers
- f. Diskette adjustment aids
- g. Debug
- h. Memory test
- i. Error message routines

1.4.2.5.3 MEMORY ALLOCATION

The memory in the 1800 is both ROM and RAM. The ROM memory is used for initialization and system routines. The ROM resides in the first page from 0170000 to 0177777 octal. The ROM can be strapped to occupy any address from 0100000 up to 0177777 by changing jumpers on the ROM card.

The RAM memory occupies addresses 0 to 0167777. The area from 0140000 to 0167777 is designated for system use and contains the interrupt vectors, screen data, and macro-interface bytes for the internal modules.

1.4.2.6 BEEP AND CLICK

The function of the beep and click is to provide audible feedback to an operator who may not be looking at the CRT. The technique for beep and click involves a D/A network to generate tones under processor control. The amplitude as well as frequency can be controlled by the processor. The range of frequency is from near DC to about 5KHz. Beep and click is available in the form of a 600 ohm output on the serial communications connector.

1.4.2.7 6600 I/O BUS

Refer to the Datapoint 6600 reference manual for definitions of the I/O bus operation and timing.

The 1800 external I/O system consists of two output ports and one input port, both controlled by the control processor. The "A bus" is simulated by an 8 bit latch that is loaded whenever an EX COM type of instruction is emulated. This latch connects to drivers that provide the low impedance drive necessary for long I/O cables. The command strobes are handled by a decoder that generates the appropriate strobe on command by the control processor and generates a 2 microsecond delay that is used to time the strobe.

TABLE 1-4

1800 PROCESSOR 6600 I/O BUS PIN ASSIGNMENTS		
Signal		Pin Number
PARALLEL DATA OUTPUT	AOUT0	44
	AOUT1	45
	AOUT2	46
	AOUT 3	29
	AOUT4	30
	AOUT5	31
	AOUT6	32
	AOUT7	33
CONTROL PULSES TO PERIPHERALS	AOUT8 (Parity Out)	34
	INPUT	12
	EX ADR	15
	EX STATUS	13
	EX DATA	14
	EX WRITE	19
	EX COM1	20
	EX COM2	21
PARALLEL DATA INPUTS	EX COM3	22
	EX COM4	23
	AIN0	1
	AIN1	2
	AIN2	3
	AIN3	4
	AIN4	
	AIN5	6
	AIN6	7
	AIN7	18
	AIN8 (Parity In)	17
	PERR (Parity Error Flag from external peripherals)	16
	INTERFACE CLOCK	39
	GROUND	40,41,42,43
	+5V	8,9,10,11
	Spare (unused)	24,25,26,27,28,35,36,37,38,47,48,49,50
On the I/O Bus: True (logic "1") = 0 volts False (logic "0") = 5 volts		

The input bus is routed to line receivers that clean up the "A bus inputs" and direct them to a control processor input port that is read when an INPUT, PIN, or MIN instruction is emulated.

The 1800 processor does not supply peripheral device operating power by the 6600 I/O bus. The 1800 processor does supply +5VDC by the 6600 I/O bus for peripheral device I/O bus drivers. This +5VDC is fused at two amperes. An LED, visible at the right end of the bus connector on the rear of the processor, indicates when the fuse is blown.

1.4.2.8 MICRO BUS I/O BUS

The 1800 contains, in addition to the standard 6600 I/O bus, a micro-I/O bus that operates at much higher transfer rates and allows the control processor in the 1800 to communicate directly with the dual diskette controller. This micro bus is separate from the standard 5500 I/O bus and allows the microprocessor to take over some of the functions previously performed by the diskette drive controller.

The micro bus is composed of an 8 bit command bus, an 8 bit data bus, 3 command strobes, and an interrupt request line. These signals are all TTL level and are not intended to be used over cable lengths beyond ten feet. The cable used on the micro bus is a 26 conductor flat cable containing an integral ground plane consisting of an expanded copper shield. The connectors are 3M type 26 pin sockets with the integral strain relief. The daisy chaining of cables is performed by having two connectors on each peripheral. The connectors on the cable are female at both ends. The last peripheral in the daisy chain will have a terminator board that will plug into its next device connector. There are no power connections in the micro bus cable. The maximum cable length is 10 feet.

Block diagrams of the processor I/O structure and I/O port decoding are shown in Figure 1-15 and 1-16.

1.4.2.8.1 MICRO BUS ORGANIZATION

a. Command and Address Bus

This bus presents four bits of address and four bits of command from the 1800 to the peripheral. This bus is not tri-state, is always active, and is ground true. Bits zero through three contain a four bit address used to specify one of fifteen device addresses. The all zero address is not used. Bits four through seven specify one of sixteen commands

I/O STRUCTURE BLOCK DIAGRAM

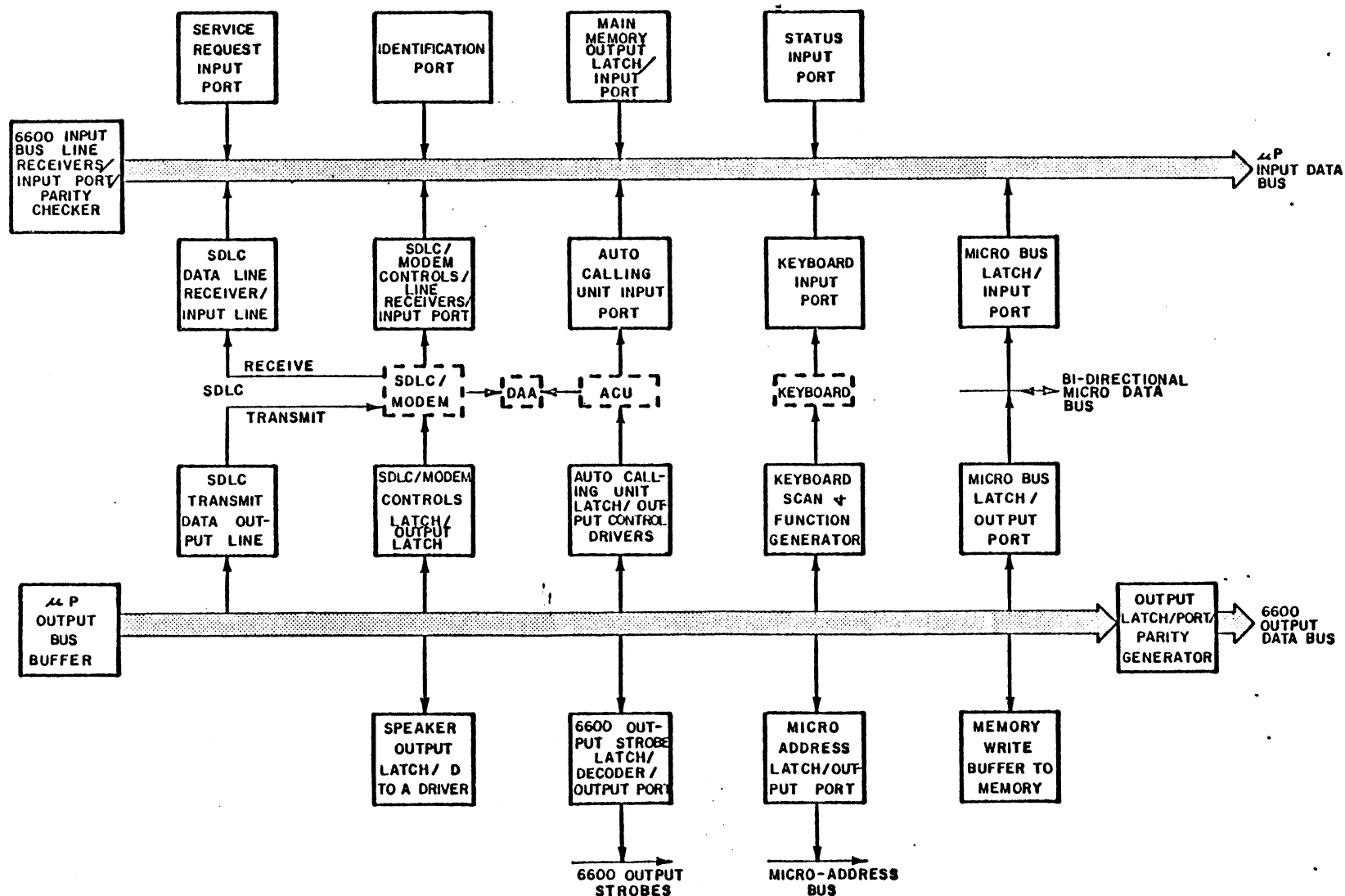


Figure 1-15. 1800 Processor I/O Structure (Display-I/O Board)

1-34

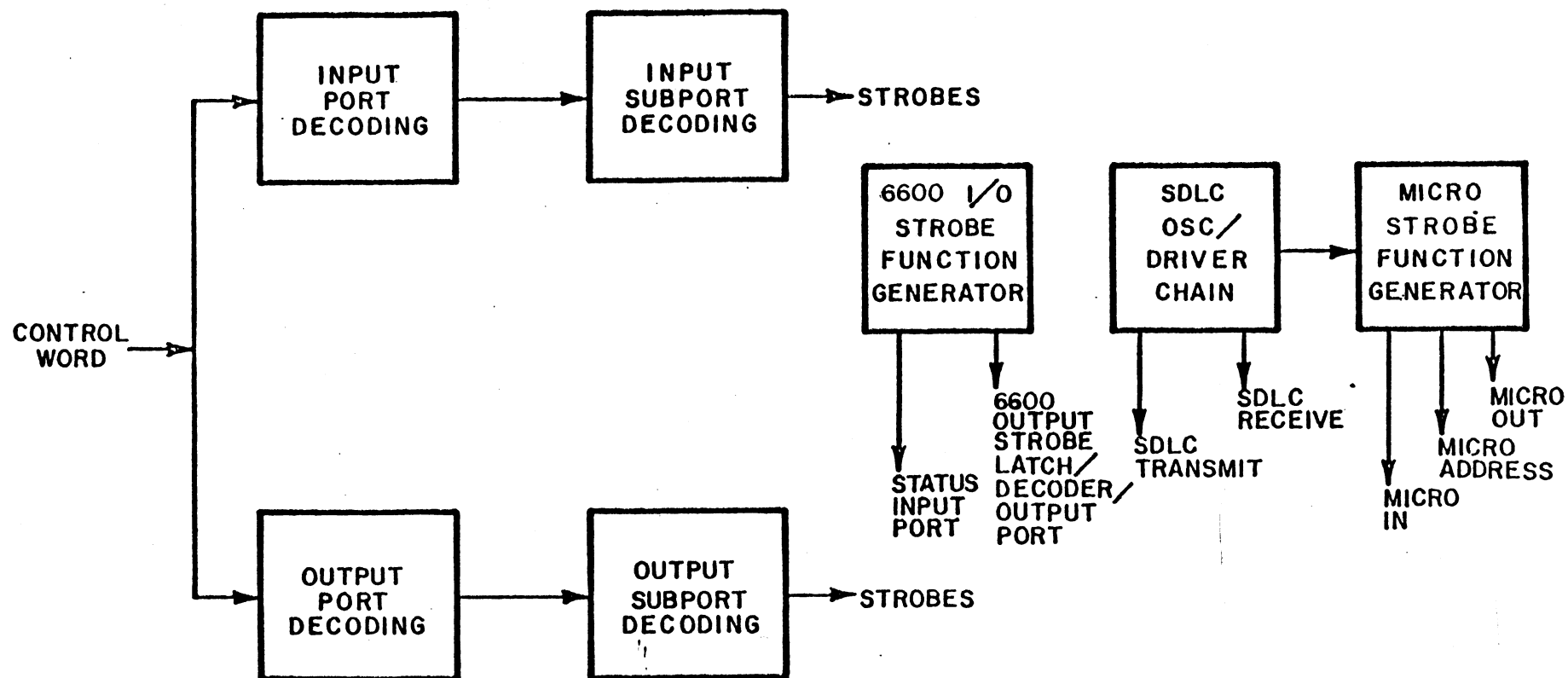


Figure 1-16. 1800 Processor I/O Port Decoding (Display-I/O Board)

that are defined by the requirements of the particular peripheral. The contents of the command and address bus will always be stable for 100 nanoseconds prior to the leading edge of any strobe and will hold for 100 nanoseconds after the trailing edge of a strobe.

Bit Definitions:

0 thru 3 - address
4 thru 7 - command

b. Strobes

There are three strobes in the micro bus. These are used to transfer commands to the peripheral and to synchronize micro interrupts. These signals are identified as Strobe 1, Strobe 2, and Iack. Strobes 1 and 2 are 500 nanoseconds long and their functions are defined according to the requirements of the peripheral. Iack is 700 nanoseconds long and is used to synchronize interrupts. Iack is propagated through each peripheral in a "daisy-chain" manner to assign an interrupt priority. The bi-directional data bus is controlled by the strobes according to the specific needs of each peripheral. The strobes are unique and will never occur simultaneously. The minimum spacing between strobes is 400 nanoseconds. Commands will be executed and data accepted only on the trailing edge of each strobe.

c. Data Bus

The data bus is an 8 bit bi-directional bus used to communicate data to and from the peripheral. This is an open collector bus and is in the off state between strobes. The direction of data transfer on this bus can be defined differently for different peripherals as required as the control processor determines the direction by loading or not loading the data out buffer before each strobe. This means that the number of input and output commands can be tailored to each specific device. For all output instructions the data bus will be valid from 150 nanoseconds before the start of the strobe to 100 nanoseconds after the trailing edge. For input instructions the peripheral should place its data or status on the data bus as soon as the strobe is received

and remove the data when the strobe is complete. The data bus is ground true.

d. Interrupt Request

The interrupt request line is an open collector line used by a peripheral to interrupt the control processor. This line is pulled to ground when an interrupt is desired and is held down until the control processor clears the interrupt with the appropriate command.

e. Power Indication

The power indication signal is provided to allow peripherals to slave their power switches to the 1800 unit. By using solid state switches in the peripherals, they can be made to power themselves up whenever the processor is powered up. The power indication signal is a 68 ohm resistor to +5 volts to provide a signal between +5 and +3.5 volts. The maximum current that can be sourced by this line is 3 ma per device (this allows for 10 switched devices).

1.4.2.8.2 MICRO BUS SIGNALS

All signals from the 1800 microbus are ground true TTL levels with pull ups. A zero is defined as +0.4 volts or less and a one is +4.0 volts or greater. Signals from the peripheral on the data bus and the interrupt request line must meet the following requirements: a zero is +0.4 volts or less and a one is +4.0 volts greater. The minimum sink capability of the data drivers on the peripheral must be 100 ma or more. The maximum leakage current in the off state is 0.1 ma for each data line (including receiver input current). The maximum current of each receiver on the command and address bus is 0.1 ma. Table 1-5 shows the micro bus signals versus pin numbers for connector J7 on the Display-I/O board (A1).

TABLE 1-5

MICRO BUS PIN ASSIGNMENTS	
<u>SIGNAL NAME</u>	<u>PIN NO.</u>
GROUND	1
STROBE 1	2
GROUND	3
STROBE 2	4
GROUND	5
IACK	6
GROUND	7
ADDRESS 0	8
ADDRESS 1	9
ADDRESS 2	10
ADDRESS 3	11
COMM 0	12
COMM 1	13
COMM 2	14
COMM 3	15
SPARE	16
INTERRUPT REQ	17
DATA 0	18
DATA 1	19
DATA 2	20
DATA 3	21
DATA 4	22
DATA 5	23
DATA 6	24
DATA 7	25
+5 (POWER INDICATION)	26

1.4.2.8.3 MICRO BUS OPERATION

a. Output Operations

The direction of data transfer (or command only) is from the 1800 terminal to the peripheral. The 1800 unit first loads the address and command on the address and command bus (Figure 1-17). This operation can occur as late as 150 nanoseconds before the strobe but will normally occur 400 or more prior to the strobe. After the command and address bus is loaded, the 1800 unit will load the data bus with the data to be sent (optional). This also can occur as late as 150 nanoseconds prior to the strobe. At the time the data bus is loaded, it will change from the off state to the levels corresponding to the data word. A

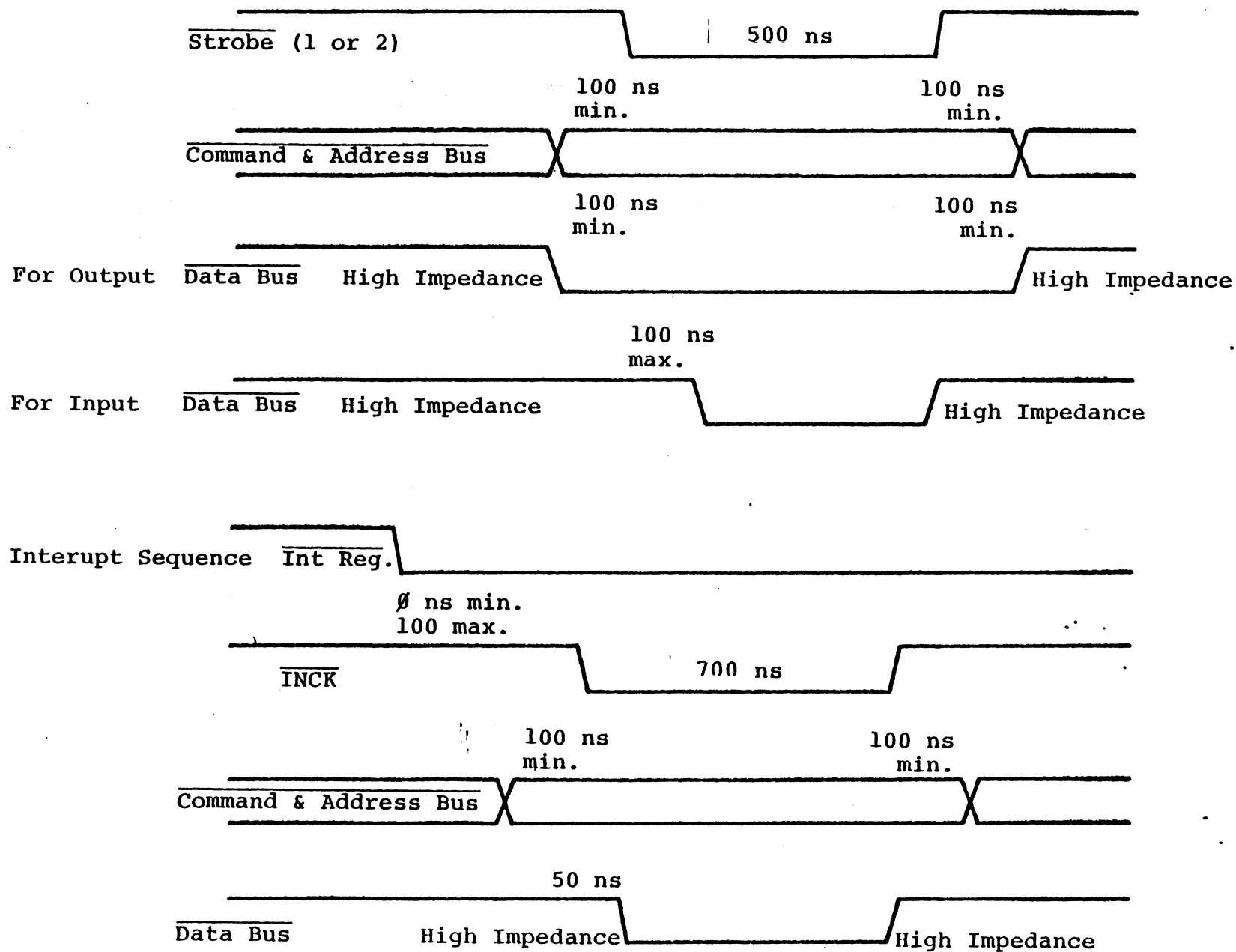


Figure 1-17. Micro I/O Bus Timing

minimum of 150 nanoseconds after the data bus (if loaded) goes active the strobe 1 or 2 will occur. The strobe will last for 400 nanoseconds and during this interval the peripheral will examine bits 0 through 3 of the address and command bus. If the address on bits 0 to 3 matches the peripherals address, it will accept the command and data (optional) on the trailing edge of the strobe. If the address does not match, the peripheral will ignore the strobe. Note that certain of the 16 possible commands for each strobe will be defined as input commands and operate as described in the next section.

b. Input Operations

Input operations transfer data or status from the peripheral to the 1800 unit (Figure 1-17). As in the output operation the address and command bus is first loaded with the address of the particular peripheral and the command desired (it must have been defined as an input command). The appropriate strobe will then be generated (strobe 1 or 2) and the peripheral will put its data or status on the data bus (the processor leaves the bus in the off state for inputs by not loading the data bus latch). The peripheral being addressed by bits 0 to 3 of the command and address bus will place its data or status on the data bus and will remove it when the strobe ends. The processor will take the data on the trailing edge of the strobe. The peripheral will leave its drivers in the off state unless strobe 1, strobe 2, or Iack is active.

c. Interrupt Sequence

A peripheral can request service by interrupting the control processor with the interrupt request line (Figure 1-17). This line is open collector to allow "wire or'ing" all of the interrupt request lines onto the same pin. A peripheral may request an interrupt (by pulling interrupt request to ground) at any time and the 1800 unit will respond by issuing an Iack. The purpose of the Iack is to assign a priority to each peripheral and to acknowledge the interrupt. Priority is assigned by routing the Iack through logic on each peripheral daisy chain fashion to allow each peripheral to "block" the Iack from

reaching lower priority devices. This assigns the highest priority to devices nearest (through the cable) the 1800 unit and lowest priority to the device at the end. When an interrupting device receives an Iack it will respond by placing its address on the data bus in the same manner as in an input. It will also "block" the Iack signal from reaching any lower priority devices that may also be requesting interrupts. This allows the 1800 unit to identify an interrupting device without "polling" each device on the micro bus. It will also be possible to issue a command on the address and command bus concurrent with the Iack to perform any additional control necessary (inhibiting certain classes of interrupts, for example).

1.4.2.9 POWER SUPPLY

The 1800 Power Supply (Figure 1-18) is a pulse-width modulated DC-DC converter operating from rectified and filtered AC power line voltage. The supply operates from 115VAC into a voltage doubler, or from 230VAC into a bridge rectifier to produce a nominal 300VDC from the input filter. This voltage is switched at a 20KHz rate across the primary of a step down power transformer to produce, from multiple secondaries, all the desired output voltages. Regulation is accomplished by pulse width modulation of the power switches. The pulse width modulation technique produces, at the input to LC filters, pulses with varying amplitudes and widths, but constant average value.

The +5V output is sensed, and therefore, well regulated. Due to converter and inductor IR drops, the remaining outputs are less well regulated, especially against load changes.

Protection circuits are provided to prevent damage from output short circuits, AC line over or under voltage, and +5V output overvoltage. If one of these conditions arise, the protection circuit will shut off the power supply. At shut off one or two LED indicators will light showing which protection circuit was activated. The LED'S (LV, OV, IL, and CB, located on the power supply control board) are explained in Paragraph 1.4.1.1.

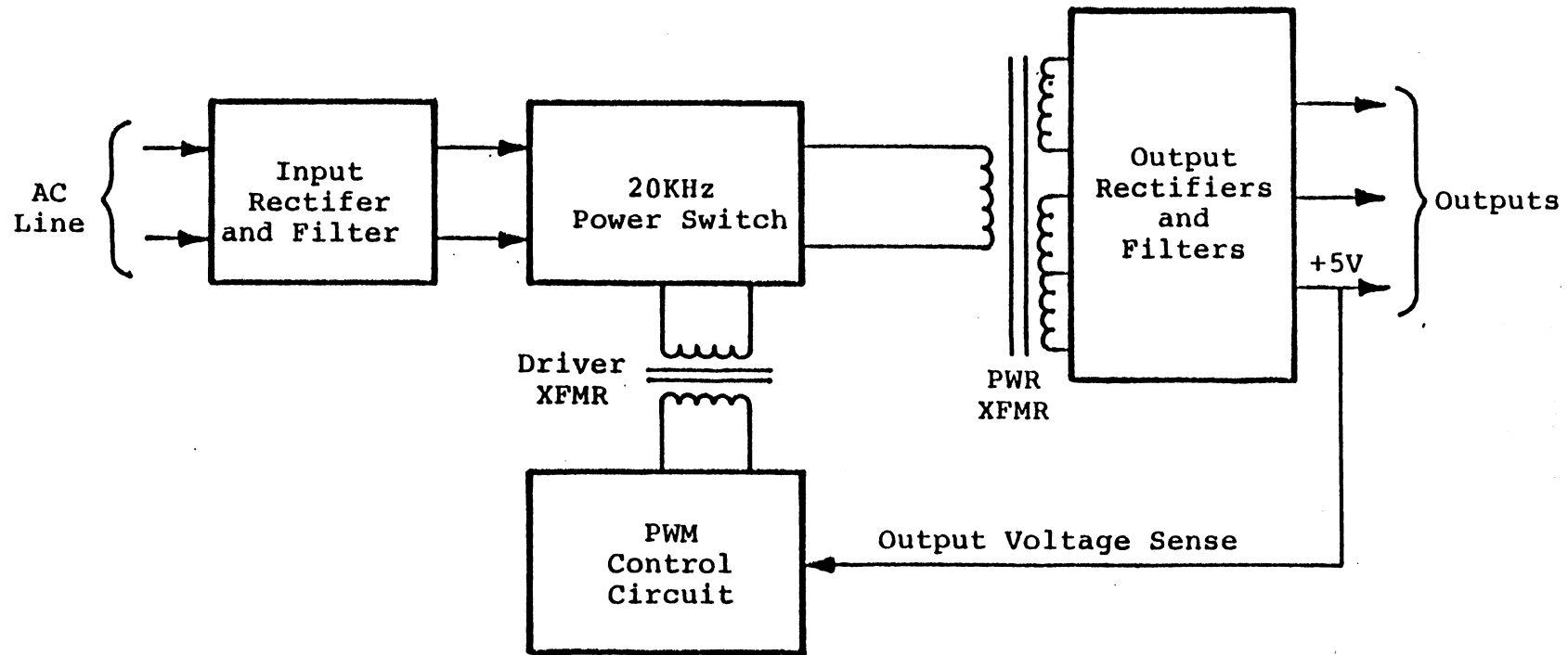


Figure 1-18. Power Supply Block Diagram

SECTION 2

INSTALLATION

2.1 GENERAL

The 1800 processor installation procedures are given in this section. Test equipment required for installation is given in Table 3-1. A complete installation includes the following procedure.

- a. Unpacking and inspection.
- b. Initial checkout.
- c. Installation.
- d. System checkout.

The 1800 processor is to be placed on a user supplied table or desk. The table or desk must support 60 pounds. If a processor and disk drive are to be placed on one table, the table must support the combined weight of both units. Refer to applicable manuals for weights of other equipment.

2.2 UNPACKING AND INSPECTION

The 1800 processor and removable keyboard are shipped in a cardboard container. Inspect the container for exterior damage such as crushed corners and punctures. All damage found during unpacking and inspection must be recorded.

- a. The processor and keyboard are packed between two polystyrene plastic end caps (See Figure 2-1). Carefully remove the processor and keyboard, with the end caps, from the container. Verify that all items are present as per the shipping list. Missing items must be recorded.
- b. Place the processor on a flat surface capable of supporting 60 pounds. Position the processor on the base plate only. Do not attempt to support the processor on the housing. Remove the end caps and place processor on table with keyboard in front of processor
- c. Inspect processor and keyboard exterior for cracks, scratches and any other evidence of damage incurred during shipment.

① Corner Caps (8, One at each corner).

② Processor Box with corner caps is placed in a Carton for shipment (not shown).

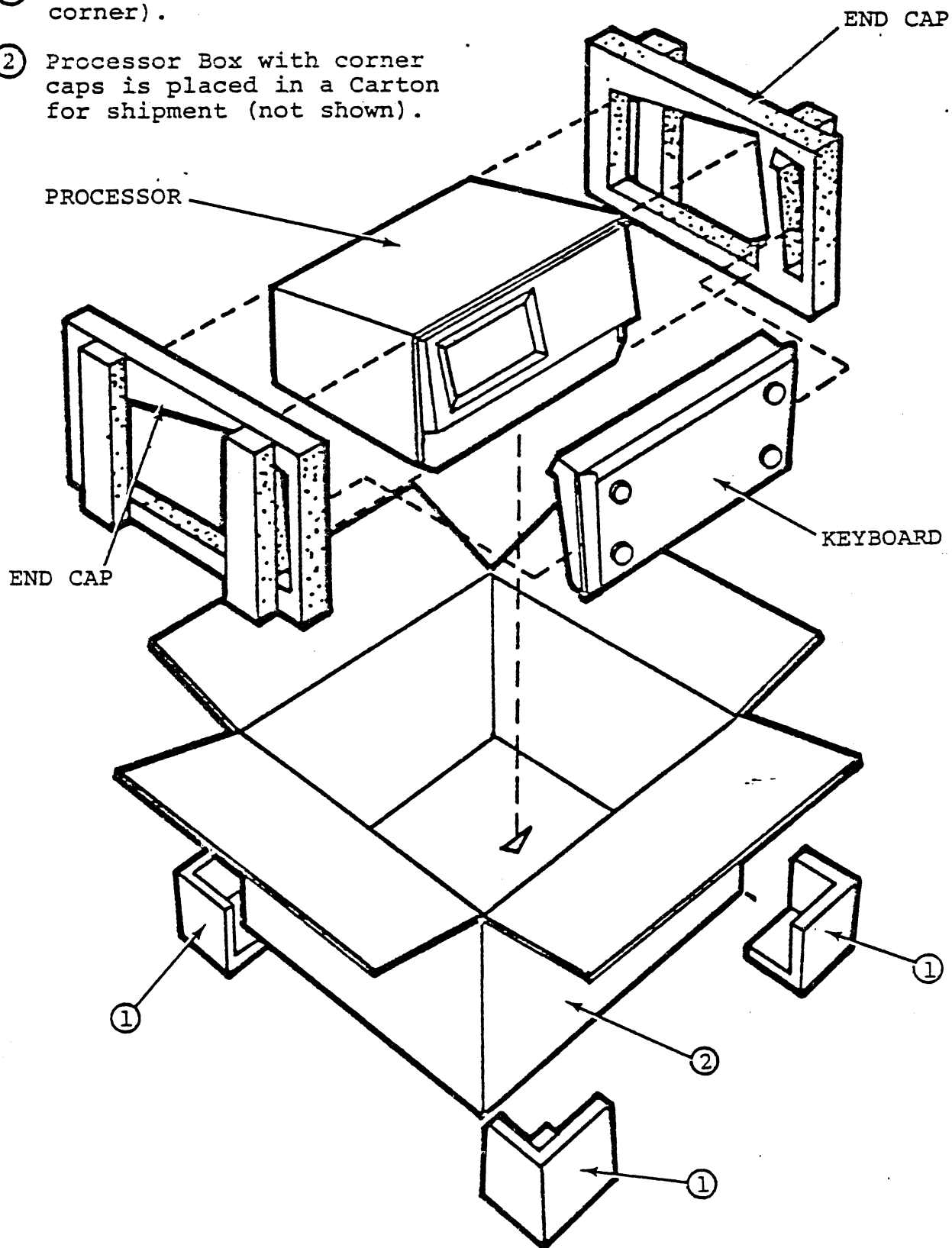


Figure 2-1. 1800 Processor Shipping Container

- d. Check power cable connector for bent or broken pins. Do not connect cable at this time.
- e. Remove the processor housing. The housing is secured to the base plate by two 1/4 turn fasteners (one on each side of the base plate).
- f. Remove from processor, all memory boards, and check for foreign material on boards and in memory bay. Ensure that no damage or broken components exist. Check edge connectors for damage or corrosion.
- g. Replace all memory boards and check that they are firmly seated in connectors.
- h. Check that processor contains a ROM memory card in memory bay card slot 1 (far left-hand slot next to CRT). Check that processor contains a RAM memory card in card slot 2. Up to three additional RAM cards may be installed in card slots 3 through 5. Card slot 6 must remain empty.
- i. Remove screw and lift power supply control board up.
- j. Check all accessible printed circuit boards for loose or damaged components. Check for foreign material on boards. Check inside and outside the processor chassis for loose or damaged hardware. Check that all printed circuit boards and assemblies are secure. Check that input power harness is secure and contains a 3 ampere fuse.

. NOTE

To ensure a connector is fully seated, press it onto its jack.

- k. Check that all connectors inside the chassis are fully seated. Check that the yoke and flyback transformer connectors (P1/J8, P2/J9, and P1/J7) on the deflection raster scan board are fully seated. Ensure that the high voltage connector on the CRT is secure. Ensure that the yoke is tight on the CRT and has not moved out of place during shipment. Check for loose adjusting magnets around yoke.

- l. Check that all connectors on the rear of the display-I/O and processor-emulation boards are fully seated. Check that keyboard cable connector on front of display-I/O board is fully seated.
- m. Check that all power supply connectors are fully seated. Check for any loose or damaged components on the power supply control board.

NOTE

Do not replace cover at this time.

- n. Remove keyboard cover. The cover is secured to the keyboard base plate by two screws (one on each end of the base plate).
- o. Check for foreign material on keyboard, printed circuit boards, and in keyboard housing. Ensure that no damage or broken components exist. Check that all cable connectors are firmly in place. Check that keyboard cable ground lead is secure.
- p. Check keyboard for loose keycaps. Reseat any keycaps that appear to be loose.
- q. Check keyboard latch adjustment key attaching and detaching keyboard to processor. If keyboard is difficult to attach or detach to processor, or if keyboard is loose when attached to processor, then adjust keyboard latches (Paragraph 5.2.5).

NOTE

Do not replace keyboard cover at this time.

2.3 INITIAL CHECKOUT

NOTE

To ensure that moisture has not condensed on cool surfaces, allow equipment to reach room temperature before applying power.

CAUTION

Check input power requirements on identification label to ensure processor is configured for site power service. Check that site power service has correct voltage and has proper third wire ground connection.

- a. Ensure processor power switch is OFF and connect power cable to input power source.
- b. Connect voltmeter to monitor +5VDC between test point at upper left corner of keyboard PWA and ground.

CAUTION

When applying AC power to unit, if +5VDC is not indicated on voltmeter, immediately remove AC power to prevent damage to printed wiring boards.

- c. Momentarily set the processor power switch to ON, and check for +5VDC on voltmeter. The blower motor should operate immediately.
- d. If +5VDC was present, set processor power switch to ON. Check the output of the +5VDC supply and adjust if necessary (Refer to Paragraph 4.2.1).
- e. Check the output of +12VDC supply and adjust if necessary. Refer to Paragraph 4.2.2.
- f. Check the output of +14VDC supply and adjust if necessary. Refer to Paragraph 4.2.3.
- g. Check processor display alignment and adjust if necessary. Refer to Paragraph 4.3.1.
- h. Press and hold RESTART and DISPLAY keys and press INT. The internal debug program should appear in the lower right hand corner of the CRT.
- i. Type the following on the keyboard: "12345T". Let the internal memory test run for 50 passes. Return to Debug.
- j. Set the processor power switch to off.
- k. If applicable, set processor identification switch S1 (Paragraph 6.2.4).

1. Replace the processor and keyboard housing.

2.4

INSTALLATION

- a. Place the processor in its operating location. Allow at least 6 inches clearance to gain access to rear of unit.

NOTE

The 1800 processor does not supply power to peripheral equipment by the 6600 I/O port. All 6600 peripheral equipment must supply own power or utilize an auxiliary I/O power supply.

- b. If possible, verify that peripheral equipment is operational prior to connecting to the processor. Refer to applicable equipment manuals.
- c. Connect and secure peripheral equipment to the proper I/O connector on the rear of the processor. Maximum 6600 I/O cable length is 24 feet. See Figure 2-2.
- d. Connect power cable to input power source.

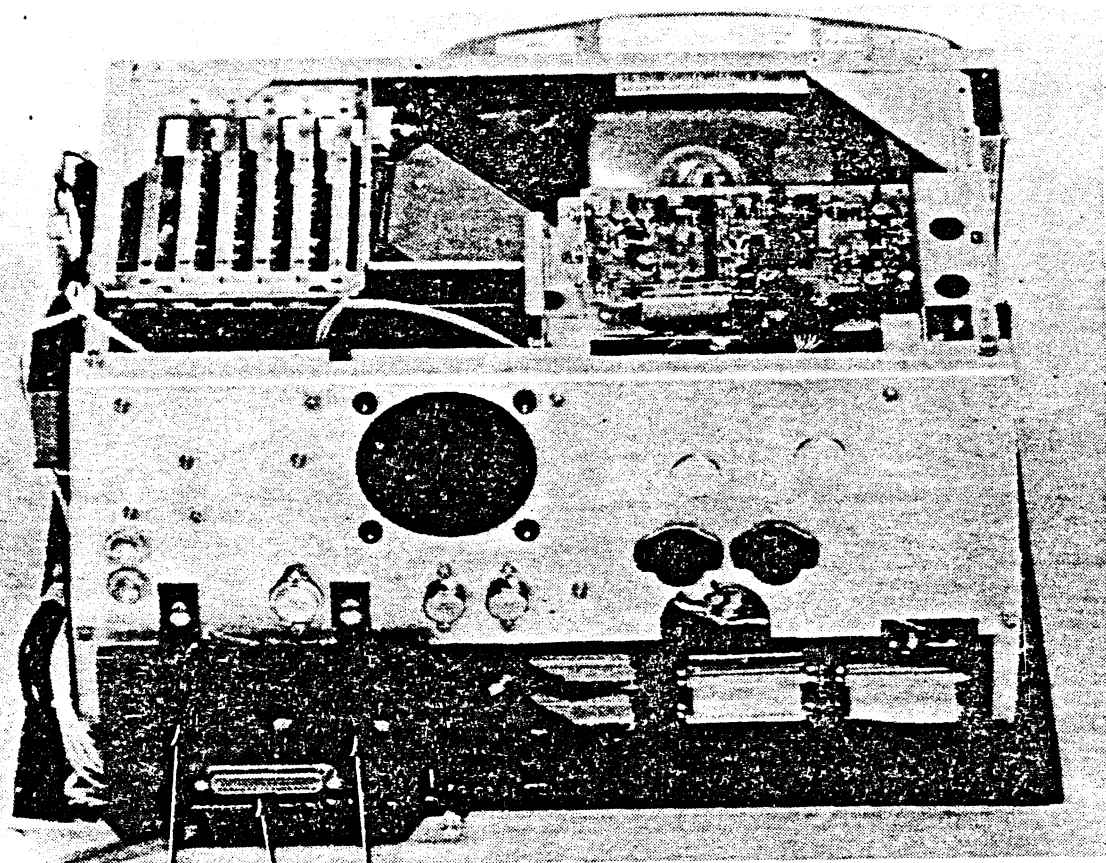
2.5

SYSTEM CHECKOUT

NOTE

When running tests on equipment, all failures must be recorded.

- a. Position processor power switch to ON.
- b. Run applicable diagnostic or operational tests for the processor and dual diskette drive.
- c. Run applicable diagnostic or operational tests for other attached peripheral equipment.
- d. Place all equipment in operational status.



J7, Microbus I/O
 J1, 660Q I/O
 J6, Communications I/O

Figure 2-2. 1800 Processor I/O Connectors

SECTION 3

MAINTENANCE

3.1 GENERAL

This section contains procedures for the on-site maintenance of the 1800 Processor. On-site maintenance in cases of malfunctions is normally limited to replacement of subassemblies and selected components, such as transformers and switches, that are not a part of a readily removable subassembly. In situations where first level maintenance of the system leads into procedures that are considered beyond first level capabilities, assistance should be requested from Customer Service Technical Support. Test equipment required for first level maintenance is listed in Table 3-1.

TABLE 3-1

TEST EQUIPMENT
Multimeter or DVM Oscilloscope (10MHz band width) 5"X7.9" Linearity Mask 12 inch scale (Graduated in 1/100 increments) Paint Brush, 1 inch

3.2 PHOTOGRAPHIC VIEWS

Three photographic views of the processor are given in Figures 3-1 thru 3-3.

3.3 PREVENTIVE MAINTENANCE

Preventive maintenance for the 1800 Processor consists primarily of unscheduled cleaning, inspection and diagnostic checkout. Scheduled maintenance operations should be performed at the indicated intervals to ensure reliable operation of the system.

The following procedures should be accomplished at a minimum interval of 12 months.

- a. Check the output of the +5VDC supply and adjust if necessary (Paragraph 4.2.1).
- b. Check the output of the +12VDC supply and adjust if necessary (Paragraph 4.2.2).

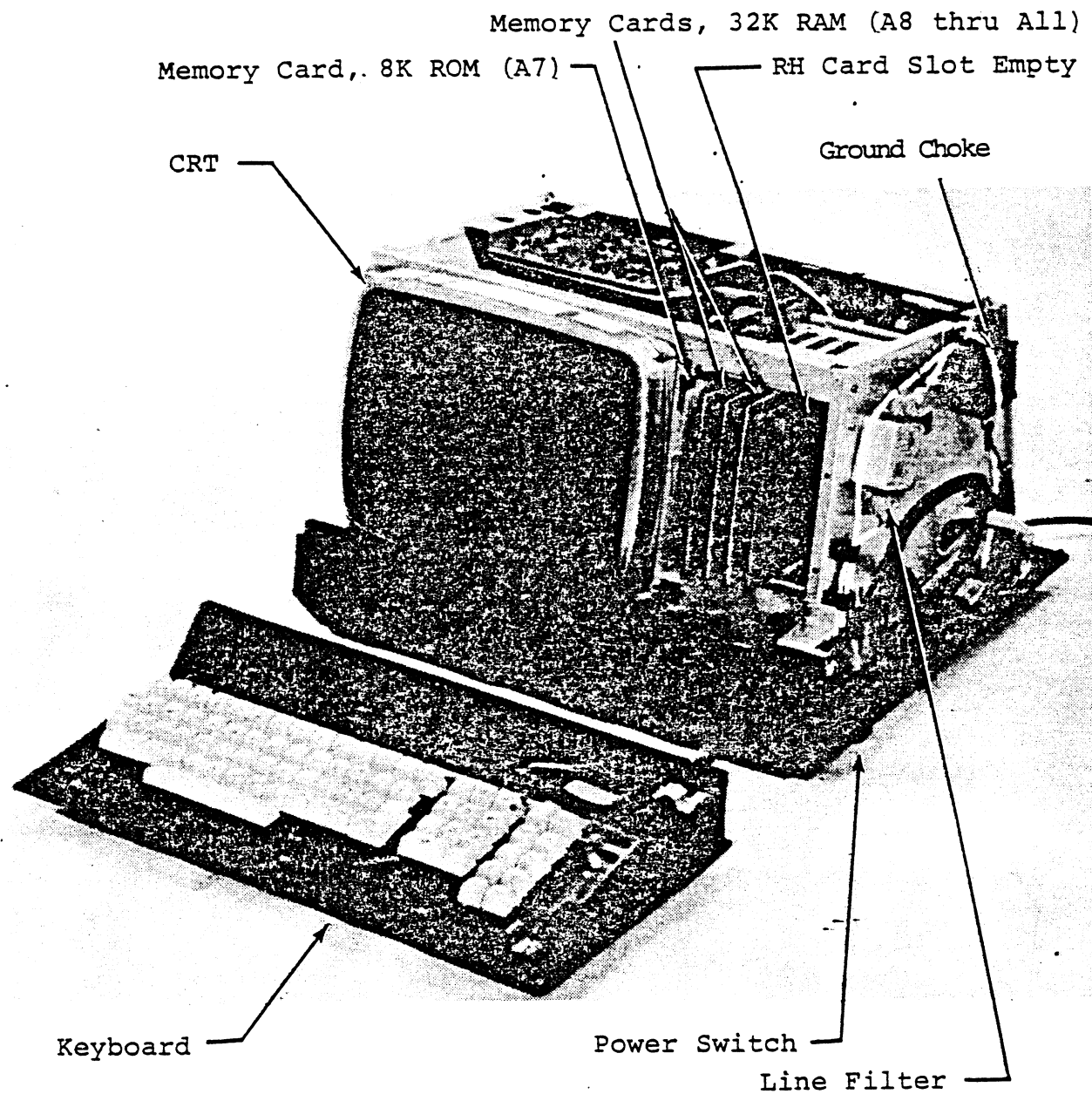


Figure 3-1. 1800 Processor Major Component Locations-
Front View

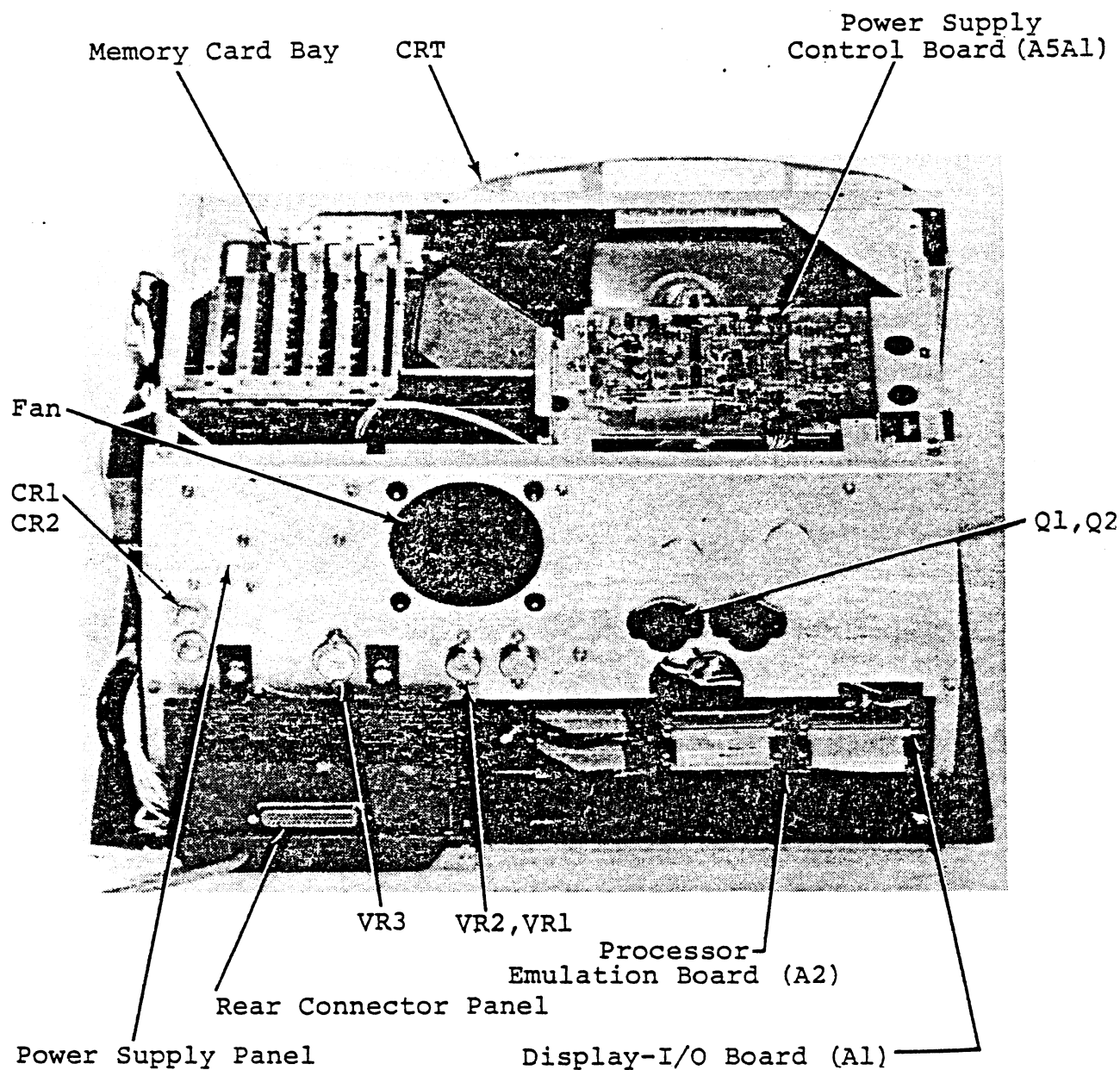


Figure 3-2. 1800 Processor Major Component Locations-Rear View

- | | |
|--------------------------------------|---|
| 1. Memory Card Bay | 7. Power Supply Panel (Removed) |
| 2. Flyback Transformer | 8. Power Supply Board II (A5A3) |
| 3. CRT | 9. Power Supply Control II Board (A5A1) |
| 4. Deflection Raster Scan Board (A4) | 10. Secondary Regulator Board (A5A2) |
| 5. Display-I/O Board (A1) | 11. Memory Motherboard (A6) |
| 6. Processor-Emulation Board (A2) | |

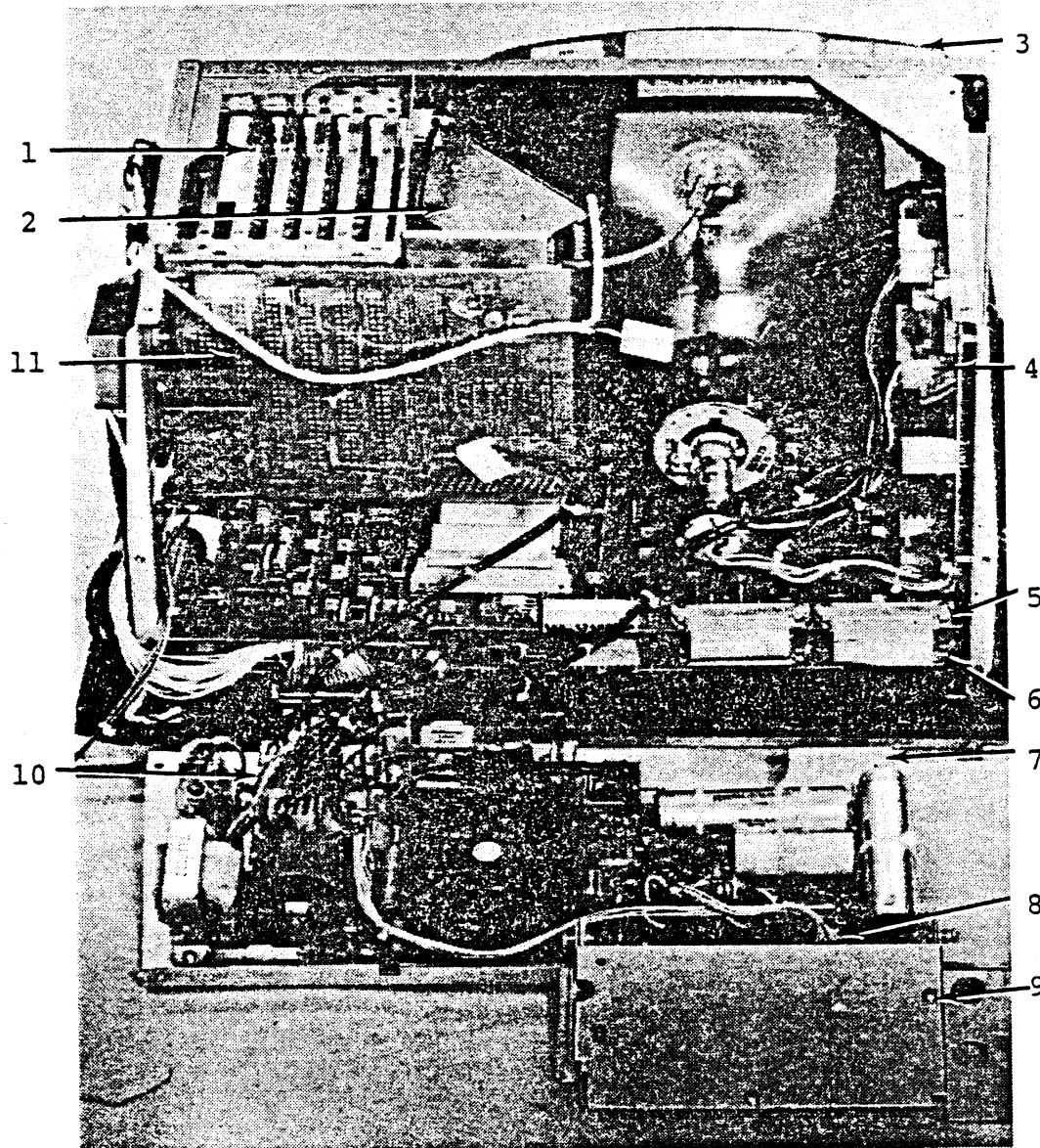


Figure 3-3: 1800 Processor Major Component Locations-
Interior View

- c. Check the output of the +14VDC supply and adjust if necessary (Paragraph 4.2.3).
- d. Check for any airflow restrictions, such as paper or tissue, under the keyboard.
- e. Check operation of the cooling fan. If fan motor is noisy, overheats or fails to operate, replace the fan assembly.
- f. Using 1 inch paint brush, clean keyboard and screen area. Clean cover if necessary with damp cloth.
- g. Ensure that I/O connector screws are secure.
- h. Run applicable operational test.

3.4 CORRECTIVE MAINTENANCE

Corrective maintenance of the 1800 Processor normally consists of verifying and correcting reported malfunctions incurred during operation.

3.4.1 FAULT ISOLATION

The fault isolation procedures contained in Figure 3-4 are based upon malfunctions that could occur during routine use of the system. All peripheral equipment should be disconnected and remain disconnected until the malfunction has been isolated and corrected, or it has been definitely determined that the malfunction is not in the Processor.

Removal and replacement procedures for subassemblies and components are included in Section 5. Section 8 of this manual includes schematics and diagrams required for wiring continuity checks. Section 8 also includes the 1800 Processor ROM Guide.

SYMPTOM	PROBABLE CAUSE	REMEDY
Processor off. Fan off.	1. No input power.	1. Check connection to input power source. 2. Check processor power switch ON. 3. Check AC fuses F1 and F2 (between power switch and line filter). 4. Check source voltage at power supply board II (A5A3) between J3-2 and J3-3. 5. Check for bad power switch or line filter.
Processor off. Fan running. Display off. Keyboard indicator off.	1. Power supply off.	1. Set processor main power switch OFF then ON (to reset power supply). 2. Check LED indicators on power supply control board (A5A1). a. LV-indicates that AC line voltage fell below 90VAC (or 180VAC).

Figure 3-4. Fault Isolation

SYMPTOM	PROBABLE CAUSE	REMEDY
		b. OV-indicates that AC line voltage rose above 140VAC (or 280VAC). c. IL-indicates current overload or short-circuit. d. CB-indicates that +5VDC regulated voltage exceeded +7.0VDC. Adjust +5VDC (Paragraph 4.2.1).
Processor on. Processor not functioning properly.	1. Power supply voltages.	1. Check for +15VDC between J6-6 and ground on deflection raster scan board. 2. Check for +12VDC between J1-3 and ground on memory motherboard. 3. Check for -12VDC between J1-4 and ground on memory motherboard. 4. Check +5VDC regulated voltage and adjust if necessary (Paragraph 4.2.1).
Processor on. Display off.	1. General	1. Increase intensity of raster with R14 on deflection raster scan board until raster appears. If raster good go to symptom:

Figure 3-4. (Cont)

SYMPTOM	PROBABLE CAUSE	REMEDY
		Processor on, raster good, bad or no characters displayed. If raster off go to symptom: Processor on, raster off.
Processor on. Raster off.	1. 60Hz vertical sync from power supply.	1. Check vertical reset at P5-5 on deflection raster scan board. Use oscilloscope.
	2. Horizontal sync from display I/O board.	1. Check horizontal drive at P5-4 on deflection raster scan board. Use oscilloscope.
	3. CRT filament or filament voltage from filament transformer.	1. Check for 12.6VDC filament voltage between E3 or J6-2 and ground on deflection raster scan board.
	4. High voltage from flyback transformer.	1. Check high voltage circuitry from J7 on deflection raster scan board to high voltage lead on CRT.
	5. Cabling.	1. Check as necessary. See Figure 8-1.

Figure 3-4. (Cont)

SYMPTOM	PROBABLE CAUSE	REMEDY
Processor on. Raster good. Bad or no characters displayed.	1. Character generation RAM on display-I/O board.	1. Substitute display-I/O board.
	2. Standard character set not loaded properly from ROM memory board.	1. Substitute ROM memory board (A7).
	3. Special character set not loaded properly from user software.	1. Load special character set from known good software. 2. Substitute display-I/O board.
	4. Deflection raster scan board.	1. Substitute deflection raster scan board.
Processor will not load program from disk.	1. Micro Bus cable.	1. Perform a read operation using internal ROM routine and check that disk read/write head will seek and restore. 2. Check if micro bus cable is secure. 3. Substitute micro bus cable.

Figure 3-4. (Cont)

SYMPTOM	PROBABLE CAUSE	REMEDY
	1. Processor.	1. Run DEBUG internal ROM routine. If DEBUG will not run go to symptom: Processor will not run DEBUG internal ROM routine. 2. If DEBUG runs, run MEMORY TEST internal ROM routine. If MEMORY TEST will not run, go to symptom: Processor will not run MEMORY TEST internal ROM routine. 3. If MEMORY TEST runs, run SYSTEM TEST internal ROM routine. If SYSTEM TEST will not run, substitute processor/emulation board and/or check processor cabling.
Processor will not run DEBUG internal ROM routine.	1. Processor/emulation board.	1. Substitute processor/emulation board.
	2. Display-I/O board.	1. Substitute display-I/O board.
	3. ROM memory board.	1. Substitute ROM memory board.
	4. Keyboard.	1. Substitute keyboard.
	5. Memory motherboard.	1. Substitute memory motherboard.

Figure 3-4. (Cont)

SYMPTOM	PROBABLE CAUSE	REMEDY
	6. Cabling.	1. Check processor cabling as necessary. See Figure 8-1.
Processor will not run MEMORY TEST internal ROM routine.	1. RAM memory board.	1. Substitute RAM memory board as indicated by internal ROM routine via CRT.
	2. Memory Motherboard.	1. Substitute memory motherboard.
	3. Display-I/O and/or processor/emulation board.	1. Substitute display-I/O and/or processor/emulation board.
	4. Cabling.	1. Check processor cabling as necessary. See Figure 8-1.

Figure 3-4. (Cont)

SECTION 4
ALIGNMENT AND ADJUSTMENT

4.1 GENERAL

The following alignment and adjustment procedures should be performed whenever a component is replaced and as a part of preventive maintenance. The tools and test equipment are listed in Table 3-1.

4.2 VOLTAGE ADJUSTMENTS

4.2.1 +5 VOLT ADJUSTMENT

- a. Connect meter ground probe to ground and voltage probe to the +5 VDC. Test points are on the upper left corner of the keyboard PWA. An alternate test point for +5 VDC is Pin 4 of connector J1 on memory motherboard (Figure 4-2). Meter should read +5.0 to +5.1 VDC.
- b. Adjust R15 on the power supply control board (A5A1) for +5.0 VDC. See Figure 4-1.

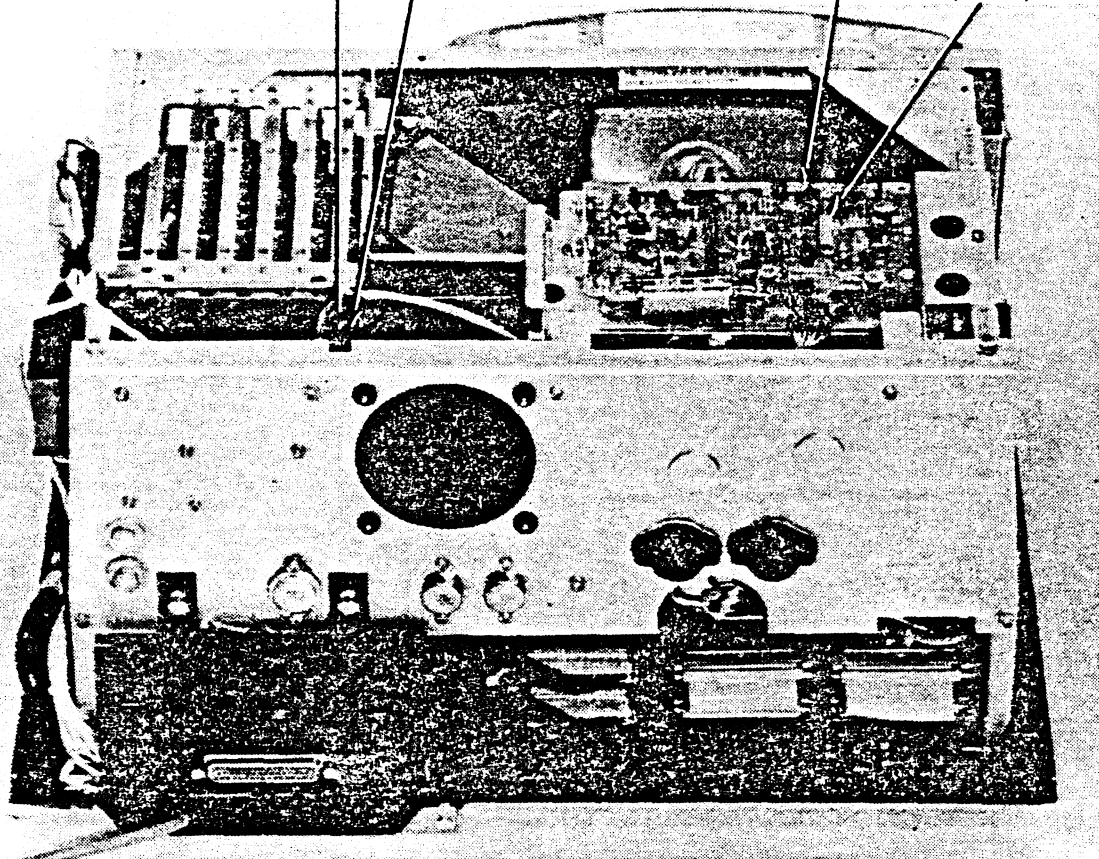
4.2.2 +12 VOLT ADJUSTMENT

- a. Connect meter ground probe to ground and voltage probe to the +12 VDC. Test point is Pin 6 of connector J1 on memory motherboard (Figure 4-2). Meter should read +12.0 $\pm$ 0.6 VDC.
- b. Adjust R9 on the secondary regulator board (A5A2) for +12.0 (Figure 4-1).

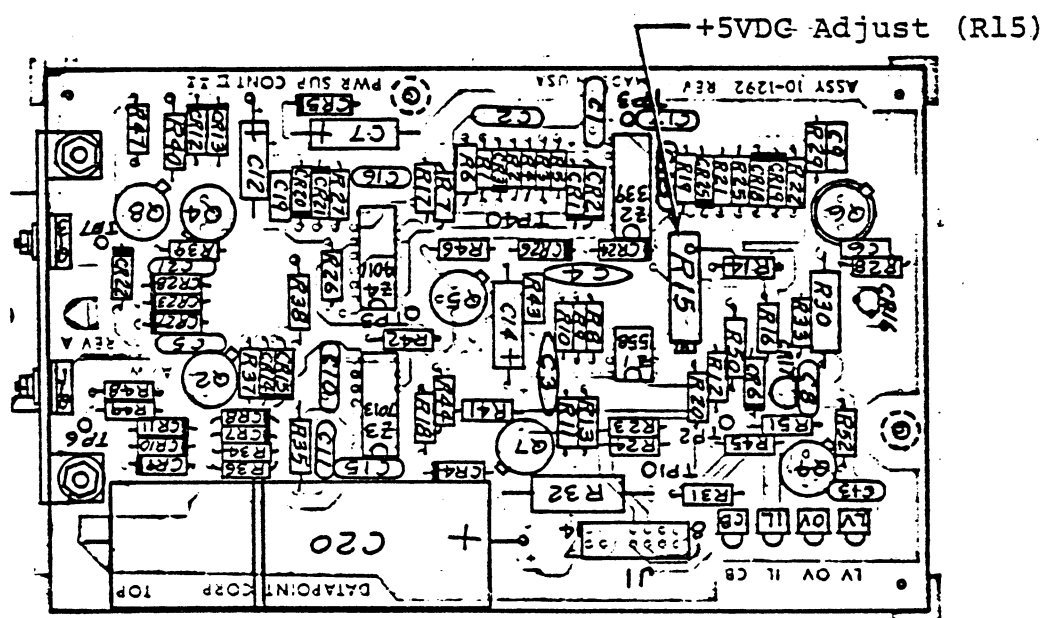
4.2.3 +14 VOLT ADJUSTMENT

- a. Connect meter ground probe to ground and voltage probe to the +14 VDC. Test point is Pin 7 of connector J1 on memory motherboard (Figure 4-2). Meter should read +14.0 $\pm$ 0.0/-2.0 VDC.
- b. Adjust R6 on the secondary regulator board (A5A2) for +14.0 VDC (Figure 4-1).

Power Supply Control Board (A5A1)
 +12VDC Adjust (R9) +14VDC Adjust (R6) +5VDC Adjust (R15)

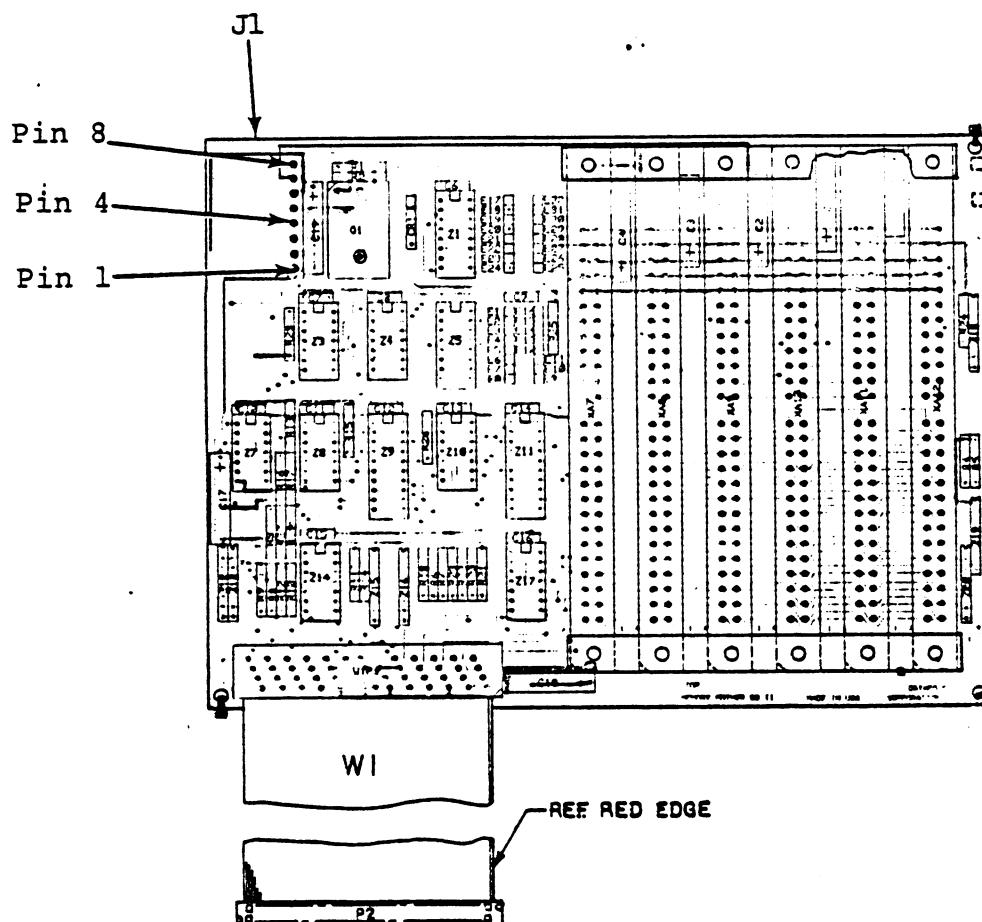


(a) General View



(b) Power Supply Control Board (A5A1)

Figure 4-1. 1800 Processor Voltage Adjustments



```
+14VDC on Pin 7 of J1
+12VDC on Pin 6 of J1
+ 5VDC on Pin 4 of J1
```

Figure 4-2. Test Points for +5VDC, +12VDC, and +14VDC Adjustments

4.3 DISPLAY ALIGNMENT

The following alignment procedures should be accomplished after replacement of the CRT, yoke, flyback transformer, or deflection raster scan board (A4). See Figure 4-3 for location of display adjustments.

- a. Position Processor power ON-OFF switch to ON.
- b. Fill the CRT screen with "H"'s as follows:
 - (1) Enter Debug routine.
 - (2) To generate "H"'s, enter 110J.
 - (3) To generate inverse "H"'s, enter 310J.

WARNING

With housing removed and power ON, 12,000 volts are present at the CRT.

- c. Adjust the brightness control R14 on the deflection raster scan board (A4) until the retrace line appears at the bottom of the screen, then turn the control back until the retrace line just disappears. See Figure 4-4 for location of controls.
- d. Adjust focus control R12 to focus the display.
- e. Adjust the vertical size control R30 to set the vertical size to 5 ± 0.05 inches.
- f. Adjust the vertical position control R21 to center the display in the viewing area.
- g. Check horizontal linearity by measuring the width of the displayed characters that appear to have the greatest and least width. The maximum width of the characters should be less than 0.100 inch. The minimum width of the characters should be greater than 0.06 inch.
- h. If horizontal linearity is not within the above limits, adjustment must be made by adding from one to three correction magnets to variable inductor L4. If adjustment is required proceed as follows:

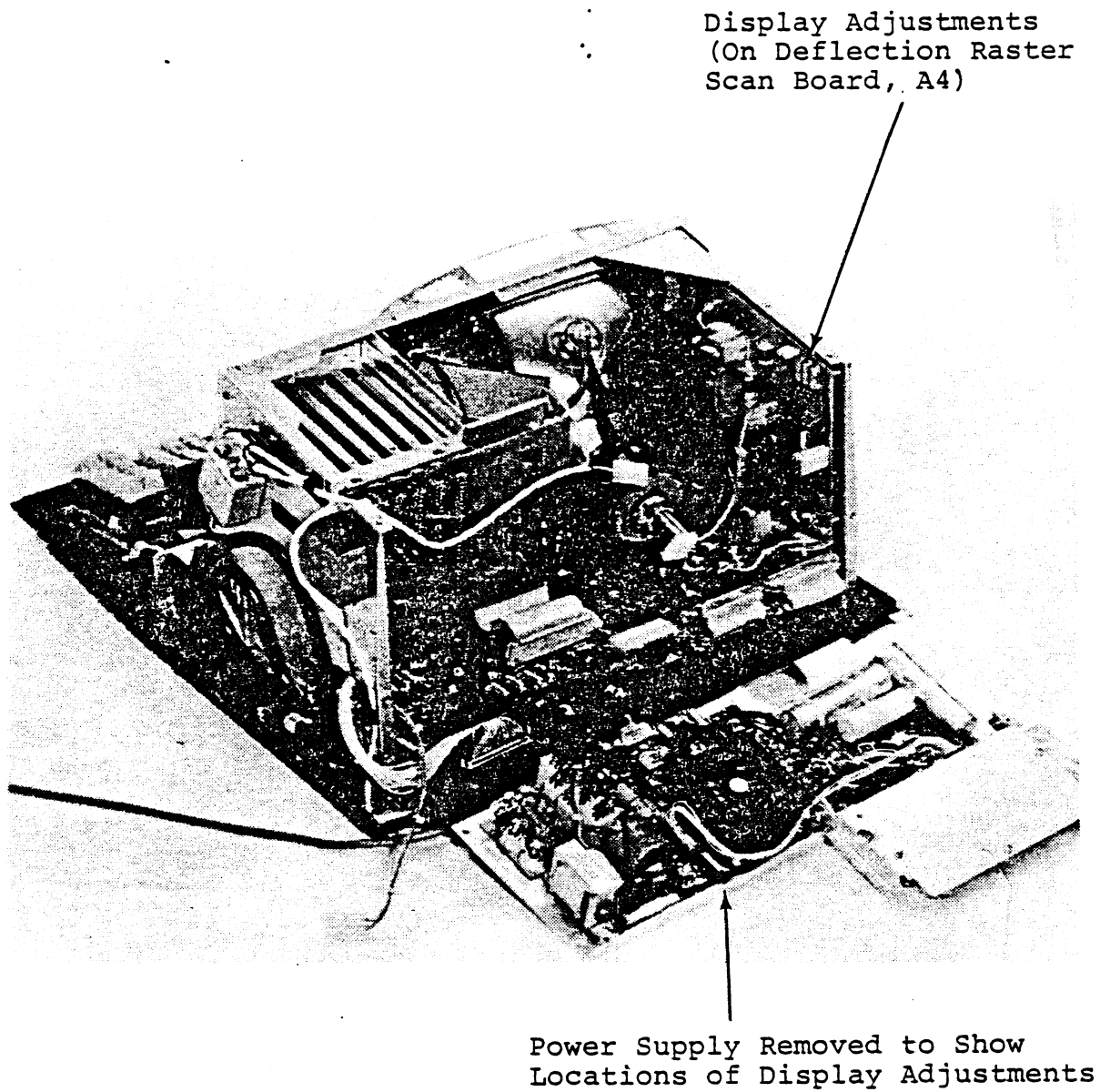


Figure 4-3. 1800 Processor Display Adjustments

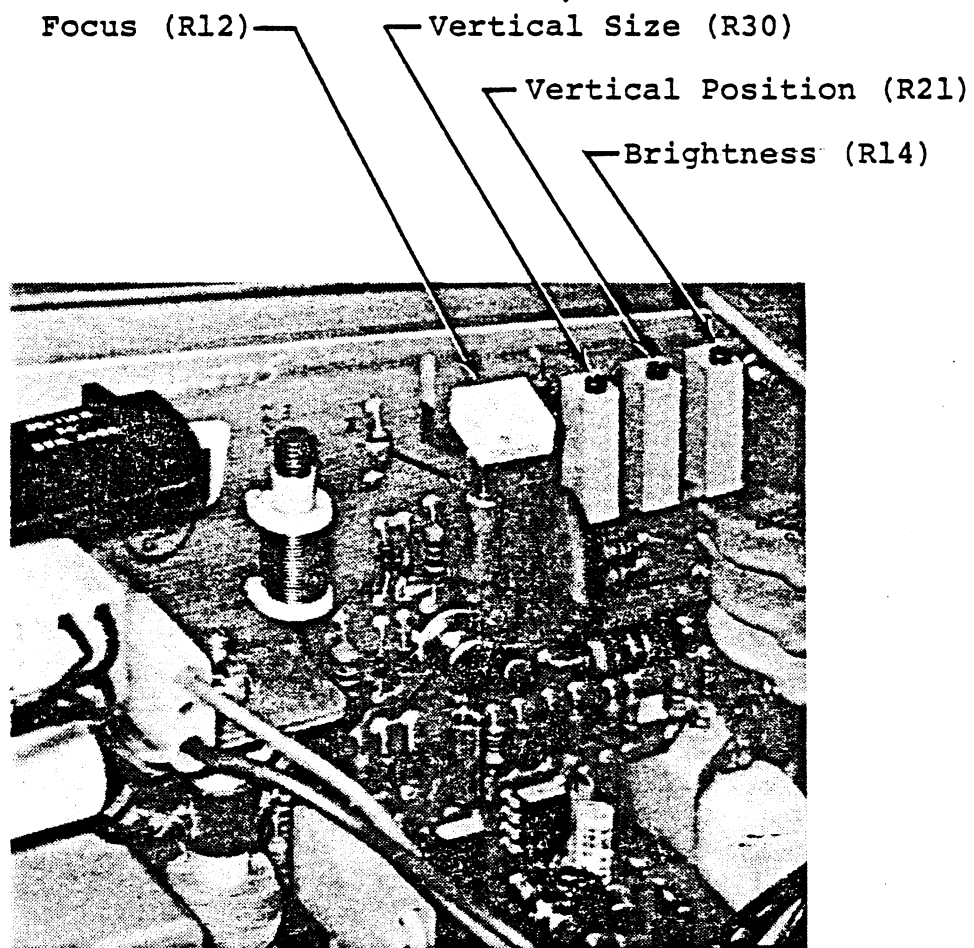


Figure 4-4. Display Adjustment

1. Position power switch to OFF.
 2. Locate inductor L4 on the deflection raster scan board (A4). See Figure 4-5.
 3. Position a correction magnet against the extended edges of the coilform of L4. See Figure 4-6. Temporarily secure the magnet to L4 with a small cable tie.
 4. Position power switch to ON. Repeat step g.
 5. Position power switch to OFF. If linearity is within limits, permanently secure the magnet to L4 with RTV-108 adhesive. If linearity is not within limits add a second magnet (step 3).
 6. Position power switch to ON. Repeat step g.
 7. Position power switch to OFF. If linearity is within limits permanently secure the magnets to L4. If linearity is not within limits repeat the procedures to add a third magnet. If the addition of the third magnet does not bring the linearity within limits refer to Fault Isolation, Paragraph 3.4.1.
- i. Position the power switch to ON.
 - j. Adjust the centering magnets on the deflection yoke to center the display in the viewing area. See Figure 4-7. Move the centering magnets by the tab provided on each magnet. Use caution to avoid contact with the high voltage connection on the CRT. Note: This adjustment may require re-adjustment of the vertical position (step f).
 - k. Adjust variable inductor L5 (Figure 4-5) to set the horizontal width of the display to 7.9 ±0.05 inches.
 - l. Check the alignment of the columns and lines of characters of the display by placing a 5 X 7.9 inch mask on the screen. The four sides of the display should be straight to within ±1/2 character.
 - m. Position power switch to OFF.

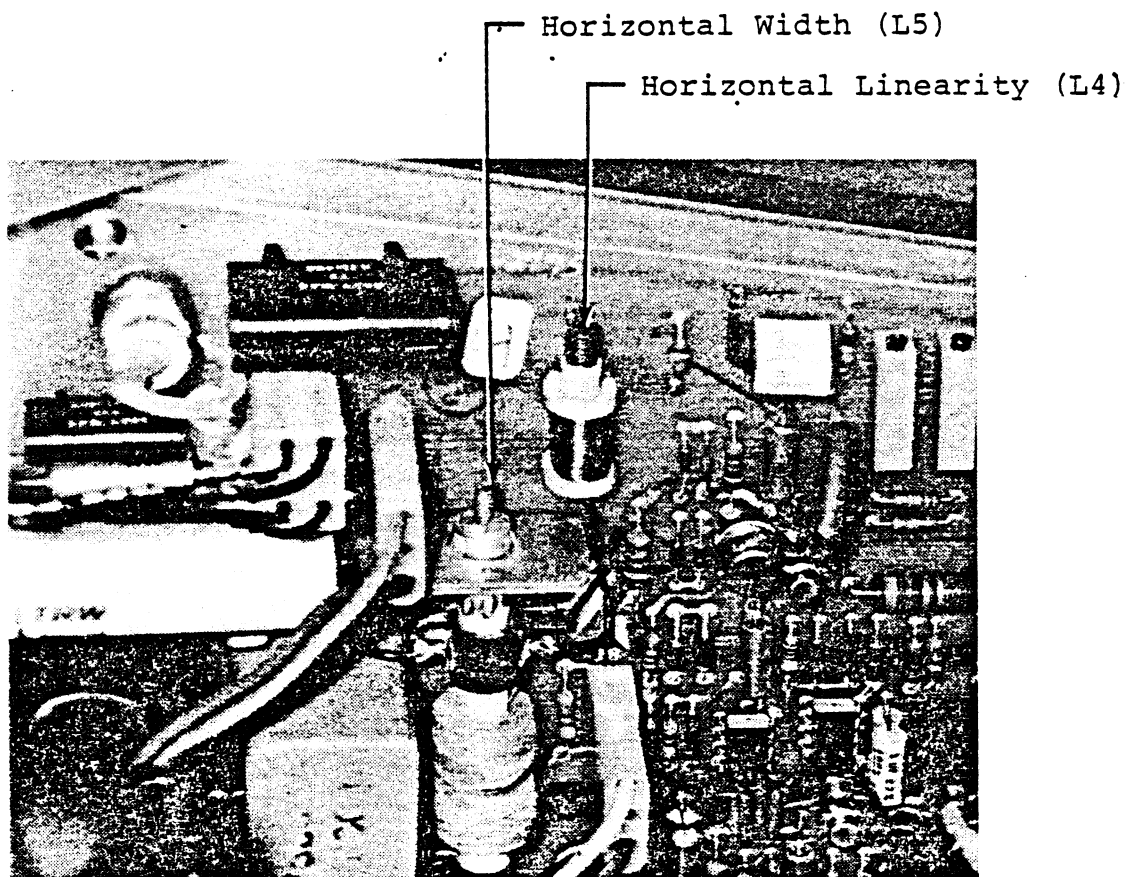


Figure 4-5. Horizontal Adjustments

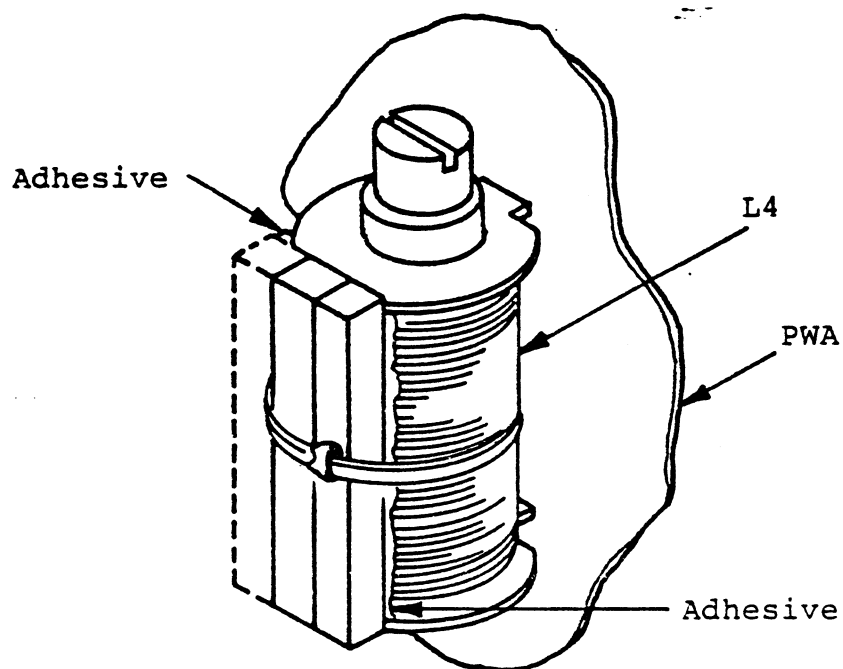
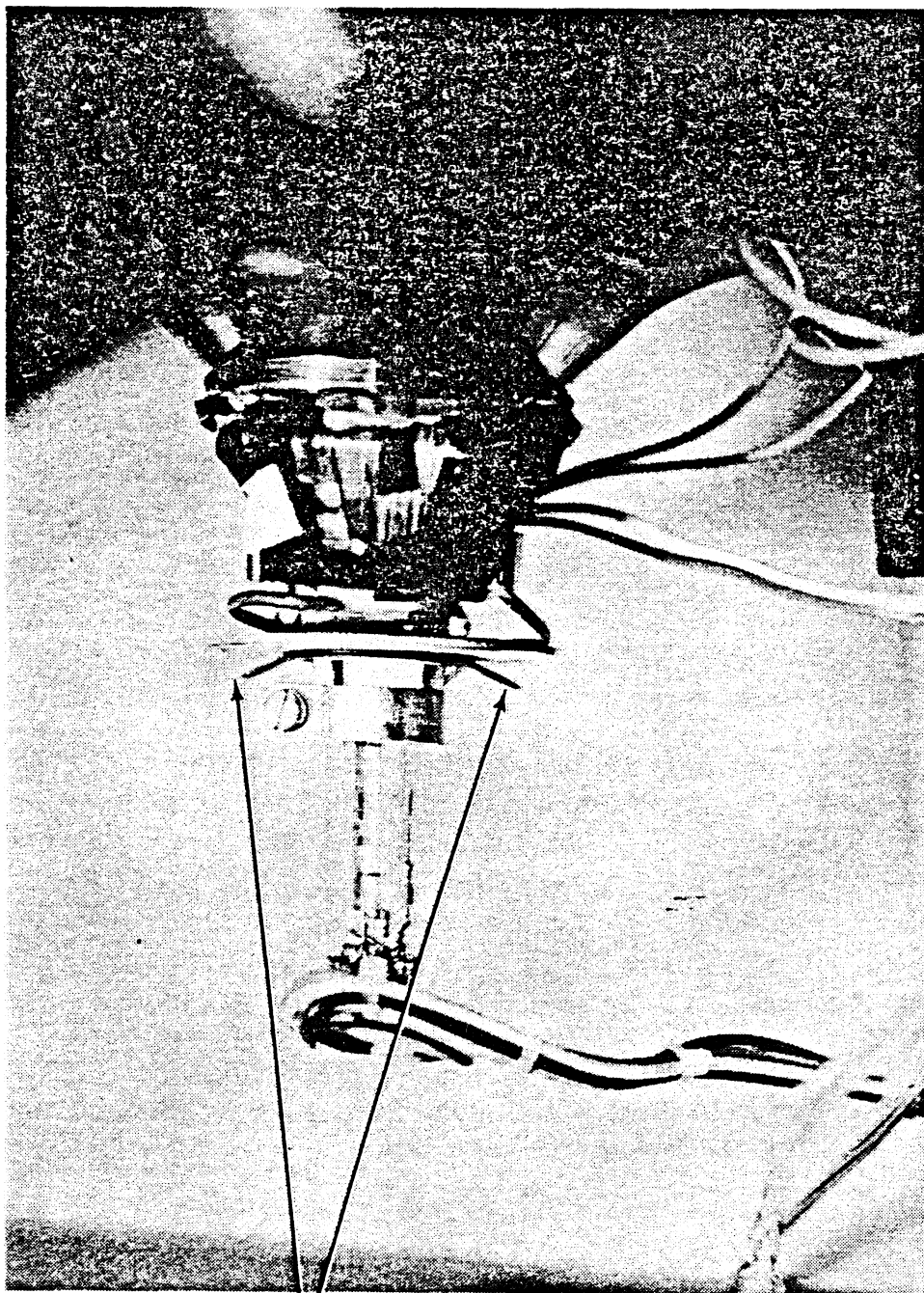


Figure 4-6. Correction Magnet (L4)



Centering Magnets (2)

Figure 4-7. Centering Magnets

SECTION 5

REMOVAL AND REPLACEMENT

5.1 GENERAL

Section 5 contains the procedures for removal and replacement of major assemblies and subassemblies. In some cases it may be necessary to remove an assembly (or subassembly) to gain access to another component. If so, a reference will be made to the paragraph that contains the procedure.

5.2 REMOVABLE KEYBOARD

5.2.1 DETACH KEYBOARD FROM PROCESSOR

The removable keyboard is attached to the lower front of the processor cabinet with two spring latches (one latch at each end of the keyboard). The keyboard, when detached, may be moved from the processor the length of the keyboard cable which is approximately one meter (Figure 5-1).

- a. To detach keyboard, press release button next to each latch and pull keyboard from processor cabinet.
- b. To attach keyboard, push keyboard cable into processor cabinet and slide keyboard spring latches into recesses in processor cabinet until latches catch.
- c. If keyboard is difficult to attach or detach to processor, or if keyboard is loose when attached to processor, then adjust keyboard latches (Paragraph 5.2.5).

5.2.2 KEYBOARD COVER

The keyboard cover is secured to the base plate by two screws (one screw at each end of the keyboard), see Figure 5-1.

- a. Detach keyboard from processor (Paragraph 5.2.1).
- b. From bottom of keyboard, remove two screws securing keyboard cover to base plate and remove keyboard cover.
- c. To install cover, place cover on base plate and secure with two screws.

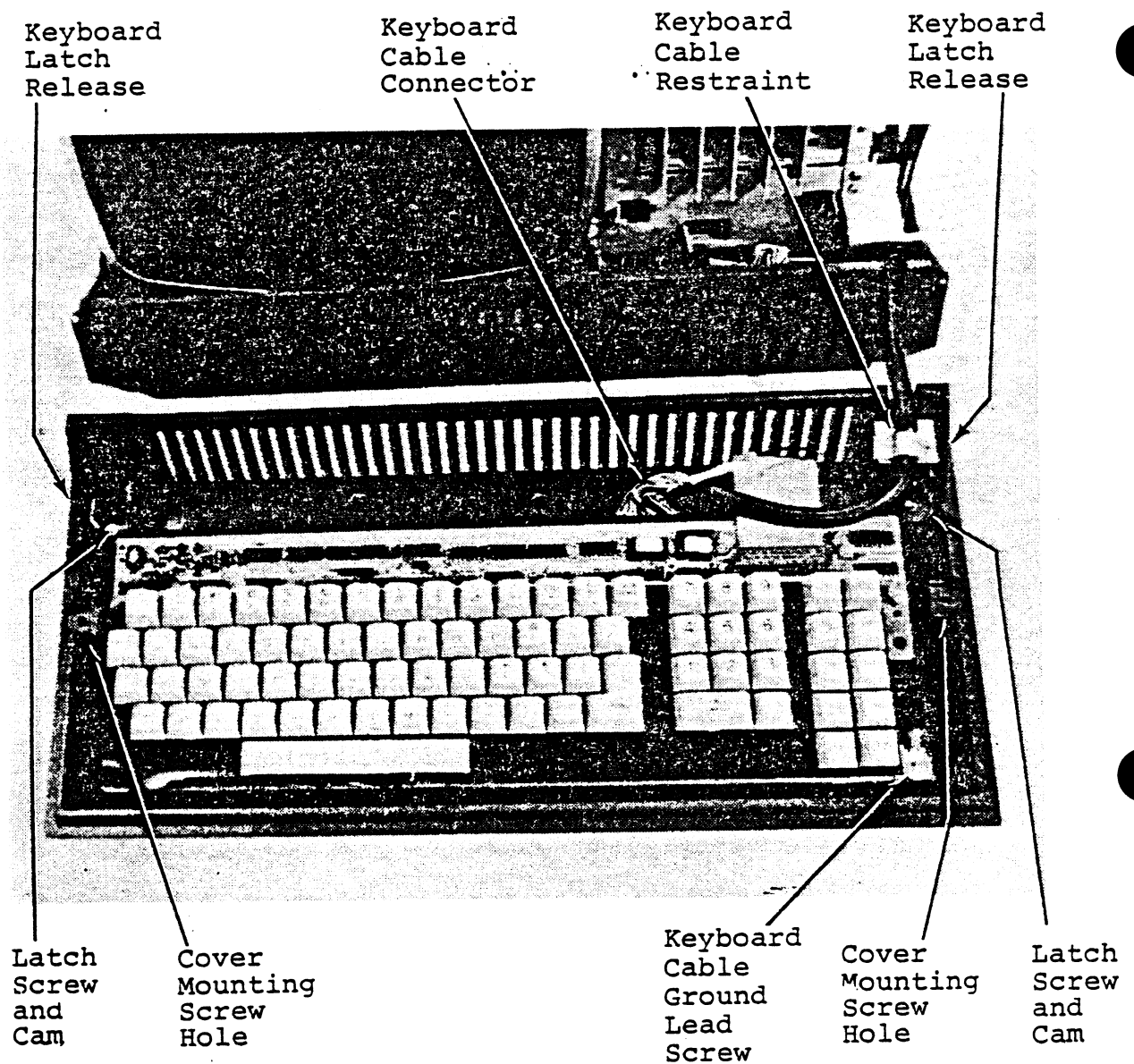


Figure 5-1. Keyboard Removal

- d. If keyboard was attached to processor, then attach keyboard to processor.

5.2.3 KEYBOARD ASSEMBLY

The keyboard assembly is mounted on the keyboard base plate with four screws (two screws at each end of the keyboard), see Figure 5-1.

- a. Remove all power from processor.
- b. Detach keyboard from processor (Paragraph 5.2.1).
- c. Remove keyboard cover (Paragraph 5.2.2).
- d. At cable entrance to keyboard, remove cable restraint (secured with one screw).
- e. Tilt keyboard to gain access to bottom of base plate. Remove four screws securing keyboard to base plate and remove keyboard assembly from base plate.
- f. At lower right edge of keyboard, remove keyboard cable ground lead (secured with one screw).
- g. Disconnect keyboard cable from keyboard assembly.
- h. To install keyboard assembly, position keyboard assembly on base plate and secure with four screws.
- i. Connect keyboard cable to keyboard assembly.
- j. At cable entrance to keyboard, secure cable with cable restraint and one screw.
- k. At lower right edge of keyboard, install keyboard cable ground lead with one screw.
- l. Replace keyboard cover.
- m. Check operation of keyboard keys for alignment with keyboard cover. If keys rub against cover, adjust keyboard alignment by loosening four keyboard assembly mounting screws (bottom on keyboard) and sliding keyboard so keys do not rub. Tighten keyboard mounting screws.

n. If keyboard was attached to processor, then attach keyboard to processor.

o. Power up processor.

5.2.4 DIRECT BUFFER BOARD

The direct buffer board is mounted to the bottom of the keyboard assembly with two screws.

a. Remove all power from processor.

b. Detach keyboard from processor (Paragraph 5.2.1).

c. Remove keyboard cover (Paragraph 5.2.2).

d. Remove keyboard assembly from base plate (Paragraph 5.2.3).

e. Disconnect keyboard cable from direct buffer board.

f. From bottom of keyboard assembly, remove two screws securing direct buffer board to keyboard assembly and remove direct buffer board.

g. To install direct buffer board, position direct buffer board on keyboard assembly and secure with two screws.

h. Connect keyboard cable to direct buffer board.

i. Install keyboard assembly to base plate.

j. Replace keyboard cover.

k. If keyboard was attached to processor, then attach keyboard to processor.

l. Power up processor.

5.2.5 KEYBOARD LATCH ADJUSTMENT

The keyboard is held to the processor base with two keyboard latches. To ensure that the keyboard can be easily attached and detached from the processor and to ensure that the keyboard contains no noticeable looseness when attached to the processor, the keyboard latches must be adjusted. The latches are located at the rear of either end of the keyboard base (Figure 5-1).

- a. Detach keyboard from processor (Paragraph 5.2.1).
- b. Remove keyboard cover (Paragraph 5.2.2).
- c. Loosen latch screw (Figure 5-1).
- d. Rotate latch cam (with pliers or wrench) for maximum retraction of latch hook into keyboard (Figure 5-1).
- e. Insert keyboard into processor base.
- f. Press or hold keyboard and processor bases together with hand or fingers and rotate latch cam until latch hook seats into processor base.

NOTE

The keyboard latch is properly adjusted when the following three conditions hold:

- (1) The force needed to depress the latch pushbuttons should be approximately the same for the attached keyboard. The latch should not hang or exhibit any drag on the processor base.
 - (2) When attaching keyboard to processor, the latch hooks should seat into the processor base without excessive force on the keyboard.
 - (3) There should be no noticeable play between the processor and attached keyboard.
- g. Check keyboard latch adjustment by detaching and attaching keyboard to processor. Also check for play between keyboard and processor when keyboard is attached.
 - h. If keyboard does not properly attach to processor, then with keyboard attached to processor, rotate latch cam to tighten or loosen keyboard to processor as required. Repeat step g.
 - i. Tighten latch screw.
 - j. Replace keyboard cover.
 - k. If keyboard was attached to processor, then attach keyboard to processor.

5.3 PROCESSOR

5.3.1 HOUSING

The processor housing is secured to the base plate by two 1/4 turn fasteners.

- a. Release two 1/4 turn fasteners located at the lower edge of the processor base plate on each side of the processor.
- b. Lift the housing straight up from the base plate.
- c. Install the housing by positioning the housing on the base plate. Ensure the housing is clear of wiring and connectors. Secure housing with the two quarter turn fasteners.

5.3.2 MEMORY BOARDS

The five memory boards are located in the memory bay behind the processor front panel (Figure 5-2).

- a. Remove processor cover (Paragraph 5.3.1).
- b. Remove boards by pulling boards straight out from the memory bay.
- c. Replace boards with component side to the left by pushing boards down guides until connector seats.
- d. Replace processor cover.

5.3.3 PROCESSOR/EMULATION AND DISPLAY-I/O BOARDS

The processor/emulation and display-I/O boards are the two large boards located in the lower part of the processor. The display-I/O board is on top and the processor/emulation board is on the bottom.

- a. Remove all power from the processor.
- b. At the left rear of the processor at the rear connector panel (Figure 5-3) disconnect I/O cables from J1, J6, and J7.
- c. At the left rear of the processor, loosen two screws and remove the rear connector panel.

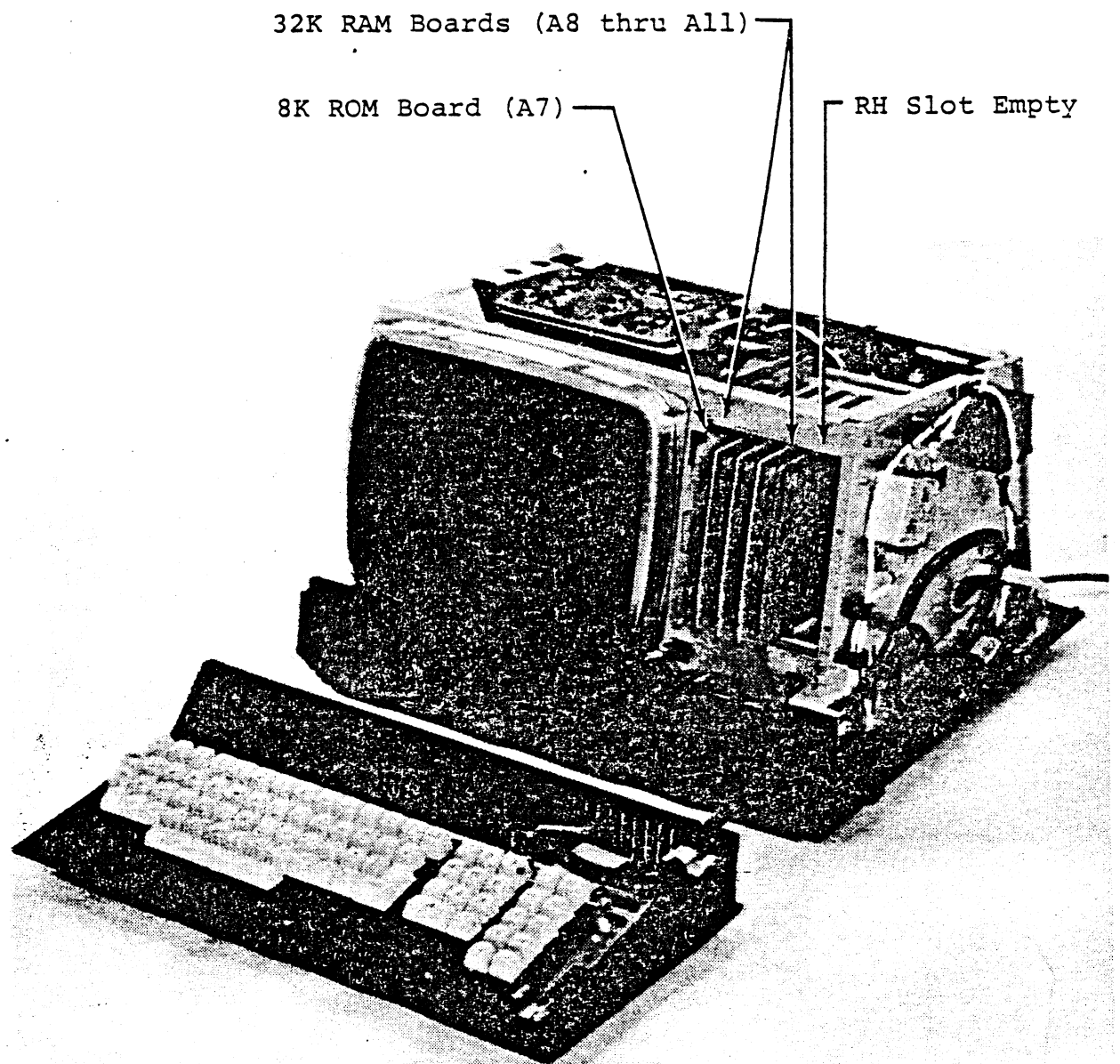


Figure 5-2. Memory Boards Removal

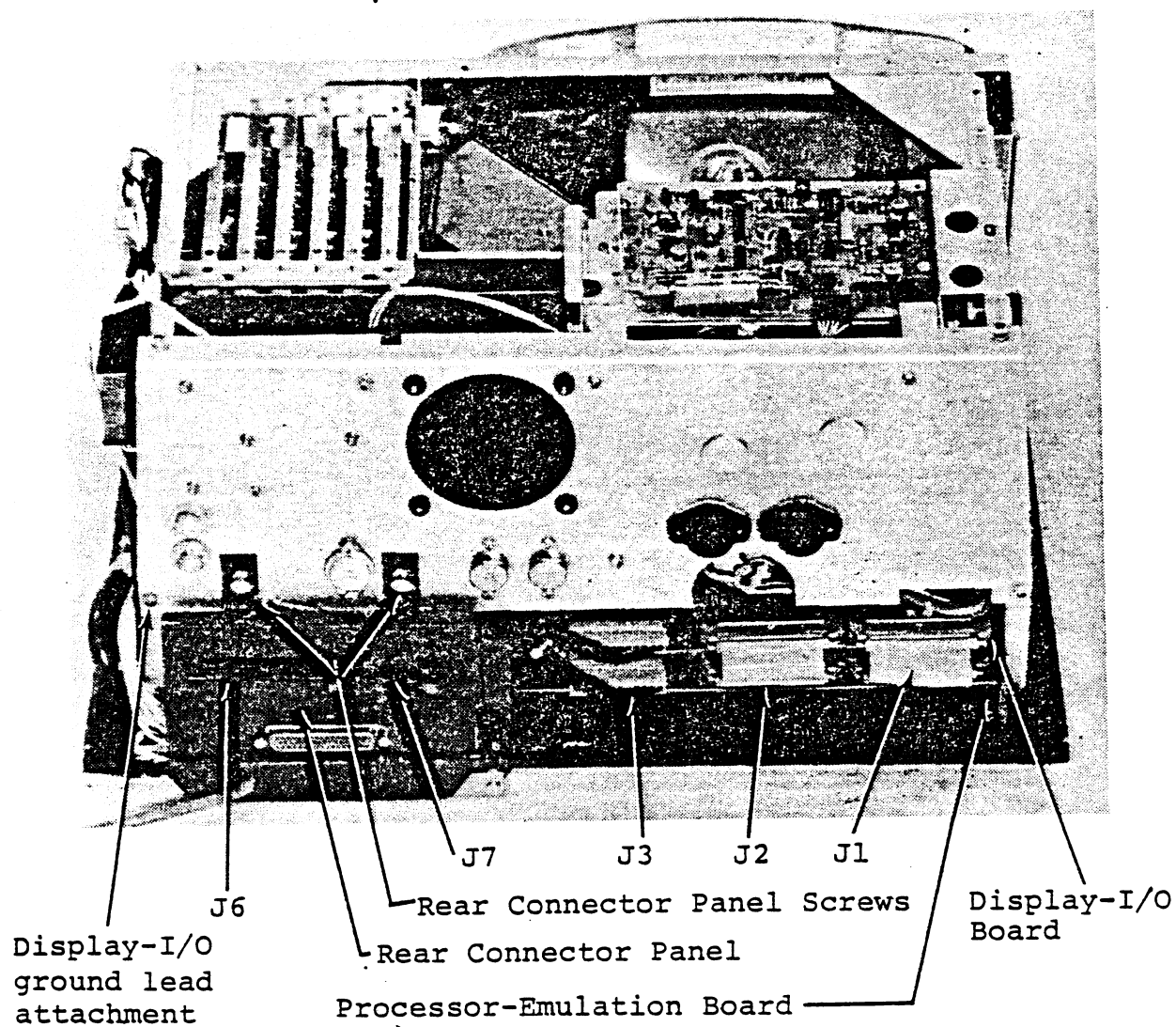


Figure 5-3. Processor/Emulation Board

- d. On the processor/emulation board, disconnect J1, J2, and J3.
- e. On the display-I/O board (Figure 5-4), disconnect J1 thru J5, J8, J9, and J11.
- f. Remove two ground leads to display-I/O board from the lower left mounting screw of power panel (Figure 5-3).
- g. Remove boards by pulling boards straight out from the processor.
- h. Replace boards with component side up by pushing boards down guides until boards seat. The processor/emulation board goes in the lower slot. The display-I/O board goes in the upper slot.
- i. Attach two ground leads from display-I/O board to the lower left mounting screw of power panel.
- j. On the processor/emulation board, connect J1, J2, and J3.
- k. On the display-I/O board, connect J1 thru J5, J8, J9, and J11.
- l. Replace the rear connector panel with two screws.
- m. At the left rear of the display-I/O board (at the rear connector panel), connect I/O cables to J1, J6, and J7.
- n. Power up processor.

5.3.4 MEMORY MOTHERBOARD

The memory motherboard is mounted on the rear of the processor memory bay with four Phillips screws. See Figures 5-5 and 5-6.

- a. Remove all power from processor.
- b. On the memory motherboard, disconnect J1.
- c. On display I/O board, disconnect P2/J3.
- d. Remove all memory boards.

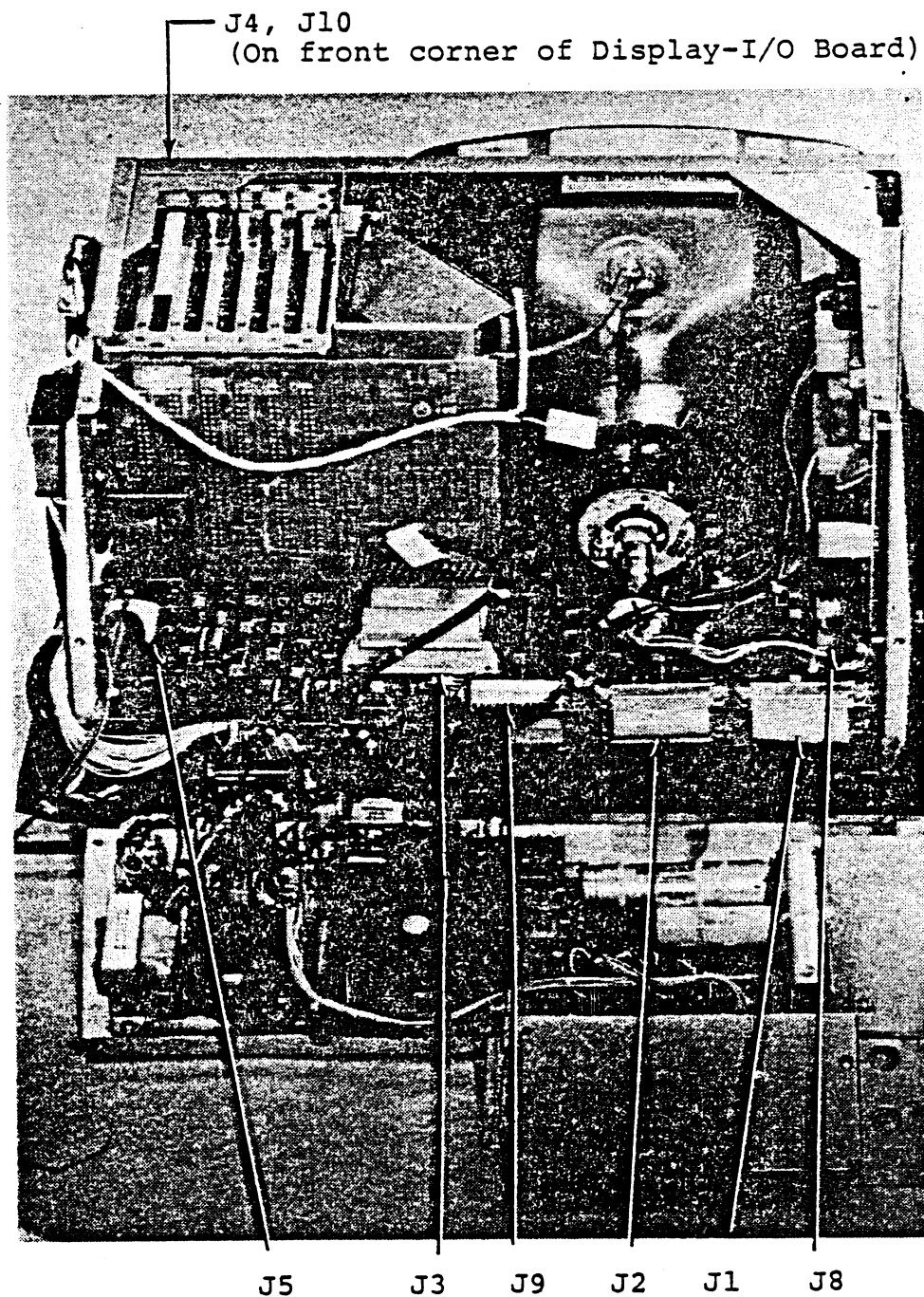


Figure 5-4. Display-I/O Board

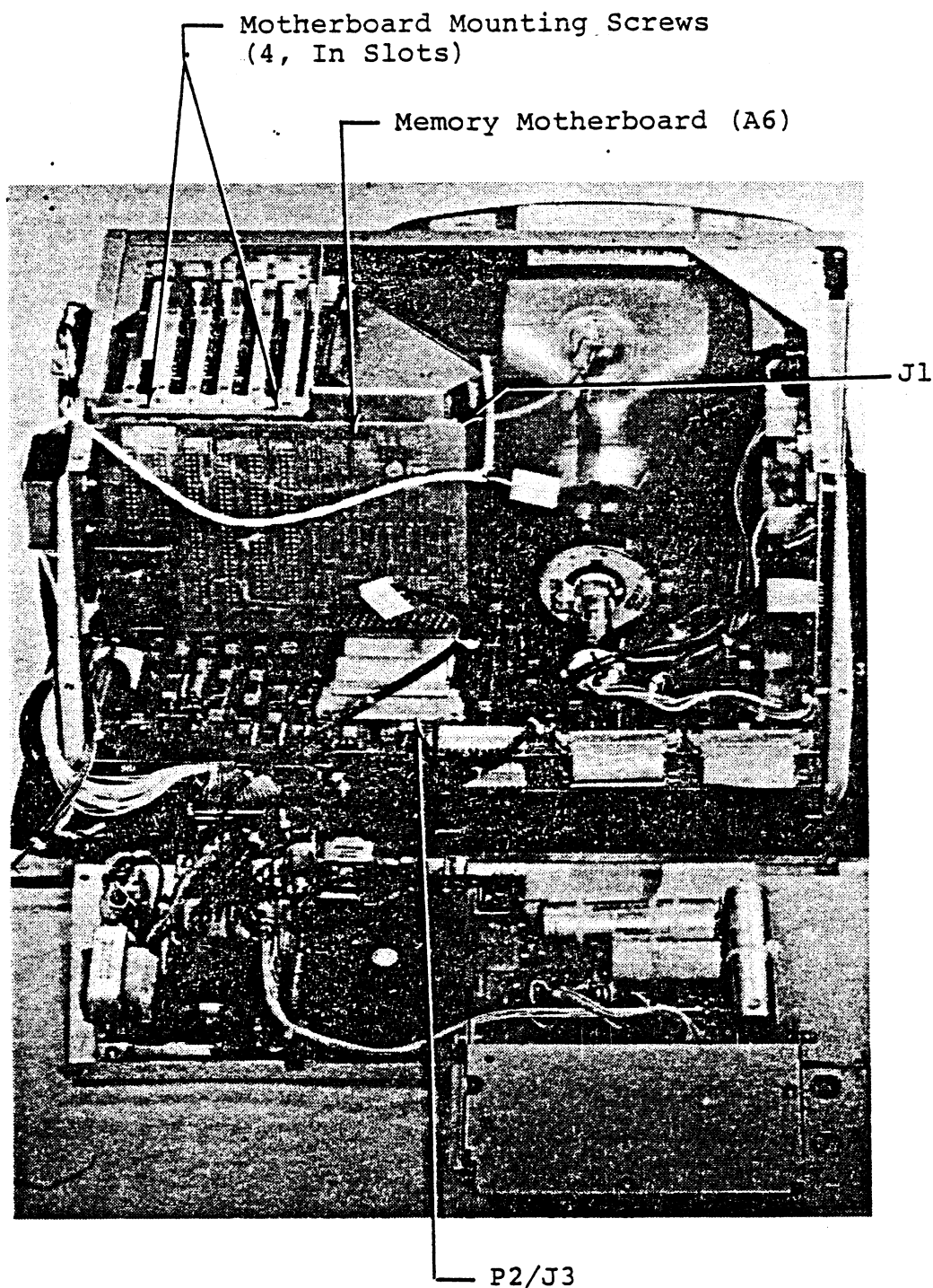


Figure 5-5. Memory Motherboard

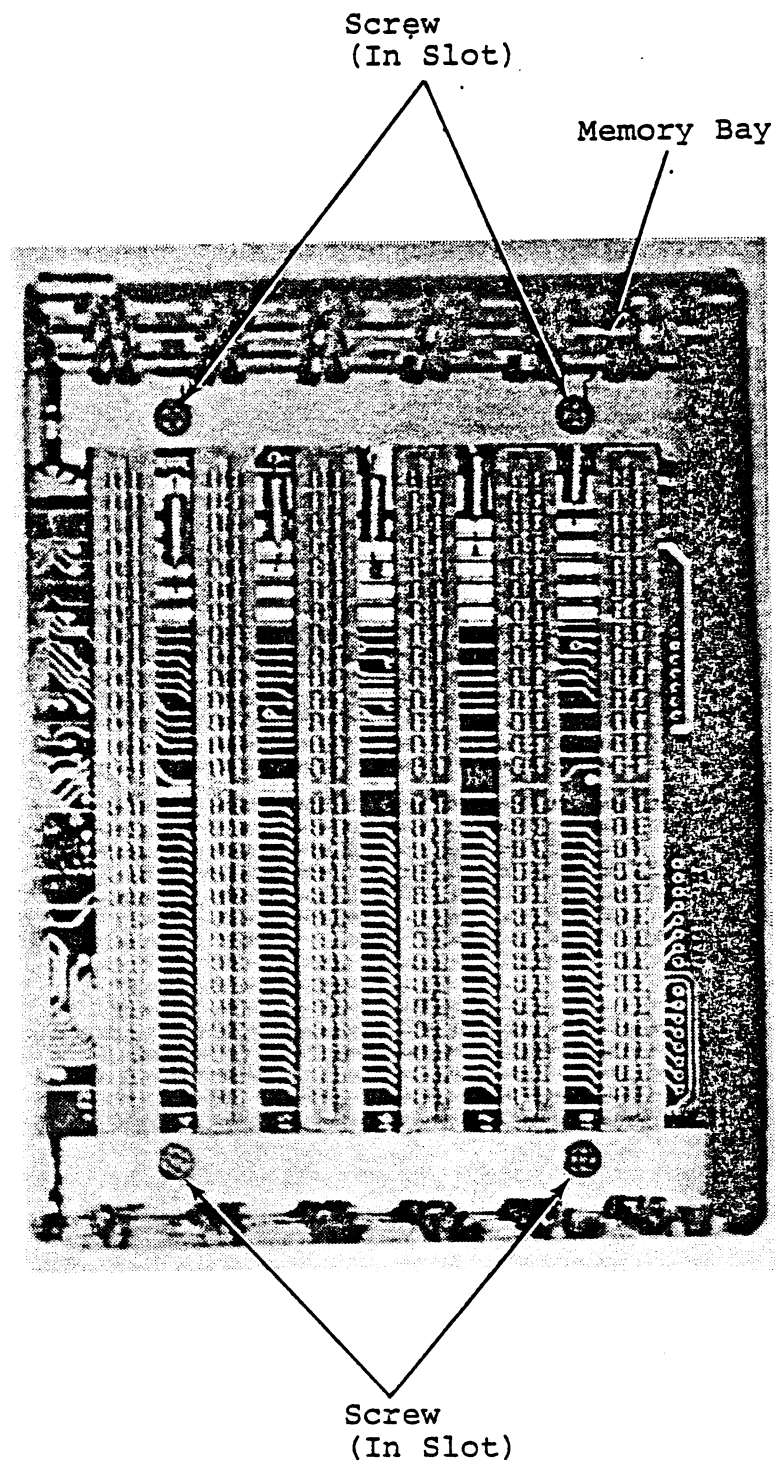


Figure 5-6. Memory Motherboard Mounting Screws
(View thru Memory Bay)

- e. At inside rear of memory bay, loosen (do not remove) four phillips screws on the motherboard.
- f. Slide motherboard up until screws slide out of slots.
- g. Install motherboard by inserting the four mounting screws in the slots at rear of memory bay. Tighten screws.
- h. Install all memory boards.
- i. On the motherboard, connect J1.
- j. On display I/O board, connect P2/J3.
- k. Power up processor.

5.3.5 DEFLECTION RASTER SCAN BOARD

The deflection raster scan board is mounted on the left side plate of the processor with four Allen head screws (See Figure 5-7).

- a. Remove all power from processor.
- b. Remove power panel from processor (Paragraph 5.3.10).
- c. Disconnect the yoke cable connectors at J8 and J9 on the deflection board.
- d. Disconnect the power supply cable connector at J6 and the flyback transformer cable connector at J7 on the deflection board.
- e. Disconnect P10 from the base of the CRT and P5/J8 from the processor/emulator board.
- f. Remove the four Allen head screws that secure the assembly to the left side of the terminal. Carefully lift the board assembly out of the top of the terminal.
- g. Position the replacement assembly in the terminal and secure with the four mounting screws.
- h. Install connector P5/J8 on the display-I/O board and P10 on the CRT.

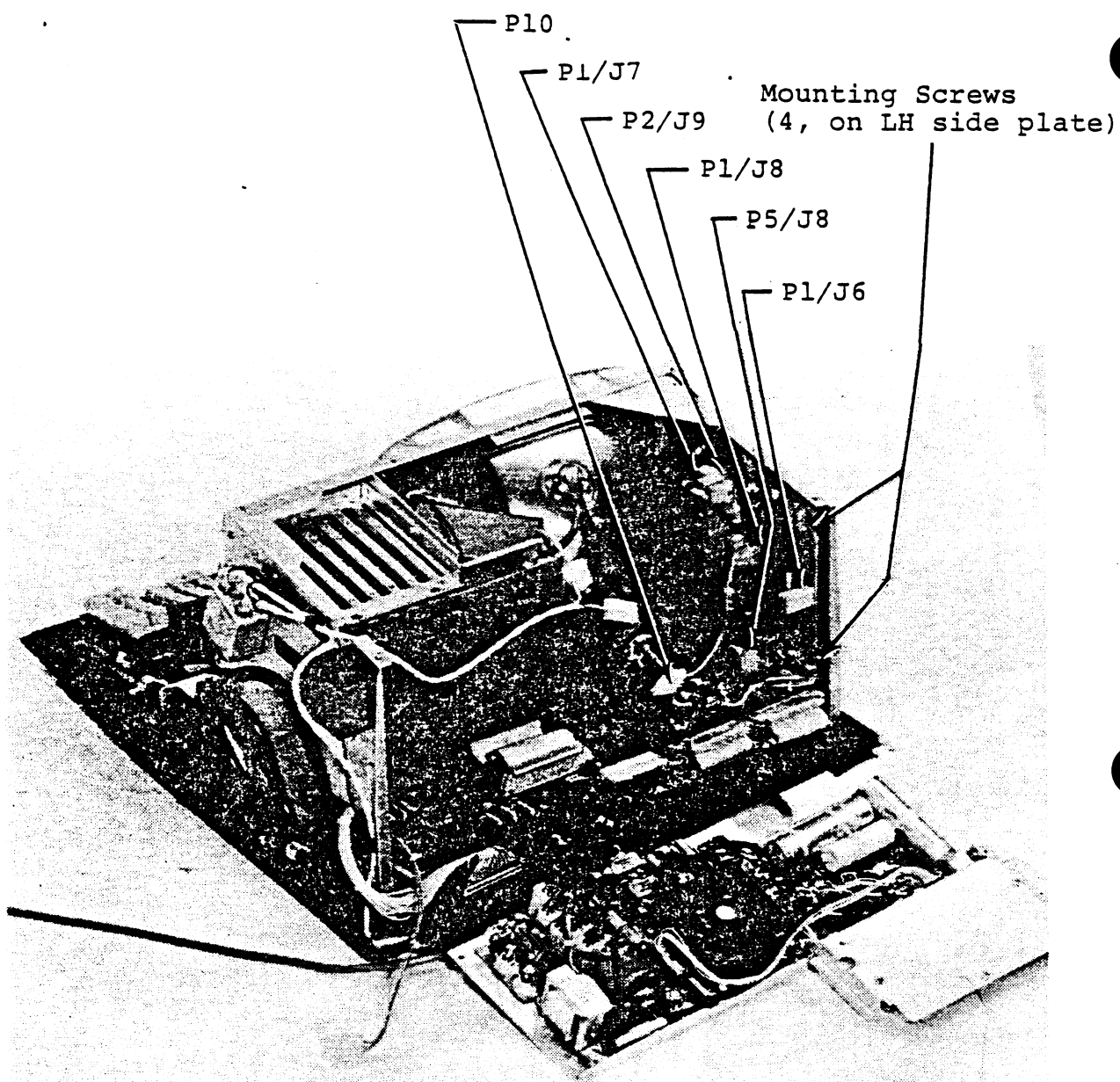


Figure 5-7. Deflection Raster Scan Board

- i. Install connectors J6, J7, J8 and J9 on the deflection board assembly.
- j. Replace power panel.

5.3.6 FLYBACK TRANSFORMER

The flyback transformer is mounted on the flyback transformer bracket with two retaining nuts. The assembly is located at the left rear of the memory card bay. See Figure 5-8.

- a. Remove all power from processor.

CAUTION

Before attempting to remove the Flyback Transformer Assembly, ensure that the post accelerator has been discharged by shorting the post accelerator connection to ground. The post accelerator connector is located under the rubber cap on top of the CRT. Use extreme caution in grounding this connection because a 12K volt potential may be present.

- b. Discharge the post accelerator by carefully slipping the blade of a common screwdriver under the rubber cap and grounding the shank of the screwdriver to the chassis.
- c. Disconnect the high voltage lead spring clip connector (under the rubber-cap) from the CRT.
- d. Disconnect the flyback transformer cable at J7 on the deflection board.
- e. Remove flyback transformer assembly by removing two mounting screws on flyback transformer housing.
- f. Position replacement transformer assembly on the mounting bracket and secure with the two screws.
- g. Reconnect high voltage lead to CRT and transformer cable at J7 on deflection board.
- h. Power up processor.

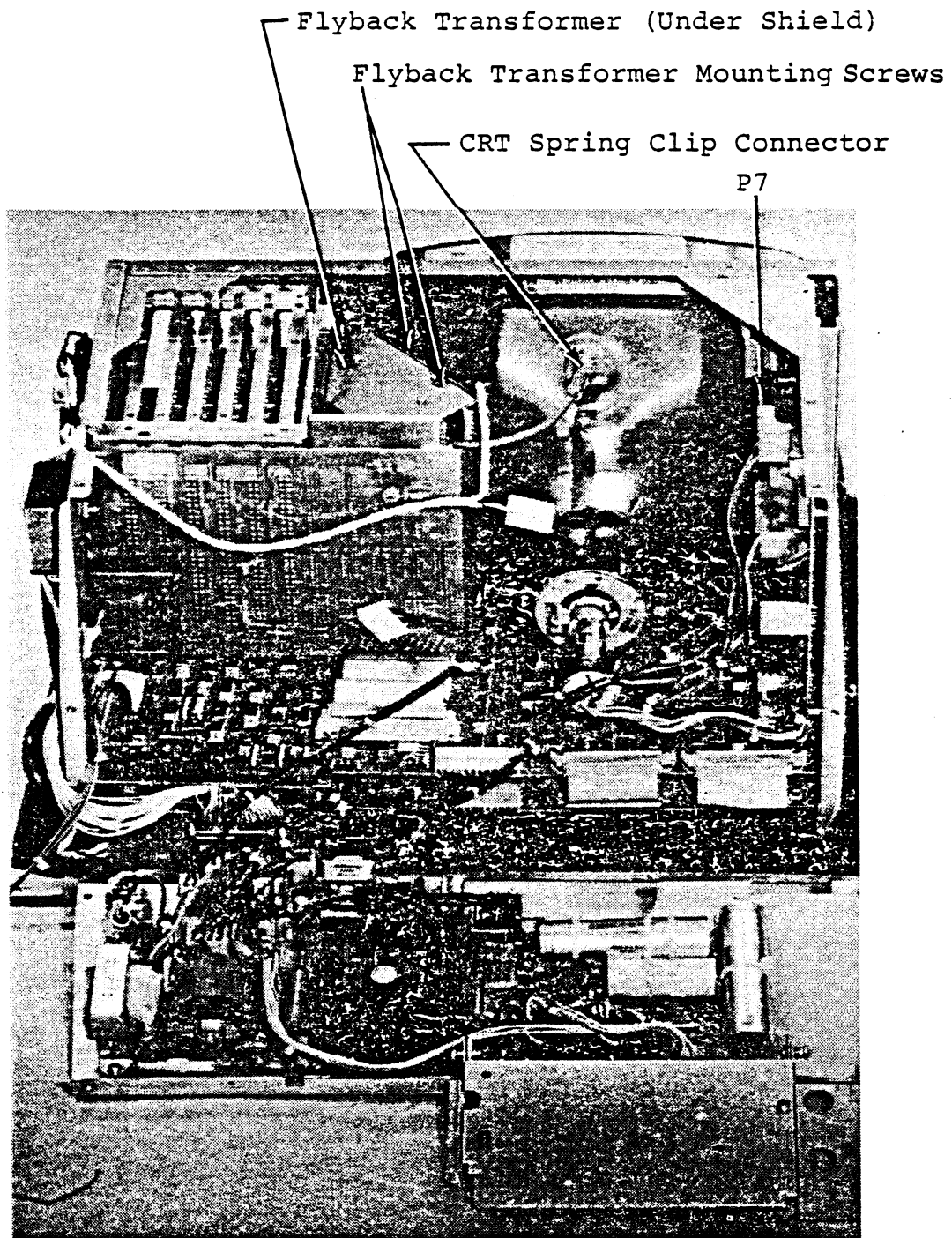


Figure 5-8. Flyback Transformer

5.3.7 CRT/YOKE ASSEMBLY

- a. Remove all power from processor.

CAUTION

Before attempting to remove the CRT/yoke Assembly, ensure that the post accelerator has been discharged by shorting the post accelerator connection to ground. The post accelerator connector is located under the rubber cap on top of the CRT. Use extreme caution in grounding this connection because a 12K volt potential may be present.

- b. Discharge the post accelerator by carefully slipping the blade of a common screwdriver under the rubber cap and grounding the shank of the screwdriver to the chassis. See Figure 5-9.
- c. Disconnect the spring clip connector (under the rubber cap) from the CRT.
- d. Disconnect connector P10 from the base of the CRT.
- e. Disconnect the yoke cable connectors at J8 and J9 on the deflection board.

NOTE

To remove the CRT, the processor chassis must be raised to allow the CRT to clear the front edge of the base plate.

- f. Loosen or remove four screws holding processor chassis to base plate and prop up chassis to allow removal of CRT.

CAUTION

Use extreme caution in handling the CRT to avoid breakage.

- g. Remove the four Allen head screws from the front of the tube holder. Move the CRT, with the yoke assembly, forward and out of the terminal.

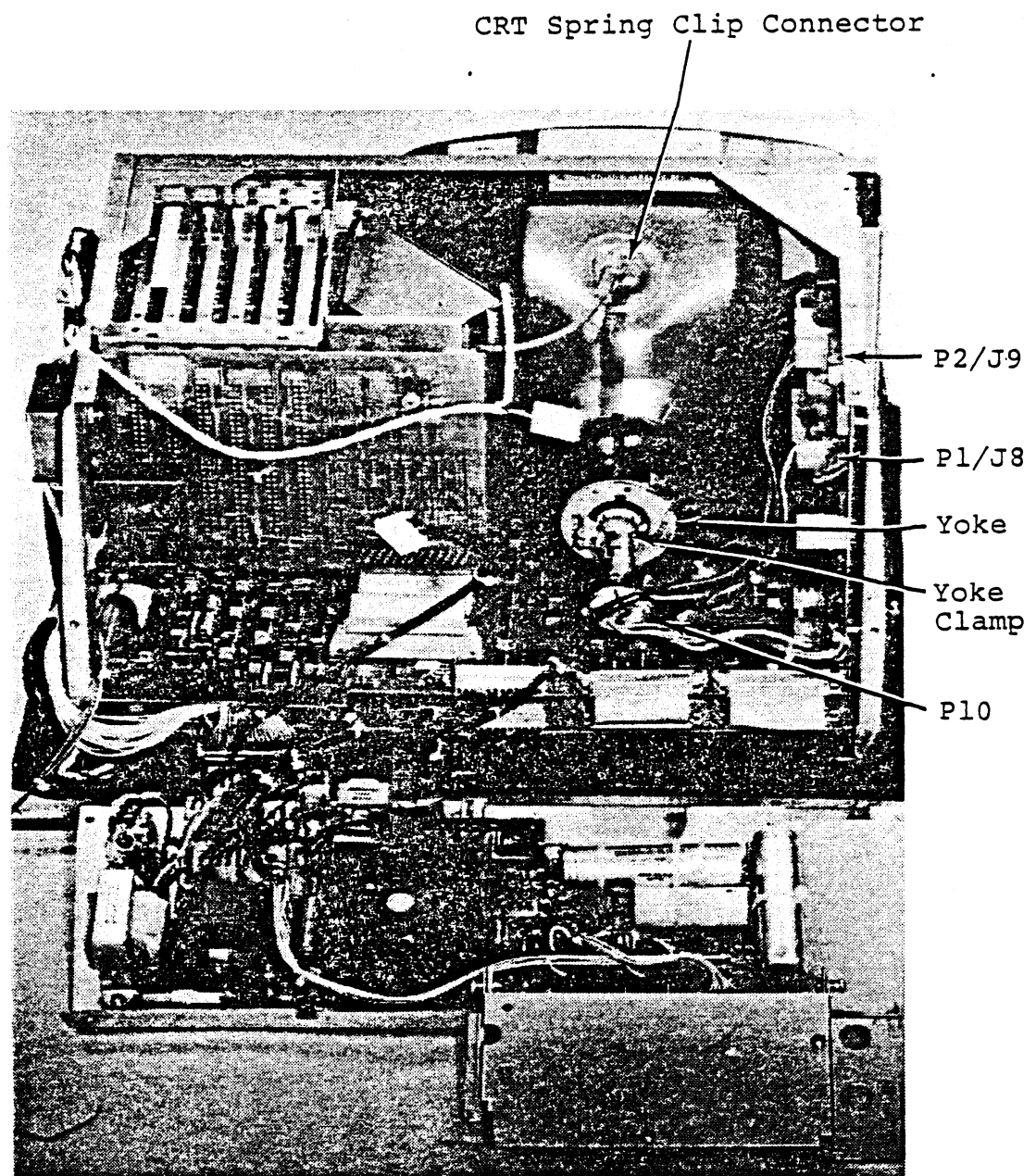


Figure 5-9. CRT/Yoke Assembly

- h. Remove the yoke assembly from the CRT as follows:
 - (1) Remove the adhesive (RTV-108) that bonds the front of the yoke to the CRT.
 - (2) Loosen the yoke clamp screw and slide the yoke assembly from the neck of the tube.
- i. Install the yoke assembly on the replacement CRT as follows:
 - (1) Position the yoke on the CRT. The yoke should be positioned so that the sector where the leads come out of the yoke is at the bottom of the neck (down).

CAUTION

Do not over-tighten the yoke clamp.

- (2) Slowly tighten the yoke clamp screw until the clamp restricts movement of the yoke.
 - (3) Bond the yoke to the tube with adhesive. Apply a fillet of RTV-108 approximately 1-1/4 inch long by 3/8 inch wide to the front of the yoke.
- j. Position the replacement CRT in the terminal and install the four mounting screws in the tube holder.
- k. Lower processor chassis and install and/or tighten four screws holding chassis to base plate.
- l. Connect yoke cable connectors at J8 and J9 on the deflection board.
- m. Install connector P10 on the base of the CRT.
- n. Install spring clip connector to CRT.
- o. Align display (Paragraph 4.3).

5.3.8 CONTROL TRANSFORMER

The control transformer is attached inside the processor RH side plate by two screws. See Figure 5-10.

- a. Remove all power from processor.

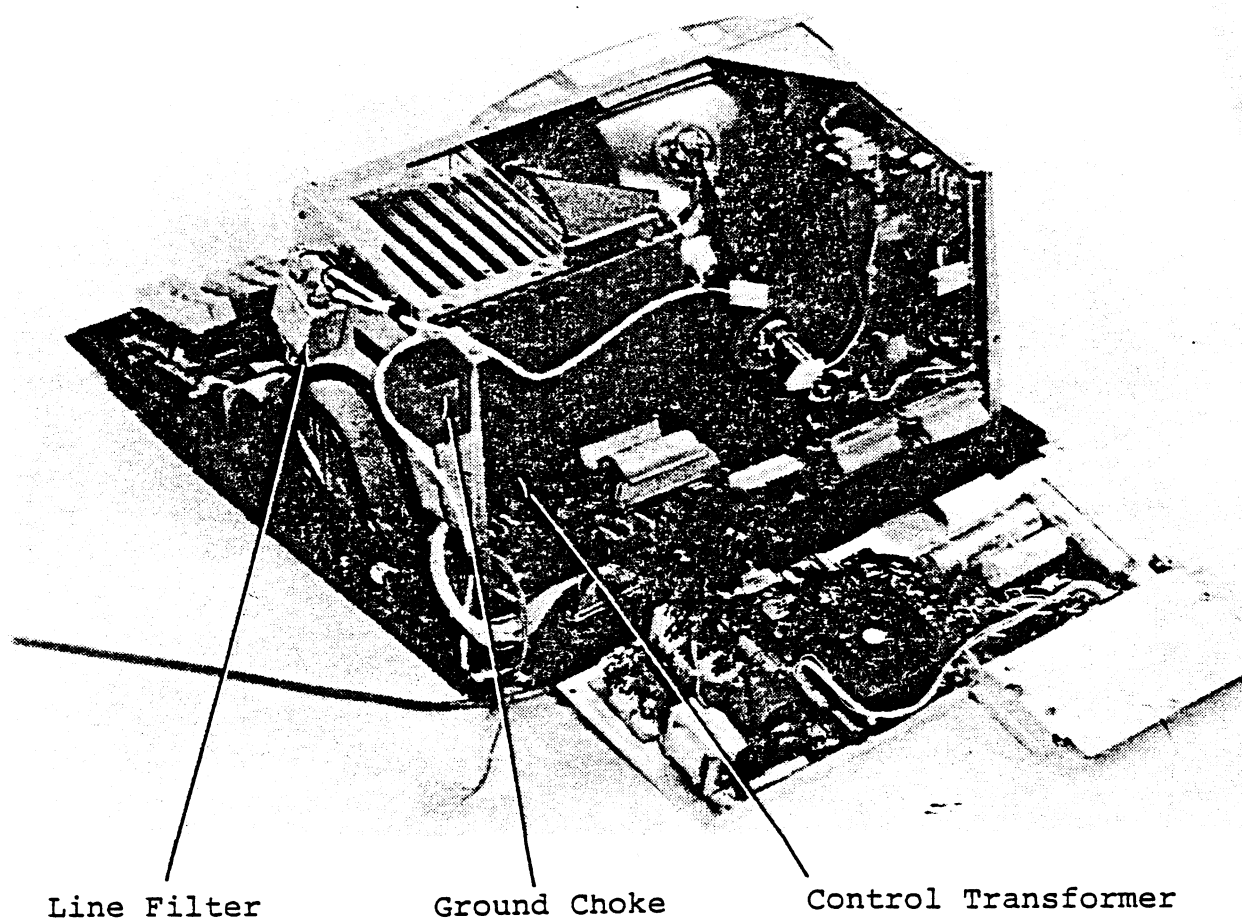


Figure 5-10. Control Transformer and Line Filter Removal

- b. Remove power panel from processor (Paragraph 5.3.10).
- c. Remove two screws that hold the transformer to the processor RH side plate.
- d. Install transformer by inserting two screws thru transformer and into the processor RH side plate.
- e. Replace power panel.
- f. Power up processor.

5.3.9 LINE FILTER

The line filter is attached to the processor RH side plate by two screws (Figure 5-10).

- a. Remove all power from processor.
- b. Disconnect soldered leads to the line filter.
- c. Remove line filter from processor side plate.
- d. Install new line filter to processor side plate.
- e. Solder leads to line filter.
- f. Power up processor.

5.3.10 POWER PANEL

The power panel is attached to the top rear of the processor by five Allen head screws (Figure 5-11). For power supply connections see Figure 5-12.

- a. Remove all power from processor.
- b. Loosen two screws and remove rear connector panel.
- c. Remove five Allen head screws (two at left end and three at right end of panel) and lift panel from processor.
- d. Disconnect following connectors from secondary regulator board:
 - (1) P12 to memory motherboard.
 - (2) P19 to display I/O board.

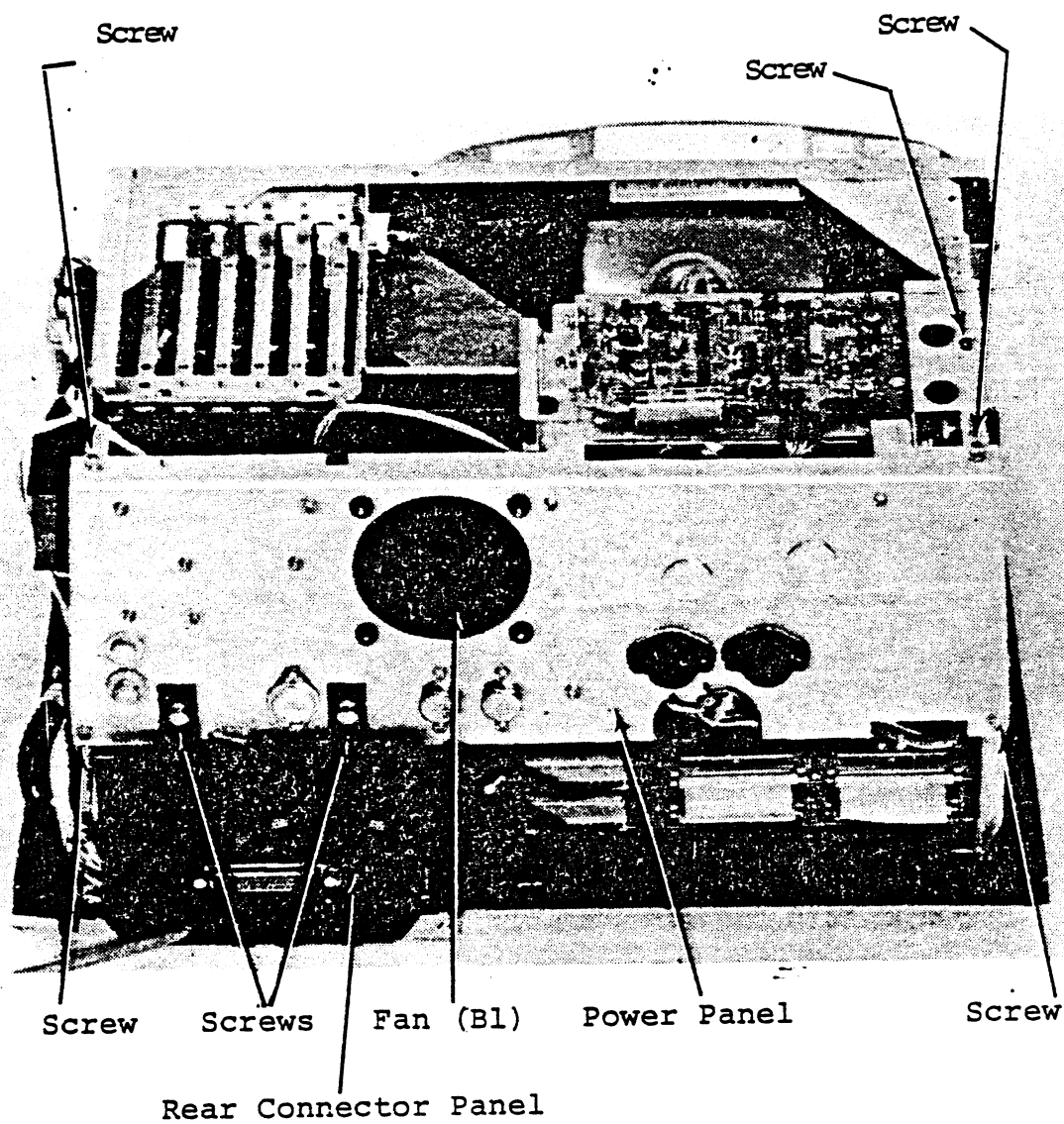


Figure 5-11. Power Panel and Fan

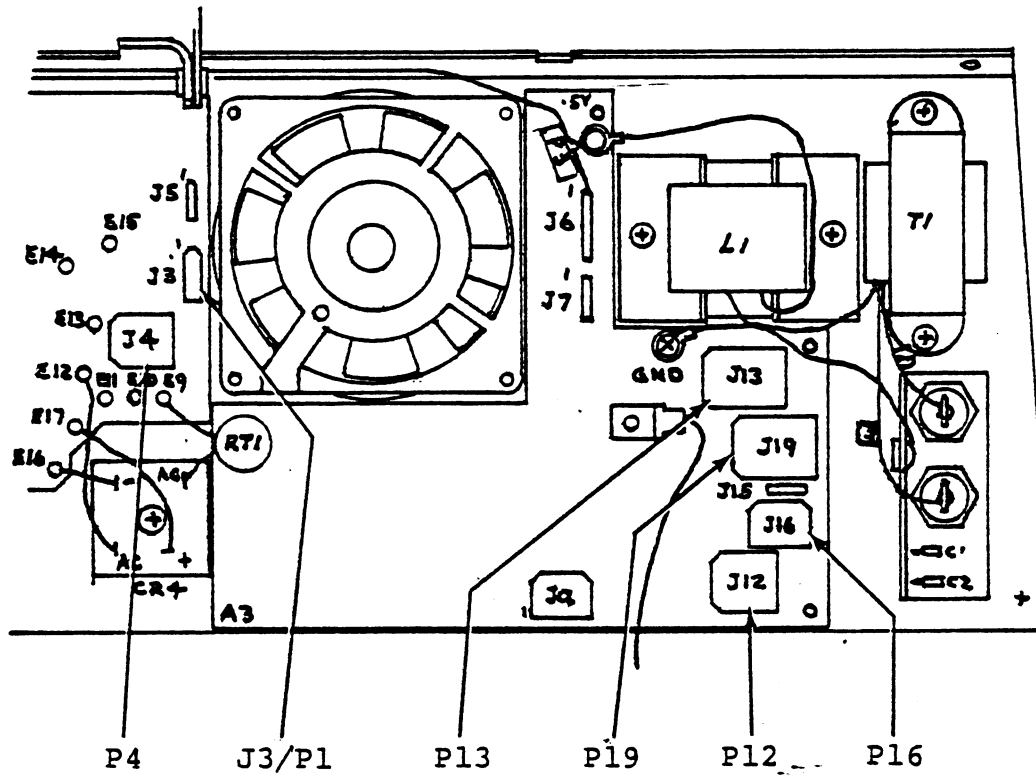


Figure 5-12. Power Supply Connections

- (3) P16 to deflection raster scan board.
- (4) P13 to processor/emulation board.
- e. Disconnect following connectors from power supply II board:
 - (1) J3/P1 from power switch S1.
 - (2) P4 to control transformer A17T1.
- f. To install power panel, place panel near rear of processor.
- g. Connect following connectors on power supply II board:
 - (1) J3/P1 from power switch S1.
 - (2) P4 from control transformer A17T1.
- h. Connect following connectors on secondary regulator board:
 - (1) P12 from memory botherboard.
 - (2) P19 from display I/O board.
 - (3) P16 from deflection raster scan board.
 - (4) P13 from processor/emulation board.
- i. Install power panel on rear of processor with five Allen head screws.
- j. Install rear connector panel with two screws.
- k. Power up processor.

5.3.11 FAN

The fan is mounted on the power panel on the rear of the processor with four Allen screws. See Figure 5-11.

- a. Remove all power from processor.
- b. Remove power panel from processor (Paragraph 5.3.10).
- c. Disconnect fan connector P6/J1.
- d. Remove four Allen screws holding fan to power panel.

- e. Lift fan from power panel.
- f. Position fan on power panel with fan connector positioned as before.
- g. Secure fan with the four mounting screws.
- h. Connect fan connector P6/J1.
- i. Install power panel.
- j. Power up processor.

SECTION 6

OPTIONS

6.1 115VAC/230VAC POWER OPTION

The 1800 processor can be connected to operate on either 115VAC or 230VAC. The connections for both input voltages are shown in Figure 6-1. All voltage connections are made on power supply board II (A5A3).

6.2 COMMUNICATIONS JUMPERS

All of the following jumpers are located on the Display-I/O board (A1), Figure 6-2.

6.2.1 BAUD RATE CONVERSION

The 1800 processor communications module provides internal generated baud rates of 150 baud thru 9600 baud selected by jumpers as follows:

Receive Clock

Jumper from E32
to one of following
Baud Rate E points.

Transmit Clock

Jumper from E33
to one of following
Baud rate E points.

Baud Rate E Points

E34 9600

E35 4800

E36 2400

E37 1200

E38 600

E39 300

E40 150

6.2.2 RECEIVE/TRANSMIT CLOCK SOURCE

The communications module can operate from either an internal or external source for receive or transmit clock. Each clock source may be selected with jumpers as follows:

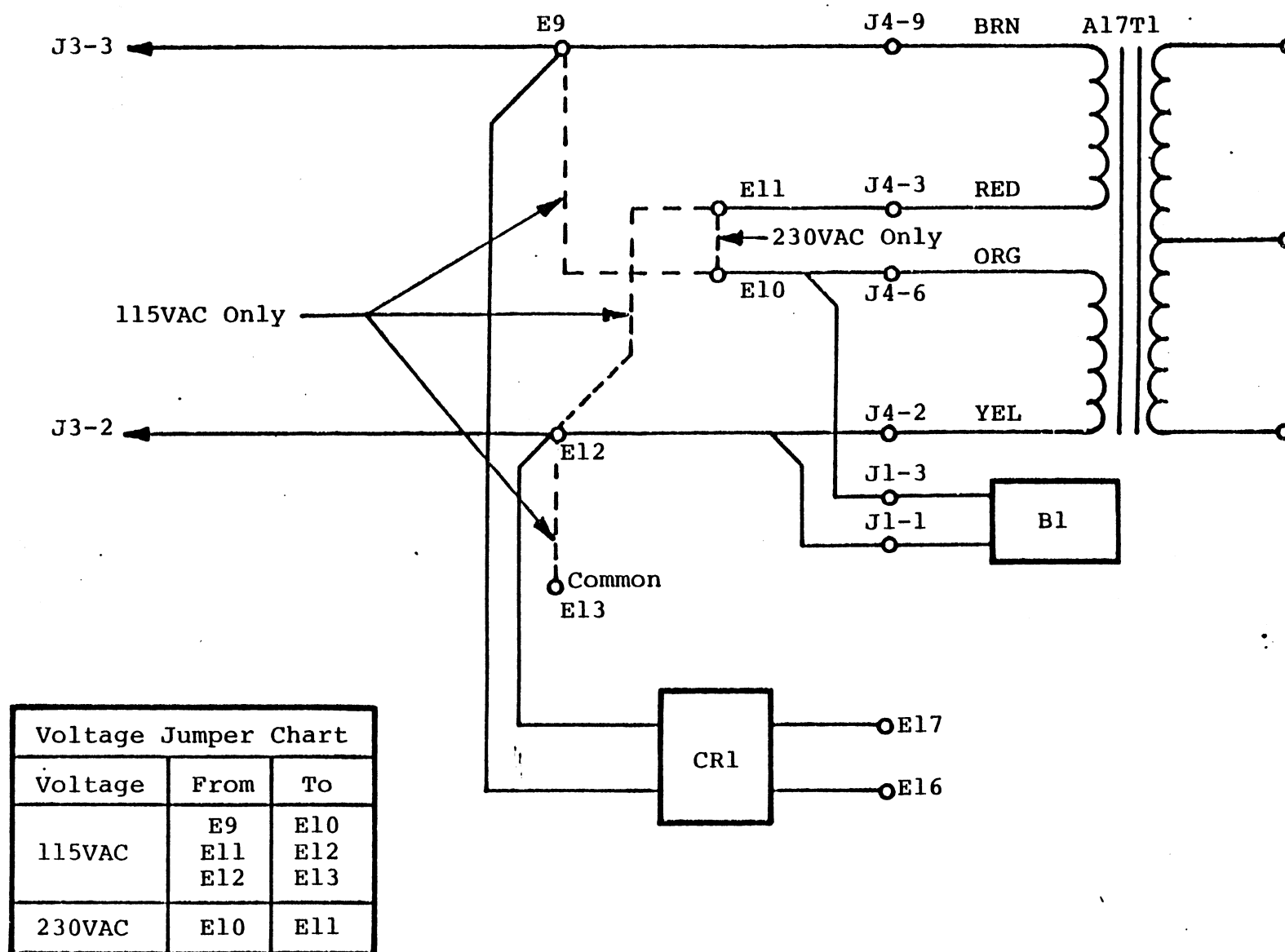


Figure 6-1. Processor Power Supply Connections for 115VAC/230VAC Input Power

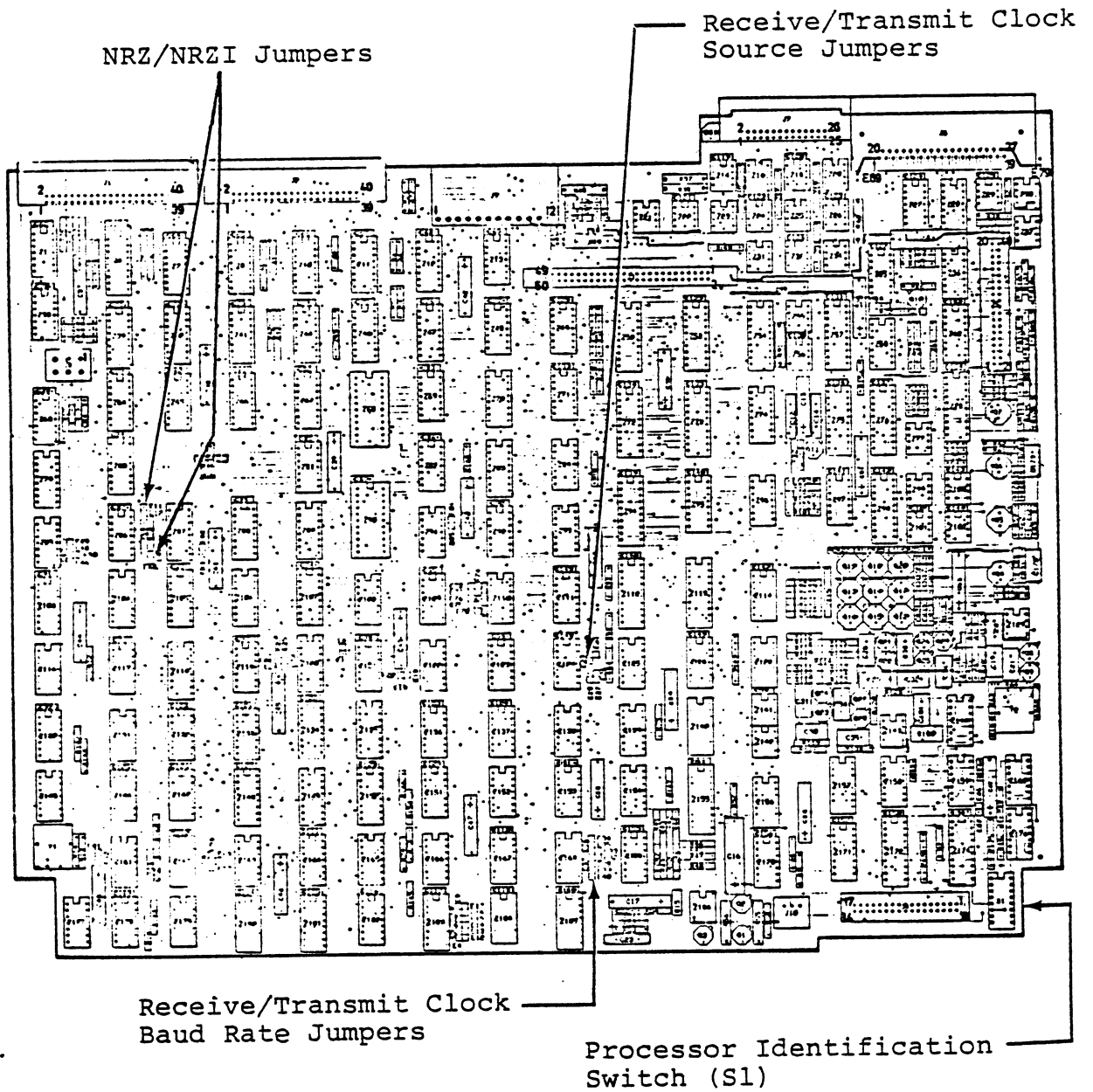


Figure 6-2. Display-I/O Board

Receive Clock Source

External E27 to E26
Internal E27 to E28

Transmit Clock Source

External E30 to E29
Internal E30 to E31

6.2.3 NRZI JUMPERS

The communications module can operate in either the NRZI or non-NRZI mode. Either mode can be selected by jumpers on the Display-I/O board (A1) as follows:

NRZI Jumpers (NRZ if open)

E10 to E11
E88 to E89

6.2.4 PROCESSOR IDENTIFICATION SELECTION

The 1800 processor identification can be switch selected by switch S1 on the display - I/O board (Figure 6-2). To access the switch, the processor cover must be removed. After the cover is removed, the switch is located behind the air vent panel of the base plate on the lower right side of the processor (Figure 6-3). The switch is an eight pole switch. Each pole represents a bit of the eight bit identification number.

Processor Identification Switch

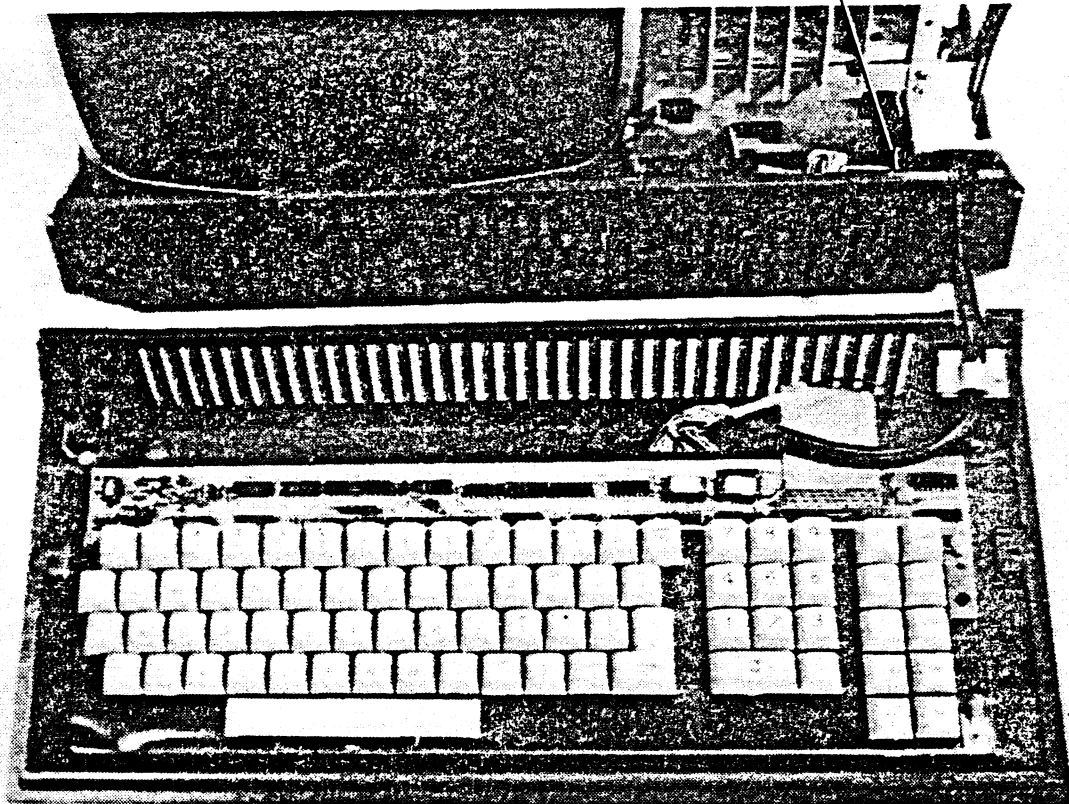
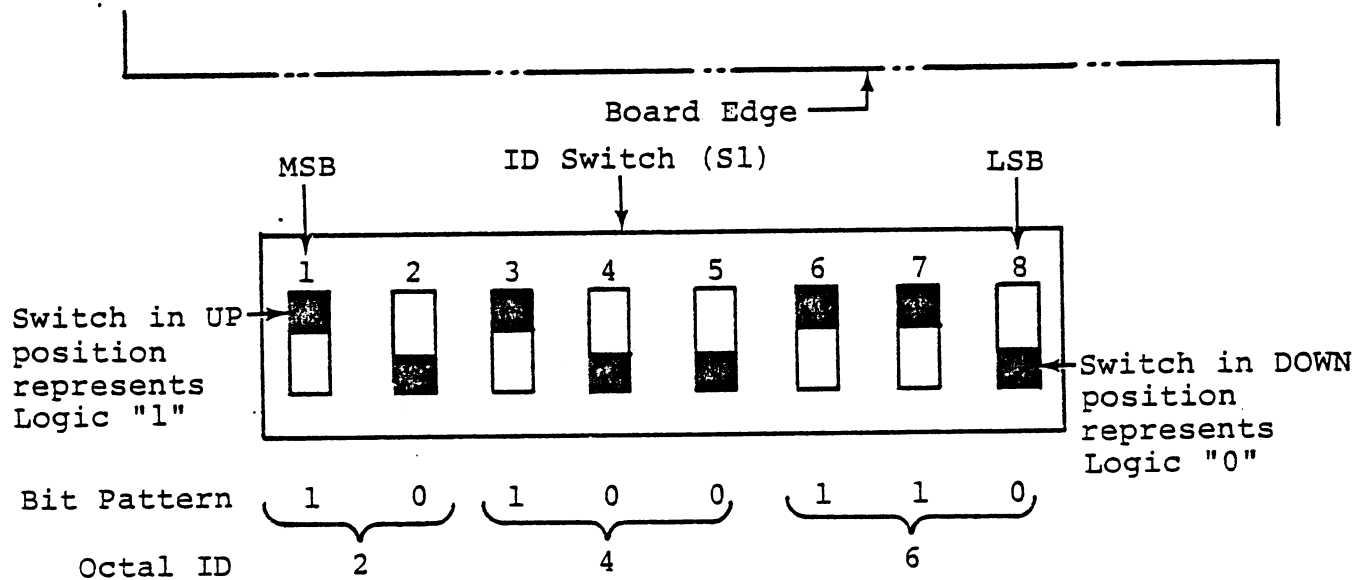


Figure 6-3. Location of Processor Identification Switch

The processor identification can be selected as follows:



NOTE

The identification switch has an "arrow" and an "ON" designation on the left side of the switch module. Disregard this convention as it does not apply to the setting of this switch.

To change identification number, set all switch poles to down position. This represents an identification number of zero. Then set poles that should be ones for the desired identification to the up position. Possible identification numbers range from 001 to 377 octal. This switch is not factory set.

SECTION 7
PARTS LIST AND IPB'S

7.1 PARTS LIST

<u>PART NUMBER</u>	<u>DESCRIPTION</u>	<u>REF DES</u>
<u>ASSEMBLIES</u>		
11-0522-001(4)	Assy, 1800 Terminal and Keyboard	U1
10-1211-001(3)	Assy, Control Transformer	A17
10-1384-005(2)	Assy, Removable Keyboard	A3
10-1402-001(7)	Assy, 1800 Terminal (without Keyboard)	U1
10-1420-001(5)	Assy, Power Panel II	A5
10-1448-001(3)	Assy, Transformer, Power	A5A3
10-1456-001(4)	Assy, Keyboard and Bracket	A3
10-1497-001(5)	Assy, Flyback Transformer III	A14
<u>PWA'S</u>		
10-0696-001(7)	PWA, Deflection Raster Scan	A4
10-1002-001(1)	PWA, 32K RAM I	A8-A11
10-1166-005(6)	PWA, 8K ROM I	A7
10-1167-001(7)	PWA, Power Supply II	A5A3
10-1292-002(5)	PWA, Power Supply Control II	A5A1
10-1340-001(0)	PWA, Display I/O III	A1
10-1342-001(6)	PWA, Processor/Emulation II	A2
10-1392-001(1)	PWA, Direct Buffer II	
10-1416-001(6)	PWA, Secondary Regulator	A5A2
10-1417-001(9)	PWA, Memory Motherboard II	A6

<u>PART NUMBER</u>	<u>DESCRIPTION</u>	<u>REF DES</u>
<u>WIRE AND CABLES</u>		
10-1047-002(7)	CA, 40 Conductor, 1 in.	W1
10-1133-001(4)	CA, 50 Conductor PC	A6W1
10-1134-001(7)	CA, Display to External Devices	
10-1147-001(6)	CA, 26 Conductor, 36 in. (Micro bus cable)	
10-1168-001(0)	CA, Speaker	A15
10-1388-002(5)	CA, Keyboard to Terminal	
10-1419-001(5)	HA, Power Panel II	A5W1
10-1431-001(5)	CA, 5500 I/O, Internal	
10-1439-001(9)	CA, Interboard, Filament/Sync	A5W2
10-1440-001(9)	CA, Memory Motherboard Power	W4
10-1441-001(2)	CA, Defl. Raster Scan Bd. Power	W3
10-1442-001(5)	CA, Display I/O Power	W2
10-1443-001(8)	CA, Processor/Emulation Bd. Power	W1
10-1453-001(5)	HA, Power Input II	A13
10-1509-001(7)	CA, 1800 to Synchronous Modem and ACU	
10-1510-001(7)	CA, 1800 to Async Modem W/Rev. Ch.	
10-1511-001(0)	CA, 1800 to Sync Modem	
10-1512-001(3)	CA, 1800 to Async Modem and ACU	
<u>MISC PARTS</u>		
47-0022-001(8)	Fuse, 3a, 250V, NB, 3AG (Power Line)	
47-0050-001(3)	Fuse, PICO, 2a (Display I/O Board)	
48-0007-001(6)	Filter, Line, 3a	

<u>PART NUMBER</u>	<u>DESCRIPTION</u>	<u>REF DES</u>
<u>MISC PARTS (Cont)</u>		
56-0029-001(1)	Yoke, CRT	
57-0002-001(3)	Fan	
78-0093-001(4)	Switch, Power	
81-0038-001(7)	Transformer, Flyback	
81-0064-001(6)	Transformer, Power	
83-0010-001(3)	CRT	
85-0074-013(4)	Keyboard and Bracket, 1800/3800 Std	
90-0044-001(4)	Loctite	
90-0053-001(8)	Thermacote	
90-0060-001(6)	Adhesive, PL10-BOND	
90-0099-001(4)	Adhesive, RTV-108	

7.2 ILLUSTRATED PARTS BREAKDOWN

The included set of IPB's cover the major mechanical assemblies of the 1800 Processor. The physical views of the electrical assemblies behind their corresponding schematic diagrams in Section 8 of this manual.

The IPB set is composed of the following assembly drawings.

<u>FIGURE NUMBER</u>	<u>DRAWING NUMBER</u>	<u>DRAWING TITLE</u>	<u>REFERENCE DESIGNATOR</u>
7-1	11-0522	1800 Assembly, Removable Keyboard	U1
7-2	10-1402	1800 Terminal Assembly, Removable Keyboard	U1
7-3	10-1384	Removable Keyboard Assembly	A3
7-4	10-1420	Power Panel Assembly II	A5

SECTION 8

REFERENCE MATERIAL

8.1 1800 PROCESSOR ROM DEBUG GUIDE

The 1800 Processor ROM Debug Guide is included on Page 8-4.

8.2 REFERENCE DRAWINGS

The reference drawings consist of wiring and cabling diagrams, schematic diagrams, and PWA outlines.

NOTE

The schematics and drawings contained in this section are copies of released drawings and may or may not include all existing Engineering Order (E.O.) changes. Schematics and drawings are replaced when outstanding E.O.'s are incorporated in the released drawing. If the accuracy or effectivity of a drawing is questionable, the Customer Service Engineer should review applicable Tech Tips and Field Change Orders for current E.O. status.

<u>FIGURE NUMBER</u>	<u>DRAWING NUMBER</u>	<u>DRAWING TITLE</u>	<u>REFERENCE DESIGNATOR</u>
<u>WIRING AND CABLING</u>			
8-1	01-0699	ICD, Power Panel II	A5
8-2	01-0701	ICD, 1800 II	U1
8-3	10-1134	CA, Display to External Devices	
8-4	10-1168	CA, Speaker	A15
8-5	10-1211	Assy, Control Transformer	A17
8-6	10-1388	CA, Removable Keyboard to Terminal	
8-7	10-1419	HA, Power Panel II	A5W1
8-8	10-1431	CA, 5500 I/O, Internal	
8-9	10-1439	CA, Filament/Sync, Interboard	A5W2

<u>FIGURE NUMBER</u>	<u>DRAWING NUMBER</u>	<u>DRAWING TITLE</u>	<u>REFERENCE DESIGNATOR</u>
<u>WIRING AND CABLING (Cont)</u>			
8-10	10-1440	CA, Memory Motherboard Power	W4
8-11	10-1441	CA, Defl. Raster Scan Bd. Power	W3
8-12	10-1442	CA, Display I/O Board Power	W2
8-13	10-1443	CA, Proc/Emulation Bd Power	W1
8-14	10-1448	Assy, Transformer, Power Panel II	A5A3
8-15	10-1453	HA, Power Input II	A13
8-16	10-1497	Assy, Flyback Transformer III	A14
8-17	10-1509	CA, 1800 to Synchronous Modem and ACU	
8-18	10-1510	CA, 1800 to Async Modem W/Rev. Ch.	
8-19	10-1511	CA, 1800 to Sync Modem	
8-20	10-1512	CA, 1800 to Async Modem and ACU	
<u>PROCESSOR SCHEMATICS AND PWA'S</u>			
8-21	01-0044	SD, Deflection Raster Scan	A4
8-21A	10-0696	PWA	
8-22	01-0213	SD, 32K RAM Memory	A8-A11
8-22A	10-1002	PWA	
8-23	01-0370	SD, 8K ROM I	A7
8-23A	10-1166	PWA	
8-24	01-0569	SD, Processor/Emulation II	A2
8-24A	10-1342	PWA	
8-25	01-0570	SD, Display I/O III	A1
8-25A	10-1340	PWA	

<u>FIGURE NUMBER</u>	<u>DRAWING NUMBER</u>	<u>DRAWING TITLE</u>	<u>REFERENCE DESIGNATOR</u>
<u>PROCESSOR SCHEMATICS AND PWA'S (Cont)</u>			
8-26	01-0697	SD, Memory Motherboard II	A6
8-26A	10-1417	PWA	
<u>POWER PANEL SCHEMATICS AND PWA'S</u>			
8-27	01-0371	SD, Power Supply II	A5A3
8-27A	10-1167	PWA	
8-28	01-0538	SD, Power Supply Control II	A5A1
8-28A	10-1292	PWA	
8-29	01-0696	SD, Secondary Regulator	A5A2
8-29A	10-1416	PWA	
<u>KEYBOARD SCHEMATICS AND PWA'S</u>			
8-30	01-0677	SD, Direct Buffer II	
8-30A	10-1392	PWA	
8-31	35-1496	SD, Keyboard (OEM)	
8-31A	65-1496	PWA (OEM)	

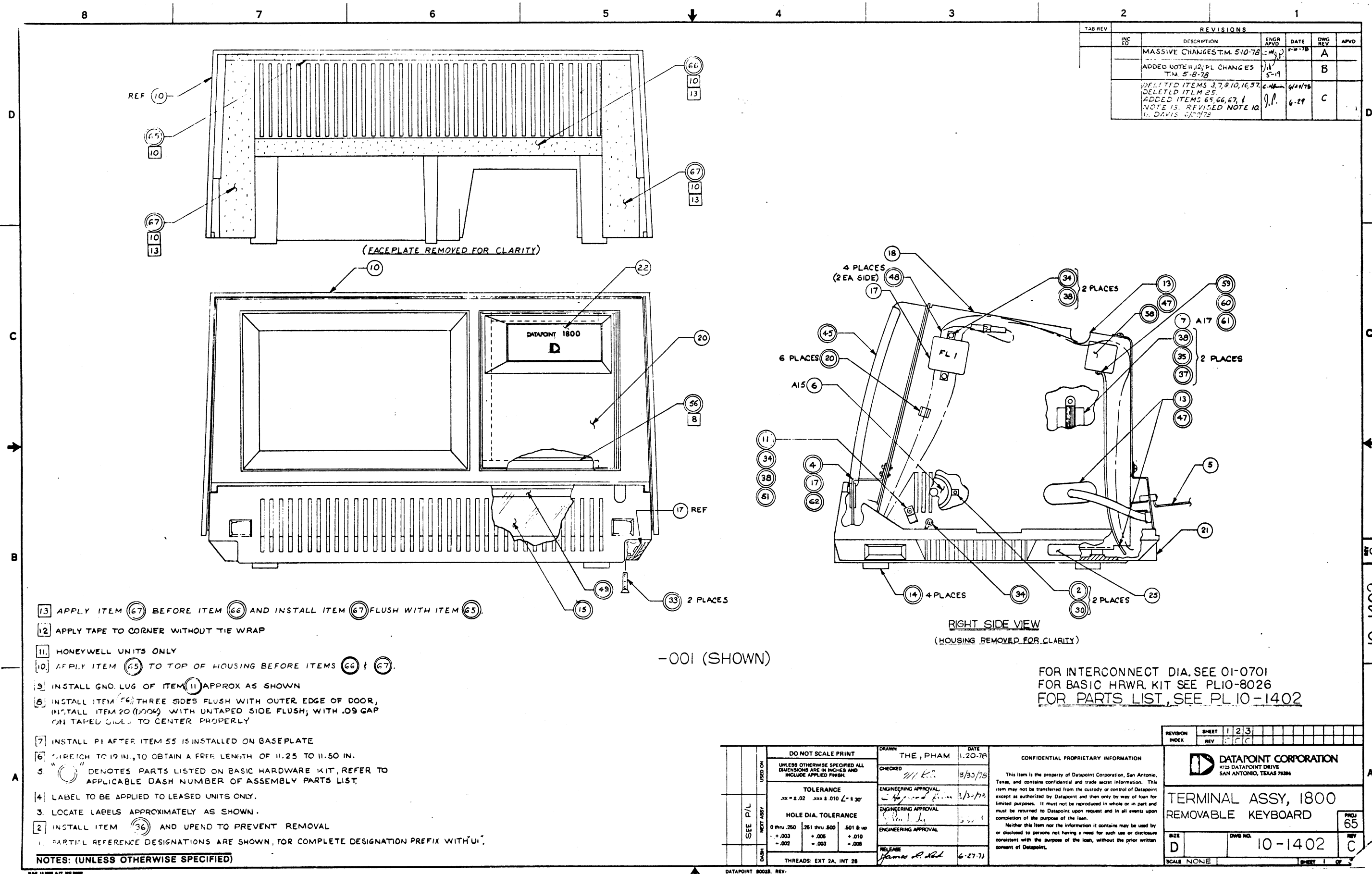
DATAPOINT 1800 PROCESSOR

ROMGUIDE

System ROM Operating Description

NOT AVAILABLE

AT THIS TIME



TAB REV	REVISIONS					
	INC	ED	DESCRIPTION	ENGR	DATE	APVD
			MASSIVE CHANGES T.M. 5-10-78	J.M.P.	5-10-78	A
			ADDED NOTE 11, 12, PL CHANGES T.M. 5-8-78	J.M.P.	5-19-78	B
			DELETED ITEMS 3, 7, 9, 10, 16, 57, 58, 59, 60, 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153, 154, 155, 156, 157, 158, 159, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232, 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308, 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 334, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 374, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385, 386, 387, 388, 389, 390, 391, 392, 393, 394, 395, 396, 397, 398, 399, 400, 401, 402, 403, 404, 405, 406, 407, 408, 409, 410, 411, 412, 413, 414, 415, 416, 417, 418, 419, 420, 421, 422, 423, 424, 425, 426, 427, 428, 429, 430, 431, 432, 433, 434, 435, 436, 437, 438, 439, 440, 441, 442, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 455, 456, 457, 458, 459, 460, 461, 462, 463, 464, 465, 466, 467, 468, 469, 470, 471, 472, 473, 474, 475, 476, 477, 478, 479, 480, 481, 482, 483, 484, 485, 486, 487, 488, 489, 490, 491, 492, 493, 494, 495, 496, 497, 498, 499, 500, 501, 502, 503, 504, 505, 506, 507, 508, 509, 510, 511, 512, 513, 514, 515, 516, 517, 518, 519, 520, 521, 522, 523, 524, 525, 526, 527, 528, 529, 530, 531, 532, 533, 534, 535, 536, 537, 538, 539, 540, 541, 542, 543, 544, 545, 546, 547, 548, 549, 550, 551, 552, 553, 554, 555, 556, 557, 558, 559, 560, 561, 562, 563, 564, 565, 566, 567, 568, 569, 570, 571, 572, 573, 574, 575, 576, 577, 578, 579, 580, 581, 582, 583, 584, 585, 586, 587, 588, 589, 590, 591, 592, 593, 594, 595, 596, 597, 598, 599, 600, 601, 602, 603, 604, 605, 606, 607, 608, 609, 610, 611, 612, 613, 614, 615, 616, 617, 618, 619, 620, 621, 622, 623, 624, 625, 626, 627, 628, 629, 630, 631, 632, 633, 634, 635, 636, 637, 638, 639, 640, 641, 642, 643, 644, 645, 646, 647, 648, 649, 650, 651, 652, 653, 654, 655, 656, 657, 658, 659, 660, 661, 662, 663, 664, 665, 666, 667, 668, 669, 670, 671, 672, 673, 674, 675, 676, 677, 678, 679, 680, 681, 682, 683, 684, 685, 686, 687, 688, 689, 690, 691, 692, 693, 694, 695, 696, 697, 698, 699, 700, 701, 702, 703, 704, 705, 706, 707, 708, 709, 710, 711, 712, 713, 714, 715, 716, 717, 718, 719, 720, 721, 722, 723, 724, 725, 726, 727, 728, 729, 730, 731, 732, 733, 734, 735, 736, 737, 738, 739, 740, 741, 742, 743, 744, 745, 746, 747, 748, 749, 750, 751, 752, 753, 754, 755, 756, 757, 758, 759, 760, 761, 762, 763, 764, 765, 766, 767, 768, 769, 770, 771, 772, 773, 774, 775, 776, 777, 778, 779, 780, 781, 782, 783, 784, 785, 786, 787, 788, 789, 790, 791, 792, 793, 794, 795, 796, 797, 798, 799, 800, 801, 802, 803, 804, 805, 806, 807, 808, 809, 810, 811, 812, 813, 814, 815, 816, 817, 818, 819, 820, 821, 822, 823, 824, 825, 826, 827, 828, 829, 830, 831, 832, 833, 834, 835, 836, 837, 838, 839, 840, 841, 842, 843, 844, 845, 846, 847, 848, 849, 850, 851, 852, 853, 854, 855, 856, 857, 858, 859, 860, 861, 862, 863, 864, 865, 866, 867, 868, 869, 870, 871, 872, 873, 874, 875, 876, 877, 878, 879, 880, 881, 882, 883, 884, 885, 886, 887, 888, 889, 890, 891, 892, 893, 894, 895, 896, 897, 898, 899, 900, 901, 902, 903, 904, 905, 906, 907, 908, 909, 910, 911, 912, 913, 914, 915, 916, 917, 918, 919, 920, 921, 922, 923, 924, 925, 926, 927, 928, 929, 930, 931, 932, 933, 934, 935, 936, 937, 938, 939, 940, 941, 942, 943, 944, 945, 946, 947, 948, 949, 950, 951, 952, 953, 954, 955, 956, 957, 958, 959, 960, 961, 962, 963, 964, 965, 966, 967, 968, 969, 970, 971, 972, 973, 974, 975, 976, 977, 978, 979, 980, 981, 982, 983, 984, 985, 986, 987, 988, 989, 990, 991, 992, 993, 994, 995, 996, 997, 998, 999, 1000	U. DAVIS	6-27-78	C

Figure 7-2. (Sht. 1)

Figure 7-2. (Sht. 2)

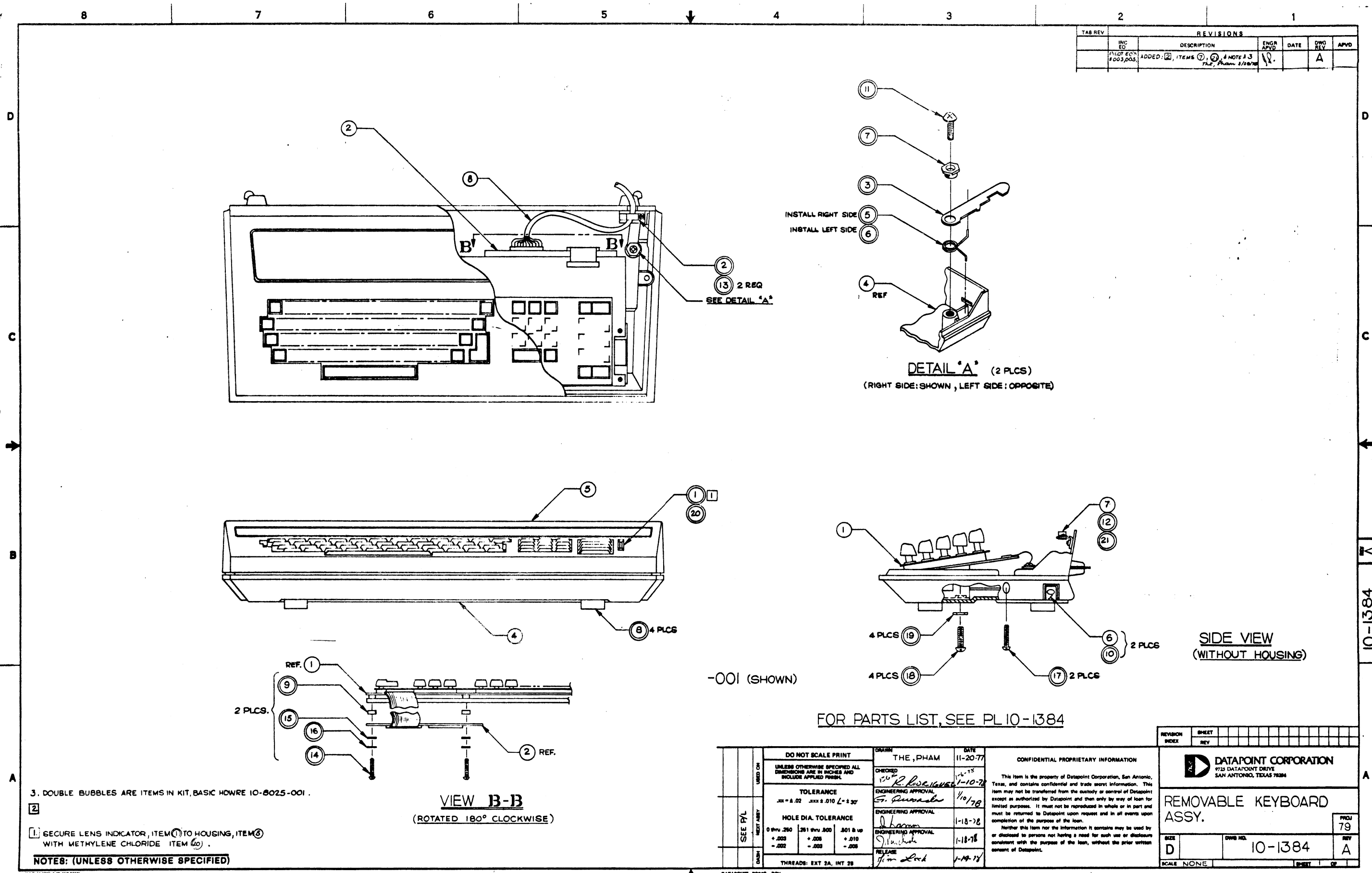


Figure 7-3.

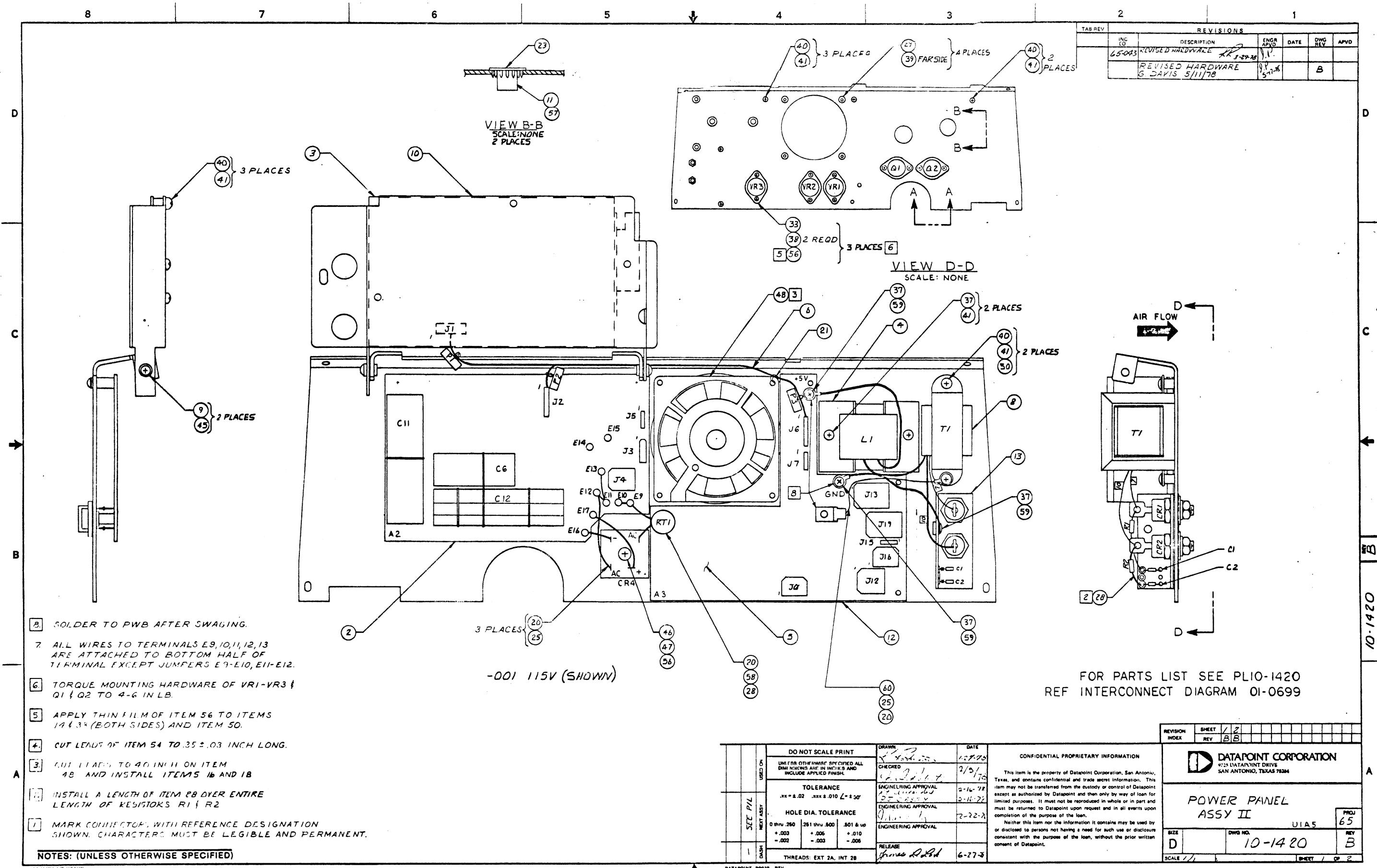


Figure 7-4. (Sht. 1)

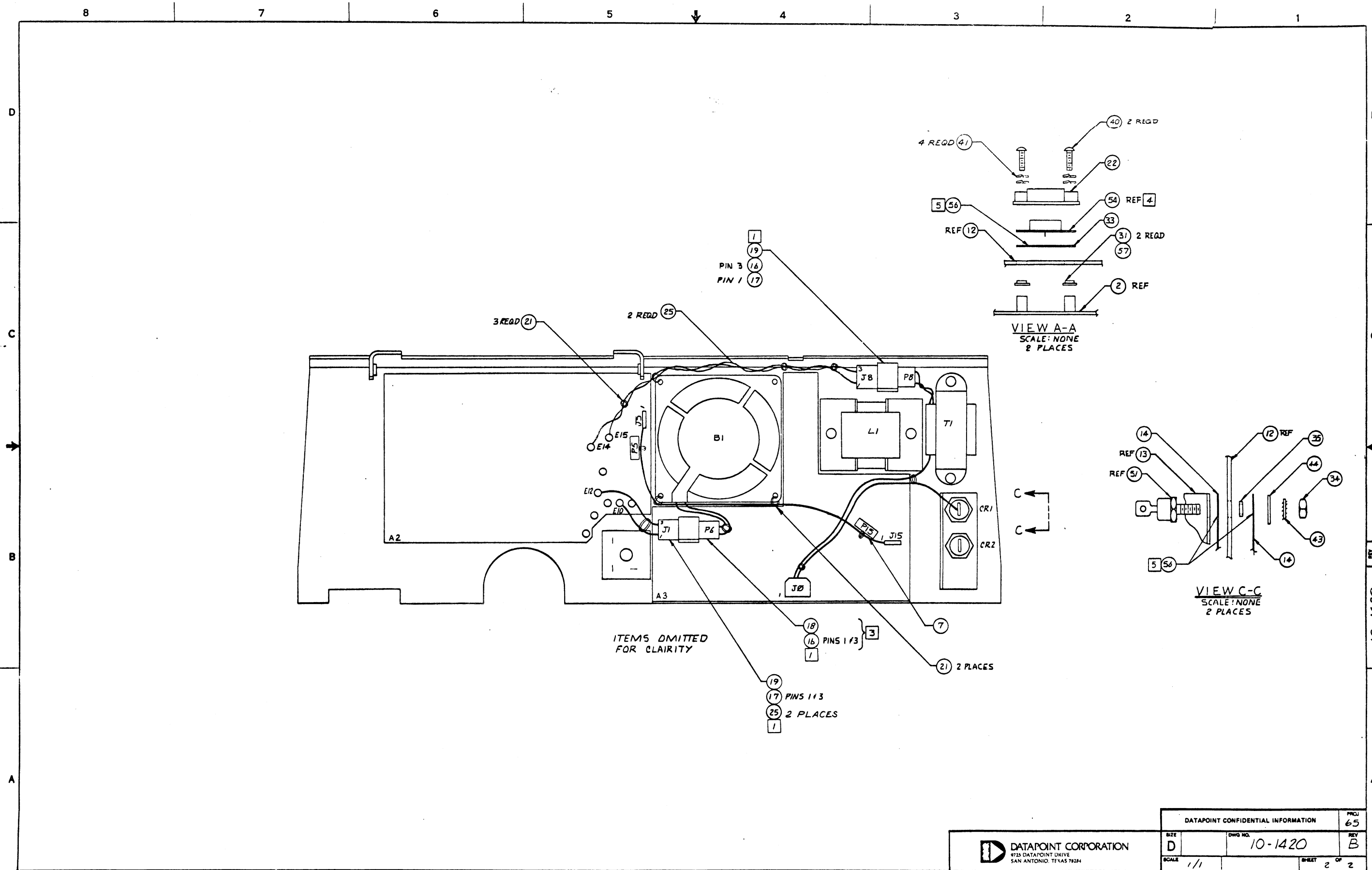
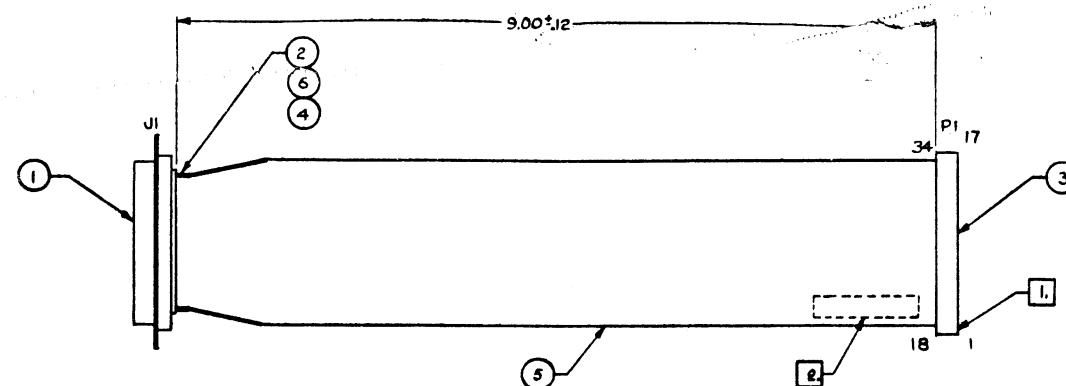
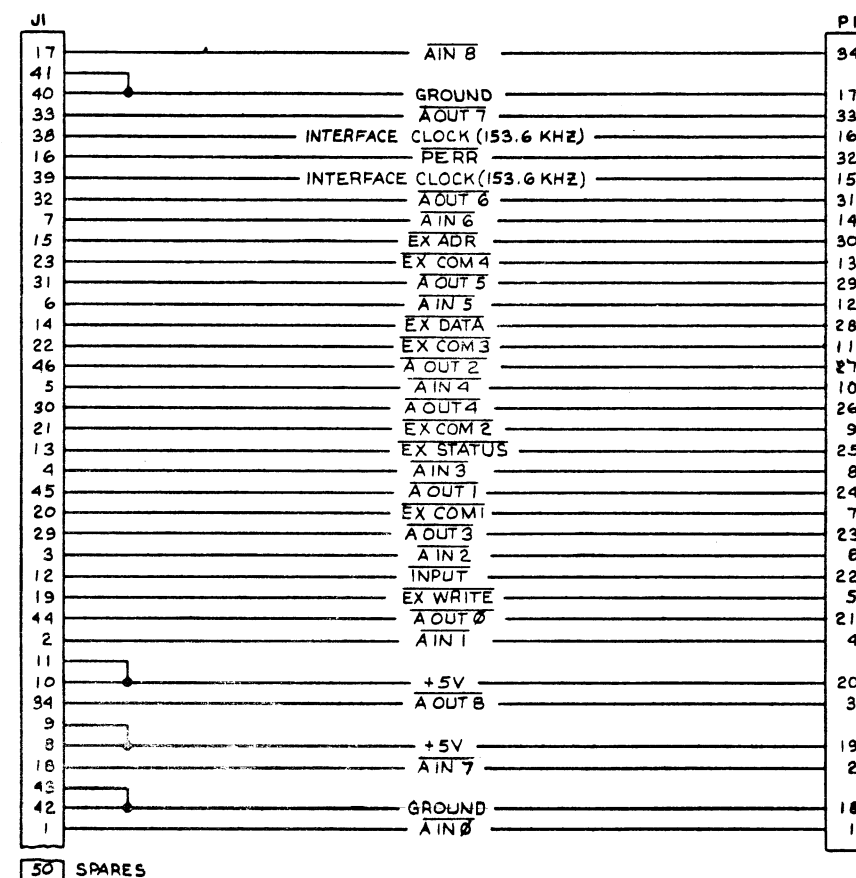


Figure 7-4. (Sht. 2)

TAB REV		REVISIONS			
NO	REV	DESCRIPTION	ENGR	DATE	APVD
8773		ADDED "W4" TO TITLE; NOTE 3	Engr	1-25-77	202
		TOOL WAS #3440, Serial #2-77	Engr	1-25-77	84



-001 SHOWN



50 SPARES

FOR PARTS SEE PL10-1134

3. RECOMMENDED 3M TOOL: #3440 (MANUAL) OR #3445 (PNEUMATIC)

2. MARK PART NO., APPLICABLE DASH NO. AND REV. LETTER LOCATE APPROX. AS SHOWN.

1. TRIANGULAR INDEX MARK, DENOTES PIN 1

NOTES: (UNLESS OTHERWISE SPECIFIED)

DO NOT SCALE PRINT		DRWN	DATE	CONFIDENTIAL PROPRIETARY INFORMATION	
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH.		Cabun W. Browner	10-15-74	This item is the property of Datapoint Corporation, San Antonio, Texas, and contains confidential and trade secret information. This item may not be transferred from the custody or control of Datapoint except as authorized by Datapoint and then only by way of loan for limited purposes. It must not be reproduced in whole or in part and must be returned to Datapoint upon request and in all events upon completion of the purpose of the loan.	
TOLERANCE X.XX = ± .02 X.XX = ± .010 L = ± .30"		CHECKED	DATE	This item may not be transferred from the custody or control of Datapoint except as authorized by Datapoint and then only by way of loan for limited purposes. It must not be reproduced in whole or in part and must be returned to Datapoint upon request and in all events upon completion of the purpose of the loan.	
HOLE DIA. TOLERANCE 0 thru .250 ± .003 .251 thru .500 ± .006 .501 & up ± .010		F. DELAVEGA	10/26/74	This item may not be transferred from the custody or control of Datapoint except as authorized by Datapoint and then only by way of loan for limited purposes. It must not be reproduced in whole or in part and must be returned to Datapoint upon request and in all events upon completion of the purpose of the loan.	
THREADS: EXT 2A, INT 2B		ENGINEERING APPROVAL	DATE	This item may not be transferred from the custody or control of Datapoint except as authorized by Datapoint and then only by way of loan for limited purposes. It must not be reproduced in whole or in part and must be returned to Datapoint upon request and in all events upon completion of the purpose of the loan.	
		RELEASE	DATE	This item may not be transferred from the custody or control of Datapoint except as authorized by Datapoint and then only by way of loan for limited purposes. It must not be reproduced in whole or in part and must be returned to Datapoint upon request and in all events upon completion of the purpose of the loan.	

REVISION INDEX		SHEET		1	
		REV		A	

DATAPOINT CORPORATION		7233 DATAPOINT DRIVE		SAN ANTONIO, TEXAS 78234	
CABLE ASSEMBLY, DISPLAY TO EXTERNAL DEVICES W4					
SIZE		D		REV	
		10-1134		A	

Figure 8-3.

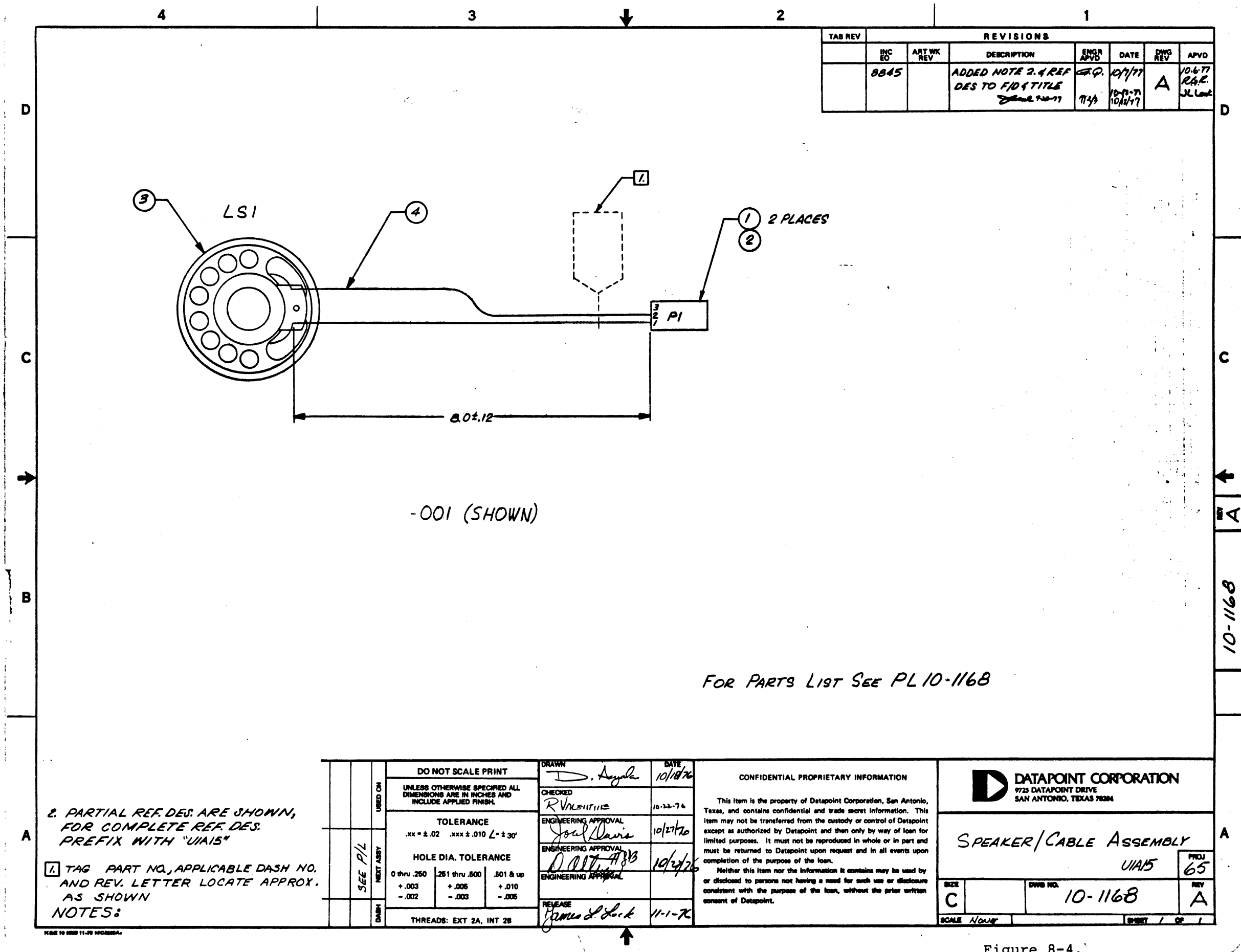


Figure 8-4.

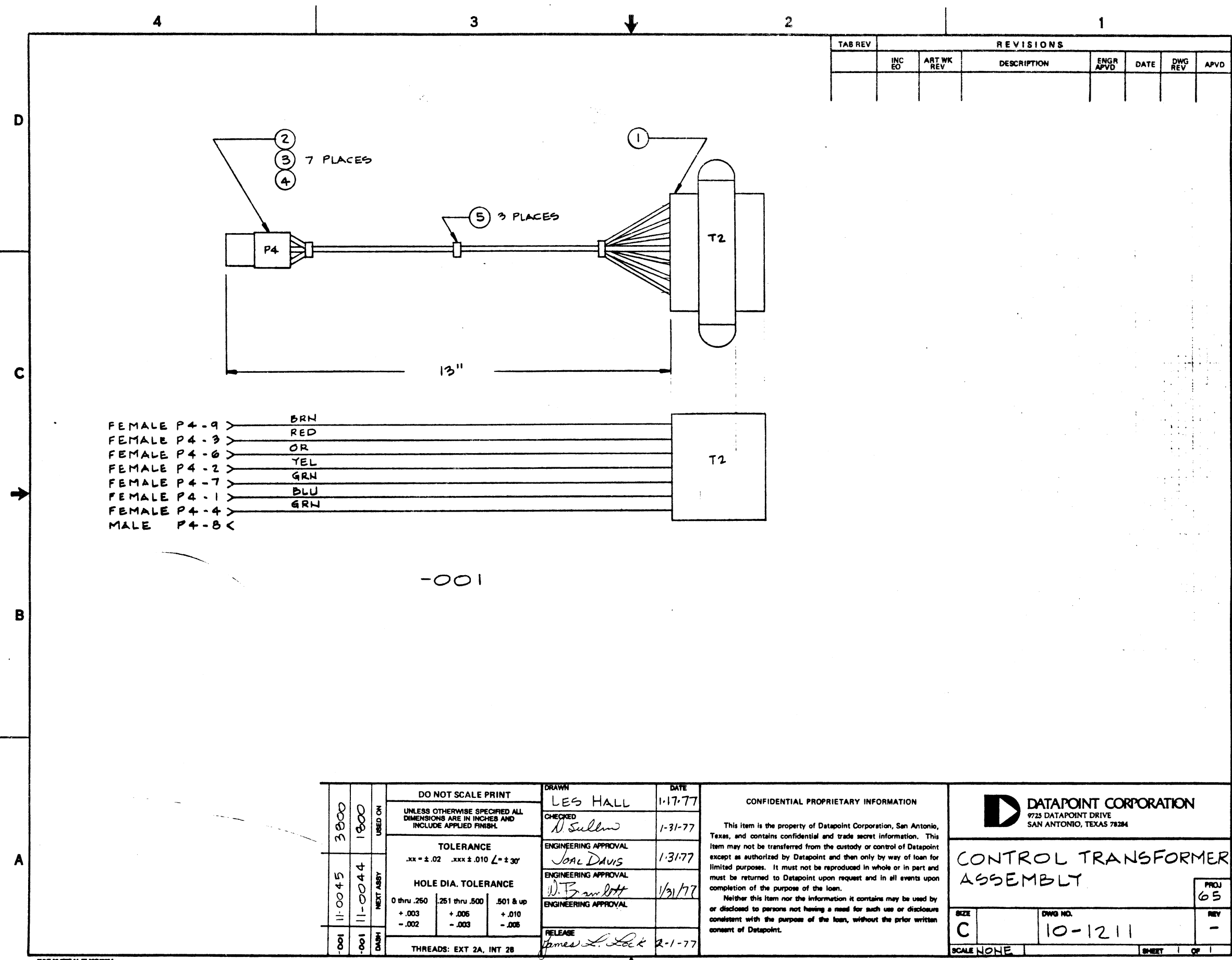
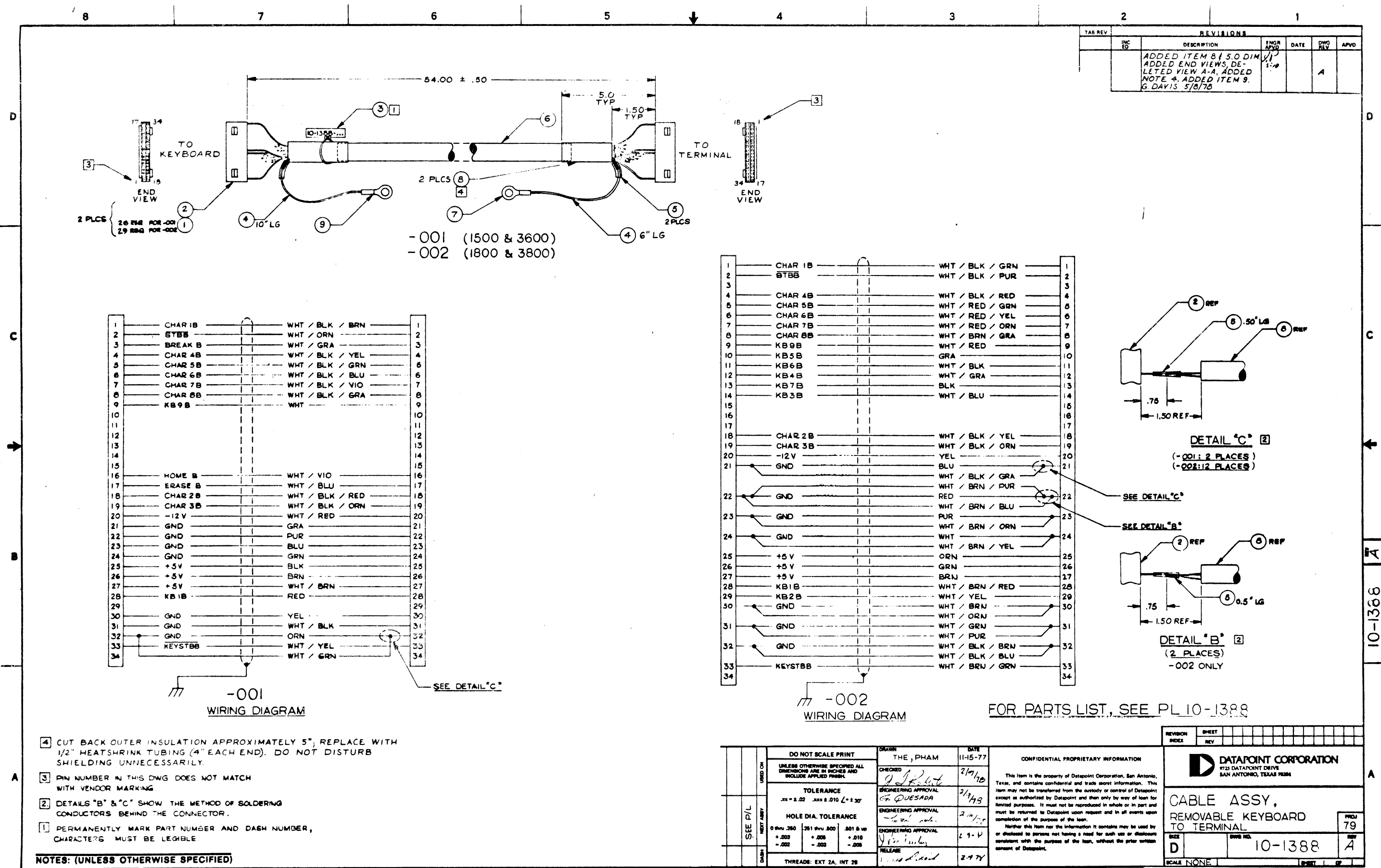


Figure 8-5.



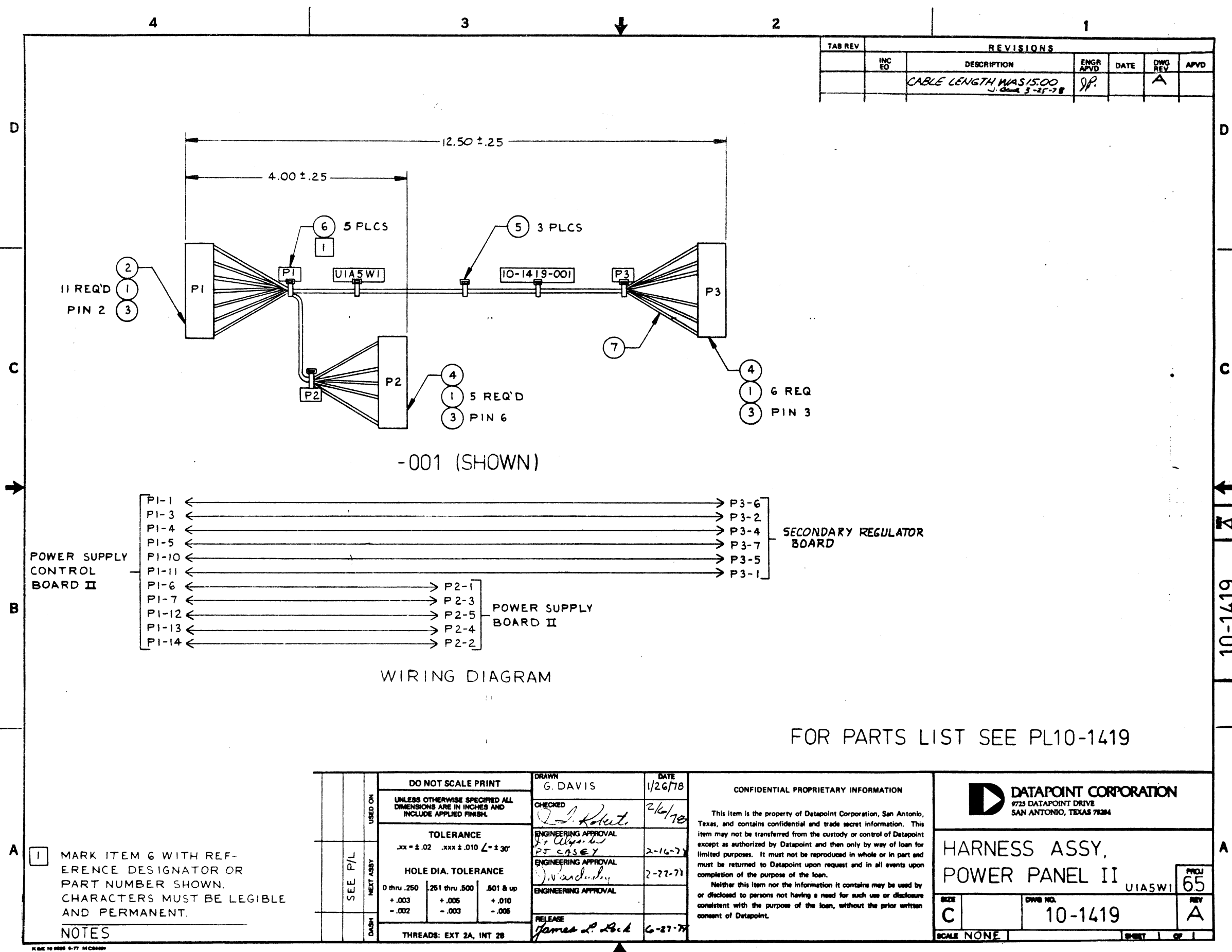
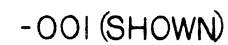


Figure 8-7.



WIRING DIAGRAM

1. PERMANENTLY MARK PART, APPLICABLE DASH NUMBER, OR REF DES. SHOWN, CHARACTERS MUST BE LEGIBLE

NOTES: (UNLESS OTHERWISE SPECIFIED)

REVISION INDEX	SHEET																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																																						</
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Figure 8-8.

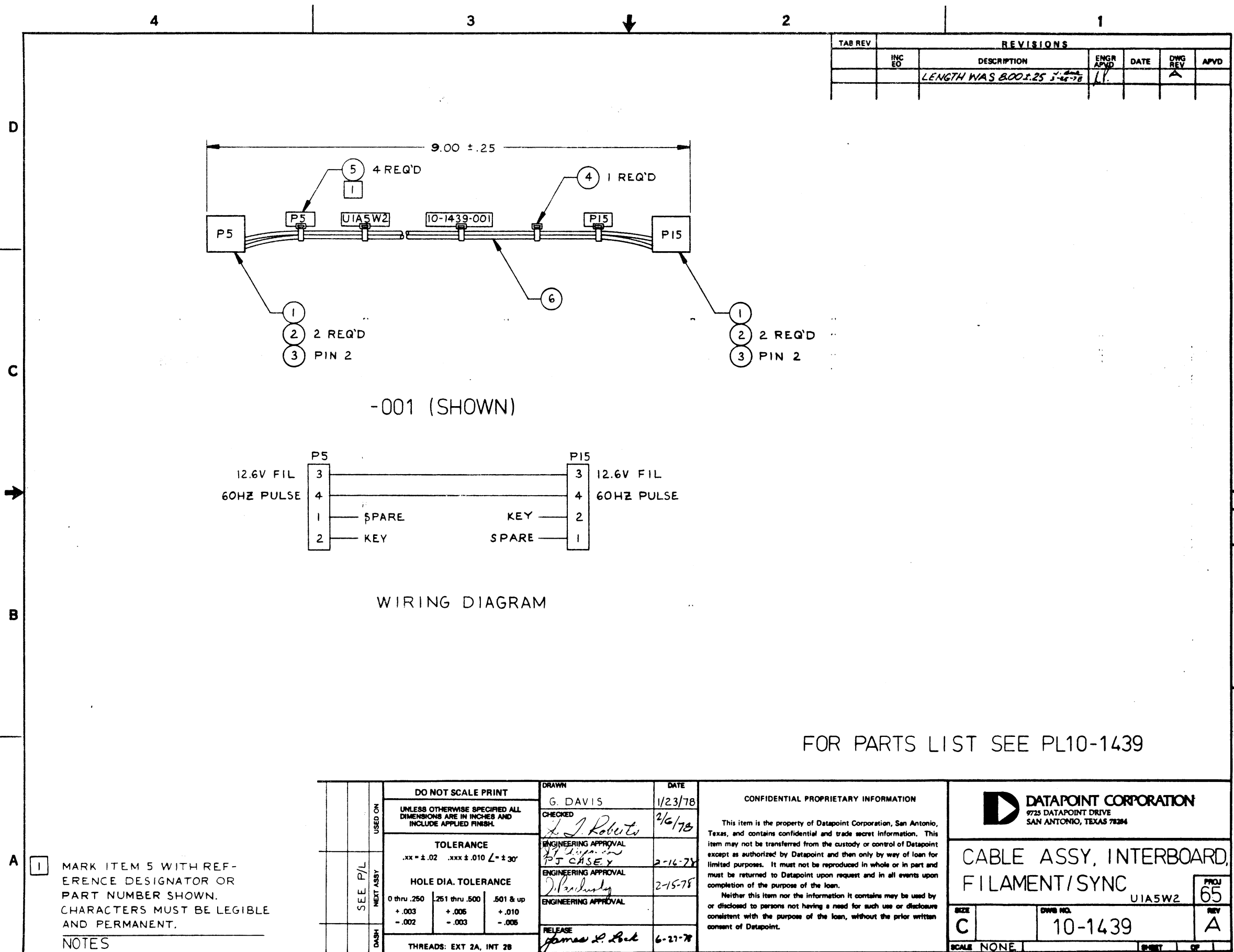


Figure 8-9.

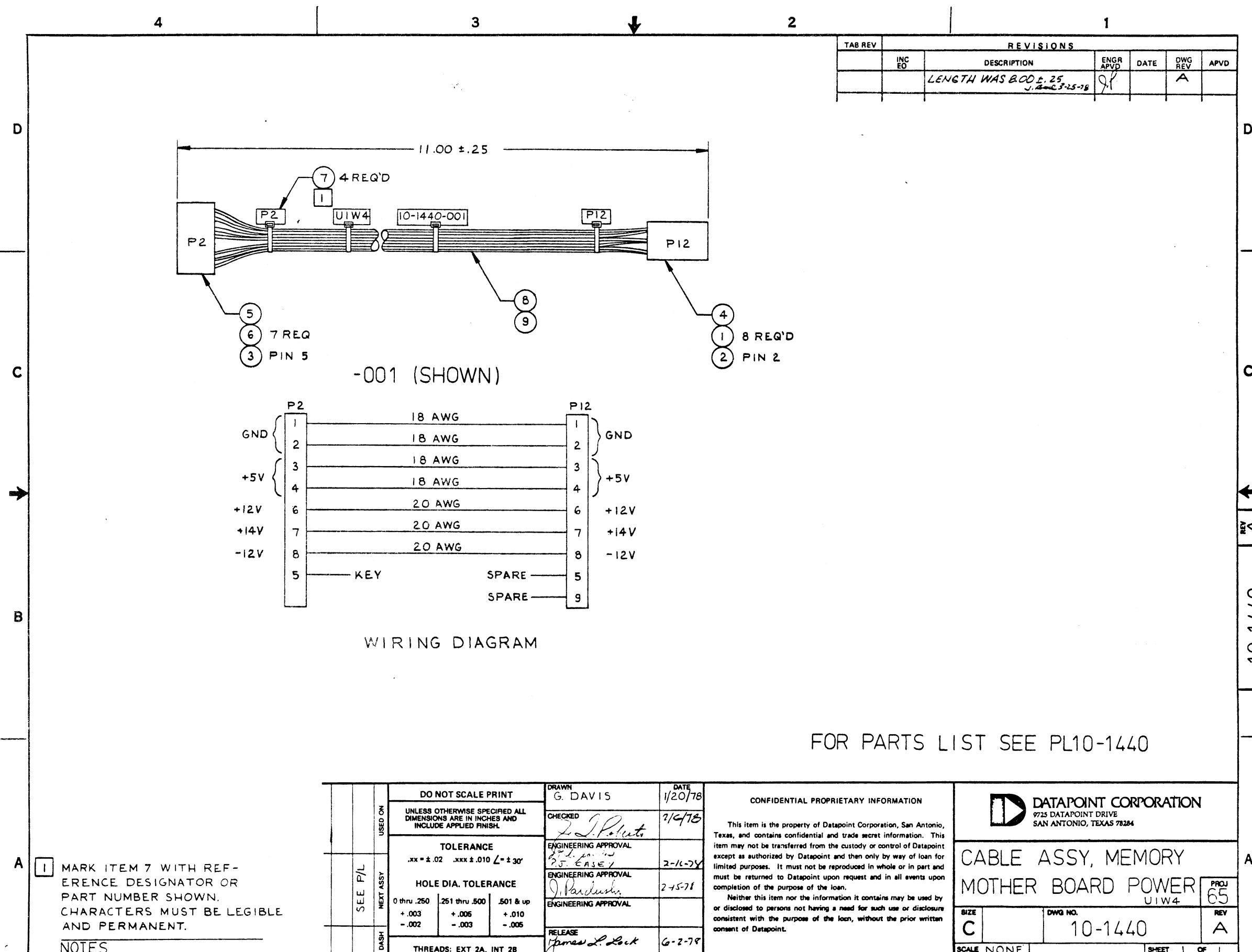


Figure 8-10.

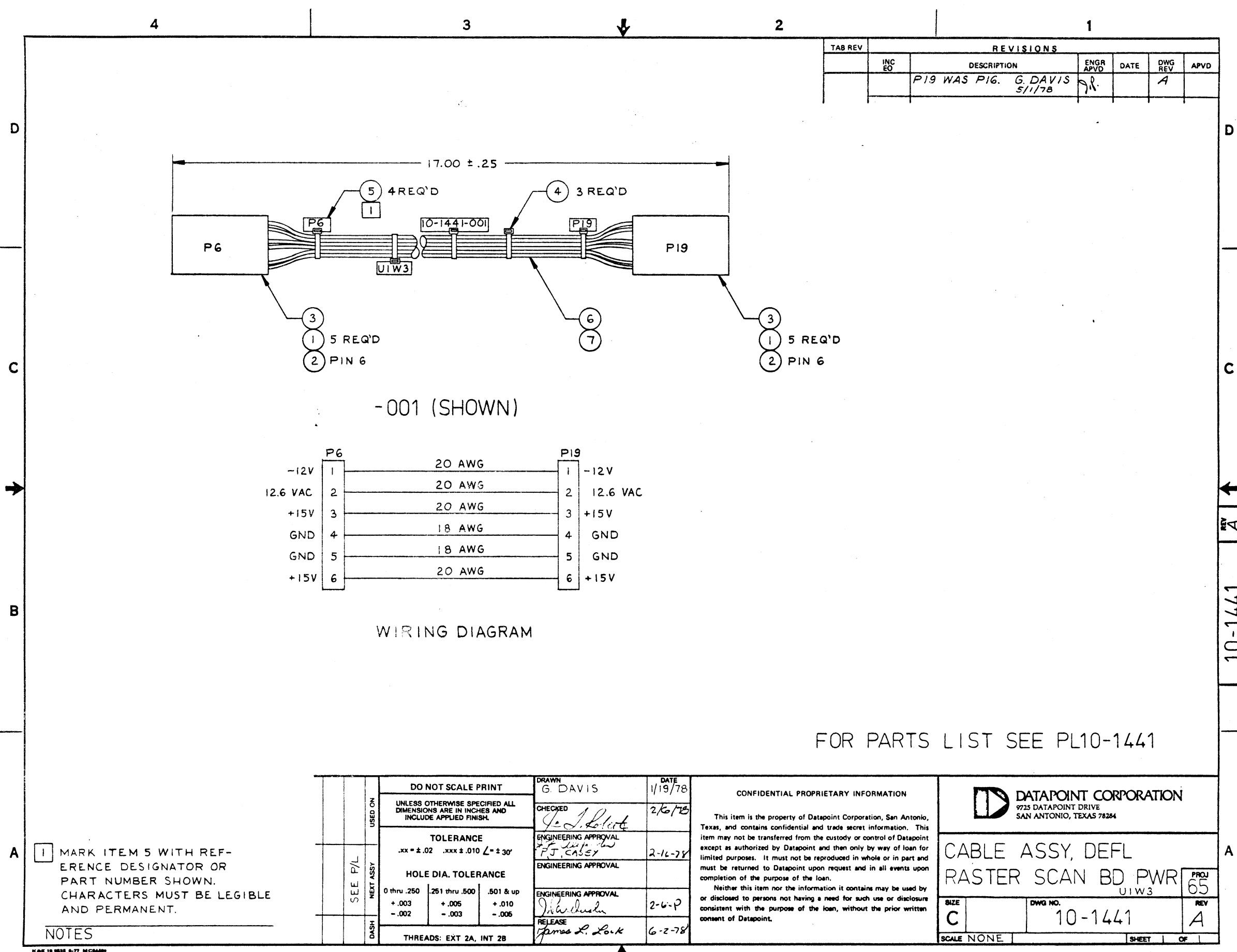


Figure 8-11.

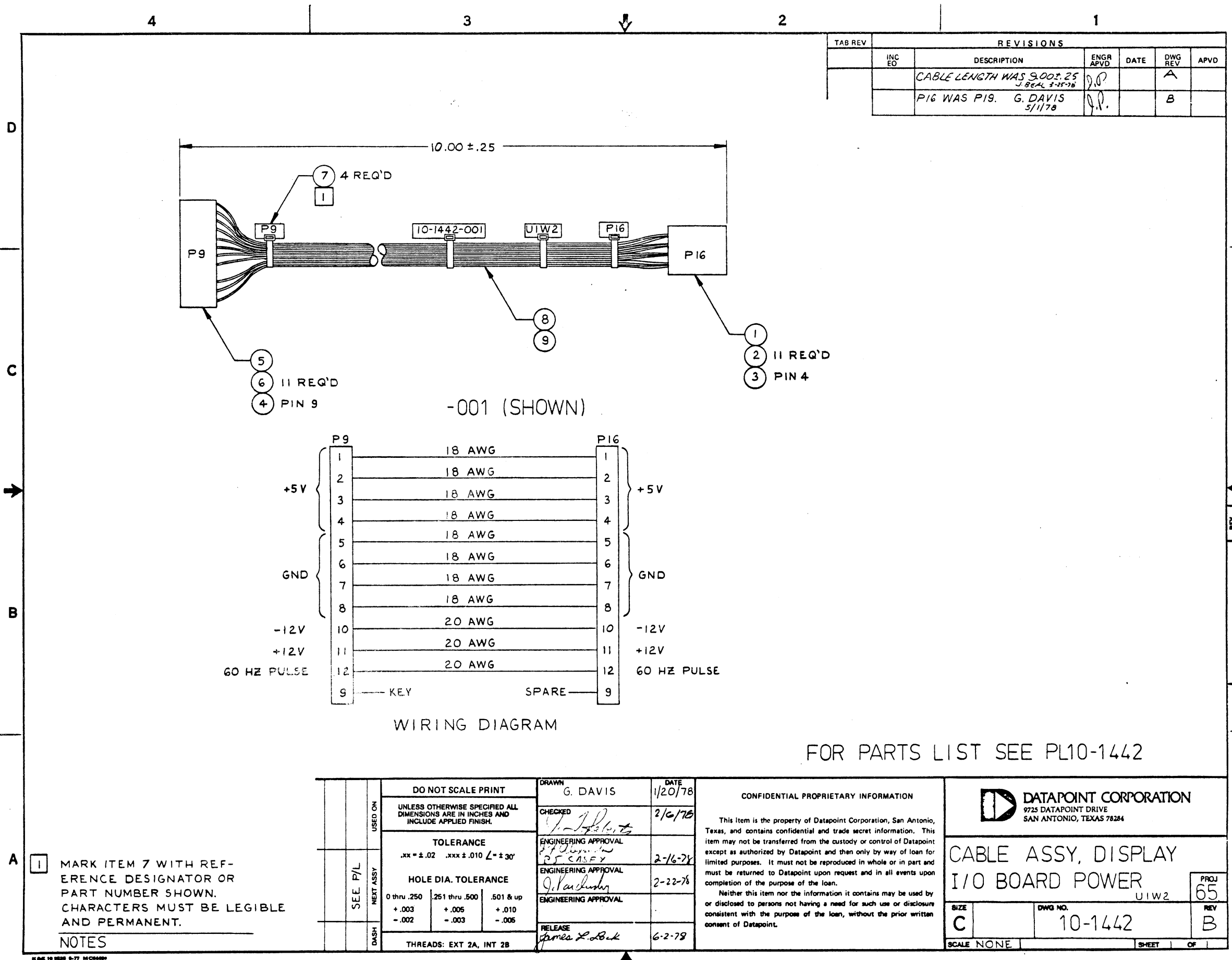


Figure 8-12.

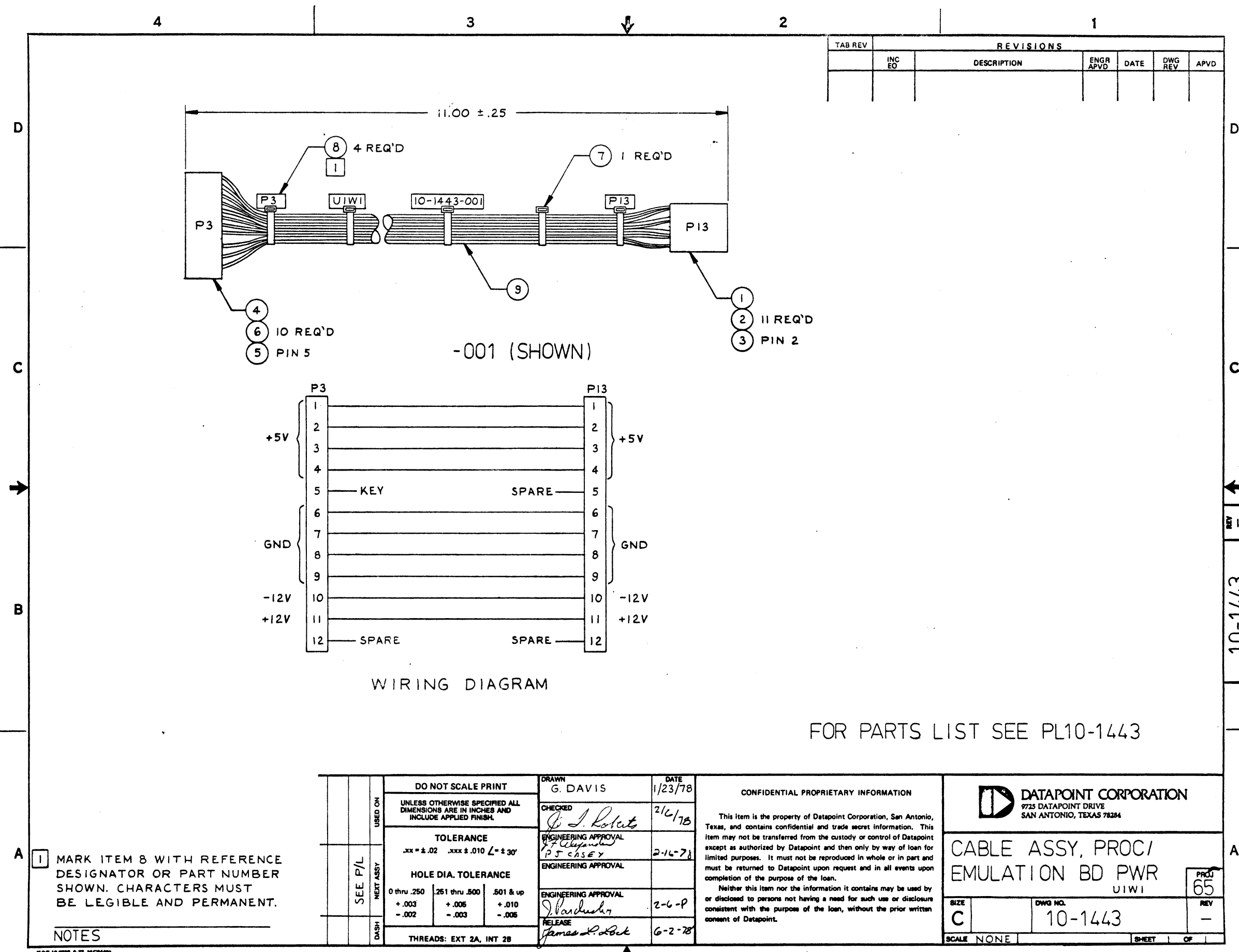


Figure 8-13.

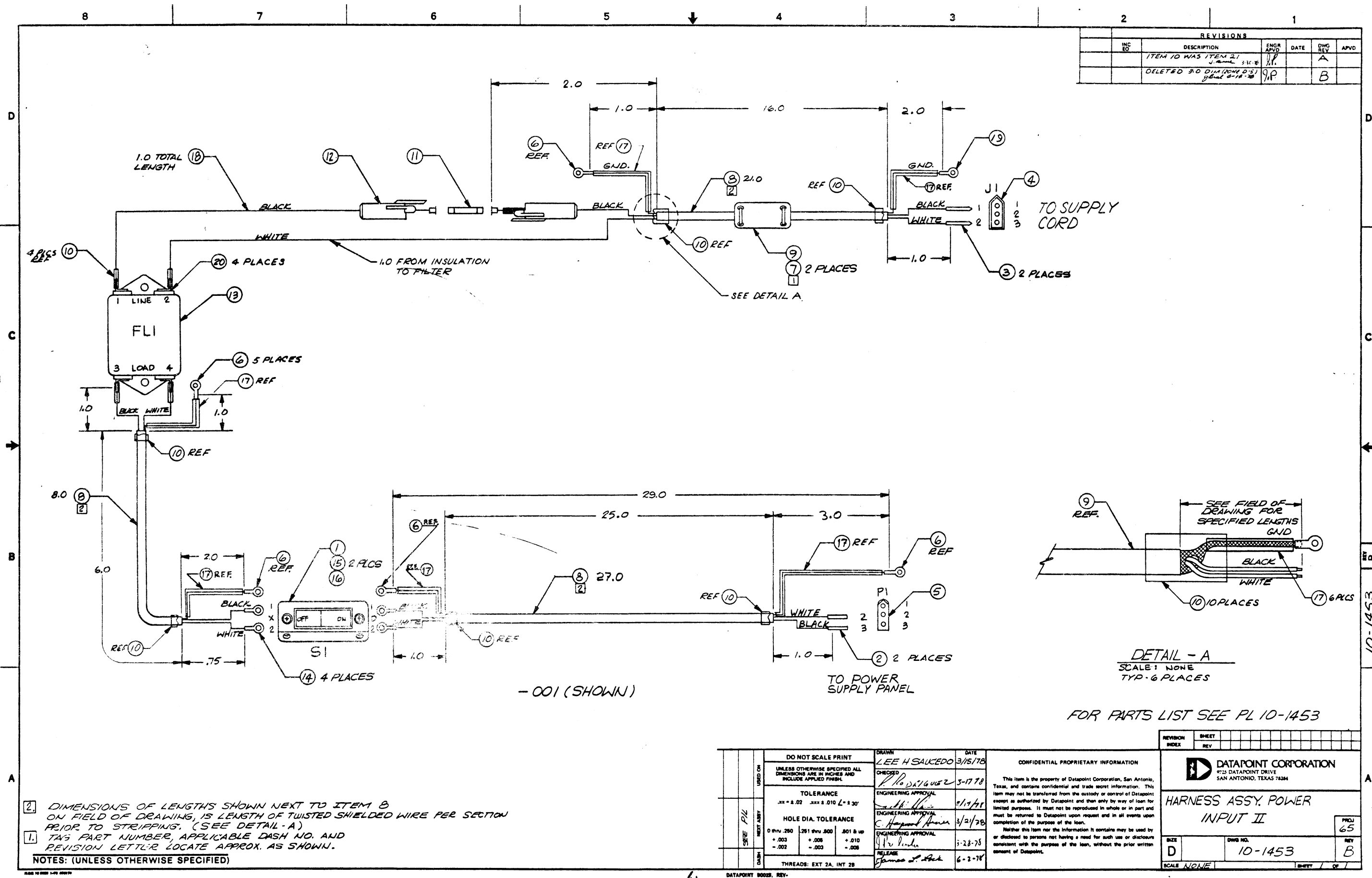


Figure 8-15.

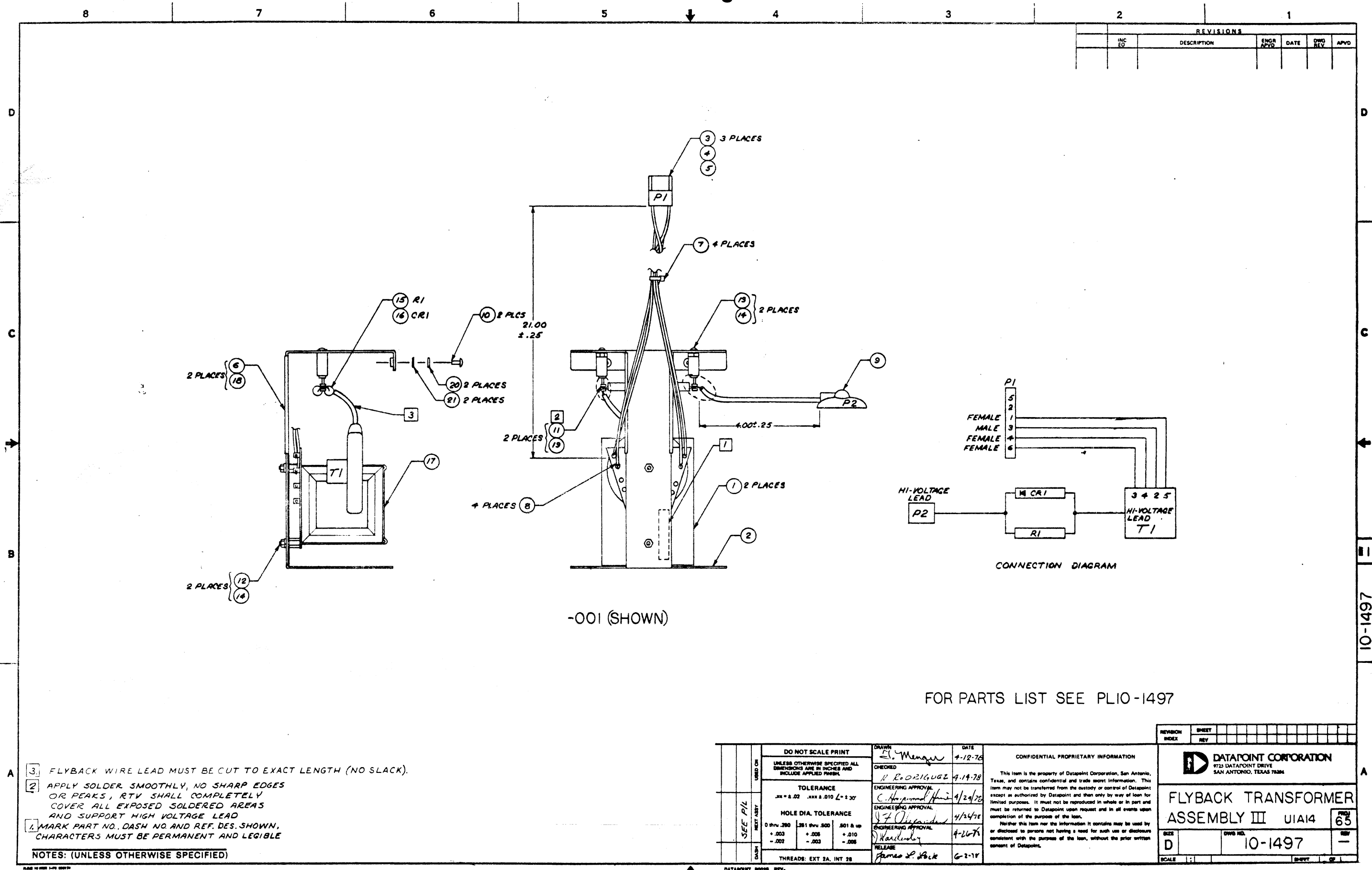


Figure 8-16.

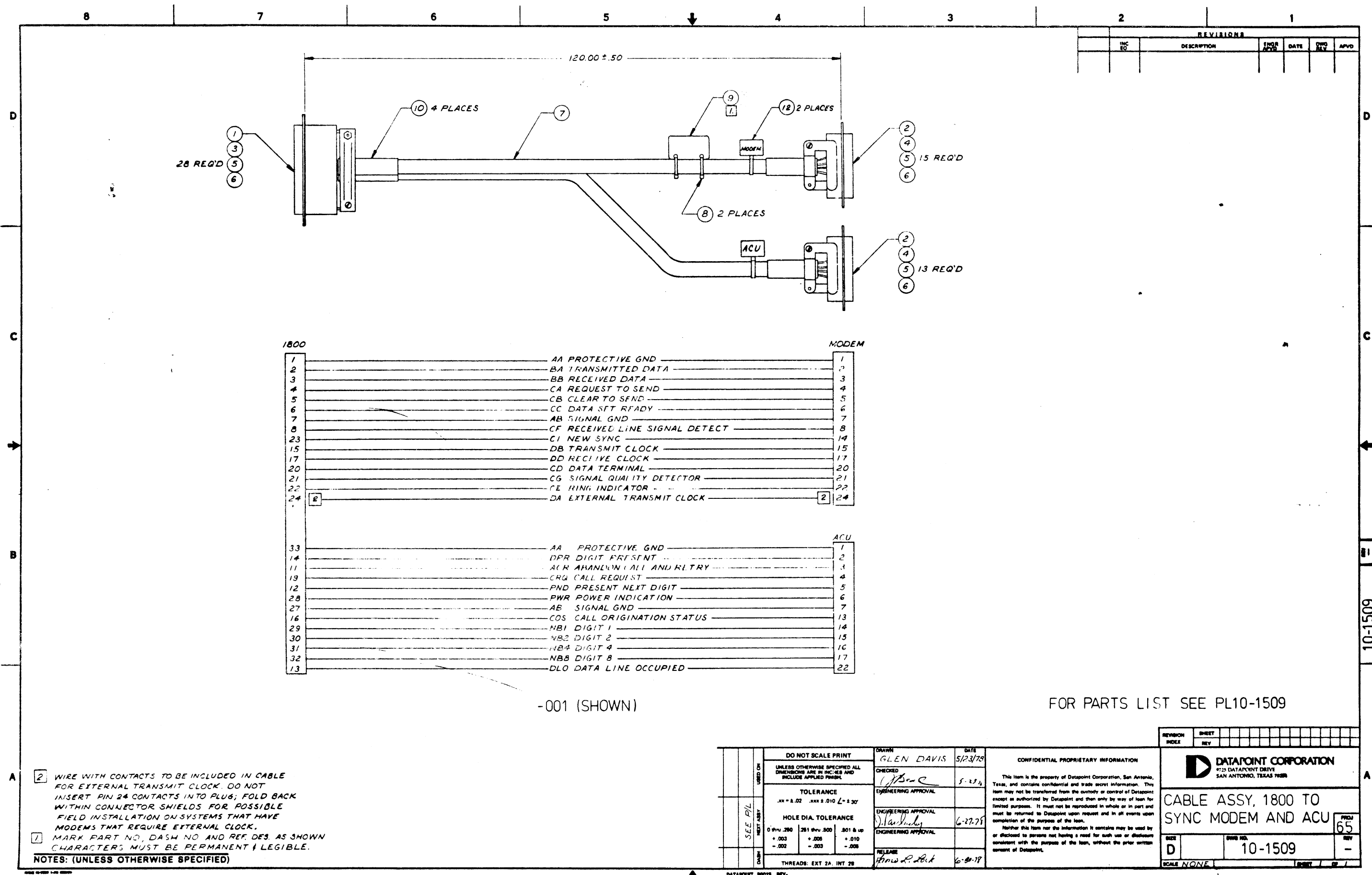
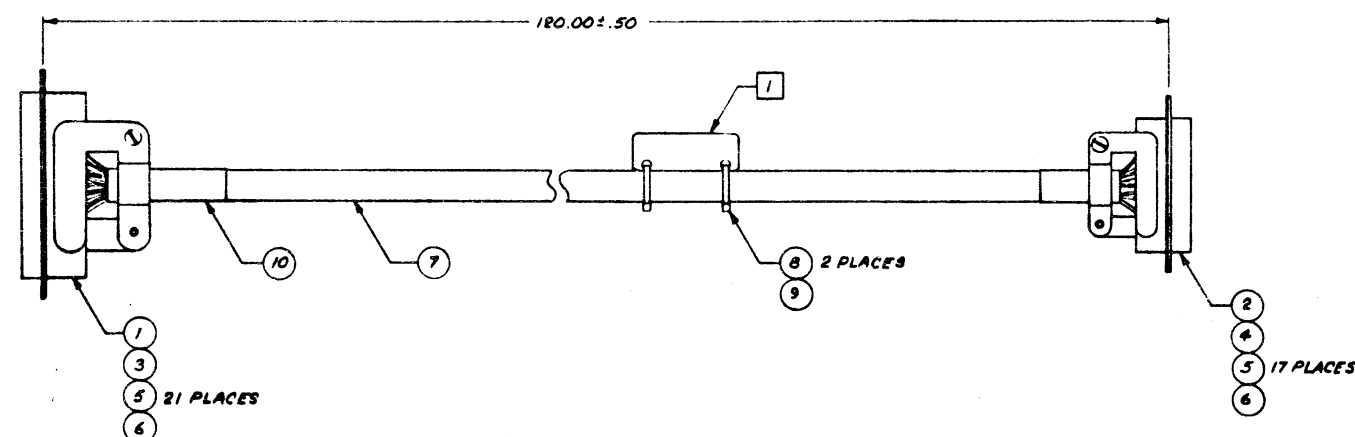


Figure 8-17.

REVISIONS					
REV	DESCRIPTION	DATE	BY	CHK	APP



-001 (SHOWN)

1800		MODEM
1	AA PROTECTIVE GND	1
2	BA TRANSMITTED DATA	2
3	BB RECEIVED DATA	3
4	CA REQUEST TO SEND	4
5	CB CLEAR TO SEND	5
6	CC DATA SET READY	6
7	AB SIGNAL GND	7
8	CF RECEIVED LINE SIGNAL DETECT	8
12	SCF SECONDARY CARRIER DETECT	12
13	SCB SECONDARY CLEAR TO SEND	13
14	SBA SECONDARY TRANSMITTED DATA	14
16	SBB SECONDARY RECEIVED DATA	16
19	SCA SECONDARY REQUEST TO SEND	19
20	CD DATA TERMINAL READY	20
21	CG SIGNAL QUALITY DETECT	21
22	CE RING INDICATOR	22
23	CH RATE SELECT	23
15	XMIT CLK (IN)	
17	RCV CLK (I)	
34	INT RCV CLK (INT)	
35	INT XMIT CLK (OUT)	

FOR PARTS LIST SEE PLIO-1510

7 MARK PART NO., DASH NO. AS SHOWN
CHARACTERS MUST BE PERMANENT & LEGIBLE

NOTES: (UNLESS OTHERWISE SPECIFIED)

DO NOT SCALE PRINT		DATE	5-12-78
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH.		CHECKED	5-28-78
TOLERANCE		ENGINEERING APPROVAL	
.XX ± .02 .XXX ± .010 L ± .30"		ENGINEERING APPROVAL	6-27-78
HOLE DIA. TOLERANCE		ENGINEERING APPROVAL	
0 thru .250 ± .003 .251 thru .500 ± .008 .501 & up ± .010		RELEASE	6-30-78
THREADS: EXT 2A INT 2B			
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Neither this item nor the information it contains may be used by or disclosed to persons not having a need for such use or disclosure consistent with the purpose of the loan, without the prior written consent of Datapoint.			
DATAPOINT CORPORATION 712 DATAPoint DRIVE SAN ANTONIO, TEXAS 78244		CABLE ASSY 1800 TO ASYNC MODEM W/REV CHANNEL	
SIZE	D	DWG NO.	10-1510
SCALE	NONE	SHEET	65

Figure 8-18.

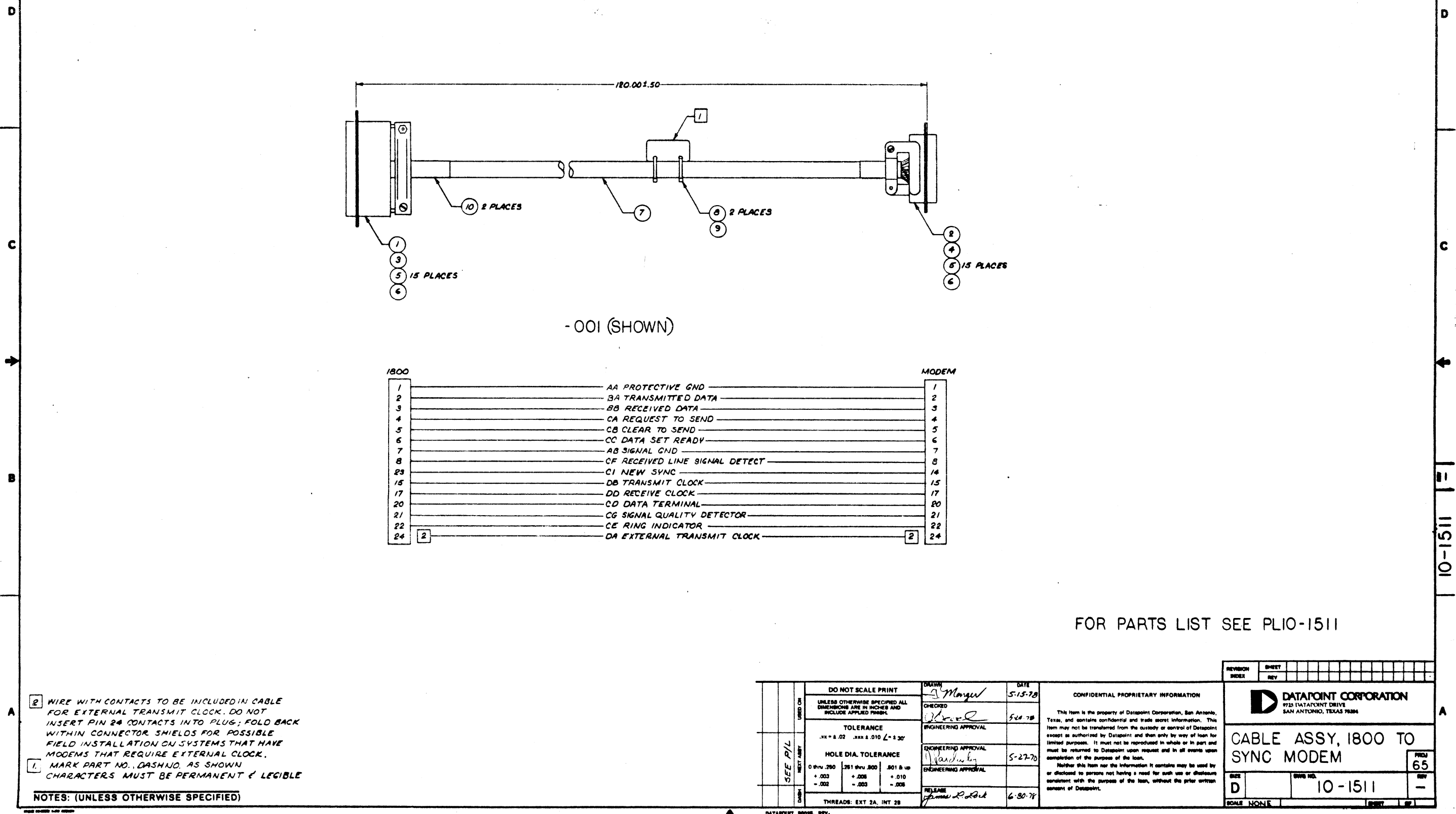


Figure 8-19.

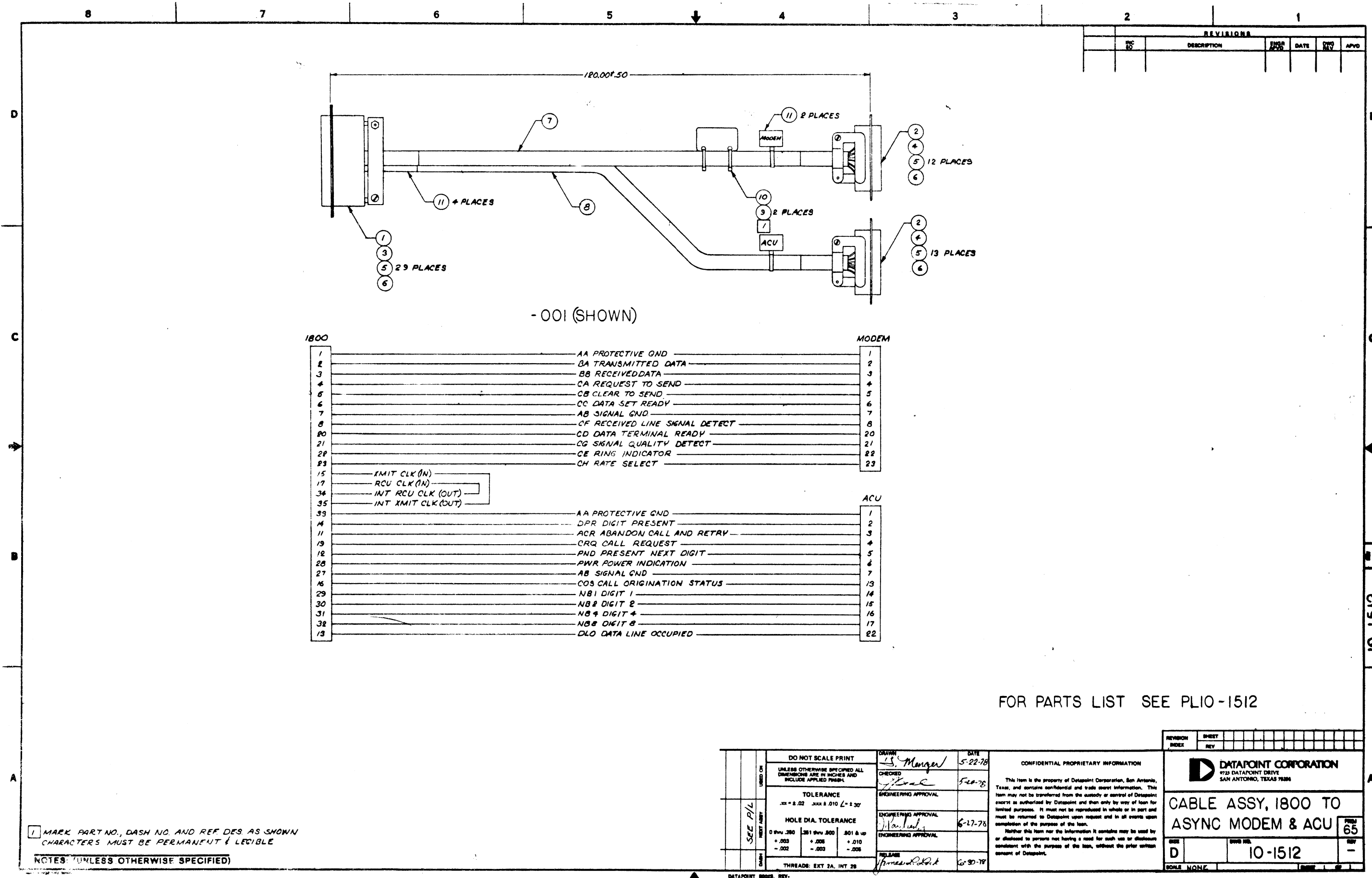
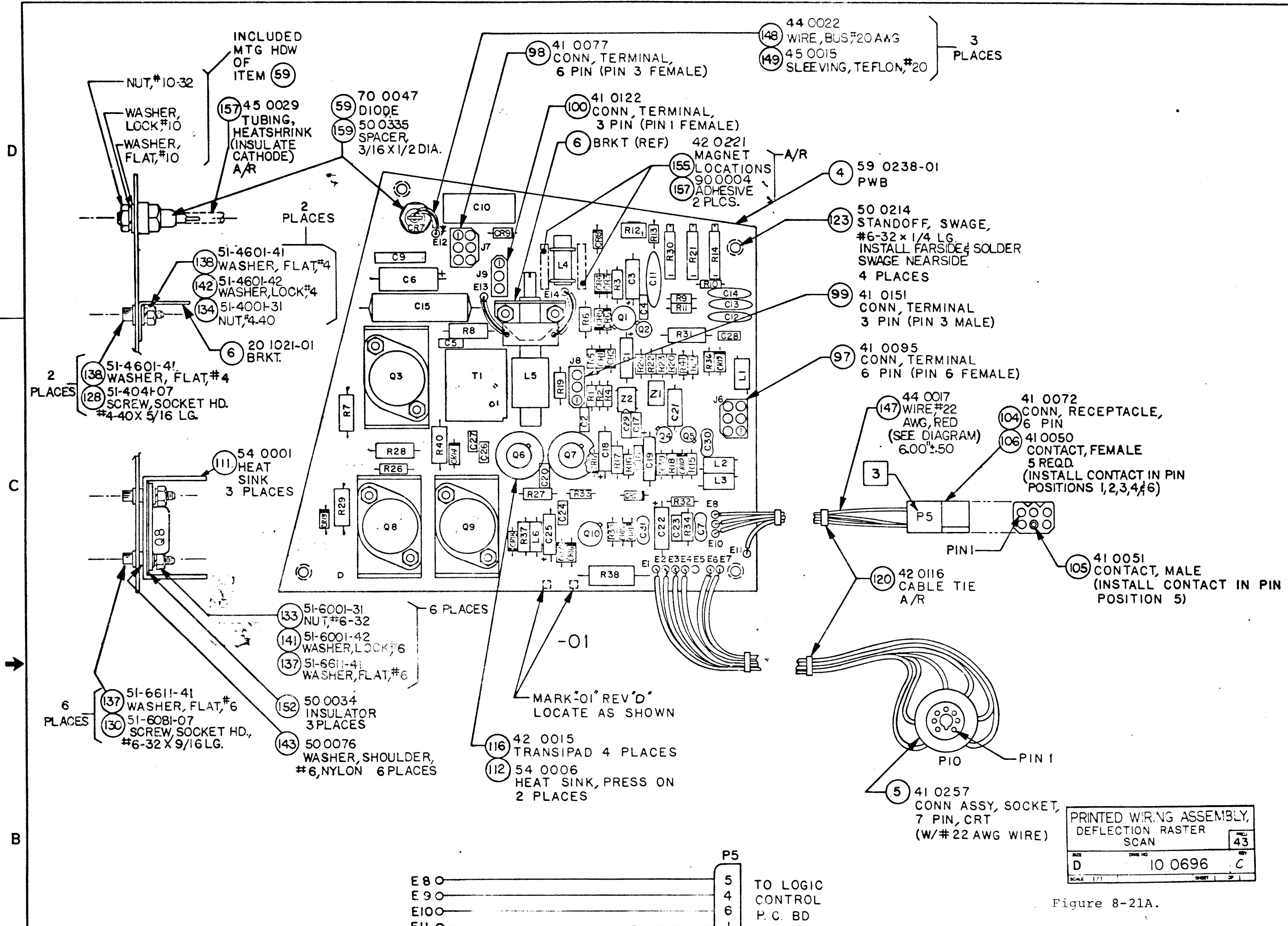
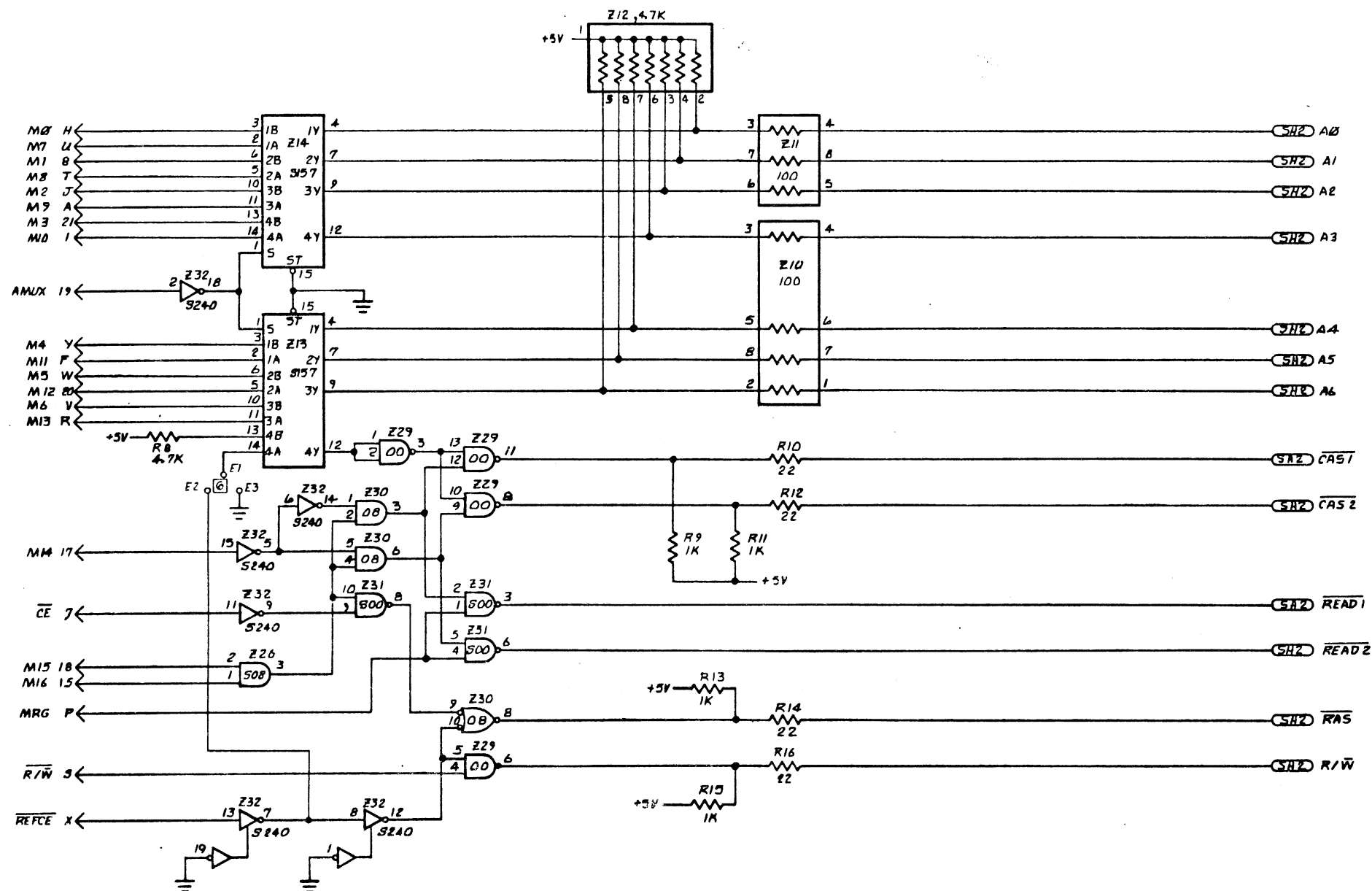
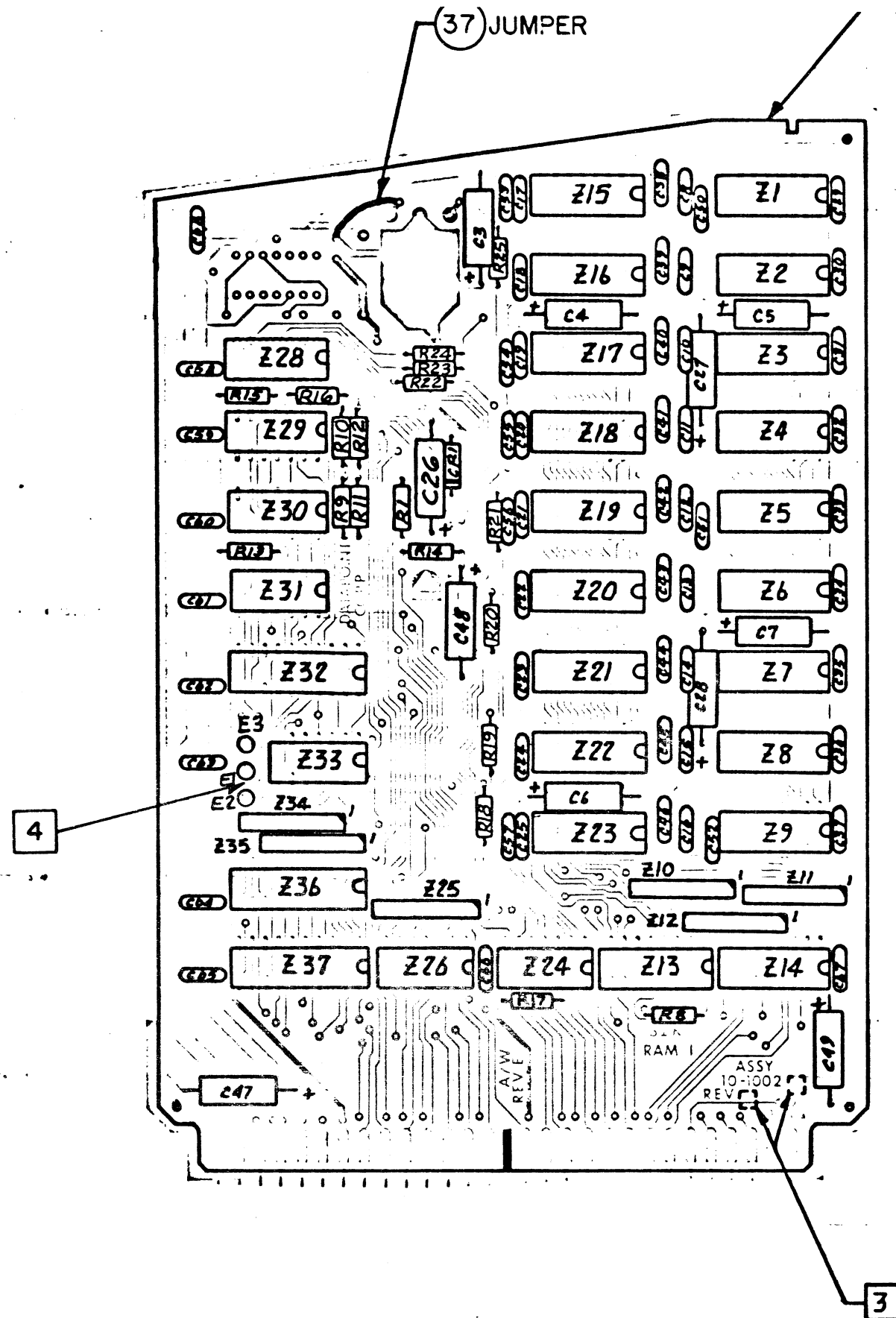


Figure 8-20.



TAB REV	INC	REV	DESCRIPTION	ENG	DATE	DWG	APVD
			ENG. CHANGE		5/4/77	C	ZSC
21312			ADDED-002 TO NOTE 4 G.P. 20-4-8-77		4-4-77	D	1-10-73 ZSC

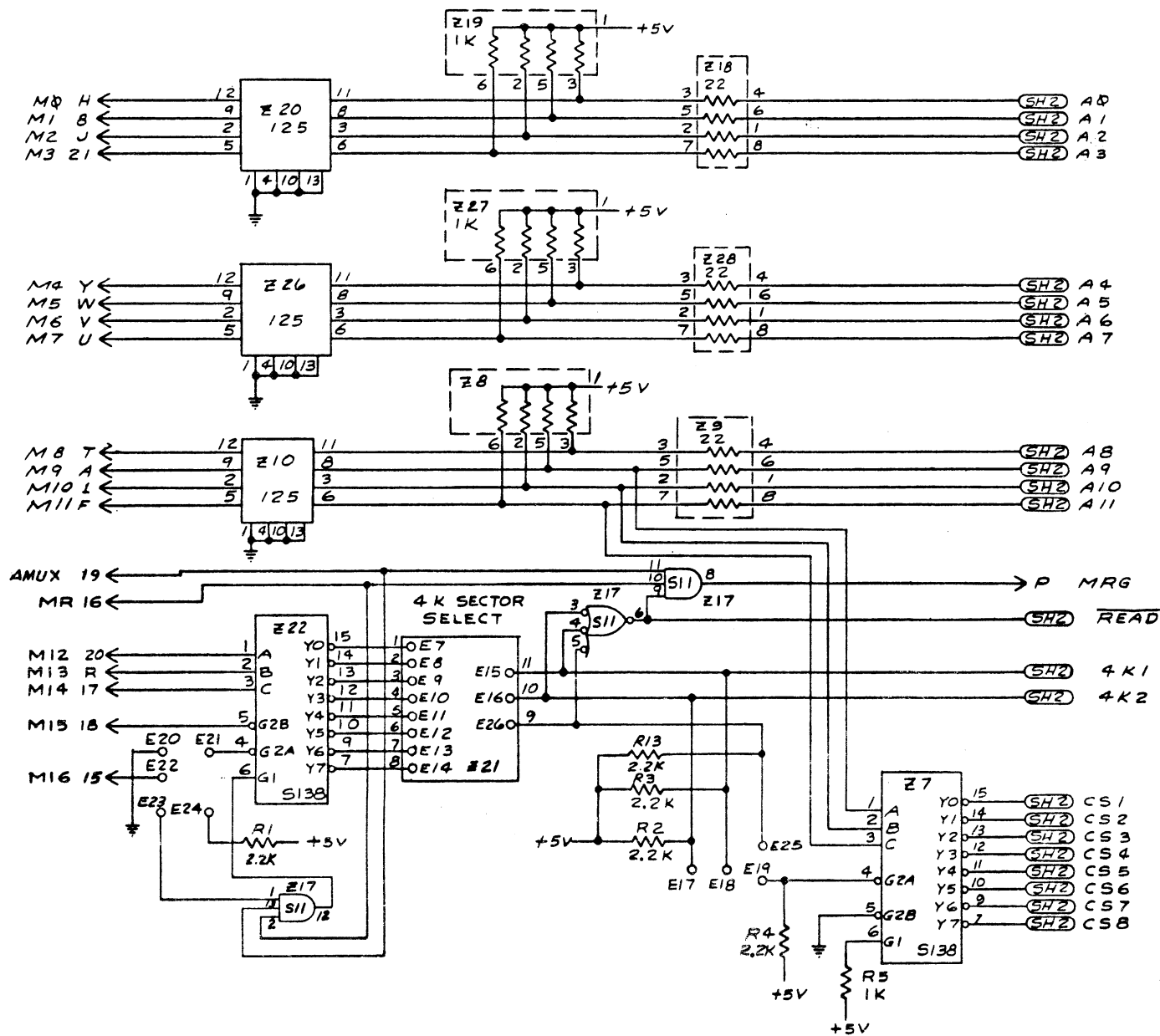




D DATAPOINT CORPORATION 725 DATAPOINT DRIVE SAN ANTONIO, TEXAS 78248			
PRINTED WIRING ASSEMBLY, 32 K RAM I			FIG. 64
REV. D	REV. 10-1002	REV. E	
SCALE 1:1			

Figure 8-22A.

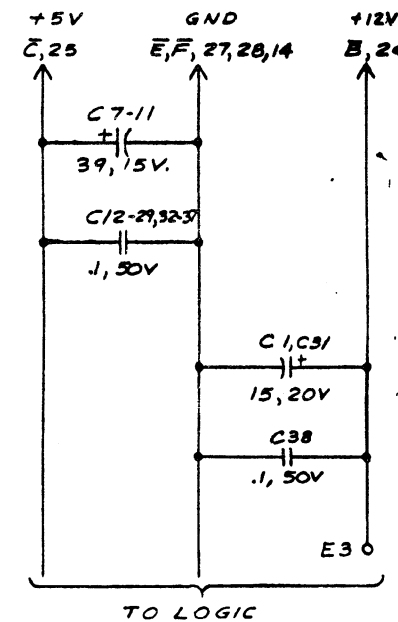
TAB REV		REVISIONS			
INC	ED	DESCRIPTION	ENGR	DATE	APVD
		PROD REL. JAW.		5-577	A



REF. DES.	TYPE	INPUT	OUTPUT
Z25	S04	3	4
Z25	S04	5	6
Z25	S04	9	8
Z25	S04	11	10
Z25	S04	13	12
Z29	125	4,5	6
Z29	125	10,9	8
Z29	125	12,13	11

JUMPER CHART			
-001	-002	FROM	TO
E20	E21	E20	E21
E22	E23	E23	E24
E19	E25	E19	E25
E7	E26	E14	E26

E26	
Q1	
Z32	Z5
C39	C2
R13	50, 10K
LAST	NOT USED



5. ALL RESISTANCE VALUES IN OHMS, 1/4W, $\pm 5\%$.
4. ALL CAPACITANCE VALUES IN MICROFARADS.
3. LOGIC SYMBOLS PER USA-STD Y32-14, ELECTRONIC SYMBOLS PER USA-STD Y32.2-67
2. NUMBERS SHOWN BELOW REFERENCE DESIGNATION WITHIN LOGIC SYMBOLS ARE SEGMENTS OF VENDOR PART NUMBER DESCRIBED IN PARTS LIST.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATION PREFIX WITH UNIT AND/OR ASSEMBLY DESIGNATION.

NOTES: (UNLESS OTHERWISE SPECIFIED)

DO NOT SCALE PRINT		DATE
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH.	CHECKED	4/14/76
TOLERANCE	ENGINEERING APPROVAL	5-577
HOLE DIA. TOLERANCE	ENGINEERING APPROVAL	5-577
THREADS: EXT 2A, INT 2B	RELEASE	5-6-77

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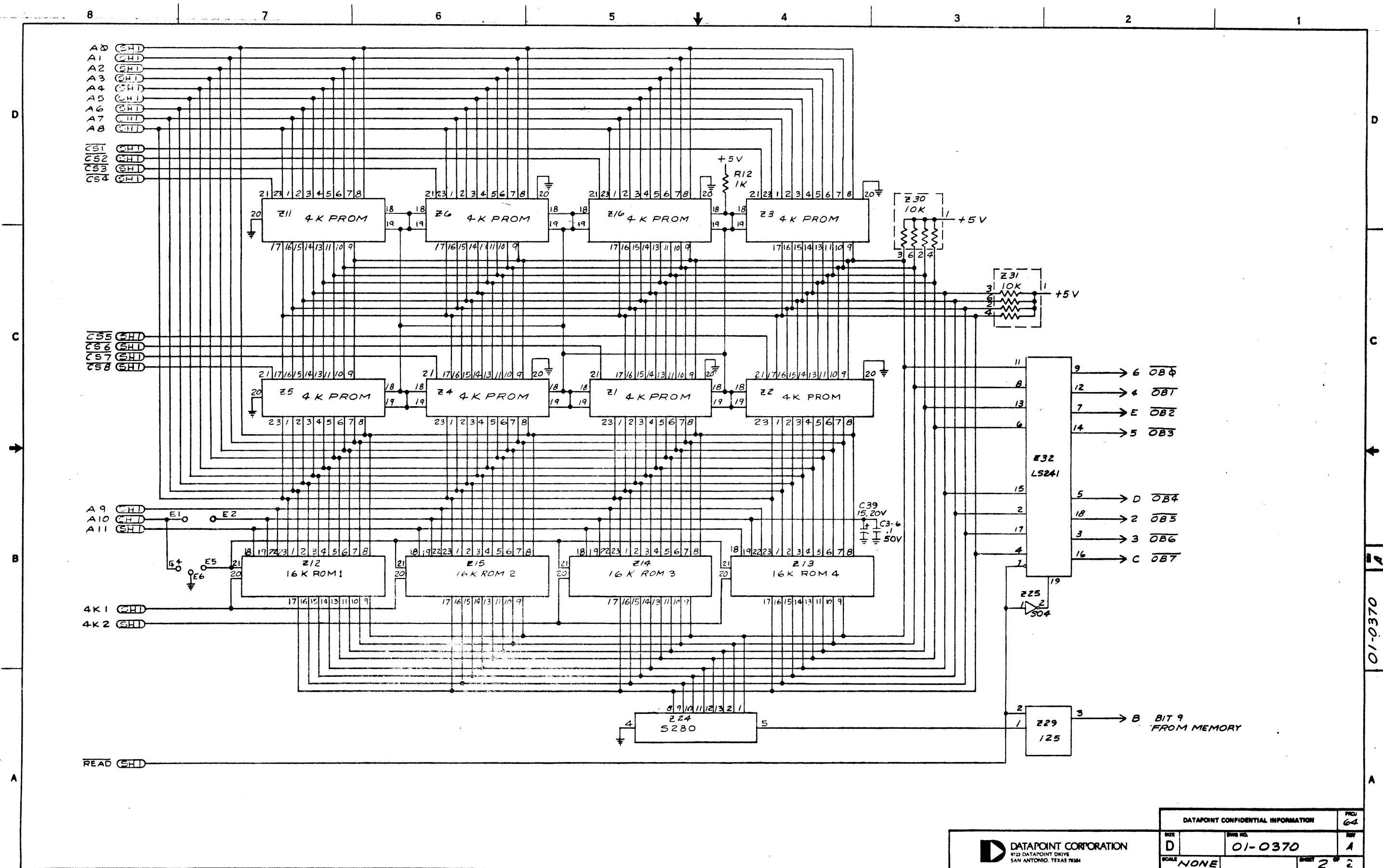
Neither this item nor the information it contains may be used by or disclosed to persons not having a need for such use or disclosure consistent with the purpose of the loan, without the prior written consent of Datapoint.

REVISION	SHEET	1	2
INDEX	REV	A	A

DATAPOINT CORPORATION	
733 DATAPoint DRIVE	
SAN ANTONIO, TEXAS 78241	

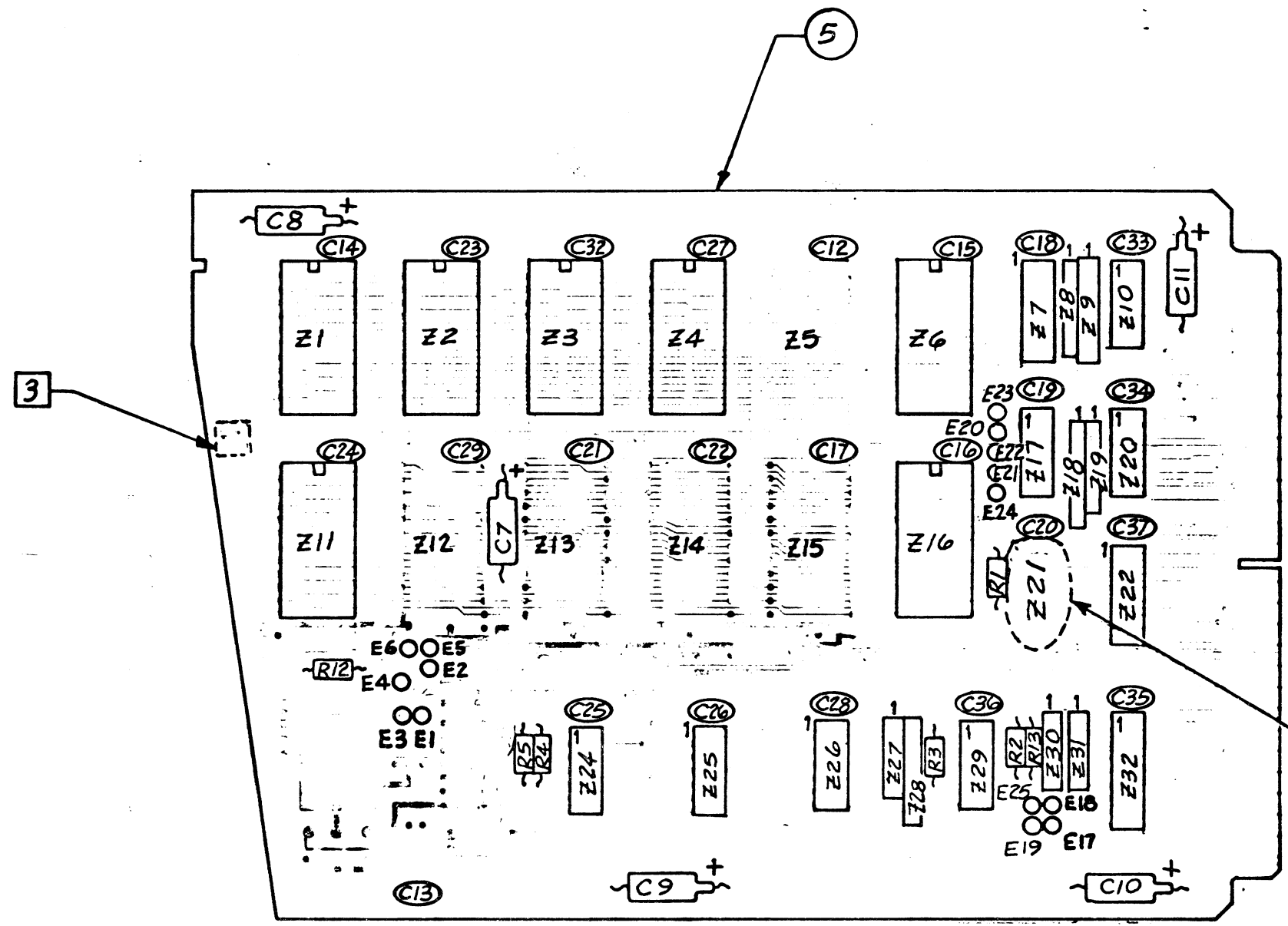
SCHEMATIC DIAGRAM, MEMORY	
8K ROM I	
SIZE	64
D	01-0370
SCALE	NON

Figure 8-23. (Sht. 1)



DATEPOINT CONFIDENTIAL INFORMATION			
SIZE	64	REV	1
D	01-0370	SCALE	NONE
2	2	2	2

Figure 8-23. (Sht. 2)



-001		-002	
FROM	TO	FROM	TO
E21	E20	E21	E20
E23	E22	E23	E24
E19	E25	E19	E25
E7	E26	E14	E26

1	E7
2	E8
3	E9
4	E10
5	E11
6	E12
7	E13
8	E14
9	E15
10	E16
11	E17
12	E18
13	E19
14	E20
15	E21
16	E22
17	E23
18	E24
19	E25
20	E26

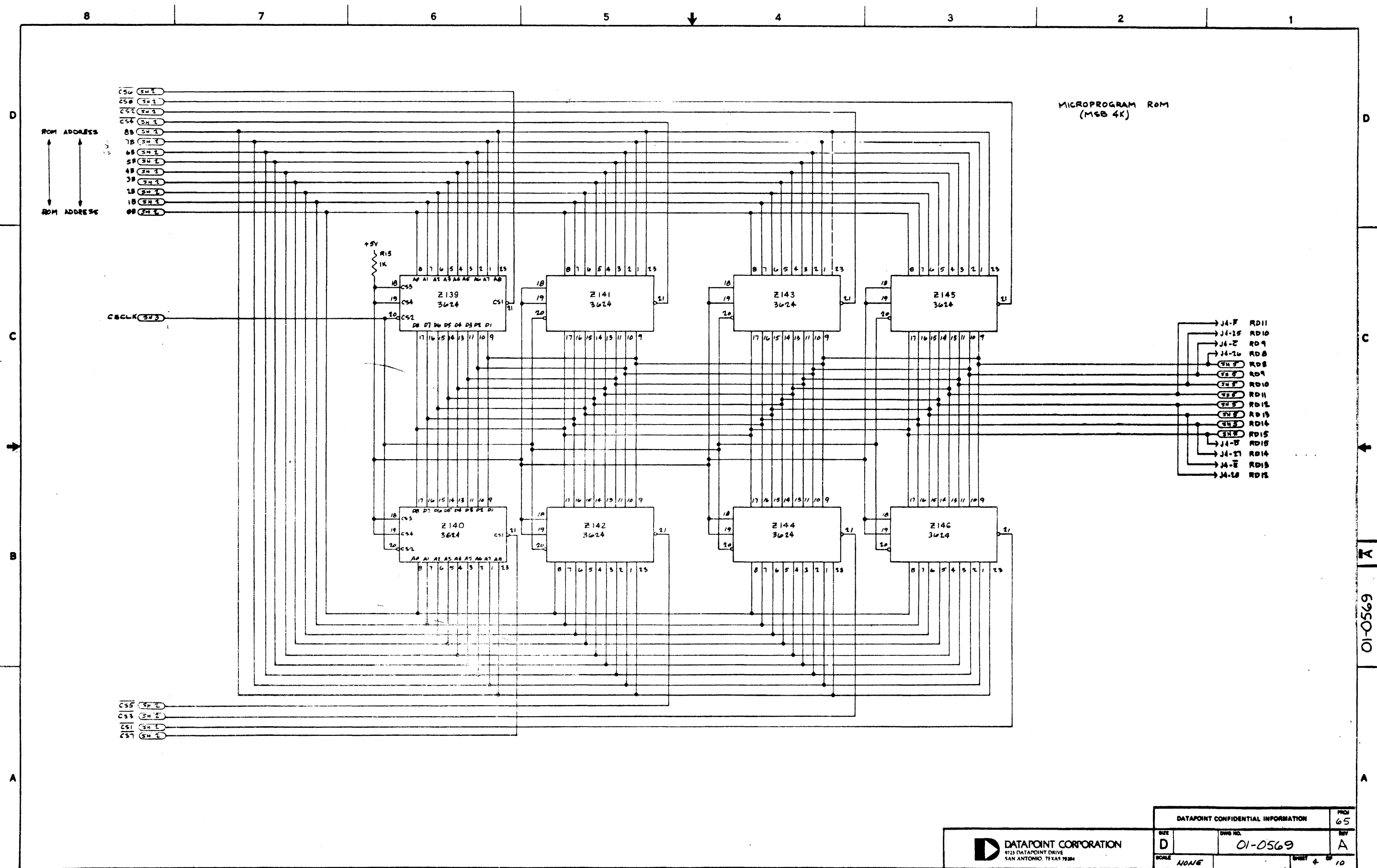
DETAIL "A"
SCALE IN NONE

SEE DETAIL "A"

-001 SHOWN

DATAPoint CORPORATION 7125 DATAPoint DRIVE SAN ANTONIO, TEXAS 78244			
PRINTED WIRING ASSEMBLY, MEMORY 8K ROM I			
SIZE	DATE	REV	QTY
D	10-1166	A	44
SCALE 1:1		SHEET 1 OF 1	

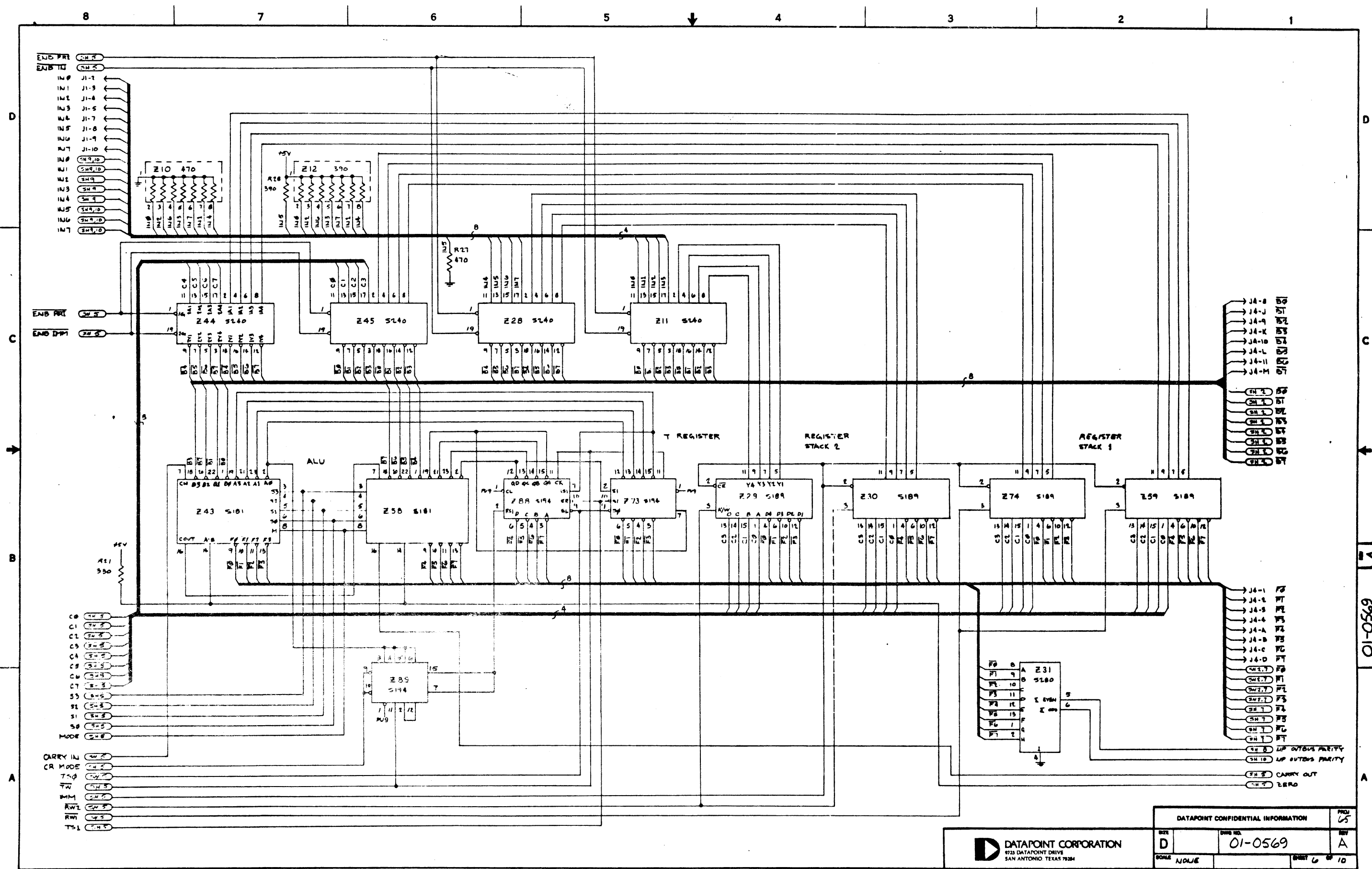
Figure 8-23A.



D DATAPoint CORPORATION
9723 DATAPoint DRIVE
SAN ANTONIO, TEXAS 78244

DATAPoint CONFIDENTIAL INFORMATION			PROJ
REV	DWG NO.	REV	65
D	01-0569	A	
SCALE	NONE	SHEET	4 OF 10

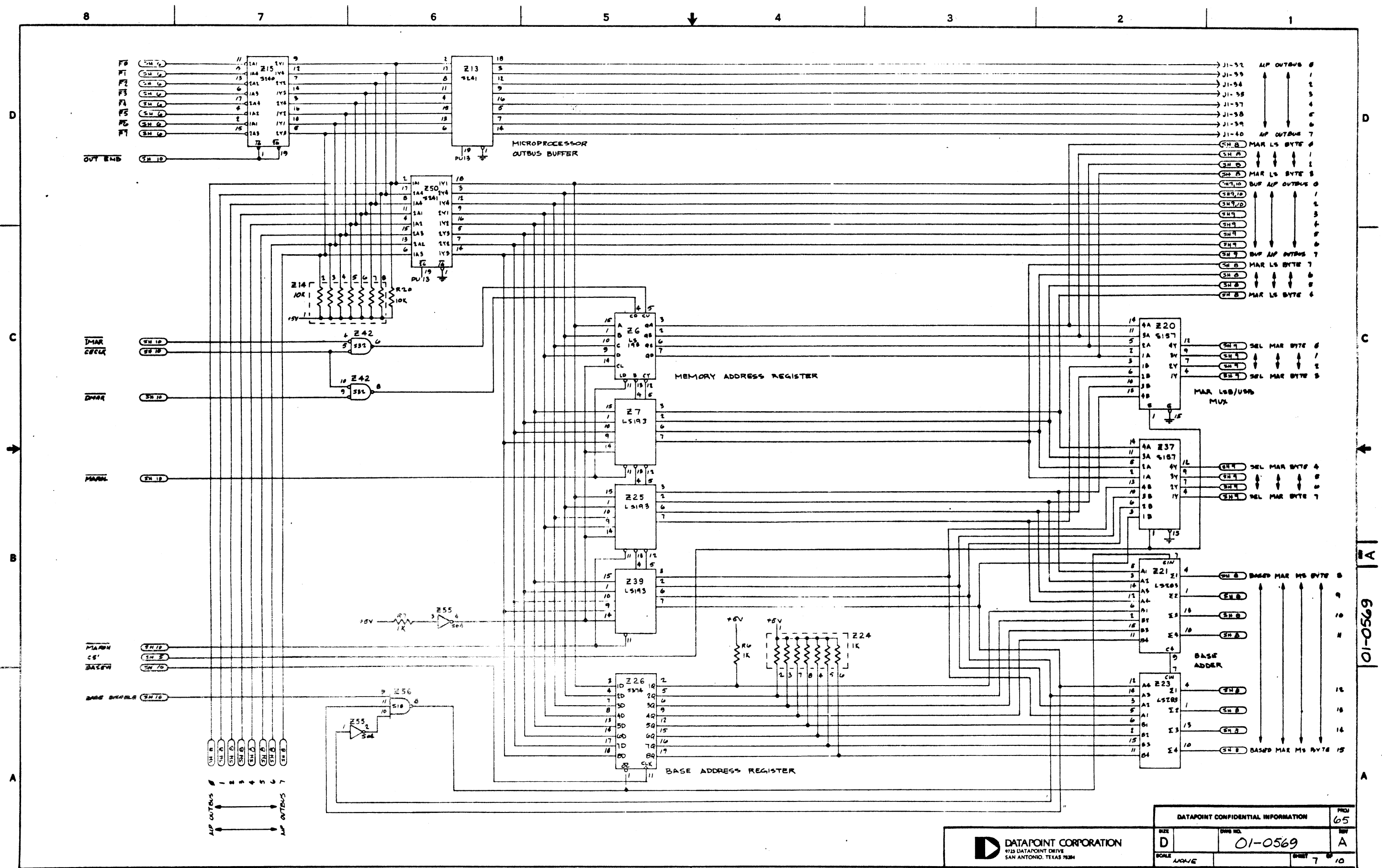
Figure 8-24. (Sht. 4)



DATAPoint CONFIDENTIAL INFORMATION				PROJ
REV	D	DATE	01-0569	US
SHEET	10	OF	10	

D DATAPoint CORPORATION
9735 DATAPoint DRIVE
SAN ANTONIO, TEXAS 78204

Figure 8-24. (Sht. 6)



D DATAPOINT CORPORATION
9723 DATAPoint DRIVE
SAN ANTONIO, TEXAS 78241

DATAPoint CONFIDENTIAL INFORMATION			PROJ
REV	DATE	01-0569	65
SCALE	AS SHOWN		A
		SHEET	7 10

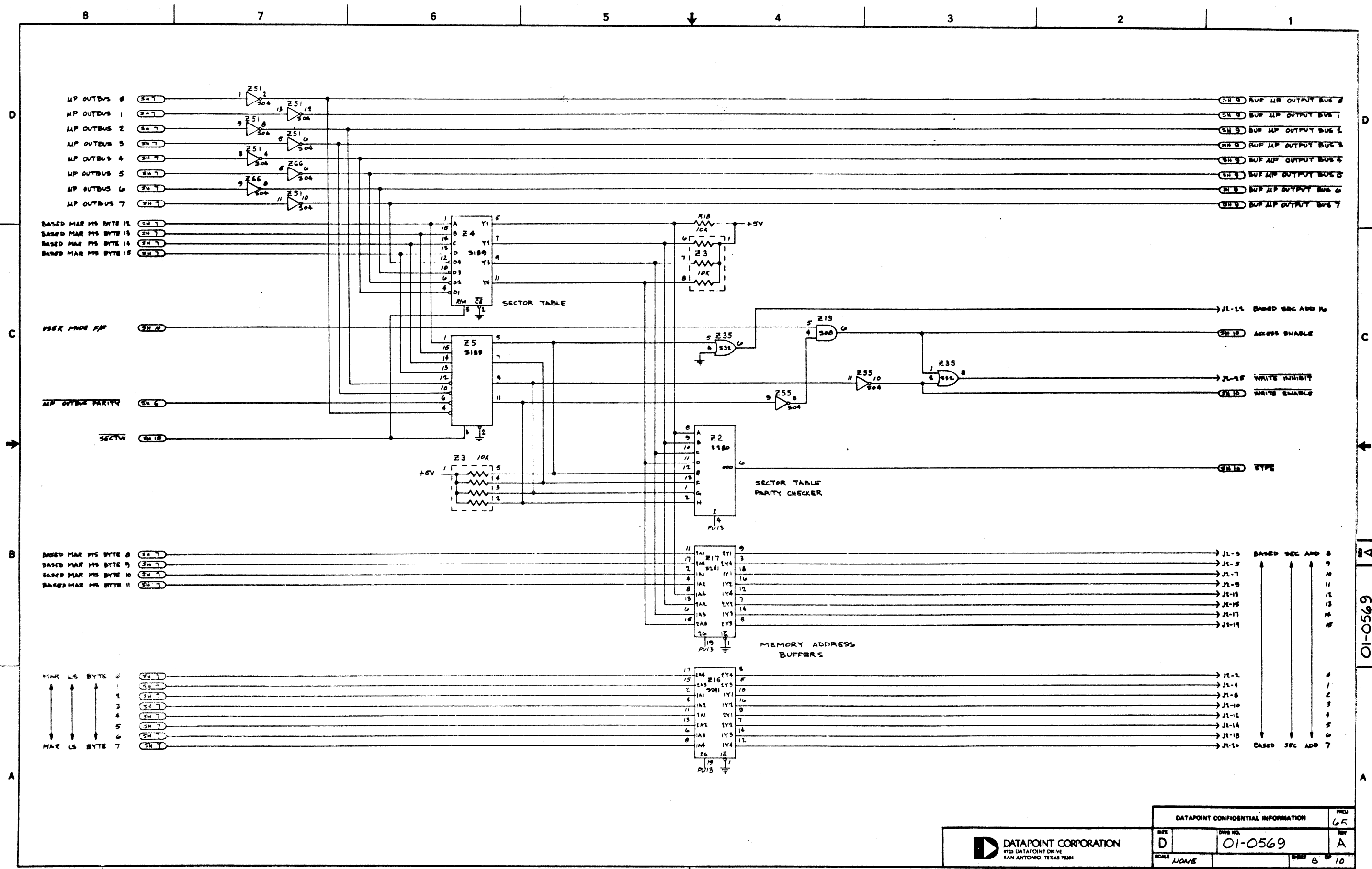


Figure 8-24. (Sht. 8)

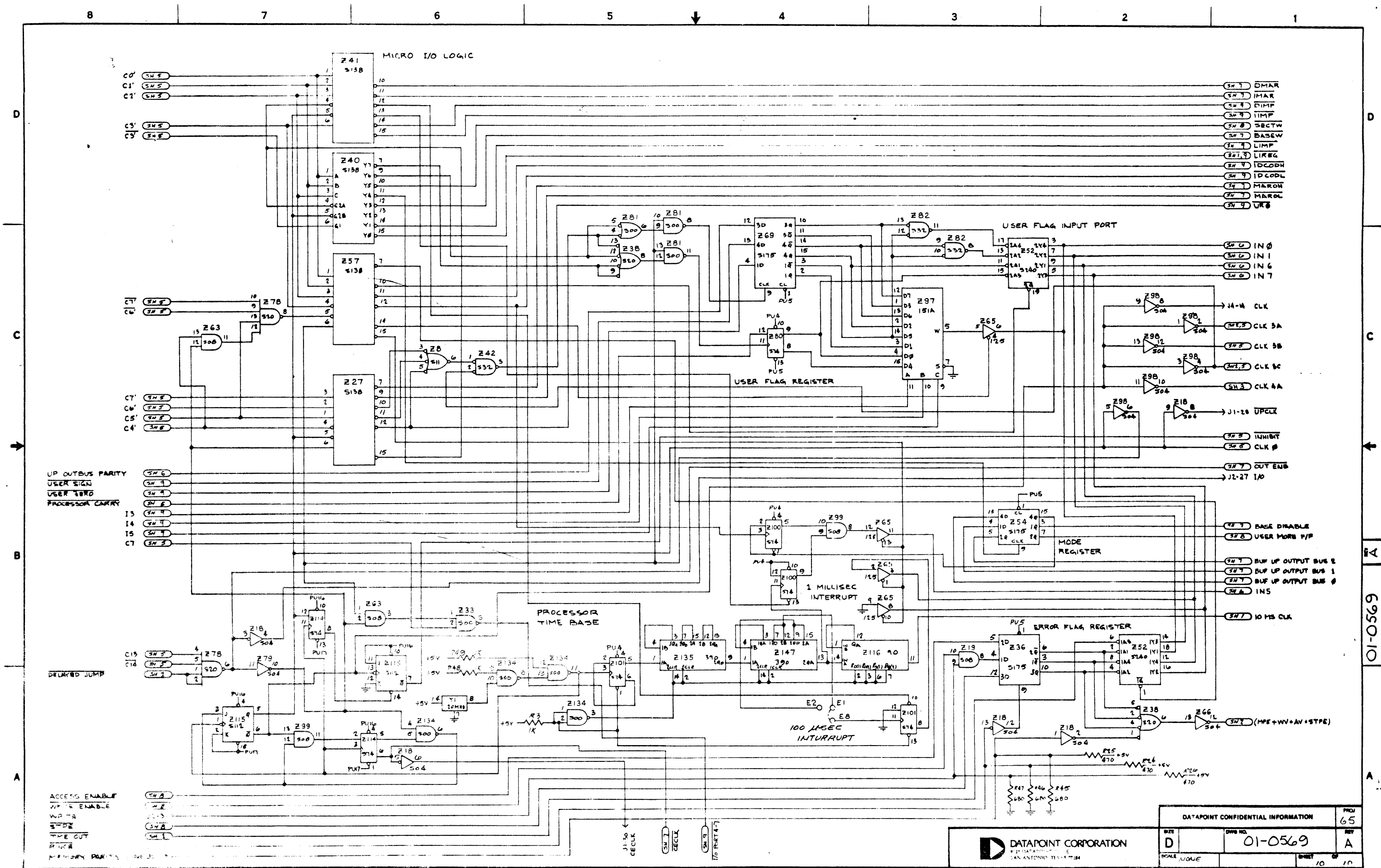
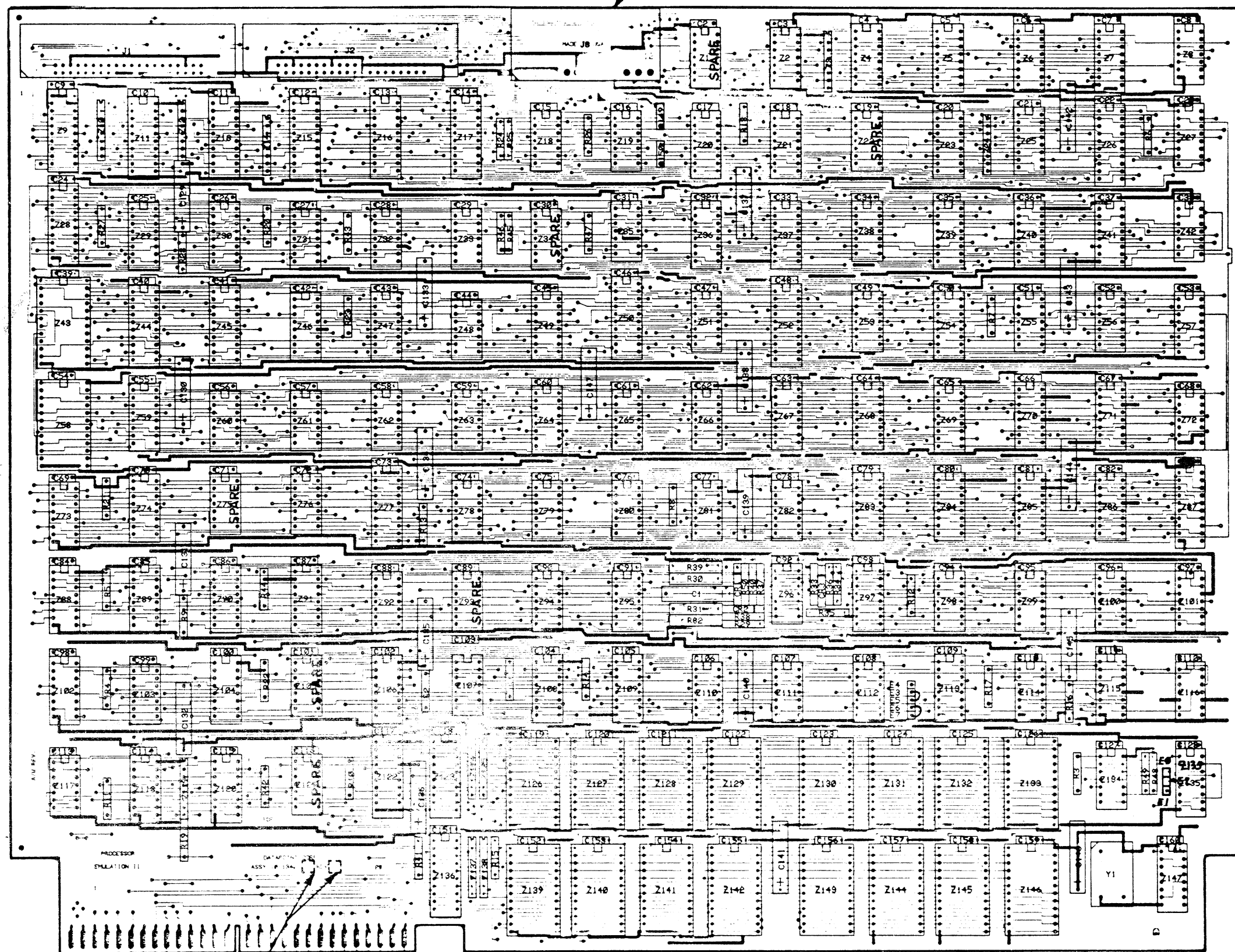


Figure 8-24. (Sht. 10)



JUMPER CHART		USE ITEM 8	
FROM	TO	FROM	TO
E1	E8	E2	E8
E3	E8	E3	E8
E6	E7	E6	E7

DATAPOINT CORPORATION
 2222 DATAPOINT DRIVE
 SAN ANTONIO, TEXAS 78244

**PRINTED WIRING ASSEMBLY,
 PROCESSOR/EMU BD II**

REV 65

SIZE D DWG NO. 10-1342 REV B

SCALE 1:1

Figure 8-24A.

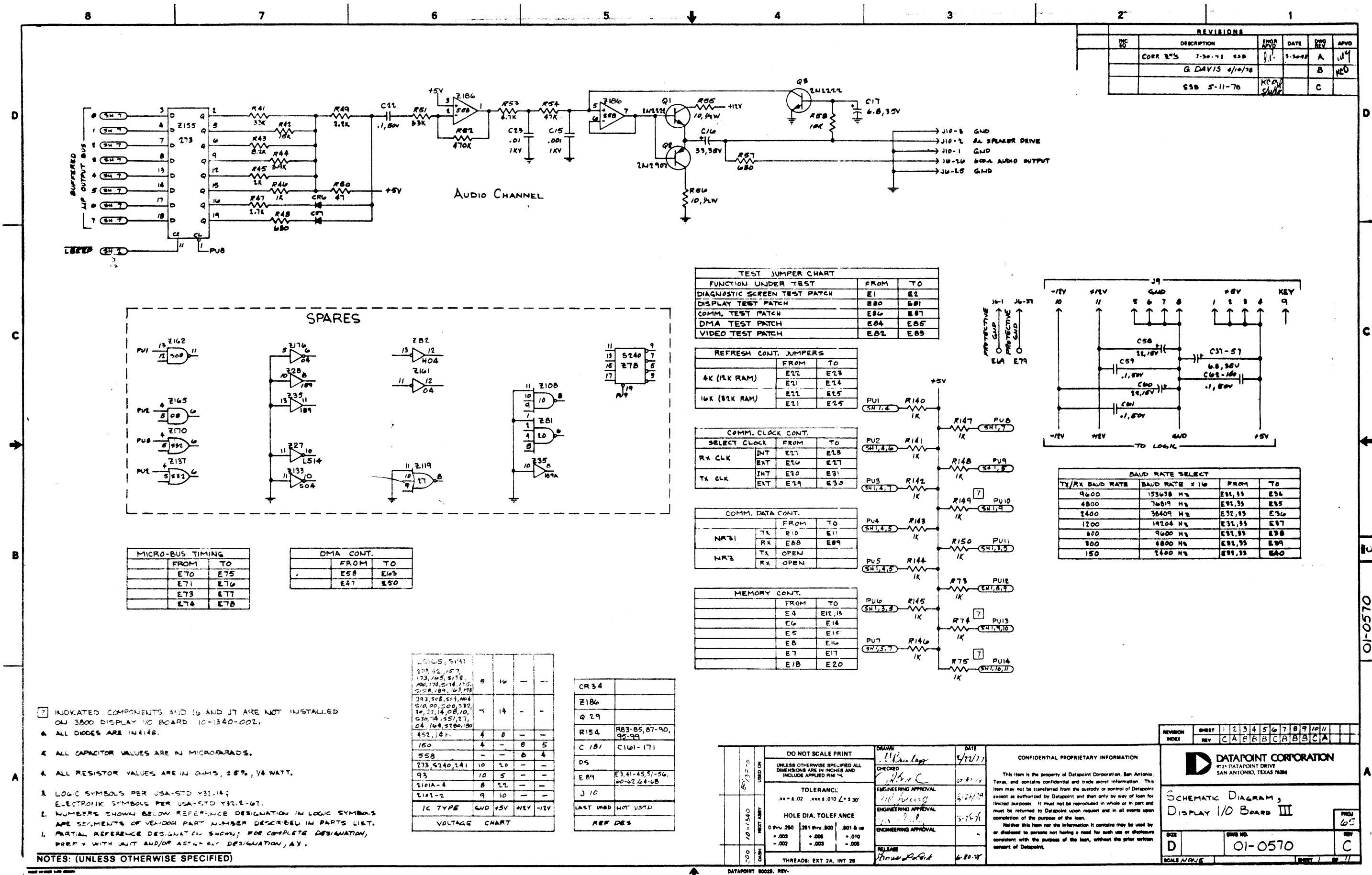
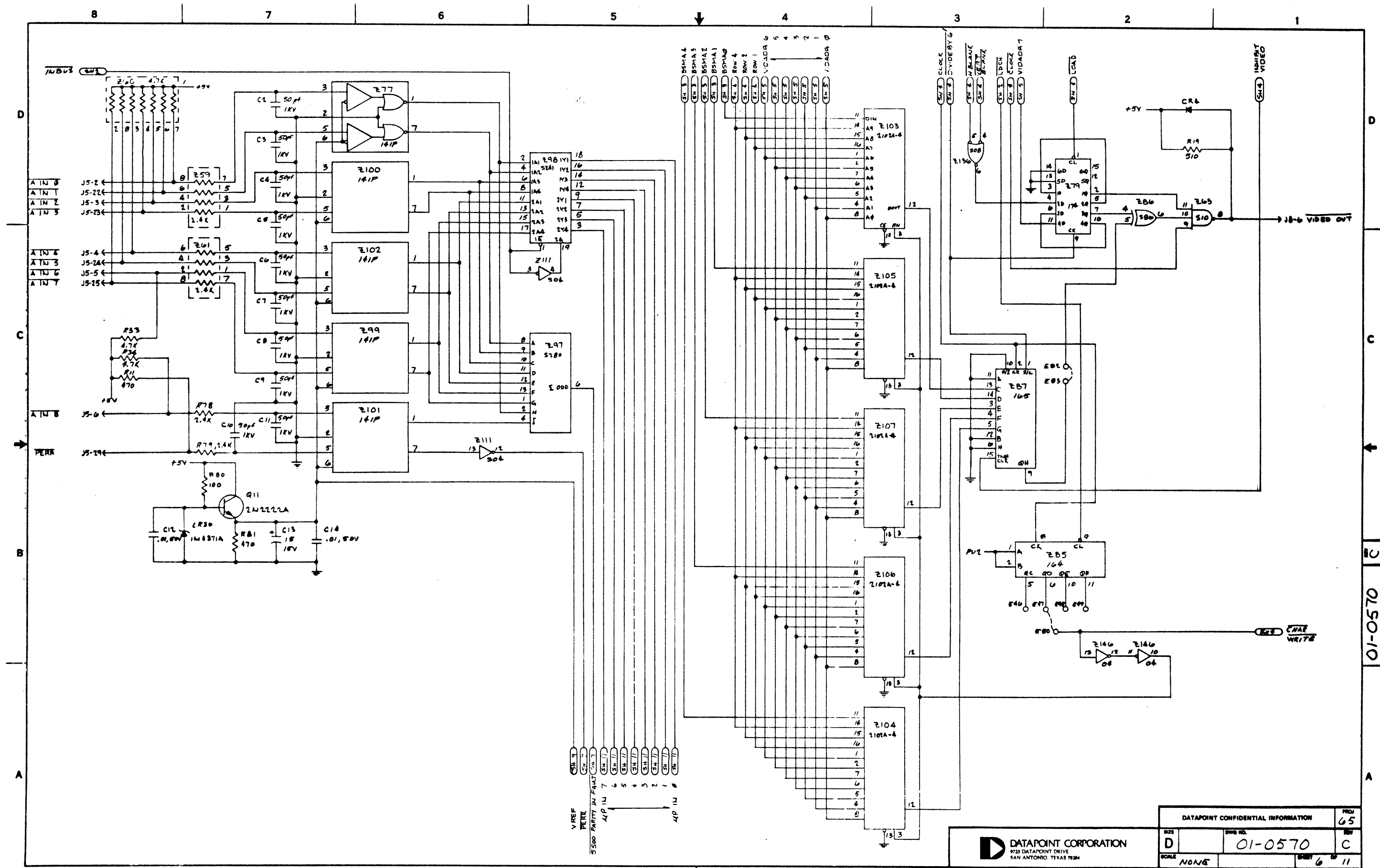


Figure 8-25. (Sht. 1)

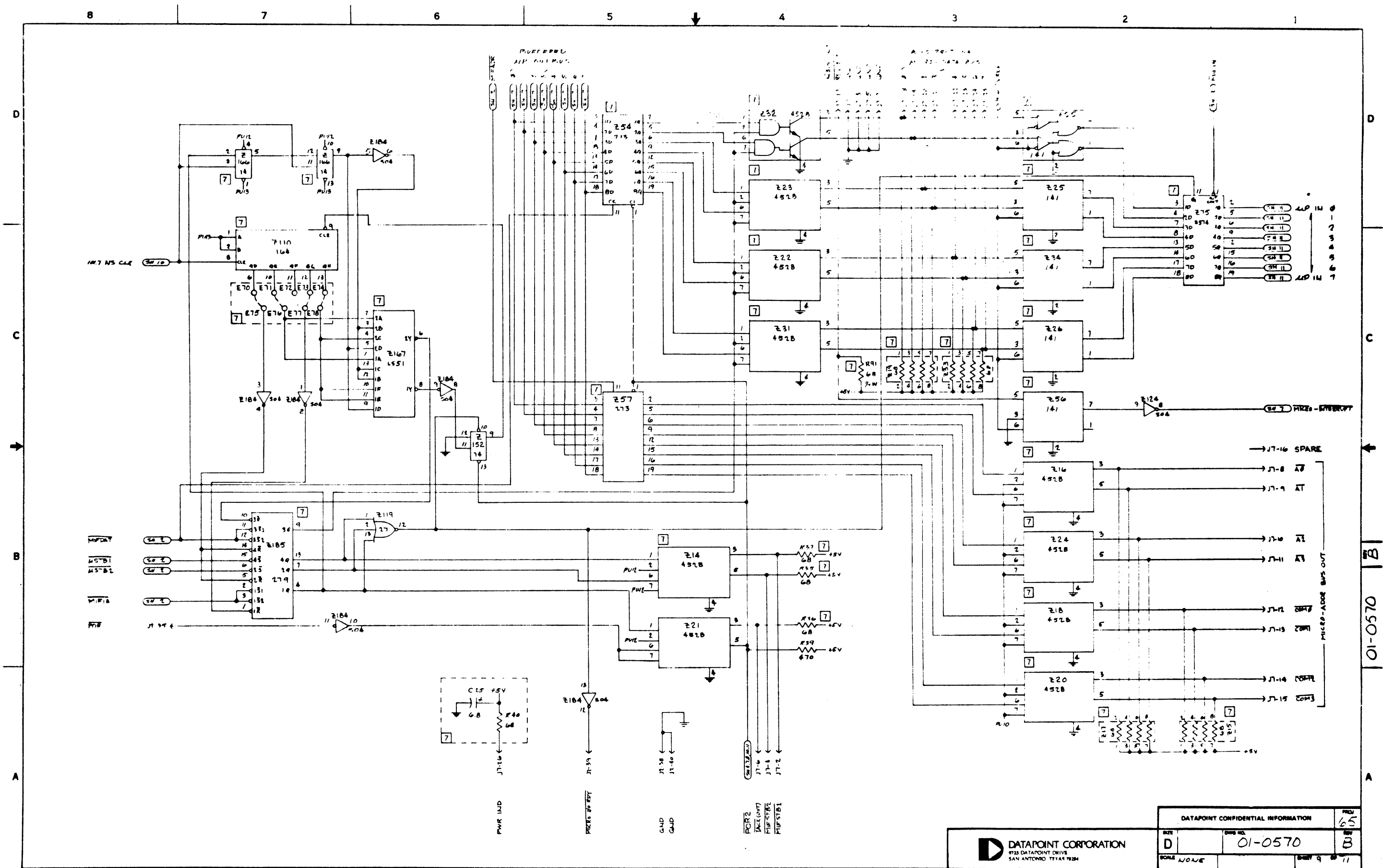




DATAPoint CORPORATION
9725 DATAPoint DRIVE
 SAN ANTONIO, TEXAS 78244

DATAPoint CONFIDENTIAL INFORMATION			REV
SIZE	D	DWG NO.	01-0570
SCALE	NONE	SHEET	6 OF 11

Figure 8-25. (Sht. 6)



D DATAPoint CORPORATION
 7133 DATAPoint DRIVE
 SAN ANTONIO, TEXAS 78204

DATAPoint CONFIDENTIAL INFORMATION		
REV	01-0570	REV
SCALE	1/1000	REV

Figure 8-25. (Sht. 9)



Figure 8-25. (Sht, 10)

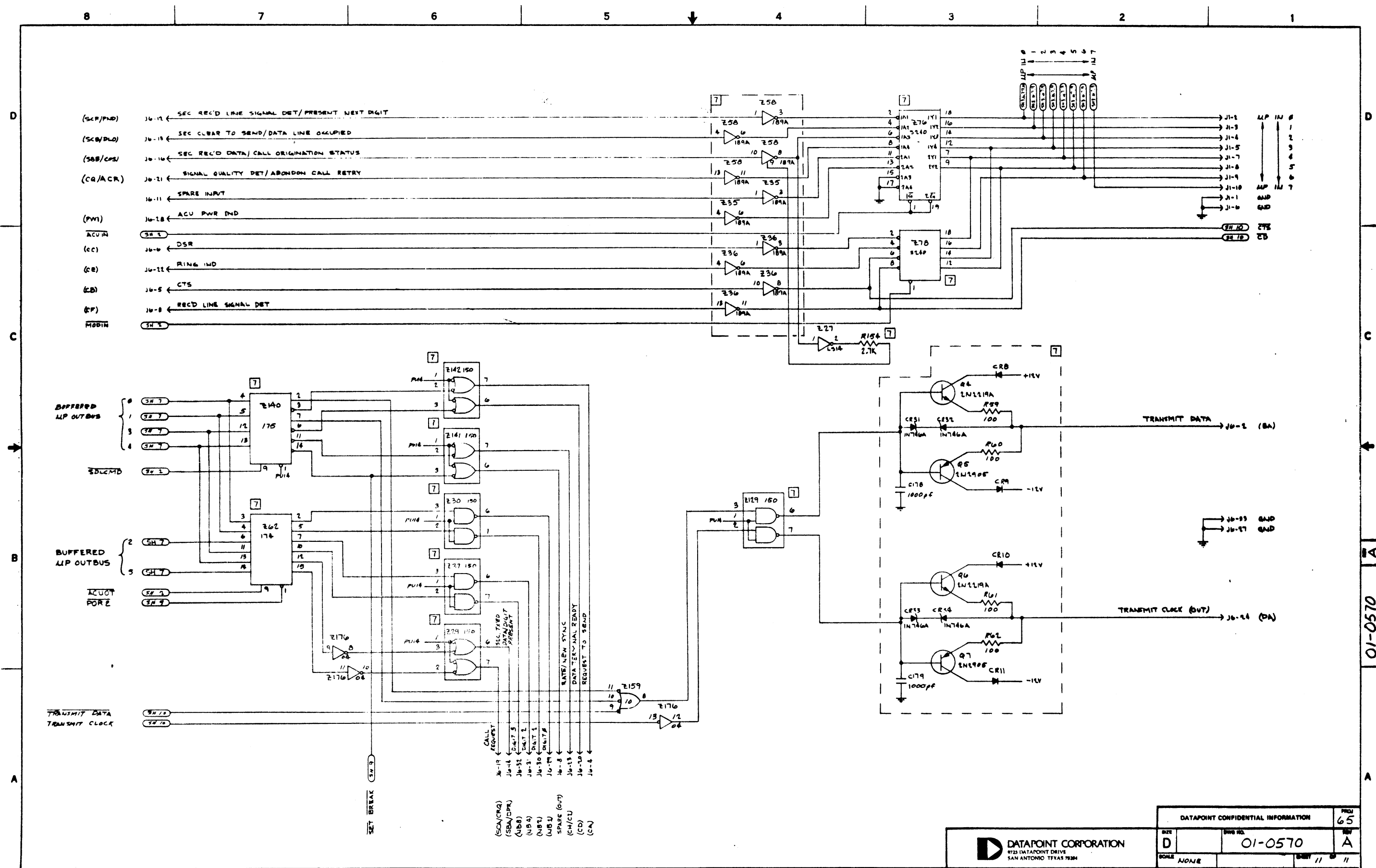
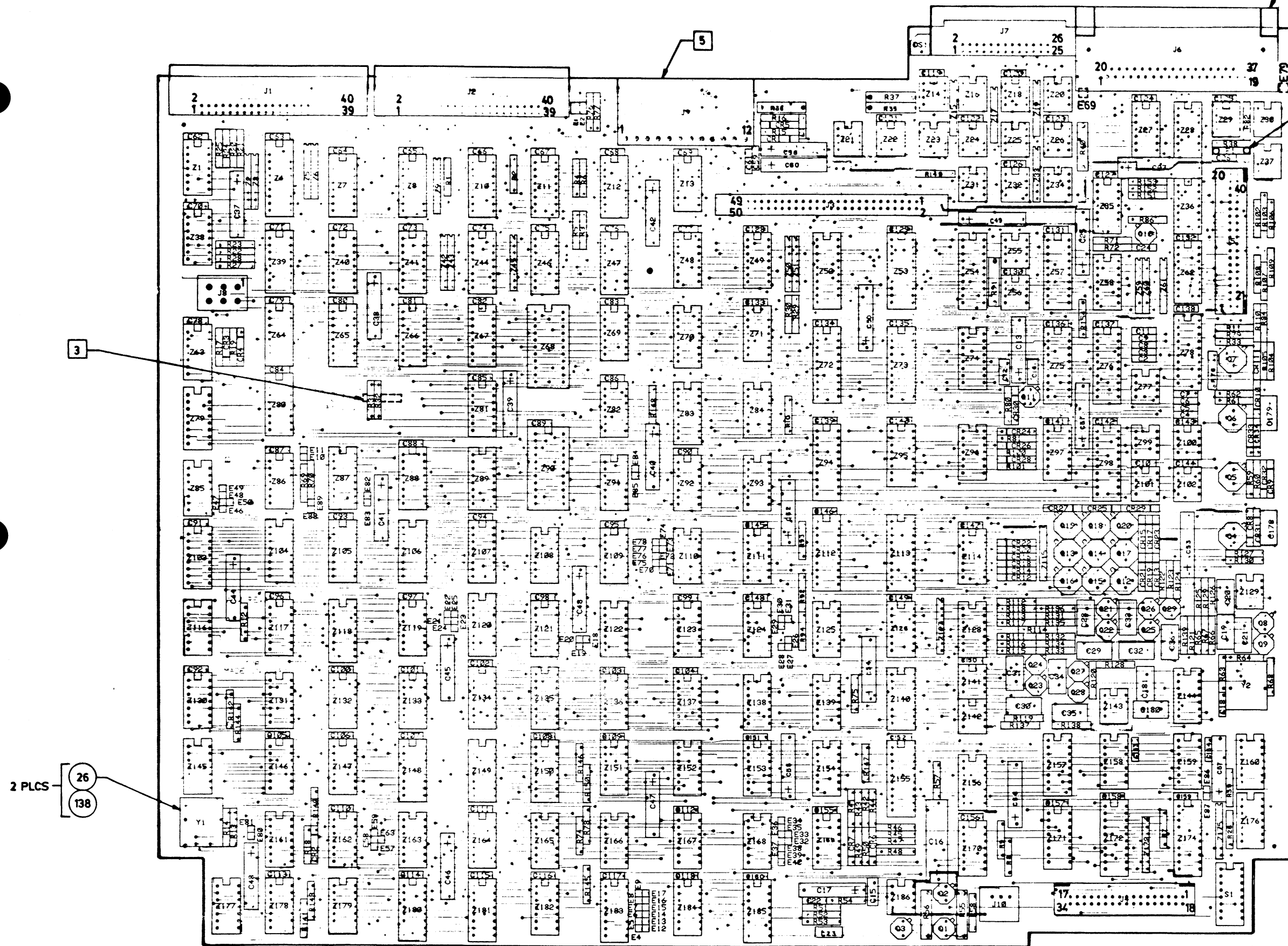


Figure 8-25. (Sht, 11)



-001 1800
-002 3800

E80	E81	
E86	E87	
E84	E85	
E82	E83	
E74	E78	
E73	E77	
E71	E76	
E70	E75	
E58	E63	
E47	E50	
E29	E30	
E26	E27	
E18	F20	
E8	E16	
E7	E17	
E6	E14	
E5	E15	
E4	E13	
E4	E12	
FROM	TO	USE ITEM

E33	E35	
E32	E35	
E22	E25	
E21	E25	
FROM	TO	USE ITEM
-001-002		
JUMPER CHART		

DATAPOINT CORPORATION
2222 DATAPoint DRIVE
SAN ANTONIO, TEXAS 78244

PRINTED WIRING ASSEMBLY,
DISPLAY I/O BD. II

REV. 65

D 10-1340 D

Figure 8-25A.

FOR PARTS

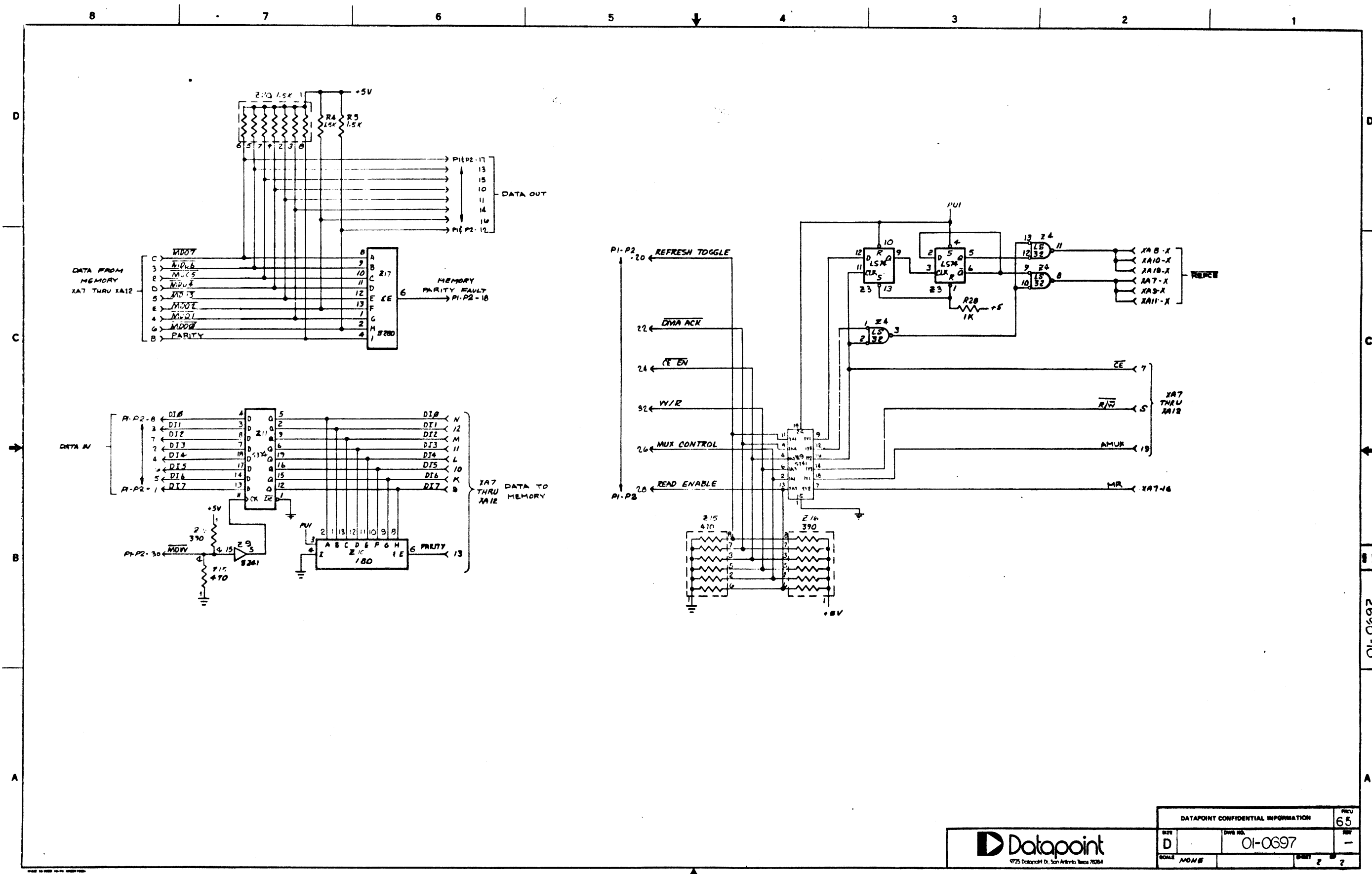


Figure 8-26. (Sht. 2)

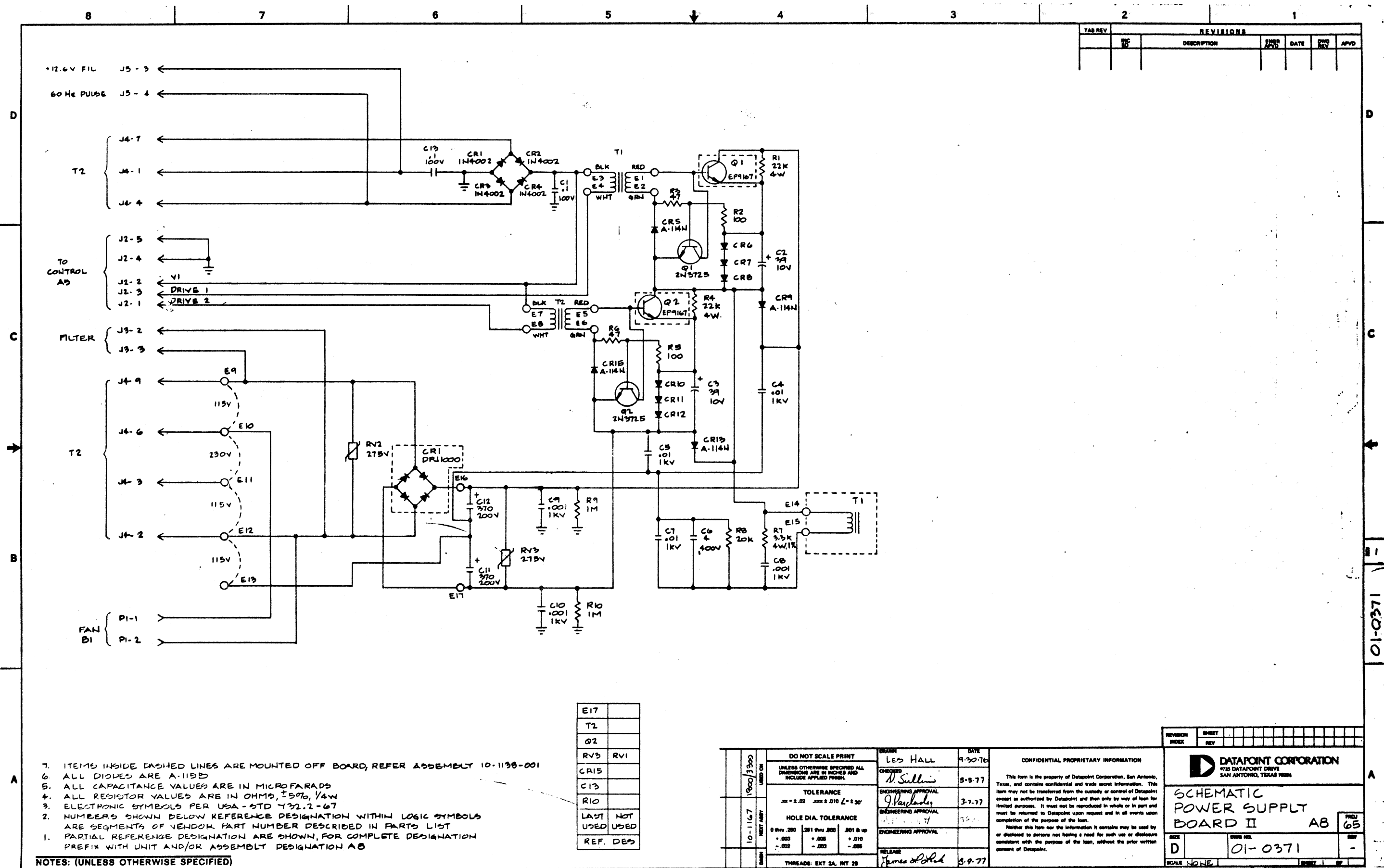
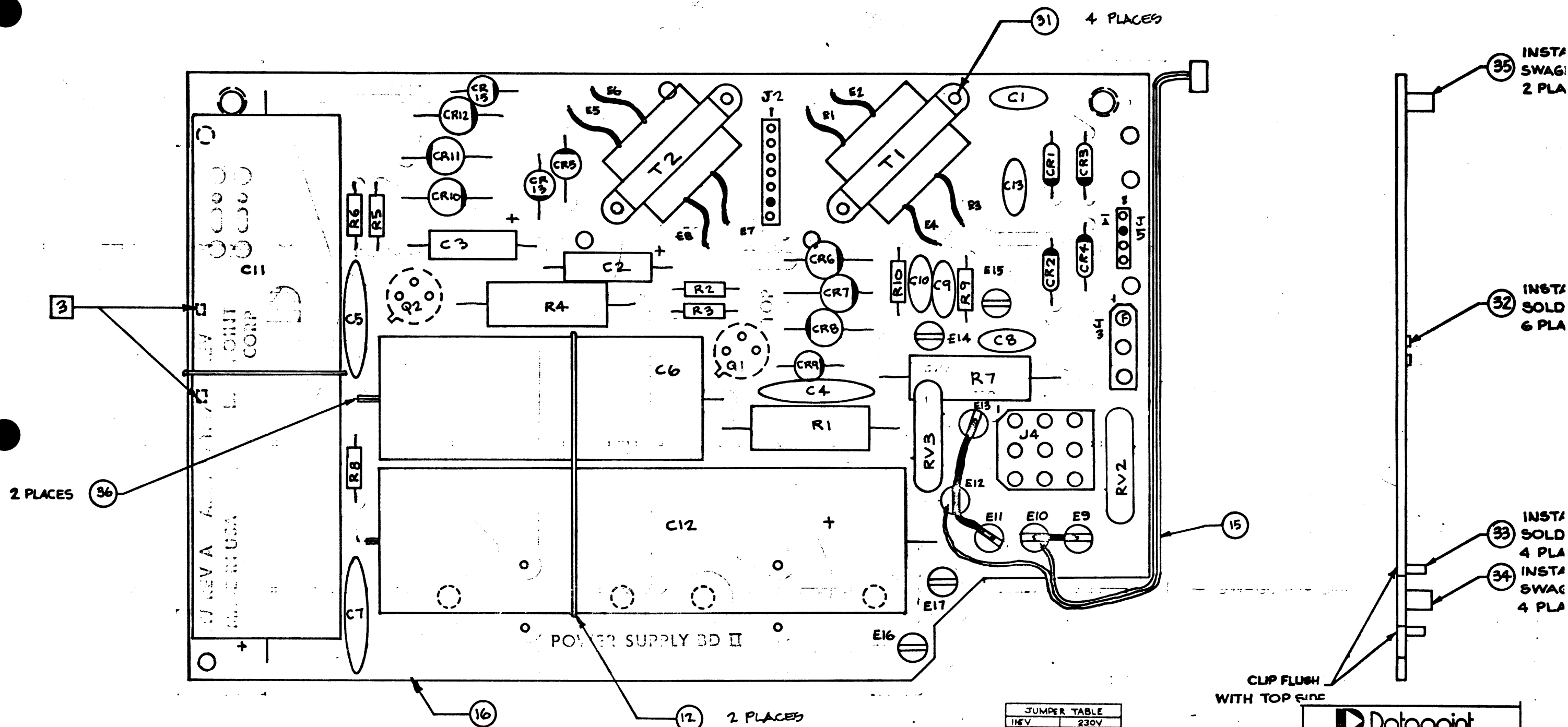


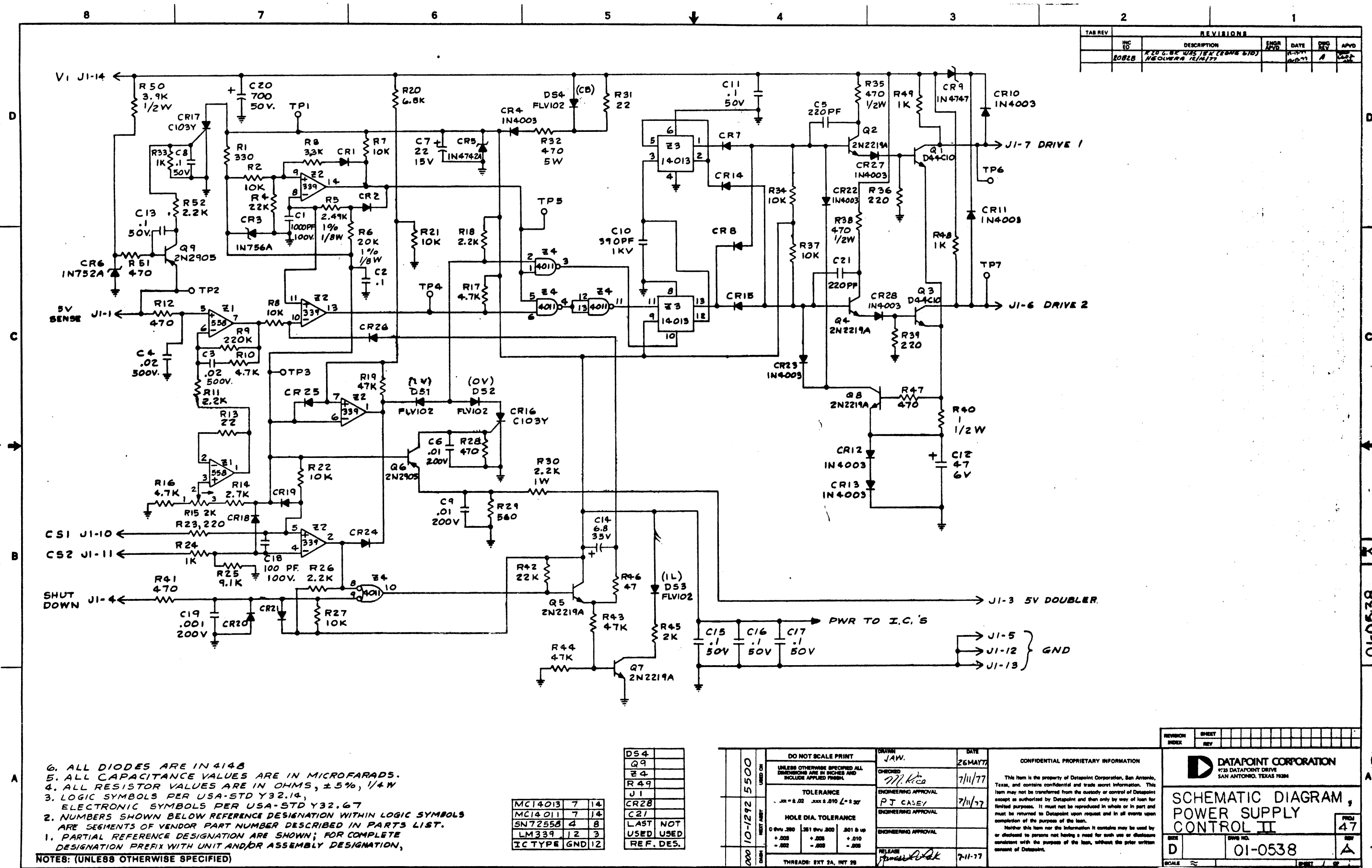
Figure 8-27.



-001 (SHOWN) 115V

Datapoint 9725 Dickinson Dr. San Antonio, Texas 78204			
PRINTED WIRING ASSEMBLY, POWER SUPPLY BOARD II			A8 65
SIZE D	DWG NO. 10-1167	REV -	PROJ 65
SCALE 2:1		SHEET 1 OF 1	

Figure 8-27A.



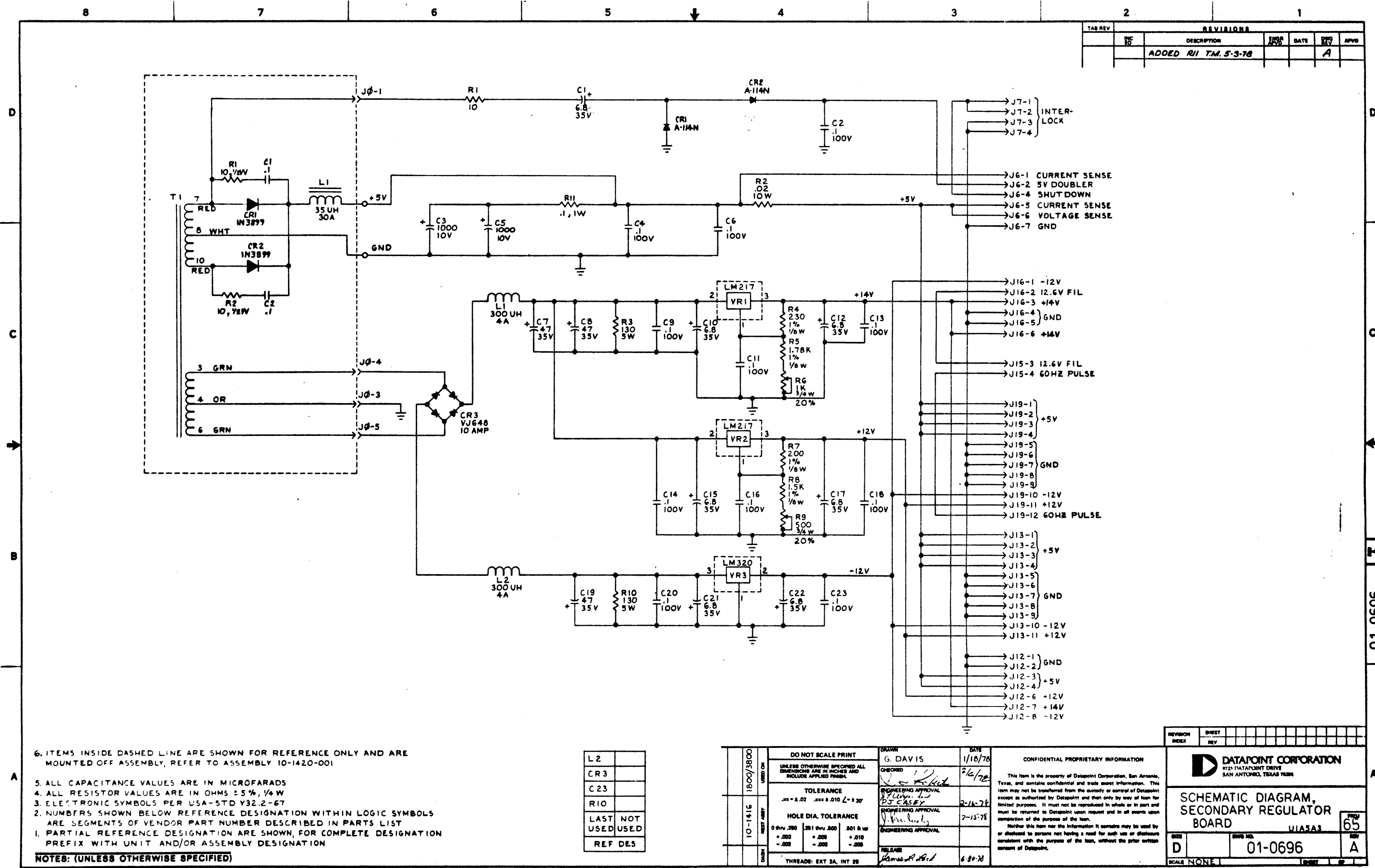
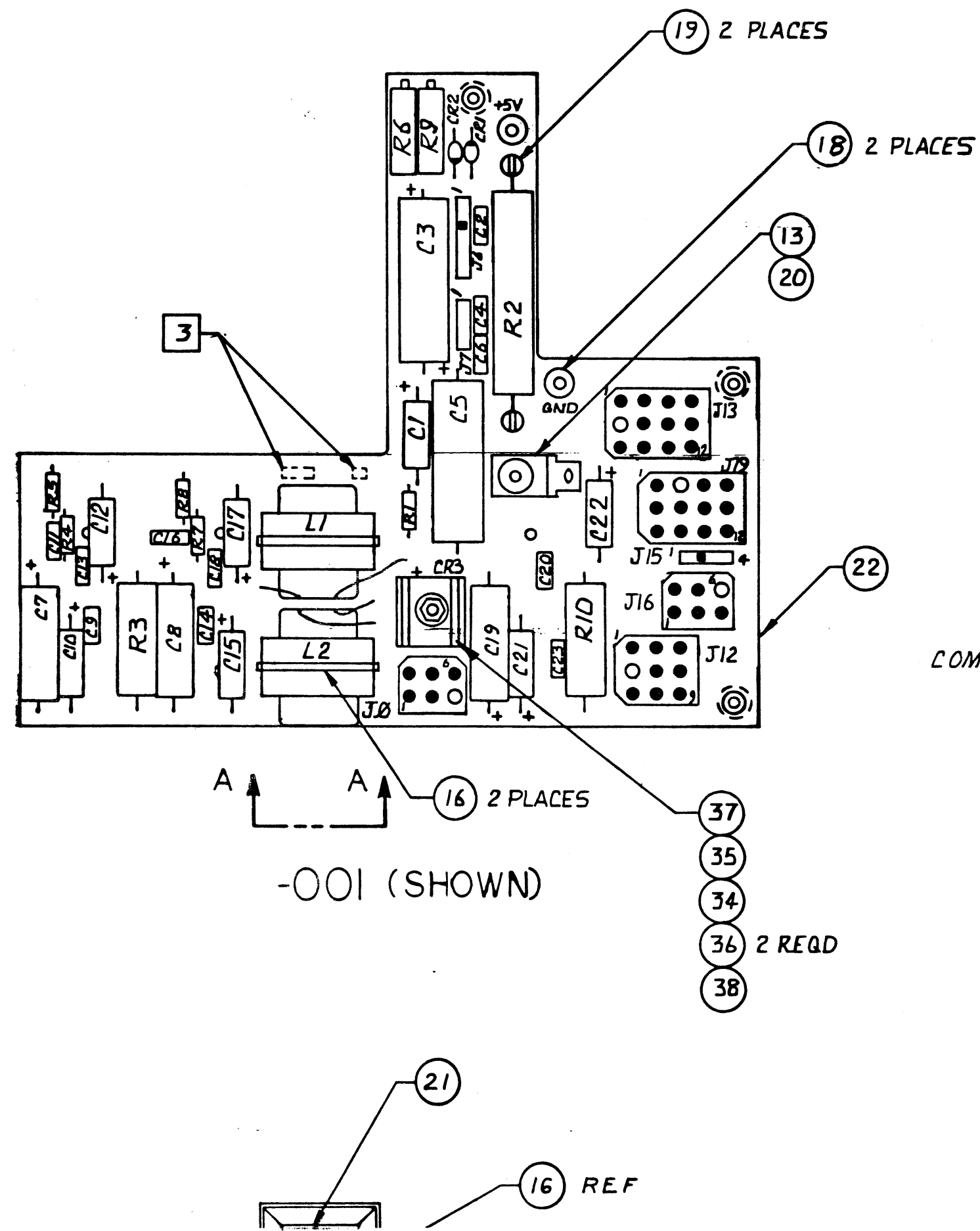
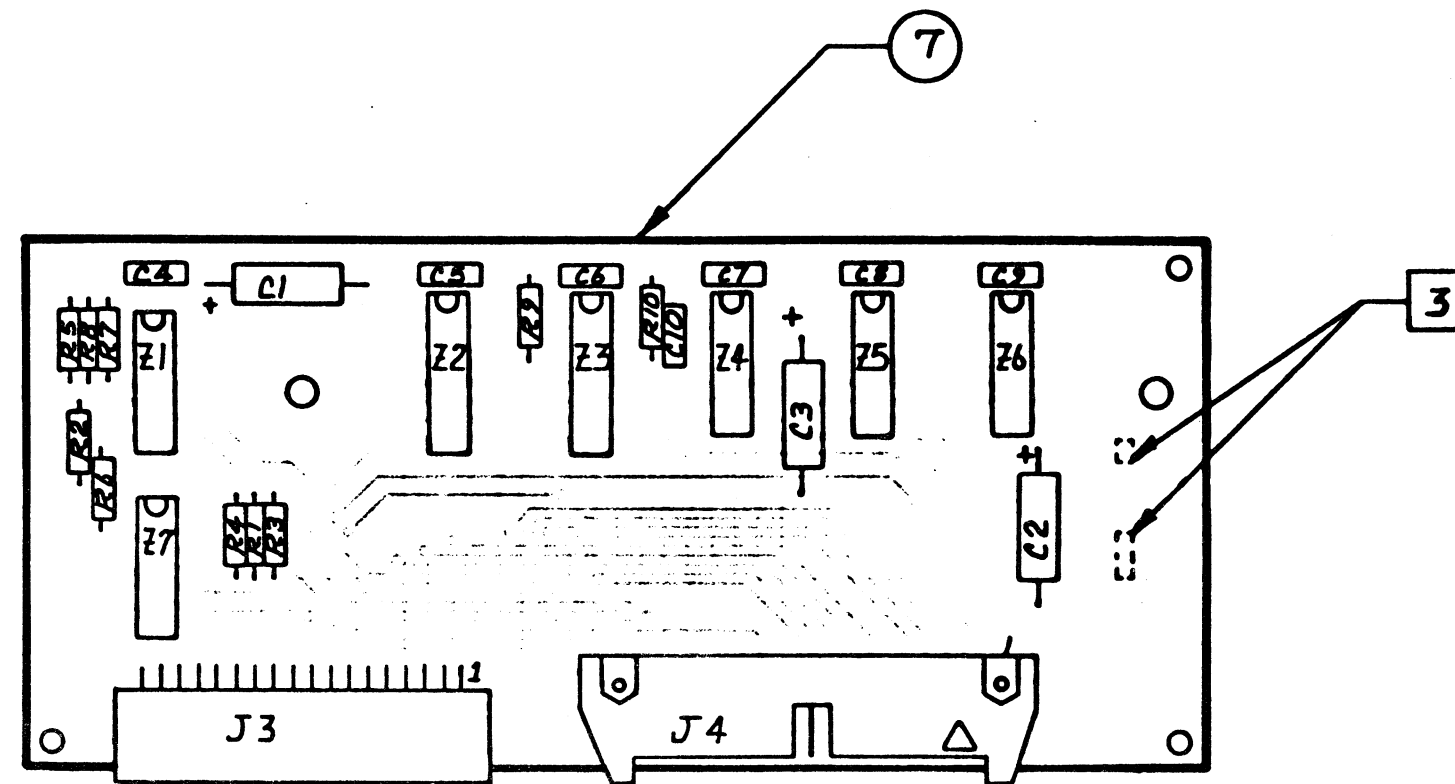


Figure 8-29.



DATAPOINT CORPORATION 2215 EASTERN DRIVE SAN ANTONIO, TEXAS 78204			
PRINTED WIRING ASSEMBLY, SECONDARY REGULATOR BOARD			
SIZE	DATE	REV	PROJ
D	10-1416	A	65
SCALE	1/1	1/1	1/1

Figure 8-29A.



-001 SHOWN

 DATAPoint CORPORATION 2510 EAST 10TH STREET SAN ANTONIO, TEXAS 78204			
PRINTED WIRING ASSEMBLY, DIRECT BUFFER			
BOARD # 2			79
REV D	DATE 10-1392	REV A	SCALE 1/1

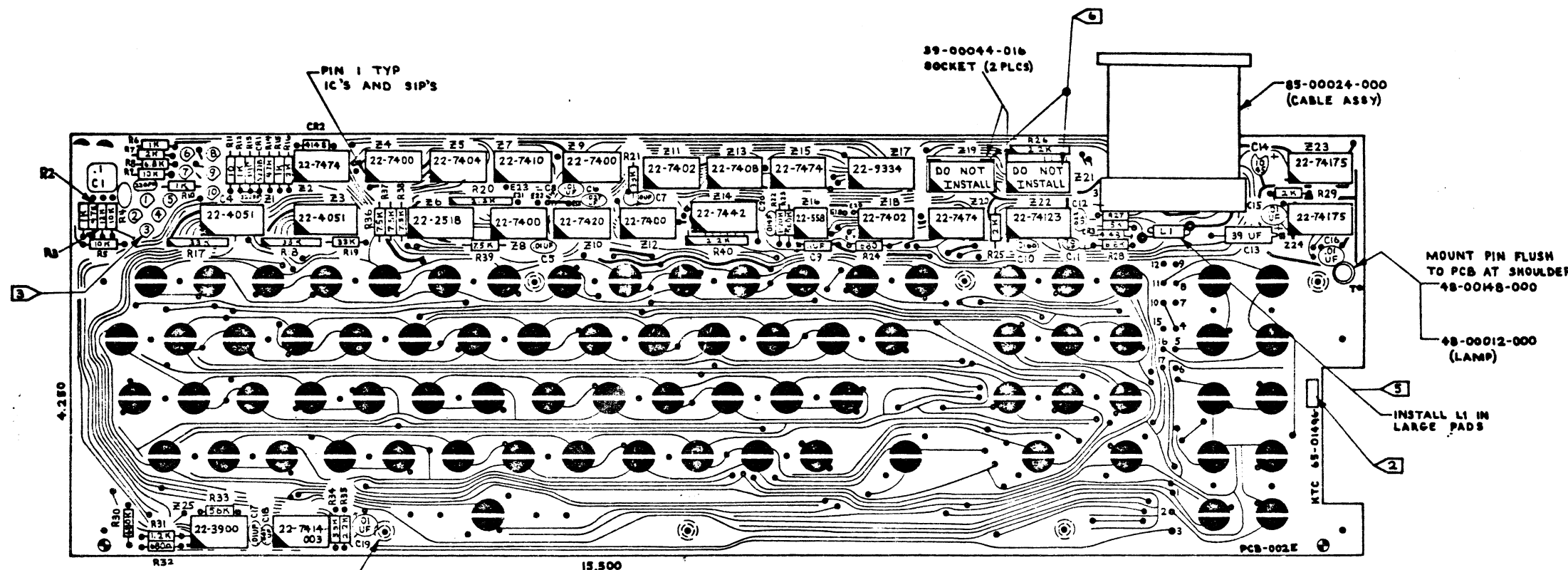
Figure 8-30A.

Figure 8-31.

4 INSTALL JUMPERS AS LISTED

E2 TO E3, E5 TO E6, E8 TO E9, E11 TO E12, E13 TO E14, E16 TO E17, E18 TO E19 ON -001, -007, -008, -011, -013 ASSYS
 E1 TO E2, E10 TO E11, E13 TO E14, E18 TO E19 ON -003, -004, -005, -010, -012 ASSYS
 E1 TO E2, E10 TO E11, E18 TO E19, E21 TO E22 ON -006 ASSY
 E2 TO E3, E5 TO E6, E8 TO E9, E11 TO E12, E16 TO E17, E18 TO E19, E21 TO E22 ON -009 ASSY

EFF.	REV.	REC.	ECO.	BY	DESCRIPTION	APP.
					REVISED	
5-15-6	A	1245	1337	WES	REVISED PCB 1979	
5-20-6	B	1256	1405	WES	REVISED PCB 1979	
5-16-6	C	1257	1405	WES	REVISED PCB 1979	
7-10-6	D	1257	1405	WES	REVISED PCB 1979	
7-26-6	E	1257	1405	WES	REVISED PCB 1979	
8-1-6	F	1257	1405	WES	REVISED PCB 1979	
8-1-6	G	1257	1405	WES	REVISED PCB 1979	
8-1-6	H	1257	1405	WES	REVISED PCB 1979	



-001, -003 THRU -013 ASSYS

PARTIAL: SEE SH 3 FOR MECH ASSY
 SEE SH 4 FOR -001 KEYTOPS
 SEE SH 5 FOR -003 KEYTOPS
 SEE SH 6 FOR -004 KEYTOPS
 SEE SH 7 FOR -005 KEYTOPS
 SEE SH 8 FOR -006 KEYTOPS
 SEE SH 9 FOR -007 KEYTOPS
 SEE SH 10 FOR -008 KEYTOPS
 SEE SH 11 FOR -009 KEYTOPS
 SEE SH 12 FOR -010 KEYTOPS
 SEE SH 13 FOR -011 KEYTOPS
 SEE SH 14 FOR -012 KEYTOPS
 SEE SH 15 FOR -013 KEYTOPS

- SEE FROM LIST 65-1496 SHEET 16 (DO NOT INSTALL-FOR TESTING ONLY)
 - LI PN 48-00038-000
 - INSTALL JUMPERS AS LISTED (48-00110-125)
 - (Q3, Q5, Q7, Q9 ARE 23-04274-001)(Q1, 2, 4, 6, 8, 10 ARE 23-03640-000)
 - RUBBER STAMP APPROPRIATE DASH NO. AFTER KTC PART NUMBER (BLACK)
 1. APPLY DATE-SERIAL NO. PRESSURE ADHESIVE TAG, TO COMPONENT SIDE OF PCB.
- NOTES:

MANUFACTURE PARTS AND OR ASSY PER KTC DOCUMENT	UNLESS OTHERWISE NOTED ALL DIMENSIONS ARE IN INCHES	TOL EXCEPT AS NOTED	ITEM	PART NO	DESCRIPTION	QTY
MO06 MO07	XX3 DIMENSION NOT TO SCALE	HOLE DIA FRACT 11-64 XX 1 01 XXX 1 05 ANG 2 11	SCALE	KEYBOARD ASSY (ELECT. ASSY.)		
USED ON DATA POINT MODEL 3600	RELEASED			key tronic corporation	65-1496	
					SHEET 1 OF 1	C

Figure 8-31A.