NCR ARCNET® Controller/Transceiver

With PC XT Bus Interface

FEATURES

- Only five support chips needed to implement an ARCNET node on a PC XT bus
- Includes IBM PC XT interface
- No additional wait states with 10 MHz bus clock
- Supports three reset options
  - Power-On-Reset
  - External Reset
  - Software Generated Reset
- 20 MHz on-chip oscillator
- Includes RAM, ROM and I/O decoding
- Software compatible with the NCR90C26 and the NCR90C98
- Diagnostic routine for duplicate ID detection
- Token Received status bit
- I/O and memory mapped registers
- Fully controls 8K of external SRAM
- Supports buffer chaining in external RAM
- Two modes
  - Mode 0: Encoded I/O & Memory space selections, direct connections of switches
  - Mode 1: Continuous I/O & Memory space selections, supports dual port memory
- 68-pin PLCC package

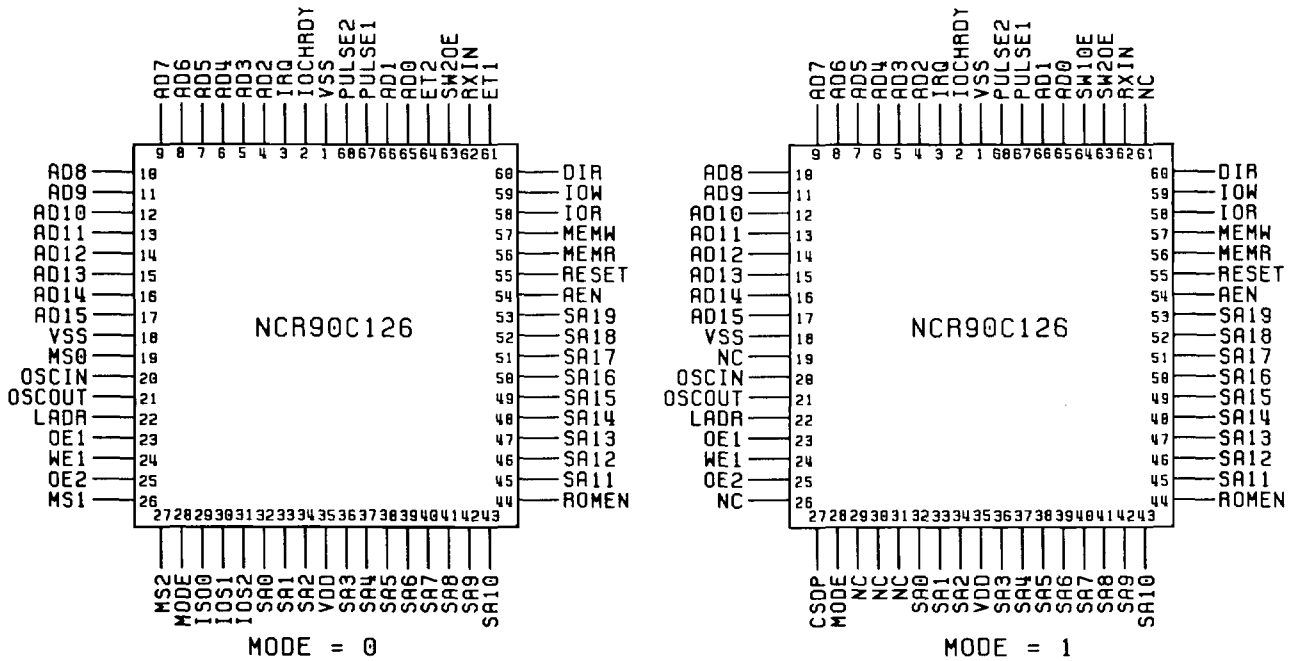


Figure 1 Pinout Diagrams

PINOUT SUMMARY

Signal Name (Mode 0)	Signal Name (Mode 1)	Type	Pin No.	Pin Description (Mode 0)	Pin Description (Mode 1)
VSS	VSS	Ground	1	Ground	Ground
IOCHRDY	IOCHRDY	Output	2	I/O Channel Ready	I/O Channel Ready
IRQ	IRQ	Output	3	Interrupt Request	Interrupt Request
AD2	AD2	In/Out	4	Address/Data bus	Address/Data bus
AD3	AD3	In/Out	5	Address/Data bus	Address/Data bus
AD4	AD4	In/Out	6	Address/Data bus	Address/Data bus
AD5	AD5	In/Out	7	Address/Data bus	Address/Data bus
AD6	AD6	In/Out	8	Address/Data bus	Address/Data bus
AD7	AD7	In/Out	9	Address/Data bus	Address/Data bus
AD8	AD8	In/Out	10	Address/Data bus	Address/Data bus
AD9	AD9	In/Out	11	Address/Data bus	Address/Data bus
AD10	AD10	In/Out	12	Address/Data bus	Address/Data bus
AD11	AD11	In/Out	13	Address/Data bus	Address/Data bus
AD12	AD12	In/Out	14	Address/Data bus	Address/Data bus
AD13	AD13	In/Out	15	Address/Data bus	Address/Data bus
AD14	AD14	In/Out	16	Address/Data bus	Address/Data bus
AD15	AD15	In/Out	17	Address/Data bus	Address/Data bus
VSS	VSS	Ground	18	Ground	Ground
MS0	NC	Input	19	Memory Select	No Connect
OSCIN	OSCIN	Input	20	Oscillator & clock input	Oscillator & clock input
OSCOUT	OSCOUT	Output	21	Oscillator Output	Oscillator Output
LADR	LADR	Output	22	Latch Address	Latch Address
OE1	OE1	Output	23	Memory Output Enable	Memory Output Enable
WE1	WE1	Output	24	Write Enable	Write Enable
OE2	OE2	Output	25	Output Enable 2	Output Enable 2
MS1	NC	Input	26	Memory Select	No Connect
MS2	CSDP	In/Out*	27	Memory Select	Chip Select Dual Port Memory
MODE	MODE	Input	28	Mode select	Mode select
IOS0	NC	Input	29	I/O Select	No Connect
IOS1	NC	Input	30	I/O Select	No Connect
IOS2	NC	Input	31	I/O Select	No Connect
SA0	SA0	Input	32	System Address bus	System Address bus
SA1	SA1	Input	33	System Address bus	System Address bus
SA2	SA2	Input	34	System Address bus	System Address bus
VDD	VDD	Power	35	+5 volt supply	+5 volt supply
SA3	SA3	Input	36	System Address bus	System Address bus
SA4	SA4	Input	37	System Address bus	System Address bus
SA5	SA5	Input	38	System Address bus	System Address bus
SA6	SA6	Input	39	System Address bus	System Address bus
SA7	SA7	Input	40	System Address bus	System Address bus
SA8	SA8	Input	41	System Address bus	System Address bus
SA9	SA9	Input	42	System Address bus	System Address bus
SA10	SA10	Input	43	System Address bus	System Address bus
ROMEN	ROMEN	Output	44	ROM enable	ROM enable

PINOUT SUMMARY [continued]

Signal Name (Mode 0)	Signal Name (Mode 1)	Type	Pin No.	Pin Description (Mode 0)	Pin Description (Mode 1)
SA11	SA11	Input	45	System Address bus	System Address bus
SA12	SA12	Input	46	System Address bus	System Address bus
SA13	SA13	Input	47	System Address bus	System Address bus
SA14	SA14	Input	48	System Address bus	System Address bus
SA15	SA15	Input	49	System Address bus	System Address bus
SA16	SA16	Input	50	System Address bus	System Address bus
SA17	SA17	Input	51	System Address bus	System Address bus
SA18	SA18	Input	52	System Address bus	System Address bus
SA19	SA19	Input	53	System Address bus	System Address bus
AEN	AEN	Input	54	Address Enable	Address Enable
RESET	RESET	Input	55	Reset	Reset
MEMR	MEMR	Input	56	Memory Read command	Memory Read command
MEMW	MEMW	Input	57	Memory Write command	Memory Write command
IOR	IOR	Input	58	I/O Read command	I/O Read command
IOW	IOW	Input	59	I/O Write command	I/O Write command
DIR	DIR	Output	60	Buffer Direction control	Buffer Direction control
ET1	NC	Input	61	Extended Timeout functions	No Connect
RXIN	RXIN	Input	62	Receive Data In	Receive Data In
SW2OE	SW2OE	Output	63	Switch 2 Output Enable	Switch 2 Output Enable
ET2	SW1OE	In/Out*	64	Extended Timeout functions	Switch 1 Output Enable
AD0	AD0	In/Out	65	Address/Data bus	Address/Data bus
AD1	AD1	In/Out	66	Address/Data bus	Address/Data bus
PULS1	PULS1	Output	67	Pulse 1 (transmitter out)	Pulse 1 (transmitter out)
PULS2	PULS2	Output	68	Pulse 2 (transmitter out)	Pulse 2 (transmitter out)

*Input mode 0, output mode 1.

GENERAL DESCRIPTION

The NCR90C126 Controller/Transceiver includes all logical functions of an ARCNET RIM (Resource Interface Module) plus an economical PC XT interface. The 1.5-micron, CMOS technology increases the level of integration, improves the performance and lowers the power consumption of the NCR90C126. ARCNET is a popular token-passing Local Area Network (LAN) developed by Datapoint Corporation. The NCR90C126 handles all tasks for transferring data between the node and the LAN. It reads from and writes to message buffers in an external RAM, it initiates and responds to valid ARCNET transmissions, and it passes control between itself and the other RIMs on the network. The NCR90C126 also contains the interface to the cable-driving circuitry that connects to the physical LAN media.

The NCR90C126 consists of an ARCNET controller, ARCNET transceiver, on-chip oscillator, and an IBM PC XT interface as shown in Figure 3. Only five support chips are required to use an ARCNET node on a PC XT compatible bus with the NCR90C126. See Figure 2.

The NCR90C126-based ARCNET LAN typically requires no additional wait states: a maximum of one with PC XT buses up to 10 MHz. Products other than the NCR90C126 require 4 to 15 additional wait states from the PC XT bus to transfer the same data.

Two modes provide flexibility for decoding I/O and Memory address space. Both dual port and standard memory are supported with the NCR90C126. This chip controls up to 8K bytes of external buffer RAM.

The Token Received status bit enables the node to confirm its connection to the network. This bit allows the upper OSI layers to confirm that the token has been received and the node is connected to the network.

The NCR90C126 has a unique diagnostic routine to identify duplicate node IDs on an ARCNET LAN. If there is already a node on the network with that ID, the duplicate ID status bit is set. Without this diagnostic routine, the network would be in a constant state of reconfiguration when duplicate node IDs exist.

Buffer chaining improves the network performance especially in file server applications. When buffer chaining is enabled, the automatic receive function allows the receive buffer to accept multiple packets of data without interrupting the host between each reception. When transmitting, buffer chaining allows one command to enable the transmission of multiple packets without host intervention. Buffer chaining reduces overhead, and has improved system throughput by 20 to 80 percent depending on the specific hardware and software.

The NCR90C126 provides the ability to upgrade performance as needed. It is backward software compatible with the NCR90C26 and defaults to this mode of operation. Changing to the NCR90C98 mode after initialization allows the node to support buffer chaining.

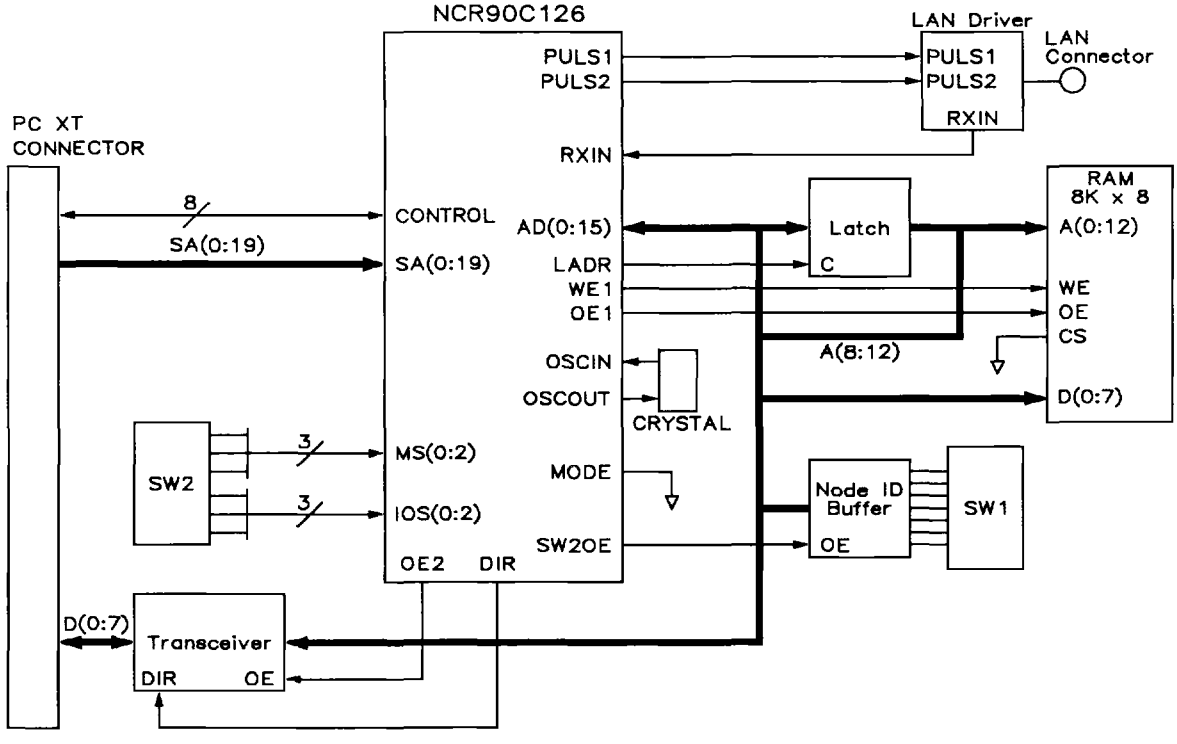


Figure 2 Minimum System Configuration Block Diagram

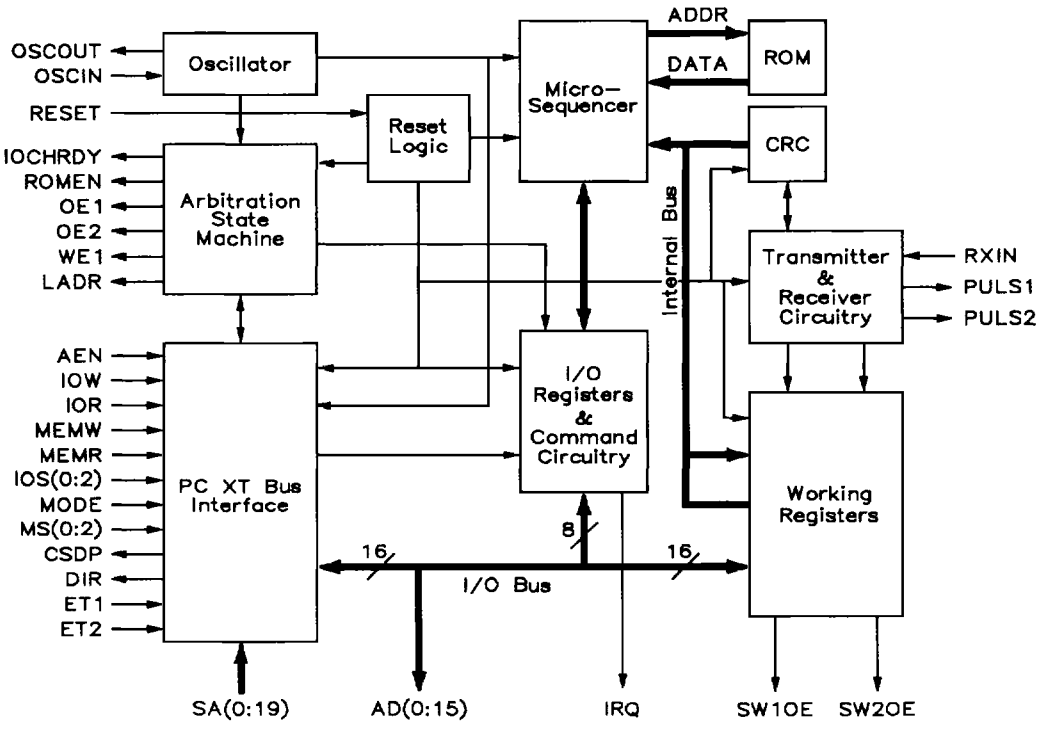


Figure 3 Chip Block Diagram

ARCNET OVERVIEW

LINE PROTOCOL

The NCR90C126 implements an asynchronous line protocol, with each Information Symbol Unit (ISU) consisting of the following:

- Two clock units of mark (logic 1)
- One clock unit of space (logic 0)
- Eight clock units of data

A single clock unit is 400ns in duration. A byte of data is transmitted every 4.4μs (400ns x 11 clock units) so the time to transmit any message can be determined exactly. Transmissions start with an Alert Burst, which is six clock units of mark. The line idles in spacing condition. The five types of ARCNET transmissions are:

Invitations To Transmit

An Alert Burst followed by three ISUs: one EOT (End of Transmission) and two repeated DID (Destination IDentification) ISUs. This message passes control (the "token") from one node to another.

Free Buffer Enquiries

An Alert Burst followed by three ISUs: one ENQ (ENQuiry) and two repeated DID ISUs. This message asks another node if it is able to accept a message packet.

Packets

An Alert Burst followed by 8 to 516 ISUs:

- one SOH (Start of Header) ISU
- one SID (Source IDentification) ISU
- two repeated DID ISUs
- an inverse COUNT ISU = 256−N, for N data ISUs to be sent
- one system code ISU
- from 0 to 507 data ISUs
- two CRC (Cyclic Redundancy Check) ISUs

Acknowledgments

An Alert Burst followed by a single ACK (ACKnowledgment) ISU. This message is used as a positive response to Free Buffer Enquiries, and to acknowledge the valid reception of a packet.

Negative Acknowledgments

An Alert Burst followed by a single NAK (Negative ACKnowledgment) ISU. This message gives a negative response to Free Buffer Enquiries.

Line Protocol Notes

The codes (all in HEX) for the special ISUs mentioned above are

- EOT - 04
- ENQ - 85
- SOH - 01
- ACK - 86
- NAK - 15

The COUNT ISU for packets may be equal to (512 - N) if a "long packet" is being sent. The CRC polynomial used for data packets is: $X^{16} + X^{15} + X^2 + 1$.

As a receiving node, the NCR90C126 will verify incoming transmissions by checking for:

- At least one mark and exactly one space preceding each byte.
- A valid EOT, ENQ, SOH, ACK, or NAK following the Alert Burst.
- Proper CRC for data packets.
- Correct number of bytes, depending on the transmission

NETWORK CONTROL

All nodes in an ARCNET system are distinguished by a unique 8-bit ID (IDentification) value. This value is configurable with DIP switches associated with each NCR90C126 chip. An ID of 0 may not be assigned to any node, since that ID indicates a Broadcast to all nodes. Control of the Local Area Network (LAN) is based on token passing. To send a message, a node must first receive the token. The token is received in an Invitation to Transmit message containing its own ID. To send a message, the host processor loads the message data and the destination ID into the NCR90C126's buffer RAM, then the host writes an "Enable Transmit" command to the NCR90C126. The NCR90C126 will know it has a message to send if the TA (Transmitter Available) bit in its Status Register is low. When the NCR90C126 has the token, it transmits a Free Buffer Enquiry to the destination ID to see if it is able to receive the message. If the destination is not able to receive (RI=1), it transmits an NAK back to the controlling node which passes the token. If the destination is able to receive, it transmits an ACK back to the controlling node. The controlling node then transmits the packet, complete with a 16-bit CRC. After it sends a packet, the NCR90C126 waits a specified response time. If it receives an ACK within that time, it sets both the TMA (Transmit Message Acknowledged) and the TA Status bits and passes the token. If it does not receive an ACK in time, it only sets TA and then passes the token. If there is no activity on the line within 75.6μs of transmitting a Free Buffer Enquiry, TA is set and the token passed. When the NCR90C126 receives the token, but its TA bit is high (it has no message to send), it sends an Invitation to Transmit to pass the token.

Any node recognizes a packet when it sees the Start of Header ISU, and will write the Source ID to its receive buffer. If the NCR90C126 sees the first DID (Destination ID) as its own, or if the packet is a Broadcast message (see the *RECONFIGURATION AND BROADCAST* section on page 7), the chip will write the second DID and the rest of the message to its receive buffer. Otherwise, the NCR90C126 will ignore the rest of the packet. After the packet has been fully received, it must pass three conditions to be considered a valid message:

1. the CRC comparison
2. correct length of ISUs
3. valid DID in byte 0 of the receive buffer

Valid DIDs equal zero (indicating Broadcast), or the NCR90C126's own ID. An ACK is sent if a message is valid by these conditions and addressed to the NCR90C126's ID. If the message is a broadcast message, no ACK will be sent. The NCR90C126 sets its RI status bit after receiving a valid message if no more receive buffers are available. In the buffer chaining mode, the Received Packet (RP) status bit is set when a valid message is received addressed to the NCR90C126's own ID. If any of the conditions fail, the NCR90C126 ignores the message and writes over it with future packets.

RECONFIGURATION AND BROADCAST

Two activities involve all nodes on the ARCNET system: Reconfiguration of the system and Broadcasts to the system.

Reconfiguration

Reconfiguration of the network is performed any time a node is removed from or added to the system. The NCR90C126 will instigate a Reconfiguration when it is first powered on or when it has not received an Invitation to Transmit within 840ms. It does this by transmitting a Reconfiguration Burst: 8 marks and 1 space repeated 765 times. This burst terminates all activity on the network. This burst is longer than all the other transmissions so it interferes with the next Invitation to Transmit, destroys the token, and no other node can take control of the line. The Reconfiguration Burst also provides enough line activity so the NCR90C126 that just sent the token will also release control of the network.

When any NCR90C126 sees the line idle for 82.4µs, it begins a network reconfiguration cycle. It sets the internal NID (Next ID) register to its own ID. Besides resetting the NID, the NCR90C126 also starts a time-out of 146µs times the quantity 255 minus its own ID [146µs x (255-ID #)]. If this time-out expires with no other line activity, the NCR90C126 will start transmitting Invitation to Transmit with the DID pointing to itself. Only the NCR90C126 with the largest ID value will actually time-out.

After sending an Invitation to Transmit, the NCR90C126 will look for any line activity, indicating that the DID is a valid node. If the sending NCR90C126 detects no activity after 75.6µs, it increments its NID and sends another invitation. Eventually, the NCR90C126 with the ID that is next will see its ID in the invitation and take control of the line. The previous NCR90C126 will then have its NID set correctly. The process repeats with the end result showing each NCR90C126 with a NID stored representing an active node to pass the token. The token is not sent to nonexistent nodes. If a node is removed from an active network, then the previous node will time out when passing the token. The previous NCR90C126 goes through a cycle of incrementing its NID and transmitting an invitation until it finds the next valid node. The total time to perform a Reconfiguration will vary depending on the system configuration, but is typically between 24 and 61ms.

Broadcasts

A packet is considered to be a Broadcast Packet if the DID (Destination ID) equals 0. No regular node may be assigned the Broadcast ID. Nodes are set to receive Broadcasts by issuing a "Write Configuration" command with the most significant bit of the command set to one. All NCR90C126 commands are described in the *COMMAND REGISTERS* section starting on page 12.

TIMECHECK FUNCTIONS

A standard baseband system using RG-62 coaxial cable (the ARCNET standard) can take up to 31µs for one-way propagation. This corresponds to a distance of about 4 miles. The maximum turn-around time that any NCR90C126 takes to respond to an incoming message is 13.3µs. A maximum response time for any transmission is 31 + 31 + 13.3 = 75.3µs. To allow a margin, the NCR90C126 uses 75.6µs as its basic response time-out. This is the interval a controlling node expects to see line activity after a transmission.

An idle time-out interval transpires at the onset of a Reconfiguration. After the Reconfiguration Burst, all nodes commence the Reconfiguration process when they detect no line activity for the idle time-out. In a standard network, the idle time-out is 82.4µs. The transfer time-out is the ID-dependent interval associated with Reconfiguration. This time-out is given by 146µs x (255-ID). It transpires only for the node with the highest ID on the network which will start to pass the token. In a standard network, if any node has not received an Invitation to Transmit within a Reconfiguration time-out of 840ms, it issues a Reconfiguration Burst and starts a network reconfiguration.

ET2	ET1	Response Timeout	Reconfiguration Timeout
1	1	75.6µs	0.84 seconds
1	0	302.4µs	1.68 seconds
0	1	604.8µs	1.68 seconds
0	0	1209.6µs	1.68 seconds

TABLE 1 Response and Reconfiguration Settings

The time-out values in Table 1 apply to a basic network with no two nodes farther apart than four miles. The network may operate over longer distances by appropriate setting of the ET1 and ET2 inputs. Table 1 shows the effect of ET1 and ET2 on two of the more pertinent timeouts. It is important that ET1 and ET2 be set to the same value for all nodes on the network.

HOST INTERFACE OVERVIEW

The NCR90C126 contains a full-featured PC XT bus interface. In a minimal configuration, only five integrated circuits are required to build a fully functional board (see Figure 2). Additions to the minimal system supported by the NCR90C126 are on-board ROM, more switches for increased flexibility in locating the buffer RAM and I/O registers in the memory and I/O maps, and hardware for dual port RAM and LAN Driver disable. Two hardware operating modes (0 & 1) reconfigure the pinout to accommodate these options. More information is in the *DETAILED HOST INTERFACE DESCRIPTION* on page 18.

PC XT INTERFACE

All transactions on the NCR90C126 board are controlled by the NCR90C126. Accesses to the NCR90C126 internal registers can be accomplished by I/O commands or memory commands. Access to the RAM buffer memory and/or the on-board ROM goes through the NCR90C126 and the multiplexed address/data bus. The NCR90C126 also uses the multiplexed address/data bus to store and retrieve data that is received and transmitted over the LAN.

I/O AND MEMORY ACCESSES

The host has the option of accessing the registers within the NCR90C126 with an I/O command or with a memory command. With I/O commands, the registers are mapped into a 16-address space in the I/O map. When accessing the registers with a memory command, the registers appear in the 16 highest addresses in the ROM memory map. When SA13 is high, the ROM memory map is accessed. When SA13 is low, the RAM memory map is accessed. See Figure 4.

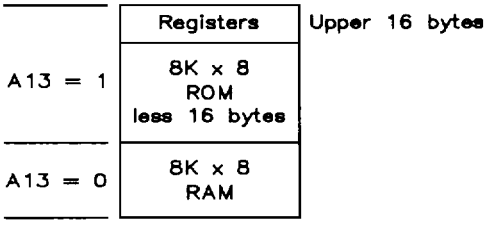


Figure 4 Memory Map

HARDWARE OPERATING MODES (MODE 0 and MODE 1)

Mode 0 and 1 allow the designer to optimize the system for cost or for additional features by changing the pinout. Mode 0 is used to optimize the design for cost. Using this mode, only five chips are required to implement a system. Mode 1 is used to gain more flexibility where the I/O and memory maps are located. More memory address space is available to the system by disabling the ROM. The use of Dual Port RAM is also supported in this mode.

LAN DRIVER CONTROL

The NCR90C126 supports the enabling and disabling of the LAN driver by issuing a command to the NCR90C126.

DUAL PORT MEMORY

Dual port memory is supported in mode 1 to offer faster system speed. When the dual port memory is enabled, no arbitration takes place on the multiplexed address/data bus.

FUNCTIONAL DESCRIPTION

SOFTWARE OPERATING MODES (NCR90C26 and NCR90C98)

The NCR90C126 supports two software operating modes: The NCR90C26 and the NCR90C98. In the NCR90C26 mode, the chip is programmed the same as the NCR90C26.

The NCR90C126 starts in the NCR90C26 mode. The power-on routine within the NCR90C126 writes the NCR90C26 hex signature D1 to address 0 in the buffer memory. When the host CPU writes to Command Register 2, the NCR90C126 switches to the NCR90C98 mode. All bits in Command Register 1 take on the new functions of the NCR90C98 mode. The chip must be reset (Power-on, Reset signal or Reset command) to switch back to the NCR90C26 mode.

BUFFER CHAINING

This feature relieves the host from the task of enabling a new receive buffer for each packet received. It also lets the host transmit multiple packets per transmit command.

Packet Reception

In the receive buffer chaining mode, the NCR90C126 automatically fills all the pages that are assigned to the receive buffer. If the circular mode is enabled, the NCR90C126 automatically restarts at the beginning of the receive buffer after reaching the end. The NCR90C126 keeps track of available buffers and stops receiving when there are no more buffers available. The host must update the pointer that keeps track of the packets that have been read.

The pointers associated with the receive buffer are the Next Page to Receive (NPRX), Next Page to Read (NPRD) and Start of RX Buffer (SRXB). When a packet has been received successfully, the NCR90C126 increments the NPRX pointer and sets the RP bit which generates an interrupt. After determining the source of the interrupt, the host reads the NPRX pointer which clears RP, reads the packet and increments the NPRD pointer.

Packet Transmission

In the transmit buffer chaining mode, the NCR90C126 transmits all the packets the host wrote into the transmit buffer. The host must update the pointer that points to the last packet to be transmitted. The NCR90C126 will keep track of which packets to send and when to stop. If the circular mode has been enabled, the NCR90C126 automatically restarts at the beginning of the transmit buffer after reaching the end.

The pointers associated with the transmit buffer are the Next Page to Write (NPWR), Next Page to Transmit (NPTX) and Start of TX Buffer (STXB). When the host transmits a packet, it must write the packet into the page pointed to by the NPWR pointer. If the host transmits multiple packets, it must write the packets into the subsequent pages, and then move the NPWR pointer to the page after the last written page. The NCR90C126 will start to transmit one packet per token when the Enable Transmit or Enable Chain Transmit commands are executed. Upon a successful transmission, the TA and TMA bit will be set.

POINTERS

There are both fixed (SRXB, STXB) and variable (NPRD, NPWR, NPTX, NPRX) pointers. The variable pointers NPRD and NPWR are managed by the host; NPTX and NPRX are managed by the controller. The pointers have a resolution of 256 bytes/page so they are incremented by 1 in the short packet mode (256 bytes/packet) and by 2 in the long packet mode (512 bytes/packet). If a short packet is being received or transmitted in the long packet mode, NPTX or NPRX is incremented by 2. Figure 5 shows the function of each pointer.

Next Page to Write (NPWR).

The NPWR pointer contains the page address (in the buffer RAM) for the host to write the next packet of data to be transmitted. NPWR is incremented by the host after a packet has been written to the buffer

Next Page to Transmit (NPTX).

The NPTX pointer contains the page address for the next packet to be transmitted. NPTX is incremented by the controller after a successful transmission.

Start TX Buffer (STXB).

The STXB pointer contains the starting page address of the transmit buffer RAM. The transmit buffer memory ranges from this address to the end of memory.

Next Page to Receive (NPRX).

The NPRX pointer contains the page address of the next packet to be received. NPRX is incremented by the controller after a packet has been received with correct CRC.

Next Page to Read (NPRD).

The NPRD pointer contains the page address in the buffer RAM of the next packet to read. NPRD is incremented by the host after a packet has been read out of the buffer.

Start RX Buffer (SRXB).

The SRXB pointer contains the starting page address of the receive buffer RAM. The receive buffer memory ranges from this address up to the STXB page address.

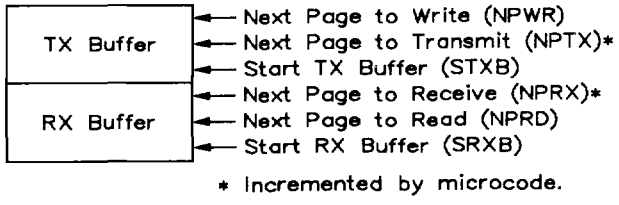


Figure 5 Buffer RAM Pointer Diagram

PIN DESCRIPTIONS

AD(0:7): Low-Order, Address/Data Bus
During host accesses to the NCR90C126, data is transferred on this bus. During host access to memory, the low address byte is output and latched by LADR during the first part of the cycle. During the second part of the cycle, these pins are in high impedance state. During the NCR90C126 accesses to memory, the low address byte is output and latched by LADR during the first part of the cycle, and data is transferred during the second part of the cycle. Data is transferred on this bus during the NCR90C126 read of configuration switches.

AD(8:15): High-Order, Address/Data Bus
These pins output the high-order address bits during controller & host accesses to memory. During NCR90C126 read of configuration switches, data is transferred on this bus. Bit AD15 is used to write a LAN driver disable bit during the first part of a NCR90C126 memory access cycle.

AEN: Address Enable
This input enables address decoding when low.

CSDP: Chip Select Dual Port Memory
This signal functions as an output in mode 1. It enables the dual port memory when low.

DIR: Buffer Direction Control
This output controls the direction of the data buffer between the PC XT bus and the multiplexed address/data bus. When high, the buffer drives the multiplexed address/data bus. When low, the buffer drives the PC XT bus.

ET1, ET2: Extended Timeout Functions
These inputs select the time-out durations of NCR90C126. They are primarily used to check responses from other nodes on the LAN. These pins should be tied high for normal operation. See Table 1 on page 7.

IOCHRDY: I/O Channel Ready
The NCR90C126 uses this output to insert wait states during host accesses. When low, this extends the access until it is released.

IOR: I/O Read
When low, this input from the PC XT bus instructs the NCR90C126 to put data on the data bus for the host to read.

IOS0-2: I/O Select
These input signals tell the NCR90C126 which I/O address to respond to as shown in Table 2. These inputs are only valid during mode 0.

IOS2	IOS1	IOS0	I/O Address Range
0	0	0	260-26F hex
0	0	1	290-29F hex
0	1	0	2E0-2EF hex
0	1	1	2B0-2BF hex
1	0	0	300-30F hex
1	0	1	350-35F hex
1	1	0	380-38F hex
1	1	1	3E0-3EF hex

TABLE 2 IOS Decode

IOW: I/O Write
When low, this input signal from the PC XT bus instructs the NCR90C126 to receive data from the data bus.

IRQ: Interrupt Request
The NCR90C126 drives this output high to signal the host that an enabled interrupt condition has occurred. IRQ returns low after clearing the interrupt status condition or the corresponding mask bit.

LADR: Latch Address
The falling edge of this output latches the lower 8 address lines when accessing the RAM buffer memory. This signal is active during NCR90C126 memory accesses and host memory accesses.

MEMR: Memory Read Command
When low, this input signal from the PC XT bus instructs the NCR90C126 and on-board memory to put data on the PC XT bus.

MEMW: Memory Write Command
When low, this input signal from the PC XT bus instructs the NCR90C126 and on-board memory to receive data from the PC XT bus.

MODE: Mode Select
This input configures the chip to mode 0 when low and to mode 1 when high. It should be hardwired to the appropriate mode.

MS0-2: Memory Select
These inputs tell the NCR90C126 which memory addresses to respond to as shown in Table 3. They are only valid in mode 0.

MS2	MS1	MS0	Memory Address Range
0	0	0	C0000-C3FFF hex
0	0	1	C4000-C7FFF hex
0	1	0	E0000-E3FFF hex

TABLE 3 MS Decode

MS2	MS1	MS0	Memory Address Range
0	1	1	CC000–CFFFF hex
1	0	0	D0000–D3FFF hex
1	0	1	D4000–D7FFF hex
1	1	0	D8000–DBFFF hex
1	1	1	DC000–DFFFF hex

TABLE 3 MS Decode [continued]

OE1: Output Enable 1
This output goes low to enable the RAM. When low, data from the RAM is expected on the multiplexed address/data bus. OE1 goes low when SA13 is low and the host performs a memory access with the NCR90C126.

OE2: Output Enable 2
This output goes low to allow the host access to the multiplexed address/data bus. It goes high to allow the NCR90C126 access to the multiplexed address/data bus.

OSCIN & OSCOUT: Oscillator Input and Output
These input and output pins connect an external 20 MHz crystal to the internal oscillator. The OSCIN pin may also be used to drive the NCR90C126 with an external clock. OSCOUT is left floating in this case.

PULS1 & PULS2: Pulse 1 & 2 (Transmitter Out)
These outputs are nonoverlapping, negative-going pulses that control the cable-driving circuitry. The output signals correspond to the data being transmitted over the LAN from this node. Pulse 1 is the first and Pulse 2 is the second pulse in this dual-pulse process.

RESET: Reset
This input resets the state of the NCR90C126 when driven high. Upon power-up, the internal power-on-reset cell resets the chip. During reset, the NCR90C126 sequence counter is set to zero and the Reset status bit is set to 1. See Table 4.

ROMEN: ROM Enable
This output goes low to enable the ROM. When low, data from the ROM is expected on the multiplexed address/data bus. This signal goes low when SA13 is high and the host is performing a memory read with the NCR90C126. The 16 highest addresses in the ROM memory map access the internal registers. ROMEN is disabled when these addresses are accessed.

RXIN: Receive Data In
This input receives serial data from the LAN cable circuitry.

SA(0:19): System Address Bus
This input bus is driven by the PC XT address lines. Addresses from this bus determine the I/O and memory addresses used when accessing this chip.

SW1OE: Switch 1 Output Enable
In mode 1, this output goes low to read the switch settings for the memory and I/O select addresses. The NCR90C126 responds to these addresses when accessed by the host.

SW2OE: Switch 2 Output Enable
This output goes low to read the switch settings for the Node ID. This value is used to uniquely identify the node on the LAN. In mode 1, three additional switches are read also. See *Mode 0 and Mode 1* on page 20.

WE1: Write Enable 1
This output goes low when a write occurs from the host or the NCR90C126 to the memory buffer RAM.

NAME	STATE
Registers and Pointers	**MSB LSB**
Command Register 1	See Note 1
Command Register 2	See Note 1
Status Register 1 (See Note 2)	1 x x 1 0 0 0 1
Status Register 2 (See Note 3)	1 1 0 x x 0 0 0
Interrupt Mask 1	0 0 0 0 0 0 0 0
Interrupt Mask 2	0 0 0 0 0 0 0 1
Next Page to Write (NPWR)	1 1 1 1 1 1 1 1
Next Page to Transmit (NPTX)	1 1 1 1 1 1 1 1
Start TX Buffer (STXB)	1 1 1 1 1 1 1 1
Next Page to Receive (NPRX)	1 1 1 0 0 0 0 0
Next Page to Read (NPRD)	1 1 1 0 0 0 0 0
Start RX Buffer (SRXB)	1 1 1 0 0 0 0 0

Output Pins	STATE
AD(0:15), CSDP	Resistive high
IRQ, IOCHRDY	High impedance
PULS1, PULS2, OE1, WE1, OE2, SW1OE, SW2OE, ROMEN	1 (high)
LADR	0 (low)

[1] See the REGISTER DESCRIPTIONS section on the following page.

[2] In Status Register 1, bits 5 & 6 reflect the state of the ET1 & ET2 pins.

[3] In Status Register 2, bits 3 & 4 reflect the state of the IL0 & IL1 pins.

TABLE 4 NCR90C126 Reset State

REGISTER DESCRIPTIONS

The registers of the NCR90C126 occupy seven addresses in a memory or I/O map. The host system has access to ten registers which are:

- Command Registers 1, 2 & 3
- Interrupt Mask Registers 1 & 2
- Status Registers 1 & 2
- NPRX Pointer Register
- NPTX Pointer Register
- RESET Command Register

SA 3 2 1 0	WRITE	READ
0 0 0 0	Interrupt Mask 1	Status Register 1
0 0 0 1	Command Reg. 1	Reserved
0 0 1 0	Command Reg. 2	NPRX Pointer
0 0 1 1	Reserved	NPTX Pointer
0 1 0 0	Interrupt Mask 2	Status Register 2
0 1 0 1	Command Reg. 3	Reserved
1 0 0 0	Reset Chip	Reset Chip

COMMAND REGISTERS

NCR90C26 Mode

In the NCR90C26 mode, only Command Register 1 is valid. Command Register 1 is a write-only register accessed by writing to address 1. The commands recognized by Command Register 1 are described below.

Command Register 1

Data MSB LSB	Function
0 0 0 0 0 0 0 1	Disable Transmitter: This causes the NCR90C126 to cancel any pending transmit command. This command will cause the TA bit to set the next time the NCR90C126 receives the token.
0 0 0 0 0 0 1 0	Disable Receiver: This causes a pending receive command to be canceled and the RI bit to set the next time the NCR90C126 receives the token. If a packet has already started arriving, this command has no effect.

Command Register 1

0 0 0 n n 0 1 1	Enable Transmit from Page nn: This tells the NCR90C126 to prepare for a transmit operation out of RAM buffer page nn when it next receives the token. The TA and TMA bits are reset when the NCR90C126 receives this command. The TA bit equals 1 at completion of the transmission. The TMA bit will be set when the destination node has sent back an acknowledgment. If TA=0, this command should not be issued. During reset, nn=11.
b 0 0 n n 1 0 0	Enable Receive to Page nn: This allows the NCR90C126 to receive messages in RAM buffer page nn. The RI bit is set to zero by this command. If b=0, only messages addressed to the NCR90C126's ID are received. If b=1, broadcast messages are accepted, also. RI is set by a successful message reception. During reset, nn=00 and b=0.
0 0 0 0 s 1 0 1	Buffer size: This tells the NCR90C126 the size of its RAM buffer. If s=0, the buffer is 1K bytes and only short packets are sent and received. If s=1, the buffer is 2K bytes and both short and long packets are used. During reset, s=0.
0 0 0 r p 1 1 0	Clear Flags: This resets the POR and/or the RECON status bits depending on the variable bits. If r=1, the RECON flag is cleared. If p=1, POR is cleared. During reset, r=0 and p=0.
0 0 0 0 t 1 1 1	Enable Duplicate ID routine: When t=0, the Duplicate ID (DPID) routine is disabled. When t=1, the DPID routine is enabled. During reset, t=0.

NCR90C98 Mode

Command Registers 1, 2 & 3 are write-only registers accessed by writing addresses 01, 02 or 03 respectively. Eight-bit commands transfer control information to the NCR90C126. The commands are described below.

Command Register 1

Data MSB LSB	Function
0 0 0 0 0 0 0 1	Disable Transmitter: This causes the NCR90C126 to cancel any pending transmit commands by setting the TA bit. After execution, wait 2.3ms to ensure complete packet transmission before reusing the buffer or re-enabling the transmitter.
0 0 0 0 0 0 1 0	Disable Receiver: This causes the NCR90C126 to cancel any pending receive commands by setting the RI bit. If a packet is already arriving when executing this command, it will finish and no more packets will be received. After execution, wait 2.3ms to ensure complete packet reception before re-enabling the receiver.
n n n n n 0 1 1	Enable Transmit from Page nnnnn: This transmits a packet out of buffer RAM nnnnn upon receipt of the token. This command clears TA and TMA. TA = 1 at the completion of the transmission. TMA = 1 when an ACK is received from the destination node. During reset, nnnnn = 11111.
n n n n n 1 0 0	Enable Receive to Page nnnnn: The NCR90C126 receives packets in buffer RAM starting at page nnnnn. This command sets the pointers SRXB, NPRD and NPRX to nnnnn and clears the RI bit. RI is set when no more buffers are available. During reset, nnnnn = 00000.
p 0 0 s s 1 0 1	Size Definition: This tells the NCR90C126 the size of its RAM buffer and if it can receive long or short packets. During reset, ss=00 and p=0.

ss	RAM	p	Packet
00	1K	0	256 bytes
01	2K	1	256/512 bytes
10	4K	When ss=00, only short	
11	8K	packets are supported	

When p=1, AD8 is driven by an internal counter and not by the least significant bit in the NPTX or NPRX pointers so a page must start on an even boundary.

Command Register 1

0 0 0 r p 1 1 0	Clear Flags: This resets the RECON status bit if r=1 and/or the Reset status bits if p=1. During reset, r=0 and p=0.
0 0 0 0 t 1 1 1	Enable Duplicate ID routine: The Duplicate ID (DPID) routine is disabled when t=0 and enabled when t=1. During reset, t=0.

Command Register 2

Data MSB LSB	Function
n n n n n 0 0 1	Write Next Page to Write Pointer (NPWR): This initializes the NPWR pointer to page nnnnn. During reset, nnnnn = 11111.
n n n n n 0 1 0	Write Next Page to Read (NPRD) pointer: This initializes the NPRD pointer to page nnnnn. During reset, nnnnn = 00000.
n n n n n 0 1 1	Initialize Transmit pointers: This initializes Next Page to Transmit (NPTX), Next Page to Write (NPWR) and Start Transmit Buffer (STXB) pointers to page nnnnn. During reset, nnnnn = 11111.
0 0 0 0 0 1 0 0	Enable Chain Transmit: Tells the NCR90C126 to start transmitting from the page pointed to by the NPTX pointer. It stops when the NPTX pointer has reached the NPWR pointer. This command clears TA and TMA. The TA bit is set to 1 at the completion of the transmission. TMA is set to 1 when an ACK is received from the destination node.
b r c 0 0 1 0 1	Write Configuration: This tells the NCR90C126 what mode it is in. When b=1, broadcast messages will be accepted. When r=1, chain receive is enabled. When c=1, circular buffer chaining is enabled. During reset, b=0, r=0, and c=0.

Command Register 3

Data MSB LSB	Function
0 0 0 0 e 0 0 0	LAN Driver Enable/Disable: When e=0, the LAN driver is disabled. When e=1, the LAN driver is enabled. Writing this command causes the NCR90C126 to perform a memory cycle and write the enable/disable bit inverted on AD15. On reset, e=0. This is an optional command used to control the external LAN driver circuitry.

STATUS REGISTERS

Status Registers 1 & 2 are read-only registers that allow the host to monitor the status of the LAN.

Status Register 1 is read from address 00 and Status Register 2 is read from address 04. In the NCR90C26 mode, only Status Register 1 is used.

Status Register 1

7	6	5	4	3	2	1	0
RI	ETS2	ETS1	RESET	DPID	RECON	TMA	TA

Bits	Name	Description
0	TA	Transmitter Available: When TA=1, the node is available for a transmit sequence. It also indicates that any previous Enable Transmit process is complete. TA is cleared by the Enable Transmit and Enable Chain Transmit commands. TA is set after packets have been transmitted and acknowledged or if there is no ACK and the node has timed out.
1	TMA	Transmit Message Acknowledged: When TMA=1, a message sent from a previous Enable Transmit command was acknowledged by the receiving node. TMA is cleared by the Enable Transmit and Enable Chain Transmit commands. TMA is set after the packets have been transmitted and acknowledged by the receiving node.
2	RECON	Reconfiguration Flag: When RECON is set to 1, a system reconfiguration took place due to the expiration of an idle time-out. RECON is reset by the Clear Flags command.
3	DPID	Duplicate ID: This status bit is set when the Duplicate ID routine is enabled and a duplicate node ID is detected. It is cleared when the Duplicate ID routine is disabled. See the DPID Diagnostic Routine for more information.
4	RESET	Reset: When this bit is set to 1, the NCR90C126 experienced a reset from one of three sources: 1. An active signal on the RESET input. 2. The power-on-reset cell has been triggered by the application of power. 3. The Reset command has been executed. The RESET status bit is cleared by the Clear Flags command.
5-6	ETS1, ETS2	Extended Timeout Status 1 & 2: The state ETS2 of these bits reflects the logic level on the ETS1 & ETS2 pins. Under normal operating conditions, ETS1 & ETS2 will be 1.
7	RI	Receiver Inhibited: When RI is set to 1, the NCR90C126 is not receiving any messages from other nodes. RI is cleared by the Enable Receive command when a buffer is available in the Buffer Chain mode. RI is set when a packet has been received or when no more buffers are available in the Buffer Chain mode.

Status Register 2

7	6	5	4	3	2	1	0
1	1	1	TR	IL1	IL0	CD	RP

Bits	Name	Description
0	RP	Received Packet: When RP=1, a packet has been received in the Buffer Chain mode. RP is cleared by the read NPRX command.
1	CD	Carrier Detect: When CD=1, the NCR90C126 is detecting activity on the RXIN pin. CD is cleared when the NCR90C126 switches between transmit and receive modes.
2-3	IL0, IL1	Interrupt Level Encode Bits: The user encodes the interrupt level at which the board is set using these bits. These are for software use only; no hardware function is associated with these bits.
4	TR	Token Received: This bit is set each time the token is addressed to and received by this node. It is cleared by the Enable Receive command.

Interrupt Mask Registers

The Interrupt Mask Registers are write-only registers that determine which of the five maskable conditions will cause an interrupt. (See the HOST INTERRUPTS section on page 16 for details.)

Pointers

The Next Page to Receive (NPRX) pointer is read from address 02. The format of the data is:

1 1 1 A12 A11 A10 A9 A8 - Read NPRX pointer. By executing this, the RP bit will be reset.

The Next Page to Transmit Pointer is read from address 03. The format of the data is:

1 1 1 A12 A11 A10 A9 A8 - Read NPTX pointer.

Reset Register

When register 08 is accessed (read or write), the NCR90C126 is reset. This provides the host a means for resetting the NCR90C126 from software.

RESET OPTIONS

There are three reset options for the NCR90C126. When power is applied to the chip, the POR cell senses this and generates an internal signal to reset the chip. Another option resets the chip when a high signal is applied to the Reset pin for a minimum of 100ns. It is also possible to reset the controller section of the chip by reading or writing to I/O location 08.

The NCR90C126 executes a reset routine that writes D1H to address 0 and writes the node ID to address 1 in buffer RAM. In mode 1, the configuration switches are also read.

SOFTWARE CONSIDERATIONS

NCR90C98 MODE

The transmit and receive buffers can be used as standard or circular buffers with the latter being the most efficient. The standard method for the host to transmit packets of information in the buffer chaining mode follows.

1. Initialize transmit pointers.
2. Write a packet to the buffer pointed to by the NPWR pointer.
3. Set the NPWR pointer to next free page.
4. If TA=1, execute the Enable Chain Transmit command.
5. If more packets are to be transmitted, go back to step 2.
6. When NPWR=NPTX, TA & TMA are set as described in the *STATUS REGISTERS* description on page 14.
7. If not in the circular mode, go to step 1 when reaching the end of the buffer.

The NPTX pointer will stop when it has reached the end of the buffer. However, if the circular mode has been enabled, the NPTX pointer will reload the STXB pointer when it has reached the end of the buffer. For short packets, the last page of the buffer is unavailable if the circular mode is disabled.

It is possible for the chain transmit to be blocked. If the destination node has its receiver disabled, the controller will get NAKs and pass the token, so every transmission must have a timer associated with it. The timer should be reset each time a packet is loaded. Its value should be equal to the maximum time allocated to transmit a packet (100ms) multiplied by the number of packets in the transmit buffer. If the timer expires, the disable transmitter command must be executed.

Follow these steps if the chain transmit stopped due to a blocked transmitter or an error (TA=1, TMA=0 due to a nonexistting node or a destination node failed to send back an ACK).

1. Transmit the remaining packets one by one with the Enable Transmit command. (The NPTX pointer points to the offending packet.)
2. Execute the Initialize Transmit Pointers command to reset the transmit pointers to the start of the transmit buffer.
3. Resume normal operation.

The standard method for the host to receive packets of information in the buffer chaining mode follows.

1. Execute the Enable Receive command.
2. When the RP interrupt occurs, read the packet pointed to by the NPRD pointer.
3. Increment the NPRD pointer and write it to the controller.
4. Read the NPRX pointer which will reset the RP flag.
5. If the NPRX pointer is not equal to the NPRD pointer, more packets have been received. Read the packet pointed to by the NPRD pointer and go to step 3.
6. If the NPRX pointer equals the NPRD pointer, all the received packets have been read. Go to step 2.

With the circular mode disabled, NPRX=STXB after the last page has been filled with the RI bit set. With the circular mode enabled, the NPRX will reload the SRXB pointer when it has reached the end of the buffer. When NPRX=NPRD, the RI bit is set.

DPID DIAGNOSTIC ROUTINE

The Duplicate ID (DPID) routine functions as a diagnostic tool to be run before a node goes on line. It checks to see if there are other nodes on the network that respond to its own node ID during a token pass.

The routine listens for token passes to its own node ID. If one occurs, the node waits for the maximum time a node has to respond to a token pass. If activity is detected on the line during this time, another node is responding to the token pass, and the DPID bit is set. If no activity is detected, the routine restarts and listens for token passes to itself again.

The DPID bit has a maskable interrupt bit associated with it which generates an interrupt when the DPID bit is set. The minimum time it takes to detect a duplicate ID is one token rotation around the loop. The maximum time is the time it takes to reconfigure the system.

In the DPID mode, the NCR90C126 does not reset the reconfiguration counter so this node experiences a reconfiguration when the counter expires. To avoid reconfiguring the network, the node should be designed so the LAN transmitter can be disabled/enabled by the software. This is done with the Enable/Disable LAN transmitter command. Bit AD15 controls the transmitter enable signal via an external flip-flop. When the node executes the power-on routine, a 1 will be written on AD15 which should be used to disable the LAN transmitter.

This is the procedure for using the DPID routine.

1. Enable the DPID interrupt by writing the correct mask to the Interrupt Mask register.
2. Enable the DPID routine by the Enable Duplicate ID command which puts the node in a listen only mode.
3. If no duplicate ID was detected after 840ms, disable the DPID routine and enable the LAN transmitter. The node will go through a normal reconfiguration to put itself on line.

HOST INTERRUPTS

The NCR90C126 generates an interrupt on the IRQ pin in response to several of the conditions that set status bits. The Interrupt Mask Registers determine which of the five conditions will cause an interrupt. The status bits TMA, ETS1, ETS2 and CD have no corresponding mask bits and do not cause interrupts. The five maskable status bits are outlined in the following diagram.

Interrupt Mask Register 1

7	3	2	0
RECEIVE INHIBIT	DPID	RECON TIMEOUT	TRANSMITTER AVAILABLE

Interrupt Mask Register 2

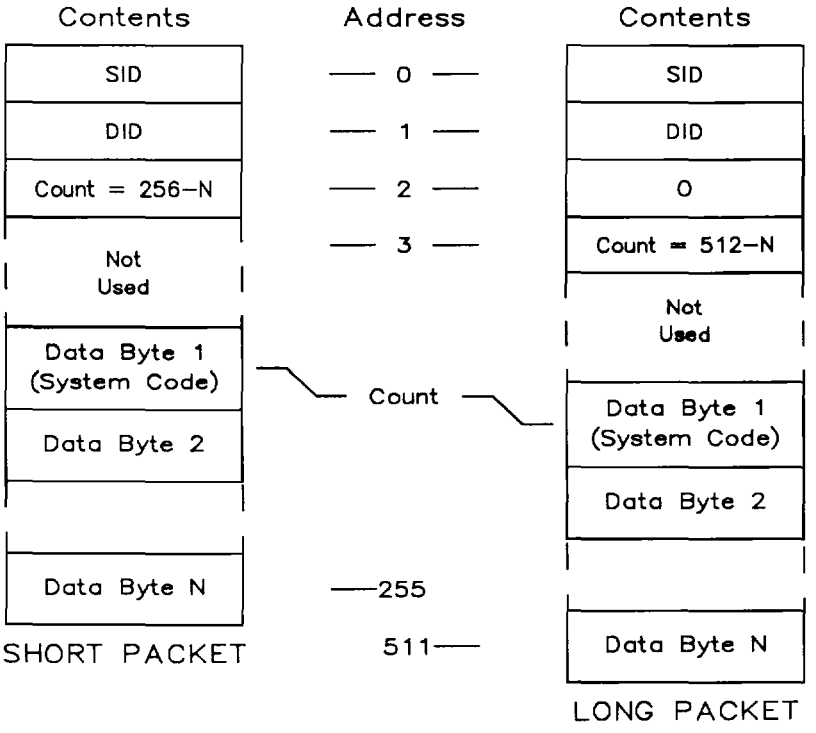
	0
	RECEIVED PACKET

Setting any of these bits to 1 will enable the IRQ signal to be asserted high when the corresponding status bits go high. The unused bits in the Interrupt Mask Register 2 must be written to zero. Once the IRQ signal is high, it can be

cleared by clearing the corresponding bit in the Status Register or the Mask Register. RP is cleared by reading the NPRX pointer. Reset generates a nonmaskable interrupt. It is cleared by the Clear Flags command.

RAM BUFFER MEMORY MAP

Figure 6 shows the locations of the major components for both Short (up to 256 bytes) and Long (up to 512 bytes) packets.



NOTE: Adresses shown are relative to a Page, not absolute. SID = Source ID (not written in Transmit Packets). DID = Destination ID (set=0 for Broadcasts). N = Message Length. Not Used bytes imply message is less than maximum length. These bytes would be written for Max. Messages: SHORT = 253 bytes, LONG = 508.

Figure 6 RAM Buffer Map

DETAILED HOST INTERFACE DESCRIPTION

PC XT INTERFACE

The PC XT interface consists of 20 address lines, 8 data lines and 8 control lines. These correspond to similar signals on the PC XT bus. Figures 7 and 8 show the NCR90C126 in mode 0 and mode 1 respectively, and include the ROM and LAN driver control hardware. The address lines combined with the control lines are decoded by the chip to determine valid accesses. The NCR90C126 controls all the data transfers on the multiplexed address/data bus and does the arbitration between the host and itself. The transceiver ('245) is used to isolate the host and the local bus. Its direction is controlled by the DIR signal and its output drivers are controlled by OE2.

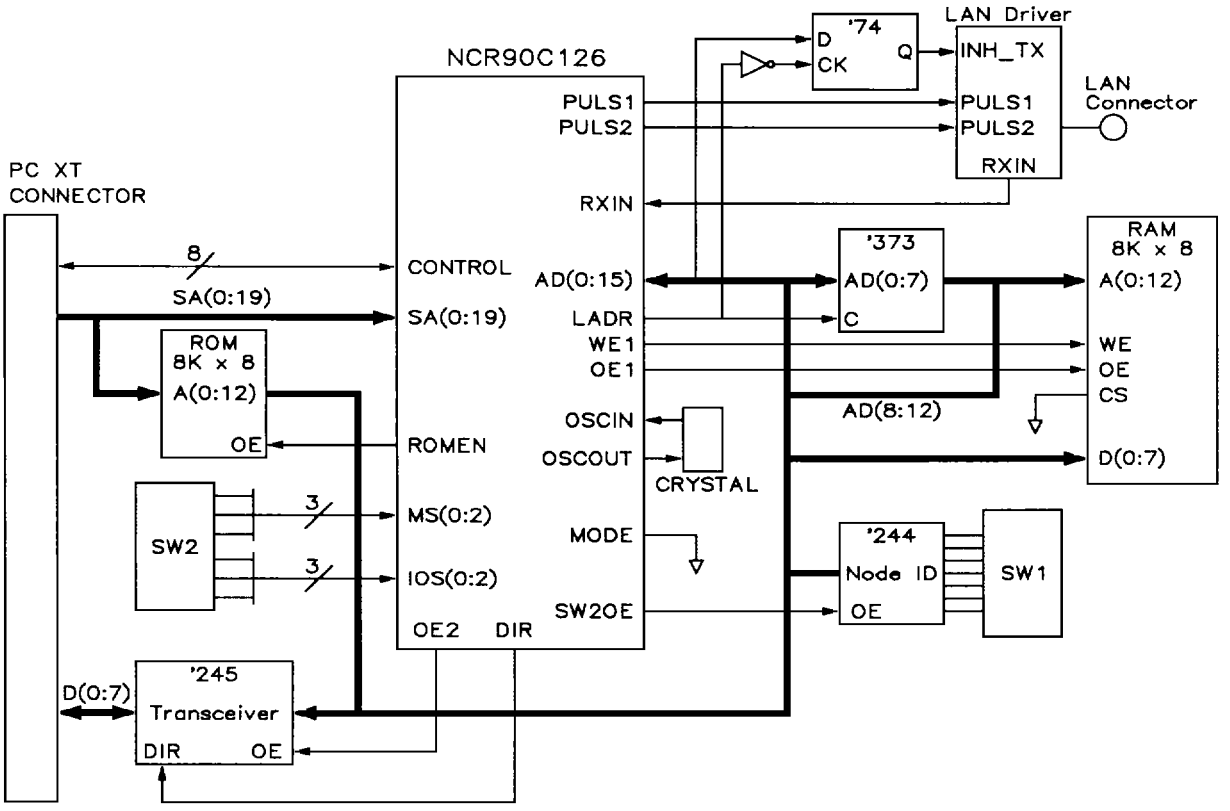


Figure 7 Mode 0 System Block Diagram

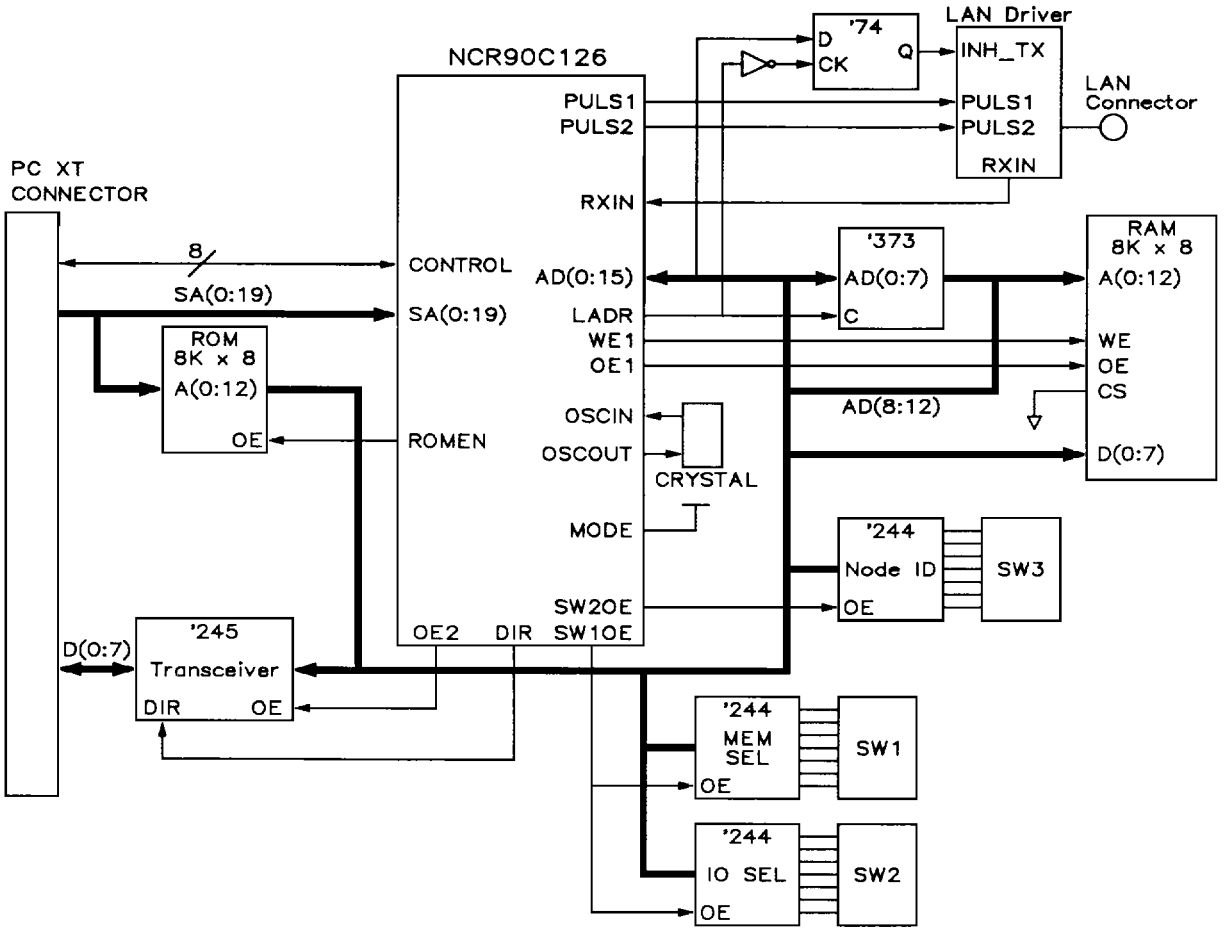


Figure 8 Mode 1 System Block Diagram

I/O AND MEMORY ACCESSES

The internal registers are I/O and memory mapped. The internal registers are available in the memory map only if the MIO bit is set when the node ID value is read.

When the NCR90C126 accesses the RAM buffer memory over the multiplexed address/data bus, the ('373) latches the low-order address byte on the falling edge of LADR. The high-order address lines are driven on AD(8:12) throughout the cycle. The 8-bit data is then transferred over the multiplexed address/data bus during the second half of the cycle.

Figure 9 shows how the on-board ROM, RAM buffer memory and internal registers appear in the host's memory map.

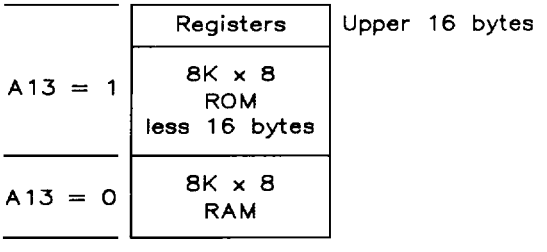


Figure 9 16K Byte Memory Organization

MODE 0 AND MODE 1

Mode 0 and 1 control what options are available on the NCR90C126. All address decoding is disabled until the chip has read the configuration switches. The node ID/Options are read into the NCR90C126 from the multiplexed address/data bus on the rising edge of SW2OE. The buffers ('244s) in Figures 7 and 8 put the data onto the bus when the appropriate strobe occurs.

In mode 0, the part count is reduced by reading the memory and I/O switch settings on dedicated pins. The memory and I/O switch settings are read into the NCR90C126 from the MS(0:2) and IOS(0:2) signals. The ROM is always enabled in this mode.

In mode 1, more features are supported by reading 16 bits of information from the multiplexed address/data bus. The memory and I/O switch settings are read into the NCR90C126 from the address/data bus on the rising edge of SW1OE.

The switch settings are described below. To read the correct data, all bits must be driven when SW1OE and SW2OE are active.

Memory and I/O Switch Settings (read by SW1OE)

AD line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	ET2	ET1	A9	A8	A7	A6	A5	A4	RD	S/D	A19	A18	A17	A16	A15	A14

Bits	Name	Description
0–5	A14–A19	Upper Memory Address Bits: These bits indicate which address range the NCR90C126 responds to during memory reads or writes. The NCR90C126 responds when the upper system address bits (SA14–SA19) match these bits and the appropriate control lines are active. This allows the user to configure the NCR90C126 system into any 16K address space, instead of being limited to eight address ranges in mode 0.
6	S/D	Standard/Dual Port Memory: When set, this bit disables bus arbitration. It is cleared during reset.
7	RD	ROM Disable: During reset, this bit enables use of an on-board ROM. When cleared, the ROM is disabled.
8–13	A4–A9	I/O Address Bits: These bits indicate which address the NCR90C126 responds to during I/O reads or writes. The NCR90C126 responds when the system address bits (SA4–SA9) match these bits and the appropriate control lines are active. This allows the user to configure the NCR90C126 system into any 16-byte address space, instead of being limited to eight address ranges in mode 0.
14–15	ET1–ET2	Extended Timeout: In mode 1, these bits provide the values for the extended time-out functions. Their value is reflected in bits 5 and 6 of Status Register 1.

Node ID Switch Settings (read by SW2OE)

AD line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	MIO	IL1	IL0	–	–	–	–	–	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bits	Name	Description
0–7	ID0–ID7	Node ID Bits: These node ID symbols represent the 8-bit node ID with ID0 as the least significant bit.
13–14	IL0–IL1	Interrupt Levels: These bits reflect the switch settings on AD13 and AD14 when the node ID is read. They are available to system designers to define as they wish. One use is for the software to prioritize an interrupt based on the value read here.
15	MIO	Memory Mapped I/O: When set, this bit disables memory mapped access to the NCR90C126 registers. When cleared, the registers are accessible through the memory map. The registers are always available through the I/O map.

LAN DRIVER ENABLE/DISABLE

If disabling of the LAN driver is desired, a flip-flop to hold the disable bit and an inverter ('04) must be added to the system. The LAN Driver Enable/Disable command allows the host to selectively turn the LAN driver on or off. See *the COMMAND REGISTER* description for the NCR90C98 Mode starting on page 12.

DUAL PORT MEMORY

In mode 1, when the S/D bit is set, the NCR90C126 does not arbitrate during memory cycles. The ARCNET protocol ensures data integrity in RAM but in test modes, the same location must not be accessed by the NCR90C126 and host at the same time; the dual port RAM will inhibit one of the accesses. Figure 10 shows a dual port memory system.

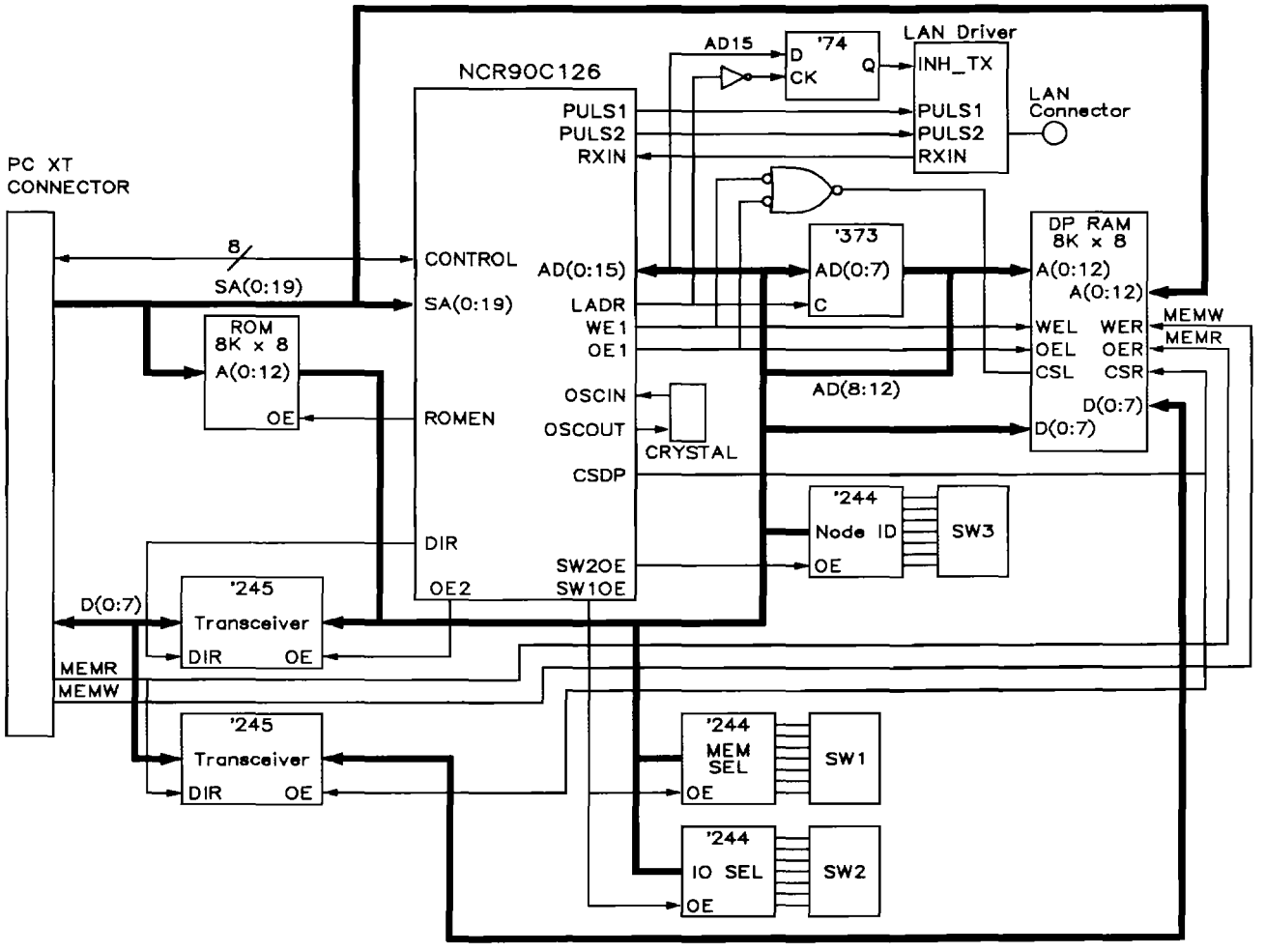
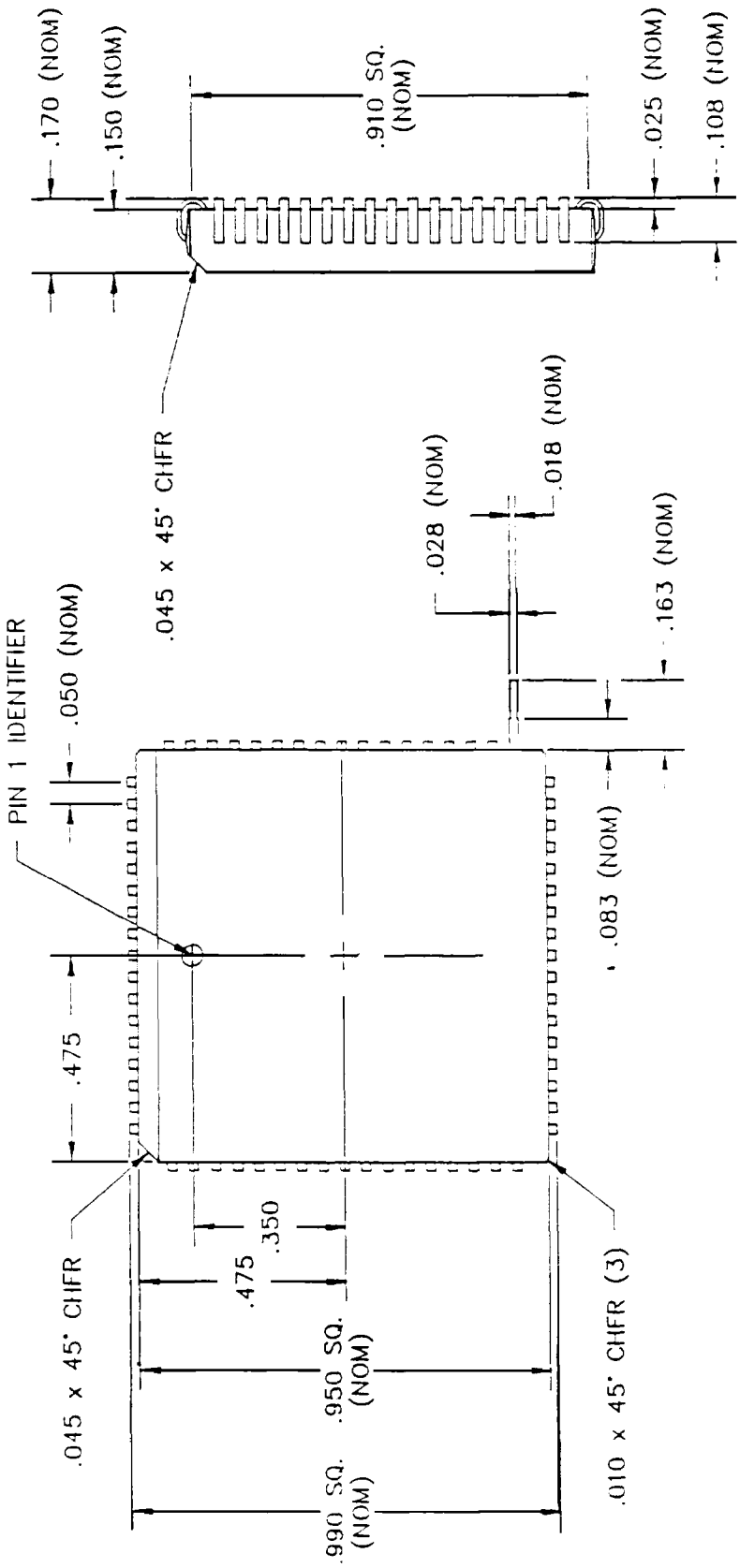


Figure 10 Dual Port Memory System Block Diagram

MECHANICAL SPECIFICATIONS



NOTE : All dimensions are in inches.

ORDERING INFORMATION

The NCR90C126 is available in a 68-pin Plastic Leaded Chip Carrier (PLCC). The following part number should be used to order the part.

Package Type	Part Number
68-pin PLCC	NCR90C126PP

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUMS

Symbol	Parameter	Minimum	Maximum	Units
T_A	Operating Temperature	0	70	°C
T_S	Storage Temperature	−55	150	°C
V_{DD}	Supply Voltage	−0.5	7.0	V
V_{IN}	Input Voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS} − 0.5	V_{DD} + 0.5	V
T_L	Lead Temperature (Soldering 10 seconds maximum)		250	°C

DC CHARACTERISTICS

(V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
V_{IL}	Low Input Voltage		0.8	Volts
V_{IH}	High Input Voltage	2.0		Volts
V_{IL}	Clock Low Input Voltage (OSCIN)		1.35	Volts
V_{IH}	Clock High Input Voltage (OSCIN)	3.85		Volts
V_{IL}	Low Input Voltage for AEN, IOR, IOW, MEMR, MEMW (Schmitt trigger)	0.9	1.5	Volts
V_{IH}	High Input Voltage for AEN, IOR, IOW, MEMR, MEMW (Schmitt trigger)	1.3	1.9	Volts
V_{OL}	Low Output Voltage (V_{DD} = 4.5V) (I_{OL} = 4mA)		0.4	Volts
V_{OH}	High Output Voltage (V_{DD} = 4.5V) (I_{OH} = −2mA)	2.4		Volts
C_{IN}	Input Capacitance		10	pF
I_P	Input Pullup Current for AD(0:15), ET1, MS(0:2), IOS(0:2), and MODE (V_{OL} = 0.0V)	50	165	µA
I_{IL}	Input Leakage Current (V_{DD} = 5.5V)		±10	µA
I_{DD}	Power Supply Current (V_{DD} = 5.5V)		25	mA
I_{OL}	Low Output Current for IOCHRDY and IRQ (V_{OL} = 0.4V)		24	mA

AC CHARACTERISTICS

(V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
1	OSC low	11, 13		25		ns
2	OSC period	11, 13		50		ns
3	Request to IOCHRDY	11, 13			32	ns
4	OE2 to IOCHRDY high (Memory Read/Write)	13	100			ns
5	Delay from request to OE1, OE2 inactive	11, 13			39	ns
6	Request to DIR	11, 13			20	ns
7	LADR pulse width	13, 15		25		ns
8	Address setup to LADR	13, 15	12			ns
9	Address hold from LADR	13, 15	15			ns
10	AD invalid to OE1, OE2	13, 15	0			ns
11	OE2 to valid data	11			60	ns
12	Data setup to WE1, NCR90C126 cycle	16	90			ns
13	Data hold from WE1, NCR90C126 cycle	16	50			ns
14	WE1 pulse width	14, 16		100		ns

(V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Fig.	Min.	Typ.	Max.	Units
15	OE2 to WE1 high	14	90			ns
16	OE1 pulse width, NCR90C126 cycle	15		100		ns
17	Synchronization time	13, 14	50		150	ns
18	MEMR to ROMEN low	19	50			ns
19	MEMR to OE2 low	19	50			ns
20	OE2 to IOCHRDY high (ROM access)	19	150			ns
21	Request to CSDP	17, 18			30	ns
22	SW1OE, SW2OE pulse width	20		100		ns
23	Data setup to SW1OE, SW2OE rise	20	30			ns
24	Data hold from SW1OE, SW2OE rise	20	0			ns
25	RXIN pulse width	21	10			ns
26	OE2 to Data	12			50	ns
27	OE2 to IOCHRDY high (I/O Read/Write)	11, 12	150			ns
28	RESET pulse width	22	100			ns

OSCILLATOR/CRYSTAL SPECIFICATIONS

(V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

Parameter	Minimum	Typical	Maximum
CRYSTAL			
Tolerance			±0.01%
Motion Resistance			25 Ω
Frequency		20 MHz	
EXTERNAL CLOCK			
Duty Cycle	40%		60%

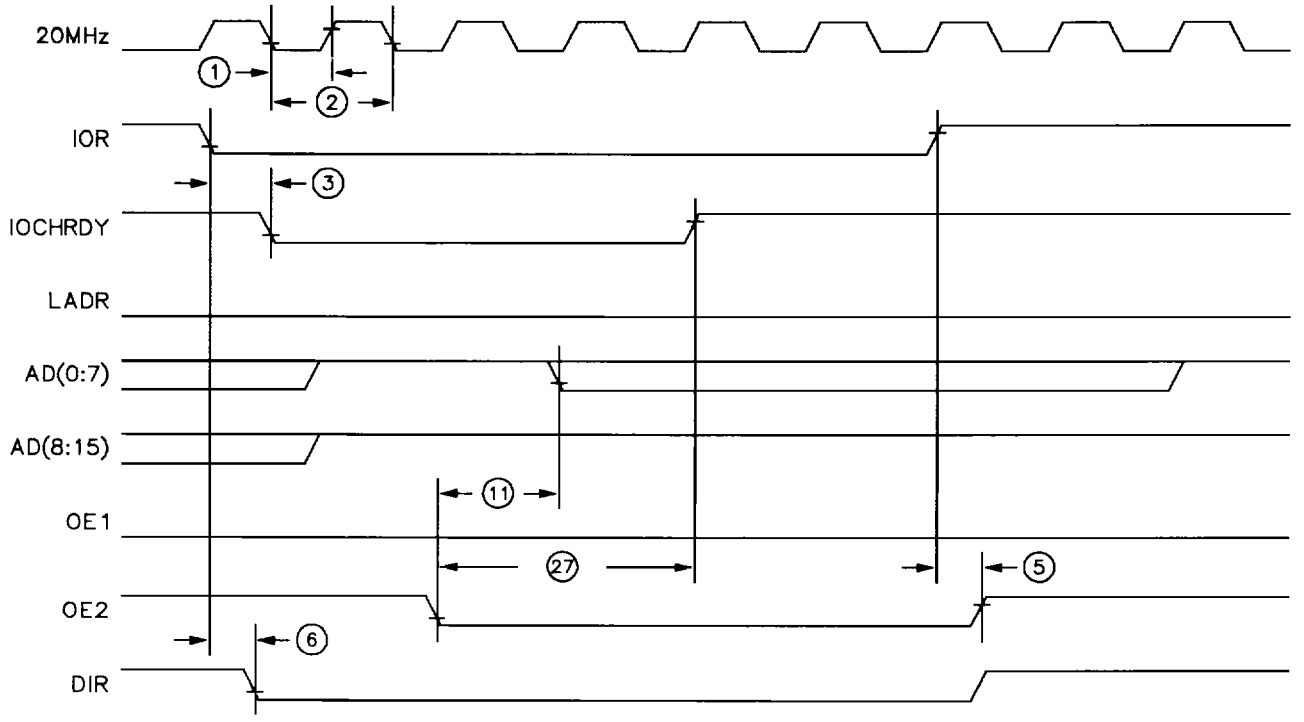


Figure 11 PC XT I/O Read Cycle

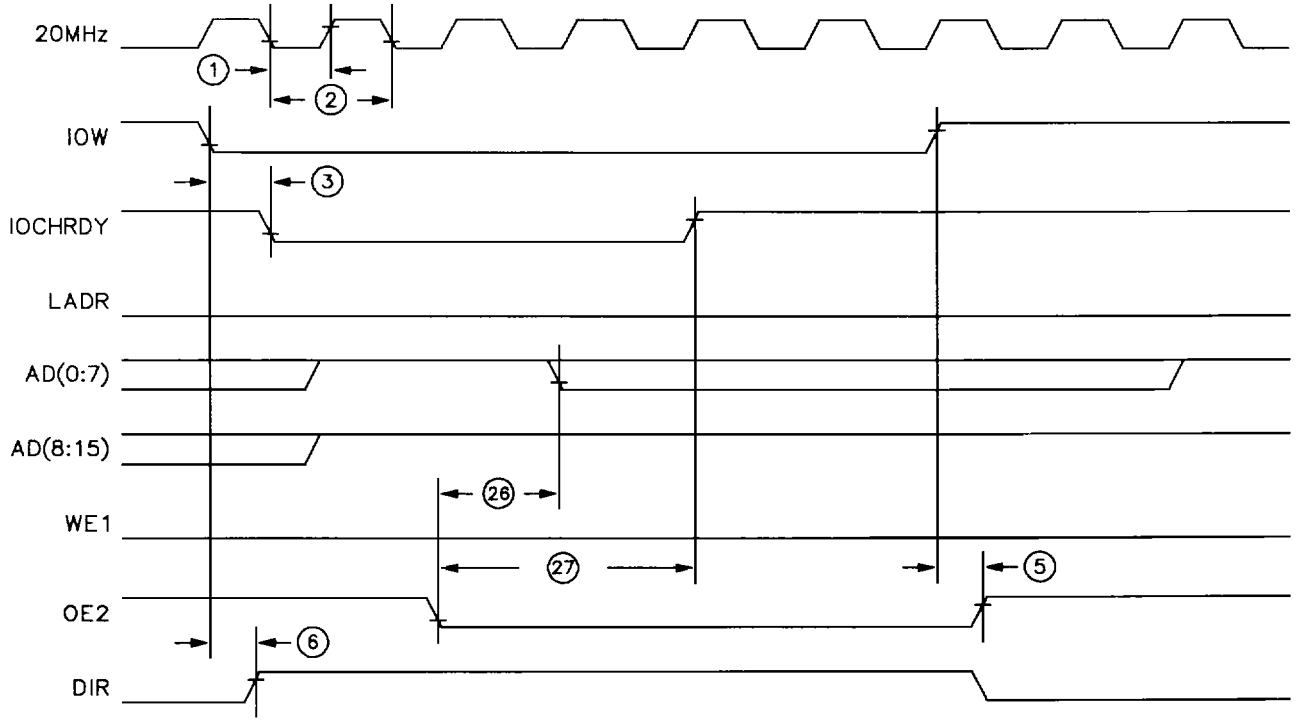


Figure 12 PC XT I/O Write Cycle

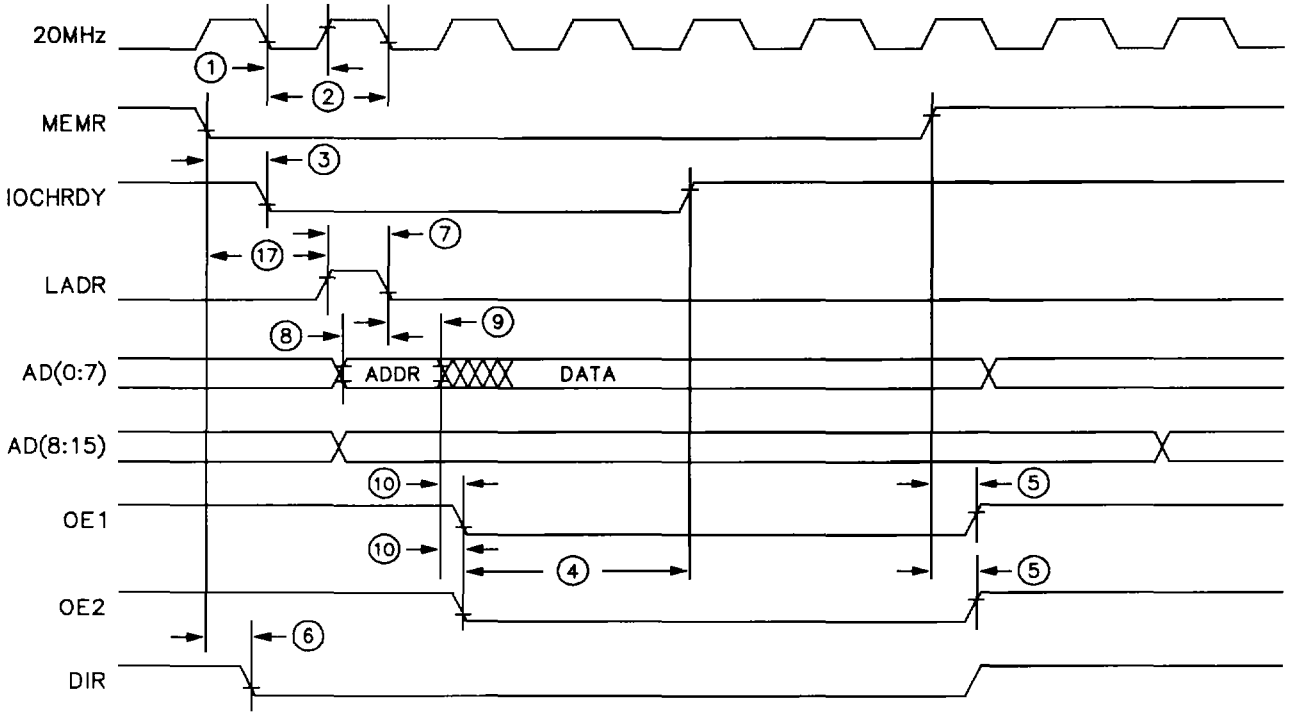


Figure 13 PC XT Memory Read Cycle

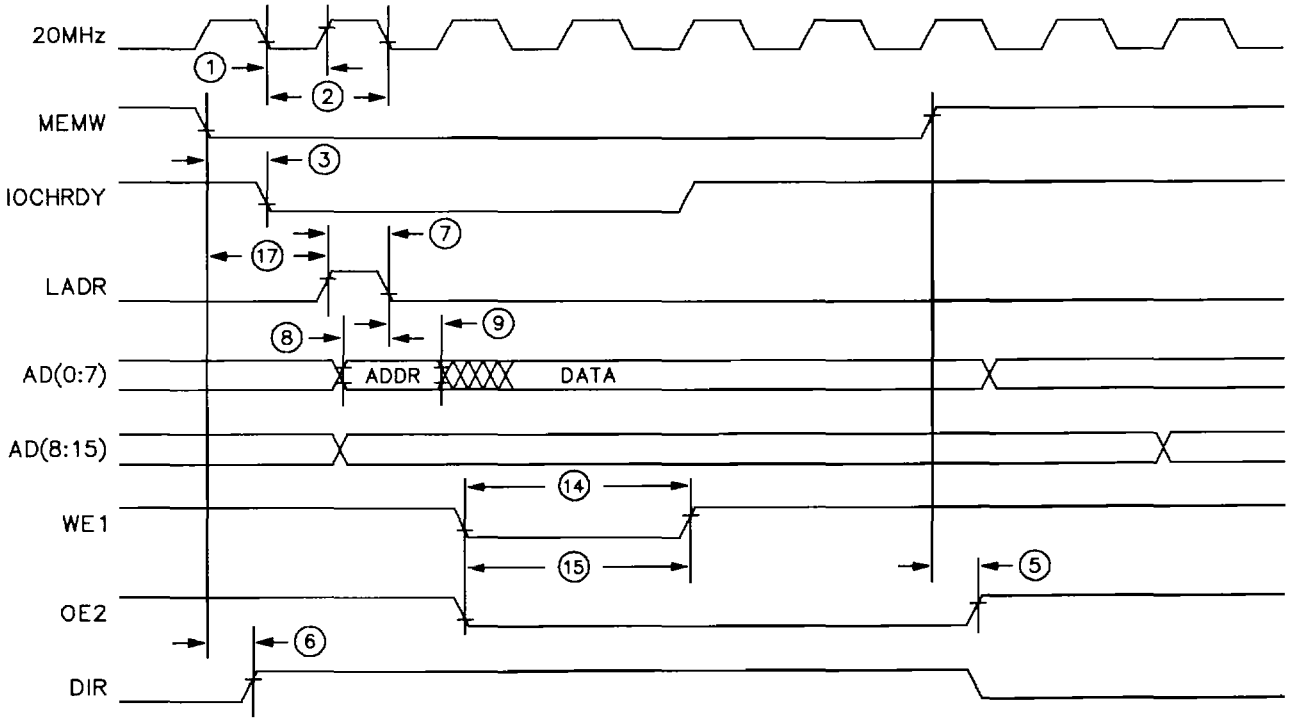


Figure 14 PC XT Memory Write Cycle

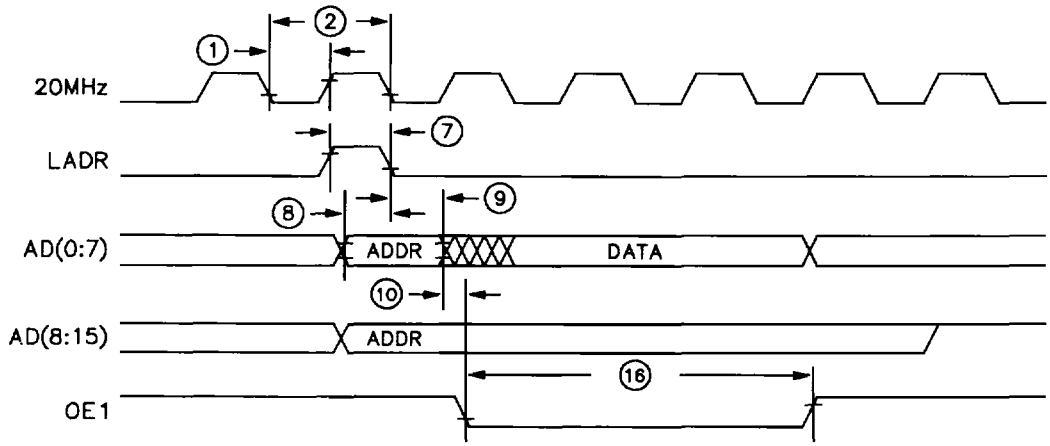


Figure 15 NCR90C126 Memory Read Cycle

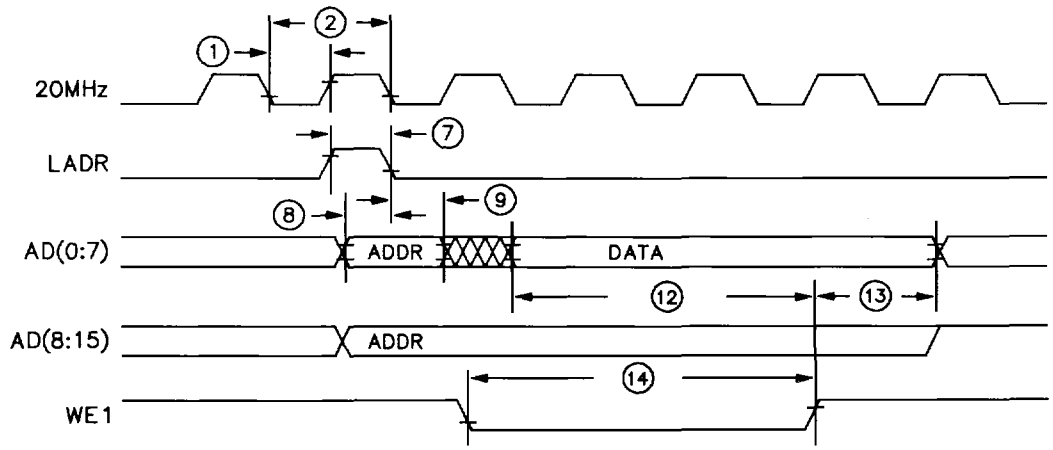


Figure 16 NCR90C126 Memory Write Cycle

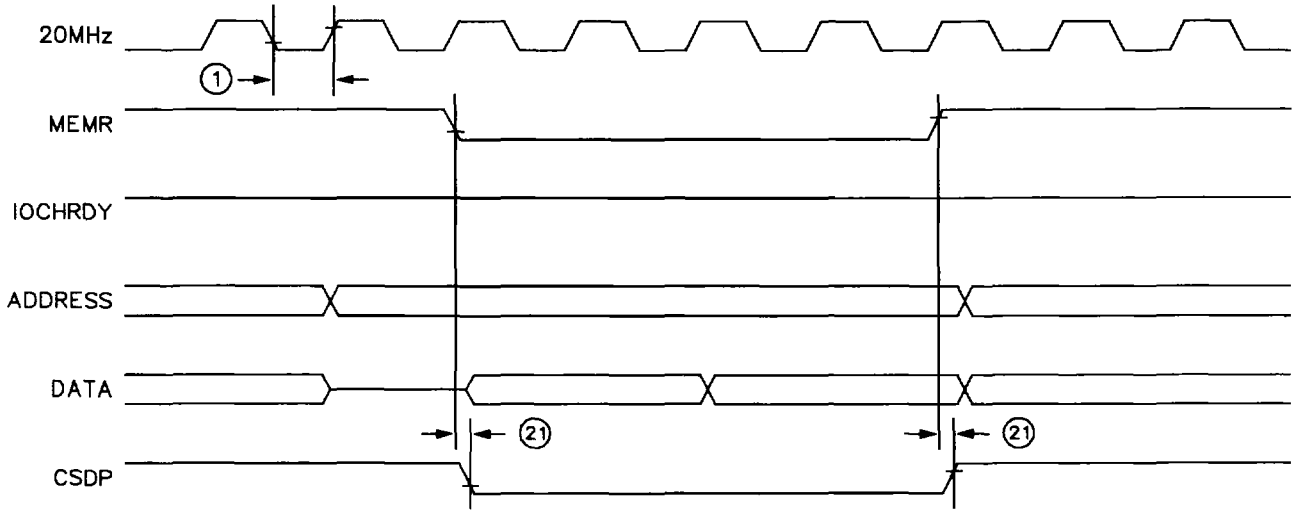


Figure 17 Dual Port Memory Read Cycle

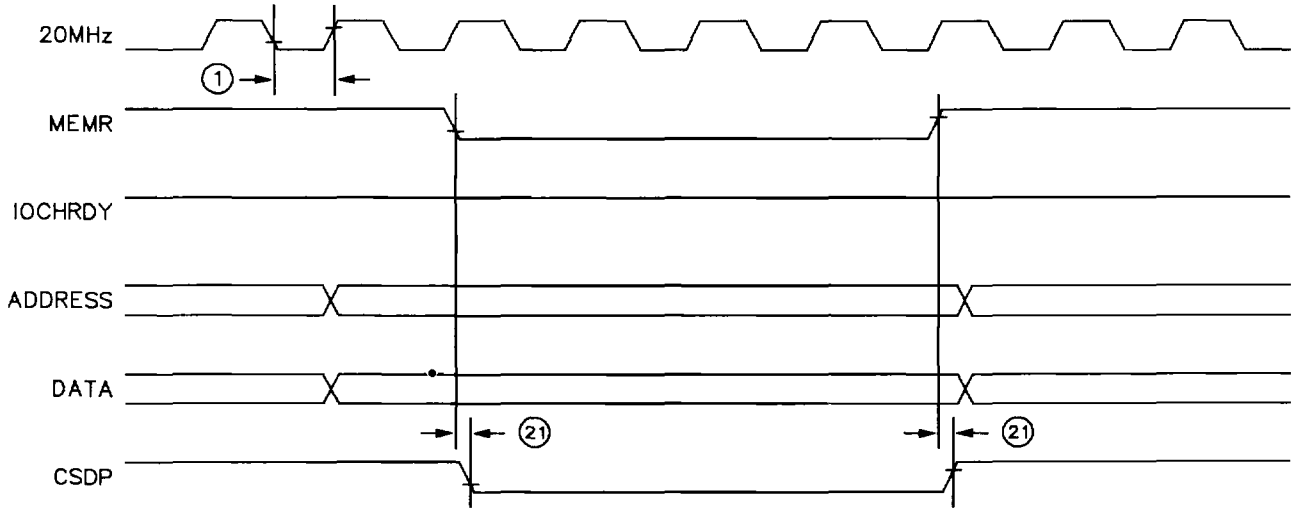


Figure 18 Dual Port Memory Write Cycle

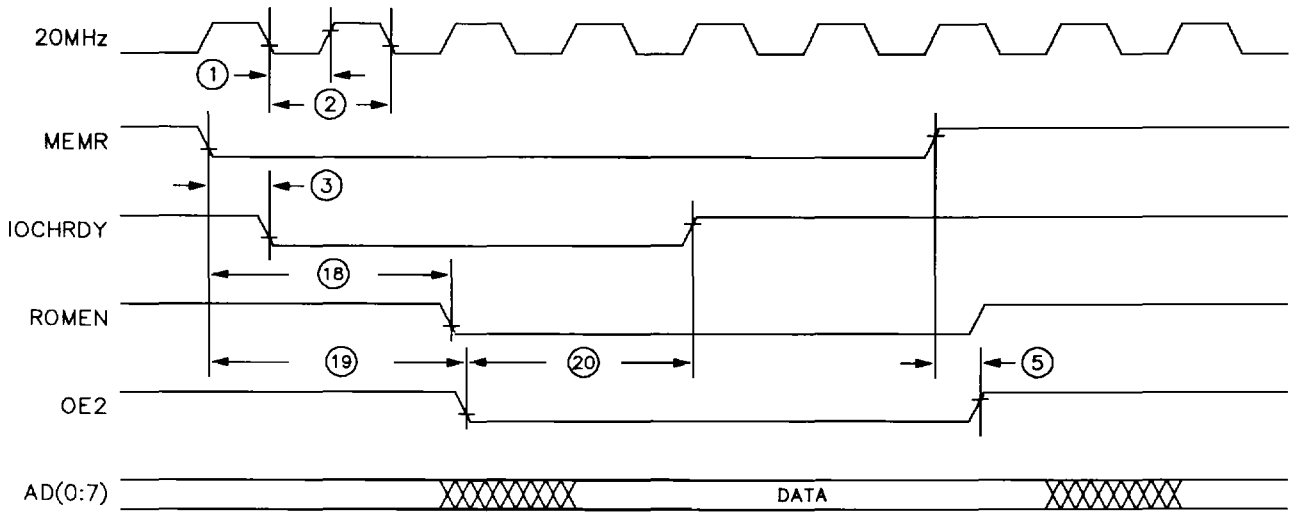


Figure 19 ROM Read Cycle

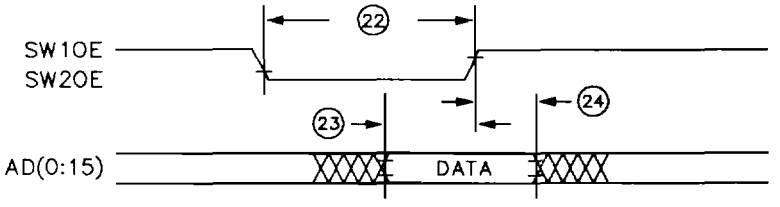


Figure 20 Read Switch Timing

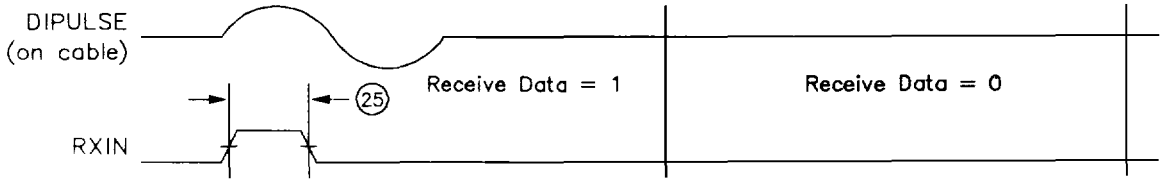


Figure 21 Receive Data

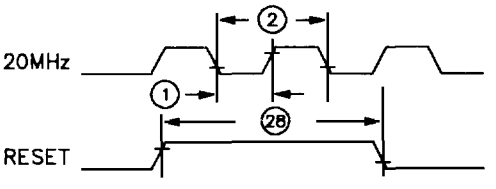


Figure 22 RESET Pulse Width

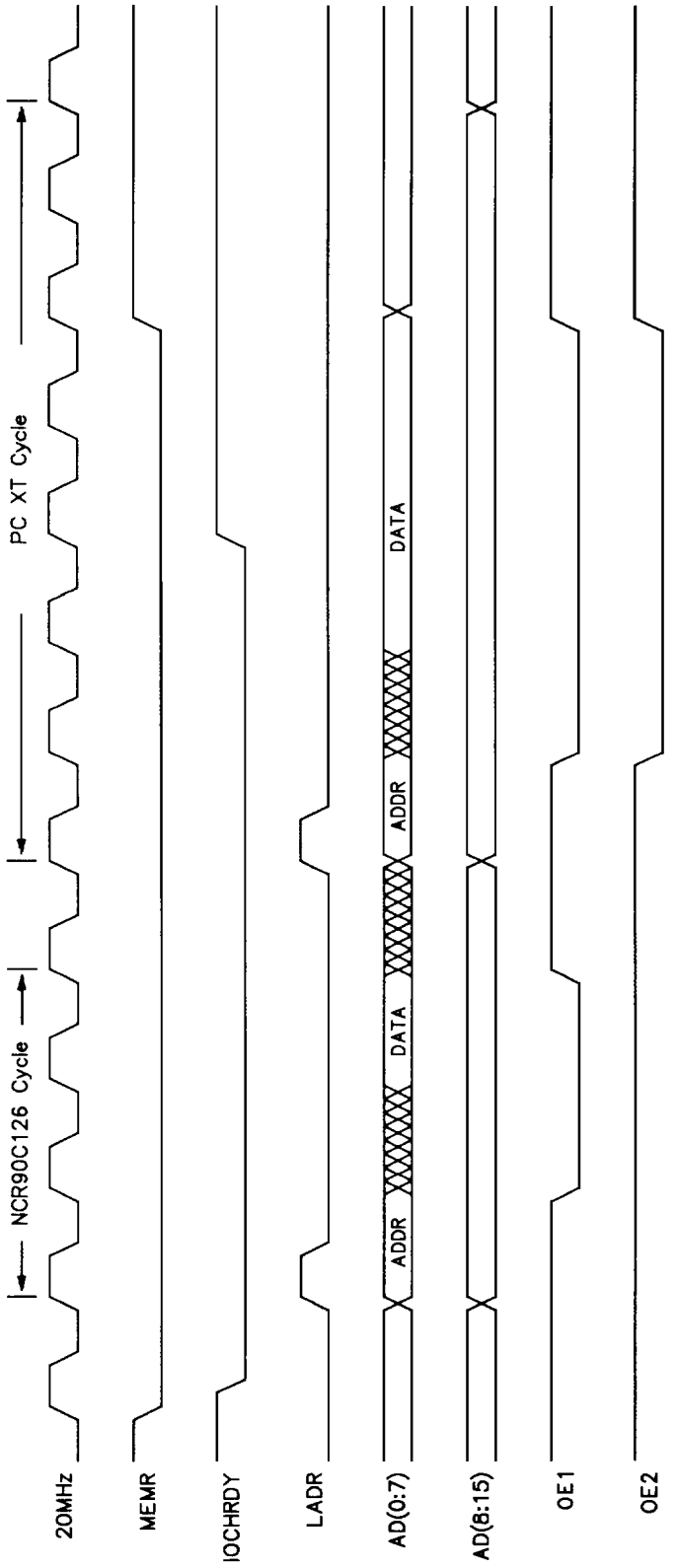


Figure 23 PC XT/NCR90C126 Memory Read Cycle, Worst Case

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