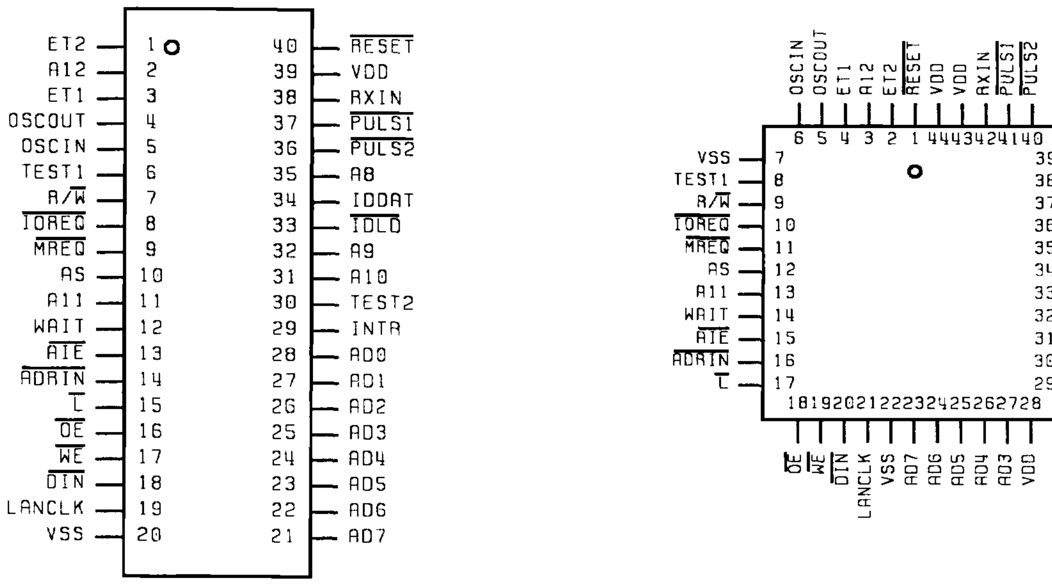
NCR ARCNET®
CONTROLLER/TRANSCEIVER

FEATURES

- Supports Buffer Chaining in external SRAM
- Fully controls 8K bytes of external SRAM containing host messages
- Host arbitration and memory access times are twice as fast as the NCR90C26.
- Supports three Reset Options
  - Power-On-Reset (no external signal required)
  - External Reset
  - Software Generated Reset
- 20 MHz On-chip Oscillator
- ADRIN & DIN signals are provided to multiplex address and data
- Software Compatible with the NCR90C26
- Flexible microprocessor interface
- Supports broadcast messages to all nodes on LAN
- Token Passing Protocol provides predictable transfer intervals
- Network supports up to 255 nodes
- Maximum distance between active elements is 610 meters, total system distance 6100 meters.
- Data transferred at 2.5 Megabits per second
- Automatically reconfigures when the number of nodes change
- Available in 40-pin DIP and 44-pin PLCC



40-pin DIP

44-pin PLCC

Figure 1 40-pin DIP and 44-pin PLCC

NCRMS006

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NCRMS006

Pin Out Summary

Signal Name	Type	Pin Number		Pin Description
		40-pin DIP	44-pin PLCC	
$\overline{RESET}$	Input	40	1	Reset
ET2	Input	1	2	Extended timeout functions
A12	Output	2	3	Page Select
ET1	Input	3	4	Extended timeout functions
OSCOUT	Output	4	5	Output from internal OSC
OSCIN	Output	5	6	Input to internal OSC or external clock
V_{SS}	Ground	-	7	Ground
TEST1	Input	6	8	Test pin 1
R/$\overline{W}$	Input	7	9	Read/Write
$\overline{IOREQ}$	Input	8	10	I/O request
$\overline{MREQ}$	Input	9	11	Memory request
AS	Input	10	12	Address Strobe
A11	Output	11	13	Page select
WAIT	Output	12	14	Wait
$\overline{AIE}$	Output	13	15	Address input enable
$\overline{ADRIN}$	Output	14	16	Address/data input enable
$\overline{L}$	Output	15	17	Latch enable
$\overline{OE}$	Output	16	18	Output enable
$\overline{WE}$	Output	17	19	Write enable
$\overline{DIN}$	Output	18	20	Data input enable signal
LANCLK	Output	19	21	Network clock
V_{SS}	Ground	20	22	Ground
AD7	In/Out	21	23	Address/data bus pin
AD6	In/Out	22	24	Address/data bus pin
AD5	In/Out	23	25	Address/data bus pin
AD4	In/Out	24	26	Address/data bus pin
AD3	In/Out	25	27	Address/data bus pin
V_{DD}	Power	-	28	+5 volt supply
V_{SS}	Ground	-	29	Ground
AD2	In/Out	26	30	Address/data bus pin
AD1	In/Out	27	31	Address/data bus pin
ADO	In/Out	28	32	Address/data bus pin
INTR	Output	29	33	Interrupt
TEST2	Input	30	34	Test pin 2
A10	Output	31	35	Page select
A9	Output	32	36	Page select
$\overline{IDLD}$	Output	33	37	ID load
IDDAT	Input	34	38	ID data in
A8	Output	35	39	Address line 8
$\overline{PULS2}$	Output	36	40	Pulse 2 (transmitter out)
$\overline{PULS1}$	Output	37	41	Pulse 1 (transmitter out)
RXIN	Input	38	42	Receive data in
V_{DD}	Power	39	43	+5 volt supply
V_{DD}	Power	-	44	+5 volt supply

GENERAL DESCRIPTION

The NCR90C98A Controller/Transceiver includes all logical functions of an ARCNET RIM (Resource Interface Module - see Figure 2). CMOS technology makes it ideal for low-power applications. ARCNET is a popular token-passing Local Area Network (LAN) scheme developed by Datapoint Corp. The NCR90C98A handles all tasks for transferring data between the node and the LAN. It reads and writes Message Buffers in an external RAM, it initiates and responds to valid ARCNET transmissions, and passes control between itself and the other RIMs on the network. The NCR90C98A also contains the interface to the cable-driving circuitry that hooks up to the physical LAN media.

The NCR90C98A is an enhanced single-ichip version of the NCR90C26 and NCR90C32 combining the ARCNET controller and transceiver functions. A few of the enhancements include increased buffer size, buffer chaining, and an on-chip POR cell and oscillator. (See Figure 3).

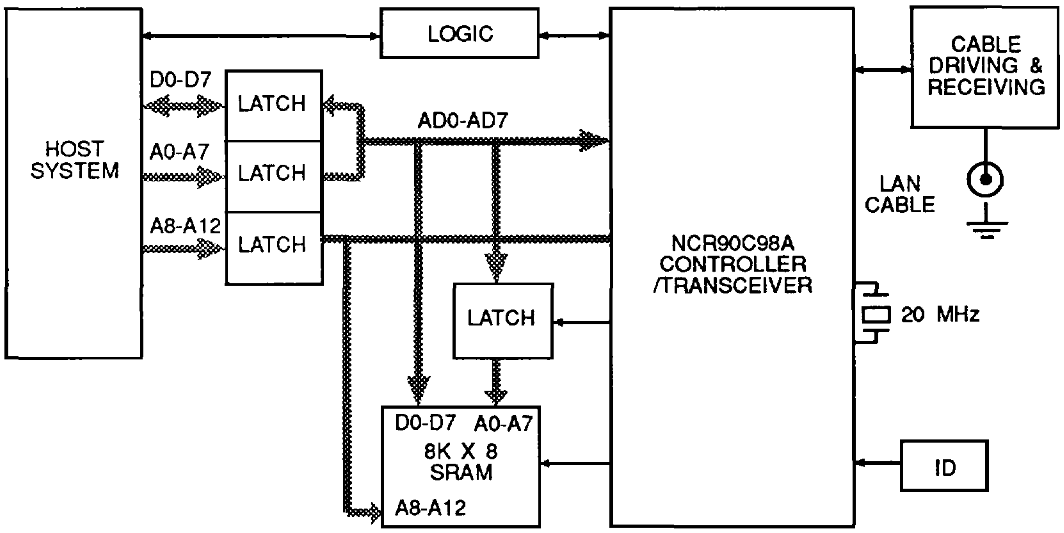


Figure 2 RIM Simplified Block Diagram

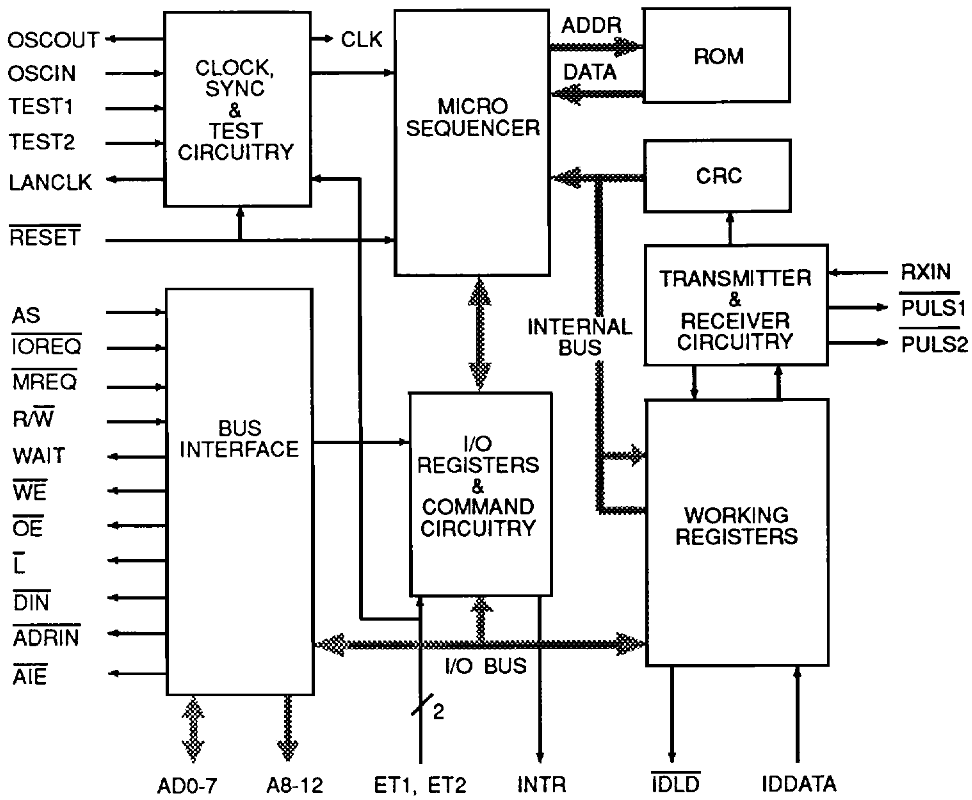


Figure 3 Chip block diagram

NEW FEATURES

The new features on the NCR90C98A make ARCNET interfaces easier to implement. The new features are:

- Buffer Chaining. Buffer Chaining lessens the overhead required by the host when receiving or transmitting multiple message packets. This increases throughput, especially in server applications.
- On-chip Power-On-Reset (POR) cell. The POR Cell reduces the number of external components required by putting all Power On Reset circuitry on-chip.
- On-chip Oscillator. The on-chip oscillator permits the replacement of the external crystal oscillator with a crystal.
- Reduces the wait states during host accesses. The arbitration circuitry services host access requests in half the time required by the NCR90C26.
- Increased Buffer Size. The NCR90C98A is now capable of supporting 8K of buffer RAM. This allows the system to support multiple transmit and receive buffers.
- Simplified Interface control Lines. The $\overline{\text{ADRIN}}$ and $\overline{\text{DIN}}$ signals simplify the circuitry for controlling Address and Data on the bus.

PINOUT DIFFERENCES BETWEEN THE NCR90C26 AND THE NCR90C98A

The Integration of the NCR90C26 and NCR90C32 into a single chip eliminated the following signals:

- CA
- TX
- DSYNC

In addition the following signals were eliminated because they now have little or no value to the system designer.

- DWR
- REQ
- CKSEL
- TTLCLK
- BLNK
- INHTX

The following new pins were added because of the on-chip oscillator and the expanded RAM buffer address space.

- OSCIN
- OSCOUT
- A11
- A12

The following signals have changed logically to accommodate non-multiplexed address and data bus.

- $\overline{\text{ADIE}}$ to $\overline{\text{ADRIN}}$
- $\overline{\text{ILE}}$ to $\overline{\text{DIN}}$

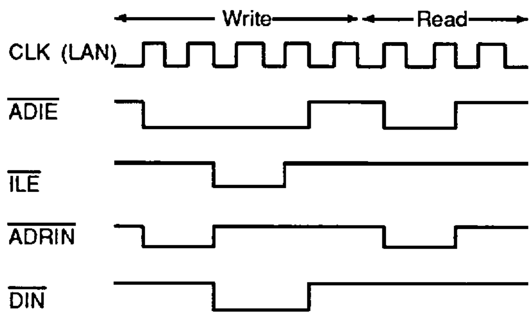


Figure 4

ARCNET OVERVIEW

LINE PROTOCOL

The NCR90C98A implements an asynchronous line protocol, with each Information Symbol Unit (ISU) consisting of the following:

- 2 clock units of mark (logic 1)
- 1 clock unit of space (logic 0)
- 8 clock units of data

A single clock unit is 400 nanoseconds in duration, so a byte of data is transmitted every 4.4 (400 ns x 11 clock units) microseconds. Thus, the time to transmit any message can be determined exactly. All transmissions start with an ALERT BURST, which is 6 clock units of mark. The line idles in a spacing condition. The five types of ARCNET transmissions follow:

Invitations To Transmit
: An ALERT BURST followed by three ISUs: one EOT (End of Transmission) and two repeated DID (Destination IDentification) ISUs. This message passes control (the "token") from one node to another

Free Buffer Enquiries
: An ALERT BURST followed by three ISUs: one ENQ (ENQuiry) and two repeated DID ISUs. This message asks another node if it is able to accept a message packet.

Packets
: An ALERT BURST followed by 8 to 516 ISUs:

- one SOH (Start Of Header) ISU
- one SID (Source IDentification) ISU
- two repeated DID ISUs
- two CRC (Cyclic Redundancy Check) ISUs
- one sytem code ISU
- from 0 to 507 data ISUs
- an inverse COUNT ISU = 256-N, for N data ISUs to be sent

Acknowledgments
: An ALERT BURST followed by a single ACK (ACKnowledgment) ISU. This message is used as a positive response to FREE BUFFER ENQUIRIES, and also to acknowledge the valid reception of a PACKET.

Negative Acknowledgments
: An ALERT BURST followed by a single NAK (Negative AcKnowledgment) ISU. This message gives a negative response to FREE BUFFER ENQUIRIES.

Line Protocol Notes:

- The codes (all in HEX) for the special ISUs mentioned above follow.
  - EOT - 04
  - ENQ - 85
  - SOH - 01
  - ACK - 86
  - NAK - 15
- The COUNT ISU for PACKETS may be equal to (512 - N) if a "long packet" is being sent. The CRC polynomial used for data packets is: $X^{16} + X^{15} + X^{2} + 1$.
- As a receiving node, the NCR90C98A will verify all incoming transmissions by checking for:
  - At least one mark and exactly one space preceding each byte.
  - A valid EOT, ENQ, SOH, ACK, or NAK following the ALERT BURST.
  - Proper CRC for data packets.
  - Correct number of bytes, depending on the transmission

NETWORK CONTROL

All nodes in an ARCNET system are distinguished by a unique 8 bit ID (IDentification) value. This value is configurable with DIP switches associated with each NCR90C98A chip. An ID of '0' may not be assigned to any node, since that ID indicates a BROADCAST to all nodes. Control of the Local Area Network (LAN) is based on token passing. In order to send a message a node must first receive the token. The token is received in an INVITATION TO TRANSMIT message containing its own ID. To send a message, the host processor loads the message data and the destination ID into its NCR90C98A's buffer RAM. Then the host writes an "Enable Transmit" command to the NCR90C98A. The NCR90C98A will know it has a message to send if the TA (Transmitter Available) bit in its Status Register is LOW. When the NCR90C98A has the token, it then transmits a FREE BUFFER ENQUIRY to the destination ID to see if it is able to receive the message. If the destination is able to receive, it transmits an ACK back to the controlling node. The controlling node then transmits the PACKET, complete with a 16-bit CRC. If there is no activity after sending this message, a "time out" (74.7 µs) occurs (see *Timecheck Function* Section). Upon Timeout, the NCR90C98A sets its TA bit, and passes the token. When an NCR90C98A receives the token, but its TA bit is high (it has no message to send), it sends an INVITATION TO TRANSMIT to pass the token.

When an NCR90C98A is sent a FREE BUFFER ENQUIRY, it will poll its RI (Receiver Inhibited) Status bit. If the RI bit is set, the NCR90C98A will transmit a NAK, and the controlling node will then pass the token. If an NCR90C98A with a packet to send gets a NAK, then it will pass the token and re-transmit a FREE BUFFER ENQUIRY the next time it receives the token. If there is no activity on the line within 74.7 µs of transmitting a FREE BUFFER ENQUIRY a time out occurs (see *Timecheck Function* Section). The NCR90C98A increments its NID (Next ID) pointer and tries again. After it has sent a PACKET, an NCR90C98A waits a specified response time. If within that time, it receives an ACK, it sets both the TMA (Transmit Message Acknowledged) and the TA Status bits and passes the token. If it does not receive an ACK in time, it only sets TA and then passes the token.

All nodes recognize a PACKET when they see the SOH ISU, and all NCR90C98As will write the SID into their Receive Buffers. If an NCR90C98A perceives the first DID as its own, or the PACKET is a Broadcast message (see the *Reconfiguration and Broadcast* section), the chip will write the second DID and the rest of the message into its Receive Buffer. Otherwise, the NCR90C98A will ignore the rest of the PACKET. After the PACKET has been fully received, it must pass three conditions to be considered a valid message:

- the CRC comparison
- correct length of ISUs, and
- valid DID in byte 0 of the Receive Buffer.

Valid DIDs are either '0' (indicating Broadcast), or the NCR90C98A's own ID. An ACK is sent if a message is valid by these conditions and addressed to the NCR90C98A's own ID. However if the message is a broadcast message no ACK will be sent. The NCR90C98A sets its RI status bit after receiving a valid message if no more receive buffers are available. In the buffer chaining mode, the Received Packet (RP) status bit is set when a valid message is received addressed to the NCR90C98A's own ID. If any of the conditions fail, the NCR90C98A ignores the message and will write over it with future PACKETS.

RECONFIGURATION AND BROADCAST

There are two activities that involve all nodes on the ARCNET system. These are Reconfiguration of the system and Broadcasts to the system.

A **Reconfiguration** of the network is performed any time a node is removed from, or added to the system. Specifically, an NCR90C98A will instigate a Reconfiguration when it is first powered on, or when it has not received an INVITATION TO TRANSMIT within 840 milliseconds. It does this by transmitting a RECONFIGURATION BURST: 8 marks and 1 space repeated 765 times. This burst has the effect of terminating all activity on the network. This burst is longer than all the other types of transmissions. Thus, it will interfere with the next INVITATION TO TRANSMIT, destroying the token and no other node will take control of the line. The RECONFIGURATION BURST also provides enough line activity so the NCR90C98A that just sent the token will also release control of the network.

When any NCR90C98A sees the line idle for 78 µs it begins a network reconfiguration cycle. It sets the internal NID (Next ID) register to its own ID. The NID is normally the DID sent with an INVITATION TO TRANSMIT. Besides resetting the NID, the NCR90C98A also starts a timeout of 146 µs times the quantity 255 minus its own ID

[146 μs x (255-ID #)]. If this timeout expires with no other line activity the NCR90C98A will start transmitting INVITATIONS TO TRANSMIT, with the DID pointing to itself. Only the NCR90C98A with the largest ID value will actually timeout.

After sending an INVITATION TO TRANSMIT, the NCR90C98A will look for any line activity, indicating that the DID is a valid node. If the sending NCR90C98A detects no activity after 74.7 μs, it increments its NID, and sends another INVITATION. Eventually, the NCR90C98A with the ID that is next, will see its ID in the INVITATION, and take control of the line. The previous NCR90C98A will then have its NID set correctly. The process repeats, with the end result that each NCR90C98A will have an NID stored representing an active node to pass the token. No time is wasted trying to send the token to nonexistent nodes. If a node is removed from an active network, then the previous node will time out when passing the token. The previous NCR90C98A goes through a cycle of incrementing its NID and transmitting INVITATIONS TO TRANSMIT until it finds the next valid node. The total time to perform a Reconfiguration will vary depending on the system configuration, but is typically between 24 and 61 ms.

A **Broadcast** Packet is the second operation that pertains to all the nodes in the network. A PACKET is considered to be Broadcast if the DID is a value of '0'. No regular node may be assigned the Broadcast ID. Nodes are set up to receive Broadcasts by issuing a "Write Configuration" command with the most significant bit of the command set to '1'. All the NCR90C98A commands are described in the *Command Register* sections.

TIMECHECK FUNCTIONS

A standard baseband system using RG-62 coax cable (the ARCNET standard) can take up to 31 μs for a one-way propagation. This corresponds to a distance of about 4 miles. The maximum turnaround time that any NCR90C98A takes to respond to an incoming message is 12 μs A maximum Response Time for any transmission is 31 + 31 + 12 = 74μs To allow a margin, the NCR90C98A uses 74.7 μs as its basic Response timeout. This is the interval a controlling node expects to perceive any line activity after it makes a transmission.

An IDLE Timeout is the interval that transpires at the onset of a Reconfiguration. After the RECONFIGURATION BURST, all the nodes commence the Reconfiguration process when they detect no line activity for the Idle timeout. In a standard network, the Idle timeout is 78.2 μs The TRANSFER timeout is the ID-dependent interval that is also associated with Reconfiguration. This timeout is given by 146 μs x (255-ID), and it transpires only for the node with the highest ID on the network. The last timeout is the interval that instigates a Reconfiguration. In a standard network, if any node has not received an INVITATION TO TRANSMIT within a Reconfiguration timeout of 840 ms, it issues a RECONFIGURATION BURST and starts a network Reconfiguration.

Table 1 Timeout Response and Reconfiguration Settings

ET2	ET1	Response Timeout	Reconfiguration Timeout
1	1	74.7 μs	0.84 seconds
1	0	283.4 μs	1.68 seconds
0	1	561.8 μs	1.68 seconds
0	0	1118.6 μs	1.68 seconds

The timeout values in Table 1 apply to a standard, or "basic" network with no 2 nodes farther apart than 4 miles. The network may operate over longer distances by appropriate setting of the ET1 and ET2 inputs. Table 1 shows the effect of ET1 and ET2 on two of the more pertinent timeouts. It is important that ET1 and ET2 be set to the same value for all nodes on the network.

HOST INTERFACE OVERVIEW

The host accesses the NCR90C98A and associated buffer RAM over a multiplexed address/data bus. 'D'-type latches provide the interface between the host's bus and the multiplexed address/data bus. The NCR90C98A controls the activity on this bus with arbitration logic. By controlling the multiplexed bus the NCR90C98A makes sure it has access to the buffer RAM for incoming data. See Figure 2.

The host controls the ARCNET node by reading and writing the I/O registers in the NCR90C98A. The host transfers all its message data with the buffer RAM. The NCR90C98A was designed to allow efficient data transfers between the host and the LAN. Buffer Chaining allows multiple packets to be transferred before service is required by the host. Simultaneous access to packet information in the buffer RAM is possible because of the arbitration logic on the NCR90C98A. A dual port RAM implementation using a standard RAM is accomplished by the RAM arbitration circuitry on the NCR90C98A. Since the host makes its access at arbitrary times, the NCR90C98A synchronizes the host by asserting WAIT at every access attempt by the host. In addition to passing messages, the host uses the Address-Data bus and latches to access the NCR90C98A directly. A low level on the $\overline{\text{IOREQ}}$ at the falling edge of AS identifies I/O cycles. These are used to read the NCR90C98A's status, or to write commands. A low level on the $\overline{\text{MREQ}}$ at the falling edge of AS identifies memory cycles. These are used to read or write the buffer RAM. See *HOST INTERFACE DESCRIPTION* section.

FUNCTIONAL DESCRIPTION

OPERATING MODES DESCRIPTION

The NCR90C98A supports two operating modes. The first is the NCR90C26 mode and the second is the NCR90C98 mode. In the NCR90C26 mode the chip is programmed the same as the NCR90C26. In the NCR90C98 mode all the features of the NCR90C98 are available.

The NCR90C98A powers-up in the NCR90C26 mode. The power-on routine within the NCR90C98A writes the NCR90C26 hex signature D1 to address 0 in the buffer memory. When the host CPU writes to Command Register 2, the NCR90C98A switches to the NCR90C98 mode. All bits in Command Register 1 take on the new functions of the NCR90C98 mode. The chip must be reset (Power-on, Reset Signal or Reset Command) to switch back to the NCR90C26 mode.

BUFFER CHAINING

This feature relieves the host from the task of enabling a new receive buffer for each packet received. It also lets the host transmit multiple packets per transmit command.

Packet Reception

In the receive buffer chaining mode, the NCR90C98A automatically fills all the pages that are assigned to the receive buffer. If the Circular mode is enabled, the NCR90C98A automatically restarts at the beginning of the receive buffer when the end has been reached. The NCR90C98A keeps track of available buffers and stops receiving when there are no more buffers available. The host must update the pointer that keeps track of the packets that have been read.

The pointers associated with the receive buffer are the Next Page to Receive (NPRX), Next Page to Read (NPRD) and Start of RX Buffer (SRXB). When a packet has been received successfully, the NCR90C98A increments the NPRX pointer and sets the RP bit which generates an interrupt. The host, after determining the source of the interrupt, reads the NPRX pointer which clears RP, reads the packet and then increments the NPRD pointer.

Packet Transmission

In the transmit buffer chaining mode the NCR90C98A transmits all the packets the host wrote into the transmit buffer. It is the responsibility of the host to update the pointer that points to the last packet to be transmitted. The NCR90C98A will keep track of which packets to send and when to stop. If the Circular mode has been enabled, the NCR90C98A automatically restarts at the beginning of the transmit buffer when the end has been reached.

The pointers associated with the transmit buffer are the Next Page to Write (NPWR), Next Page to Transmit (NPTX) and Start of TX Buffer (STXB). When the host wants to transmit a packet, it must write the packet into the page pointed to by the NPWR pointer. If the host wants to transmit multiple packets, it must write the packets into the subsequent pages. Then move the NPWR pointer to the page that follows the last written page. The NCR90C98A will start to transmit one packet per token when the enable transmit or enable chain transmit commands are executed. Upon a successful transmission the TA and TMA bit will be set.

See Figure 5 for a diagram depicting the relative function of each pointer. Following are brief descriptions of each pointer.

Next Page to Write (NPWR).

The NPWR pointer contains the page address (in the buffer RAM) for the host to write the next packet of data to be transmitted.

Next Page to Transmit (NPTX).

The NPTX pointer contains the page address for the next packet to be transmitted.

Start TX Buffer (STXB).

The STXB pointer contains the starting page address of the transmit buffer RAM. The transmit buffer memory ranges from this address to the end of memory.

Next Page to Receive (NPRX).
The NPRX pointer contains the page address of the next packet to be received.

Next Page to Read (NPRD).
The NPRD pointer contains the page address (in the buffer RAM) of the next packet to be read.

Start RX Buffer (SRXB).
The SRXB pointer contains the starting page address of the receive buffer RAM. The receive buffer memory ranges from this address up to the STXB page address.

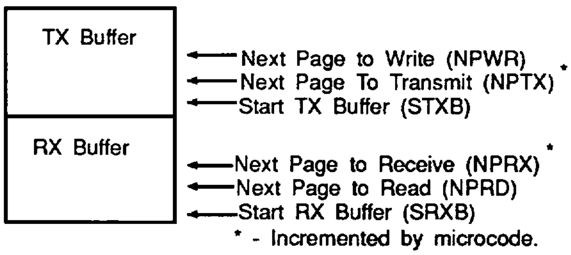


Figure 5 Buffer RAM Pointer Diagram

PIN DESCRIPTION

AD0-AD7: Address/Data Bus.
These pins serve as the multiplexed eight-bit address and data bus for the NCR90C98A.

During **host accesses with the** NCR90C98A, this bus carries the data and lower address bits. During host writes data is input to the NCR90C98A over this bus. During host reads the NCR90C98A outputs data over this bus. During the first part of these accesses the lower eight address bits are input to the NCR90C98A from this bus.

During **buffer RAM accesses by the** NCR90C98A, this bus carries the data and lower address bits. Data is output from the NCR90C98A during writes and input to the NCR90C98A during reads. The lower eight address bits are output from the NCR90C98A during the first part of both reads and writes.

During **buffer RAM accesses by the host, the** NCR90C98A keeps these lines at a high impedance state.

A8-A12: Page Select.
These outputs are the five most significant address bits to the buffer RAM. They supply the page address when the NCR90C98A accesses the RAM. These outputs are in the high impedance state when the NCR90C98A is not accessing the buffer RAM.

$\overline{\text{ADRIN}}$: Address Input Enable.
The NCR90C98A uses this signal to control the host's lower address lines. When the NCR90C98A drives this signal low the host's address bus latch drives the Address-Data bus. When driven high the lower address lines driving the Address-Data bus are assumed to be in a high impedance state.

$\overline{\text{AIE}}$: Address Input Enable.
The NCR90C98A uses this signal to control the host's upper address lines. When the NCR90C98A drives this signal low the host's upper address lines drive the RAM. When driven high the upper address lines to the buffer RAM are assumed to be in a high impedance state.

AS: Address Strobe.
On the falling edge of AS the NCR90C98A latches the state of R/$\overline{\text{W}}$, $\overline{\text{MREQ}}$, and $\overline{\text{IOREQ}}$. This initiates arbitration of the Address-Data bus.

$\overline{\text{DIN}}$: Data Input Enable.
The NCR90C98A uses this signal to control the host's data bus. When the NCR90C98A drives this signal low the host's data bus latch drives the Address-Data bus. When $\overline{\text{DIN}}$ is driven high the host's data bus latch is assumed to be in a high impedance state.

ET1, ET2: Extended Timeout Functions.
These signals are used to select the timeout durations of the NCR90C98A. This is primarily used in checking responses from the other nodes on the LAN. These pins should be tied high for normal operation. See Table 1.

IDDAT: ID Data In.
This input is used to serially shift the node ID into the NCR90C98A. Each bit of the data is latched into the NCR90C98A on the falling edge of LANCLK. The shift register is clocked by the rising edge of LANCLK. The ID data is shifted into the NCR90C98A MSB first, with a high level representing a logic 1. (See $\overline{\text{IDLD}}$).

$\overline{\text{IDLD}}$: ID Load.
This output is used to synchronously load the state of the ID switches into an external shift register. (See IDDAT).

INTR: Interrupt.
The NCR90C98A drives this signal high to indicate to the host that an enabled interrupt condition has occurred. INTR will return low after clearing the interrupt status condition or the corresponding mask bit.

$\overline{\text{IOREQ}}$: I/O Request.
This signal is sampled by the NCR90C98A on the falling edge of AS. When this signal goes low, it indicates that the host wishes to communicate with the NCR90C98A.

L: Latch.
The NCR90C98A uses this signal to control the lower address lines driving the RAM. When the NCR90C98A drives this signal low the lower address lines driving the RAM are latched until the RAM access is finished.

LANCLK: Network Clock.
A free running 5 MHz clock used for clocking the ID shift register.

$\overline{\text{MREQ}}$: Memory Request.
This signal is sampled by the NCR90C98A on the falling edge of AS. When low it indicates that the host wishes to transfer data with the buffer RAM.

$\overline{\text{OE}}$: Output Enable.
The NCR90C98A drives this control line low on all RAM read cycles, enabling the buffer RAM to output data over the Address-Data bus.

OSCIN, OSCOUT: Oscillator Input & Output.
This input and output pin connect an external 20 MHz crystal to the internal oscillator. The OSCIN pin may also be used to drive the NCR90C98A with an external clock. OSCOUT is left floating in this case.

$\overline{\text{RESET}}$: Reset.
This input pin when driven low resets the state of the NCR90C98A. Upon Power Up the internal power on reset cell will reset the chip. During reset the NCR90C98A sequence counter is set to zero and the Reset status bit is set to a 1. See Table 2.

$\overline{\text{PULS1}}$, $\overline{\text{PULS2}}$: Pulse 1 & Pulse 2.
These outputs are non-overlapping negative going pulses that drive the cable circuitry. The output signals correspond to the data being transmitted over the LAN from this node. Pulse1 is the first and Pulse2 is the second pulse in this dual-pulse process.

R/$\overline{\text{W}}$: Read/Write.
This input line indicates to the NCR90C98A that the pending host access request is either a read or a write cycle. R/$\overline{\text{W}}$ is sampled on the falling edge of AS.

RXIN: Receive Data In.
This input pin receives serial data from the LAN cable circuitry.

VDD: Power.
Connect this pin to +5 Volts.

VSS: Ground.
Connect this pin to ground.

WAIT: Wait.
This output signal is driven high by the NCR90C98A at the beginning of host access requests. It indicates that the bus arbitration has started. WAIT is returned low when the NCR90C98A is ready for the host to complete its access.

$\overline{\text{WE}}$: Write Enable.
The NCR90C98A drives this control line low on all RAM write cycles. This enables the buffer RAM to clock in data from the Address-Data bus. Data is clocked into the RAM on the rising edge of WE.

Table 2 NCR90C98A Reset State

Name	State
Registers and Pointers	**msb lsb**
Command Register 1	0 0 0 0 0 1 0 1
Command Register 2	0 0 0 0 0 1 0 1
Status Register 1*	1 x x 1 0 0 0 1
Status Register 2	x x x x x x 1 0
Interrupt Mask 1	0 0 0 0 0 0 0 0
Interrupt Mask 2	0 0 0 0 0 0 0 1
Next Page to Write (NPWR)	x x x 1 1 1 1 1
Next Page to Transmit (NPTX)	x x x 1 1 1 1 1
Start TX Buffer (STXB)	x x x 1 1 1 1 1
Next Page to Receive (NPRX)	x x x 0 0 0 0 0
Next Page to Read (NPRD)	x x x 0 0 0 0 0
Start RX Buffer (SRXB)	x x x 0 0 0 0 0
Output Pins	
ADO-AD7, A8-A12	High Impedance
Control Lines:	Inactive
$\overline{\text{ADRIN}}$, $\overline{\text{AIE}}$, $\overline{\text{DIN}}$, $\overline{\text{L}}$, $\overline{\text{IDLD}}$	1 (high)
$\overline{\text{WE}}$, $\overline{\text{OE}}$, INTR	1 (high)
WAIT,	0 (low)
$\overline{\text{PULS1}}$, $\overline{\text{PULS2}}$	Inactive (high)

*In Status Register 1, bits 5 & 6 reflect the state of the ETS1 & ETS2 pins.

REGISTER DESCRIPTIONS

The registers of the NCR90C98A occupy six addresses in a Memory or I/O Map. The host system has access to eight registers which are:

- Command Registers 1 & 2,
- Interrupt Mask Registers 1 & 2,
- Status Registers 1 & 2,
- NPRX Pointer Register,
- NPTX Pointer Register, and the
- $\overline{\text{RESET}}$ Command Register.

The registers are decoded with the AD0-AD3 signals and the R/$\overline{\text{W}}$ line on the falling edge of AS. See Table 3.

Table 3 Register Addresses

AD 3 2 1 0	WRITE	READ
0 0 0 0	Interrupt Mask 1	Status Register 1
0 0 0 1	Command Reg. 1	Reserved
0 0 1 0	Command Reg. 2	NPRX Pointer
0 0 1 1	Reserved	NPTX Pointer
0 1 0 0	Interrupt Mask 2	Status Register 2
1 0 0 0	Reset Chip	Reserved

Command Registers Description

NCR90C26 Mode In the NCR90C26 mode, only Command Register 1 is valid. Command Register 1 is a write-only register accessed by writing to address 1. The commands recognized by Command Register 1 are described below.

Command Register 1

Data (msb lsb)	Function
0 0 0 0 0 0 0 1	Disable Transmitter: Causes the NCR90C98A to cancel any pending transmit command. This command will cause the TA bit to be set the next time the NCR90C98A receives the token.
0 0 0 0 0 0 1 0	Disable Receiver: Causes a pending receive command to be canceled. This command causes the RI bit to be set the next time the NCR90C98A receives the token. If a PACKET has already started arriving, then this command has no effect.
0 0 0 n n 0 1 1	Enable Transmit from Page nn: Tells the NCR90C98A to prepare for a transmit operation out of RAM buffer page nn when it next receives the token. The TA and TMA bits are reset by the NCR90C98A receiving this command. The TA bit is set to logic '1' at completion of the transmission; the TMA bit may already be set at that time if the destination node has sent back an acknowledgment. If TA is not true, this command should not be issued.
b 0 0 n n 1 0 0	Enable Receive to Page nn: Allows the NCR90C98A to receive messages into RAM buffer page nn. The RI bit is set to '0' by this command. If 'b' in the command is '0', then only messages addressed to the NCR90C98A's ID are received. If 'b' is '1', then Broadcast messages are also accepted. RI is set by a successful message reception.
0 0 0 0 s 1 0 1	Buffer Size: Tells NCR90C98A the size of its RAM buffer. If bit 's' is '0', the buffer is 1K bytes, and only short packets are sent and received. If 's' is '1', the buffer is 2K bytes and both short and long packets are handled.
0 0 0 r p 1 1 0	Clear Flags: Resets the POR and/or the RECON status bits depending on the variable bits. If 'r' is '1', the RECON flag is cleared, and if 'p' is '1', then POR is cleared.

NCR90C98 Mode Command Registers 1 & 2 are write-only registers accessed by writing to addresses 01 or 02 respectively. Eight-bit commands are written to transfer control information to the NCR90C98A. The commands recognized by Command Registers 1 & 2 are described below.

Command Register 1

Data (msb … lsb)	Function
0 0 0 0 0 0 0 1	Disable Transmitter: Causes the NCR90C98A to cancel any pending transmit command. The TA bit is set the next time the NCR90C98A receives the token.
0 0 0 0 0 0 1 0	Disable Receiver: Causes a pending receive command to be cancelled. This command causes the RI bit to be set the next time the NCR90C98A receives the token. If a PACKET has already started to arrive, then this command will have no effect.
n n n n n 0 1 1	Enable Transmit from page nnnnn: Transmit a packet out of buffer RAM nnnnn upon receipt of the token. This command clears TA and TMA. The TA bit is set to a logic '1' at the completion of the transmission. TMA is set to a logic '1' when an ACK is received from the destination node.
n n n n n 1 0 0	Enable Receive to page nnnnn: Allows the NCR90C98A to receive packets into buffer RAM starting at page nnnnn. This command sets the pointers SRXB, NPRD and NPRX to nnnnn and clear the RI bit. RI is set when no more buffers are available.
p 0 0 s s 1 0 1	Size Definition: Tells the NCR90C98A the size of its buffer RAM and whether it can receive long or short packets.

ss	RAM	p	Packet
00	1K	0	256 bytes
01	2K	1	512 bytes
10	4K		
11	8K		

Data (msb … lsb)	Function
0 0 0 r p 1 1 0	Clear Flags: Resets the RECON status bit if r=1 and/or the Reset status bits if p=1.

Command Register 2

Data (msb … lsb)	Function
n n n n n 0 0 1	Write Next Page to Write Pointer (NPWR): Initializes the NPWR pointer to page nnnnn.
n n n n n 0 1 0	Write Next Page to Read (NPRD) pointer: Initializes the NPRD pointer to page nnnnn.
n n n n n 0 1 1	Initialize Transmit pointers: Initializes Next Page to Transmit (NPTX), Next Page to Write (NPWR) and Start Transmit Buffer (STXB) pointers to page nnnnn.
0 0 0 0 0 1 0 0	Enable Chain Transmit: Tells the NCR90C98A to start transmitting from the page pointed to by the NPTX pointer. It stops when the NPTX pointer has reached the NPWR pointer. This command clears TA and TMA. The TA bit is set to a logic '1' at the completion of the transmission. TMA is set to a logic '1' when an ACK is received from the destination node.
b r c 0 0 1 0 1	Write Configuration: Tells the NCR90C98A what mode it is in. When b=1, broadcast messages will be accepted. When r=1, chain receive is enabled. When c=1, circular buffer chaining is enabled.

Status Register Description

Status Registers 1 & 2 are read-only registers that allow the host to monitor the status of the LAN. Status Register 1 is read from address 00 and Status Register 2 is read from address 04. In the NCR90C26 mode, only Status Register 1 is used.

Status Register 1

7	6	5	4	3	2	1	0
RI	ETS2	ETS1	Reset	TEST	RECON	TMA	TA

Bits	Name	Description
0	TA	Transmitter Available: When TA is set to a '1' the node is available to carry out a transmit sequence. It also indicates that any previous ENABLE TRANSMIT process has been completed. TA is cleared by the Enable Transmit and Enable Chain Transmit commands. TA is set after packet(s) have been transmitted and ACK'ed. TA is also set if there is no ACK and the node has timed out.
1	TMA	Transmit Message Acknowledged: When TMA is set to a '1' the message sent from a previous ENABLE TRANSMIT command was acknowledged by the receiving node. TMA is cleared by the Enable Transmit and Enable Chain Transmit commands. TMA is set after packet(s) have been transmitted and ACK'ed by the receiving node.
2	RECON	Reconfiguration Flag: When RECON is set to a '1' a system Reconfiguration took place due to the expiration of an Idle timeout. RECON is reset by the CLEAR FLAGS command.
3	TEST	This bit is used for test and diagnostic purposes. Under normal operating conditions this bit is set to a '0'.
4	Reset	Reset: When the Reset bit is set to a '1' the NCR90C98A has experienced a reset from one of three sources. The reset could come from 1. an active signal on the $\overline{\text{RESET}}$ input, 2. the power-on cell has been triggered by the application of power, or 3. the Reset command has been executed. The Reset status bit is cleared by the Clear Flags command.
5-6	ETS1, ETS2	Extended Timeout Status 1 & 2: The state ETS2 of these bits reflects the logic level on the ETS1 & ETS2 pins. Under normal operating conditions ETS1 & ETS2 will be '1'.
7	RI	Receiver Inhibited: When RI is set to a '1' the NCR90C98A is not receiving any messages from other nodes. RI is cleared by the Enable Receive command and when a buffer has been made available in the Buffer Chain mode. RI is set when a packet has been received or when there are no more buffers available in the Buffer Chain mode.

Status Register 2 (NCR90C98 Mode Only)

7	6	5	4	3	2	1	0
X	X	X	X	X	X	CD	RP

Bits	Name	Description
0	RP	Received Packet: When RP is set to a '1' a packet has been received in the Buffer Chain mode. RP is cleared by the read NPRX command.
1	CD	Carrier Detect: When CD is set to a '1' the NCR90C98A is detecting activity on the RXIN pin. CD is cleared when the NCR90C98A transmit/receive mode is enabled.
2-7		Reserved.

Interrupt Mask Registers

The Interrupt Mask Registers are write-only registers that determine which of the five maskable conditions will cause an interrupt. (See *HOST INTERRUPTS* section for details).

Next Page to Receive (NPRX) Pointer Register

The Next Page to Receive (NPRX) pointer is read from address 02. The format of the data with the register follows.

X X X A12 A11 A10 A9 A8 - Read NPRX pointer. By executing this read the RP bit will be reset.

Next Page to Transmit Pointer Register

The Next Page to Transmit Pointer is read from address 03. The format of the data with the register follows.

X X X A12 A11 A10 A9 A8 - Read NPTX pointer.

Reset Register Description

When the following value is written to this register at address 08 the NCR90C98A is reset. This provides the host a means for resetting the NCR90C98A from software.

0 0 0 0 0 0 0 1 - RESET. Resets the NCR90C98A.

RESET OPTIONS

There are three reset options for the NCR90C98A. When power is applied to the chip, the POR cell senses this and generates an internal signal to reset the chip. Another option resets the chip when a low signal is applied to the Reset pin for a minimum of 200 ns. It is also possible to reset the chip by writing a reset command to I/O location 08.

The NCR90C98A executes a reset routine that writes D1H to address 0 and writes the node ID to address 1 in buffer RAM.

NCR90C98 MODE SOFTWARE CONSIDERATIONS

The standard method for the host to transmit a packet(s) of information in the buffer chaining mode follows.

1. Initialize transmit pointers.
2. Write the packet(s) to the page.
3. Write the NPWR pointer.
4. Write Enable Chain Transmit.
5. When NPWR=NPTX TA & TMA is set as described in the Status Register Description.
6. If more packets are ready to go, repeat step 3,4.
7. If not, repeat steps 2, 3, and 4.

The standard method for the host to Receive a packet(s) of information in the buffer chaining mode follows.

1. Write Enable Receive.
2. When the RP interrupt occurs, read the NPRX pointer. This resets the RP flag.
3. Read the packet(s). Write the NPRD pointer.
4. If NPRX indicated missed interrupts, repeat step 3.
5. If not, go back to step 2.

When any register with reserved bits is read, the state of the reserved bits will be a '1'.

The buffer memory can be reconfigured at any time. However, the receiver and transmitter must be disabled and all packets read/transmitted to insure that no packets are lost.

HOST INTERRUPTS

The NCR90C98A generates an interrupt on the INTR pin in response to several of the conditions that set status bits. The Interrupt Mask Registers determine which of the five conditions will cause an interrupt. The status bits TMA, ETS1, ETS2 and CD have no corresponding mask bits and do not cause interrupts. The five maskable status bits are outlined in the following diagram.

Interrupt Mask Register 1

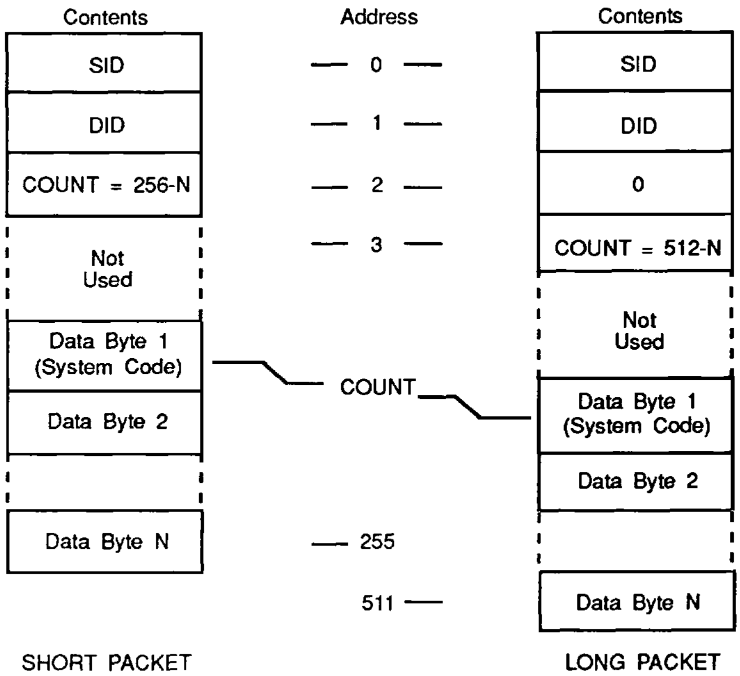
7	3	2	0
RECEIVE INHIBIT	TEST	RECON TIMEOUT	TRANSMITTER AVAILABLE

Interrupt Mask Register 2

	0
	RECEIVED PACKET

Setting any of these bits to a "1" will enable the INTR signal to be asserted high when the corresponding status bits go high. The unused bits in the Interrupt Mask register must be written to a zero. Once the INTR signal is high, it can be cleared by clearing the corresponding bit in the Status Register or the Mask Register. RP is cleared by reading the NPRX pointer.

Reset generates a non-maskable interrupt. It is cleared by the Clear Flags Command.



NOTE: Addresses shown are relative to a Page, not absolute. SID = Source ID (not written in Transmit Packets). DID = Destination ID (set = 0 for Broadcasts). N = Message Length. "Not Used" bytes imply message is less than maximum length. These bytes would be written for Max. Messages: SHORT = 253 bytes, LONG = 508.

Figure 6 RAM Buffer Map

RAM BUFFER MEMORY MAP

Figure 6 shows the locations of the major components for both Short (up to 256 bytes) and Long (up to 512 bytes) PACKETS.

HOST INTERFACE DESCRIPTION

The Typical System Block Diagram (Figure 7) illustrates the hardware aspects of a host processor interface to the NCR90C98A. The block on the left contains the signals of a generic processor with an eight-bit data bus and a 16-bit address bus. The upper address bits are used to decode whether a pending host access is to/from the buffer RAM ($\overline{\text{MREQ}}$), or the NCR90C98A ($\overline{\text{IOREQ}}$). The buffer RAM in Figure 7, an 8K x 8 Static RAM, can hold 16 pages with 512 bytes per page or 32 pages with 256 bytes per page. Entire PACKETS are stored in a page in the buffer RAM. A 512 byte page corresponds to a Long Packet and a 256 byte page to a Short Packet. The 'D' Latches with the output control signal (OC) driven by $\overline{\text{AIE}}$, latch the Host's Upper Address Bus (A8-A15) signals for buffer RAM accesses by the host. The 'D' Latches with OC driven by L, latch the lower address bus for buffer RAM accesses, by both the NCR90C98A and the host. For host access cycles (read and write) to the NCR90C98A or to the buffer RAM, the latches with OC driven by $\overline{\text{ADRIN}}$, latch the incoming lower addresses (A0-A7) from the host system. For host access write cycles to the NCR90C98A or to the buffer RAM, the latches with OC driven by $\overline{\text{DIN}}$, latch the data (D0-D7) from the host system. For host access read cycles to the NCR90C98A or to the buffer RAM, the latches with OC driven by RD, latch the data (D0-D7) from the NCR90C98A or buffer RAM. A typical device for these latches is the '373.

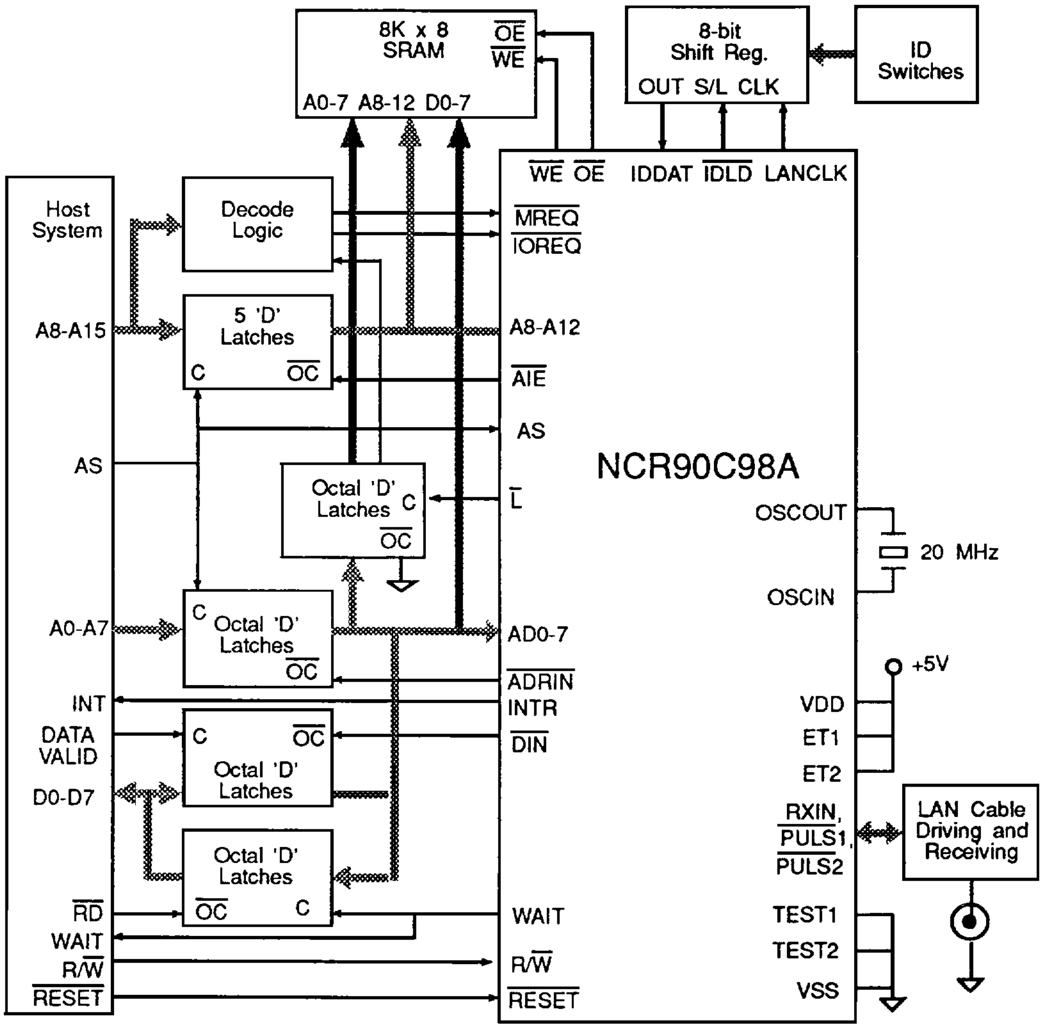
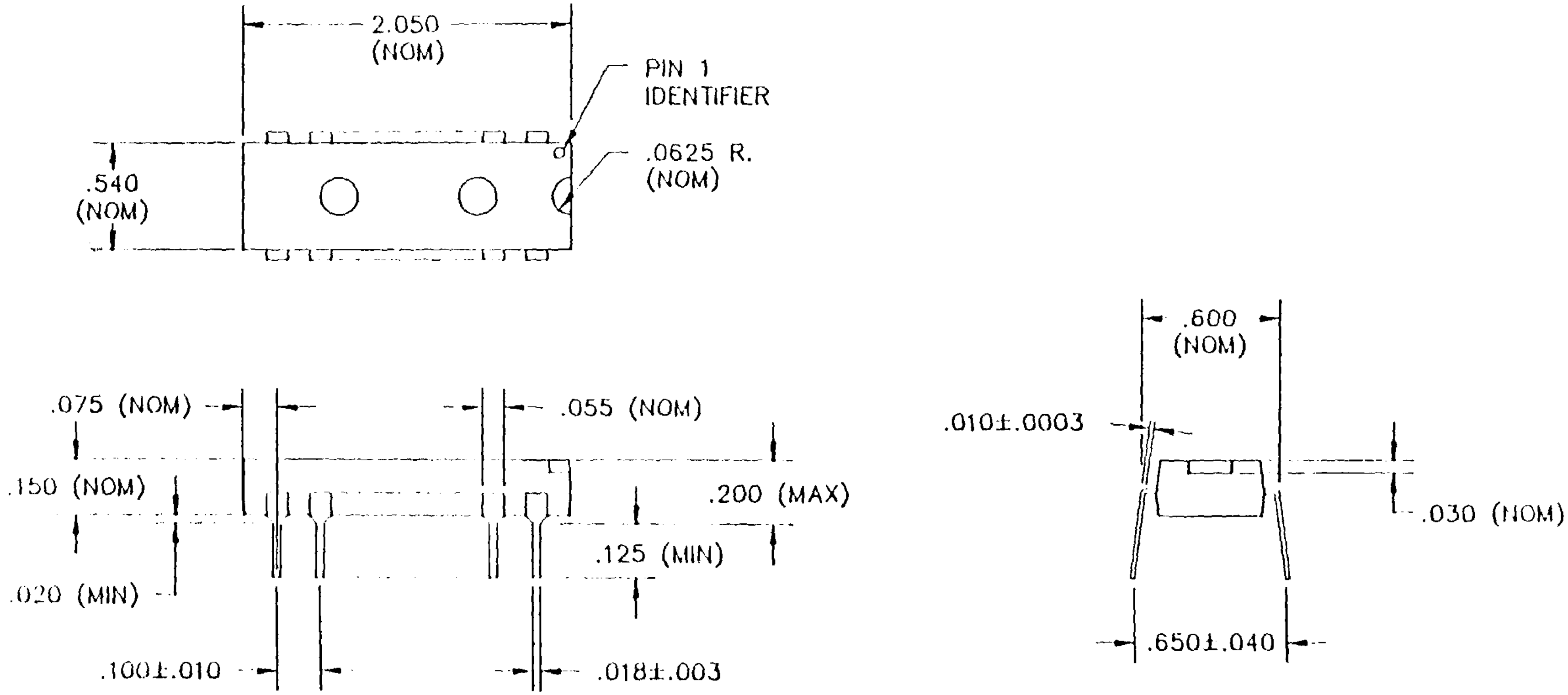
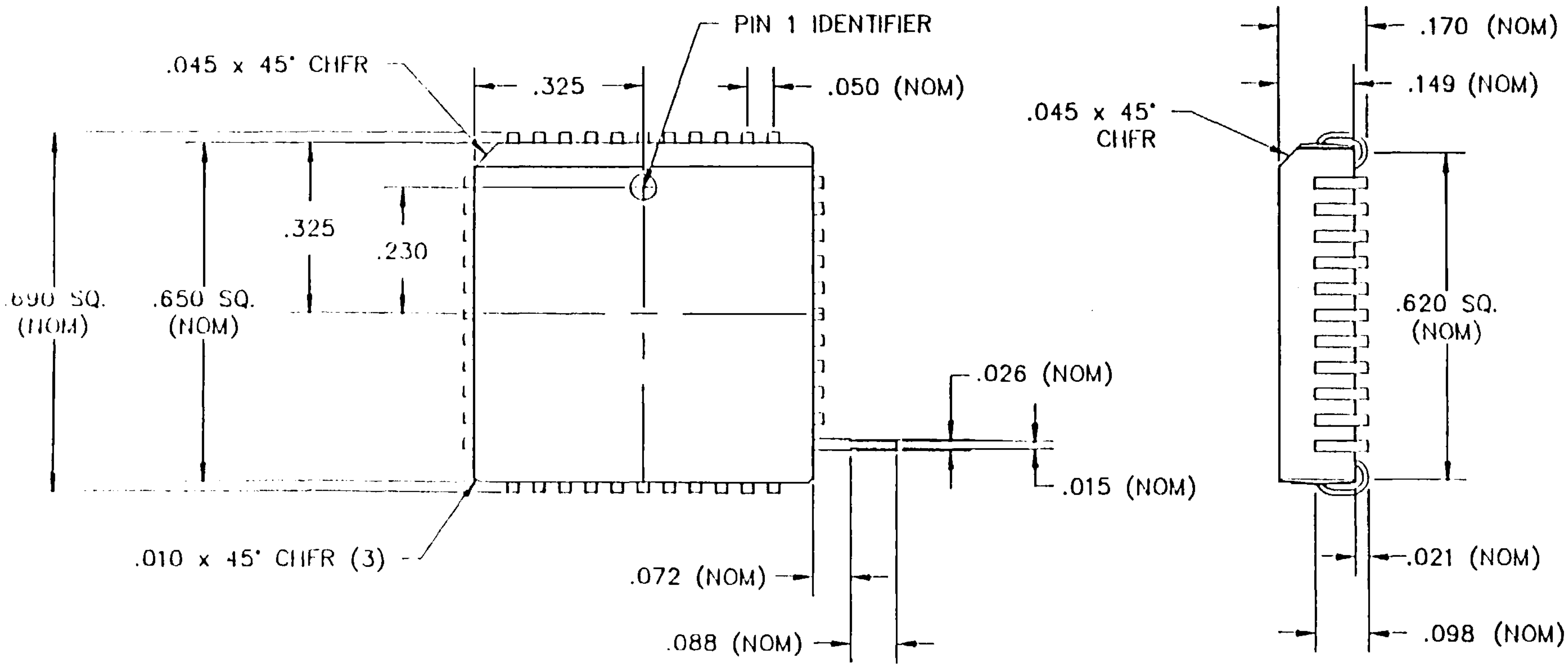


Figure 7 Typical system block diagram



NOTE : All dimensions
are in inches.

40 LEAD PLASTIC
DIP PACKAGE



NOTE : All dimensions
are in inches.

44 LEAD PLCC
PACKAGE

ORDERING INFORMATION

The NCR90C98A is available in two different package types, the 40-pin Dual Inline Package (DIP) and the 44-pin Plastic Leaded Chip Carrier (PLCC). The following part numbers should be used to order the desired package.

Package Type	Part Number
40-pin DIP	NCR90C98APD
44-pin PLCC	NCR90C98APP

ELECTRICAL SPECIFICATIONS

Absolute Maximums

Symbol	Parameter	Minimum	Maximum	Units
T_A	Ambient Temperature	0	70	°C
T_S	Storage Temperature	-55	150	°C
V_{DD}	Supply Voltage	-0.5	7.0	Volts
V_{IN}	Input Voltage	-0.5	V_{DD} + 0.5	Volts
V_{OUT}	Output Voltage,	-0.5	V_{DD} + 0.5	Volts
T_L	Lead Temperature (Soldering 10 seconds max)	-	250	°C

DC Characteristics (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A =0°C to 70°C.)

Symbol	Parameter	Minimum	Maximum	Units
V_{IL}	Input Voltage, Low	V_{SS} - 0.5	0.8	Volts
V_{IH}	Input Voltage, High	2.0	V_{DD}	Volts
V_{IH} CLK	Clock Input High Voltage (OSCIN pin)	3.85	V_{DD}	Volts
V_{IL} CLK	Clock Input Low Voltage (OSCIN pin)	V_{SS}	1.35	Volts
V_{OH}	Output Voltage, High (I_{OH} = -2mA, V_{DD} = 4.5V) (except AD0-7)	2.4		Volts
V_{OL}	Output Voltage, Low (I_{OL} = 4mA) (except AD0-7)		0.4	Volts
V_{OH} AD	Output Voltage, High for AD0-7 (I_{OH} = -1mA)	2.4		Volts
V_{OL} AD	Output Voltage, Low for AD0-7 (I_{OL} = 2mA)		0.4	Volts
C_{IN}	Input Capacitance		10	pF
I_I	Input Leakage Current		± 10	µA
I_{DD}	Power Supply Current (V_{DD} = 5.5V)		30	mA

AC Characteristics (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C.)

#	Description	Min	Typ	Max	Units	Comments
1	AS pulse width	25			ns	
2	Period of AS	900			ns	incl. bus arbitration
3	Control valid before AS low	25			ns	
4	Control valid after AS low	25			ns	
5	AS low to WAIT high	5		30	ns	
6	Processor cycle delay	100		650	ns	
7	$\overline{\text{ADRIN}}$ to WAIT low	230		270	ns	
8	$\overline{\text{ADRIN}}$ pulse width	90		110	ns	
9	Delay from $\overline{\text{ADRIN}}$ to $\overline{\text{L}}$	45		55	ns	
10	Delay from WAIT to $\overline{\text{AIE}}$	45		65	ns	
11	L pulse width	225		275	ns	
12	Delay $\overline{\text{ADRIN}}$ to $\overline{\text{DIN}}$	100		140	ns	
13	Delay $\overline{\text{WE}}$ to $\overline{\text{AIE}}$	45		60	ns	
14	$\overline{\text{WE}}$ hold to $\overline{\text{DIN}}$	50		80	ns	
15	Delay $\overline{\text{ADRIN}}$ to $\overline{\text{WE}}$	90		110	ns	
16	$\overline{\text{WE}}$ pulse width	130		165	ns	
17	Delay $\overline{\text{ADRIN}}$ to $\overline{\text{OE}}$	135		180	ns	

AC Characteristics (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C.)

#	Description	Min	Typ	Max	Units	Comments
18	$\overline{OE}$ hold after WAIT	50		80	ns	
19	$\overline{DIN}$ low to WAIT low	110		155	ns	
20	Delay WAIT to $\overline{DIN}$	50		85	ns	
21	$\overline{ADRIN}$ delay to valid data			60	ns	
22	Data setup before WAIT (write)	25			ns	
23	Data setup before WAIT (read)	50			ns	
24	Data hold after WAIT	45			ns	
25	Data valid to $\overline{L}$	70			ns	
26	$\overline{L}$ to data invalid	45			ns	
27	Data setup before $\overline{WE}$	115			ns	
28	Data hold after $\overline{WE}$	90			ns	
29	$\overline{L}$ turnoff delay from LANCLK high	50		80	ns	
30	ADD valid to $\overline{L}$	85			ns	
31	ADD hold from $\overline{L}$	45			ns	
32	RAM data hold for AC	50			ns	
33	Addr./Data bus Hi-Z before $\overline{OE}$	0			ns	
34	RAM data delay after $\overline{OE}$	0		140	ns	
35	Address valid before data	300			ns	
36	$\overline{IDLD}$ valid from LANCLK	0		120	ns	
37	IDDAT valid from LANCLK	0		50	ns	
38	LANCLK pulse high	95			ns	
39	LANCLK pulse low	95			ns	
40	LANCLK period	190	200	210	ns	
41	RXIN Pulse Width	10			ns	
42	Period of one bit		400		ns	

Oscillator/Crystal Specifications (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

Parameter	Min	Typ	Max
XTAL			
Motional Resistance			25 Ω
Frequency		20 MHz	
External Clock			
Duty Cycle	40%		60%

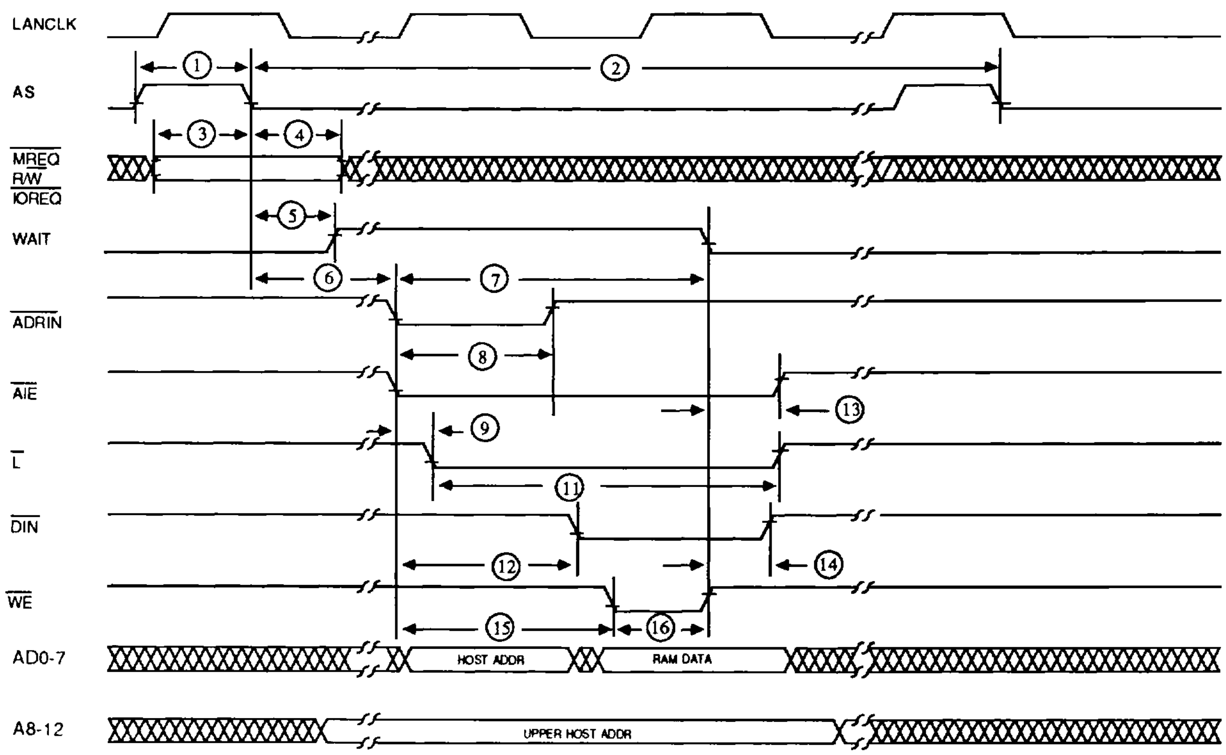


Figure 13 Write RAM by Host Timing Diagram

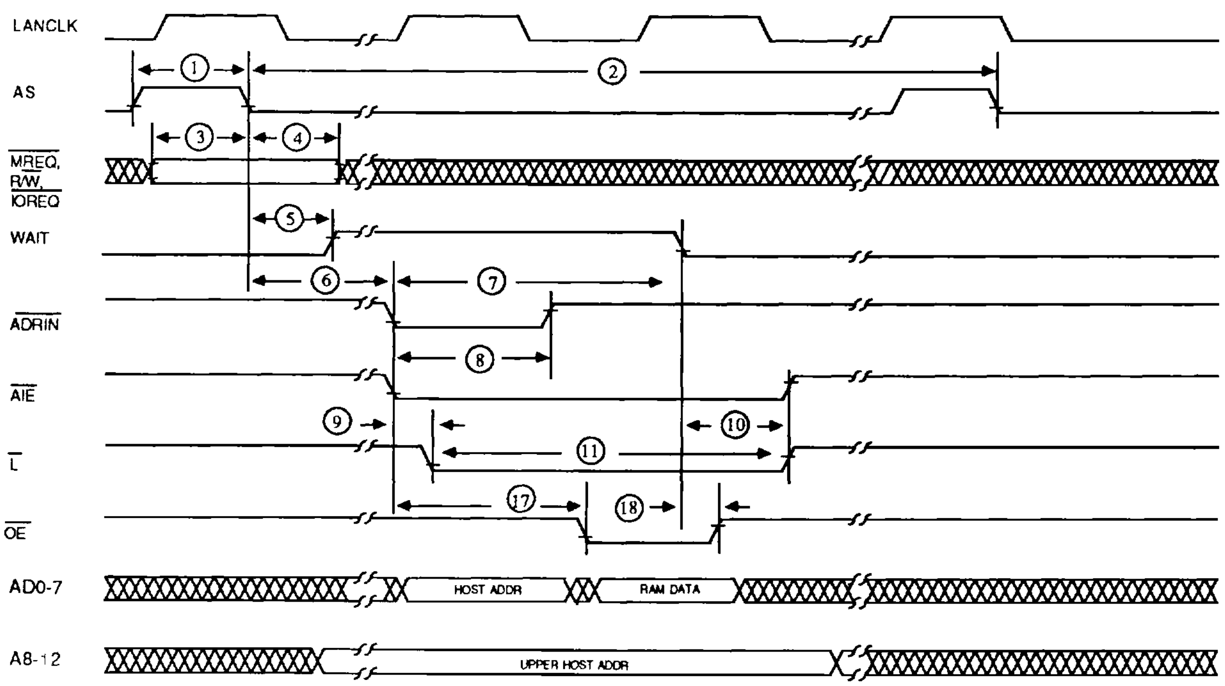


Figure 14 Read RAM by Host Timing Diagram

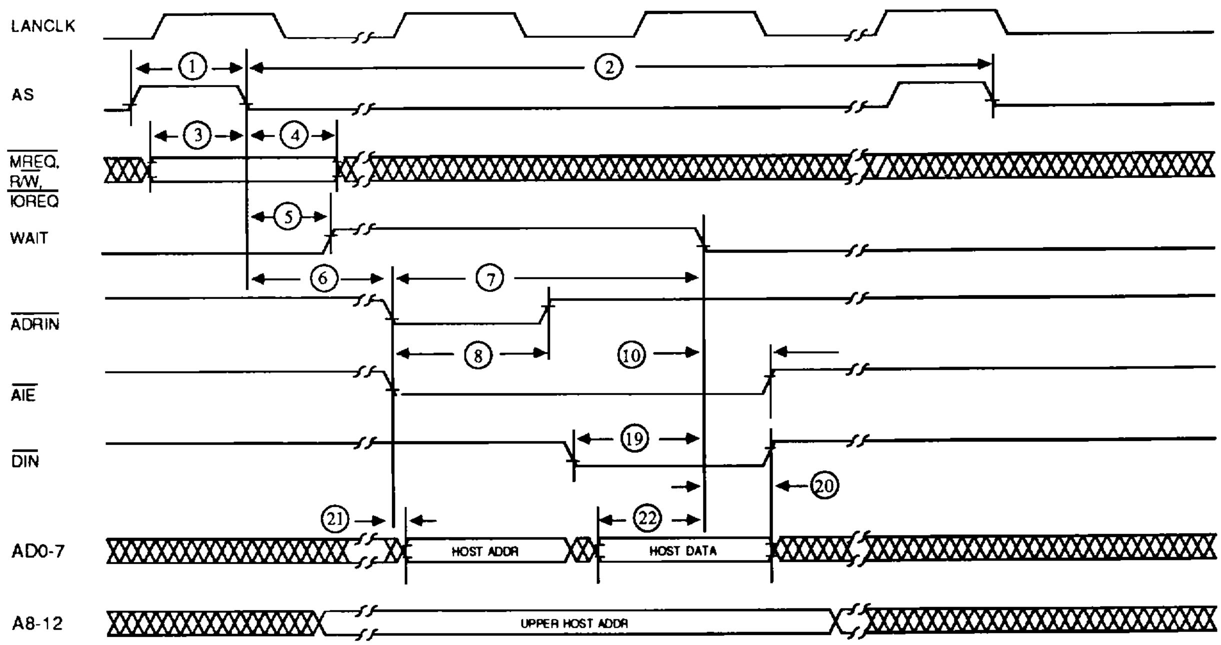


Figure 15 Write NCR90C98A by Host Timing Diagram

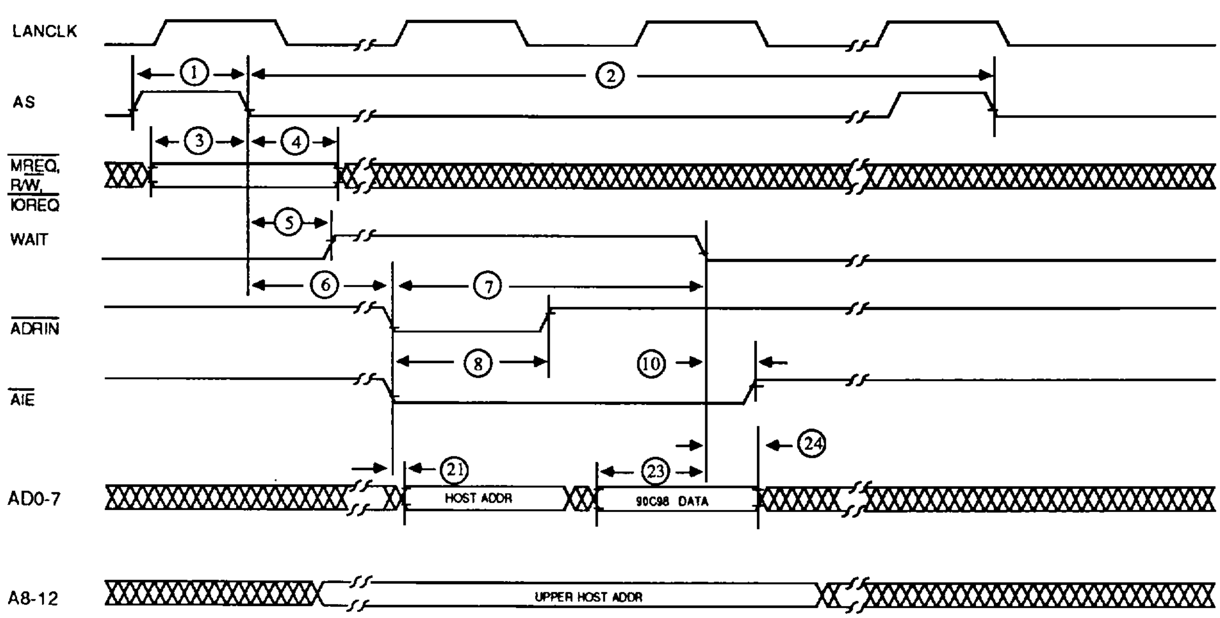


Figure 16 Read NCR90C98A by Host Timing Diagram

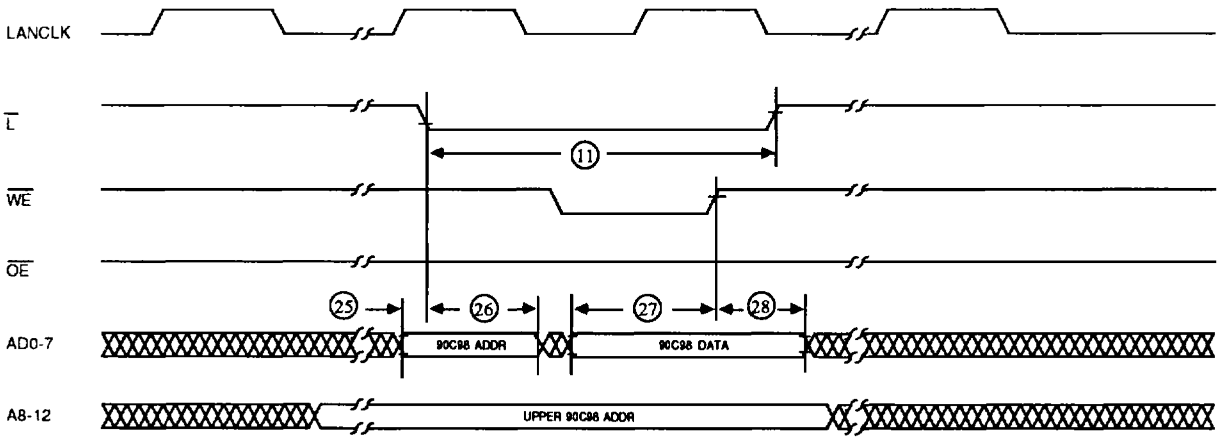


Figure 17 Write RAM by NCR90C98A Timing Diagram

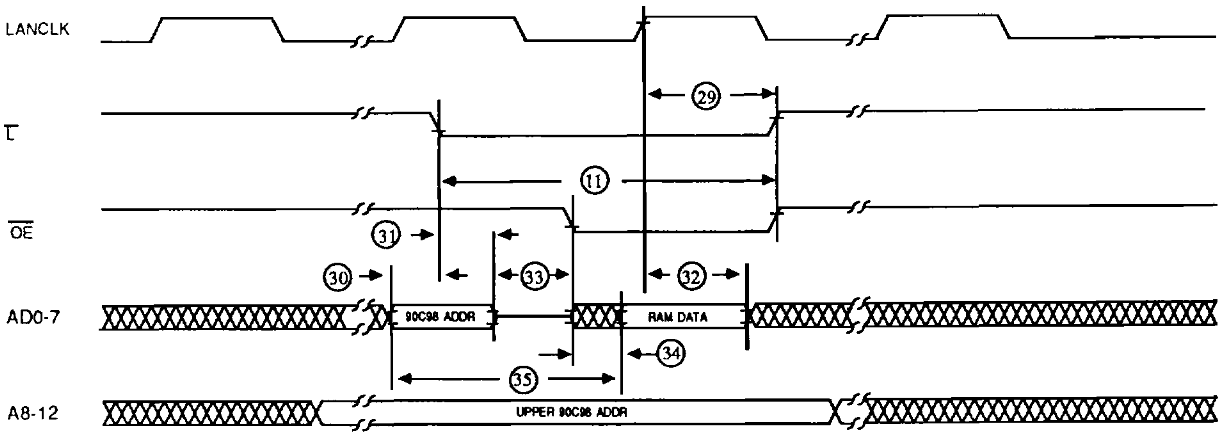


Figure 18 Read RAM by NCR90C98A Timing Diagram

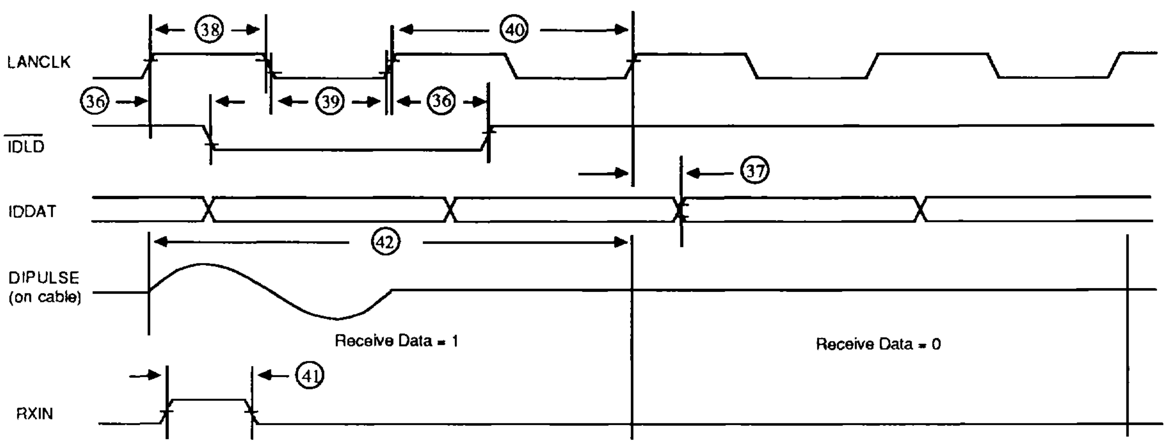


Figure 19 Clock, ID Signal, and Receive Timing Diagram

SALES INFORMATION

For more information on the NCR90C98A, or any other Communications Group device, please call the NCR hotline at

1 - 800 - 334 - 5454

or contact your local NCR Sales Representative or one of the following NCR Sales Offices.

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