



STANDARD
MICROSYSTEMS
CORPORATION

COM90C66
Data Sheet with Erratas for
Rev. B and Rev. D devices

ARCNET[®] Controller/Transceiver with AT[®] Interface and On-Chip RAM

FEATURES

- ARCNET LAN Controller/Transceiver/Support Logic/Dual-Port RAM
- Integrates SMSC COM90C65 with 16-Bit Data Bus, Dual-Port RAM, and Enhanced Diagnostics Circuitry
- Includes IBM[®] PC/AT[®] Bus Interface Circuitry
- Supports 8- and 16-Bit Data Buses
- Full 2K x 8 On-Chip Dual-Port Buffer RAM
- Zero Wait State Arbitration for Most AT Buses
- SMSC COM90C26 Software Compatible
- Command Chaining Enhances Performance
- Supports Memory Mapped and Sequential I/O Mapped Access to the Internal RAM Buffer
- Compatible with the SMSC HYC9058/68/ 88 (COAX and Twisted Pair Drivers)
- Token Passing Protocol with Self Reconfiguration Detection
- Variable Data Length Packets
- 16 Bits CRC Check/Generation
- Includes Address Decoding Circuitry for On-Chip RAM, PROM and I/O
- Supports up to 255 Nodes
- Contains Software Accessible Node ID Register
- Compatible with Various Topologies (Star, Tree, Bus, ...)
- On-Board Crystal Oscillator and Reset Circuitry
- Low Power CMOS, Single +5V Supply

GENERAL DESCRIPTION

The SMSC COM90C66 is a special purpose communications controller for interconnecting processors and intelligent peripherals using the ARCNET Local Area Network. The COM90C66 is unique in that it integrates the core ARCNET logic found in Standard Microsystems' original COM90C26 and COM90C32 with an on-chip 2K x 8 RAM, as well as the 16-bit data bus interface for the IBM PC/AT. Because of the inclusion of the RAM buffer in the COM90C66, a complete ARCNET node can be implemented with only one or two additional ICs (8- or 16-bit applications, respectively) and a media driver circuit. The ARCNET core remains functionally untouched, eliminating validation and compatibility concerns. The enhancements exist in the integration and the performance of the

device. Maximum integration has been achieved by including the 2K x 8 RAM buffer on the chip, providing the immediate benefits of a lower device pin count and less board components. The performance is enhanced in four ways: a 16-bit data bus for operation with the IBM PC/AT; a zero wait state arbitration mechanism, due partly to the integration of the RAM buffer on-chip; the ability of the device to do consecutive transmissions and receptions via the Command Chaining operation; and improved diagnostics, allowing the user to control the system more efficiently. For most AT compatibles, the device handles zero wait state transfers.

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TABLE OF CONTENTS

FEATURES	1
GENERAL DESCRIPTION	1
PIN CONFIGURATION	3
DESCRIPTION OF PIN FUNCTIONS	4
PROTOCOL DESCRIPTION	9
NETWORK PROTOCOL	9
NETWORK RECONFIGURATION	9
BROADCAST MESSAGES	10
EXTENDED TIMEOUT FUNCTION	10
LINE PROTOCOL	10
SYSTEM DESCRIPTION	12
MICROPROCESSOR INTERFACE	12
TRANSMISSION MEDIA INTERFACE	13
FUNCTIONAL DESCRIPTION	13
MICROSEQUENCER	13
ADDRESS DECODING	19
INTERNAL REGISTERS	22
INTERNAL RAM	29
SOFTWARE INTERFACE	29
SOFTWARE COMPATIBILITY CONSIDERATIONS	31
COMMAND CHAINING	32
RESET DETAILS	34
READ AND WRITE CYCLES	35
NODE ID LOGIC	43
TRANSMIT/RECEIVE LOGIC	43
IMPROVED DIAGNOSTICS	43
OSCILLATOR	45
OPERATIONAL DESCRIPTION	46
MAXIMUM GUARANTEED RATINGS	46
DC CHARACTERISTICS	46
TIMING DIAGRAMS	49

Please see Addendum 1 entitled Data Sheet Errata for Revision B COM90C66, which discusses changes to this data sheet which apply to the Revision B device, on Page 62.

Please see Addendum 2 entitled Data Sheet Errata for Revision D COM90C66, which discusses changes to this data sheet which apply to the Revision D device, on Page 64.



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For other machines, the IOCHRDY signal may be briefly negated to give the device the extra time necessary to support the faster machines. Aside from the implementation of a 16-bit data bus interface, the remaining bus interface logic is identical to that found in the SMC COM90C65, which contains all the support logic circuitry.

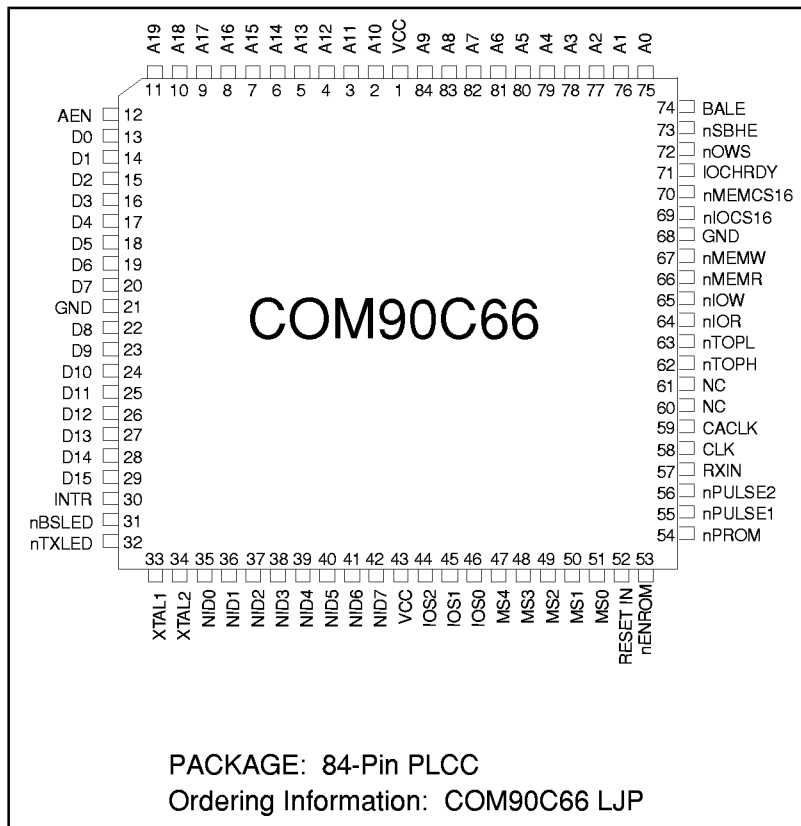
The ARCNET Local Area Network is a token passing network which operates at a 2.5 Mbps data rate. A token passing protocol provides predictable response times because each network event occurs within a known time interval. Throughput can be reliably predeter-

mined based upon the number of nodes and their expected traffic.

The COM90C66 establishes the network configuration and automatically reconfigures the token passing order as new nodes are added or deleted from the network.

The COM90C66 performs address recognition, CRC checking and generation, packet acknowledgement, and other network management functions. The COM90C66 interfaces directly to the IBM PC/AT or compatibles. The internal 2K x 8 RAM buffer is used to hold up to four data packets with a maximum length of 508 bytes each.

PIN CONFIGURATION



DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
PROCESSOR INTERFACE			
75-84, 2-11	Address 0-19	A0-A19	Input. These signals are connected to the address lines of the host processor and are used to access memory and I/O locations of the COM90C66, as well as to access the external ROM through the COM90C66.
13-20, 22-29	Data 0-15	D0-D15	Input/Output. These signals are used by the host to transmit data to and from the internal registers and buffer memory of the COM90C66 and are connected to weak internal pull-up resistors.
63, 62	nTransceiver Direction Control	nTOPL, nTOPH	Output. These active low signals control the data bus transceiver. When these signals are high, data gets sent from the PC to the COM90C66. When these signals are low, data gets sent from the COM90C66 to the PC, or from the PROM to the PC if the PROM signal is also low.
71	I/O Channel Ready	IOCHRDY	Output. This signal, when low, is optionally used by the COM90C66 to extend host cycles. This is an open-drain signal. An external pull-up resistor is typically provided by the system.
12	Address Enable	AEN	Input. This signal, when low, acts as a qualifier for I/O Address Selection. When the signal is high, I/O decoding is disabled. This signal has no effect on Memory Address Selection.
74	Address Latch Enable	BALE	Input. The falling edge of this signal is used by the COM90C66 to latch the A0-A19 lines and the nSBHE signal via an internal transparent latch. This signal is connected to a weak internal pull-up resistor.
64	nI/O Read	nIOR	Input. This active low signal is issued by the host microprocessor to indicate an I/O Read operation. A low level on this pin when the COM90C66 is accessed enables data from the internal registers of the COM90C66.
65	nI/O Write	nIOW	Input. This active low signal is issued by the host microprocessor to indicate an I/O Write operation. A low pulse on this pin when the COM90C66 is accessed enables data from the Data Bus into the internal registers of the COM90C66.

DESCRIPTION OF PIN FUNCTIONS

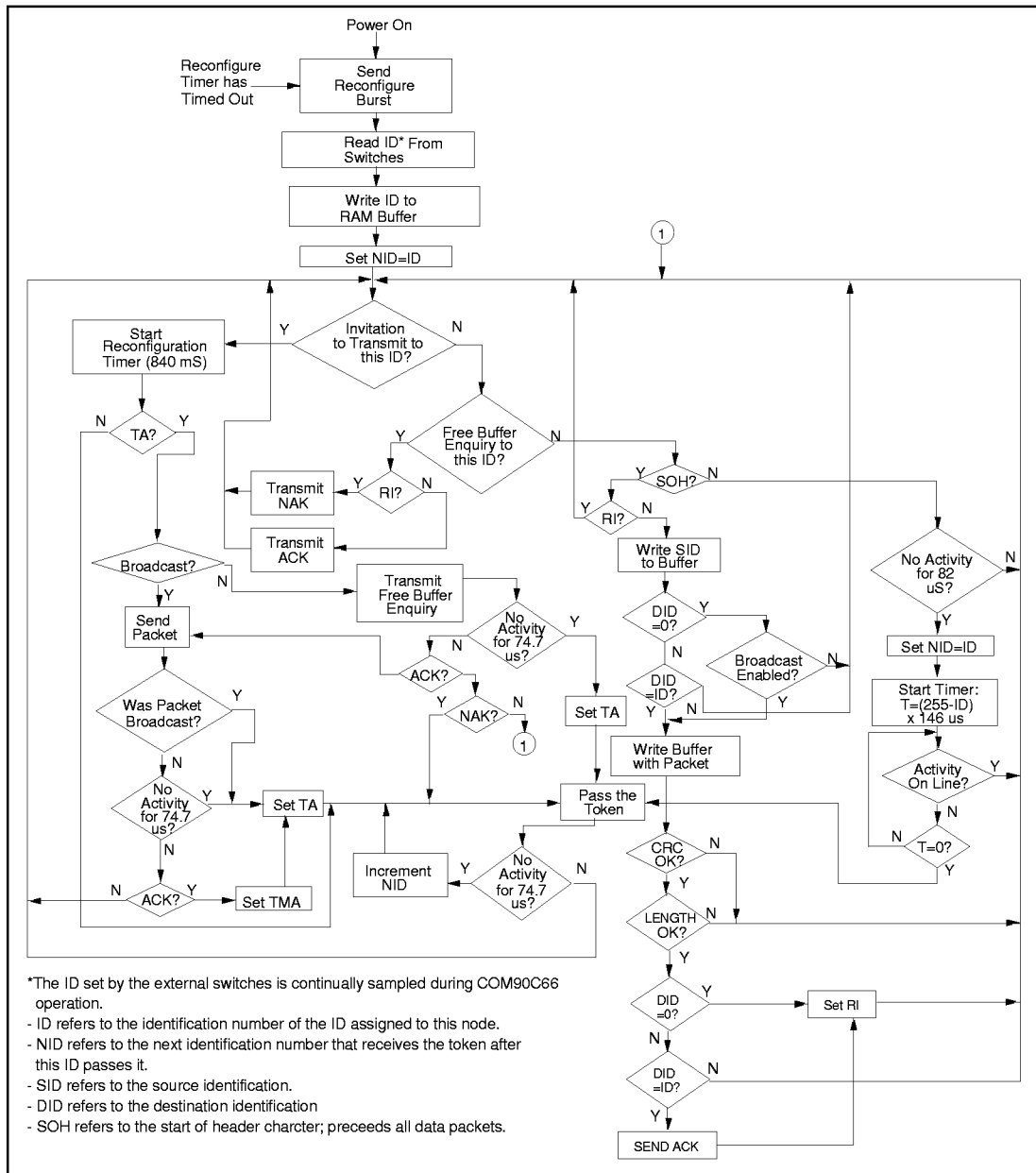
PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
66	nMemory Read	nMEMR	Input. This active low signal is issued by the host microprocessor to indicate a Memory Read operation. A low level on this pin when the COM90C66 is accessed enables data from the internal RAM of the COM90C66 or the PROM onto the data bus to be read by the host.
67	nMemory Write	nMEMW	Input. This active low signal is issued by the host microprocessor to indicate a Memory Write operation. A low pulse on this pin when the COM90C66 is accessed enables data from the data bus into the internal RAM of the COM90C66.
52	Reset In	RESETIN	Input. This active high signal is the power on reset signal from the host. It is used to activate the internal reset circuitry within the COM90C66.
53	nROM Enable	nENROM	Input. This active low signal enables the decoding of the external PROM. This signal also affects the timing of IOCHRDY and the number of address lines used to decode nMEMCS16. This signal is connected to a weak internal pull-up resistor.
54	nROM Select	nPROM	Output. This active low signal is issued by the COM90C66 to enable the external 8-bit wide PROM or the external register of the COM90C66.
30	Interrupt Request	INTR	Output. This active high signal is generated by the COM90C66 when an enabled interrupt condition occurs. INTR returns to its inactive state when the interrupt status condition or the corresponding interrupt mask bit is reset.
72	nZero Wait State	n0WS	Output. This active low signal is used to force zero wait state access cycles on the IBM PC Bus. This is an open-drain signal. An external pull-up resistor is typically provided by the system.
70	nMemory 16-Bit Chip Select	nMEMCS16	Output. This active low signal is used to indicate that the present data transfer is a 16-bit memory cycle. The COM90C66 can be configured to use A19-A17 or A19-A11 to generate nMEMCS16. This is an open-drain signal. An external pull-up resistor is typically provided by the system.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
69	nI/O 16-Bit Chip Select	nIOCS16	Output. This active low signal is used to indicate that the present data transfer is a 16-bit I/O cycle. A15-A2 are used to generate nIOCS16. This is an open-drain signal. An external pull-up resistor is typically provided by the system.
73	nSystem Bus High Enable	nSBHE	Input. This active low signal is used to enable the COM90C66 to transfer data on D8-D15 of the Data Bus.
TRANSMISSION MEDIA INTERFACE			
56, 55	nPulse 2, nPulse 1	nPULSE 2, nPULSE 1	Output. These active low signals carry the transmit data information, encoded in pulse format, from the COM90C66 to the LAN Driver.
57	Receive In	RXIN	Input. This signal carries the receive data information from the LAN Driver to the COM90C66.
MISCELLANEOUS			
51-47	Memory Base Address Select	MS0-MS4	Input. These signals are generated by external switches. They are used by the memory decoder to select a block of memory. These signals are connected to weak internal pull-up resistors.
46-44	I/O Base Address Select	IOS0-IOS2	Input. These signals are generated by external switches. They are used by the I/O decoder to select a block of 16 I/O locations. These signals are connected to weak internal pull-up resistors.
35-42	Node ID Select	NID0-NID7	Input. These signals are generated by external switches. The Node ID code represents the node identification of this particular COM90C66. These signals are connected to weak internal pull-up resistors.
32	nTransmit Activity LED	nTXLED	Output. This active low signal is used for direct connection to an LED through a resistor to V _{cc} to indicate transmit activity. This signal has 12mA sink capability.
31	nBoard Select Activity LED	nnBSLED	Output. This active low signal is used for direct connection to an LED through a resistor to V _{cc} to indicate board activity. This signal has 12mA sink capability.

DESCRIPTION OF PIN FUNCTIONS

PLCC PIN NO.	NAME	SYMBOL	DESCRIPTION
33, 34	Crystal Oscillator	XTAL1, XTAL2	An external parallel resonant 20 MHz crystal should be connected to these pins. If an external 20 MHz TTL clock is used instead, it must be connected to XTAL1 with a 390 Ω pull-up resistor and XTAL2 should be left floating.
59	CA Clock	CACLK	Output. This is the start/stop CA clock and should be left floating for typical operation.
58	Clock	CLK	Output. This is a general purpose 5 MHz clock and should be left floating for typical operation.
1, 43	Power Supply	V _{cc}	+5 Volt Power Supply pin.
21, 68	Ground	GND	Ground pins.
60-61	No Connect	NC	Make no connection to these pins.



- *The ID set by the external switches is continually sampled during COM90C66 operation.
- ID refers to the identification number of the ID assigned to this node.
 - NID refers to the next identification number that receives the token after this ID passes it.
 - SID refers to the source identification.
 - DID refers to the destination identification
 - SOH refers to the start of header character; precedes all data packets.

FIGURE 1 - COM90C66 OPERATION

PROTOCOL DESCRIPTION

NETWORK PROTOCOL

Communication on the network is based on a token passing protocol. Establishment of the network configuration and management of the network protocol are handled entirely by the COM90C66's internal microcoded sequencer. A processor or intelligent peripheral transmits data by simply loading a data packet and its destination ID into the RAM buffer and issuing a command to enable the transmitter. When the COM90C66 next receives the token, it verifies that the receiving node is ready by first transmitting a FREE BUFFER ENQUIRY message. If the receiving node transmits an ACKnowledge message, the data packet is transmitted followed by a 16-bit CRC. If the receiving node cannot accept the packet (typically its receiver is inhibited), it transmits a Negative Acknowledgement message and the transmitter passes the token. Once it has been established that the receiving node can accept the packet and transmission is complete, the receiving node will verify the packet. If the packet is received successfully, the receiving node transmits an ACKnowledge message (or nothing if it is received unsuccessfully) allowing the transmitter to set the appropriate status bits to indicate successful or unsuccessful delivery of the packet. An interrupt mask permits the COM90C66 to generate an interrupt to the processor when selected status bits become true. Figure 1 is a flow chart illustrating the internal operation of the COM90C66.

NETWORK RECONFIGURATION

A significant advantage of the COM90C66 is its ability to adapt to changes on the network. Whenever a new node is activated or deactivated, a NETWORK RECONFIGURATION is performed. When a new COM90C66 is turned on (creating a new active node on the network), or if the COM90C66 has not received an INVITATION TO TRANSMIT for 840 mS, or if a software reset occurs, the device causes a

NETWORK RECONFIGURATION by sending a RECONFIGURE BURST consisting of eight marks and one space repeated 765 times. The purpose of this burst is to terminate all activity on the network. Since this burst is longer than any other type of transmission, the burst will interfere with the next INVITATION TO TRANSMIT, destroy the token and keep any other node from assuming control of the line.

When any COM90C66 senses an idle line for greater than 82 μ S, which will only occur when the token is lost, each COM90C66 starts an internal timeout equal to 146 μ S times the quantity 255 minus its own ID. It also sets the internally-stored NID (next ID representing the next possible ID node) equal to its own ID. If the timeout expires with no line activity, the COM90C66 starts sending INVITATION TO TRANSMIT with the Destination ID (DID) equal to the currently-stored NID. Within a given network, only one COM90C66 will timeout (the one with the highest ID number). After sending the INVITATION TO TRANSMIT, the COM90C66 waits for activity on the line. If there is no activity for 74.7 μ S, the COM90C66 increments the NID value and transmits another INVITATION TO TRANSMIT using the NID equal to the DID. If activity appears before the 74.7 μ S timeout expires, the COM90C66 releases control of the line. During NETWORK RECONFIGURATION, INVITATIONS TO TRANSMIT will be sent to all 256 possible IDs. Each COM90C66 on the network will finally have saved a NID value equal to the ID of the COM90C66 that it released control to. At this point, control is passed directly from one node to the next with no wasted INVITATIONS TO TRANSMIT being sent to IDs not on the network until the next NETWORK RECONFIGURATION occurs. When a node is powered off, the previous node will attempt to pass it the token by issuing an INVITATION TO TRANSMIT. Since this node will not respond, the previous node will timeout and transmit another INVITATION TO TRANSMIT to an incremented ID and eventually a response will be received.

The time required to do a NETWORK RECONFIGURATION depends on the number of nodes in the network, the propagation delay between nodes, and the highest ID number on the network, but will be in the range of 24 to 61 mS.

BROADCAST MESSAGES

Broadcasting gives a particular node the ability to transmit a data packet to all nodes on the network simultaneously. ID zero is reserved for this feature and no node on the network can be assigned ID zero. To broadcast a message, the transmitting node's processor simply loads the RAM buffer with the data packet and sets the DID equal to zero. Figure 9 illustrates the position of each byte in the packet with the DID residing at address 01 HEX of the current page selected in the TRANSMIT command. Each individual node has the ability to ignore broadcast messages by setting the most significant bit of the ENABLE RECEIVE TO PAGE nn command (see Table 7) to logic "0".

EXTENDED TIMEOUT FUNCTION

There are three timeouts associated with the COM90C66 operation:

Response Time

The Response Time is equal to the round trip propagation delay between the two furthest nodes on the network plus the maximum turn around time (the time it takes a particular COM90C66 to start sending a message in response to a received message), which is approximately 12.7 μ S. The round trip propagation delay is a function of the transmission media and network topology. For a typical system using RG62 coax in a baseband system, a one-way cable propagation delay of 31 μ S translates to a distance of about four miles. The flow chart in Figure 1 uses a value of 74.7 μ S ($31 + 31 + 12.7$) to determine if any node will respond.

Idle Time

The Idle Time is associated with a NETWORK RECONFIGURATION. Figure 1 illustrates that during a NETWORK RECONFIGURATION, one node will continually transmit INVITATIONS TO TRANSMIT until it encounters an active node. Every other node on the network must distinguish between this operation and an entirely idle line. During NETWORK RECONFIGURATION, activity will appear on the line every 82 μ S. This 82 μ S is equal to the Response Time of 74.7 μ S plus the time it takes the COM90C66 to retransmit another message (usually another INVITATION TO TRANSMIT).

Reconfiguration Time

If any node does not receive the token within the Reconfiguration Time, the node will initiate a NETWORK RECONFIGURATION.

The ET2 and ET1 bits (bits 3 and 4 of the Configuration Register) allow the network to operate over longer distances than the four miles stated earlier. The logic levels on these bits control the maximum distances over which the COM90C66 can operate by controlling the three timeout values described above. See the description of the ET1 and ET2 bits, found in Table 8, for the table containing the combinations of these bits. It should be noted that for proper network operation, all COM90C66s connected to the same network must have the same Response Time, Idle Time, and Reconfiguration Time.

LINE PROTOCOL

The ARCNET line protocol can be described as isochronous because each byte is preceded by a start interval and ended with a stop interval. Unlike asynchronous protocols, there is a constant amount of time separating each data byte. Each byte takes up exactly 11 clock intervals with a single clock interval being 400 nS in duration. As a result, one byte is

transmitted every 4.4 μ S and the time to transmit a message can be precisely determined. The line idles in a spacing (logic "0") condition. A logic "0" is defined as no line activity and a logic "1" is defined as a negative pulse of 200 nS duration. A transmission starts with an ALERT BURST consisting of six unit intervals of mark (logic "1"). Eight-bit data characters are then sent with each character preceded by two unit intervals of mark and one unit interval of space. Five types of transmission can be performed as described below:

Invitations To Transmit

An Invitation To Transmit is used to pass the token from one node to another and is sent by the following sequence:

- An ALERT BURST
- An EOT (End Of Transmission--ASCII code 04 HEX)
- Two (repeated) DID (Destination IDentification) characters

ALERT BURST	EOT	DID	DID
-------------	-----	-----	-----

Free Buffer Enquiries

A Free Buffer Enquiry is used to ask another node if it is able to accept a packet of data and

ALERT BURST	SOH	SID	DID	DID	COUNT	data	data	CRC	CRC
-------------	-----	-----	-----	-----	-------	------	------	-----	-----

is sent by the following sequence:

- An ALERT BURST
- An ENQ (ENquiry--ASCII code 85 HEX)
- Two (repeated) DID (Destination IDentification) characters

ALERT BURST	ENQ	DID	DID
-------------	-----	-----	-----

Data Packets

A Data Packet consists of the actual data being sent to another node and is sent by the following sequence:

- An ALERT BURST
- An SOH (Start Of Header--ASCII code 01 HEX)
- An SID (Source IDentification) character
- Two (repeated) DID (Destination IDentification) characters
- A single COUNT character which is the 2's complement of the number of data bytes to follow if a short packet is being sent or 00 HEX followed by a COUNT character which is the 2's complement of the number of data bytes to follow if a long packet is being sent
- N data bytes where COUNT = 256-N (or 512-N for a long packet)
- Two CRC (Cyclic Redundancy Check) characters. The CRC polynomial used is $X^{16} + X^{15} + X^2 + 1$.

Acknowledgements

An Acknowledgement is used to acknowledge reception of a packet or as an affirmative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- An ACK (ACKnowledgement--ASCII code 86 HEX) character



Negative Acknowledgements

A Negative Acknowledgement is used as a negative response to FREE BUFFER ENQUIRIES and is sent by the following sequence:

- An ALERT BURST
- A NAK (Negative Acknowledgement--ASCII code 15 HEX) character



SYSTEM DESCRIPTION

The System Block Diagram shown in Figure 2 illustrates a typical implementation of an ARCNET node using the COM90C66. The only external components required to complete an ARCNET node design are one or two bus transceivers (for 8-bit or 16-bit applications, respectively) and the LAN Driver, making the COM90C66 the most highly-integrated ARCNET solution. The COM90C66 provides for simple interfacing to both sides of the ARCNET system, namely the microprocessor and the transmission media.

MICROPROCESSOR INTERFACE

The left half of Figure 2 illustrates a typical COM90C66 interface to the PC. The sections outlined in dotted lines represent the portion which distinguishes the 16-bit interface, while the remaining interface exists for both 8-bit and 16-bit applications. The interface consists of a 20-bit address bus, a 16-bit data bus and a control bus. All accesses to the internal RAM, the optional PROM and the internal registers are controlled by the COM90C66.

The microprocessor's address lines are directly connected to the COM90C66. The address decoding circuitry of the COM90C66 monitors the address bus to determine valid accesses to the device.

Figure 2 shows octal bus transceivers utilized as the interface between the microprocessor's data lines and the COM90C66. The transceivers are only necessary when interfacing to a high current drive data bus such as the IBM PC data bus, and may otherwise be omitted. The COM90C66 provides the nTOPL and nTOPH signals which control the direction of the external transceiver(s). The nTOPL signal is also activated during PROM Read Cycles.

The microprocessor's control bus is directly connected to the COM90C66 and is used in access cycle communication between the device and the microprocessor. All accesses support zero wait state arbitration in most machines. The Control Bus has been optimized to support the intricacies of the IBM AT Bus and the EISA Bus.

TRANSMISSION MEDIA INTERFACE

The right half of Figure 2 illustrates the COM90C66 interface to the transmission media used to connect the node to the network. The HYC9058/68/88 may be used to drive the media. During transmission, the COM90C66 transmits a logic "1" by generating two 100 nS non-overlapping negative pulses, nPULSE1 and nPULSE2. These signals are sent to the LAN Driver, which in turn creates a 200 nS dipulse signal on the media. A logic "0" is transmitted by the absence of the two negative pulses, that is, the nPULSE1 and nPULSE2 outputs remain high, therefore there is an absence of a dipulse.

During reception the 200 nS dipulse appearing on the media is coupled through the RF transformer of the LAN Driver. A positive pulse at the RXIN pin of the COM90C66 is interpreted as a logic "1". Again, if no dipulse is present, the COM90C66 interprets a logic "0".

Typically, RXIN pulse occur at multiples of 400 nS. The COM90C66 can tolerate distortion of plus or minus 100 nS and still correctly capture the RXIN pulses.

During Reset, the transmitter portion of the COM90C66 is disabled and the nPULSE1 and nPULSE2 pins are inactive high.

The COM90C66 includes the nTXLED and nBSLED signals which, when tied to LEDs, provide indication of transmit and board access activity. In addition, it is possible for the user to completely disable the transmitter through software. These two unique features represent two of the improvements made in the diagnostics of the device. Please see the Improved Diagnostics section of this document for further detail.

FUNCTIONAL DESCRIPTION

MICROSEQUENCER

The COM90C66 contains an internal microsequencer which performs all of the control operation necessary to carry out the ARCNET protocol. It consists of a clock generator, a 554 x 8 ROM, a program counter, two instruction registers, an instruction decoder, a no-op generator, jump logic, and reconfiguration logic.

The COM90C66 derives a 5 MHz and a 2.5 MHz clock from the external crystal. These clocks provide the rate at which the instructions are executed within the COM90C66. The 5 MHz clock is the rate at which the program counter operates, while the 2.5 MHz clock is the rate at which the instructions are executed. The microprogram is stored in the ROM and the

instructions are fetched and then placed into the instruction registers. One register holds the op code, while the other holds the immediate data.

Once the instruction is fetched, it is decoded by the internal instruction decoder, at which point the COM90C66 proceeds to execute the instruction. When a no-op instruction is encountered, the microsequencer enters a timed loop, in which case the program counter is temporarily stopped until the loop is complete.

When a jump instruction is encountered, the program counter is loaded with the jump address from the ROM. The COM90C66 contains an internal reconfiguration timer which interrupts the microsequencer if it has timed out.

At this point the program counter is cleared, after which the MYRECON bit of the Diagnostic Status Register is set.

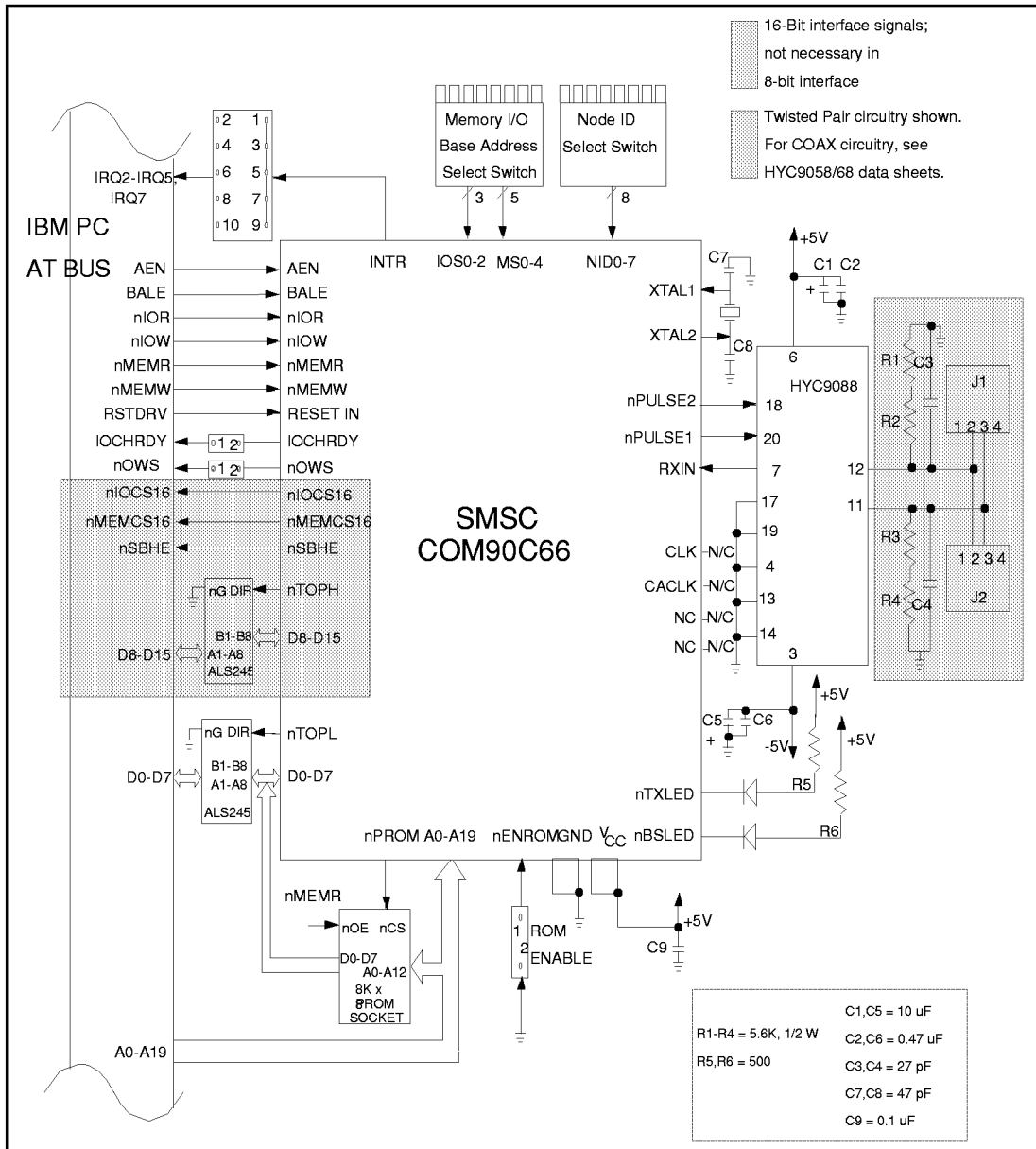


FIGURE 2 - SYSTEM BLOCK DIAGRAM

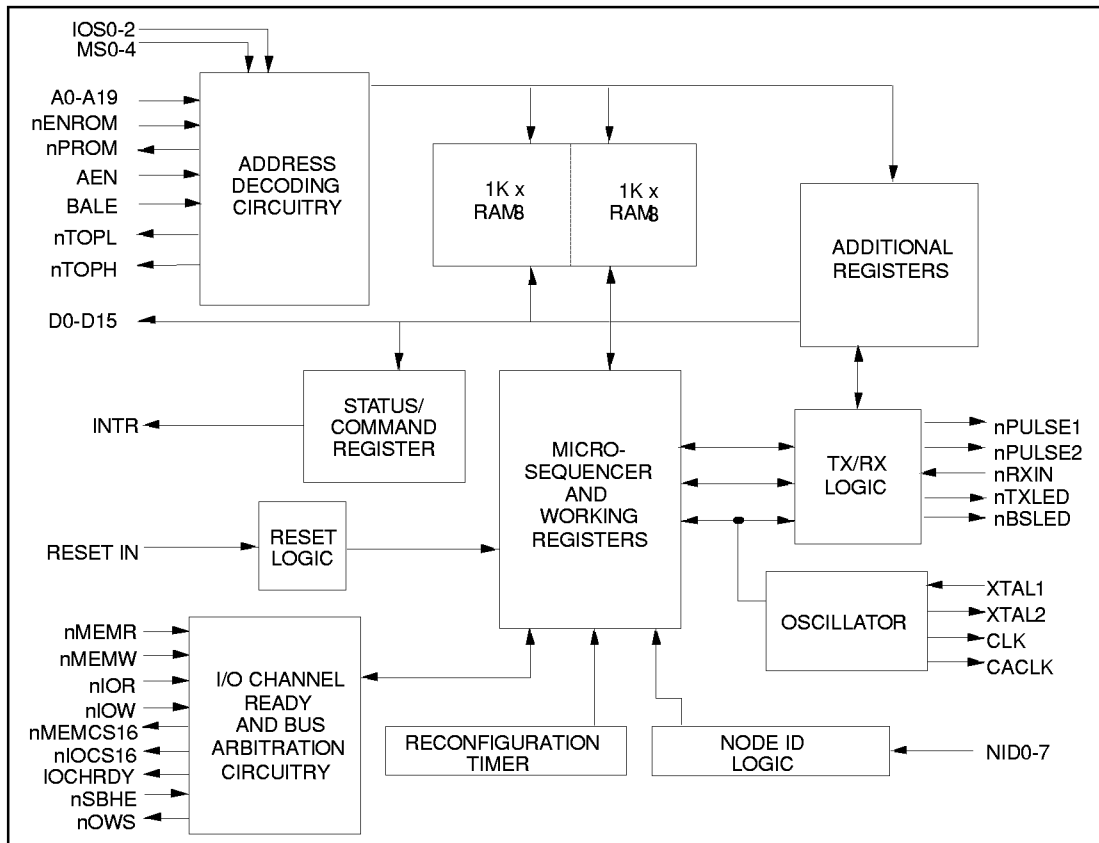


FIGURE 3 - INTERNAL BLOCK DIAGRAM

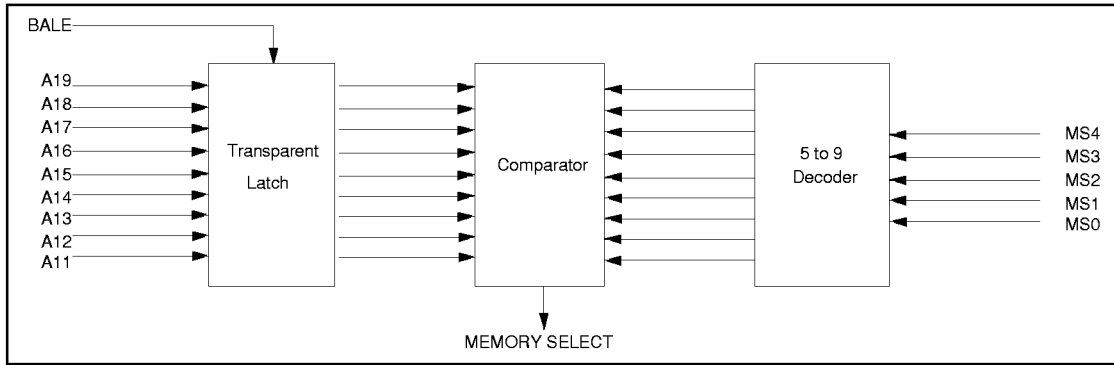


FIGURE 4 – MEMORY SELECTOR

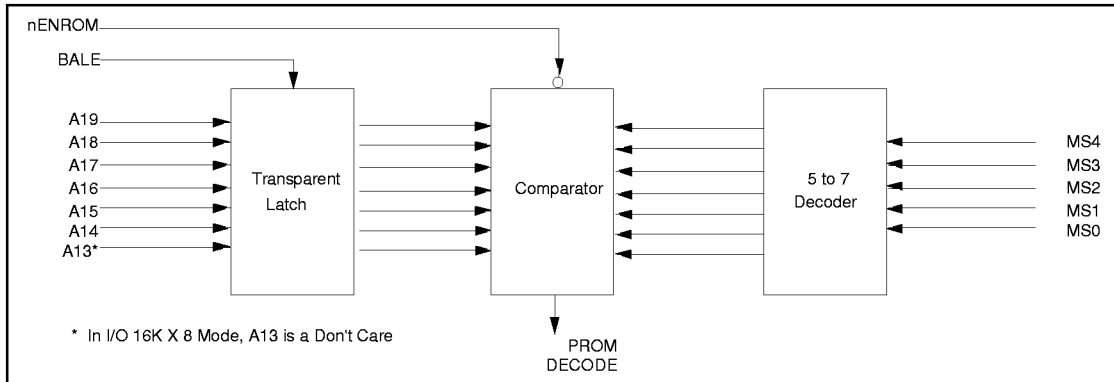


FIGURE 5 – PROM SELECTOR

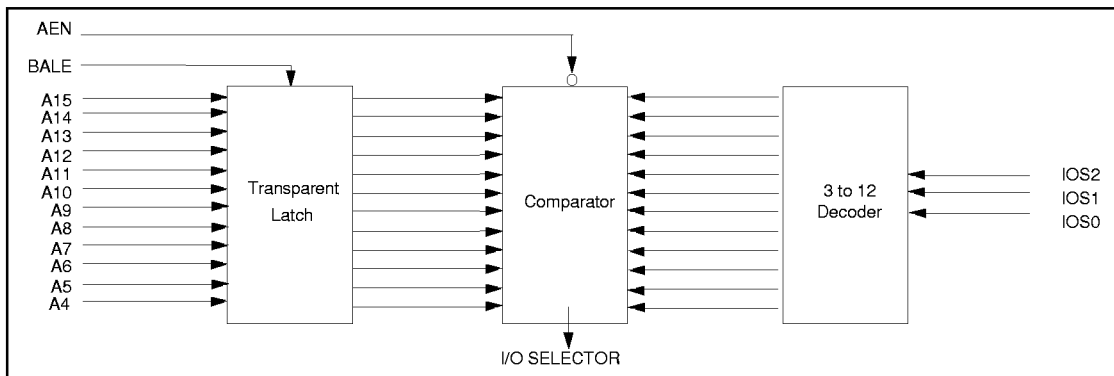
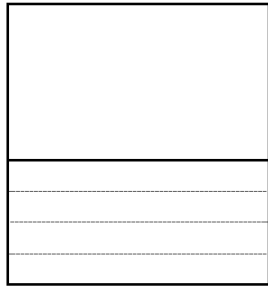


FIGURE 6 – I/O SELECTOR



**FIGURE 7 - 16K MEMORY SEGMENT
CHOSEN BY MS0-MS4
(Memory Mapped Mode)**



**FIGURE 8 - 16K PROM SEGMENT
CHOSEN BY MS0-MS4
(I/O Mapped, 16K X 8 Mode)**

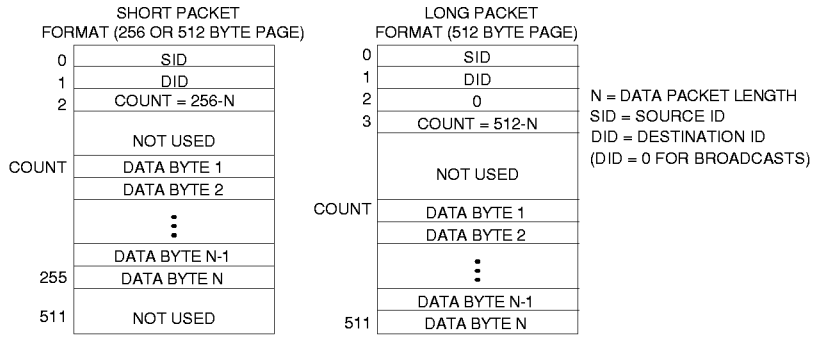


FIGURE 9 – RAM BUFFER PACKET CONFIGURATION

Table 1 – User Configuration of Memory Map

MS4	MS3	MS2	MS1	MS0	DECODED BITS FOUND IN DATA REGISTER								RAM ADDRESS RANGE	PROM ADDRESS RANGE
					D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	1	1	0	0	0	0	0	0	C:0000-C:07FF	C:2000-C:3FFF
0	0	0	0	1	1	1	0	0	0	0	0	1	C:0800-C:0FFF	C:2000-C:3FFF
0	0	0	1	0	1	1	0	0	0	0	1	0	C:1000-C:17FF	C:2000-C:3FFF
0	0	0	1	1	1	1	0	0	0	0	1	1	C:1800-C:1FFF	C:2000-C:3FFF
0	0	1	0	0	1	1	0	0	0	1	0	0	C:4000-C:47FF	C:6000-C:7FFF
0	0	1	0	1	1	1	0	0	0	1	0	1	C:4800-C:4FFF	C:6000-C:7FFF
0	0	1	1	0	1	1	0	0	0	1	1	0	C:5000-C:57FF	C:6000-C:7FFF
0	0	1	1	1	1	1	0	0	0	1	1	1	C:5800-C:5FFF	C:6000-C:7FFF
0	1	0	0	0	1	1	0	0	1	1	0	0	C:C000-C:C7FF	C:E000-C:FFFF
0	1	0	0	1	1	1	0	0	1	1	0	1	C:C800-C:CFFF	C:E000-C:FFFF
0	1	0	1	0	1	1	0	0	1	1	1	0	C:D000-C:D7FF	C:E000-C:FFFF
0	1	0	1	1	1	1	0	0	1	1	1	1	C:D800-C:DFFF	C:E000-C:FFFF
0	1	1	0	0	1	1	0	1	0	0	0	0	D:0000-D:07FF	D:2000-D:3FFF
0	1	1	0	1	1	1	0	1	0	0	0	1	D:0800-D:0FFF	D:2000-D:3FFF
0	1	1	1	0	1	1	0	1	0	0	1	0	D:1000-D:17FF	D:2000-D:3FFF
0	1	1	1	1	1	1	0	1	0	0	1	1	D:1800-D:1FFF	D:2000-D:3FFF
1	0	0	0	0	1	1	0	1	0	1	0	0	D:4000-D:47FF	D:6000-D:7FFF
1	0	0	0	1	1	1	0	1	0	1	0	1	D:4800-D:4FFF	D:6000-D:7FFF
1	0	0	1	0	1	1	0	1	0	1	1	0	D:5000-D:57FF	D:6000-D:7FFF
1	0	0	1	1	1	1	0	1	0	1	1	1	D:5800-D:5FFF	D:6000-D:7FFF
1	0	1	0	0	1	1	0	1	1	0	0	0	D:8000-D:87FF	D:A000-D:BFFF
1	0	1	0	1	1	1	0	1	1	0	0	1	D:8800-D:8FFF	D:A000-D:BFFF
1	0	1	1	0	1	1	0	1	1	0	1	0	D:9000-D:97FF	D:A000-D:BFFF
1	0	1	1	1	1	1	0	1	1	0	1	1	D:9800-D:9FFF	D:A000-D:BFFF
1	1	0	0	0	1	1	0	1	1	1	0	0	D:C000-D:C7FF	D:E000-D:FFFF
1	1	0	0	1	1	1	0	1	1	1	0	1	D:C800-D:CFFF	D:E000-D:FFFF
1	1	0	1	0	1	1	0	1	1	1	1	0	D:D000-D:D7FF	D:E000-D:FFFF
1	1	0	1	1	1	1	0	1	1	1	1	1	D:D800-D:DFFF	D:E000-D:FFFF
1	1	1	0	0	1	1	1	0	0	0	0	0	E:0000-E:07FF	E:2000-E:3FFF
1	1	1	0	1	1	1	1	0	0	0	0	1	E:0800-E:0FFF	E:2000-E:3FFF
1	1	1	1	0	1	1	1	0	0	0	1	0	E:1000-E:17FF	E:2000-E:3FFF
1	1	1	1	1	1	1	1	0	0	0	1	1	E:1800-E:1FFF	E:2000-E:3FFF

ADDRESS DECODING

The COM90C66 includes address decoding circuitry that compares the value of the Address Bus to the address range selected by the Memory Select (MS0-MS4) and I/O Select (IOS0-IOS2) pins in order to determine

processor accesses to the on-board PROM, the on-chip RAM, and I/O locations. By placing switches on the MS0-MS4 and the IOS0-IOS2 pins, the user configures the Memory Map and I/O Map according to the possible address ranges shown in Tables 1 and 2.

Table 2 - User Configuration of I/O Map

IOS2	IOS1	IOS0	I/O ADDRESS RANGE
0	0	0	0260-026F
0	0	1	0290-029F
0	1	0	02E0-02EF
0	1	1	02F0-02FF
1	0	0	0300-030F
1	0	1	0350-035F
1	1	0	0380-038F
1	1	1	03E0-03EF

Memory Address Decoding

The Memory Address Decoding circuitry is used to select a block from the memory map of the processor for PROM and RAM accesses. Figure 4 illustrates how the memory selection works. The MS4-MS0 pins are decoded through a 5 to 9 Decoder to generate a 9-bit value. These nine bits are compared to the A19-A11 lines of the Address Bus in order to select a particular 16K memory segment. Figure 7 illustrates a 16K block of memory that has been selected by the MS4-MS0 pins. The PROM occupies the upper 8K area of the selected 16K segment and is accessed when A13 = 1. The RAM occupies one of four selectable 2K areas of the selected 16K segment and is accessed when A13 = 0. A11 and A12 are used to determine which 2K segment of the lower 8K area will be used for the RAM buffer.

Figure 5 illustrates how the external PROM selection works. The MS4-MS0 pins are

decoded through a 5 to 7 Decoder to generate a 7-bit value. These seven bits are compared to the A19-A13 lines of the Address Bus in order to select an 8K memory range. Figure 7 illustrates an 8K block of memory for the PROM. In I/O 16K x 8 Mode only a 16K memory range is selected for the PROM. Figure 8 illustrates a 16K block of memory for the PROM.

The nENROM pin is used to enable decoding for the on-board PROM. If nENROM is connected to a logic "1", the COM90C66 will not generate the nPROM signal, the nTOPL signal, or the IOCHRDY signal for accesses to the PROM. In this configuration, the COM90C66 will only occupy a 2K segment of memory.

I/O Address Decoding

This section is used to select a block of 16 I/O locations from the I/O map of the processor. Figure 6 illustrates how the I/O selection

Table 3 – Read Register Summary

REGISTER	READ								ADDRESS
	MSB							LSB	
STATUS	RI	X	X	POR	TEST	RECON	TMA	TA	00
DIAG. STATUS	MYRECON	X	RCVACT	TOKEN	X	X	X	X	01
CONFIGURATION	16EN	CCHEN	DECODE	ET1	ET2	WAIT	IO-ACCESS	TXOFF	02
I/O SELECT	0	0	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	03
MEMORY SELECT	MEM7	MEM6	MEM5	MEM4	MEM3	MEM2	MEM1	MEM0	04
NODE ID	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	05
RESERVED	X	X	X	X	X	X	X	X	06
RESERVED	X	X	X	X	X	X	X	X	07
RESET	X	X	X	X	X	X	X	X	08
RESET	X	X	X	X	X	X	X	X	09
RESET	X	X	X	X	X	X	X	X	0A
RESET	X	X	X	X	X	X	X	X	0B
DATA LOW	D7	D6	D5	D4	D3	D2	D1	D0	0C
DATA HIGH	D15	D14	D13	D12	D11	D10	D9	D8	0D
ADDRESS PTR LOW	A7	A6	A5	A4	A3	A2	A1	A0	0E
ADDRESS PTR HIGH	X	AUTO-INC	X	X	X	A10	A9	A8	0F

Table 4 – Write Register Summary

ADDRESS	WRITE								REGISTER
00	RI	0	0	0	0	RECON	0	TA	INTERRUPT MASK
01	D7	D6	D5	D4	D3	D2	D1	D0	COMMAND
02	16EN	CCHEN	DECODE	ET1	ET2	WAIT	IO-ACCESS	TXOFF	CONFIGURATION
03	0	0	0	0	0	0	0	0	RESERVED
04	0	0	0	0	0	0	0	0	RESERVED
05	NID7	NID6	NID5	NID4	NID3	NID2	NID1	NID0	NODE ID
06	0	0	0	0	0	0	0	0	RESERVED
07	D7	D6	D5	D4	D3	D2	D1	D0	EXTERNAL REGISTER
08	X	X	X	X	X	X	X	X	RESET
09	X	X	X	X	X	X	X	X	RESET
0A	X	X	X	X	X	X	X	X	RESET
0B	X	X	X	X	X	X	X	X	RESET
0C	D7	D6	D5	D4	D3	D2	D1	D0	DATA LOW
0D	D15	D14	D13	D12	D11	D10	D9	D8	DATA HIGH
0E	A7	A6	A5	A4	A3	A2	A1	A0	ADDRESS PTR LOW
0F	0	AUTO-INC	0	0	0	A10	A9	A8	ADDRESS PTR HIGH

process works. The IOS2-IOS0 pins are decoded through a 3 to 12 Decoder to generate a 12-bit value. These 12 bits are compared to the A15-A4 lines of the address bus in order to determine which block of 16 I/O locations will be used by the chip. A logic "0" on the AEN signal enables the I/O decoding process. Tables 3 and 4 illustrate the COM90C66 register map. Reserved locations should not be accessed.

INTERNAL REGISTERS

The COM90C66 contains internal registers which may be accessed by the microprocessor. All undefined bits are read as undefined and must be written as logic "0".

Status Register

The COM90C66 Status Register is an 8-bit read-only register which can be accessed by the microprocessor. All of the bits in this register (except for bits 5 and 6) are software-compatible with previous SMSC ARCNET devices. The Extended Timeout bits are now in the Configuration Register. The Status Register contents are traditionally defined as in Table 5. The Status Register contents are defined differently during the Command Chaining operation. Please refer to the "Command Chaining" section of this document for these definitions. The Status Register defaults to the value 1XX1 0001 upon either hardware or software reset.

Interrupt Mask Register (IMR)

The COM90C66 is capable of generating an interrupt signal when certain status bits become true. A write to the IMR specifies which status bits will be enabled to generate the interrupt. The bit positions in the IMR are in the same position as their corresponding status bits in the Status Register, and a logic "1" in a particular position enables the corresponding interrupt. While the Receiver Inhibited, Reconfiguration,

and Transmitter Available status bits are capable of generating an interrupt if enabled, the TMA status bit will never cause an interrupt. The IMR takes on the following bit definition:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RI	X	X	X	X	RE-CON	X	TA

The three maskable status bits are ANDed with their respective mask bits, and the results are ORed to produce the processor interrupt signal INTR. An RI or TA interrupt is masked when the corresponding mask bit is reset to logic "0", but will reappear when the corresponding mask bit is set to logic "1" again, unless the interrupt status condition has been cleared by this time. A RECON interrupt is cleared when the CLEAR FLAGS command is issued. The Interrupt Mask Register defaults to the value 0000 0000 upon either hardware or software reset.

Diagnostic Status Register

The Diagnostic Status Register contains three read-only bits which give the user the ability to troubleshoot network or node operation. The various combinations of these bits and the Transmitter Off bit of the Configuration Register represent different situations and can be used during troubleshooting. These bits are reset to logic "0" upon reading the Diagnostic Status Register or upon software or hardware reset. The register contents are as in Table 6. The Diagnostic Status Register defaults to the value 0X00 XXXX upon either hardware or software reset.

Command Register

Execution of commands are initiated by performing a processor I/O write with the written data defining the commands listed in Table 7. Any combinations of written data other than those listed in Table 7 are not permitted and may result in incorrect chip and/or network operation.

Table 5 - Status Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	Receiver Inhibited	RI	This bit, if high, indicates that a packet has been deposited into the RAM buffer page nn as specified by the last ENABLE RECEIVE TO PAGE nn command. No messages will be received until this command is issued, and once the message has been received, the RI bit gets set, thereby inhibiting the receiver. The RI bit is cleared by issuing an ENABLE RECEIVE TO PAGE nn command. This bit, when set, will cause an interrupt if the corresponding bit of the Interrupt Mask Register is also set.
6	(not used)		This bit is undefined.
5	(not used)		This bit is undefined.
4	Power On Reset	POR	This bit, if high, indicates that the COM90C66 has been reset by either a software reset, a hardware reset, or setting the Node ID = 00H. The POR bit is cleared by the CLEAR FLAGS command.
3	Test	TEST	This bit is intended for test and diagnostic purposes. It is a logic "0" under normal operating conditions.
2	Reconfiguration	RECON	This bit, if high, indicates that the Line Idle Timer has timed out because the RXIN pin (pin 57) was idle for 82 S. The RECON bit is cleared during a CLEAR FLAGS command. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set. The interrupt service routine should consist of looking at the MYRECON bit of the Diagnostic Status Register to make sure that there are not consecutive reconfigurations caused by this node.
1	Transmitter Message Acknowledged	TMA	This bit, if high, indicates that the packet transmitted as a result of an ENABLE TRANSMIT FROM PAGE nn command has been positively acknowledged. This bit should only be considered valid after the TA bit (bit 0) is set. Broadcast messages are never acknowledged. The TMA bit is cleared by issuing the ENABLE TRANSMIT FROM PAGE nn command.
0	Transmitter Available	TA	This bit, if high, indicates that the transmitter is available for transmitting. This bit is set at the conclusion of an ENABLE TRANSMIT FROM PAGE nn command or upon execution of a DISABLE TRANSMITTER command. The TA bit is cleared by issuing the ENABLE TRANSMIT FROM PAGE nn command after the node next receives the token. This bit, when set, will cause an interrupt if the corresponding bit in the Interrupt Mask Register is also set.

Table 6 - Diagnostic Status Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7	My Reconfiguration	MY-RECON	This bit, if high, indicates that the reconfiguration that has just occurred was caused by this node. This bit is set when the Token Reception Timer times out. This bit is typically read after the RECON bit of the Status Register is found to be set. Refer to the Improved Diagnostics section of this document for further details.
5	Receive Activity	RCVACT	This bit, if high, indicates that receive activity (data transition) is detected on the RXIN pin of the device. This bit may be used in diagnostic troubleshooting of the network or node. Refer to the Improved Diagnostics section of this document for further details.
4	Token Seen	TOKEN	This bit, if high, indicates that a token has been seen on the network, sent by a node other than this node. This bit may be used in diagnostic troubleshooting of the network or node. Refer to the Improved Diagnostics section of this document for further details.
6, 3-0	(not used)		These bits are undefined.

Table 7 - Command Register

WRITTEN DATA	COMMAND NAME	DESCRIPTION
0000 0000	CLEAR TRANSMIT INTERRUPT	This command is only used in the Command Chaining operation. Please refer to the Command Chaining section of this document for definition of this command.
0000 0001	DISABLE TRANSMITTER	This command will cancel any pending transmit command (transmission that has not yet started) and will set the TA (Transmitter Available) status bit to logic "1" when the COM90C66 next receives the token.
0000 0010	DISABLE RECEIVER	This command will cancel any pending receive command. If the COM90C66 is not yet receiving a packet, the RI (Receiver Inhibited) bit will be set to logic "1" the next time the token is received. If packet reception is already underway, reception will run to its normal conclusion.

Table 7 - Command Register

WRITTEN DATA	COMMAND NAME	DESCRIPTION
000n n011	ENABLE TRANSMIT FROM PAGE nn	This command prepares the COM90C66 to begin a transmit sequence from RAM buffer page nn the next time it receives the token. When this command is loaded, the TA and TMA bits are reset to logic "0". The TA bit is set to logic "1" upon completion of the transmit sequence. The TMA bit will have been set by this time if the COM90C66 has received an acknowledgement from the destination node. This acknowledgement is strictly hardware level, which is sent by the receiving node before its controlling processor is even aware of message reception. It is also possible for this acknowledgement to get lost due to line errors. This implies that the TMA bit is not a guarantee of proper destination reception. Refer to Figure 1 for details of the transmit sequence and its relation to the TA and TMA status bits.
b00n n100	ENABLE RECEIVE TO PAGE nn	This command allows the COM90C66 to receive data packets into RAM buffer page nn and resets the RI status bit to logic "0". If the value of "b" is a logic "1", the COM90C66 will also receive broadcast transmission. A broadcast transmission is a transmission to ID zero. The RI status bit is set to logic "1" upon successful reception of a message.
0000 c101	DEFINE CONFIGURATION	This command defines the maximum length of packets that may be handled by the device. If the value of "c" is a logic "1", the COM90C66 will handle long as well as short packets. If the value of "c" is a logic "0", the COM90C66 will only handle short packets (packets less than 254 bytes).
000r p110	CLEAR FLAGS	This command resets one or both flags of the COM90C66. If the value of "p" is a logic "1", the POR status flag is reset. If the value of "r" is a logic "1", the RECON status flag is reset.
0000 1000	CLEAR RECEIVE INTERRUPT	This command is only used in the Command Chaining operation. Please refer to the Command Chaining section of this document for definition of this command.

Table 8 - Configuration Register

BIT	BIT NAME	SYMBOL	DESCRIPTION																														
7	16-Bit Enable	16EN	This bit, if high, enables 16-bit operation of the device. A low level on this bit enables only 8-bit operation. This bit defaults to a logic "0" upon hardware reset.																														
6	Command Chaining Enable	CCHEN	This bit, if high, enables the Command Chaining operation of the device. Please refer to the Command Chaining section of this document for further details. A low level on this bit ensures software compatibility with previous SMSC ARCNET devices. This bit defaults to a logic "0" upon hardware reset.																														
5	Decode Mode	DECODE	In I/O Mapped applications, this bit is used to choose between an 8K or 16K block of ROM. In this case, a logic "0" defines 8K, while a logic "1" defines 16K. In Memory Mapped applications, this bit and the nMEMCS16 signal are used to choose whether the nMEMCS16 signal will be generated by decoding a block of 128K or 2K. In this case, a logic "0" defines 128K, while a logic "1" defines 2K. For more details on the use of this bit, refer to the Memory vs. I/O Cycles section of this document. This bit defaults to a logic "0" upon hardware reset.																														
4, 3	Extended Timeout 1, 2	ET1, ET2	<p>These bits allow the network to operate over longer distances than the default four miles by controlling the Response Time, the Idle Time, and the Reconfiguration Time. For proper network operation, all nodes should be configured for the same timeout values. The bit combinations follow:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2"></th> <th>RESPONSE</th> <th>IDLE</th> <th>RECONFIGURATION</th> </tr> <tr> <th>ET2</th> <th>ET1</th> <th>TIME (μs)</th> <th>TIME (μs)</th> <th>TIME (mS)</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1193.6</td> <td>1312</td> <td>1680</td> </tr> <tr> <td>0</td> <td>1</td> <td>596.8</td> <td>656</td> <td>1680</td> </tr> <tr> <td>1</td> <td>0</td> <td>298.4</td> <td>328</td> <td>1680</td> </tr> <tr> <td>1</td> <td>1</td> <td>74.7</td> <td>82</td> <td>840</td> </tr> </tbody> </table> <p>These bits default to a logic "1" upon hardware reset.</p>			RESPONSE	IDLE	RECONFIGURATION	ET2	ET1	TIME (μs)	TIME (μs)	TIME (mS)	0	0	1193.6	1312	1680	0	1	596.8	656	1680	1	0	298.4	328	1680	1	1	74.7	82	840
		RESPONSE	IDLE	RECONFIGURATION																													
ET2	ET1	TIME (μs)	TIME (μs)	TIME (mS)																													
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0	1	596.8	656	1680																													
1	0	298.4	328	1680																													
1	1	74.7	82	840																													

Table 8 - Configuration Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
2	Wait State	WAIT	This bit is used to select the type of cycle. A logic "1" on this bit negates the IOCHRDY signal for approximately one or two XTAL1 clocks, creating one wait state. A logic "0" selects zero wait state arbitration to the buffer RAM and generates the Zero Wait State signal. Refer to the wait State Details section of this document for further information. This bit defaults to a logic "1" upon hardware reset.
1	I/O Access	IO-ACCESS	A logic "1" on this bit configures the buffer RAM for sequential I/O mapped accesses, while a logic "0" configures the buffer RAM for memory mapped accesses. This bit defaults to a logic "0" upon hardware reset.
0	Transmitter Off	TXOFF	A logic "1" on this bit disables the transmitter of the COM90C66, while the receiver remains functional. A logic "0" keeps the transmitter enabled. This bit may be used in diagnostic troubleshooting of the network or node. Refer to the Improved Diagnostics section of this document for further details. This bit defaults to a logic "0" upon hardware reset.

Table 9 - Address Pointer Low Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7-0	Address 7-0	A7-A0	These bits hold the lower eight address bits which provide the addresses to the on-chip RAM.

Table 10 - Address Pointer High Register

BIT	BIT NAME	SYMBOL	DESCRIPTION
7, 5-3	(not used)		These bits are undefined.
6	Auto Increment	AUTO-INC	This bit controls whether or not the address pointer will increment automatically when the device is in I/O Mapping Mode. A logic "1" on this bit will automatically increment the pointer after each access. A logic "0" will disable this function. Please refer to the Memory Vs. I/O section of this document for further detail.
2-0	Address 10-8	A10-A8	These bits hold the upper three address bits which provide the addresses to the on-chip RAM.

Configuration Register

The Configuration Register is a read/write register which can be accessed by the microprocessor to configure the different modes of the COM90C66. The register contents are as in Table 8. The Configuration Register defaults to the value 0001 1100 upon hardware reset only.

Memory Select Register

This register contains the decoded bits of the Memory Select 0-4 switch. For further details, refer to the Memory Address Decoding section of this document, as well as Figure 4 and Table 1.

I/O Select Register

This register contains the decoded bits of the I/O Select 0-2 switch. For further details, refer to the I/O Address Decoding section of this document, as well as Figure 6 and Table 2.

Node ID Register

The Node ID Register contains the values of the Node ID switches. The microprocessor may read from the Node ID Register at any time for diagnostic purposes. In addition, the COM90C66 may be put into a special mode whereby the microprocessor may write to the Node ID register, thus software programming the Node ID. To enter this special mode, the Node ID switches must be set to 00H. Note that when the Node ID switches are set to 00H, the COM90C66 is put into a Disable Transmitter mode and it will not attempt to join the network. When the device is in the Disable Transmitter mode, tokens are not passed and reconfigurations are not generated by the node. The Receiver portion of the device will provide the user with useful information about the network. The device will not attempt to rejoin the network until a valid Node ID value is placed into the Node ID Register. In addition to keeping the device in the

Disable Transmit mode, when the Node ID switches are set to 00H, the RAM of the COM90C66 is kept hidden from the microprocessor. The RAM may be enabled by issuing a software reset, followed by a valid write to the Node ID Register. Refer to the System Reset Logic section for details on resetting the device in a non-IBM-compatible environment. The I/O address of the Node ID Register is 05H. Tables 3 and 4 illustrate the Node ID Register, as well as the other registers of the COM90C66. The Node ID Register defaults to the value 0000 0000 upon hardware reset only.

External Register

The optional write only external register may be used for application-dependent functions. A read operation at this location will provide invalid data. Whenever a write to address 07H occurs, the COM90C66 activates the nPROM signal. In this case, the nPROM signal is to be used as the nChip Select signal and the nLOW signal should be used to write to the external register. The external PROM should use the nPROM signal as nChip Select and the nMEMR signal as nOutput Enable, as usual.

Reset Register

Any read or write access to I/O offsets 08H, 09H, 0AH, or 0BH generates a software reset. These four I/O locations were preserved for software compatibility with the COM90C65 ARCNET Controller. Refer to the Reset Logic section of this document for further details.

Data Low and High Registers

These read/write registers are each 8-bits wide and are used in I/O Mapped Mode only. The Data Register contains the byte or word which is meant to be read from or written to the address location presently specified by the address pointer. The contents of the Data Registers are undefined upon hardware reset.

Address Pointer Low and High Registers

These read/write registers are each 8-bits wide and are used in I/O Mapped Mode only. These bits contain undefined data upon software or hardware reset. The contents of the Address Pointer Registers are defined as in Tables 9 and 10. The COM90C66 is capable of incrementing the address automatically, as explained in Table 10. The contents of the Address Pointer Registers are undefined upon hardware reset.

INTERNAL RAM

The integration of the 2K x 8 RAM in the COM90C66 provides several advantages to the user. Firstly, a significant amount of real estate is saved due to the elimination of the external RAM, the external latch, and the multiplexed address/data bus and control functions which used to be necessary to interface to the RAM.

Secondly, the system designer is no longer dependent upon the fluctuating cost of external RAM. This, and the fact that the entire solution is more integrated (reducing reliability problems, assembly time and costs, and layout complexity), adds up to significant cost reductions.

Thirdly, with the eliminated need for RAM interfacing signals, several other innovative features now take the place of the freed-up pins without the need for increased package size and pinout. Some of the pins have been replaced with such useful features as the 16-bit data bus, the Zero Wait-State signal, the diagnostic pins, and the choice of Memory or I/O Mapped functionality.

Fourthly, the COM90C66 is very high speed. The ability of the device to implement zero wait state cycles is partly due to the fact that the RAM is internal to the device.

The Configuration Register contains the I/O Access bit, which determines whether the RAM will be configured for sequential I/O mapped accesses or memory mapped accesses. Additionally, the Decode Mode bit allows the choice of 8K or 16K block of ROM if set for I/O mapped access, or the choice of the activation of the nMEMCS16 signal upon access to 2K or 128K of RAM if set for memory mapped access.

When the device is configured for a 16-bit data bus, the on-chip RAM is seen by the processor as 1K x 16 rather than 2K x 8.

SOFTWARE INTERFACE

The microprocessor interfaces to the COM90C66 via software by accessing the various registers. These actions were discussed in the Internal Registers section of this document. Additionally, it is necessary to understand the details of how the Internal Registers are used in the transmit and receive sequences and how the internal RAM buffer is properly set up. The sequence of events that tie these actions together are discussed as follows.

Transmit Sequence

During a transmit sequence, the microprocessor selects a 256 or 512 byte segment of the RAM buffer and writes into it. The appropriate buffer size is specified in the DEFINE CONFIGURATION command. When long packets are enabled, the COM90C66 interprets the packet as a long or short packet, depending on whether the content of the buffer address 2 is zero or non-zero. The format of the buffer is shown in Figure 9. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and Address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 would contain the value 512-N, where N

represents the message length. The SID in Address 0 is used by the receiving node to reply to the transmitting node. The COM90C66 puts the local ID in this location, therefore, it is not necessary to write into this location.

Please note that a short packet may contain between one and 253 data bytes, while a long packet may contain between 257 and 508 data bytes. A minimum value of 257 exists on a long packet so that the COUNT is expressible in eight bits. This leaves three exception packet lengths which do not fit into either a short or long packet; packet lengths of 254, 255, or 256 bytes. If packets of these lengths must be sent, the user must add dummy bytes to the packet (00's) in order to make the packet fit into a long packet.

Once the buffer is written into, the microprocessor awaits a logic "1" on the TA bit, indicating that a previous transmit command has concluded and another may be issued. Each time the message is loaded and a transmit command issued, it will take a variable amount of time before the message is transmitted, depending on the traffic on the network and the location of the token at the time the transmit command was issued. Typically, the conclusion of the transmit command, which is flagged when TA becomes a logic "1", generates an interrupt. If the device is configured for the Command Chaining operation, please see the Command Chaining section of this document for further detail on the software.

Once the TA bit becomes a logic "1", the microprocessor issues the ENABLE TRANSMIT FROM PAGE nn command, which resets the TA and TMA bits to logic "0". If the message is not a BROADCAST, the COM90C66 automatically issues a FREE BUFFER ENQUIRY to the destination node in order to send the message. At this point, one of three possibilities may occur:

The first possibility is if a free buffer is available at the destination node, in which case it responds with an ACKnowledgement. At this point, the COM90C66 fetches the data from the Transmit Buffer and performs the transmit sequence. If a successful transmit sequence is completed, the TMA bit and the TA bit are set to logic "1". If the packet is not transmitted successfully, TMA will not be set. A successful transmission occurs when the receiving node responds to the packet with an ACK. An unsuccessful transmission occurs when the receiving node does not respond to the packet.

The second possibility is if the destination node responds with a Negative Acknowledgement. A NAK occurs when the RI bit of the destination node is a logic "1". In this case, the token is passed on from the transmitting node to the next node. The next time the transmitter receives the token, it will try to retransmit a FREE BUFFER ENQUIRY. If a NAK is again received, the token is again passed onto the next node. A software timeout on the TA bit is used to prevent this from happening endlessly. That is, if no software timeout existed, the transmitting node would keep trying to issue a Free Buffer Enquiry, even though it keeps receiving NAKs as a response. The software timeout on the TA bit is used to tell the microprocessor to disable the transmitter via the DISABLE TRANSMITTER command, which will cause the transmission to be abandoned and the TA bit to be set to a logic "1" when the node next receives the token, while the TMA bit remains at a logic "0".

The third possibility which may occur after a FREE BUFFER ENQUIRY is issued is if no response is received from the destination node. In this case, the TA bit is set to a logic "1" in preparation for the next time the token is received, while the TMA bit remains at a logic "0". The user should determine whether the node will try to retransmit the next time it receives the token.

The fourth possibility is if a non-traditional response is received (some pattern other than ACK or NAK, such as noise). In this case, the token is not passed onto the next node, which causes the Lost Token Timer of the next node to time out, thus generating a network reconfiguration.

The DISABLE TRANSMITTER command may be used to cancel any pending transmit command when the COM90C66 next receives the token. Normally, in an active network, this command will set the TA status bit to a logic "1" when the token is received. If the DISABLE TRANSMITTER command does not cause the TA bit to be set in the time it takes the token to make a round trip through the network, one of three situations exists. Either the node is disconnected from the network, or there are no other nodes on the network, or the external receive circuitry has failed. These situations can be determined either by using the improved diagnostic features of the COM90C66 or by using another software timeout which is greater than the worst case time for a round trip token pass, which occurs when all nodes transmit a maximum length message.

Receive Sequence

A receive sequence begins with the RI status bit becoming a logic "1", which indicates that a previous reception has concluded. The microprocessor will be interrupted if the corresponding bit in the Interrupt Mask Register is set to logic "1". Otherwise, the microprocessor must periodically check the Status Register. Once the microprocessor is alerted to the fact that the previous reception has concluded, it may issue the ENABLE RECEIVE TO PAGE nn command, which resets the RI bit to logic "0" and selects a new page in the RAM buffer. Again, the appropriate buffer size is specified in the DEFINE CONFIGURATION command. Typically, the page which just received the data packet will be read by the microprocessor at this point.

Once the ENABLE RECEIVE TO PAGE nn command is issued, the microprocessor attends to other duties. There is no way of telling how long the new reception will take, since another node may transmit a packet at any time. When another node does transmit a packet to this node, if the DEFINE CONFIGURATION command has enabled the reception of long packets, the COM90C66 interprets the packet as a long or short packet, depending on whether the content of the buffer location 2 is zero or non-zero. The format of the buffer is shown in Figure 9. Address 0 contains the Source Identifier (SID), Address 1 contains the Destination Identifier (DID), and address 2 contains, for short packets, the value 256-N, where N represents the message length, or for long packets, the value 0, indicating that it is indeed a long packet. In the latter case, Address 3 contains the value 512-N, where N represents the message length. Note that on reception the COM90C66 deposits packets into the RAM buffer in the same format that the transmitting node arranged it, which allows for a message to be received and then retransmitted without rearranging any bytes in the RAM buffer other than the SID and DID. Once the packet is received and stored correctly in the selected buffer, the COM90C66 sets the RI bit to logic "1" to signal the microprocessor that the reception is complete.

SOFTWARE COMPATIBILITY CONSIDERATIONS

The COM90C66 guarantees compatibility with previous SMSC ARCNET devices. Upon hardware reset, the device defaults to compatibility mode, that is, 8-bit, memory mapped cycles, non-Command Chaining mode and non-Zero Wait State mode.

COMMAND CHAINING

The Command Chaining operation allows consecutive transmissions and receptions to occur without host intervention. Through the use

of a dual two-level FIFO, commands to be transmitted and received, as well as the status bits, are pipelined.

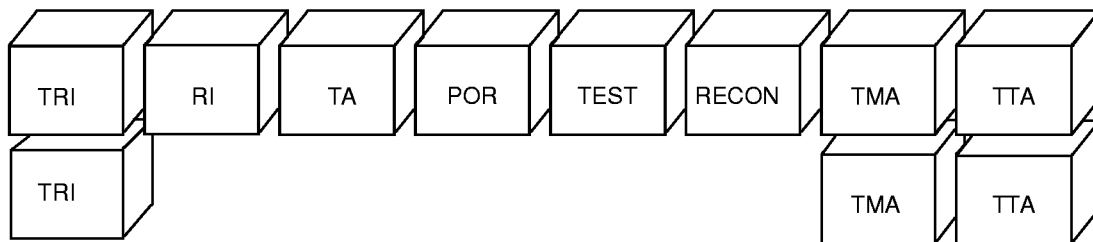
In order for the COM90C66 to be compatible with previous SMSC ARCNET devices, the device defaults to the non-chaining mode. In order to take advantage of the Command Chaining operation, the Command Chaining Mode must be enabled via a logic "1" on bit 6 of the Configuration Register.

The following is a list of Command Chaining guidelines for the software programmer to follow. Further detail can be found in the Transmit Command Chaining and Receive Command Chaining sections of this document.

- The device is designed such that the interrupt service routine latency does not affect performance. The first interrupt maybe serviced prior to the generation of the second interrupt.

- Up to two outstanding transmissions and two outstanding receptions can be pending at any given time. The commands may be given in any order.
- Up to two outstanding transmit interrupts and two outstanding receive interrupts are stored by the device, along with their respective status bits.
- The Interrupt Mask bits act on TTA (Rising Transition on Transmitter Available) for transmit operations and TRI (Rising Transition of Receiver Inhibited) for receive operations. TTA is set upon completion of a packet reception only. Typically there is no need to mask the TTA and TRI bits after clearing the interrupt.
- The traditional TA and RI bits are still available to reflect the present status of the device.

In Command Chaining, the Status Register looks as follows:



Transmit Command Chaining

When the processor issues the first ENABLE TRANSMIT TO PAGE nn command, the COM90C66 responds in the usual manner by resetting the TA and TMA bits to prepare for the transmission from the specified page. The TA bit can be used to see if there is currently a transmission pending, but the TA bit is really meant to be used in the non-chaining mode only. The TTA bits provide the relevant information of the device in the Command Chaining mode.

In the Command Chaining Mode, at any time after the first command is issued, the processor can issue a second ENABLE TRANSMIT FROM PAGE nn command. The COM90C66 stores the fact that the second transmit command was issued, along with the page number.

After the first transmission is completed, the COM90C66 updates the Status Register by setting the TTA bit, which generates an interrupt. The interrupt service routine will read the Status Register. At this point, the TTA bit will be found to be a logic "1" and the TMA (Transmit Message Acknowledge) bit will tell the processor whether the transmission was successful. After reading the Status Register, the CLEAR TRANSMIT INTERRUPT command is issued, thus resetting the TTA bit and clearing the interrupt. Note that only the CLEAR TRANSMIT INTERRUPT command will clear the TTA bit and the interrupt. It is not necessary, however, to clear the bit or the interrupt right away because the status of the transmit operation is double buffered in order to retain the results of the first transmission for analysis by the processor. This information will remain in the Status Register until the CLEAR TRANSMIT INTERRUPT command is issued. Note that the interrupt will remain active until the command is issued, and the second interrupt will not occur until the first interrupt is cleared. The TMA bit is also double buffered to reflect whether the appropriate transmission was a success. The TMA bit should only be considered valid

after the corresponding TTA bit has been set to a logic "1". The TMA bit never causes an interrupt.

When the token is received again, the second transmission will be automatically initiated after the first is completed by using the stored ENABLE TRANSMIT FROM PAGE nn command. The operation is as if a new ENABLE TRANSMIT FROM PAGE nn command has just been issued. After the first Transmit status bits are cleared, the Status Register will again be updated with the results of the second transmission and a second interrupt resulting from the second transmission will occur. The COM90C66 guarantees a minimum of 200nS interrupt inactive time interval before the following edge.

The Transmitter Available (TA) bit of the Interrupt Mask Register now masks only the TTA bit of the Status Register, not the TA bit as in the non-chaining mode. Since the TTA bit is only set upon transmission of a packet (not by RESET), and since the TTA bit may easily be set by issuing a CLEAR TRANSMIT INTERRUPT command, there is no need to use the TA bit of the Interrupt Mask Register to mask interrupts generated by the TTA bit of the Status Register.

In both the Command Chaining mode and the non-chaining mode, the DISABLE TRANSMITTER command will cancel the oldest transmission. This permits canceling a packet destined for a node not ready to receive. If both packets should be canceled, two DISABLE TRANSMITTER commands should be issued.

Receive Command Chaining

Like the Transmit Command Chaining operation, the processor can issue two consecutive ENABLE RECEIVE FROM PAGE nn commands.

After the first packet is received into the first specified page, the TRI bit of the Status Register will be set to logic "1", causing an interrupt. Again, the interrupt need not be serviced

immediately. Typically, the interrupt service routine will read the Status Register. At this point, the RI bit will be found to be a logic "1". After reading the Status Register, the CLEAR RECEIVE INTERRUPT command is issued, thus resetting the TRI bit and clearing the interrupt. Note that only the CLEAR RECEIVE INTERRUPT command will clear the TRI bit and the interrupt. It is not necessary, however, to clear the bit or the interrupt right away because the status of the receive operation is double buffered in order to retain the results of the first reception for analysis by the processor, therefore, the information will remain in the Status Register until the CLEAR RECEIVE INTERRUPT command is issued. Note that the interrupt will remain active until the CLEAR RECEIVE INTERRUPT command is issued, and the second interrupt will not occur until the first interrupt is acknowledged.

The second reception will occur as soon as a second packet is sent to the node, as long as the second ENABLE RECEIVE TO PAGE nn command was issued. The operation is as if a new ENABLE RECEIVE TO PAGE nn command has just been issued. A second interrupt will not occur until the first interrupt is acknowledged by issuing the CLEAR RECEIVE INTERRUPT command. After the first Receive status bits are cleared, the Status Register will again be updated with the results of the second reception and a second interrupt resulting from the second reception will occur. A minimum of 200nS interrupt inactive time interval is guaranteed.

In the COM90C66, the Receive Inhibit (RI) bit of the Interrupt Mask Register now masks only the TRI bit of the Status Register, not the RI bit as in the non-chaining mode. Since the TRI bit is only set upon reception of a packet (not by RESET), and since the TRI bit may easily be set by issuing a CLEAR RECEIVE INTERRUPT command, there is no need to use the RI bit of

the Interrupt Mask Register to mask interrupts generated by the TRI bit of the Status Register.

In both the Command Chaining mode and the non-chaining mode, the DISABLE RECEIVER command will cancel the oldest reception, unless the reception has already begun. If both receptions should be canceled, two DISABLE RECEIVER commands should be issued.

RESET DETAILS

Internal Reset Logic

The COM90C66 includes special reset circuitry to guarantee smooth operation during reset. Special care is taken to assure proper operation in a variety of systems and modes of operation. The design ensures that the COM90C66 will not disturb the microprocessor or the system bus until the system has reached a certain level of operation. Furthermore, in order to eliminate conflicts with other memory elements, the internal RAM of the COM90C66 is hidden from the system until a software reset is issued to the device and until a valid Node ID is placed in the Node ID Register. When the system software determines that no conflicts will arise, it then may enable the internal memory of the COM90C66 via a software reset.

Because most system buses are inherently noisy, the COM90C66 contains digital filter circuitry and a Schmitt Trigger on the RESET IN signal to reject glitches in order to ensure fault-free operation.

The COM90C66 supports two reset options; software and hardware reset. An internal reset signal of pulse width equal to 102.4 μ S is generated from either a hardware or a software reset. The hardware reset occurs when a high signal is asserted on the RESET IN input (pin 65). The minimum reset pulse width is 120 nS (or $2T+20$ nS for crystal frequencies other than 20 MHz, where $T = 1/f$). This pulse width is

used by the internal digital filter, which filters short glitches to only allow valid resets to occur. A software reset is generated when the microprocessor accesses I/O locations 8, 9, A, or B.

Upon reset, the transmitter portion of the device is disabled and the internal registers assume those states outlined in the Internal Registers section.

The COM90C66 will start 102.4 μ S after the RESET IN signal is removed. Please note that the internal RAM buffer cannot be seen by the processor unless a software reset is issued. Therefore, following power up or hardware reset, a software reset must be issued. Please refer to System Reset Logic for the steps to bring the device out of reset. As the device comes out of reset, the COM90C66, after reading its own ID, will execute two write cycles to the RAM buffer. Address 00 HEX will be written with the data D1 HEX and the address 01 HEX will be written with the ID number read from the Node ID Select Switch. The processor may then read RAM buffer address 01 to determine the COM90C66 ID. It should be noted that the data pattern D1 written into the RAM has been chosen arbitrarily. Only if the D1 pattern appears in the RAM buffer can proper operation be assured.

System Reset Logic

The IBM AT Bus automatically provides continuously running cycles for nMEMR, nMEMW, nIOR, and nIOWn which are utilized by the COM90C66 in its internal reset sequence.

Buses other than the IBM AT (or compatible) typically do not provide continuously running cycles. In this case, the user will need to note the following COM90C66 internal reset sequence so that the software interface will provide the proper accesses utilized by the device. Please refer to Figure 10. By satisfying

the simple requirements below, the user can be assured proper operation of the COM90C66's reset sequence in a non-IBM AT environment.

A hardware or software reset begins the COM90C66's internal Power On Reset. Certain steps must be taken to bring the device out of reset. In the case of a hardware reset with the Node ID Switches set to 00H in a non-AT or XT-compatible, the following steps should be taken:

1. Hardware Reset
2. Dummy access cycle (nMEMR, nMEMW, nIOR or nIOW) to end the internal Power On Reset
3. Write to the Node ID Register
4. Wait 114.4 μ s (or 256 bit clocks + 12 μ s)
5. Dummy access cycle
6. Write to the Configuration Register
7. Software Reset to wake up the internal RAM
8. Dummy access cycle
9. Write to the Node ID Register
10. Wait 114.4 μ s (or 256 bit clocks + 12 μ s)
11. Dummy access cycle

If only a software reset occurred, then steps 1-7 are not necessary. If the Node ID Switches are set to a value other than 00, then steps 3 and 9 are not necessary. If the machine is an AT- or XT-compatible, then steps 2, 5, 8 and 11 are not necessary. Once these steps are taken, the COM90C66 comes out of reset. Any accesses thereafter are considered valid accesses.

READ AND WRITE CYCLES

Memory vs. I/O Cycles

In addition to Memory Mapping, the COM90C66 performs Sequential I/O Mapped Memory accesses, thus a packet that is placed in the internal RAM buffer can be accessed by addressing only one 8- or 16-bit I/O location. The processor places the address that needs to be accessed into the Address Pointer by writing

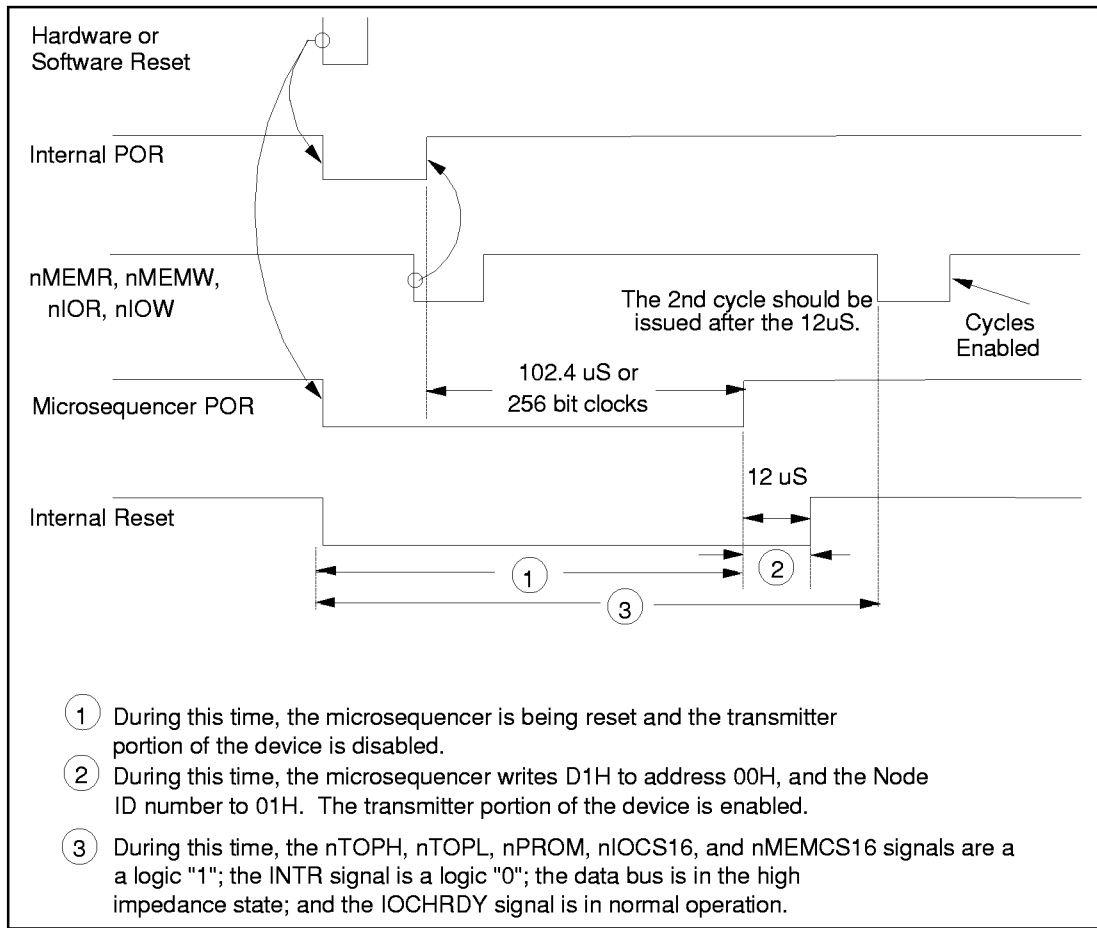


FIGURE 10 - INTERNAL RESET SEQUENCE

it as data to addresses OFH and OEH (Address Pointer High and Low Registers). The processor then reads/writes from/to address 0CH (for 8-bit) or OCH and ODH (for 16 bit) the data found/to be placed at that address. If the Auto Increment bit is turned on, the Address Pointer will then increment the address until the entire packet is obtained/sent. The device in 8-bit mode increments the pointer by one; 16-bit mode increments the pointer by two.

Although Sequential I/O Mapped Memory accesses require more steps than Memory Mapped accesses, I/O Mapped is just as efficient as Memory Mapped and does not require the large block of memory in the host addressing space that Memory Mapped does. On the other hand, Memory Mapped access is more flexible and allows the processor to analyze the data and make decisions without emptying the entire packet into system memory. Refer to Figure 11 for an illustration of the Sequential I/O Mapped Memory access operation.

The fact that the COM90C66 contains independent nMEMCS16 and nIACS16 signals provides design versatility. The board can be software configured for memory mapped or I/O mapped mode, depending on the system constraints. The following is some basic information on both Memory and I/O Modes so that the user can determine which mode is best suited for the application:

Memory Mapped Mode:

On any address bus, all address lines must at some point be latched. On the AT Bus, LA17-LA23 are not latched on the motherboard. These are faster, unlatched addresses which can tell the user immediately when the board is being accessed. These unlatched lines must be

latched externally by the user. The COM90C66 provides the transparent latch necessary for these unlatched address lines, as well as the transparent latch necessary for the additional unlatched addresses on the Micro Channel® Bus. On the AT Bus, the lower, latched address lines (SA0-SA19) come out to the bus a little later than the unlatched lines.

The existence of the faster, unlatched addresses allows the COM90C66 board to recognize accesses immediately, thereby activating the nMEMCS16 signal for any access to a 128 KByte block of memory. The unlatched version of the nMEMCS16 mode of the COM90C66 will meet the timing specification of nMEMCS16 for every machine, but the limitations are that this mode may complicate co-existence with other 8-bit boards in the same 128 KByte block, and an 8-bit auto-boot PROM cannot be supported in this mode. Therefore, the device must be configured for memory mapped, 16-bit mode and the nENROM signal must be high.

In order to use a PROM on the board, the nMEMCS16 signal should be activated for decoding to a 2 KByte block of memory. In this case, the nENROM signal will of course be a logic "0", enabling the PROM. In this mode, co-existence with other 8-bit boards will be supported, as well as the use of the 8-bit PROM, which will be directly controlled by the device. However, this is at the expense of slower nMEMCS16 timing.

Refer to Table 11 for the 16-bit memory mapped decode table as a function of the nENROM pin and the DECODE MODE bit. Refer to Figure 12 for an illustration of the generation of the nMEMCS16 signal.

Table 11 - 16-Bit Memory Mapped Decode

n ENROM	DECODE MODE	RAM	n MEMCS16	ROM
0	X	2K	2K	8K
1	0	2K	128K	-
1	1	2K	2K	-

The internal latches of the COM90C66 go transparent on BALE high and latch on BALE low. If all addresses being used are already latched or valid for the entire duration of the cycle, then the BALE signal may be tied to a logic "1".

I/O Mapped Mode:

The system can also be configured as I/O mapped. In this case, the data transfers to and from the packet buffer are done by accessing an I/O location and having the internal pointer in the device sequentially address memory. The nIOCS16 signal is activated upon accesses to the 16-bit pointer register or to the 16-bit data register.

In the I/O mapped mode, addresses up to A15 are decoded to determine accesses to the device. On the AT bus the A0-A15 lines are provided as latched addresses. Therefore, the BALE signal may be tied to a logic "1". In the I/O Mode, no memory is used by the board except for the optional PROM. The nMEMCS16 signal is not used at all.

A logic "0" on the nENROM pin enables ROM mapping, and in the I/O mapped mode the user can choose between an 8K or 16K block of RAM.

Refer to Table 12 for the 16-bit I/O mapped decode table as a function of the nENROM pin and the DECODE MODE bit. Refer to Figure 12A for an illustration of the generation of the nIOCS16 signal.

Table 12 - 16-Bit I/O Mapped Decode

n ENROM	DECODE MODE	RAM	n MEMCS16	ROM
0	0	I/O	-	8K
0	1	I/O	-	16K
1	X	I/O	-	-

Wait State Details

In the typical computer, the Bus Speed will be slower than the CPU speed so that the peripherals will be able to keep up with the machine. In many cases, the peripheral will need additional delays to be able to keep up, and will therefore use the IOCHRDY signal to tell the processor whether or not it is ready to continue. The use of the IOCHRDY signal effectively "slows down" the bus.

The COM90C66 is quick enough to take advantage of the maximum bus speed of most AT compatibles. The function employs the use of the nOWS signal and guarantees the fastest microprocessor cycles. The use of the nOWS signal effectively "speeds up" the bus.

Upon power up, the COM90C66 defaults to the non-zero wait state mode. The nOWS mode can be easily configured by writing a logic "0" into bit 2 of the Configuration Register.

For machines with faster buses, the COM90C66 can be configured to negate the IOCHRDY line for the minimal period of time necessary. If the IOCHRDY signal is used, it is negated for one XTAL1 clock for RAM and internal register cycles. If the optional PROM is on board, it might require a slower cycle to accommodate its access time even if the device is configured for Zero Wait State Mode. When the nENROM signal is active (logic "0"), the COM90C66 will negate the IOCHRDY signal for two XTAL1 clocks on ROM read accesses. If the optional external register is used, I/O Write

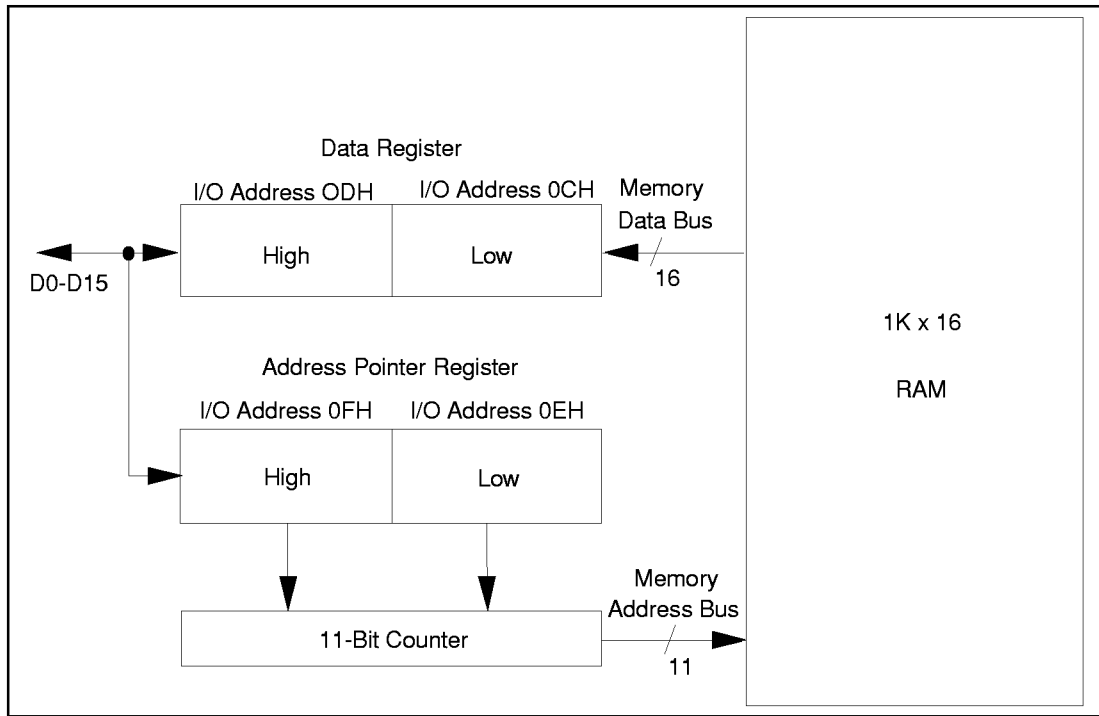


FIGURE 11 - SEQUENTIAL I/O MAPPED MEMORY ACCESS OPERATION

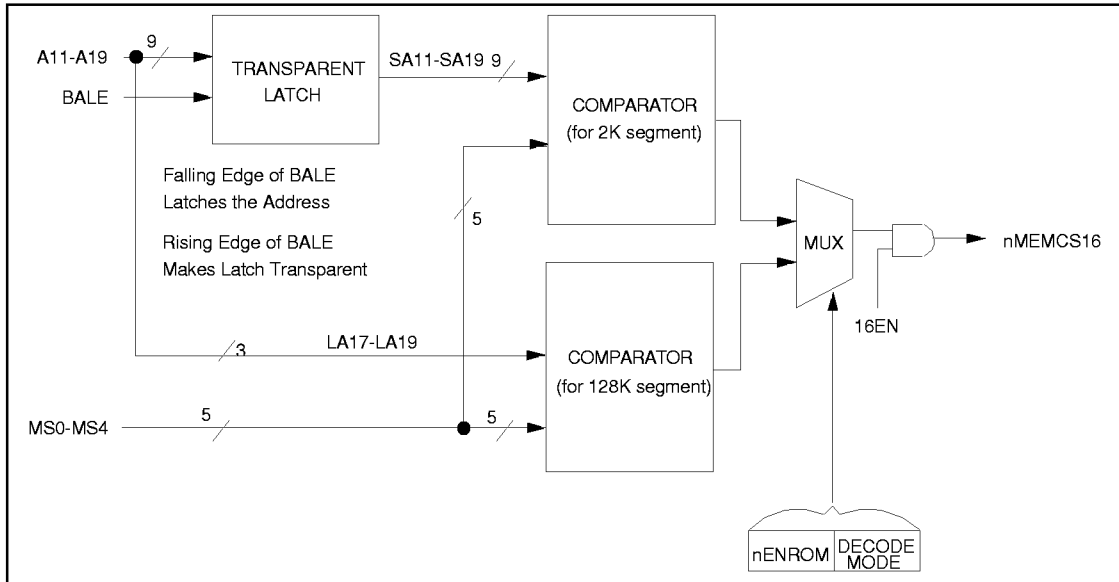


FIGURE 12 – nMEMCS16 GENERATION

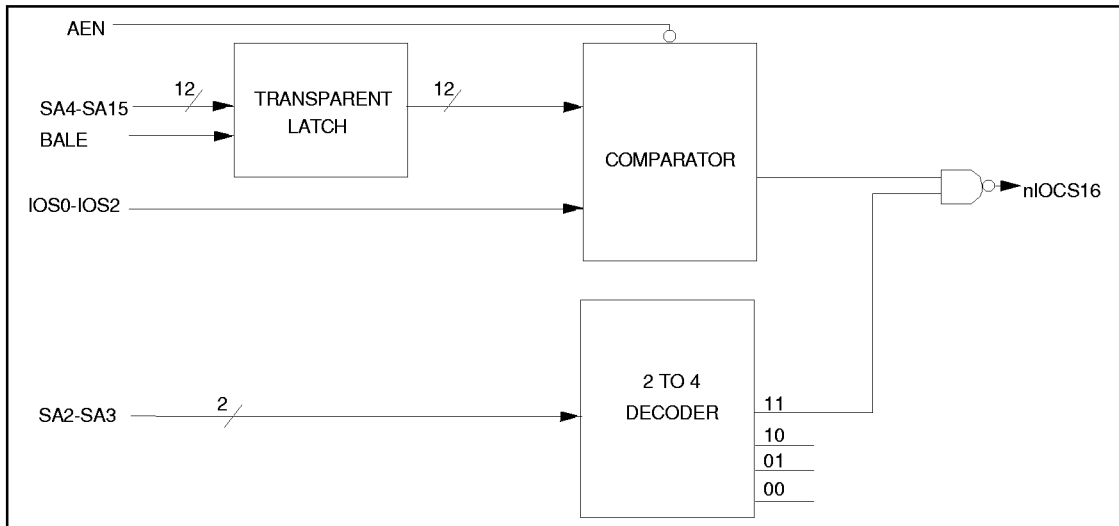


FIGURE 12A - nIOCS16 GENERATION

cycles to it will also cause a negation of the IOCHRDY signal for two XTAL1 clocks. Note that by timing the ready circuitry from the XTAL1 clock, the IOCHRDY signal is timed in absolute time rather than relative to the bus clock.

Either the nOWS signal or the IOCHRDY signal may be used (but not both), depending upon speed of the bus. In the case where the COM90C66 spec meets the bus speed and the user does not need to "speed up" or "slow down" the bus, neither the nOWS nor the IOCHRDY signal should be used. In this case, the Wait State bit of the Configuration Register should be reset to logic "0" to configure the device for Zero Wait State, but the nOWS signal should not be connected to the bus. Figure 2 shows a jumper between the nOWS signal and the bus to illustrate that the signal may be left unconnected. Table 13 shows the IOCHRDY and nOWS signal behavior for RAM, internal register PROM, and external register access.

Table 13 - IOCHRDY and nOWS Signal

WAIT STATE BIT	IOCHRDY	nOWS
0	logic "1"	Activated on Access
1	Negated for One or Two XTAL1 Clocks	logic "1"

Behavior

Please refer to the Zero Wait State and IOCHRDY Timing Diagram for further details on the specifications of these two signals.

8-Bit vs. 16-Bit Accesses

In 8-Bit Mode, the nMEMCS16 and nIOCS16 signals remain in their inactive high state. All register and memory accesses transfer data on the lower half of the data Bus (D0-D7) while the upper half (D8-D15) remain in the high impedance state.

In 16-Bit Mode, the nMEMCS16 signal is activated for RAM accesses in the memory Mapped Mode, while the nIOCS16 signal is activated only for accesses to the pointer or to the data registers. All other registers are only 8-bit registers and thus do not require the nIOCS16 signal. In 16-Bit Mode, register and memory accesses transfer data on the entire Data Bus (D0-D15), except for accesses to 8-Bit registers, which transfer data only on the lower half of the Data Bus (D0-D7) while the upper half (D8-D15) remains in the high impedance state.

8-Bit I/O Mapped Mode:

In order to perform an 8-Bit I/O Mapped Cycle, the 16-Bit Address Pointer Register should be programmed by writing the High Register first, and then the Low Register. All pointer bits are loaded only after the Low Register is written. In 8-Bit I/O Mapped Mode, the A10-A0 register bits determine the byte address to be accessed through the lower portion of the Data Register (address offset OCH). Refer to Table 14 for signal level requirements in 8-bit I/O Mapped accesses.

8-Bit Memory Mapped Mode:

In 8-Bit Memory Mapped Mode, the A10-A0 lines of the Address Bus determine the byte address to be accessed within the 2K block of RAM. Refer to Table 14 for signal level requirements in 8-Bit Memory Mapped accesses.

16-Bit I/O Mapped Mode:

In order to perform a 16-Bit I/O Mapped Cycle, the 16-Bit Address Pointer Register should be programmed by writing the High Register first, and then the Low Register, or writing both the High and Low Registers simultaneously. All pointer bits are loaded only after the Low Register is written. In 16-Bit I/O Mapped Mode, the A10-A0 register bits determine the word

address to be accessed through the Data Register. If a 1K x 16 space is desired, the A0 bit should be forced to a logic "0" and A1-A10 will be used to load the Address Pointer Register. A single byte access at the defined word address is still possible by accessing either the upper or lower portion of the Data Register. When the device is configured for Auto Increment Mode, the access to the upper portion of the Data Register automatically increments the pointer. Refer to the Memory Vs. I/O Cycles section of this document for further information on Sequential I/O Mapped

Memory cycles and the Auto Increment Mode. Refer to Table 14 for signal level requirements in 16-Bit I/O Mapped Mode.

16-Bit Memory Mapped Mode:

In 16-Bit Memory Mapped Mode, the A10-A1 lines of the Address Bus determine the word address to be accessed, while A0 and nSBHE determine which byte within the word location will be accessed. Refer to Table 14 for signal level requirements in 16-Bit Memory Mapped accesses.

Table 14 - 8-Bit vs. 16-Bit Signal Level Requirements*

	ACCESS	A0	nSBHE	nIOCS16	nMEMCS16	DATA TRANSFER
8-Bit I/O Accesses	Address Pointer Low Register	0	X	1	X	D0-D7
	Address Pointer High Register	1	X	1	X	D0-D7
	Data Register	X	X	1	X	D0-D7**
	Other Registers	X	X	1	X	D0-D7
8-Bit Memory	RAM Access	X	X	X	1	D0-D7
16-Bit I/O Accesses	Pointer Register Word	0	0	0	X	D0-D7, D8-D15
	Address Pointer Low Register	0	1	0	X	D0-D7
	Address Pointer High Register	1	0	0	X	D8-D15
	Data Register Word	0	0	0	X	D0-D7, D8-D15**
	Even RAM Byte	0	1	0	X	D0-D7
	Odd RAM Byte	1	0	0	X	D8-D15**
	Other Registers	X	X	1	X	D0-D7
16-Bit Memory Accesses	RAM Access, Word	0	0	X	0	D0-D7, D8-D15
	Even RAM Byte	0	1	X	0	D0-D7
	Odd RAM Byte	1	0	X	0	D8-D15

* Any combinations other than those defined above are illegal.

**This access will increment the pointer

NODE ID LOGIC

The Node ID code generated by the external Node ID Select Switches is used to identify this particular COM90C66. The code, which is input by the COM90C66 in parallel format, is used by the COM90C66 during transmission, reception, reset, and reconfiguration.

Upon reset, the COM90C66 reads the Node ID code set up on the switches and loads them into the Node ID Register. For diagnostic purposes, the Node ID may be read by the microprocessor. The ARCNET protocol maintains that a destination Node ID of 00H will allow the source node to broadcast a message.

In addition, in order to provide the user with increased flexibility and to eliminate the cost of the Node ID switch on board, the COM90C66 provides special circuitry which allows the user to program the Node ID of any node via software. To software program the Node ID register, the Node ID switches of that node must be physically set to 00H. 00H is not recognized by the ARCNET protocol as a valid Node ID and therefore is used only to switch to this special mode. Setting the Node ID switches to all zero's puts the COM90C66 into reset. The device will not attempt to join the network and no microcode is performed. Tokens are not passed and reconfigurations are not generated by the node. The device will not attempt to rejoin the network until a valid Node ID value is placed into the Node ID Register.

For normal operation, the Node ID switches will be set to some valid address between 01H and FFH. Writing a nonzero value to the Node ID register will allow the COM90C66 to join the network.

TRANSMIT/RECEIVE LOGIC

Figure 13 illustrates the events which occur in transmission or reception of data consisting of

1,1,0. The COM90C66, during transmission, produces two 100 nS nonoverlapping pulses on the nPULSE1 and nPULSE2 lines to indicate a logic "1", whereas a lack of pulses indicates a logic "0". The nPULSE1 and nPULSE2 signals are used to drive the HYC9058, the HYC9068 or the HYC9088, which in turn creates a 200 nS dipulse signal on the transmission media. During reception, each dipulse appearing on the transmission media is coupled through the RF transformer of the LAN Driver to produce a positive pulse on the RXIN pin. The pulse is captured by the COM90C66 and is then converted to NRZ data. Typically, RXIN pulses occur at multiples of 400nS, plus or minus 100 nS and still correctly capture and convert the RXIN pulses to NRZ format.

IMPROVED DIAGNOSTICS

The COM90C66 allows the user to better manage the operation of the network through the use of improved diagnostics within the device.

A high level on the My Reconfiguration (MYRECON) bit indicates that the reconfiguration which has just taken place was caused by this particular node. After the Reconfiguration (RECON) bit of the Status Register interrupts the processor, the interrupt service routine will typically read the MYRECON bit of the Diagnostic Status Register. Successive occurrences of a logic "1" on the MYRECON bit indicates that something is wrong with this node. At that point, the transmitter should be disabled so that the entire network is not continuously brought down while the node is being evaluated.

The Receive Activity (RCVACT) bit of the Diagnostic Status Register will be set to a logic "1" whenever a rising edge of NRZ data is detected on the RXIN pin.

The Token Seen (TOKEN) bit of the Diagnostic Status Register will be set to a logic "1" whenever any token has been seen on the network (except

those tokens transmitted by this node).

The RCVACT and TOKEN bits of the Diagnostic Status Register may help the user to troubleshoot the network or the node. If

unusual events are occurring on the network, the user may find it valuable to use the TXOFF bit of the Configuration Register to qualify events. Different combinations indicate different types of problems.

Table 15 - Diagnostic Bits for Troubleshooting Network Activity

RCVACT	TOKEN	TXOFF	DESCRIPTION
NORMAL RESULTS			
1	1	1	The node is not part of the network. The network is operating properly without this node.
1	1	0	The node sees receive activity and sees the token. The basic transmit function is enabled. Network and node are operating properly.
ABNORMAL RESULTS			
1	0	X	The node sees receive activity, but is not seeing the token. Perhaps no other nodes exist on the the network, or some type of data corruption exists, or the media driver is not functioning properly, or the topology is set up incorrectly, or there is noise on the network, or a reconfiguration is occurring.
0	0	0	No receive activity is seen and the basic transmit function is enabled. The transmitter and/or receiver are not functioning properly.
0	0	1	No receive activity is seen and the basic transmit function is disabled. This node is not connected to the network.

In addition to the Diagnostic Status Register bits, the COM90C66 contains two pins for direct connection to LED's. These pins are meant to immediately provide basic visual information on board and network activity with decreased dependence upon software. The COM90C66 contains an internal retriggerable digital one-shot which allows the nTXLED to light for 726 uS +/-10% each time the

COM90C66 transmits information. Every time the host accesses either the internal RAM, registers, or external PROM, the nBSLED will light for 400 mS +/- 20%. The sink capability of both the nTXLED and nBSLED pins is 10mA, thus allowing direct connection to the LED's to be supported by the COM90C66. The only additional components are 500Ω resistors between the LED's and V_{CC}.

OSCILLATOR

The COM90C66 incorporates on-board circuitry which, in conjunction with an external parallel resonant crystal, forms an oscillator. The oscillator frequency may vary from 8 MHz to 20 MHz to allow for a variable data rate from 1.0 Mbps to 2.5 Mbps.

The COM90C66 crystal oscillator has been designed to work with a parallel resonant crystal. Only two capacitors are needed (one from each leg of crystal to ground). The values of the capacitors are two times the lead capacitance of the crystal. The COM90C66 contains an internal $1\text{ M}\Omega$ resistor. The external crystal must have an accuracy of 0.020% or better.

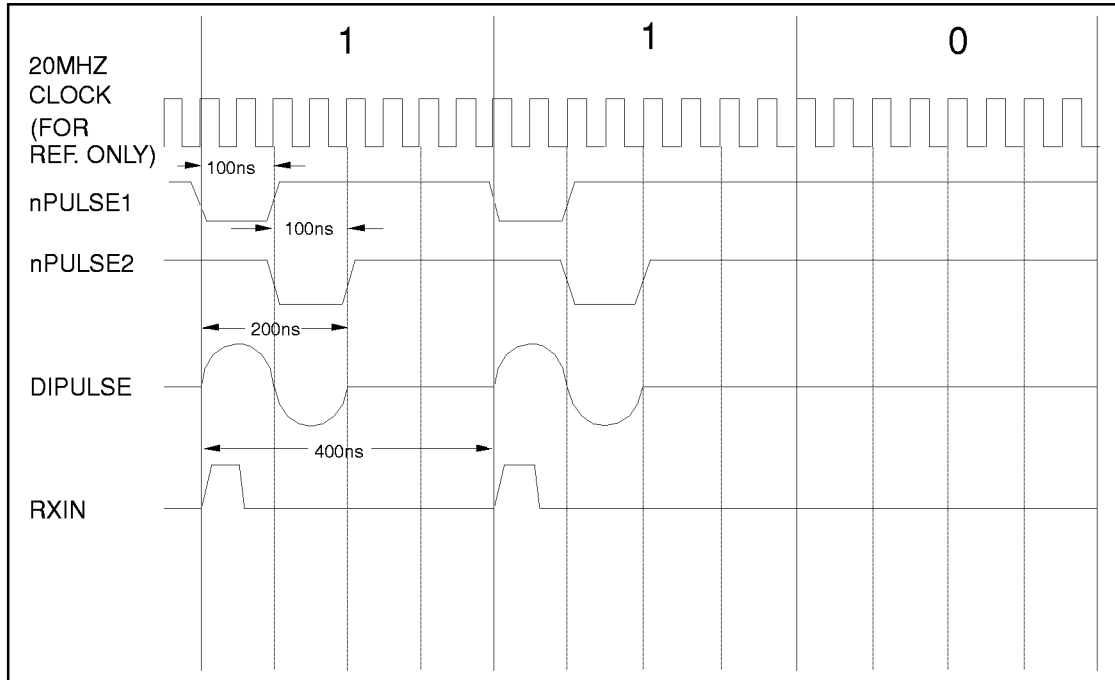


FIGURE 13 - DIPULSE GENERATION AND RECEIVE WAVEFORM FOR DATA OF 1-1-0

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range.....	0°C to +70°C
Storage Temperature Range.....	-55°C to +150°C
Lead Temperature (soldering, 10 seconds).....	+325°C
Positive Voltage on any pin, with respect to ground.....	$V_{CC}+0.3V$
Negative Voltage on any pin, with respect to ground.....	-0.3V
Maximum V_{CC}	+7V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ C$ to $70^\circ C$, $V_{CC} = 5.0V \pm 5\%$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	COMMENTS
Low Input Voltage 1 (All inputs except XTAL1, RESET, AEN, nIOR, nIOW, nMEMR, nMEMW)	V_{IL1}			0.8	V	TTL Levels
High Input Voltage 1 (All inputs except XTAL1, RESET, AEN, nIOR, nIOW, nMEMnR, nMEMW)	V_{IH1}	2.0			V	TTL Levels
Low Input Voltage 2 (XTAL1)	V_{IL2}			1.0	V	TTL Clock Input
High Input Voltage 2 (XTAL1)	V_{IH2}	4.0			V	

DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C , $V_{CC} = 5.0\text{V} \pm 5\%$)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	COMMENTS
Low to High Threshold Input Voltage (RESET, AEN, nIOR, nIOW, nMEMR, nMEMW)	V_{ILH}		1.8		V	Schmitt Trigger, All Values at $V_{DD} = 5\text{V}$
High to Low Threshold Input Voltage (RESET, AEN, nIOR, nIOW, nMEMR, nMEMW)	V_{IHL}		1.2		V	
Low Output Voltage 1 (nPULSE1, nPULSE2, nTOPL, nTOPH, nPROM, CLK, CACLK)	V_{OL1}			0.4	V	$I_{SINK} = 4\text{mA}$
High Output Voltage 1 (nPULSE1, nPULSE2, nTOPL, nTOPH, nPROM, CLK, CACLK)	V_{OH1}	2.4			V	$I_{SOURCE} = -2\text{mA}$
Low Output Voltage 2 (D0-D15)	V_{OL2}			0.4	V	$I_{SINK} = 16\text{mA}$
High Output Voltage 2 (D0-D15)	V_{OH2}	2.4			V	$I_{SOURCE} = -12\text{mA}$
Low Output Voltage 3 (INTR)	V_{OL3}			0.8	V	$I_{SINK} = 24\text{mA}$
High Output Voltage 3 (INTR)	V_{OH3}	2.4			V	$I_{SOURCE} = -10\text{mA}$
Low Output Voltage 4 (IOCHRDY, n0WS, nMEMCS16, nIOCS16)	V_{OL4}			0.5	V	$I_{SINK} = 24\text{mA}$ Open Drain Driversn
Low Output Voltage 5 (nTXLED, nBSLED)	V_{OL5}			0.4	V	$I_{SINK} = 12\text{mA}$
V_{CC} Supply Current	I_{CC1}			20.0	mA	
Input Pull-Up Current	I_P		60		μA	$V_{IN} = 0$ to V_{CC}
Input Leakage Current	I_L	-10.0		+10.0	μA	

CAPACITANCE ($T_A = 25^\circ\text{C}$; $f_C = 1\text{MHz}$; $V_{CC} = 0\text{V}$)

Output and I/O pins capacitive load specified as follows:

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	COMMENTS
Input Capacitance	C_{IN}			5.0	pF	
Output Capacitance 1 (All outputs except IOCHRDY, n0WS, nMEMCS16, nIOCS16, INTR) Output	C_{OUT1}			45	pF	
Capacitance 2 (IOCHRDY, n0WS, nMEMCS16, nIOCS16)	C_{OUT2}			240	pF	
Output Capacitance 3 (INTR)	C_{OUT3}			120	pF	

TIMING DIAGRAMS

The AC parameters in Figures 14-26 are preliminary. Enhancements will follow.

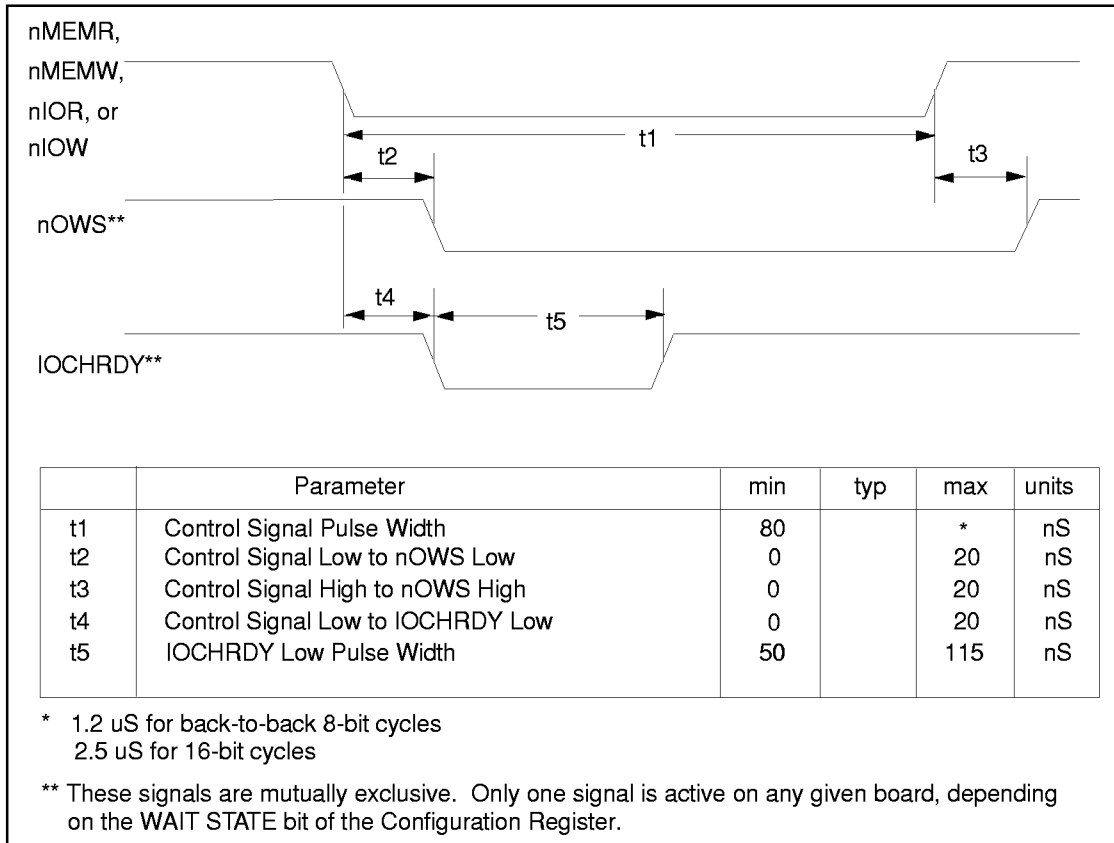


FIGURE 14 - ZERO WAIT STATE AND IOCHRDY TIMING

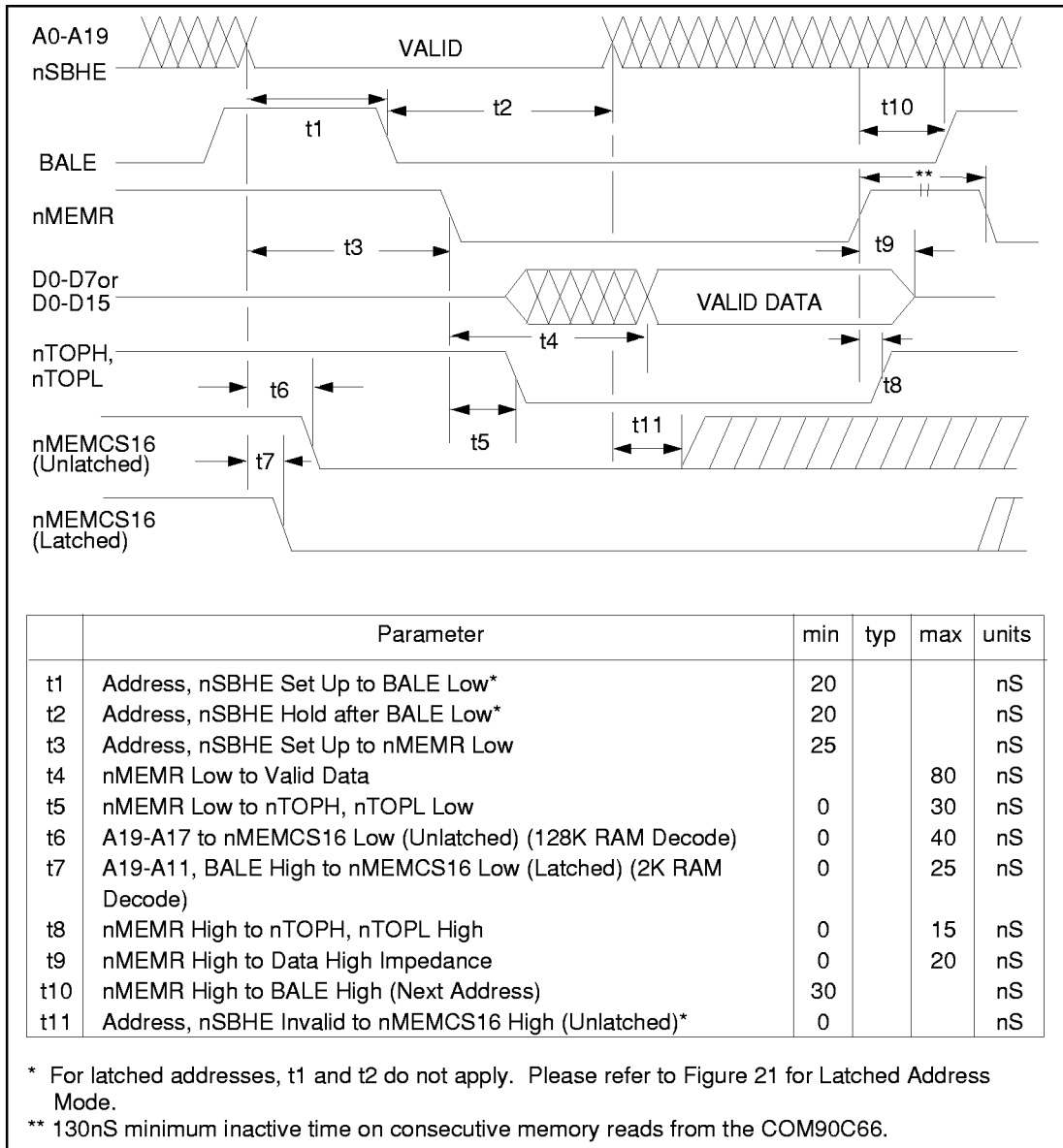


FIGURE 15 - READ RAM CYCLE

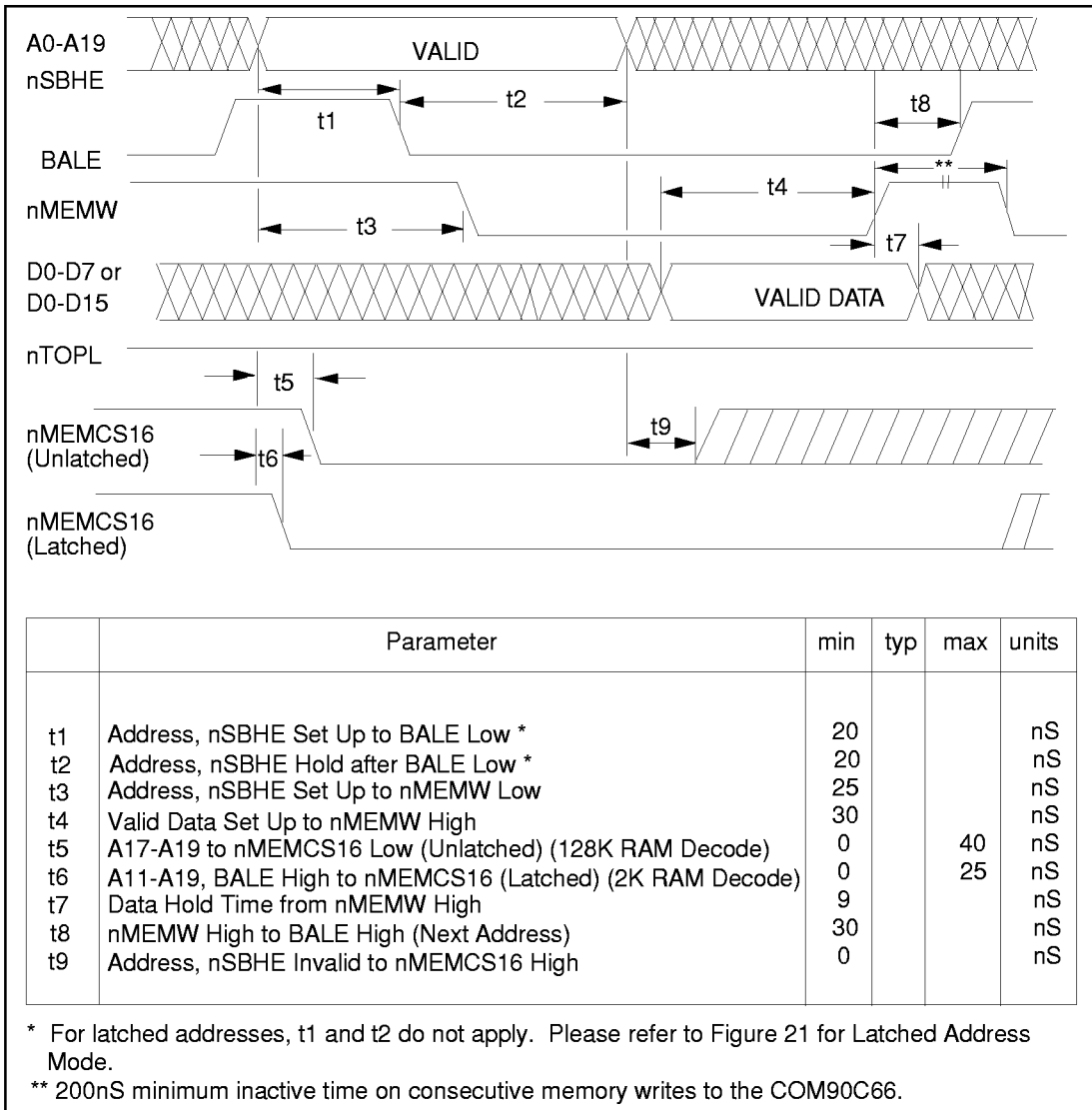


FIGURE 16 - WRITE RAM CYCLE

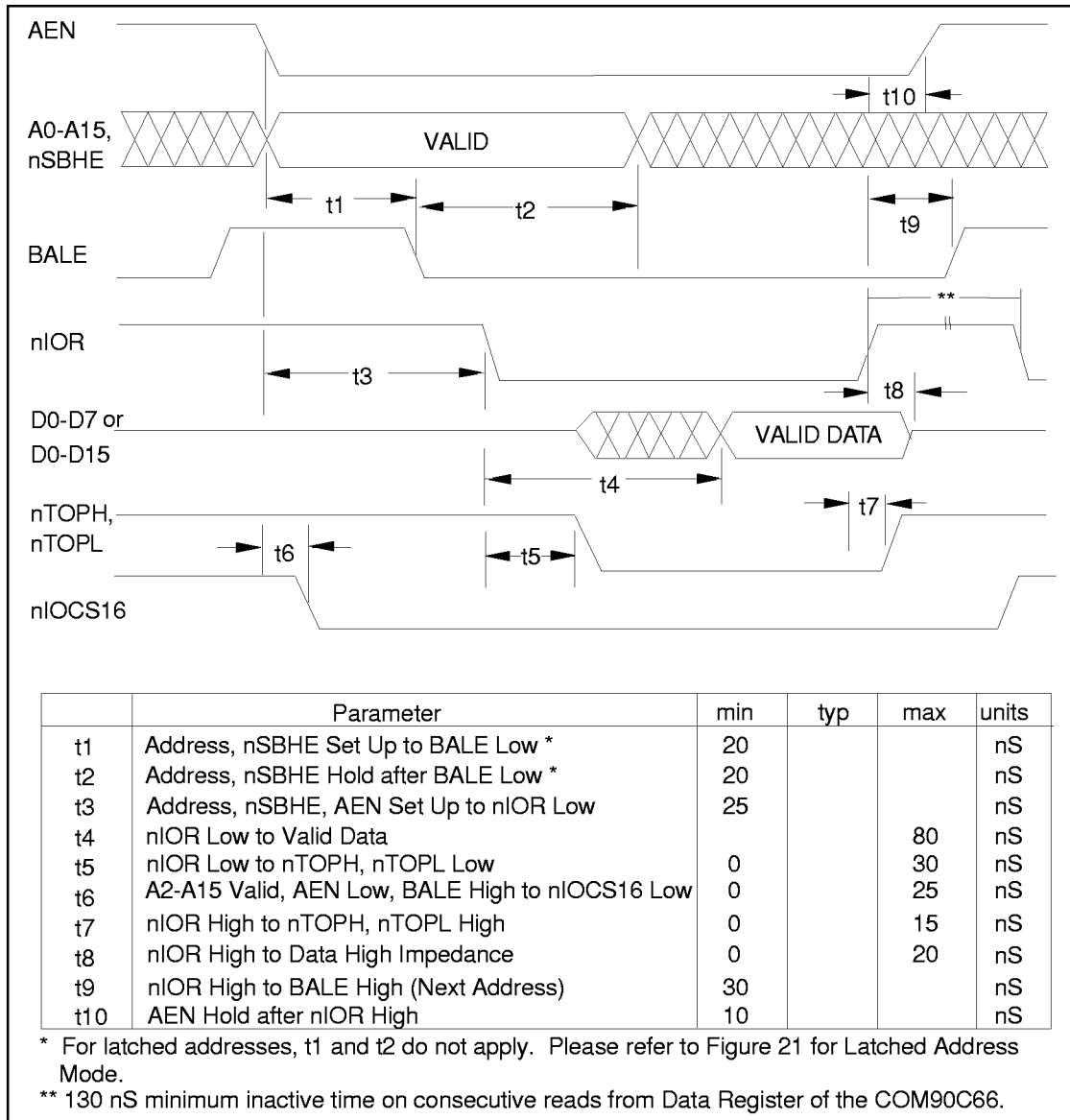


FIGURE 17 - READ I/O CYCLE

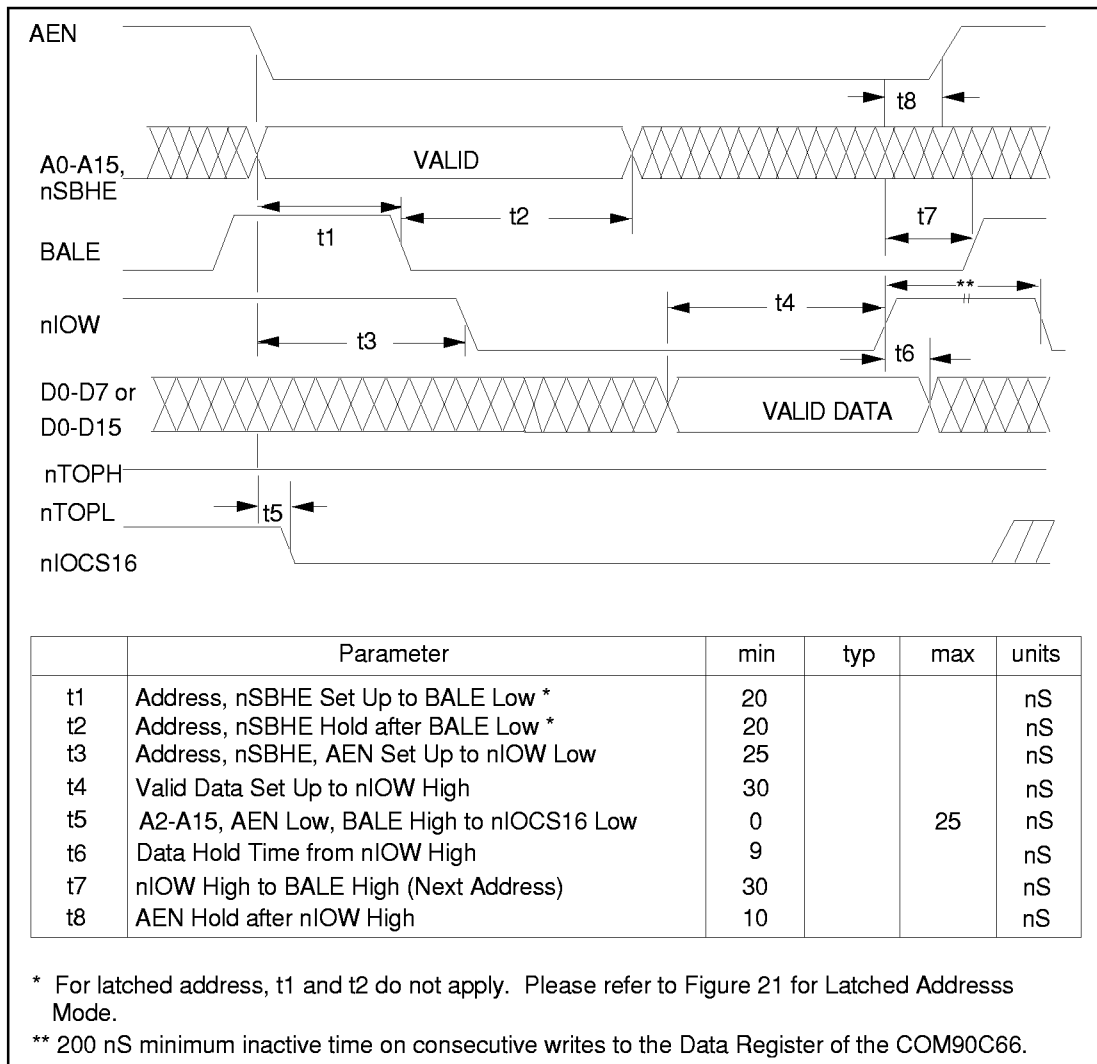


FIGURE 18 - WRITE I/O CYCLE

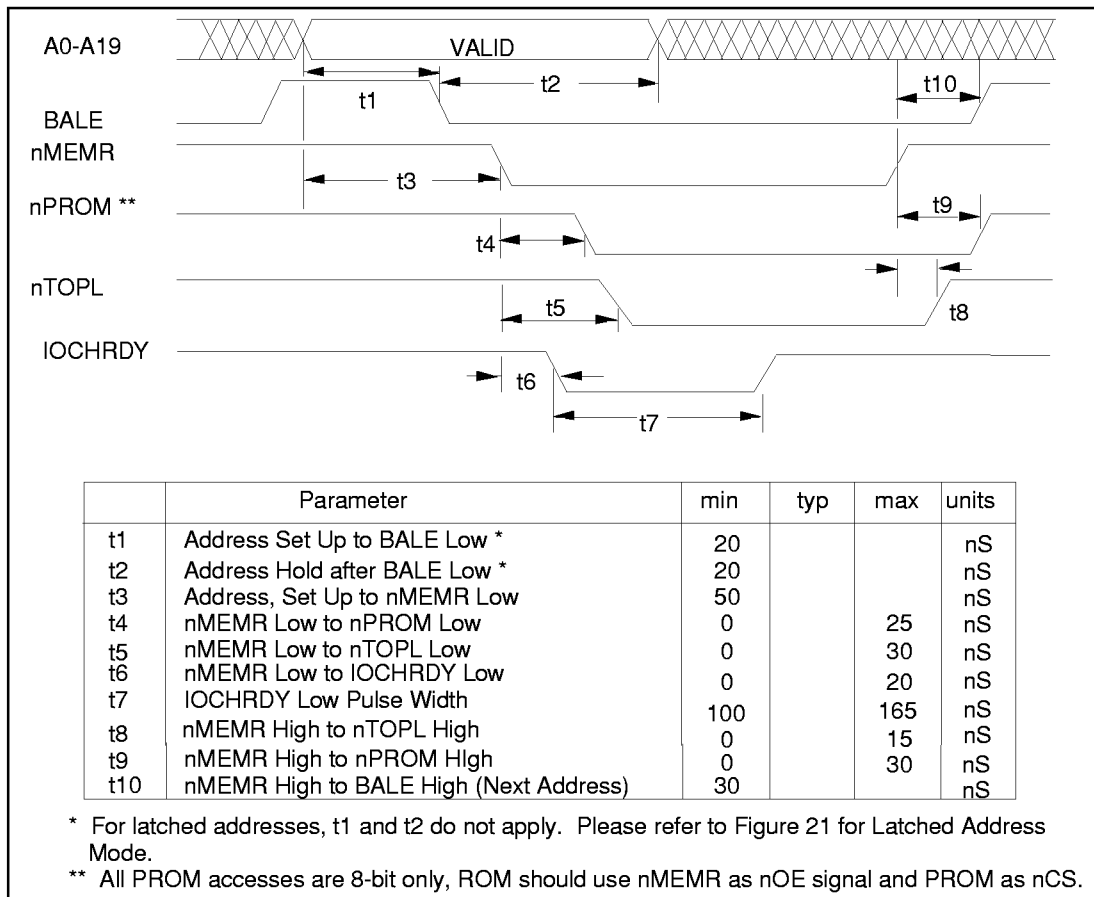


FIGURE 19 - READ PROM CYCLE

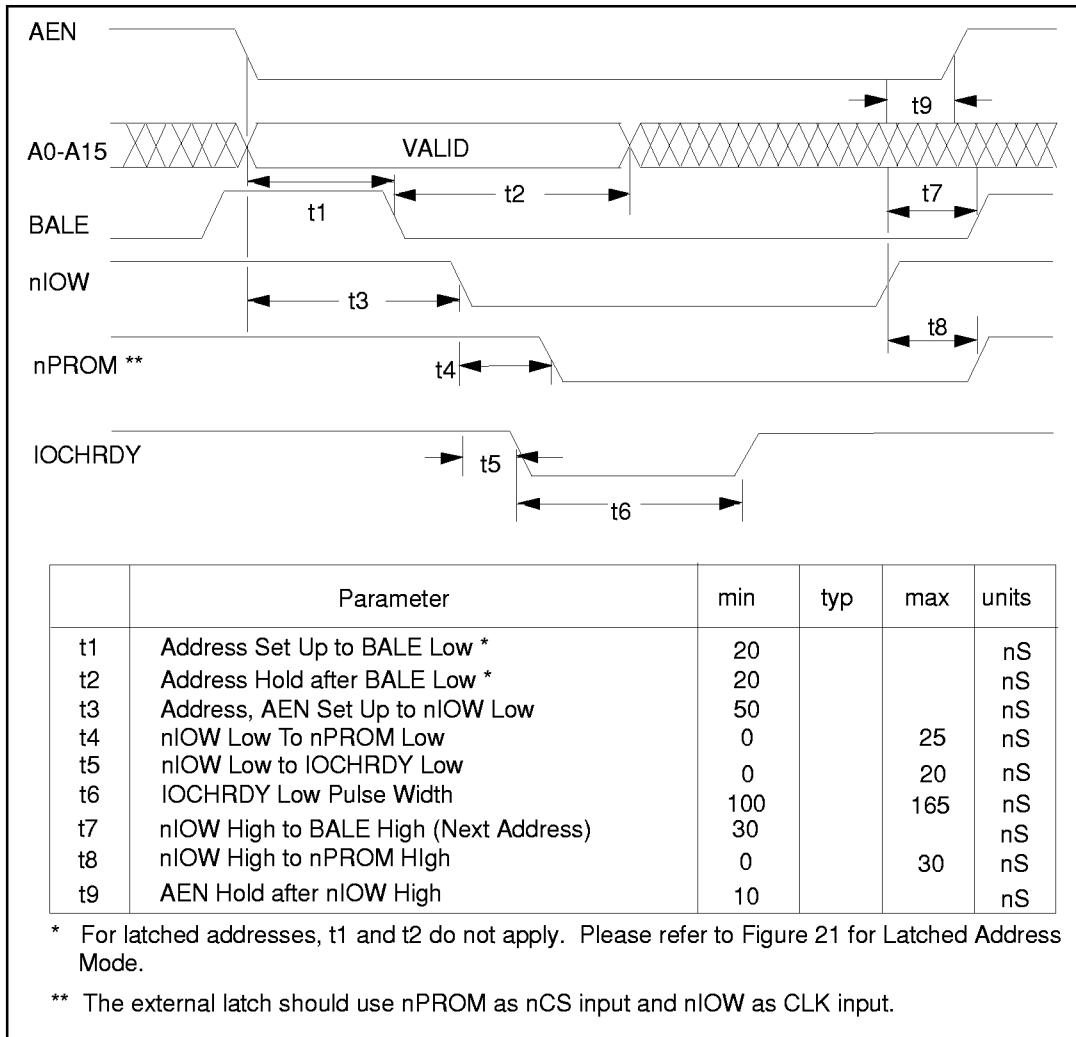


FIGURE 20 - WRITE EXTERNAL REGISTER CYCLE

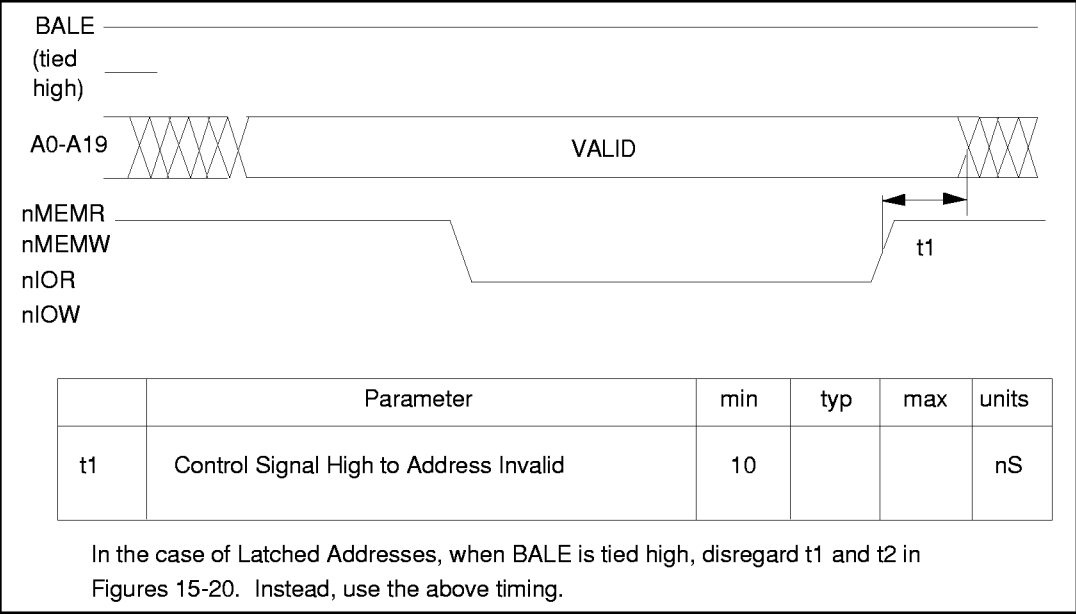


FIGURE 21 - LATCHED ADDRESS MODE

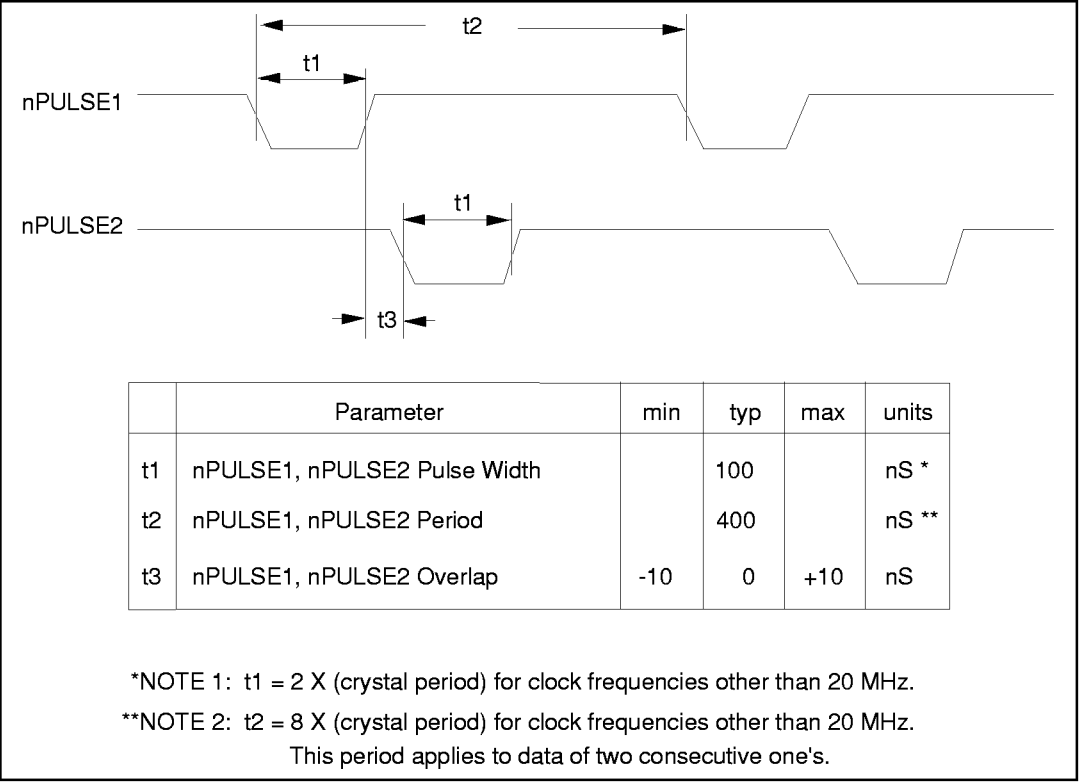


FIGURE 22 - TRANSMIT TIMING

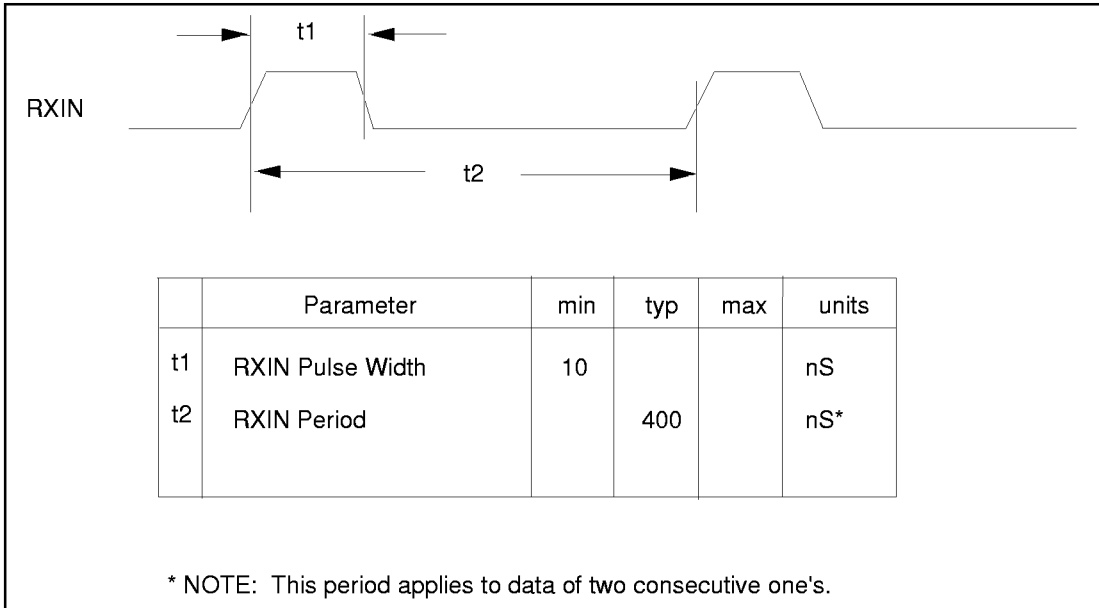


FIGURE 23 - RECEIVE TIMING

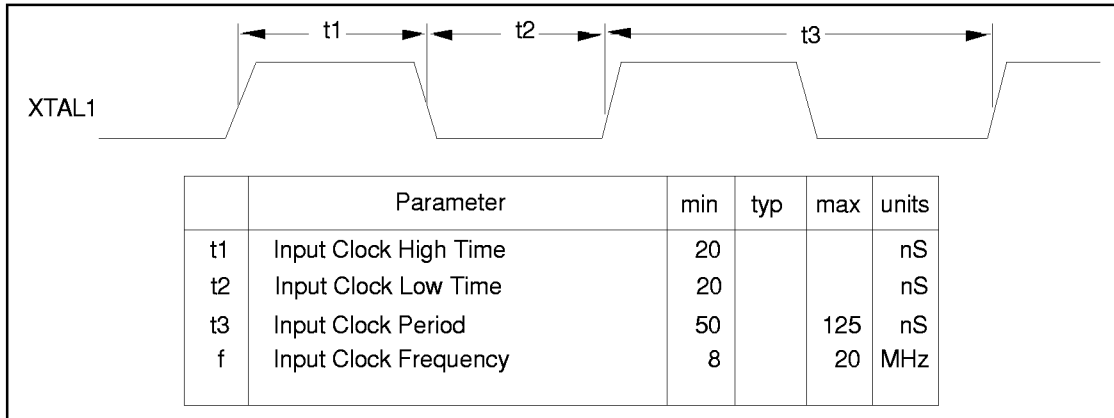


FIGURE 24 – TTL INPUT CLOCK TIMING ON XTAL1 PIN

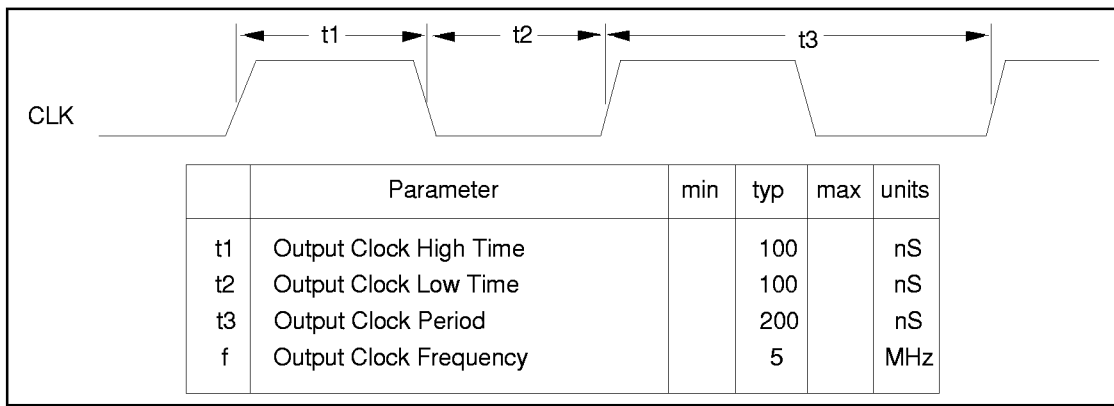


FIGURE 25 - CLK OUTPUT TIMING

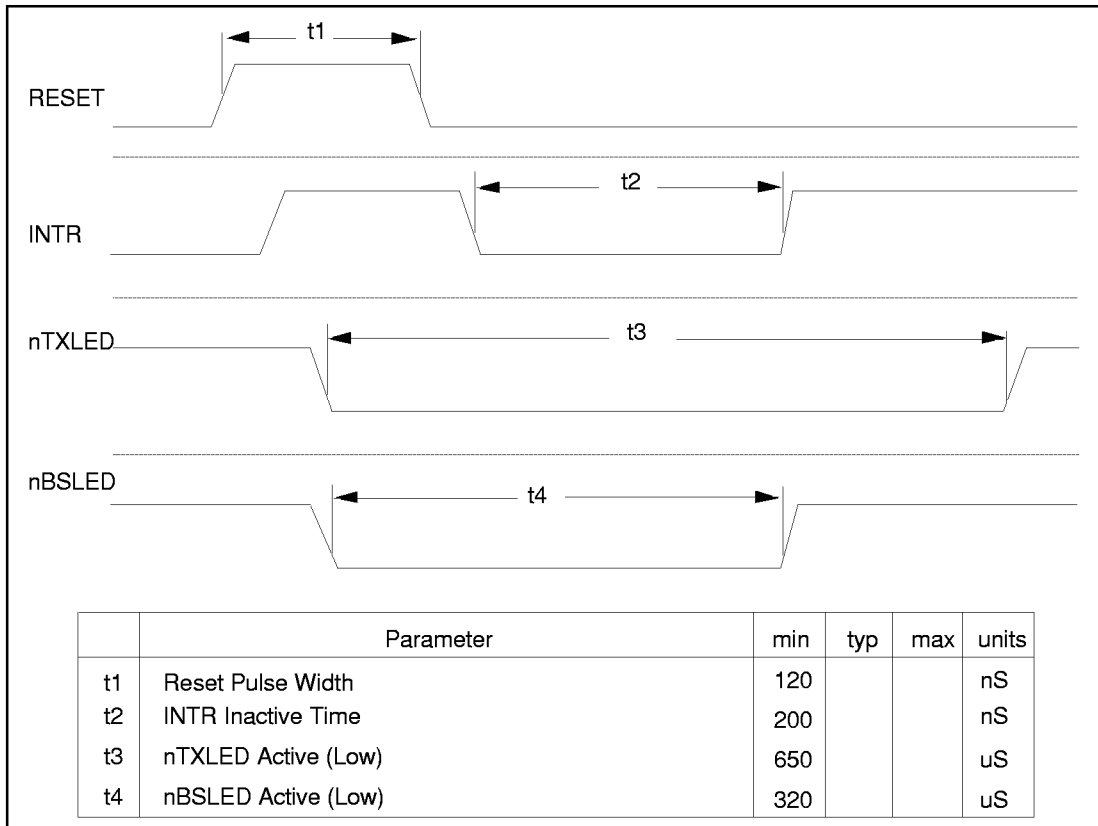


FIGURE 26 - RESET, INTERRUPT, AND LED TIMING

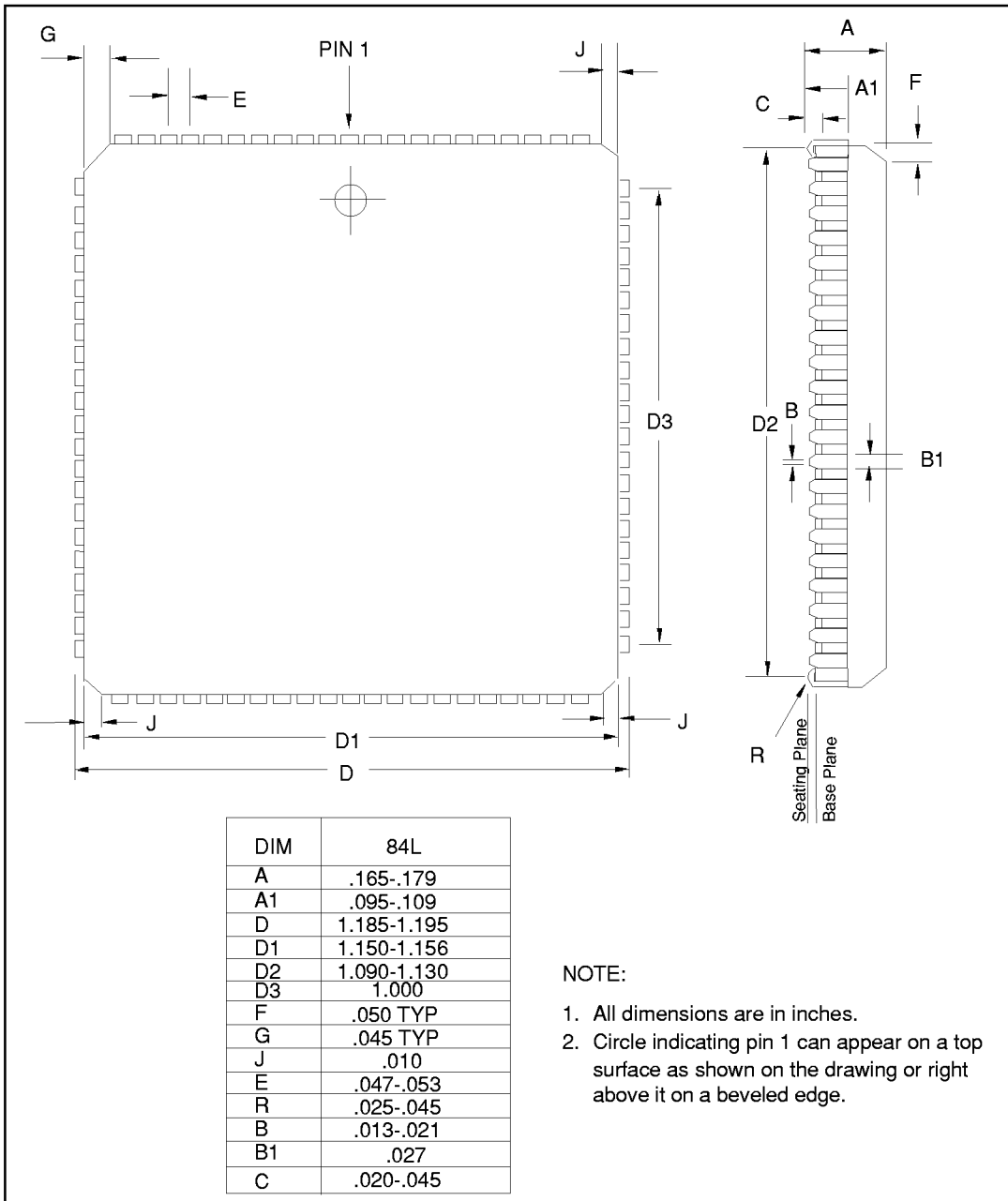


FIGURE 27 - 84-PIN PLCC PACKAGE DIMENSIONS

ADDENDUM 1

DATA SHEET ERRATA FOR REVISION B COM90C66

- The Revision B device does not operate properly in 8-bit mode. Therefore, any reference to 8-bit operation should be disregarded.
- The Revision B device asserts the n0WS signal on any memory read or memory write cycle, not just those associated with the COM90C66. Therefore, the n0WS signal should not be connected and any reference to Zero Wait State operation should be disregarded.
- The Revision B device, when used in Command Chaining Mode, effectively has only one level of status bits. Therefore, disregard any reference to double buffering of the interrupt status bits.
- In the Revision B device, the Decode Mode bit has no effect on the memory mapped decode. Therefore, programming bit 5 of the Configuration Register is ineffective. The nENROM signal must be used alone to control the decode of either 128K or 2K of memory.
- In the Revision B device, when the device is in 16-bit I/O Mapped Mode, byte writes to odd locations overwrites the adjacent even location, therefore, byte writes to odd locations should not be done. It is suggested to perform all writes as word writes, or to temporarily place the device into 8-bit mode (only for this odd byte write) and then switch back to 16-bit mode for subsequent accesses.
- In the Revision B device, the nTXLED active width is only 314 μ sec.

These corrections apply to this data sheet only when used for Revision B of the COM90C66. This COM90C66 revision is identified on the part by the letter "B" preceding the date code.

Specific entries in table format appear on the following page.

DATA SHEET ERRATA FOR REVISION B COM90C66

PAGE	SECTION/FIGURE/ENTRY	CORRECTION
4	Description of Pin Functions - n0WS	Make no connection to this pin.
13	Figure 2 - Bus Interface	16-Bit Interface Signals must always be present. The n0WS signal should be left disconnected.
20,21, 25,37, 39	Tables 3, 4, 8 - Configuration Register Bit 7 (16EN) and Bit 5 (DECODE); Tables 11, 12; Figure 12	Bit 7 (16-Bit Enable) of the Configuration Register must be written to as a logic "1" for proper device operation. Bit 5 of the Configuration Register (Decode Mode) is not effective.
31-33	Command Chaining section	The status bits are only single-level.
34,36	READ AND WRITE CYCLES - Memory vs. I/O Cycles section	In I/O Mapped Mode, packets in the internal RAM buffer must be accessed by addressing one 16-bit I/O location. The device in 16-bit mode increments the pointer by two. The device should not be used in 8-bit mode.
37,40	Wait State Details section; Table 13	The Wait State bit may be written to as a logic "0" to avoid IOCHRDY negation, but the n0WS signal must be left disconnected.
40	8-Bit vs. 16-Bit Accesses section	Disregard references to 8-bit Memory and 8-bit I/O Mapped Mode. All accesses to internal memory should be 16-bit. When the device is in 16-bit I/O Mapped Mode, byte writes to odd locations should not be done.
41	Table 14	8-bit I/O accesses to the Data Register and 8-bit Memory accesses should not be done.
48	Figure 14	Disregard the n0WS timing signal. This signal should not be used.
59	Figure 26	t3 should read 314 µsec minimum.

ADDENDUM 2

DATA SHEET ERRATA FOR REVISION D COM90C66

- The Revision D device contains 16-bit detection circuitry on the input of pin 60 to allow the device to power up in 16-bit mode. If pin 60 senses a low level any time between hardware reset and writing to the Configuration Register, the device defaults to 16-bit mode. If a low level is not sensed on pin 60, the device defaults to 8-bit mode. The mode may be overridden via software, if desired.
- In the generation of the nMEMCS16 signal, the Revision D device decodes the A19-A11 addresses *before* they are latched by the device. The earlier comparison allows the nMEMCS16 signal to be activated and deactivated more quickly by being independent of the BALE signal.
- In the generation of the nIOCS16 signal, the Revision D device decodes the A15-A2 addresses *before* they are latched by the device. The earlier comparison allows the nIOCS16 signal to be activated and deactivated more quickly by being independent of the BALE signal.
- In the Revision D device, when the IOCHRDY signal is negated for internal accesses, it is always negated for two to three XTAL1 clock periods rather than one to two.
- In the Revision D device, the leading edges of the nMEMR and nMEMW signals internally latch the addresses. When the device is used in 8-bit mode, the BALE signal should be tied high. In this case, the 16-bit cycles which get broken into two 8-bit cycles will now be addressed properly for both cycles because the ALE signal is no longer depended upon. Any reference to the requirement of the ALE signal should be disregarded.

These corrections apply to this data sheet only when used for Revision D of the COM90C66. This COM90C66 revision is identified on the part by either the letter "D" preceding the date code or no letter at all preceding the date code.

Specific entries in table format appear on the following pages.

DATA SHEET ERRATA FOR REVISION D COM90C66

PAGE	SECTION/FIGURE/ENTRY	CORRECTION
2,6,13	Pin Configuration - Pin 60; Description of Pin Functions - Pin 60; Figure 2 - System Block Diagram - Pin 60	In Revision D, Pin 60 is not a No Connect, but rather, "n16-Bit Detect". The symbol is "n16DETECT", and the Description should read "Input. When this signal is low any time between hardware reset and writing to the Configuration Register, the device defaults to 16-bit Mode. If a logic "0" is not sensed, the device defaults to 8-bit Mode. The default setting obtained as a result of this input may be overridden via software. This signal is connected to a weak internal pull-up resistor. For a board designed to support both 8- and 16-bit buses, it is recommended that this signal be connected to a signal which is low only in the presence of a 16-bit bus, such as connector D18 of the AT bus (AT ground)."
25	Table 8 - Configuration Register - Bit 7	The last sentence in the Description should read "This bit defaults to a logic "1" (16-bit mode) if Pin 60 senses a low level any time between hardware reset and the writing of the Configuration Register. If a logic "0" is not sensed, bit 7 defaults to a logic "0" (8-bit mode). Writing to the Configuration Register overrides the bus-size default determined by Pin 60."

PAGE	SECTION/FIGURE/ENTRY	CORRECTION
40	8-Bit vs. 16-Bit Accesses	The following paragraph should be inserted after the heading 8-Bit Vs. 16-Bit Accesses : "The COM90C66 defaults to the appropriate bus-width mode when Pin 60 is connected to a signal which is low only in the presence of a 16-bit bus, such as connector D18 of the AT bus (AT ground). If Pin 60 senses a low level, the device defaults to 16-bit mode. If Pin 60 senses a high level (such as when Pin 60 is left disconnected), the device defaults to 8-bit mode. In either case, bit 7 of the Configuration Register automatically reflects the bus-width default. The user may override the default obtained via Pin 60 by writing a new value into bit 7 of the Configuration Register."
39	Figure 12 - nMEMCS16 Generation	For Revision D, the transparent latch and the BALE signal should not appear in Figure 12. The addresses are actually latched by the device for proper addressing, but the nMEMCS16 signal is generated by the addresses which come directly into the device rather than the internally latched version of these addresses.
49,50	Figure 15 - Read RAM Cycle - t7, t11; Figure 16 - Write RAM Cycle - t6, t9	For Revision D, parameters t7 of Figure 15 and t6 of Figure 16 should not reference BALE, but should instead read "A19-A11 to nMEMCS16 Low (Latched) (2K RAM Decode)". Also, parameters t11 of Figure 15 and t9 of Figure 16 should apply to both Latched and Unlatched versions of the nMEMCS16 signal.
39	Figure 12A - nIOCS16 Generation	For Revision D, the transparent latch and the BALE signal should not appear in Figure 12A. The addresses are actually latched by the device for proper addressing, but the nIOCS16 signal is generated by the addresses which come directly into the device rather than the internally latched version of these addresses.
51,52	Figure 17 - Read I/O Cycle - t6; Figure 18 - Write I/O Cycle - t5	For Revision D, t6 of Figure 17 and t5 of Figure 18 should not reference BALE, but should instead read "A2-A15, AEN Low to nIOCS16 Low" Also, parameters should be added for the deactivation of nIOCS16.

PAGE	SECTION/FIGURE/ENTRY	CORRECTION
3	Description of Pin Functions, Pin 53	In Revision D, The nENROM signal does not affect the timing of IOCHRDY.
26	Configuration Register, Bit 2	For Revision D, the second sentence in the Description should read "A logic '1' on this bit negates the IOCHRDY signal for at least two XTAL1 clocks, creating one wait state".
37,40	Wait State Details section; Table 13 - IOCHRDY and n0WS Signal Behavior	For Revision D, the fourth paragraph under Wait State Details should convey that the IOCHRDY signal, when used, is always negated for at least two XTAL1 clocks. There should be no distinction made between RAM, internal register, PROM, and external register cycles. All cycles will negate IOCHRDY for at least two XTAL1 clocks if IOCHRDY is used. The entry in Table 13 which correlates to the IOCHRDY signal when the Wait State Bit=1 should read "Negated for Two to Three XTAL1 Clocks".
48	Figure 14 - Zero Wait State and IOCHRDY Timing	For Revision D, the timing parameter for t5 should be a minimum of 100 nsec, and a maximum of 165 nsec.
3	Description of Pin Functions - Pin 74	For Revision D, the BALE signal is no longer required to latch the unlatched addresses. All addresses are latched by the leading edge of the nMEMR and nMEMW signals for Revision D. BALE must be tied high or left disconnected if the device is placed in 8-bit mode.
4	Description of Pin Functions - Pins 66, 67	For Revision D, the leading edge of these signals automatically latch addresses. If the device is in 8-bit mode, the BALE signal should be tied high or left disconnected, and the nMEMR and nMEMW signals should be responsible for latching the unlatched addresses.
15	Figures 4, 5 - Memory Selector, PROM Selector	For Revision D, Figures 4 and 5 should contain a second Transparent Latch, controlled by the Control Signal. If BALE is tied high or left disconnected, the address is latched by only the second latch-stage, which is controlled only by the nMEMR and nMEMW signals. If BALE is connected to the bus, the address is latched by both the first and second stage latches.

PAGE	SECTION/FIGURE/ENTRY	CORRECTION
49, 50, 53	Figures 15,16,19 - Read RAM Cycle, Write RAM Cycle, Read PROM Cycle	For Revision D, a new timing parameter should exist: Address, SBHE hold after Control Low...20 nsec minimum. This parameter is only required if the BALE signal is tied high or left disconnected.

Modified Version of Pages 16 and 41 for Rev. D COM90C66 Only.

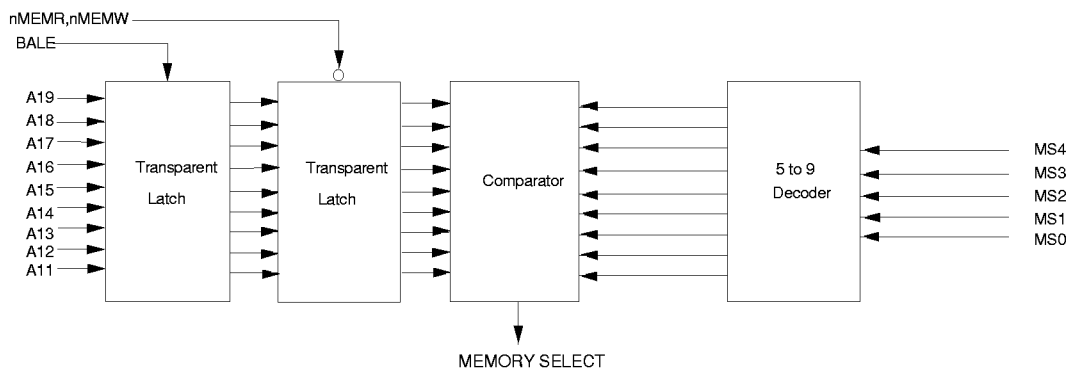
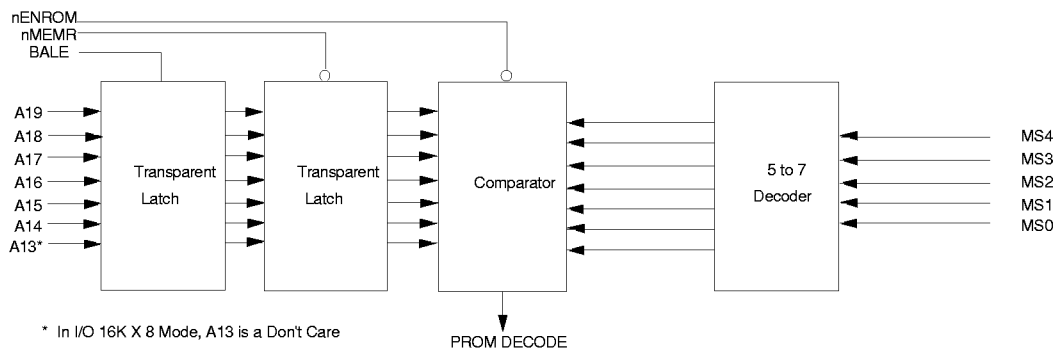


FIGURE 4 - MEMORY SELECTOR



* In I/O 16K X 8 Mode, A13 is a Don't Care

FIGURE 5 - PROM SELECTOR

WAIT STATE BIT	IOCHRDY	nOWS
0	logic "1"	Activated on Access
1	Negated for Two to Three XTAL1 Clocks	logic "1"

TABLE 13 - IOCHRDY and nOWS Signal Behavior

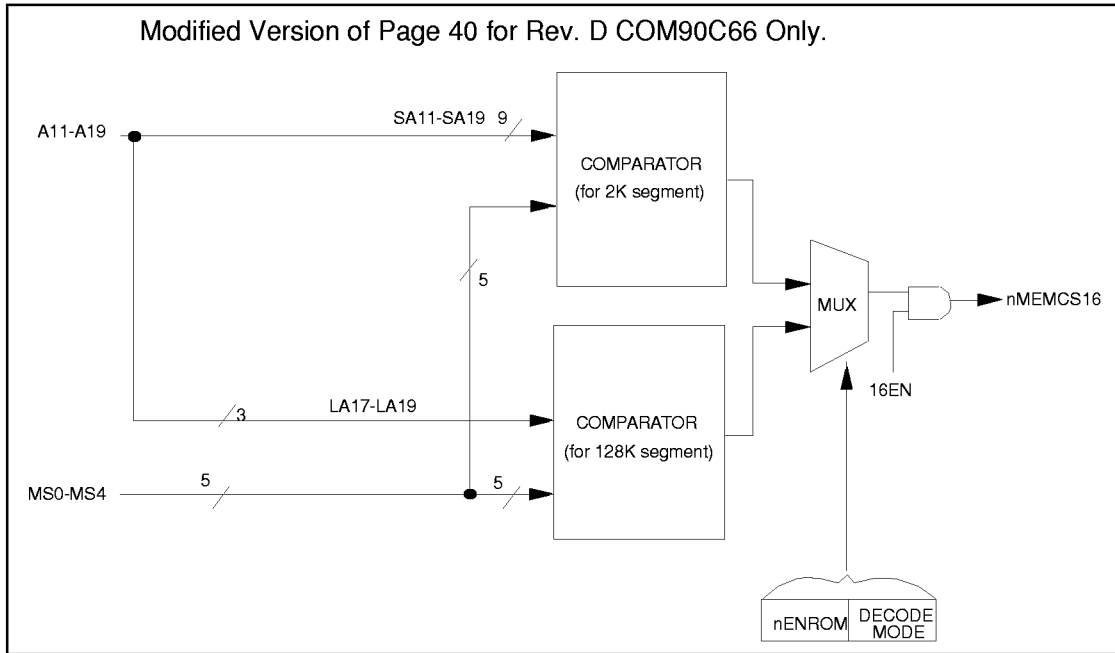


FIGURE 12 – $nMEMCS16$ GENERATION

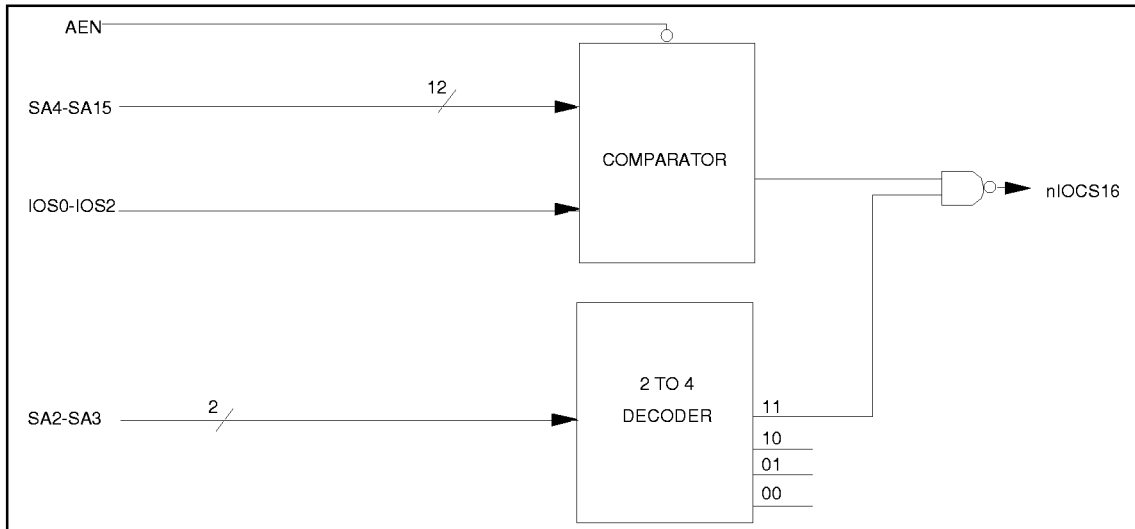
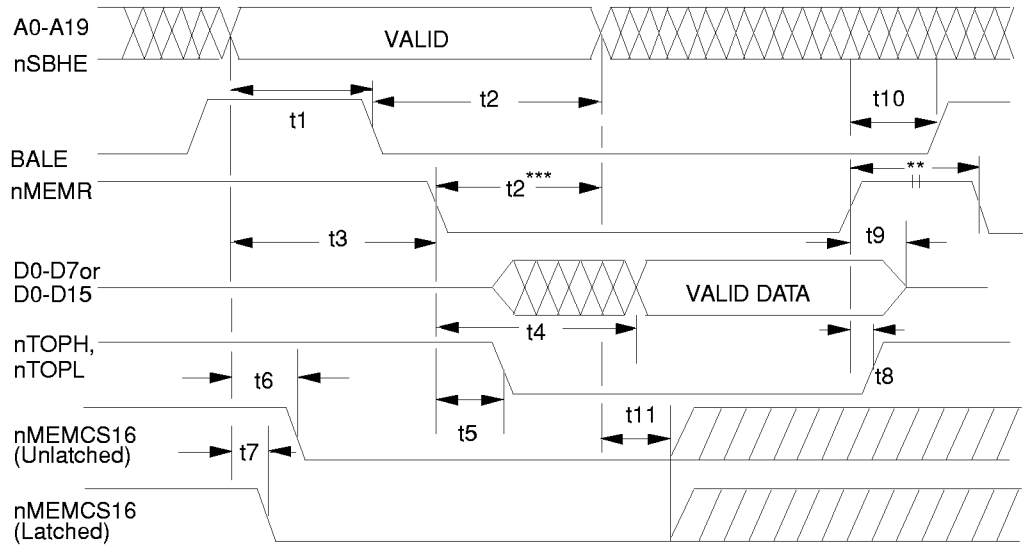


FIGURE 12A - $nIOCS16$ GENERATION

Modified Version of Page 50 for Rev. D COM90C66 Only.



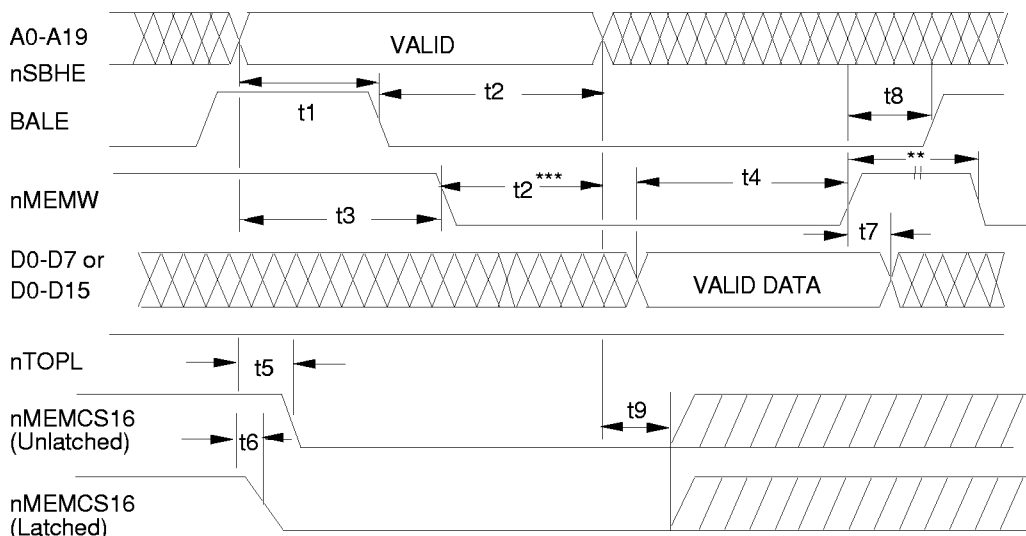
	Parameter	min	typ	max	units
t1	Address, nSBHE Set Up to BALE Low *	20			nS
t2	Address, nSBHE Hold after BALE Low *	20			nS
t3	Address, nSBHE Set Up to nMEMR Low	25			nS
t4	nMEMR Low to Valid Data			80	nS
t5	nMEMR Low to nTOPH, nTOPL Low	0		30	nS
t6	A19-A17 to nMEMCS16 Low (Unlatched) (128K RAM Decode)	0		40	nS
t7	A19-A11 to nMEMCS16 Low (Latched) (2K RAM Decode)	0		25	nS
t8	nMEMR High to nTOPH, nTOPL High	0		15	nS
t9	nMEMR High to Data High Impedance	0		20	nS
t10	nMEMR High to BALE High (Next Address)	30			nS
t11	Address, nSBHE invalid to nMEMCS16 High	0			nS

* For latched addresses, t1 and t2 do not apply. Please refer to Figure 21 for Latched Address Mode

** 130ns minimum inactive time on consecutive memory reads from the COM90C66.

*** For Revision D devices, if BALE is tied high, then Address, nSBHE must be held for 20nsec after nMEMR Low.

FIGURE 15 - READ RAM CYCLE



	Parameter	min	typ	max	units
t1	Address, nSBHE Set Up to BALE Low *	20			nS
t2	Address, nSBHE Hold after BALE Low *	20			nS
t3	Address, nSBHE Set Up to nMEMW Low	25			nS
t4	Valid Data Set Up to nMEMW High	30			nS
t5	A17-A19 to nMEMCS16 Low (Unlatched) (128K RAM Decode)	0		40	nS
t6	A11-A19 to nMEMCS16 (Latched) (2K RAM Decode)	0		25	nS
t7	Data Hold Time from nMEMW High	9			nS
t8	nMEMW High to BALE High (Next Address)	30			nS
t9	Address, nSBHE Invalid to nMEMCS16 High	0			nS

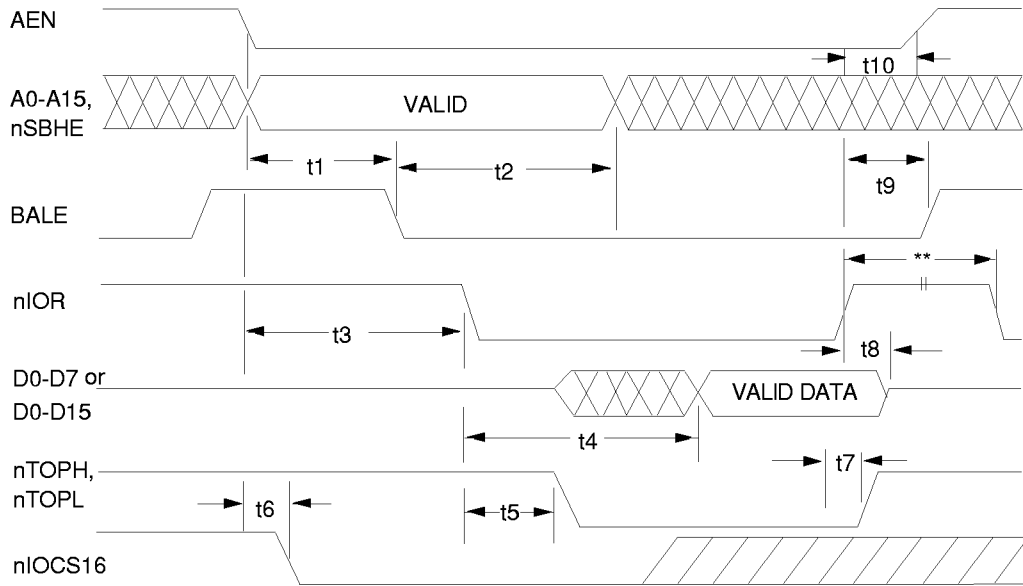
* For latched addresses, t1 and t2 do not apply. Please refer to Figure 21 for Latched Address Mode.

** 200nS minimum inactive time on consecutive memory writes to the COM90C66.

*** For Revision D devices, if BALE is tied high, then Address, nSBHE must be held for 20 nsec after nMEMW Low.

FIGURE 16 - WRITE RAM CYCLE

Modified Version of Page 52 for Rev. D COM90C66 Only.

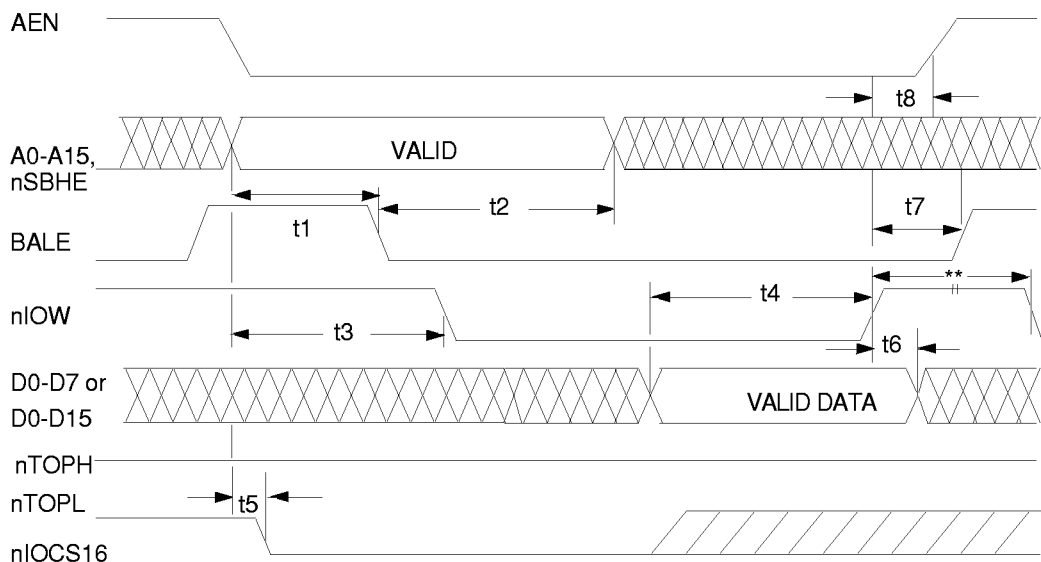


	Parameter	min	typ	max	units
t1	Address, nSBHE Set Up to BALE Low *	20			nS
t2	Address, nSBHE Hold after BALE Low *	20			nS
t3	Address, nSBHE, AEN Set Up to nIOR Low	25			nS
t4	nIOR Low to Valid Data			80	nS
t5	nIOR Low to nTOPH, nTOPL Low	0		30	nS
t6	A2-A15 Valid, AEN Low to nIOCS16 Low	0		25	nS
t7	nIOR High to nTOPH, nTOPL High	0		15	nS
t8	nIOR High to Data High Impedance	0		20	nS
t9	nIOR High to BALE High (Next Address)	30			nS
t10	AEN Hold after nIOR High	10			nS

* For latched addresses, t1 and t2 do not apply. Please refer to Figure 21 for Latched Address Mode.

** 130 nS minimum inactive time on consecutive reads from Data Register of the COM90C66.

FIGURE 17 - READ I/O CYCLE

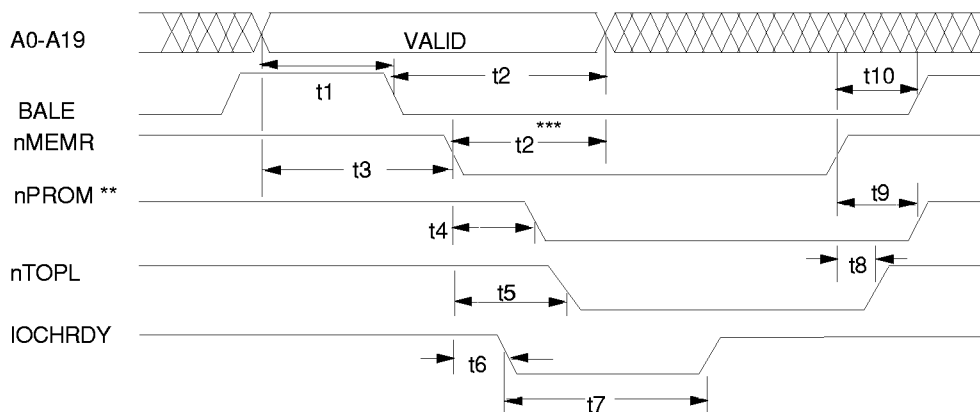


	Parameter	min	typ	max	units
t1	Address, nSBHE Set Up to BALE Low *	20			nS
t2	Address, nSBHE Hold after BALE Low *	20			nS
t3	Address, nSBHE, AEN Set Up to nIOW Low	25			nS
t4	Valid Data Set Up to nIOW High	30			nS
t5	A2-A15, AEN Low to nIOCS16 Low	0		25	nS
t6	Data Hold Time from IOW High	9			nS
t7	nIOW High to BALE High (Next Address)	30			nS
t8	AEN Hold after nIOW High	10			nS

* For latched address, t1 and t2 do not apply. Please refer to Figure 21 for Latched Address Mode.

** 200 nS minimum inactive time on consecutive writes to the Data Register of the COM90C66.

FIGURE 18 - WRITE I/O CYCLE



	Parameter	min	typ	max	units
t1	Address Set Up to BALE Low *	20			nS
t2	Address Hold after BALE Low *	20			nS
t3	Address, Set Up to nMEMR Low	50			nS
t4	nMEMR Low to nPROM Low	0		25	nS
t5	nMEMR Low to nTOPL Low	0		30	nS
t6	nMEMR Low to IOCHRDY Low	0		20	nS
t7	IOCHRDY Low Pulse Width	100		165	nS
t8	nMEMR High to nTOPL High	0		15	nS
t9	nMEMR High to nPROM High	0		30	nS
t10	nMEMR High to BALE High (Next Address)	30			nS

* For latched addresses, t1 and t2 do not apply. Please refer to Figure 21 for Latched Address Mode.

** All PROM accesses are 8-bit only, ROM should use nMEMR as nOE signal and PROM as nCS.

*** For Revision D devices, if BALE is tied high, then Address must be held for 20 nsec after nMEMR Low.

FIGURE 19 - READ PROM CYCLE

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COM90C66 Rev. 09/26/91