Honeywell Series 60, Level 6

MANAGEMENT SUMMARY

The Level 6 series, introduced by Honeywell in January 1976, provides a level of architectural flexibility, modularity, and top down design ideal for custom configurations. The DPS 6 series, Honeywell's newest minicomputer offering (described in Report M11-480-501) builds on the successful Level 6 Megabus structure. The Level 6 and its modular design is a complete departure from the company's earlier minicomputer systems, which were descendants of Computer Control Corporations DDP-116, the first commercial 16-bit system.

The Megabus forms the basis for the Level 6 extreme configurability. The single system bus, although not a new concept, has several design innovations to improve performance. The Megabus itself is completely self-contained with interface logic in every board. Up to 16 processors can be connected to it. The slots on the Megabus are all identical and are not dedicated to specific functions. The Megabus utilizes a split cycle, so that it is released after the data request and is not used until a memory unit seizes it to return the data.

The Level 6 line provides a wide range of capabilities, from the Models 23, 33, 37, 43, 47, and 53 to the 57, the largest in the series. The Model 37 is an interesting new development. Honeywell is using a DPS 6/48 processor in the Level 6 line to provide a commercially-oriented system in the smaller-sized processor range. The model nomenclature reveals the "flavor" of each processor. The Models 23, 33, 43, and 53 are general purpose computer systems while the Models 37, 47, and 57 incorporate ➢

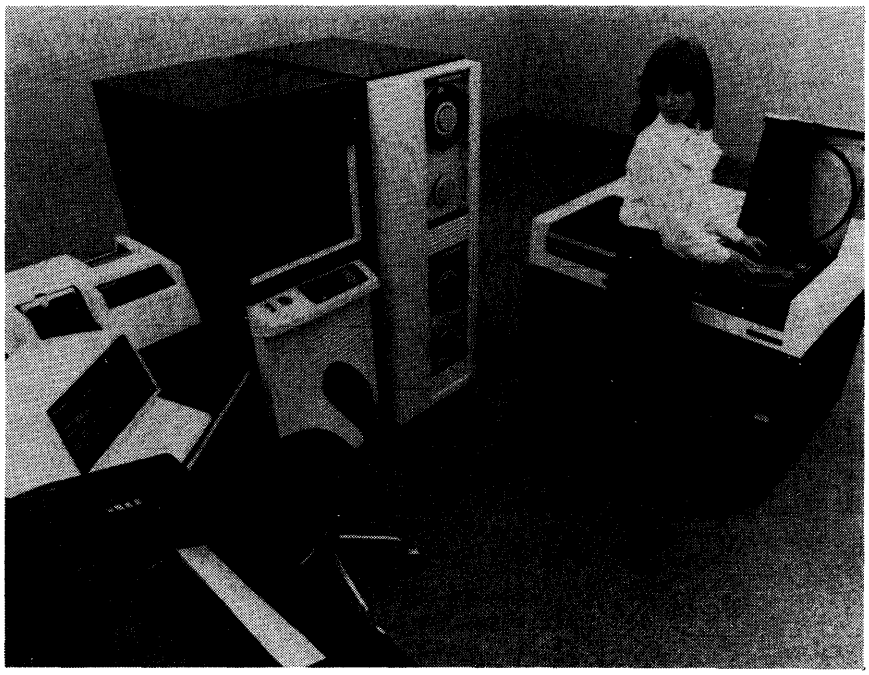
The Level 6 minicomputers provide flexibility in configuration and performance for both OEM and end-users. The microprocessor-based systems offer processing power and open-ended design. Seven processors form the Level 6 product offering: the Model 23 and 33 which are designed primarily for small and medium-size applications; the 43 and 53, more powerful general-purpose processors intended for OEM's, systems houses, and large end users; and the 37, 47, and 57 commercial models, which offer increased commercial throughput to better serve the business community.

MAIN MEMORY: 32K bytes to 2 megabytes
DISK CAPACITY: 10- to 2048-megabytes
WORKSTATIONS: 1 to 64
PRINTERS: 55 cps to 900 lpm
OTHER I/O: Magnetic tape, card reader/punch, flexible diskettes, document handler, and factory data collection terminals.

CHARACTERISTICS

MANUFACTURER: Honeywell Information Systems, Inc., 200 Smith Street, Waltham, Massachusetts 02154. Telephone (617) 895-6000.

Honeywell Information Systems is a division of Honeywell, Incorporated, an international corporation whose products include industrial and residential control systems, sophisticated test instruments for both medical and industrial applications, aircraft guidance systems and instrumentation, photographic equipment, satellite support subsystems, and ➢



The integrated design of Honeywell's Level 6 series is illustrated by the fact that the system shown here could be any one of the six largest members of the family: the Model 33 or Model 37; the Model 43, with 60 percent greater performance than the 33; the Model 47, with seven times the Model 33's COBOL performance; or the cache-equipped Model 53 or Model 57. The Model 57, equipped with a Scientific Instruction Processor, processes both COBOL and FORTRAN programs up to 15 times faster than the Model 33.

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CHARACTERISTICS OF THE HONEYWELL LEVEL 6 SYSTEMS

	Model 23	Model 33	Model 37	Model 43	Model 47	Model 53	Model 57
Memory capacity, bytes: Minimum	32K	32K	32K	32K	32K	32K	32K
Maximum	128K	128K	1024K	2M	2M	2M	2M
Disk capacity, bytes	Up to 320M	10M to 2,048M	10M to 2,048M	10M to 2,048M	10M to 2,048M	10M to 2,048M	10M to 2,048M
Typical register-to-register add time (microseconds)	3.0	1.9	1.2	1.0	1.0	0.8	0.8
Floating point processor*	NA	NA	Optional	Optional	Optional	Optional	Optional
Commercial instruction processor*	NA	NA	Standard	NA	Standard	NA	Standard
Memory management	NA	NA	Standard	Standard	Standard	Standard	Standard
Cache memory	NA	NA	NA	NA	NA	Standard	Standard
Writeable control store	NA	NA	NA	Optioal	Optional	Optional	Optional

*Instructions are trapped for processing if the processor is not installed.

NA—Not Available.

features to enhance COBOL performance for commercial customers.

The Level 6 series and the DPS 6 models complement each other's capabilities. The Level 6 is ideal for those applications requiring a custom configuration. The Megabus allows what the Honeywell engineers describe as an "a la carte configuration" to fine tune a system's performance. The major Level 6 customers tend to be large OEM distributors and sophisticated end-users.

HARDWARE

The Level 6 models use four main processors: Model 23, Model 33, Model 37, and Models 43 through 57. A model number with a leading "5" indicates cache memory and a trailing "7" adds a Commercial Instruction Processor. All employ similar packaging and construction techniques that reduce production costs. All system elements are constructed on 4-level multi-layer PC boards, enabling the CPU to be mounted on one 15-by-16-inch board.

The Model 23 is available in a 5- or 9-slot chassis. Models 33, 37, and 43 are available in 5- or 10-slot chassis (expandable to 23 slots) with either a basic or full control panel, while Models 47, 53, and 57 are available in a 10-slot chassis. The processors all include hardware multiply/divide, a ROM bootstrap loader for three devices, 64 vectored interrupt levels, a real-time clock, and a power supply. The Model 37 provides a commercial instruction processor and memory management unit.

All of the Level 6 systems employ essentially the same internal register organization and instruction sets, allowing software compatibility. The only significant architectural difference is that a synchronous bus is used

electronic data processing products. The parent company is also a leader in solar energy research. Honeywell's computer operations were enhanced by the 1970 merger with General Electric's computer systems division. Honeywell systems are marketed overseas by CII-HB and the International Group of Honeywell. CII-HB serves most of Europe except Italy, most of Latin America south of Mexico, and most Arab and Eastern Bloc countries. The International Group markets primarily in Africa, Asia, Canada, England, and Mexico. The company currently employs about 100,000 persons worldwide.

MODELS: Series 60, Level 6, Models 23, 33, 37, 43, 47, 53, and 57.

DATE ANNOUNCED: Model 33, January 1976; Model 43, January 1977; Models 47 and 53, January 1978; Models 23 and 57, June 1978; Model 37, January 1981.

DATE OF FIRST DELIVERY: Model 33, January 1976; Model 43, January 1977; Models 47 and 53, January 1978; Models 23 and 57, June 1978; Model 37, January 1981.

NUMBER INSTALLED TO DATE: Over 12,000 as of end of 1980.

DATA FORMATS

BASIC UNIT: 16-bit word.

FIXED-POINT OPERANDS: Signed 15-bit single-precision or signed 31-bit double-precision operands. Byte and bit operands are also possible. In both single- and double-precision operands, the high-order bit of the first word is the sign bit. Signed data is always in two's-complement notation. Ranges for signed double words, signed words, signed bytes, unsigned words, and unsigned bytes are, respectively, + about 2 billion, -32,768 to 32,767, -128 to 127, 0 to 65,535, and 0 to 255.

FLOATING-POINT OPERANDS: In the Models 23 and 33, floating-point arithmetic is available only through software routines. Single-precision operands include a 7-bit

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	PERIPHERALS/TERMINALS	
DEVICE	**DESCRIPTION & SPEED**	**MANUFACTURER**
MAGNETIC TAPE EQUIPMENT		
MTU9104	Industry-compatible, 9-track, 45 ips, 800 bpi, NRZI tape drive; 10.5-reels; requires MTC9101 Controller and MTM9102 Device Pac for up to four drives; 36 KBS	STC
MTU9105	Same as MTU9104 but 75 ips with dual vacuum columns; 60 KBS	STC
MTU9112	Industry-compatible, 7-track, 45 ips, 556/800 bpi, NRZI tape drive; 10.5-inch reels; requires MTC9101 Controller and MTM9101 Device Pac for up to four drives; 25/36 KBS	STC
MTU9113	Same as MTU9112 but 75 ips with dual vacuum columns; 41.7/60 KBS	STC
MTU9109/10	Industry-compatible, 9-track, 45/75 ips, 800/1600 bpi, NRZI/PE; 10.5-reels, requires MTC9102 controller and MTM9102 Device Pac for up to four drives; 36/72 KBS	STC
MTU9114/5	Same as MTU9109/10 except 1600 bpi only	STC
PRINTERS		
PRT1004	Letter quality printer, 55 cps, 128-character set, bidirectional	Honeywell
PRU1001/1003	Serial printer, receive only, 30 cps, 64-character buffer	Honeywell
PRU1005	Serial printer, receive only, 120 cps, 1200-character buffer	Honeywell
PRU9617	Band printer, 300 lpm, 64-character set, 132-col, vertical format unit, built-in diagnostics	Dataproducts
PRU9618	Band printer, 600 lpm, 64-character set, 132 col, vertical format unit, built-in diagnostics	Dataproducts
PRU910	Line, drum, 132 positions, 64 ASCII character set optional, 10 characters per inch, 4 to 19-inch paper, 6 or 8 lines per inch; 900 lpm, built-in diagnostics	Dataproducts
PRU9112	Serial, 9 x 7 dot matrix, 132 positions, 64 ASCII character set, 10 characters per inch, 6 lines per inch, 4 to 15-inch paper, 2-channel VFU, 120 characters per second	Honeywell
PRU9114	Same as 9112 except 7 x 7 dot matrix, bidirectional, 160 cps	Honeywell
PUNCHED CARD EQUIPMENT		
CRU9107	Reader, 80-column punched cards, 1000-card input hopper and output stacker; 1050 cpm	Honeywell
CRU9111	Reader, 80-column punched cards, 1000-card input hopper and output stacker; 500 cpm	CII-Honeywell Bull
CRU9112	Reader, mark sense, IBM-mode, up to 40 mark sense columns on an 80-column card; 1000-card input and output stacker; 500 cpm	CII-Honeywell Bull
PCU9101	Punch, 80-column punched cards; 100 to 400 cpm	Honeywell
CCU9101	Reader/punch; 80-column cards; 400/100 cpm	Honeywell

in the Model 23 instead of the standard Level 6 Megabus. The 23's performance level is approximately 60 percent of the Model 33's. Relative to the Model 33, the Model 37 has 1.3 times the basic performance and five times the commercial performance capabilities. The overall performance of the Models 43 and 47 is 1.6 times greater than that of the 33, and the overall performance of the 53 and 57 is 2.3 times greater. In commercial performance, the rated throughput is 7 and 15 times greater, respectively, for the Models 47 and 57. The Scientific Instruction Processor increases the scientific performance of the Model 43 and larger models by up to 15 times.

The Level 6 peripheral and communications controllers are also microprocessor-based, permitting unusually powerful systems, especially in communications applications.

The memory management option divides the first 128K bytes of memory into 16 8K-byte segments. The remaining memory is divided into 15 128K-byte segments.

exponent and a 24-bit fraction plus the sign of the fraction. Double-precision operands have a 56-bit fraction formed by adding two words to the single-precision format. In both single- and double-precision formats, the 7 most significant bits of the first word form the exponent expressed in excess-64 notation. Following the exponent is the 1-bit fraction sign field and the fraction.

The larger models perform floating-point arithmetic by using either the scientific instruction processor (SIP) or software simulation as described for the Models 23 and 33. Formats for SIP and floating-point software simulation are the same.

INSTRUCTIONS: Level 6 instructions are predominantly 16 or 32 bits in length, depending on the addressing mode employed. A 48-bit format is used for double-precision immediate-operand instructions. All instructions, except generic types, have a one-bit control field (bit 0), a three-bit register designator (bits 1 through 3), and a four- or five-bit op code (bits 4 through 7 or 8). The use of the remaining seven or eight bits varies with the type of instruction. Branch instructions have a seven-bit displacement field (126 locations; displacements of 0 and 1 have special significance). Shift instructions have eight bits to

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PERIPHERALS/TERMINALS (Continued)

DEVICE	DESCRIPTION & SPEED	MANUFACTURER
TERMINALS		
DKU9101	CRT display/keyboard; 960 characters, 12 lines of 80 characters, 64 ASCII character set, audible alarm, 60-key keyboard with shift, RS-232-C interface for printer; selectable data rates of 110 to 9600 bps	Honeywell
DKU9102	CRT display/keyboard; 960 characters, 12 lines of 80 characters, 95 ASCII character set, audible alarm, 60-key keyboard with shift, RS-232-C interface for printer; selectable data rates of 110 to 9600 bps	Honeywell
DKU9103	CRT display/keyboard; 1920 characters, 24 lines of 80 characters, 64 ASCII character set, 86-key keyboard, page buffer	Honeywell
DKU9104	Same as DKU9103 except 96 ASCII character set	Honeywell
VIP7700R	Synchronous CRT, 64-character set	Honeywell
VIP7705R	Synchronus CRT, 96-character set	Honeywell
TWU9104/08	Keyboard typewriter console; serial, 7 x 9 dot matrix, 132 positions, 10 characters per inch, 6 lines per inch, 96 ASCII character set, 4 to 15 inch paper, 60-key keyboard; 30 cps; 08 adds numeric keypad	Honeywell
TWU9106/10	Same as TWU9104 but 120 cps; 10 adds numeric keypad	Honeywell
VIP7801	CRT display/keyboard; 1920 characters, 24 lines of 80 characters; 139 ASCII character set, status line, detachable 108-key typewriter keyboard, 12-inch screen, 20-mA current loop interface, 7 x 9 dot matrix, transmission at 9600 bps	Honeywell
VIP7802	Same as VIP7801 but with a 15-inch screen	Honeywell
VIP7803	Same as VIP7801 but with special word processing character set and key board	Honeywell
VIP7804	Synchronous version of VIP7801	Honeywell
VIP7805	Synchronus version of VIP7802	Honeywell
VIP7207	CRT display/keyboard; 1920 characters, 24 lines of 80 characters, 128 ASCII character set, detachable 86-key data entry keyboard, 12-inch screen, 20-mA current loop interface, transmission at 9600 bps, customized for use with Data Entry Facility-II software	Honeywell

Virtual addresses in each segment are the automatically relocated to physical segments, each of which has its own read-write-execute protection level. Four levels of protection are available, based on level of privilege. The unit also provides descriptor validation. Memory management is not field-installable.

The Scientific Instruction Processor (SIP) is designed for number crunching; it plugs into the Megabus and contains three double-precision registers. The SIP allows single- and double-precision floating-point arithmetic plus automatic conversion of non-floating-point integer operands. Both single- and double-word integer operands can be operated upon. The SIP allows FORTRAN programs to run three times faster on the Model 43 than on the 33.

The Models 23 and 33 have 108 standard instructions, while the 43 and 53 each have 124 and the 37, 47, and 57 have 154. These instruction sets are designed to operate on bits, bytes, words, and multiple words; they are expandable through several addressing modes. The Scientific Instruction Processor augments the Model 43 and 53 instruction sets with 30 additional instructions.

The Model 33 and larger systems are built up through connections to the Megabus, a central high-speed asynchronous bus that is capable of more than 3 million 16-bit transfers per second. All system elements—CPU's, memories, peripheral controllers, etc.—communicate through the Megabus and are generally independent of each other. The Megabus has separate address and data paths. A 24-bit-wide address space for up to 1024

designate the shift count. Short-value immediate instructions use bits 8 through 15 to specify immediate operands with values between -128 and +127. Memory reference instructions use bits 9 through 15 as the "address syllable," which consists of a three-bit addressing mode selector, an indirect bit, and a three-bit index register designator.

Generic instructions consist of an eight-bit op code (8 zeroes) and an eight-bit function code.

Software simulation of the scientific instruction set is accomplished via two trap handlers: the floating-point simulator, entered via trap vector number three, and the scientific branch simulator, entered via trap vector number five.

The optional scientific instruction processor (SIP) adds two types of instructions to the basic instruction set. Both of these types, the floating-point arithmetic instructions and the scientific branch instructions, are 16 or 32 bits in length, depending on the addressing mode utilized. The first 16 bits of the floating-point arithmetic instructions employs bits 4 through 8 as the op code and bits 9 through 15 as the address symbol. The first 16 bits of the scientific branch instructions is composed of four fields: field one, consisting of bits 0 and 1; field two, consisting of bits 2 and 3; field three, the 5-bit op-code; and field four, the 7-bit address displacement. If needed, a second 16 bits may be added for absolute addressing or address displacement.

INTERNAL CODE: ASCII.

MAIN STORAGE

TYPE: 16K-chip MOS RAM; the chips employ N-channel, silicon-gate technology.

CYCLE TIME: 550 nanosecond cycle time with an access time of 300 nanoseconds.

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channels (512 in and 512 out) is provided, although the Megabus is electrically limited to 23 boards at present. Circuitry has been included in each Level 6 processor to enable up to 16 CPU's to share common memory, with each processor having its own reserved area in memory.

The NMOS memories now used in Level 6 processors have a cycle time of 550 nanoseconds. The semiconductor memory is built from 16K NMOS dynamic RAM's mounted on 256K-byte boards. These modules are mounted in piggyback fashion on memory controller boards to form 2048K-byte memories. These memories are switch-selectable to provide either a single-word or double-word fetch. A two-way interleaved NMOS memory capable of a double-word fetch is available for the 37 and larger models. Double fetch operation requires that memory size be a multiple of 128K bytes.

Memory parity checking (two bits per word) is available for all Level 6 processors. In addition, 22-bit error detecting and correcting (EDAC) memories are offered that append a 6-bit Hamming code to each data word, enabling the controller to automatically correct any one-bit error without a system interruption. Multiple-bit errors, however, are not recoverable, and a trap procedure is initiated for these.

The Model 23 represents a basic minicomputer system intended for use in small dedicated systems, such as data entry, or for distributed processing with Honeywell host systems or other mainframes using IBM protocols. It is limited to 128K bytes of parity memory and is sold as either an execute-only or program development system.

The Model 33 is intended for use in larger OEM systems and also for the end-user market. This model is offered in a 5-slot or 10-slot chassis. Maximum memory for the 33 is 128K bytes of either parity or error-correcting (EDAC) memory, and the 33 is expandable to 23 Megabus slots. The Model 33 is similar to the older 6/36 but uses the Model 53 power supplies and console, as do all of the new Level 6 processors. The Model 33 offers a choice of parity or error detection and correction (EDAC) single-fetch memories.

Honeywell has aimed the Model 23 and 33 at applications currently employing competitive minicomputers such as the Hewlett-Packard 1000 series, the Data General Nova series, the Interdata 6/16 and 7/16, the Texas Instruments 990/10, and the DEC PDP-11/03 through PDP-11/45.

The faster logic of the Model 43 results in a 60 percent performance increase over the Model 33. Options for the Model 43 include either a full or base control panel, single- or double-fetch NMOS memory (32K to 2048K bytes), and a scientific instruction processor (SIP). Memory management and a watch-dog timer are standard. The Model 43 has 124 standard instructions. Commercial instructions (30) are always trapped; if the SIP is not installed, scientific instructions (30) are also trapped.

CAPACITY: Level 6 high-density memory, based on 16K chips, contains 256 bytes per board. The Model 23 can have one memory controller board (65,536 bytes), while the Model 33 can have up to two such boards (131,072 bytes). Models 37, 43, 47, 53, and 57 can address up to 2,097,152 bytes of memory and can have as many controllers as there are slots available on the bus.

CHECKING: One parity bit per byte is standard, and 22-bit EDAC memories are available as options for Models 33 and 43. EDAC memories employ a 6-bit Hamming code to detect and correct all internally caused single-bit errors and detect all double-bit errors.

With both EDAC and parity memory, address parity accompanies the most significant eight bits on the address bus. When memory detects an error on these bits, it does not respond; the result is a bus timeout. Each device controller/communication processor on the Megabus checks parity on information received from the Megabus and indicates an error by setting a parity error status bit.

STORAGE PROTECTION: None on the Model 23 or 33.

To facilitate multi-user systems, the Model 37 and larger central processors accommodate a standard memory management unit (MMU) that permits the allocation and assignment of memory among several users. The MMU divides the first 128K bytes of memory into 168K segments for short-form addresses on a modulo-256 basis, and the remaining memory (up to 2 million bytes) into 15 128K segments using long-form addresses. Virtual addresses in each segment are then automatically relocated to physical segments, each of which has its own read-write-execute protection level.

Protection is based on a six-bit descriptor employing two bits for read, two bits for write, and two bits for execute protection. Four levels of protection, numbered 0 through 3, are available, allowing read, write or execute access only if priority is greater than or equal to current priority. A hardware context save/restore facility automatically loads a new descriptor map at context switching time from an area reserved for this purpose. The unit also provides base relocation and descriptor validation.

RESERVED STORAGE: The first 256 locations are reserved for use by hardware. Among the 256 locations are 4 locations used by the real-time clock and watchdog timer, 4 locations for interrupt mask storage, 92 locations for trap vectors, and 64 locations for interrupt vectors, each of which points to a specific interrupt save area with its starting address of the interrupt subroutine and register storage area. The remainder are reserved for present and future system software usage.

Traps are caused by events such as overflows, parity errors, addressing nonexistent resources, or executing a scientific instruction if the SIP is not installed. A trap can occur at any priority level, and several can be nested at the same level. A trap could be entered at one level, that level interrupted during the execution of the trap routine, and then the same trap routine re-entered in the new level.

Each type of trap has its own trap vector containing a pointer to the trap-handler procedure. Also utilized is a pointer to the next available trap save area. The latter are pooled, and pointers to the next available area are automatically adjusted by firmware. When a trap occurs, some, but not all, register contents are automatically stored in the trap save area.

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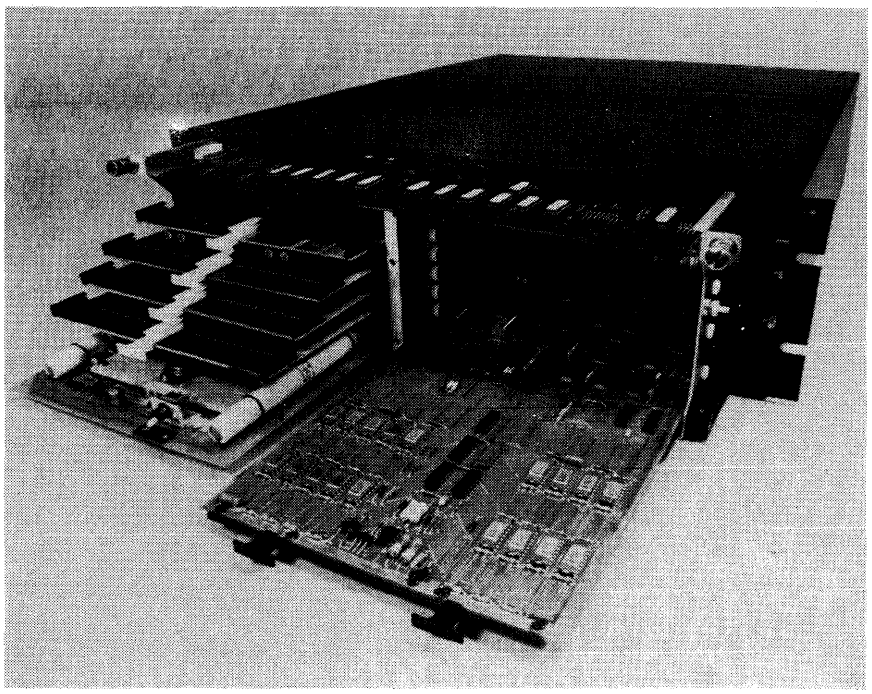

The entry-level Model 23 CPU can contain up to 128K bytes of memory on a half-size board using the 16K-bit memory chips shown in the right foreground. The chassis holds the Model 23 processor and up to 12 half-size modules for memory and peripheral and communications controllers.

The Model 37 utilizes the processor from the DPS 6/48. This provides a 30 percent performance increase over the Model 33. The integral Commercial Instruction Processor increases COBOL performance by a factor of five. The Model 37 supports up to one megabyte of memory and the optional Scientific Instruction Processor.

The Model 47 is a commercially oriented member of the Level 6 line that operates at approximately four and a half times the speed of the Model 43 in commercial applications. The additional speed is gained through a second processor that operates in parallel with the main processor. This second processor, known as the commercial instruction processor (CIP), is a Model 47 standard feature. Other standard features include the Model 53 power supplies and full or basic control panel, memory management, a watch-dog timer, a 10-slot chassis expandable to 23 slots, and single- or double-fetch NMOS memory (32K to 2048K bytes). Optional features include the SIP.

The Model 47 commercial instruction processor features a 30-instruction set that includes decimal arithmetic, binary to decimal and decimal to binary conversion, edit, and branch instructions. The CIP also handles alphanumeric data. Both packed (4-bit) and string (8-bit) decimal formats are supported. Decimal operands may be signed or unsigned. CIP numeric operations can be performed upon mixed data types. As an example, a packed unsigned number can be added to an unpacked number with a trailing sign. Maximum operand lengths are 31 digits for decimal operands and 255 characters for alphanumeric operands.

The Model 53 is similar to the Model 43 with 8192 bytes of cache memory added. For average program mixes, the

CENTRAL PROCESSORS

The Model 23 CPU includes multiply/divide hardware, 5 or 9 slots, power distribution unit, DMA or Direct Multiplexed Control (I/O channels, and a control panel bootstrap loader.

The Model 33 and larger systems include multiply/divide hardware; real-time clock; ROM bootstrap loader for keyboard console or diskette; power supply; Megabus chassis; extensive use of firmware to support task dispatching and I/O control; special circuit with LED display to report on connect status; and automatic basic logic tests as part of the bootstrap operation.

Standard with the Model 33, 37, and 43 is a 5- or 10-slot chassis, a memory controller with parity, and either a basic or full control panel. The 47, 53, and 57 are available only with 10-slot chassis. A watchdog timer is standard on the Model 43 and larger processors. The previously mentioned memory management unit is standard on the Model 37, 43, 47, 53, and 57.

The Model 37 incorporates the central processor from the DPS 6 Model 48 to provide a single board processor with a commercial instruction set and memory management functions. The Model 37 is said to offer a performance level 30 to 100 percent higher than the Level 6 Model 33.

Logic within the Model 43 offers a 30 percent performance increase over the Model 33. Honeywell claims that an additional 30 percent performance increase can be implemented on the Model 43 through the use of the interleaved double-fetch memory.

The standard Commercial Instruction Processor, operating simultaneously with the standard processor, allows the Model 47 to run commercial applications at approximately 4 times the speed of the Model 43. The 8K byte cache memory included in the Model 53 increases its performance by 40 percent over that of the Model 43. The Model 57 has approximately one and one-half times the throughput rate of the 43.

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Model 53 will execute programs about 50 percent faster than the Model 43. Other features of the Model 53 include a 10-slot chassis expandable to 23 slots, full control panel, power supplies, memory management, and single- or double-fetch NMOS memory (32K to 2048K bytes), Honeywell recommends double-fetch memory for this processor. The instruction set is the same as that of the Model 43, and the SIP is an optional feature.

Main memory in the Model 53 is accessed only if the desired word is not stored in cache memory. Once the word, whether instruction or data, is accessed, it is stored in cache for quick reference should it be needed again. The cache "listens in" to the Megabus and grabs words as they go by, retaining those which are not already in cache. Older information is dropped out. Whenever a word already in cache is written, it is modified both in main memory and in cache. The cache memory has a cycle time of 145 nanoseconds.

The top member of the Level 6 line, the Model 57, executes COBOL programs up to twice as fast as the Model 47. It can function as the host computer in a distribued processing network composed of various-sized Level 6 models, allowing a closer match of processing needs and capabilities. This approach can also be directed toward competitive users as a more cost-effective alternative to, for instance, IBM's SNA/SDLC-based communications systems.

Like the Model 47, the Model 57 has two processors, one for executing the standard Level 6 instruction set and a second that executes an additional set of COBOL instructions. The Model 57 also includes an 8K cache memory buffer, a memory management unit, and the Level 6 Megabus architecture that is common to all Level 6 systems from the Model 33 upward. The Megabus can contain from 10 to 23 slots for the central processor, memory management unit, cache memory, commercial and scientific instruction processors, and main memory and peripheral controllers. Main memory capacity ranges from 32K to 2000K bytes. The Model 57 CPU can execute over 700,000 instructions per second, supports direct addressing of two million bytes of memory, and includes a scientific instruction processor for efficient Fortran execution.

The Models 37, 43, 47, 53, and 57 are intended to help Honeywell penetrate the upper range of the commercial and scientific minicomputer market, where it will compete with machines such as the Data General S/250 and C/350, the DEC PDP-11/34 and 11/70, and the Hewlett-Packard 3000 Series. Like the Model 33, the 37 and 43 are offered in either a 5-slot or 10-slot chassis with expansion possible to 23 slots. The Models 47, 53, and 57 are available only in 10-slot chassis, expandable to 23 slots. Up to two megabytes of memory is directly addressable.

Peripherals offered with the Level 6 systems include disk and diskette drives manufactured by Magnetic

A choice of two types of control panels is offered. The basic panel controls system initialization and offers security since programs cannot be modified through its use. It also enables connection of the portable plug-in panel, which brings the unit up to full panel functionality.

The full control panel allows the CP register and main memory contents to be entered and displayed. It can control, in a step-by-step fashion, the system initialization sequence by single-stepping a program, and stopping and starting program execution. The full panel includes a 7-digit hexadecimal (hex) display and a 16-key hex pad.

A vertical panel mounting option is available for any rack-mounted system where physical space limitations exist. The panel replaces the standard inclined panel mounting and is designed for OEM's with their own cabinetry.

The memory save and auto restart unit is an optional feature that ensures data retention for two memory controller boards for a two-hour period. Support circuit power runs are separated to minimize standby power drain. Electronics within the optional unit maintains the battery charge, retains memory contents when the system is manually powered down, regulates outputs, and indicates holdup failures. Power failures generate an interrupt with the auto restart feature. Following power failures, operations are automatically resumed, starting at memory location zero. Up to 1.5 microseconds are allowed for the user program interrupt handler.

The Scientific Instruction Processor (SIP) (not available on the Model 23 or 33) is a single-board processor constructed around an LSI 40-pin chip and 17 4-bit-slice bipolar microprocessors. The SIP features mixed-precision arithmetic, mixed-mode arithmetic, automatic normalization, rounding and truncation of results under software control, and the support of maskable traps. Data integrity checks can be performed for hardware, data, or program. The SIP allows FORTRAN programs to run fifteen times as fast on the Model 33.

Both 32-bit single-precision floating-point operands with an accuracy of 6 hex characters and 64-bit double-precision floating point operands with an accuracy of 14 hex characters can be handled by the SIP, as well as single-word and double-word integer operands. Mixed-mode arithmetic is possible since integer values in certain central processor general registers are automatically converted to floating-point prior to processing with floating-point values in the SIP scientific registers. The traps available to the SIP include reference to unavailable resources, SIP program error, division by zero, exponent overflow, significance error, exponent underflow, and precision error.

Upon decoding a scientific instruction and resolution of address syllable and memory management, the CPU sends the command and the operand memory address (if required) to the SIP, and goes on to the next instruction. The SIP gets the operand from memory under DMA control and overlaps processing with the CPU processing.

The SIP includes "double-fetch" logic and gets operands from memory two words at a time if interleaved memory is included in the system.

The Commercial Instruction Processor (CIP), a standard feature of Models 37, 47, and 57, includes 30 instructions for numeric, alphanumeric, edit, and branch operations. Decimal (both 4-bit packaged and 8-bit string), alphanumeric, and binary data can be processed with mixed data types in the same operation. The maximum length of decimal operands is 31 digits, while alphanumeric operands can be up to 255 characters in length.

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Peripherals, Inc., the joint-venture company formed by Control Data and Honeywell Information Systems. Other peripherals include card readers, line printers, magnetic tape units, and both CRT and teletypewriter terminals. The current array of peripherals shows a definite trend toward vertical integration, with between one-half and two-thirds of the units being manufactured by Honeywell.

Peripheral device controllers are microprocessor-based and support up to four specialized interfaces called Device-Pacs. These interfaces allow one controller to support a mixture of devices and reduce hardware costs by sharing common interface logic. All data transfers, including those to and from slow I/O devices, occur through the DMA channel and are initiated by passing a descriptor block from memory to the controller. A multiple-device controller for console, diskette, card reader, and printer control is offered, as well as a general-purpose DMA controller for non-standard, user-specified peripherals.

Of even greater significance than the device controllers is the communications controller, constructed similarly to the peripheral controllers but with an important added feature. The communications controller mounts up to four one- or two-line interfaces, all of which share a 4K-byte read/write memory included on the controller board. The microprocessor supports a variety of standard protocols normally used. The MLCP allows users to write special-purpose line-control programs using a 28-instruction set. This feature provides user programmability beyond the level normally found in units offered by other manufacturers. The instructions available for the line control microprocessors include add, subtract, compare, AND, OR, block check, table look-up, and branches, and are supported by the Level 6 assembly language. User-developed line programs can be stored in main memory, and transferred in and out of the controller memory along with data under program control.

On all Level 6 processors, all system elements, except memories and the general-purpose interface, contain independent self-test features that are initiated automatically each time the system is powered up or at any time by command. Memories are tested by the CPU after it performs its own self-check. Each module in the system has an LED failure indicator that is normally extinguished by the test routine. Users can isolate failed modules by observing the indicators, and thereby reduce maintenance costs.

SOFTWARE

Level 6 GCOS 6 is a disk/diskette-based operating system with executive, file management, and communications facilities that support multitasking, real-time, and data communication applications; batch processing; transaction processing; and time-sharing. One of three executive modules can be selected.

CONTROL STORAGE: In the Model 33, ROM consists of 512 56-bit micro-instructions with a variable 290-380 nanosecond microcycle time. The Model 37 includes 1024 micro-instructions, 80 bits in length, with a 210 nanosecond micro-cycle time. ROM in the Model 43 and larger systems currently consists of 1024 64-bit micro-instructions. One of four access times is possible for the larger ROM: 185 nanoseconds, 205 nanoseconds, 225 nanoseconds, or 345 nanoseconds.

REGISTERS: Models 23 and 33 each include 18 program-visible hardware registers, while the Model 43 has this basic complement of 18 plus from 2 to 8 more depending on the options included. The Model 37 provides 22 basic registers plus 6 optional registers. Included in the basic registers are 7 distinct data registers (R1-R7) used for accumulators, data manipulation, etc., and 7 distinct base registers (B1-B7) used for memory addressing purposes. By separating these functions, Honeywell is able to offer various ranges of direct addressing capability in the various Level 6 models, yet preserve program compatibility among them.

This architecture is based on the fact that the data registers are 16 bits in length on all models, thus preserving the integrity of arithmetic and logical operations. The base registers, on the other hand, vary in size between models. On the Models 23 and 33, these registers (plus the separate program counter) are 16 bits in length, thus allowing these models to directly address up to 128K bytes of memory. The base registers on the Model 37 and larger systems are 20 bits in length, thereby allowing them to directly address 2 million bytes.

In the Level 6, the base registers are used to address memory to the *word* level. While the 16- or 20-bit base registers can be used directly for word addresses, *byte* operands can be addressed by appending a 17th or 21st bit to the generated address. This is done automatically through the use of indexing. The first three data registers (R1-R3) serve as index registers and can be used to count bits, bytes, words, or double-words. If, for example, a byte instruction is being indexed, the contents of the index registers will be shifted right one place before being added to the base register contents, thereby providing a 17- or 21-bit address. Auto-indexing increases or decreases the contents of an index register by one regardless of the unit of data it is addressing.

Additional registers in the Models 23 and 33 include one program counter (P register), one system status register (S register), one indicator register (I register), and one eight-bit special trap register for implementing trace routines called the mode control register (M1). Three of the seven accumulators can be used for address indexing. One floating-point accumulator is defined in standard software packages on all models where the SIP is not installed.

The Model 37 and larger systems have up to eight additional program-visible hardware registers in the standard complement. These include the 20-bit stack address register (T register), and additional mode registers (M2 through M7) for various options.

If the optional SIP is installed, the standard register complement is increased by three 64-bit scientific accumulators, two 8-bit SIP mode registers (M4 and M5), and an 8-bit SIP indicator register (S1).

ADDRESSING: All Level 6 models have 18 addressing modes in addition to register addressing: direct (to 128K bytes in the Models 23 and 33, 2 megabytes in the larger systems); indirect; indexed; indirect indexed; immediate (half-, one-, and two-word operands); base register direct; base register indexed address; base register indirect address, base register indirect address post-indexed; base register pre-

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The GCOS 6 MOD 200 Entry-Level Transaction Processing System combines executive and transaction components with the GCOS 6 language processors and file systems. MOD 200 provides standard I/O, input/output drivers, file and data management, program and overlay loading, memory acquisition, and task and request management services. MOD 200 supports CRT's in transaction mode, using COBOL and BASIC.

GCOS 6 MOD 400 and MOD 600 support the execution of application tasks and enable users to control the execution of individual tasks while synchronizing multiple tasks with one another and with time-related events. The executives control the loading of programs and manage requests for memory. They provide trap handling routines for exception conditions, and also allow users to specify trap conditions and to provide their own trap handling routines.

The MOD 400 executive supports concurrent execution of one batch stream and one or more interactive streams. The batch application memory can be rolled out to gain memory for interactive applications. Interactive applications may be loaded and started at any time after system initialization. The number of applications in operation is limited only by the amount of available memory. When one application terminates, its memory is released. Programs can be relocated only at load time. Multiple tasks sharing the same priority level are serviced in round-robin fashion. The Memory Management Unit, included in Model 37 or larger models, protects application tasks in different memory pools.

Honeywell offers its version of the widely used TOTAL data base management system for Model 33 and larger Level 6 computers using MOD 400. The INFO 6 conversational data file management system provides data entry, update and query language, and report writing capabilities for such configurations with 64K bytes of memory. INFO 6 can run concurrently with any other application.

GCOS 6 MOD 600 provides support for the Level 66-compatible I-D-S/II data base management system and Transaction Driven System (TDS). Entry-Level FORTRAN, FORTRAN, Intermediate-Level COBOL, and Advanced COBOL are also supported. Users execute in either time-sharing or non-time-sharing mode, as determined at registration time. In time-sharing mode, tasks are dispatched according to an adaptive algorithm. MOD 600 supports a segmented address space into which one or more 512 byte to 128K byte segments can be loaded. Any of the relocatable segments can be given a priority for swapping, and they need not be contiguous.

The GCOS 6 File System provides device-independent access to sequential files, and direct and indexed sequential access to direct-access files. The File System also manages the space utilization of mass storage volumes, allowing users to create and expand files.

decremented (push addressing); base register post-incremented (pop addressing); base register auto-indexed pre-decremented (push indexed); and base register auto-indexed post-incremented (pop indexed). All the previous addressing modes are for one-word instructions; the following are for 32-bit instructions: program relative direct; program relative indirect; base register relative direct; base register relative indirect; and interrupt vector relative.

In push addressing, 1 is subtracted from the contents of an address register prior to its being used as an address except for for double-word load or store, where 2 is subtracted. Push indexed addressing is similar to push addressing but subtracts 1 or 2 from the contents of an index register before the contents of this register are added to the contents of an address register. Pop addressing is the reverse of push addressing, in that 1 or 2 is added to the contents of an address register prior to its being used as an address. Again, pop indexed is the reverse of push indexed, since 1 or 2 is added to the contents of an index register prior to the contents of this register being added to the contents of an address register.

Relative addressing employs the second word of the instruction for storage of an algebraic displacement of ±32K relative to either the program counter, an address register, or the interrupt vector for the current central processor level.

Indirect addressing is to one level only, and indexing is always post-indexing. Auto-increment/decrement can be performed on any index register or any base register. The increment/decrement unit is 1 regardless of the data element implied by the instruction, i.e., word, byte, bit, or double-word.

INSTRUCTION REPERTOIRE: The Models 23 and 33 have 108 standard instructions while the Model 37 has 124, designed to operate on bits, bytes, words, and multiple words. Instructions of the Models 23 and 33 consist of 12 types, including 9 modify, 6 control, 5 bit-oriented, 7 byte-oriented, 12 word-oriented, 2 double-word-oriented, 8 mode register, 10 branch on register, 22 branch on indicator, 8 shift short, 4 shift long, 8 generic, 4 short value immediate, and 3 I/O instructions. The Models 37 and larger systems' instruction sets build on that of the 23 and 33, adding two word-oriented instructions and 14 generic instructions. The SIP augments the Model 37 set with 4 single-operand scientific instructions, 8 double-operand scientific instructions, 6 branch on register, and 12 branch on indicator.

INSTRUCTION TIMINGS: The following times are for full-word fixed-point operands on the Model 33, in microseconds.

Load/Store:	**1.5/2.1**
Add/Subtract:	**1.9/1.9**
Multiply/Divide:	**12.7/17.0**
Compare and Branch:	**2.1**

The following instruction timings are based on a register/register format on the Model 37.

Load/Store	**1.0/1.3**
Add/Subtract	**1.2**
Multiply/Divide	**10.8/14.4**
Compare and Branch	**2.4/3.2 (no branching/branching)**

The instruction times for the Model 43 are in microseconds, for single-precision floating-point operands with the optional SIP:

Load/Store	**1.9/1.3**
Add/Subtract	**1.0/1.0**
Multiply/Divide:	**7.5/12.0**
Compare and Branch	**1.9-2.3**

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The GCOS 6 operating system allows remote and local terminals to be accessed through the sequential file interface of file management or, for more direct control, by using the system's physical I/O interface.

The Data Entry Facility (DEF), running under either the MOD 400 or MOD 600 Executive, can support up to 14 of Honeywell's VIP 7200, 7801, or 7802 CRT terminals in applications such as order entry, inventory control, and accounts payable/receivable. Users can write data entry and other required subroutines in COBOL or Level 6 Assembly Language. The subroutines can be run concurrently with other DEF functions and with processing such as file transmission. Basic forms data entry with editing, validation, and table lookup do not require the use of any subroutines.

Interactive communication between a Level 66 host computer and DEF terminals on a Level 6 is supported by the Interactive Entry Facility (IEF). The IEF allows VIP 7200 terminals to operate in either forms mode or free-format mode. Connected Level 6 printers and disk files, as well as up to 14 terminals, can be accessed.

The GCOS 6 on-line test and verification routines allow testing to occur concurrently with user applications. The system keeps an error log for detection of failing components.

Communications support is provided by GCOS 6 MOD 200, 400, and 600. MOD 200 supports Honeywell's VIP 7200 and VIP 7801 asynchronous terminals, multileaving HASP, and file transmission between Level 6 and Level 66 processors. MOD 400 and MOD 600 support access to remote terminals for high-level languages and the operating system through references to the terminals as sequential files. MOD 400 and 600 also allow Level 6 processors to communicate with Honeywell Series 2000, Level 62, Level 64, and Level 66 computer systems, and, through BSC protocols, with non-Honeywell processors.

The GCOS 6 communications subsystem serves as a foundation for building a user's communications systems. The file transmission capability provides the ability to exchange ASCII and binary files between Level 6 and remote host processors. Honeywell hosts include the Series 60 and Series 200/2000, using polled VIP or HDLC (High-Level Data Link Control) protocols. For IBM hosts, Level 6 processors convert ASCII data to EBCDIC code for transmission using the BSC 2780 protocol. In either case, line speeds up to 9600 bits per second are possible.

Honeywell's Programmable Facility/3271 is a software offering designed to provide IBM 3271-compatible interactive operation and to serve as a base for enhancements. The DPS 6 system appears to be the host processor as an IBM 3271 Control Unit Model 2 with IBM 3277 Display Stations Model 2 and IBM 3284 or 3286 Printers Model 2, attached. The system is capable of concurrent operation with user-developed or Honeywell-supplied software.

INTERRUPTS: All Level 6 models have a single vectored party-line interrupt system with up to 64 priority levels. Each interrupting device transmits a unique identifier to the CPU that causes control transfer through a vector table. The vector table entry points to the Interrupt Save Area (ISA), a memory block of at least 6 entries and as many as 23 entires. The first five entries of the ISA are preloaded by the software and contain: 1) the Trap Save Area (TSA) pointer, used only if trap processing was in progress at the time of the interrupt; 2) the device identifier, indicating the I/O device to which the interrupt level is assigned; 3) the Interrupt Save Mask (ISM) that specifies which of the 16 accumulators, base registers, indicators, and mode registers are to be saved; and 4) the address of the interrupt handler routine. The remaining entries are used to store the system status register and those registers specified by the interrupt save mask.

The Level 6 processors also have provisions for 46 trap vectors, for use with hardware enhancements and internally detected conditions such as nonrecoverable memory errors, program errors, unimplemented instructions, privileged operations violations, or program trace operations The SIP adds traps for such conditions as reference to unavailable resources, exponent overflow, exponent underflow, and precision errors. Trap vectors are stored in reserved memory locations and point directly to the trap handler routines, unlike the interrupt vectors which point to a control block in memory. Also associated with trap functions are Trap Save Areas, in which trap parameters and program context are stored during trap processing.

PHYSICAL SPECIFICATIONS: The 5-slot Model 23 Minimount chassis and the 5-slot Megabus chassis utilized for the Model 33, 37, and 43 are both 5.25 inches high, 19 inches wide, and 28.25 inches deep. The 10-slot Megabus chassis for the Model 33 and larger systems is the same width and depth as the 5-slot chassis but is 10.5 inches high.

The RETMA (Rack-mounted Electronic Terminal Manufacturers Association) cabinet with all panels and doors for the Level 6 central processor is 60 inches high including casters, 20.5 inches wide,and 30 inches deep (36.25 inches with control panel overhang). The unit weighs 155 pounds. Interior dimensions are 56 inches high, 19 inches wide, and 29.2 inches deep. Servicing requirements necessitate an area approximately three feet wide and nine feet deep. For an expansion cabinet, add two feet to the required width; for a second expansion cabinet, add two feet more. Adequate space for the typical system including a printer, processor cabinet with extension table wing, and console is 146.5 inches wide and 162.25 inches deep.

Power requirements for the Level 6 processors are either 110 VAC single-phase (for small configurations) or 208 VAC ±10 percent, 55 Hertz ±7.5 Hertz, single-phase, three-wire plus ground source. Higher-voltage operation with 50-Hertz power is available. Peripherals generally require 120 VAC +10/-15 percent, at 60 Hertz ±0.5 Hertz.

Operating environment for all Level 6 processors is 32 to 122 degrees F. at 5 to 95 percent relative humidity, noncondensing. For a typical system including printer and magnetic media, the temperature may be 60 to 90 degrees F. at 30 to 60 percent relative humidity. The central processor alone outputs in excess of 4,100 BTU/hour, so that air conditioning in some from is required.

INPUT/OUTPUT CONTROL

I/O CHANNELS: All processors feature the Megabus, an asynchronous high-speed bus implemented as a printed-circuit backplane to which all system components are connected and through which all inter-device communication occurs. The Megabus has an addressing range of over 16 million bytes and supports data rates up to 6 million bytes per second. Most I/O controllers are microprocessor-based and transfer all data directly to or from the DMA channel.

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The Level 6 HASP Multileaving Facility and the 2780/3780 Workstation Facility are both also supported by the MOD 400 and MOD 600 executives. Both of these remote transmission facilities utilize binary synchronous communications (BSC). The HASP facility causes the Level 6 to appear to the host as an IBM System/360 Model 20, and the 2780/3780 emulation system causes the Level 6 to appear as an IBM 2780 or 3780 remote batch terminal.

APPLICATIONS

Application areas for Honeywell's Level 6 computers include distributed processing networks, both large- and small-scale business systems, word processing, industrial and process control, and medical applications. The commitment to network and distributed processing is evidenced by the number of system applications discussed below.

In conjunction with the ongoing enhancement of the Level 6, Honeywell has released several products containing Level 6 technology and Level 6 processors. The Datanet 6678, for example, is a front-end processor based on Level 6 technology. The 6678 is designed to service large-scale Honeywell Level 66 and Level 68 host computers. The basic configuration includes the processors with cache memory, 128K bytes of main memory, a host processor attachment, a controller for the console and cassette/diskette drive attachment, and six channel interface bases.

Level 6 minicomputers have also been ruggedized for special factory, environmental, and military applications. Features and performance of these RL 6 versions are identical with the commercial versions of the Level 6 machines. The systems consist of standard Level 6 boards which are braced and mounted in a cast chassis. Capabilities have been added for shock, vibration, and RFI/EMI (radio frequency interference/electro-magnetic interference) resistance. Another enhancement is Tempest, a U.S. government design specification to prevent reading data from the system's electromagnetic emissions. Two versions of each Level 6 Model will be offered: a version to meet standard Tempest-level specifications and a dynamic shock/vibration-resistant version.

The ruggedized RL 6 systems have undergone environmental testing related to ground, mobile, and shipboard applications as specified by government standards. The marketing thrust will encompass a broad range of military, non-military, government, and industrial applications, with competition expected to come mainly from the Rolm ruggedized versions of the Data General Nova and Eclipse minicomputers. Other competitors include Varian/Univac's RV70, the Norden version of DEC's PDP-11, and the Electronic Memories & Magnetics Severe Environment offerings.

Training courses in Level 6 programming and maintenance

Currently, these controllers are available: the MSC9101 mass storage controller for up to four disk drives, the MSC9102 for higher-speed disk drives and two tape controllers, the MDC9101 multiple device controller for conventional I/O devices (card readers, card punch, document handler, console, printers and diskette), and the MLC910X multi-line communications processors. All require additional interfaces, called Device-Pacs for peripherals or Communications-Pacs for communications lines, to match the controllers to the individual devices or lines. Also available is the non-microprocessor-based GIS9001 general-purpose DMA interface, on which users can construct single-channel specialized device controllers.

SIMULTANEOUS OPERATIONS: During direct memory access (DMA) operations, once a channel is set up by the central processor, data transfers are effected via the bus independently of the central processor. Thus, I/O is interleaved with the processor cycles and memory cycles. In addition, the central processor can accept interrupts from other units between the read request and the read response bus cycles to/from memory.

The memory does not initiate the read response cycle until after it has accessed the data. This is done during a 550-nanosecond memory cycle which partially overlaps the two bus cycles. During this time the bus is free to accept requests from other units, interleaving bus cycles and effectively overlapping operations.

CONFIGURATION RULES

The Level 6 Megabus Structure allows the user total flexibility in system configuration. Each Level 6 system can be configured to meet a specific user's needs. The Model 23 is configured with a 5- or 9-slot chassis. The 33, 37, and 43 are available in either 5- or 10-slot chassis while the larger 47, 53, and 57 use a 10-slot chassis for the base configuration. All Level 6 systems, except the Model 23, can be expanded to a 23-slot Megabus. The maximum configuration, parameters outlined below are based on total system capacities:

- **Up to 2 million bytes of main memory**
- **Up to 2048 million bytes of on-line disk storage**
- **Up to 64 workstations**
- **Up to 8 magnetic tape drives**
- **Up to 8 printers.**

WORKSTATIONS: Up to eight communications lines can be handled by each Multi-Line Communications Processor (MLCP). The maximum recommended number of workstations for each Level 6 processor is as follows: Model 23, 8; Model 33, 16; Model 37, 32; Model 43, 40; Model 47 40; Model 53, 64; and Model 57, 64.

DISK STORAGE: The Model 23 supports up to four cartridge disk units, either 26- or 80-megabytes each, with a total system storage capacity of 320 megabytes. The cartridge disk units provide media transferability with the larger Level 6 systems. The Model 33 and larger systems can now handle two mass storage controllers which each support up to four disk drives. The available disk units have either a 10-, 26-, 80-, 67-, or 256-megabyte capacity. Total on-line capacity for the Model 33 and larger systems is over two billion bytes of data.

MAGNETIC TAPE: All of the Level 6 processors support magnetic tape operation. Seven- and nine-track drives are available with either NRZI or Phase Encoded recording at 45 or 75 ips. The magnetic tape controller will handle up to four tape units or no more than two tape drives plus two unit

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nance are offered at Honeywell's training centers in Wellesley, Massachusetts and Phoenix, Arizona.

Level 6 systems may be purchased or leased for terms of three to seven years. After expiration of the lease term, users can either terminate upon 90 days' notice, continue usage at the same monthly charge, or purchase the equipment at its fair market value. System additions and upgrades can be purchased or leased.

USER REACTION

The 1980 Datapro User Reaction Survey prompted responses from 29 Level 6 users. The system life reported for each system varied from three to 35 months with an average experience level of slightly over one year. Twenty three users purchased their systems while five preferred a lease arrangement and one rented their Level 6 system.

Accounting was the principal application listed with 7 responses. Payroll/personnel functions rated 11 votes with manufacturing applications commanding nine responses. The remaining applications listed and the corresponding number of responses received follow: Distributed processing = 6; transaction processing = 4; medical/health applications = 3; retail = 2; utilities/power = 2; construction = 2; and education = 2.

By far, the largest source of application programs was reported to be in-house personnel. Nineteen users reported that they were developing their own application programs. Seven users employed contract programmers, six used proprietary software packages, six utilizes the manufacturer's personnel as their application source, and five purchased "ready-made" programs from the manufacturer. COBOL was the language used by 22 of the respondents. BASIC rated three responses; FORTRAN, two; and RPG, one.

The majority of the users have one Level 6 systems with anywhere from two to fifteen workstations. Two users have larger systems, a Level 47 and 57, with 100 workstations reported on each. Three users reported on multiple systems to bring the total number of CPUs in our survey to 37. Six systems run under GCOS 6 MOD 200; 13 utilize MOD 400; and two, MOD 600.

Planned acquisitions for the coming year will provide additional software from the manufacturers for eight Level 6 users. Five others plan to purchase proprietary software from other suppliers. The remaining users were divided between adding distributed processing capabilities and integrating word processing capabilities. Twenty-seven users are not expecting to replace their computer system over the next year. One user is expecting to trade their Level 6 for another Honeywell system while one intends to leave the Level 6 and Honeywell fold for another manufacturer.

The users who responded to our survey were equally vocal about the good and bad aspects of their Level 6

record devices, such as card readers, serial printers, or line printers.

LINE PRINTERS: A printer hard-copy console, or printer terminal must be configured with every Level 6 system. The Multiple Device Controller (MDC) will connect up to four low- to medium-speed peripheral devices, including line printers. The available line printers range in speed from 240 to 900 lines per minute.

MASS STORAGE

CARTRIDGE MODULE DISKS: These units are available in two different capacities: 26-megabytes (13-megabytes fixed and 13-megabytes removable) and 80-megabytes (67-megabytes fixed and 13-megabytes removable). The 13-megabyte removable cartridge is transferrable between both types of units. The fixed portion of this unit consists of either one platter with a single surface storing 13 megabytes of data or three platters with five surfaces storing 67 megabytes of data.

The units have 823 tracks per surface with either 2 or 6 surfaces depending on the capacity. The disks are available with either a fixed length sector of 256 bytes or an alternate of 2304 bytes. The GCOS operating system only supports the 256-byte sector format however. Utilizing this format will provide 64 sectors per track and a total capacity per unit of either 26,968,064 or 80,904,192 bytes. The average latency is 8.33 milliseconds based on a rotational speed of 3600 rpm. The minimum, average, and maximum seek times are 6, 30, and 55 milliseconds, respectively. The tranfer rate is 1.2 megabytes per second with a recording density of 6030 bits per inch and 384 tracks per inch.

Up to four units may be handled by one controller. During data transfers on one unit, simultaneous seek operations can be performed on all other units attached to the same controller. These disks are available with either one or two drives mounted in a 30-inch minimount cabinet. These drives are manufactured by Magnetic Peripherals, Inc., a Honeywell-Control Data joint venture.

DISK PACK DRIVES: These units are available in a 67-megabyte and a 256-magabyte capacity. The 67-megabyte version ues a technology similar to that of the IBM 3330, applied to a five-platter disk pack. Three of the five platters are actually used, with five surfaces for data and the sixth for servo use. The top and bottom platters are for protection. The 256-megabyte drive employs 12 platters with 19 of the 21 surfaces actually used. The recording format for both units is identical.

Bit density for both units is 6000 bpi, with a track density of 384 tpi. There are 808 tracks per surface plus 15 spares. Each cylinder contains five tracks (67-megabyte unit) or 19 tracks (256-megabyte unit). Formatted track capacity is 16,384 bytes (64 256-byte sectors). Track-to-track, average, and across-all-tracks head movement times are 6, 30, and 55 milliseconds respectively. Average rotational delay is 8.3 milliseconds, based on a rotational speed of 3600 rpm. The data transfer rate is 1.2 megabytes per second.

The controller handles up to four drives intermixed in any fashion. The 67-megabyte version is available with either one or two drives housed in a 36-inch high cabinet. The 256-megabyte version is housed in the same size cabinet but is limited to one drive per cabinet. The drives are manufactured by Magnetic Peripherals Inc.

FLOPPY DISK SUBSYSTEM: This subsystem uses the Multiple Device Controller (MDC) to control up to four single-sided or double-sided diskette drives. Data is recorded in IBM 3740-compatible format on 77 tracks and 26 128-byte sectors per track, providing a total storage capacity of 512,512

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experience. Fourteen respondents noted that the delivery and/or installation of their equipment was late. Ten added that their required software was also late. Ten users felt that the vendor did not provide all the promised software or support. Another eight felt that system costs exceeded their expectations. To counter these problems, nineteen users were pleased with the expansion and reconfiguration potentials of the Level 6. Fifteen users noted that they were happy with the system response time. Possibly the most important comment was made by ten users who were able to keep their programming costs down by using the system's productivity aids. Seven others noted the Level 6 to be power and energy efficient.

A summary of the ratings provided by these users follows:

	Excellent	Good	Fair	Poor	WA*
Ease of operation	6	13	1	2	3.0
Reliability of mainframe	11	10	7	0	3.1
Reliability of peripherals	6	17	5	0	3.0
Maintenance Service					
Responsiveness	7	13	5	2	2.9
Effectiveness	5	14	6	3	2.8
Technical Support					
Trouble-shooting	3	12	10	4	2.5
Education	2	6	15	6	2.1
Documentation	1	10	13	5	2.2
Manufacturer's Software					
Operating system	6	16	3	3	2.9
Compilers and assemblers	7	15	1	3	3.0
Applications programs	4	10	7	4	2.6
Ease of programming	6	14	5	1	3.0
Ease of conversion	3	9	8	2	2.6
Overall satisfaction	4	16	8	1	2.8

*Weighted Average based on 4.0 for Excellent.

The Level 6 rated pretty good marks in the reliability and actual operations areas (ease of operation and programming). The operating system, compilers, and maintenance service also held their own. The traditional vendor weak areas, education and documentation, are considered Honeywell's downfall as far as our users are concerned. This area seems to be the bane of computer vendors and would seem important enough to warrant attention. The other viewpont, however, may be that the new system users don't utilize the available training or documentation until there is a problem and then it is too late to help.

The final question "Would you recommend this system to another user in your situation" prompted 22 positive replies to seven negative responses. Honeywell is keeping 80 percent of their customer base happy so they must be doing something right.□

bytes per double-sided diskette. Recording density is 3200 bpi. The drive rotates at 360 rpm. Average rotational delay is 83 milliseconds and average head-positioning is 95 milliseconds including head-settling time. Data transfer rate is 32,248 bytes per second. The floppy disk drives are manufactured by Magnetic Peripherals Inc.

INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

COMMUNICATIONS CONTROL

Communications control is achieved through the MLC9103 multi-line communications processor, a microprocessor-based control for up to eight synchronous or asynchronous full- or half-duplex lines operating at a data rate between 300 and 10,800 bps or one broadband line operating at up to 72,000 bps. Total hardware throughput for the MCL9103 is 16,000 characters per second. The MLC9103 controls the various lines through specialized interfaces called Communications-Pacs that mount on the controller board. Up to four Communications-Pacs can be mounted on each MLC9103.

Two packaged configurations, based on the MLC9103, are also available. The MLC9101 Multi-Line Communications Subsystem for up to eight asynchronous lines includes one MLC9103 multi-line controller and four DCM9103 Synchronous Communications-Pacs. The MLC9104 Multi-Line Communications Subsystem for up to eight asynchronous lines includes the MLC9103 and four DCM9114 Current Loop Communications-Pacs.

The characteristics and specifications of the MLC9103 and the individual Communications-Pacs are described in detail below.

MLC9103 MULTI-LINE COMMUNICATIONS PROCESSOR (MLCP): Interfaces up to eight mixed asynchronous or synchronous lines through Communications-Pac interfaces that mount on the controller board. The microprocessor-based controller performs message separation, algorithm checking and delimiting, check character generation and detection, and special editing functions to reduce processing overhead. The MLC9103 transmits in full- or half-duplex mode over switched or private lines or by direct connection.

The MLCP has a 4K-byte read/write memory that can be allocated in any proportions to the attached lines and features dynamic assignment of program interrupt levels. About 1K bytes are used by the standard operating software for line control tables leaving about 3K bytes for MLCP programs. These programs are either the standard protocols offered by Honeywell or are customized protocols generated from a 28-instruction set especially designed for communications processing that includes such functions as add, subtract, compare, several branches, and internal register transfers. User programs and data can be stored in main memory and transferred in and out of the MLC9103 memory as required, permitting multiple programs for each line. The differences between line protocols and the specific requirements of each Communications-Pac/line combination are handled by small re-entrant software routines shared by all lines.

Up to four Communications-Pac interfaces can be accommodated by the MLC9103 with a maximum subsystem throughput of 16,000 characters per second. Eight full-duplex low-speed lines (300 bps or less) and medium-speed lines (600 to 19,200 bps) or one broad-band line (up to 72,000 bps) can be controlled. Asynchronous Pacs feature 15 program-selectable data rates from 50 to 19.2K bps. Synchronous Pacs can handle data rates from 2000 to 72,000 bps. Character length (5, 6, 7, or 8 bits per line), stop bits (1, 1.5, or 2 per line), and parity (odd, even, or none) are also program-selectable, as are four cyclic redundancy check (CRC) characters: CRC-16, CCITT-16, CRC-12, and LRC-8.

DCM9100 COMMUNICATIONS-PACS: Honeywell currently offers 17 Communications-Pac modules for the MLC9103.

The DCM9101 and DCM9102 are, respectively, two- and one-line asynchronous RS-232C/CCITT V.24 interfaces for full- or half-duplex lines operating at data rates up to

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19,200 bps. The DCM9101 and DCM9102 are designed for use with Bell 103, 113, 202, 301, and 303 or equivalent direct-connect modems.

Models DCM9103 and DCM9104 are the synchronous counterparts of the DCM9101 and 9102. These Communications-Pacs are used for synchronous communications at rates up to 19,200 bps, and interface Bell 201, 203, 208, 301, and 303 or equivalent modems and low-speed direct digital service (DDS).

Model DCM9105 is a high-speed single-line interface for lines operating at up to 72,000 bps. The DCM9105 can be used with Bell 301 and 303 or equivalent modems or with Bell DDS at 72,000 bps, and conforms to the CCITT VS.35 specifications.

Model DCM9106 is for synchronous HDLC communications at rates up to 19,200 bps. Model DCM9108 is CCITT-V.35 compatible and contains one broad-band line with data rates up to 72,000 bps. Model DCM9109 is MIL188C compatible with transmission speeds up to 10,800 bps.

Model DCM9110 supports up to two auto call units (ACU's). The ACU's may be any devices meeting the EIA RS-366 specifications, such as the Bell System 801A (rotary dialing) or 801C (Touch-Tone dialing). The data connection may be via any supporting modems, e.g., Bell Type 103, 201, 202, 203, 208, or 209.

Model DCM9114 provides two current-loop connections with data rates up to 9600 bps. The DCM9126 supplies two asynchronous lines for Series 3000 terminals.

The DCM9112 and DCM9113 are both broadband High-Level Data Link Control (HDLC) interfaces. The DCM9112 is compatible with Bell 301 and 303 modems for transmission speeds of up to 56,000 bps. The DCM9113 is CCITT-V35 compatible with speeds up to 72,000 bps.

The DCM9115, 9116, 9120, and 9121 provide MIL 188C compatibility for a number of different communication configurations. The DCM9115 provides a single synchronous broadband communication line with speeds to 72,000 bps maximum. The DCM9116 is an asynchronous communications interface for two lines with speeds to 9600 baud. The DCM9120 provides one HDLC communications line with speeds to 19,200 bps. The DCM9121 is a one-line broadband HDLC communications interface with a maximum speed of 72,000 bps. Both the DCM9120 and DCM9121 are double-sized communications-pacs and require two MLCP ports.

SOFTWARE

OPERATING SYSTEMS: All Series 60 systems run under a variation of Honeywell's GCOS operating system.

LEVEL 6 GCOS 6: The Level 6 subset of GCOS is disk or diskette based, with executive, file management, and communications facilities that support multi-tasking, real-time, and data communications applications; batch processing; transaction processing; and time-sharing. Three levels of Level 6 GCOS 6 are available.

The *GCOS 6 MOD 200* executive, within the GCOS 6 MOD 200 Entry-Level Transaction Processing System, is a forms-driven system that supports Model 23 and larger Level 6 computers. Major MOD 200 facilities include concurrent on-line and batch application processing, program development, and remote job entry. These capabilities are based on:

- Dynamic task scheduling and allocation of memory, files, and other system resources.
- Sixteen priority levels with user-assigned queuing at each level.
- Event-based or time-slice scheduling.
- Automatic roll-in/roll-out of either overlays or complete task images.
- Automatic volume recognition.

The main executive functions performed by GCOS 6 MOD 200 are: standard I/O control; re-entrant I/O driver operation; and file and data management services for sequential, relative, and indexed sequential files.

Several utility programs are available with GCOS 6 MOD 200 to support program development in BASIC, entry-level and intermediate GCOS COBOL, as well as file management. The volume preparation utility formats and labels disk packs and creates disk bootstrap records. The file utility allows files to be created, deleted, or renamed. Copy moves files and entire volumes from disk to either another disk or a printer, or from a card reader to disk. Compare matches files and volumes, and prints any discrepancies. The print utility prints sequential files, and the file dump prints program files by logical or physical record in both numeric and hexadecimal form. List prints all file entries, or a subset, within a directory showing file type, attributes, and size. A text editor and linker complete the list of program development aids.

The minimum system requirements for the MOD 200 Entry-Level Transaction Processing System for execute-only configurations include a Level 6 CPU, a dual single-sided diskette, a VIP 7200 display terminal, and 32K bytes of memory.

The *GCOS 6 MOD 400* executive Revision 2.1 includes program and task management facilities, multi-program control, I/O and communications support, file and data management, utilities, and support for a wide range of hardware configurations. It also supports a hierarchical file system and 64 vectored priority levels, and automatically recognizes interrupts.

Revision 2.1 contains several significant enhancements involving system availability, memory utilization, and file system capabilities. The system availability enhancements include a power resumption facility which uses the memory save and auto-restart option to presume the memory image and re-activate system operation. A file recovery function saves record images before they are updated in order to provide file integrity in the event of system or program failure. A checkpoint restart procedure is included to provide a file recovery and program restart capability.

The Revision 2.1 file system enhancements include a provision for alternate index (multi-key) file access. This meets the COBOL requirement for indexed files that have a prime record key and any number of alternate record keys. Record locking is now available to provide multi-user interference protection for shared file access. For indexed or random files, only a single control interval is locked.

The memory utilization improvements involve a buffer pool to conserve memory for disk file access. All buffers in a pool are the same size and any number of files can be assigned to the same pool. At any one time, a file is assigned to one and only one pool. Buffer pools may be "public" and reside in system memory or "private" and reside in user memory.

MOD 400 supports both interrupt-driven, multiple-user operation and batch processing. Programs are assigned to

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resource sets called task groups. Concurrently executing task groups can occupy dedicated memory areas, or they can contend for space within a memory pool. Device usage and access to shareable files is controlled by file attributes, access control lists, and concurrency procedures. The executive itself is partially memory-resident. It is controlled, through a terminal, by the Operator Control Language (OCL) for interactive operation, or from a peripheral by the Execution Control Language (ECL). OCL allows the operator to control the composition of the interactive and batch operations and to abort malfunctioning programs. Executing programs can also add and delete tasks, place requests against the tasks, and initiate batch requests.

Monitor services supported by GCOS 6 MOD 400 are called using the Monitor Control Language (MCL). MCL instructions are generated by compilers, and can also be coded in assembly-language macro-instructions. The monitor services include task, trap, memory, file, basic communications, and clock management; a loader; standard I/O functions and input/output drivers; and a scientific instruction simulator based on traps.

MOD 400 is available in two versions. One supports memory sizes up to 128K bytes, and the other operates on Model 37 and larger systems with 128K or more bytes of memory. MOD 400 supports all of the MOD 200 utilities plus an interactive debugging aid, a memory dump editor, a patching facility, and file modification programs.

Minimum system requirements for a GCOS 6 MOD 400 program development system are a Model 23 or larger CPU; 64K bytes of memory in Short Address Form (SAF) or 80K bytes in Long Address Form (LAF); two cartridge disks, four single-sided diskettes, or three double-sided diskettes; and a console.

GCOS 6 MOD 600 provides users of Model 37 and larger Level 6 systems with support for real-time, time-sharing, and transaction-driven applications. It features memory management through a segmentation/ring technique, expended task dispatching and Execution Control Language capability, automatic roll-in/out of blocked tasks, spooling and deferred output processing, and the ability to automatically execute previously-constructed command files for batch processing.

The Memory Management Unit (MMU), the log-on processor with system administration commands, and user-controlled access lists and concurrency controls provide memory management and access control. User address space creation and maintenance and segmentation support are included.

The MOD 600 Executive is built of modules that provide facilities for the monitor, file system, and communications. The monitor supports user application task execution and enables users to control task execution through a set of system services. The file system provides a full set of logical input/output access methods to sequential files for any device and direct access to disk files. Directories and files are arranged in a hierarchical structure to facilitate file system use by multiple independent users. The same directories and structures are used by MOD 400 as well. Files and volumes are fully transportable between the two operating systems. Remote and local communications terminals access the system through the file management sequential file interface. This also is shared by MOD 400.

All MOD 400 monitor functions and utility programs are included in MOD 600.

The minimum system requirements for GCOS 6 MOD 600 are a Model 37 or larger CPU, 256K bytes of memory (including 56K bytes for the resident executive) plus variable amounts of memory for configuration tables, MMU, two cartridge disks (10 megabytes) or equivalent capacity, and an operator console.

COMMUNICATIONS SOFTWARE: Level 6 supports communications under GCOS 6. This support consists of a communications supervisor employing file manager I/O with connect and disconnect, a multi-line communications processor (MLCP) driver, and communications protocol handlers.

The communications supervisor runs in an on-line environment using the file manager I/O with connect and disconnect. The supervisor is transparent to user-level programs. The file manager and the status command offer high-level language access to communications.

The MLCP driver provides a single interface between the two portions of the protocol handler, the CPU-resident line type processor (LTP) and the communications control program (CCP), for the dual purpose of data transmission and communication. The CCP handles character-order processing of the protocol, while the LTP is responsible for event processing specific to the communications protocol and interfacing to the communications supervisor.

Asynchronous protocol and terminal support includes the VIP 7200 and 7801 CRT display units. Synchronous support includes the VIP 7700 keyboard/screen and support of a subset of the IBM BSC/2780 protocol for communication to another Level 6 and from a Level 6 to a Honeywell Level 66 computer. Half-duplex point-to-point connections, normal and transparent mode, primary and secondary procedures, and auto-answer are supported.

The MOD 400 and MOD 600 operating systems also support a synchronous communications feature to transmit files between Level 6 and Level 66 processors. This capability allows a sequential file on mass storage to be transmitted to a remote Level 6 or 66 processor. The protocol used is either polled VIP 7700 or High-Level Data Link Control (HDLC). Files are processed by the Level 66 in standard GCOS format. Terminals supported are the VIP 7700 (with hard-copy option), 7700R, and 7760 in either a polled or non-polled environment. In addition to the Level 6 processor, minimum hardware requirements are a multi-line communications processor, appropriate Communications-Pac(s), and communications resources as follows: Bell System Type 201A, 201B, or equivalent data sets; EIA RS-232C interface; synchronous, two-way alternate, nonpolled VIP 7700 protocol; modified ASCII 7-bit code set; GCOS 6/MDT communications software, including VIP device handler and file management; file transmission program; Level 66 central processor; front-end network processor (DATANET 6600, 355, or 305); GCOS operating system; remote terminal supervisor (GRTS); and file transmission program.

LANGUAGES: Five program development languages, plus a macro-preprocessor that allows development of macros in any higher-level language, are currently available for the Level 6 processors. The program development languages are FORTRAN, COBOL, RPG II, BASIC, and an assembler.

Level 6 FORTRAN is an entry-level compiler available under GCOS 6 MOD 400 and 600. The entry-level FORTRAN compiler is based on Level 1 of the ANSI 1977 revision. It is a one-pass compiler that produces either object code or assembly-language statements, a feature that permits users to include assembler statements in a FORTRAN program stream or to modify compiled programs and modules prior to final execution. Significant features include direct-access files that contain formatted records; formatted I/O operations, usable with both direct and sequential access files; output lists that contain both data references and expressions; OPEN and CLOSE statements to facilitate file usage; EQUIVALENCE statements; uses of any character,

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array variable, or array element as a format identifier; a format identifier which can also be an integer variable assigned a statement label; DO statements that can use expressions as parameters; a computer GO TO statement controlled by an integer expression; character data types which can be used in equivalence, I/O, comparison, and manipulation operations; use of any integer expression as a subscript; and an internal file facility that allows conversion of character-type data.

Entry-level FORTRAN includes a double-precision data type with all computational operations; I/O, intrinsic function repertoire, function specification, and argument passing of the single-precision data type; use of a generic name to call an intrinsic function; an alternate return from a subroutine capability that allows execution to continue from one of several points selected by the subroutine; new and advanced format descriptors; and improved optimization. FORTRAN programs can be used in configurations with the SIP installed or with equivalent software routines.

Advanced FORTRAN is based on ANSI X3.9-1977 specifications and includes a few extensions. The features of Advanced FORTRAN includes re-entrant code, optimized object code, complete set of ANSI-78 FORTRAN library routines, and modular re-entrant and shareable object libraries. Advanced FORTRAN utilizes either the Scientific Instruction Processor or software SIP simulator for compilation as well as execution. In addition, this version of FORTRAN supports direct and sequential formatted or unformatted I/O and all standard ANSI data tapes: integer real, double precision, logical, complex, and character.

Advanced FORTRAN also includes several extensions to the 1977 standard. These are: free form source input; additional data types (fixed, double fixed, fractional, double fractional, and double integer); ISA extensions, and an INCLUDE statement. Advanced FORTRAN requires either the MOD 400 or MOD 600 Executive and 50K-bytes of main memory.

Level 6 COBOL is available in three versions, designated entry-level, intermediate, and advanced.

Entry-level COBOL is a subset of Series 60 COBOL for Level 6 and is based on the ANSI 1974 standard. It does not implement the Indexed I/O, Sort/Merge, Report Writer, Segmentation, Library, or Communications modules. The Nucleus, Table Handling, Sequential I/O, Relative I/O, and Debug modules are all essentially Level 1 implementations. Entry-Level COBOL requires a processor with 13K words of main memory, a dual diskette unit or cartridge disk drive, and a system console.

Intermediate COBOL is a low intermediate level (2 of 4) with extensions. An additional module, Indexed I/O, is essentially supported on Level 1 with some Level 2 extensions. Intermediate COBOL provides support for modular programming via the CALL statement; provides table handling, subscripting, or indexing to three levels; supports the SET statement; provides full editing facilities; and supports data handling via DISPLAY data and picture.

Intermediate COBOL includes certain features not found in entry-level COBOL, such as support for UFAS files; tape support; implementation of indexed I/O files; provision for true variable-length records; addition of the computational data type for 16-bit binary; and enhanced program communication through support of CANCEL, overlays, and mixed-language applications with FORTRAN. In addition, the intermediate version provides for both compilation and text editing on-line. Intermediate COBOL requires 48K bytes of main memory, four diskette units or a cartridge disk drive, and a system console.

Advanced COBOL compiles with the ANSI X3.23-1974 specification except that it does not include Report Writer or Data Communications modules. This represents Level 4 of the COBOL standard. Advanced COBOL includes the following features: re-entrant object code, additional data types (COMP-1/2/5), optional listings (Source Program with Library Text, Cross Reference with Data Allocation, Procedure Map, and Generated Code), interspersed diagnostics, optional line number sequence checking, on-line documentation, capability to re-define margin R, diagnostic severity control, and object code suppression. FIPS leveling allows the user to specify the operating level of the COBOL compiler. If the user specifies Level 3 COBOL, the compiler will flag any usages beyond this level, even if they are valid COBOL instructions at the next level. Advanced COBOL requires either the MOD 400 or MOD 600 Executive and 64K bytes of main memory.

Level 6 RPG II is supported under GCOS 6 MOD 400 and 600 and is a subset of Honeywell's Series 60 RPG II. The RPG II compiler supports source input reading from cards or card images on disk or diskette; automatic file manipulation and diskette or disk handling; sequential, indexed, and direct file organizations; static and dynamic table handling; a look-ahead feature; linkage of external routines with RPG object programs; and utilization of standard data management access routines by object programs. RPG II also supports file forcing, fetch overflow, and exception output. Chain editing codes are supported, but edit words have not yet been implemented. RPG II requires a processor with 64K bytes of main memory, four diskette units or one cartridge drive, and a system console.

GCOS 6 BASIC is available either as Interpreter or Interpreter/Compiler. Each may run under either the GCOS MOD 200, MOD 400, or MOD 600 operating system.

The BASIC Interpreter/Compiler is a multi-user language processor used to interactively develop and execute BASIC programs. For a MOD 200 system, the Interpreter/Compiler is available in a 32K-byte overlaid configuration. This allows the 16K-byte root to be shared. The MOD 400 and 600 systems provide BASIC in a non-overlaid configuration that is completely shareable.

Features of the BASIC Interpreter/Compiler include extensive string support, mathematical functions, double-precision options, and a comprehensive set of matrix facilities. Three types of files are supported by the BASIC Interpreter/Compiler: terminal format files, virtual array files, and record I/O files. Debugging facilities allow the user to set and re-set breakpoints and traces. User-defined functions, statement modifiers, and shareable code all contribute to this version of the BASIC Interpreter/Compiler. Four modes of operation are provided: Command mode, Execution mode, Immediate mode, and Compile mode.

GCOS 6 Assembler processes source statements written in symbolic language, translates these statements into relocatable object code and produces a listing of the source program with its assembled version. The Assembler requires 22K bytes of main memory on a system running under either the MOD 400 or MOD 600 Executive. Assembly language elements include mnemonic op codes, symbolic names, constants, and expressions. Data may be accessed at the bit, byte, word, or multi-word level. Pseudo instructions are provided and a cross-reference listing can be optionally produced.

The *Macro-Preprocessor* is a non-overlaid, one-pass processor, designed to operate in a stand-alone environment, that permits users to define single-line abbreviations (macro calls) for a group of statements written in any higher-level language. The preprocessor then inserts these subprograms into the program stream. It will also accept macros residing in a disk library file. Up to 35 parameters can be handled by

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each macro call. Macros can also contain control statements (macro variables) that modify themselves or other macros in the system. Up to 35 of each type of macro variable (local or global) may be contained in a macro. Nesting of macro calls in macros is unlimited. A nested macro call may call the same macro in which it is contained (recursive call). Depth of recursion is limited only by available memory. Other macro control statements permit conditional reordering of the processing sequence within an individual macro. Macro functions that facilitate character string operations are also included in the preprocessor.

The preprocessor requires 32K bytes of memory, two diskette drives or one cartridge drive, and a system console.

APPLICATIONS PROGRAMS: For a complete listing of the available Level 6 software, please refer to the price list at the end of this report. For a detailed review of these communications, applications, and end-user facilities, please refer to the DPS 6 Report M11-480-501.

UTILITIES: GCOS 6 MOD 200, 400, and 600 utilities support peripheral I/O, debugging aids, program patch, copy/compare, print, dump/edit, file dump, data transcription, file formatting, sort/merge, and file maintenance functions. The GCOS 6 Sort/Merge can be called by any of the three operating systems or compilers. It includes 16 sort key fields and the capability for user processing of input and output records.

TOTAL 6: This general-purpose data base management system is supported by GCOS 6 MOD 400, but not by MOD 600. However, it is a subset of the Series 60 Level 62 TOTAL DBMS. It is implemented much along the lines of the CODASYL Data Base Task Group Report, except that the user can use other host languages as well as COBOL. TOTAL 6 provides an effective means for organizing and managing diverse data to make it both efficient and convenient for application programmers to maintain and retrieve the data for processing. It was developed by Cincom Systems, Inc. and is widely used with large computer systems. It has been well received and highly rated by users.

TOTAL 6 can manage virtually an unlimited number of data sets on an "integrated, non-redundant" basis and provides for association of each of these data sets with other data sets to form an integrated data base. TOTAL 6 allows the user to relate data across many functional and/or departmental boundaries, permitting the data processing applications to mirror the system of management within an organization.

TOTAL 6 permits the establishment of two types of records: a single-entry or master record and a variable-entry record. Each group of records, of either type, forms a file (data set). Linkages can be set up that permit automatic retrieval of all variable-entry records associated with a particular single-entry record based on the linkage. A variable-entry record can be part of many linkage paths or chains.

A TOTAL 6 data base is composed of multiple data sets or files. Linkages can exist between any master file and any variable-entry file. Multiple file data bases can be established. A particular master file or variable-entry file can be part of more than one data base. The multiple paths of access allowed by such a structure, called a network structure, simplify the logic of application programs using the data. In the case of TOTAL 6, they also reduce the amount of disk storage required to hold information by eliminating duplicate fields or records.

To one familiar with sequential and hierarchical sequential files, the benefits of a network structure are not immediately evident. It seems at first glance that the power of a network structure is limited because only one sublevel of linking is possible; i.e., master to variable-entry. The real power of this structure lies in the fact that multiple master files can be established, each for a particular relationship, and any number of variable files can be related to any number of these master files. Each variable file can handle up to 2500 different record types.

A randomizing algorithm is used by TOTAL 6 to calculate master record physical addresses based on the value of the control field. If duplicate addresses are calculated, a pointer is used in that record to show where the "duplicate" or synonym record is stored. Thus, the complete disk space allocated can be used. Once all space is used up, the data file must be reloaded with new parameters. Cincom provides a utility to handle such occurrences.

Access to TOTAL 6 files is provided through the Call statement for application programs written in COBOL, FORTRAN, or assembly language. The applications programmer cannot establish new data sets or alter existing linkages among data items; this function is accomplished separately through a generator program using a special data base definition language.

TOTAL 6 requires 41K bytes of main memory, plus an additional amount for I/O buffers, on a Model 33 or larger system under GCOS 6 MOD 400. A read-only version that requires only 7K bytes is also offered.

I-D-S/II: Honeywell's I-D-S/II data base management system is supported by GCOS 6 MOD 600 in the form of a subset of the Series 60 Level 66 implementation. I-D-S/II is designed to conform completely to the CODASYL architectural specifications. It includes a Data Definition Language for schema and subschema description, a Device Media Control Language (DMCL) to provide additional user control over mapping the data base to the physical devices, an implementation of the DBTG Data Manipulation Language (DML), the full CODASYL privacy and security facilities, and controls for "integrated" (or network) data base organizations.

I-D-S/II is a logical extension of the I-D-S/I data base management system developed and implemented in the 1960's. The I-D-S/II data structure is defined in a schema Data Description Language (DDL) and translated onto a schema file that becomes the central repository for all information about the data base structure and its physical parameters. Programs to process the data in the data base use a subset of the schema, the subschema, that defines those portions of the full structure relevant to each program.

The DDL for the schema deals with records and data items (sometimes referred to as fields) grouped into records, set relationships that tie together records according to their logical relationships, and areas that correspond to files to hold various records that need to be physically collected together. The Data Base Administrator (DBA) is responsible for converting the logical information processing requirements of the data base into a collection of area, set, record, and data item descriptions. To assist the DBA, I-D-S/II incorporates a Data Base Administrator Control System (DBACS), which is effectively an on-line data dictionary and control system. This tool is used by the DBA to design and create the data base and to establish and monitor control over data base accesses.

In I-D-S/II the record is the fundamental item of reference. Data values can be held in a record in one of five formats: Character—a string of ASCII characters or bytes, consisting of any values of the character set for data (character strings can be either fixed or variable in length); Decimal Numeric—which is held as a string of packed numeric digits with an optional sign; Binary Numeric—which also represents numeric data, but is stored as the binary equivalent to the data value and is stored in either 18-bit or 36-bit items;

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Data Base Key—a numeric equivalent of the location on the data base file where a record is located; and Unspecified—a string of one or more 9-bit units whose content is processed by user-supplied data base procedures.

In the schema DDL, fields are defined at the elementary data item level only; that is, no group items are permitted. The subschema allows aggregations so that the group effect can be obtained in the program using the data base. Data structures allow different types of records to be related in a specified manner. A set is defined as a named collection of records. In I-D-S/II sets can be implemented by a chaining technique that constructs a thread from a single owner record through each related member record occurrence. Pointer space is reserved in each record to accommodate the linking mechanism. When a record is stored in the data base, it is assigned a unique internal identifier that indicates its position on the file.

All necessary information about the logical and physical nature of the data base resides in the schema file. Once the schema has been successfully translated, the physical storage factors are supplied through the Device Media Control Language (DMCL), which deals with actual mass storage considerations such as total space allocation, page sizes and characteristics, and inventory control factors.

The Data Base Administrator (DBA) uses the DBACS to perform all translation and utility functions. In order to begin the process of defining a data base, the schema file must be created as a random GCOS file. When a schema source is translated, the schema file is automatically initialized. Once the schema DDL/DMCL translation is complete, the schema file contains the complete definition of the data base.

The DBA can specify two levels of privacy controls in the schema DDL. One protects the schema itself from unauthorized use or alteration. The other is a protection placed on the actual use of the data base being defined. Records, sets, and data items can be locked to restrict specific functions from being performed against them. When a privacy lock is used in the schema, the subschema must provide the key to open this lock. When a subschema is validated against a schema, a list of permitted and prohibited Data Manipulation Language (DML) operations is produced. This list can further be prohibited or can be produced with selected information so that the user sees only that information designated by the DBA for his use.

TEST AND VERIFICATION PROGRAMS: An integral part of the Honeywell maintenance strategy, these programs consist of automatically executed processor and memory tests which are permanently resident in ROM and a family of free-standing routines. These programs consist of eight central subsystem tests for the central processor, memory, scientific instruction processor, power failure detection, and real/time clock/watchdog timer; seven I/O subsystem tests for the console, card reader, printer, diskette, general-purpose DMA interface, cartridge disk, and magnetic tape units; and three communications subsystem tests.

PRICING

POLICY: Honeywell Information Systems offers the Level 6 computers for purchase or lease. Leases are full-payout leases with terms of three to seven years. After expiration of the lease term, users can either terminate upon 90 days' notice, continue usage at the same monthly charge, or purchase the equipment at its fair market value. System additions and upgrades can be purchased or leased.

System lease prices include maintenance. All software is licensed on a fully paid basis. A 12-month financing plan for the paid-up license has recently been introduced.

Honeywell provides maintenance and field support through its own network of more than 400 support locations and thousands of field support personnel worldwide. Systems engineering support is provided at $23 per hour.

The warranty period for systems purchased under the OEM contract is 30 days from the date of shipment and includes return-to-factory repair service. End-user contract warranties extend 90 days form installation and provide including parts and labor charges.

Users with OEM service contracts qualify for discounts of up to 36 percent, while end users receive discounts of up to 21 percent. In both instances, the maximum discount rate is achieved at 100 systems.

Prices given in the Equipment Prices section of this report apply to both OEM and end-user service contracts.

Non-contract service is priced at $40 per hour for standard business hours, Monday through Friday; $45 per hour for other weekday hours plus Saturday; and $53 per hour on Sundays and holidays. The minimum charge is 3 hours, and mileage is charged at 15 cents per mile, portal to portal.

EQUIPMENT: The following typical purchase and rental prices include the controllers and adapters.

MODEL 23 TYPICAL SYSTEM: Consists of a CPU with a 64K-bytes main memory, two single-sided diskette drives (256K bytes), two workstations, a 120-cps printer, and one synchronous communications line interface, plus the basic Mod 200 execute-only software. The single-unit purchase price is $22,238.

MODEL 43 TYPICAL SYSTEM: Includes the processor in a 10-slot chassis with full control panel, memory management, and 256K bytes of double-fetch, EDAC, NMOS, 16K-chip, parity memory and controllers; a VIP 7207 console and keyboard device pac; two 80-megabyte disk drives and controller/device-pac; a multiple-device controller; a 300-lpm line printer and device pac; eight VIP 7200 VDT terminals; two multiline communications processors; four communications device pacs, each for two asynchronous lines; and a communications device pac for one synchronous line (for a host computer link). The single-unit purchase price is $97,333. This does not include software.

MODEL 57 TYPICAL SYSTEM: Consists of a CPU with 384K bytes of main memory, 4K cache memory buffer, 512 million bytes of disk storage, tape drive, line printer, card reader, console, 16 communication line interfaces, GCOS MOD 600 executive, and FORTRAN. The single-unit purchase price is $170,946.■

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PROCESSORS			
Model 23 Minimount Systems; include processor, 5 or 9 available slots, Power Distribution Unit (PDU), and space for 1 or 2 pairs of diskettes.			
Minimount Program Development Processors; include full control panel:			
CPS9350	With 32K bytes of memory, 5 available slots	$5,755	$54
CPS9351	With 64K bytes of memory, 5 available slots	7,250	64
CPS9352	With 64K bytes of memory, 9 available slots	7,615	68
CPS9353	With 128K bytes of memory, 5 available slots	9,775	84
CPS9354	With 128K bytes of memory, 9 available slots	10,140	88
Minimount Execute-Only Processors; include basic control panel:			
CPS9355	With 32K bytes of memory, 5 available slots	4,965	54
CPS9356	With 64K bytes of memory, 5 available slots	6,460	64
CPS9357	With 64K bytes of memory, 9 available slots	6,830	68
CPS9358	With 128K bytes of memory, 5 available slots	8,985	84
CPS9359	With 128K bytes of memory, 9 available slots	9,355	88
All Model 33, 43, 47, 53, and 57 systems include real-time clock, ROM bootstrap loader, power fail interrupt, and control panel; memory must be ordered separately.			
Model 33 Processors; will support from 16K to 128K bytes of memory.			
CPS9470	5-slot Megabus chassis, program development system, full control panel	5,250	59
CPS9471	10-slot Megabus chassis, program development system, full control panel	8,700	61
CPS9472	5-slot Megabus chassis, execute-only system, basic control panel	4,750	55
CPS9473	10-slot Megabus chassis, execute-only system, basic control panel	8,200	57
Model 37 Processors; will support from 32K to 1024K bytes of memory			
CPS9480	5-slot Megabus chassis; full control panel	8,500	76
CPS9481	10-slot Megabus chassis; full control panel	12,500	80
Model 43 Processors; will support from 32K to 2048K bytes of memory			
CPS9560	5-slot Megabus chassis, program development system, full control panel and memory management unit	9,500	86
CPS9561	10-slot Megabus chassis, program development system, full control panel and memory management unit	13,500	90
CPS9562	5-slot Megabus chassis, execute-only system, basic control panel and memory management unit	9,000	84
CPS9563	10-slot Megabus chassis, execute-only system, basic control panel and memory management unit	13,000	88
Model 47 Commercial Processors; will support from 32K to 2048K bytes of memory:			
CPS9566	Program Development system in 10-slot Megabus chassis; full control panel, memory management unit	25,000	210
CPS9567	Execute-Only System 10-slot Megabus chassis; basic control panel, memory management unit	24,500	203
Model 53 Cache Processors; will support 32K to 2048K bytes of memory:			
CPS9570	Program Development System in 10-slot Megabus chassis with Memory Management	25,000	147
Model 57 Commercial Cache Processors; will support 32K to 2048K bytes of memory:			
CPS9572	Program Development system in 10-slot Megabus chassis with Memory Management Unit	40,000	315
PROCESSOR OPTIONS			
CPS9518	Memory Management Option for Models 43 and 47, field installed	3,990	5
PSS9001	Memory save for up to 128K bytes; includes auto-restart, rackmount; does not include batteries	693	6
PSS9003	Mini Memory Save, 5-10 minutes (Model 23 only)	551	5
CPF9401	Watchdog Timer (Model 33 only)	462	3
CPF9503	Scientific Instruction Processor for Model 43, 47, 153, 157	5,303	12
CPF9504	Portable Plug-in Control Panel	1,155	7
GIS9001	General-Purpose DMA Interface	950	—
MDC9101	Multiple Device Controller (device pacs listed under equipment category)	1,500	10
DIM9101	Diskette Device-Pac; requires 2 ports	730	5
PROCESSOR EXPANSION			
CPF9515	Model 33 to Model 43 with Memory Management Unit	6,000	—
CPF9516	Model 33 to Model 53	18,500	—
CPF9519	Model 43 to Model 47	14,400	—
CPF9520	Model 43 to Model 53	12,500	—
CPF9521	Model 53 to Model 57	22,200	—
CPF9522	Model 47 to Model 57	20,300	—

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
MEMORY			
CMM9307	32K bytes parity MOS memory adapter (Model 23 only)	1,500	10
CMM9308	64K bytes parity MOS memory adapter (Model 23 only)	2,550	20
CMC9009	High-Density Memory Controller with parity, and 64K byte memory-pac (maximum of 4 pacs per controller)	4,700	65
CMM9006	64K byte memory-pac with parity	2,250	34
CMC9010	High-Density Memory Controller with EDAC, and 64K byte memory-pac (maximum of 4 pacs per controller)	4,700	65
CMM9007	64K byte EDAC memory pac	2,250	34
CMC9038	256K byte EDAC memory subsystem (controller and four 64Kb pacs)	7,000	120
MASS STORAGE			
MSC9101	Mass storage controller for up to four cartridge disk drives of same recording density	3,600	16
CDM9101	Device-pac for up to four cartridge disk drives; mounts on MSC9101 controller	1,100	12
CDU9115	5.0-megabyte cartridge disk drive; high-density, one removable, no fixed cartridge; requires DCM9101 Device-Pac	7,000	60
CDU9116	10.0-megabyte cartridge disk drive, high-density, one fixed and one removable cartridge; requires CDM9101 Device-Pac	8,000	80
DIM9101	Diskette device-pac; requires 2-ports, single-sided diskettes	767	5
DIM9102	Diskette device-pac; requires 2-ports, single/double sided diskettes	919	5
DIM9301	Model 23 diskette adapter	1,260	5
DIU9101	Single diskette drive, rack mount	1,785	18
DIU9102	Dual diskette drive, rack mount	2,940	29
DIU9103	Single diskette drive, rack mount, double sided	2,336	21
DIU9104	Dual diskette drive, rack mount, double sided	3,833	32
The following equipment and controllers are for use on Level 6 Models 33 to 57			
CDS9136	26-megabyte cartridge disk with controller, 13-megabytes fixed & 13 megabytes removable, 30-inch cabinet	19,700	116
CDS9123	Rack-mountable version of CDS9136	14,700	116
CDS9137	Two 26-megabyte cartridge disks with controller, 30-inch cabinet	31,700	205
CDS9138	80-megabyte cartridge disk with controller, 67-megabyte fixed & 13 megabytes removable, 30-inch cabinet	21,700	168
CDS9125	Rack-mountable version of CDS9138	21,000	168
CDS9139	Two 80-megabyte cartridge disks with controllers, 30-inch cabinet	35,700	299
CDU9136	Add-on 26-megabyte cartridge disk, 30-inch cabinet	12,700	89
CDU9123	Rack-mountable version of CDU9136	12,000	89
CDU9137	Two add-on 26-megabyte cartridge disks, 30-inch cabinet	24,700	179
CDU9138	Add-on 80-megabyte cartridge disk, 30-inch cabinet	14,700	131
CDU9125	Rack-mountable version of CDU9138	14,000	131
CDU9139	Two add-on 80-megabyte cartridge disks, 30-inch cabinet	28,700	263
CDS9116	10-megabyte cartridge disk with controller, rack-mountable, 5-megabytes fixed & 5-megabytes removable	12,075	113
CDU9116	Add-on 10-megabyte cartridge disk, rack mountable, 5-megabytes fixed & 5-megabytes removable	8,400	84
MSS9102	67-megabyte Mass Storage Unit, includes controller and freestanding cabinet	24,675	168
MSS9104	256-megabyte Mass Storage Unit, includes controller and freestanding cabinet	34,650	242
MSS9107	Two 67-megabyte Mass Storage Units, includes controller and single freestanding cabinet	42,525	284
MSU9102	Add-on 67-megabyte Mass Storage Unit in freestanding cabinet	18,900	116
MSU9104	Add-on 256-megabyte Mass Storage Unit in freestanding cabinet	28,875	189
MSU9107	Two add-on 67-megabyte Mass Storage Units in a single, freestanding cabinet	36,750	231
The following equipment and controllers are for use on Level 6 Model 23			
CDS9336	26-megabyte cartridge disk unit, with controller, 30-inch cabinet	14,280	100
CDS9337	Two 26-megabyte cartridge disk units, with controller, 30-inch cabinet	24,255	189
CDS9338	80-megabyte cartridge disk unit, with controller, 30-inch cabinet	20,580	137
CDS9339	Two 80-megabyte cartridge disk units, with controller, 30-inch cabinet	36,855	268
CDU9136	Add-on 26-megabyte cartridge disk, 30-inch cabinet	10,650	89
CDU9137	Two add-on 26-megabyte cartridge disks, 30-inch cabinet	20,580	179
CDU9138	Add-on 80-megabyte cartridge disk, 30-inch cabinet	16,905	131
CDU9139	Two add-on 80-megabyte cartridge disks, 30-inch cabinet	33,180	263
MAGNETIC TAPE EQUIPMENT			
MTC9101	Magnetic Tape Controller for NRZI tape drives	2,100	21
MTM9102	Device-Pac for four 9-track NRZI tape drives; requires MTC9101	1,050	11
MTU9104	9-track, NRZI, 800-bpi, 45-ips Magnetic Tape Drive	8,400	74
MTU9105	9-track, NRZI, 800-bpi, 75-ips Magnetic Tape Drive	10,500	95
MTM9101	Device-Pac for four 7-track NRZI tape drives; requires MRC9101	1,050	11
MTU9112	7-track, NRZI, 556/800-bpi, 45-ips Magnetic Tape Drive	8,400	74
MTU9113	7-track, NRZI, 556/800-bpi, 75-ips Magnetic Tape Drive	10,500	95
MTC9102	Magnetic Tape Controller and Adapter for up to four PE tape drives	6,930	63
MTU9109	Magnetic Tape Drive; 9-track, 800/1600 bpi, NRZI/PE, 45 ips	11,130	63
MTU9110	Magnetic Tape Drive; 9-track; 800/1600 bpi, NRZI/PE, 75 ips	16,380	126
MTU9114	Magnetic Tape Drive; 9-track, 1600 bpi, PE, 45 ips	8,610	63
MTU9115	Magnetic Tape Drive; 9-track, 1600 bpi, PE, 75 ips	13,125	126

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
PRINTERS			
PRM9101	Printer Device-Pac	500	3
PRM9301	Model 23 Printer Adapter	683	6
PRU9617	Band Printer, 300 lpm, 64 ASCII char. set, VFU	10,500	115
PRU9618	Band Printer, 600 lpm, 64 ASCII char. set, VFU	15,700	170
PRU9109	Line Printer; Drum; 64-character set; 900 lpm	24,150	194
PRF9102	Vertical Format Unit for line printers	945	8
PRU9112	Serial Matrix; 120 cps, 96-character set	3,360	53
PRT1004	Letter quality word processing printer, 55 cps, bidirectional	5,300	59
PUNCHED CARD EQUIPMENT			
CRM9101	Card Reader Device-Pac	600	7
CRM9104	Card Reader/Punch Device-Pac for high speed equipment	840	7
CRU9107	Card Reader, 1050 cpm, requires CRM9104 Device-Pac	12,000	105
CRU9111	Card Reader, 80-column punched cards, 500 cpm; requires CRM9101 Device-Pac	5,930	98
CRU9112	80-column IBM mark sense cards	7,350	98
PCU9101	Punch; 80-column; 100-400 cpm; requires CRM9104 Device-Pac	14,500	137
CCU9101	Reader/Punch; 80-column, 400/100 cpm; requires CRM9104 Device-Pac	16,725	158
TERMINALS			
KCM9101	Keyboard Console Device-Pac	315	5
KCM9302	Dual Console Adapter (Model 23)	525	5
TWU9014	Typewriter Console; 30 cps, 96-character set; requires KCM9101 Device-Pac	2,520	27
TWU9106	TWU9104 except 120-cps version	2,888	46
TWU9108	TWU9104 with numeric keypad	2,625	27
TWU9110	TWU9106 with numeric keypad	2,993	46
DKU9101	Asynchronous CRT/keyboard terminal, 64-character set (VIP7100)	1,500	23
DKU9102	Asynchronous CRT/keyboard terminal, 96-character set (VIP7105)	1,600	24
VIP7700R	Synchronous CRT/keyboard terminal, 64-character set	3,990	33
VIP7705R	Synchronous CRT/keyboard terminal, 96-character set	3,990	33
DKU9103	CRT display/keyboard console, 64 ASCII character set (VIP7200)	1,980	28
DKU9104	CRT display/keyboard console, 96 ASCII character set (VIP7205)	2,100	28
VIP7207	Level 6 data entry keyboard/display terminal	1,980	25
VIP7801	CRT terminal, 96-character set, 24 lines x 80 characters, 12-inch screen	2,885	32
VIP7802	CRT terminal, 139-character set, 24 lines x 80 characters, 15-inch screen	3,195	36
PRU1001	Serial printer, receive-only, 30 cps, 64-character buffer	2,260	28
TWU1001	Serial printer, with keyboard, 30 cps, 64-character buffer	2,470	29
PRU1003	Serial printer, receive-only, 30 cps, 64-character buffer	2,640	39
TWU1003	Serial printer, with keyboard, 30 cps, 64-character buffer	2,850	40
PRU1005	Serial printer, receive-only, 120 cps, 1200-character buffer	3,390	50
TWU1005	Serial printer, with keyboard, 120 cps, 1000-character buffer	2,600	51
COMMUNICATIONS			
MLC9101	Multi-Line Communications Processor for up to eight asynchronous lines; includes four DCM9101 Communications-Pacs	6,000	27
MLC9103	Multi-Line Communications Processor for up to eight lines; does not include Communications-Pac	2,500	13
MLC9104	Multi-Line Communications Processor for up to eight asynchronous lines; includes four DCM9114 Communications-Pacs	6,000	37
DCM9101	Communications-Pac for two asynchronous lines with data rates to 9600 bps; requires MLC9103 control	1,000	6
DCM9102	Communications-Pac for one asynchronous line with data rates up to 9600 bps; requires MLC9103 control	546	3
DCM9103	Communications-Pac for two asynchronous lines with data rates up to 10,800 bps; requires MLC9103 control	1,500	9
DCM9104	Communications-Pac for one synchronous line with data rates up to 10,800 bps; requires MLC9103 control	1,000	5
DCM9105	Communications-Pac for one broad-band line with data rates up to 72,000 bps; requires MLC9103 control	2,000	10
DCM9106	Communications-Pac for one synchronous HDLC line with data rates up to 19,200 bps; requires MLC9103 control	945	12
DCM9108	Communications-Pac for one broad-band line with data rates up to 72,000 bps; CCITT-V35 compatible; requires MLC9103 control	2,000	8
DCM9109	Communications-Pac for one synchronous line; MIL188C-compatible; requires MLC9103 control	1,000	5
DCM9110	Communications-Pac; Autocall unit for one or two synchronous or asynchronous communications lines	1,050	9
DCM9114	Communications-Pac for two current-loop connections with data rates up to 9600 bps; requires MLC9103 or 9104 control	1,000	6
DCM9112	Communications Pac; broadband, HDLC, Bell 301 and 303 compatible; up to 72,000 bps	3,000	15
DCM9113	Communications Pac; broadband, HDLC, CCITT/V35 compatible; up to 72,000 bps	3,000	15
DCM9115	Communications Pac; broadband, synchronous MIL188C compatible; up to 72,00 bps	2,000	10
DCM9116	Communications Pac; dual asynchronous lines, MIL188C compatible; up to 9,600 bps	1,000	6
DCM9120	Communications Pac; HDLC, MIL188C compatible, requires 2 MLC9103 ports	2,500	12
DCM9121	Communications Pac; broadband, HDLC, MIL188C compatible; requires 2 MIC9103 ports	1,995	15
DCM9126	Communications Pac; dual asynchronous lines for Series 3000 terminals	788	13

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.
COMMUNICATIONS (Continued)			
DCM9301	Communications Adapter for two asynchronous lines, up to 9600 baud (Model 23)	1,050	11
DCM9302	Communications Adapter for one synchronous line; up to 9600 baud (Model 23)	1,050	11
DCM9303	Communications Adapter for two asynchronous lines, up to 9600 baud (Model 23)	1,575	13
DCM9304	Communications Adapter for one synchronous line and one asynchronous line, up to 9600 baud (Model 23)	1,208	12
HARDWARE			
CAB9401	4-slot Megabus expansion chassis; includes power supply (Models 33 to 57)	5,000	8
CAB9402	9-slot Megabus expansion chassis; includes power supply (Models 33 to 57)	9,000	11
CAB9035	Free-standing 60-inch cabinet for magnetic tape units	1,129	—
CAB9036	Cabinet; 60 inches of vertical rack space; includes panels and doors	998	—
CAB9010	Extension table wing for 60-inch cabinet	347	—
CAB9037	60-inch Expansion Cabinet	1,103	—
CAB9020	Desk Packaging for Level 6; includes integrated VIP display mounting and tilt-up vertical control mounting	1,470	—
CAB9023	Desk Packaging for Level 6; includes integrated VIP display mounting, desk-top control panel mounting, and vertical cover for processor	1,680	—
CAB9016	30-inch Mini-Rack for processor; includes front and rear doors and tilt-up vertical control panel mounting	630	—
CAB9026	30-inch Mini-Rack Expansion; includes front and rear doors	700	—
CAB9033	Office packaging desktop wing for minimount Model 23, side control	315	—
CAB9034	9022 with full control panel mounted on desktop	525	—

SOFTWARE PRICES

	License Fee	One-Year Support
GCOS 6 MOD 200	$2,090	$633
GCOS 6 MOD 200 Program Development System (PDS), including screen manager, sort, and entry-level COBOL	5,555	1,265
GCOS 6 MOD 400, Release 2.0	3,500	2,500
GCOS MOD 400, Release 2.1	4,500	2,500
GCOS 6 MOD 600	5,610	770
Intermediate-level COBOL; re-entrant	5,170	1,045
GCOS 6 Advanced COBOL	5,395	3,385
Entry-level FORTRAN (formerly MDT FORTRAN)	809	402
Advanced-level FORTRAN	3,025	440
GCOS 6 BASIC Interpreter	1,150	210
GCOS 6 BASIC Interpreter/Compiler	3,125	410
RPG	3,190	693
GCOS 6 Assembler and Macro-Preprocessor	330	44
GCOS 6 Data Entry Facility/Data Entry Facility II	1,540	220
Interactive Entry Facility	220	44
GCOS 6 Remote Batch Facility	990	176
GCOS 6 2780/3780 Workstation Facility	1,804	286
GCOS 6 Programmable Facility/3721	3,300	1,650
GCOS 6 HASP Multi-Leaving Facility	2,420	319
GCOS 6 MOD 200 HASP II Emulator	2,640	319
INFO 6 Data Inquiry/Update	5,000	500
GCOS 6 Sort Utility	292	44
I-D-S/II; under GCOS 6 MOD 600	14,300	1,320
I-D-S/II runtime services	7,700	880
GCOS 6 Transaction Processing Facility (MOD 400)	7,700	770
GCOS 6 TPS 6 Screenwrite Translator	2,860	220
GCOS 6 TPS COBOL Run Time Director	660	110
GCOS 6 Transaction Control Language Facility (MOD 400)	500	32
TDS; under GCOS 6 MOD 600	8,800	990
TDS runtime services	5,500	660
TOTAL 6 Data Base Management System	12,705	1,525
IBM Communications & File Transfer Facility; includes BSC 2780/3780	220	44
Honeywell Communications & File Transfer Facility; features HDLC via remote batch facility, non-polled VIP emulation, polled VIP emulation including remote terminal concentration facility, connection to Honeywell Level 62, 64, 66, and 68 (Multics), and connection to Honeywell Series 6000, 2000, and 200 computer systems.	440	88
Full set of test and verification routines	303	—
Full set of test and verification listings	242	—
Full set of test and verification microfiche listings	121	—