Chapter 9

PDP11

9.1 11/24

This article by Brian Hailstone . . .

9.1.1 11/24 CPU MODULE M7133/M7133-YA

There are two versions of the 11/24 CPU module, the M7133 and the M7133-YA. Both modules are functionally identical and can be freely interchanged. However the modules are physically different and the layout and use of the jumpers and switches are also different.

Table 9–1: Module jumpers and switches

M7133		M7133-YA	
W1		**E128:SW5**	
IN	One stop bit	ON	One stop bit
OUT	Two stop bits	OFF	Two stop bits
W2		**W2**	
IN	Boot on power up	IN	Boot on power up
OUT	Power up via 24	OUT	Power up via 24
W3		**W3**	
IN	Halt instr in kernal ok	IN	Halt instr in kernal ok
OUT	Halt instr trap thru 10	OUT	Halt instr trap thru 10
	SLU2 baud rate select		
W4,W9-W13		**E129:SW1-SW6**	
	See Table 9–2		
	SLU parity select		
W5-W8		**E128:SW3,SW1**	
W5 OUT	SLU1 parity disabled	SW3 OFF	SLU1 parity disabled
W6 OUT	SLU1 even parity		
W7 OUT	SLU2 parity disabled	SW1 OFF	SLU2 parity disabled
W8 OUT	SLU2 even parity		

Table 9–1 (Cont.): Module jumpers and switches

M7133		M7133-YA	
	Boot address at power up		
W14		**W1**	
IN	165000	IN	165000
OUT	173000	OUT	173000
	Baud rate 1 and 2 select		
E135:SW1-SW8		**E121:SW1-SW8**	
M7133 switch pack E135 and M7133-YA switch pack E121 are equivalent. See Table 9–3			
	SLU1 baud rate select		
E124:SW1-SW4		**E129:SW7-SW10**	
	See Table 9–4		
	SLU1 maintenance		
E124:SW5		**E128:SW7**	
OFF	Normal operation	OFF	Normal operation
	18 vs 22 bit addressing		
E124:SW6		**E128:SW8**	
ON	22 bit (normal)	ON	22 bit (normal)

Table 9–2: SLU2 baud rate selection

	M7133				M7133-YA E129		
Transmit	**W11**	**W10**	**W13**	**Transmit**	**SW4**	**SW5**	**SW6**
Receive	**W9**	**W12**	**W4**	**Receive**	**SW1**	**SW2**	**SW3**
Baud rate 1	IN	OUT	OUT	**Baud rate 1**	ON	OFF	OFF
Baud rate 2	OUT	IN	OUT	**Baud rate 2**	OFF	ON	OFF
19.2K Baud	OUT	OUT	IN	**19.2K Baud**	OFF	OFF	ON

Table 9–3: Baud rate selection. E135 or E121

Baud rate 1		**5**	**6**	**7**	**8**
Baud rate 2		**1**	**2**	**3**	**4**
Baud rate	50	ON	ON	ON	ON
	75	ON	ON	ON	OFF
	110	ON	ON	OFF	ON
	134.5	ON	ON	OFF	OFF
	150	ON	OFF	ON	ON
	200	ON	OFF	ON	OFF
	300	ON	OFF	OFF	ON
	600	ON	OFF	OFF	OFF
	1200	OFF	ON	ON	ON
	1800	OFF	ON	ON	OFF
	2000	OFF	ON	OFF	ON
	2400	OFF	ON	OFF	OFF
	3600	OFF	OFF	ON	ON
	4800	OFF	OFF	ON	OFF
	9600	OFF	OFF	OFF	ON
	19200	OFF	OFF	OFF	OFF

Table 9–4: SLU1 baud rate selection

	M7133		**M7133-YA**	
	E124		**E129**	
Transmit	**2**	**1**	**9**	**10**
Receive	**3**	**4**	**8**	**7**
Baud rate 1	ON	OFF	ON	OFF
Baud rate 2	OFF	ON	OFF	ON

Figure 9–1: M7133

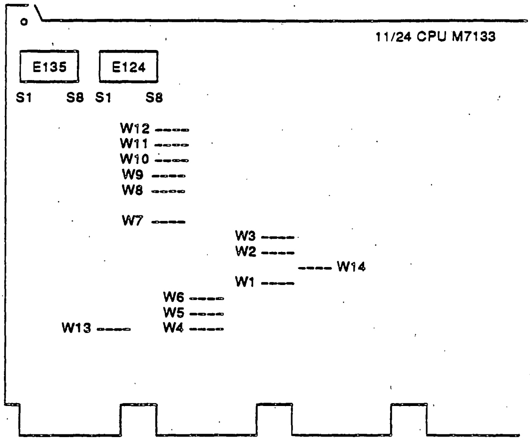
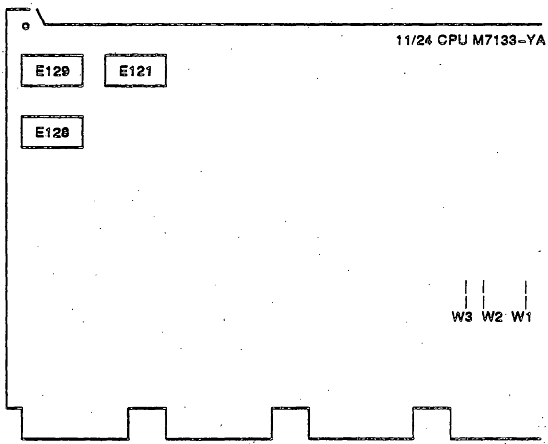


Figure 9–2: M7133-YA



9.2 11/70

This article by Vic Taylor . . .

9.2.1 Bootstrap Error Halts

For the first time in the history of mankind here is a complete list of 11/70 bootstrap error halts for the three possible kinds of boot module.

Table 9–5: 1170 Bootstrap Error Halts

Failing Test	M9301-YC	M9301-YH	M9312
BR	165004	165004	165052
CLR,BMI,BVS,BHI,BLOS	165020	165020	165070
DEC,BPL,BEQ,BGE,BGT,BLE	165036	165036	165104
ROR,BVC,BHIS,BHI,BNE	165052	165052	165116
BHI,BLT,BLOS	165066	165066	n/a
BLE,BGT	165076	165076	n/a
REGISTER DATA PATH	165134	165126	165146
ROL,BCC,BLT	165146	165136	165156
ADD,INC,COM,BCS,BLE	165166	165154	165174
ROR,BIS,ADD,BLO,BGE	165204	165172	165214
DEC,BLOS,BLT	165214	165202	n/a
COM,BLOS	165222	165210	165222
COM,BIC,BGT,BGE,BLE	165236	165224	165234
ADC,CMP,BIT,BNE,BGT,BEQ	165260	165246	165256
BPL	165270	165256	165266
MOVB,SOB,CLR,TST,BNE	165312	165300	165310
ASR,ASL	165346	165334	n/a
ASH,SWAB	165374	165352	n/a
JSR	165510	165376	165322
WRONG VALUE PUSHED ON STACK	165520	165406	165332
RTS	165530	165416	165342
RTI	165542	165430	165354
JMP	165550	165436	165362
MAIN MEMORY DATA ERROR	165742	165520	165460
MAIN MEMORY DATA ERROR	165760	165540	165500
CACHE DATA ERROR	173644	165604	165544
NO CACHE HITS	173654	165614	165554
DATA ERROR CACHE/MAIN MEM	173736	165720	165664
NO CACHE HITS	173746	165732	165676
CACHE OR MAIN PARITY ERROR	173764	165752	165716

9.2.2 M9312 Bootstrap Terminator

This section is for VAXMEN who are not familiar with the PDP11 concept of the "Bootstrap Terminator", some of this covers areas not strictly related but included for completeness. The job of the M9312 is to provide termination for one end of the Unibus (normally the CPU end) AND it has ROMs on it which contain machine code and are addressed like any Unibus device. The M9312 can be set up to run some tests and then boot, if a test fails you get a Halt at one of the addresses above. The M9312 replaced the M9301 series which used to have different variants for different jobs. The flexibility of the M9312 extends to choosing from lots of different BOOT ROMS (for different devices, a maximum of 4 can be fitted in any order) and from 2 CPU ROMs (which run tests etc). I will use the $ sign to signify lots of leading 1s as per the RDC convention.

The starting address of the CPU ROM is $65000; if word $65774 reads out as 041060 all is well - you have the 1170/1160 CPU ROM (23-233F1), but if it contains 040460 then it is a 1134/1104 CPU ROM (23-848F1).

The starting addresses of the 4 BOOT ROMs are $3000, $3200, $3400 and $3600; to determine your configuration Examine the start address of each and compare the contents with the WORD0 column of Table 9–6 notice this is the ascii equivalent of what you would type to Boot the device on an 1134). If the readout is 177776 it means the ROM is missing.

There are several ways to Boot a machine . . .

1. You could try the INIT button, this can be connected to the M9312 faston tabs, and the on-board switch pack can be set to cause a jump to the ROM and consequently run the selected boot code. Normally, however, the switch pack is set to go via 24 (the power-fail vector) on an INIT, so this will not work!

   If the INIT does not work you **MUST KNOW YOUR M9312 CONFIGURATION!** Once you have decided which device you want to boot and which address the relevant BOOT ROM is at, you can go ahead.

2. You can set the Console switch register and Start at $65744. In the switch register D0:8 is an offset address into $3000 (set it up as an OR of the OFFSET column in Table 9–6 and D7:8 of the start address of the relevant BOOT ROM) and D9:11 specifies the unit. This method always runs the tests before booting. For instance to boot RM03 unit 0 when the BOOT ROM (755A9) is at address $3000 just needs 56,$65744G whereas to boot RK07 unit 1 when the BOOT ROM (752A9) is at address $3200 would require 1212,$65744G.

3. You can steam straight into the BOOT ROM at the address in the ENTRY column of Table 9–6, you should add 2 to this entry point to run through the Tests prior to booting. This method will only use unit 0. For instance if the TE16 BOOT ROM was at $3400, a simple $3406G would do the tests and then boot unit 0.

Other minor points about the M9312 . . .

- A faston tab can be connected to the memory battery status, this prevents a vector 24 restart if the memory is known to be empty because the battery has discharged.
- The state of the switch pack can be determined by $3024/ this will return a 1 in D7 to D0 for each of SW3 to SW10. Also if the top digits are 165 it means SW1 is on, 173 means SW1 is off.
- W1 thru W12 are CPU dependent, check these if replacing the M9312

Table 9–6: M9312 Configurations

DEVICE	WORD0	ASCII	OFFSET	ENTRY	ROM
RA	042124	DU	12	4	23767A9
RK6/7	042115	DM	12	4	23752A9
RP/RM	042120	DP†	56	50	23755A9
TE16	046515	MM	12	4	23757A9
TS11	046523	MS	12	4	23764A9

†Note DP because the RP02 is also supported by this ROM

Note

A fuller list of M9312 Configurations can be found in the 1134 or 1144 Pocket Guides

9.2.3 Booting second RH70

If the M9312 tests pass but you are still having problems (normally the cpu is looping for instance) you would Halt the cpu and see what the PC was set to. At some stage you may decide to attempt a boot by putting a disc drive on the second RH70 which lives at $6300 on the unibus.

```
$6302/ xxxxxx 177000 (L/F)    ......sets word count
       xxxxxx      0 (L/F)    ......sets bus address
       xxxxxx      0 (L/F)    ......sets disk address
       xxxxxx      0 (C/R)    ......sets unit 0
$6300/ xxxxxx     23 (C/R)    ......sets pack ack
$6312/ 010700 (C/R)   .............shows o/k
    0/ xxxxxx 012345 (C/R)    ......set a known pattern
$6300/ xxxxxx     73 (C/R)    ......starts the read
    0/ 000240 (C/R)   .............shows o/k
```

Now you have the first sector in memory o/k (if not look at the RH70 registers to see what went wrong), if you have the latest software it will be able to run from the second RH, do a 0G to proceed.

9.2.4 11/70 Hints and Tips

This article by Vic Taylor . . .

9.2.4.1 11/70's and DECX11

When you run DECX11 on an 11/70 with MK11 memory it disables ECC correction in MK11 which means any Single Bit errors will cause a fatal Double Bit error,this is OK while testing a machine but when you stop DECX11 it does not re-enable ECC correction,so if you now give the machine back to the customer any SBE will cause a fatal error instead of being corrected. So after running DECX11 on an 11/70 you have to re-enable ECC correction by one of the following methods . . .

1. Run EMKA and halt in the correct way by putting 400 in SWR.
2. Manually deposit 1 in the first MK11 CSR.
3. Power off/on the MK11 box.

9.2.4.1.1 DECX11 using XMONE0.LIB monitor E

DECX11 RTE using XMONE0.LIB monitor "E" appears to hang on an 11/70.

The symptoms are :-

All diagnostics seem to run. If DECX11 RTE is run, XXDP types the filename then nothing appears to happen, the 11/70 is however "running". If the CPU is halted and singled-stepped round the loop the PC's will typically be 65526-65530 (different PC's for different configurations).

The problem is due to a bug, which mis-manages memory management.

This problem does not occur in XMONF0.LIB.

9.2.4.2 False Cache Data Parity Errors

Because the 11/70 stores the parity generated by main memory as the parity on the data cache, if you have a main memory error the bad parity will be written into the cache, this means that you can then get a false cache data parity error, so if you get cache data parity errors coincident with main memory parity errors you can safely ignore the cache data parity errors.

9.2.4.3 Main Memory Address Parity Error

On both MJ11 and MK11 memories the Address parity error led on the control modules is a non resettable latch, this means that the only way to clear the led is to power off. The implication of this is that diagnostics set this latch so unless you are sure that the led was off when the machine was last given back to the customer you CANNOT believe the led.

9.2.4.4 MJ11 Troubleshooting

Because the 11/70 always reads two words at a time, when you get a parity error from MJ11 memory it may not be in the word you requested, this means that the address latched in the HI and LO error address registers will not correctly reflect whether the error was in the even or odd word (i.e words that end in 0,4 are even words and words that end in 2,6 are odd words). So to determine the actual failing stack you have to look in the memory error register to determine if the error was in the odd or even word (bits 2 and 3) and then use the address in the HI and LO error address registers to work out the area of memory it is in.

For example . . .

```
Memory error register = 104004
LO error address register = 030112
HI error address register = 000002
```

Combining the lo and hi error address registers results in a address of 430112 which is in address range 64-128Kw. This address implies the failure is in the odd word because it ends in 2 but by examining the memory error register you see that in fact bit 2 is set which means the error was actually in the even word. So the fault would be in the LO (even) stack that lies in address range 64-128Kw.

9.2.4.5 MK11 Array in error determination

When a Double Bit Error occurs in MK11 the array being accessed at the time is latched in the MK11 csr's. You determine the array number using bits 5-7 of CSR1 and bit 9 of CSR2 as follows . . .

Table 9–7: MK11 Bit In Error Determination

	CSR1			CSR2	Array in
Bit Number	7	6	5	9	Error
	0	0	0	0	0
	0	0	0	1	1
	0	0	1	0	2
	0	0	1	1	3
	0	1	0	0	4
	0	1	0	1	5
	0	1	1	0	6
	0	1	1	1	7
	1	0	0	0	8
	1	0	0	1	9
	1	0	1	0	10
	1	0	1	1	11
	1	1	0	0	12
	1	1	0	1	13
	1	1	1	0	14
	1	1	1	1	15

9.2.4.6 System Size register Switches

As you know the system size register on the M8140 should reflect the amount of memory you actually have, page 3-43 of the 11/70 maintenance manual and page SCCN of M8140 printset drawing describe how to set these switches but both have the same error in them, which is as follows, the drawing of the switch pack shows W9,W13,W14,W10,W16,W15,W12,W11 LEFT TO RIGHT but it should be W9,W13,W14,W10,W16,W12,W15,W11.

9.2.4.7 Memory Bus Cabling

On MJ11 and MK11 memory systems the cabling is as follows,at the cpu end the four memory cables should be installed RIBBED SIDE UP with the red stripe towards the module handles. At the memory box end the four cables should be installed SMOOTH SIDE UP with the red stripe towards the front of the box.

The cables that are used are BC06R's.

9.2.5 Modifications to the 11/70 by SYSTIME

All 11/70's with Systime 5311 disk controllers have been modified to stop false memory type problems due to timing problems with the 11/70 and this disk controller.

So BEWARE when changing cpu modules or the backplane or option swapping a system that these changes must be done.

There are three elements that are modified as follows :-

- The CPU Backplane.
- The M8136 cpu unibus control module.
- The M8142 cache control module.

9.2.5.1 Backplane Modification

The backplane has a wire added between SLOT 12 pin DC1 and SLOT 17 pin FB1.

9.2.5.2 M8136 Modifications

The M8136 has three wires and a resistor added as follows :-

- Add wire from E61 pin 13 to edge connector DC1.
- Add wire from E61 pin 12 to E80 pin 3.
- Add wire from E61 pin 11 to E45 pin 9.
- Add 330 ohm resistor across E61 pins 13 and 14.

9.2.5.3 M8142 Modifications

The modifications to the M8142 are quite extensive as follows :-

- Two extra chips have been added E114 (type 74S08) and E107 (type 74S112).
- Add wire from E107 pin 15 to E94 pin 14.
- Add wire from E107 pin 1 to E94 pin 13.
- Add wire from E107 pin 4 to E94 pin 10.
- Add wire from E107 pin 3 to E114 pin 8.
- Add wire from E107 pin 5 to E48 pin 10.
- Add wire from E107 pin 2 to edge connector FB1.

- Add wire from E114 pin 1 to E95 pin 8.
- Add wire from E114 pin 2 to E48 pin 8.
- Add wire from E114 pin 3 to E90 pin 3.
- Add wire from E114 pin 9 to E85 pin 5.
- Add wire from E114 pin 10 to E108 pin 5.
- Add wire from E91 pin 6 to E48 pin 9.

9.3 11/84

This article by Vic Taylor . . .

9.3.1 11/84 Known Problems

9.3.1.1 M8191 (UBA)

When using a KMC11 to poll a DZ11 or a DUP11 the 1184 operating system will crash, replacing the M8191 with a rev B1 or later cures the problem.

9.3.1.2 11/84's and TU80's

11/84's with the UBA (M8191) at etch E and cs B will give write errors on TU80's under software and Decx.(non existent mem errors), FCO TU80-R-011 on speed bulletin 405 fixes this problem.This is a simple wiring change to the TU80 M7454.

9.3.1.3 BATTERY BACKUP SUPPORT (H7231-E/F)

Battery Backup is not supported on the 1184 unless you have the following modules.

- MSV11-J memory modules.
- M7677-YA MDM module.
- Front panel (54-16196-01) rev B1 or later.

9.3.1.4 11/84's AND EMULEX SC21'S

Emulex SC21's on 11/84's can cause flakey problems. An Emulex SC21 on an 11/84 is a unsupported configuration. Install an Emulex SC31 instead.

9.3.1.5 LINE TIME CLOCK

There is a problem with 11/84's where the line time clock appears to run fast. This only occurs when Parameter H in setup command 2 is set to "0". "0" tells the CPU to use the line clock signal from the power supply. The solution is to set Parameter H to "1", which tells the CPU to use an internal 50Hz clock.

This problem affects both the 15Mhz and 18Mhz versions.

It is important that this parameter is check at installation and on the replacement of the CPU module as the default setting is "0".

9.3.1.6 DHU11 DIAGNOSTIC ZDHX

The DHU11 diagnostic ZDHX may fail the DMA test on some 11/84's there is cuurrently no fix for this.

9.3.2 MINIMUM LOAD MODULE (MLM M7556)

Power supply's require a minimum of 370 millamps at -15 volts and a minimum of 2 amps at +5 volts VBB. If these requirements are not closely watched the system will become flakey. These load modules must be removed if the power requirements are met. The only exception is when one memory module is used, that load module has to stay in the empty memory slot.

9.3.2.1 Requirements for having load modules

1. If there is only one PMI memory (slot 2) in the system. (This applies to MSV11-J only as MSV11-R draws enough current)
2. If the total current drawn (active or nonactive) in the CPU Backplane (slots 5 thru 12) on -15 volts is less than 1.0 amp.
3. In the case of an expansion backplane in the system cabinet, if the same condition exists as in (2) for -15 volts. (This applies to the cabinet version only as there is no room for an expansion backplane in the box version)

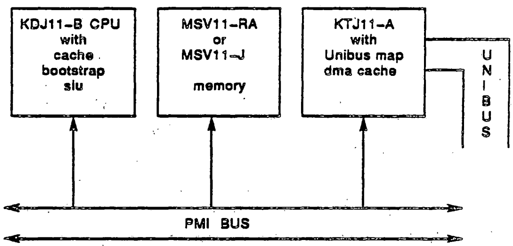
9.3.2.2 Where to install load modules

1. Install MLM (M7556) in rows C and D of slot 3.
2. Install MLM (M7556) in rows E and F of slot 12.
3. Install MLM (M7556) in last SPC slot rows E and F.

9.3.3 1184 General Information

The 11/84 is based around the KDJ11-BF processor which is used in the 11/83.The 11/84 has a Unibus adapter module and a private memory bus (PMI).There are two versions of the 11/84 the 11/84A and the 11/84P . The 11/84A is the 18Mhz version which has hot floating point. The 11/84P is the 15Mhz version which has warm floating point. You will mainly see 11/84A's.

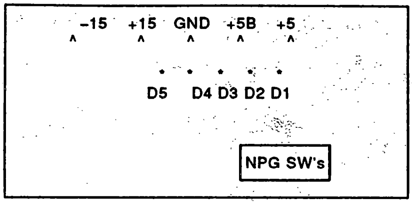
Figure 9–3: Block Diagram



9.3.4 MDM MODULE

The MDM module has four main functions,it has easily accessible voltage test points,it has five leds to indicate voltage presence, it has a switch pack to set NPG jumpers on the cpu backplane and it has an audible alarm to notify when a fan or blower stops and is normally accompanied by an error 25 on the front panel.

Figure 9–4: MDM Module Layout



The four voltage test points are for the CPU power supply only.

9.3.4.1 MDM NPG switches

```
The MDM module has an eight pole dip switch for configuring
the NPG jumpers on the cpu backplane the layout is as follows :-

        12  11  10  9  8  7  6  5    Slot numbers
       ---------------------------
       +        NPG Switches     +     on  = jumper in
       ---------------------------     off = jumper out
```

9.3.4.2 MDM Leds

D1 = Main +5V ok
D2 = Main +5VB/+12V ok
D3 = Main +/-15V ok
D4 = Expansion +5V ok (will not be on if no expansion supply)
D5 = Expansion +/-15V ok (will not be on if no expansion supply)

9.3.5 CPU Switches and Jumpers

The M8190 cpu module has several jumpers,these are factory set and should never need to b
touched.

The M8190 cpu module has an 8 pole dip switch E83,these switches should always be off.

The M8190 cpu module has a green led to indicate DC OK and six red leds which correspond t
the front panel error codes in octal,the most right hand led with component side up being th
LSB.

9.3.6 UBA Boot Roms

The UBA module M8191 has M9312 compatibility and so has four rom sockets for bootroms a
follows :-

ROM	SOCKET	ADDRESS
1	E145	173000-173176
2	E144	173200-173376
3	E143	173400-173576
4	E142	173600-173776

The purpose of the M9312 compatibility is to be able to provide boot roms for devices no
supported by the cpu on board rom.

9.3.7 Part Numbers

Part #	Description
M8190-AE	KDJ11-BF cpu module (18Mhz)
M8190-AB	KDJ11-BC cpu module (15Mhz)
M8191	KTJ11-B uba adapter module
M7677	MDM module
M7677-YA	New MDM module
M7458-A	MSV11-RA 1Mb parity memory
M8637-BA	MSV11-JB 1Mb ecc memory
M8637-CA	MSV11-JC 2Mb ecc memory
M7556	Minimum Load module
70-20650-01	Cpu backplane
54-16058-01	Console slu board
H7202-KA	Power supply (Not a FRU)
H7202-KB	Expansion psu for cabinet version (Not a FRU)
H7211	+/- 15V regulator
H7213	+12V and +5VBB regulator
H7200	+5V regulator
H7231-E	Battery Backup Unit
70-21888-01	Front panel assembly
12-22001-01	Blower for cabinet version
12-22271-02	Fan for box version

9.3.8 Module Utilisation

	M7677/M7677-YA (MDM)	
Slot 1	M8190-AB/M8190-AE (cpu)	
Slot 2	MSV11R / MSV11J	
Slot 3	MSV11R / MSV11J / MLM	
Slot 4	M8191 KTJ11-B UBA	
Slot 5	Hex or Quad Unibus option	
Slot 6	Hex or Quad Unibus option	
Slot 7	Hex or Quad Unibus option	
Slot 8	Hex or Quad Unibus option	
Slot 9	Hex or Quad Unibus option	(MUD)
Slot 10	Hex or Quad Unibus option	(MUD)
Slot 11	Hex or Quad Unibus option	(MUD)
Slot 12	Unibus out Quad Unibus option	

9.3.9 Diagnostics

```
OKDA??          KDJ11-B cpu diagnostic
OKTA??          KTJ11-B uba diagnostic
VMJA??          MSV11R and MSV11J memory diagnostic
```

```
OKDA rev B0 will fail several tests if the console terminal
is set  below 9600 baud.
OKDA rev C0 runs o.k
OKDA rev D0 has a similar problem to rev B0,the patch is below :-

OKDAD0 patch    Location        From            To
                --------        ----            --
                4614            30104           31104
                46634           157776          147776
                122470          150000          175000

OKDAE0 patch    Location        From            To
                --------        ----            --
                26506           177737          177761
                27262           177737          177761
                27516           177737          177761

n.b      If OKDA or OKTA halt or you halt them you must do the following
         before restarting at 200 or else reboot ,

         Deposit    0   in 17777572
         Deposit 1000   in 17777520
         Deposit  400   in 17777746

         OKDAG0 works ok and should be used wherever possible as it
         also checks for the FPJ11 fco.
```

9.3.10 Decx11

Decx library XMONF0.LIB supports the 11/84 under monitor E. There are two new commands under decx for the 11/84 " EON" and "EOFF" these are ECC ON and ECC OFF for the new MSV11-J ecc memories.

When Decx starts it turns off ECC,so single bit errors will cause a trap through 114. To stop this issue the "EON" command.

9.3.11 Power supplies

The base power supply is a H7202-KA which is found in the box and cabinet versions,it consists of three regulators H7200,H7211,H7213.

The H7200 regulator generates the main +5V and LTC and ac/dc lo and also controls the other two regulators.

The H7211 regulator generates +/- 15V.

The H7213 generates +5VB,which is only used by the memory,and +12V which is only used by the fans/blower.

The H7202-KB is the expansion power supply used in the cabinet version,it is basically the same as the H7202-KA except it does not have the H7213 regulator in it.

9.3.11.1 Power supply ratings

```
CPU power supply H7202-KA (Supplies CPU backplane only)

          +5V at 60 Amps
          +15V at 2 Amps
          -15V at 3 Amps
          +12V at 3 Amps (Used by fans only)
          +5VB at 15 Amps (Used by memories only)

Expansion power supply H7202-KB (Cabinet Versions only)
```

```
+5V at 32 Amps
+15V at 2 Amps
-15V at 3 Amps
```

9.3.12 Register information

9.3.12.1 CPU Registers

9.3.12.1.1 CPU Error Register(Address 17777766)

```
15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
-----------------------------------------------------------------
! 0 ! 0 ! 0 ! 0 ! 0 ! 0 ! 0 ! 0 !   !   !   !   !   !   ! 0 ! 0 !
-----------------------------------------------------------------
                                  !   !   !   !   !   !
                                  !   !   !   !   !   !
illegal halt            ----------!   !   !   !   !   !
odd address error       --------------!   !   !   !   !
main memory timeout(nxm)------------------!   !   !   !
i/o page timeout        ----------------------!   !   !
yellow  stack violation --------------------------!   !
red stack violation     ------------------------------!
```

9.3.12.1.2 Maintenance Register(Address 17777750)

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
-----------------------------------------------------------------
! 0 ! 0 ! 0 ! 0 ! 0 !   ! 1 !   ! 0 ! 0 ! 1 ! 0 !   ! 1 ! 0 !   !
-----------------------------------------------------------------
        reserved     -!   !   !   !   !   !   !   !   !   !   !
   unibus system        --!   !   !   !   !   !   !   !   !   !
   fpa available        ------!   !   !   !   !   !   !   !   !
                        ----------!   !   !   !   !   !   !   !
bits 7-4 are            --------------!   !   !   !   !   !   !
module type (fixed)     ------------------!   !   !   !   !   !
halt/trap option        ----------------------!   !   !   !   !
bits 2-1 are            --------------------------!   !   !   !
power up option(fixed)  ------------------------------!   !   !
        bpok H          ----------------------------------!
```

9.3.12.1.3 Memory Error Register(Address 17777744)

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
-----------------------------------------------------------------
!   !   !   ! 0 ! 0 ! 0 ! 0 ! 0 !   !   !   ! 0 ! 0 ! 0 ! 0 ! 0 !
-----------------------------------------------------------------
  !   !   !                       !   !   !   !
  !   !   !--DTS par              !   !   !   !---Cache dma tag PE
  !   !------DTS cmp              !   !   !-------Cache cpu tag PE
  !----------cpu abort            !   !------Cache lo byte data PE
                                  !----------Cache hi byte data PE
```

n.b Bit 3 of the memory error register "Cache dma tag parity error" does NOT refer to the dma cache on the KTJ11-B, it refers to the dma tag on the cpu module.

Bits 13 and 14 are for diagnostic use.

9.3.12.1.4 Cache Control register(Address 17777746)

```
     15   14   13   12   11   10    9    8    7    6    5    4    3    2    1    0
    -----------------------------------------------------------------------------
    ! 0 ! 0 ! 0 ! 0 ! 0 !    !    !    !    !    ! 0 ! 0 !    !    !    !    !
    -----------------------------------------------------------------------------
                           !    !    !    !    !              !    !    !    !
write wrong tag parity ---!    !    !    !    !              !    !    !    !
        cache bypass   -------!    !    !    !              !    !    !    !
        flush cache    -----------!    !    !              !    !    !    !
parity error abort     ---------------!    !              !    !    !    !
write wrong data parity-------------------!              !    !    !    !
                                                          !    !    !    !
                                                          !    !    !    !
force cache miss       -----------------------------------!    !    !    !
force cache miss       ----------------------------------------!    !    !
diagnostic mode        ---------------------------------------------!    !
disable cache parity trap------------------------------------------------!

n.b     Bits 2 and 3 (force cache miss) both do the same thing
```

9.3.12.1.5 Boot and Diagnostic CSR(Address 17777520)

```
     15   14   13   12   11   10    9    8    7    6    5    4    3    2    1    0
    -----------------------------------------------------------------------------
    !    ! 0 !    !    !    !    !    !    !    !    !    !    ! 0 !    !    !    !
    -----------------------------------------------------------------------------
      !         !    !    !    !    !    !    !    !    !    !         !    !    !
BBU reboot      !    !    !    !    !    !    !    !    !    !         !    !    !
  enable        !    !    !    !    !    !    !    !    !    !         !    !    !
Force LTC  ---!    !    !    !    !    !    !    !    !    !         !    !    !
Disable LTC reg --!    !    !    !    !    !    !    !    !         !    !    !
Clock sel 1      ---!    !    !    !    !    !    !    !         !    !    !
Clock sel 2      -------!    !    !    !    !    !    !         !    !    !
Enable halt on brk -----------!    !    !    !    !    !         !    !    !
Standalone mode  ---------------!    !    !    !    !         !    !    !
Disable 173000   -------------------!    !    !    !         !    !    !
Disable 165000   -----------------------!    !    !         !    !    !
Rom 3 at 165000  ---------------------------!    !         !    !    !
Rom 3 write enable -------------------------------!         !    !    !
                                                             !    !    !
PMG cnt2         --------------------------------------------!    !    !
PMG cnt1         -------------------------------------------------!    !
PMG cnt0         ------------------------------------------------------!

        This register is loaded from the information in the parameter
        table from Setup 2 .Refer to Setup 2 for more information.
```

9.3.12.2 KTJ11-B Registers (UBA)

9.3.12.2.1 Memory Configuration register(Address 17777734)

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
-----------------------------------------------------------------
!   !   !   !   !   !   !   !   !   !   !   !   !   !   !   !   !
-----------------------------------------------------------------
  !                       !   !   !   !   !   !               !
  !                       !   !   !   !   !   !               !
  !-----------------------!   !   !   !   !   !---------------!
             !                !   !   !   !           !
        DMA cache             !   !   !   !     Unibus memory
       status bits            !   !   !   !         size
                              !   !   !   !
                              !   !   !   !
select status           ------!   !   !   !
reboot pulse            ----------!   !   !
dma cache enable        --------------!   !
18 bit mode             ------------------!
```

n.b Bits 0-4 are the octal representation of the number of 8Kb banks on the Unibus starting at 757777 and working down. Bits 9-15 are not of much interest.

9.3.12.2.2 Diagnostic CSR(Address 17777730)

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
-----------------------------------------------------------------
!   ! 0 ! 0 ! 0 ! 0 ! 0 ! 0 !   !   ! 0 ! 0 ! 0 !   !   !   !   !
-----------------------------------------------------------------
  !----Diag mode NXM          !   !               !   !   !   !
                              !   !               !   !   !   !
 Diagnostic mode        ------!   !               !   !   !   !
 Diag NPR done          ----------!               !   !   !   !
                                                  !   !   !   !
                                                  !   !   !   !
 Boot rom disable       --------------------------!   !   !   !
 DDR select             ------------------------------!   !   !
 DDR select             ----------------------------------!   !
 Diag dati go           --------------------------------------!
```

n.b Bits 1 and 2 are used to select the contents of the diagnostic data register.

9.3.12.2.3 Diagnostic data register(Address 17777732)

```
 15  14  13  12  11  10   9   8   7   6   5   4   3   2   1   0
-----------------------------------------------------------------
!   !   !   !   !   !   !   !   !   !   !   !   !   ! 0 !   !   !
-----------------------------------------------------------------
                                  !   !   !   !   !       !   !
                 MSYN       ------!   !   !   !   !       !   !
                 SSYN       ----------!   !   !   !       !   !
                 PB         --------------!   !   !       !   !
                 C1         ------------------!   !       !   !
                 C0         ----------------------!       !   !
                                                          !   !
                                                          !   !
                 A17        ------------------------------!   !
                 A16        ----------------------------------!
```

Note

The bit positions shown above are for when DCSR bits 1 and 2 are a 1

The contents of this register depends on the DDR select bits in the DCSR.

DCSR DDR select bits Bit 2	Bit 1	
0	0	Diagnostic npr register
0	1	Unibus data lines D15-0
1	0	Unibus address lines A15-0
1	1	Unibus address lines A17-16 and various unibus control lines.

9.3.13 Memory Switch Settings

9.3.13.1 MSV11-RA

There is only one switch pack on MSV11-RA's, switches 3,4 are not used and should be off.

SW1	SW2	Starting Address	
off	off	00000000	(0-512Kw)
off	on	04000000	(512-1024Kw)
on	off	10000000	(1024-1536Kw)
on	on	14000000	(1536-2048Kw)

SW5	SW6	SW7	SW8	CSR Address
on	on	on	on	17772100
on	on	on	off	17772102
on	on	off	on	17772104
on	on	off	off	17772106

9.3.13.2 MSV11-J

There are two switch packs on MSV11-J's, switch pack 1 is for the starting address, switch pack two is for the csr address.

Switch pack 1

1	2	3	4	5	6	7	8	Starting Address
off	off	off	off	off	off	off	off	00000000 (0Kw)
off	on	off	off	off	off	off	off	04000000 (512Kw)
on	off	off	off	off	off	off	off	10000000 (1024Kw)
on	on	off	off	off	off	off	off	14000000 (1536Kw)

Switch Pack 2

1	2	3	4	CSR Address
off	off	off	off	17772100
off	off	off	on	17772102
off	off	on	off	17772104
off	off	on	on	17772106

9.3.14 Console commands

```
There are six console commands as follows :-

    HELP       Type short help text.
    BOOT       Boot a device.
    LIST       List available boot roms and where they reside.
    SETUP      Enter setup mode.
    MAP        Print memory size and i/o page addresses that respond.
    TEST       Do continuous self test.

    All commands can be abbreviated to one letter.
```

Console commands are issued in what is termed "DIALOG MODE",there are three ways of entering dialog mode,firstly by setting parameter C in the set up table to a 0 so that a restart will enter dialog mode,secondly by typing a CONTROL C during the power up/restart self test and lastly by putting the FORCE DIALOG MODE slide switch at the rear of the machine into the on position.

9.3.14.1 Boot Command

```
There are three switches applicable to the boot command,they are
as follows :-

       /A       To enter non-standard CSR address

       /U       If a boot rom exists on the cpu and the UBA
                it forces the use of the UBA rom.

       /O       The unit number is octal instead of decimal
                for unit numbers greater than 7

Examples :-

       B DU0/A                 !Boot DU0 at address 17760400
       Address = 17760400

       B DU10/O                !Boot DU unit 8 (Decimal)

       B DU8/U                 !Boot DU unit 8 using UBA rom

       B DU11/OU               !Boot DU unit 9 using UBA rom
```

9.3.14.2 Test Command

```
The Test command will continually run test 70 through 30 until
a CONTROL C is typed.

You can continually run one test by typing a test number after the
command,(i.e T 60 will continually run test 60).
```

9.3.14.3 Setup Command

```
The setup command enters the setup mode where various parameters can be
tailored for each particular system.

The setup mode commands are :-

   Command                              Description
   =======                              ===========
```

```
 1                          Exit setup mode
 2                          List/change setup table
 3                          List/change boot translations
 4                          List/change Automatic boot table
 5                          Reserved
 6                          List/change switch boot selections
 7                          List boot programs
 8                          Initialize setup table
 9                          Save setups into EEPROM
10                          Load EEPROM data into setup table
11                          Delete an EEPROM boot
12                          Load an EEPROM boot into memory
13                          Edit/create an EEPROM boot
14                          Save boot into EEPROM
15                          Enter ROM odt
```

In the following paragraphs commands 1,2,3,4,7,8,9 will be described,for information on commands 10-15 refer to the 11/84 technical manual. During set up mode commands 2,3,4 CONTROL Z can be typed at anytime to exit that command without loosing any changes you have made.

9.3.14.3.1 Set up command 1

Set up command 1 exits setup mode and returns to console dialog mode.

9.3.14.3.2 Set up command 2

Set up command 2 enables you to list and/or change the set up table. The setup table is self explanatory and the only parameters you are likely to need to change are A,B,C,H .

Parameter A is to tell the boot rom whether you have a VDU or a hardcopy terminal as the console device.

Parameter B is to decide what action to take on power up
(normally a 1)

Parameter C is to decide what action to take on a restart
(normally a 1)

Parameter H is to determine the frequency of the line time clock
(normally a 1 in the UK)

9.3.14.3.3 Setup Table Typical example for UK

```
A - ANSI Video terminal          0=NO    1=Yes    =0
B - Power up  0=Dialog,1=Automatic,2=odt,3=24     =1
C - Restart   0=Dialog,1=Automatic,2=odt,3=24     =1
D - Ignore battery               0=NO    1=Yes    =0
E - PMG 0-7 1=.4us,2=.8,3=1.6,4=3.2..7=25.6       =7
F - Disable clock csr            0=NO    1=Yes    =0
G - Force clock interrupts       0=NO    1=Yes    =0
H - Clock 0=power supply,1=50Hz,2=60Hz,3=800Hz    =1
I - Enable ecc test              0=No    1=Yes    =1
J - Disable long memory test     0=NO    1=Yes    =0
K - Disable rom 0=NO,1=dis 165,2=dis173,3=both    =0
L - Enable trap on halt          0=NO    1=Yes    =0
M - Allow alternate boot block   0=NO    1=Yes    =0
N - Disable setup mode           0=No    1=Yes    =0
O - Disable all testing          0=No    1=Yes    =0
P - Enable Unibus memory test    0=No    1=Yes    =1
Q - Disable uba rom              0=No    1=Yes    =0
R - Enable uba cache             0=No    1=Yes    =1
S - Enable 18 bit mode           0=No    1=Yes    =0
```

9.3.14.3.4 Set up command 3

Set up command 3 is used to configure the boot translation table,this is used where non standard CSR addresses are used. You can set up to nine translations,you enter the device name and number and its base CSR address and optionally its real unit number.

```
An example :-

                Device name      = DL
                Unit number      = 4 0
                CSR address      = 17760400

            In the above typing boot DL4 would result in DL0 at
CSR address 17760400 being booted.  If the second unit number is
not specified it would mean that 4 is the real unit number.
```

9.3.14.3.5 Set up command 4

Set up command 4 is used to select the device/s that are to be tried to be booted on an automatic restart (i.e Setup parameter B or C is a 1).

There are six possible boot selections and they are tried in order. Besides device names there are four special mnemonics they are as follows :-

```
A  =   Boot the first bootable disk MSCP device found.
       (This can cause booting to take some while so use the
        specific device name where possible i.e DU0)

B  =   Transfer control to a boot rom on the unibus (i.e a M9312)

E  =   This is to signify that there are no more devices to try
       and to exit the automatic boot.

L  =   This also means that there are no more devices to try but
       it will keep trying the devices in the boot table.

An example to keep trying to boot DU0 on power up or restart :-

          Boot 1 = DU0
          Boot 2 = L     (i.e Loop)
          Boot 3 = xx
          Boot 4 = xx           (Where xx can be anything because
          Boot 5 = xx            the L in boot 2 tells it to loop
          Boot 6 = xx            back to Boot 1)
```

9.3.14.3.6 Set up command 7

Set up command 7 does the same as the "LIST" command in console dialog mode.

9.3.14.3.7 Set up command 8

Set up command 8 initializes the setup table,boot translations and automatic boot table to there default values,it DOES NOT change the EEPROM,you have to subsequently issue a command 9 to set the default values into the EEPROM.

9.3.14.3.8 Set up command 9

Set up command 9 saves any changes made using commands 2,3,4,6,8 into the EEPROM.

Note

THIS COMMAND MUST BE USED TO EFFECT A PERMANENT CHANGE TO THE SETUPS.

9.3.15 Front Panel

9.3.15.1 Rotary Switch

OFF	=	Power supplies are turned off
ENABLE	=	Power supplies are on
SECURE	=	Same as enable except the console HALT ON BREAK feature and HALT/RUN/RESTART switch are DISABLED.
STANDBY	=	Power is supplied to PMI memory and fans but other voltages are off.

9.3.15.2 Halt/restart/run switch

HALT	=	The cpu is halted and enters ODT.
RUN	=	Enables the cpu to execute instructions.
RESTART	=	This is a momentary switch to initiate the bootstrap sequence.

9.3.15.3 Front panel indicators

```
RUN     =   ON =  The cpu is executing instructions.
           OFF =  The cpu is halted or is in an interrupt wait.
                  Extended DMA also extinguishes the run light.

DC ON   =   ON =  DC is on and all voltages are ok.
           OFF =  DC voltages are not present or not in tolerance.

BATTERY =   ON =  Battery is present and charged to >80%.
    SLOW BLINK = Battery is at <80% and charging.
    FAST BLINK = Battery is either fully discharged or not present.
```

9.3.16 Front panel error codes

On power up and on restart the 11/84 does a series of self tests,if a failure is detected it leaves the failing test number in the front panel display. And may printout some error text on the console.

Note

IF AN UNEXPECTED TRAP OCCURS DURING A TEST THE TEST NUMBER PLUS 100(OCTAL) IS PRINTED OUT IN THE ERROR MESSAGE.

ERROR CODE	TEST DESCRIPTION	PROBABLE CAUSE/S
77	Initial power up value	Halt switch on. Power supply. Terminator. MDM Module. M8190. A BG or NPG line is open.(i.e grant card out or NPG jumper missing)
76	First cpu test,MMU register tests.	M8190
75	Turn on MMU. Run MMU cpu tests.	M8190
74	Turn on/off PMI.	M8190 or M8191.
73	Power up to ODT.	Not a failure.
72	Power up to 24.	M8190 or M8191.
71	EEPROM checksum tst.	M8190.
70	CPU rom checksum and PCR tests.	M8190.
67	Misc CPU and EIS tst.	M8190.
66	Console SLU test 1.	M8190.
65	Console test 2.	M8190.
64	Console test 3.	M8190.
63	Test MMU aborts.	M8190.
62	Standalone mode cpu cache tests	M8190.
61	LTC Clock test	M8190 or PSU
60	Floating point tsts.	M8190.
57	Unused.	
56	Exit standalone mode, Check 17760000 for timeout.	M8190/M8191
55	UBA register response test,check unibus for hung lines.	M8190/M8191/Hung Unibus
54	Memory size test.	Unibus failure.
53	Check memory present at location 0	PMI memory.
52	0-4K word memory tst.	PMI memory/M8190.
51	Cache testing using PMI memory.	M8190
50	Memory test 1.	PMI memory.
47	Memory parity/ecc tst	PMI memory.
46	Memory addr/short tst	PMI memory.
45	UBA rom response test	M8191.
44	UBA map registers data path test	M8191.
43	UBA unmapped diag cycles test	M8191.
42	UBA mapped diag cycles test	M8191.
41	UBA floating addr data tests	M8191.
40	UBA address overflow test	M8191.
37	UBA cache data test.	M8191.
36	UBA cache LRU test.	M8191.
35	UBA TAG test.	M8191.
34	UBA cache parity error detect test	M8191.

ERROR CODE	TEST DESCRIPTION	PROBABLE CAUSE/S
33	Unibus memory data path test	Unibus memory/M8191.
32	Unibus memory parity logic test	Unibus memory.
31	Unibus memory addr shorts test	Unibus memory.

Note

With the exception of codes 25,22,6 ,codes 30 through 1 are bootstrap problem indications not errors.

30	Test exit routine	
27	Unused	
26	Unused	
25	Air mover and voltage regulator test	Cabinet Blower box fans H7213 regulator MDM module not in. No memory or load module in system.
24	Unused	
23	XON not received	Type Cntl Q to correct
22	Console SLU xmit ready bit not set	M8190.
21	Drive error	
20	Controller error	
17	Invalid device	
16	Invalid unit number	
15	Non-existent drive	
14	Non-existent controller	
13	No tape present	
12	No disc present	
11	Non-bootable media in drive	Try setting setup parameter M to a 1.
10	Drive not ready	
6	Console disabled	
5	Unused	
4	Dialog mode	
3	UBA rom boot in progress	
2	EEPROM boot in progress	
1	CPU rom boot in progress	
Blank	Control has passed to booted code or a secondary boot (i.e M9312)	

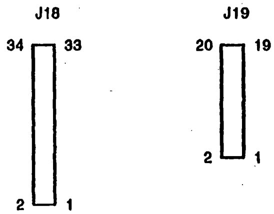
9.3.17 11/84 Unibus signal connectors

The CPU backplane on the 11/84 is totally inaccessible,this could cause problems if the need arose to scope the unibus,so there are two connectors J18 and J19 located behind a small plate in front of the cpu and memory modules.The small plate is held in place by one screw. All Unibus signals except init and the five grant lines are brought out on these connectors. Unfortunately these connectors are not as accessible as would be ideal but they suffice.

CONNECTOR PIN #	SIGNAL NAME
J18-34	DCLO
J18-33	ACLO
J18-32	BR7 L
J18-31	BR6 L
J18-30	BR5 L
J18-29	BR4 L
J18-28	PA L
J18-27	PB L
J18-26	MSYN L
J18-25	SSYN L
J18-24	C1 L
J18-23	C0 L
J18-22	A17 L
J18-21	A16 L
J18-20	A15 L
J18-19	A14 L
J18-18	A13 L
J18-17	A12 L
J18-16	A11 L
J18-15	A10 L
J18-14	A09 L
J18-13	A08 L
J18-12	A07 L
J18-11	A06 L
J18-10	A05 L
J18-09	A04 L
J18-08	A03 L
J18-07	A02 L
J18-06	A01 L
J18-05	A00 L
J18-04	BBSY L
J18-03	NPR L
J18-02	GND
J18-01	GND
J19-20	D15 L
J19-19	D14 L
J19-18	D13 L
J19-17	D12 L
J19-16	D11 L
J19-15	D10 L
J19-14	D09 L
J19-13	D08 L
J19-12	D07 L
J19-11	D06 L
J19-10	D05 L
J19-09	D04 L
J19-08	D03 L
J19-07	D02 L

CONNECTOR PIN #	SIGNAL NAME
J19-06	D01 L
J19-05	D00 L
J19-04	INTR L
J19-03	SACK L
J19-02	GND
J19-01	GND

Figure 9-5: Unibus Connector Layouts



9.4 Unibus Floating Addresses and Vectors

From an article written by Vic Taylor ...

Adding or removing a Unibus device is not straightforward because its address and vector fit in "floating address and vector space", and are subject to a "ranking" scheme. This means you also have to consider the addresses and vectors of **other devices** on the bus. These may have to be **changed** .

The 'how and why' of this is explained below and applies equally to PDPs and VAXes.

9.4.1 Floating Addresses and Vectors - your Questions Answered

Why do we need floating address and vector space?

- Because there is not enough i/o page space to enable every possible device to have a fixed address. And because the vector range would have to be huge.

Why do some devices have floating vectors but not floating addresses?

- Because there is more limitation on the vector range than the address range (i.e the address range is 4Kw but the vector range is only 1/4Kw).

Why are floating vectors contiguous but addresses not?

- An operating system identifies floating devices by seeing an address gap between different device types, so there is no need to have gaps in the vectors.

Why do you have to readdress and revector some existing devices when adding or removing a new device which has a floating address?

- Because floating addresses are assigned in a pre-defined ranked order so if you add or remove a device that has a higher rank than some existing devices then the addresses of the lower ranked devices have to shuffle up or down accordingly.

Is there an easy way to work out floating addresses and vectors?

- Yes, you can use VMS sysgen (for PDP11 and VAX configurations) as per Chapter 7, VMS, or if you do not have access to VMS sysgen then ring your local Support Group who will be very willing to supply the information.

What do you need to know to be able to use VMS sysgen to find addresses and vectors for devices?

- You need to know all of the devices you have on your particular Unibus.

Can you just add another of an existing device type without considering other devices on the same Unibus?

- No, whether the device type already exists or not it still impacts devices of lower rank.

What devices need to be considered as far as floating addresses and vectors are concerned?

- Though not all devices are in the floating range you should take all devices into account.

Is the floating address and vector allocation the same for all operating systems?

- Yes, all DEC operating systems conform to the same floating address and vector specification.

What are the effects of adding a new device in the floating range without taking into consideration existing devices?

- The typical symptom is many Unibus devices disappearing from the operating system, or the operating system getting the device types wrong.

Table 9-8: Floating Address Ranking

Ranking	Option	
1	DJ11	
2	DH11	
3	DQ11	
4	DU/DUV11	
5	DUP11	
6	LK11A	
7	DMC/DMR11	DMC before DMR
8	DZ/DZV11/DZ32	DZ11 before DZ32
9	KMC11	
10	LPP11	
11	VMV21	
12	VMV31	
13	DWR70	
14	RL/RLV11	1st RL11 is fixed
15	LPA11-K	
16	KW11-C	
17	RESERVED	
18	RX/RXV11/RXV21	1st RX11 is fixed, RX11 before RX211
19	DR11-W	
20	DR11-B	1st two DR11B's fixed
21	DMP11	
22	DPV11	
23	ISB11	
24	DMV11	
25	DEUNA	1st DEUNA fixed
26	UDA50/RQDX	1st UDA50 fixed
27	DMF32	
28	KMS11	
29	VS100	

Table 9–8 (Cont.): Floating Address Ranking

Ranking	Option	
30	TU81	1st TU81 fixed
31	KMV11	
32	DHU/DHV11	
33	DMZ32	

Table 9–9: Floating Vector Ranking

Ranking	Option	
1	DC11/TU58	
2	DL11A/B,DLV11/J	
3	DP11	
4	DM11A	
5	DN11	
6	DM11BB/BA	
7	DH11 MODEM CNTL	
8	DR11A/DRV11B	
9	DR11C/DRV11	
10	PA611	
11	LPD11	
12	DT07	
13	DX11	
14	DL11C/D/E,DLV11E	
15	DJ11	
16	DH11	
17	GT40/VSV11	
18	LPS11	
19	DQ11	
20	KW11W/KWV11	
21	DU11/DUV11	
22	DUP11	
23	DV11	
24	LK11A	
25	DWUN	
26	DMC/DMR11	DMC before DMR
27	DZ11/DZ32/DZV11	DZ11 before DZ32
28	KMC11	
29	LPP11	
30	VMV21	
31	VMV31	
32	VTV01	
33	DWR70	
34	RL/RLV11	1st RL11 fixed
35	TS11/TU80/TK25	1st fixed
36	LPA11K	
37	IP11/IP300	
38	KW11C	
39	RX/RX211,RXV11/21	1st RX fixed, RX11 before RX211
40	DR11W	
41	DR11B	1st DR11B fixed
42	DMP11	
43	DPV11	
44	ML11	

Table 9-9 (Cont.): Floating Vector Ranking

Ranking	Option	
45	ISB11	
46	DMV11	
47	DEUNA	1st DEUNA fixed
48	UDA50/KDA50	1st UDA50 fixed
49	DMF32	
50	KMS11	
51	PCL11	
52	VS100	
53	RESERVED	
54	KMV11	
55	RESERVED	
56	RESERVED	
57	DHU11/DHV11	
58	DMZ32	

Central
Region

F A C T F L A S H

Options Affected: 11/84
Submitted By: Brian Hailstone
Date: 10-APR-1990
Filing Instructions: File at end of chapter 9, PDP11

11/84 LTC failure

PROBLEM: THE LTC SIGNAL FROM THE H7200-00 REGULATOR FAILS AFTER 10 - 40 HOURS

Most of the PDP 11/84-A, 11X84-A and 11/84-D systems with an H7200-00 regulator at Part Revision E01 are experiencing the loss of the LTC signal after 10 - 40 hours of operation. This problem is caused by a component on the regulator that was part of a bad batch of components from a vendor. H7200-00s at Part Rev E01 are the only revisions that are experiencing this problem.

*The Part rev is stamped on a white label located in the middle of the H7200-00 regulator.

WORKAROUND: CHANGE THE 1184 SETUP FEATURES TO ENABLE THE CRYSTAL ON THE CPU BOARD TO BE USED AS THE SOURCE FOR THE LTC SIGNAL

PDP 11/84 systems that exhibit this problem should have the 11/84 console Setup features changed to enable the crystal on the CPU board to be used as the source for the LTC signal and not the power supply. This is done from the 1184 console terminal while in Console Dialog Mode as indicated below:

1. Type "S" <RET> - selects Setup Mode.
2. Type "2" <RET> - list/change parameters.
3. Type "H" at the first parameter question. This brings you to the question dealing with the clock source.
4. Type either "1" (50hz), "2" (60hz) or "3" (800hz) <RET> depending on the line frequency where the 1184 is installed.
5. Type "ctrl z". This brings you back to the Setup menu.
6. Type "9" <RET> - save Setup table.
7. Type "1" <RET> - writes Setup table.
8. Type "1" <RET> - puts you back in Dialog mode.

EXCEPTIONS TO THE WORKAROUND: CERTAIN APPLICATIONS AND 1184s RUNNING RSTS V9.0 TO V9.5 REQUIRE A HARDWARE FIX

Using the crystal on the CPU board as the source for the LTC pulse is the preferred solution to this problem, however, the following are exceptions to this workaround:

o Some applications require multiple 1184s to be synchronized by the LTC clock and the only acceptable method of achieving this is to use the power supply LTC source.

o Systems running RSTS versions 9.0 to 9.5 will hang during the boot sequence if the Power Supply is not generating an LTC pulse. The hang will occur after the initial line feed is output to the console terminal and before any other message is printed. This is caused because the RSTS/E initialization code disables the EEPROM set-up on the CPU and always uses the power supply as the source of the LTC signal during the boot. RSTS waits in a two instruction loop for the LTC clock to tick. In the case of a malfunctioning LTC circuit, RSTS will hang on those two instructions.

To verify this type of hang, use the following procedure:

1. Halt the system using the break key on the console or the front panel switch. The @ will be displayed.
2. Examine General purpose register 1 using the command: R1/
3. The console ODT will display the contents of R1. If the contents of R1 is the clock CSR address of 177546, then the missing LTC signal is the most likely problem.

*RSTS V9.6 AND ABOVE DOES NOT CHECK THE LTC CLOCK WHILE BOOTING IF THE CRYSTAL ON THE CPU BOARD IS SELECTED AS THE SOURCE FOR THE LTC CLOCK, THEREFORE THE WORKAROUND OF USING THE CRYSTAL AS THE LTC SOURCE IS ACCEPTABLE FOR THOSE VERSIONS.

SOLUTION FOR THE EXCEPTIONS: REPLACE THE REV E01 H7200-00 WITH A REV F01 H7200-00.

All rev E01 H7200-00 regulators have been removed from SR17 and reworked to Part Rev F01. Rev F01 power supplies do not have this problem.

Central Region

FACT FLASH

Options Affected: 1193 1194
Submitted By: Jim Egginton
Date: 10-SEP-1990
Filing Instructions: At end of chapter 9 PDPs

New processor 1193/4 KDJ11-E

The 1193 and the 1194 are now available, and the manuals for these are in the respective technical libraries.

They should not be any different to service from the 1183 or 1184, with the following exceptions. No extra training should be required.

1. The KDJ11-EA is a M8981-AA and has 2 Mbytes on board
2. The KDJ11-EB is a M8981-BA and has 4 Mbytes on board
3. They do not support any PMI memory modules.
4. It has a KDJ11 (DCJ11) chip running at 18 Mhz the same as the 1183/4. so presumably the extra 40% performance comes from the on board memory speed.
5. All the usual on board features are there i.e EIS, FP, boot, toy clock, console F/W with PUST, but no ethernet or disk ports.
6. There is a console port and **7 SERIAL LINES ON BOARD**
7. The console firmware looks the same, except the SET and SHOW commands include support for the on board SLUs.
8. Only the usual PDP disk support is included i.e. RQDX3 and KDA/UDA50.
9. The cabs used are the 1184 cab for the 1194 and the BA23 for the 1193. (can be pedestal or rack mount i.e. H96xx cab)

Upgrading to a 1193 is no problem, just swap the CPU and distribution panel inserts with their cables, I have no information on upgrading an 1184 to an 1194, but it looks straightforward. Upgrade kits are available and necessary.

Power Supply requirements are +5v 4.5A, and +12v 0.6A, I have updated the latest QBus lists with these.

Central
Region

F A C T F L A S H

Options Affected: PDP 11/84E
Submitted By: Richard Penn
Date: 27-NOV-1990
Filing Instructions: File at the end of Chapter 9.

Part No's for the 11/84E power supply.

The PDP 11/84E is housed in a 10.5 in BA-11A style system box, which has for a power supply an H7204-CB (240v version).

There are three regulator cards that make up the main FRU's in the H7204-CB.

- H7203-A...........CH 1 voltage regulator module (not an FRU).
- H7213...............CH 2 voltage regulator module.
- H7217...............CH 3 voltage regulator module.

Like with previous 11/84's there are minimum load modules.

- M7556...............**Used to load 5.1 VBB to 2amps if necessary. Memory slot.**
- M9049...............**Used to load -15v to 700mA if necessary. Slot 9 row F.**

Other numbers that may be of use.

- 70-24526-02......System box.
- 54-17228-01......Backplane.
- 17-01708-01......40 conductor cable PSU top Backplane.
- 70-22115-01......Fan assembly.
- 12-22271-03......12v Fan.