Chapter 28
Alpha

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Revision: Updated September 1993 to include reference to 7xx0 chapter, and minor corrections.

28.1 Introduction

The aim of this chapter is to provide a basic awareness of Alpha. At present it contains brief descriptions of the architecture, the chip and the first systems. It will be added to as more information becomes available.

Be aware that the information contained here is new and is, therefore, subject to change. Therefore it should be treated strictly as **internal use only** .

The LASER systems are described in detail in the new Chapter 6, DEC/VAX 7xx0/10xx0.

28.2 Alpha Architecture

The Alpha architecture is a 64 bit RISC architecture designed with emphasis on speed, multiple instruction issue, and multiple processors.

Alpha is open. The architecture is not designed for a particular Operating System. It is designed to last well into the next century and will be licensed so that other manufacturers can use it.

Alpha architecture summary:

- 64 bit virtual address space.
- 64 bits wide data paths (minimum).
- 32 64-bit integer registers.
- 32 64-bit floating point registers.
- 32 bit (longword) and 64-bit (quadword) integers.
- 32-bit and 64-bit IEEE and VAX floating point data types.
- RISC instruction set (approx 150 instructions).
- Fixed 32 bit instruction length.
- Variable page size (8K, 16K, 32K or 64K bytes).
- Privileged Architecture Library Code (PALcode).

Alpha does not have microcode. The PALcode, which runs in memory, is used instead, to perform such functions as servicing of interrupts, exceptions and TB misses etc. PALcode knows the hardware and the Operating System and provides an interface between them.

28.3 Alpha Chip

The first implementation of the Alpha architecture is the EV4 chip (DIGITAL 21064-AA). It is a 150 - 200 MHz, 64 bit, CMOS-4 based microprocessor. The microprocessor is super-scalar and super-pipelined (this means up to two instructions can be issued every clock tick). The chips are being manufactured at plants in Hudson, Ma. and South Queensferry, Scotland, and anyone can buy one.

Alpha chip features:

- Implements advanced Alpha RISC Architecture. Optimized multiprocessor support. IEEE single and double precision, VAX F_floating and G_floating, longword, and quadword data types. Cycle counter for code optimization.
- Single chip implementation. On-chip write buffer with four 32 byte entries. On-chip pipelined floating point unit. On-chip 8KB data cache. On-chip 8KB instruction cache. On- chip demand paged MMU (12 entry I-stream pages, 32 entry D- stream pages). On-chip parity and ECC generators and checkers. On-chip internal clock. Programmable on-chip performance counters.
- Dual-pipelined architecture. 200MHz cycle time, 400 mips peak instruction execution.
- Privileged Architecture Library Code (PALcode). Optimization for multiple OS. Flexible MMU. Multi-instruction atomic sequences.
- External cache. On-chip external secondary cache control. Programmable cache size and speed.
- Selectable data bus width/speed, 64 or 128 bits, 75 MHz to 18.75 MHz.
- 3.3 volt supply voltage. Power dissipation is 30 watts for 200MHz. 1.68 million transistors. 431 pin PGA package, 140 pins dedicated to VDD/VSS.

28.4 First Alpha Systems

The first DEC systems utilising the Alpha chip are shipping to customers now. Six different types have been announced so far, ranging "from Desktop to Datacentre". A description of each follows.

28.4.1 Jensen - DEC 2000 Model 300 (now DECPC AXP150)

Jensen is a high performance Alpha PC. It is designed for both client and server applications and will be a combination of a high performance Alpha cpu and high volume, low cost, commodity PC components. This product has appeared very recently, so the following information is only provisional.

Main features:

- CPU based on EV4 chip, rated at 75-100 MIPs
- 1MB cache and 16 to 256 MB main memory
- EISA controller with support for 6 option cards
- 16450 compatible serial ports, 8742 compatible keyboard controller and centronics compatible printer port
- SCSI support and 3.5" or 2.5" disks internal to enclosure
- PC Mini-Tower enclosure
- Software: Windows-NT, Alpha VMS and OSF/1

28.4.2 Sandpiper - DEC 3000 Model 400

Sandpiper is a desktop workstation. Its graphics are fully compatible with current (MIPS-based) workstations. It uses TURBOchannel, which is becoming an industry standard, as its main bus. A server version will be available called DEC 3000 Model 400S.

Main features:

- Single board, non-expandable.
- CPU based on 7.5nS EV4 chip, rated at 100-120 SPECmarks [1], 20-30 MFlops
- 512KB cache and 8 to 512 MB main memory
- Turbochannel (3 slots)
- Integral accelerator colour graphics, 1280x1024, 8/8 planes, 72MHz.
- Choice of 17", 19" and 21/22" monitors.
- Dual SCSI-II.
- Disks: 2 x 3.5" and 1 x 5.25" internal to enclosure
- Ethernet
- 2 asynchronous lines - one full modem control.
- Keyboard, mouse and 2 serial lines.
- Software: OSF/1, Alpha VMS.

[1] 1 SPECmark is approximately 1 VUP, or 1 VAX 11/780s worth of performance

28.4.3 Flamingo - DEC 3000 Model 500

Flamingo is a deskside or rackmount workstation. It is basically the same as the Sandpiper but can have more memory and I/O.

Main features:

- CPU based on EV4 chip, rated at 125 SPECmarks
- 1 MB cache and 32 to 256GB main memory (1GB later)
- 8-plane colour or greyscale base video
- 16" and 19" monitors with 66Hz/72Hz refresh
- 6 Turbochannel slots
- Dual SCSI-II
- Disks: 4 x 3.5" or 2 x 5.25" internal to enclosure
- Ethernet (+ FDDI Turbo option)
- 2 Asynchronous lines - 1 full modem control
- Keyboard, mouse, 2 serial lines, ISDN and Audio port
- Software: Alpha VMS and OSF/1

28.4.4 Cobra - DEC 4000 Model xxx

Cobra is an open office system designed to house as much SCSI based storage as can be powered from a normal mains socket. Comes in two flavours: One for the technical market where CPU performance and I/O bandwidth are most important. One for the commercial market where availability is most important. Storage configuration is flexible so customer can optimise for bulk capacity ($/MB) or performance (QIOs/sec). Cobra is intended to provide an upgrade path for VAX 4000 users, and is thus termed "VAX 4000 style".

Main features:

- 1 or 2 CPUs based on EV4 chip, rated at 135-270 SPECmarks
- 2MB Cache (per CPU) and 32 to 512MB main memory (1GB later)
- 5 x SCSI or DSSI
- 16 x 3.5" or 4 x 5.25" drives internal to enclosure
- 2 x 1/2 height or 1 full height tape and CDROM in enclosure
- 2 x Ethernet
- Futurebus+ (6 slots)
- Software: Alpha VMS and OSF/1

28.4.5 Laser - DEC7000 Model xxx or VAX 7000 Model xxx

See Chapter 6, DEC/VAX 7xx0/10xx0.

28.4.6 Blaser - DEC 10000 Model xxx or VAX 10000 Model xxx

See Chapter 6, DEC/VAX 7xx0/10xx0.