



M8108

System Status Registers, KT11-C

PROCESSOR TYPE PDP-11/45, PDP-11/50

CODE: D CS: A M8108-00001

APR-72 - PROBLEM: 1: Wrong termination.

CORRECTION 1: Eliminate resistor R2; change R1 to 150 ohms.

PROBLEM 2: Race condition at 1.2 usec ROM cycle.

CORRECTION 2: Synchronize INHIBIT signal with flip-flop on SSRK .

PROBLEM 3: NO ERROR flip-flop not setting. CORRECTION 3: Clock register SRO earlier.

CORRECTION 4: Drawings changed to correct print errors.

PROBLEM 5: TIG changes.

CORRECTION 5: Change prints.
PROBLEM 6: Hole in EXECUTE ONLY space.

CORRECTION 6: Change I SPACE logic -SSRB .

In-plant effectivity -03 rework immediately

M8108-00002 CODE: D CS: B

APR-72 - PROBLEM: An MTPI instruction, when "D" space is enabled and current and previous modes are both USER, will now write into the "D" space if "D" space is write-enabled.

CORRECTION: Under the above circumstances, allow MTPI to try to write in "I" space. This is OK since "I" space will normally be "read when set up as an EXECUTE ONLY situation hence, the MTPI will be aborted. Signal SSRJ C1 B L determines whether it is MTPI or MFPI.

NOTE: See correction supplement ECO M8108-00003 In-plant effectivity -Rework immediately

M8108-00003 CODE: D CS: C

APR-72 - CORRECTION 1: Corrects note on ECO M8108-00002.

PROBLEM 2: On a KT11-C abort, using CONSOLE PHYSICAL for an examine, sometimes gave an address error on trying to examine KT11-C

CORRECTION 2: Clear INHIBIT signal with the fact that the access is a CONSOLE PHYSICAL operation.

In-plant effectivity -03 rework immediately

M8108-B0004 CODE: DF CS: D ETCH: B

APR-72 - PROBLEM: Etched board has etch cuts and jumpers from ECO's M8108-00001 through M8108-00003.

CORRECTION: Correct etched board to reflect revision level "C" Circuit Schematic.

NOTE: See correction supplement FCO M8108-A004A.

In-plant effectivity -02 -Phase-in

Field effectivity -Rework all etch revision "A" M8108's

(Time To Install And Test 1.0 Hour) (Kit Contents -FCO/Prints)

M8108-B004A CODE: DF

JUN-72 - PROBLEM: FCO M8108-B0004 incorrect. Must also retrofit etch revision "A" boards to make actual circuit identical to schematic. CORRECTION: To "A" etch revision boards only, add jumper from E85

pin 4 to PTH below pin 1 on E107, connects signal SSRL INT CLRA L to E85 pin 4, also update CS revision "D".

NOTE: Attempt to access any SUPERVISOR PAGE ADDRESS REGIS-TER with the KT11-C enabled may cause the processor to hang. In-plant effectivity -03 -Rework all etch revision "A" M8108's Field effectivity -Initiated

M8108-00005 CODE: P CS: E

MAR-73 - ECO M8108-00005 was cancelled by supplement ECO M8108-0005A. FCO M8108-00006

PROBLEM: Circuit Schematic drawing showing etch revision "B" still says "Etch revision A".

CORRECTION: Change etch letter on Circuit Schematic drawing to "B" ; update Module History and Assembly Hole drawing.

In-plant effectivity -06 documentation change only

M8108-B0007 CODE: F CS: F

MAY-73 - PROBLEM: Fails to abort when illegal address is internal register; SSRK INHIBIT 1 L fails to block TIGD T5BH on SSRL D-S. CORRECTION: On SSRK , replace signal SSRK TS4 H with TIGC T4BH at E79 pin 13.

NOTE: The KB11-A must be at WL revision "N" or later; reference FCO KB11A-B0017.

In-plant effectivity -03 * -All etch revision "A" and etch revision "B" M8108's must be reworked. KB11-A must also be reworked.

Field effectivity -Rework all etch revision "A" and "B" M8108's (Time To Install And Test .5 Hour.) (Kit Contents -F951 -FCO/Prints)