Digital Equipment Corporation Maynard, Massachusetts

VR14
CRT display
user's manual
 J

# VR14 <br> CRT display <br> user's manual 

1st Edition, April 1971
2nd Printing (Rev) June 1971
3rd Printing (Rev) June 1972
4th Printing (Rev) January 1973
5th Printing, July 1973

Copyright © 1971, 1972, 1973 by Digital Equipment Corporation

The material in this manual is for reference only. Operating characteristics and functional descriptions are provided solely as reference information and are subject to change at any time without prior notice. The drawings, specifications, and descriptions herein are the property of Digital Equipment Corporation and shall not be reproduced or copied in whole or in part as the basis for the manufacture or sale of items without written permission.
This manual was written by the PDP-12 Engineering Department with assistance from individuals in other product groups at DEC.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC
FOCAL12

PDP
FLIP CHIP

## CONTENTS

Page
CHAPTER 1 GENERAL INFORMATION
1.1 General Description ..... 1-1
1.2 Specifications ..... 1-1
1.3 Block Diagram Description ..... 1-3
CHAPTER 2 OPERATION
2.1 Installation ..... 2-1
2.2 Front Panel Controls ..... 2-3
2.3 Rear Panel Controls and Connectors ..... 2-3
2.4 Internal Controls ..... 2-5
2.5 Input Signal Requirements ..... 2-7
CHAPTER 3 THEORY OF OPERATION
3.1 $X$ - and $Y$-Deflection Circuits ..... 3-1
3.2 Plus and Minus Low Voltage Regulated Supply ..... 3-7
3.3 CRT Electrode Voltages ..... 3-12
3.4 High Voltage Power Supply ..... 3-12
3.5 Intensity Circuit ..... 3-14
CHAPTER 4 MAINTENANCE
4.1 Preventive Maintenance ..... 4-1
4.2 Troubleshooting ..... 4-1
4.2.1 No Picture ..... 4-3
4.2.2 Faulty Picture ..... 4-5
4.3 Assembly Replacement Instructions ..... 4-6
4.3.1 Deflection Heat Sink Removal ..... 4-6
4.3.2 7007165 Power Regulator Assembly Removal ..... 4-8
4.3.3 Regulator Heat Sink Removal ..... 4-8
4.3.4 Yoke and CRT Removal ..... 4-9
4.3.5 High Voltage Supply Removal ..... 4-13

## CONTENTS (Cont)

Page

## APPENDIX A POWER SUPPLY TROUBLESHOOTING

## APPENDIX B DEFLECTION AMPLIFIER TROUBLESHOOTING

## APPENDIX C A225 REPAIR

## CHAPTER 5 ENGINEERING DRAWINGS

## ILLUSTRATIONS

| Figure No. | Title | Art No. | Page |
| :--- | :--- | :--- | :--- |
| 1-1 | VR14 Block Diagram |  | $1-4$ |
| $2-1$ | Input Power Jumper |  | $2-2$ |
| $2-2$ | VR14 Rear View | $5481-24$ | $2-4$ |
| $2-3$ | VR14 Top View | $5481-1$ | $2-6$ |
| $3-1$ | X- and Y-Deflection Circuit |  | $3-3$ |
| $3-2$ | G836 Circuit Board, Part of The | $3-9$ |  |
|  | 7007165 Power Regulator Assembly |  |  |
| $3-3$ | Intensity Amplifier W682, Circuit Schematic | $3-13$ |  |
| $3-4$ | Circuit Diagram, G838 |  | $3-16$ |
| $4-1$ | Voltage Chart |  | $4-2$ |
| $4-2$ | Deflection Heat Sink Removal | $5481-15,5481-20$ | $4-7$ |
| $4-3$ | 7007165 Power Regulator Assembly |  | $4-9$ |
| $4-4$ | 7007165 Removal | $5481-3,5481-8$ | $4-10$ |
| $4-5$ | Regulator Heat Sink Removal | $5481-13,5481-18$ | $4-11$ |

TABLES
Table No. Title Page
2-1 Rear Connector Pin Assignments 2-4
2-2 Control Settings 2-9
5-1 Engineering Drawings 5-1

## WARNING

Maintenance procedures should be performed by qualified service personnel only.

High voltages are present within the unit and, under certain conditions, are potentially dangerous. All electrical safety precautions must be observed.

Inherent implosion protection is employed in the CRT design; however, the tube may be damaged if it is subjected to rough treatment or dropped while being removed from or installed in the display. Exercise caution during these operations.


## CHAPTER 1 <br> GENERAL INFORMATION

### 1.1 GENERAL DESCRIPTION

The VR14 is a completely self-contained CRT display that provides a 6.75-in. x 9-in. viewing area in a compact 19-in. package. The VR14 requires only analog $X$ - and Y -position information and an intensity pulse to generate sharp, bright point-plot displays. Except for the CRT itself, the unit is composed of all solid-state circuits, utilizing high-speed magnetic deflection to enhance brightness and resolution. The inputs for the $X$ - and $Y$-deflection may be balanced or single ended, bipolar or offset, and positive- or negative-going without any modification to the VR14. The intensity pulse may be time multiplexed or gated by a separate input to allow the screen to be timeshared between two inputs.

VR14 construction is modular for easy maintenance. Any subassembly or major component can be replaced in minutes using only a screwdriver. The VR14 is available in a standard 19-in. rack-mounted unit or in a free standing table-top version.

### 1.2 SPECIFICATIONS

VR14 Specifications are as follows:

| Physical: | Height <br> Width <br> Depth <br> Weight <br> Viewable <br> Area | $\begin{aligned} & 10-1 / 2 \\ & 19 \mathrm{in} . \\ & 17 \mathrm{in} . \\ & 75 \mathrm{lb} \\ & 6-3 / 4 \mathrm{ir} \end{aligned}$ |
| :---: | :---: | :---: |
| Spot Size: | $\begin{aligned} & \leqslant 20 \mathrm{mils} \\ & \text { of } 30 \mathrm{fL} \end{aligned}$ | de the us |
| Jitter: | $\leqslant \pm 1 / 2 \mathrm{sp}$ | diameter |
| Repeatability: | $\leqslant \pm 1$ spot (Repeatab of any giv | ameter y is the spot) |


| Gain Change: | From a fixed point on the screen, less than $\pm 0.3 \%$ <br> gain change for each $\pm 1 \%$ line voltage variation |
| :--- | :--- |
| Temperature Range: | $0^{\circ} \mathrm{C}$ to $50^{\circ} \mathrm{C}$ (operating) |
| Relative Humidity: | $10 \%$ to $90 \%$ (noncondensing) |
| Brightness: | $\geqslant 30 \mathrm{fL}$; measured using a shrinking raster technique |
| Linearity: | Maximum deviation of any straight line will be $\leqslant 1 \%$ <br> of the line length measured perpendicular to a best-fit <br> straight line |
| Deflection Method: | Magnetic ( $70^{\circ}$ diagonal deflection angle) |
| Focus Method: | Electrostatic |
| High Voltage: | 10.5 kV de nominal (voltage proportional to input line <br> voltage). Supply is self-contained and equipped with |
| Shielding: | a bleeder resistor |
| Overlaod Protection: | CRT is fully enclosed in a magnetic shield |

Deflection Amplifier
a. Deflection Amplifiers are dc coupled and are capable of sustaining a full screen ac or dc deflection at environmental extremes.
b. Input Specifications

1. Inputs are differential
2. Differential input impedance, $5 \mathrm{k} \Omega$ minimum
3. Input sensitivity, $500 \mathrm{mV} / \mathrm{in}$. maximum ( $200 \mathrm{mV} / \mathrm{in}$. with resistor change)
4. Common Mode Rejection Ratio, 40 dB
5. Maximum operating input, $\pm 6 \mathrm{~V}$. (Maximum operating input is the sum of the common mode input and the differential input)
6. Input offset not to exceed $\pm 1 / 2$ peak-to-peak input signal
7. Maximum nonoperating input, $\pm 50 \mathrm{~V}$
c. Full screen deflection and settling time to within $\pm 1$ spot diameter, $\leqslant 18 \mu \mathrm{~s}$.
d. Small signal settling time to within $1 / 2$ spot diameter, $\leqslant 1 \mu$ for a 0.1 -in. deflection
e. Small signal linear slew rate, $\geqslant 0.4 \mathrm{in} . / 1 \mu \mathrm{~s}$
f. Velocity error coefficient, 500 ns maximum. (Average ramp delay between input and output)

## Z-Axis

a. Z-Input

A negative transition from $\geqslant+2.4 \mathrm{~V}$, but not exceeding +8 V , to $\leqslant+0.8 \mathrm{~V}$, but not more negative than -4 V , in $\geqslant 20$ ns will cause an unblanking pulse at the CRT cathode from approximately +60 V to ground with a duration of $\geqslant 200 \mathrm{~ns}$ at the 50 percent points. Delay between the 50 percent point of the negative input transition to the 50 percent point of the output pulse is less than 100 ns . Driver must sink 4 mA .
b. Z-Direct

A positive-going pulse not exceeding 65 V , but at least 45 V in height and not exceeding $10 \mu \mathrm{~s}$, but at least $1 \mu \mathrm{~s}$ in duration, will unblank the CRT to a viewable intensity. This signal is ac coupled to the CRT grid.
c. Shannel Select

With the Channel Select Switch in the Channel 1 position, a positive level of greater than +2.4 V , but not exceeding +8 V will enable the Z -input circuit. A level of less than +0.8 V , but not more negative than -4 V , will disable the circuit. With the switch in the channel 2 position, a positive level will disable the Z-circuits; a negative level will enable it. Placing the switch in the channel 1 and 2 position disables this input.

## Power

a. All power supplies necessary for operation of the unit are self-contained.
b. Input Requirements

Voltage: $\quad 100 \mathrm{~V} \pm 10 \%$
$115 \mathrm{~V} \pm 10 \%$
$230 \mathrm{~V} \pm 10 \%$
Selectable by tap changes.

| Frequency: | $50-60 \mathrm{~Hz}$ |
| :--- | :--- |
| Power: | $\leqslant 500 \mathrm{~W}$ |
| Current: | $\leqslant 5 \mathrm{~A}$ |
| Type: | Single Phase |

### 1.3 BLOCK DIAGRAM DESCRIPTION

Figure $1-1$ is the functional block diagram of the VR14. The $X$ - and $Y$-position signals are connected to their respective A225 deflection amplifier circuit boards through polarity reversal switches. The A225s boost the input signal to a level sufficient to drive the power transistors, while also providing gain and position controls. In furn, the power transistors drive the deflection yoke that positions the electron beam on the screen. The yoke currents are then passed through a 0.5 -ohm resistor that converts the yoke currents back into voltages that are used as feedback for each A225 deflection amplifier.


Figure 1-1 VR14 Block Diagram

This feedback allows the A225 to produce an exact current replica in the yoke of the input signals. The intensity input is applied to the W682 circuit board that converts this input to a 60 V pulse which drives the cathode. The cathode pulse is negative going; this pulse turns on the electron beam, creating a spot on the screen. The W682 accepts a gating input that allows the intensity pulse to be timemultiplexed between two input sources. The G838 fault protection board disables the intensity circuit in the event of $a \pm 20 \mathrm{~V}$ failure. This prevents the phosphor screen from burning, as there would be no deflection under these conditions.

Line power is passed through a fuse, an on-off switch, and then through two normally closed thermal cutout switches. The switches are located on the +20 V regulator heat sink and the X -deflection heat sink and, in the event of a fan failure or excessive temperature on either heat sink, VR14 input power will be shut off until they cool down. The line power is then connected to the power transformer, the high voltage power supply, and the fans. The high voltage supply converts the input line voltage to 11.5 kV that is connected to the CRT anode. The power transformer has three basic secondaries, a 6.3V for filament, a $35 / 130$ for CRT electrodes, and a 58 V center tapped for deflection. The 58 Vac is rectified and filtered to provide $\pm 35 \mathrm{Vdc}$ unregulated. This $\pm 35 \mathrm{Vdc}$ is regulated with circuits on the G836 board, along with four power transistors on the regulator heat sink assembly. The regulated output is $\pm 20 \mathrm{Vdc}$ and is distributed to the deflection amplifiers. The $35 / 130$ ac is rectified and filtered on the $\mathbf{G} 836$ to generate $\pm 80 \mathrm{Vdc}$ and +400 Vdc . The -80 Vdc is used for the brightness potentiometer which is tied to the grid. One side of the brightness control is connected to another potentiometer on the $G 836$ which can adjust the maximum brightness range of the brightness potentiometer. The +400 Vdc is supplied directly to $\mathrm{G}_{2}$ and also to one side of the focus potentiometer on the G836 board. The wiper of the focus potentiometer goes directly to the focus electrode on the CRT.

## CHAPTER 2

## OPERATION

### 2.1 INSTALLATION

The VR14 is shipped either as a standard RETMA 19-in. by $10-1 / 2 \mathrm{in}$. (10-7/16 in.) rack-mounted unit or as a table-top model (without chassis slides) with its own decorator cover. The VR14 can operate from a power line frequency between 47 and 63 Hz . The input line voltage, however, is specified by the letter designation after the VR14 (O,C is $115 \mathrm{~V} ; \mathrm{A}, \mathrm{D}$ is 230 V ; and $\mathrm{B}, \mathrm{E}$ is 100 V .) The VR14 can operate with any of the three input line voltages simply by changing the jumpers and interconnects on TB1 and TB2 (see Figure 2-1).

Equipment cooling is the most important VRT4 installation requirement. Fans draw air from the bottom of the unit; therefore, at least 1 in . of free air space must be provided below the bottom chassis. The table-top model keeps the bottom 1 in . above the table surface with four adjustable feet. In the rackmounted unit, if equipment is mounted immediately below the VR14, as long as there is open area under the VR14 fans (a screen is acceptable; a solid plate closer than 1 in . is not), proper cooling can occur. The same requirements apply, on the rack-mounted unit, to the area immediately above the unit. The table-top model has a solid top cover. The cooling air exits from the rear of the unit. Therefore, at least 2 in . of free space must be provided immediately behind the unit. (Do not push the VR 14 flush against a wall or solid vertical surface that would cut off air circulation.)

## NOTE

Before applying power to the VR14, ensure that the polarity switches on the rear panel and the position potentiometers are set for the particular input signals being used. Because of the universal nature of allowable input signals, the deflection amplifiers may be driven into saturation far off screen by a wrong combination of polarity and position settings. Leaving the deflection amplifiers saturated way off screen continuously may cause damage. See Paragraph 2.5 and Table 2-2 for proper settings.

115 Vac

TB1


230 Vac


100 Vac


Figure 2-1 Input Power Jumper

### 2.2 FRONT PANEL CONTROLS

The on/off, brightness control, and the channel select control switches are located on the front panel. The on/off switch turns on input power to the VR14 when the knob is rotated clockwise from the maximum counter-clockwise off position. Turning the knob clockwise also increases the brightness of the displayed information. A delay of about 30 s occurs before information appears on the screen while the CRT filament warms up. In an operating system, it is recommended that power be left on the display even when it is not in continuous use so that the filament warmup delays do not occur.

The channel select switch works in conjunction with the channel select signal applied at the rear connector. When not using the dual-channel feature, the select switch should be in the 1 and 2 position. When using the dual-channel system, points on the screen will be intensified from Z-intensity inputs only when the channel select signal at the rear connector is high and the channel select switch is in the channel 1 position. If the channel select input signal goes low while the select switch is at 1 , intensification ceases. On the other hand, the channel 2 position works in the opposite manner. If the channel select input signal is low and the select switch is at 2, Z-intensification signals will intensify on the screen. Thus, if a group of information points is to be separated from another group, separation can be achieved by having group 1 intensification pulses occur only when $Z$-select line is high, and group 2 intensification pulses occur only when the $Z$-select line is low. Channel select position $1 \& 2$ overrides the select input signal and displays every intensification pulse of both channels at once. To observe only channel 1 information, select channel 1 and all channel 2 points are locked out. By selecting channel 2, only channel 2 points are displayed.

### 2.3 REAR PANEL CONTROLS AND CONNECTORS

The rear panel (see Figure 2-2) has two slide switches, seven BNC connectors, and an Amphenol 24 contact Blue Ribbon (DEC type) connector. (The mate is DEC No. 12-03466, Amphenol No. 57-30240). Table 2-1 lists rear connector pin assignments.

The two slide switches allow the polarity of the X - and Y -input signals to be selected as to their response on the CRT screen. Physically all the switches do is interchange the $+X$ with the $-X B N C$ connections and the $+Y$ with the $-Y$ BNC connections. With the polarity switches in the - position, the CRT beam, when viewed from the front, will go up and to the right if the $Y$ - and $X$-input signal voltage becomes more positive; with the polarity switches in the + position, the beam goes up and to the right when the input signals become negative. The input reference is always the +BNC referred to the -BNC (pin 7 with respect to pin 8 for X , pin 10 with respect to pin 11 for Y ).

## NOTE

When unipolar inputs are used (such as OV to +2 V or OV to -6 V representing the full screen) the polarity switches must not be reversed from their originally setup position. If the input is $0 V$ to +2 V and the switches are in the position, switching to the + position will drive the deflection amplifiers into current limit because, instead of offsetting the unipolar input signal, the offset and input will aid driving the deflection into current limit off screen.


Figure 2-2 VR14 Rear View

Table 2-1
Rear Connector Pin Assignments

| 24 Pin | BNC | Function |
| :---: | :---: | :---: |
| Pin No. 1 | Z-Select | High input enables Z-intensify to occur <br> if channel select switch on 1. A low <br> input enables Z-intensify to occur if <br> channel select switch on 2. <br> Chassis ground |
| Pin No.2 No.3 | Chassis ground |  |
| Pin No.4 When this input goes from high to low, |  |  |
| an intensity pulse is generated |  |  |

Table 2-1 (Cont)
Rear Connector Pin Assignments

| 24 Pin | BNC | Function |
| :---: | :---: | :---: |
| Pin No. 5 |  | Chassis ground |
| Pin No. 6 |  | Chassis ground |
| Pin No. 7 | +X Input | One side of the X -input signal line |
| Pin No. 8 | -X Input | Other side of the X -input signal line (or ground for single ended inputs) |
| Pin No. 9 | $\pm \mathrm{X}$ input Shell | Shield or signal reference ground for X-input |
| Pin No. 10 | +Y Input | One side of the Y -input signal line |
| Pin No. 11 | -Y Input | Other side of the Y -input signal line (ground for single ended input) |
| Pin No. 12 | $\pm$ Y Input Shell | Shield or signal reference ground for Y-input |
| Pin No. 13 | Z-Direct | Input signal that directly modulates CRT grid (ac coupled) |
| Pin No. 14 |  | Chassis ground |
| Pin No. 15 |  | Chassis ground |
| Pin No. 16 |  | Not used, assigned for VR14 options |
| Pin No. 17 |  | Not used, assigned for VR 14 options |
| Pin No. 18 |  | Not used, assigned for VR14 options |
| Pin No. 19 |  | Light Pen output (only on VR14L) |
| Pin No. 20 |  | Light Pen output (only on VR14L) |
| Pin No. 21 |  | Chassis ground (only on VR14L) |
| Pin No. 22 |  | Not used |
| Pin No. 23 |  | Not used |
| Pin No. 24 |  | Not used |

### 2.4 INTERNAL CONTROLS

The VR14 internal adjustments include six potentiometers, X -position, X -gain, Y -position, Y -gain, focus, and brightness preset. All adjustments are accessible through the top of the VR14 (see Figure $2-3$ ). On the rack-mounted model, the unit is moved forward on the chassis slides until the adjustments can be reached. The table-top model has access holes though the top of the case only for position and gain. Access for focus and brightness preset is gained by removing the case cover.


Figure 2-3 VR14 Top View

The gain and position adjustments are located on the top, left central portion of the VR14 (as viewed from the front). The two forward potentiometers on the deflection circuits are the horizontal gain on the left, the vertical gain on the right. The two rear potentiometers are the horizontal position on the left, the vertical position on the right. The gain adjustments allow the VR14 to accommodate a range of input signal amplitudes and expand or contract the horizontal and vertical deflection to suit fullscreen requirements. The position controls accommodate a variety of input signals and allow offset inputs to be centered on the CRT screen. Once initially adjusted for the particular input signals used, the gain and position controls will rarely have to be adjusted. Gross positioning off screen or excessive gain deflecting off the extremities of the screen should be avoided, since the deflection amplifiers will go into current limiting and may overheat if allowed to stay in this condition any length of time. Turning the X - and Y -gain controls clockwise increases the gain or displayed image size. Turning the X - and Y -positions clockwise moves the displayed information left and down, respectively.

The focus and brightness preset adjustments are located at the top, right central portion of the unit. They are on the power supply regulator circuit (G836) that is somewhat recessed from the top of the unit. The brightness preset is the rear of the two. This potentiometer allows the range of the front panel brightness control to be limited to any maximum brightness desired. Turning the brightness preset counter-clockwise increases the maximum brightness range of the front panel control. Generally, this control is set so that at maximum brightness setting on the front panel knob, the displayed information does not "bloom" causing a degradation in resolution. The focus potentiometer is in front of the brightness preset. The adjustment is quite insensitive and requires several turns to go through focus.

### 2.5 INPUT SIGNAL REQUIREMENTS

## NOTE

The deflection amplifiers must not be driven so that the CRT beam is off screen for any length of time or permanent damage may occur. Ensure that input deflection signals fail to a safe, on-screen value.

The VR14 requires analog voltage inputs for the $X$ - and $Y$-deflection, and a logic level change or pulse for intensify. The X - and Y -inputs are identical, however, because the CRT is a $3 \times 4$ rectangle, only $3 / 4$ the horizontal deflection is required for full vertical. The deflection inputs are differential but may be driven from single-ended sources. When using single-ended sources, the differential input is helpful in eliminating annoying ground loops and hum, etc. By carrying the "local" common or ground along with the deflection signal from where it is generated, a quasidifferential signal is generated. Instead of terminating this ground at the VR 14 chassis, use the ground as if it were one side of a differential signal (the other side being the deflection signal itself). The VR14 will use the deflection signal with respect to its own ground and not the VR14 ground, which, most likely, will be different causing picture ripple and hum. If a separate ground is not available, the single deflection signal is applied to one side of the differential input, the remaining differential input is terminated with the source impedance of the driving signal or, if this is low, the input is simply grounded (signal ground not chassis ground. Signal ground is the shell of the BNC connectors that are isolated from the chassis or pin no. 9 and pin no. 12 that are $X$ - and $Y$-signal ground, respectively). Never use chassis ground for X - and Y -input reference - always use signal ground. When using balanced or differential inputs, tie each side of the twisted-pair shielded cable to the two inputs and the shield to the signal ground. The importance of using signal ground cannot be overstated; most noise and washing displays are a result of indiscriminate grounding.

The minimum voltage signal for full X -deflection is 2 V peak-to-peak and 1.7 V for Y and R 1 and R2 on the A225 are 3.3k (see Figure 3-1). For larger input signals, R1 and R2 are normally 10k. With 10 k , the maximum input sensitivity is 0.5 V in. The input impedance is $5 \mathrm{k} \Omega$ minimum for maximum sensitivity (R1 and R2: 3.3k) and 20k minimum for R1 and R2 $=10 k$. When driving long cables (more than 30 ft ) high-speed deflection may not be possible unless the cables are terminated in a low impedance (less than $100 \Omega$ ) since the VR14 input impedance is too high for this application. An easy way to attain high-speed deflection is to use the 24-pin rear connector for the input signals and place the terminator across the BNC connectors (since they are in parallel with the input). Needless to say, if terminated lines are used, the X - and Y -driving source must be of low enough impedance to tolerate the additional load.

The deflection amplifiers can be operated as inverting or noninverting by selecting either + or - on each polarity switch at the rear panel. If the polarity switches are down, -, the deflection on the screen will go up and to the right when the deflection signal on the +BNC (pins no. 7 and no. 10) goes more positive with respect to the - BNC (pins no. 8 and no. 11). If the polarity switches are up, + , the deflection on the screen will go up and to the right when the deflection signal on the + BNC (pins no. 7 and no. 10) becomes more negative with respect to the -BNC (pins no. 8 and no. 11).

Input signals larger than 2 V may be used by attenuating with the gain controls and R1 and R2 on the X - and Y -deflection circuit boards. However, the potentiometers become much too sensitive for input signals greater than 10 V peak-to-peak and R1 and R2 should be increased to provide pre-attentuation for these larger input signals. The input signals may be bipolar such as $\pm 5 \mathrm{~V}$ or unipolar such as 0 V to +5 V or 0 V to -5 V . The position potentiometer allows the deflection to be offset plus or minus half a screen; thus, a unipolar signal may be completely centered on the screen. Offsets more than half of the full-scale inputs cannot be handled. In other words, if the full-scale deflection is offset from 0 V by more than half its full scale value, centering on the screen cannot be accomplished. A 3 V peak-to-peak deflection signal, for example, may not be offset from 0 by more than $\pm 1.5 \mathrm{~V}$. So $\pm 1.5 \mathrm{~V}$, 0 V to -3 V or V to +3 V are all acceptable, but a deflection input that goes from +TV to +4 V cannot be used until it is shifted down a minimum of IV. Table 2-2 summarizes the control settings for various inputs.

The Z-intensify input requirement is simply a TTL transistion from high to low. This triggers the intensity circuit to generate a 300-ns intensify pulse. The driver must sink 4 mA when low.

## NOTE

The intensify signal must be delayed from the X - and Y position signal for an appropriate length of time to allow the deflection coil to settle the electron beam to its required position. Failure to do so displays smeared dots that are located incorrectly on the screen.

Table 2-2
Control Settings

| Input Deflection | Position Setting | Rear <br> Polarity Switch |
| :---: | :---: | :---: |
| $\begin{aligned} & \pm 2 \mathrm{~V} \text { to } 5 \mathrm{~V} \\ & 0,0=\text { center } \\ & +2 \mathrm{~V} \text { to }+5 \mathrm{~V} \text { is up } \\ & \text { and to right } \end{aligned}$ | With no inputs, set position on $X$ and $Y$ to center ( 0 V at A02-A (for X) A03-A (for Y)) | Down (-) |
| 0 V to +2 V to +5 V <br> $0,0=$ upper right <br> screen | With no inputs, set -2.2V@A02-A, A03-A with $X$ - and $Y$-position potentiometers | $\underset{(+)}{U_{p}}$ |
| $\begin{aligned} & 0 \mathrm{~V} \text { to }-2 \mathrm{~V} \text { to }-5 \mathrm{~V} \\ & 0,0=\text { lower left } \end{aligned}$ | With no inputs, set +2.2 V dc@A02-A A03-A with $X$ - and $Y$ position potentiometers | $\begin{gathered} \mathrm{Up}_{(+)} \end{gathered}$ |
| All signals are + BNC with respect to -BNC. Reversing input connections is the same as reversing the rear polarity switches. All single-ended signals applied to + BNC must have -BNC tied to signal source ground. The -BNC cannot be left open circuited. |  |  |

Also, at least a 500 ns waiting period must be allowed to intensify a dot before commanding the electron beam to move to its next location. Not giving enough time to intensify a dot after the deflection is settled will also smear the dot, since the deflection amplifier will start "dragging" the dot to the new position. The amount of delay required from the time new X - and Y -position information is presented to the VR14 and the intensify pulse is requested depends upon how large a position change is requested and how perfectly settled the dot has to be to its final ideal position. Full-scale deflection changes, such as far left to far right or corner to corner, require a $20-\mu \mathrm{s}$ waiting period for the dot to settle to within 0.01 in . of its final value. If larger errors can be tolerated, $18 \mu \mathrm{~s}$ may be used. Small deflection changes require much less time. A 0.1 in . change can be settled in less than $1 \mu \mathrm{~s}$. If there is no way for the circuits driving the VR14 to distinguish small position changes from large ones, each change must be assumed to be large and thus requires the worst-case delay. Also, if the D/A converters driving the display have "gliches" (error spikes generated while changing values), proportionately longer delays are required, since the deflection amplifiers will have to recover from the "gliches".

The Z-direct allows direct modulation of the brightness. Positive-going signals increase brightness. This input is not direct coupled; therefore, de brightness information cannot be used. The RC time constant is approximately 30 ms . The Z-direct may be used with or without the Z-intensify input. If Z-direct is used with Z-intensify, it can alter the brightness of the normal intensify pulse by adding or subtracting at the CRT grid. This is accomplished by pulsing the Z-direct with a pulse of equal duration with the Z-intensify. By varying the amplitude and polarity of the Z-direct pulse, the dot will be of a different brightness. When using Z-direct without the Z-intensify (such as for vector intensity control or any other nonpoint plotting application) the signal must be large enough to overcome the CRT cutoff. A typical direct signal will have 5 V to 10 V of actual brighness information riding on top of a 40 V pedestal; the 40 V pedestal insures that the CRT will reside below cutoff.

The Z-select works in conjunction with the front panel channel select switch. The Z-select allows the Z-intensify pulse to be gated or time multiplexed. When the channel select switch is on the 1 and 2 position, Z-select inputs have no affect on the VR14. When the channel select switch is in the 1 position, Z-intensification occurs only when Z-select input is a TTL high. When the channel select switch is at 2, Z-intensification occurs only when Z-select is held at a TTL low. Thus, if two separate pieces of information are to be displayed, by placing Z-select at a high only during channel 1 intensification times, and low only during channel 2 intensification times, both curves will be displayed when the channel select switch is at $1 \& 2$ and only channel 1 when channel 1 is selected, and channel 2 when channel 2 is selected.

## CHAPTER 3 THEORY OF OPERATION

### 3.1 X-AND Y-DEFLECTION CIRCUITS

The X - and Y -deflection circuits are identical; therefore, only one axis will be described. The deflection circuit consists of the A225 circuit board, two power transistors, and a deflection yoke (see Figure 3-1). The input signal, after going through a polarity reversal switch, is applied to pins E and B on the A225 circuit board. The input signal is handled as a differential or balanced signal, even if the input is driven from a single-ended source (the single-ended source being a special case of a balanced input where one side is grounded). R1 and R2 establish the minimum input impedance and form an attentuator with R3, the gain potentiometer. The voltage developed across R3 is amplified and converted from balanced to single-ended by amplifier E1. El is an inverting amplifier whose gain is established by the resistor ratios of R7 to R4 and R6 to R5. The bandwidth of the amplifier is tailored by C5 and C6, which act internally on the integrated circuit, and C13 and C14, which act at high frequency to roll off the low frequency gain established by the R7 to R4 and R6 to R5 ratios. A $\pm 6 \mathrm{~V}$ is generated for both E1 and E2 from the $\pm 20 \mathrm{~V}$. This is done by dropping resistors R18 and R19 and zener diodes D5 and D6.

Cl and C 3 and C 2 and C 4 are local high frequency bypass filters for the $\pm 6 \mathrm{~V}$ to reduce any high frequency signal noise at each operational amplifier, thus avoiding the possibility of parasitic oscillation. The single-ended output of El is connected to R4, which is the input to the actual deflection amplifier; E1 serves more as a signal conditioner-preamplifier.

The amplifier is essentially an inverting voltage to current amplifier, that is, an input voltage is converted to an output current $180^{\circ}$ out of phase or inverted with respect to this input. Because the input is a voltage, however, the output current must be converted back into a voltage in order that the feedback compare volts with volts. Current is converted to voltage with a $0.5 \Omega$ resistor in series with the yoke. The voltage across this resistor is an exact replica of the current flowing in the yoke; thus, the amplifier compares the input voltage with the yoke current to ensure that the yoke current is an exact replica of the input position signal. E2 compares the input voltage at R4 with the feedback voltage at R33, R10.


Figure 3-1 X - and Y -Deflection Circuit

Because the amplifier has voltage gain, only a small voltage is needed between pins 10 and 9 of E2 to cause large changes in the output. Pin 9 of E2 is referenced to ground through R13, which is strictly an impedance balancing resistor that minimizes offsets in E2 due to temperature changes. Therefore, pin 9 is essentially grounded. If any voltage appears at pin 10 of E2, the output will immediately respond in a manner that tends to reduce the voltage at pin 10 to zero; thus, a null is always achieved at pin 10 of E2. If a variable voltage is present at the input of R4, the output (or yoke current) will vary in such a manner that a continuous null is achieved at pin 10 . The only way this can occur is if instantaneously the yoke current undergoes exact equal and opposite changes to those occurring at the input to R4. Therefore, the yoke current will be an exact but opposite polarity replica of the input voltage.

In absolute numbers, the actual yoke current versus input voltage can be determined by comparing resistor ratios. For example, if +IV is applied to the input of $\mathrm{R} 4,1 \mathrm{~mA}$ will flow through R4. This occurs because the amplifier forces pin 10 of E2 to 0 V ; thus, one side of R 4 is 0 V , the other is 1 V , so 1 mA flows. This current does not flow into pin 10 of E2 because, if it did, pin 10 would rise in voltage because the input of E2 looks like a high impedance. The current must flow through R10 and R33. The only way for this to happen is if the feedback voltage is a negative value, because $R 10 / R 33$ is tied to pin 10 which is $0 V$; so pin A must be negative. In fact, if 1 mA flows through R10 and R33, the feedback voltage must be 3.2 V and negative. The -3.2 V originates from the $0.5 \Omega$ resistor in series with the yoke; therefore -3.2 V divided by $0.5 \Omega$ current is flowing through the yoke. This, of course, is -6.4A which is an excessive amount of voltage and current limit circuits (explained later) would probably be called into action to limit the output transistors.

The remaining transistors on the A225 boost the current from E2 to a sufficient drive level to operate the power transistors on the large heat sink. The output of E2 drives Q1 through its base resistor R14. Q1 serves two purposes: a stage of inversion and a level shifter. Inversion is necessary to get the final output in the proper polarity for negative feedback. Level shifting is required to drive Q2 at its base voltage; E2 cannot do this alone. The Q1 stage has no voltage gain but has current gain. Q2, however, has voltage and current gain and is where the true output voltage is first generated. Q2 is a "grounded" emitter amplifier where, in this case, the emitter, although tied to +20 V , can be considered "grounded" and the collector resistor R23 is not tied to -20 V but, for analysis, tied to -40 V . Q2 has the capability of swinging its collector almost a full $\pm 20 \mathrm{~V}$. This large swing is necessary for the yoke and must swing as close as possible to the $\pm 20 \mathrm{~V}$. The reason for this will be explained later.

The collector of Q2. drives Q3 and Q4 which are emitter followers for the positive and negative outputs. Since a low output impedance is necessary, emitter followers are used; however, Q3 and Q4 are not capable of handling the output power necessary since each can only drive 0.5A. A bootstrap power stage is used to raise the emitter follower current capability to the $\pm 4 \mathrm{~A}$ required. This is accomplished with two power transistors on an external forced-air cooled heat sink.

These external transistors are essentially "slaved" to the Q3 and Q4 emitter followers. Because the positive swing and negative swing work in the same way, only the positive is described. When the amplifier is required to deliver positive current in the yoke, the circuit responds by turning Q2 on, thus placing a positive voltage on the base of Q3. Q3's emitter responds in a similar manner; however, it cannot supply the necessary yoke current. Still, Q3 attempts to deliver the necessary current . Unlike a normal emitter follower, Q3's collector is not tied to +20 V , but instead to the base of the 2N4399 Power Transistor. Thus, when Q3 tries to deliver the output current from its emitter, this very current must flow into Q3's collector from the base of the 2N4399 which will now turn on. Because the 2N4399's collector is also tied to the output (the yoke) it also supports the output current and, in fact, becomes the primary source of output current. Depending on Q3's demands, the 2N4399 0 is completely slaved to Q3. If Q3 turns on harder, so does the $2 N 4399$. If Q3 shuts off, so does the 2N4399. Therefore, the output looks like it is an emitter follower (Q3) but the 2N4399 delivers all the current and handles the necessary power dissipation requirement.

To minimize power consumption, the output would like to operate in Class B; that is, while positive current is required, no negative current transistors should be turned on and vice versa. However, this approach creates problems at the point where the transition between positive and negative current takes place. The reason is that one set of transistors does not shut off exactly where the other set takes over, but instead shut off prematurely. This creates a dead zone or "no man's land" where neither the positive nor the negative transistors are on and controllable. The appearance on the CRT screen of such a phenomenon is a bunching or nonlinear compression of displayed information where it occurs (usually near the center of the screen). This problem can be solved by not allowing the positive transistors to shut off at zero, but rather conduct somewhat into the opposite side's region. In so doing, the positive transistors would not shut off, for example, until the negative transistors were well turned on. Thus, the amplifier would have control to cancel any nonlinearities that might occur. This task is accomplished with R23, R26, R27. The major influence is R23 because it places voltage between Q3 and Q4 bases which allow one to be on a little into the conduction region of the other. If R23 were 0 , the dead zone would be very abrupt causing maximum distortion. On the other hand, as R23 is increased, the transistor conducts further and further into the opposite side's operating region. This creates two major problems. The power dissipation causes excessive heating of the output stage and the extra current required overloads the power supply. The value of R23 is chosen, therefore, to minimize dissipation but also to minimize the cross-over distortion.

The output at the yoke has the capability of swinging a full $\pm 20 \mathrm{~V}$. This is necessary because even though the yoke is less than $0.1 \Omega$ at dc , it has inductance; thus, to force current through at high speeds requires a lot of voltage $(V=L \Delta i / \Delta t)$. To change 2 A through $20 \mu \mathrm{H}$ in $2 \mu$ s requires 20 V . That is why the A225 not only has to boost the input signal to a large current but also has to have good voltage capability to force the yoke current to change quickly.

Position control in the A225 is accomplished by adding another input to E2 exactly the way the signal comes in. This is accomplished with R9. The position "signal" is nothing more than an adjustable dc level (from R8) which, through R9, adds or subtracts voltage from the actual input signal. This allows the displayed information to move up/down, left/right on the screen or, in the case of offset input signals, allows the information to be centered on the screen.

The remaining component on the A225 is frequency compensation which allows the amplifier to operate over its required bandwidth without oscillation. Because the amplifier must operate from dc to beyond 1 MHz , the voltage gain must be reduced continuously at higher and higher frequencies. If this were not done, excessive phase shift between input and output (from feedback) could cause the output to be in phase with the input and thus oscillate. R12, C15 and R32, and C16, R3, and C11 perform the required gain reduction functions. R12 reduces the open-loop gain of E2 at all frequencies. C11 reduces the gain of $Q 2$ at high frequencies and is of major significance to the overall bandwidth. The yoke itself represents a major roll off for the amplifier, and its high frequency characteristics dominate the stability of the amplifier. An RC network across the yoke enhances the high frequency settling characteristics of the yoke.

The power output stage (2N5302 and 2N4399) is current limited by the +20 V and -20 V power supply regulators. If the deflection amplifiers are driven way off screen, the power supply limits the maximum current to 11 amps . If this condition is allowed to exist, eventually either the +20 V fuse or the -20 V fuse will blow rendering the circuit safe from such overloads.

### 3.2 PLUS AND MINUS LOW VOLTAGE REGULATED SUPPLY

The input line voltage is stepped down in the power transformer to approximately 30 V rms. There are two identical secondary windings to deliver these 30 V . Both windings are connected in series making a 60 V center-tapped winding. Using full wave bridge rectification, the ac becomes approximately 70 Vdc . By grounding the center tap, these 70 Vdc split evenly with respect to ground; thus, $a+35 \mathrm{~V}$ and a -35 V are available with respect to ground. A filter capacitor on each $\pm 35 \mathrm{~V}$ line smooths the ripple and finishes the task of generating the raw, unregulated dc for the $\pm 20 \mathrm{~V}$ regulators. The regulators are contained on the G836 circuit board (see Figure 3-2) and the heat sink adjacent to the G836. Since the $\pm 20 \mathrm{~V}$ regulators are symmetrical, only the negative regulator is described. The raw $\pm 20 \mathrm{~V}$ (actually $\pm 35 \mathrm{~V}$ ) is dropped by R33 and R34 and preregulated with D5 and D6 to +12 Vdc and D7 and D8 to -12 Vdc . The $\pm 12 \mathrm{Vdc}$ are the voltages necessary to operate E 1 and E2; they are also used to generate the reference voltage with which the output voltage will be compared. The reference for the -20 V regulator

is made with the +12 Vdc passing through R 1 and establishing +6.2 V across D 1 . Cl across D 1 reduces the dynamic resistance of the reference by removing high frequency fluctuations. The +5.6 V reference voltage is delivered to R2, which ties to the summing point (pin 2) of operational amplifier E1.

The feedback from the output regulated voltage through R3 is also applied to the summing point of E1. The nature of the circuit is that a null will be maintained at pin 2 of E1. Therefore, because the voltage on R2 (reference) is stable, the only variable is the output. Whenever the output changes for any reason, the null is disturbed at pin 2 of E1; El then forces the output to change in a manner that returns the null. For example, if the input line voltage increases causing the raw -20 V to increase, the -20 V regulated output starts to climb. The null would then be disturbed and E1 would shut the output down somewhat so that the null could be maintained. On the other hand, if a heavy load occurred on the -20 V regulator causing the -20 V to drop, the null would again be disturbed and El would act in a way that would turn on the output hard enough to return to its proper level, the level that maintains the null.

This regulating action takes place in a matter of microseconds. The actual output voltage at which the null will be maintained is determined by the ratio of R3 to R2 times the reference voltage. The mechanics of how El controls the output can be traced stage by stage. El drives an emitter follower, Q1 to give the output of E1 sufficient drive capability to fully turn on Q2, if required. Q2, through R12, controls the base current of the series pass transistors that are external to the G836 board. The pass transistors maintain a constant output, since they are supplied power from the raw dc source. Because of the high open-loop voltage gain, high frequency networks are used to roll off the gain of the regulator to ensure stable nonoscillatory operation. C2, R5, and C5 serve this purpose.

The actual point where the output voltage is regulated is determined by where the sense leads are tied. The sense leads are nothing more than the feedback and the reference ground for the regulator. If the regulator simply monitored its regulated voltage at the G836 circuit board, voltage drops across the wires carrying the current to the deflection amplifier could not be cancelled. By tying the sense leads at the deflection amplifier, -20 V is maintained where it is needed, at the load (deflection amplifier).

The output power transistors are current limited by D13, D14. These diodes conduct whenever excessive collector current is demanded. In so doing, the diodes limit the base drive, thereby limiting the maximum fault current that may flow.

### 3.3 CRT ELECTRODE VOLTAGES

The CRT electrode voltages are the filament, cathode, grid 1, grid 2, focus, and anode. The filament is simply a step down winding on the power transformer that delivers 6.3 Vac directly to the filament. The cathode and grid 1 bias voltages are generated from a $35-\mathrm{Vrms}$ winding on the power transformer. This winding terminates on the G836 (see Figure 3-2). Through D11, C17, R36, and C16 this winding generates a -80 Vdc by half-wave rectification. The same winding in like manner generates +80 Vdc from D12, C18, R37, and C19. The -80V is applied to one side of the front panel brightness potentiometer. The wiper of this potentiometer goes to grid 1 and the remaining side of the potentiometer returns to the brightness preset potentiometer (R38). R38 sets the maximum "positive" value the front panel potentiometer can achieve. The front panel potentiometer, when turned full counterclockwise, connects the wiper and grid 1 to -80 V , cutting the CRT beam off completely. As the potentiometer is turned clockwise, grid 1 becomes less negative (or more "positive"), the maximum value determined by setting R38 on the G836. Intensity on the screen is generated by cathode pulses from the W682 card. When not intensifying, the cathode is held at +60 V . The +60 V is derived from the +80 Vdc at the W682 board (see Figure 3-3). When the beam is to be turned on, the +60 V on the cathode is "grounded" or made OV. However, this alone does not determine brightness, since intensity is related to grid-to-cathode voltage. Thus, the cathode is constantly going between +60 V and 0 V but, depending on where the grid voltage (brightness potentiometer) is set, the beam may never be on, dim, or very bright.

Grid 2 of the CRT is operated at approximately 400 Vdc . The 400 V are generated by a voltage doubler on the G836 board. The ac passes through C4 and is prevented from going negative by D9. This causes the entire peak-to-peak voltage to become positive. D10 rectifies this voltage and C15 filters; the resultant output is +400 Vdc . The 400 Vdc goes directly to G 2 . If G 2 is not substantially positively biased, the CRT beam can never be turned on, regardless of how much grid to cathode drive occurs. The 400 Vdc also goes to one side of the focus potentiometer R35 on the G836 board. The other side of the potentiometer goes to -80 Vdc . The wiper goes to the focus electrode on the CRT. Because of CRT manufacturing tolerances, proper focus may occur from unit to unit anywhere between -80 Vdc and +400 Vdc . The focus potentiometer has sufficient range to accommodate any 12 M 63 CRT. The anode is supplied 11.5 kV from the high voltage supply.

### 3.4 HIGH VOLTAGE POWER SUPPLY

The high voltage supply is a self-contained high voltage source that requires only line voltage input. The input is actually the split primary of its own internal step-up transformer. For 115 V operation, the primary windings are operated in parallel; for 230 V operation, they are operated in series. The step-up transformer delivers high voltage ac to a voltage doubler and filter. The ultimate de voltage


E1 IS DEC 7400 N
PIN 7 ON IC $=$ GND
PIN 14 ON IC $=+5 \mathrm{~V}$
RESISTORS ARE $/ 14 \mathrm{~W}, 10 \%$

Figure 3-3 Intensity Amplifier W682, Circuit Schematic
is 11.5 kV and unregulated. Thus, the high voltage is slaved to the line voltage, i.e., when the line is 105 Vac , the high voltage is 10.5 kV ; when the line is 125 Vac , the high voltage is 12.5 kV .

Because the electron beam is accelerated by the high voltage, the ability to deflect the beam will change as the high voltage changes. If a constant deflection current flows through the yoke, the amount of deflection is reduced if the anode high voltage is increased (smaller displayed picture); the deflection grows if the anode high voltage decreases (larger displayed picture). The actual deflection factor change is proportional to the square root of the ratio of the old anode voltage to the new anode voltage, i.e., deflection factor $=\sqrt{V_{1}}$. For example, if the high voltage is halved, the deflection would grow $1.414(\sqrt{2 / 1})$. In terms of line voltage, the deflection factor is approximately 0.4 of the change, i.e., a 5 percent line change causes a 2 percent deflection change.

### 3.5 INTENSITY CIRCUIT

The intensification of points on the screen is controlled by the W682 circuit board. The intensity signal is routed to pin J. This signal is a transition from a high to a low. While the Z-signal is at a high (above +2.4 V ), the output from gate A (pins $8,9,10$ ) is low. When the Z-input is low momentarily, the output of A goes high. This positive going transition is ac coupled through C2 and becomes a positive spike that exponentially decays to 0 . The time constant of this decay is determined by C2 and R4. This positive going spike is the input to gate $B$ (pins 11,12 , and 13 ). Also, as input to $B$, is the channel select information which comes from pin $R$. This information either enables gate $B$ to respond to the intensification spike or not. Assuming $B$ is enabled from pin $R$, the positive spike causes the output of $B$ to go to a low. This low remains as long as the input spike to $B$ is above its 1 or high threshold level. As soon as the spike decays below the threshold, B's output immediately reverts to the high state. B's output is fed back to A's input (pin 10) to allow A's output to latch high, thus not requiring $A$ 's input (pin 9) to remain low, but rather be a momentary drop from a high. Of course, when the spike decays at $B$ 's input, the latching input is removed from $A$ (pin 9) thus enabling A to respond to the next negative going transition on the Z-intensify input. D5 clamps the input from going negative during the negative going transition that occurs when $A$ resets. Gate $C$ simply inverts the intensify pulse to drive the output pulse amplifier Q1. Gate C normally is low until a pulse comes along. This low "grounds" out the base drive for Q1; therefore, it will be off. D13 and D15 guarantee that Q1 will be off, even though there is a residual voltage drop across D6 and the output of gate C. Q1's collector is tied through R7 and D8 to +80 Vdc . With Q1 off, the collector tries to ride up to +80 Vdc , but D 7 begins to conduct at +60 V clamping the collector at +60 V . The +60 V is generated by dropping the +80 V across R8 and zener diode D14. Q1's collector is tied through R12 to the CRT cathode. Therefore, in the absence of an intensify input, the cathode resides at +60 V . This, along with the negative bias on the grid, keep the CRT beam shut off. When an intensify signal
occurs, gate C 's output goes high, allowing Q1 to receive base current from the +80 Vdc via $\mathrm{DI7}$, R11, R5, D13, and D15. This base drive turns on Q1 causing its collector (and the cathode of the CRT) to go from +60 V to 0 V . This turns the CRT beam on. The duration of this intensify pulse is determined by the time constant of C2, R4 and is normally 300 ns . D16 prevents the voltage supplied to R 5 from exceeding 5 V ; this is necessary to prevent damage to gate C .

When power is removed from the VR14, the CRT must be prevented from blooming and possibly burning the phosphor. Blooming can occur because the necessary voltages that keep the CRT grid cathode ( $\pm 80 \mathrm{Vdc}$ ) shut off drain to OV faster than the high voltage supply. When the grid-to-cathode voltage becomes more positive than cutoff, the CRT furns on very hard. D8 and C14 prevent this from happening. When power is turned off, the +80 V goes to OV but, in so doing, C 4 hangs on to its voltage and thus back biases D8 which does not allow C4 to discharge. C4 momentarily acts like Q1's power source, allowing the collector (and CRT cathode) to hold at +60 V which is the safe or off condition. Eventually C4 discharges; however, by that time the high voltage has also discharged rendering the CRT safe.

Five volts are supplied at pin A for E1 and also as a clamp for D16. A +3 V logical one level is generated across D9, 10, 11, and 12 through R2. D2 and D3 protect gate A and gate D inputs from exceeding +5 V . D1 and D4 prevent the same inputs from becoming negative.

The two remaining inputs on the W682 are the Z-select and Z-direct. The Z-select is a bit that allows the intensity pulse to be multiplexed or time enabled. As mentioned before, whether or not the intensity pulse is allowed to pass to the output through gate $B$ depends on whether or not a high input is available at pin 13 of gate B. This high is continuously available independent of $Z$-select input, when the channel select switch is in the $1 \& 2$ position. When the channel select switch is in the 1 position, intensification occurs only when a high is presented at Z -select and an intensify input is presented. When the channel select switch is in the 2 position, gate B is enabled only when the Z select input is a low.

The Z-direct is an input directly to the grid through C5. Video or other time varying brightness information may be coupled to the grid at pin D.


Figure 3-4 Circuit Diagram, G838

In the event of a failure of either the $\pm 20 \mathrm{~V}$ supplies, deflection ceases and a bright spot occurs on the CRT causing a burn. To prevent this, G838 (see Figure 3-4) contains a circuit that supplies +5 V to the W682. If either the +20 V or -20 V goes to 0 (in the case of a short circuit or blown secondary fuse), the circuit supplying the +5 V shuts down. Because the G 838 has a low value resistor across the $5 \mathrm{~V}(47 \Omega)$ the 5 V line ( pin A ) on the W 682 is grounded. This causes the base drive to Q 1 to be shunted to ground through D16 and renders Q1 off ( +60 V ), which shuts off the CRT.

## CHAPTER 4

## MAINTENANCE

This chapter deals with the prevention, diagnosis, and repair of fault conditions. Successful troubleshooting of the VR14 may be performed using a volt-ohm-milliampere meter; however, an oscilloscope facilitates and expedites isolation and repair of faults.

### 4.1. PREVENTIVE MAINTENANCE

VR14 preventive maintenance consists of ensuring that the equipment is getting and maintaining proper air flow for cooling and a periodic, cursory inspection for abnormal hardware conditions. Because of the power dissipation on the deflection and regulator heat sinks, good air flow must be maintained. A periodic check is required to see that fans are operating properly and are not obstructed either by dirt, dust accumulation, or inadvertently blocked by external equipment or surfaces.

Prolonged off-screen deflection of the CRT beam can damage the VR14. Ensure that the $X$ and $Y$ driving signals into the VR14 never drive the CRT beam off screen because of intermittent incorrect signals.

### 4.2 TROUBLESHOOTING

VR14 troubleshooting may be done with a volt-ohm-milliampere meter and most tests can be done with a VOM; however, more exacting information can be seen with an oscilloscope.

NOTE
When making voltage measurements on a malfunctioning VR14, set the voltmeter (or oscilloscope) to the proper range, connect the leads to the test points, then turn the power on and off very quickly so that the anticipated reading may be taken. Power is only on for a very brief moment. In this way, fault conditions may be discovered without causing further damage. Never leave power on to a malfunctioning or repaired VR14 until all necessary checkpoints are measured and proved nominal (see Figure 4-1).
The circuit card connector block as viewed from the wiring side is labeled A01 to A04 left to right on the top section and BO 1 to BO 4 on the bottom section.

Circuit Block

| A02A | $* 2.2 \mathrm{~V}$ nominal | X-Current Sample |
| :--- | :--- | :--- |
| A03A | $* 2.2 \mathrm{~V}$ nominal | Y-Current Sample |
| A02E, B | $*$ | X-Input Signal |
| A03E, B | $*$ | Y-Input Signal |
| A01U, B01V | +22 Vdc (red) | + Regulated dc |
| A01K, B01R | -22 Vdc (blue) | -Regulated dc |
| A01P | +5 Vdc | For W682 |
| B04A | 3.5 Vrms | $1 / 2$ Filament |
| B04B | 3.5 Vrms | $1 / 2$ Filament |
| B04D | +380 Vdc | G2 |
| B04F | 0 to -80 Vdc | Brightness (G1) |
| B04J | -80 Vdc to -400 Vdc | Focus |
| B04L | $*+60 \mathrm{~V}$ | Cathode With Negative Pulses |
| Brightness Potentiometer |  |  |
| Gray/Green | -80 Vdc |  |

Deflection Heat Sink - P5
$X$-AXIS $\quad Y$-AXIS
P5-2 P5-14 +21 Vdc PNP Base (2N4399)

P5-1 P5-15 +22 Vdc PNP Emitter (2N4399)
P5-3 P5-13 * $1 \mathrm{VV} \quad$ All Collectors
P5-4 P5-12 $\quad-21 \mathrm{Vdc} \quad$ NPN Base (2N5302)
P5-5 P5-11 -22 Vdc NPN Emitter (2N5302)

Regulator Heat Sink - P3

| P3 - | +43 Vdc Orange | Emitters of 2N4399 |
| :--- | :--- | :--- |
| P3 - | +42 Vdc Gray/Yellow | Bases of 2N4399 |
| P3 - 3 | +22 Vdc Red | Collectors of 2N4399 |
| P3 - 12 | -43 Vdc Green | Emitters of 2N5302 |
| P3 - 11 | -42 Vdc Gray/Blue | Bases of 2N5302 |
| P3 - 10 | -22 Vdc Blue | Collectors of 2N5302 |

All voltages measured with respect to ground (chassis or B01M, N)
*Indicates voltage depends upon input signal.

Figure 4-1 Voltage Chart

| P1-1 | +43 Vdc | Raw + dc |
| :---: | :---: | :---: |
| P1-3, 6 | Ground |  |
| P1-4 | -43 Vdc | Raw - dc |
| P2-1 | 3.5 Vrms | 1/2 Filament |
| $P 2-2,4,7,9$ | Ground |  |
| P2-3 | 3.5 Vrms | 1/2 Filament |
| P2 -5 | 70 Vrms (200 P-P) | $\pm 80 \mathrm{~V}$ tap |
| P2-6 | 150 Vrms (400 P-P) | +400V tap |
| P4-1 | +22 Vdc Red | + Regulated |
| P4-2, 14 | Ground Black |  |
| P4-3 | +22 Vdc Red | Hot + Sense |
| P4-4 | 0 Vdc Black | Cold + Sense |
| P4-5 | ```-80 to +400 Vdc Gray/ Red``` | Focus |
| P4-6 | +400 Vdc Orarige | G2 |
| P4-7 | 3.5 Vrms Brown | Filament |
| P4-8 | 3.5 Vrms Brown | Filament |
| P4-9 | -80 Vdc Gray/Green | To Brightness Potentiometer |
| P4-10 | 0 to -40 Vdc Gray/ Violet | Brightness Preset |
| P4-11 | +80 Vdc Gray/Orange | For W682 |
| P4-12 | -22 Vdc Blue | Hot - Sense |
| P4-13 | 0 Vdc Black | Cold - Sense |
| P4-15. | -22 Vdc Blue | - Regulated |

Figure 4-1 (Cont) Voltage Chart

### 4.2.1 No Picture

Probably the most common failure mode with this type of equipment is "no picture". Unfortunately, this condition can be caused by almost any malfunction such as a loss of input intensity pulse, incorrect input deflection signals driving the beam off the screen, a power supply fuse, or fan failure (thermal cutout). The following sequence of events leads to the isolation of the fault(s):

## Step Procedure

1 Check fuses. If they are in good condition, continue. If not, replace any that are blown and then continue. (If a blown fuse is replaced, leave power on only long enough to complete each check in this procedure.)
2
Remove all input signals at the rear of the unit and all modules except W682 and G836.

3
With a voltmeter (or oscilloscope) measure the +20 Vdc ( 20 Vdc to 22 Vdc is acceptable). This can be measured between $\mathrm{BOl}-\mathrm{V}$ (red wire) and BO1-M which is ground. Momentarily apply and shut down power. If the +20 V is above +22 V , refer to Appendix A , the regulator has a fault. If 0 V or below +20 Vdc occurs, the +20 V is overloaded; continue to the next step.

Set up to measure -20 V . This can be found between $\mathrm{BO1}-\mathrm{R}$ (blue wire) and $\mathrm{BO} 1-\mathrm{M}$ which is ground. Momentarily apply and shut down power. If the -20 Vdc is above -22 Vdc (refer to Appendix A), the -20 V regulator has a fault. If 0 V or below -20 Vdc , the -20 V is overloaded; continue to next step.

With a oscilloscope or meter, measure $\pm 2.2 \mathrm{~V}$ maximum at $\mathrm{A} 02-\mathrm{A}$ with respect to ground $(B 01-M)$. This point $(A 02-A)$ is the $X$-axis deflection coil current sample. Because coil current flows through a 0.5 ohm resistor, voltage measured at A02-A multiplied by two equals the current flowing. With the A225 circuit cards removed, no coil current should flow. Momentarily turn on power to the VR14. If A02-A has any voltage plus or minus. (refer to Appendix B), a deflection power transistor is shorted.
Measure the same as in Step 5 for the Y -axis deflection coil current at A03-A with respect to ground ( $\mathrm{BO} 1-\mathrm{M}$ ). Again momentarily turn VR14 power on and off. No voltage should be read; this indicates no $Y$ deflection coil current is flowing. If any voltage is observed, refer to Appendix $B$, since a $Y$-axis deflection transistor is shorted probably.
Replace the G838 circuit into A01 and the A225 circuit into A02. (Still leave the Y -axis, A 03 board out.) Measure less than $\pm 2.2 \mathrm{~V}$ at pin A02-A with respect to ground ( $\mathrm{BO} 1-\mathrm{M}$ ). Momentarily apply power. If the voltage is within safe limits (less than $\pm 2.2 \mathrm{~V}$ ), leave power on and adjust the position potentiometer on the A225 circuit. Doing this should change the voltage reading on $\mathrm{A} 02-\mathrm{A}$, proving the A 225 indeed is controlling the coil current. Return the position potentiometer to its original position. If the voltage at $\mathrm{A} 02-\mathrm{A}$ is beyond $\pm 2.2 \mathrm{~V}$, shut down immediately. Because the position potentiometer on the A225 can drive more current than the $\pm 2.2 \mathrm{~V}$ limit, it is possible that it (the position potentiometer) has been adjusted to one extreme or the other. To prove whether this is the case or if the A225 circuit board is faulty, turn the position potentiometer as follows: clockwise if the voltage at A02-A was very negative; counter clockwise if the voltage at A02-A was very positive. If no change is noted at A02-A after adjusting the position potentiometer, the A225 board is faulty and should be replaced or repaired (refer to Appendix C).

Repeat the same tests as in Step 7 for the Y -axis deflection circuit A225 plugged into A03. Monitor A03-A. Refer to Appendix C for A225 repair.

If the fault has not been isolated, the intensity circuit W682, the electrode voltages, and the high voltage supply are suspect. The output of the W682 drives the cathode. At rest, it should be +60 V and, when triggered, go to approximately 0 V . Apply a proper input to the W682 ( +3 V to 0 V transitions) and check to see that the signal reaches A04-J. If so, check A04-R with the channel select in the 1 and 2 position to see that a high is present there. If so, see that +5 V is being supplied to $\mathrm{A} 04-\mathrm{A}$. If $\mathrm{A} 04-\mathrm{A}$ is less than +4 V , replace or repair the G 838 module as this is where the +5 V is developed. If the three preceding measurements are good and the W682 output (measured at B04-L) is not going from +60 V to 0 V for at least 300 ns , repair or replace the W682 module.

Step
10

13

Measure 6.3 Vac between $B 04-A$ and $B$ and observe the glowing filament on the CRT. No 6.3 Vac can be traced back to the G836 circuit board which routes the 6.3 Vac from the transformer .

Measure the grid 1 voltage at B04-F. It should vary from -80 Vdc to between -20 V and 0 V when the front panel brightness control is varied. The -80 Vdc comes from the G 836 board. Trace back to the G836.

Measure G2 at B04-D. It should be at least +300 V . Trace back to the G836.

The last item operating improperly for no picture is the high voltage supply itself. Generally, all other measurements should be made before considering the high voltage, since the majority of "no picture" conditions will not be caused by the high voltage supply. Measuring the high voltage is extremely dangerous and not recommended. Instead, a quick method is to take a long screwdriver and ground the blade with two separate clip leads for safety. Turn the VR14 on for 5s and then SHUT IT OFF. After it is off, ground out the anode cap on the CRT with the GROUNDED screwdriver. If done within 5 s to 10 s after power is turned off, an arc should occur to the screwdriver indicating that the CRT was charged with high voltage. If no arc occurs, replace the high voltage supply.

### 4.2.2 Faulty Picture

a. No Focus

Check the range of the focus potentiometer on the $G 838$ by monitoring the focus voltage at B04-J while adjusting the focus potentiometer through its range. Minimum range is +350 Vdc to -60 Vdc . See G 836 for repair.
b. Half or Quarter of the Picture Missing

Generally, this condition represents the fact that one of the two deflection transistors is not working; thus, only half deflection is available. The transistor in question can be identified by observing which side of the screen is not working. The left and bottom portions of the screen are controlled by the PNP (2N4399) power transistors on the deflection heat sink. These are the lower two transistors; the left side of the screen is controlled by the left lower power transistor (if the deflection heat sink is viewed from the front of the VR14), the lower part of the screen is controlled by the right lower power transistor. Of course, the upper and right are controlled by the NPN (2N5302), the right side of the heat sink controlling the upper screen, the left side of the heat sink controlling the right screen.
c. The remaining possible faulty picture patterns such as picture swim ( 60 Hz ), oscillations, distortion, etc., will be restricted generally to improper input signals (especially grounding techniques) or faults on the A225 circuit board. If input signals are not suspect, a faulty A225 may be isolated by swapping $X$ and $Y$ A225s with one another to see if the problem changes axis.
d. Weak brightness but proper operation generally indicates C 5 has shorted on the W682 board. This occurs due to a rare but possible internal arc within the CRT .
e. If a weak picture that is deflected off the screen on all sides is encountered, with excessive jitter and ripple, the high voltage supply should be replaced.

### 4.3 ASSEMBLY REPLACEMENT INSTRUCTIONS

Other than the G838, A225's, and W682 circuit modules, most repair and replacement will involve the G836 regulator subassembly; the regulator heat sink assembly; and the deflection heat sink assembly; and, in rare cases, the high voltage assembly, yoke, and CRT. It cannot be stressed too strongly that the VR14 line cord be removed from the line before doing any maintenance. Turning power off or removing fuses does not render the unit safe from shock hazards, since the power switch and fuse interrupt only one side of the ac input line voltage, the other side is permanently connected as long as the line cord is plugged in. Do not take chances, unplug the line cord.

### 4.3.1 Deflection Heat Sink Removal (see Figure 4-2)

To remove the deflection heat sink proceed as follows:


1 Remove the line cord and all circuit modules above the deflection heat sink assembly (G838, A225, A225, W682).

2 Remove the four 6-32 screws that hold the heat sink assembly to the rear chassis plate.

3
Lift the assembly out to make room for removing the assembly cable connector. The 15 -pin connector is removed by squeezing the retaining tabs on each side of the connector so that when the connector is pulled, the tabs pass through square holes that they were butted against. Do not pull the connector by its wires, only by its plastic body.

4 To remove a faulty transistor unscrew the two 6-32 screws that hold the transistor down. Then pull the transistor straight out from the socket. Apply an even coat (approximately $1 / 32$ in. thick) of thermal compound to all mating surfaces of the new transistor. Replace the new transistor, making sure that the base and emitter pins are oriented properly; otherwise, the transistor case will not align with the two screw holes. Also, ensure that the insulating washer is between the transistor and the heat sink and each mounting screw has a star washer.

a. Remove circuit boards and the four 6-32 screws holding the deflection heat sink to the rear panel.

b. Remove heat sink assembly (and its connectors
if necessary) and remove faulty power transistor.
Figure 4-2 Deflection Heat Sink Removal

### 4.3.2 7007165 Power Regulator Assembly Removal

The 7007165 Power Regulator Assembly comprises a $G 836$ regulator printed circuit board with a mounting frame for J1, J2, J3, and J4. To remove the 7007165 Power Regulator Assembly proceed as follows:
Step

1 $\quad$\begin{tabular}{l}
Remove the line cord and all circuit modules (G838, A225, W682). <br>
2

$\quad$

Remove all four cable connectors (Figure 4-3) coming into the con- <br>
nector bracket on the 7007165 by squeezing the two locking tabs on <br>
the sides of each connector, while pulling the connector straight up, <br>
allowing the locking tabs to pass through the square holes they were <br>
butted against. Do not pull the connector by its wires; only pull it <br>
by its plastic body.
\end{tabular}

## NOTE

When placing the 7007165 back into the unit, ensure that the bottom of the circuit board rests in the slotted groove insulator block provided on the bottom chassis.

5
For troubleshooting, the 7007165 may be operated outside its normal mounted position by laying the board flat and reconnecting the four cable connectors. Ensure that the etch side of the module does not touch the chassis causing short circuits by insulating the board with a book or piece of cardboard as shown in Figure 4-4b.

## NOTE

The 7007165 has $+80 \mathrm{Vdc},-80 \mathrm{Vdc}$, and +400 Vdc available. Use extreme caution when troubleshooting the board. Also, these voltages do not disappear immediately when power is shut off.

### 4.3.3 Regulator Heat Sink Removal (Figure 4-5)

To remove the regulator heat sink proceed as follows:
Step Procedure

1 Remove the 7007165. See Paragraph 4.3.2 for instructions.
2 Remove the four heat sink mounting screws on the right chassis wall (when viewed from front).


Figure 4-3 7007165 Power Regulator Assembly

Step

3
4

Procedure
Lift the heat sink assembly straight out.
To remove a faulty transistor(s) unscrew the two 6-32 screws holding the transistor(s) down; then pull the transistor(s) straight out from the socket. Apply an even coat (approximately $1 / 32$ in. thick) of thermal compound to all mating surfaces of the new transistor. Replace the new transistor, ensuring that the base and emitter pins are oriented properly; otherwise, the transistor case will not align with the two screw holes. Also, ensure that the insulating washer is between the transistor and the heat sink and that each mounting screw has a star washer.

### 4.3.4 Yoke and CRT Removal

To remove the yoke proceed as follows:

## Procedure

2 Carefully remove the yoke cable connector from its mating connector on the inner side of the circuit card mounting bracket.

a. Remove power cord and all connectors to the 7007165. Unscrew mounting screws from the opposite side of the vertical chassis wall.

b. Reconnect connectors and place a cardboard under the 7007165 to prevent shorting out the circuit against the chassis when troubleshooting the board outside the unit.

Figure 4-4 7007165 Removal

a. Remove the 7007165 as shown in Figure 4-4 and unscrew the four 6-32 heat sink mounting screws from the side chassis. Remove two pin connector from high voltage bracket.

b. Lift heat sink straight out and repair faulty transistor.

Figure 4-5 Regulator Heat Sink Removal (NOTE: Thermal cutouts have 115 Vac on them - be sure line cord is removed)

Using a $1 / 4$-in. nut driver, loosen the screw that holds the yoke neck clamp by inserting the nut driver through the access slot provided in the CRT shield. Loosen sufficiently for the yoke clamp to be slipped off the yoke.

4
Carefully remove the CRT socket connector and slide the yoke clamp off the CRT neck.
5
Slip the yoke connector through the access slot in the CRT shield and pass it, along with the entire yoke assembly, off the CRT neck and out the rear. Sometimes the yoke gets stuck at the socket end of the CRT because the yoke plastic mounting piece hugs the CRT neck tightly and must be spread to pass over the CRT socket.

To remove the CRT proceed as follows:

1 Remove the yoke first as described above and double check that the line cord is removed.

2

3

4 The CRT is held by four screws, one in each corner of its shell bond frame. As each screw is removed, support the weight of the CRT.

CAUTION
The CRT is under high vacuum and is potentially in danger of explosion if subjected to sharp blows or very rough handling.

Also, to avoid dropping the CRT accidentally, never place your hand over the anode high voltage button while picking up or carrying the CRT, in case the CRT has residual charge. The shock is not, in itself, dangerous but the surprise may cause the user to drop the CRT. Never hold the CRT by the neck (the thin cylindrical portion) alone since it will break off.

### 4.3.5 High Voltage Supply Removal

To remove the high voltage supply proceed as follows:

Step
1 Remove the yoke and CRT as outlined in Paragraph 4.3.4. Ensure that the line cord is unplugged.
2 Disconnect the two red and two white wires from the high voltage supply from TB1 and TB2 of the right side chassis.
3 Remove the cast bezel by removing the three right and left retaining screws.

4
Remove the two side and two bottom high voltage assembly mount- ing bracket screws and remove the high voltage assembly out toward the front of the unit.

## CHAPTER 5

## ENGINEERING DRAWINGS

The drawings in this chapter are current at the printing date of this manual. If any discrepancies exist between these drawings and those delivered with the unit, the set of drawings shipped with the unit are to be considered the most accurate.

Table 5-1
Engineering Drawings

| Drawing No. | Title | Page |  |
| :--- | :--- | :--- | :--- |
| A-ML-VR14-0 | Master List (VR14-0) | $5-3$ | Sheets |
| D-UA-VR14-0-0 | VR14 Display Assy | $5-7$ | $(4)$ |
| A-PL-VR14-0-0 | VR14 Display Assy | $5-15$ |  |
| D-AD-7007077-0-0 | Top Mtg. Assy (VR14) | $5-23$ | $(4)$ |
| D-IC-VR14-0-1 | Block Schematic (VR14) | $5-27$ |  |
| D-DI-VR14-0-2 | Drawing Index List | $5-33$ | $(2)$ |
| A-PL-VR14-0-3 | Module Utilization List | $5-37$ | $(2)$ |
| C-MU-VR14-0-3 | Module Utilization Chart | $5-39$ | $(1)$ |
| D-AD-7007078-0-0 | Wired Assy (VR14) | $5-41$ | $(1)$ |
| A-PL-7007078-0-0 | Wired Assy (VR14) | $5-43$ | $(2)$ |
| D-UA-G836-0-0 | G836 Power Regulator Board Assy | $5-47$ | $(1)$ |
| A-PL-G836-0-0 | G836 Power Regulator Board Assy | $5-49$ | $(3)$ |
| D-CS-G836-0-1 | VR14 Power Supply and Regulator Bd G836 | $5-55$ |  |
| D-AD-7007080-0-0 | P.S. Heat Sink Assy (VR14) | $5-57$ |  |
| A-PL-7007080-0-0 | P.S. Heat Sink Assy | $5-59$ | $(1)$ |
| C-CS-7007080-0-1 | Circuit Schematic (Heat Sink) | $5-61$ | $(1)$ |
| D-AD-7007082-0-0 | Deflection Heat Sink Assy | $5-63$ | $(1)$ |
| A-PL-7007082-0-0 | Deflection Heat Sink Assy | $5-65$ | $(1)$ |
| C-CS-7007082-0-1 | Circuit Schematic (Deflection) | $5-67$ | $(1)$ |
| D-AD-7007084-0-0 | Power Supply Assy (VR14) | $5-69$ | $(1)$ |
| A-PL-7007084-0-0 | Power Supply Assy (VR14) | $(2)$ |  |
| D-CS-7007084-0-1 | Circuit Schematic (Pwr. Sup.) | $(3)$ |  |



| PRINT SET |  |  |  | DWG. NO. |  | no. of SHEETS | title | OPTION NO. |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\begin{aligned} & Q \\ & Q \\ & \underset{y}{4} \\ & B \\ & \hline \end{aligned}$ |  |  |  |  | $\begin{aligned} & \text { REV. } \\ & \text { LET. } \end{aligned}$ |  |  |  |
| X |  |  |  | D-DI-VR14-0-2 | E | 2 | DRAWING INDEX LIST |  |
|  |  |  |  |  |  |  |  |  |
| x |  |  |  | D-CS-G836-0-1 | \# | 1 | POWER SUPPLY \& REGULATOR SCHEMATIC |  |
| x |  |  |  | C-CS-7007080-0-1 | A | 1 | POWER SUPPLY HEAT SINK SCHEMATIC |  |
| x |  |  |  | C-CS-7007082-0-1 | A | 1 | DEFLECTION HEAT SINK SCHEMATIC |  |
| X |  |  |  | D-CS-7007084-0-1 | D | 2 | POWER SUPPI Y Y SCHEMATIC |  |
|  |  |  |  |  |  |  |  |  |
| x |  |  |  | C-MU-VR14-0-3 |  | 1 | MODULE UTILIZATION |  |
|  |  |  |  |  |  |  |  |  |
| X |  |  |  | D-IC-VR14-0-1 | F | 3 | VR14 BLOCK SCHEMATIC |  |
|  |  |  |  |  |  |  |  |  |
| X |  |  |  | A-PL-VR14-0-3 |  | 1 | MODULE UTILIZATION (PL) |  |
|  |  |  |  |  |  |  |  |  |
| X |  |  |  | D-UA-VR14-0-0 | E | 3 | DISPLAY ASSEMBLY |  |
| x |  |  |  | A-PL-VR14-0-0 | E | 3 | DISPLAY ASSEMBLY (PL) |  |
|  |  |  |  |  |  |  |  |  |
| X |  |  |  | C-AD-7007078-0-0 | C | 1 | WIRED ASSEMBLY |  |
| X |  |  |  | A-PL-7007078-0-0 | c | 1 | WIRED ASSEMBLY (PL) |  |
|  |  |  |  |  |  |  |  |  |
| X |  |  |  | A-SP-VR14-0-4 |  | 4 | ENGINEERING SPECIFICATION |  |
| X |  |  |  | A-SP-VR14-0-5 | A | 31 | CHECKOUT \& ACCEPTANCE PROCEDURE |  |
|  |  |  |  |  |  |  |  |  |
| x |  |  |  | D-UA-G836-0-0 | \# | 1 | POWER SUPPLY \& REGULATOR ASSY |  |
| x |  |  |  | A-PL-G836-0-0 | \# | 3 | POWER SUPPLY \& REGULATOR ASSY (PL) |  |
|  |  |  |  |  |  |  |  |  |
| x |  |  |  | D-AD-7007080-0-0 |  | 1 | POWER SUPPLY HEAT SINK ASSY |  |
| x |  |  |  | A-PL-7007080-0-0 |  | 1 | POWER SUPPLY HEAT SINK ASSY (PL) |  |
|  |  |  |  |  |  |  |  |  |
| X |  |  |  | D-AD-7007082-0-0 | B | 1 | DEFLECTION HEAT SINK ASSY |  |
| X |  |  |  | A-PL-7007082-0-0 | B | 1 | DEFLECTION HEAT SINK ASSY (PL) |  |
|  |  |  |  |  |  |  |  |  |
| x |  |  |  | D-AD-7007084-0-0 | D | 2 | POWER SUPPLY ASSY |  |
| X |  |  |  | A-PL-7007084-0-0 | D | 3 | POWER SUPPLY ASSY (PL) |  |
| TITL | TLE |  | VR14 | DISPLAY |  |  |  | REV. <br> M |

DEC 16-(325)-1048-1-N47






DEC FORM
DRA 110















DEC FORM NO.16-1031
DRA 110


DEC FORM NO.16-1031
DRA 110














[^0]


DEC FORM NO.16-1031
DRA 110



## APPENDIX A <br> POWER SUPPLY TROUBLESHOOTING


#### Abstract

NOTE The power regulator heat sink contains a thermal cutout connected to the input line voltage. Always remove the line cord before handling the heat sink.


Generally, if the $\pm 20 \mathrm{~V}$ reads above $\pm 25 \mathrm{~V}$, one or both of the regulator transistors has shorted. The +20 V is controlled by the PNPs (2N4399) that are the front set of transistors on the regulator heat sink (as viewed from the front of the VR14). The -20V is controlled by the NPNs (2N5302) on the rear section of the regulator heat sink. If, after replacing the power transistors, the problem is not corrected, the G836 board itself is suspect. If the regulator circuits are not working, the output could be beyond its nominal value. The MC1709 is most likely suspect, followed by the drive transistors, 2 N 4923 for +20 V and 2 N 4920 for -20 V .

If, on the other hand, the $\pm 20 \mathrm{~V}$ read zero, the same power transistors are still suspect (they may be open). Also, in this case, if the two 1 N 4001 diodes used as current limiting for the power transistors are shorted, the power transistors cannot receive base current and thus will not turn on, rendering their output 0 V . To check for this condition, turn off the power and measure resistance with a VOM set at RX1 across D15 and D16 if the +20 V was 0 , and D13 and D14 if the -20 V was 0 . The resistance with the VOM lead connected either way should always be above $5 \Omega$.

## APPENDIX B <br> DEFLECTION AMPLIFIER TROUBLESHOOTING

When the deflection circuit cards (A225) are removed, their respective power transistors receive no drive and, therefore, are off. When monitoring A02-A (X-yoke current sample) and A03-A (Y-yoke current sample) no reading should be observed. Any voltage at these points indicates a power transistor is on by itself. Generally this transistor is shorted. To determine which transistor is faulty, observe which pin, A02-A or A03-A, has voltage. The A02-A (X-axis) transistors are on the right side of the heat sink assembly when viewed from the front of the VR14; A03-A ( $Y$-axis) transistors are on the left side. In both cases, a plus voltage at A02-A or A03-A means the PNP (2N4399) is at fault. This is the lower transistors on both sides. If the voltage at A02-A or A03-A is minus, the NPN (2N5302) are faulty. These are the upper transistors on both sides.

If no readings are observed at A02-A or A03-A when the A225 boards are removed, then the deflection fault is on the boards themselves (assuming, of course, proper input signals are applied and all power supply voltages are nominal). If the yoke current goes full negative only when the A225 card is plugged into that axis, the most likely suspect is the 2N2904A, Q2. If one axis is faulty, a quick check can be made by swapping the X - and Y -deflection boards (A225) to see if the faulty axis follows the circuit board in question.

## APPENDIX C A225 REPAIR

After the power supply and deflection power transistors have been proven sound, incorrect deflection coil current readings may be isolated to the A225 circuit board itself. If, when the A225 is plugged in, the deflection current goes full negative (about -4 V as measured at $\mathrm{A} 02-\mathrm{A}$ for $\mathrm{X}, \mathrm{A} 03-\mathrm{A}$ for Y ) and not controllable, Q2 has probably opened and should be replaced. If only half deflection is working (no positive current or no negative current capability) and the power transistors are operating properly, Q3 should be replaced for no positive current and Q4 for no negative current. Also, check R26 and R27 for burns. These resistors overheat if the deflection amplifier is operated in the fault current limit condition for any length of time. Finally, if C9 or C10 become shorted, R9 or R10, respectively, will burn out. Check C9 or C10 with an ohmmeter to verify this type of failure.


[^0]:    DERA 110

