Showcase:

Proposal for a single board, high performance workstation

Charles R. Rupp

17 Nov. 1983

I. Market Trends

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MARKET TRENDS

Ref: "WORKSTATION MARKET ANALYSIS: RESOLUTION AND REFRESH"
Lorraine M. Tartaglia, 6 Oct. 1983

1. WINDOW EXISTS AND IS CLOSING

2. HISTORICALLY A STRONG MARKET FOR DEC

3. MUST PLAY THE SPEC GAME:
   - MAXIMUM WHETSTONES
   - MAXIMUM DISPLAY PERFORMANCE (USER)
   - MAXIMUM MASS STORAGE

4. CONSISTENT TREND TOWARD MORE PIXELS ON THE SCREEN ("RESOLUTION")
   - LEADERSHIP PRODUCT NEEDS AT LEAST 1600 x 1280 GOING TO 2000 x 1600.

5. REFRESH RATE:
   - 60 Hz IS A MUST
   - CUSTOMERS WILL GENERALLY CHOOSE HIGHER RESOLUTION OVER HIGHER REFRESH RATE FOR SAME $

6. COLOR SPEC GAME:
   - RESOLUTION IS BASED UPON THE MEMORY AND NOT THE TUBE
   - ⇒ MUST PROVIDE THE MEMORY EVEN IF IT DOESN'T EFFECTIVELY INCREASE RESOLUTION

7. INTEGRATED OPERATING ENVIRONMENT ("ION") IS A MUST... EVEN IF NOT USED!

The SHOWCASE VAXstations

- A SET OF 6 HIGH PERFORMANCE, LOW COST WORKSTATIONS BASED ON DEC'S 1980'S SHOWCASE TECHNOLOGIES:
  - uVAX
  - Linear Bitmap Displays with programmable resolution, performance and planes.
  - LAN file, print and compute servers
- EXECUTE ALL NON-PRIVELEGED VAX SOFTWARE
  - Multiple process windows to remote compute server using virtual terminal capabilities

  IN ANY COMBINATION WITH:
  - Local software application process windows running under:
    - uVMS
    - ELAN (with or without SDA)
    - UNIX
- APPLICATION - EVERY PROFESSIONAL APPLICATION WHICH REQUIRES DISPLAYINTERACTION IN OFFICE, FACTORY, LABORATORY AND FIELD ENVIRONMENTS.
- GOAL - BECOME THE DOMINANT END USER AND OEM SUPPLIER IN THE WORKSTATION MARKETPLACE:

  1985-1990 Revenues > $2B

Showcase BLOCK DIAGRAM

C.Re.
Rev.0 5/3/83
Rev.1 5/12/83

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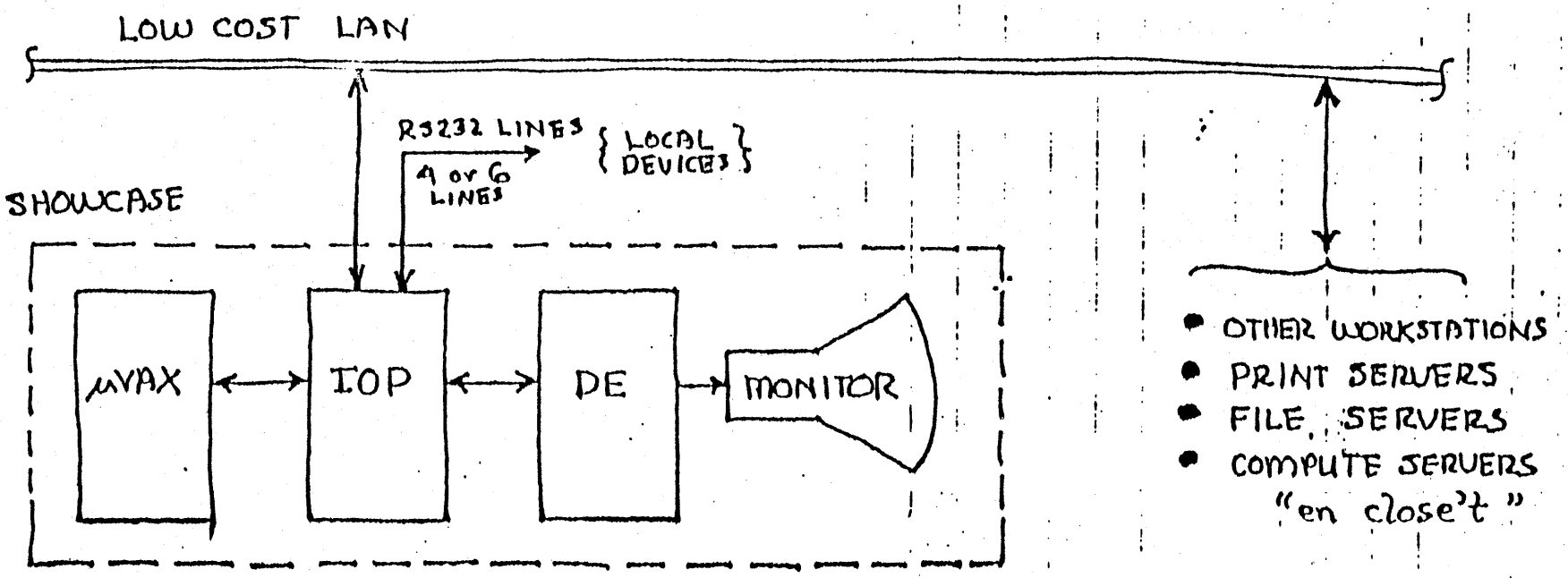

- 2 VERSIONS USING 1 CHIP μVAX:
  1. 1/2 MB
  2. 2 MB
- DEVICE EMULATORS
- PERIPHERAL EMULATORS
- PROCESS LEVEL WINDOW MANAGEMENT
- DISPLAY CONTROL
- USER I/O CONTROL
- LINEAR BITMAP ARCHITECTURE IN 2 VERSIONS:
  1. 16x2 → 3 ADDRESSING MODES
  2. 16x8 → 5 ADDRESSING MODES
- 6 VERSIONS:
  1. 1088 x 864 BW, 1 PLANE (15")
  2. 800 x 640 COLOR, 2 OR 4 PLANE (15")
  3. 1088 x 864 BW, 1-8 PLANES (15")
  4. 1600 x 1080 BW, 1-4 PLANES (19")
  5. 2000 x 1600 BW, 1, 2 PLANES (25")
  6. 1088 x 864 COLOR, 1-8 PLANES (19")

SHOWCASE PRODUCT SET

	MODEL #	1	2	3	4	5	6
(1)	CPU ENGINE	uVAX	uVAX	uVAX	uVAX	uVAX	uVAX
(2)	CPU MEMORY	1/2 MB	1/2 MB	2 MB	2 MB	2 MB	2 MB
	CPU OS	ELAN	ELAN	uVMS UNIX ELAN	uVMS UNIX ELAN	uVMS UNIX ELAN	uVMS UNIX ELAN
	DISPLAY	15" B&W (7)	15" COLOR	15" B&W	19" B&W	25" B&W	19" COLOR
	HxV RESOLUTION	1088x 864	800x 640	1088x 864	1600x 1080	2000x 1600	1088x 864
	PLANES/ ADDRESS MODES	1, 3	4, 2	1,2,4 5	8 1,2,4 4	1,2 3	1,2,4 5
(3)	RS232 LINES	4	4	6	6	6	6
(4)	PERSONAL STORE	NO	NO	YES	YES	YES	YES
(5)	CGI XFM OPTION	NO	NO	YES	YES	YES	YES
(6)	TRANSFER COST						

(1) SINGLE CHIP uVAX IN ALL VERSIONS
(2) MOSTLY 256Kbit CHIPS
(3) 1 DEDICATED FOR KEYBOARDS; IOP SUPPORT FOR: MODEM, MOUSE, TABLET, LOCAL HARDCOPY, etc.
(4) VERY LOW COST MINIFLOPPY OR TAPE USING 1 RS232 LINE > 50Kbytes
(5) FOR ADVANCED APPLICATIONS: ADDTIONAL $850 COST CGI =. COMPUTER GENERATED IMAGE
(6) GOAL AT MATURE MANUFACTURING RAMP
(7) ALTERNATIVE IS 15" VR210 MONITOR AT 800x640

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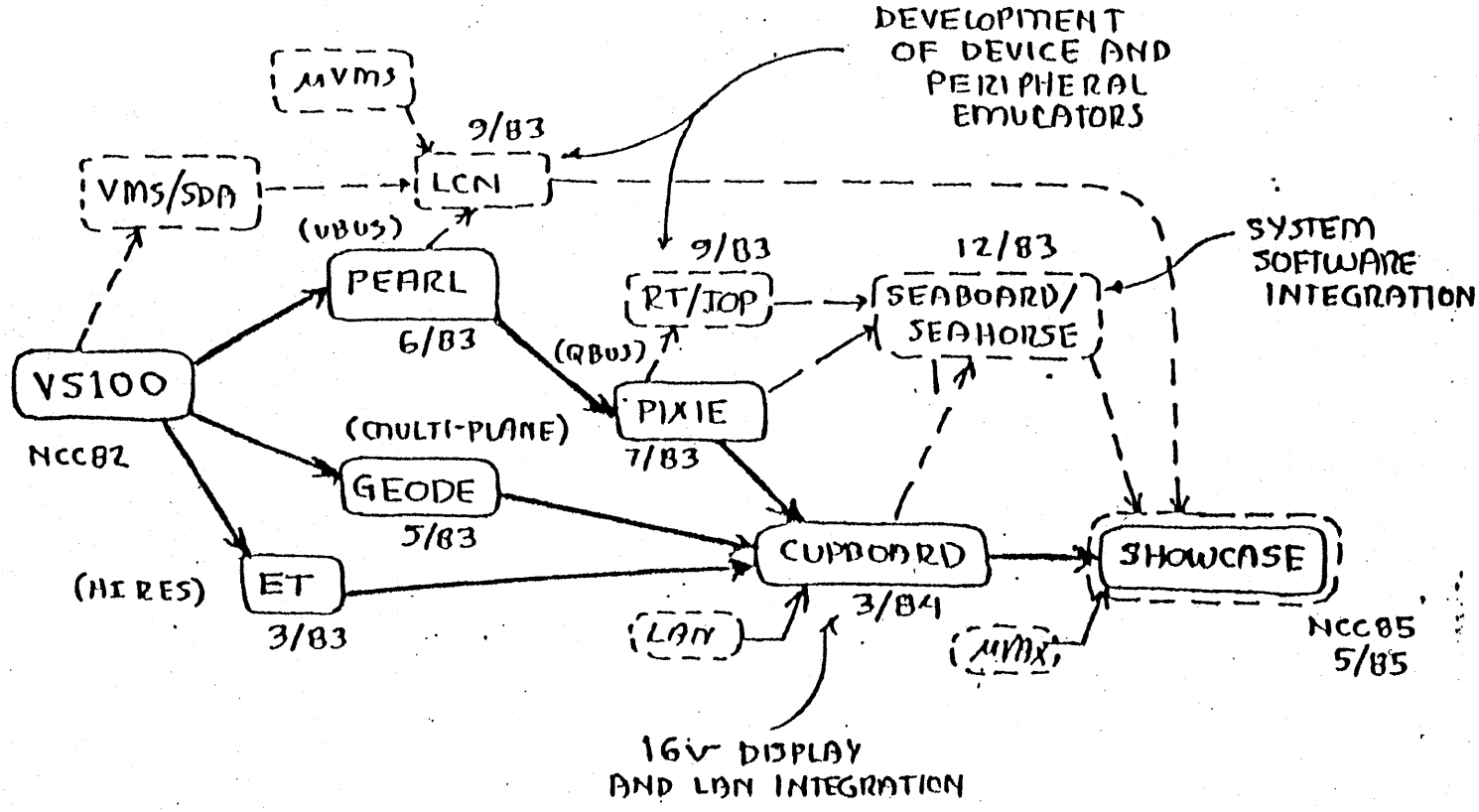

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SHOWCASE DEVELOPMENT SCENARIO

Charles R. Rupp
5 May 1983

SOFTWARE COMMENTS

① IO EMULATION...

A SINGLE MICROPROCESSOR HAS SUFFICIENT CAPABILITY TO PERFORM THE FUNCTION OF A NUMBER UNSOPHISTICATED "BUS PERIPHERALS" SUCH AS...

- D2 EMULATOR
- DISK EMULATOR
- TERMINAL EMULATORS SUCH AS VT100, VT125, TEK4014

EMPHASIS ON HIGHER PERFORMANCE THAN BUS/SERIAL LINE COUNTERPARTS
i.e. 50 K baud effective vice 9.6K baud

② "ION"

- DOUBTFUL THAT ONE APPROACH WILL SATISFY ANY LARGE PROPORTION OF ALL POSSIBLE APPLICATIONS

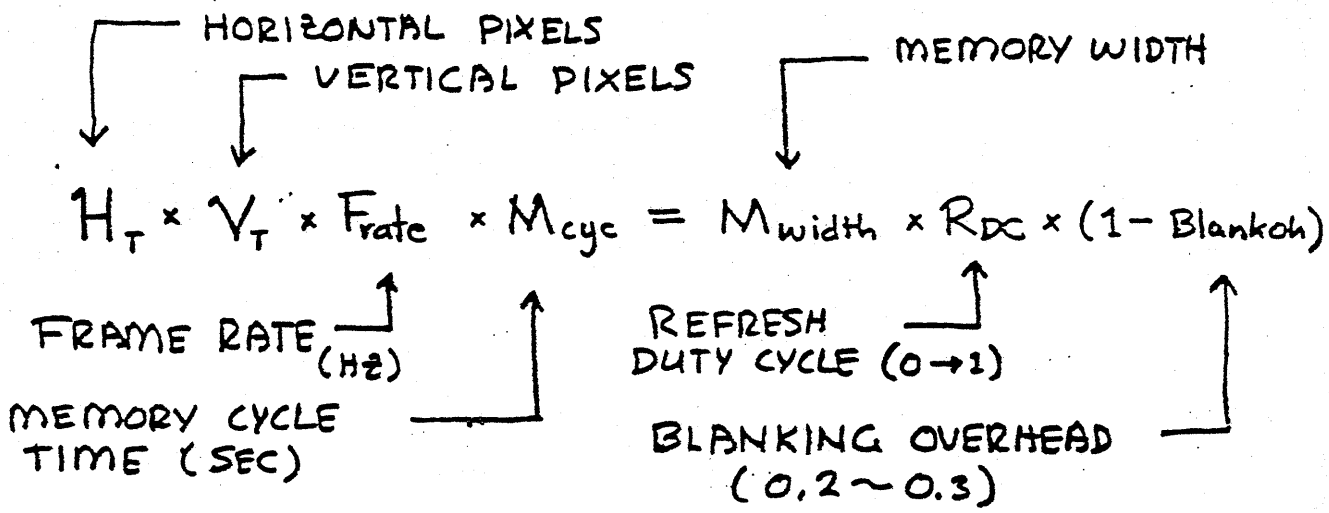
⇒

① ALLOW AT LEAST CURRENT ENVIRONMENTS

② ALLOW FOR ALTERNATIVE IONS DEVELOPED BY OEMS.

BASIC DISPLAY METRICS

- DISPLAY REFRESH CONSISTENCY: (SIMPLIFIED)



⇒ CHANGE IN ANY ONE PARAMETER MUST BE ACCOMPANIED BY: PROPORTIONAL CHANGE IN ONE OR MORE OTHER PARAMETERS.

EXAMPLE: (VS100)

$H_T = 1088$ (HORIZONTAL PIXELS)

$V_T = 864$ (VERTICAL PIXELS)

$F_{rate} = 60$ (60 Hz REFRESH)

$M_{cyc} = 0.4 \times 10^{-6}$ (400 nsec MEMORY)

$M_{WIDTH} = 64$ (64 MEMORY CHIPS)

* $R_{DC} = 0.5$ (1 OF EVERY 2 MEMORY CYCLES IS USED FOR DISPLAY REFRESH)

$Blankoh = 0.295$ (HORIZONTAL AND VERTICAL BLANKING INTERVALS REPRESENT 29.5% OF A FRAME TIME).

* NOTE: ACTUALLY PERCENT OF TIME THAT MEMORY IS USED FOR REFRESH.

- MAXIMUM UPDATE RATE (U_{MAX}) CONSISTENCY

  ↓ MAXIMUM POSSIBLE PIXELS/SECOND WRITTEN

$$U_{MAX} \times M_{cyc} \leq U_{DC} \times M_{WIDTH} \times (1 + Blankoh)$$

  ↑ UPDATE DUTY CYCLE ($0 \rightarrow 1$)

- FOR STANDARD DYNAMIC RAMS

$$U_{DC} = 1 - R_{DC}$$

($U_{DC} < 2$ FOR "VRAMs")

} $U_{DC} = R_{DC} = 0.5$ TENDS TO BE COST/PERFORMANCE OPTIMAL

⇒ COMMON PARAMETERS WITH THE REFRESH CONSISTENCY EQUATION IS THE BASIS FOR UPDATE VS. RESOLUTION TRADEOFFS.

EXAMPLE: (VS100)

$$U_{MAX} \leq \frac{U_{DC} \times M_{WIDTH} \times (1+Blankoh)}{M_{cyc}} = 103.6\ MHz$$

OR 9.6 nsec/pixel

- LEAST UPPER BOUND UPDATE RATE (U_{LUB})

  ⇒ MAXIMUM WRITING RATE FOR TYPICAL DISPLAY PRIMITIVES INCLUDING CHARACTERS AND VECTORS TAKING INTO ACCOUNT THE SETUP OVERHEAD.

- DISPLAY UPDATE "ARCHITECTURAL EFFICIENCY"

$$e = \frac{U_{LUB}}{U_{MAX}} \qquad 0 < e \leq 1.0$$

BASIC UPDATE PRIMITIVES

AOPs AREA OPERATIONS

(LARGE NUMBER OF PIXELS MOVED ⇒ NEGLIGIBLE SETUP OVERHEAD)

- "CLEAR OP" ⇒ WRITE ONLY
- "WINDOW OP" ⇒ READ + WRITE CYCLE

$U_{WINDOW\,OP} = 1/2 \cdot U_{CLEAROP}$

COPs "CHARACTER OPERATIONS"

- SIGNIFICANT OVERHEAD
- AREA WIDTH $<<$ M_{WIDTH} ⇒ RELATIVELY INEFFICIENT

VOPs VECTOR OPERATIONS

- MODERATE OVERHEAD
- 1 PIXEL / MEMORY CYCLE IS TYPICAL.

⇒

- ANYBODY CAN DO FAST AOPs (THE SPEC GAME)
- FAST COPs AND VOPs REQUIRES SPECIAL ATTENTION

ARCHITECTURAL EFFICIENCY EXAMPLES

VK100/VT125

$M_{WIDTH} = 12$
$U_{DC} = 0.5$
$M_{cyc} = 500$ nsec
Blankoh $= 0.25$

$\Big\}$ $U_{MAX} = 15.48$ MHz

ACTUAL WRITING RATES:

CLEAR: $U_{CLEAR} = 12$ MHz ($e_{CLEAR} = 0.77$)

COPs ?
VOPs $\Big\}$ $\Rightarrow$ 1 pixel / 2 update cycles

$\Rightarrow U_{COP} = U_{VOP} = 0.45$ MHz ($e = 0.03$)

$e_{avg} \approx 0.04$ (Weighting average by primitive frequency)

VS100 (CAN ONLY READ/WRITE 16 BITS / MEMORY CYCLE)

AOPs: CLEAR $= 20$ MHz ($e = 0.19$)
WINDOW $= 10$ MHz ($e = 0.10$)

COPs: 50 μsec/char $= 0.9$ MHz ($e = 0.009$)

VOPs: 2 μsec/pixel $= 0.5$ MHz ($e = 0.005$)

$e_{avg} \approx 0.015$

TYPICAL FLIGHT SIMULATOR

$e_{avg} > 0.9$

SHOWCASE GOALS

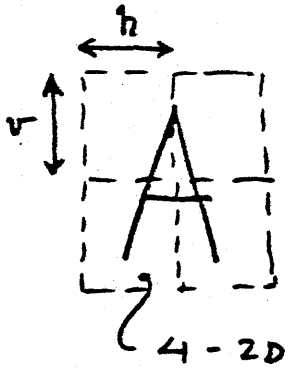
$\Big\{$
$e_{CLEAR} \approx 1$
$e_{WINDOW} \approx 0.45$
$e_{COP} \approx 0.25$
$e_{VOP} \approx 0.08$
$e_{avg} > 0.2$

BITMAP DISPLAY ARCHITECTURE EVOLUTION

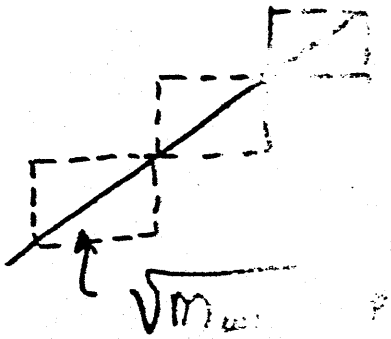
GENERATION		EXAMPLE	POTENTIAL e
MEMORY	0.	FRAME BUFFER (QUSS)	NO ATTEMPT TO USE U_{max}
(1×1)	1.	POINT GENERATOR VK100 / VT125	0.04
(h×1)	2.	REFRESH WORD RASTER OP (VS100)	0.05 ~ 0.09
(h×v)	3.	TWO DIMENSIONAL RASTER OP (SHOWCASE)	0.15 ~ 0.3

2D RASTER OP CONCEPT ($M_{WIDTH} = h \times v$)

- ABILITY TO WRITE 2D CHUNK OF COPs AND VOPs IN ONE MEMORY CYCLE



4 - 2D RASTER OPS VICE 10 - 2D RASTER OPS



$\sqrt{M_{WIDTH}}$ PIXELS / CYCLE VICE 1 PIXEL / CYCLE

The 8 by 8 Display

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December 1981

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- BASIC CONCEPTS:
  1. TWO-DIMENSIONAL RASTER OPS ("BLOCK")
  2. X-Y ADDRESSING BY ASSOCIATING COORDINATES WITH DRAM ROWS AND COLUMNS.

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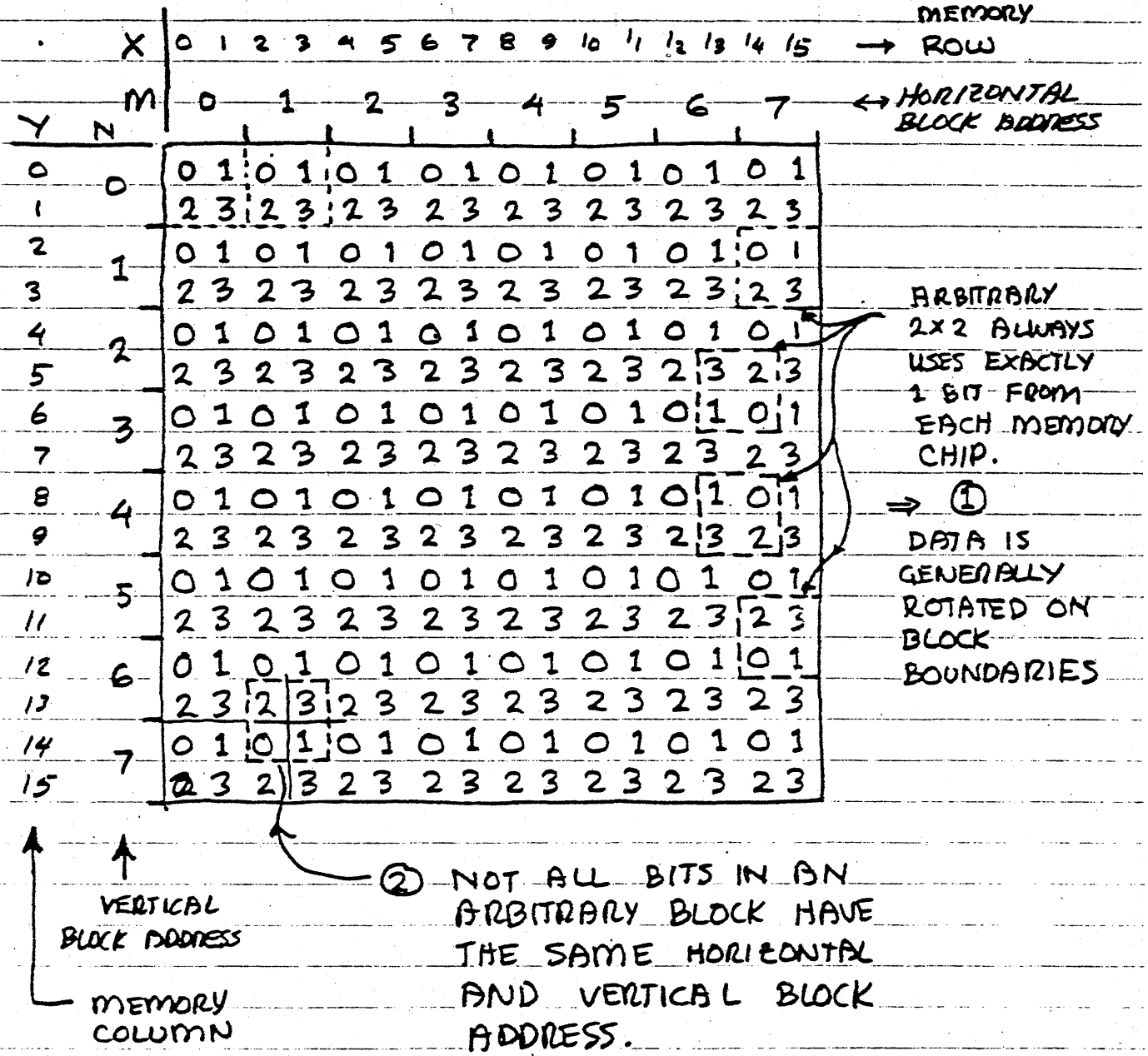
BIT ADDRESSING FOR A 2×2 MACHINE

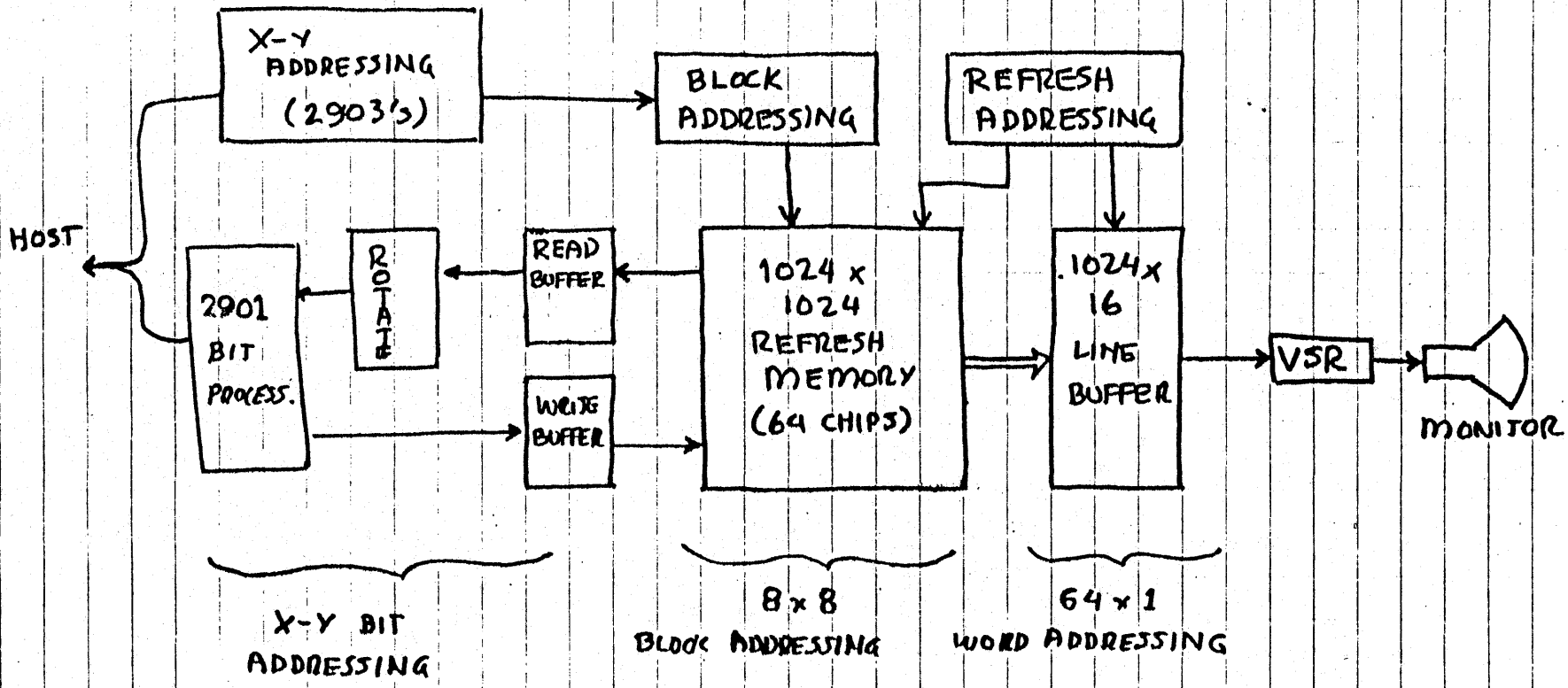
- NAME EACH MEMORY CHIP 0, 1, 2 AND 3 (1 CHIP PER PIXEL IN THE BLOCK)



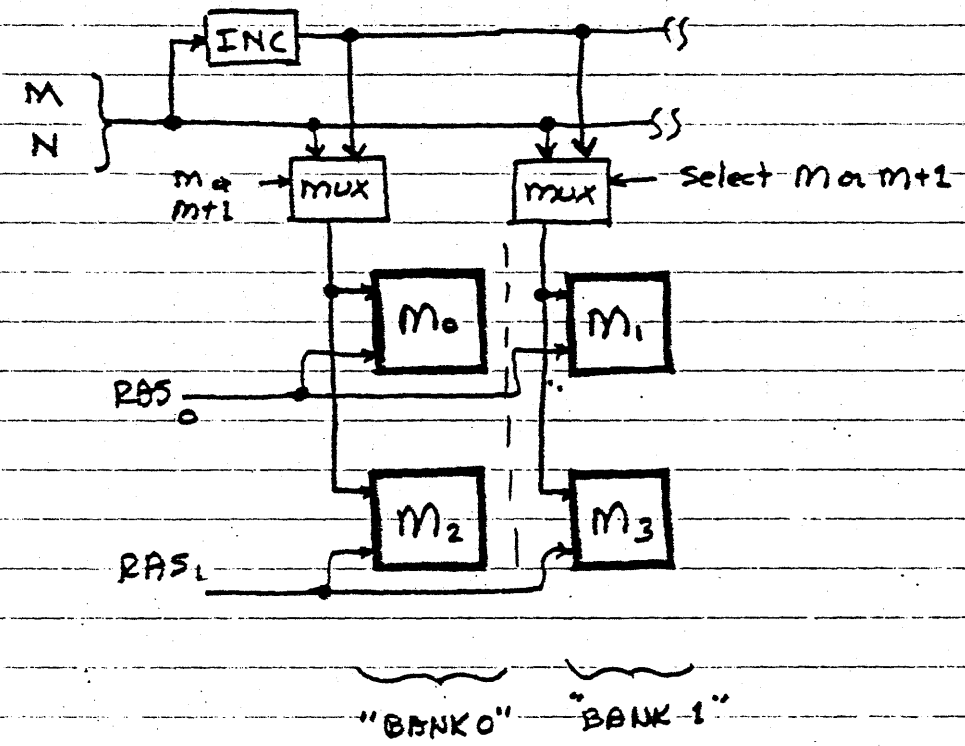
$M = X \text{ div } 2$; $i = X \bmod 2$

$N = Y \text{ div } 2$; $j = Y \bmod 2$

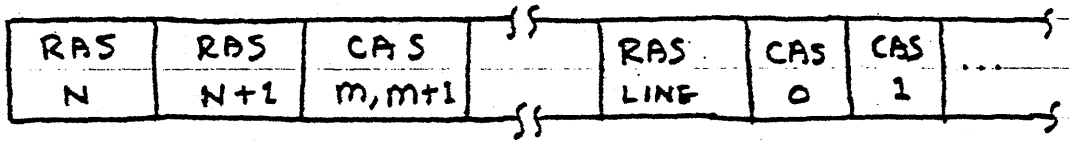
CMU 8×8 BLOCK DIAGRAM



MEMORY ADDRESS GENERATION AND CONNECTION



MEMORY CYCLE:



UPDATE READ/WRITE

PAGE MODE READ OUT INTO LINE BUFFER.

OTHER POINTS:

1. INVESTIGATED 64×1, 8×8 AND 1×64 CONFIGURATIONS. USED ONLY THE 8×8

   ⇒ CHOSEN FOR "SYMMETRY" REASONS

   ⇒ CONCEPT OF "ADDRESSING MODES"

2. CONCEPT OF "STAGGERED ADDRESSING" DISCARDED DUE TO COMPLEXITY

3. NEED FOR PARALLEL SET OF ROTATERS AND FUNCTION OPERATORS TO GET ULTIMATE POTENTIAL PERFORMANCE.

COMMENT: RESTRICTIONS ① AND ② ARE A RESULT OF IMPOSING THE X (ROW), Y (COLUMN) ADDRESSING SCHEME.

2DLBMC IMPLEMENTATION OF THE 8×8 CONCEPT

---

① USE LINEAR BIT MAP ADDRESSING

⇒ VAXstation COMPATIBILITY

⇒ PROGRAMABLE RESOLUTION

⇒ ARBITRARY BIT MAPS

⇒ NO OPPORTUNITY TO USE ROW/COLUMN ASSOCIATION

② MULTIPLE ADDRESSING MODES USING THE STAGGERED APPROACH } $h \times v$, $(h \cdot 2) \times (v/2)$, ⋮, $(h \cdot v) \times 1$

⇒ NO NEED FOR SEPARATE LINE BUFFER

⇒ ARBITRARY VERTICAL BUT FIXED HORIZONTAL BOUNDARIES

⇒ COST/PERFORMANCE OPTIMAL MULTI-PLANE (COLOR) CAPABILITY } $h \times v \times 1$ (planes), $h \times 1 \times v$

③ MEMORY COMPONENTS

⇒ CAN USE ANY TYPE OR SIZE INCLUDING VRAM

⇒ SELF REFRESH CAPABILITY

⇒ PROGRAMMABLE DUTY CYCLES:

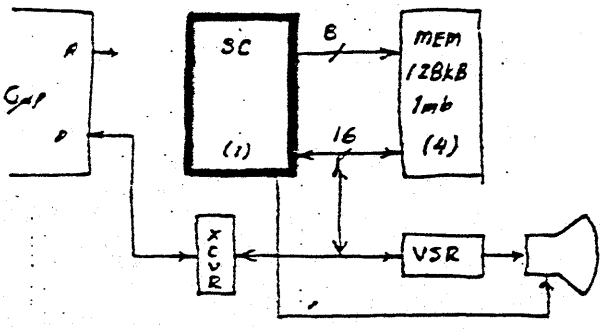
RESOLUTION vs. UPDATE SPEED

& # PLANES vs. UPDATE SPEED

⇒ DON'T NEED INDIVIDUAL CHIP RAS CONTROL

Ⓓ SC16×1 / 40 PINS — DAL w/ SEPARATE XCVR — { 16×1 → 800×640

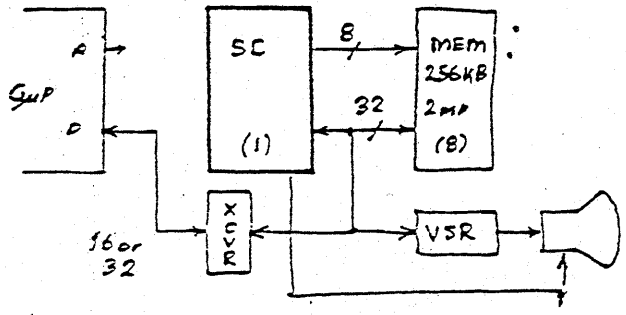
PREFERRED LOW COST CONFIGURATION



Same displays as Configuration Ⓒ BUT WITH Half-speed GμP Interface.

≈ 20 Mbits

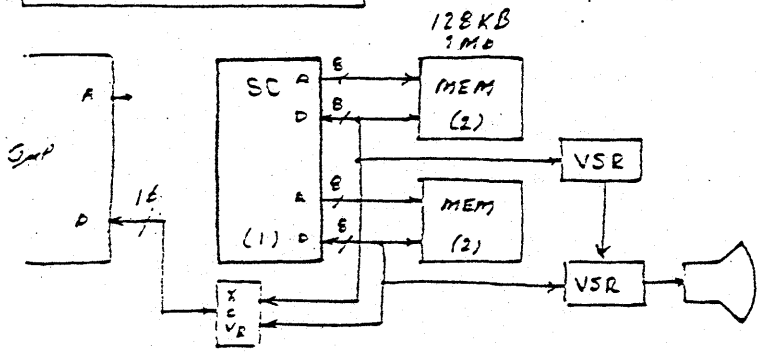
Ⓕ SC32×1 / 56 PINS — DAL w/ SEPARATE XCVR



MEM	R BW	60 Hz M-pixels	30 Hz M-pixels
150 ns	106.6	1.33	2.66
200 ns	80.0	1.0	2.0
250 ns	64.0	0.8	1.6

maximum GμP rate:
≈ 20 Mixels (16 bit)
≈ 40 Mixels (32 bit)

Ⓖ SC8×2 / 56 PINS — DAL w/ XCVR

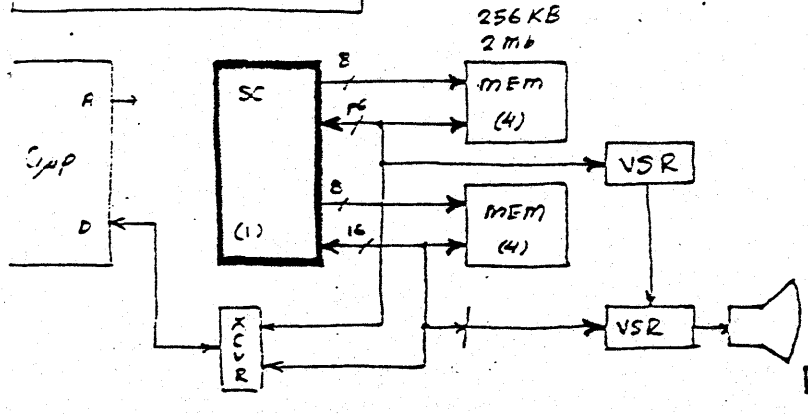


Same displays as configurations Ⓒ, Ⓓ & Ⓔ for single plane plus 2-plane capability for displays in configurations Ⓐ, Ⓑ

GμP Interface same performance as Ⓓ

"OPEN" HIGHER COMPLEXITY CHIP

Ⓗ SC 16×2 / 64 PINS — { 16×2 → 1088×864



Single plane display formats same as configurations Ⓕ.

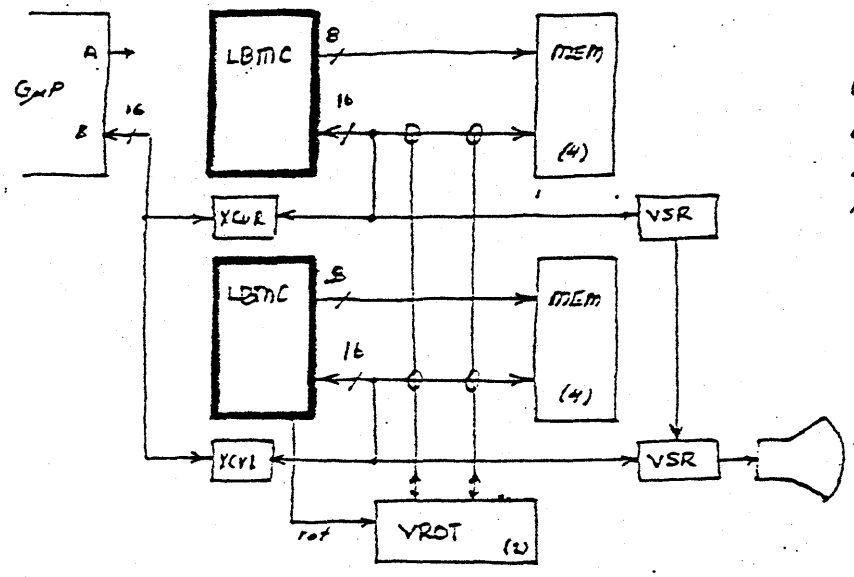
2-plane formats same as configurations Ⓒ, Ⓓ, & Ⓔ

GμP Interfaces same as configurations Ⓕ.

MULTIPLE CHIP LBMC CONFIGURATIONS :

C.M.M.
10/23/83

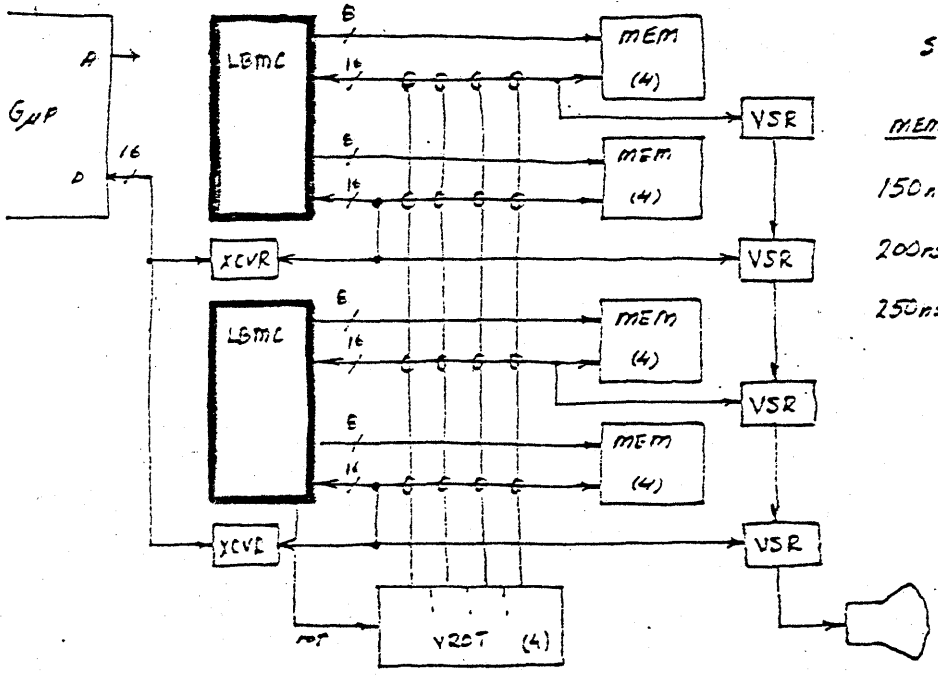
MULTI-D | MC 16 x h / 40 PINS EACH | { 16 x 2 ⇒ 1088 x 864



Characteristics same as configuration H, but more chips, not necessarily greater cost.

MULTI-H | MC 16 x 2h / 64 PINS EACH | { 16 x 4 ⇒ 1600 x 1280

4-PLANE SYSTEM IS SAME AS CONFIGURATIONS ©, Ⓔ, Ⓔ



SINGLE PLANE SYSTEM :

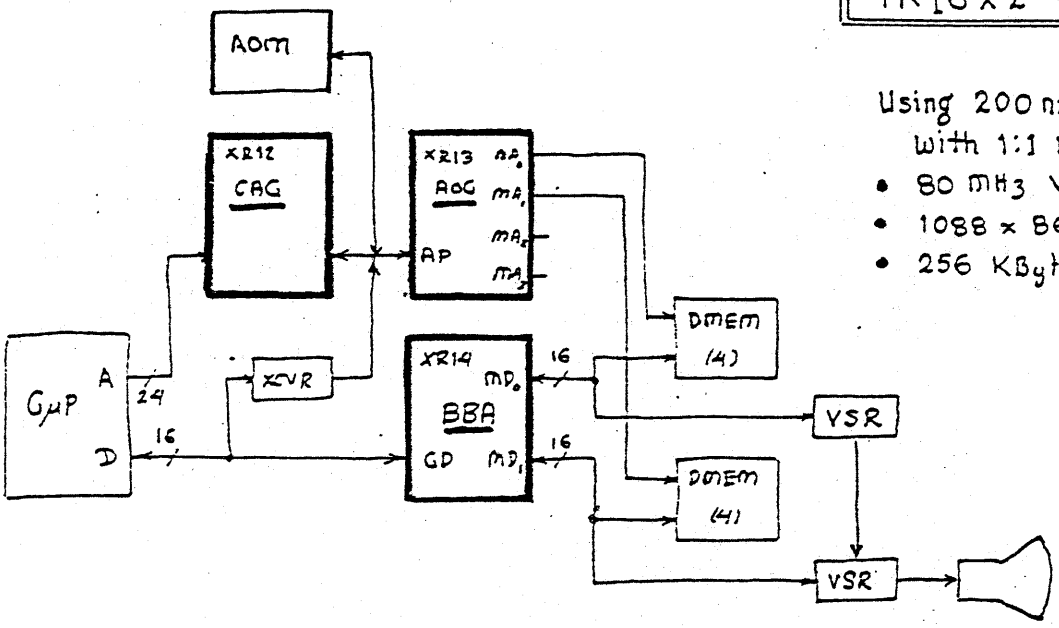
MEM	BW	60 Hz PIXELS	30 Hz PIXELS
150ns	213.2	2.67	5.34
200ns	160.0	2.0	4.00
250ns	128.0	1.6	3.2

COST EXAMPLE FOR CONFIGURATION H :

COST 64K x 4	ALLOWED COST FOR (LBMC + VROT)
$50	$120
$25	$60
$10	$12

4K16X2 SHOWCASE

Using 200 nsec Memory:
with 1:1 DC ⇒
- 80 MHz Video
- 1088 x 864 Screen Format (60 Hz)
- 256 KByte Memory (2 screens)



4K16X8 SHOWCASE

B&W • 1:3 DC (Superscroll)
- 160 MHz Video
- 1600 x 1100 screen

Color • 1:1 DC
- 8 PLANES
- 40 MHz
- 960 x 800