PVN PROPOSAL WRKSYS

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digital

For Internal Use Only

Semiconductor Engineering Group

PRESENTED TO STAFF @ PTC 2/20/91

Introduction

- Look into TTM focused PVN
- Use NVAX+ in PMariah platform
- NVAX chip can't be used because ~~it~~ NVAX requires a writeback Bcache
- Minimal changes to PMariah platform
- FRS gated by NVAX+ availability
- Performance goal - 16 to 18 VUPs
- AFL has design team available now

Technical Issues

- 3.3V Power
  - 5.6A avail. which can go to 6.6A
  - Reserving 1.5A for ScanPROC, leaves 5.1A which supports 11ns NVAX+ cycle time
- Cooling
  - Class B environment and 200 lfm supports 11ns NVAX+ at Tj = 85C
- Functionality
  - NVAX+ 128 bit data bus requires 16 cache rams
  - Cache size can be 128k, 256k, or 512k
  - Backmap logic needs one more address bit to support 512K cache
- Performance
  - Very sensitive to Memory bandwidth

ELIMINATED DUE TO COMMENT

PVN Performance Data

PM runs with various options, all numbers are in VUPs.

14ns CPU, 2.5X MCLKA, 16 QW write buffer, 512KB cache,

MCLKA	35ns	35ns	42ns
Write cycles	8.0	9.5	9.5
MAIL	17.7	17.2	15.6
NFORT	18.4	16.9	14.7
NLINKU	19.5	17.8	15.4
RUNOFF	14.7	13.2	11.4
SORT	21.5	21.0	19.0
GEO. MEAN	18.2	17.0	15.0

14ns CPU, 2.5X MCLKA(35ns), 16 QW wr buff, 256KB cache, 9.5 cycle writes

	256KB cache	st 1st QW(512KB)
MAIL	15.9	17.5
NFORT	15.8	17.2
NLINKU	17.3	18.2
RUNOFF	11.6	13.3
SORT	20.3	21.4
GEO. MEAN	15.9	17.3

12ns CPU, 3X CLKA(36ns), 16 QW wr buff, 512KB cache, 9.5 cycle writes

MAIL	18.2
NFORT	17.2
NLINKU	18.0
RUNOFF	13.3
SORT	22.3
GEO. MEAN	17.6

PMariah/PVN Performance Comparison

Geometric mean of performance running Uhler 5, all numbers are in VUPs.

System	Cycle time	MCLKA	System Performance 256KB	512KB
PMariah	20ns	40ns	10.8	-
PMariah	18ns	36ns	* 11.9	-
PMariah	16ns	32ns	* 13.2	-
PVN	16ns	32ns	15.7?	
PVN	15ns	30ns	16.8?	
PVN	14ns	35ns	15.9	17.0
PVN	13ns	32.5ns	* 17.0	* 18.2
PVN	12ns	30ns	* 18.3	* 19.6
PVN	12ns	36ns	* 16.5	17.6

ONE OF THESE

* extrapolated performance

SYSTEM MODULE CHANGES

- Redesign system etch board
- Redesign MARR Gate Array (20K used gates)
- Replace 3 Mariah Chips with 1 NVAX+
- Double number of Bcache chips
- Increase 3.3V current (resistor change)
- Replace 4 MSI parts with 2 PALS
- New Components
  - 32Kx9 20ns cache data rams (speed qual)
  - 16Kx4 15ns cache tag rams (qualified)
  - 286MHz oscillator (being qual'd for NVAX)

MAR chip changes

- Use MAR for design base, but this is a new design
- Support for NVAX+ DAL/Cache protocol
- Fewer commands to support(no CWB, no Read Interrupt Vector)
- Increase Write buffer size
- Maintain most of CDAL control
- 2 times gate count(data path changes)
- Larger package (need 330 pins)

Airflow

12-FEB-1991
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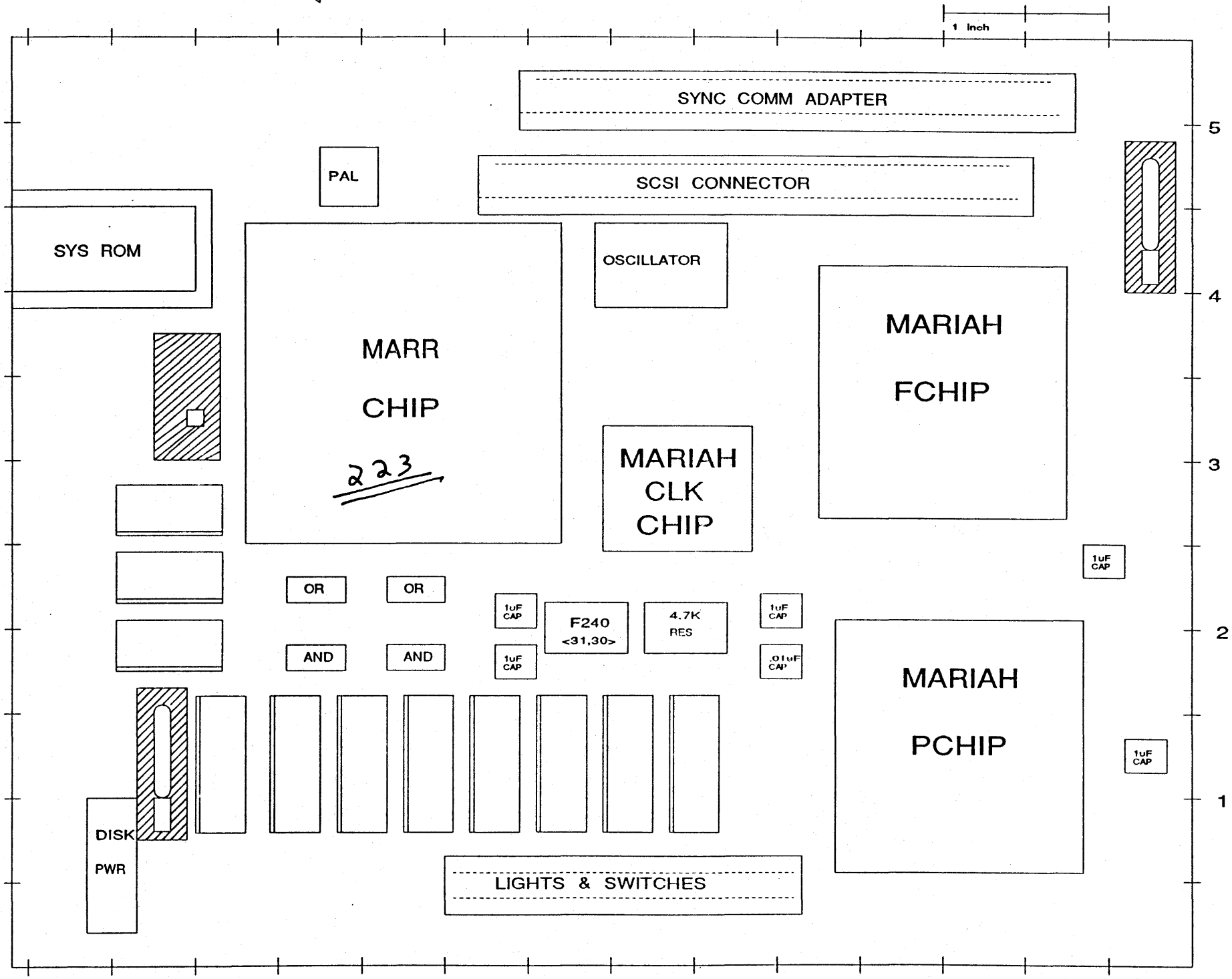

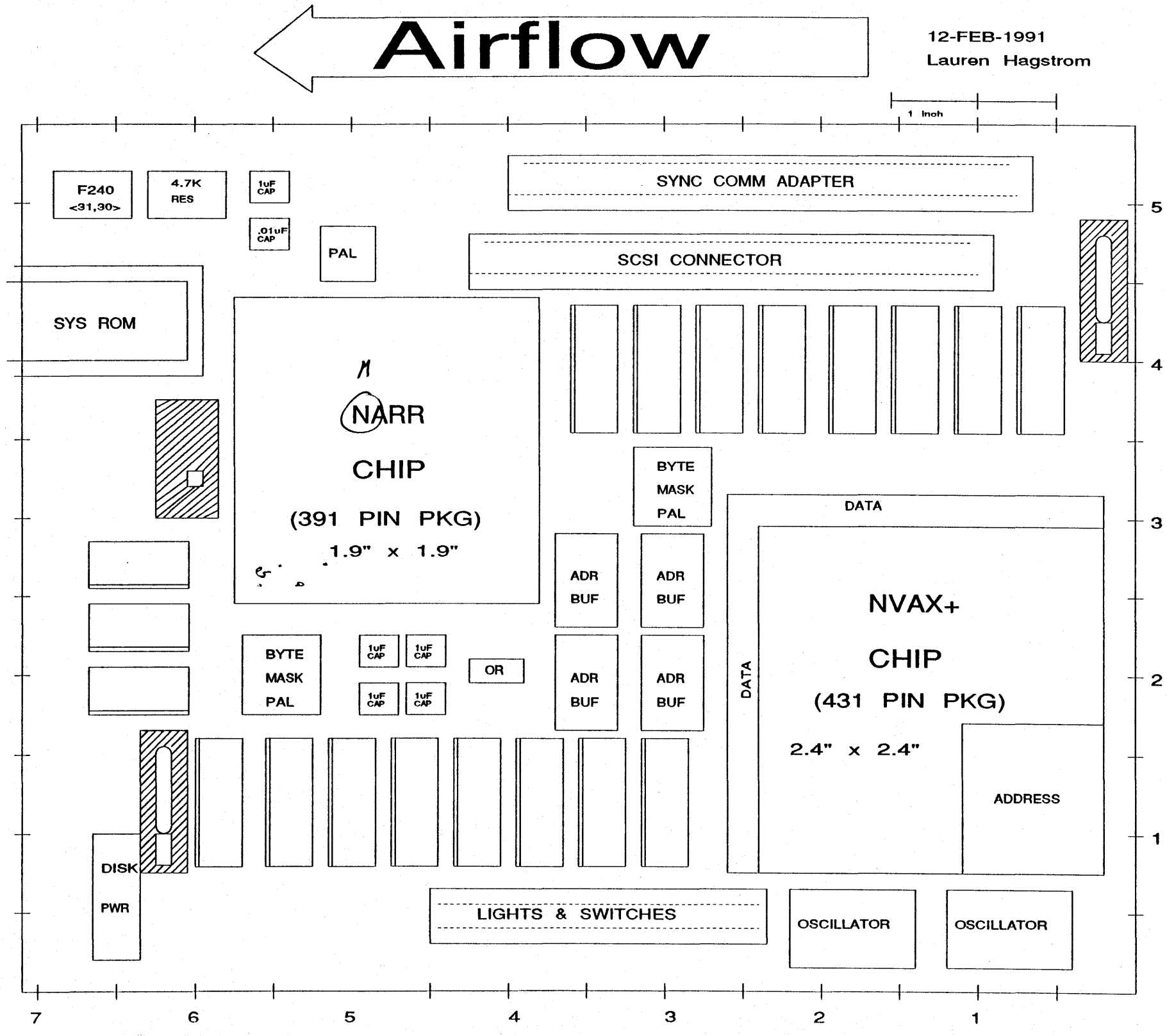
Airflow
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1 inch
F240
<31,30>
4.7K
RES
1uF
CAP
.01uF
CAP
PAL
SYNC COMM ADAPTER
SCSI CONNECTOR
SYS ROM
NARR
CHIP
(391 PIN PKG)
1.9" x 1.9"
BYTE
MASK
PAL
ADR
BUF
ADR
BUF
DATA
NVAX+
CHIP
(431 PIN PKG)
2.4" x 2.4"
DATA
ADDRESS
BYTE
MASK
PAL
1uF
CAP
1uF
CAP
1uF
CAP
1uF
CAP
OR
ADR
BUF
ADR
BUF
DISK
PWR
LIGHTS & SWITCHES
OSCILLATOR
OSCILLATOR
1
2
3
4
5
6
7

PROJECT SCHEDULE

Start Date	- 3/1/91
NVAX Plus PG	- 5/30/91
NARR 2nd sign off	- 7/30/91
Pass 1 NVAX+ avail	- 9/1/91
Pass 1 power on	- 9/1/91
Start DVT/Qual	- 11/1/91
Pass 2 NVAX+ avail	- 1/15/92
Start Field test	- 2/15/92
* CMOS4 Process Qual	- 6/30/92
* FRS	- 6/30/92

* Might be able to pull in to 5/30/92

RESOURCES

NARR chip	- 3 engineers (avail now)
System board	- 1 eng, 1 tech (avail now)
Simulation	- 2 engineers (1 avail now)
VMS	- 1 engineer
Console SW	- wrksys group
Diagnostics	- wrksys group

TRANSFER COST DELTAS

OPPORTUNITY WITH CACHE G/A PACKAGE

	PMariah FY92			PVN FY93		
	Qty	cost	total	Qty	cost	total
CPU CHIP SET	1	380.00	380.00	1	500.00?	500.00?
MARR vs NARR CHIP	1	161.87	161.87	1	300.00?	300.00?
32KX9 SRAM 20NS	8	13.98	111.84	16	12.00	192.00
64K/16KX4 SRAM 15NS	6	13.98	83.88	6	3.50	21.00
OSCILLATOR 220 vs 286MHZ	1	19.00	19.00	1	65.00	65.00
OSCILLATOR, CRYS 16MHz	0	1.00	0.00	1	1.00	1.00
Total Cost			756.59			1079.00
Cost Delta						322.41

Additional MSI parts:

2 4.5ns PALS replace 2 74F32s and 2 74F08s
4 240 BUFFERS for address fanout
1 74F08(OR) for TagOE control

TOTAL XFER COST DELTA FOR AVIO SYSTEM ~ 10%

ISSUES

- Find 33x pin pkg for NARR chip
- Lower transfer cost delta
- Using 70% mem BW for CPU
- Forecast WRKSYS NVAX+ needs to SCMT
- Prioritize NVAX+
- Other enhancements
  - Minor change to S-chip for higher performance
  - Replace 5 MSI chips($25) with a $7 gate array

Recommendation

- Design PVN with 14ns NVAX+, 256KB cache - 16VUPs
- Offers 50% perf improvement, 1 yr after PMariah
- AFL design team can start now
- Very low risk approach - simple change to 1 gate array
- FRS - 6/30/92 - gated by CMOS4 qual in SQF
- Faster NVAX+ and larger cache allow up to 20VUPs
- PVN Linpak performance is ?x PMariah