EK-OTK50-TM-001

TK50 Tape Drive Subsystem

Technical Manual

digital™

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TK50 Tape Drive Subsystem

Technical Manual

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of
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CHAPTER 1
INTRODUCTION AND SPECIFICATIONS

1.1 GENERAL

The TK50 Tape Drive Subsystem is a mass storage device. It uses removable 94.5M byte tape cartridges to provide backup storage capacity and a software distribution capability for Digital's low-end computer systems.

The subsystem consists of three components: the TK50 Tape Drive, the TK50 Tape Drive Controller, and an interface cable that connects the tape drive to the controller. The TK50 Subsystem may reside entirely within the system unit of a MicroPDP-11 or MicroVAX (I or II); or it can be set up as an external add-on peripheral that can be plugged into other systems, including the PDP/11-23+. The drive unit and the controller are the only field replaceable units (FRUs) in the subsystem.

Future updates of this manual will describe controllers used with buses other than the Q-bus. This version contains information on the TK50 Tape Drive and the TQK50 controller (M7546).

This manual does not contain installation or remove/replace procedures for the two FRUs. Since the TK50 fits a 5-1/4 inch footprint and is power-plug compatible with the RX and RD50 series disk drives, it may reside in a variety of different systems. It may replace the RX50 in certain configurations.

Refer to the appropriate system documentation for installation and FRU remove/replace procedures. For example, if you are troubleshooting a TK50 subsystem problem when the TK50 is in a MicroPDP-11 computer, refer to your Micro-11 Pocket Service Guide.

NOTE

See Chapter 4 for detailed information about the TK50 Subsystem controller(s). See Chapters 2 and 3 for detailed information about the TK50 streaming tape drive.

The storage medium is a tape cartridge containing a magnetic tape that is 1/2 inch wide and 600 feet long. The tape cartridge is about 4 by 4 inches square, and is labeled CompacTape.

1.2 TK50 TAPE DRIVE UNIT SPECIFICATIONS

Tape speed	75 inches per second (in/s)
Bit density	6667 bits per inch (bits/s)
Data rate	500 Kbits/second; 45 Kbytes/second
Number of tracks	22
Media type	Single reel, 1/2 inch, 600 feet long
Capacity	131 megabytes unformatted, 94.5 megabytes formatted
Read/write gap spacing	0.3 inches
Recording method	MFM, bit serial data, serpentine recording
Power required	+5 Vdc, 1.2 amps (typ), 1.4 amps (max) +12 Vdc, 2.0 amps (typ), 2.4 amps (max)

1.3 DRIVE TO CONTROLLER INTERFACE SPECIFICATIONS

Interface type	Differential using RS-422 drivers and receivers
Connector type	26-pin flat ribbon, polarized; right angle header; PN 12-16832-02
Cable type	26-wire flat ribbon; PN 17-00034-02; max length 10 ft
Receiver type	AM 26LS32, differential
Driver type	AM 26LS31, differential

Table 1-1 TK50 Related Documentation

Title	Order Number	Contents
TK50-D, -R Tape Drive Subsystem Owner's Manual	EK-LEP05-OM	Provides installation, service, use, and programming information for the desktop and rack-mounted versions of the TK50.
TK50 Tape Drive Subsystem User's Guide	EK-OTK50-UG	Provides information on using the TK50 Tape Drive. Written for operators and secretaries with little or no technical background.
TK50 Tape Drive Subsystem Illustrated Parts Breakdown (IPB)	EK-OTK50-IP	Provides an exploded view drawing of the TK50 Tape Drive Subsystem and a comprehensive parts list.
TK50 Tape Drive Subsystem Field Service Print Set	MP-2054 (Drive unit) MP-2055 (M7546 module)	The complete set of prints needed to troubleshoot the TK50 Tape Drive Subsystem to the component level.

CHAPTER 2
DRIVE UNIT
THEORY OF OPERATION

2.1 GENERAL

This chapter provides theory of operation information about the TK50 Tape Drive. The controller(s) to which the drive connects is discussed in succeeding chapters.

Use the block diagrams and mechanical drawings referenced to help you understand the text. For troubleshooting, the Field Service Print Set takes precedence over any block diagrams or mechanical drawings in this book.

This chapter describes how the various components in the TK50 Drive Unit interact during operation. Following the overview theory is more specific information including signal definition and timing, command summary and explanation, and a discussion of the basic drive/controller communications protocol.

Chapter 3 provides the information necessary to remove and replace a subassembly that failed in the drive.

2.2 UNIT DESIGNATIONS

This section lists and describes the unit variations in which the TK50 Tape Drive Subsystem is available.

2.2.1 Drive Unit Variations

TK50	Plain drive, ordered with no system.
TK50-AA	Single unit in packaging with tape cartridge.
TK50-AX	Single unit in packaging, no tape cartridge.
TK50-D	Desktop version of TK50 -- external drive version.
TK50-R	Rackmount version of TK50 -- external drive version.

2.2.2 M7546 Controller

TQK50-AB — This variation is the controller and cable for a BA23 enclosure and an external TK50-D, -R drive, and accommodates the MSCP Q-bus. One controller handles one TK50 drive.

Use this kit when configuring a MicroPDP-11 or MicroVAX system in a BA23 enclosure.

TQK50-PB — This kit is the same as the one above, except that the controller cable accommodates a PDP-11/23+ system.

Use this kit when configuring a PDP-11/23+.

17-00484-01 — This 2.75 meter (9 foot) host-to-external-drive interface cable is a 50-pin subminiature male to a 50-pin "D" subminiature female shielded, molded cable. This cable comes with the TK50-D, TK50-R subsystem.

TQK50-AA — Controller and cable in BA23 cabinet, 30 inch cable with BA23 specific access door.

TQK50-BA — Controller in BA123 cabinet, 30 inch cable.

TQK50-BB — Controller in BA123 and external drive, 21 inch cable with I/O panel insert.

TQK50-CB — Controller in cabinet mount BA23 with H3490 I/O panel and external drive. Also, 36 inch cable with I/O panel insert.

TQK50-RB — Controller in non-FCC compliant Q-bus enclosure with no I/O panel, 120 inch cable with bracket to mount I/O panel insert on cabinet rails. For Field upgrade only.

The TK50 Tape Drive Subsystem must always be ordered in two separate pieces: the drive unit itself and, separately, the controller. For example, if customers own a MicroVAX I system (BA23 enclosure) and want to add an external TK50 Subsystem, they would order the following parts.

1. TK50-D -- Desktop, external version of drive
2. 17-00484-01 -- External drive-to-system cable.
3. TQK50-AB -- Controller and internal cable.

2.3 CABLING

In the system-integrated version of the TK50 (Figure 2-1), the drive is connected to the controller via a 26-pin flat ribbon cable. When the TK50 is in a tabletop or rackmount enclosure, the configuration includes an FCC shielded cable that connects the separate enclosure to the host system (Figure 2-2).

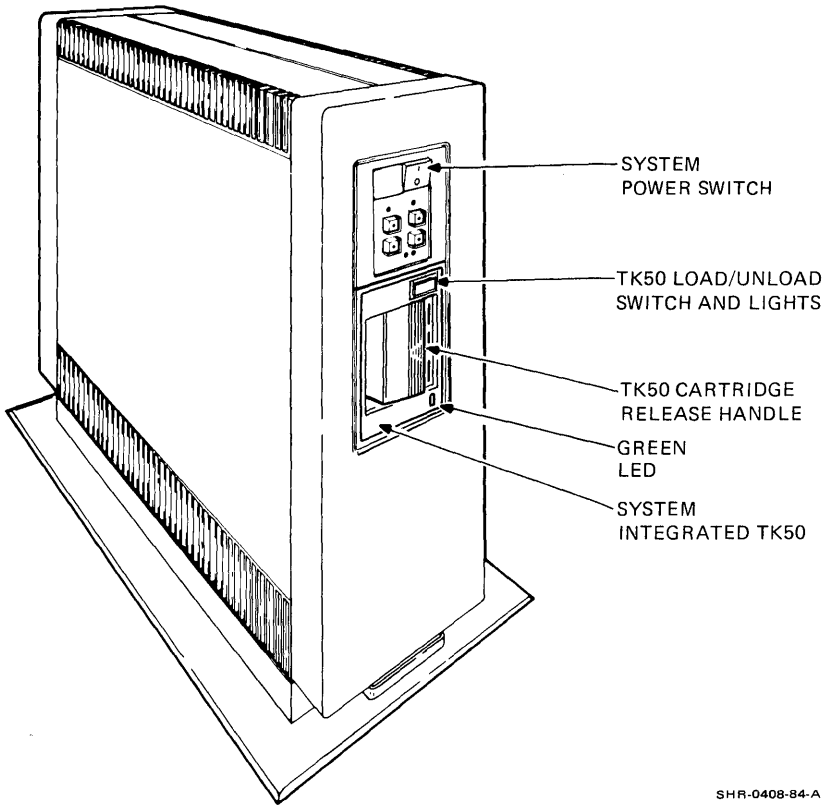


Figure 2-1 System Integrated TK50

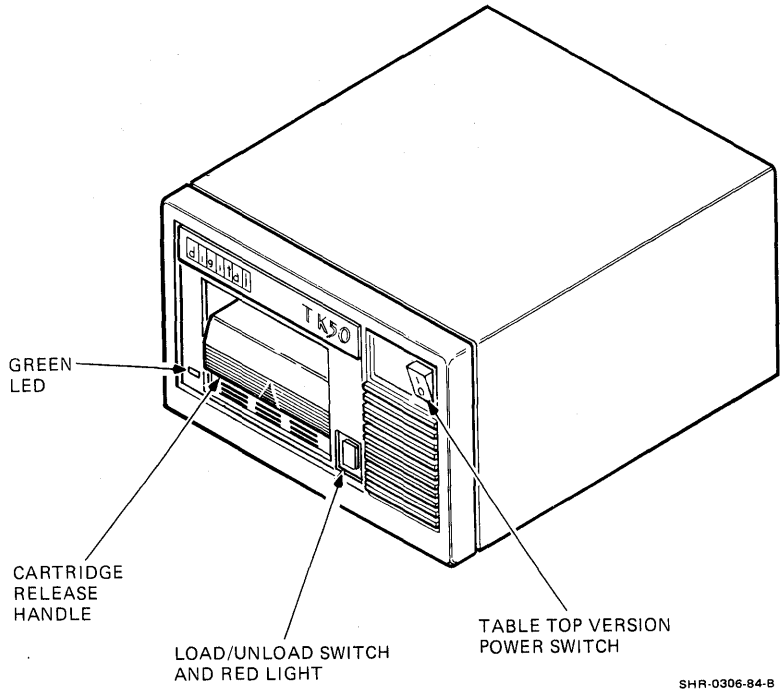


Figure 2-2 Desktop TK50

The signal lines on these cables provide serial commands and data sent from the controller to the drive, via differential lines. The drive recognizes the commands and data by interpreting the differences in voltages on the lines. The differential method provides good noise isolation. See Table 2-2 and Sections 2.16 and 2.17 for signal definition, connector pin-outs, and timing diagrams.

2.4 POWER

The TK50 has no internal power supply. The host system must provide the TK50's required voltages, which are: +12 Vdc at about 2 amps and +5 Vdc at about 1 amp. The power connector is the same as the RX and RD50 series floppy diskette drives. The drive uses a 4-pin power plug (PN 12-18855-00), located at J7 on the drive board, to accept power provided by the host system. If an external TK50-D, or -R drive is used, the ac power source should be the same as that used for the host computer.

2.5 PHYSICAL DESCRIPTION

The TK50 drive unit consists of two major components: the tape transport and a printed circuit board attached to the bottom of the drive. These two assemblies together are one FRU. The controller that resides in the system backplane is the other FRU.

2.5.1 Drive Board

The drive board is connected to the bottom of the drive and has discrete analog and digital components.

This module includes an 8751 microprocessor that interprets commands, runs on-board diagnostics, and controls the entire drive operation. The write and read circuits necessary to translate data to and from the MFM format reside on this board. Also included is an 8155 I/O and RAM chip used to sense various conditions, including Beginning of Tape/End of Tape (BOT/EOT), Handle Switch Open/Closed, and Load/Unload Switch Open/Closed. The circuits on this board are detailed as they apply to a specific operation. Figure 2-3 is a simplified block diagram of the entire drive, including the drive board.

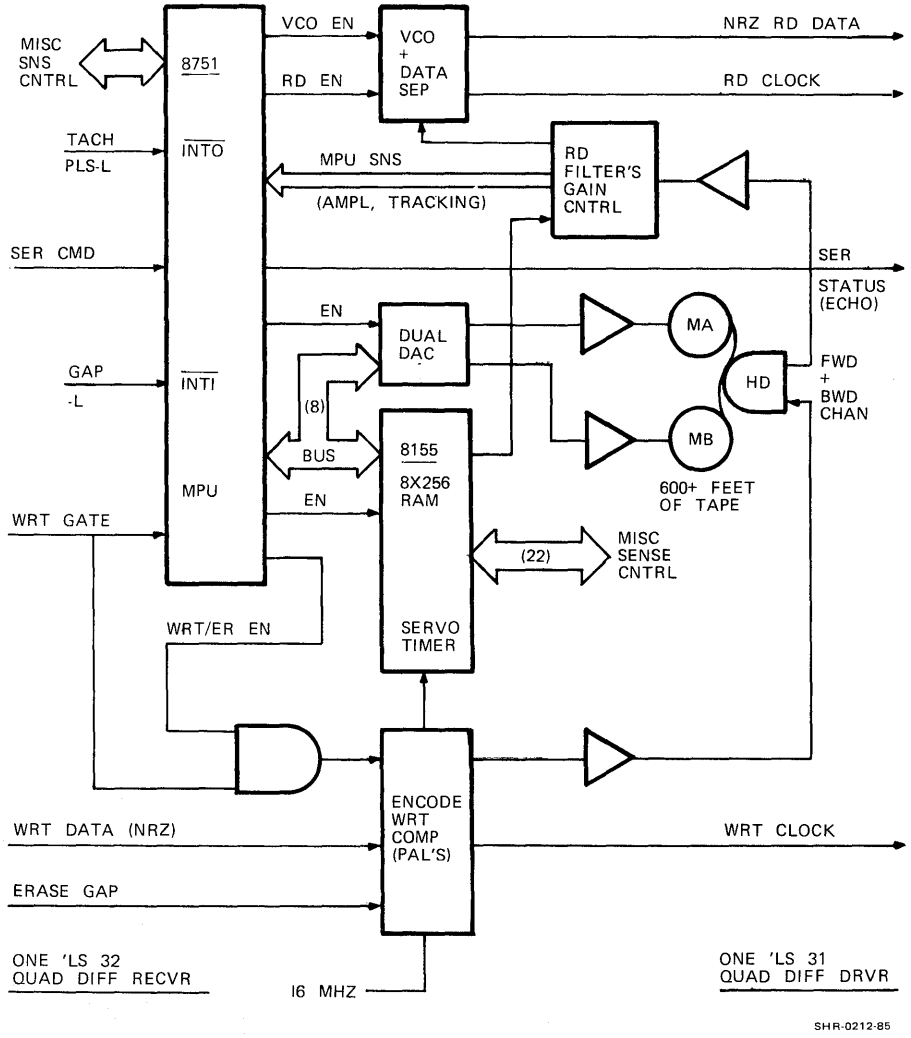


Figure 2-3 Block Diagram: Drive Board

2.5.2 Tape Transport (Figure 2-4)

The tape drive transport encompasses the mechanical and electromechanical components that allow the TK50 to perform its functions; that is, to read and write data to magnetic tape. These components include: the magnetic read/write head and its stepper motor; the take-up reel and its motor; the tape hub (which serves, effectively, as the supply reel when a tape cartridge is inserted) and its reel motor; and the tachometer, which provides feedback to the 8751 microprocessor regarding tape speed.

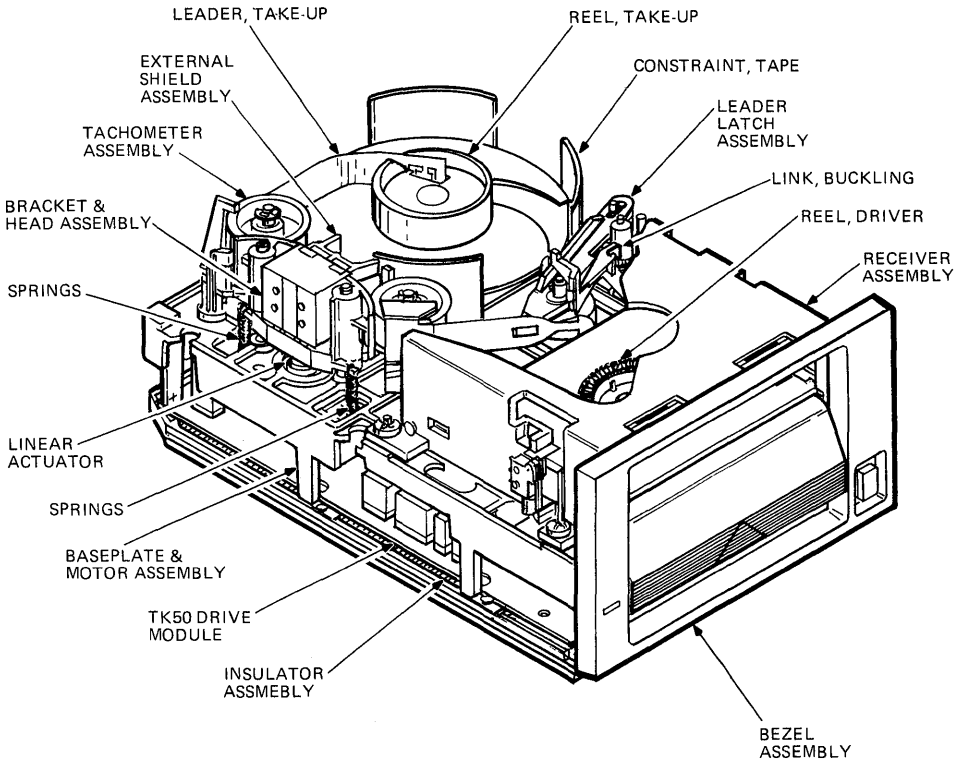


Figure 2-4 TK50 Tape Drive Transport

2.6 CONTROLS AND INDICATORS

On the front of the TK50 Drive is a combination Load/Unload switch and LED indicator (Figure 2-5). When power is applied and a tape cartridge is in place, the Load/Unload switch is used to load the tape for operation. Loading the tape involves coupling two leaders together (one is on the beginning of the tape and the other is part of the drive), then bringing the tape to the Beginning of Tape (BOT) indicator. Unloading the tape involves rewinding to BOT, then unbuckling the two leaders so the tape can seat in the cartridge for removal.

Also on the front of the drive is the cartridge release lever or handle. This handle must be raised to insert or remove a tape cartridge, and lowered to lock the cartridge in place. The handle must never be raised when the light is on or blinking, or when the system power is off.

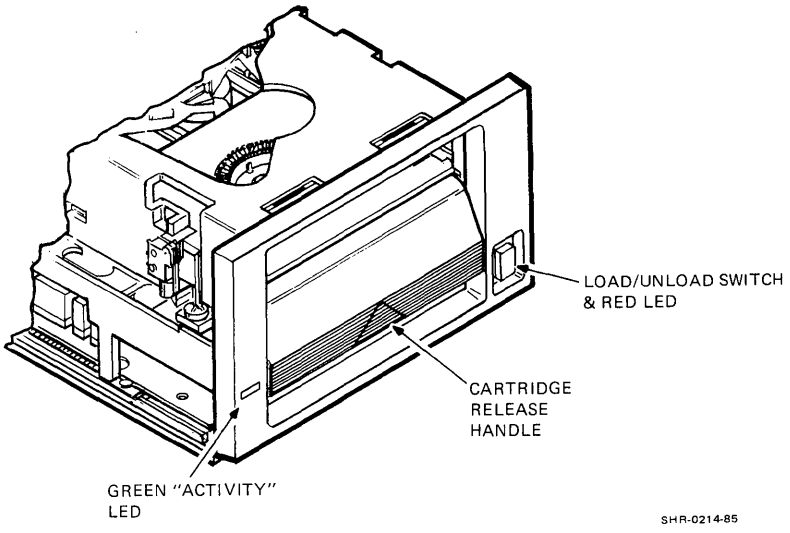


Figure 2-5 TK50 Front View

2.6.1 Load Procedures

1. When power is turned on and no cartridge is in the drive, the red light goes on steady during initialization (about two seconds). Then the red light goes off and the green light comes on.

2. With the red light off and the green light on, lift the handle.

3. Insert the cartridge. As soon as the cartridge is within about 1/2 inch of being fully inserted, the solenoid clicks, the red light goes on steady, and the cartridge locks in place. The green light is off.

4. Lower the handle so the reel drive engages the tape cartridge hub. The red light goes off, and the green light goes on. You may lift the handle and remove the cartridge now, if desired.

5. Press the switch to the in position. The red light goes on and the green goes off.

6. Tape loads to BOT (beginning of tape). When the tape is successfully loaded and waiting at BOT, the green light is on steady. During the time the drive is responding to a command to read or write, including the time to seek the correct part of the tape, the green light is blinking.

2.6.2 Unload Procedures

1. Red light is on. Press the switch to the out position.

2. Red light and green light both blink (slowly, but not together) as the tape is being rewound to BOT. This rewind operation can also be initiated from software. The lights blink in either case.

3. Red light stays on and green light goes off as the tape continues rewinding to the unload position.

4. When the tape is completely rewound into the cartridge, the red light goes off. Then the green light comes on.

5. Raise the handle. The cartridge comes out far enough to easily grasp and remove it.

6. Lower the handle. The green light is still on to show that there is power to the drive.

NOTE

Do not power down the TK50 when the tape cartridge is still in the drive. Always remove the cartridge before powering down.

2.6.3 Lights

Table 2-1 describes the state of the lights.

Table 2-1 States of Lights

Red	Green	Conditions
Off	Off	No power to the drive.
Off	On	The handle can be lifted.
On	Off	Do NOT lift the handle: -- Self-test (initialization) is running -- Cartridge is inserted but handle is still up -- Tape is loading or unloading -- Tape is stopped.
On	On	Tape loaded successfully (at BOT, no controller command yet).
On	Flashing	Tape motion (except rewind) -- Read/Write commands are being processed. Irregular, fast blinking means calibration is occurring.
Flashing	Flashing	Tape is being rewound.
Fast flash	Off	Fault.

In summary, when both lights are off, there is no power to the drive. When one or both lights are on, the red light indicates handle and fault conditions.

- Red light on steady always means the handle may NOT be lifted.
- Red light off steady means the handle MAY be lifted to insert or remove a cartridge.
- Red light flashing fast always means a fault condition; the handle may NOT be lifted. Double toggling the switch clears the fault.
- Blinking light means rewind is occurring (and the handle can soon be lifted).

The green light indicates tape and power conditions.

- Green light on steady means two things.

  1. Power is on and the handle may be lifted to insert or remove a cartridge (if red light is off).

  2. Tape has loaded properly (if red light is on).

- Green light off steady means the tape is not being used (it is stopped, initialization is occurring, tape is loading or unloading, or fault).

- Green light blinking always means that tape is in motion.

  1. Calibration is occurring.
  2. Read/write activities are being performed.
  3. The tape is rewinding to BOT.

2.7 DRIVE BOARD DESCRIPTION

Refer to the drive board schematics in the TK50's Field Service Print Set (MP-2054-CS) while reading this section.

In the following logic description, the component being described is followed in parentheses by the circuit schematic sheet number and location zone. For example, E13 (1-B8) is in Field Maintenance Print Set MP-2054, Circuit Schematic (CS) sheet 1, location zone B8.

2.7.1 Write Data Chain

Write data comes into the drive's logic board via the differential signal cable on 26-pin connector J1 (PN 12-16832-01) (see Figure 2-6). It connects to pins one and two of the differential receiver at E13 (1-B8). The shift register at E4 (to which the output of the differential receiver is connected) accepts serial data and outputs a five-bit parallel data pattern into the Programmable Array Logic (PAL) at E9 (1-B5). The data is clocked through the shift register by the 500 KHz clock. The 500 KHz clock is divided down by the PAL from the 24.0 MHz crystal oscillator. The 500 KHz clock is the write pulse rate, or write data rate. The M7546 controller that is in the host computer accepts this clock also, and must keep up with it.

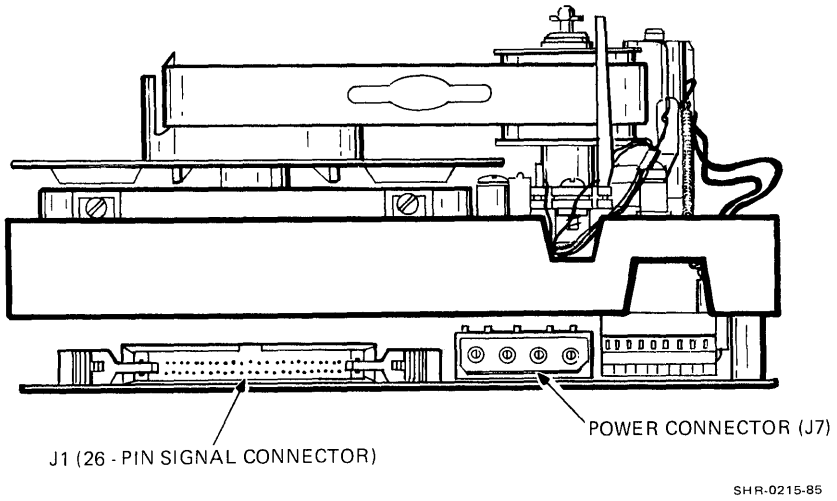


Figure 2-6 TK50 Rear View

The PAL at E9 accepts the five parallel bits from the shift register at E4 (1-B6), and from those bits generates WR PLS L. This PAL performs the precompensation and encoding needed to translate data to MFM format.

The signal WR PLS L is connected to pin 3 of the 74S74 flip-flop at E19 (2-D4), which is set up as a toggle flip-flop. The sense of the flip-flop switches each time WR PLS L goes high. The toggling of E19, in conjunction with the 7426 at E23 (2-D4) and the write driver circuit, pumps current alternately into each coil of the selected write head. This toggle action results in the transitions necessary to write data to tape.

2.7.2 Write Erase

The PAL at E9 controls the write erase function. When the signal WR ERASE L (write erase) is asserted, the PAL shuts off write pulses. Write current, however, is still flowing to the write heads. Therefore, an erase function is performed; that is, write with no data. This function is used to write gaps on tape. When the write erase signal is released, the PAL goes back to MFM encoding and resumes the generation of write pulses.

2.7.3 Write Head Selection

The write heads are selected by the signals WR HD 1 SEL or WR HD 2 SEL (E23 pins 8, 9, 10; pins 11, 12, 13). Head one writes data in the forward direction, head two in the reverse direction.

With the signals HD 1(2) SEL H asserted high, a logic 1 is applied to pin 10 or pin 13 of the 7426 at E23. E23 then outputs a logic 0, which grounds the centertap of the selected write head. Current is then alternately applied to each side of the write head coil, through the transistor pairs at E30 (pins 8, 9, 10 and 12, 13, 14), or E30 (pins 5, 6, 7 and 1, 2, 3), each time the sense of flip-flop E19 switches. This provides a constant current source of 15 milliamps to each write head coil. The alternate application of the current results in the transitions needed to write data to magnetic tape.

2.7.4 DC Low Circuit (Sheet 2)

The DC Low circuit senses a low voltage condition (either +5 or +12 V dropping below their acceptable levels) and shuts down the functions of the tape drive. It shuts down the motor current, resets the 8751 microprocessor at E1 (1-D6), and disables the write current circuitry.

2.7.4.1 +12 Volt Path -- As long as +12 volts doesn't go below an acceptable level (about 10 V) the transistor at E6 (pins 1, 15, 16 -- 1-A1) is turned on.

If the voltage drops lower than the base-emitter junction voltage of that transistor, E6 (1, 15, 16) turns off. Pin 1 rises, turning on E6 (6, 7, 8). When E6 (6, 7, 8) turns on, its pin 7 drops, asserting the signal DC LOW L.

A 330 nf capacitor (C47) provides positive feedback and some hysteresis. When DCLOW goes to a logic level 0, the capacitor discharges, dumping some charge back to pin 16 of E6, and turning it off harder. The hysteresis prevents the transistor from oscillating if there is noise at its base (pin 16) when the voltage drops. The hysteresis, then, is to make sure that the DCLOW signal is of a long enough duration.

Also as E6 pin 1 rises (pulled up by R19 to +5 V), transistor E6 (pins 2, 3, 4) is turned on and the reset signal RST H is asserted. The 1 MF capacitor at C3 (1-A3) discharges. C3 holds the reset line to the 8751 microprocessor asserted on power-up until +5 volts has ramped up completely and cleanly.

2.7.4.2 + 5 Volt Path -- The signal DCLOW is asserted through the same transistor pair as +12 V (E6).

The +5 V low circuit consists essentially of E6 (9, 10, 11) and E6 (12, 13, 14). If +5 V drops lower than about 4.6 V, E6 pin 12, and E6 pin 11 reach about 3.9 V. This asserts DCLOW through E6 (1, 15, 16) and E6 (6, 7, 8).

2.7.4.3 Low Voltage Effect -- When DCLOW is asserted, it places a low on the set input of the 74S74 flip-flop at E19, pin 10 (2-D4). When the set input is asserted, it causes the flip-flop to assert pin 9 of the PAL at E9. When this pin is asserted, the PAL shuts off the 1 MHz clock. In this way the -1.25 volt reference is shut down. DCLOW also disables the write head select circuit at E23 pins 13 and 9.

When the PAL shuts off the 1 MHz clock, it also shuts off the -1.25 reference voltage used by the DACs which drive the reel motors. Regardless of what else happens at this point, the motor current is shut down when the minus voltage reference is removed.

2.7.5 DAC Reference Voltage Generation Circuit

This section explains how the minus reference voltage is generated and how the DACs use that voltage to energize the reel motors.

The minus reference voltage is generated from the 1 MHz clock that originates at pin 17 of the PAL at E9 (1-B5).

When the 1 MHz signal rises to about 4 V, it charges capacitor C6 (plus voltage on pin 1, minus voltage on pin 2). When the 1 MHz signal comes down, C6 discharges, and, through diode D5, charges C11. When the 1 MHz signal goes up again, D5 is reverse biased and C11 holds the charge. This provides a minus 2.1 V constant voltage source at pin 1 of C11.

The minus voltage source goes to the 1K resistor at R3 (3-D6). The diode at D4 develops a -1.25 reference voltage for the multiplying Digital-to-Analog Converter at E8 (3-D5). The inputs to the DAC at E8 are the data bus bits from the 8751 microprocessor. The micropocessor selects the DAC, then writes numbers into it, using the data bus. The DAC acts like a programmable current source. Its output current through the op-amps at E16 (3-D3) controls the speed of the reel motors. Thus the microprocessor can speed up or slow down the motors by writing larger or smaller numbers into the DAC.

The signals Control A and Control B drive the two reel motors (control A for motor A and control B for motor B). These signals are actually connected to three darlington transistors on the motors' printed circuit board. The signals Feedback A and Feedback B are current return signals from the motors that provide a reference to the DAC.

2.7.6 Automatic Gain Control (AGC) Circuit (Sheet 2)

The 4024 at E12 (2-D7) binary ripple counter and resistor network (R31 -- R36) make up a digital-to-analog converter (DAC). The existence of the AGC circuit means that the microprocessor has only to set up a value initially by asserting CLR AGC H (E12 pin 2), then applying the signal STP AGC L to step the counter up to the desired gain value.

The gain value is translated to a voltage across R21 (12K) and is applied to the op-amp at E16 (2-C8)(pin 10). The LM324 at E16 (2-C8) compares the gain voltage (set by the microprocessor through E12) to a voltage developed by the intensity with which transistors Q2 and Q3 are turned on. Q2 and Q3 are turned on by developing a voltage across R104 and R105. These voltages are averaged together and then applied to E16 pin 9.

The intensity with which Q2 and Q3 are turned on can be controlled by the op-amp. The output of the op-amp (pin 8) is connected to resistors R94 and R95. The higher the voltage goes, the harder Q2 and Q3 are turned on. This configuration, then, works to control the gain of this pre-amp circuit: The microprocessor clears the counter at E12 and steps it up to a desired gain. The gain value is translated to an analog voltage that is then applied to the op-amp at E16. The output of the op-amp turns Q2 and Q3 on with the appropriate intensity, which results in a value being averaged at the junction of R94 and R95, then applied to pin 9 of the op-amp.

2.7.7 Read Head Select Circuitry (Sheet 2)

The quad-transistor package at E27 (sheet 2 -- lower left) is the read head select circuit. Unlike the write head, the read head coil is not centertapped. E27 (5, 6, 7) and E27 (8, 9, 10) select read head 1; E27 (1, 2, 3) and E27 (12, 13, 14) select read head 2.

The two transistor pairs are biased at different levels, so either one of the pairs may be selected by a single control signal (HD 1 SEL H).

For example, the bases of the top pair of transistors (read head 1) are set at about 3.1 V and are not switchable. The other pair, though, (head 2) are influenced by the select signal HD SEL 1 H. When HD SEL 1 H is a logic 1, then about 5 V is applied to E27 pin 2 and E27 pin 13. In this case, the top two pairs of transistors are turned on because the emitters of all four transistors are tied together and pulled up to +12 V. If HD 1 SEL H is low, however, the bottom pair of transistors is turned on and head 2 is selected.

2.7.8 Read Amplifier Circuit (Sheet 2)

The differential preamplifier circuit feeds into the differential input of the 3470 read amplifier chip at E26 (2-B5).

Pins 3 and 4 on the 3470 control the gain of the amplifier. R100 and R101 are controlling the gain of the 3470: if their combined resistance was lower, the gain of the read amplifier would be higher.

The output of the first stage of the 3470 is on pins 16 and 17 (differential output). The read amplifier chip raises the approximately 40 millivolt signal on its inputs (pins 1 and 2) to about 1 V peak-to-peak on each line, or 2 V differential peak-to-peak at ouput pins 16 and 17.

The first stage output is connected to transistors E18 pin 6 and E18 pin 3, and then to inductors L5 and L6. These inductors, along with transistors E18, form a differentiator circuit.

This differentiator circuit takes the signal from the 3470 circuit, amplifies it, and performs a differentiating function. The differentiated, amplified differential analog read signal now passes through a low pass filter composed of L3, L4, C40, C39, L1, L2, and C38.

The output of the differentiator and filter circuit (ANA1 and ANA2) goes back to the 3470 (pins 14 and 15). With the 3470's pins 12 and 13 tied together, this 3470 stage acts like a comparator and is used as a zero crossing detector for peak detection.

The differentiated and filtered signals ANA1 and ANA2 are also connected to an amplitude detection circuit consisting of E18 9, 10, 11; and 12, 13, 14.

The purpose of the 3470 chip is to generate the digital signal RD DATA PLS H. This signal represents the data read from the tape and it consists of a positive pulse for each detected peak.

Pin 10 of the 3470 (RD DATA PLS H) outputs a 100 ns pulse when a zero-crossing detection is found on its input pins 14 and 15. The position of this pulse represents the timing of the analog peaks that were read from the tape. This raw data is sent to the phase lock loop where the clock signal is recovered and the MFM data is decoded and sent to the controller in the host system via the serial bus.

2.7.9 Phase Lock Loop Circuit (Sheet 4)

The read data pulse from the read amplifier circuit is connected to the PAL at E25 (4-D4)(pin 9) in the phase lock loop circuit. The 500 KHz write clock is also connected to the PAL at E25 (pin 8).

Whenever there is a gap going into the phase lock loop (a burst of non-existent or invalid data), the phase lock loop locks in high gain mode on the 500 KHz write clock. This is so the integrating capacitor C25 stays charged nominally, keeping the voltage control oscillator (VCO) running at a nominal frequency. Keeping the integrating cap charged nominally means that not as much correction has to occur when the preamble (first burst of valid data) to the data field comes along.

On the left side of sheet 4, three signals enter the analog circuitry: Pump Up L, Pump DN L, and RD EN H. The PAL at E29 (4-D7) sources these signals. Pump Up L and Pump Dn L are the phase error correction signals to the charge pump. These signals are in place so that the frequency of the VCO can be changed. The signal RD EN H is a gain control signal for the charge pump. It changes the gain of the charge pump to about 5 to 1, so that in high gain mode, there is about five times more current for the corrections than when in low gain mode.

In the gap (and during the early part of the preamble), the phase lock loop is in high gain mode. When in high gain mode, the Read Enable signal is low. When the Read Enable signal goes high, the circuit is in low gain mode. The circuit goes into low gain mode about halfway through the preamble and stays there during the data field.

When the phase lock loop is locked on the 500 KHz clock (write clock) the loop is in high gain mode and RD EN H is low. With RD EN H low, E22 (2,3,4) is turned off. With E22 (2,3,4) turned off, there are two constant current sources providing charge to the loop filter consisting of C24, R53, and C25.

2.7.10 Pump Down Circuit

When the signal Pump Dn L goes low, transistor E22 (8,7,6) is turned off, enabling the pump down constant current source.

A resistor-divider network is connected to the base of E22 (11, 10, 9), which produces about 2.9 V at the base of E22 (pin 9). There is a 0.7 V drop across the base-emitter junction of E22, producing about 2.1 V at pin 10. This results in a current through diode D10 and resistors R79 and R83 in high gain mode, and through R79 alone in low gain mode.

The collector of transistor E22 is connected to the filter cap at C25. C25 is the major integrating cap in this circuit. R53 develops the phase correction voltages for the VCO.

So when a pump down occurs (Pump Dn L goes low), a pump down correction is telling the VCO clock to slow down, through the 74S124 chip at E21. The output of E21 (VCO OUT H) is connected to the clock input of the PAL at E25.

When the Pump Dn signal is not asserted, E22 (6, 8, 7) turns on, pulling up pin 10, reverse biasing the base-emitter junction of E22 - 10 and 9, and turning the constant current source off.

2.7.11 Pump Up Circuit

The constant current source for the pump up circuit consists of resistors R49 and R50, diodes D7 and D8, and transistor Q1.

A resistor-divider network is connected across the base (pin 1) of transistor Q1. When the Pump Up signal (Pump Up L) is asserted low, it pulls the base of Q1 down to about 4.5 V. When the base is pulled to 4.5 V, a drop across the base-emitter junction means that the emitter voltage is about 5.2 V.

At this point, there is 5.2 V on one side of the parallel network (R49, R50, D7, D8) and 12 V on the other side (R49 and R50 pins 2). The current [determined by 6.8 volts across R50 (low gain mode) or that current plus the six volts which is across R43 in high gain mode] goes to the loop filter through the collector at Q1. A pump up correction causes the charge to be dumped into integrating capacitor C25 and develops a phase error correction voltage across R53. Both the charge being dumped and the phase error correction voltage cause the VCO to run faster.

In the case of pump down, the cap at C25 was discharged slightly. In this case, however, C25 is charged slightly.

2.7.12 VCO Generation

The VCO E21 (4-C3) chip's output frequency is essentially controlled by the voltage at it's input pin 2. The higher that voltage is, the higher frequency its clock output will be (pin 7).

The circuit that consists of E22 (12, 13, 14) (4-A4), R48, R55, and D9 is a compensation circuit that compensates for differences in VCO chips' center frequencies. It also eliminates the need for adjustments to the frequency-determining capacitor that is part of the VCO circuit.

Optimum range and linearity are achieved by operating the VCO such that the center frequency occurs at 3.2 input volts. To achieve this goal, and to compensate for differences between VCO chips, a varactive diode (D9) is included in the circuit. This diode adjusts its capacitance based on how much reverse bias voltage is across its capacitor (D9).

The 8751 microprocessor sends out the Read Enable control signal (RD EN H) by synchronizing on the occurences of the gap interrupt (the signal GAPL on the microprocessor's input pin 13). When the microprocessor is first locking on the gaps (after the tape has come up to speed), it looks for the assertion of the gap interrupt signal, sets an internal timer running, waits until about halfway through the preamble, then asserts read enable.

When Read Enable is asserted, transistor E22 (2, 3, 4) turns on. When the transistor turns on, it pulls the anode (pin 2) of the 1N4152 diode at D7 (junction of R49) low, and pulls the cathode of D10 and R83 up, so it effectively disconnects R49 and R83 from being part of the network for the pump up and pump down current sources.

On the lower half of the constant current source (D10), 2.1 V are present at the emitter of E22 (pin 10). But instead of 5 milliamps of current from the constant source, there is only about 1 milliamp. This lower current results because the diode D10 and resistor R83 have effectively been eliminated from the circuit. The result is that there is only 1 milliamp of correction current going to the loop filter.

The upper half of the constant current source (D7, R49, R50) works much the same way as the lower half; that is, R49 and D7 are effectively out of the circuit, which means that R50 limits the current flowing to about 1 milliamp.

The Read Enable Signal, in addition to being connected to the transistor E22, is also connected to the PAL at E25 (pin 7).

When the read enable signal is asserted, the phase lock loop circuit is decoding the data, which it knows is all logic 1s, in the preamble. When it sees a missing transition in a data cell (a 0), it clocks out that first zero onto the serial bus, through the quad driver at E5 (26LS31). The read clock is also output from this quad driver at the same time. E5 is connected to the differential signal cable that connects to the 7201 chip on the controller.

This zero acts almost like a start bit, in that it informs the 7201 to begin its CRC checking and to start its serial UART. Followed by the zero is the data, the CRC, and the postamble from the phase lock loop circuit.

2.7.13 Pump Up and Pump Down Signal Generation (Sheet 4)

The PAL at E25 (4-D4), in conjunction with the PAL at E29 (4-D7), generates the Pump Up and Pump Down signals. The PAL at E29 is being used as a phase detector.

The PAL at E25 has the 140 ns (approximately) read pulse on its input pin 9. It uses the read pulse, with the VCO clock on its pin 1, to form the load pulse LOAD PLS H. The load pulse lasts exactly one VCO clock period in duration. The result is one load pulse per read data pulse through the PAL at E25.

This synchronized (in effect) version of the read pulse is connected to the PAL at E29 (pin 6). E29 provides a counting function (CNT0 - CNT4) such that each data cell has 16 VCO clocks and each clock cell has 14 VCO clocks. So the data cell has a maximum of eight clocks for pump down and eight clocks for pump up.

If the read data is exactly on time, the load pulse to E29 is at the exact center of the data cell, and no correction needs to be performed. But if the load pulse is early (due, for example, to peak shift), then the VCO clock has to go faster to catch up to the pulse in relation to the data cell. In this case, the PAL asserts the signal Pump Up L. Pump up increases the frequency of the VCO clock. When the center of the cell occurs, the Pump Up signal is withdrawn and the PAL at E29 continues counting.

If the load pulse is late, the counter at E28 gets loaded with the 2's complement of the number of VCO periods for which it was late; then pump down is asserted until the carry signal is asserted.

2.7.14 Data Detection

When a load pulse occurs in any part of a data cell, it is considered a logical one and is clocked out from the PAL at E25 as a one. Any missing load pulse within a data cell is considered a zero.

2.7.15 Drive Commands and Status

Serial Drive status is sent back to the controller by the microprocessor, via the 26LS31 quad driver at E5 (4-D2). Drive status is sent to the 7201 MPSC chip on the controller over the serial bus.

Commands are received by the 8751 microprocessor via the 26LS32 quad receiver at E13 (1-D8). Commands are sent over the serial bus from the 7201 MPSC chip on the controller.

Status information is sent back to the controller from the microprocessor's TxD pin. It is usually sent in response to a commmand from the controller which is accepted on pin 10 of the microprocessor. The 8751 in this case is set up similar to a full-duplex uart.

2.8 TAPE HUB (Refer to Figures 2-4 and Appendix A-2)

When the cartridge release handle is lifted, the supply motor's hub is withdrawn (see Figure A-2 in Appendix A). The part of the hub containing the teeth mates with the hub in the tape cartridge to align the height of the tape in the drive. This vertical alignment is needed for two reasons:

1. The tape must be at the correct height for the leader in the cartridge to couple with the leader in the drive.

2. The height of the tape must be the same on both the supply reel (tape cartridge) and the take-up reel, because tight tolerances are needed for the read/write heads to correctly access the tracks on the tape.

2.9 LINK ARMS

The link arms to the left and right of the hub align the cartridge horizontally in the drive. Horizontal alignment is neeeded to make sure that the cartridge cannot shift forward or backward.

The handle mechanism controls both the tape hub and link arms.

2.10 TAPE CARTRIDGE INSERTION

As the cartridge is inserted the door on the cartridge opens, exposes the leader mechanism, and then swings out of the way. Two plastic arms are used as guides to mate the supply leader with the take-up leader.

When the cartridge is completely inserted, the interposer is released, locking the cartridge into the drive. The front reel lock inside the cartridge is now also released. The rear reel lock is held until the handle is lowered. As the handle lowers, the tape hub moves to mate with the cartridge and provide vertical tension. At the same time, the link arms move into place to provide horizontal stability to the cartridge.

2.11 TAPE LOAD TO BEGINNING OF TAPE (BOT)

The next operation is to instruct the tape drive to load the tape to the BOT hole. To do this, press and lock the Load/Unload switch on the front right side of the drive. (See also the TK50 Tape Drive Subsystem User Guide EK-OTK50-UG.) Pushing in the switch informs the drive to move the tape from the Load Point (where the leaders couple) to the BOT marker. The 8155 senses both the Load/Unload switch closing and when the tape reaches BOT. When the 8155 senses BOT it informs the controller, through the 8751, that the drive is on-line and ready for use.

2.12 TAPE MOTION

The tachometer senses tape motion. The tachometer consists of a capstan and a finely etched disk. The rear portion of the tachometer has an LED and phototransistor that senses the holes in the etched disk. The capstan and the disk spin as the tape moves across the capstan. In this way, the tachometer can sense the speed of the tape.

The 8751 controls all tape speed and tensioning. The TK50 does not use any driven capstans or air bearings. The tachometer provides all feedback regarding tape speed to the 8751. Tach pulses are connected to the 8155 via one of its I/O Ports.

The tachometer (tach) has a sensor on a phototransistor to tell the microprocessor that the tach is working correctly. The feedback loop from the tach is tested as part of the power-up diagnostics.

The tape moves forward to BOT at about 6 inches per second under about 3 ounces of tension. When the tape reaches BOT, the 8155 informs the 8751, which then informs the controller that it is ready for use. The controller responds by telling the drive to complete the initialization.

2.13 READ/WRITE HEAD

The read/write head consists of four cores: a read core and write core for the forward direction and a read and write core for the reverse direction. The write cores are 18 mils wide and the read cores are 8 mils wide.

The different widths between the track written (18 mils) and the track read (8 mils) give the read core more leeway to read data. It allows for easier recovery from soft errors inherent in tape media, and it also provides the flexibility to move slightly to either side, to compensate for defects in the tape.

The four cores are physically on one head mechanism. The head is driven by a 1 mil per step stepper motor and is held in contact with the stepper by two springs around the head carriage.

2.14 INITIALIZATION: WRITING AND READING CALTRACKS

The next step is for the head to read or write/read calibration tracks 1 and 2 (CALTRACK1 and CALTRACK2). The controller sends a command to write and read the CALTRACKS.

If the cartridge has never been used, the following sequence takes place.

1. The drive tries to find and read CALTRACKS 1 and 2. Finding neither, it decides that this is a new cartridge.

2. The head seeks to the top of the tape.

3. Once at the top, the head moves down about 0.2 inches.

4. The write core writes a data burst (CALTRACK 1) in the forward direction.

5. The read core immediately reads CALTRACK1. This is called a read-after-write operation. The read core lags the write core by 0.3 inches, so a slight delay is to be expected before the CALTRACK is read back.

6. The head performs the same operation in the reverse direction for CALTRACK 2.

If the cartridge has a previously written CALTRACK, the following sequence takes place.

1. The linear actuator moves the head to its top position.

2. Once at the top, the head moves down about 0.2 inches.

3. The read core reads CALTRACK 1.

4. The head performs the same operation in the reverse direction for CALTRACK 2.

Writing and reading the CALTRACKS are done at operational speed (75 in/s) and tension (5 ounces). After the TK50 reads the first CALTRACK (used cartridge), it comes to a controlled stop, then reverses direction, ramps up to speed, and reads CALTRACK 2.

If CALTRACK1 is not found but CALTRACK2 is okay, or if CALTRACK1 is okay but CALTRACK2 is not found, there is a defective component (refer to Chapter 3). If neither CALTRACKS 1 and 2 are found, the current cartridge is a new one and the CALTRACKS are written. Three retries are performed before the CALTRACK error is reported.

NOTE

There is no way to rewrite CALTRACKS except to bulk erase the cartridge, which destroys all data on the tape.

2.15 WRITING DATA (Figures 2-7 and 2-8)

The TK50 writes data in a serpentine fashion over the entire length of the tape. It writes data down the entire length of tape, on one track, until it reaches a logical EOT marker. (The physical EOT marker is a hole in the tape. The logical EOT marker is a preset, microprocessor-calculated location.) The tape direction is then reversed and the reverse write and read cores are used to write data in the reverse direction the entire length of the tape until it senses logical BOT. Then the direction is changed to the forward direction, the head is stepped up 19 mils, and the forward direction cores are again used.

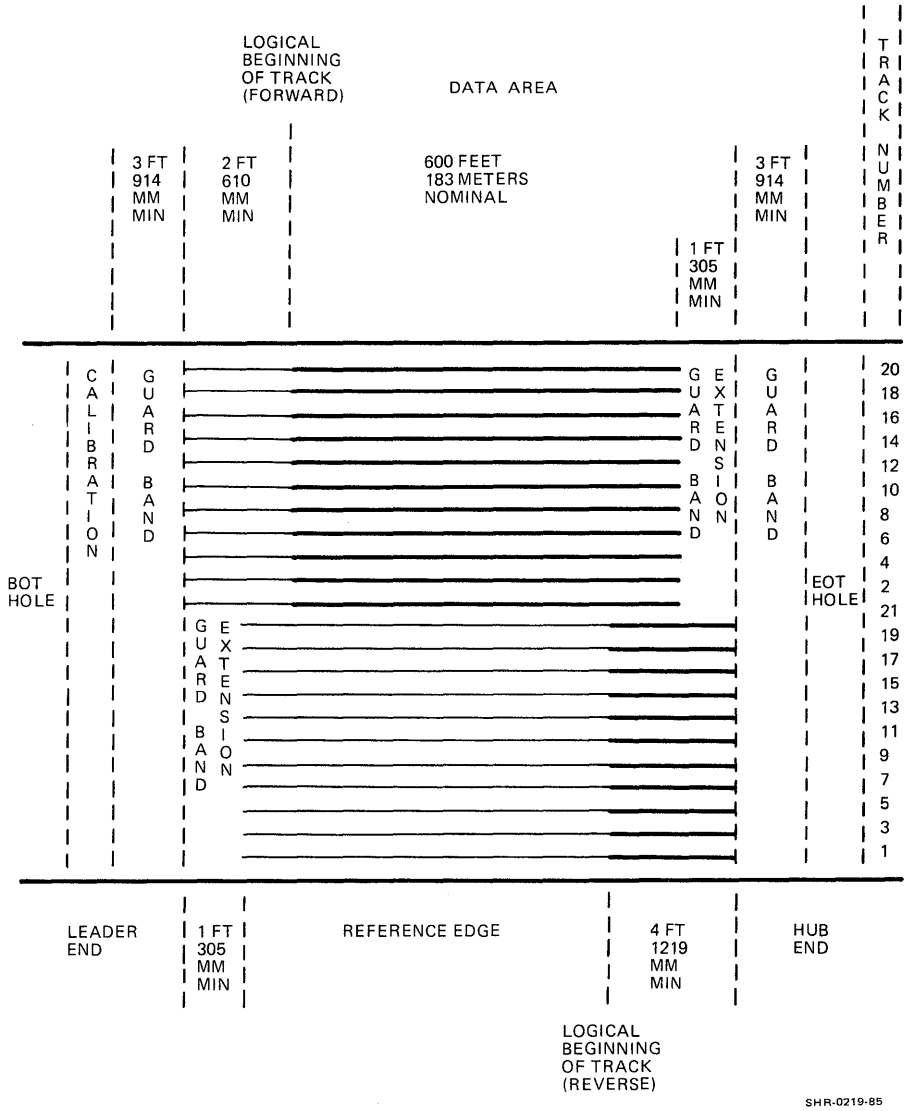


Figure 2-7 Physical Tape Configuration

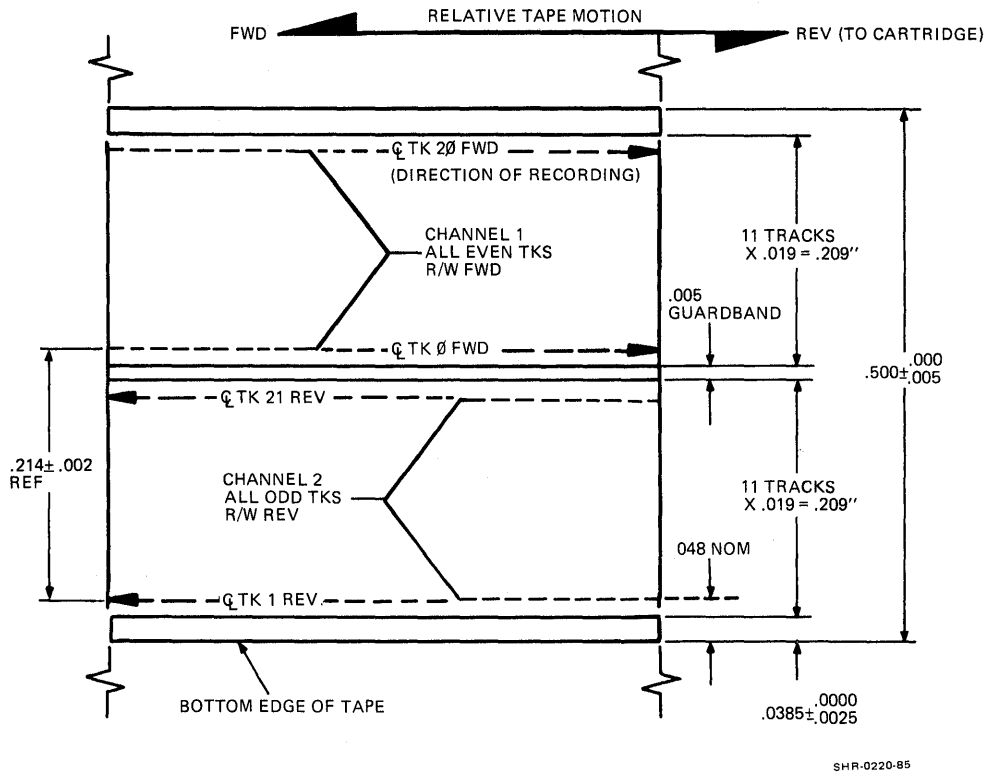


Figure 2-8 Recording Direction

Table 2-2 lists the 26 signals generated by the controller and accepted over the 26-pin flat ribbon cable by the drive.

Table 2-2 TK50 Signal Definition

Pin	Signal
1	GND
2	WRT DATA HIGH
3	WRT DATA LOW
4	GND
5	DR CMD HIGH
6	DR CMD LOW
7	GND
8	WRT GATE HIGH
9	WRT GATE LOW
10	GND
11	ERASE LOW
12	ERASE HIGH
13	GND
14	DR RD CLK LOW
15	DR RD CLK HIGH
16	GND
17	RD DATA LOW
18	RD DATA HIGH
19	GND
20	DR STATUS HIGH
21	DR STATUS LOW
22	GND
23	DR WRT CLK HIGH
24	DR WRT CLK LOW
25	GND
26	CABLE SENSE

2.16 DIFFERENTIAL SIGNAL PAIR DESCRIPTION

Eight differential signal pairs, along with the non-differential signal Cable Sense, are shown in Table 2-3. The direction of these signals is with respect to the drive.

Table 2-3 Differential Signal Pairs

Pins	Signal	Direction	Description
2,3	WRT DATA	In	Write data in NRZ format
5,6	DR CMD	In	Serial Drive Command (see also Table 2-5)
8,9	WRT GATE	In	Write enable gate
11,12	ERASE	In	Erase enable
14,15	DR RD CLK	Out	Drive read clock
17,18	RD DATA	Out	Read data in NRZ format
20,21	DR STATUS	Out	Serial drive status
23,24	DR WRT CLK	Out	Drive write clock
26	CABLE SENSE	Out	Cable sense. Used by the controller to determine drive presence (0 = present).

2.17 SIGNAL INTERFACE TIMING

The critical timing for the signals back and forth between the drive and the controller is shown in Figures 2-9 and 2-10. The notes in the timing diagrams are coded A through U. Table 2-4 explains the coded portions of the timing diagrams.

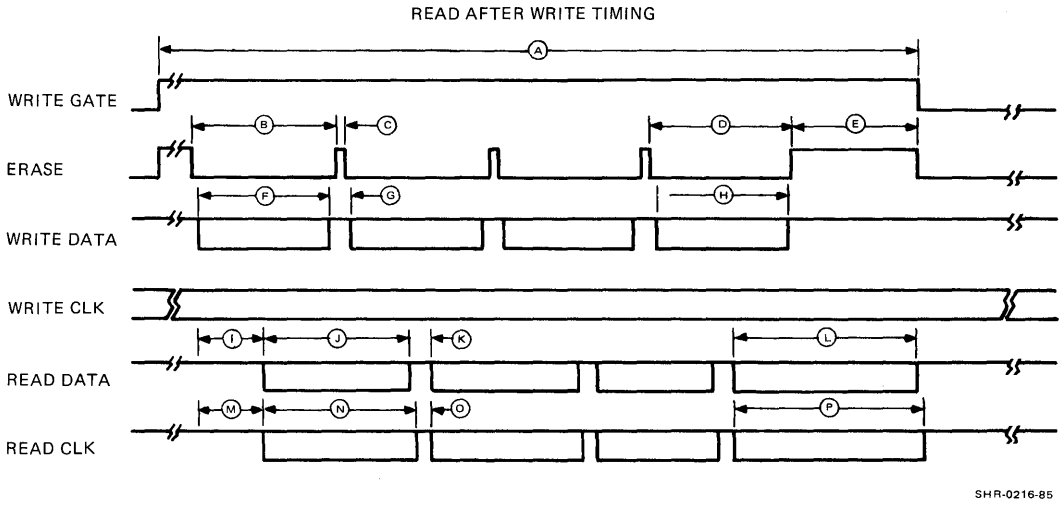


Figure 2-9 Signal Interface Timing (A-P)

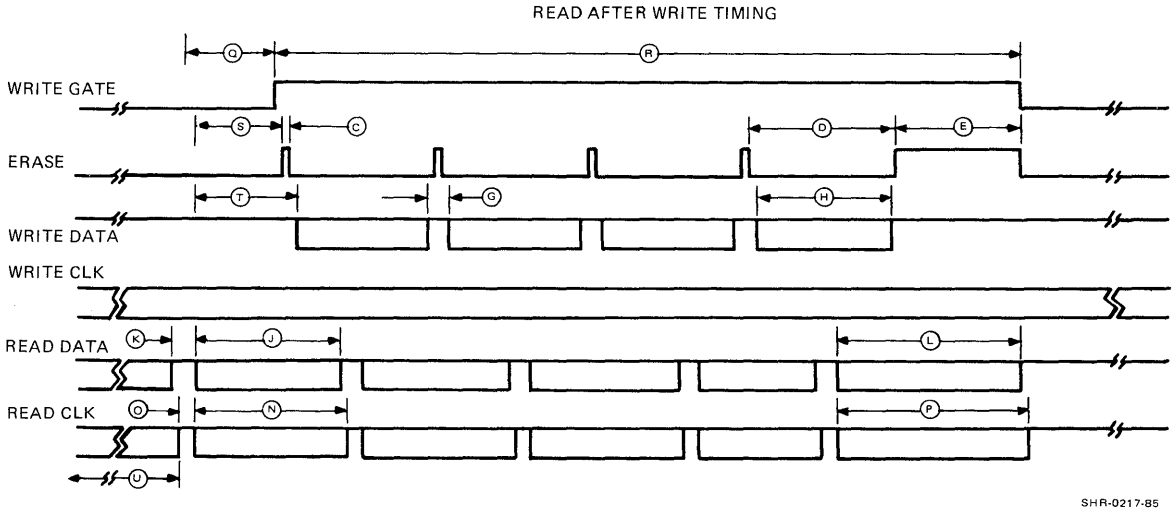


Figure 2-10 Signal Interface Timing (Q-U)

Table 2-4 Signal Interface Timing

Code	Activity	Time
A	Write gate active	From beginning to end of write
B	Erase inactive	8960 us + 10 us (overhead)
C	Erase active	128 us + 10 us (overhead)
D	Erase inactive for last block written	8960 us + 10 us (overhead)
E	Erase active for last block written	3872 us + 1.5% (speed var)
F	Write data active	8480 us + 10 us (overhead)
G	Write data inactive	608 us + 10 us (overhead)
H	Write data active for last block	8480 us + 10 us (overhead)
I	First erase to read data active	4000 us + 1.5% (speed var)
J	Read data active	8480 us + 1.5% (speed var)
K	Read data inactive	608 us + 1.5% (speed var)
L	Read data active for last block	8480 us + 1.5% (speed var)
M	First erase to read CLK active	4000 us + 1.5% (speed var)
N	Read CLK active	8480 us + 1.5% (speed var)
O	Read CLK inactive	416 us + 1.5% (speed var)
P	Read CLK active for last block	8480 us + 1.5% (speed var)
Q	Read CLK to write gate for append	4642 us + 1.5% (speed var)
R	Write gate active for appended write	(Same as A)
S	Read CLK to erase active	4640 us + 1.5% (speed var)
T	Read CLK to write data active	5024 us + 1.5% (speed var)
U	Minimum number of good blocks for VCO lookup	3

Overhead time (overhead) in Table 2-4 is due to microprocessor interrupt handling delays. Speed variation time (speed var) is due to tape speed variation.

2.18 SERIAL CONTROLLER TO DRIVE COMMUNICATIONS

The controller sends commands to the drive through the differential signal pair DR CMD. Status is returned to the controller via the differential signal pair DR Status. The drive's 8751 microprocessor receives and interprets the commands through its built-in serial port, set up as a full-duplex UART. The drive receives drive commands via the AM26LS32 differential receiver (E13) and the microprocessor's RxD (receive data) line. Drive status is transmitted to the controller, via the AM26LS31 differential driver, from the microprocessor's TxD (transmit data) line.

The communications (UART) portion of the 8751 is programmed as follows (Figure 2-11).

Frame format	1 start, 8 data, 2 stop bits.

This is the 8751's UART Mode 2, with T88 set high to create the second stop bit.

Baud rate	187500
Frame time	59 microseconds

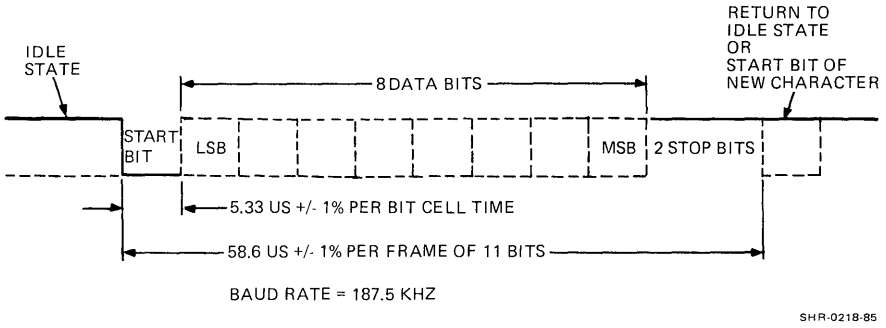


Figure 2-11 Frame Format of Data Coming from Controller

2.19 BASIC CONTROLLER/DRIVE COMMUNICATIONS PROTOCOL

This section explains the handshaking needed to transfer commands, data, and status between the drive and the controller.

2.19.1 Controller-to-Drive Command Protocol

The drive always echoes commands back to the controller to insure the integrity of the transmission. If data bytes other than the initial command byte are required by the command in question, they are also sent by the controller and echoed by the drive.

All commands but one must be echoed by the drive within 500 milliseconds, and all other solicited bytes must be received by the controller within one second, or it assumes that a communications error exists. The only exception is the send status command, which allows up to 9.75 seconds for the status message to be received.

2.19.2 Drive-to-Controller Status Protocol

Status sent from the drive to the controller always requires the transmission of an acknowledge message from the controller (40H), before the drive proceeds with any further communication. Two types of status messages can be transmitted from the drive to the controller: solicited and unsolicited.

Solicited status messages are those drive transmissions sent in response to a controller invoked command. Unsolicited status messages are those sent to the controller that were not requested. Drive "change of state" and "drive detected error" result in unsolicited status messages.

2.19.2.1 Change of Drive State -- A drive change of state results in the tranmission by the drive of the one-byte drive status message. Examples of this change of state message are: up to speed, rewind complete, and change of load switch state. Change of state message transmission causes an interruption of drive/controller communication until the controller acknowledges the message.

2.19.2.2 Drive Detected Errors -- An error detected by the drive results in an unsolicited "drive detected error" message to the controller. This message is always preceded by an error notification (80 hex) to the controller. After the controller acknowledges the error notification message, one of the error codes defined in section 3.2 is transmitted to the controller. The transmit/acknowledge protocol is used throughout the error message interchange between the drive and the controller.

2.20 TK50 COMMANDS

Table 2-5 lists and defines the commands that the controller provides to the drive via the 26-pin flat ribbon cable. These serial commands are received and decoded by the 8751 microprocessor at E1 on the drive logic module. The 8751 controls the remainder of the circuits in the drive logic, to perform the operations necessary to successfully execute the command.

Table 2-5 TK50 Commands

Command	Code	Definition
RESET	00	Reset MPU and drive
SNDREV	01	Send software/hardware revision level
SDSTAT	02	Send Drive Status Byte (DRSTAT)
CLRERR	03	Clear Drive Error Bytes
SDREGO	04	Send register contents
SDREGC	05	Continue sending register contents
SDBKAD	06	Send tape count
LDBKAD	07	Load tape count
SNDERR	08	Send the two error bytes
SDDOCT	09	Send dropout data
SKTRKX	0A	Step head to track X
STDAGC	0B	Set read gain to standard value
LOAD	0C	Load tape command (Diagnostic)
MEDIA	0D	Diagnostic test for media dropout
B5CMD	0E	Diagnostic automatic exercise
CALEDG	0F	Calibrate to tape edge only
CALIBR	10	Calibrate track position
REWIND	11	Rewind to BOT
UNLOAD	12	Software unload tape
LOAD	13	Move forward at load speed
MOVFWD	14	Move forward (TRKADR)
MOVBWD	15	Move backward (TRKADR)
SEEK	16	Seek to block
BSPACE	17	Backspace for R/W forward
FSPACE	18	Space forward for R/W backward
DOSTOP	19	Media test, stop on dropout
BSTOP	1A	Space opposite, before stop
STOP	1B	Stop tape
HEAD1	1C	Select head 0
HEAD2	1D	Select head 1

Table 2-5 TK50 Commands (Cont)

Command	Code	Definition
ENWRT	1E	Enable write
CLRWRT	1F	Clear write and erase mode
SMPDRP	20	Sample dropout data, in "WM"
ENVCO	21	Software enable VCO
ENREAD	22	Software enable read (Diagnostic)
DISCRP	23	Disable sampling dropouts
SMPCIR	24	Sample motor current, tape speed
TRK-1	25	-1 mil offset during present move
TRK+1	26	+1 mil offset during present move
ONESTP	27	1 mil step command

TK50 commands can be grouped into four basic types: Control, Motion, On-the-Fly, and Diagnostic commands.

2.21 TK50 DRIVE STATES

There are two classes of drive states: Drive Normal Status and Drive Error Status. Changes in drive state into either one of these classes cause an unsolicited status message to be sent to the controller (see Section 2.19.2 -- Drive to Controller Protocol). The controller processes and acts on state change messages as detailed in this section.

2.21.1 Drive State Status

Drive state changes that do not indicate a drive detected error result in the drive sending a hexadecimal code to the controller indicating the current drive state (or state changed to). The controller responds to this type of state change transmission with an acknowledge. Table 2-6 lists the non-error drive states and the following subsections explain them.

Table 2-6 Non-Error Drive States

Code	Status
40	Done
50	Enable write gate
60	Dropout sensed
70	Track boundary
NA	Load/run state change (see Paragraph 2.21.1.5)

2.21.1.1 DONE (40) -- The Done state has multiple meanings, depending on the drive/controller events occuring before the Done message is transmitted. This state usually signifies that the drive has completed a controller-invoked event, such as up to speed, BOT sensed, or tape motion stopped.

2.21.1.2 ENABLE WRITE GATE (50) -- The enable write gate state is used during the head calibration sequence. It requests the controller to assert the Enable Write Gate signal.

2.21.1.3 DROPOUT SENSED (60) -- Dropout Sensed status is transmitted for every dropout detected by the drive when in the dropout test diagnostic mode.

2.21.1.4 TRACK BOUNDARY (70) -- The Track Boundary state signals to the controller that the beginning or end of a logical track was encountered during normal tape motion.

2.21.1.5 LOAD/RUN STATE CHANGE (Table 2-7) -- Load/Run State Change is sent to the controller when the drive senses that its front panel load switch is changed from run to unload. Drive initiation of the unload operation won't begin until the controller issues a Stop or Reset command.

Table 2-7 Send Status Byte Bit Assignments

Bits	7	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	0	Request for initialization
	0	0	X	X	X	X	X	1	Cartridge is present
	0	0	X	X	X	X	1	X	Head is positioned on Track 0
	0	0	X	X	X	1	X	X	Unload state
	0	0	X	X	1	X	X	X	Write Lock state
	0	0	X	1	X	0	X	1	BOT state
	0	0	1	X	X	0	X	1	Run state
	0	0	1	1	X	0	X	1	Rewind in progress
	1	0	0	0	0	0	0	0	Error state

X = Don't care

2.21.2 Drive Error Status

When a drive detected error occurs, it causes the drive to send an unsolicited error message (80H) to the controller. The controller acknowledges the error indication with a normal acknowledge message (40H). When the drive receives and decodes the 40H, it sends the error code that corresponds to the drive detected error.

Drive error status messages all have bit 7 of their corresponding hexadecimal code set. All drive error status codes that are less than 90H are fatal drive errors and cause the termination of drive/controller communication. All non-fatal drive errors have a hexadecimal code of 90H or greater, and allow resumption of drive/controller communication after the controller issues a Clear Drive Error command.

CHAPTER 3
DRIVE UNIT REPAIR

3.1 GENERAL

This chapter provides information on diagnosing and repairing the Drive Unit of the TK50 Tape Drive Subsystem. The chapter is divided into two major sections: first, it lists the error codes that the subsystem microcode generates when an error is detected; second, it provides instructions on how to remove a failed subassembly.

This chapter is not intended to be used for field troubleshooting. Since the drive unit is a Field Replaceable Unit (FRU), the field engineer will not be troubleshooting it to the subassembly level, but replacing it as a whole. This chapter is for technicians at Field Repair Depots.

3.2 ERROR CODES

This section provides error codes, lists probable causes for the error, and recommends actions to be taken to repair the drive. Section 3.3 gives instructions for removing and replacing subassemblies that failed. The error codes listed are those reported to the operating system error log.

3.2.1 Failure to Load to Beginning of Tape (BOT) -- (81H)

Causes:

1. Supply/takeup leader length is incorrect (if second error byte = 96H = BOTER).

2. There is an obstruction in tape path (if second error byte = 87H = DRAGER).

3. BOT sensor is marginal.

Recommended Action:

1. Replace cartridge and retest.
2. Check for and fix causes of drag, if possible.
3. Inspect BOT/EOT sensor and wiring. Replace BOT/EOT sensor if necessary.

3.2.2 Failure to Load Tape into Cartridge (82H)

Causes:

1. Supply/takeup leader length is incorrect; second error byte = 096H (BOTER).
2. There is an obstruction in tape path; second error byte = 87H (DRAGER).
3. Motor A (supply motor) rotated in wrong direction; second error byte = 8FH.

Recommended Action:

1. Replace cartridge, retest.
2. Check for and fix causes of drag, if possible.
3. Inspect BOT/EOT sensor and wiring. Replace BOT sensor if necessary.

3.2.3 General Motor or Tachometer Failure (83H) -- A hard pull on Motor B produces less than 5 tach pulses with BOT off.

Causes:

1. Motor B stalled or is not connected.
2. Tachometer is bad or not connected (produces no pulses).
3. Leader is stuck in tape path.
4. Cartridge jammed.

Recommended Action:

1. Check all cable connections.
2. Check for and remove friction in tape path.
3. Replace Motor B or tachometer.

3.2.4 Motor A Failure (Supply Motor) -- (84H)

Motor A was pulling against motor B without sensing a reversal of direction via the motor A Hall switches.

Causes:

1. Supply motor is bad or not connected.

Recommended Action:

1. Replace Motor A (supply motor).

3.2.5 Motor B Failure (Take-up Motor) -- (85H)

Motor B was pulling with excessive current and motor A did not rotate a minimum of 90 degrees. Tachometer pulses were present.

Causes:

1. Motor B is bad or there was an obstruction in the tape path.
2. Motor A Hall switches are not functioning or not properly received.

Recommended Action:

1. Check for obstruction in tape path and cabling problem.
2. Check whether both Hall switches at MPU are toggling when Motor A rotates.
3. Replace faulty motor (A or B).

3.2.6 Drive Lost Control of Tape or Bad Tachometer -- (86H)

The drive experienced either incorrect spacing of tach pulses or an insufficient number of pulses were detected.

Causes:

1. Motor A or Motor B is bad.
2. Tach problem, high friction on the tape, or the tape stalled.
3. There is no tape in path.

Recommended Action:

1. Check for tape presence.
2. Check for drag in tape path.
3. Check motors.
4. If no trouble is found, reset drive and get detail error report (if any) via initialization procedure.

3.2.7 Excessive Drag in Tape Transport -- (87H)

Currents to the motors exceeded limits in servo mode.

Causes:

1. There is a jam or interference in tape path.
2. Tape overran EOT marker, now is at tape end.
3. One of the motors is bad.

Recommended Action:

1. Check for obstruction in tape path.
2. Reset drive and observe any error messages during drive initialization (repeat several times).

3.2.8 Failure to Stop Tape or Remain Stopped -- (88H)

Excessive tach pulses during deceleration mode.

Causes:

1. Motors are out of spec.
2. One of the motors is bad.
3. Bad tape reel estimate during initialization.

Recommended Action:

1. Reset drive several times and observe stop at low speed and after rewind.
2. Replace faulty motor(s).

3.2.9 Cartridge Insert Error -- (89H)

The drive experienced improper timing or occurrences of the unload/BOT signal or tachometer signal.

Causes:

1. Leaders are misaligned.
2. EOT/BOT circuit is bad.
3. There is high drag in tape path.
4. Handle switch is bad.

NOTE:
Specific error in second error byte.

Recommended Action:

1. Check for and remove obstruction in tape path.
2. Check and repair leader alignment.
3. Check and/or replace cartridge.
4. Check and/or replace leader mechanism.

3.2.10 Cartridge Extract Error -- (8AH)

BOT sense was lost or there were insufficient tachometer pulses in 25 seconds.

Causes:

1. Leaders are misaligned.
2. BOT/EOT circuit is bad.
3. Cartridge only partially ejected.
4. There are too many tach pulses. Drive leader did not engage.

Recommended Action:

1. Check for interference in receiver.
2. Check eject mechanism and springs.
3. Replace drive leader if damaged.

3.2.11 Move Error -- (8BH)

The controller tried to move the tape while the drive was in an error state, or the drive was still in an error state when the controller issued a tape motion command.

Causes:

1. Block address overflow or underflow is not received by the controller.
2. A new command and error message occurred at the same time.
3. Controller is out of sequence.
4. Operator interfered.

Recommended Action:

1. Restart.

3.2.12 Deceleration Error -- (8CH)

The servo exceeded the time allotted to slow down to 8.5 inches per second.

Causes:

1. Motor A is bad, or motors are out of spec.

Recommended Action:

1. Reset drive and observe detail error messages, if any.
2. Replace Motor A.

3.2.13 Reel Error -- (8DH)

A second attempt to balance the reels in the unit failed. Improper balance or distribution of tape between take up and supply reel.

Causes:

1. Tape overran logical EOT and is now at tape end.
2. Tape is too short between EOT hole and end.
3. Tachometer and/or Motor A Hall switch connection is intermittent.

Recommended Action:

1. Rewind tape 20 turns minimum into cartridge if at tape end.
2. Power up.
3. Replace cartridge.

3.2.14 Check Byte Error -- (8EH)

Causes:

1. 8751 microprocessor is bad.

Recommended Action:

1. Replace drive board.
2. Replace microprocessor.

3.2.15 Unload Error -- (8FH)

The unload microdiagnostic test failed.

Causes:

1. Motor A went in the wrong direction. The motor is bad.

Recommended Action:

1. Replace Motor A.

3.2.16 8155 Memory Error -- (90H)

The memory microdiagnostic test failed during initialization. 8155 RAM locations were loaded with an address, then read back wrong.

Causes:

1. The 8155 is bad.
2. The 8751 microprocessor has a bad bus.

Recommended Action:

1. Inspect drive board for broken leads, etches.
2. Re-seat socketed 8751 microprocessor, retest.
3. Replace drive board.

3.2.17 8155 Timer Error -- (91H)

A timer in the 8155 failed. The 8155 timers were tested against the 8751's timers and were incorrect or not operational.

Causes:

1. The 8155 is bad.
2. The 8751 has a bad I/O bus.

Recommended Action:

1. Re-seat 8751 microprocessor and retest.
2. Replace the 8155 or the drive board.

3.2.18 Read Head 1 Error -- (92H)

The read amplitude on head 1 was too low during calibration. The signal during calibration was insufficient.

Causes:

1. Calibration tracks on the tape are bad.
2. Read head cables are bad or intermittent.
3. Head is contaminated.

Recommended Action:

1. Inspect the head and cables. Is there continuity?
2. Wipe the head with a dry tissue (not on customer site).
3. Replace the head.

3.2.19 Read Head 2 Error -- (93H)

The read amplitude on head 2 was too low during calibration. The signal during calibration was insufficient.

Causes:

1. Calibration tracks on the tape are bad.
2. Read head cables are bad or intermittent.
3. Head is contaminated.

Recommended Action:

1. Inspect the head and cables. Is there continuity?
2. Wipe the head with a dry tissue (not on customer site).
3. Replace the head.

3.2.20 Cartridge Insert/Extract Error -- (94H)

A runaway condition during the insertion or extraction of the tape cartridge.

Causes:

1. Handle microswitch is bad or not connected.

Recommended Action:

1. Check handle microswitch connector.
2. Replace handle microswitch connector.

3.2.21 EOT Sensed in Read/Write/Seek State -- (95H)

The drive failed to handle the logical end of tape marker and reached physical end of tape.

Causes:

1. Communication between the drive and the controller is faulty. The controller lost power while the tape was moving.
2. There is a drive/controller communications protocol problem.
3. Tachometer is intermittent.
4. Tape is too short.
5. There are hole(s) in the tape.
6. BOT/EOT circuit failed.

Recommended Actions:

1. Inspect tachometer connections.
2. Reset.
3. Restart, retest.

4. Replace the drive board.

3.2.22 BOT Sensed in Read/Write/Seek State -- (96H)

The drive failed to handle the logical beginning of tape marker and encountered physical beginning of tape.

Causes:

1. Communication between the drive and the controller is faulty. The controller lost power while the tape was moving.
2. There is a drive/controller communications protocol problem.
3. Tachometer is intermittent.
4. Tape is too short.
5. There are hole(s) in the tape.
6. BOT/EOT circuit failed.
7. Bad reel size estimate during initialization.

Recommended Actions:

1. Inspect tachometer connections.
2. Reset.
3. Restart, retest.
4. Replace the drive board.

3.2.23 Address Overflow Error -- (97H)

A drive block address overflow occurred and exceeded the usable area on the tape.

Causes:

1. The controller failed to issue a stop command or lost power.

Recommended Action:

1. Clear error and rewind.
2. Reset, restart.

3. Troubleshoot loss of power; replace controller.

3.2.24 Address Underflow Error -- (98H)

A drive block address underflow occurred and exceeded the usable area on the tape.

Causes:

1. The controller lost power while tape was moving backward.

Recommended Action:

1. Clear error and rewind.
2. Reset, restart.
3. Troubleshoot loss of power; replace controller.

3.2.25 Servo Error -- (99H)

Excessive speed variations, exceeding limits, wobble (balance problem in tape reels).

Causes:

1. There is a problem with the cartridge, bearing, and spring load.
2. There is a problem with the radial/vertical runout of hubs.
3. There is a problem with the runout/balance of capstans.
4. Tach connection is intermittent, extra pulses.
5. One motor is bad.

Recommended Action:

1. Inspect for excessive runout.
2. Inspect tachometer connection.
3. Reset drive. Observe detail error messages, if any.

3.2.26 Failure in Tracking -- (9AH)

Reserved for future use.

3.2.27 Command Error (9BH)

The command from the controller was not recognized.

Causes:

1. Interface cabling is faulty.
2. There is a bad receiver chip on the drive module, or bad driver chip on the controller module.

Recommended Action:

1. Reinsert or replace cable.
2. Replace module(s).

3.2.28 Illegal Command -- (9CH)

The command issued was incompatible with the drive state.

Causes:

1. There is a communication/protocol error with controller.
2. Operator forced an unload while the controller started to read, write, or seek.

Recommended Action:

1. Restart and observe sequence.
2. Potential hardware/software problem.

3.2.29 Write Lock Error -- (9DH)

The tape was in a write-locked state when a write operation was requested.

Causes:

1. Cartridge write protect tab was in wrong position.
2. Write protect switch on the cartridge is faulty or misaligned.
3. There is a bad cable connection or broken wire.
4. There is a bad cartridge (broken plastic pin).

Recommended Action:

1. Check the write protect switch on the cartridge.
2. Check the cable.
3. Replace the cartridge.

3.2.30 Write Gate Signal Timing Error -- (9EH)

The write gate signal from the controller was received when the tape was stopped.

Causes:

1. There is a problem with the controller timing/logic.
2. Drive to controller cable.
3. Bad receiver chip on the drive board.
4. Bad driver chip on the controller.

Recommended Action:

1. Restart, retest.
2. Replace module(s) -- controller, then drive.
3. Replace the cable.

3.2.31 No Write Gate Error -- (9FH)

Write gate was not asserted after the request during calibration.

Causes:

1. There is a problem with the controller timing/logic.
2. There is a problem with the drive/controller cable.
3. Receiver (drive) or driver (controller) is bad.
4. Pin connection on microprocessor is bad.

Recommended Action:

1. Reinsert the cables.
2. Reinsert the 8751 microprocessor.

3. Restart.

4. Replace module(s).

3.2.32 Error Sensing CALTRACK1 -- (A0H)

Causes:

1. Media has degraded.
2. There is a problem with head cables, connector.
3. Head is failing.
4. Head is contaminated.
5. Tape is partially erased or overwritten.

Recommended Action:

1. Replace cartridge.
2. Inspect head cables and connectors.
3. Wipe the head with a clean dry tissue (not on customer site).
4. Replace the head.

3.2.33 Error Sensing CALTRACK2 -- (A1H)

Causes:

1. Media has degraded.
2. There is a problem with head cables, connector.
3. Head is failing.
4. Head is contaminated.
5. Tape is partially erased or overwritten.

Recommended Action:

1. Replace cartridge.
2. Inspect head cables and connectors.
3. Wipe the head with a clean dry tissue (not on customer site).
4. Replace the head.

3.2.34 CALTRACK 1 Error - (A2H)

Edge detection of CALTRACK1 was out of specification.

Causes:

1. Media has degraded.
2. There is a problem with head cables, connector.
3. Head is failing.
4. Head is contaminated.
5. Tape is partially erased or overwritten.

Recommended Action:

1. Replace cartridge.
2. Inspect head cables and connectors.
3. Wipe the head with a clean dry tissue (not on customer site).
4. Replace the head.

3.2.35 CALTRACK2 Error -- (A3H)

Edge detection of CALTRACK2 was out of specification.

Causes:

1. Media has degraded.
2. There is a problem with head cables, connector.
3. Head is failing.
4. Head is contaminated.
5. Tape is partially erased or overwritten.

Recommended Action:

1. Replace cartridge.
2. Inspect head cables and connectors.
3. Wipe the head with a clean dry tissue (not on customer site).
4. Replace the head.

3.2.36 CALTRACK2 Offset Error -- (A4H)

The offset of CALTRACK2 from CALTRACK1 is too great. The distance and number of steps needed to move from CALTRACK1 to CALTRACK2 is too great.

Causes:

1. Tape is partially erased.
2. The read/write head is bad.
3. Stepper motor is bad.

Recommended Action:

1. Replace cartridge.
2. Wipe head with clean dry tissue (not on customer site).
3. Inspect head cables and connectors.
4. Replace the head.
5. Replace the stepper motor.

3.2.37 Tape Edge Error -- (A5H)

A search for the top edge of the tape failed.

Causes:

1. Stepper motor is bad.
2. Top head is not writing or reading.
3. There is excessive feed through.
4. Drive board is bad.
5. Head is contaminated.

Recommended Action:

1. Inspect cables and shield.
2. Wipe the head with a clean, dry tissue (not on customer site).
3. Replace the read/write head.
4. Replace the drive board.

3.2.38 Top Tape Edge Tolerance Error -- (A6H)

Causes:

1. Stepper motor is bad.
2. There is a problem with the cabling to stepper motor.

Recommended Action:

1. Check the mounting of the stepper motor and the cabling to it.
2. Operate the stepper motor in self-test mode if not cycling.
3. Replace the stepper motor.

3.2.39 Drive is Overheating -- (A7H)

Causes:

1. Airflow is blocked.
2. System fans are inoperative.
3. Thermal sensor is bad.

Recommended Action:

1. Remove air flow blockage.
2. Troubleshoot system fan problem.

3.2.40 BOT Sensor Error -- (A8H)

There is no current in the BOT/EOT sensor/assembly.

Causes:

1. Cable is unplugged.
2. BOT/EOT sensor is faulty.
3. LED driver/sense circuit is bad.

Recommended Action:

1. Check cable, replace if necessary.
2. Replace the BOT/EOT Sensor.
3. Replace the drive board.

3.2.41 No Hall Switch Signals -- (A9H)

The microprocessor on the drive board does not receive hall switch signals from motor A.

Causes:

1. There is a problem with the cable connection between motor A (supply) and the 8751 microprocessor.
2. Motor A is bad.

Recommended Action:

1. Inspect and/or repair cable connections if necessary.
2. Reseat the 8751 microprocessor in its socket.
3. Replace the supply reel motor.

3.2.42 No Tachometer Pulses Present -- (AAH)

The tachometer does not produce tachometer pulses while the tape is moving, as sensed by the motor A hall switches.

Causes:

1. The cable connection is bad, plugged in incorrectly.
2. Tachometer is bad.
3. Comparator in drive board is bad.
4. Pulley seized on bearings.

Recommended Action:

1. Inspect the cabling. Check to be sure that plugs are in the right place.
2. Reseat the 8751 microprocessor in its socket.
3. Replace the tachometer.
4. Replace the drive board.

3.3 SUBASSEMBLY REMOVE/REPLACE PROCEDURES

The following subsections provide instructions for removing subassemblies that fail. To replace a subassembly, reverse the removal procedure.

The following procedures assume that the drive has already been removed from the host system, that all cables have been disconnected, and that the cartridge has been removed.

NOTE

While performing the removal procedures, refer to the annotated exploded view drawing of the TK50 Tape Drive in Appendix A. Also required are the manufacturing tools, jigs, and procedures used to build a TK50.

3.3.1 Drive Board Removal

1. Remove the four 6-32 x 1/2 inch panhead screws on the bottom of the drive, holding the skid plate on.
2. Remove two 6-32 x 1/4 inch panhead screws holding the drive board.
3. Stand the drive on its front bezel with the drive board oriented up and down.
4. Disconnect read/write head connectors J8 and J9.
5. Disconnect J106 (tachometer and EOT/BOT connectors).
6. Disconnect J6 (handle down switch connector, stepper motor and head sensor).
7. Disconnect J100 (connectors for motors A and B).
8. Disconnect J103 (LED and load switch connector).
9. Swing the drive board out and pull gently to unseat it from its snap mounts.

3.3.2 Front Bezel Removal

1. Trip the interposer. The interposer only moves easily in one direction.

2. While holding the interposer, lift the cartridge release handle.

CAUTION
Do not force the handle up. Lift the handle gently while holding the white interposer in the "tripped" position.

3. Remove the two 6-32 x 1/4 inch screws that are visible under the handle after it has been lifted up.

4. Unsnap the locks and remove the bezel by pulling it straight out.

CAUTION
Don't pull it out too far until you've unplugged the connectors.

5. Unplug connectors J103 and J17.

3.3.3 Read/Write Head Bracket Assembly Removal

1. Remove the skid plate, then loosen the two screws holding the drive board.

2. Disconnect connectors J8 and J9.

3. Pull the grommets up through the edges of the casting (be careful of the rear one because the EOT/BOT assembly wires are underneath it).

4. Remove the quarter cover.

5. Remove the leader by retracting the link arm and pulling out the plastic leader.

6. Remove the springs from their connections on the read/write head.

7. Slide the head up and off the mount.

3.3.4 Tachometer Removal

Pre-conditions for Tachometer Removal

1. Remove the quarter enclosure.

2. Remove the read/write head.

Tachometer Removal

1. Disconnect connector J10. **NOTE PLACEMENT OF CONNECTORS.** There are two double connectors with red and green wires. Place them in the same position when reassembling.

2. Remove two 6-32 x 5/8 inch panhead screws (holding the EOT/BOT assembly).

3. Remove a 6-32 x 3/4 inch panhead screw that holds a small silver plate in place.

4. Lift off the tachometer assembly.

3.3.5 Solenoid/Interposer Removal

1. Disconnect J103 (pins 1, 2, and 3).

2. Disconnect connector J100 (pins 21 and 22).

3. Snap out the top white piece of the interposer.

4. Pull the interposer up and out. Be careful to watch for small springs.

5. Pull the solenoid up and out.

When replacing the solenoid and interposer, they should snap back into place without being forced, and should move freely on its pivot.

3.3.6 Take-up Motor (Motor A) Removal

Preconditions for Take-up Motor Removal

1. Remove the skid plate covering the drive board.

2. Remove the drive board.

3. Remove the quarter enclosure.

4. Remove the tape leader.

Take-up Motor Removal

1. Remove the take-up reel by unscrewing the screw at its top. Take care because there are several parts holding in the take-up reel, including small spring washers.

2. Remove the plastic tape constraint. The tape constraint is snap fitted in place, but can be removed by inserting a screwdriver under one corner.

3. Turn the tape drive metal casting over.

4. Remove three 6-32 x 5/8 inch panhead screws. Take care that the screws don't fall inside the motor due to its magnet.

3.3.7 Stepper Motor Removal

Preconditions for Stepper Motor Removal

1. Remove the skid plate covering the drive board.

2. Remove the drive board.

3. Remove the quarter enclosure.

4. Remove the tape take-up leader.

Stepper Motor Removal

1. The stepper motor can be removed by removing two 6-32 x 5/16 inch panhead screws.

> **CAUTION:**
> **The small plate under the stepper motor is a magnetic shield. It must be in place when the stepper is replaced, or the stepper motor will interfere with read/write operations, due to its coil windings.**

3.3.8 Heat Sensor Removal

Preconditions for Heat Sensor Removal

1. Remove the skid plate covering the drive board.

2. Remove the drive board.

Heat Sensor Removal

1. Remove the two 6-32 x 1/2 inch panhead screws to remove the heat sensor.

3.3.9 Supply Motor Removal

Preconditions for Supply Motor Removal

1. Receiver assembly must be removed.
2. Remove the skid plate covering the drive board.
3. Remove the drive board.

Supply Motor Removal

1. Remove the three panhead screws that hold the motor in place.
2. Lift the motor out.

CAUTION

See the manufacturing procedure for building a TK50 Tape Drive when trying to re-install the supply motor. There are some close tolerances that must be observed and which may require special shims.

3.3.10 Receiver Assembly Removal

1. Remove the front bezel (see Section 3.3.2)
2. Put the handle back down.
3. Remove springs (how many, what kind).
4. Remove four screws.
5. Feed connectors up through the holes.
6. Make sure that the springs are put back in the correct places when replacing the receiver assembly.

CHAPTER 4
TQK50 CONTROLLER THEORY OF OPERATION

4.1 GENERAL

This chapter details the TK50 Subsystem Q-bus TMSCP controller (module M7546).

The TK50 M7546 controller is a standard size (8 X 5.5 inch) dual-height printed circuit board that connects a TK50 Tape Drive to the Q22 Bus. The main functional element on the controller is the 80186 microprocessor. The board also contains the following hardware.

1. Two 27128 16K ROMs
2. Two 6264 8K RAMs
3. One 82S105 Field Programmable Logic Sequencer (FPLS)
4. One 7201 Multi-Protocol Serial Communications Chip (MPSC)
5. Q-bus Drivers and Receivers
6. Tape Drive Interface Drivers and Receivers

NOTE

The M7546 controller operates on the Q-bus under the control of the Tape Mass Storage Control Protocol (TMSCP). It is not the purpose of this manual to document TMSCP operations. Since all Q-bus activity with respect to this controller (during normal operation) is under TMSCP control, you will find several instances of the phrase "the controller responds as TMSCP requires." Usually, this phrase indicates that for more information about exactly what happens in an operating environment, you should refer to the TMSCP specification. In many cases, problems with this board are diagnosed and fixed in an environment not associated with TMSCP. Therefore, ONLY hardware operations have been detailed in this manual. For example, when the controller is communicating over the Q-bus, this book explains the DMA sequencing operations involved, as well as explaining how the internal circuitry functions so the controller can work on the Q-bus. However, data and command packets, response rings, and other specific TMSCP constraints are not discussed.

There are six main functional blocks on the M7546 controller (Figures 4-1 and A-1).

1. 80186 Processor
2. Memory (ROM and RAM)
3. Miscellaneous Control and Status Registers
4. Q22 Bus Interface and Control Circuitry
5. Drive Interface and Control Circuitry
6. Diagnostic Hardware

The 80186 microprocessor (with two DMA channels) is connected to the 7201 MPSC chip. One DMA channel is used for write operations to the tape, the other for read operations. The 80186 also has three timer/counters and two external interrupts that control two on-board Programmable Array Logic (PAL) chips and the 82S105 FPLS. The PALs and the FPLS handle data transfer to and from the Q-bus.

Following is a functional/technical description of the M7546 Q/TMSCP controller. Refer to the Field Service Print Set (MP-2055-CS) when reading this chapter.

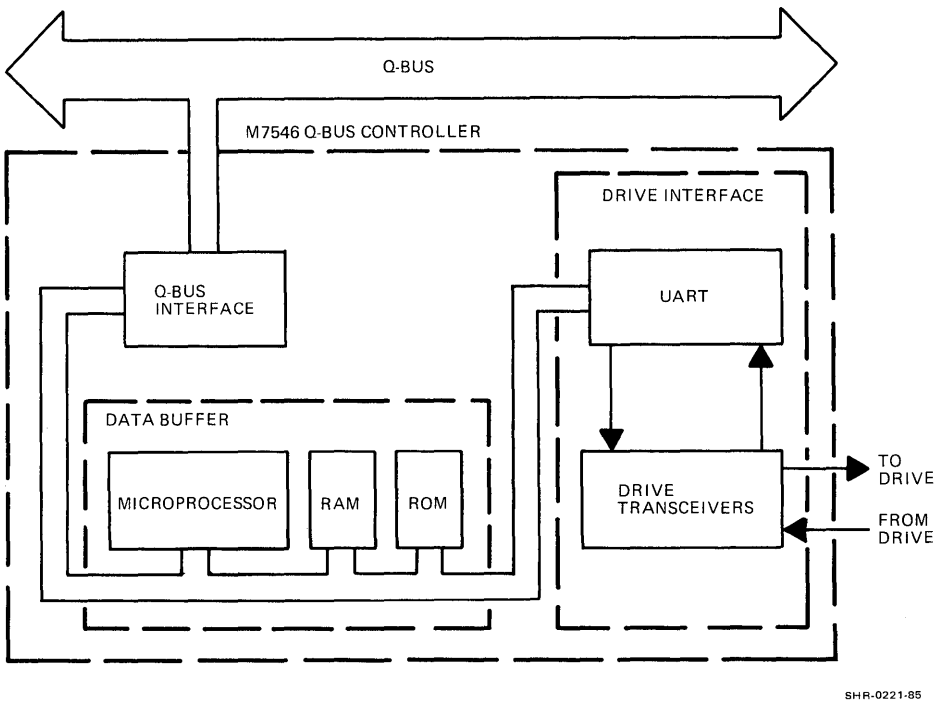


Figure 4-1 TQK50 High Level Block Diagram

4.2 THE 80186 MICROPROCESSOR

This section details the main engine of the M7546 Q-bus controller -- the 80186 Microprocessor.

4.2.1 Power-up Reset

When the controller is powered-up, the 80186 is reset through assertion of the Reset signal, which is connected to pin 24 of the 80186. The reset line must be asserted for a minimum of four clock cycles, after the dc power has stabilized, to insure proper operation.

The signal MTC2 RESET H is asserted when either -BDCOK L or -BINIT L from the backplane (CPU signals) are a logic level 0 (2-A7). MTC2 RESET H resets the 74LS74 flip-flop at E5 (5-B3) to generate MTC5 MICRO RESET H and -MTC5 MICRO RESET L. MTC5 MICRO RESET L is the signal that is connected to pin 24 of the 80186 (2-B7).

MTC5 RESET COUNT L, from the 74LS00 at E6 (5-A4) and MTC5 MICRO RESET H together let the 74LS161 counter (E1) (5-B4) begin counting. The counter counts up to 4 (which resets the FPLS that handles Q-bus interfacing) and then up to 8, which sets the D input of E5 to a logic 1. On the next count, E5 is set (MTC5 MICRO RESET H is de-asserted), and the counter is disabled.

At this point, both the 80186 and the FPLS are reset and begin executing code.

The same counter reset circuitry is used when the host CPU executes a "Write IP Register." The reset of the board whenever the CPU writes to the IP register is part of the U/Q Port Protocol (see the U/Q Port Protocol Specifications).

The rest of the circuitry on the board is reset when the 80186 generates a reset from its pin 57. This Reset signal is inverted and driven to the rest of the board by the 7414 at E36 (2-A6) to become MTC2 INIT L.

4.2.2 Microprocessor Cycle Time

The processor cycle time is derived from the 12 MHz crystal oscillator (E37) that is inverted and driven by the 7414 at E36 (2-D6). MTC2 CLK H connects to pin 59 of the 80186. The 80186 divides this 12 MHz clock by two to generate MTC2 CLK/2 H. This 6 MHz signal is the processor's clock rate and equates to 166 ns per clock.

A bus cycle is 664 ns in duration (four 80186 clock periods). Under certain conditions, a bus cycle can take more than four clock periods. Refer to the 1983 Intel Microprocessor and Peripheral Handbook.

4.2.3 Memory Chip Select Lines

The 80186 uses an internal memory select unit, which is programmed when power is applied. This memory select unit asserts the appropriate chip select lines for the memory addresses used by the controller. These memory select lines access the on-board ROM and RAM, as well as a 64K byte block of Q-bus memory.

The Upper Chip Select (UCS) line (80186 pin 34) accesses the 27128 EPROMs E28 and E29 (3-A6, C6), which are the upper 32K bytes of address space (F8000-FFFFF). The 80186 address lines AD0-AD15 access a particular location within the selected 64K byte block.

The Lower Chip Select (LCS) line (80186 pin 33) accesses the 6264 RAMs [E20 and E21 (2-A2, C2)], which are the lower 16K bytes of address space (00000-03FFF).

The Middle Chip Select Line 0 (MCS0) signal enables reads and writes to the Q-bus memory. The controller accesses a 64K byte block of Q-bus memory. Since the entire MCS block in the 80186 can access 256K bytes of memory, each MCS line is able to access 64K bytes. MCS0 enables access to 64K bytes, beginning on a 64K byte boundary (40000-4FFFF).

The M7546 controller does not use MCS1-MCS3.

4.2.4 Peripheral Chip Select Lines

In addition to the memory select unit, the 80186 also uses a peripheral chip select unit. The 80186 has seven peripheral chip select lines that it uses to access external peripheral devices such as the 7201 MPSC chip, serial ports, and various registers.

The peripheral chip select lines are memory mapped on the M7546 for fast interrupt servicing. The memory mapped locations for these lines follow.

PCS0	F800-F87F
PCS1	F880-F8FF
PCS2	F900-F97F
PCS3	F980-F9FF
PCS4	FA00-FA7F
PCS5	FA80-FAFF
PCS6	FB00-FB7F

The 80186 first addresses lines AD0-AD15, then accesses a particular location or locations, within the 128-byte range of a PCSX line, to address a particular register. This addressed register may be a register consisting of discrete components on the board, such as the Miscellaneous Control Register, or one of the programmable registers within a device such as the MPSC.

The Peripheral Chip Select Lines are assigned as follows:

PCS0	Reserved.
PCS1*	Enable 7201 MPSC chip.
PCS2	Enable Q22 bus register loading.
PCS3	Enable SA register writes and reads; terminate Q-bus transfers.
PCS4	Enable writes to vector register; Enable reads from hardware revision level register; Reset FPLS interrupts after a Q-bus error.
PCS5	Enable Miscellaneous Control Register for writes; Enable Miscellaneous Status Register for reads
PCS6*	Enable 7201 MPSC Chip (DMA Acknowledge)

4.2.5 Interrupts

The 80186 uses two types of interrupts: internal and external. Internal interrupts occur when a terminal count is reached during a DMA transfer, or when a counter/timer maximum count has been reached.

There are two external interrupts serviced by the 80186. The 7201 MPSC chip can interrupt the 80186 when communicating with the tape drive. The FPLS can interrupt the 80186 to alert it of a Q-bus transfer error (for example, a Q-bus memory parity error).

4.2.5.1 MPSC Interrupts -- The MPSC interrupt line is connected to pin 44 of the 80186 (INT1). The 80186 acknowledges this interrupt by asserting INT3 (pin 41). The 80186 is configured in cascade mode, so that it gives two interrupt acknowledges (INTAS) to the MPSC chip. The first INTA from the 80186 acknowledges receipt of the interrupt and informs the MPSC that the interrupt is being serviced. The second INTA pulse from the 80186 tells the MPSC to place its interrupt vector on the internal data bus.

4.2.5.2 FPLS Interrupts -- The FPLS interrupt to the 80186 is not responded to with an INTA. Instead, the 80186 responds to this interrupt by asserting PCS4 (MTC2 ENB VEC REG L). PCS4 performs two functions:

1. It resets the memory parity error flip-flop at E2 (5-A7) to inform the system that a Q-bus error occurred.

2. It resets FPLS interrupts.

The 80186 also interrupts the host CPU and puts the vector on the Q-bus. It asserts pin 19 of E19 (6-B5). E19 is connected to the DC003 on page 5 (E27)(5-A1).

---

* PCS1 and PCS6 are logically ANDed for an MPSC enable so that assertion of both lines enables the MPSC.

4.2.5.3 Non-Maskable Interrupt (NMI) -- The 80186 accepts a non-maskable interrupt on pin 46. This pin monitors BPOK (BB1 on the backplane). This signal is an early indication that power is going down, and alerts the 80186 to take the proper steps to power-down cleanly.

4.2.6 DMA Operations

4.2.6.1 DMA Write -- The 80186 has two DMA channels to which DMA request lines are connected from the 7201 MPSC chip (E4, 7-CA). Each time the MPSC chip requests data to write on the tape, the 80186 moves the data from RAM to the MPSC, a byte at a time, until a terminal count is reached. The terminal count is pre-programmed into the DMA controller in the peripheral control block of the 80186. The MPSC asserts the signal MTC7 WR DRQ H through the 74LS74 at E5 (7-C2) and the 74S11 gate at E17. MTC7 WR DRQ H connects to the DMA write request pin of the 80186 (pin 18). DMA HAI clears the flop and the request.

4.2.6.2 DMA Read -- The MPSC chip alerts the 80186 that it has a byte of data to be read by asserting the MTC7 RD DRQ H signal through the 74LS74 at E2 (7-D2) and the 74LS11 at E17. The DMA controller in the 80186 transfers the data, a byte at a time, to RAM until a DMA terminal count is reached. DMA HAI clears the flip-flop and the request.

4.3 MEMORY

This section details the memory (RAM and EPROM) that is contained on the M7546 Q-bus controller.

4.3.1 EPROM

The M7546 controller contains two EPROMs (E28 and E29, 3-C7 and B7) that make up its 32K bytes of read only memory. The 80186 accesses this ROM space through two 74LS373 address latches at E52 and E57 (2-C4 and B4).

The 80186 signal labeled MTC2 ALE H (Address Latch Enable) latches address lines 0 -- 14, as well as -HIGH BYTE ENB H (Byte High Enable) into the 74LS373 latches at E52 and E57 (2-A4, B4). Byte High Enable, in conjunction with Address Line 0 (ADR0), enables either a 16-bit word or an 8-bit byte to be read from the ROMs. For a byte-wide access, either the high or low byte may be chosen. See the following chart.

	HIGH BYTE ENB L	MTC2 AD0 H	
Word access enabled	0	0	E28,29
High byte access	0	1	E28 enabled
Low byte access	1	0	E29 enabled
No access	1	1	

4.3.2 Data Transceivers

The 80186 reads data from the ROM area through the transceivers at E33 and E46 (2-A2, C2). It enables the transceivers in the receive direction by setting the signal -MTC2 DTR H to a logic 0. In this way, the 80186 can read and execute the microcode resident in the ROMs, via MTC2 AD0-MTC2 AD15 H.

When the 80186 wants to output data to other devices (for example, the MPSC chip), it sets -MTC2 DTR H to a logic level 1, then outputs MTC2 AD0 H through MTC2 AD15 H. The data is then transmitted out the transceivers at E33 and E46.

There is one other condition necessary for the 80186 to transmit and receive data through the transceivers: pin 19 of the transceivers must be a logic level 0. The 80186 can enable the transceivers by setting the signal MTC2 DEN L to a logic level 0. Under normal circumstances, this sets the enable pin of the transceivers to a logic 0 and enables a data transfer. However, if a Q-bus memory access or a write or read of the SA register is in progress, the transceivers cannot be enabled. The 74LS00 gate at E30 (2-A3) outputs a logic 1 if either of the above conditions is true. Therefore, the 74LS32 at E47 is not able to output the logic 0 necessary to enable the transceivers, even if the 80186 sets MTC2 DEN L to a logic 0. In this way, internal bus contention problems are avoided. For a summary of the conditions necessary for enabling data in either direction through the transceivers, see the following charts. All enable signals in the charts are the signals from the 80186, before buffering or gating.

80186 Read Through Transceivers

```
-MTC2 DTR H = 0
 MTC2 DEN L = 0
 MTC2 ENB SA REG L = 1
 MTC2 ENB QBUS MEM L = 1
```

80186 Write Through Transceivers

```
-MTC2 DTR H = 1
 MTC2 DEN L = 0
 MTC2 ENB SA REG L = 1
 MTC2 ENB QBUS MEM L = 1
```

4.3.3 RAM

The M7546 controller's RAM area consists of two 6264 RAM chips, located at E20 and E21 (2-D2, B2). Logically, the RAM area is at addresses 00000-03FFF.

Write and read operations to and from the on-board RAM use the same data path through the transceivers as a ROM read, except that the 80186 asserts its pin 33 (MTC2 ENB RAM L) rather than pin 34 (MTC2 ENB ROM L). Byte high enable and address line 0 determine high-byte, low byte, or word-wide access from the RAM exactly the same way as they do for ROM read operations.

The signal MTC2 WR L from the 80186 is used to write to the RAMs.

4.4 CONTROL AND STATUS REGISTERS

This section details two of the I/O Registers used by the 80186 microprocessor to perform part of its functions.

4.4.1 Miscellaneous Control Register

This register is a 74LS259 8-bit addressable latch located at E35 (4-C6).

The output bits associated with this latch perform various functions on the controller. This section lists and describes those functions.

The 80186 can set or reset any of the bits in the latch, by setting a combination of ADR 1 -- ADR 3, accessing an address in the range of PCS5 (FA80-FAFF), then either asserting (to set) or negating (to reset) DAT0. Table 4-1 lists the addresses of each bit in the Miscellaneous Control Register, and the subsections following the Table describe each function.

Table 4-1 Miscellaneous Control Register Bit Assignments

Address	Latch-Bit Function	MTC2 ADR3 H-MTC2 ADRlH
FA80	Drive erase	000
FA82	Drive write gate	001
FA84	Enable gap detect	010
FA86	Clear SA initialization	011
FA88	Clear IP initialization	100
FA8A	Diagnostic mode	101
FA8C	Reset LED 1	110
FA8E	Reset LED 2	111

4.4.1.1 Drive Erase (High True) -- Drive erase signals the drive to start an erase operation on the tape. The purpose of the erase is to put gaps between data blocks on the tape. Erase works only if Drive Write Gate is also set, and the tape cartridge is not write protected. If the tape cartridge is write protected, the drive returns an error message to the controller that informs it of the write protected condition.

The signal MTC4 DRV Erase H, from the 74LS259 latch at E35 (4-D6) connects to the 26LS31 quad differential transmitter at E25 (7-B2). The quad transmitter drives the signal out the interface cable to the drive.

4.4.1.2 Drive Write Gate (High True) -- Drive write gate signals the drive to start writing to the tape. Drive write gate must be asserted to perform an erase or write operation. If the tape cartridge is write protected, and a write operation is tried, the drive returns an error message to the controller. As with drive erase, the signal is driven by the 26LS31 differential transmitter at E25.

4.4.1.3 Enable Gap Detect (High True) -- Enable gap detect connects to pins one and two of the 74LS164 shift register at E10 (7-D6). Each time a drive write clock (DRIVE WR CLK H) occurs, the shift register shifts another position. Either one of two conditions clear the shift register: a reset (MTC2 INIT L); or the occurrence of a Drive Read Clock.

If neither clear condition occurs, the shift register continues shifting until it reaches an 8 count. At the eighth count, it clocks the gap detect flip-flop at E11, which causes pin 9 to toggle. The transition of 1 to 0 or 0 to 1 on pin 6 of the MPSC (which is connected to the gap detect flip-flop) causes the MPSC to issue an interrupt to the 80186. The interrupt signals the 80186 that a gap on the tape has been detected.

Note the 74LS157 multiplexer at E12 (7-C6). This MUX lets a diagnostic signal clock the shift register for diagnostic checking of the MPSC and Gap Detect circuitry. See Section 4.7 for a detailed explanation of on-board diagnostic hardware.

4.4.1.4 Clear SA Initialization (High True) -- The CLR SA INIT signal clears the flag indicating that the CPU has written to the SA register. The flag is set in the PAL at E40 (5-B7) -- pin 12. The 80186 continually monitors this flag in a polling loop. Once it detects that the flag has been set, it clears the flag by asserting CLEAR SA INIT (connected to pin 8 of the PAL). The 80186 then executes the appropriate response to the WRITE SA REG command from the CPU, according to TMSCP protocol. The Flag is set under the following conditions.

1. MATCH address from DC005 transceiver is asserted.
2. TS DAL 1 is set.
3. RSYNC is set.
4. RDOUT is set.

The combination of the above signals decodes as a WRITE SA REG from the CPU according to the Digital standard for Q-bus interfacing. It sets the SA WR INIT flag at pin 15 of the PAL.

4.4.1.5 Clear IP Initialization (High True) -- Clear IP Initialization clears the flag (PAL at E40, pin 14), indicating that the CPU has read the IP Register. The 80186 continually monitors the flag in a polling loop. Once the 80186 detects that the flag has been set, it executes an appropriate response that TMSCP requires. The following conditions result in the flag being set in the PAL.

1. MATCH address from DC005 transceiver is asserted.
2. TS DAL 1 is not set.
3. RSYNC is set.
4. RDIN is set.

The combination of those signals decodes as a read from the IP register according to the Digital standard for Q-bus interfacing.

4.4.1.6 Diagnostic Mode (High True) -- This bit, when set, enables the loopback diagnostic MUX at E12 (7-C6) and disables the 26LS31 drive differential transmitter at E25 (7-B2). With the diagnostic MUX enabled, diagnostic tests can be run that check out the Gap Detect circuitry and the MPSC chip. With the transmitter at E25 disabled, no commands or data reach the drive.

4.4.1.7 Reset LED 1 (High True) -- On power-up, the 74LS259 addressable latch is reset, which turns on LED 1. After the power-up diagnostics have completed, this signal turns off the LED.

4.4.1.8 Reset LED 2 (High True) -- On power-up, the 74LS259 addressable latch is reset, which turns on LED 2. After the TMSCP port has gone through its four step initialization process, this signal turns off the LED. This indicates that the board is fully functional.

4.4.2 Unit Number and Status Register

E24, E32, and E41 on page 4 of the schematics make up a 16-bit buffer that is enabled by the signals RD and ENB MISC REG. ENB MISC REG is peripheral chip select line 5 (PCS5) from the 80186. The Unit Number and Status Register provides a TMSCP unit number for the controller, as set in the switch pack at E31; as well as eight status bits that reflect the status of the controller. The assigned bits in the Unit Number and Status Register are listed in the following chart, and detailed in the following subsections.

```
DATA0                   SA write initialization
DATA1                   IP read initialization
DATA2                   Drive erase
DATA3                   Drive write gate
DATA4                   Q-bus interrupt request
DATA5                   Q-bus interrupt request done
DATA6                   Q-bus memory parity error
DATA7                   Drive cable in

DATA8-------------------LSB
DATA9
DATA10
DATA11         ---------TMSCP
DATA12                  Unit number
DATA13
DATA14
DATA15------------------MSB
```

4.4.2.1 SA Write Initialization (High True) -- DATA0 -- This bit is a flag that indicates to the 80186 that the U/Q Port Protocol has written to the SA Register and that the controller should respond as TMSCP requires.

4.4.2.2 IP Read Initialization (High True) -- DATA1 -- This bit is a flag that indicates to the 80186 that the U/Q Port has read the IP Register and that the controller should poll the command rings in CPU memory as TMSCP requires.

4.4.2.3 Drive Erase (Low True) -- DATA2 -- This bit is for diagnostic use. It determines whether the 80186 can set and reset the Drive Erase signal through the drive erase circuitry. The 80186 generates this signal through the Miscellaneous Control register and reads it back through the Unit Number and Status register.

4.4.2.4 Drive Write Gate (Low True) -- DATA3 -- The 80186 generates this signal through the Miscellaneous Control register already explained. The read back capability through the Unit Number and Status register is for diagnostic purposes, to check that the 80186 can set and reset the bit.

4.4.2.5 Q-bus Interrupt Request (Low True) -- DATA4 -- A diagnostic loopback signal that lets the 80186 check that it can set and reset its Q-bus Interrupt Request (Host CPU Interrupt Request) through the Q22 Bus register.

4.4.2.6 Q-bus Interrupt Request Done (Low True) -- DATA5 -- This bit indicates to the 80186 that its Q-bus interrupt request has been serviced and that the host has read the interrupt vector into the CPU.

4.4.2.7 Q-bus Memory Parity Error (Low True) -- DATA6 -- This flag indicates to the 80186 that a parity error occurred during a Q-bus memory transfer, and that the 80186 should transfer the data block again.

4.4.2.8 Drive Cable In (High True) -- DATA7 -- This signal indicates to the 80186 that the cable to the drive is connected.

4.4.2.9 Unit Number (High True) -- DATA8-DATA15 -- These eight lines are connected to switch pack E31. The user can set the switches to reflect a unit number for each controller board in a system, per TMSCP. The 80186 reads the Unit Number and Status register bits DATA8-DATA15, and returns the information to the host CPU via TMSCP.

4.4.3 Vector Register (High True)

The Vector register is a 16-bit register that consists of E50 and E56 (74LS646 bi-directional 8-bit registers) (6-A7, C7). This register is a multi-function register, and serves as the Vector register, the SA register, and the DMA Data register. This section details the functions of the Vector register only.

The 80186 loads the Vector register with the Q-bus Interrupt Vector. The value of the vector address is loaded by the U/Q Port Protocol on initialization (TS DAL0-TSDAL15). When the controller interrupts the host CPU, the host enables the interrupt vector onto the Q-bus at the appropriate time, as required by the U/Q Port Protocol.

The register is loaded and enabled through the PAL at E45 (6-D5) of the schematics. The PAL decodes the signals WR and ENB SA REG to generate the signal CLK A, which loads the register with the vector. To enable the vector onto the Q-bus, the signal Vector is decoded, which generates the signal ENA from the PAL. This signal is connected to the Vector register, and is the Enable signal that lets the vector be placed on the Q-bus.

4.4.4 Hardware Revision Register (High True)

This register, which is a buffer for the 80186 bus, lets the 80186 read switch pack E38 (4-C7). The switch pack is set at the factory and reflects the hardware revision level of the controller, as required by TMSCP. The Hardware Revision Level register consists of two 74LS240 drivers at E32 and E41. The following chart shows the relationship of the switch pack to the 80186 data bus.

DATA0	SW1	LSB
DATA1	SW2	
DATA2	SW3	
DATA3	SW4	
DATA4	SW5	
DATA5	SW6	
DATA6	SW7	
DATA7	SW8	MSB

4.4.5 SA Register

The SA register is part of the U/Q Port Protocol, and is used to initialize the controller and return status to the host CPU.

To initialize the controller, the U/Q Port Protocol uses the SA register to send the vector address, command and response ring address, and to inform the controller how long the rings are.

The SA register consists of the two 8-bit multifunction chips at E50 and E56 (6-C7, B7). These two registers also make up the Vector register discussed in Section 4.4.3, and the DMA Data Register (Section 4.5.5.2)

The PAL at E45 controls SA register loading and enabling, as it does the vector register. The SA register is a bi-directional, latched register. It consists of two sets of registers: one loaded and enabled in one direction, and one loaded and enabled in the other direction. This configuration allows the 80186 to write to one register, which the Q-bus can read; and lets the Q-bus write to the other register, which the 80186 can read.

The 80186 writes to the SA register by generating the signals ENB SA REG and WR, which the PAL at E45 decodes to generate CLK A. CLK A enables the 80186 to write data to the SA register. The 80186 reads the SA register by generating the signals ENB SA REG and RD, which the PAL decodes to generate ENA and DIR. ENA and DIR enable the contents of the SA register onto the 80186's data bus.

The following sequence occurs when the CPU writes to the controller's SA register.

1. PAL at E40 (sheet 5) decodes MATCH, TS DAL, RSYNC, and RDOUT to generate WR SA REG.

2. PAL at E45 decodes WR SA REG to generate CLK B.

3. CLK B enables the host CPU to write to the SA register.

The combination of MATCH, TS DAL, RSYNC, and RDOUT generates WR SA REG through the PAL at E40 (5-B7). The 80186 monitors the signal SA WR INIT continually in a polling loop. When the 80186 finds this flag set, it responds as required by TMSCP.

The following occurs when the CPU reads the controller's SA register.

1. The PAL at E40 (5-87) decodes MATCH, TS DAL 1, RSYNC, and RDIN to generate RD SA REG.

2. The PAL at E45 (6-D5) decodes RD SA REG to generate the signals ENA and DIR.

3. ENA and DIR enable the contents of the SA register onto the Q-bus transceivers at E44, E49 (1-B2, D2), E53, and E54 (1-B4, D4). INIT SA RD from the PAL at E45 enables the data through the transceivers to the host CPU.

The combination of MATCH, TS DAL 1, RSYNC and RDIN are decoded by the PAL at E40 to generate RD SA REG.

After power-up or after a WRITE IP REGISTER command, the SA register always contains zero. The CPU reads zero from the SA register until the 80186 has loaded it with the correct value. This prohibition is accomplished by keeping the INIT SA RD signal low to disable the DC005 transmitters (E44, E49, E53, and E54) from transmitting data onto the Q-bus.

For further information about the SA register, refer to the U/Q Port Protocol Specification.

4.4.6 IP Register

Logically, the IP register is part of the TMSC Protocol. Physically, however, it is not a register on the M7546 Controller. The 80186 must only decode whether the host CPU has written to or read from the IP Register I/O Location, and then respond as TMSCP requires.

The PAL at E40 on page 5 of the schematics decodes the signals MATCH, TS DAL de-asserted, and RSYNC to generate the signal IP REG SEL.

The following sequence occurs when the host CPU reads the IP Register.

1. The signals RDIN and IP REG SEL generate the flag IP RD INIT, which the 80186 can read through the Miscellaneous Control register E41 (4-C6)). The 80186 then takes the appropriate steps as required by the U/Q Port Protocol, after detection of the flag.

2. The flag stays set until the 80186 clears it through assertion of the signal CLR IP INIT, generated through the Miscellaneous Control register E35 (4-D6).

The following sequence occurs during a CPU write to the IP register.

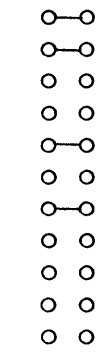
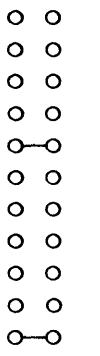
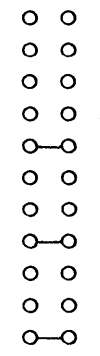
1. The signals IP REG SEL and RDOUT are used to set the power-up reset circuitry to initialize the controller, as part of the U/Q Port Protocol.

For further information about the IP register, refer to the U/Q Port Protocol Specification.

4.4.7 Module Starting Addresses/Interrupt Vectors

Any M7546 module you install must be set to the correct starting address and interrupt vector. The interrupt vector (260) is under program control and does not need to be set. The starting address of the first TK50 module installed in a system is fixed at 1774500. Table 4-2 lists the jumper setting for the first M7546 modules.

Table 4-2 Common Jumper Pack Settings

774500	7760404	7760444
		
Unit Number 0	Unit Number 1	Unit Number 2

The starting address of any additional TQK50 modules installed in your system is a floating address of 17760nnn and is set using the jumpers. The floating address of the M7546 module starts at 17760404 and increments by 4; for example 17760404, 17760410, 17760414. Table 4-4 shows the floating CSR address of some common combinations of devices that require configuration.

Check off all the devices in the system you want to reconfigure and find the column in Table 4-4 that makes the best match. In most cases, if you do not install a device listed in the middle of the column, the addresses of the devices that follow changes. Observe the following rules.

1. Check each module installed in the system.

2. Find the column that corresponds to all the installed modules, where:

   Number = installed
   *number = may be installed or not.

   NOTE
   When an address is preceded by an *, the address of the following device(s) does not change.

3. Assign the floating CSR address according to the numbers shown in Table 4-4. The numbers are the last three digits of the address for the module.

Use Table 4-3 to determine the starting address of modules that may be installed in your system.

Table 4-3 Address/Vector Worksheet

Option	Module	Check Unit Number	If In System	Vector	CSR Address (N=177)
KDJ11-BC	M8190	1	X	--	--
MSV11-PL	M8067	1	X	--	N72100 start address=0
MSV11-PL	M8067	2		--	N72102 start address=512
MSV11-PL	M8067	3		--	N72104 start address=1024
MSV11-PL	M8067	4		--	N72106 start address=1536
DEQNA	M7504	1		120	N74440
DPV11	M8020	1		V	F
DRV11-JP	M8049	1		V	N64120
DRV11-JP	M8049	2		V	N64140
DRV11-B	N7950	1		124	N72410
DRV11-B	M7950	2		V	N72420
LPV11	M8027	1		200	N77514
DLVE1	M8017	1		V	N75610
DLVJ1	M8043	1		V	N76500
DLVJ1	M8043	2		V	N76510
DZV11	M7957	1		V	F
DHV11	M3104	1		V	F
DMV11-CP	M8064	1		V	F
DUV11	M7951	1		V	N60040
TQK25	M7605	1		224	N72520
TQK50	M7546	1		260	N74500
TQK50	M7546	2		V*	N60404
KLESI-QA	M7740	1		154	N72150
RLV12	M8061	1		160	N74400
RQDX1,2	M8639	1		154	N72150

* The vector for additional TQK50 modules becomes a floating vector and is set under program control.

NOTE

If a module has a floating vector and CSR address, additional modules of the same type also have a floating vector and CSR address.

Substitute the numbers in Table 4-4 for the nnn in address 1776nnn to find the floating CSR address for a second TQK50 module.

Table 4-4 Floating CSR Address Chart

Option	Common Configurations							
DZQ/V 1				100	100	100	100	100
DZQ/V 2				*100	*100	100	100	100
DZQ/V 3				*120		120		120
DPV11	*270	*270	*270		*310	*330	*310	*330
DMV11			320				340	360
Second MSCP		334	*354		354	374	374	414
Second TK50	*404	*444	*444	*444		*504	*504	504
DHV11	440	500	500	500	500	540	540	
DHV11	460	520	520	520	520			

If the system you want to configure does not resemble the common configurations shown in Table 4-4, refer to the following list for information. See also your system technical manual; Configuration Chapter.

- The first DUV11 CSR address is 17760040.
- The first DZV11 CSR address is 17760100 is no DUV11s are present.
- The first DPV11 CSR address is 17760270 if no DUV11s or DZV11s are present.
- The first DMV11 CSR address is 17760320 if no DUV11s, DZV11s, or DPV11s are present.
- The first disk MSCP CSR address is always 17772150.
- The second disk MSCP CSR address is 17760334 if no DUV11s, DZV11s, DPV11s, or DMV11s are present.
- The first tape MSCP CSR address is always 17774500.

- The second tape MSCP CSR address is 17760404 if no DUV11s, DZV11s, DPV11s, or DMV11s are present and no more than one disk MSCP is present.

- The first DHV11 CSR address is 17760440 if no DUV11s, DZV11s, DPV11s, or DMV11s are present and no more than one disk MSCP is present and no more than one tape MSCP is present.

4.4.8 Unit Number DIP Switch

The unit number DIP switch must be set to correspond to the jumper setting. The first setting in Tables 4-5 and 4-2 shows the factory switch setting that matches the jumper setting for a starting address of 17774500. The remaining settings show the DIP switch setting for additional modules set for a starting address of 17760nnn (second device) and 17760nnn (third device) respectively.

Table 4-5 Unit Number Switch Pack Settings

Jumper Set for an Address of	Unit Number Switch Pack Bits 1	2	3	4	5	6	7	8	Unit Number Name
774500	0	0	0	0	0	0	0	0	MU0 (first TK50)
760nnn	1	0	0	0	0	0	0	0	MU1 (second TK50
760nnn	0	1	0	0	0	0	0	0	MU2 (third TK50)
760nnn	1	1	0	0	0	0	0	0	MU3 (fourth TK50)

0 = switch open
1 = switch closed

4.4.9 Revision Level Switch Pack

Make sure the revision level DIP switch matches the revision level of the module that is stamped on the back (see Table 4-6).

Table 4-6 Revision Level Switch Pack

Revision Level Number	Switches 1	2	3	4	5	6	7	8
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0
3	1	1	0	0	0	0	0	0
4	0	0	1	0	0	0	0	0
5	1	0	1	0	0	0	0	0

0 = Switch open
1 = Switch closed

Rev Level 0	Rev Level 1	Rev Level 2
1 - Off	1 - On	1 - Off
2 - Off	2 - Off	2 - On
3 - Off	3 - Off	3 - Off
4 - Off	4 - Off	4 - Off
5 - Off	5 - Off	5 - Off
6 - Off	6 - Off	6 - Off
7 - Off	7 - Off	7 - Off
8 - Off	8 - Off	8 - Off

4.5 Q22 Bus Interface Logic

This section explains the fourth major functional block of the M7546 Controller: The Q-bus Interface Logic. Included in this functional block are:

- FPLS Control Logic
- Q22 Bus Register
- DMA Address and Data Registers
- Q-bus Interrupt Logic

4.5.1 FPLS Control Logic

The 82S105 Field Programmable Logic Sequencer (FPLS) at E3 (5-C5) works directly with the 80186 to control all Q-bus address and data transfer, as well as handling all the timing requirements that let the controller work on the Q-bus.

A DMA transaction on the Q-bus can be divided into three phases:

1. Bus mastership acquisition
2. Data transfer
3. Bus mastership relinquish phase.

4.5.1.1 Bus Mastership Acquisition Phase -- To initiate a Q-bus transfer, the 80186 accesses a Q-bus memory location within the range accessible by its MCS0 line (40000-4FFFF). The FPLS recognizes the signal MCS0 (ENB QBUS MEM) from the 80186 through the synchronized latch E9 (74F374, 5-D7). Assertion of MCS0, with Address Latch Enable (ALE), also enables the DMA address through the DMA Address Registers at E51 and E55 (6-B2, C2), to the DC005 Q-bus Transceivers at E44, 49, 53, and 54 (sheet 1). See also the section on the Q22 Bus Register for information on the upper six bits of Q-bus address (16 -- 21).

The DMA Address is now on the inputs of the Q-bus Transceivers.

When the FPLS detects the ENB QBUS MEM signal through the latch, it asserts the signal TDMR/TDOUT. Asserting this signal is the start of a Q-bus DMA operation. TDMR/TDOUT becomes the DMA request signal to the host CPU, BDMR L through the 8881 at E13 (5-D1).

The controller waits for the host CPU to respond to the request through assertion of the signal BDGMI L (Bus Grant) on pin AR2. BDGMI L becomes DMGI through the 8640 Q-bus Receiver at E7 (5-C8). DMGI lets the controller know that it has control of the bus (has become bus master) for the duration of its transfer.

The FPLS sees the Bus Grant signal on its pin 4, and asserts TSACK. TSACK enables the Q-bus drivers at E15 (8641), E13 (8881) and E23 (8881) (sheet 5 B-1, C-1, D-1), onto the Q-bus, per Q-bus DMA protocol. The controller waits until BSYNC L and BRPLY L are negated, then asserts BSACK L (E23) and negates BDMR L. The host then ends the bus grant sequence. It negates BDMGO L and waits for the DMA transfer to be completed. The FPLS handles all bus handshaking operations once the 80186 has started the process. See Figure 4-5 for Q-bus DMA timing.

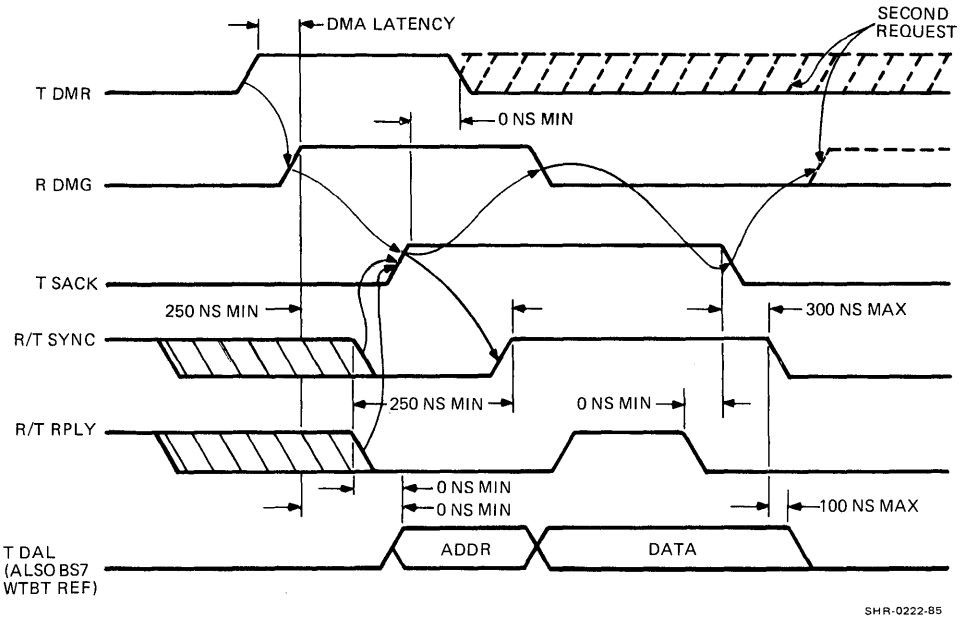


Figure 4-2 Q-bus Timing

4.5.1.2 Data Transfer Phase -- After a delay to enable the Q-bus transfer address through the DC005 Transceivers, the FPLS asserts the TSYNC signal, which clocks the address of the transfer through the transceivers. This is the address of the DMA slave device (memory in this case), which was placed on the transceivers by the 80186.

TSYNC asserts the RSYNC signal through the 8641 at E15 (5-B1). RSYNC is connected to the PAL at E40 (5-B7). The PAL generates the DAL XMIT signal when it decodes RSYNC.

During the address transfer time, the FPLS asserts TDMGO/TWTBT to signal the DMA slave device that the transfer is either a read or write. When TWTBT is a logic 1, the operation is a write.

After a delay (see Q-bus transfer timing), the FPLS asserts the ENB DATA/FPLS INTR signal to enable data onto the Q-bus, or clock data from the Q-bus (depending on whether the transfer is a read or write). In the case of a DMA write, ENB DATA/FPLS INTR tells the 80186 to gate data from the RAM area, through the transceivers at E33 and E46 (2-B2, 2-D2), through the DMA Data register at E56 and E50, to the Q-bus transceivers at E44, E49, E53, and E54 (sheet 1).

In the case of a DMA read from the Q-bus, the FPLS tells the 80186 to transfer data from the Q-bus transceivers, through the DMA data register (in the opposite direction), through the data transceivers at E33 and E46, to RAM.

During the data transfer, the FPLS decodes Byte High Enable (on its input pin 23) and ADR0 (on its input pin 24), and asserts TDMGO/TWTBT if the transfer is byte-wide. TDMGO/TWTBT is not asserted if the transfer is wordwide.

4.5.1.3 Bus Mastership Relinquish Phase -- The FPLS relinquishes its mastership of the bus by negating TSACK, which, through the 8881 at E23, negates BSACK L to the Q-bus. The FPLS negates this signal after completing or aborting the last data transfer cycle.

4.5.2 Error During Q-bus DMA Transfer

During the DMA request/grant sequence (Bus Mastership Acquisition Phase), the FPLS waits for BRPLY from the slave device. While waiting, it de-asserts the ARDY signal, which stalls the 80186 until BRPLY is negated. If BRPLY does not occur within a specified time, a timer (TMR1, or DIAG CLK) in the 80186 times out, informing the FPLS that the response did not occur.

An example of this type of error would be the controller trying to access non-existent memory.

If the time-out occurs, the FPLS terminates Q-bus transfers by de-asserting TSACK and interrupting the 80186 to inform it of the error. The 80186 then determines if the error was a Q-bus parity error, or if the controller had tried to access non-existent memory.

If the DMA transfer completes with no errors, the 80186 writes to the SA register. The FPLS decodes the SA register write and de-asserts TSACK to end the DMA operation.

4.5.3 FPLS Interrupt

An FPLS interrupt can occur during a Q-bus acquisition phase. This can happen when the 7201 MPSC chip interrupts the 80186 for servicing. In this case, the TSACK L signal (80186 pin 47) had been stalling the 80186 while the controller was waiting for the bus grant signal (BDGMI). The FPLS monitors interrupts (pin 2) during this time, and, if an MPSC interrupt occurs, it withdraws the DMA request (BDMR) by de-asserting TDMR/TDOUT, then interrupts the 80186. The 80186 clears the FPLS interrupt by reading the hardware revision level register (ENB VEC REG) and services the MPSC interrupt.

4.5.4 Q22 Bus Register

The Q22 bus register consists of the 74LS273 flip-flop at E19 and the 8881 Q-bus drivers at E13, E18, and E23 (sheet 6). The 80186 uses this register to access up to four megabytes of Q-bus slave memory for data transfers.

The 80186 configures its data bus (DATA0 -- DATA5) for the memory page it has to access, then performs a write (WR), and at the same time, asserts its PCS2 line (ENB Q22 REG). The signal enable address (ENB ADDR) enables these bits onto the Q-bus through the Q-bus drivers.

Each time the controller needs to cross a 64K byte boundary, this register must be updated before the transfer involved in crossing the boundary. The Q22 bus register cannot be changed during a Q-bus transfer, which means that the controller has to do variable length transfers, making sure that it updates the Q22 bus register before crossing a 64K byte boundary.

In addition to the six upper address lines already mentioned, the Q22 bus register has two more bits under control of the 80186: BBS7 and QINTR.

BBS7 lets the controller access the I/O Page in Q-bus memory; QINTR is a Q-bus interrupt request line to the host CPU. This signal is normally low, and must be asserted high to initiate a Q-bus interrupt to the host.

The following is a list of the relationships between the 80186 data bus and the Q-bus bits already mentioned.

DATA0	BDAL16
DATA1	BDAL17
DATA2	BDAL18
DATA3	BDAL19
DATA4	BDAL20
DATA5	BDAL21
DATA6	BBS7
DATA7	QINTR

4.5.5 DMA Address and Data Registers

4.5.5.1 DMA Address Register -- This register consists of two 8-bit latches on page 6 of the schematics (74S374s at E51 and E55 -- 6-B2, 6-D2). Each time the 80186 accesses a Q-bus memory location, these registers are loaded with that address (through the 80186's transceivers at E33 and E46 -- 2-B2, D2). The FPLS controls the timing regarding when the address is loaded onto the Q-bus transceivers, but the PAL at E45 provides the signals that actually enable the address. The PAL decodes the TSACK, ENBDATA (de-asserted) and TDIN (de-asserted) signals, from the FPLS, to generate the ENB ADDR (enable address) signal. The FPLS provides the correct combination of TSACK, ENB DATA, and TDIN when the appropriate signals are asserted on its inputs.

4.5.5.2 DMA Data Register -- This register consists of the same two 74LS646 multifunction registers that make-up the SA and Vector registers already mentioned.

During a DMA Write to the Q-bus, the 80186 retrieves data from on-board memory, gates it through its bus transceivers with the DEN and ENB QBUS MEM signals, and loads it into the DMA Data register with the CLK A signal. CLK A is generated by the PAL at E45 after it has decoded the 80186 signals WR (write) and ENB QBUS MEM (enable Q-bus Memory). The contents of the DMA data register are enabled onto the Q-bus transceivers with ENA and DIR. ENA and DIR are generated by the PAL at E45 when it decodes TSACK and ENB DATA (provided by the FPLS at the appropriate time). The FPLS provides TSACK and ENB DATA when the appropriate signals have been asserted on its inputs.

During a DMA Read from the Q-bus, the host CPU loads the DMA Data Register (through the Q-bus transceivers). The DMA Data register is actually loaded by the CLK B signal, which is generated by the PAL at E45 after it decodes TSACK and ENB DATA (from the FPLS). The FPLS generates TSACK and ENB DATA when the appropriate combination of signals on its inputs are asserted. The 80186 reads the data (through its bus transceivers) by asserting RD and ENB QBUS MEM, which the PAL decodes to generate ENA and DIR (connected to the DMA Data register).

4.5.6 Q-bus Interrupt Logic

When the controller has to interrupt the host CPU, it asserts the QINTR signal in the Q22 bus register logic. QINTR clocks the request into the DC003 Interrupt Control Chip at E27, sheet 5 (pins 17 and 14 are the request and clock, respectively). The DC003 then enables BIRQ (pin AL2) onto the backplane of the CPU. When the DC003 detects the signal BIAKI (pin AM2) on the backplane, and it receives the signal BDIN, it generates Vector. The Vector signal is decoded by the PAL at E45, which generates CLK A to clock the vector address through the Vector register to the Q-bus Transceivers.

The PAL at E40 also detects the Vector signal, which it decodes to generate XMIT DAL to the Q-bus transceivers. XMIT DAL enables the vector address onto the Q-bus for the host CPU to read.

To initiate another interrupt, QINTR is reset, then set again. The DC003 needs the low to high transition to assert BIRQ.

4.6 TAPE DRIVE INTERFACE

This section describes the fifth main functional block of the M7546 Controller. The tape drive interface circuitry consists essentially of the 7201 Multi-Protocol Serial Controller (MPSC) Chip at E4 on sheet 7, the 26LS31 quad driver at E25, and the 26LS32 quad receiver at E22. Also included in this section is a connector, into which the tape drive signal interface cable is plugged.

4.6.1 7201 Multi Protocol Serial Controller (MPSC)

The 7201 MPSC provides the communications interface between the drive and the 80186. It communicates commands and status to and from the drive and also handles data transfer between the drive and the 80186. It accepts parallel data from on-board memory on its D0 -- D7 inputs (pins 19 -- 12), then transmits the data serially to the drive, via the 26LS31 Quad Driver at E25. Conversely, it accepts serial data from the drive, via the 26LS32 Quad Receiver at E22, converts it to parallel format, then sends the data to on-board memory through its D0 -- D7 outputs (also pins 12 -- 19).

Once programmed by on-board microcode, the MPSC works with the DMA control block in the 80186 to transfer data. The MPSC is configured so that Channel B is in asynchronous mode for commmand and status transfers, while channel A is in synchronous mode for data transfer to and from the tape drive. The timing for read data transfers is shown in Figure 4-3.

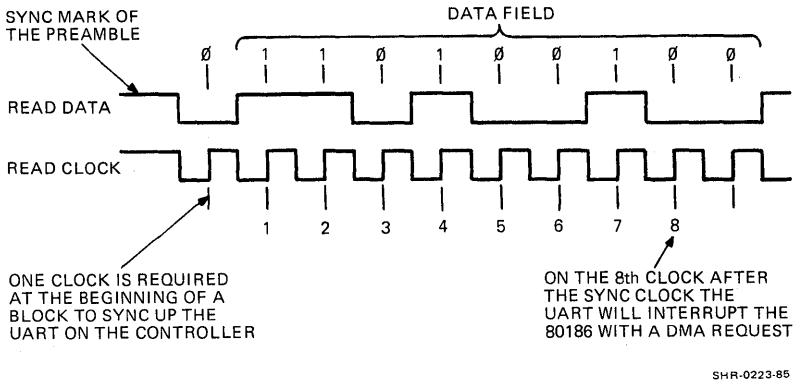


Figure 4-3 Read Data Timing

On power-up, the MPSC's internal registers are programmed for the configuration already mentioned. The registers are altered during data transfer, to let the MPSC interrupt the 80186. The MPSC interrupts the 80186 under the following conditions:

1. On detection of a read gap.
2. First character received, to start read DMA transfers.
3. Transmit Buffer Empty, to append the CRC on a write to the tape drive.

The MPSC is programmed so that DMA is enabled each time a byte is required on a write or read. The MPSC asserts a DMA request (pin 11 or pin 32, read and write respectively), to one of the DMA request lines to the 80186, through E2 and E17 (sheet 7) for DMA reads, and E5 and E17 for DMA writes.

The MPSC interrupts the 80186 when it receives the first character, either from the drive or from on-board memory. This is the beginning of the DMA transfer. The sequences for DMA read (data), DMA write (data) follow:

DMA Read

1. The MPSC generates DRIVE DR CMD from its TxDB pin.

2. The MPSC receives a clock (DRIVE RD CLK) on RxCA (pin 35).

3. The MPSC receives serial data from the drive (DRIVE RD DATA) RxDA (pin 34), through E22.

4. The MPSC generates a DMA Read Request (RDYA, pin 32) to the 80186 through E2 and E17.

5. The 80186 responds with DMA HAI through E6 to enable the MPSC.

6. The 80186 asserts RD (MPSC pin 22).

7. The MPSC sends parallel data via D0 -- D7 (pins 19 -- 12) to on-board memory.

8. The MPSC asserts Read DMA Request for each byte, until the 80186 DMA terminal count is reached.

DMA Write

1. The MPSC generates a DMA Write Request (from RDYB).

2. The 80186 responds with DMA HAI through E6 to enable the MPSC.

3. The 80186 provides WR (MPSC pin 21) and data on D0 -- D7 (MPSC pins 19 -- 12) from on-board RAM.

4. The MPSC ouputs serial characters for write command (DRIVE DR CMD).

5. The Drive provides DRIVE WR CLK for MPSC input RxCA (pin 35).

6. The 80186 provides DRIVE WR GATE through the Miscellaneous Control register.

7. The MPSC provides serial DRIVE WR DATA from TxDA (MPSC pin 37).

8. The MPSC asserts WR DMA REQ for each succeeding byte until an 80186 DMA terminal count is reached.

4.6.2 Differential Drivers and Receivers

There is one differential driver that sends data and commands to the drive and one differential receiver that accepts clocks, data, and status from the drive.

The 26LS31 differential driver at E25 (7-B2) sends the following signals to the drive.

- Serial Drive Write Gate (DRIVE WR GATE)
- Serial Drive Erase (DRIVE ERASE)
- Serial Drive Commands (DRIVE DR CMD)
- Serial Drive Data (DRIVE WR DATA)

The 26LS32 differential driver at E22 (7-A7, 7-C7) accepts the following signals.

- Serial Drive Status (DRIVE DR STATUS)
- Serial Drive Read Data (DRIVE RD DATA)
- Drive Read Clock (DRIVE RD CLK)
- Drive Write Clock (DRIVE WR CLK)

4.7 Diagnostic Hardware

The last major section of logic on the M7546 Controller is the gates that have been assigned diagnostic functions. The hardware detailed in this section has been specifically provided for diagnostic checking of the various logic elements on the controller.

4.7.1 Diagnostic Indicators

LED1 and LED2, controlled by the 80186 through the Miscellaneous Control register (Section 4.4.1), signal pass/fail of the on-board microdiagnostics. On power-up, both LEDs light. After the power-up diagnostics have completed, LED1 goes out. LED2 goes out after TMSCP has successfully initialized the controller.

4.7.2 Miscellaneous Register Loopback

Three signal lines in the Miscellaneous Read register are for direct diagnostic feedback to the 80186. This is so the register can check that the lines can be set and reset.

- **Drive Write Gate**
  This signal is set in the Miscellaneous Write register by the 80186, then checked by the 80186 through the Miscellaneous Read register.

- **Drive Erase**
  This signal is also set in the Miscellaneous Write register and checked through the Miscellaneous Read register.

- **QINTR**
  This signal is set by the 80186 through the Q22 bus register and checked by the 80186 through the Miscellaneous Read register.

4.7.3 7201 MPSC Diagnostic Loopback

The 7201 MPSC chip can be tested without a tape drive connected to the controller. This is accomplished by the 74LS157 quad two-to-one multiplexer at E12 (7-C6). Commands sent by the MPSC are looped back through this mutiplexer as drive status, and write data sent by the MPSC is looped back as read data.

In this mode, the 80186 asserts the signal DIAG in the Miscellaneous Control register (74LS259 Latch at E35, 4-D7). The signal DIAG performs the following functions.

1. DIAG connects write data (from the MPSC's pin 37 -- TxDA), through the MUX (pin 13), to the MPSC's input pin 34 (RxDA). The 80186 sends data out through the MPSC, with DIAG asserted, reads it back through the MPSC, and compares it to the data originally sent. This checks that the MPSC can read and write data through Channel A.

2. DIAG connects drive commands (from the MPSC's pin 8 -- TxDB), around through the MUX (pin 10) to the MPSC's input pin 9 (RxDB) for drive status. The 80186 sends data out through the MPSC's channel B, then, with DIAG asserted, reads it back through the receive section of MPSC Channel B. The 80186 compares the data received to the data sent. This checks that the MPSC can write and read data through its channel B (commands and status during normal operation).

3. When data read/write and command/status diagnostic operations are happening, the 80186 is using DIAG CLK to clock the data to and from the MPSC. This makes sure that the MPSC can accept transmit and receive clocks (Drive Read and Drive Write Clocks, respectively, during normal operation).

   DIAG CLK can also be gated through the MUX to the Gap Detect Counter at E10 (7-D6). In this configuration, the MPSC can be checked to make sure it is capable of generating an interrupt when a gap on the tape is detected.

   This capability also checks the Gap Detect Counter (E10) and the Gap Detect Flip-flop at E11. The counter generates a clock to the gap detect flip-flop on the eighth occurrence of DIAG CLK. The Gap Detect Flip-flop generates the GAP DETECT signal (connected to pin 6 of the MPSC). When the MPSC detects the falling edge of GAP DETECT, it interrupts the 80186 to inform it of the gap.

4.7.4 Soft Grounds

For GR and QV testers, the M7546 controller provides resistors to ground on some gates. These can be used by testers to disable these gates for testing. The following are the locations of soft grounds.

1. Page 2 of the schematics. The Output Enable Pins (pin 1) of the 80186 address latches, by a 68 ohm resistor. The enable can be pulled high so the testers can inject any address into the latches.

2. Page 5. The output enable (pin 1) of the 74F374 latch at E9. The testers can pull the enable high to inject any combination of signals into the FPLS.

3. Page 7. Connects the enable signal of the MUX at E12 to ground with a 68 ohm resistor. The testers can pull up the enable signal so they can inject signals into the MPSC to test it.

APPENDIX A
TQK50 DETAILED BLOCK DIAGRAM, TK50 EXPLODED VIEW

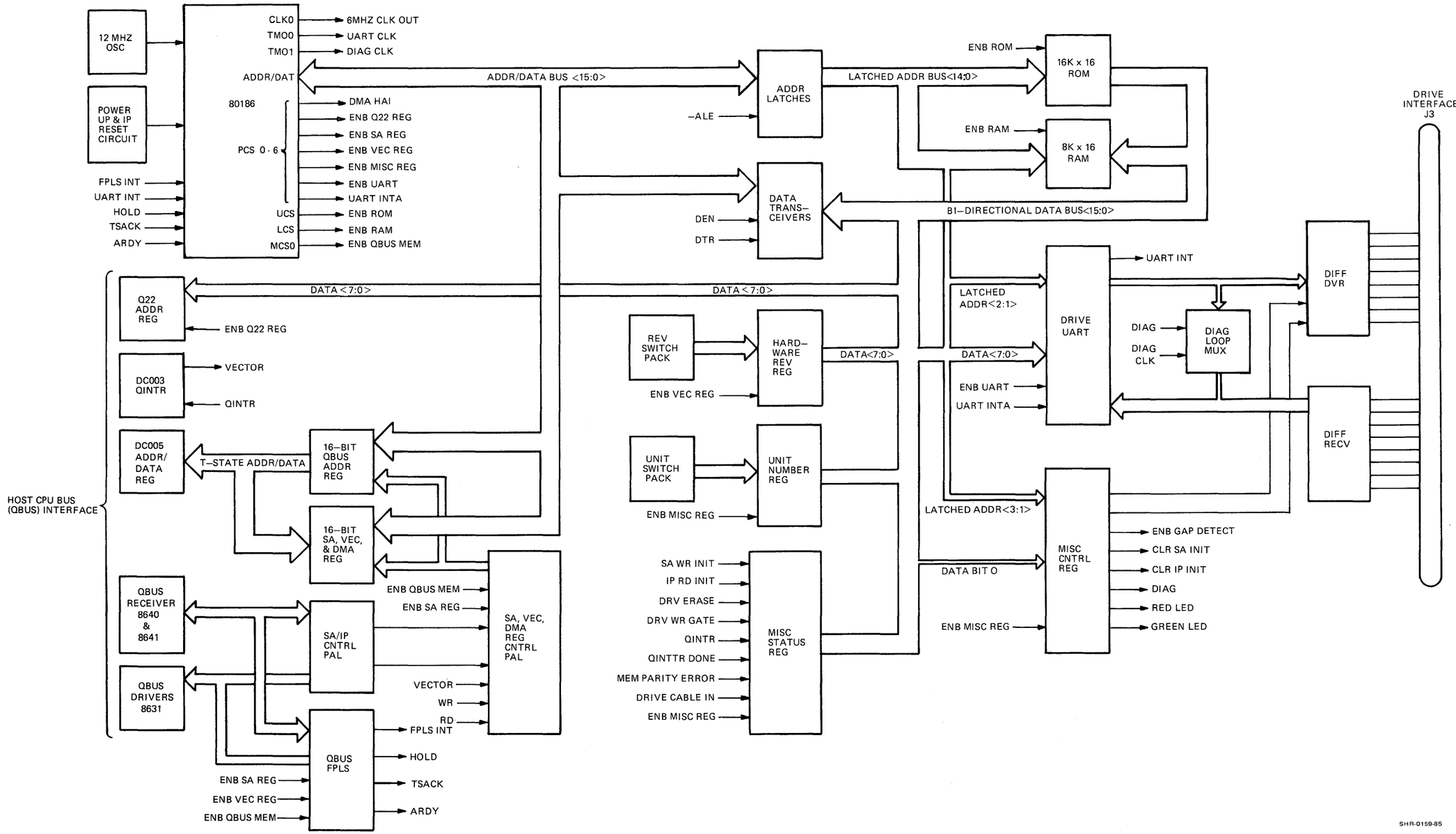


Figure A-1 TQK50 Detailed Block Diagram

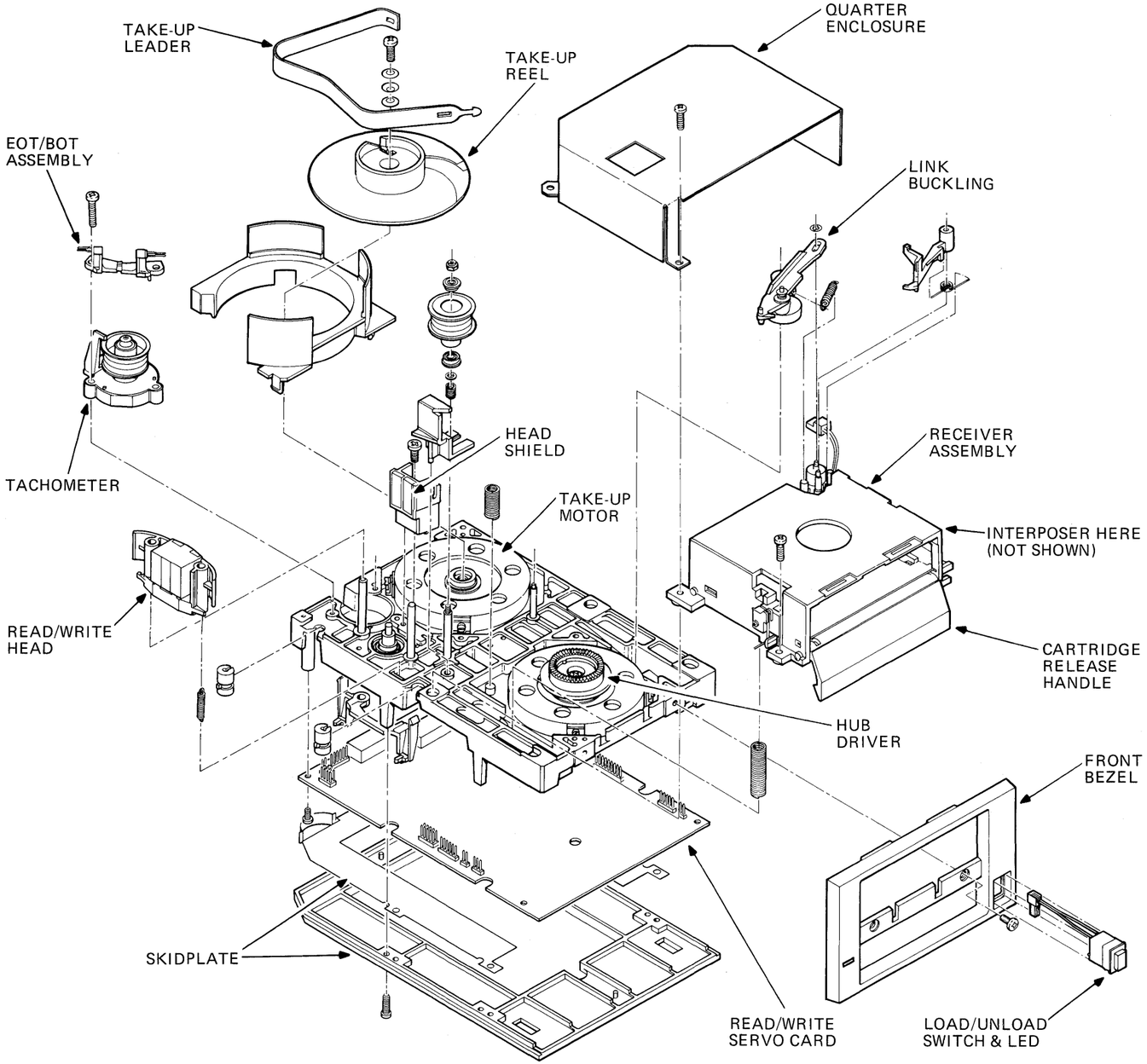


Figure A-2 TK50 Exploded View

APPENDIX B
TK50 SUBSYSTEM ERROR CODES AND STATUS

This Appendix lists error and status codes sent from the TK50 controller to the host system.

Table B-1 Drive Error Sub-code Values

Sub-code	Code + Sub-code Dec	Oct	Hex	EV	ST	Status or Event Sub-Code
1	43	53	28	*	*	Drive command timeout. The controller has timed out a command exchange with the drive.
2	75	113	48	*	*	Controller detected transmission error. The controller has detected a protocol violation during a command exchange with the drive.
3	107	153	68	*	*	Recoverable drive fault The drive has detected and reported a recoverable fault during a transfer operation.
4	139	213	88	*	*	Unrecoverable drive fault The drive has detected and reported an unrecoverable fault during a transfer operation.

Table B-2 Controller Internal Status Byte

Value Dec	Value Oct	Value Hex	Controller Internal Status
0	0	0	Done
2	2	2	Retry
4	4	4	Hard Error
6	6	6	Tape Mark Read
8	10	8	Logical EOT Detected
10	12	A	End of Media
12	14	C	Drive Error
14	16	E	Communications Exception
16	20	10	End of Data
18	22	12	Failed to Find Append Target
20	24	14	Leaving EOT Trailer Region
22	26	16	ECC Correction on Data
24	30	18	ECC Correction on Tape Mark
26	32	1A	BOT Encountered
28	34	1C	Data Synchronization Error
30	36	1E	EOT detected
32	40	20	Seek Aborted
34	42	22	Unload

Table B-3 Drive Error Code Byte

Value Dec	Value Oct	Value Hex	Drive Error Code
1	1	1	Hardware Write Protect
2	2	2	Drive Fault
4	4	4	Communications Exception
6	6	6	Wrong Track
16	20	10	Sync Failure
19	23	13	Communications Error
34	42	22	Positioning Error
35	45	23	Channel B Overrun
39	47	27	Channel A Overrun

Table B-4 Recoverable Drive Faults

Value Dec	Value Oct	Value Hex	Recoverable Drive Fault Code
144	220	90	8155 RAM failure in self-test
145	221	91	8155 timer failure
146	222	92	Read amplitude (HD1) too low in calibrate
147	223	93	Read amplitude (HD2) too low in calibrate
148	224	94	--
148	225	95	EOT sensed in R/W/S state
149	226	96	BOT sensed in R/W/S state
150	227	97	Drive block address overflow
151	230	98	Drive block address underflow
152	231	99	Servo error -- excessive speed variations
153	232	9A	Failure in tracking
154	233	9B	Command error -- command not recognized
155	234	9C	Illegal command -- incompatible with drive state
156	235	9D	Write lock error
157	236	9E	Write gate at wrong time
158	237	9F	No write gate for cal track write
159	240	A0	Error sensing cal track 1 -- bad head
160	241	A1	Error sensing cal track 2 -- bad head
161	242	A2	Detection of edges of cal track 1 out of spec
162	243	A3	Detection of edges of cal track 2 out of spec
162	244	A4	Offset of cal track 2 from cal track 1 is too large
164	245	A5	Search of bottom tape edge failed
165	246	A6	Bottom tape edge tolerance error
166	247	A7	Drive is overheating
167	250	A8	No current in LED of BOT sensor (cable?)
168	251	A9	Hall switch sense lines Motor A questionable
169	252	AA	Tachometer failure

Table B-5 Unrecoverable Drive Faults

Value Dec	Oct	Hex	Unrecoverable Drive Fault Code
129	201	81	Failure to load to BOT
130	202	82	Failure to unload tape into cartridge
131	203	83	General motor or tach failure
132	204	84	Motor A failure
133	205	85	Motor B failure
134	206	86	Drive lost control of tape or bad tach
135	207	87	Excessive drag in tape transport
136	210	88	Failure to stop tape or remain stopped
137	211	89	Cartridge insert error
138	212	8A	Cartridge extract error
139	213	8B	CU attempted to move tape with drive in error
140	214	8C	Deceleration timeout error
141	215	8D	Second attempt to balance reels in init failed

Table B-6 Drive Flags

Bit Number	Bit Mask Oct	Hex	Drive Flags
0	1	1	Cartridge Present
1	2	2	Head at Track Zero
2	4	4	Tape Unloaded
4	10	8	Hardware Write Protected
5	20	10	Positioned at BOT
6	40	20	Drive in Run State

Note: Bits 5 and 6 together indicate that the drive is rewinding to BOT

Table B-7 U/Q Port Generic SA Error Codes

Value Dec	Value Oct	Value Hex	Failure Code
1	1	1	Envelope/Packet Read (parity or timeout)
2	2	2	Envelope/Packet Write (parity or timeout)
3	3	3	Controller ROM and RAM parity
4	4	4	Controller RAM parity
5	5	5	Controller ROM parity
6	6	6	Queue Read (parity or timeout)
7	7	7	Queue Write (parity or timeout)
8	10	8	Interrupt Master
9	11	9	Host Access Timeout (higher level protocol dependent)
10	12	A	Credit Limit Exceeded (reporting this condition optional)
11	13	B	Bus Master Error
12	14	C	Diagnostic Controller Fatal Error
13	15	D	Instruction Loop Timeout
14	16	E	Invalid Connection Identifier
15	17	F	Interrupt Write Error
16	20	10	MAINTENANCE READ/WRITE Invalid Region Identifier
17	21	11	MAINTENANCE WRITE Load to non-loadable controller
18	22	12	Controller RAM error (non-parity)
19	23	13	INIT Sequence Error
20	24	14	High Level Protocol Incompatibility Error
21	25	15	Purge/poll hardware failure
22	26	16	Mapping register read error (parity or timeout)
23	27	17	Attempt to set port data transfer mapping when option not present

Note: 24 -- 99 are unassigned

Table B-8 Controller Specific SA Error Codes

Value			
Dec	Oct	Hex	Failure Code
600	1130	258	Divide Interrupt Error
601	1131	259	Single Interrupt Error
602	1132	25A	Non-maskable Interrupt Error
603	1133	25B	Breakpoint Interrupt Error
604	1134	25C	INT0 Detected Interrupt Error
605	1135	25D	Array Bound Interrupt Error
606	1136	25E	Unused Opcode Interrupt Error
607	1137	25F	ESC Opcode Interrupt Error
608	1140	260	--
609	1141	261	Reserved Interrupt Error
610	1142	262	--
611	1143	263	--
612	1144	264	INT0 Interrupt Error
---	----	---	--
625	1161	271	ROM Checksum Error
626	1162	272	MPU Error
627	1163	273	RAM Error (Odd Byte)
628	1164	274	RAM Error (Even Byte)
629	1165	275	MPU Timer Error
630	1166	276	Miscellaneous Register Wrap Error
631	1167	277	Gap Detection Circuitry Error
632	1170	278	USART Wrap Mode Error
633	1171	279	USART Wrap Mode Error (Good CRC)
634	1172	27A	USART Wrap Mode Error (Bad CRC)
635	1173	27B	Drive Cable Error
636	1174	27C	FPLS Buffer Error -- Nibble 1
637	1175	27D	FPLS Buffer Error -- Nibble 2
638	1176	27E	FPLS Buffer Error -- Nibble 3
639	1177	27F	FPLS Buffer Error -- Nibble 4
640	1200	280	Word Count Error
641	1201	281	FPLS Test Error
651	1213	28B	Reserved -- ECC
652	1214	28C	Write Sequence Fault
653	1215	28D	ECC Logic Error Type 1
654	1216	28E	ECC Logic Error Type 2
655	1217	28F	ECC data structure consistency failure

Note: 613 -- 624, 642 -- 650 and 656 -- 699 are unassigned

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