decsystem10

Advanced Systems Group

DT03-CC SWITCH CONTROLLER
AND INTERPROCESSOR BUFFER

digital

DT03-CC SWITCH CONTROLLER AND INTERPROCESSOR BUFFER

The material in this manual is for informational purposes and is subject to change without notice.

SECTION 1
INTRODUCTION

1.1 GENERAL

The DT03-CC Switch Controller and Interprocessor Buffer provides the means for two systems to control or configure system I/O and memory devices. That is, each system can programmably attach system devices or share devices in the system with another system. The interprocessor buffer is a general purpose buffer. It provides half-duplex communications on a single word basis. Data transfers take place on a request/ acknowledge basis. For example, processor A sends a word, the B side is interrupted, reads the word, and sends back an interrupt to inform A that B received the word.

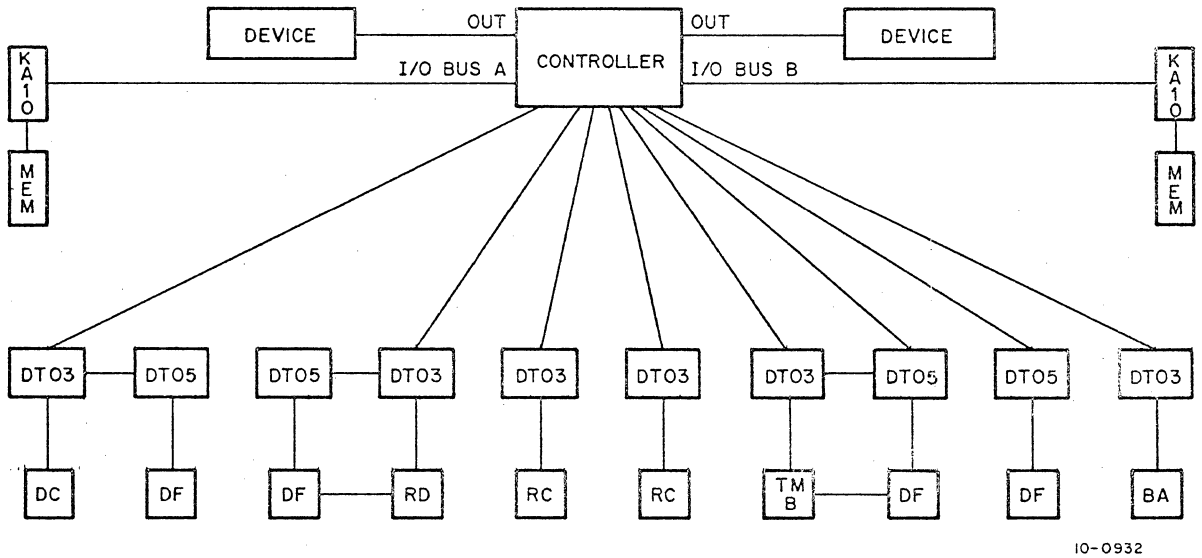


Figure 1-1 Typical DT03-CC System Configuration

1.2 SPECIFICATIONS

A. Mechanical

Cabinet	H950 Cabinet
Logic Panels	Three, H911K
Height:	15-3/4 in. (0.39m)
Width:	19 in. (0.48m)
Depth:	6-3/4 in. (0.17m)
Weight:	60 lb (27 kg)

B. Electrical

Power Control	One 844
Power Supply	One H721
Logic Potentials	+5V; -15V
Line Voltage	115/208 Vac ± 10%, 60 Hz ± 1 Hz, Single Phase
DC Line Current	+5 Vdc = 360 mA; -15 Vdc = 150 mA
AC Line Current	6A
Module Series	M-Series

C. Environmental

Operating Temperature	45° to 95°F (7° to 35°C)
Storage Temperature	40° to 110°F (5° to 45°C)
Relative Humidity	20% to 80%

1.3 FUNCTIONAL DESCRIPTION

The DT03-CC is a controller designed to programmably or manually handle DT03-CS and DT05-CS manual bus switches. This controller is attached to two PDP-10 I/O buses, so they can programmably or manually configure a system. The DT03-CC is used to initially configure each PDP-10 system and to share some or all the peripherals. Up to eight peripherals attached to this controller can be controlled. The DT03-CS's and DT05-CS's are attached only by a radial connecting cable which carries three signals. The signals are A remote, B remote, and select. The A and B remotes are sent to the switches; select is returned to the controller if the switch did switch and the switch is not in LOCAL.

The "A" or "B" selected levels are ANDed with the switch register flops which can cause the setting of an error flop. If the error flop does get set it will cause an interrupt at which time the handler will CONI the status and discover error condition bit 30 set.

The maximum distance between the DT03-CS's and DT05-CS's and the controller is 100 ft.

SECTION 2
INSTALLATION

2.1 SITE CONSIDERATIONS

The DT03-CC is housed in one H950 Cabinet which contains all the necessary indicators, fans, power supplies, and power control. Figure 2-1 shows the floor plan required for the cabinet.

2.2 CABLES

The DT03-CC can be installed anywhere along the PDP-10 I/O Bus. Consideration must be made however, for the total length of I/O Bus Cable from the central processor through the various DT03-CS units to the commonly-shared options. Refer to the DECsystem-10 Site Preparation Guide for detailed information on the I/O Bus.

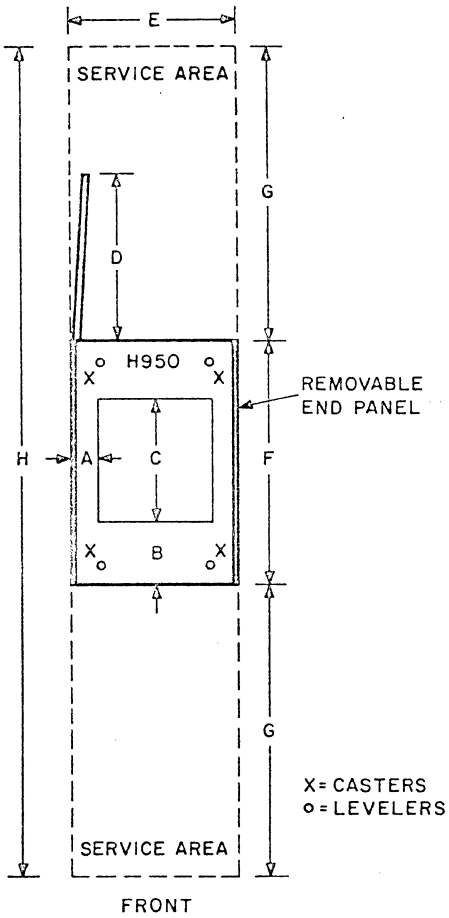
A standard BC10A I/O Bus Cable connects each of the two central processors to the DT03-CC controller. I/O Bus A plugs into locations AB1-4 and continues from location AB5-8 to the next peripheral device on the I/O Bus. The I/O Bus B plugs into slots EF1-4 and continues from slots EF5-8 out to the next device.

The only connection between the DT03-CC controller and a DT03-CS or DT05-CS switch is the radial switch cable which contains a W023 connector. Up to eight DT03-CS or DT05-CS switches may be connected to the controller. The allocated slots in the controller for the eight radial switch cables are C29–C32, D29–D32. Slot C29 is for switch 1, C30 for switch 2 continuing up to slot D32 for switch 8.

2.3 RELATED DOCUMENTS

The following DEC publications contain material which supplements this option description:

DECsystem-10 Interface Manual	DEC-10-HIFC-D
DECsystem-10 System Reference Manual	DEC-10-HGAC-D
DECsystem-10 Site Preparation Guide	DEC-10-SITE-D



DIMENSIONS	A	B	C	D	E	F	G	H
INCHES	3.2	7.5	15	20	20.5	30	36	102
METERS	0.08	0.19	0.38	0.5	0.52	0.76	0.91	2.58

10-0871

Figure 2-1 DT03-CC Floor Plan

SECTION 3
OPERATION AND PROGRAMMING

3.1 CONTROLS

The DT03-CC Controller has no operating controls since operation is under control of the PDP-10 program. However, there is a test panel for maintenance purposes. There are eight 3-position switches on the panel. These switches must be in the OFF position when not in use. The toggle switches are for the remote manual configuring of the switches attached to the DT03-CC. These toggle switches are labeled 1 through 8.

The REMOTE/LOCAL switch is normally set in the REMOTE position so the DT03-CC can be program-controlled. The LOCAL position is for the enabling of the eight configuration toggle switches. If this switch is in the LOCAL position when the program performs a CONI to obtain the status from either the "A" side or the "B" side, an error bit will be read back.

3.2 PROGRAMMING

The DT03-CC controller utilizes only the PDP-10 CONO and CONI instructions for the switch controller portion. Refer to the DECsystem-10 System Reference Manual for further information concerning I/O instructions. The switch controller can handle up to eight pairs of single switches as shown in Figure 1-1. They are set or cleared on a CONO or CONI instruction as shown in Figure 3-3.

There are eight slots for control cables which are radial buses to each switch. The cables have three signals on them as listed below.

A SELECT
B SELECT
SELECTED

If "A" has the switched bus and "B" side makes a request, the "B" request flop is set. When "A" side releases, the switched bus "B" side is interrupted and a CONI is performed to determine which one of the SW ENA bits is free.

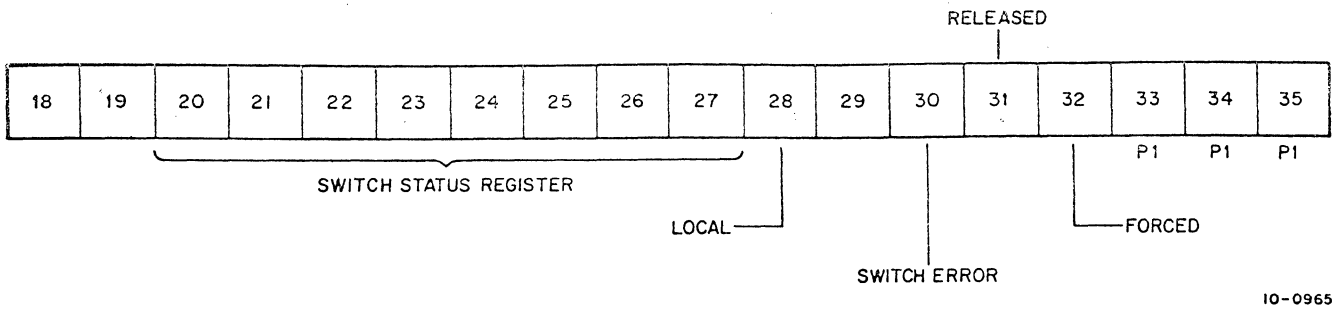


Figure 3-1 CONI Status

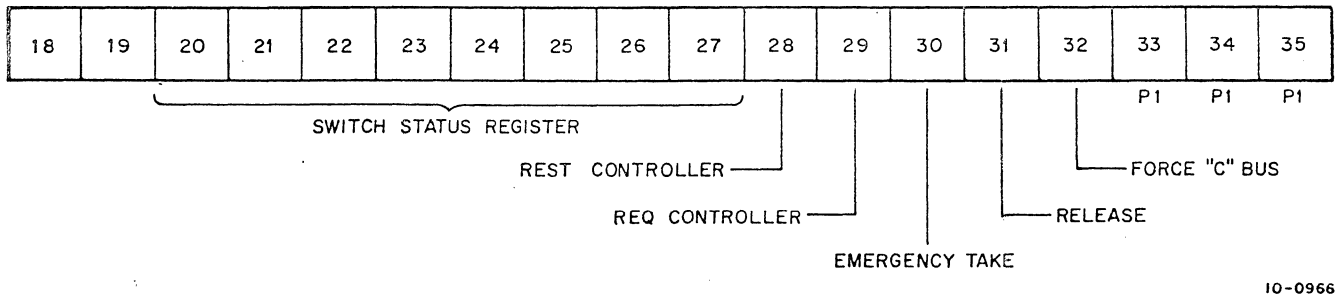


Figure 3-2 CONO Status

The switch STATUS REGISTER is a single register of eight flops which is set on a CONO and can be read back on a CONI, to determine which one is free. If they did not switch, it might indicate a switch element in the local state. The switch controller can have any device address using W921 jumper boards.

Descriptions of STATUS REGISTER on a CONO:

FORCE C BUS:	Bit 32 – used when one side has an emergency condition such as the power fail flag setting in the CPU. In the soft-fail routine, one side could set its switched devices free for the other side to use and cause an interrupt to let the other side know it can have these devices.
RELEASE:	Bit 31 – The side which has the bus simply lets go of the switch. It causes an interrupt to the other side if the other side had request set.
EMERGENCY TAKE:	Bit 30 – This is used when one side wants to override the other side's conditions.

REQUEST CONTROLLER: Bit 29 – Used to simply request use of the control and log a request. If a requested device is in use, this request enables an interrupt when the other system does a release.

RESET CONTROLLER: Bit 28 – The setting of this bit resets switch controller SW ENA condition.

Description of CONI STATUS REGISTER bits:

SWITCH ERROR: Bit 30 – Indicates the switch status register does not agree with the levels from the remote elements. It could mean the element is in the LOCAL condition.

RELEASED: Bit 31 – Indicates the other LOCAL case side released a device. An interrupt occurs because this side issued a CONO with bit 29 set which is REQ. Thus, when the other side releases the requested device, this side is informed.

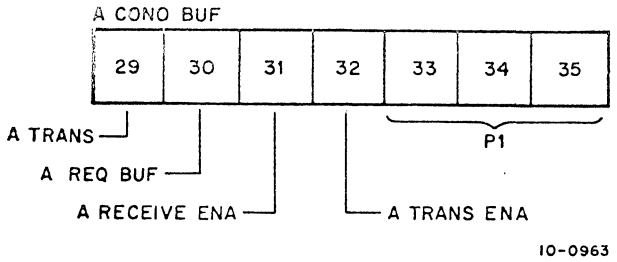
LOCAL: Bit 28 – Means that the controller LOCAL switch is on. If the switch is off, it forces all switch elements to the "A" or "B" side.

FORCED: Bit 32 – The side which had the switch causes this bit to be set when it detects an error condition such as power-fail and forces the switch to free. At the same time, it interrupts the other side by setting bit 32.

3.2.1 Programming Buff

When using the interprocessor buffer, a CONO instruction must first be issued. The corresponding bits for the type of transfer (receive or transmit) and the PI assignments must be on a one (see Figure 3-3).

If Transmit Enable is on a one, and a DATAO word has been sent to the other system, an interrupt is sent back confirming the receipt of the word. A second word can now be transmitted if desired. If only a single word is to be sent, Trans Enable need not be set. The Receive Enable bit is only used to inform the other system that the first system will accept data.



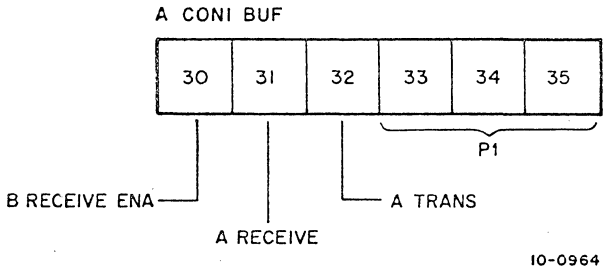


Figure 3-3 CONO, CONI BUF Bit Assignments

CONO BUFF

A TRANS — Bit 29 – used to implement a BLOCK OUT instruction. It saves the use of a DATAO instruction preceeding the BLOCK OUT if one is going to transfer blocks of words. This bit will force an interrupt if transmit enable is set, thus starting the block out instruction.

A REQ BUFF — Bit 30 – used to stop one system from changing data during a transfer. Locks out the other system.

A RECEIVE ENA. — Bit 31 – used to let the other system know that this system will take data or that it is running.

A TRANS ENA. — Bit 32 – used to inform one system, via the interrupt, that the other system has taken the word of data. Data transfers via a BLOCK OUT. This interrupt would reenter the service routine and send another word.

CONI BUFF

B RECEIVE ENA.	Bit 30 – indicates the other system will take data or is running.
A RECEIVE	Bit 31 – indicates the system has been sent data and it should now perform a DATAI.
A TRANS	Bit 32 – indicates the word of data has been taken and another word can be sent.

3.2.2 General Programming Techniques

Because of the nature of a remote switch controller, one system could easily crash the other system that is tied to the switches. With this in mind, it is necessary, when programming the controller, to always start with a CONI to determine the state of the switches in the system. Before the switches can be altered, the CONI is necessary within the logic. Therefore, the procedure would be to follow the CONI with a CONO REQUEST and the enable bits for the switch or switches desired to use. If, on the CONI, one of the desired switches is on the other system, it cannot be switched back to the first system. This could only be accomplished by an EMERGENCY TAKE, which would clear the other side out and provide the user with all the resources required.

If a device in the system is predetermined to be a high-contented device, the software on both sides should take this into account by releasing the device after it has completed its current task. The CONO release causes an interrupt to the other system which would then be followed by a CONI to determine the condition that caused the interrupt. At this point, the device is available for use. A CONO REQ is issued with the normal configuration plus the new device enable bit.

3.2.2.1 Interrupt Service Device Polling

There are certain aspects the programmer should be aware of when polling the DTO3-CC from an interrupt service routine. Any CONI or CONSx instruction that is issued to the controller may set the HOLD flip-flop for that side. If HOLD is set, the other side is prevented from requesting any switches until HOLD is reset.

Therefore, the following coding serves as a possible technique to be used to prevent permanent lockout of one side.

```
54/JSR CH6
55/

CH6:    0
        JRST  DTINT          ;CHECK DT03-CC FIRST

DTINT:  MOVEM 1, SAC         ;SAVE AC 1
        CONI STATUS, 1       ;GET CONTROLLER STATUS
        TRNE 1, FLAG         ;CHECK FLAG(s)
        JRST .+5             ;JUMP AHEAD 5 IF SET
        TRZ 1, 37B32         ;OTHERWISE CLR BITS 28 THRU 32
        CONO STATUS,
          1B29(1)            ;ISSUE CONO WITH REQUEST BIT SET
        MOVE 1, SAC          ;GET BACK AC 1
        JRST DEVINT          ;GO POLL ANOTHER DEV
            .
            .                } DTO3-CC  INTERRUPT SERVICE
            .
        JEN @ CH6
```

The above polling technique ensures that:

1. The HOLD flip-flop does not stay on.
2. No switch enable register bits are lost.
3. The PI channel assignment is not lost.

3.2.2.2 Selecting/DeSelecting Switches

Before a new switch is selected, the switch enable register should be read to determine if the switch is free. As an example, if this side wanted SW1:

```
CONI STATUS, 1          ;GET STATUS
TRNN 1, 1B20            ;IS SW1 FREE
TRO 1, 1B20             ;YES – SET SELECTION BIT
TRZ 1, 37B32            ;CLR BITS 28-32
CONO STATUS, 1B29(1)    ;REQUEST SW1 - ALSO RELOAD ORIGINAL BITS
```

```
CONSZ STATUS, 1B30          ;SELECTION ERROR
JRST SELERR                 ;YES - GO HANDLE
        .
        .                   ;NO - CONTINUE
        .
```

If a side wants to release a switch it could do the following. (Example uses SW1)

```
CONI STATUS, 1              ;GET STATUS
TRZ 1, 1B20 + 37B32         ;ZERO SW BIT PLUS 28-32
COND STATUS, 1B29 +
  1B30(1)                   ;RELEASE SW AND RESET HOLD
```

NOTE

CONO Request must always follow CONI to ensure HOLD is reset.

SECTION 4
THEORY OF OPERATION

4.1 SWITCH SELECTION

The switch controllers device decoder generates A IOC 1 ALLOW if the "B" system does not have CONNECT on a one. The A IOC 1 ALLOW level gates in the CONI signal which sets the "A" side HOLD flip-flop. Then the "A" side issues a CONO with the PI status and the request bit (IOB 29) along with the SWITCH ENA bits for the device requested by the "A" side. The HOLD flip-flop is cleared by CONNECT going to a one. The connect flip-flop is only set by the request bit (IOB 29) and HOLD flip-flop on a one to ensure the switch register enable register is read in. This allows the program to determine what switches are available for selection. The setting of the connect flip-flop causes the "A" LATCH flip-flop to set which locks-in the contents of the switch enable flip-flop. At this time the switch enable flip-flop could be cleared by the other system, but this action would not have any effect on "A" switches which are now latched up. This case is remote however, because the "B" side would not normally zero out the switch enable register. If anything, the "B" side would CONI the register status so it could make a selection of the remaining switches. If the "B" side desires a switch that is already on a one, indicating it is on the "A" system, it would CONO request (IOB 29) with the new status. Now, when the "B" side is done with that switch or switches it would be cleared by a CONO RELEASE (IOB 31). This action causes an interrupt to the "B" system which would then poll the interrupt and find that bit IOB 31 is set indicating "A" released a device. In addition, the "B" side determines if a desired switch is available. If a switch is available, the "B" side issues a CONO containing the new status and takes the switch it requested.

When polling interrupts (performing a CONI), a CONO should always be issued with either the new status or the same status. This is required because if the status of the switches is to be changed, it should be preceded by issuing a CONI to read the status of the entire system. There is logic to stop the "A" system from selecting the same switch that is in the "B" system.

4.2 ERROR DETECTION

The switching error detection logic is enabled only during the CONO instruction. If the switch enable register is a one and a selected level comes back from the switch, no error condition occurs. If the selected level does not come back within 1 microsecond, an error condition is detected and the "A" error flip-flop is

set. The error generates an interrupt to the "A" system so the program will be notified of the error condition. The error could indicate that the switch is powered down, or the switch is in the local position, or a logic failure. In any case, that switched device did not get attached to the system. The program could notify the CTY of the error and tell the operator to locally switch the bus switch so the program could use this device.

If the two systems are running and one system detects a CPA error condition, such as Power Fail flag or parity errors, the monitor program can notify the failing system of its error. The other system then relinquishes its switched device to the system with the error condition. The logic uses bit IOB 32 which is the force interrupt bit and sets the force flip-flop in the "B" system. The "B" system performs a CONI to determine the cause of the interrupt. The CONI indicates bit IOB 32 is set and that all switch enable register flip-flops are zero which indicates the "B" system can have all system resources if desired.

Another condition which could occur is one system crashes with some of the system resources attached. The other system, through repeated requests, decides to perform an emergency take (bit IOB 30). This will grab all switched devices which have their corresponding bit set in the switch enable register. The condition in effect will take all switches if the "A" side has bits 20–27 set. The "B" side issues a CONO with bit IOB 30 set which clears the "A" latch flip-flop and sets the "B" latch flip-flop thus acquiring the system devices. This condition does not generate an interrupt to the "A" side because it is assumed the "A" side has crashed.

4.3 POWER FAILURE

If power is lost in the system, and then restored, the switch controller and switches come up zero ready for the monitor program to configure the system.

Power clear clears the switch controller thus releasing all switches attached to that system. Therefore, if the monitor program issues a system clear, the program must re-establish switch attachment by means of the CONI, CONO REQUEST.

SECTION 5
ACCEPTANCE TESTING

5.1 GENERAL

The DT03-CC test programs (DCDTA and DCDTB) detect errors and assist in diagnosing error causes. The programs are device code-independent and are capable of testing the I/O bus section in one pass. The programs operate in EXEC and USER modes. Interrupt logic is tested in EXEC mode only.

5.2 EXEC MODE ACCEPTANCE (DCDTA)

The switch controller section is tested during this test. For more information on the program operation, refer to the program listing. The switch settings are in the front section of the listing along with the loading and starting procedures. This test should be run for 15 minutes using both processors A and B together.

5.3 EXEC MODE ACCEPTANCE (DCDTB)

The interprocessor buffer is tested during this test. For loading and starting procedures, refer to the front section of the program listing. This program should be run for 15 minutes using both processors A and B together.

5.4 USER MODE TESTING

Diagnostics DCDTA and DCDTB can be run in I/O user mode only. Acceptance testing of this option is not necessary since all logic is tested in EXEC mode. In the user mode, some sections are omitted.

APPENDIX A
MODULE LIST

Type	Quantity	Function
M564	13	IO Bus Receiver
M921	4	Device Decoder Jumper Board
M664	12	IO Bus Driver
M151	2	Dual Binary-to-Octal Decoder
M111	10	Inverter
M112	11	Two-Input NOR Gate
M119	1	8-Input NAND Gate
M143	13	Two-Input NAND
M650	7	Negative Output Converter
M050	1	Inverter Driver
M500	2	Negative Bus Receiver
M612	4	6 Power Gates
M126	4	AND/OR Gate
M602	3	2 Pulse Amplifiers
M606	1	6 Pulse Amplifiers
M241	3	6 D Flip-Flop (1 common clock)
M243	6	8 D Flip-Flops (2 common clocks)
M246	4	5 D Flip-Flops
M171	3	2,2,2,3 AND, NOR
M311	4	Tapped Delay Line
M135	3	Three-Input NAND Gate
W023	10	18-Line Connector
M592	2	IO Device Select
Total =	124	