decsystem10

Advanced Systems Group

DT05-CS MEMORY
BUS SWITCH

digital

DT05-CS MEMORY
BUS SWITCH

SECTION 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

The DT05-CS Memory Bus Switch designed and manufactured by Digital is a solid state switching device. Use of the DT05-C allows either of two PDP-10 memory buses or MX10 Memory Data Multiplexor buses to communicate with a direct-memory-access (DMA) peripheral device connected to a switched memory or multiplexor bus. Switching of the DT05-CS can be controlled by either local or remote contact closures. The DT05-CS is composed basically of two sets of transistor gates; one set is associated with each multiplexer. The two sets of gates are arranged to provide, in effect, a 74-pole, three-position switch with a center Off position.

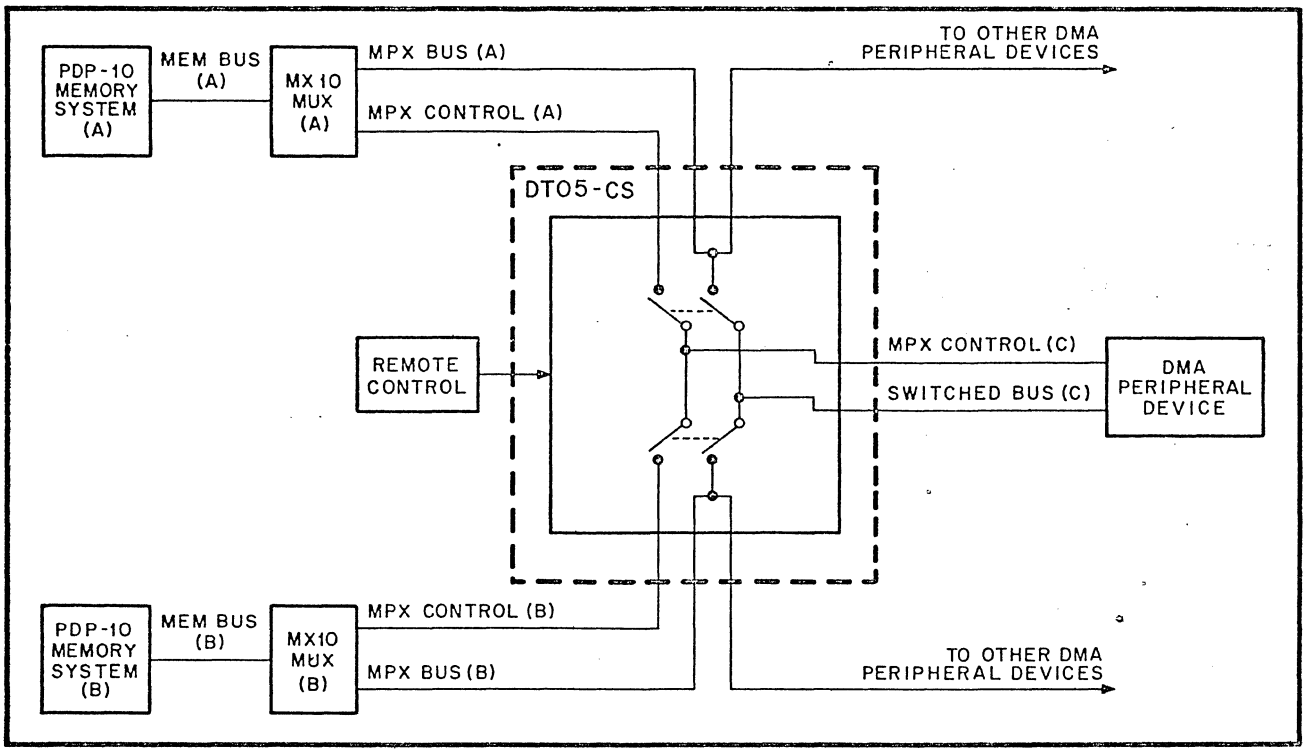

Figure 1-1 Simplified System Block Diagram

1.2 SPECIFICATIONS*

a. Mechanical:

Cabinet	Mounts in a DF10 Data Channel cabinet
Logic Panels	Two, Type H911
Dimensions	10-1/2 in. h, 19 in. w, 6-3/4 in. d
Weight	50 lb

b. Electrical:

Power Supply and Control	Controlled and provided by DF10
Power Dissipation	215W (180W at low duty factor)
Logic Potentials	+10V, -15V
Module Series	B and W-Series

c. Operational:

Switched Positions	Memory Bus A On/Off Memory Bus B On/Off
Normal Combinations**	(1) Memory Bus A On, Memory Bus B Off (2) Memory Bus A Off, Memory Bus B Off (3) Memory Bus A Off, Memory Bus On
Transfer Type	Bidirectional bus transfers allowed when switch combination (1) or (3) above is selected
Control	Local or remote contact closures
No. of Signals Switched	Seventy-Four

1.3 OPERATION

To connect the switched bus (Bus C) to either the PDP-10 (A) memory or the multiplexor bus (Bus A), the Remote A Control wire is connected to the common wire by means of a pair of local switch contacts or by a remote contact closure. Similarly, Bus C is connected to the PDP-10 (B) memory or multiplexor bus (Bus B) by connecting together the Remote B Control and Common wires. The normal sequence when switching Bus C from one memory bus to the other is to open the closed control pair before closing the other control pair. A single-pole, three-position control switch with a center Off position is recommended, wired as shown in Figure 1-2.

*Specifications are subject to change without notice.

**The two memory or multiplexor buses must never be simultaneously connected to the switched bus.

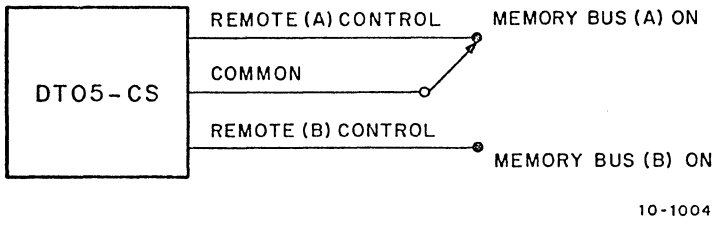

Figure 1-2 Switch Wiring

An equivalent circuit using relay contacts may optionally be used instead of the three-position switch circuit shown.

Each control pair controls a set of transistor gates associated with one of the two memory or multiplexor buses (Figure 1-3). When a control pair is open, the associated transistor gates inhibit the transfer of data between the associated memory or multiplexor bus and switched Bus C. When a control pair is closed, the associated transistor gates are enabled thus effectively connecting switched Bus C to the associated memory or multiplexor bus.

For bidirectional signal lines such as the memory bus data and parity lines, two sets of gates are used (one for each direction). The switching control logic section of the DT05-CS enables either the READ gates or the WRITE gates automatically upon monitoring the status of the WRITE Request and READ Request memory bus control lines. However, only those READ and WRITE gates enabled by the control pair are enabled by the switching control logic.

In addition to switching the memory or multiplexor bus signals, the DT05-CS also contains provisions for optionally switching the multiplexor control cable signals under the control of the same control pair used for bus switching.

1.4 AVAILABILITY

The DT05-CS is a product of Digital's DECsystem-10 Advanced Systems Group and is available, with new installations or for add-on to existing compatible systems, from engineering and manufacturing facilities in Maynard, Massachusetts. Main offices are located at 146 Main Street, Maynard, Massachusetts 01754.

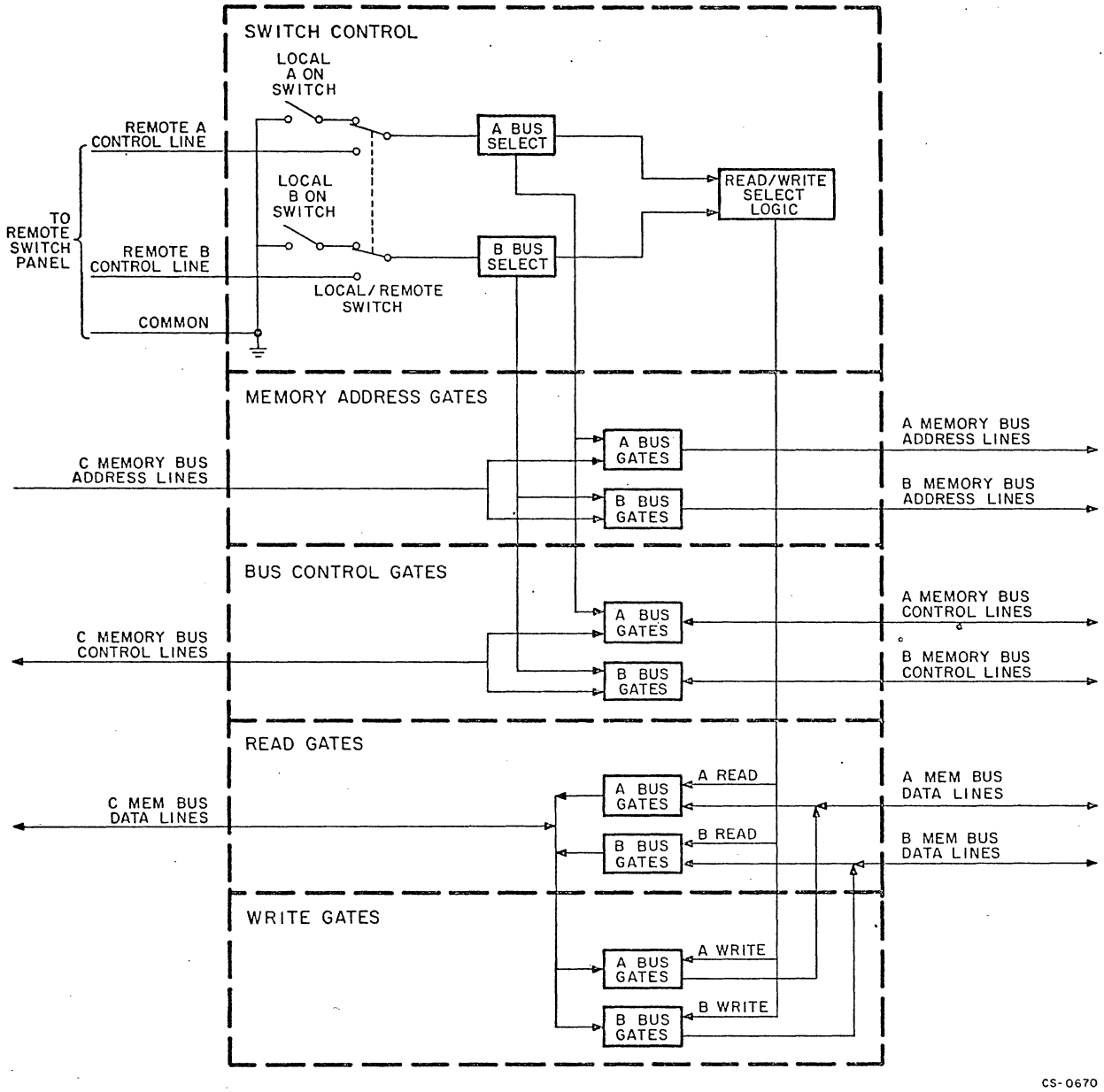

Figure 1-3 DT05-CS Block Diagram

SECTION 2
INSTALLATION

2.1 SITE CONSIDERATIONS

All general environmental requirements specified for the DECsystem-10 in the DECsystem-10 Site Preparation Guide also apply to the DT05-CS. The DT05-CS logic is on two Type H911 panels which mount in available space in a DF10 Data Channel 19 inch cabinet. Figure 2-1 shows the mounting method.

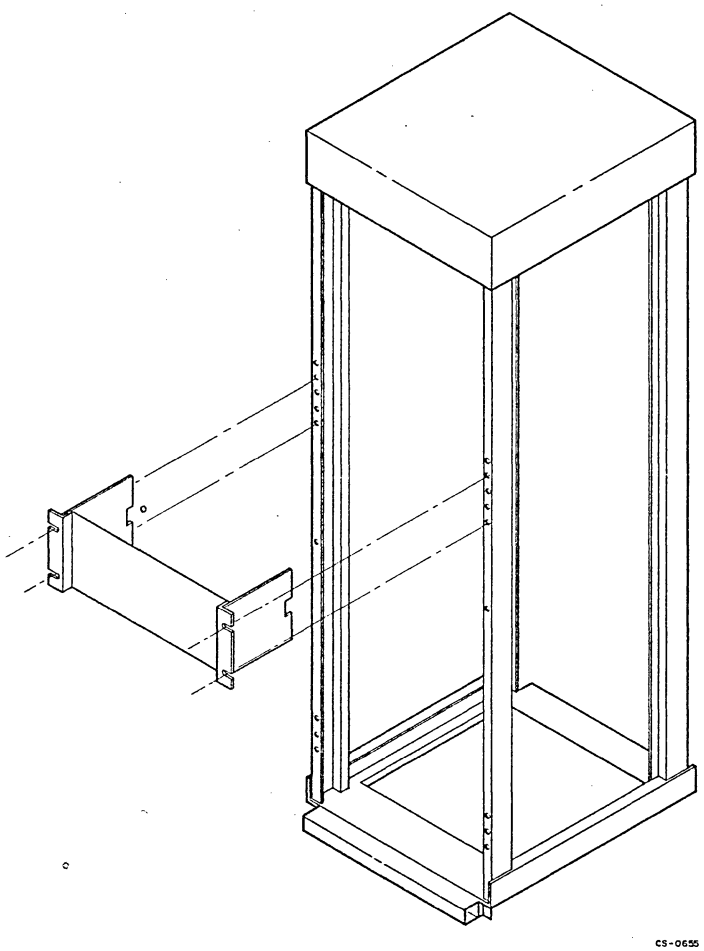

Figure 2-1 H911 Panel Mounting Details

The cabinet must be located so that the worst case multiplexor and/or memory bus length, including the switched bus, does not exceed 100 feet. In calculating the worst case bus length, an allowance of 20 feet should be made for propagation delay in the DT05-CS. When using an MX10 Memory Multiplexor to connect the DT05-CS to a memory bus, an additional 20 feet should be allowed for MX10 propagation delays.

Thus, for an MX10 and a DT05-CS in series, approximately 60 feet are allowed for the total bus length from the furthest memory unit to the peripheral controller on the switched bus.

Some examples of calculating the length of memory bus between devices are shown in Figure 2-2. The length between point A and point B is 100 feet. The lengths between both points A and C and A and D are 100 feet taking into account the allowance of 20 feet for propagation delay in the DT05-CS.

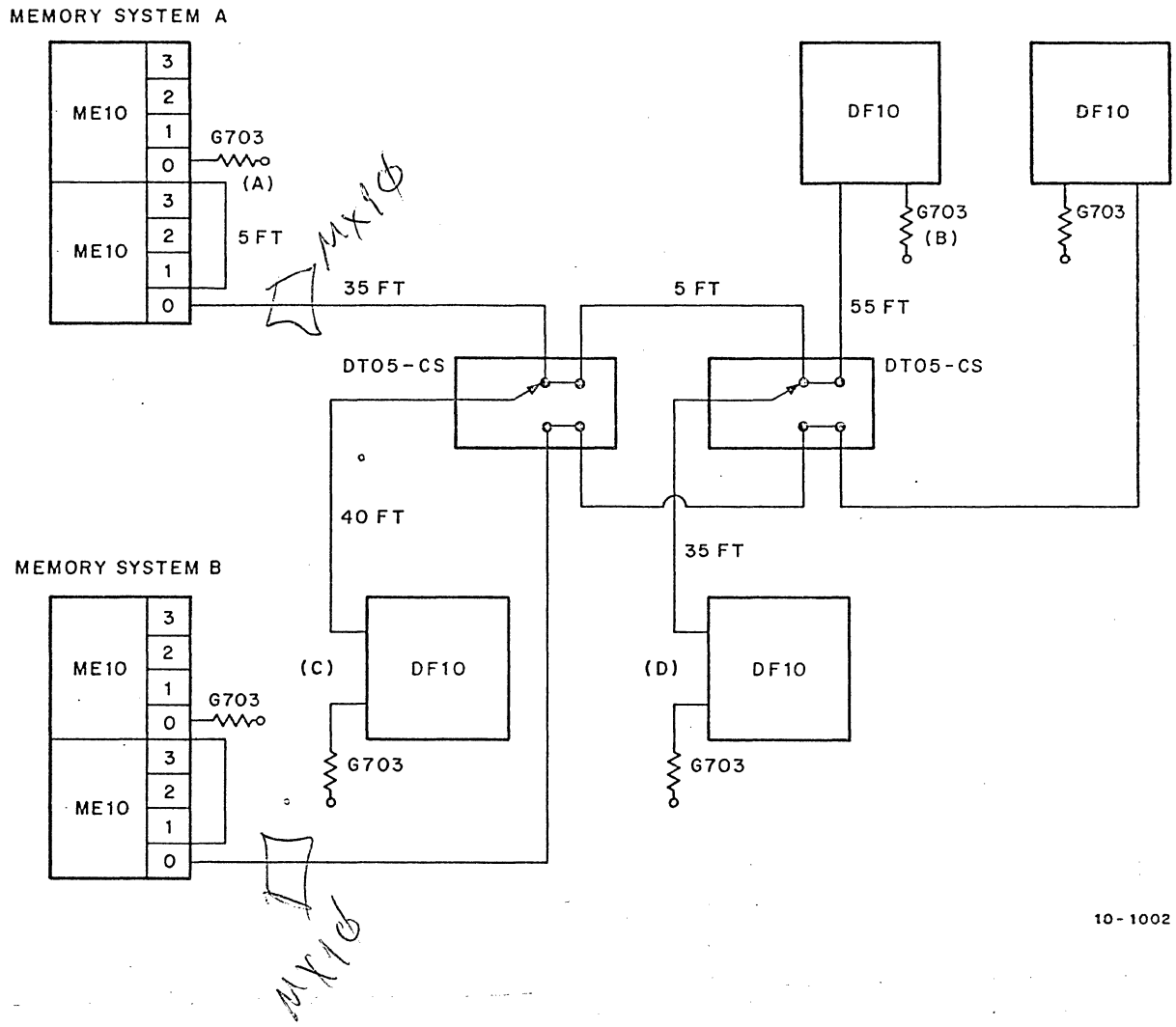

Figure 2-2 Memory Bus Length Calculation

2.1.1 Cooling

Cooling air is normally provided by a floor cutout in false-floor sites, or by raising the cabinet to provide air access in solid-floor sites. Air flow is in an upward direction and is exhausted at the top of the cabinet.

2.2 CABLES

Input and output slots are provided for the two cables associated with each of the two memory or multiplexor buses, thus the DT05-CS may be located anywhere along the memory or multiplexor bus of each PDP-10. One set of slots is provided for the two cables of the switched bus. Additional sets of slots are provided for the optional switching of multiplexor control cables. Refer to Appendix A for interface cable slot and pin information.

For installations involving the use of an MX10 Memory Multiplexor, the length of the multiplexor control cable from a DT05-CS to an MX10 should not be less than the total multiplexor bus length between the DT05-CS and the MX10.

The control wires from the remote control switches to the DT05-CS should be twisted and shielded. For those installations in which a DT03-CS I/O Bus Switch, in conjunction with a DT05-CS, switches a controller from one system to another, the same remote contacts used to switch the DT03-CS may also be used to switch the DT05-CS. This is accomplished by connecting the remote control wires from the DT05-CS to special terminals on the DT03-CS Remote Control Cable Connector Module (W023), specifically provided for this purpose.

The ac and dc electrical power wiring for a typical DT05-CS logic panel is shown in Figure 2-3.

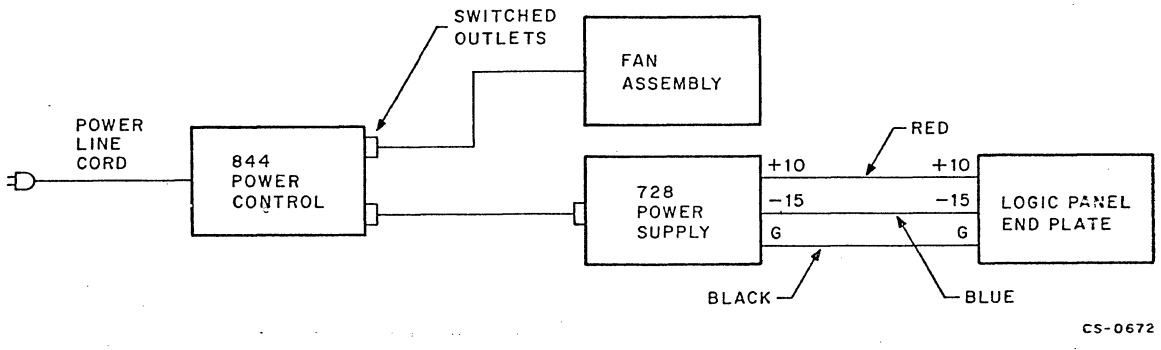

Figure 2-3 Typical Power Wiring

2.3 GROUNDING

The control wire shield is grounded at the DT05-CS. The shield may be optionally grounded at the remote control switch panel; however, the control wires should remain isolated from any grounding points at the remote control switch panel.

The remote control wires are customer-provided. All other cables required by the addition of the DT05-CS are provided by DEC.

2.4 TURN-ON PROCEDURE

To place the DT05-CS in its normal operating condition, place the associated type 844 Power Control (Figure 2-4) circuit breaker ON and the Local/Off/Remote switch to the LOCAL position. Then switch the DT05-CS Local/Remote switch to the REMOTE position. The A ON and B ON indicators should never be illuminated simultaneously.

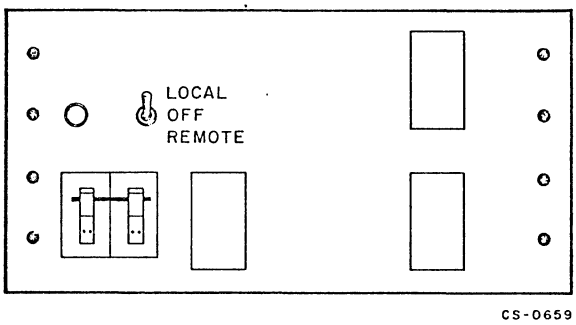

Figure 2-4 Type 844 Power Control Panel

2.5 ACCEPTANCE TEST

The DT05-CS logic meets the acceptance requirements if the diagnostic test associated with the controller connected to the switched bus runs without a DT05-CS caused error. The diagnostic program should be run twice, once for each switched position.

2.6 RELATED DOCUMENTS

The following documents contain material that supplements the information in this Option Description.

Title	Date	Document No.
PDP-10 Interface Manual	4/70	10-HIFC-D
MX10 Memory Data Multiplexor Maintenance Manual	5/69	10-HICA-D
DF10 Data Channel Maintenance Manual	9/71	10-HDFC-D
DECsystem-10 Site Preparation Guide	4/72	10-HAAB-D

2.7 EQUIPMENT FURNISHED

Appendix B contains a list of the components which comprise a complete DT05-CS option.

SECTION 3
OPERATION AND PROGRAMMING

3.1 CONTROLS

The DT05-CS contains three local control switches (Drawing C-UA-DT05-CS-0). These perform the following functions:

a. LOCAL/REMOTE: This DPDT switch allows control of the DT05-CS from the remote control switches, or locally from DT05-CS maintenance switch assembly.

b. A ON/A OFF: This SPST switch connects (A ON) or disconnects (A OFF) switched Bus C from memory Bus A.

c. B ON/B OFF: This SPST switch connects (B ON) or disconnects (B OFF) switched Bus C from memory Bus B.

A ON and B ON must never be selected simultaneously; this has the effect of connecting switched Bus C to both memory (or multiplexor) buses simultaneously.

In normal operation, the LOCAL/REMOTE switch is set to the REMOTE position. This disables the remaining two local control switches and enables the remote control contacts. As an option, relay contacts may replace the switch for the remote control function; simultaneous closure of both control wires to the common wire must not be allowed.

When the LOCAL/REMOTE switch is set to the LOCAL position, the remote control contacts are disabled and the remaining two local control switches are enabled. Each of these two local control switches controls one control wire and is usually used for maintenance purposes.

Power is controlled by an 844 Power Control (Figure 2-4). See Paragraph 2.4 for the turn-on procedure.

3.2 PROGRAMMING CONSIDERATIONS

Although the DT05-CS is not programmable, the capability of programmable switching can be realized by adding a separate programmable device. This device would be used to control the opening and closing of the remote control lines.

During the time interval within which the DT05-CS is switching from one bus to another, no bus signal transfers should be in process on any bus connected to the DT05-CS.

3.3 OPERATION

The 71 memory bus signals switched by the DT05-CS are carried on the following lines:

36	Bidirectional Data Lines
1	Bidirectional Parity Line
27	Memory Address Lines
7	Memory Bus Control Lines
71	Total

In addition to these lines, the DT05-CS provides for the optional switching of the three Multiplexor Control Line signals, thus a total of 74 signals may be switched by the DT05-CS. When a control wire is open, the transistor gates associated with that wire inhibit the transfer of signals in either direction, thus effectively disconnecting the signal lines on the associated memory or multiplexor bus. The voltage levels existing at the open control pair contacts are approximately -6V and 0V.

Upon closing a control wire circuit, the 0V ground potential is applied to the switching control logic. This enables all unidirectional transistor gates associated with that control wire. The switching control logic also enables either the READ or WRITE gates associated with that control wire, depending upon the status of the "RD RQ" and "WR RQ" lines at the time of the active "REQ CYC" level on the bus control lines. Additionally, the gates isolate the switched bus from the memory or multiplexor bus, thus preventing undesired reflections and impedance mismatches. Signals are regenerated by the DT05-CS in the same manner used by the MX10.

SECTION 4
THEORY OF OPERATION

This section should be read in conjunction with the DT05-CS Engineering Drawing Set (DT05-CS-0).

4.1 SWITCH CONTROL (Drawing D-BS-DT05-CS-02)

Drawing D-BS-DT05-CS-02 shows all signals associated with switching control within the DT05-CS. The Local/Remote Switch (S3) selects either the remote control lines or the local control switches (S1 and S2) as the inputs to the W501 Schmitt Triggers (C32 and D32). A ground applied to a W501 input causes a low (-3V) level to be applied the associated W051 Indicator Driver and B685 Bus Driver which lights the associated indicator and generates the corresponding A ON or B ON low level. This level is one of the inputs used by the B685 Bus Drivers.

4.1.1 Read/Write Control

The remaining input to the Bus Drivers is the output of the RDWR flip-flop which determines whether the Read gates or the Write gates associated with A ON or B ON become enabled. A low on RDWR pin D enables the Write gates. A low on RDWR pin E enables the Read gates. The quiescent state of RDWR is the "Write Enabled" state with a low on RDWR pin D.

During the beginning of a Write cycle, the C ADR ACK signal received from the ME10 in response to a C REQ CYC signal is gated with the C WR RQ signal to produce a positive transition at B29F. This transition resets RDWR pin D to a low "Write Enable" level, if it was not already in that state. Because this is the normal quiescent state of the RDWR flip-flop, no further action is required at the completion of the Write cycle.

During the beginning of a Read cycle, the C ADR ACK signal received from the ME10 in response to a C REQ CYC signal is gated with the C RD RQ signal to produce a positive transition at B29L. This transition sets RDWR pin E to a low "Read Enable" level.

At the end of a Read cycle, the C RD RS signal in conjunction with the ENDRD flip-flop resets the RDWR flip-flop to the quiescent "Write Enable" state. The negative transition of C RD RS is inverted at B29V to trigger ENDRD pin N to a low level. The positive transition at the trailing edge of C RD RS is inverted at B29V and, with the low level at END RD pin N, provides a positive transition at B29R. This transition, after a 40-60 ns delay, triggers RDWR pin D to the desired low quiescent level. The corresponding positive transition of RDWR Pin E triggers ENDRD Pin N to a high level, which causes B29R to return to a low level. This allows the RDWR flip-flop to be triggered to the "Read Enable" state whenever the next Read cycle begins.

4.1.2 Gating Signals

Each B685 has three signals at its output. These are identical, dividing the load among three output pins. Essentially six different switch gating signals exist: A CON, B CON, A RD, A WR, B RD and B WR. Signal A CON gates unidirectional signals between the A Bus and the C Bus. Signal A RD gates the MBD

and Parity signals from A Bus to C Bus during read cycles. Signal A WR gates the MBD and parity signals from C Bus to A Bus during write cycles. The B RD and B WR control levels gate those same signals in a similar manner between the B Bus and C Bus. The enabling state of each of these six different signals is a low (-3V). Signals A CON, A RD and A WR are all disabled whenever C32 pin U is ungrounded. Similarly, B CON, B RD and B WR are all disabled whenever D32 pin U is ungrounded.

4.2 MEMORY ADDRESS GATES (Drawing D-BS-DT05-CS-03)

Drawing D-BS-DT05-CS-03 shows the gating of the MADR signals from the C Bus to either the A Bus or the B Bus. The B683 Bus Driver gates a given MADR signal without inverting; the gating signal is either A CON or B CON. The CROBAR signal from the Power Control, whenever at ground level, inhibits the B683 output. Upon turning off or losing power, the CROBAR signal transitions immediately to ground, thus preventing transients from being inserted into the memory bus. Approximately four seconds after normal power resumes, the CROBAR signal returns to a low level.

4.3 BUS CONTROL GATES (Drawing D-BS-DT05-CS-04)

Drawing D-BS-DT05-CS-04 shows the gating of additional signals by the A CON and B CON gating signals. The W132 Pulsed Bus Transceiver, when enabled, generates a nominal 100 ns negative-going pulse upon receiving a negative input pulse of 30 to 100 ns. To minimize propagation delay, only the transmit portion of the W132 is used in the DT05-CS. The receive portion of the W132 is gated permanently off by grounding pin D of each W132.

4.4 READ GATES (Drawing D-BS-DT05-CS-05)

Drawing D-BS-DT05-CS-05 shows the gating of all MBD signals to the C Bus from either the A Bus or the B Bus by the respective A RD or B RD gating signals. Again, only the transmit portion of each W102 is used. Each MBD signal is twisted with a ground wire to minimize crosstalk, reflections, and other interference.

4.5 WRITE GATES (Drawing D-BS-DT05-CS-06)

Drawing D-BS-DT05-CS-06 shows the gating of all MBD signals from the C Bus to either the A Bus or the B Bus by the respective A WR and B WR gating signals.

SECTION 5
MAINTENANCE

5.1 GENERAL

An oscilloscope and a multimeter are required for maintaining the DT05-CS. No special test equipment is needed. Figure 5-1 shows the standard DEC method for designating module slots and pins.

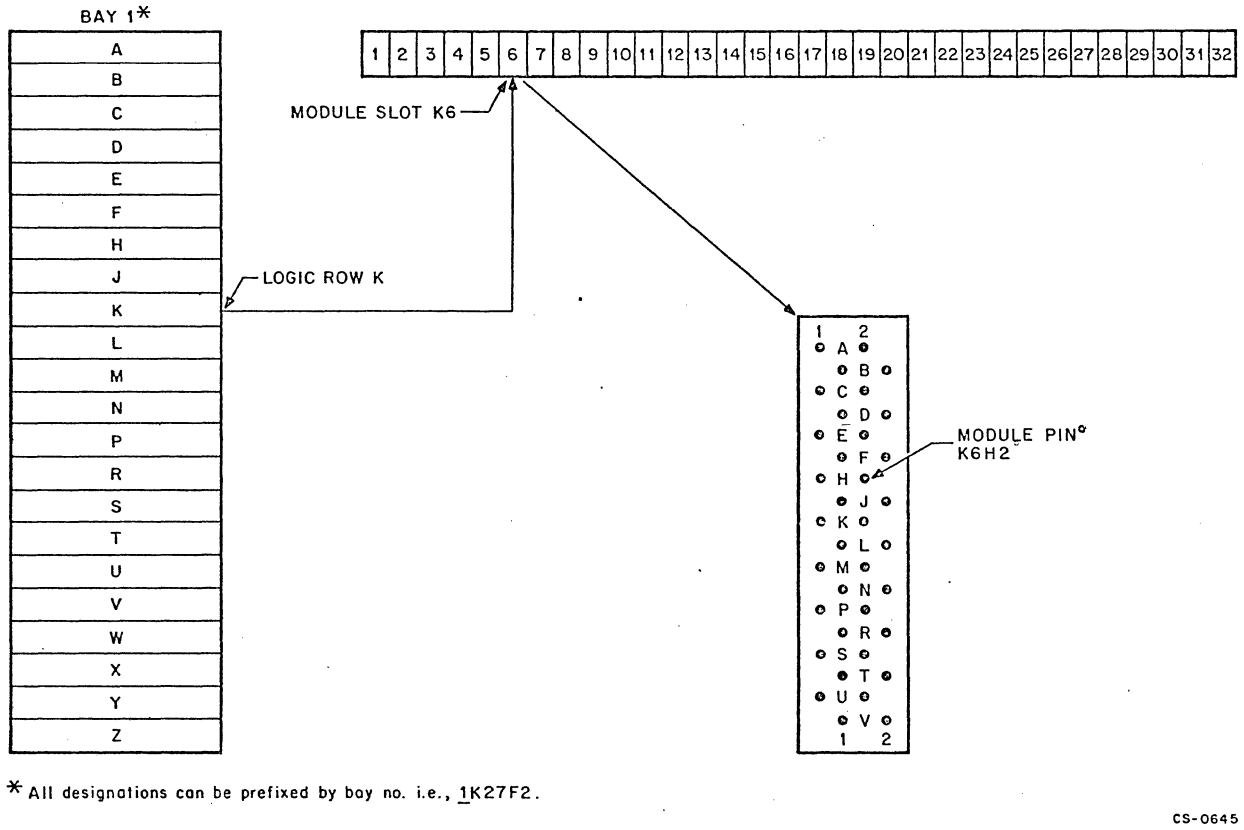

Figure 5-1 Module Slot Designation Example

5.2 MAINTENANCE TECHNIQUES

No preventive maintenance or special test procedures apply. Proper operation of each DT05-CS is validated by performing the diagnostic tests associated with the controller connected to the switched bus. The diagnostic program should be run twice, once for each switched position.

5.3 MARGIN SPECIFICATIONS

Rack	+10V	-15V
A	17.5 6.0	17.5 12.0
B	17.5 6.0	17.5 12.0
C	17.5 6.0	17.5 12.0
D	17.5 6.0	17.5 12.0

SECTION 6
MODULES

6.1 MODULE LIST

Table 6-1 lists the DT05-CS modules by type number, function, quantity in use and suggested spare quantities. Refer to the Module Utilization section of the Engineering Drawing set for module slot assignments.

Table 6-1
Module Complement

DEC Type No.	Description	No. In Use	Suggested Spares
B133	Diode Gate	1	1
B212	Delayed Flip-Flop	1	1
B683	Bus Driver	22	3
B685	Diode Gate Driver	6	1
G700	100 Ω Terminator	1	1
G703	100 Ω Terminator	4	1
W051	100 mA Indicator and Relay Driver	1	1
W102	Pulsed Bus Transceiver	6	1
W132	Pulsed Bus Transceiver	36	5
W501	Schmitt Trigger	2	1

APPENDIX A
REMOTE CONTROL INTERFACE INFORMATION FOR DUAL-PROCESSOR/DUAL-CONTROLLER INSTALLATIONS

A.1 GENERAL INFORMATION

Confusion can arise in accomplishing control wire connections in Dual-Processor/Dual-Controller installations because of the identical control line designations associated with the bus and line printer switches.

Table A-1 lists the control signals with the associated pin and slot connections for each device. This information should provide for rapid cable identification.

Table A-1

Control Line Pin Connections

Signal	LP10-SW		DT03-CS		DT05-CS	
	Slot	Pin	Slot	Pin	Slot	Pin
REMOTE A	B29	E	A32	K	B32	E
COMMON	B29	F	A32	J	B32	F
REMOTE B	B29	H	A32	L	B32	H
A			A32	P*		
GND			A32	N*		
B			A32	R*		
SHIELD	B29	J	A32	F		

NOTE

A break-before-make contact set can be used to connect COMMON to either REMOTE A or REMOTE B if desired.

*These pins can be used to provide the remote control signals for a DT05-CS thereby providing the means by which a single set of remote control lines can simultaneously switch a DT03-CS and a DT05-CS.

Table A-2 lists the DT05-CS Interface Cable slot assignments.

Table A-2

DT05-CS Interface Cable Slots

Cable	Slot Location
A Memory Bus Cable No. 1	A, B/1-4
A Memory Bus Cable No. 2	C, D/1-4
B Memory Bus Cable No. 1	A, B/23-26
B Memory Bus Cable No. 2	C, D/27-30
C Memory Bus Cable No. 1	A, B/12-15
C Memory Bus Cable No. 2	C, D/14-17
A MPX Control	A27
B MPX Control	A29
C MPX Control	A28
Remote Control	B32

APPENDIX B
SHIPPING LIST

B.1 EQUIPMENT FURNISHED

A complete DT05-CS Memory Bus Switch consists of the following:

a. DT05-CS logic on two H911 panels including all modules (1 ea).

b. Type BC10-H Memory Bus cable assemblies (4 ea).

c. Type 7405556 MPX control cable assemblies (2 ea).

d. Engineering Drawing Set, DT05-CS-0 (1 ea).

e. Option Manual (1 ea).