

pdp11

MF11S-K
MOS memory
technical manual

digital

**MF11S-K
MOS memory
technical manual**

digital equipment corporation • maynard, massachusetts

Copyright © 1977 by Digital Equipment Corporation

The material in this manual is for informational purposes and is subject to change without notice.

Digital Equipment Corporation assumes no responsibility for any errors which may appear in this manual.

Printed in U.S.A.

This document was set on DIGITAL's DECset-8000 computerized typesetting system.

The following are trademarks of Digital Equipment Corporation, Maynard, Massachusetts:

DEC	DECtape	PDP
DECCOMM	DECUS	RSTS
DECsystem-10	DIGITAL	TYPESET-8
DECSYSTEM-20	MASSBUS	TYPESET-11
		UNIBUS

CONTENTS

	Page
CHAPTER 1 INTRODUCTION	
1.1 GENERAL FUNCTIONAL DESCRIPTION	1-1
1.2 PHYSICAL DESCRIPTION	1-1
1.2.1 The Control Module (M7893).....	1-1
1.2.2 The Array Module (M7984).....	1-1
1.2.3 MF11S-K Memory Size.....	1-1
1.2.4 Internal Memory Bus	1-1
1.3 MAINTENANCE AND RELIABILITY	1-1
1.4 BATTERY SUPPORT MODE.....	1-5
1.5 SPECIFICATIONS	1-5
1.5.1 Unibus Interface.....	1-5
1.5.2 Power Supply Requirements.....	1-5
1.5.3 Access and Cycle Times	1-9
1.5.3.1 Memory Storage.....	1-9
1.5.3.2 Refresh Cycle	1-9
1.5.3.3 ECC INIT Routine.....	1-9
1.5.3.4 Control and Status Register (CSR)	1-10
1.6 BACKPLANE UTILIZATION.....	1-10
CHAPTER 2 FUNCTIONAL DESCRIPTION OF THE ERROR CORRECTION LOGIC	
2.1 GENERAL.....	2-1
2.2 MODIFIED HAMMING CODE AND CHECK BITS.....	2-1
2.3 MEMORY WORD SIZE	2-2
2.4 USE OF THE 39-BIT MEMORY WORD.....	2-2
2.5 READ OPERATION (DATI AND DATIP).....	2-2
2.5.1 Accessing the Data	2-2
2.5.2 Generation of Syndrome Bits.....	2-2
2.5.3 Example A, Data Bit 0 Set	2-2
2.5.4 The Error Correction Process	2-7
2.5.5 Example B, Handling a Double Error	2-7
2.5.6 Handling a Check Bit Error, Example C	2-8
2.6 WRITE OPERATION IN GENERAL (DATO AND DATOB).....	2-8
2.7 WRITE OPERATION FOLLOWING A DATIP.....	2-9
2.7.1 No Single Error Detected.....	2-10
2.7.2 Single Error Detected	2-10
2.8 WRITE OPERATION NOT FOLLOWING A DATIP.....	2-10
2.8.1 Error Detection on a Write	2-13
2.8.2 Double Error Condition	2-13
2.8.3 Single Error Condition	2-13

CONTENTS (CONT)

		Page
CHAPTER 3	MOS CHIP DESCRIPTION	
3.1	PHYSICAL DESCRIPTION	3-1
3.2	FUNCTIONAL DESCRIPTION	3-2
3.2.1	The Cell Storage Element	3-3
3.2.2	Read, Write, and Refresh	3-3
3.2.3	Timing	3-3
CHAPTER 4	MS11-KA STORAGE ARRAY MODULE: DETAILED EXPLANATION	
4.1	GENERAL.....	4-1
4.2	INTERNAL MEMORY BUS	4-1
4.2.1	Data and Check Bit Lines	4-1
4.2.2	Address Lines	4-1
4.2.3	Write Byte Lines Select and Modified Address	4-1
4.2.4	Memory Select Lines	4-1
4.2.5	Refresh and Selection and Memory Present Lines	4-3
4.2.6	Other Control Signals.....	4-3
4.3	POWER DISTRIBUTION.....	4-3
4.4	ARRAY MODULE FUNCTIONAL LAYOUT	4-4
4.5	ADDRESS BIT FUNCTIONS	4-4
4.6	ADDRESS RECEIVER CIRCUITRY	4-4
4.7	RAS AND CAS TIMING SIGNAL BUFFERS	4-4
4.8	TRISTATE DATA DRIVERS AND RECEIVERS	4-4
CHAPTER 5	THE CONTROL MODULE: DETAILED EXPLANATION	
5.1	GENERAL.....	5-1
5.2	DATA PATH	5-1
5.2.1	Data In Path.....	5-1
5.2.2	Data Out Path	5-1
5.3	ERROR CORRECTION LOGIC	5-2
5.3.1	Error Correction Logic on a Data In.....	5-2
5.3.2	ECC Logic on a Write Cycle	5-2
5.4	ADDRESS DECODER LOGIC.....	5-10
5.4.1	Address Bits 14-17.....	5-10
5.4.2	Address Bits 13-2	5-17
5.4.3	Address Bits 1 and 0.....	5-19
5.5	TIMING CHAIN	5-19

CONTENTS (CONT)

	Page
CHAPTER 6	MEMORY CYCLES
6.1	GENERAL.....6-1
6.2	READ CYCLE (DATI, DATIP)6-1
6.2.1	Fetching the Data, DATI/DATIP.....6-1
6.2.2	Checking the Double Word (No Error Found), DATI/DATIP.....6-13
6.2.3	Checking the Double Word (Single Error), DATI/DATIP6-14
6.2.4	Checking the Double Word (Double Error), DATI/DATIP6-19
6.3	WRITE CYCLE (DATO, DATOB) NOT FOLLOWING A DATIP6-23
6.3.1	Generating the Syndrome Bits (DATO/DATOB Not Following DATIP)...6-23
6.3.2	Gating Bytes to be Written to the MDR (DATO/DATOB Not Following DATIP)6-23
6.3.3	Manipulation of Syndrome and Check Bits (No Error) (DATO/DATOB Not Following DATIP).....6-23
6.3.4	Writing the New Data and Check Bits.....6-30
6.3.5	Manipulation of Syndrome and Check Bits (Single Error) (DATO/DATOB Not Following DATIP).....6-30
6.3.6	Handling a Double Error on a Write Cycle, Not Following DATIP6-35
6.4	WRITE CYCLE FOLLOWING A DATIP.....6-35
6.4.1	Data Manipulation (Single Error in Byte to be Written) (DATO/DATOB Following DATIP).....6-35
6.4.2	Data Manipulation (Single Error not in Byte to be Written) (DATO/DATOB Following DATIP).....6-45
6.4.3	Data Manipulation (No Error) (DATO/DATOB Following DATIP).....6-45
6.5	MEMORY REFRESH CYCLE6-45
6.5.1	Refresh Request6-45
6.5.2	Refresh Cycle Addressing6-47
6.5.3	Refreshing the Cells6-47
6.5.4	Ending the Refresh Cycle.....6-47
6.6	ECC INITIALIZATION CYCLE.....6-52
6.6.1	Triggering the ECC Initialization Cycle6-54
6.6.2	ECC Initialization Addressing6-57
6.6.3	Data and Check Bits6-57
6.6.4	Ending the ECC Initialization Algorithm.....6-58
6.7	MEMORY CYCLE CONFLICTS.....6-58
6.8	BATTERY SUPPORT MODE OPERATION6-58

CONTENTS (CONT)

	Page
CHAPTER 7	CSR FUNCTION AND LOGIC
7.1	GENERAL.....7-1
7.2	WRITING TO THE CSR.....7-1
7.3	READING THE CSR.....7-1
7.4	CSR BIT FUNCTIONS.....7-4
7.4.1	Double Error Indication Enable (CSR Bit 0).....7-4
7.4.2	Disable Error Correction Mode (CSR Bit 1).....7-4
7.4.3	Diagnostic Check Mode (CSR Bit 2).....7-4
7.4.4	Inhibit Mode Pointer (CSR Bit 3).....7-6
7.4.5	Single Error (CSR Bit 4).....7-7
7.4.6	Address and Check Bit Storage (CSR Bits 11-5).....7-7
7.4.7	Set Inhibit Mode (CSR Bit 13).....7-7
7.4.8	Double Error (Bit 15).....7-7
CHAPTER 8	INSTALLATION OF THE MF11S-K MEMORY
8.1	GENERAL.....8-1
8.2	DD11-K BACKPLANE SLOT ALLOCATION.....8-1
8.3	MF11S-K OPTIONS.....8-2
8.3.1	MF11S-K (32K MOS System Complete).....8-2
8.3.2	MS11-KA (32K × 16 MOS Array Module).....8-2
8.3.3	Options Required Per Storage Capacity.....8-2
8.4	MIXING THE MF11S-K AND OTHER MEMORIES.....8-7
8.4.1	Address Space Above MF11S-K.....8-7
8.4.2	Address Space Below MF11S-K.....8-7
8.5	SUPPLY VOLTAGES.....8-7
8.6	FIRST TIME START-UP.....8-7
CHAPTER 9	TROUBLESHOOTING THE MF11S-K
9.1	GENERAL.....9-1
9.2	ECC INITIALIZATION.....9-1
9.3	PROCEDURE TO ISOLATE FAULTS THAT PREVENT LOADING
	DIAGNOSTICS.....9-1
9.3.1	Array Module Swap.....9-1
9.3.2	Initial Check.....9-1
9.3.3	Timing Check.....9-2
9.3.4	SSYN Check.....9-2
9.3.5	CSR Address Decode.....9-2
9.3.6	ECC Initialization Check.....9-2
9.3.7	Refresh Cycle Check.....9-2
9.3.8	ECC Initialization Cycle.....9-2
9.3.9	Double-Bit Error Indication.....9-2

CONTENTS (CONT)

		Page
9.3.10	Disable Error Correction.....	9-2
9.3.11	Bit Check	9-5
9.3.12	No Double Error.....	9-5
9.3.13	Error Before ECC.....	9-5
9.3.14	Data Equals 1s	9-5
9.3.15	Data Shorts Check	9-5
9.3.16	Address Circuits Check	9-5
9.3.17	Toggle In Memory Test	9-5
9.4	CLEARING A DOUBLE ERROR	9-6
9.5	FORCING AN INTERNAL WRITE	9-7
9.6	MOS CHIP REPLACEMENT	9-7
9.7	HARDWARE REMOVAL OF ONE 8K MEMORY SEGMENT	9-7

APPENDIX A IC DESCRIPTIONS

APPENDIX B SIGNAL NAME GLOSSARY

APPENDIX C SIGNAL NAMES WITH PIN LISTS

FIGURES

Figure No.	Title	Page
1-1	Backplane with Controller and Array Modules.....	1-2
1-2	Simplified MF11S-K System Block Diagram	1-2
1-3	MF11S-K Control Module.....	1-3
1-4	MF11S-KA Array Module.....	1-4
2-1	Modified Hamming Code Matrix	2-1
2-2	Read Cycle Flowchart	2-3
2-3	ECC Logic Used on a Read Cycle Block Diagram	2-5
2-4	Syndrome Bit Decoding	2-7
2-5	Write Cycle Flowchart	2-9
2-6	ECC Logic Used on a Write Cycle	2-11
2-7	Read-Modify-Write Cycle Flowchart	2-12
3-1	MOS RAM Chip Pin Connections	3-1
3-2	(4096 × 1) Bit MOS Chip, Block Diagram	3-2
3-3	MOS Chip, Simplified Data Gating.....	3-4
3-4	Read Cycle Timing.....	3-5
3-5	Chip Write Timing	3-5
3-6	Read-Modify-Write Timing	3-6

FIGURES (CONT)

Figure No.	Title	Page
4-1	Array Module Block Diagram.....	4-2
4-2	Internal Memory Bus	4-3
4-3	Functional Layout of Array Module	4-5
4-4	Address Bit Functions.....	4-7
4-5	Distribution of Internal Bus Write Byte Signals	4-8
4-6	Fanout of Address Signals, Example Address Bit 0.....	4-9
4-7	Distribution of RAS Signals	4-11
4-8	Distribution of CAS Timing Signal.....	4-13
4-9	Distribution of the Chip Select Signal	4-15
4-10	MOS Chip Control and Data Bit Driver/Receiver	4-17
5-1	Control Module Block Diagram.....	5-3
5-2	Data Path.....	5-5
5-3	Data Path and Error Correction Logic Block Diagram	5-7
5-4	Decoder to Correct Data Bit in Error	5-9
5-5	PROM	5-9
5-6	Check Bit Correction.....	5-11
5-7	Address Decoder Logic Block Diagram	5-13
5-8	Address Bit 14-17 and Associated Logic.....	5-15
5-9	Row, Column, and Refresh Address Multiplexer Associated Logic.....	5-18
5-10	Qualifying MEM GO L.....	5-20
5-11	Generation of TIM ST H.....	5-21
5-12	Starting the Timing Chain on a Refresh Cycle.....	5-21
5-13	Starting the Timing Chain on a Data Cycle.....	5-21
5-14	Triggering the Delay Line DL 1	5-23
6-1	Resetting the Syndrome Latches on a Read	6-3
6-2	Read Cycle Flowchart	6-5
6-3	Read Cycle Timing Diagram	6-7
6-4	Column Address Timing Logic.....	6-9
6-5	INT BUS DR ENB Signal.....	6-10
6-6	Clocking the MDR.....	6-11
6-7	Setting the SSYN Flip-Flop.....	6-13
6-8	Data Word Selection	6-14
6-9	Delay Line DL 2 and DL 4.....	6-15
6-10	Error Detection and CSR Bit 4 Logic.....	6-17
6-11	Decoder to Correct Data Bit in Error.....	6-19
6-12	CSR Bit 15 and Associated Logic.....	6-20
6-13	CSR Bits 5-11 and Associated Logic.....	6-21
6-14	DATIP Cycle Flip-Flop.....	6-22
6-15	Read-Modify-Write Cycle Timing Diagram.....	6-25
6-16	DATO/DATOB Cycle Flowchart	6-27
6-17	Latching Unibus Data on a Write Cycle.....	6-29
6-18	Internal Read-Modify-Write Flip-Flop.....	6-30
6-19	Generation of INT BUS WR TIM L.....	6-31

FIGURES (CONT)

Figure No.	Title	Page
6-20	Clearing the RAS Timing Flip-Flop.....	6-33
6-21	Clearing the MBSY and Internal Read-Modify-Write Flip-Flops	6-34
6-22	Generation of Write Byte Signals.....	6-37
6-23	Write Cycle Timing Diagram (Following DATIP)	6-39
6-24	Write Timing Logic	6-41
6-25	Refresh Control and Timing Logic	6-43
6-26	Memory Cycle Initiation Logic.....	6-46
6-27	Refresh Cycle Flowchart	6-48
6-28	Refresh and ECC INIT Cycles, Timing Diagram	6-49
6-29	Refresh Address Counter.....	6-51
6-30	RAS and CAS Timing Flip-Flops.....	6-52
6-31	ECC INIT Cycle Flowchart.....	6-53
6-32	Battery Back-Up Voltage Detection Vout vs +5 VBB on Power Up	6-54
6-33	Battery Voltage Detection and ECC INIT Flip-Flop.....	6-55
7-1	CSR Bit Allocation	7-2
7-2	CSR/Data Multiplexer, a 4-Bit Slice	7-3
7-3	Generation of ECC DIAG CK L and ECC DIS L Signals.....	7-5
7-4	CSR/Check Bit Multiplexer and Check Bit Register.....	7-5
8-1	DD11-L Backplane Utilization.....	8-3
8-2	DD11-K Backplane Unibus Routing.....	8-5
8-3	Fully Configured DD11-K Backplane	8-6
9-1	No Load Fault Isolation Flowchart.....	9-3
9-2	Array Module Jumper Configuration	9-7

TABLES

Table No.	Title	Page
1-1	Backup Battery Power Requirements	1-5
1-2	Unibus Loading	1-5
1-3	Power Supply Requirements.....	1-6
1-4	System Power.....	1-7
1-5	Memory Storage – Access and Cycle Times	1-9
1-6	Refresh Repetition Rate.....	1-9
1-7	CSR Access	1-10
2-1	Syndrome Bit Generation.....	2-4
2-2	Error Correction, Example A	2-4
2-3	Double Error, Example B.....	2-8
2-4	Check Bit Error, Example C	2-8

TABLES (CONT)

Table No.	Title	Page
3-1	Chip Supply Voltages	3-1
5-1	Starting Address Selection	5-17
5-2	Multiplexer States	5-19
6-1	Memory Data Cycle Selection	6-1
7-1	CSR Address Modification	7-1
7-2	CSR/Data Multiplexer (74157)	7-4
7-3	Data Modification Through the Check Bits	7-6
C-1	Internal Memory Bus Signals.....	C-1

CHAPTER 1

INTRODUCTION

1.1 GENERAL FUNCTIONAL DESCRIPTION

The MF11S-K memory is an MOS, semiconductor, random access memory (RAM) designed to interface with the PDP-11 Unibus. It utilizes an error correction scheme that makes the MF11S-K more reliable than standard memory systems. The memory storage matrix is arranged in 39-bit words: two 16-bit PDP-11 words plus seven check bits. The check bits are used to indicate the integrity of the two 16-bit words. The error correction algorithm allows any single bit error in the entire 39-bit configuration to be detected and corrected. Two simultaneous errors in the same 39-bit word are detected but not corrected and will be treated as a fatal error. A fatal error of this type causes a trap procedure identical to a parity trap. Single errors are transparent to the Unibus.

1.2 PHYSICAL DESCRIPTION

One control module (M7983) and from one to four array modules (M7984) mounted in a dedicated 9-slot backplane (DD11-K) make up the MF11S-K MOS memory system (Figure 1-1). Figure 1-2 is a simplified block diagram of the MF11S-K system.

All backplane slots not used by the memory are available as small peripheral controller slots.

1.2.1 The Control Module (M7893)

The control module (Figure 1-3) is a hex multilayer board that contains the Unibus interface, timing control, error correction logic, the Control and Status register (CSR), MOS RAM control circuits, and refresh circuitry.

1.2.2 The Array Module (M7984)

The storage array module is also a hex multilayer board (Figure 1-4). It contains 156 MOS RAM ICs (16 pin dip, 4096 bits) and their associated drive circuitry. Although the array module is organized internally in a 16K $\times$ 39 bit configuration, in order to maximize the efficiency of the error correction logic, the MF11S-K memory responds to the processor like a standard 32K $\times$ 16 bit memory.

1.2.3 MF11S-K Memory Size

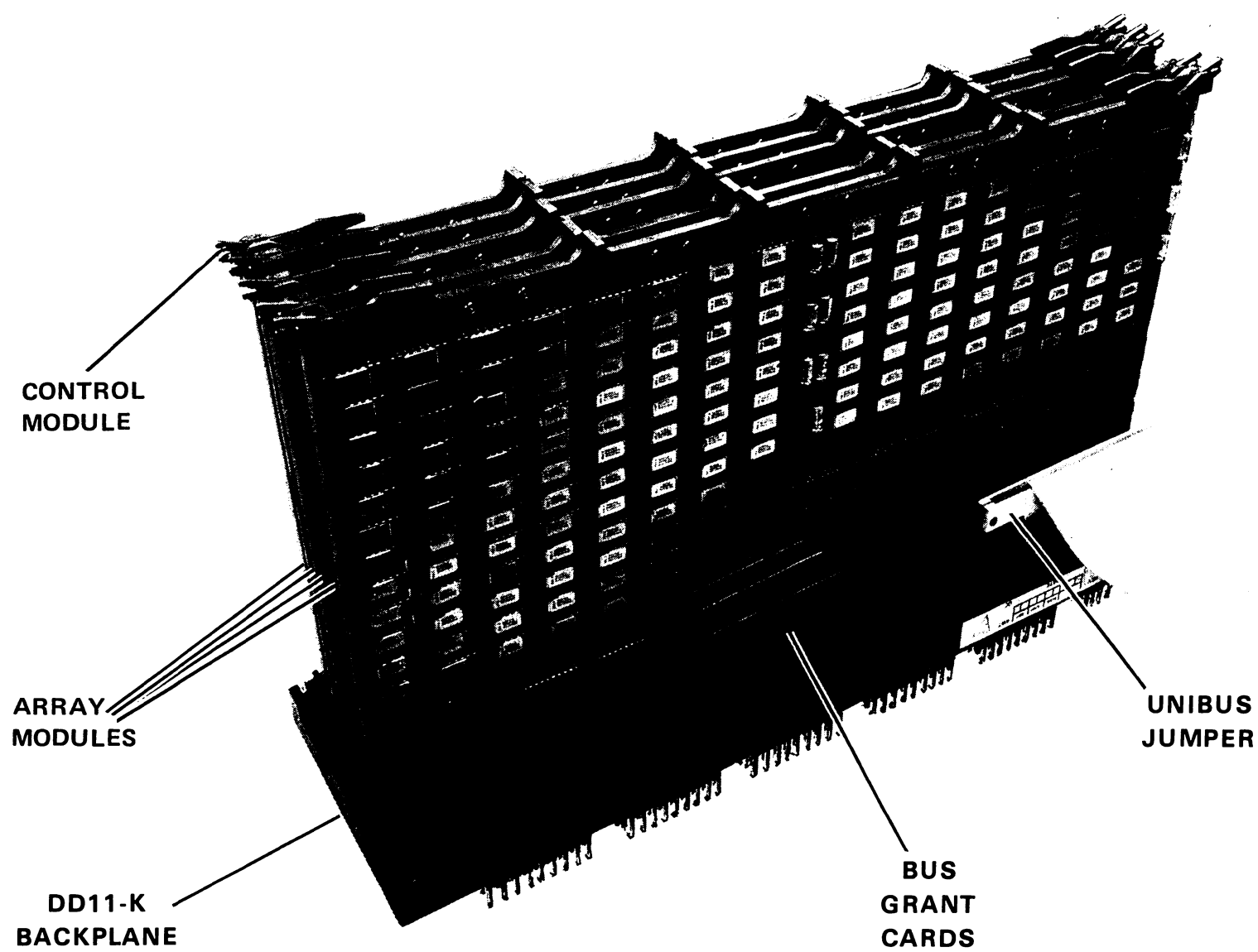
The memory can be increased in capacity from a minimum size of 32K $\times$ 16 bits (one control module and one array module) in 32K increments. The maximum MF11S-K MOS memory system capacity, 128K $\times$ 16 bits, can be obtained by using four 32K 16-bit array modules.

1.2.4 Internal Memory Bus

The MF11S-K memory utilizes an internal bus for communication between the control module and the array modules. Each module, therefore, includes drivers and receivers for the internal bus.

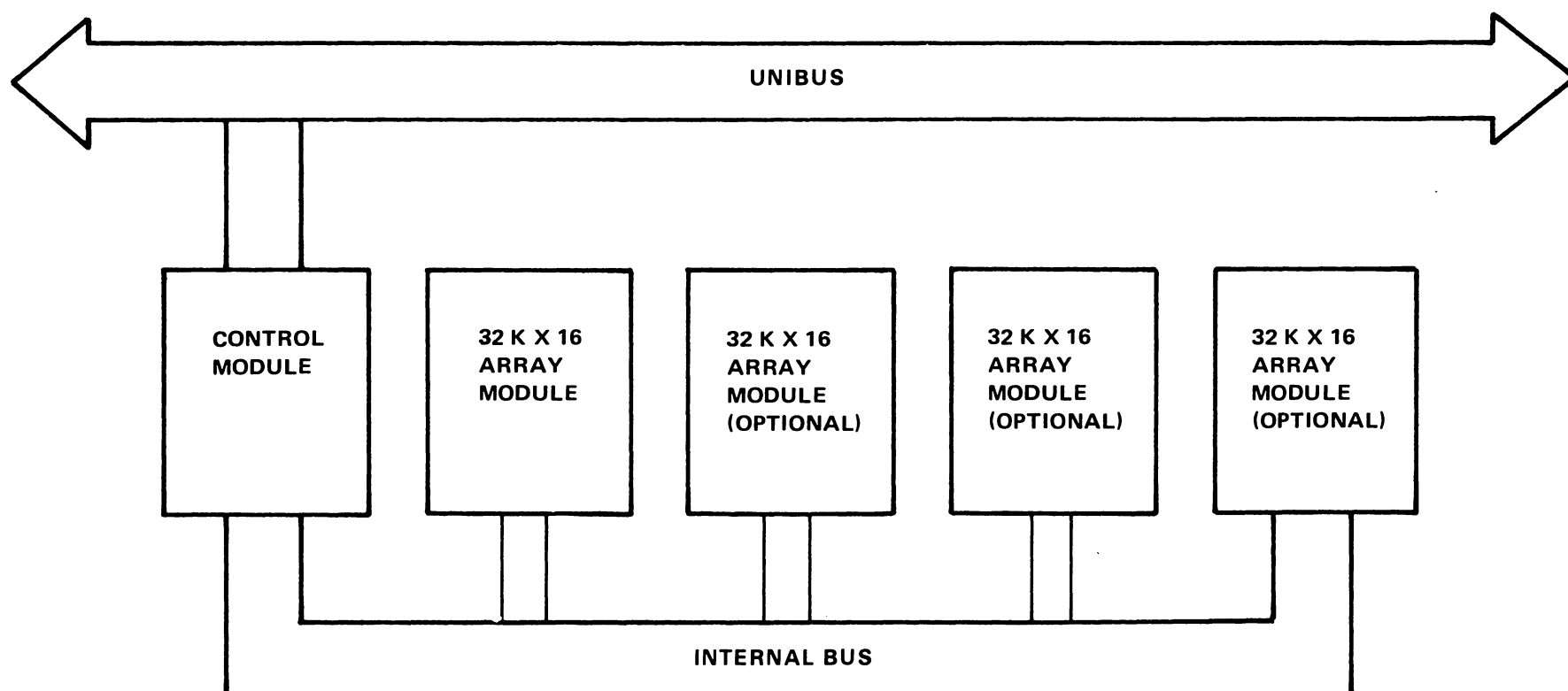
1.3 MAINTENANCE AND RELIABILITY

The error correction capability significantly increases the reliability of the MF11S-K over conventional memory systems. This is accomplished by allowing correctable faults to accumulate in the system. A service call is justified only if noncorrectable faults have been encountered. A noncorrectable fault is defined as any fault that prevents data from being stored and retrieved without apparent errors.



8539-2

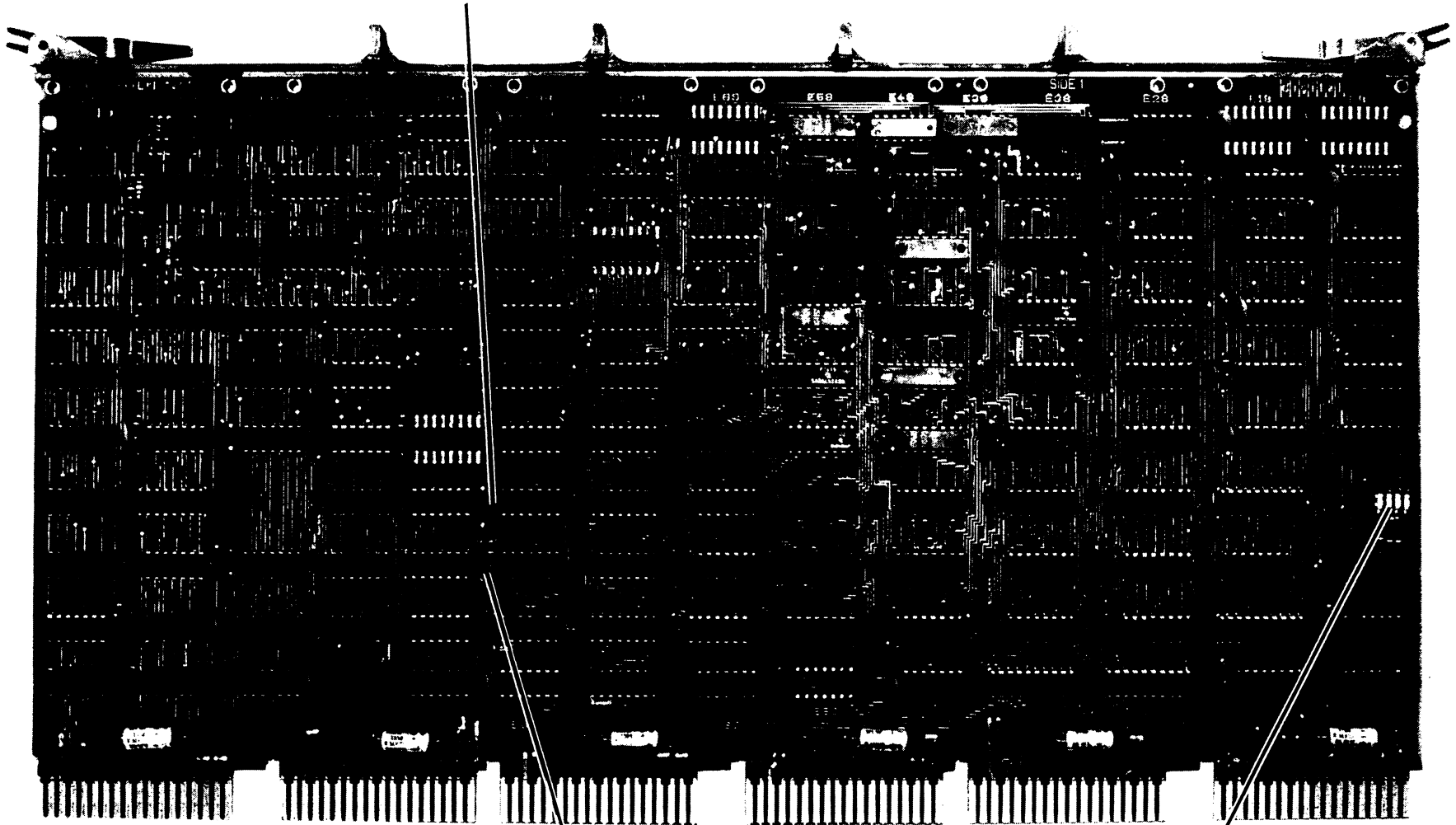
Figure 1-1 Backplane with Controller and Array Modules



11-5413

Figure 1-2 Simplified MF11S-K System Block Diagram

W2
NOT NORMALLY
USED.
WHEN INSERTED
SELECTS CSR
ADDRESS
772134



W1
NORMALLY IN
SELECTS CSR
ADDRESS
772136

ADDRESS
SWITCH
SETTING

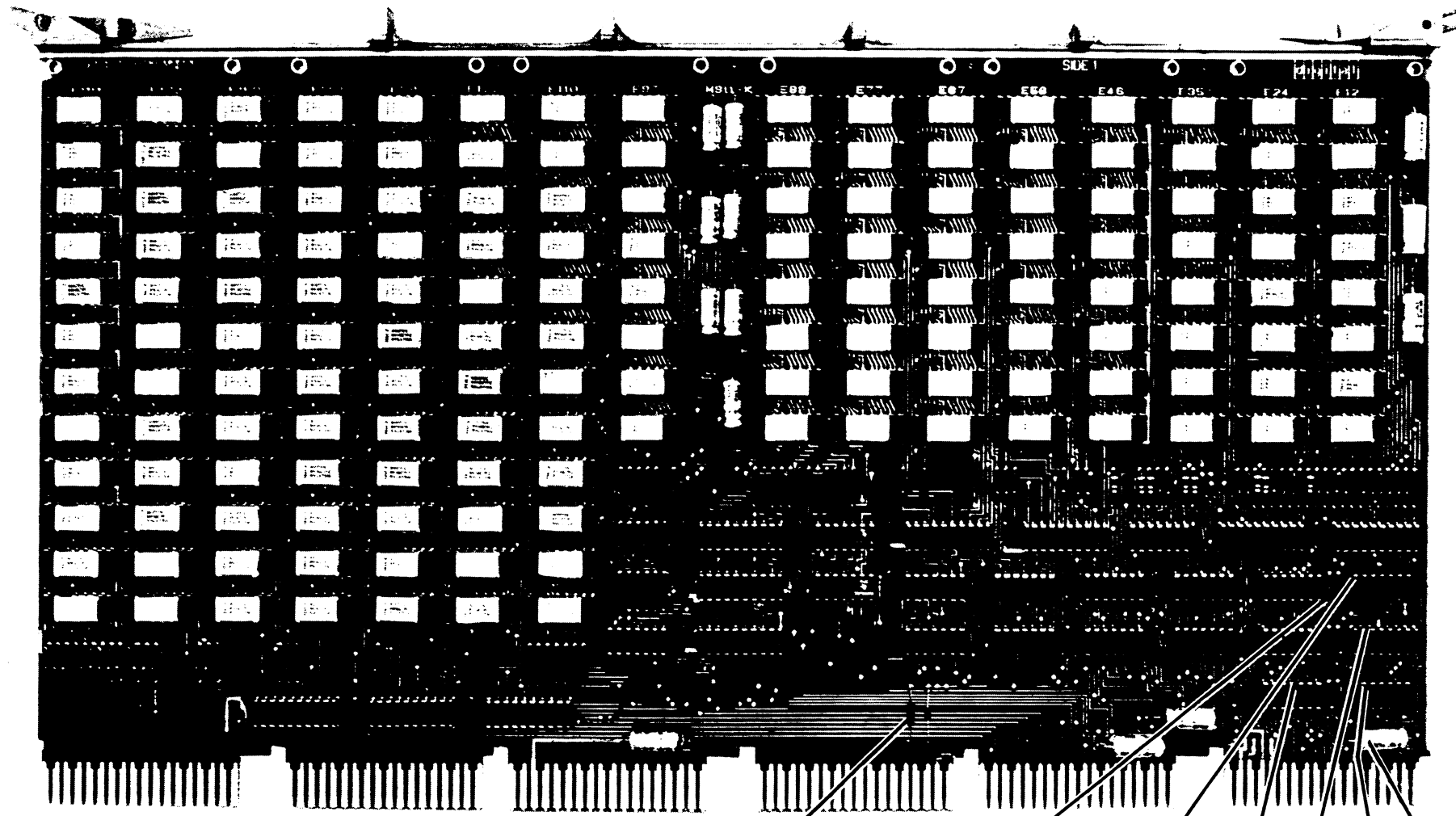
A₁₇ A₁₆ A₁₅ A₁₄

SETS
STARTING
ADDRESS
OF MEMORY

8539-7

Figure 1-3 MF11S-K Control Module

MS11KA USES JUMPERS W1, W2, W3, W4, X1
 MS11KB USES JUMPERS W1, W2, W3, W4, W6, X1



TO HARDWARE SWAP A FAULTY
 8K WORD SECTION TO THE TOP
 OF MEMORY, USE W5 AS IN THE FOLLOWING EXAMPLE.
 MOS DEVICES DRIVEN BY RAS SEL A FAULTY.
 REMOVE W1, W4, INSERT W5, CONNECT
 E1-12 TO E2-4.

X1
 ALWAYS
 USED

W6
 USED ON
 MS11KB
 ONLY

W5
 NOT
 NORMALLY
 USED

W4 W3 W2 W1

8539-9

NOTE

The MS11-KA can be replaced by the MS11-KE.
 The latter option has faster access time MOS
 RAMs. The system access time is not reduced, how-
 ever.

Figure 1-4 MF11S-KA Array Module

1.4 BATTERY SUPPORT MODE

A battery backup option can be utilized with the MF11S-K memory. Since MOS memories lose data whenever power is removed, a backup battery is necessary if the customer wishes to ensure data integrity in the case of a power failure. The power buses on the control and array modules are partitioned so that the voltage supplied by the battery, when the power is down, powers only the logic needed to refresh the memory. Table 1-1 lists the power requirements for the backup battery.

Table 1-1 Backup Battery Power Requirements

System Capacity	Battery Backup Power Required Typ	Max
32K × 16	7.2 W	11.1 W
64K × 16	12 W	18 W
96K × 16	16.7 W	24.4 W
128K × 16	21.6 W	30.6 W

1.5 SPECIFICATIONS

1.5.1 Unibus Interface

The MF11S-K memory interfaces directly with the Unibus. The Unibus loading listed in Table 1-2 should be expected.

Table 1-2 Unibus Loading

Signal	Load
Data Lines	1 Driver, 1 Receiver
All Other Signals	1 Receiver or 1 Driver

1.5.2 Power Supply Requirements

The current drawn from the +12 V supply varies directly with the frequency of operation. The figures given in Tables 1-3 and 1-4 will be for standby (includes refresh) and a cycle time of 800 ns.

Table 1-3 Power Supply Requirements

M7983 Controller					
+5 V			+5 VBB		
Typ	Max		Typ	Max	
4.0 A (20 W)	5.0 A (25 W)		0.6 A (3 W)	0.9 A (4.5 W)	

MS11-KA (32K × 16-Bit Array Module)					
+5 V			+5 VBB		
Typ	Max		Typ	Max	
0.3 A (1.5 W)	0.5 A (2.5 W)		0.45 A (2.25 W)	0.6 A (3.0 W)	
-12 V			+12 V		
		Standby		Active	
Typ	Max	Typ	Max	Typ	Max
25 mA (0.3 W)	50 mA (0.6 W)	0.16 A (1.9 W)	0.25 A (3 W)	0.6 A (7.2 W)	1.0 A (12 W)

Table 1-4 System Power

	+5 V		+5 VBB		-12 V		+12 V				Power					
	Typ	Max	Typ	Max	Typ	Max	Standby		Active		Standby		Active		Battery Backup Mode	
							Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max
32K × 16	4.3 A (21.5 W)	5.5 A (27.5 W)	1.0 A (5 W)	1.5 A (7.5 W)	25 mA (0.3 W)	50 mA (0.6 W)	0.16 A (1.9 W)	0.25 A (3 W)	0.6 A (7.2 W)	1.0 A (12 W)	28.7 W	38.6 W	34 W	47.6 W	(7.2 W)	(11.1 W)
64K × 16	4.6 A (23 W)	6.0 A (30 W)	1.5 A (7.5 W)	2.1 A (10.5 W)	50 mA (0.6 W)	100 mA (1.2 W)	0.32 A (3.8 W)	0.5 A (6 W)	0.76 A (9.1 W)	1.25 A (15 W)	35 W	48 W	40.2 W	56.7 W	(12 W)	(18 W)
96K × 16	4.9 A (24.5 W)	6.5 A (32.5 W)	2.0 A (10 W)	2.7 A (13.5 W)	75 mA (0.9 W)	150 mA (1.8 W)	0.48 A (5.8 W)	0.76 A (9.1 W)	0.92 A (11 W)	1.5 A (18 W)	41.2 W	56.9 W	46.4 W	65.8 W	(16.7 W)	(24.4 W)
128K × 16	5.2 A (26 W)	7.0 A (35 W)	2.5 A (12.5 W)	3.3 A (16.5 W)	100 mA (1.2 W)	175 mA (2.1 W)	0.64 A (7.7 W)	1.0 A (12 W)	1.1 A (13.2 W)	1.75 A (21 W)	47.4 W	65.6 W	52.9 W	74.6 W	(21.4 W)	(30.6 W)

1.5.3 Access and Cycle Times

Cycle time is defined as the time from the assertion of MSYN at the output of the Unibus memory receivers (memory not busy) to the time the memory is ready to accept the next MSYN (i.e., when the Memory Busy flip-flop is cleared). Access time is defined as the time from the assertion of MSYN at the output of the Unibus receiver to the time that SSYN is asserted on the bus.

1.5.3.1 Memory Storage – Access and cycle times are listed in Table 1-5.

Table 1-5 Memory Storage – Access and Cycle Times

		Typ	Max
DATI or DATIP	Read Access, No error	520 ns	550 ns
	Read Access, Single error Corrected or Double error	630 ns	675 ns
	Read cycle time	750 ns	800 ns
DATO or DATOB	Internal RMW SSYN response	85 ns	120 ns
	Internal RMW cycle time	1130 ns	1200 ns
DATO or DATOB Following DATIP	Write SSYN Response	85 ns	120 ns
	Write cycle time	750 ns	800 ns

1.5.3.2 Refresh Cycle – Refresh cycle time: Typ 865 ns; Max 910 ns.

Refresh cycle time is defined as the time from the assertion of REF CYC (1) H to the resetting of the MBSY flip-flop.

Note that all the access and cycle times listed in Table 1-5 are modified during a refresh cycle conflict. In the worst case, for example, memory access is increased by the refresh cycle time. Read access time would be 550 ns + 910 ns = 1460 ns.

DATOB time would be 1200 ns + 910 ns = 2110 ns.

Table 1-6 lists the refresh repetition rates.

Table 1-6 Refresh Repetition Rate

Typical Rate	25.0 μ s
Fastest Rate	22.5 μ s
Slowest Rate	29 μ s

1.5.3.3 ECC INIT Routine – ECC INIT Time: Typ 65 ms; max 70 ms.

During an ECC INIT routine, all zeros data is written at an 8 μ s repetition rate, and BUS AC LO is asserted.

1.5.3.4 Control and Status Register (CSR) – CSR access times are listed in Table 1-7.

Table 1-7 CSR Access

		Typ	Max
DATI or DATIP Cycle	CSR Read Access	60 ns	80 ns
DATO or DATOB Cycle	CSR Write SSYN Response	60 ns	80 ns

The CSR can be accessed regardless of whether a memory cycle is in progress or not; e.g., the memory can be in a refresh cycle while the CSR is being accessed. The cycle time depends on the capability of the bus master.

1.6 BACKPLANE UTILIZATION

The nine slot backplane has been designed specifically for the MF11S-K memory. The backplane specifications should be examined carefully before configuration and power application.

The M7984 array module will fit in slots 4 through 7 of the DD11-K backplane. The M7983 controller, however, must be placed in slot 8. The array slots are dedicated according to memory size. The first 32K of memory must go in slot 7, the second in slot 6, the third in slot 5, and the fourth in slot 4. Slot 1 must be used for the Unibus cable-in jumper. Slot 9 must contain either a Unibus cable-out jumper or a terminator. Slots that are unused should contain bus grant cards.

For information concerning other uses of the DD11-K backplane, see Chapter 8.

CHAPTER 2 **FUNCTIONAL DESCRIPTION OF THE ERROR CORRECTION LOGIC**

2.1 GENERAL

When the MF11S-K memory system sends data to the bus master, it checks the integrity of the data and corrects single bit errors before placing the data on the Unibus. The error correction logic makes use of a modified hamming code to carry out these checking and correcting functions.

2.2 MODIFIED HAMMING CODE AND CHECK BITS

The modified hamming code uses combinations of parity checks on various bit patterns within a memory data word. The error correction logic implements the modified hamming code by forming a parity check bit for each of these various bit patterns. Figure 2-1 shows the matrix formed by the modified hamming code used in the MF11S-K memory.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	MF11S-K WORD
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	2 PDP-11 WORDS
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	4 PDP-11 BYTES
C1	X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		X		
C2	X	X			X	X			X	X			X	X			X	X			X	X			X	X			X	X			
C4	X	X	X	X					X	X	X	X					X	X	X	X					X	X	X	X					
C8	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
C16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X									X	X	X	X	X	X	X	X	
C32	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X									
CT	X			X		X	X			X	X		X			X		X		X			X		X	X		X				X	
	BYTE 3								BYTE 2								BYTE 1								BYTE 0								

11-5414

Figure 2-1 Modified Hamming Code Matrix

Each check bit, except Ct, is the result of odd parity generated on the data bits designated by X. For example, C1 is a function of data bits 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29, and 31. Ct is the result of even parity. It ensures the detection of double errors. The fact that it uses even parity ensures that an all zeros Internal Memory Bus error is detected as a double (fatal) error.

Each data bit is described by a unique combination of 3, 5, or 7 check bits. Data bit 0, for example, is described by C32, C16, and C8. No other data bit is described uniquely by these three check bits. If, in a given 32-bit data word, bit 0 only were logic 1, C16 and C8 would be logic 0s, while Ct, along with C32, C4, C2, and C1, would be logic 1s.

2.3 MEMORY WORD SIZE

Six check bits would be required to describe a 16-bit PDP-11 word. Only one additional check bit, however, is required to describe 32 data bits. The 32-bit data configuration within the MF11S-K memory thus increases the efficiency of check bit use by more than 40 percent.

2.4 USE OF THE 39-BIT MEMORY WORD

The internal operation of the MF11S-K memory differs from that of conventional memories so that it can carry out the error correction algorithm. Since check bits are generated to correspond to two data words (32 bits) whenever one word or byte is accessed in a read or write cycle, the remaining bytes in the double-word location and the seven corresponding check bits must all be examined by the error correction logic. The following paragraphs trace, in general terms, the function of the memory as it performs read and write cycles.

2.5 READ OPERATION (DATI AND DATIP)

2.5.1 Accessing the Data

When a bus master initiates a read cycle, two bytes are addressed via the Unibus (Figure 2-2). The memory control logic brings the 39-bit memory word (32 data bits plus 7 stored check bits) from the array into the Memory Data register (MDR). The 39-bit memory word includes the requested data. A parity circuit then generates seven new check bits on the 32 data bits just read from the array.

2.5.2 Generation of Syndrome Bits

At this point, two separate sets of check bits exist. Both sets describe the 32 data bits in the MDR. In order to determine the validity of the data, the error correction logic compares the stored check bits with the newly generated check bits. The Exclusive OR function of the two sets of check bits forms a set of seven syndrome bits as shown in Figure 2-3. A discrepancy between a stored check bit and a corresponding newly generated check bit will set a syndrome bit to a logic 1 (Table 2-1). After the syndrome bits are formed, they are latched. Three examples will be used to clarify the explanation.

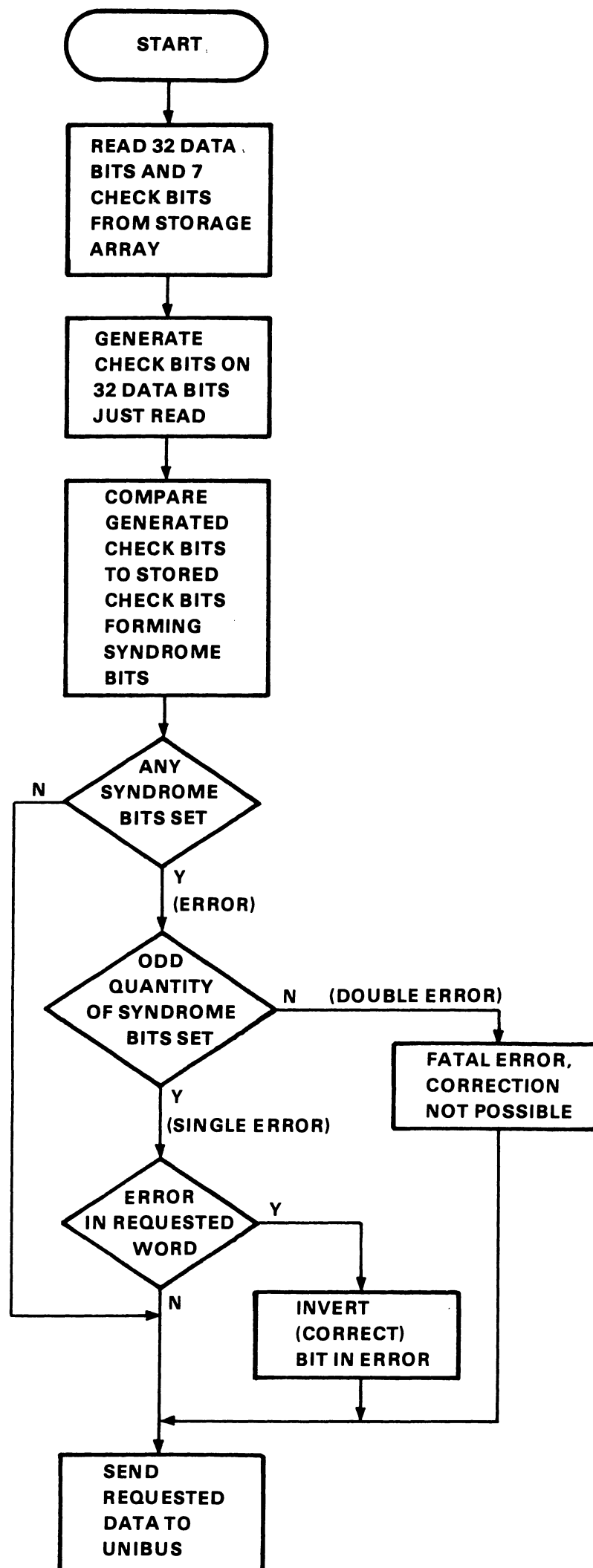
2.5.3 Example A, Data Bit 0 Set

At this point, it will be useful to follow up the example given at the end of Paragraph 2.2, in which data bit 0, only, was set. If the data that was stored in the memory location addressed is identical to the data retrieved from that location, the two sets of check bits will agree. No syndrome bits will be set to logic 1s, and when the syndrome bits are latched, all latches will be in the reset state.

However, if bit 0 is a 1 in the data stored and yet a 0 in the data that is retrieved from the array, the syndrome bits will register the discrepancy. The stored check bits, C8 and C16, will be 0s. Stored check bits Ct, C32, C4, C2, and C1 will be 1s. In the set of newly generated check bits, however, only Ct will be 0. The other newly generated check bits will be 1s (Table 2-2).

The Exclusive OR function of the syndrome generation circuit causes ST, S16, and S8 to be set and then latched as logic 1s.

An examination of the decoder chart in Figure 2-4 will show that syndrome pattern 1011000 will be decoded to point to data bit 0, within byte 0.



11-5420

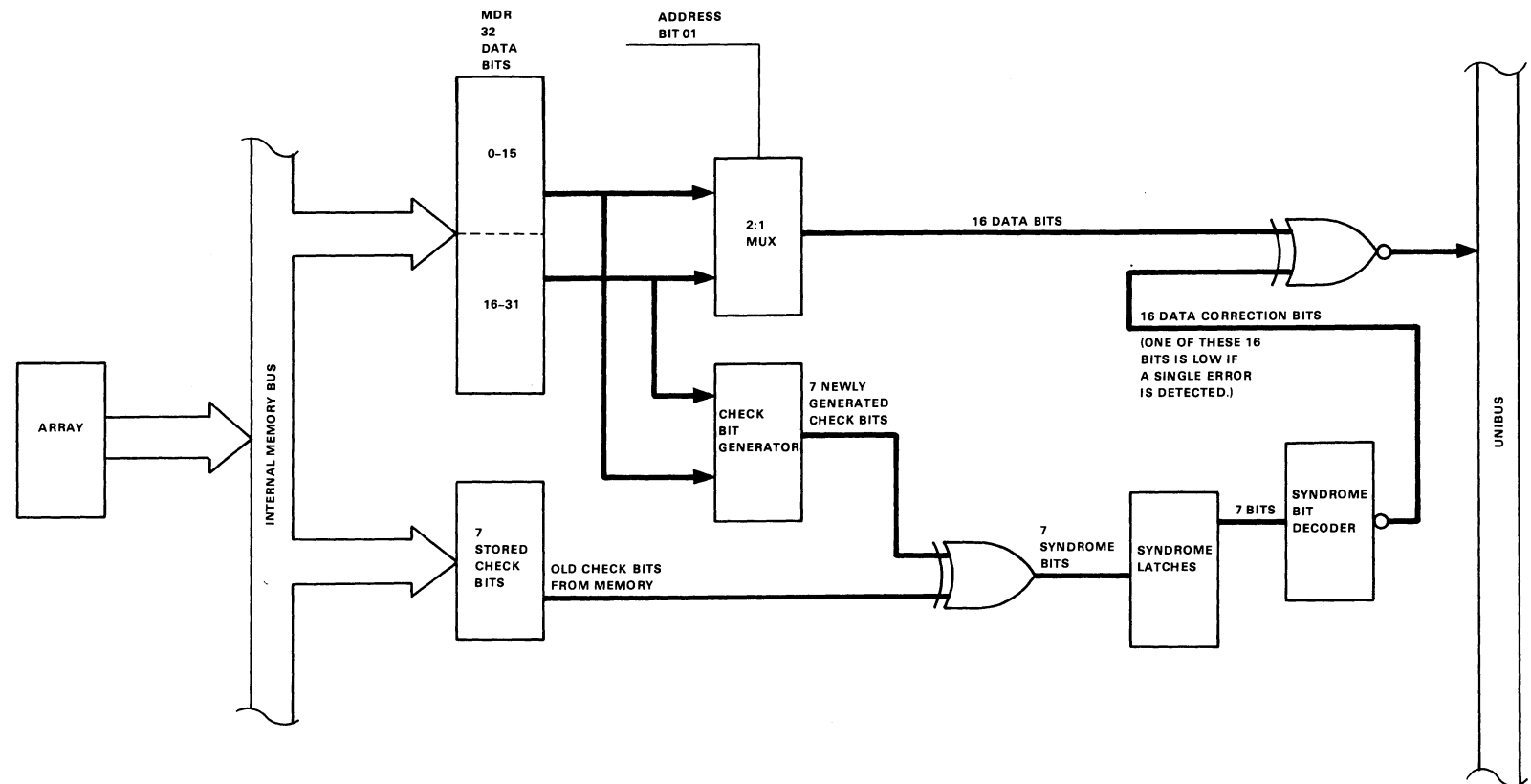
Figure 2-2 Read Cycle Flowchart

Table 2-1 Syndrome Bit Generation

Stored Check Bit	Generated Check Bit	Syndrome Bit
0	0	0
0	1	1
1	0	1
1	1	0

Table 2-2 Error Correction, Example A

	Data Bit 0	Check Bits						
		CT	C32	C16	C8	C4	C2	C1
Stored	1	1	1	0	0	1	1	1
Retrieved	0	0	1	1	1	1	1	1
	0	ST	S32	S16	S8	S4	S2	S1
Syndrome Bits	–	1	0	1	1	0	0	0



11-5419

Figure 2-3 ECC Logic Used on a Read Cycle Block Diagram

S ₃₂	S ₁₆	S ₈	
0	0	0	
0	0	1	
0	1	0	
0	1	1	BYTE 0
1	0	0	
1	0	1	BYTE 1
1	1	0	BYTE 2
1	1	1	BYTE 3

S ₄	S ₂	S ₁	
0	0	0	BIT 0
0	0	1	BIT 1
0	1	0	BIT 2
0	1	1	BIT 3
1	0	0	BIT 4
1	0	1	BIT 5
1	1	0	BIT 6
1	1	1	BIT 7

11-5417

Figure 2-4 Syndrome Bit Decoding

2.5.4 The Error Correction Process

After the syndrome bits are latched, the control logic examines them to see if any are 1s. If no syndrome bits are 1s, indicating that no error has been detected, the requested data is sent to the Unibus.

However, if, as in Example A, a logic 0 in data bit 0 is retrieved, syndrome bits ST, S16, and S8 will be set to logic 1s. The error correction logic checks to find whether the quantity of syndrome bits set to 1 is odd or even. If an odd number of syndrome bits is set, the error is treated as a single error condition.

In Example A, above, ST, S16 and S8 are logic 1s, indicating a single error condition. Latched syndrome bits S32, S16, and S8, are decoded to determine whether or not the error is in the data word requested by the bus master. If the data requested is in the lower word of the 32-bit data unit, which, in this case, contains the error, the decoder circuit further decodes latched syndrome bits S4, S2, and S1 to identify the bit in error. This bit (bit 0 in Example A, above) is then inverted before the requested data is sent to the Unibus. If the error is not in the requested data, it remains uncorrected, and the data that is requested by the bus master is sent to the Unibus. It is important to note that data is never corrected except when it is to be gated to the Unibus on a read.

2.5.5 Example B, Handling a Double Error

The MF11S-K memory does not attempt to correct double errors. It will detect a double error and, on a read, notify the processor that a fatal error has been encountered, regardless of the location of the errors within the 39-bit memory word. It is important to notice that the use of the check bit, Ct, will ensure that an even number of syndrome bits is set on a double error.

Suppose, for example, that data bits 1 and 3 are the only logic 0s in a word stored in the location accessed. When the word is retrieved, bits 1 and 3 are both logic 1s. The stored check bits are all 1s except C2, which is 0. Of the newly generated check bits, Ct will be 0, the rest will all be 1s. (Table 2-3).

The syndrome bit pattern generated, 1000010, shows an even number of bits to be 1s. The error correction logic decodes this pattern to indicate a double error. The requested data word is then sent, uncorrected, to the Unibus. The memory notifies the processor that a fatal error has occurred, causing the initiation of a trap routine, if enabled by software. The data that is sent may, or may not, contain errors depending on the location of the two errors.

Table 2-3 Double Error, Example B

	Data Bit 1	Check Bits							
		Bit 3	CT	C32	C16	C8	C4	C2	C1
Stored	0	0	1	1	1	1	1	0	1
Retrieved	1	1	0	1	1	1	1	1	1
			ST	S32	S16	S8	S4	S2	S1
Syndrome Bits			1	0	0	0	0	1	0

2.5.6 Handling a Check Bit Error, Example C

The MF11S-K memory will detect a check bit error, as well as a data bit error, on a read operation. However, it must make a distinction between the two types of errors. Data bit errors require correction; check bits errors do not.

For example, if zeros are stored in a 32-bit data location, the stored check bits C32, C16, C8, C4, C2, and C1 will all be 1s. Ct will be a 0. Suppose that when the location is accessed on a read, the data bits are retrieved without error, but that check bit C2 is a logic 0 instead of a logic 1. Syndrome bit S2 will be set to 1 and latched, as shown in Table 2-4.

Table 2-4 Check Bit Error, Example C

	Data	CT	C32	C16	C8	C4	C2	C1
Stored	0	0	1	1	1	1	1	1
Retrieved	0	0	1	1	1	1	0	1
		ST	S32	S16	S8	S4	S2	S1
Syndrome Bits		0	0	0	0	0	1	0

A look at Figure 2-4 will show that the syndrome bit pattern generated, 0000010, will cause no byte, and, therefore, no bit to be selected for error correction. The requested data will be gated to the Unibus unaltered.

2.6 WRITE OPERATION IN GENERAL (DATO AND DATOB)

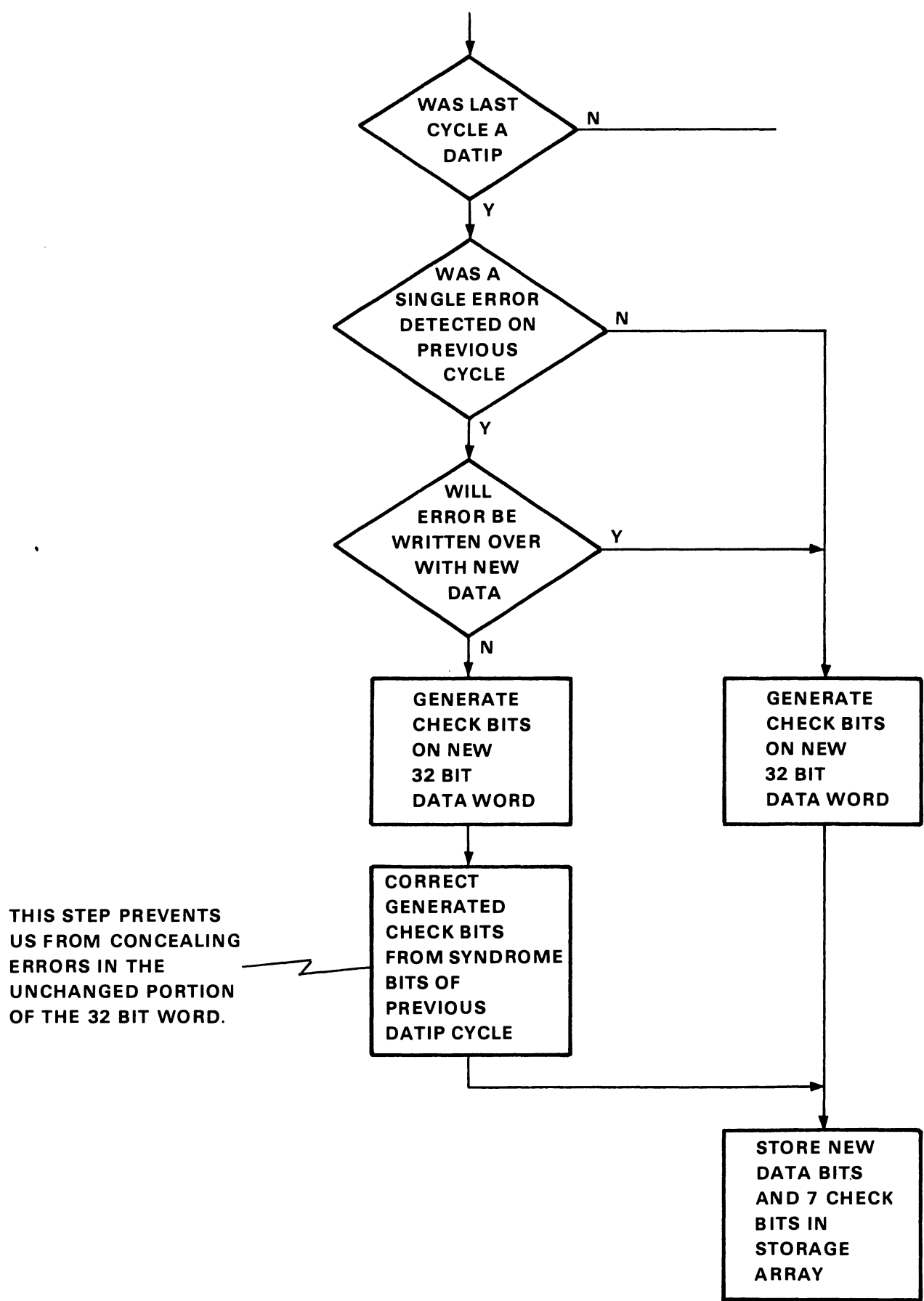
On a write operation, data is sent from the bus master in one or two byte units. However, since MF11S-K memory words are organized as four data bytes plus seven check bits, the write operation never changes more than half the data in a memory location.

The MF11S-K memory begins a normal write operation with an internal read cycle. This is necessary because new check bits must be generated on a full double word at the memory locations addressed, even though only one or two bytes are to be altered. The entire write operation thus involves an internal read-modify-write routine within the MF11S-K memory, although only a write cycle has been called for on the Unibus control lines.

However, when the memory performs a write cycle following a DATIP cycle, it accesses the same location on both cycles. This means that a read-modify-write routine is not necessary, since the data in the bytes of the double word that are not to be written over is already stored in the MDR. This data does not need to be accessed a second time to enable the generation of new check bits.

2.7 WRITE OPERATION FOLLOWING A DATIP

At the beginning of a write operation, the MF11S-K memory must determine whether or not the previous cycle was a DATIP, as shown in Figure 2-5.



11-5418

Figure 2-5 Write Cycle Flowchart

In fact, if the previous cycle was a DATIP, the error correction logic checks the syndrome bits latched during the DATIP cycle to see if a single error was detected on that cycle. Note that if a double error has been detected on the previous DATIP cycle, the memory will perform a read-modify-write cycle instead of a straight write cycle.

The memory control logic moves the data to be written from the Unibus to the appropriate byte location(s) in the MDR. The 32 data bits in the MDR, at this point, contain new data (one or two bytes) and old data from the unused bytes in the memory word (two or three bytes).

2.7.1 No Single Error Detected

If no single error from the previous cycle has been detected, the 32 data bits in the MDR should all be correct. New check bits are then generated on the 32-bit double word; and the new data (one or two bytes only), together with the seven newly generated check bits, is then stored in the array.

2.7.2 Single Error Detected

If one or more syndrome bits remain latched as logic 1 from the previous DATIP cycle, a single error has been detected. If the error is in a data bit, three, five, or seven syndrome bits will be set. If one syndrome bit is set, it indicates the presence of a check bit error.

The error correction logic then decodes the syndrome bit pattern to determine which byte in the 32-bit data word contains the bit in error. If the error is in a location to be written over, or if the bit in error is one of the old check bits, it is ignored. Check bits are generated on the new double word; the new data, together with the seven new check bits, is stored in the array.

However, a problem arises if the error is located in a byte that is to remain unaltered. Simple generation of new check bits would mean that the check bits would describe bad data as if it were correct. Check bits must be generated on the 32 data bits containing the bad data, as before. But these check bits must then be corrected so that they still point to the bit in error. Figure 2-6 shows how the Exclusive ORing of the latched syndrome bits (from the previous cycle) with the newly generated check bits accomplishes the correction process.

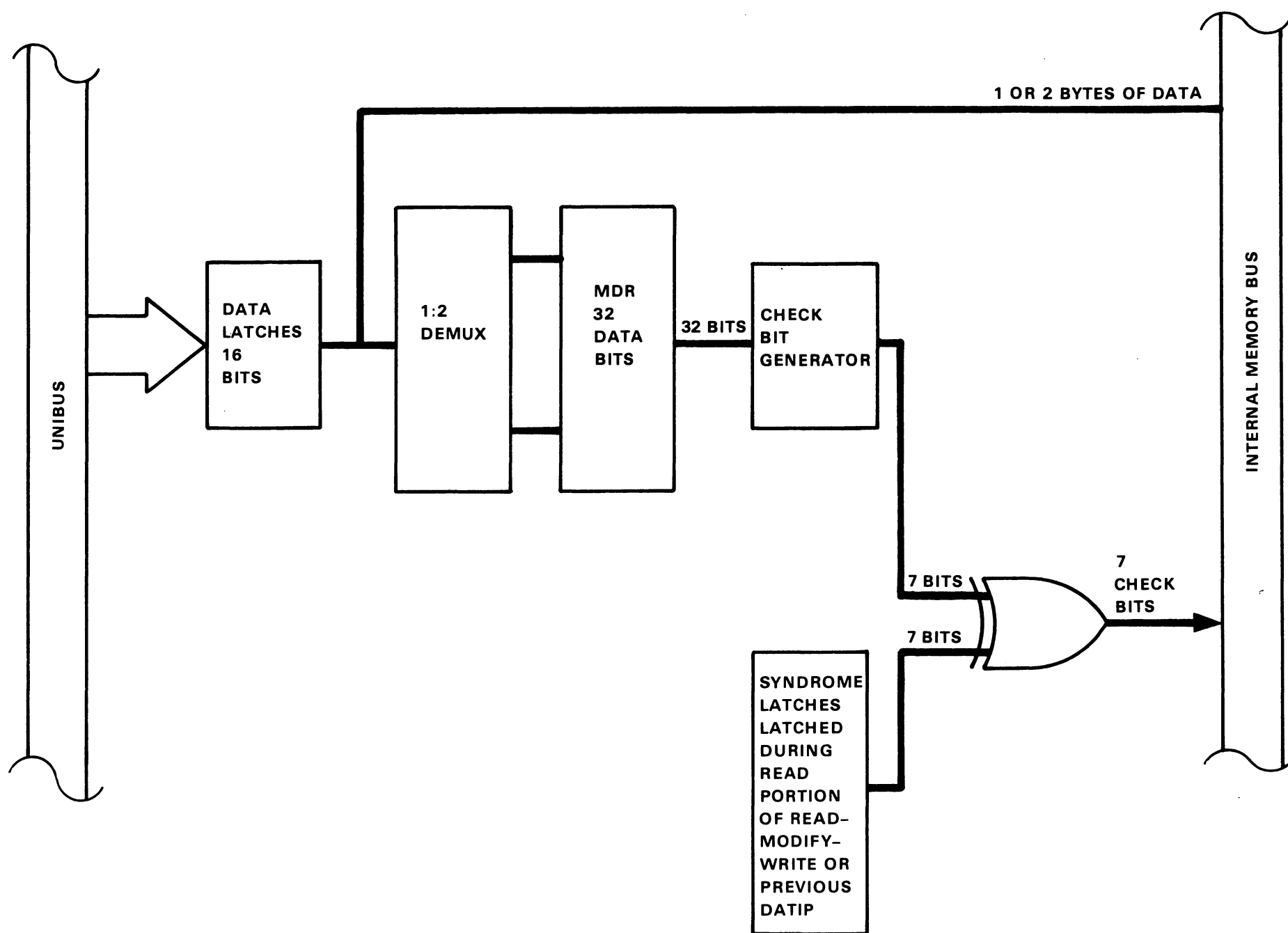
The new data and corrected check bits are then stored in the array. It is important to note that this step prevents the memory from concealing errors in the unchanged portion of the 32-bit word. Notice, also, that data containing errors is not corrected on a write cycle. Check bits that describe the memory location are merely updated so that the error information they contain remains valid.

2.8 WRITE OPERATION NOT FOLLOWING A DATIP

When the MF11S-K memory executes a read-modify-write routine in response to a write command that does not follow a DATIP, it begins by reading 32 data bits and 7 check bits from the 39-bit memory location containing the bytes to be written over (see the flowchart in Figure 2-7). Then, as on a read cycle, the error correction logic generates check bits on the data from the array and compares them with the stored check bits to form syndrome bits. These syndrome bits are latched, because it is important to keep track of any errors that are indicated.

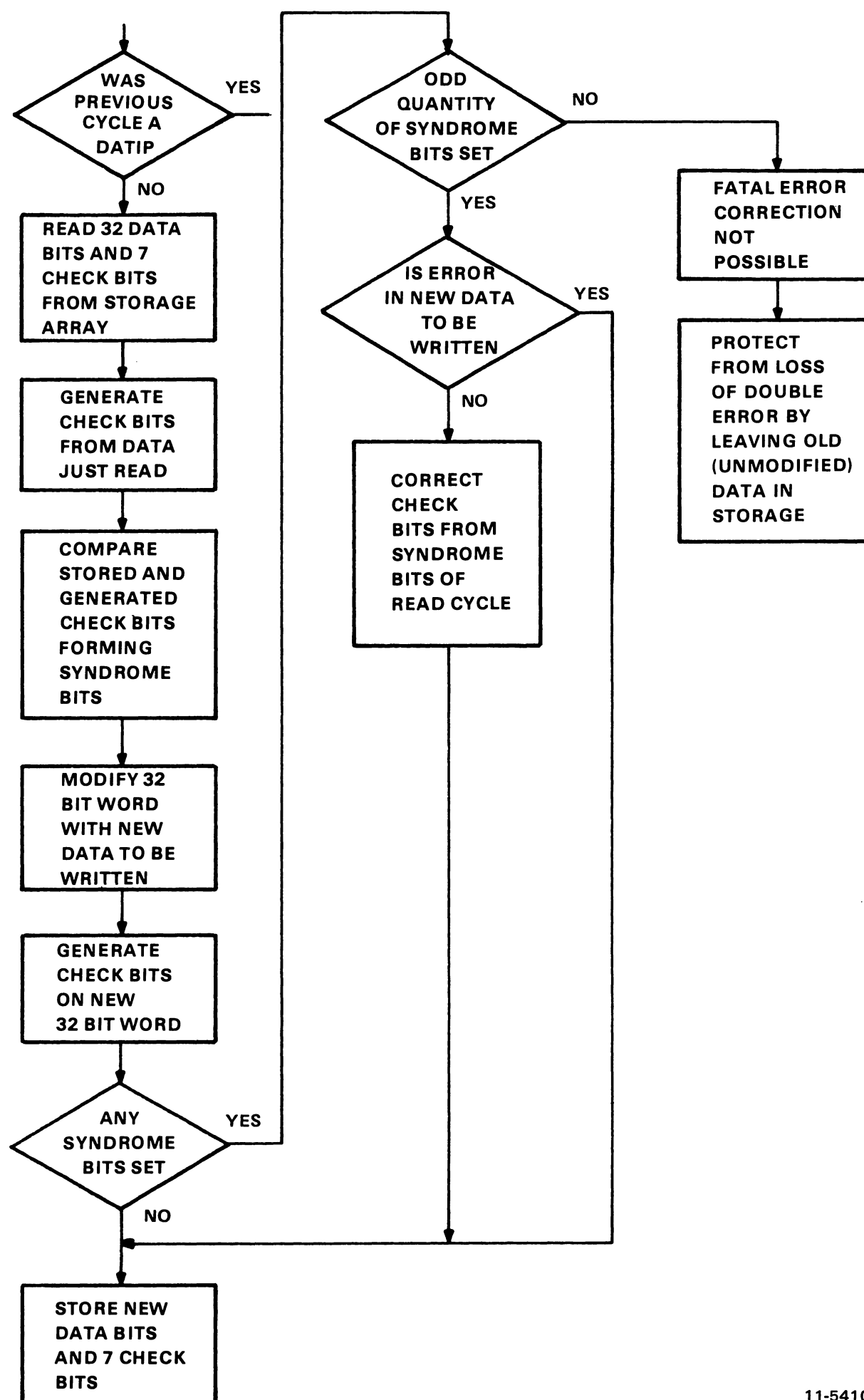
Next, the contents of the MDR are modified as the byte or bytes to be written are latched in the appropriate byte locations. At this point, check bits are generated again. This second set of newly generated check bits corresponds to the modified memory word that is to be stored in the array.

The error correction logic then checks latched syndrome bits, which reflect the old double word. If no syndrome bits are latched as 1s, the data in the MDR should be correct. The byte, or bytes, to be written, together with the second set of generated check bits, is stored in the array.



11-5415

Figure 2-6 ECC Logic Used on a Write Cycle



11-5410

Figure 2-7 Read-Modify-Write Cycle Flowchart

2.8.1 Error Detection on a Write

However, if any latched syndrome bits are 1s, an error in the old word is indicated. The error correction logic then checks to find whether the number of latched syndrome bits set to 1 is odd or even.

2.8.2 Double Error Condition

If the number of latched syndrome bits set to 1 is even, it indicates that a double error existed in the old word read from memory. To preserve the double error condition, all modification of data and check bits normal to a write operation is inhibited. The old data word and old check bits are returned unaltered to the array.

Detection of a double error on a write cycle will not cause the initiation of a trap routine or notify the processor of a fatal error. The processor is warned of double errors only on DATI and DATIP cycles.

It is important to save double error conditions for troubleshooting purposes, however. If one or both of the errors were soft, and measures were not taken to preserve the errors, the double error condition might be impossible to locate subsequently.

2.8.3 Single Error Condition

If an odd number of latched syndrome bits are found to be logic 1s on a write cycle following a DATIP, they indicate that a single error existed in the old double word. The latched syndrome bit pattern is then decoded so that the error correction logic can determine whether or not the single error is located in a byte to be written over. If the error is in a byte to be written, it is ignored, and the data to be written, together with the second set of newly generated check bits, is stored in the array.

However, if the error is found to be in a byte that is not to be written over, the check bits must be altered. The second set of newly generated check bits describes the data in the MDR as if it were correct. Exclusive ORing of the syndrome bits with the second set of newly generated check bits produces corrected check bits, as shown in Figure 2-6. At this point, the data to be written and the corrected check bits are stored in the array. Note that the bit in error remains uncorrected. Only the check bits that describe the double word have been altered, ensuring that the check bits can be used to form syndrome bits, and thus locate the error, on the next read cycle to that location.

CHAPTER 3

MOS CHIP DESCRIPTION

3.1 PHYSICAL DESCRIPTION

The MOS memory device used with the MF11S-K is a 4096-bit, dynamic, RAM circuit. The circuit is packaged in a standard 16-pin DIP that provides high system bit density and is compatible with available automatic testing and insertion equipment. Figure 3-1 is an outline drawing of the chip, showing pin connections. Table 3-1 lists the chip supply voltages.

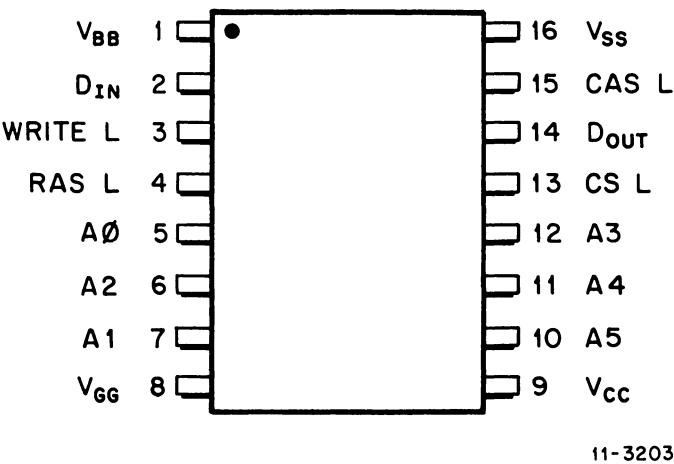
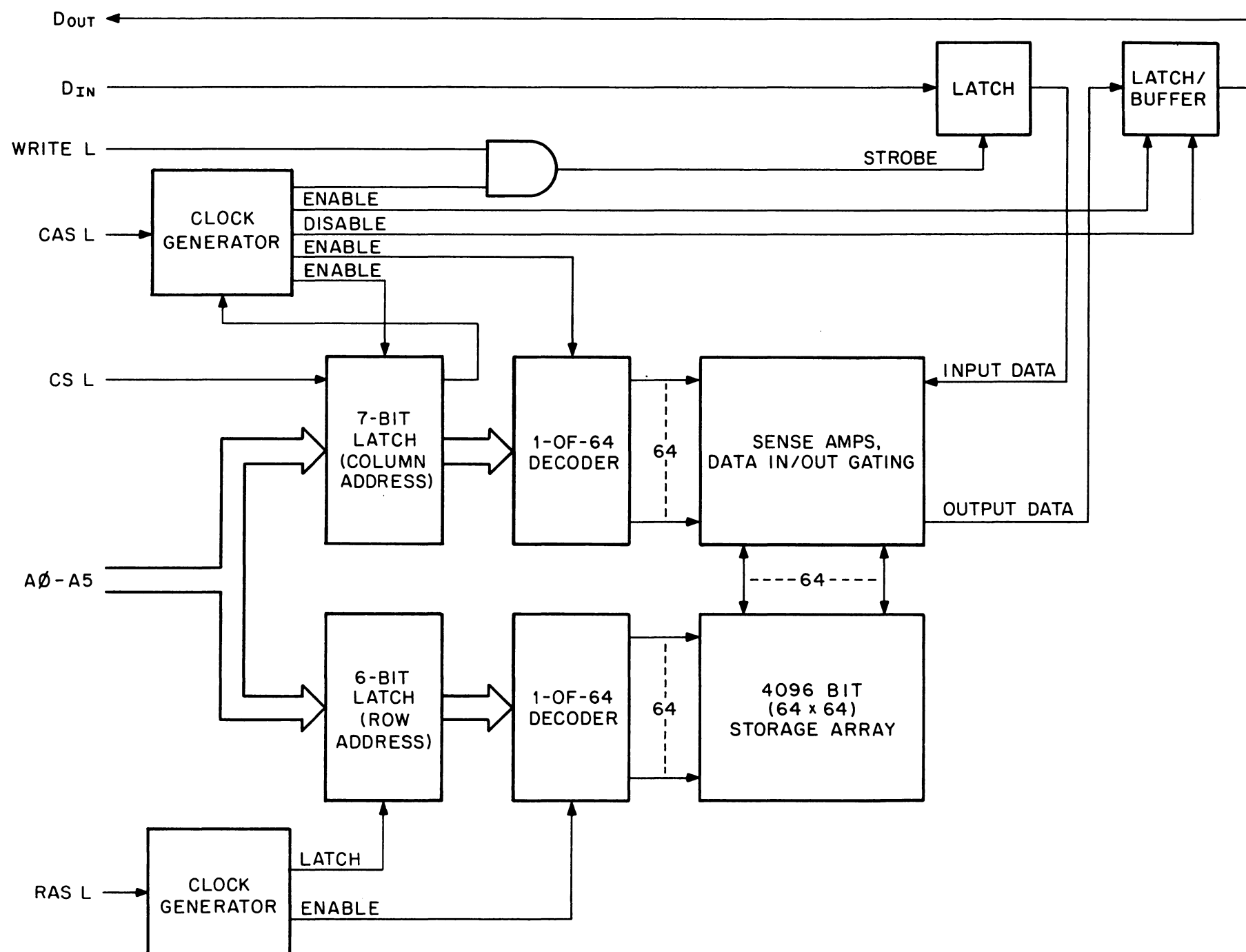


Figure 3-1 MOS RAM Chip Pin Connections

Table 3-1 Chip Supply Voltages	
Voltage	Operation
VDD	+12 Vdc
VCC	+5 Vdc
VSS	Ground
VBB	-5 V

3.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the chip is shown in Figure 3-2. The 4096 storage locations are arranged in a 64-row by 64-column array. Thus, a cell location can be specified by a 6-bit row address and a 6-bit column address. Because address information is latched into on-chip registers, the chip can be driven by six address lines. The MF11S-K logic multiplexes 12 address bits, six at a time, onto the A0-A5 lines. The RAS L (Row Address Strobe) signal causes row address information to be latched into a 6-bit register, while the CAS L (Column Address Strobe) signal causes column address information, as well as the CS L (Chip Select) signal, to be latched into a 7-bit register. Enable signals applied to 1-of-64 decoders result in the selection of one of the 4096 cell locations for a data transfer.



11-3204

Figure 3-2 (4096 x 1) Bit MOS Chip, Block Diagram

3.2.1 The Cell Storage Element

A simplified representation of the chip is shown in Figure 3-3 (the switches are merely symbolic of more detailed chip operation). The basic cell storage element is a capacitor; a charge voltage of 0–6 V represents logic 0, while a voltage of 6–12 V represents logic 1. Because the charge on the capacitor dissipates with time, it is continually refreshed so that the data it represents remains valid. Any read or write cycle results in a refresh of the data in the addressed locations. During such a cycle, the row address is latched first, and then the 1-of-64 decoder closes all the switches in the selected row. The charge voltage on each capacitor in the row is applied to a sense amplifier (SA), which refreshes the data by restoring the charge voltage to its original level. For example, the maximum charge voltage on a cell capacitor is 12 V, representing logic 1. When the cell is addressed, a portion of the full charge may have leaked off so that the voltage has decreased, for example, to 8 V. The SA forces the voltage back to its full-charge value of 12 V. Similarly, any voltage between 0 and 6 V is restored to a logic 0 level of 0 V.

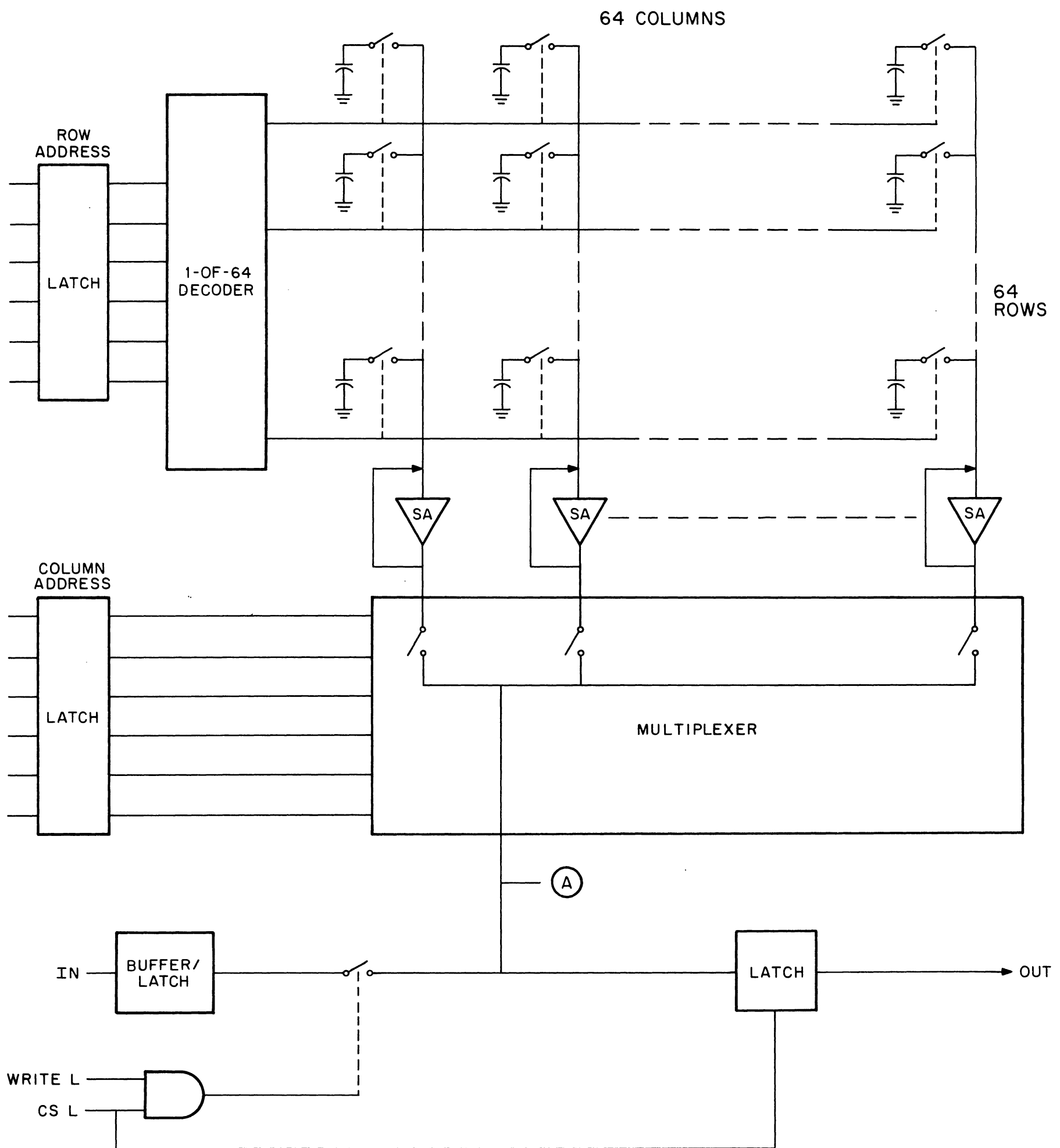
3.2.2 Read, Write, and Refresh

After the data in the selected row is accessed and refreshed, the column address is latched; the multiplexer selects one of the 64 columns; and the amplified charge voltage on a single capacitor is applied to point A in Figure 3-3. If the cycle is a read, the data is strobed into the tristate output latch and remains valid until the next time CAS L goes low. If the cycle is a write, the input buffer/latch drives point A, overriding the SA output and charging the selected cell capacitor. Since a cell may be addressed infrequently, if at all during normal read/write operations, a specially timed refresh cycle is carried out at regular intervals. In the MF11S-K memory, such a cycle occurs approximately every 25 μ s. A different row address is supplied by the MF11S-K logic during each refresh cycle so that the data in all 64 row addresses is refreshed about every 2 ms. The refresh operation is similar to a read or write cycle, i.e., the row address is latched; the data in each cell of the row is refreshed; the column address is latched (the column address supplied by the MF11S-K logic is the same during all 64 different refresh cycles); and the cell data is read out to point A. However, during a refresh cycle, the CS L signal is disabled so that neither the input circuit nor the output circuit is enabled. The output latch will go to its high impedance state, ensuring that power consumption is minimal.

3.2.3 Timing

Figure 3-4 shows the timing for a read cycle. Figures 3-5 and 3-6 show the timing for write and read-modify-write cycles, respectively. The RAS L signal starts the timing cycle internally. To reduce the overall system power, RAS L is decoded in the MF11S-K logic and supplied only to the selected bank of chips. The CAS L signal is supplied to all chips, but chips that do not receive an RAS L signal will go to their high-impedance output states.

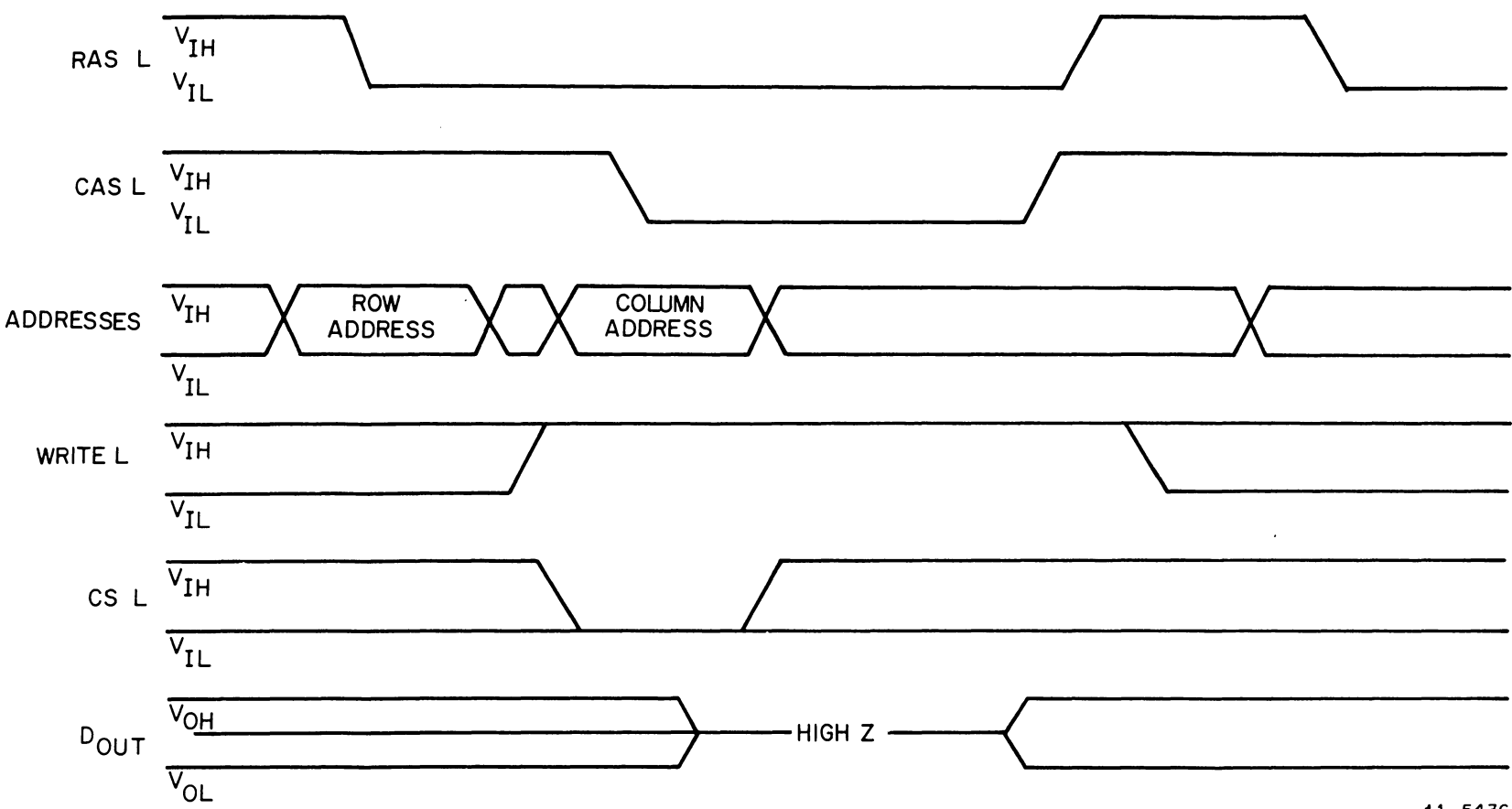
If data is to be read from the addressed location, the WRITE L signal must be high and the CS L signal must be asserted. The data is strobed into the output latch/buffer at access time (after RAS L is asserted) and remains valid until CAS L goes negative during a subsequent timing cycle. A write cycle requires that the WRITE L signal go low before access time; the WRITE L command is accepted by the chip only if CS L has been asserted. The data on the D IN line is strobed into an input latch by the negative transition of the CAS L signal.



11-3205

Figure 3-3 MOS Chip, Simplified Data Gating

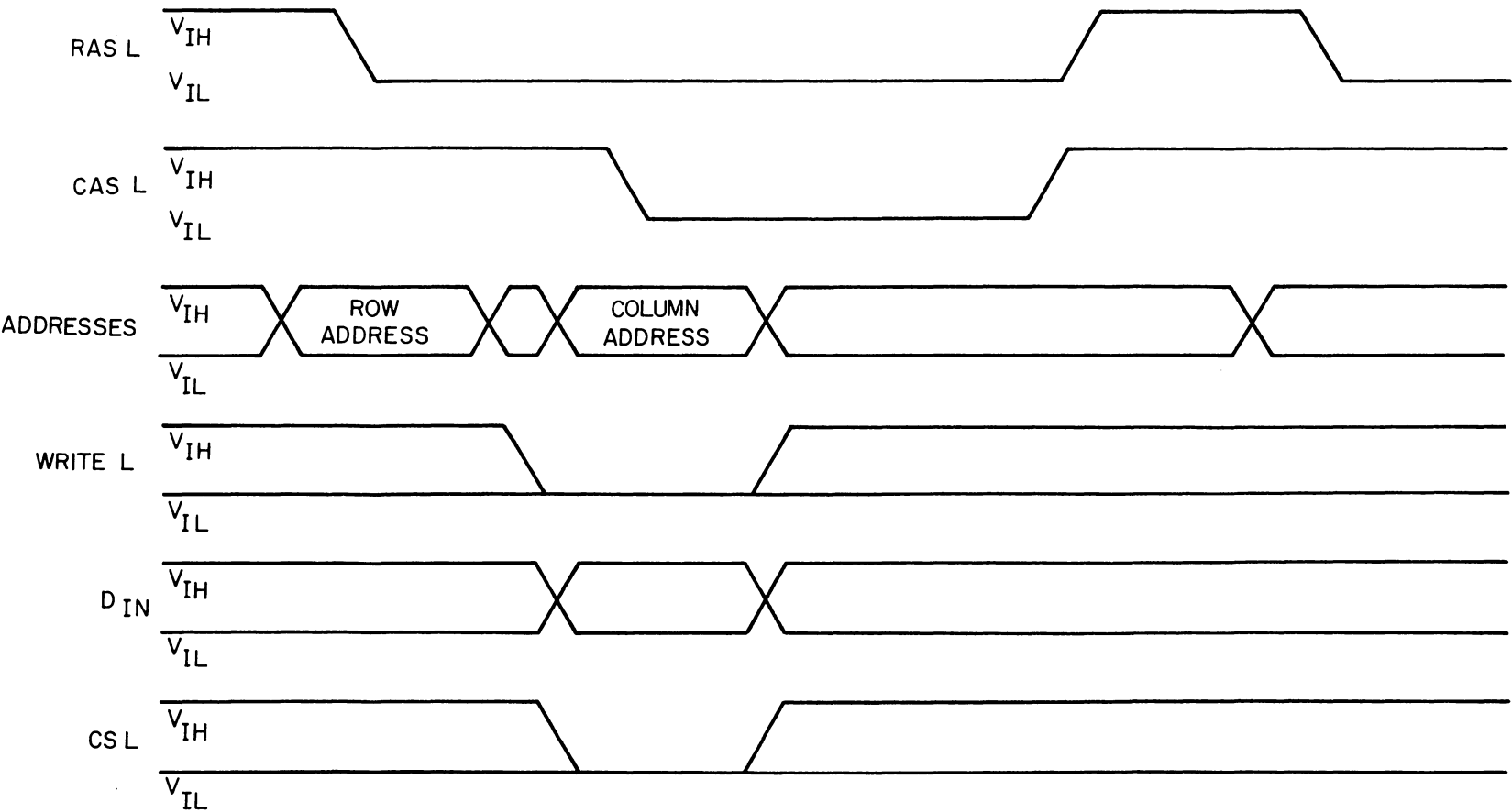
READ CYCLE (minimum timing)



11-5436

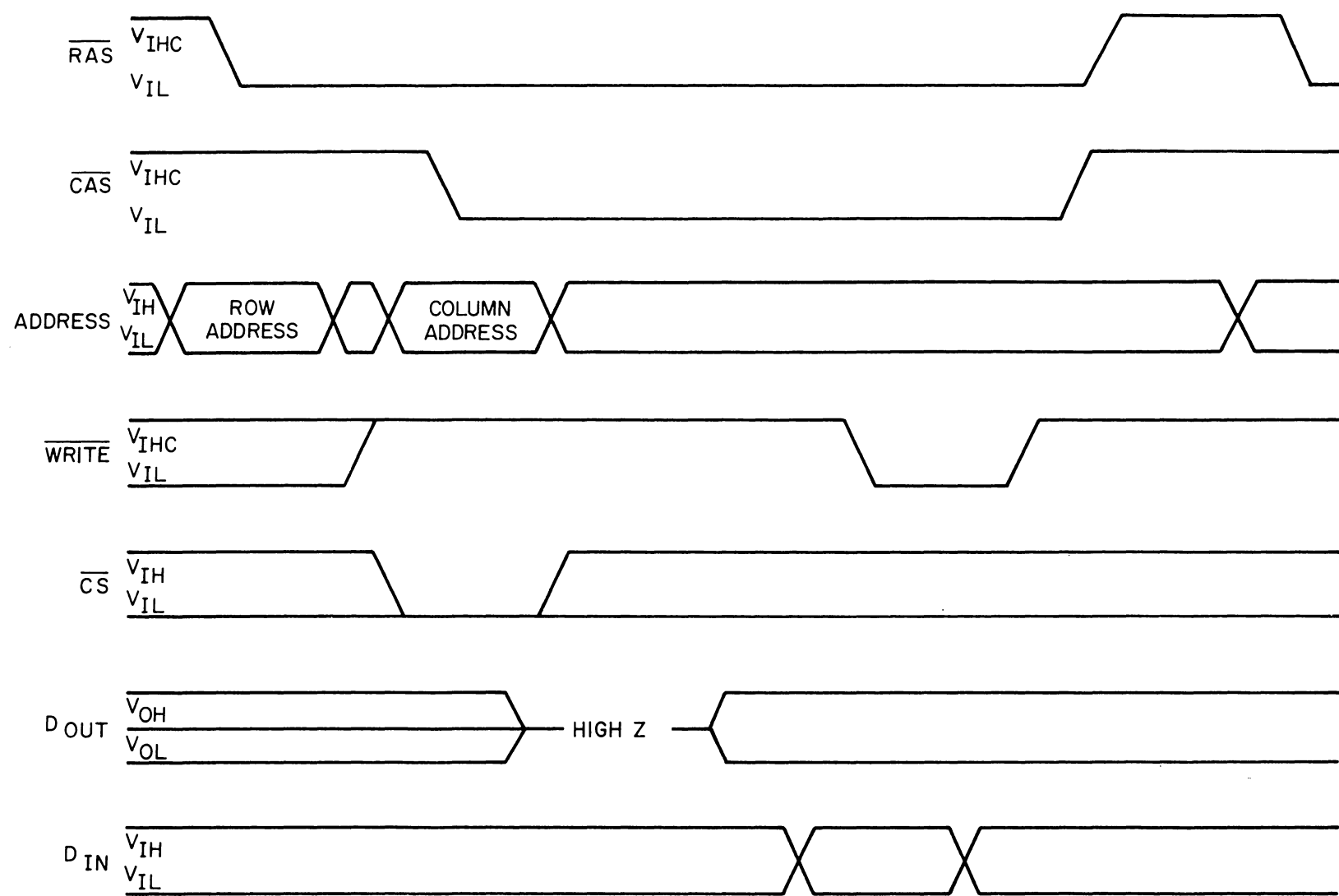
Figure 3-4 Read Cycle Timing

WRITE CYCLE (minimum timing)



11-5437

Figure 3-5 Chip Write Timing



11-5378

Figure 3-6 Read-Modify-Write Timing

CHAPTER 4

MS11-KA STORAGE ARRAY MODULE: DETAILED EXPLANATION

4.1 GENERAL

The storage array is a hex, multilayer module containing 156 16-pin RAM chips and their associated drive circuitry. It communicates with the control module via the internal memory bus on connectors A and B. The MS11-KA can be replaced by the MS11-KE. The two options are indistinguishable when used in the MF11S-K memory. Figure 4-1 shows the array circuit in block diagram form.

4.2 INTERNAL MEMORY BUS

The internal memory bus provides 62 signal lines for communication between the control module and the array on connectors A and B of slots 8, 7, 6, 5, and 4 of the DD11-K backplane.

4.2.1 Data and Check Bit Lines

The 32 data lines (DB00 – DB31 RD L) and seven check bit lines (CB1 – CBT RD L) use negative logic (low is logic 1) (Figure 4-2). These lines move the 39-bit word, or individual bytes, from the control module to the array module and from the array module to the control module, depending on the requirements of the memory cycle being performed. Tristate driver gates feed the data and check bit lines at each end of the internal memory bus.

Receiver gates on the array module pick up data bit and check bit signals from the bus. Four-bit latches are used to receive and store signals from these bus lines on the controller. The data bit and check bit lines are the only lines on the internal memory bus that are bidirectional.

4.2.2 Address Lines

The six address lines (AO–5H) are multiplexed on the control module. They carry the row and column addresses of the data to be accessed, from the control module to the array, at different stages of the addressing process (Figure 4-4).

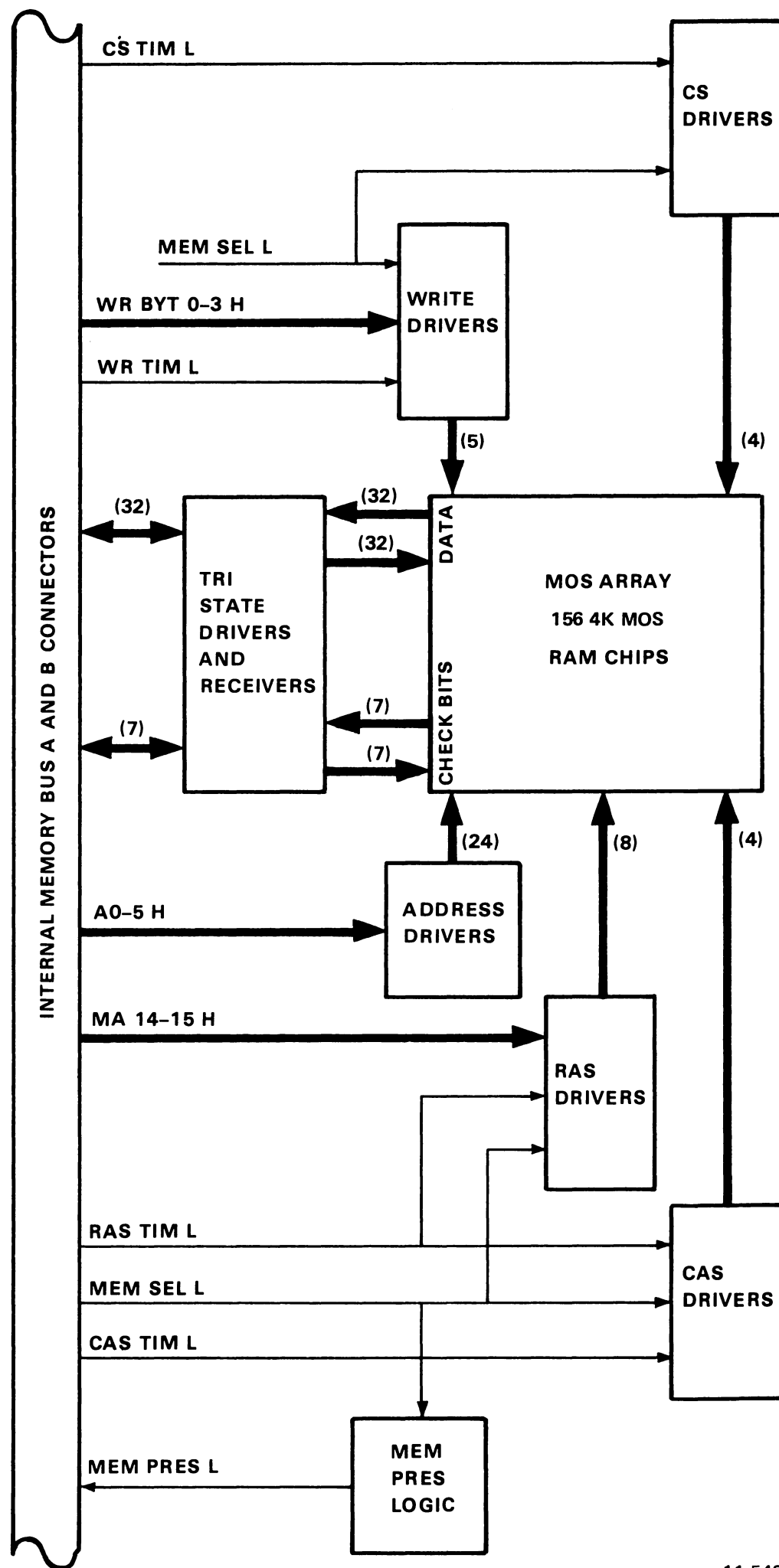
Multiplexer chip outputs on the controller drive the lines, while gates on the array module pick up the signals. Note that these signals, unlike the data signals, have only one source and are high true (high is logic 1).

4.2.3 Write Byte Lines Select and Modified Address

The four write byte select lines (WR BYT 0–3 H) and the two modified address lines (MOD A14 H and MOD A15 H) also carry high true signals.

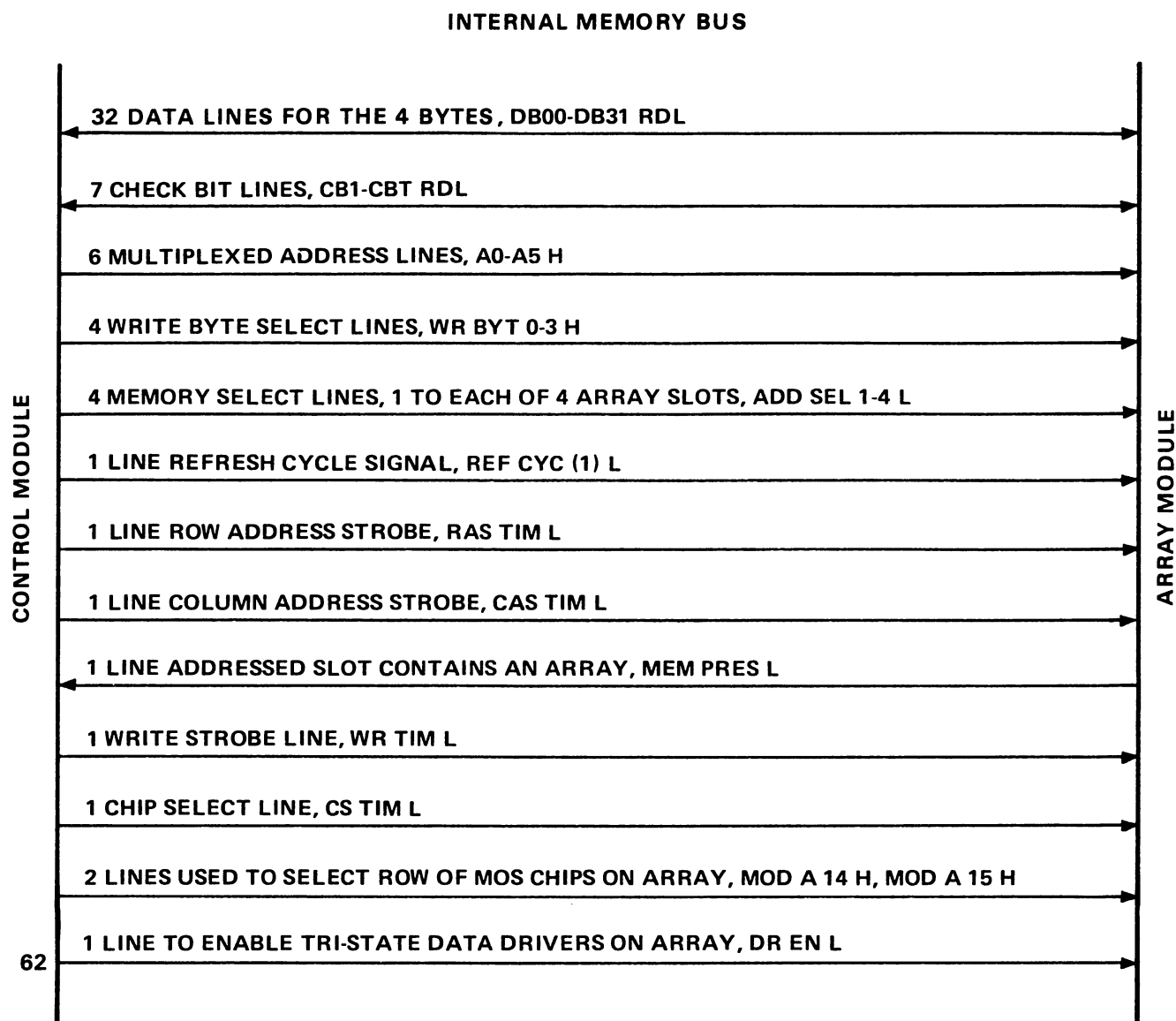
4.2.4 Memory Select Lines

Four memory select lines are driven from the controller. Each of the four lines goes to pin AE 2 on one of the array slots. This means that the array modules are interchangeable (Figure 5-8). Since the array module selection decoder circuit is located on the control module, no selection circuit is necessary on the array module.



11-5409

Figure 4-1 Array Module Block Diagram



11-5416

Figure 4-2 Internal Memory Bus

4.2.5 Refresh and Selection and Memory Present Lines

The INT BUS REF CYC (1) L (low true) signal comes into pin AE 1 on each array module. It is buffered through the E2 decoder chip on the array, and ORed with the INT BUS ADD MEM SEL L to generate the memory select signal and enable the internal memory bus signal INT BUS MEM PRES L. This signal notifies the control module that an array module is present in the slot addressed. Note that on a refresh cycle all slots are addressed.

4.2.6 Other Control Signals

The remaining internal memory bus signals, RAS TIM L, CAS TIM L, WR TIM L, CS TIM L, and DR EN L are all low true control signals. Their functions are explained in detail later in this chapter and in Chapter 5.

4.3 POWER DISTRIBUTION

Four voltages are supplied to the array module from the H7850 regulator and the power supply, namely +12 V, +5 V, +5 V battery backup, and -12 V. A zener diode (D1, shown on the logic prints sheet 1) is used to reduce the -12 V to -5 V for supply to the MOS chips.

4.4 ARRAY MODULE FUNCTIONAL LAYOUT

The MOS chips are arranged so that one of four chips supplies one bit position of a 39-bit word. The first 4K words are located in the bottom row of chips on the array module logic prints, sheets 8 through 17, beginning with E93 for bit 0, E106 for bit 1, etc. Figure 4-3 shows the relation of bytes and memory locations to chip numbers on the array module.

4.5 ADDRESS BIT FUNCTIONS

Of the 18 Unibus address bits, only bits 2–13 are gated to the RAM input pins (Figure 4-4). Lines A0H–A5H of the internal memory bus carry first the row address bits (2–7) and then the column address bits (8–13).

Address bits 14–17 may or may not be altered on the control module, depending on the starting address for the MF11S-K memory. Address bits 14 and 15 are used to form INT BUS MA 14 H and INT BUS MA 15 H. The decoder chip E2 (sheet 3 of the array module print set) generates four RAS select signals from these address bits, selecting one of the four rows of RAM chips. Address bits 16 and 17, as mentioned above, are modified, as necessary, on the controller and decoded to select one of the four array modules.

Address bits 0 and 1 are also decoded on the controller and used to generate one or two of the four INT BUS WR BYT signals on a write cycle. These signals are enabled when ANDed with INT BUS WR TIM L and MEM SEL L (Figure 4-5). Note that when MEM SEL L is high it holds all the drivers in a high impedance state, so that power consumption is kept to a minimum.

4.6 ADDRESS RECEIVER CIRCUITRY

The six internal bus lines used for row and column addresses (INT BUS A0 H through INT BUS A5 H) are ANDed with the Memory Select signal to fan out to six groups of four address drivers. These 24 drivers send the row and column addresses to the RAM chips (Figure 4-6). It should be noted that the resistors at the outputs of the drivers function as terminators, reducing overshoot on the line.

4.7 RAS AND CAS TIMING SIGNAL BUFFERS

INT BUS RAS TIM L is a timing signal generated on the controller. It is ANDed with the Memory Select signal on the array module and enables one of the four RAS SEL lines, A, B, C, or D. These lines, in turn, enable one of the four 4K, 39 chip rows of RAMs at row address time, thus gating the six row address signals to the row address registers on each of the 39 selected chips (Figure 4-7).

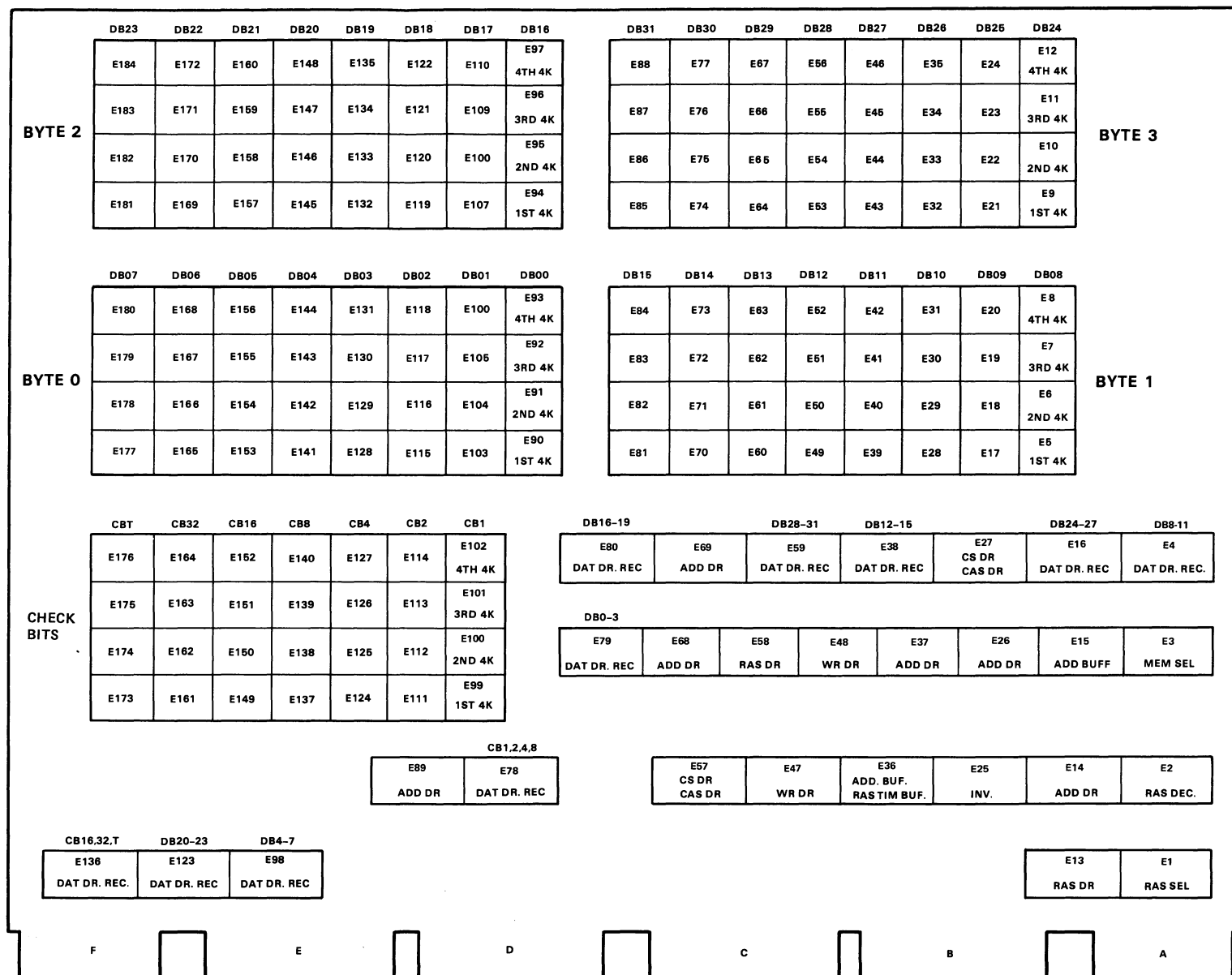
The signal INT BUS CAS TIM L is ANDed with the RAS timing signal at column address time to gate the six internal memory bus address signals to the column address registers on the 39 selected chips (Figure 4-8). Note that all chips receive the CAS signal. CAS resets (from the previous cycle) the output latches of the chips not selected by RAS. The outputs of the unselected chips thus go to a high impedance state. Note also that when RAS TIM L goes high, it disables the CAS signal on the array, thus minimizing skew.

Figure 4-9 shows the ANDing of the Chip Select and Memory Select signals. The signal formed is fanned out as CS L A and CS L B to all 156 RAM chips.

4.8 TRISTATE DATA DRIVERS AND RECEIVERS

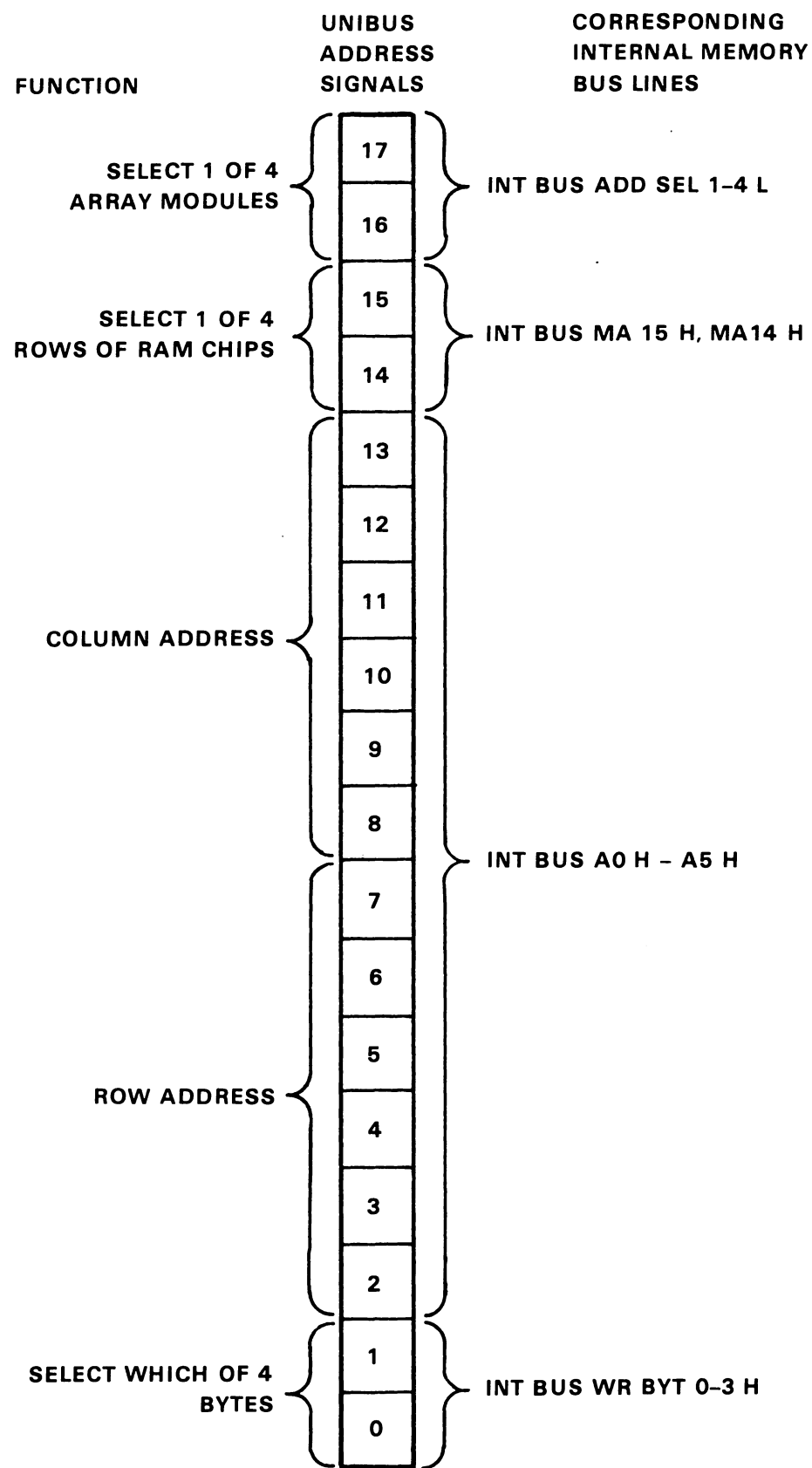
The INT BUS DR EN L signal is generated on the controller on a read or read-modify-write. This signal enables the tristate driver gates, which gate the RAM output signals to the internal memory bus. When the drivers are disabled, they go to a high impedance state, and thus free the bus for drivers on the control module. The tristate receiver gates on the array are always enabled.

The array module circuit uses 39 pairs of drivers and receivers, one for each bit in the 39-bit memory word. Thus, each driver-receiver pair services four RAM chips. Figure 4-10 shows a one bit slice.



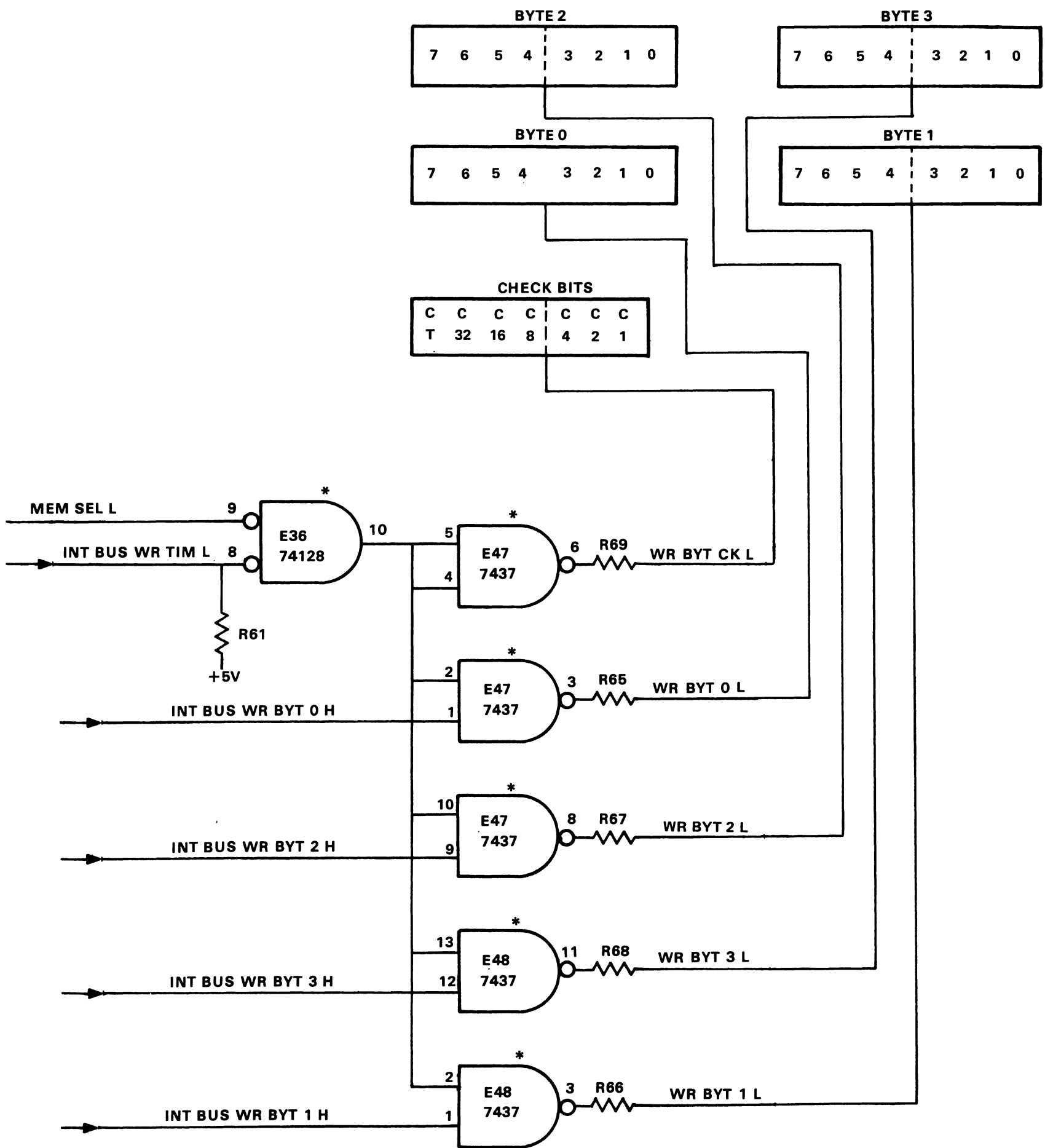
11-5403

Figure 4-3 Functional Layout of Array Module



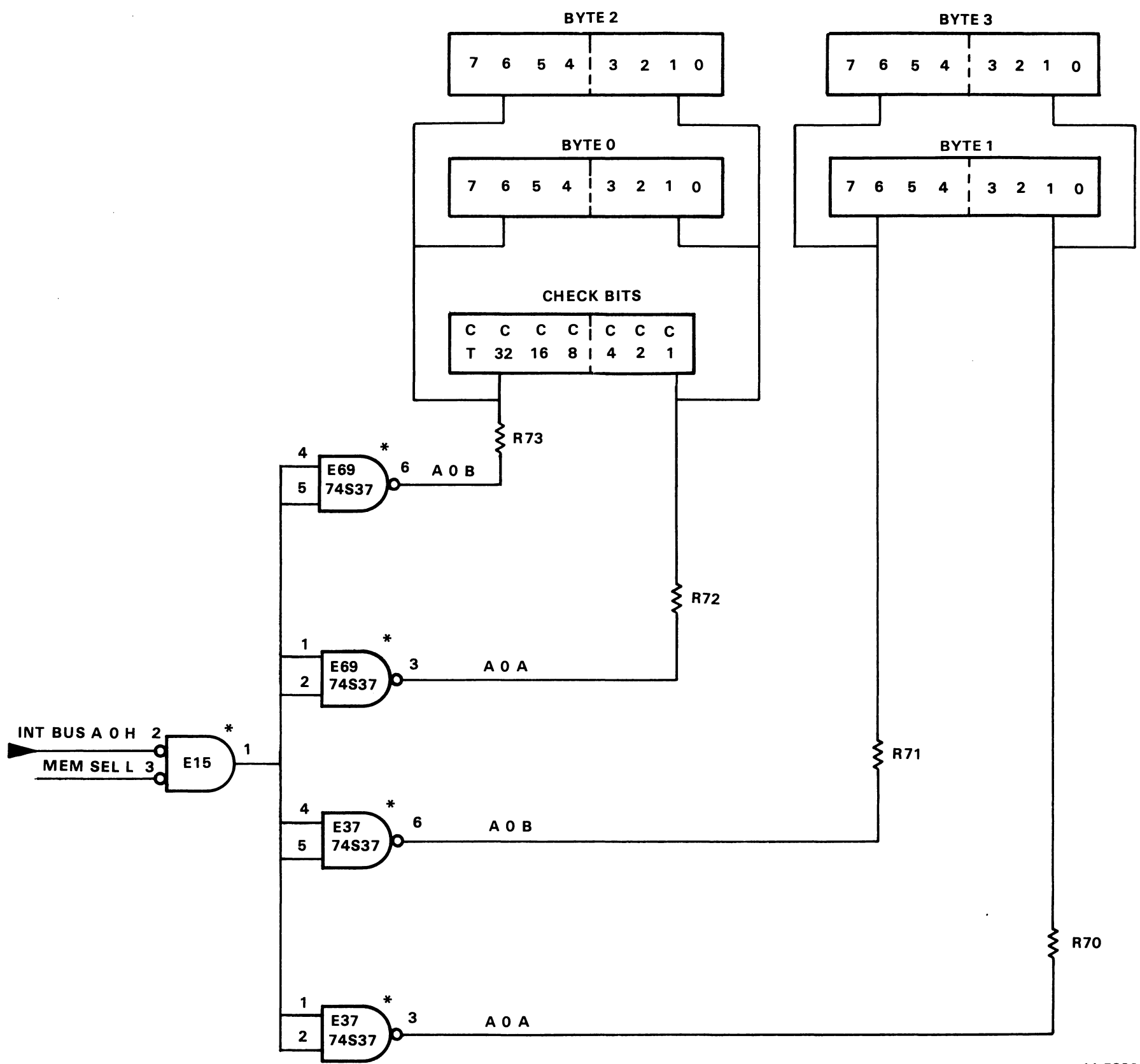
11-5423

Figure 4-4 Address Bit Functions



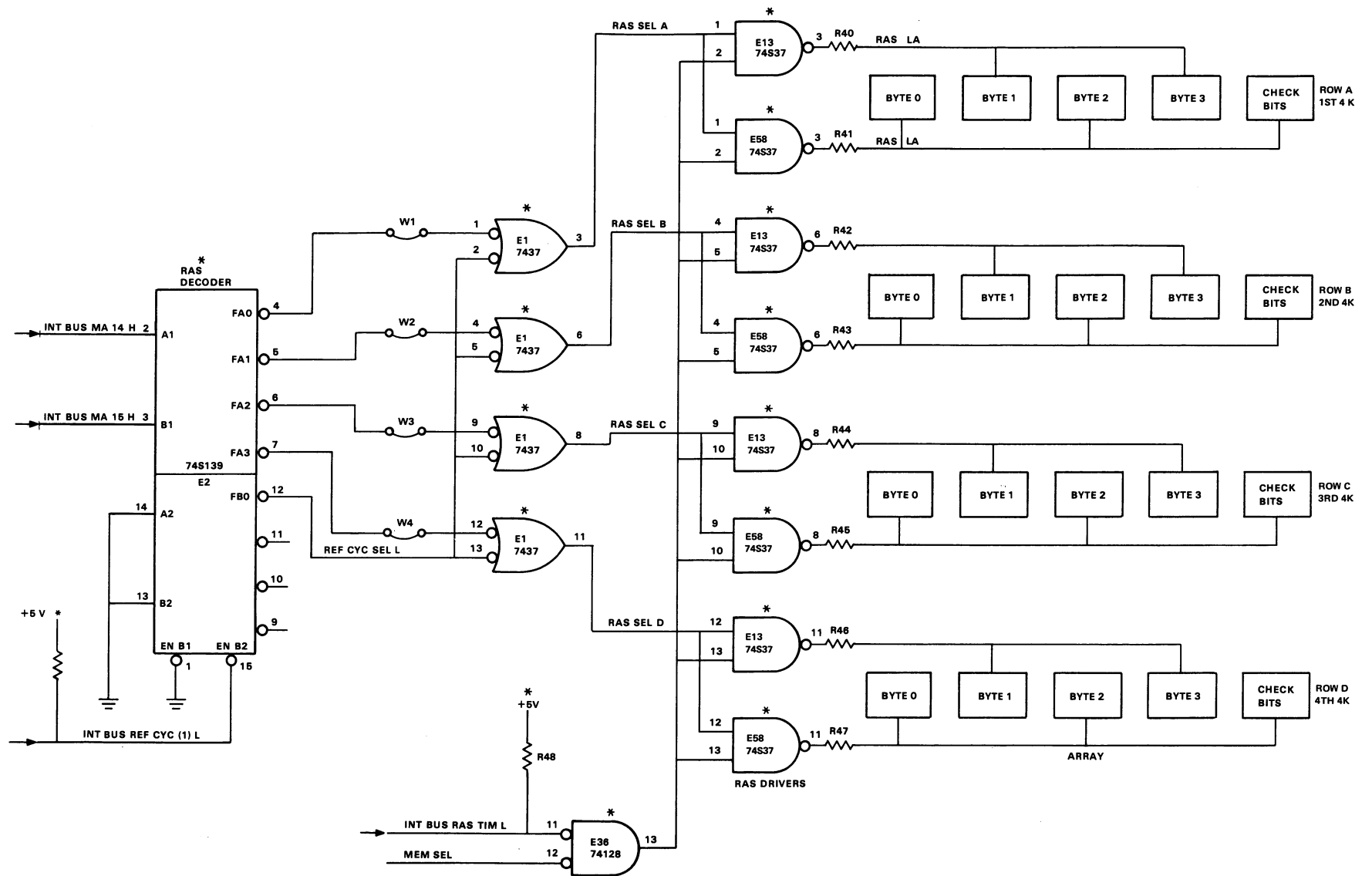
11-5422

Figure 4-5 Distribution of Internal Bus Write Byte Signals



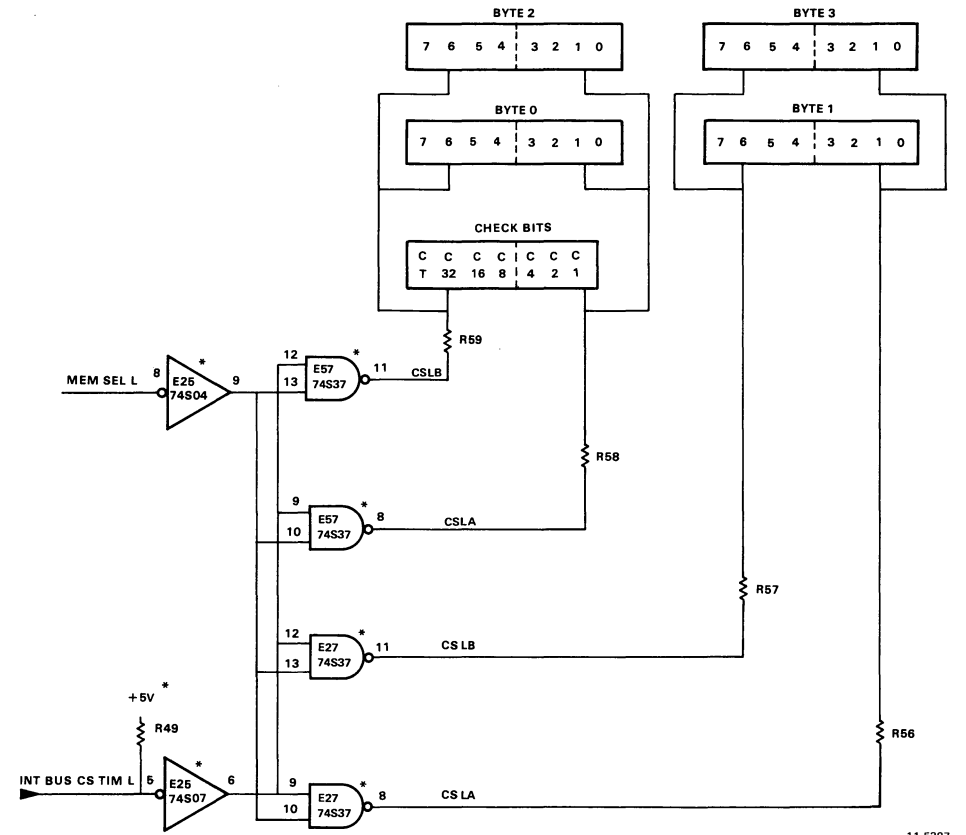
11-5386

Figure 4-6 Fanout of Address Signals, Example Address Bit 0



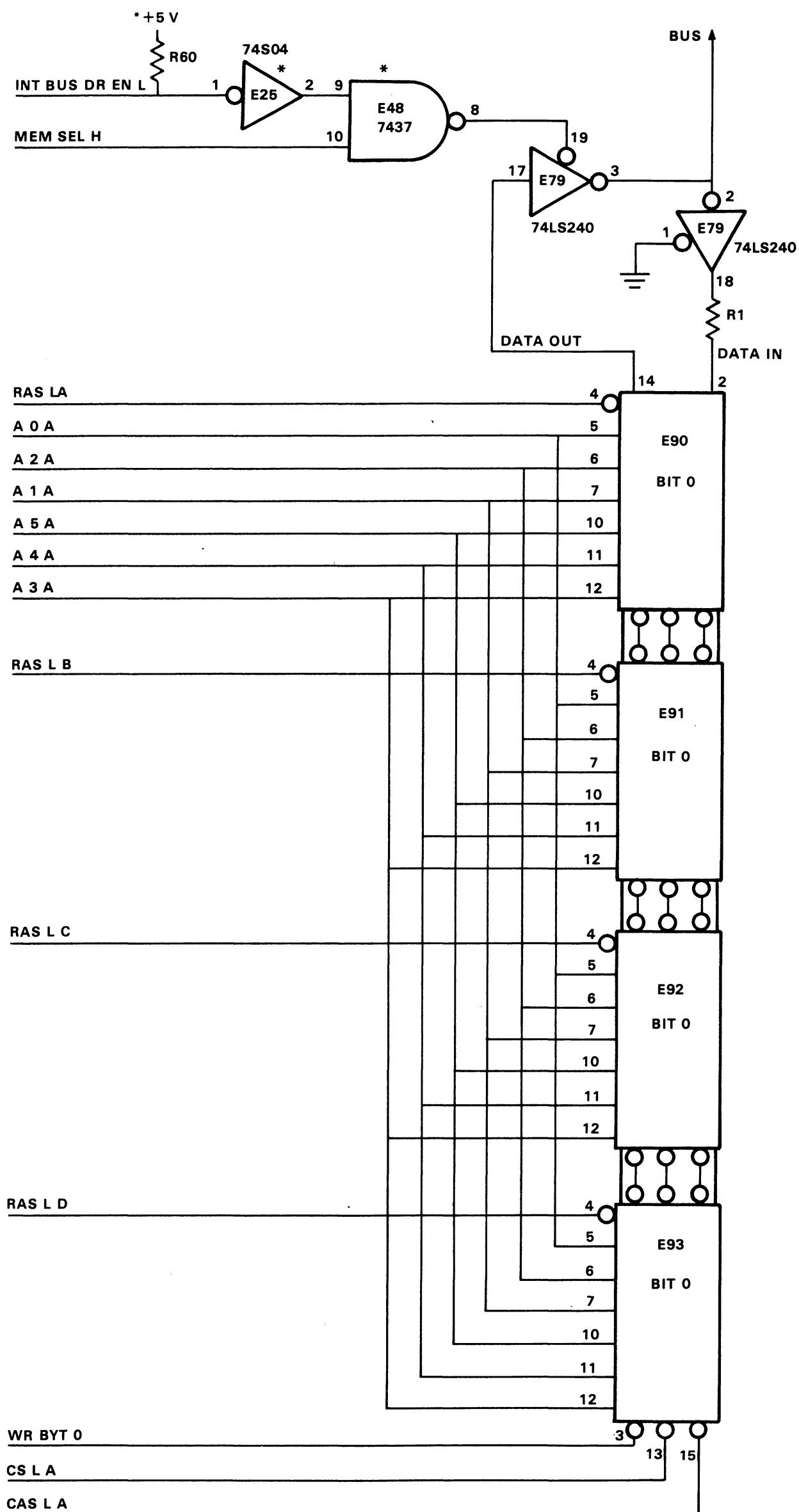
11-5421

Figure 4-7 Distribution of RAS Signals



11-5387

Figure 4-9 Distribution of the Chip Select Signal



11-5405

Figure 4-10 MOS Chip Control and Data Bit Driver/Receiver

CHAPTER 5

THE CONTROL MODULE: DETAILED EXPLANATION

5.1 GENERAL

The MF11S-K memory control module functions like an interface circuit in its relation to the bus master and the memory array. It receives address, data, and control signals from the Unibus. It then decodes the address and control signals and responds to them by triggering a timing chain and initiating read and write cycles, gating data via the data path from the Unibus to the array and from the array to the Unibus. The seven check bits that describe each double word in memory are generated and tested in the error correction circuit, enabling the control module to check the validity of data on read cycles and correct the single bit errors before gating a word to the Unibus. Figure 5-1 is a block diagram of the control module circuitry. Although the MF11S-K memory performs these storage and retrieval functions differently from other memory systems, the differences are not apparent to the processor and peripherals that act as bus masters.

The control module also initiates memory refresh cycles every 25 μ s, between data cycles, without reference to control and address signals from the Unibus. It also performs an error correction (ECC) initialization (ECC INIT) cycle, if data has been lost during a power down, writing zeros and corresponding check bit patterns into all memory locations.

5.2 DATA PATH

The data path of the MF11S-K forms a loop as shown in Figure 5-2. Data always moves clockwise through the loop, regardless of the type of data cycle in progress. It is accessible at various points in the loop for input or output on the buses and for manipulation and modification by the error correction logic and control circuits.

5.2.1 Data In Path

When data is gated from the array module to the Unibus, it is first loaded into the MDR from the internal memory bus. Although 32 data bits have been brought into the MDR, only 16 of them have been requested by the bus master. Therefore, the double word is fed into a set of 2:1 multiplexers where one of the words is selected, depending on the state of address bit 1.

The selected word is then compared with the bits that do the correcting. Any bit in error will be inverted.

The 16-bit word, which has at this point been selected and corrected, is then multiplexed with bits 00–15 of the CSR. The selected data word will be selected, again, if the CSR ADD SEL L line is false. Then, when SSYN L is asserted, it enables the Unibus drivers and the data word addressed is available to the bus master on the Unibus.

5.2.2 Data Out Path

When data is to be gated from the Unibus to the array, the one or two bytes to be moved are stored initially in the data latches shown in the block diagram (Figure 5-2). The control circuitry then demultiplexes the new data, in order to gate it to the appropriate bytes of the MDR and internal memory bus data lines.

5.3 ERROR CORRECTION LOGIC

The error correction logic performs two important functions. It corrects data bits in error on read cycles and it modifies check bits on write cycles. Figure 5-3 shows the relation of the error correction logic to the data path in block diagram form.

5.3.1 Error Correction Logic on a Data In

At the beginning of the read cycle, a 39-bit memory word is read into the control module from the array; 32 data bits are stored in the MDR; and seven check bits are stored in the check bit register. The check bit generator circuit is shown on sheet 6 of the prints. The data stored in the MDR is sent to the check bit generator, where check bits are generated on the data.

The check bits thus formed uniquely describe the 32-bit data pattern. These seven newly generated check bits are then Exclusive ORed with the seven check bits from the check bit register to form seven syndrome bits. A discrepancy will cause one of the syndrome bits to become true. If the newly generated check bits and the stored check bits are identical, the 32 data bits are correct.

The syndrome bits are then stored in the latches. Detection of a true syndrome bit will enable an error signal, ER SIG H, and thus L ER SIG H when the syndrome latches are clocked. The latched syndrome bits are then fed into an odd/even parity detector producing single-error or double-error indications. Remember that an even number of syndrome bits true indicates a double error.

Syndrome bits S1, S2, and S4 are fed into two 3:8 decoders (Figure 5-4). If a single error has been detected in the addressed word, and ECC DIS H and DERR L are both false, one of the 3:8 decoder chips will be enabled by the PROM signal ER H BYT L or ER L BYT L (Figure 5-5), and one of the 16 outputs will go low. If no error in the word addressed has been detected, or if a double error has been detected, the 3:8 decoders will remain disabled, their outputs high.

The 16 signals from the decoder circuit are then compared with the 16 bits of the word addressed (sheets 11 and 12 of the prints), forming a corrected data word.

There are three other points of interest at this time. First, the detection of a double-error condition in the 39-bit memory word will cause the 16-bit word addressed to be gated unaltered to the Unibus. Second, the syndrome bit St is used for the detection of double errors only. It is not decoded by the PROM or the 3:8 decoders. Third, detection of a check bit error will cause no alteration of data, as the PROM will not point to an error in either the high byte or the low byte.

5.3.2 ECC Logic on a Write Cycle

This discussion concerns the check bit modification process that occurs during any type of write cycle. The MF11S-K controller always reads a 39-bit memory word prior to the execution of a write operation. On a write following a DATIP cycle, the read operation is performed before the beginning of the write cycle. Otherwise, the memory performs an internal read-modify-write to accomplish the same result. The 39-bit memory word brought from the array will contain both data to be paired with the new data to be written and check bits describing the 32 data bits. Also, during the read preceding the write operation, new check bits have been generated and syndrome bits have been formed and latched. The PROM decodes the control signals, CO and C1, and the two lower address bits, LA00 and LA01, to generate signals that clock the one or two bytes to be written into the MDR.

Since the check bit generator continuously generates patterns on whatever is in the MDR, the check bit pattern generated at this point describes the double word newly formed in the MDR. The syndrome latches now point to errors, if any, in the old double word read from the array, while the generated check bits refer to the newly formed double word.

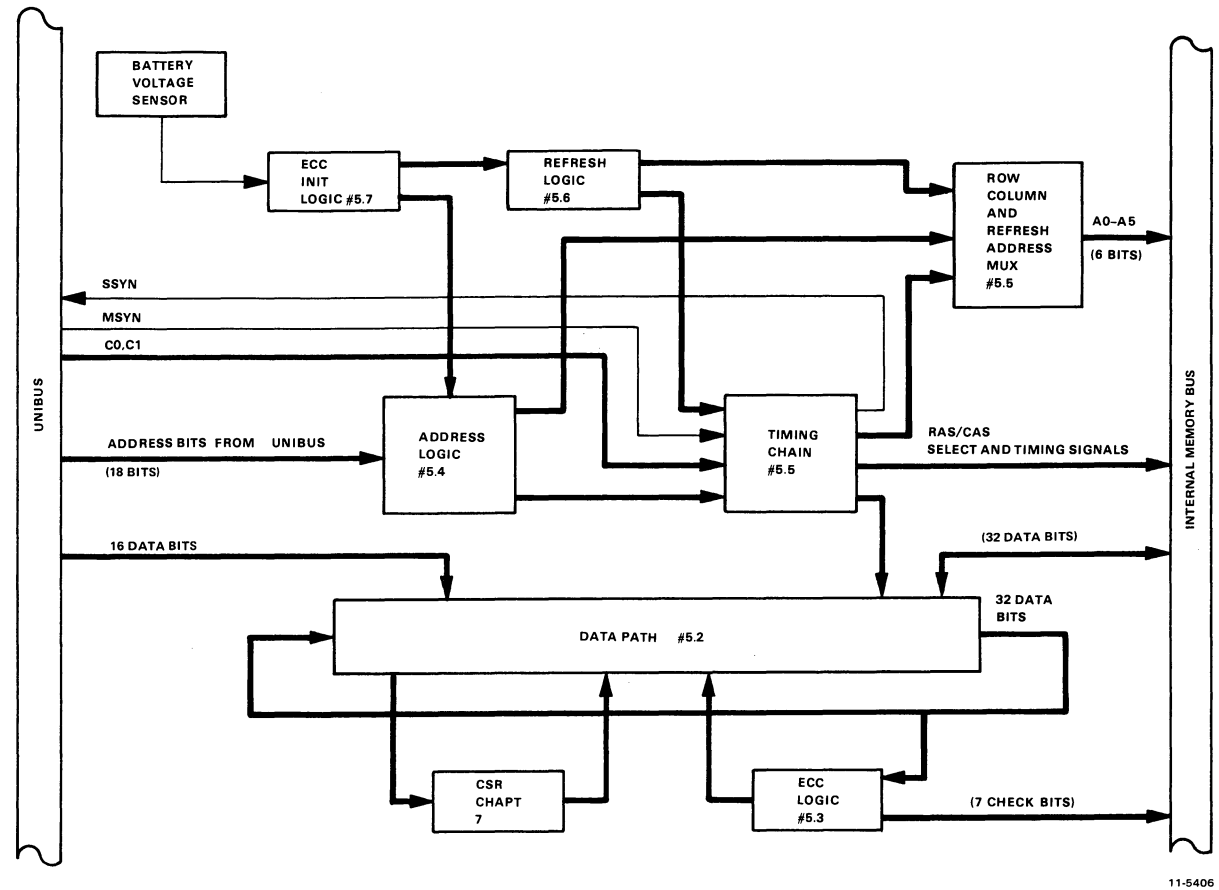
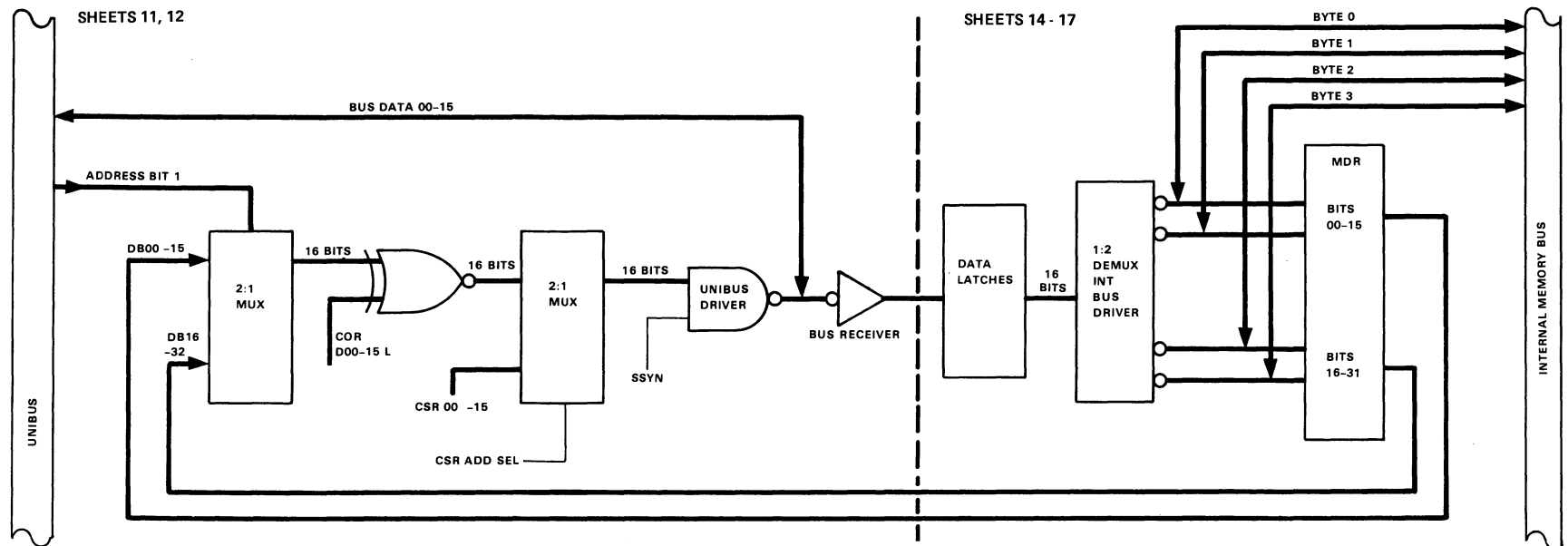
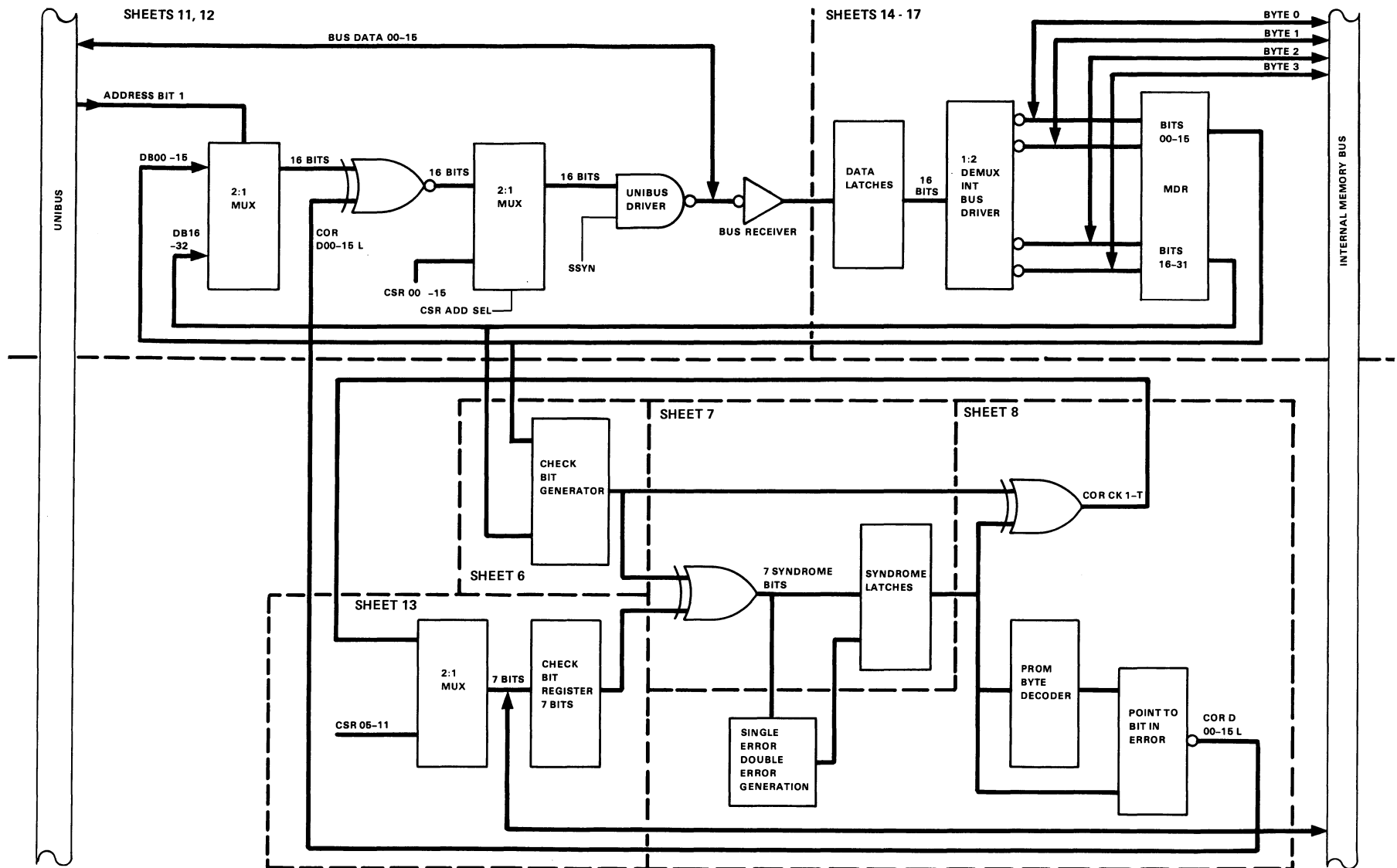


Figure 5-1 Control Module Block Diagram



11-5449

Figure 5-2 Data Path

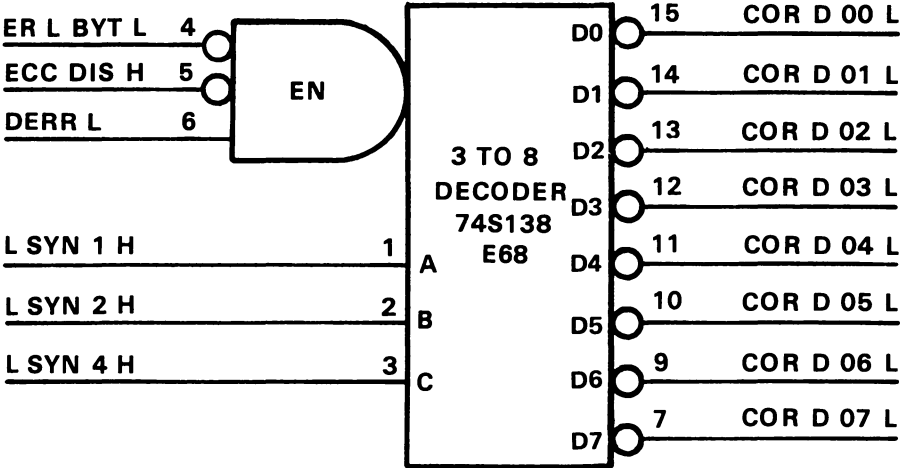


11-5448

Figure 5-3 Data Path and Error Correction Logic Block Diagram

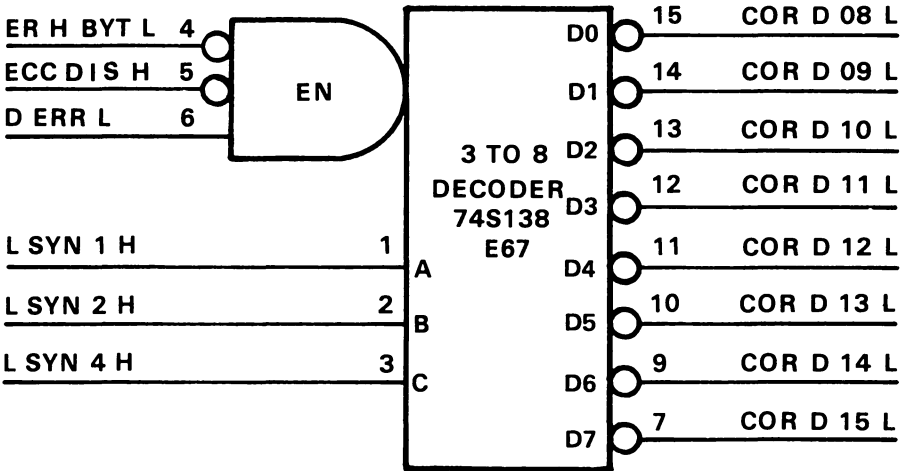
SHEET 8

CORRECT ERROR
IN LOW BYTE



THESE SIGNALS ARE USED TO
CORRECT THE APPROPRIATE
DATA BIT.

CORRECT ERROR
IN HIGH BYTE

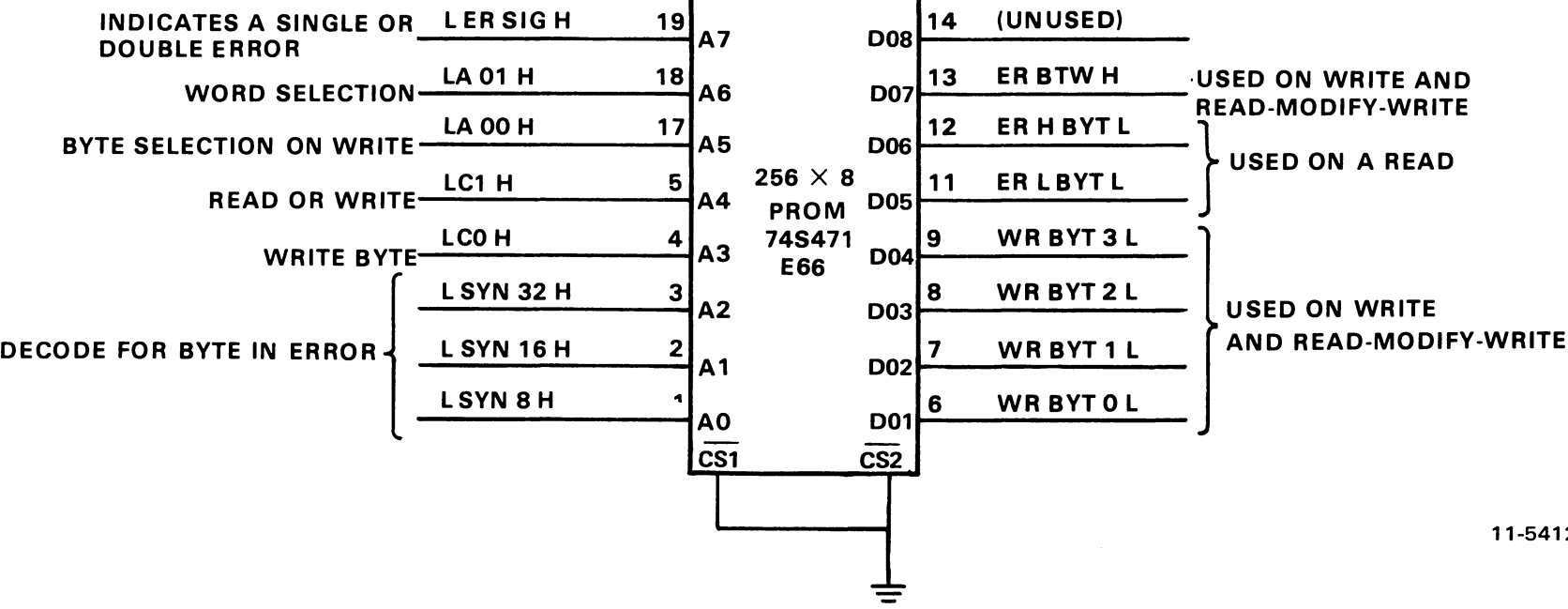


ONLY ONE OF THE SIXTEEN
OUTPUT SIGNALS CAN BE
ENABLED AT ONE TIME.

11-5411

Figure 5-4 Decoder to Correct Data Bit in Error

SHEET 8



11-5412

Figure 5-5 PROM

If one (or more) of the syndrome latches is high, the PROM decodes the upper three latched syndrome bits to determine whether or not the error is in a byte of the old double word that is to be written over. If the error is in a byte to be written over, the PROM generates the ER BTW H signal, which resets the syndrome latches (Figure 6-1 or sheet 7 of the prints). If an error is detected and it is not found to be in one of the bytes to be written, the syndrome latches will not be cleared. The error information is thus preserved.

Whether or not there is an error, the newly generated check bits are Exclusive ORed with the latched syndrome bits, forming seven corrected check bits. Then, appropriate signals from the timing chain cause the new data bytes and corrected check bits to be gated via the internal memory bus to the array (sheet 13 of the prints).

At this point, it will be useful to show how the check bit correction process functions with an example. Suppose that the old double word read from the array into the MDR contains a 1 in bit 0 and 0s in the remaining bits. Suppose, further, that bit 0 is in error, and that the data last written into that location was all zeros. A new 16-bit word containing a 1 in the MSB and 0s in the remaining bits is stored in the data latches from the Unibus. This word is to be written into byte positions 2 and 3 of the double word. Figure 5-6 shows the relationship between these groups of data and the check bits and syndrome bits formed.

A check bit pattern of 0111111 (where CT is 0) will have been stored with the old double word and latched in the check bit register. The check bit generator will then form a pattern of 0100111 on the double word in the MDR (bit 0 is in error). Syndrome bits ST, S16, and S8 will be set. The check bit pattern formed on the newly formed double word will be 0011000. Then, when the new data is written to memory, the syndrome bits will be ORed with the check bits formed on the new double word producing a corrected check bit pattern of 1000000. These corrected check bits will identify bit 0 as in error when decoded.

When the single-error/double-error generator circuit (Figure 5-3) encounters an even number of syndrome bits high, the even output is enabled, indicating a double-error condition. This signal, when enabled on a write cycle not following a DATIP, will cause the entire 39-bit memory word to be written back to the array unaltered.

5.4 ADDRESS DECODER LOGIC

A block diagram of the address decoder circuit is shown in Figure 5-7. When a device becomes bus master it causes BBSY to be asserted and then asserts a memory address on the eighteen address lines. The line receivers on the control module gate the address signals to the latch and multiplexer circuits shown.

Then, when the bus master asserts MSYN and the memory is addressed, the memory cycle timing starts, the Memory Busy flip-flop sets, and the ADD TIM (address time) H and L signals are generated, latching address and control lines until the end of the cycle.

5.4.1 Address Bits 14-17

Address bits 16 and 17 determine which array module is being addressed. Bits 14 and 15 determine which $8K \times 16$ bit ($4K \times 32$ bit) data block is being addressed. Signals A14-A17 are gated to the B inputs of a 2:1 multiplexer (Figure 5-8). The B inputs are selected at first, as the select input ADD TIM L is high before MSYN has been asserted on the Unibus. The B inputs of the multiplexer are thus gated through to the outputs, which, in turn, are routed to the A inputs of the multiplexer. At address time (ADD TIM L), therefore, when the A inputs are selected, the multiplexer forms a latch.

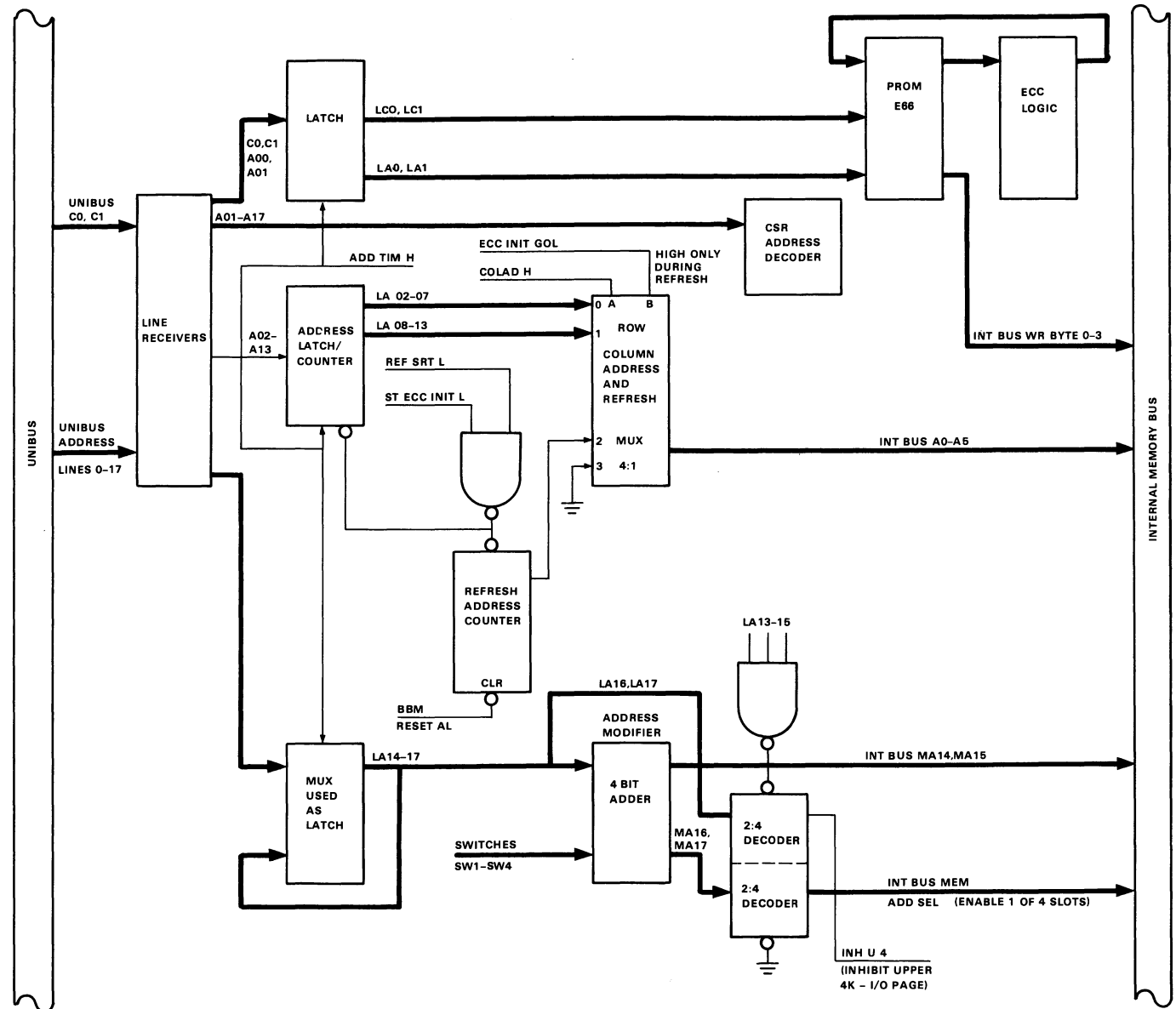
These latched address bits are added to the outputs of four microswitches in the 4-bit full adder that forms the address modifier circuit.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA STORED																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DATA RETRIEVED (MDR)																															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
DATA TO BE WRITTEN																															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NEW DOUBLE WORD (MDR)																															
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

CT	C ₃₁	C ₁₆	C ₈	C ₄	C ₂	C ₁
STORED CHECK BITS						
0	1	1	1	1	1	1
NEW CHECK BITS ON OLD DATA						
1	1	0	0	1	1	1
SYNDROME BITS						
ST	S ₃₂	S ₁₆	S ₈	S ₄	S ₂	S ₁
1	0	1	1	0	0	0
CHECK BITS FORMED ON NEW DOUBLE WORD						
0	0	1	1	0	0	0
CORRECTED CHECK BITS						
1	0	0	0	0	0	0

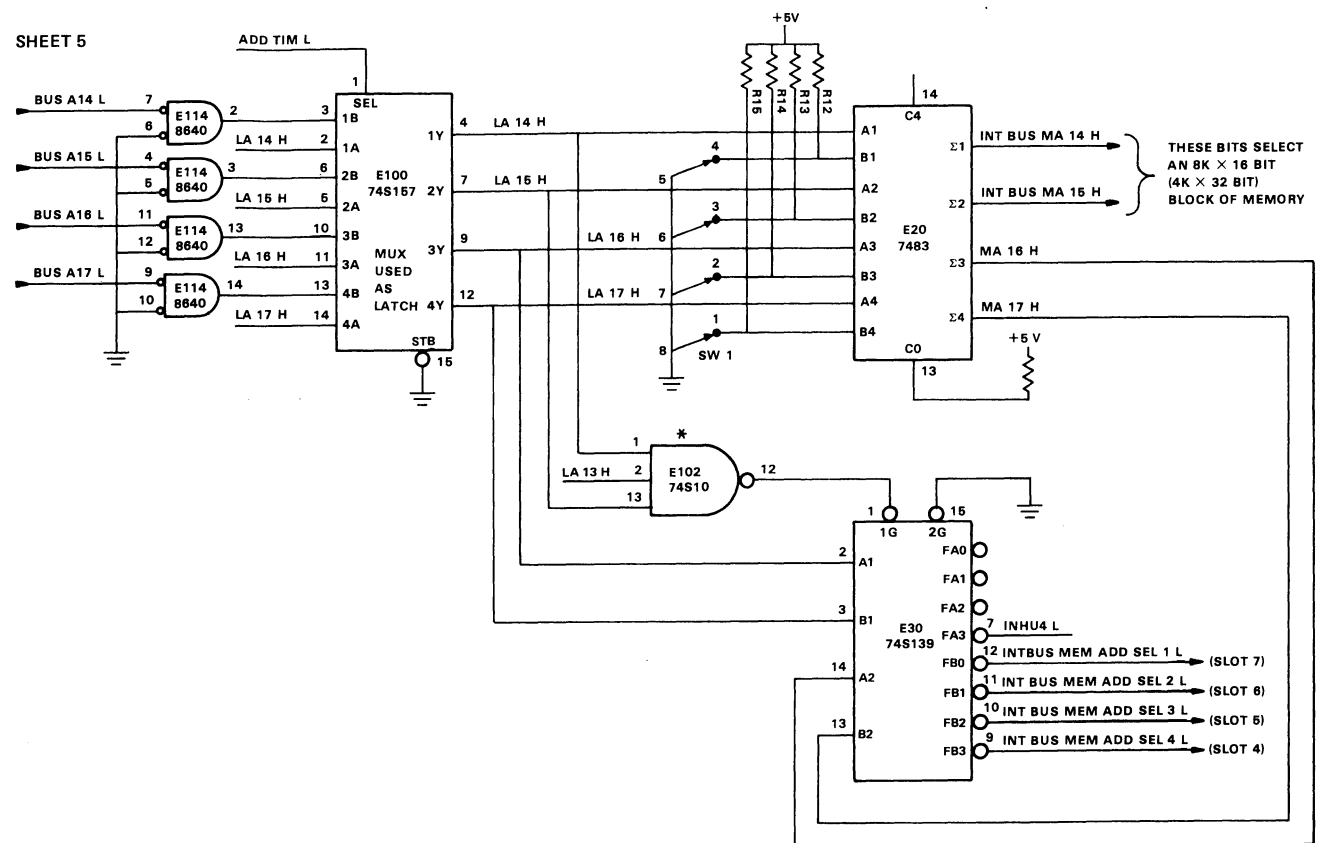
11-5433

Figure 5-6 Check Bit Correction



11-5404

Figure 5-7 Address Decoder Logic Block Diagram



11-5441

Figure 5-8 Address Bit 14-17 and Associated Logic

Table 5-1 gives the switch settings used for various starting addresses for the MF11S-K memory. Starting address 0 should be used if the MF11S-K is the only memory in the system or if it is to occupy the lowest memory address space in the system.

Table 5-1 Starting Address Selection

Starting Address Decimal	Starting Address Octal	Switch Setting			
		(A17) SW1-1	(A16) SW1-2	(A15) SW1-3	(A14) S1-4
0	0	F	F	F	F
8K	40000	F	F	F	N
16K	100000	F	F	N	F
24K	140000	F	F	N	N
32K	200000	F	N	F	F
40K	240000	F	N	F	N
48K	300000	F	N	N	F
56K	340000	F	N	N	N
64K	400000	N	F	F	F
72K	440000	N	F	F	N
80K	500000	N	F	N	F
88K	540000	N	F	N	N
96K	600000	N	N	F	F

NOTE: N = ON
F = OFF

Modified bits 14 and 15 are gated directly to the internal memory bus, while bits 16 and 17 are fed to the 2:4 decoder chip E30 as MA 16 and MA 17 (Figure 5-8). One of four internal bus memory address select lines is asserted low. Each of these four bus lines goes to the same pin number on one of the four array slots. If an array module is present in the selected slot, it responds with a memory present signal. The other half of the E30 multiplexer chip is used to generate the inhibit upper 4 signal (INH U4 L), which prevents the memory control module from addressing a memory location that is dedicated to the I/O page. INH U4 L thus disables the MEM GO L signal (see sheet 1 or Figure 5-11), preventing a memory cycle, when LA13–LA17 are all high.

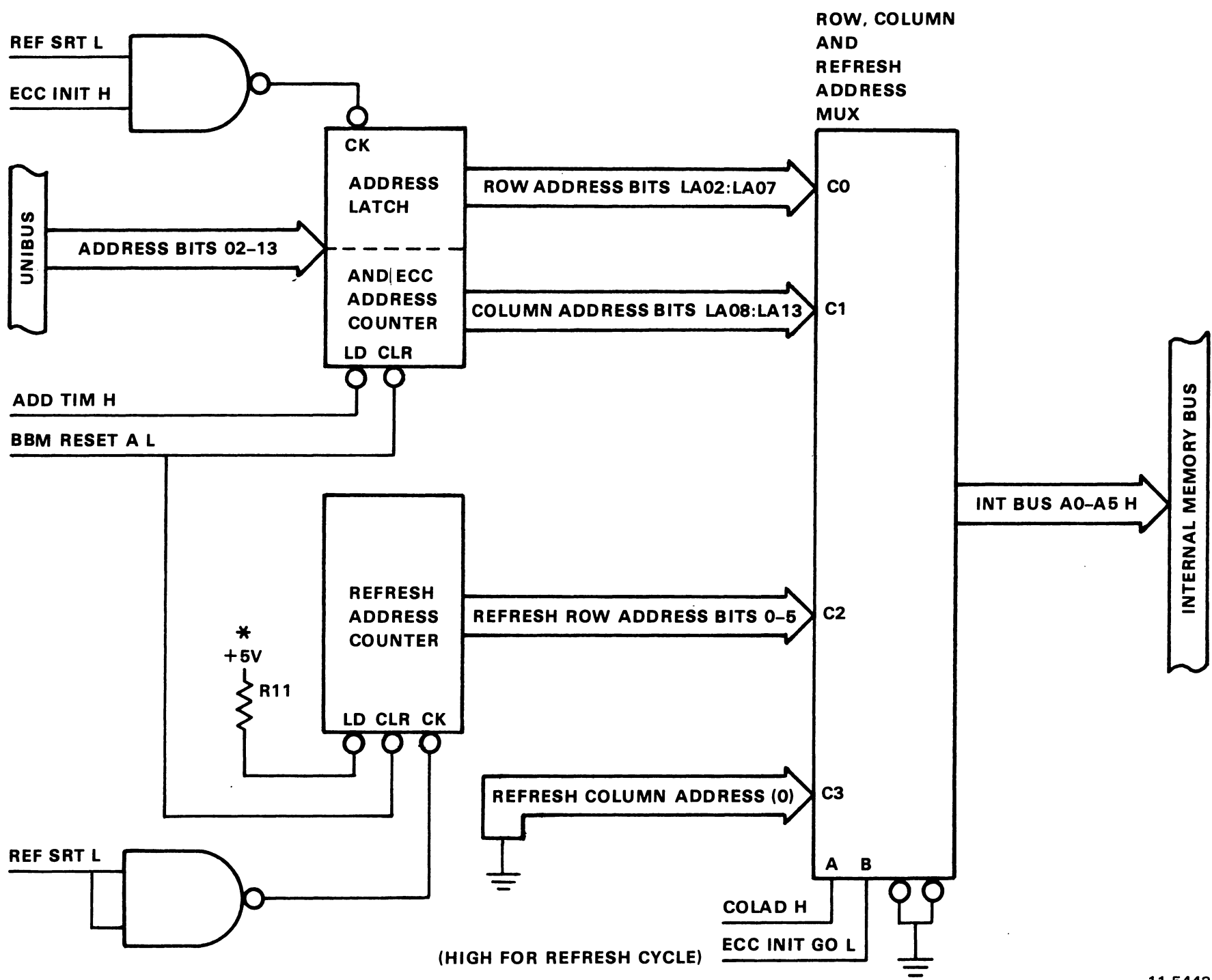
The user should notice that the maximum memory size in an MF11S-K system is 128K words. Thus, if the address switches are set improperly, and the MF11S-K memory size is too large to fit in the space allotted, an upper portion of the MF11S-K memory will wrap around to the bottom of memory. This condition may cause the MF11S-K memory to overlay some other memory within the system.

For example, if the switches are set so that S1-1 is on and S1-2, S1-3, and S1-4 are off, the starting address selected will be 64K. If three 32K array modules are installed in the system, the upper 32K address space will be wrapped around to overlay whatever memory is in the first 32K locations.

5.4.2 Address Bits 13–2

Three 4-bit programmable counter chips are used as latches for Unibus address bits 13–2. Before the memory cycle starts, the load/count input to the counters (ADD TIM H) is low (sheet 4). The latches are preset, or cleared, according to the inputs from the line receivers. When ADD TIM H goes high, it disables the inputs, and address bits 13–2 are permanently latched in the flip-flops within the counters.

These latched address bits are routed to the inputs of the row, column, and refresh address multiplexer as two pairs of six bits. Bits 2–7 form the row address, while bits 8–13 form the column address. The row address signals are gated to the internal memory bus initially. The column address signals follow at column address time. This row, column and refresh address multiplexer is a 4:1 multiplexer (Figure 5-9).



11-5442

Figure 5-9 Row, Column, and Refresh Address Multiplexer Associated Logic

The four states of the multiplexer are shown in Table 5-2.

Table 5-2 Multiplexer States

Select Lines		Signals Selected
B	A	For output to INT BUS A0 H – A5 H
ECC/INIT GO L	COLAD H	
0	0	LA 02 H – LA 07 H, Row Address
0	1	LA 08 H – LA 13 H, Column Address
1	0	Refresh Row Address Counter Outputs
1	1	Ground, Refresh Column Address

The refresh address counter outputs are selected at the beginning of a refresh cycle, row address time, when ECC INIT GO L goes high (sheet 1). Zeros are selected at column address time in the refresh cycle, when COLAD H becomes true.

Note that the signal ECC INIT GO L is a refresh override signal. It will be true if the Refresh Cycle flip-flop is reset or if the ST ECC INIT L signal is true (sheet 1). Therefore, ECC INIT GO L will go low during an ECC initialization routine, forcing the row, column, and refresh address multiplexer to select inputs A and B for row and column addresses, regardless of the state of the Refresh Cycle flip-flop.

5.4.3 Address Bits 1 and 0

Address bits 1 and 0, together with C1 and C0, are transferred to the outputs of the E91 latch before MBSY sets. When the memory cycle starts, MBSY H causes ADD TIM L to become true, retaining the data in the latches. The two lowest address bits are input to the PROM (Figure 5-5), where write byte and error location signals are generated.

5.5 TIMING CHAIN

The timing control logic is used in all memory operations. It is run from a series of delay lines for the sake of stability and accuracy, and it allows the generation of a large number of timing pulses. The memory location to be addressed and the control signals designating the type of operation to be performed are placed on the Unibus before the assertion of MSYN (master sync). The MSYN signal is gated through a line receiver to a 13 input NAND gate (Figure 5-10). The conditions that must be met in order to initiate a memory cycle are fed into the NAND gate with MSYN to qualify MEM GO L. DC LO must be high, the address decoder must have selected a slot containing an array module (INT BUS MEM PRES L true), the memory must not be busy (MBSY L and SSYN L are high), and the location addressed must not be on the I/O page (INH U4 L is high). MEM GO L is ORed with a refresh request (REF REQ H MBSY L) to produce SRT CK H.

The TIM ST H latch can be set in two ways, depending on whether the cycle initiated is a data cycle or a refresh cycle (Figure 5-11). In a data cycle the latch is set quickly (Figure 5-12). In a refresh cycle the setting of the TIM ST latch is delayed in order to allow for the settling time of the Refresh Cycle flip-flop (Figure 5-13). Note that in both cases the setting of the latch is delayed.

TIM ST H and TIM ST L are then enabled, setting the Memory Busy flip-flop, and sending a positive going signal to the delay line DL 1. Transistor Q1 and inductor L1 ensure that the input pulse to the delay line is driven to a higher voltage level than would be possible with the 8885 gate. This circuit gives good noise immunity to the pulses generated on DL 1 and DL 2, the most critical of the timing signals. Feedback from the DL 100 H line terminates the pulse (Figure 5-14), resetting the TIM ST latch.

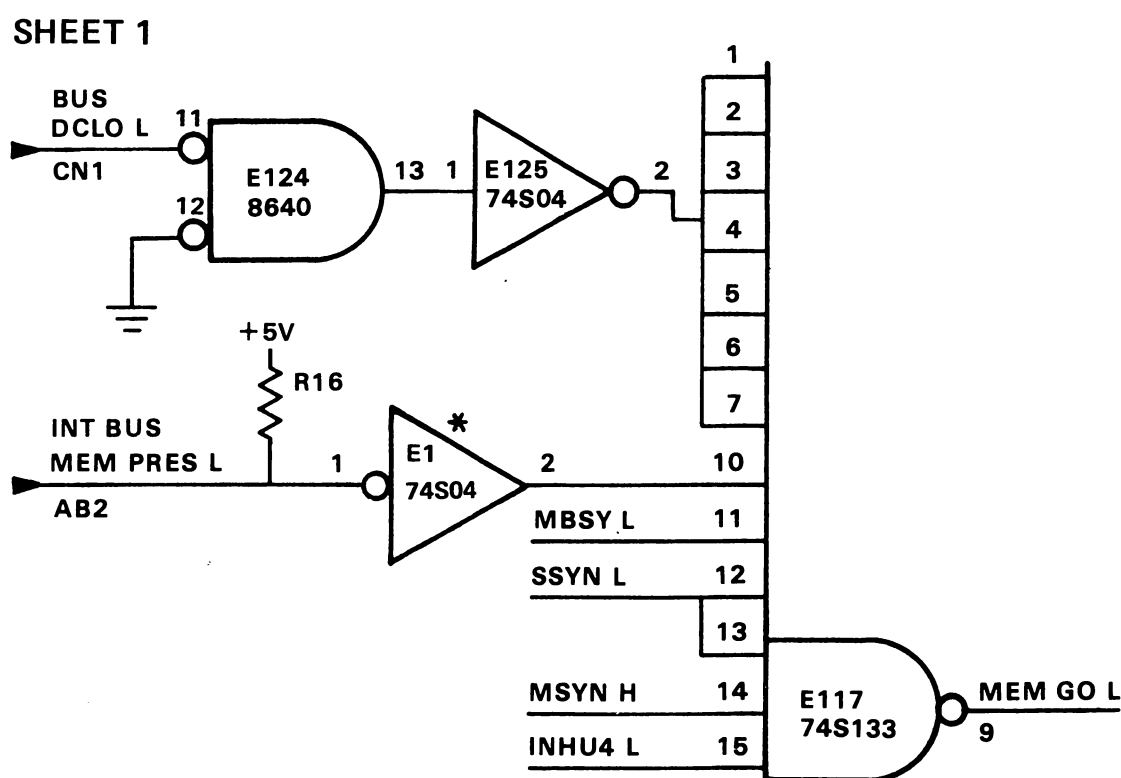
NOTE

When the circuit is in the quiescent state, current flows from the delay line through L1 and is sunk through E129. When E129 pin 6 goes high, current flows into the base of 21 forcing it into saturation. The high level of the pulse to DL 1 is, therefore, +5 V - Q1 VCE.

Delay line DL 1 triggers DL 2 producing the timed signals DL 275 H through DL 500 H. The signals from these two delay lines feed the address multiplexer (through the CAS Timing flip-flop), the RAS circuit, the internal memory bus, the internal read-modify-write circuit, and the slave sync circuit.

Delay line DL 3 is triggered only in connection with the internal read-modify-write cycle. It extends the duration of the memory cycle.

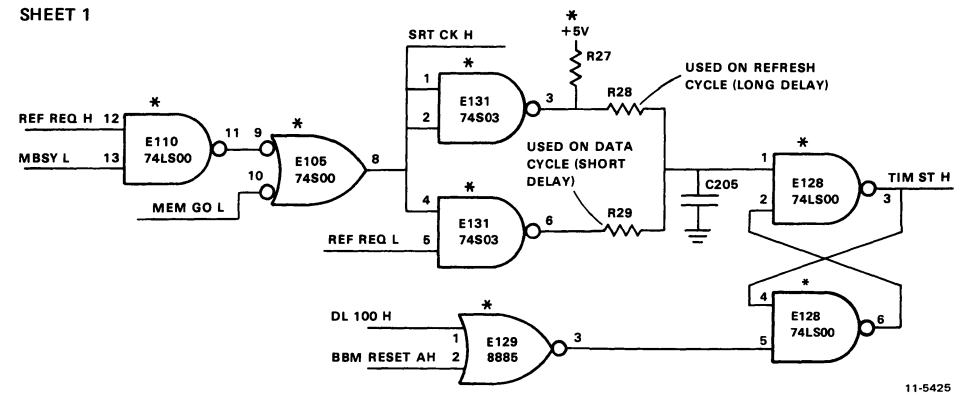
Delay line DL 4 is triggered by DL 375 H during a read cycle, an internal write cycle, a refresh cycle, and by DL 725 L, from DL 3, during an internal read-modify-write cycle. It generates signals that terminate the memory cycle.



11-5424

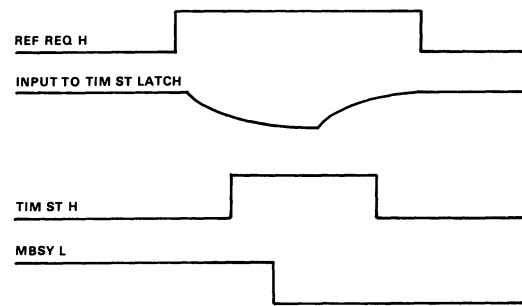
Figure 5-10 Qualifying MEM GO L

SHEET 1



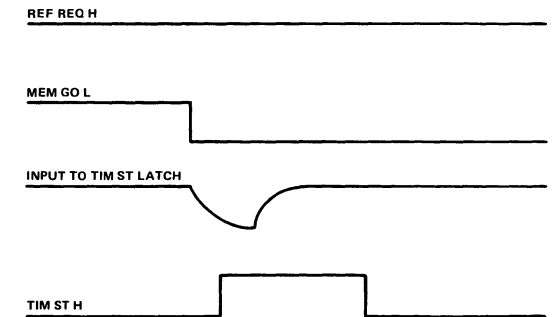
11-5425

Figure 5-11 Generation of TIM ST H



11-5426

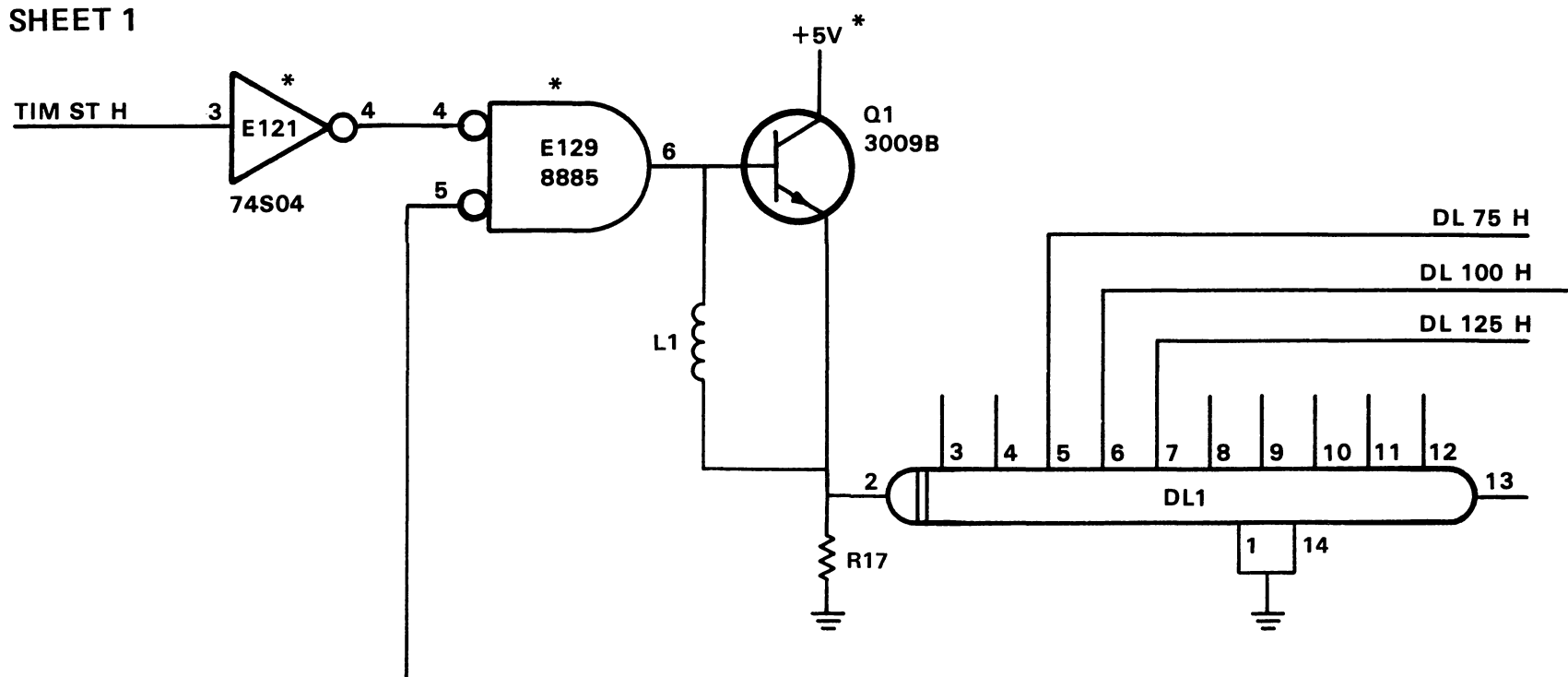
Figure 5-12 Starting the Timing Chain on a Refresh Cycle



11-5446

Figure 5-13 Starting the Timing Chain on a Data Cycle

SHEET 1



* NOTE:

When the circuit is in the quiescent state, current flows from the delay line through L1 and is sunk through E129. When E129 pin 6 goes high, current flows into the base of Q1 forcing it into saturation. The high level of the pulse to DL1 is therefore $+5V - Q1 V_{CE}$.

11-5407

Figure 5-14 Triggering the Delay Line DL 1

CHAPTER 6 MEMORY CYCLES

6.1 GENERAL

At this point, the reader should be able to use the foregoing explanations of the data path, error correction logic, address decoder logic, and timing chain in understanding a description of the memory data cycles. For the sake of clarity, some of the points previously made will be re-emphasized, and some figures will be repeated. The reader should make frequent reference to the flowcharts and timing diagrams provided when following the data cycle descriptions. It is important to maintain a concept of each cycle as a whole, while dealing with the details of the hardware.

When a bus master successfully initiates a memory data cycle and the timing chain has been triggered, the condition of line C1 (true or false) determines whether or not a write or read cycle will be performed (Table 6-1).

Table 6-1 Memory Data Cycle Selection

	C1	C0
DATI	False	False
DATIP	False	True
DATO	True	False
DATOB	True	True

6.2 READ CYCLE (DATI, DATIP)

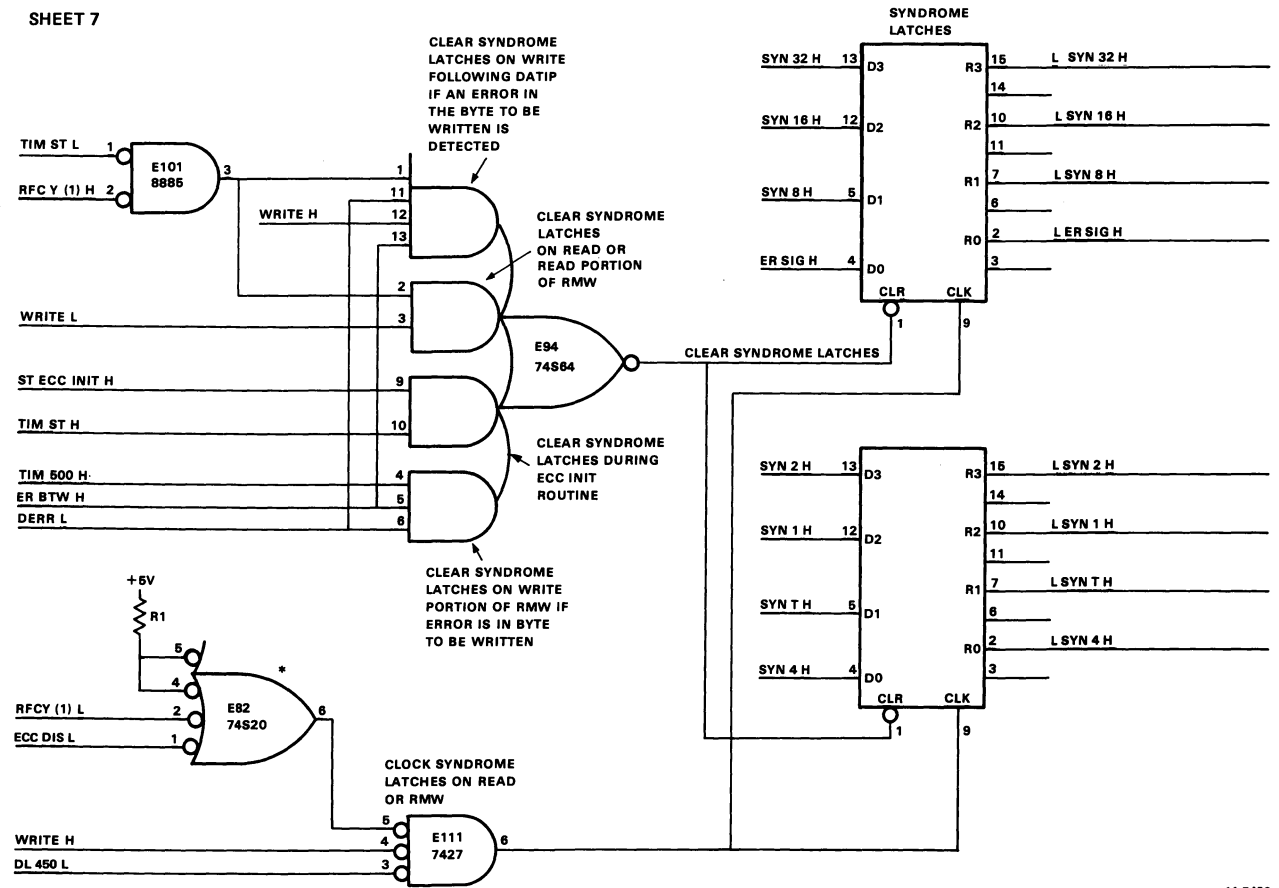
If the cycle to be performed is a read operation, the C1 signal is false (LC1 L is high), and WRITE L high is ANDed with the ANDing of TIM ST L and RECY (1) H to reset the syndrome latches (Figure 6-1). Figure 6-2 shows the read cycle flowchart.

6.2.1 Fetching the Data, DATI/DATIP

The latched address signals are gated to the array as explained in Paragraph 5.4 (address decoder logic). The array module that is being addressed is selected before MSYN is received. Row address bits 7-2 (the first of the four multiplexer inputs) are selected by the row, column, and refresh address multiplexer as COLAD H and ECC INIT GO L are both low. The row address strobe is then sent to the array at the beginning of the timing chain, when TIM ST L becomes true. Figure 6-3 is a timing diagram for the read cycle.

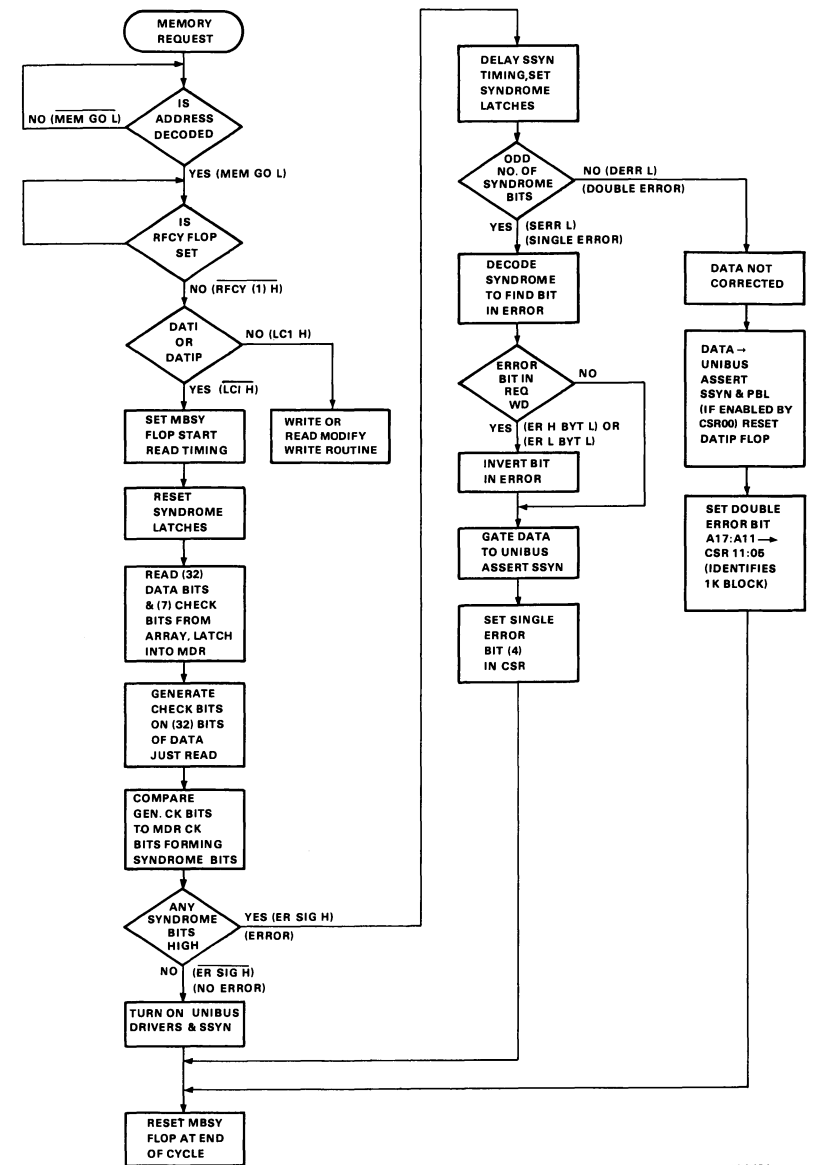
INT BUS RAS TIM L clocks the row address bits into the row address registers of the 39 selected RAM chips on the array.

SHEET 7



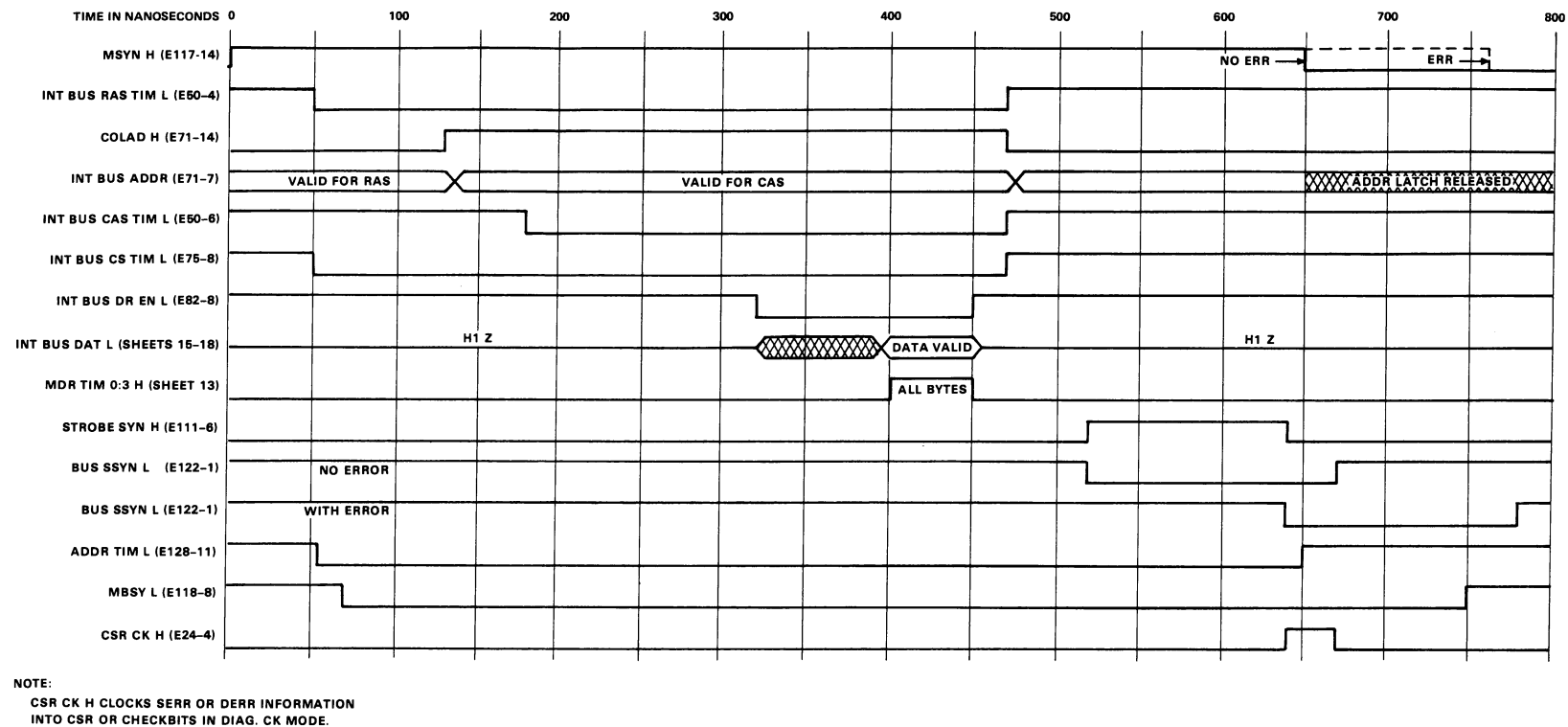
11-5432

Figure 6-1 Resetting the Syndrome Latches on a Read



11-5434

Figure 6-2 Read Cycle Flowchart



11-5439

Figure 6-3 Read Cycle
Timing Diagram

The column address bits (13–8) are selected by the multiplexer when DL 75 H goes true, enabling COLAD H. These bits are clocked into the column address registers of the selected RAM chips with DL 125 H, when the CAS Timing flip-flop sets (INT BUS CAS TIM L). Figure 6-4 shows the column address timing logic.

With the row and column addresses latched on the address registers of the RAM chips, the 39-bit word selected is gated from the RAM chip outputs on the array to the line drivers. Then, following the DL 25 signal, the INT BUS DR ENB signal is generated on the controller, enabling the RAM data onto the internal memory bus data lines (Figure 6-5). The INT BUS DR ENB signal provides a window for the data transfer. The DL 350 H signal generates the five MDR TIM signals within that window, clocking the data from the array into the 32 MDR latches and seven check bit latches (Figure 6-6).

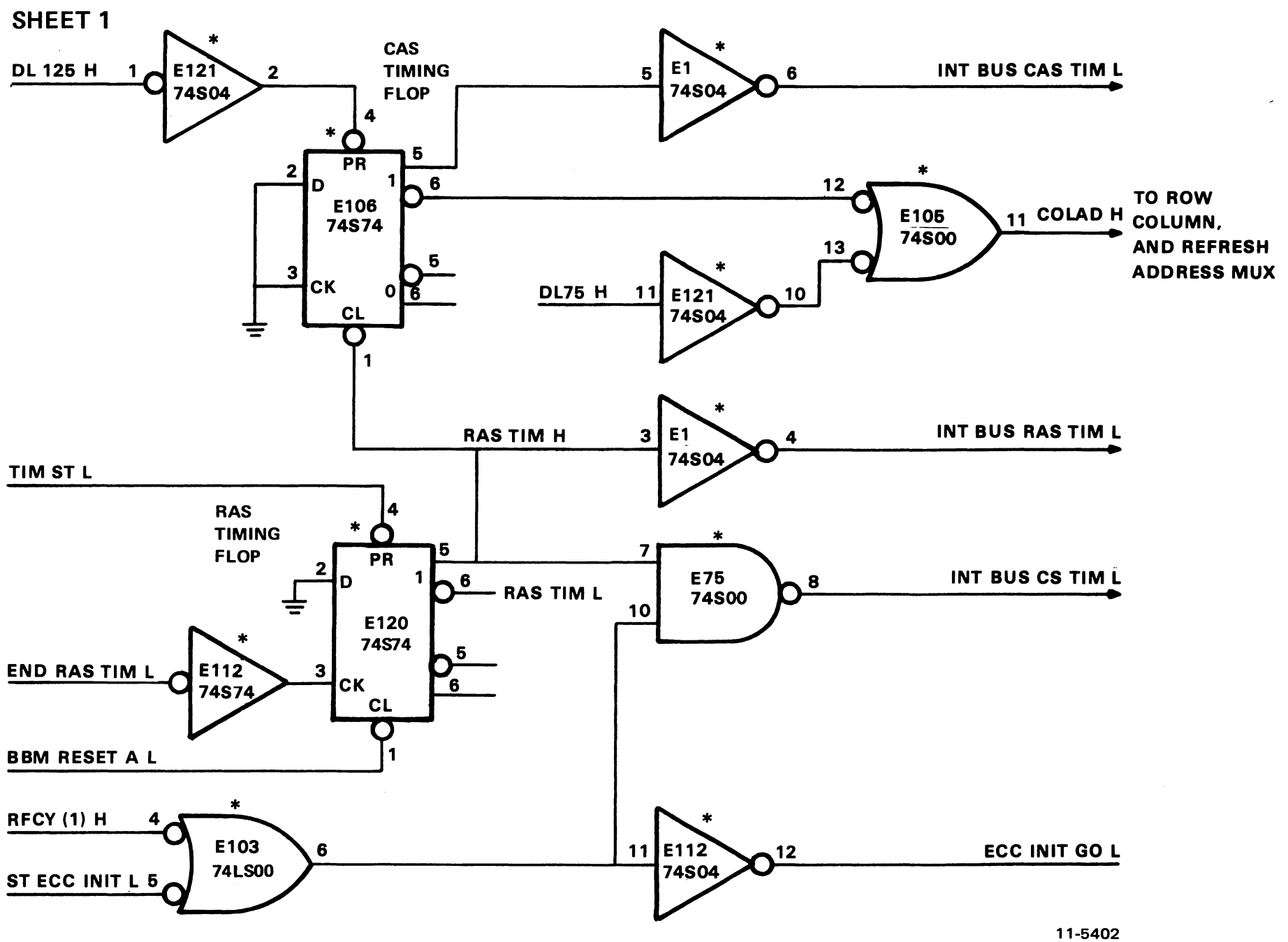
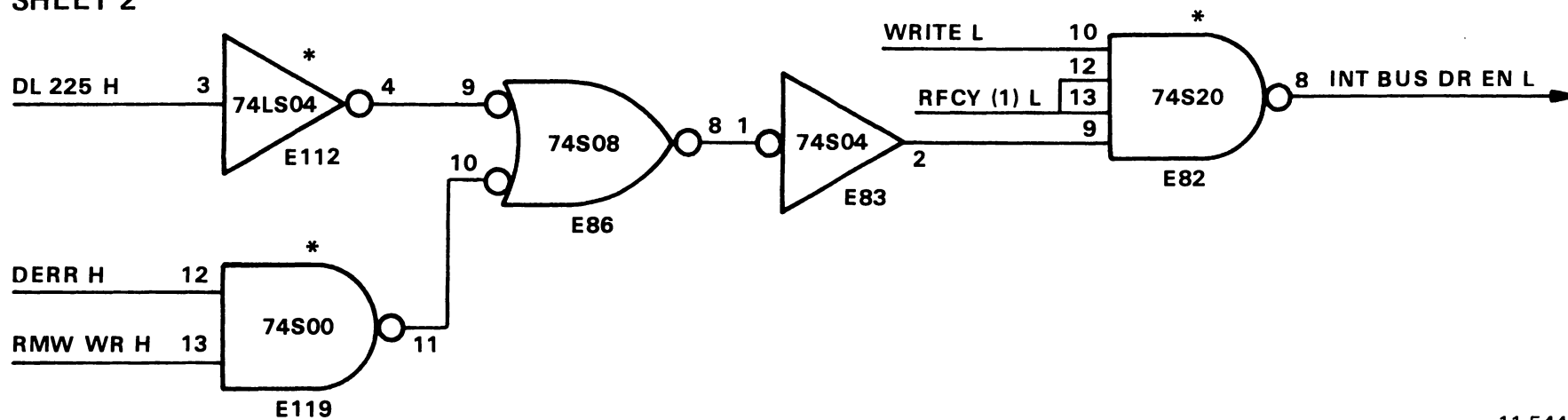


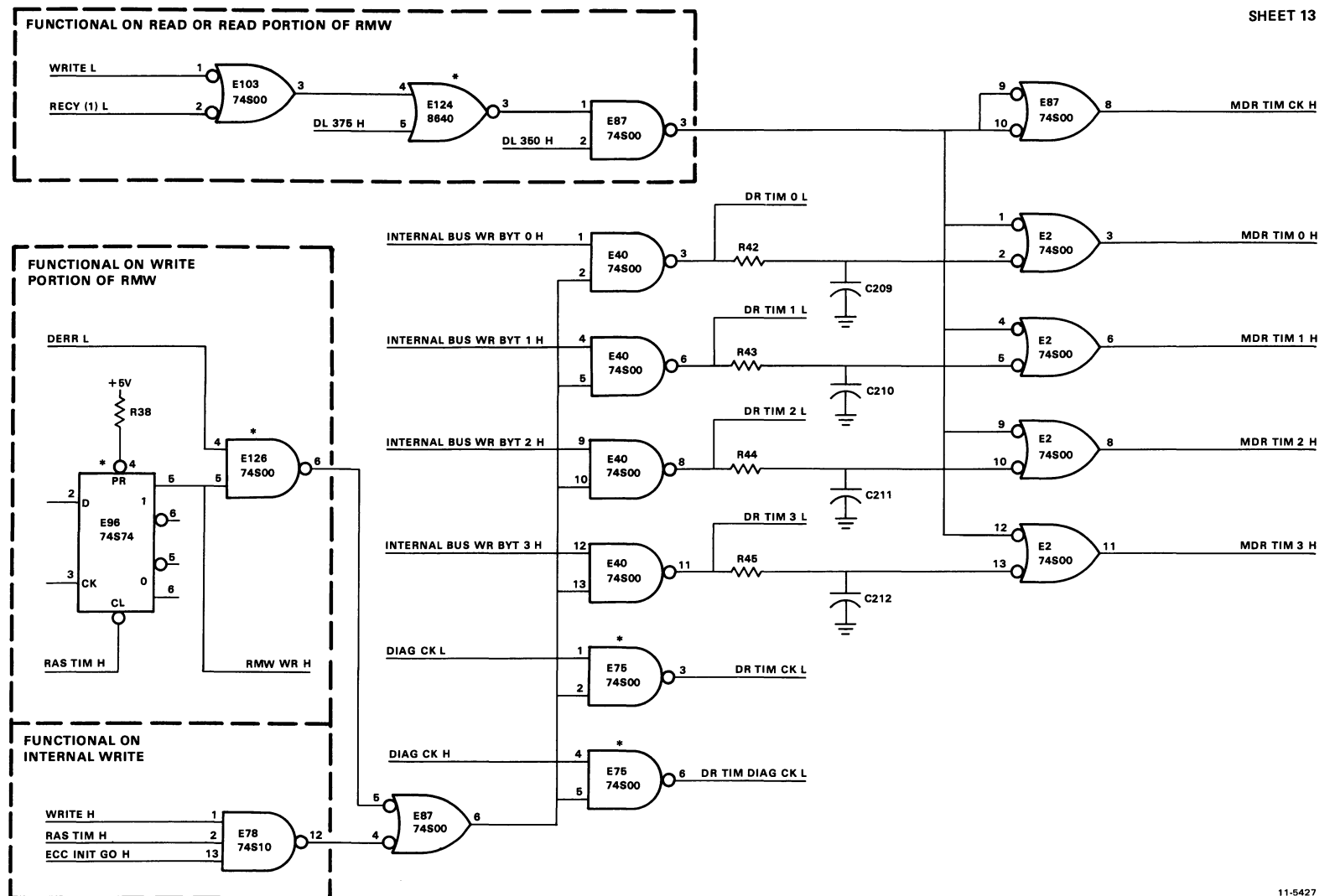
Figure 6-4 Column Address Timing Logic

SHEET 2



11-5443

Figure 6-5 INT BUS DR ENB Signal



11-5427

Figure 6-6 Clocking the MDR

6.2.2 Checking the Double Word (No Error Found), DATI/DATIP

The error correction logic forms new check bits on the double word and Exclusive ORs them with the old check bits read from memory, forming syndrome bits.

If no error is detected (no syndrome bits are high), DL 450 H is selected by the multiplexer on E95 (Figure 6-7).

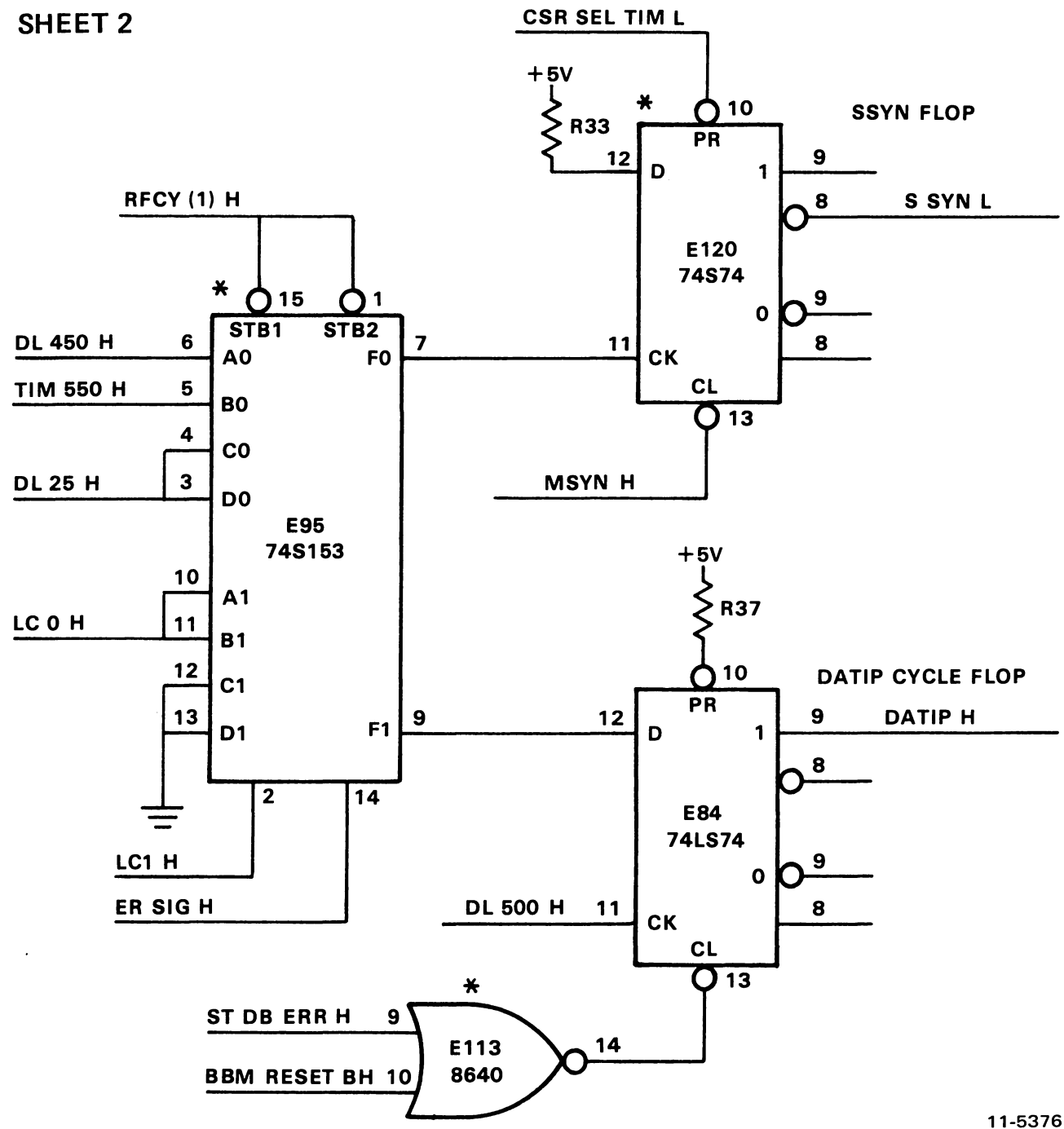
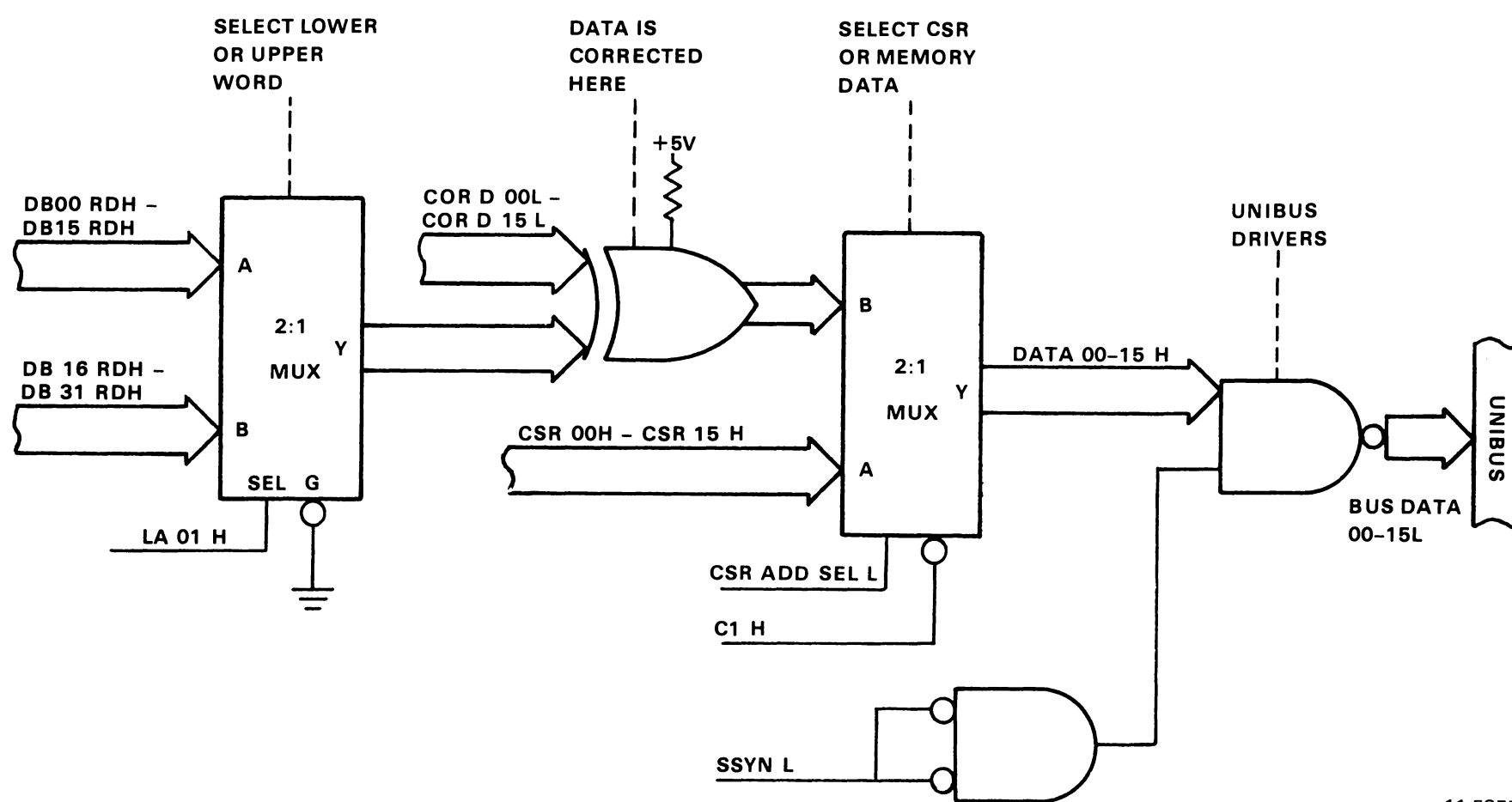


Figure 6-7 Setting the SSYN Flip-Flop

The SSYN (Slave Sync) flip-flop sets when DL 450 H goes high, generating SSYN L. This signal is gated to the Unibus as BUS SSYN L and it also enables the Unibus data drivers for the 16 Unibus data lines. The data that is put out on the bus is the word addressed on the Unibus address lines.

The data is selected as follows. The 32 data bits of the double word held in the MDR are gated to the inputs of four 2:1 multiplexers (Figure 6-8). Bytes 0 and 1 (bits 0–15) are selected if LA 01 H is low, while bytes 2 and 3 are selected if LA 01 H is high. The outputs of these four multiplexers are compared with the COR D bits COR D00 – 15 L (which should all be low if there is no error) forming one of two sets of inputs to the second group of four 2:1 multiplexers. The other set of inputs are the CSR bits (Figure 6-8). The select line, CSR ADD SEL L, will be false (unless the CSR is being addressed) and the two selected bytes will be gated to the Unibus data lines when SSYN L enables the Unibus drivers.



11-5377

Figure 6-8 Data Word Selection

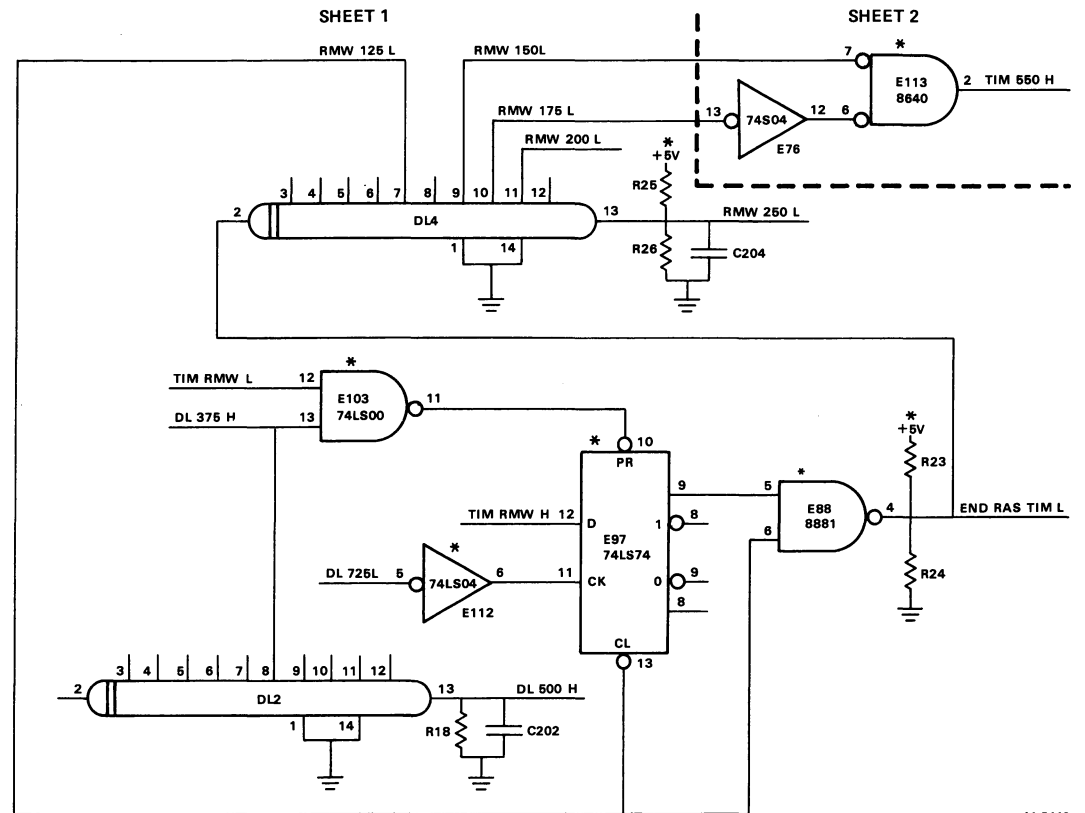
6.2.3 Checking the Double Word (Single Error), DATI/DATIP

Detection of an error (ER SIG H) in the read cycle will cause a 110 ns delay in the setting of the SSYN flip-flop, by forcing the multiplexer on E95 to select the second input, TIM 550 H, instead of the first, DL 450 H (Figure 6-14), TIM 550 H is generated, on a read cycle, after DL 375 H causes the flip-flop at E97 to be set through the preset input, triggering delay line DL 4 (Figure 6-9).

TIM 550 H goes high for 25 ns following the occurrence of RMW 150 L, setting the SSYN flip-flop. Notice that the MSYN H signal is tied to the clear input of the SSYN flip-flop, ensuring that SSYN does not set unless MSYN is asserted.

The 110 ns delay in the setting of SSYN is all that is needed to correct a single bit error, allowing corrected data to be gated to the Unibus; the process is as follows. The syndrome bits are latched when DL 450 L becomes true. The seven latched syndrome bits are fed into the 74S280 parity generator IC (E79), which checks to see if the number of syndrome bits high is odd or even. If the odd output is true, the error condition will be dealt with as a single error. S ERR H is then generated, causing CSR bit 4 to be direct set with TIM 550 H, if LC1 L is false (write cycle not in progress) (Figure 6-10).

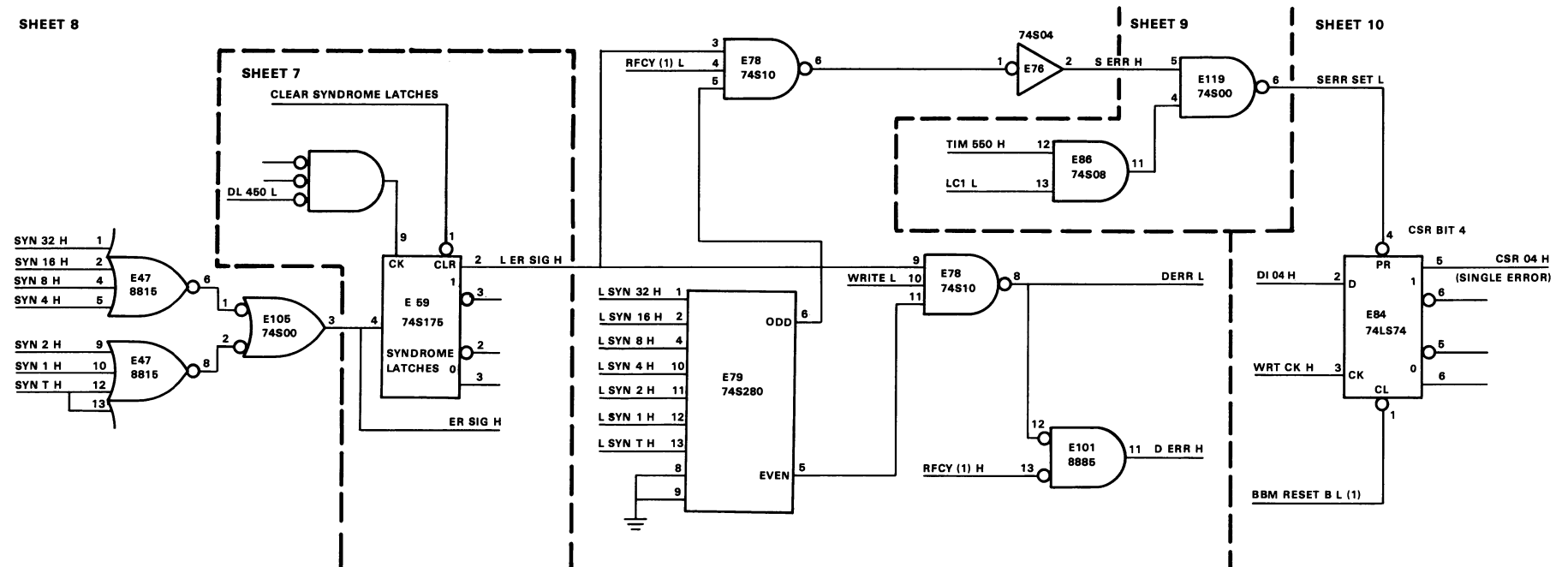
Note that any odd number of high syndrome bits will cause the circuit to treat the condition as a single error.



11-5440

Figure 6-9 Delay Line
DL 2 and DL 4

SHEET 8



11-5379

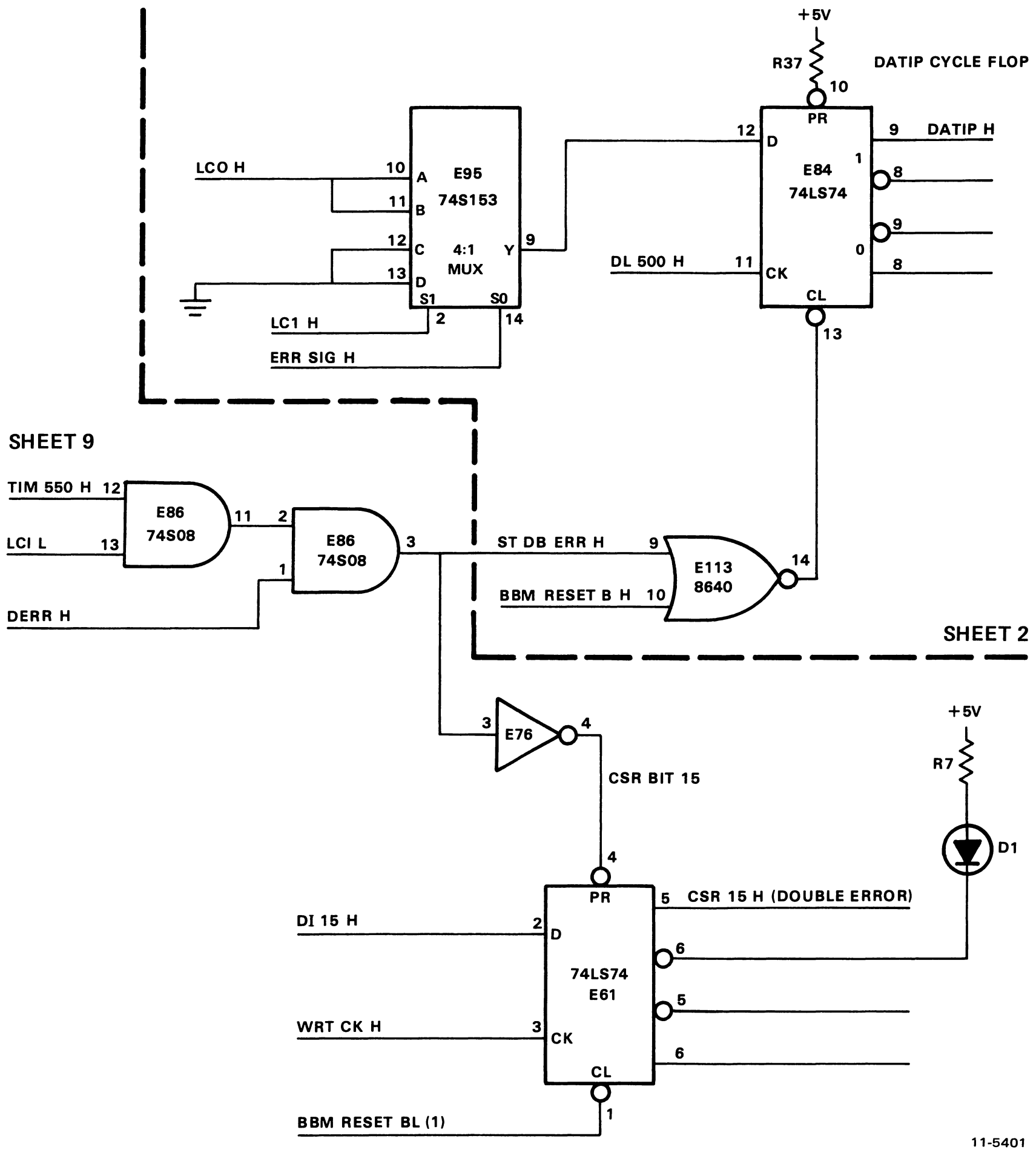
Figure 6-10 Error Detection and CSR Bit 4 Logic

10

10

10





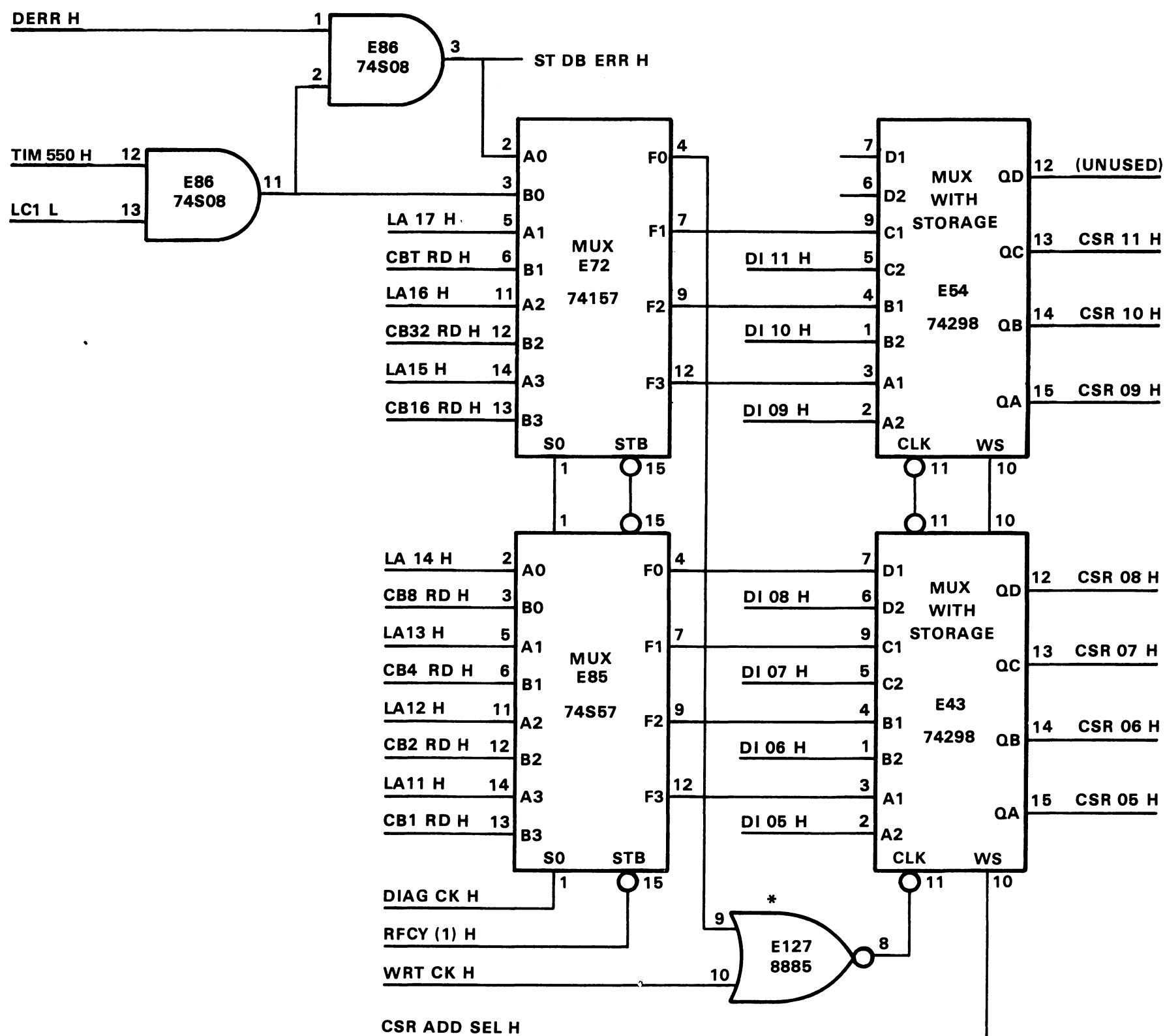
11-5401

Figure 6-12 CSR Bit 15 and Associated Logic

With the data correction signals disabled (all high) by DERR L, the uncorrected data is gated to the Unibus through the two sets of multiplexer circuits described in the previous section.

Since it is important that the approximate location of the erroneous data be retained, latched address bits LA17 H – LA11 H are gated through the multiplexers shown in Figure 6-13 (select input DIAG CK H is low).

SHEET 9



11-5408

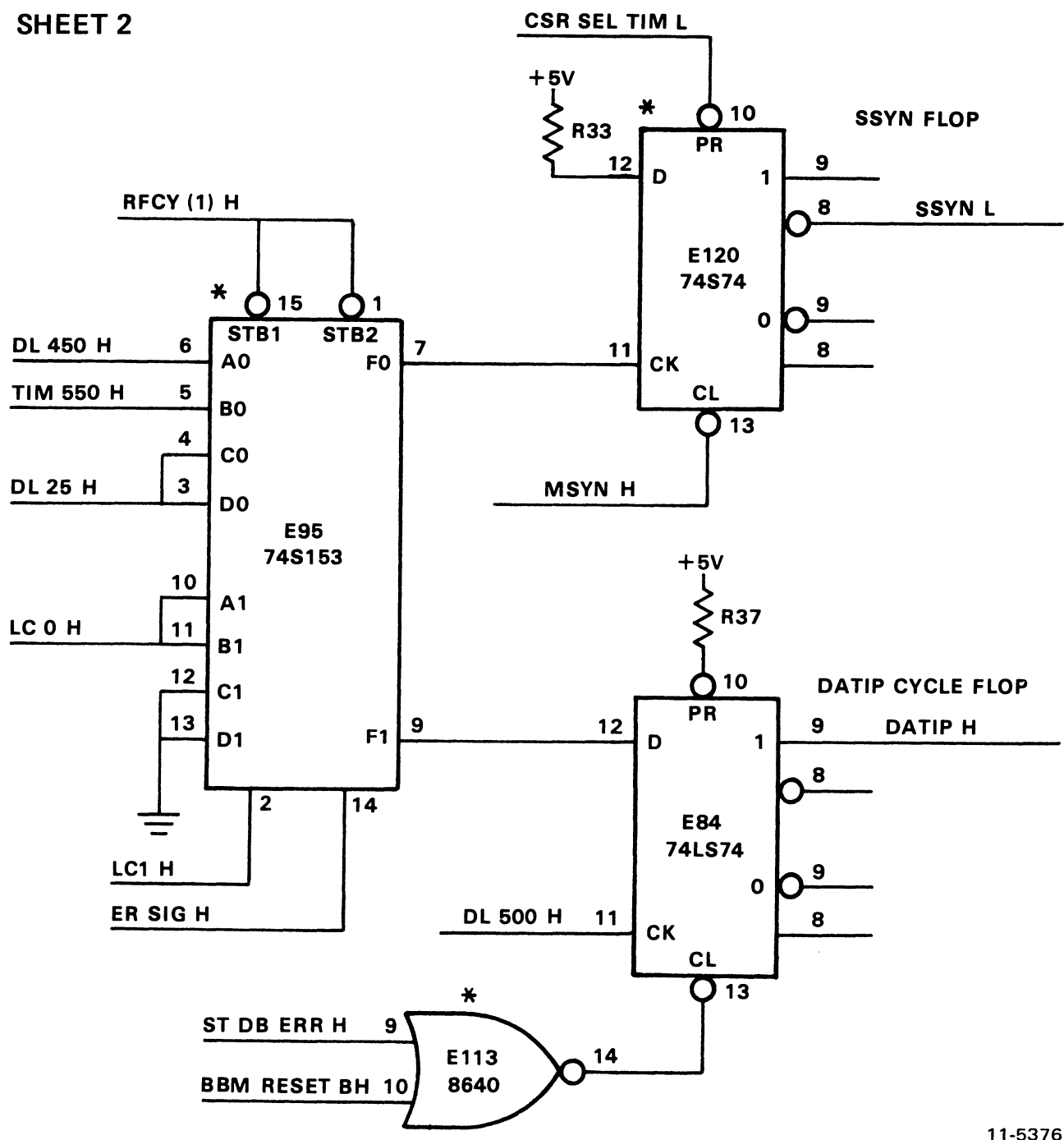
Figure 6-13 CSR Bits 5-11 and Associated Logic

These selected address bits are then latched in the two multiplexers with storage chips (E54 and E43) when the TIM 550 H signal enables the clock input lines to the chips. These upper seven address bits form bits 11–5 of the CSR, defining the 1K block of memory where the double error has occurred.

At the end of the read cycle, whether or not an error has been detected, the MBSY flip-flop will be reset, when RMW 150 L goes high (sheet 3).

If the read cycle just described is a DATI cycle, the resetting of MBSY effectively finishes the operation. However, if the cycle is a DATIP, the next cycle to be performed will be a write operation to the same location. The bytes paired with the addressed byte or word remain stored in the MDR latches so that they do not have to be accessed a second time in order to enable the generation of new check bits when the new double word is formed.

The DATIP Cycle flip-flop allows the MF11S-K control module to remember whether or not the cycle just completed was a DATIP cycle. When Unibus line C0 is high and Unibus line C1 is low, the bus master is requesting a DATIP. This condition causes the D input of the DATIP Cycle flip-flop to go high; and the flip-flop sets when DL 500 H goes high (Figure 6-14). The DATIP Cycle flip-flop will then remain set through the end of the read cycle and into the following write cycle, unless reset because of a power failure, double error condition, or BUS INIT.



11-5376

Figure 6-14 DATIP Cycle Flip-Flop

6.3 WRITE CYCLE (DATO, DATOB) NOT FOLLOWING A DATIP

If a write cycle is initiated and it does not follow a DATIP cycle, the memory must perform an internal read-modify-write cycle to generate new check bits on the double word to be formed. Figure 6-15 shows the timing for a read-modify-write cycle. Therefore, the controller must latch the data to be written, the address of the location to be written into, and the C0 and C1 signals. The memory must send an SSYN signal to indicate to the bus master that the Unibus signals have been received by the memory. Figure 6-16 is a write cycle flowchart.

As on the read cycle, MEM GO L starts the timing chain. MEM GO L also enables DAT IN TIM H (L C1 L is true), clocking the data from the Unibus into the data latches (Figure 6-17). DL 25 H is selected by the multiplexer E95, clocking the SSYN flip-flop (sheet 2). ADD TIM L latches the address bits from the Unibus; and the double word from the appropriate memory location is gated from the selected array module to the MDR via the internal memory bus within the window provided by the first of two sets of clock signals, MDR TIM 0-3 L.

Since, in this case, the previous cycle was not a DATIP, the DATIP Cycle flip-flop is not set and WRITE L remains false. At the beginning of the timing chain (TIM ST L is true), therefore, the syndrome latches are reset.

6.3.1 Generating the Syndrome Bits (DATO/DATOB Not Following DATIP)

The newly generated check bits are compared with the check bits stored with the double word; the resulting syndrome bits, together with the condition of the ER SIG H signal, are latched as in the DATI/DATIP cycle.

6.3.2 Gating Bytes to be Written to the MDR (DATO/DATOB Not Following DATIP)

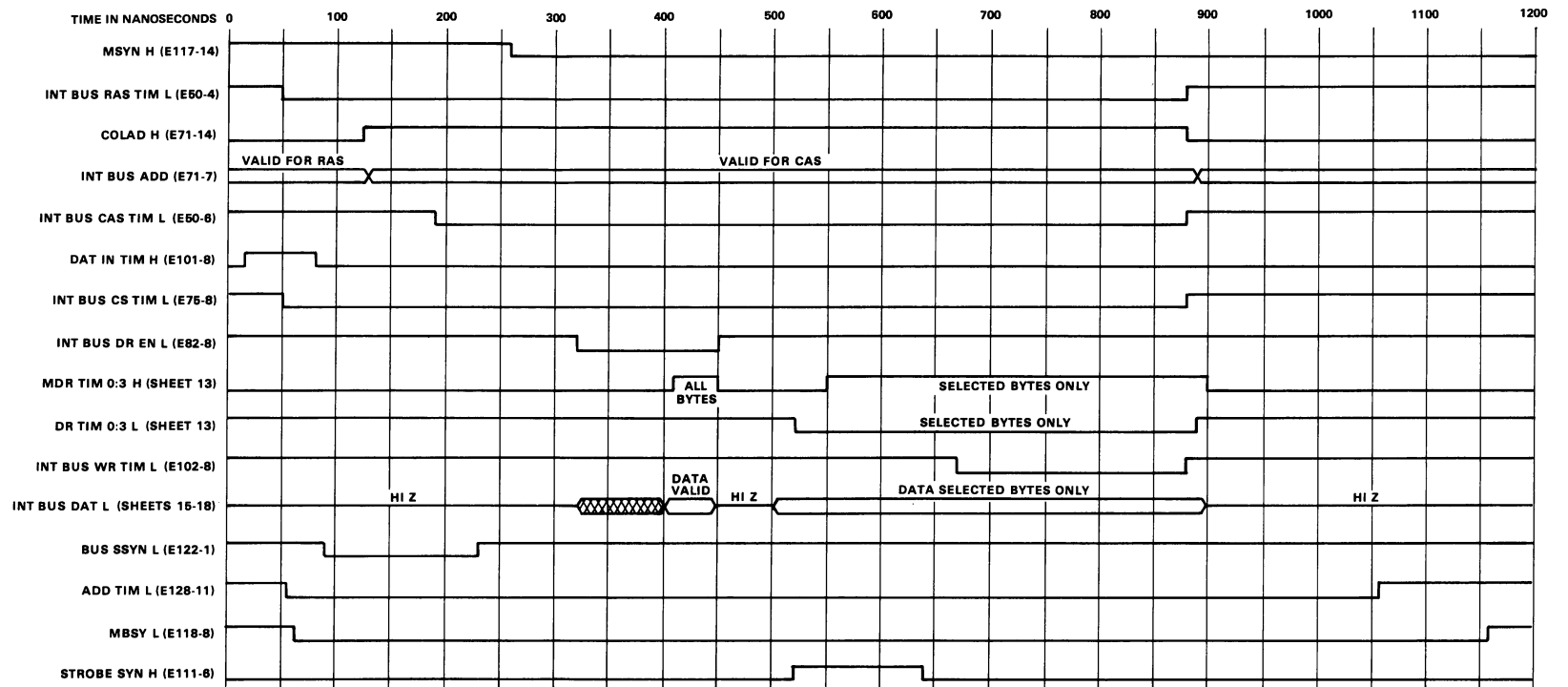
The Internal Read-Modify-Write flip-flop sets with the assertion of DL 300 H, generating TIM RMW H and starting the timing chain for the read-modify-write cycle (Figure 6-18).

With TIM RMW H true, the RMW WR H flip-flop sets when DL 425 clocks it (sheet 13). If no double error has been detected (an even number of latched syndrome bits is not high), one or two of the four signals, DR TIM 0-3 L, are enabled as complements of the write byte signals, and the data to be written is loaded into the appropriate bytes of the MDR as explained in Paragraph 5.3.2.

6.3.3 Manipulation of Syndrome and Check Bits (No Error) (DATO/DATOB Not Following DATIP)

Check bits are generated on the newly formed double word as the 32 data bits in the MDR are fed into the parity generator chips. If none of the latched syndrome bits (referring to the old double word) is high, the new double word and the newly generated check bits are all correct. The bytes to be written and the check bits are thus ready to be gated to the array.

The Exclusive ORing of the new check bits with the latched syndrome bits yields no change in the check bit pattern, since all latched syndrome bits are low. The corrected (in fact they are uncorrected in this case) check bits thus formed are placed on the internal memory bus, since the DR TIM CK L signal will be true. Note that this means that the signals on the internal memory bus check bit lines refer to the old double word when first enabled and to the new double word after the error correction circuitry has generated and processed the new check bits.

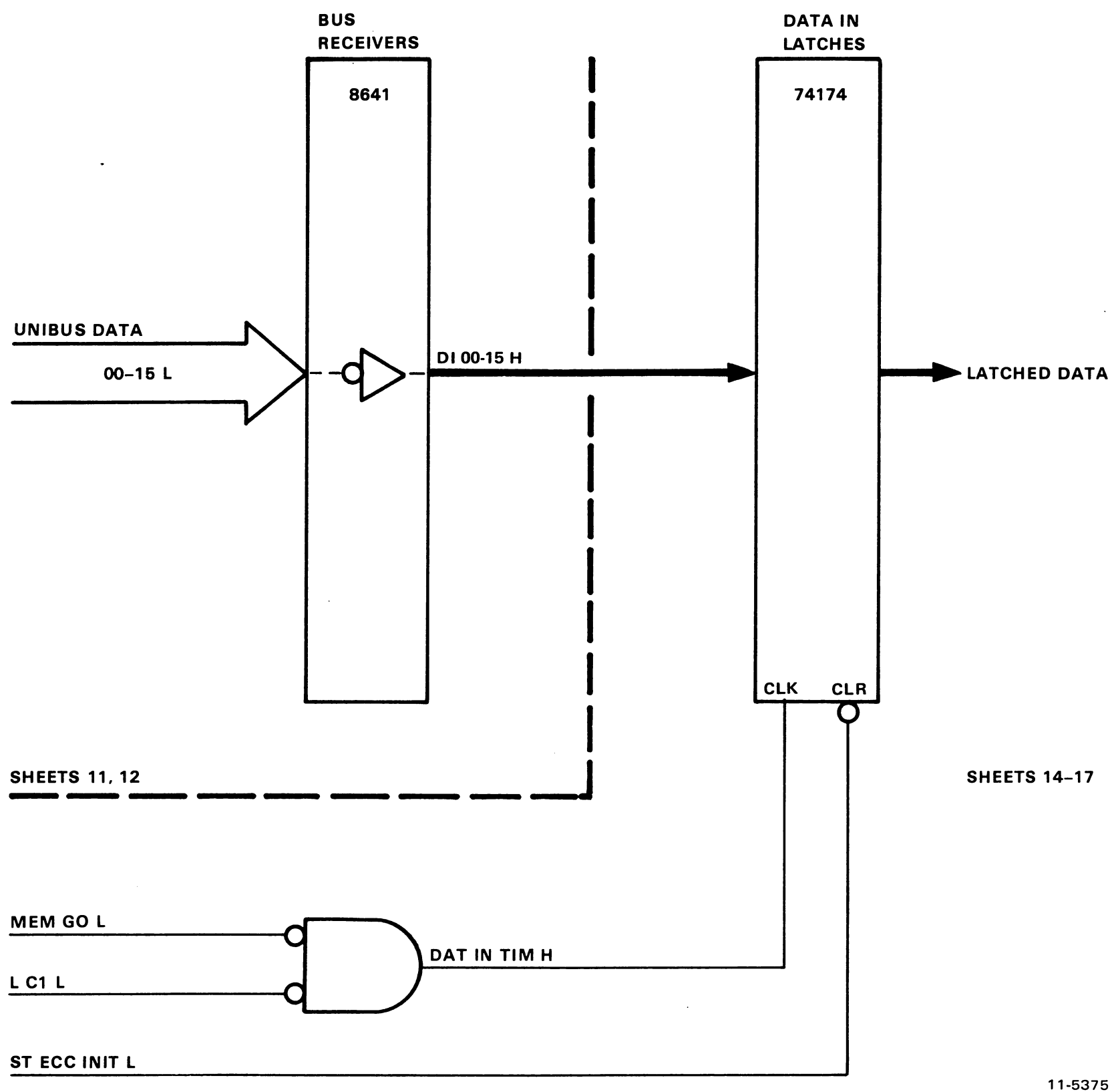


11-5438

Figure 6-15 Read-Modify-Write
Cycle Timing Diagram

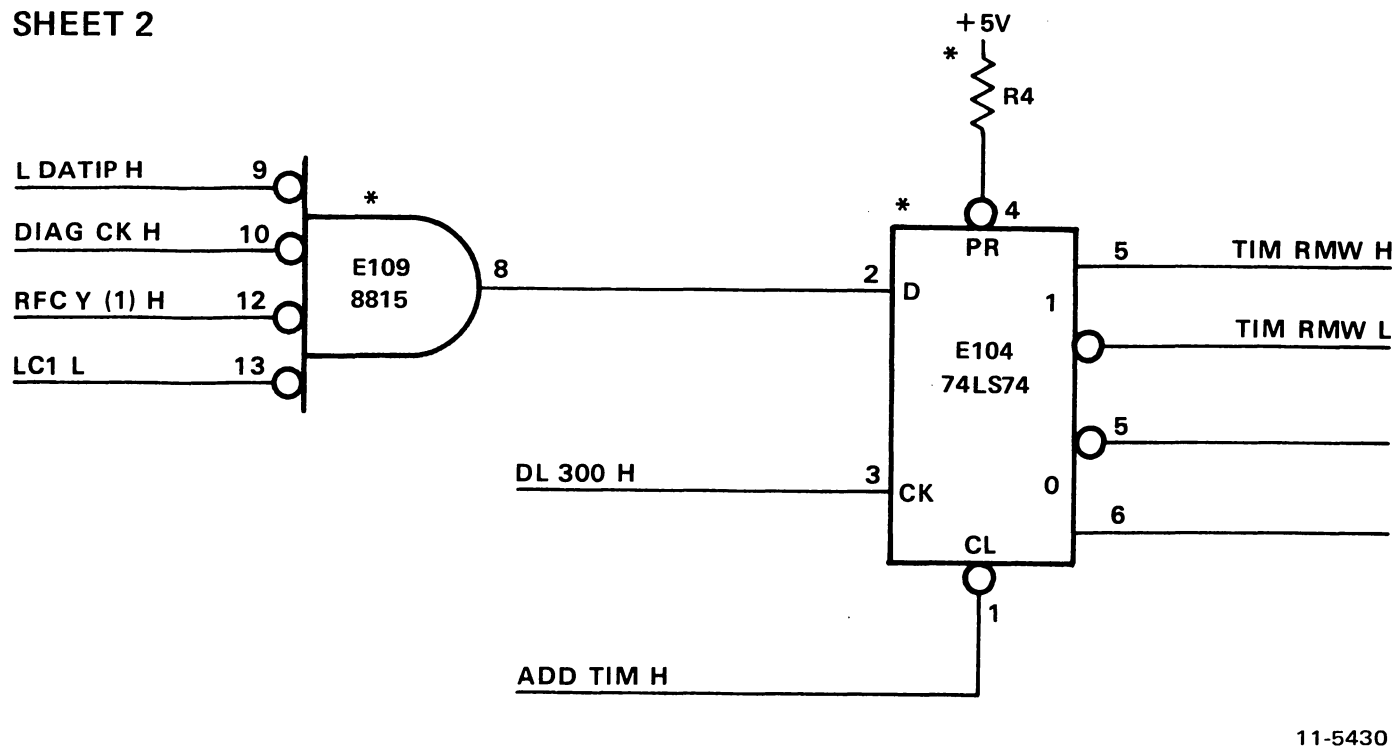


6-27



11-5375

Figure 6-17 Latching Unibus Data on a Write Cycle



11-5430

Figure 6-18 Internal Read-Modify-Write Flip-Flop

6.3.4 Writing the New Data and Check Bits

The address of the location to be written into remains stored in the address latches (sheet 4) and the address of the double-word location on the selected array module is still stored in the row and column address registers of the RAMs. The column address bits, in fact, remain enabled on the internal memory bus. The Internal Read-Modify-Write flip-flop (E104, sheet 2) remains set from the beginning of the cycle, and it causes the TIM 500 flip-flop to set with the assertion of DL 500 H (Figure 6-19). This triggers delay line DL 3. DL 550 L then direct sets the Write Timing flip-flop, which enables the signal INT BUS WR TIM L. Note that RFCY (1) H must be low.

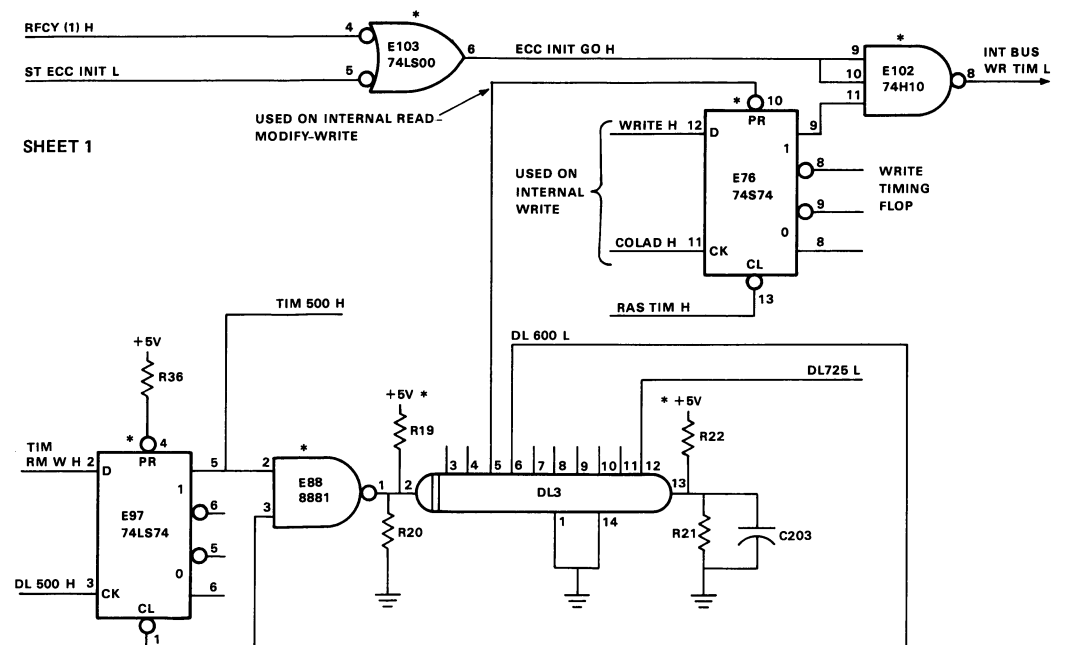
The INT BUS WR TIM L signal provides a window enabling the selected write byte lines on the array module causing the new data and new check bits to be written into the RAMs.

The transfer of data in the write cycle is complete at this point. The memory is not yet ready to begin a new cycle, however, and the timing chain is used to reset the control module. DL 725 L from delay line DL 3 is inverted to clock the flip-flop (E97) shown in Figure 6-20, which, in turn, triggers delay line DL 4 and clears the RAS Timing flip-flop.

Delay line DL 4 produces RMW 150 L and RMW 175 L. When RMW 150 L is enabled, it puts a low level on the MBSY flip-flop clock input. Then RMW 175 L is enabled, disabling ADD TIM H and L. The low level on ADD TIM H clears the Internal Read-Modify-Write flip-flop. The MBSY flip-flop resets next, when RMW 150 L goes high (Figure 6-21).

6.3.5 Manipulation of Syndrome and Check Bits (Single Error) (DATO/DATOB Not Following DATIP)

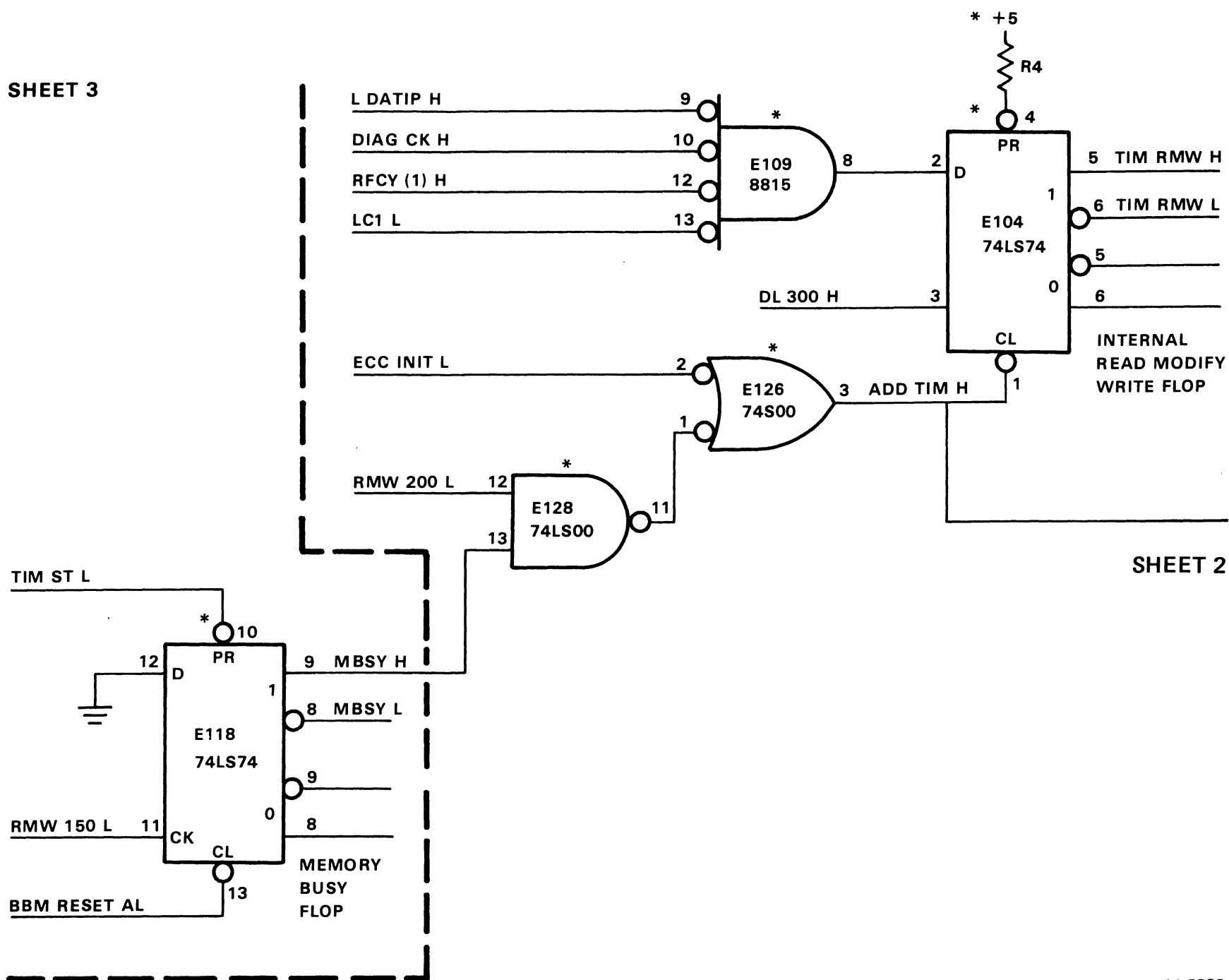
If one of the latched syndrome bits is high, following the generation of check bits on the new double word, the upper three latched syndrome bits, together with the lower two address bits, the cycle description bits (C0, C1), and the latched error bit, are decoded by the PROM.



11-5429

Figure 6-19 Generation of
INT BUS WR TIM L

SHEET 3



SHEET 2

11-5382

Figure 6-21 Clearing the MBSY and Internal Read-Modify-Write Flip-Flops

If the data bit in error (from the old double word read from the array) is in a byte location that is to be written into, ER BTW H is generated, clearing the syndrome latches when TIM 500 H (from flip-flop E97, sheet 1) becomes true. The new data is then ready to be written to the array, together with the check bits. Since reset syndrome bits do not alter the check bits, the check bits are sent to the array unaltered, as in a write cycle where no error is detected (see the previous paragraphs). Notice that the two 3:8 decoders (E68, E67), which handle the lower three syndrome bits, are not used during the write cycle or the read-modify-write cycle.

If, on the other hand, the data bit in error is not in a byte to be written, the syndrome latches are not reset. The latched syndrome bits that point to the bit in error are Exclusive ORed with the new check bits forming the seven corrected check bits. The bad data will then be allowed to stay in the array, but the check bits will be current, still pointing to the bit in error. The byte (or bytes) to be written, together with the corrected check bits, is then gated to the selected memory location as described above. After the single error has been handled, the write cycle is completed with the resetting of the MBSY and Internal Read-Modify-Write flip-flops (Figure 6-21).

6.3.6 Handling a Double Error on a Write Cycle, Not Following DATIP

If an even number of syndrome bits is detected by the error correction circuitry, a double error is indicated. New data will not be written into memory. The double word and check bits placed on the internal memory bus during the read portion of the read-modify-write cycle are written back into the array unaltered. The next DATI or DATIP cycle to that location will cause the double error to be detected, enabling BUS PB L (if CSR bit 0 is set) and setting CSR bit 15.

The DERR L signal inhibits the clearing of the syndrome latches. DERR H enables both the group of four INT BUS WR BYT H signals (Figure 6-22) and the INT BUS DR EN L signal (Figure 6-5).

At this point, while the data and check bit line drivers on the control module remain in the high impedance state, both the drivers and the receivers on the array module are active. This condition causes the 39 bit memory word addressed to be gated through the bus drivers on the array, to the receivers on the array, and back to the memory cells where the word was originally stored, thus preserving the double error. The MBSY and Read-Modify-Write flip-flops are then reset (Figure 6-21), completing the write cycle.

6.4 WRITE CYCLE FOLLOWING A DATIP

If a write cycle is initiated and the previous cycle was a DATIP, the DATIP Cycle flip-flop on the MF11S-K control module will have remained set during the interval between memory cycles. The DATIP Cycle flip-flop, when set, causes the memory to write the Unibus data to the array, without performing a read first. See the DATO/DATOB cycle flowchart, Figure 6-16, and the write cycle timing diagram, Figure 6-23.

As on the cycles previously described, the address of the location to be accessed and the C0, C1 signals are placed on the Unibus by the bus master before the assertion of MSYN. When MSYN is asserted, it enables MEM GO L. This starts the timing chain, setting the MBSY and RAS Timing flip-flops and latching the address that is asserted on the Unibus address lines.

MEM GO L is also ANDed with LC1 L, to generate DAT IN TIM H, which clocks the data to be written from the Unibus data lines into the memory data latches (Figure 6-24).

The row and column address bits are sent to the selected array module at the appropriate times, as on a read cycle, and the WRITE H signal generated at E92 causes the Write Timing flip-flop to set when COLAD H becomes true.

However, before the data to be written can be placed on the internal memory bus, it must be examined by the parity generators so that new check bits can be stored with it. The syndrome bits, together with L ER SIG H, which remain latched from the previous cycle, will still be pointing to a bit in error, if there is any, in the double word stored in the MDR.

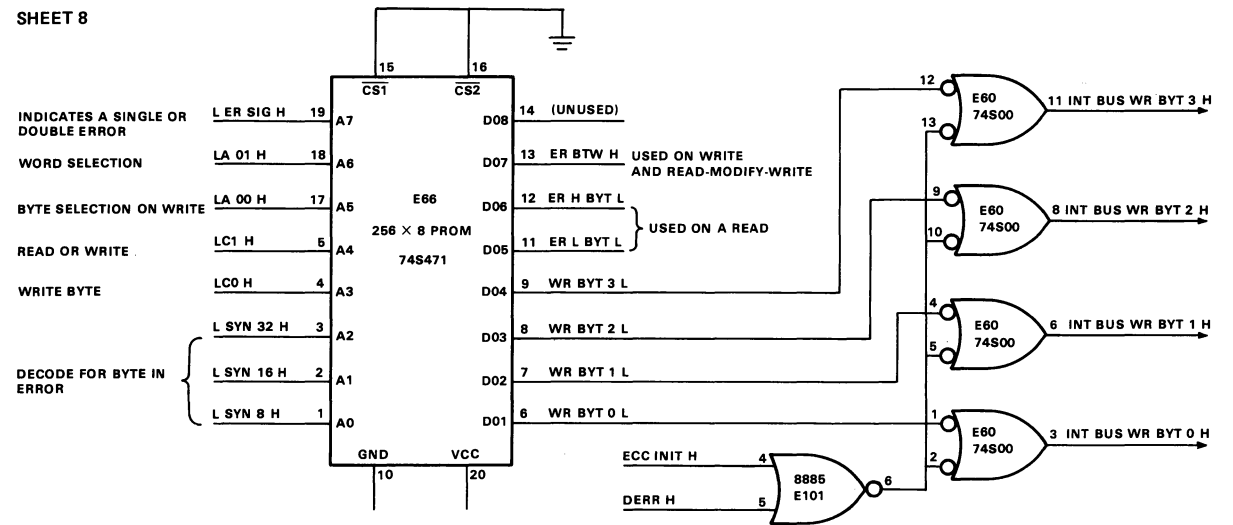
6.4.1 Data Manipulation (Single Error in Byte to be Written) (DATO/DATOB Following DATIP)

If a single error is indicated in the syndrome latches, the PROM determines whether or not the error is located where new data is to be written. If it is, the PROM generates ER BTW H, resetting the syndrome latches, and causing the control module to ignore the error.

The ECC INIT GO H signal will be true (Figure 6-25), as long as a refresh cycle is not in progress, and when WRITE H goes high at the beginning of the cycle it enables the write byte signals generated by the PROM, clocking the data to be written into the MDR.

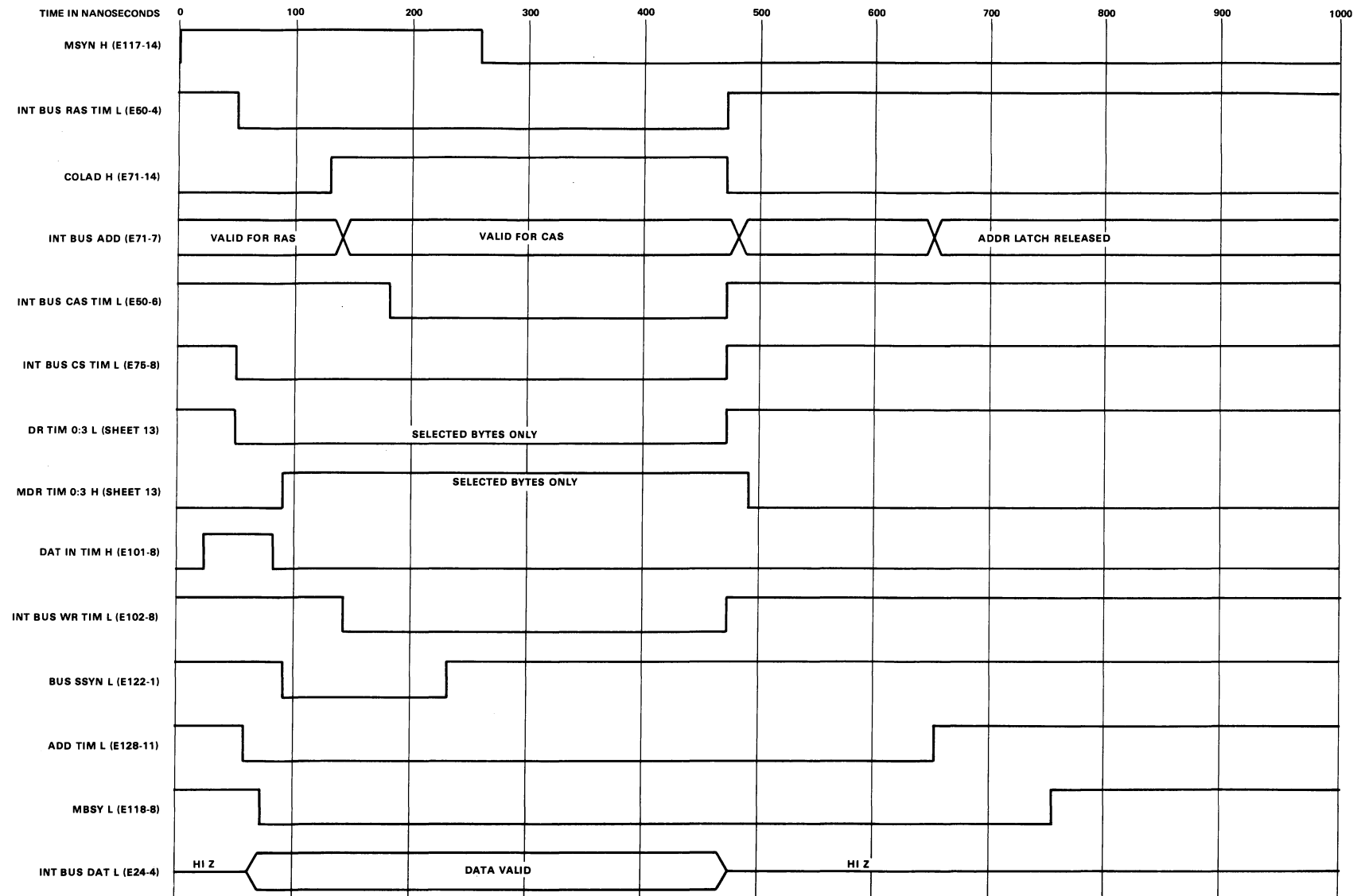
The check bit generation circuit then forms check bits on the new double word in the MDR, and the new data and new check bits are then ready to be gated to the array.

SHEET 8



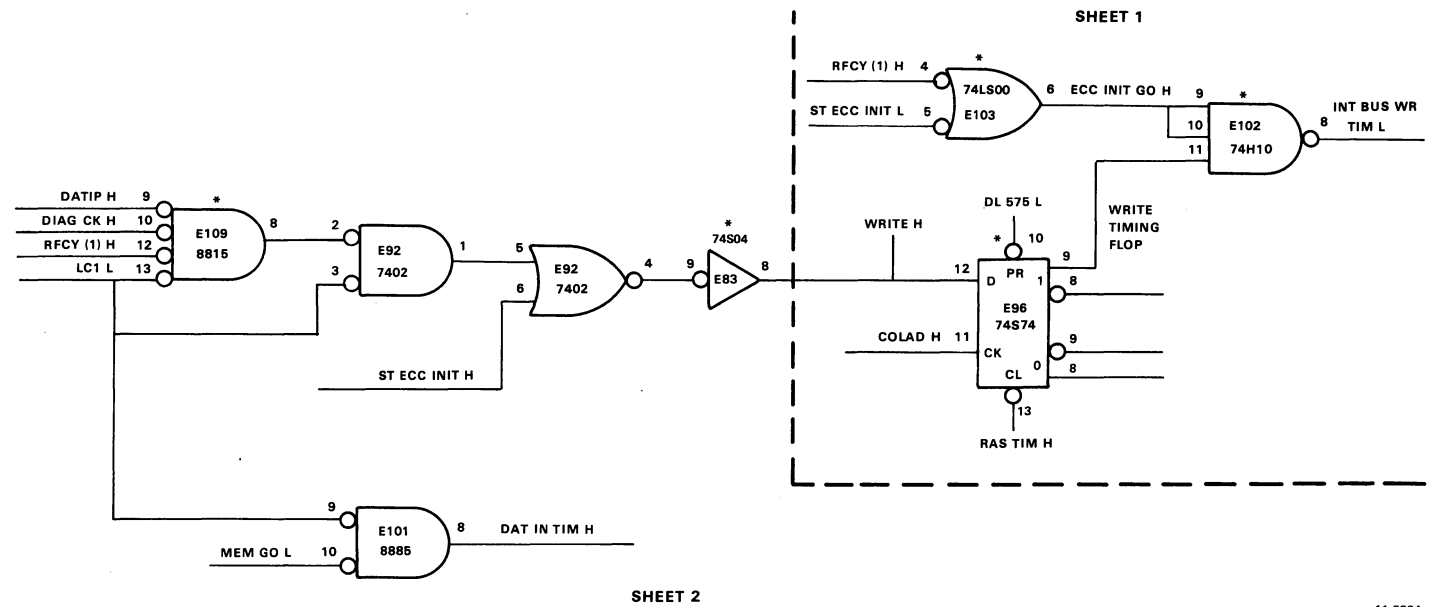
11-5381

Figure 6-22 Generation of Write Byte Signals



11-5383

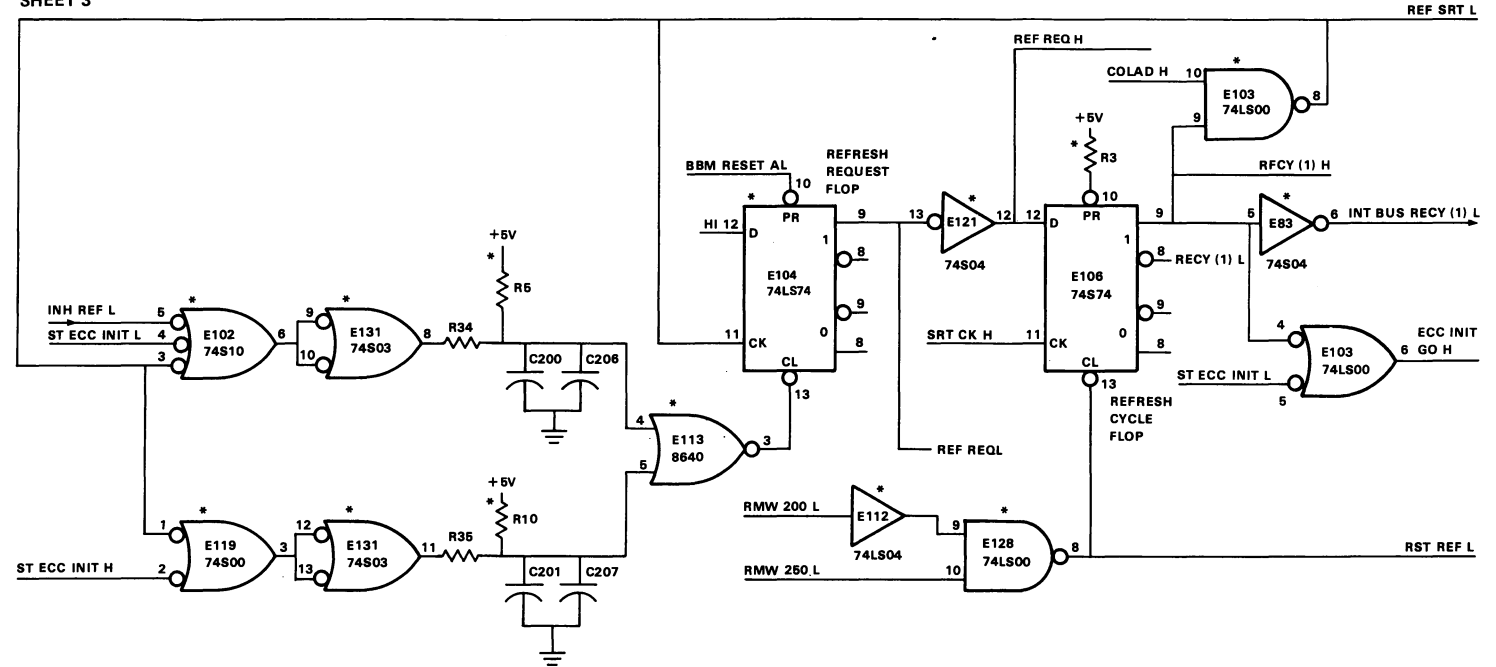
Figure 6-23 Write Cycle Timing
Diagram (Following DATIP)



11-5384

Figure 6-24 Write Timing Logic

SHEET 3



11-5385

Figure 6-25 Refresh Control and Timing Logic

When DL 25 H becomes true, it is selected by multiplexer E95, clocking the SSYN flip-flop, and causing the control module to signal the bus master that it has received the data to be written.

The setting of the Write Timing flip-flop, mentioned previously, enables the write byte signals generated by the PROM and the DR TIM CK L signal, gating the new data and the seven check bits to the array.

6.4.2 Data Manipulation (Single Error not in Byte to be Written) (DATO/DATOB Following DATIP)

If the PROM output ER BTW H is not true, but the L ER SIG H signal is true, then an error exists in a byte that is not to be altered by the write cycle. This means that the syndrome latches will not be reset. The latched syndrome bits thus correct the check bits generated on the new double word; and the corrected check bits, which now point to the old error in the new double word, will be gated to the array.

The timing diagram, Figure 6-23, indicates that the data and check bits are valid on the internal memory bus for about 400 ns. The window provided by INT BUS WR TIM L begins after the data becomes valid, however, thus allowing time for the column address to settle.

6.4.3 Data Manipulation (No Error) (DATO/DATOB Following DATIP)

If no error from the previous DATIP cycle exists when a write cycle is initiated, the outputs of the syndrome latches will be low. The Exclusive ORing of the latched syndrome bits with the check bits generated on the new double word thus produces no changes. The check bits are gated unchanged to the array when INT BUS WR TIM L is enabled.

6.5 MEMORY REFRESH CYCLE

The circuit, shown in Figure 6-25, functions as an oscillator, causing the Refresh Request flip-flop to set and reset every 25 μ s.

At the point where a refresh cycle begins, the input to NOR gate E113 pin 4 goes high, resetting the Refresh Request flip-flop.

6.5.1 Refresh Request

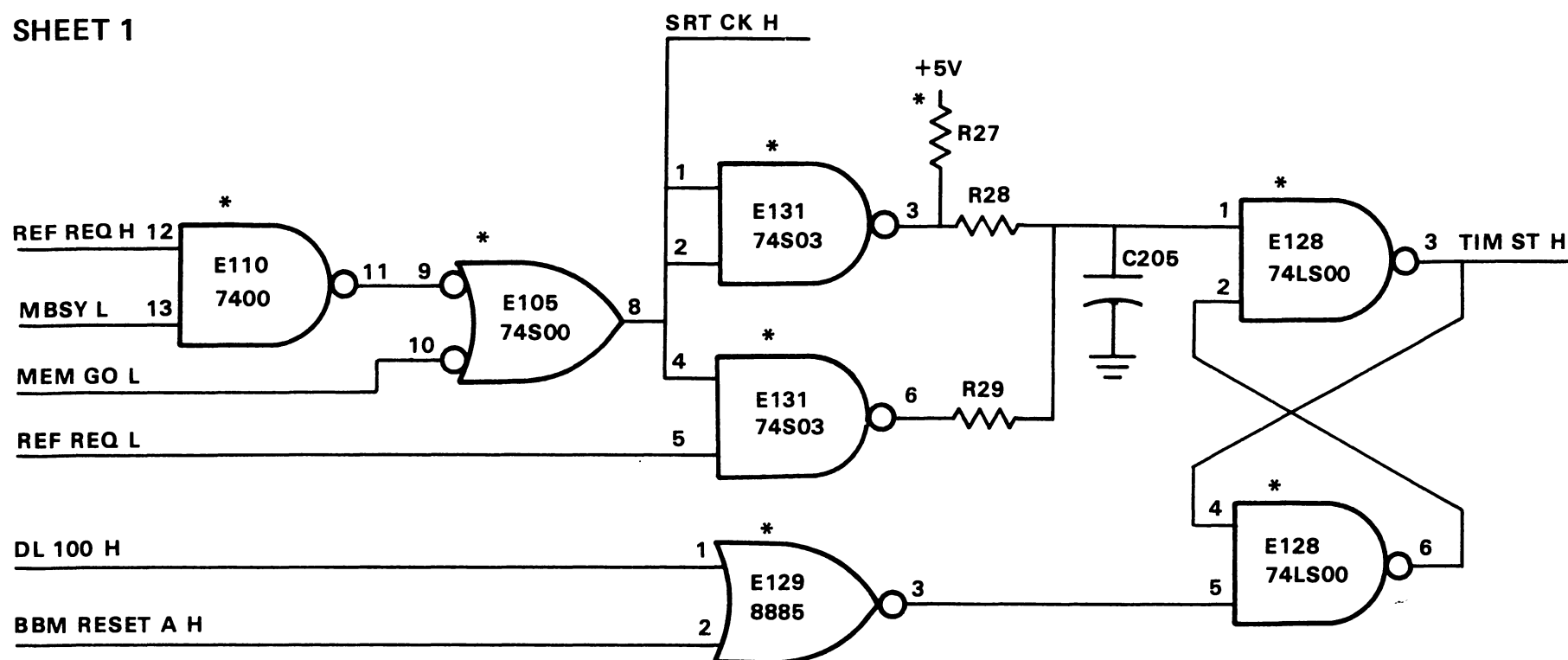
The Q output of the Refresh Request flip-flop is inverted, however, so that the clearing of the flip-flop drives REF REQ H high. REF REQ L is also true, inhibiting the initiation of a data cycle by keeping the NAND gate E131 pin 5 input low (Figure 6-26).

REF REQ H is ANDed with MBSY L generating SRT CK H, if a memory cycle is not already in progress. SRT CK H clocks the Refresh Cycle flip-flop high, initiating the refresh cycle and triggering the timing chain.

Note that the triggering of the timing chain is delayed longer at the beginning of the refresh cycle than it is at the beginning of a data cycle. REF REQ L inhibits the output of the lower NAND gate E131, pin 6. The RC time of the R28 circuit is longer than that of the R29 circuit. The approximate 150 ns difference between the delays allows time for address set up and for the Refresh Cycle flip-flop to settle.

When COLAD H becomes true, it drives REF SRT L low. This signal is then inverted twice (Figure 6-25) causing E131, pins 8 and 11, to go low. The RC network then discharges causing E113, pins 4 and 5, to go low, putting a high level on the clear input to the Refresh Request flip-flop. REF SRT L also puts a low level on the clock input to the Refresh Request flip-flop. Later in the refresh cycle, when COLAD H goes low, REF SRT L will be driven high, clocking the Refresh Request flip-flop high.

SHEET 1



11-5392

Figure 6-26 Memory Cycle Initiation Logic

The outputs of the Refresh Cycle flip-flop are used to disable data cycle circuits and enable refresh circuits as follows:

RFCY (1) H

1. Disables the 4:1 multiplexer, E95 (sheet 2), inhibiting the setting of the SSYN flip-flop.
2. Disables ECC INIT GO H, inhibiting INT BUS WR TIM L (sheet 1) causing the row, column, and refresh address multiplexer to select the outputs of the refresh address counter.
3. Disables ECC INIT GO L (sheet 1).
4. Disables WRITE L and WRITE H (sheet 2).
5. Inhibits the setting of the Internal Read-Modify-Write flip-flop (sheet 2) so that the fastest cycle is used.
6. Inhibits the clearing of the syndrome latches (sheet 7) to preserve error information for next cycle, as in a DATIP/DATO sequence.
7. Inhibits the outputs of the CSR MUX chips, E72 and E85 (sheet 9), so that nothing can be clocked into the CSR during a refresh.
8. Inhibits the DERR H signal (sheet 8) inhibiting the resetting of the DATIP flip-flop and the setting of CSR bit 15.

RFCY (1) L

1. Inhibits INT BUS DR EN L (sheet 2) to ensure that no data is put on the internal memory bus.
2. Inhibits the clock input to the syndrome latches (sheet 7) to preserve error information for the next cycle.
3. Disables the MDR TIM CK H and MDR TIM 0–3 H signals (sheet 13) to preserve data in the MDR.

Figure 6-27 is a flowchart describing the refresh cycle algorithm. Figure 6-28 shows refresh cycle timing.

With the timing chain initiated and the above circuits disabled, the refresh circuitry functions in a straightforward manner.

6.5.2 Refresh Cycle Addressing

The refresh address counter (Figure 6-29) consists of two 4-bit presettable counter chips that are wired to form a 6-bit counter during refresh cycles (Figure 6-28). Bit 0 of E123 (pin 5) is not used during the refresh cycle and bit 3 of E123 (pin 12) is not used at all. The refresh address counter is set at some 6 bit binary number (0–63, base 10) before the cycle starts. Note that it will be set at zero for the first refresh cycle after ECC initialization.

The outputs of the refresh address counter are selected by the row, column, and refresh address multiplexer at the beginning of the refresh cycle, since ECC INIT GO L is high and COLAD H is low (Table 5-2).

The contents of the refresh address counter are thus gated to the internal memory bus address lines where they are clocked into the row address register on each chip on each array with the enabling of INT BUS RAS TIM L. Note that INT BUS RFCY (1) L enables the memory select circuit on all array modules in the MF11S-K memory. Note also that the chip select line, INT BUS CS TIM L, is inhibited during the refresh cycle so that no data can be transferred to or from the individual RAM chips on the array modules.

The signal DL 75 enables COLAD H (Figure 6-30) causing the row, column, and refresh address multiplexer to select the C3 inputs, which are tied to ground. When the CAS Timing flip-flop sets, generating INT BUS CAS TIM L, therefore, the zeros gated through the multiplexer are clocked into the column address registers on the RAM chips.

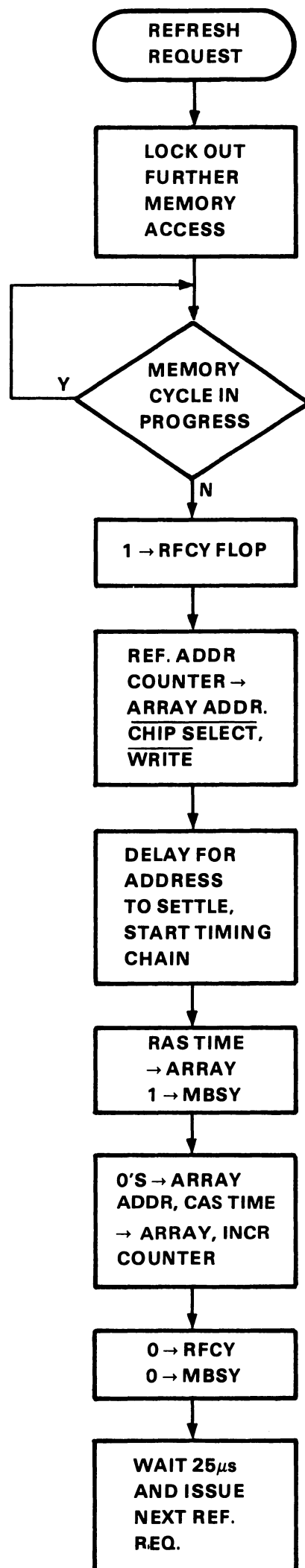
6.5.3 Refreshing the Cells

When the row and column addresses have been latched in the registers, the 64 cells in each row on each chip are refreshed. See Chapter 3 for details.

6.5.4 Ending the Refresh Cycle

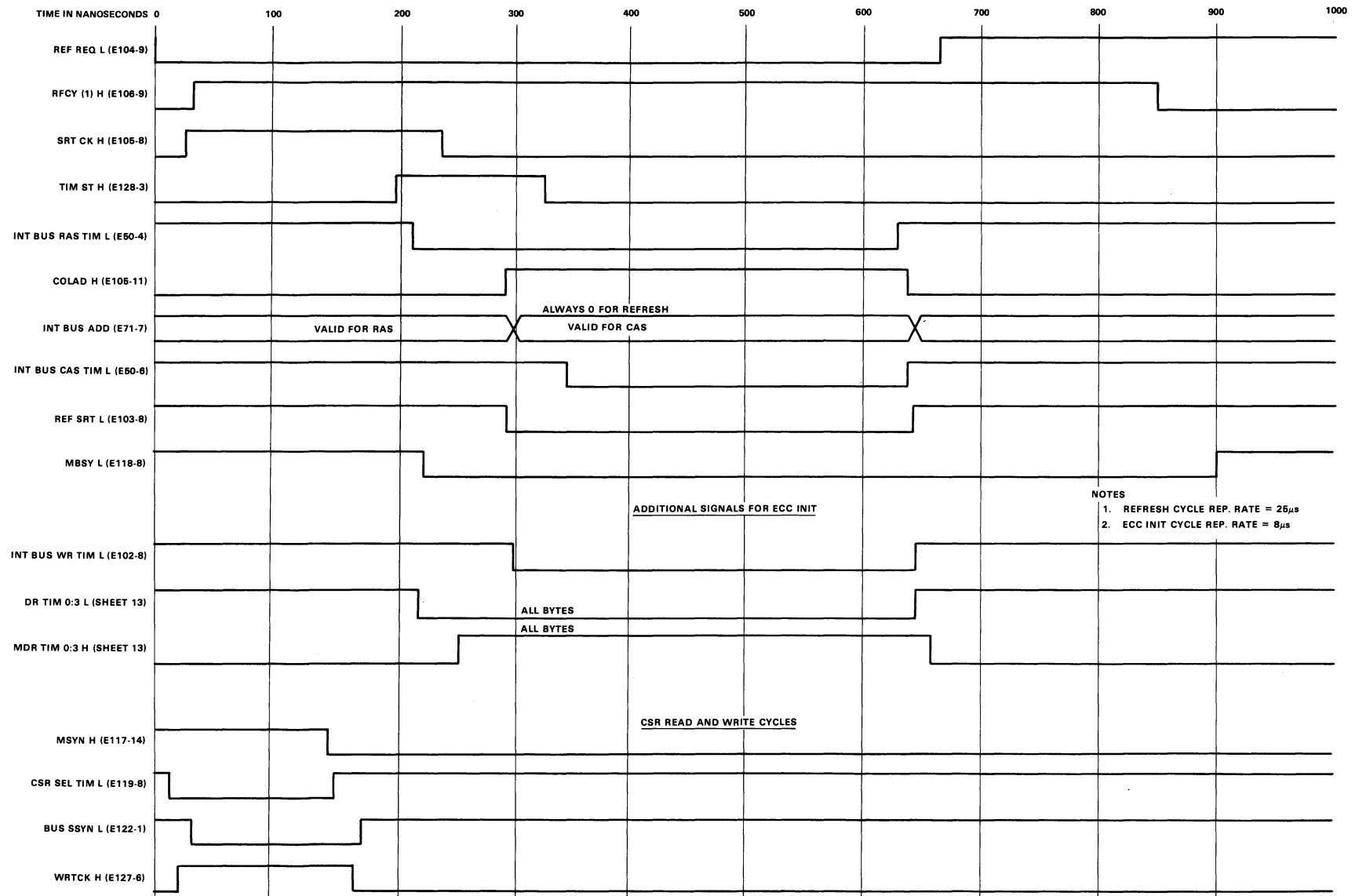
When END RAS TIM L (the input to delay line DL 4, sheet 1) goes true, it resets the RAS Timing flip-flop. RAS TIM H then goes low resetting the CAS Timing flip-flop at REF REQ plus 610 ns. This drives COLAD H low which, in turn, drives REF SRT L high. When REF SRT L goes high, it clocks the refresh address counter incrementing the address so that it points to the next row to be refreshed.

REF SRT L also causes the output of the negative input OR gate, E131, pin 8, to go high, beginning the RC network charging cycle. E113, pin 4, will reach the positive threshold 25 μ s later, initiating a new refresh cycle.



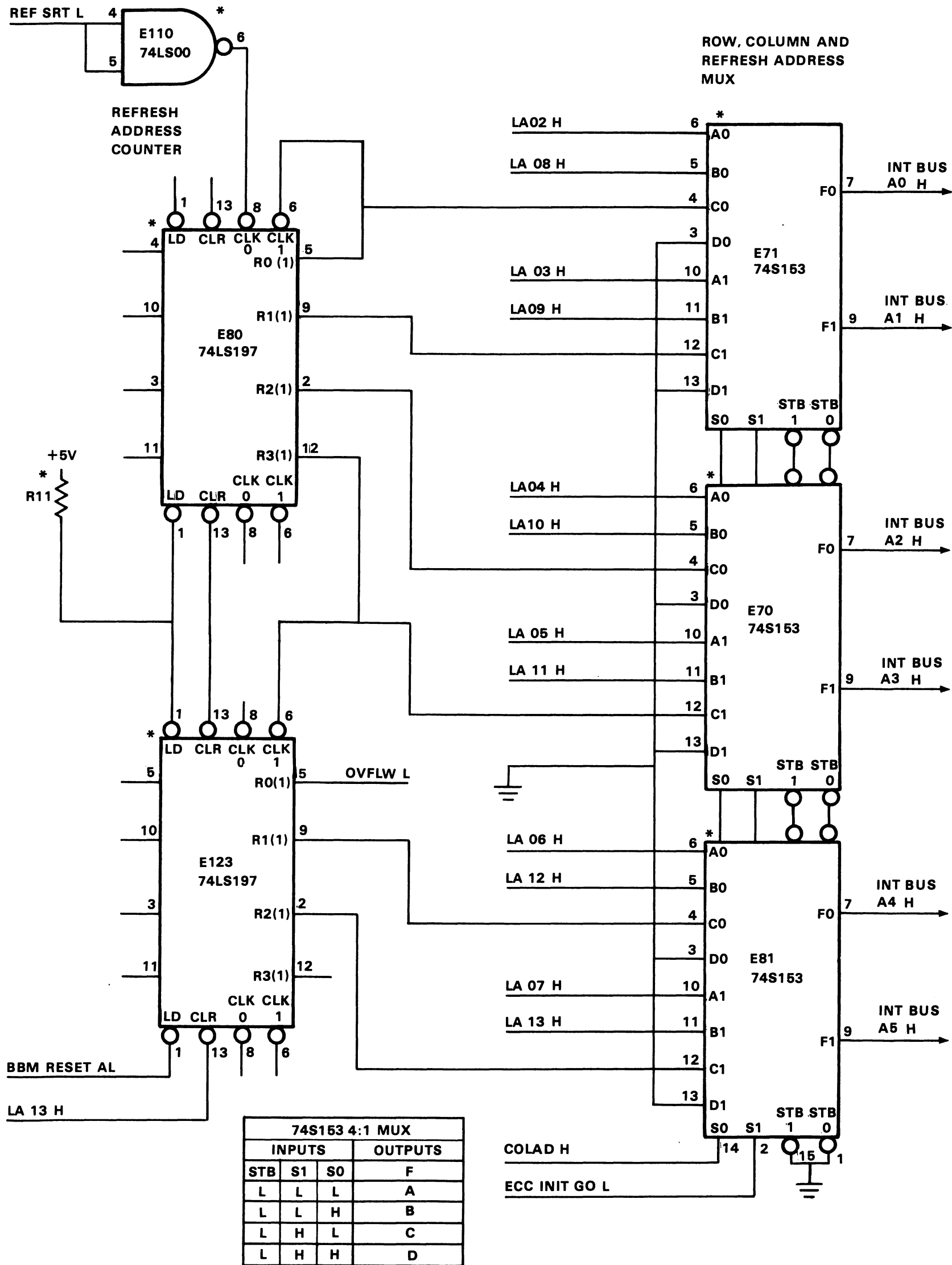
11-5390

Figure 6-27 Refresh Cycle Flowchart



11-5389

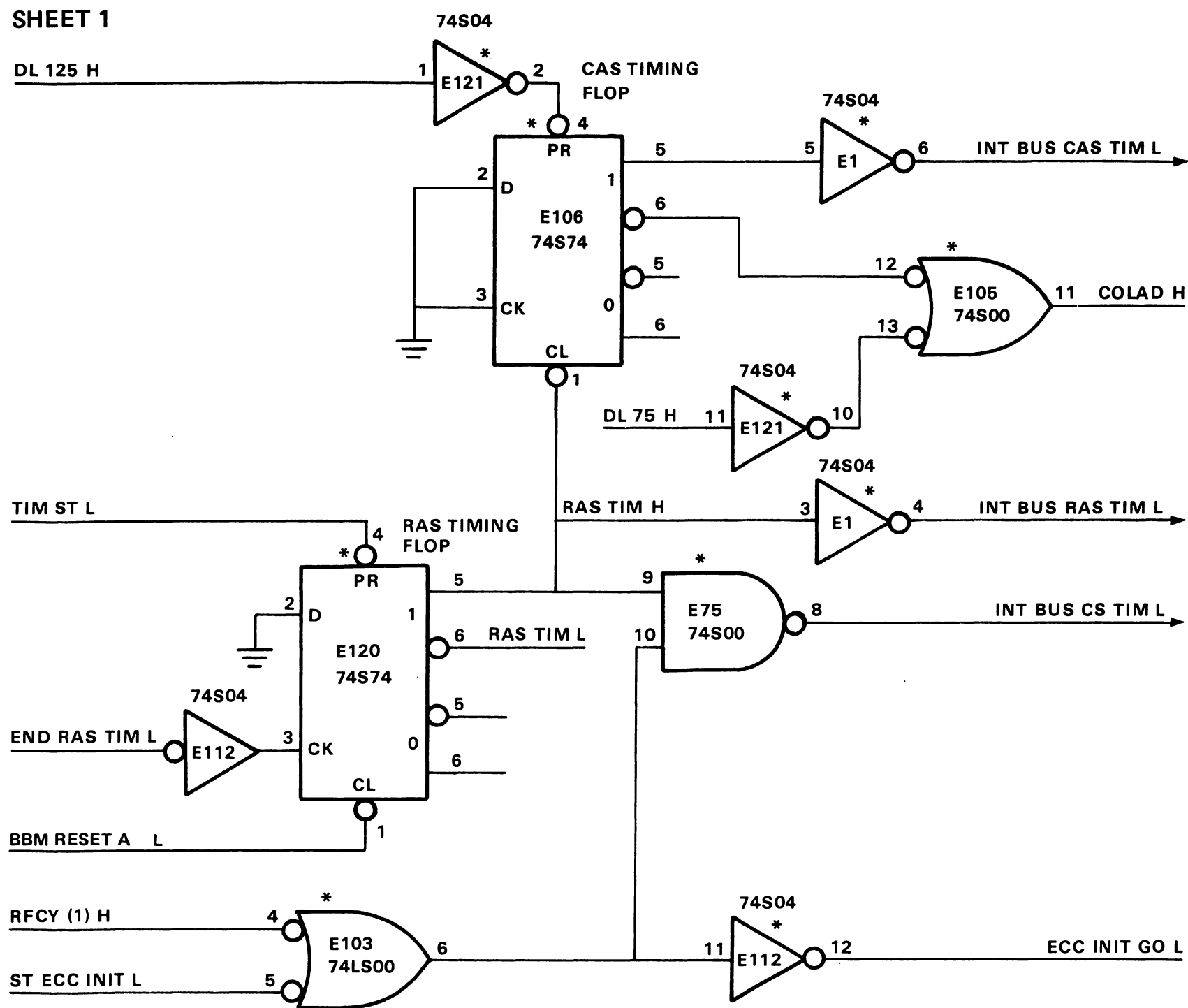
Figure 6-28 Refresh and ECC INIT Cycles, Timing Diagram



11-5393

Figure 6-29 Refresh Address Counter

SHEET 1



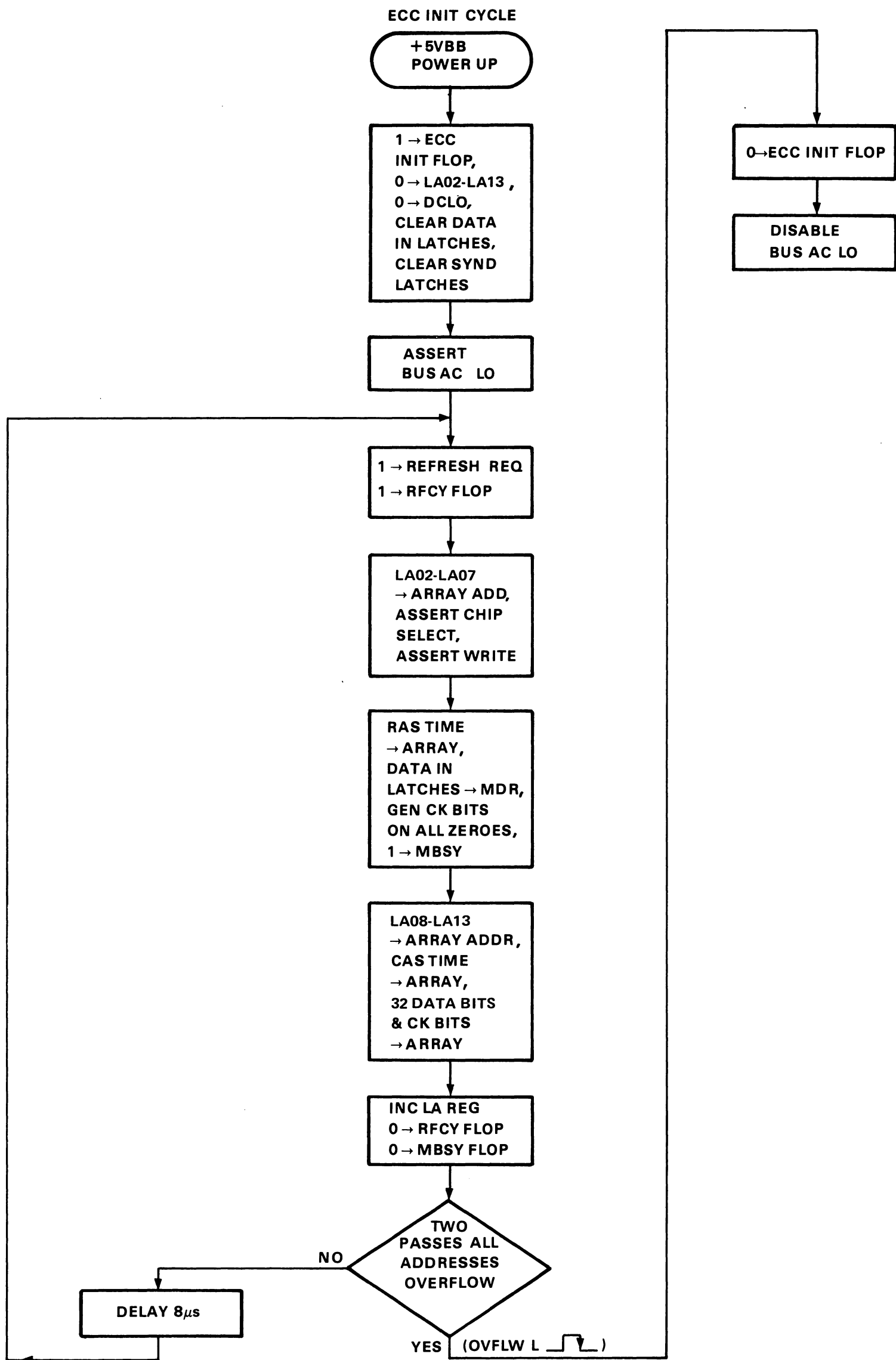
11-5397

Figure 6-30 RAS and CAS Timing Flip-Flops

After the refresh address counter is incremented, RMW 150 L from DL 4 goes low (note that RMW 125 L is fed back to NAND gate E88 forming the terminal edge of the delay line pulses). RMW 150 L puts a low level on the MBSY flip-flop clock input. When RMW 200 L is enabled 50 ns later, it is inverted and ANDed with the RMW 250 L false signal, enabling RST REF L. This resets the Refresh Cycle flip-flop. Then when RMW 150 L goes high, it clocks the MBSY flip-flop low, ending the refresh cycle.

6.6 ECC INITIALIZATION CYCLE

The ECC initialization function of the MF11S-K memory makes use of the refresh circuitry, so that little additional logic is required. The ECC initialization routine ensures that zero data and appropriate check bits are written into all memory locations, if a power up occurs when no backup battery is in use. Figure 6-31 is a flowchart showing the ECC initialization algorithm, while Figure 6-28 shows the timing.



11-5396

Figure 6-31 ECC INIT Cycle Flowchart

6.6.1 Triggering the ECC Initialization Cycle

The battery voltage detector circuit shown in Figure 6-33 will hold a low level on the negative input AND gate E113, pin 11, if no backup battery is present, or if the battery has been drained to the point where memory data has been lost on a power up. If the battery backup power goes awry, the CPU is informed that the memory data may not be valid.

If the +12 V level from the power supply drops below +10 V and AC LO L goes low, then the power supply generates BOOT ENABLE LOW. When AC LO L goes high as power is restored, the CPU will initiate a boot if the Boot Enable signal is low (on a PDP-11/60 system the key lock must also be enabled). Note that the ECC initialization routine will hold AC LO L low for 70 ms, and thus the system will not boot until after the completion of the ECC initialization. If the Boot Enable signal is high when AC LO L goes high, it indicates that the data in memory should still be valid, and the boot will not be initiated.

When the voltage on E113, pin 11, goes below the input threshold, the output of the gate is enabled, setting the BBM Reset flip-flop. On a power up, the RC network of C208 and R32 delays the voltage rise on pin 11 until the power to the chip is enabled. Figure 6-32 shows the relation of the battery back up voltage regulator voltage to the output of E113, pin 13.

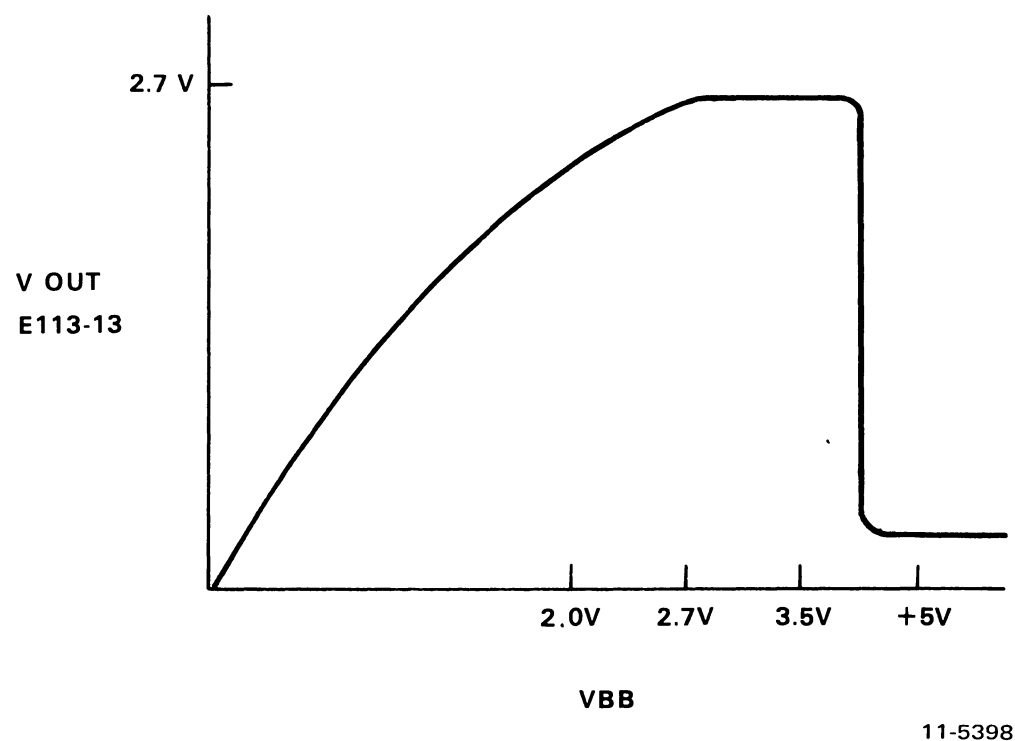
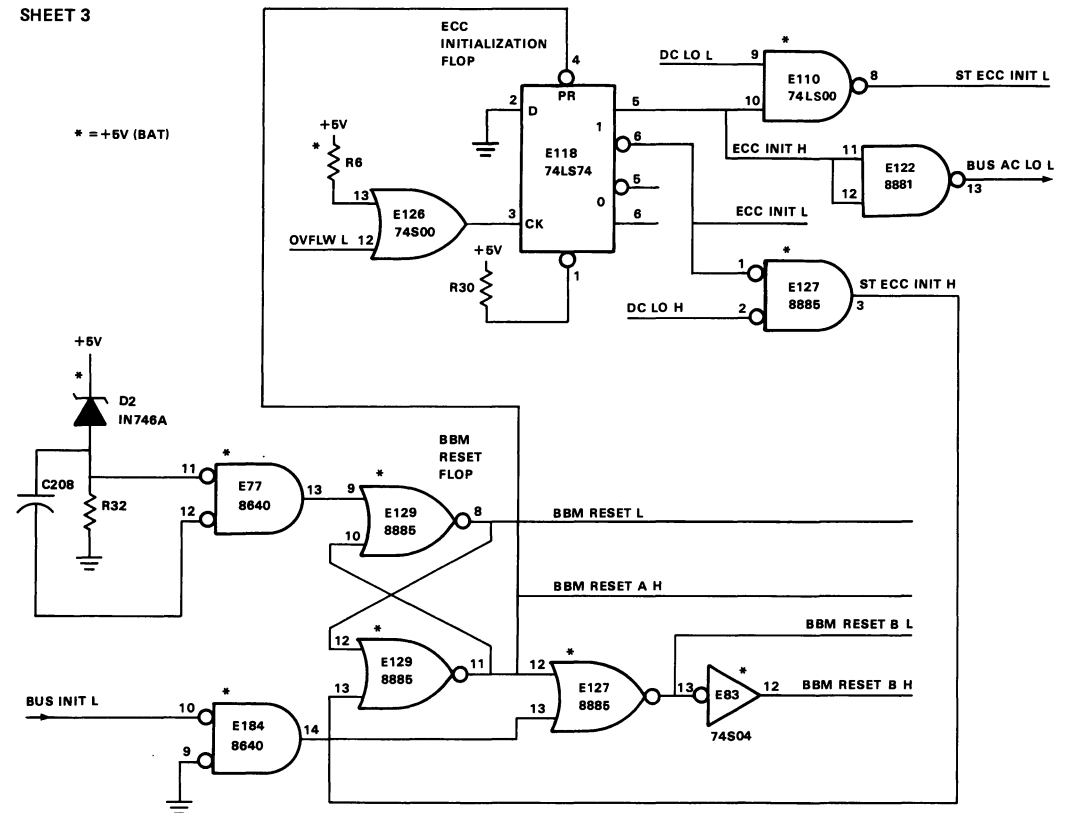


Figure 6-32 Battery Back-Up Voltage Detection Vout vs +5 VBB on Power Up

When E113, pin 13, goes high, it sets the BBM Reset flip-flop. This, in turn, direct sets the ECC INIT flip-flop. When DC LO L goes high it enables ST ECC INIT L, initiating the ECC initialization algorithm. The signals thus generated function as follows.

BBM RESET BL (1) clears CSR bits 0-4, 13, and 15 to put the CSR in a known condition (sheet 9). Notice that the BUS INIT L signal will accomplish this as well as the battery voltage detection circuit (sheet 2).

SHEET 3



11-5394

Figure 6-33 Battery Voltage Detection and ECC INIT Flip-Flop

BBM RESET A L clears the RAS Timing flip-flop (sheet 1), the MBSY flip-flop (sheet 3), the Refresh Request flip-flop (sheet 4), address latches LA13–LA02, and the refresh address counter (sheet 5). Note that it is necessary to reset the refresh address counter to synchronize it with the ECC initialization counter. During the ECC initialization routine, the memory cells in each row are addressed often enough so that they do not need to be refreshed. However, when the ECC initialization routine finishes, the refresh cycle must start at a row where the ECC initialization routine left off, in order to ensure that the all zeros data generated remains valid.

BBM RESET A H resets the TIM ST latch (sheet 1), ensuring that the latch is in a known condition.

BBM RESET B H clears the DATIP Cycle flip-flop (sheet 2).

ST ECC INIT L inhibits the 25 μ s refresh repetition RC network (sheet 3), enables ECC INIT GO H and ECC INIT GO L (sheet 1), and clears the data latches (sheets 14–17).

ST ECC INIT H enables WRITE L and WRITE H (sheet 2), feeds a high level to the 8 μ s RC network which controls E113, pin 5, resetting the Refresh Request flip-flop after a delay. It also resets the BBM Reset flip-flop, forcing E129, pin 11, low, and, ANDed with TIM ST H, clears the syndrome latches (sheet 7).

ECC INIT H is ANDed with REF SRT L high, clocking the address counter (LA13–LA02, sheet 4) and it is inverted to hold BUS AC LO L true for the duration of the ECC INIT routine (sheet 2).

ECC INIT L enables ADD TIM H (sheet 2).

6.6.2 ECC Initialization Addressing

When ST ECC INIT H causes the Refresh Request flip-flop to be cleared, REF REQ H and REF REQ L are enabled. REF REQ H is ANDed with MBSY L, high, forming SRT CK H. This signal causes the slower of the two RC networks (which feed the TIM ST latch) to discharge, setting the TIM ST latch (sheet 1) and triggering the timing chain. SRT CK H also clocks the Refresh Cycle flip-flop high before the triggering of the timing chain. ECC INIT GO L causes address counter bits LA02–LA07 to be selected initially. These bits are then clocked into the row address register on each chip on all array modules when the setting of the RAS Timing flip-flop enables INT BUS RAS TIM L.

ST ECC INIT L enables the INT BUS CS TIM L signal (sheet 1) when the RAS Timing flip-flop sets, enabling the chip select lines on all arrays. When COLAD H goes high, address counter bits LA08–LA13 are selected. INT BUS CAS TIM L clocks in the column address bits on the RAM column address registers.

6.6.3 Data and Check Bits

At the beginning of the ECC initialization cycle, ST ECC INIT L clears the 16 data latches shown on sheets 14–17. It is important to notice that initialization is performed on all array modules simultaneously. The latch outputs are enabled when WRITE H and ECC INIT GO H enable the DR TIM 0–3 L signals (sheet 13). The MDR TIM 0–3 H signals go high after the delay caused by the RC networks, clocking the zeros from the 16 data latches into the 32 MDR latches. The check bit generation circuit forms check bits describing the zero data pattern. These newly generated check bits are Exclusive ORed with the latched syndrome bits (all clear), forming the COR CK bits. DR TIM CK L (sheet 13) is low, gating the COR CK bits onto the internal memory bus.

ECC INIT H enables the four INT BUS WR BYT 0–3 H signals (sheet 8), so that the zero pattern can be written into all four bytes of the memory word. INT BUS REF CYC (1) L causes the four RAS SEL lines on the array modules to be enabled.

When COLAD H clocks the Write Timing flip-flop (sheet 1), INT BUS WR TIM L clocks the data into the first bit location of every RAM chip in the MF11S-K memory.

6.6.4 Ending the ECC Initialization Algorithm

As the first cycle ends, END RAS TIM L triggers DL 4 and resets the RAS Timing flip-flop. RAS TIM H then goes low, resetting the CAS Timing flip-flop and the Write Timing flip-flop, and causing COLAD H to go low. INT BUS WR TIM L is thus disabled, ending the access to the RAM chips.

COLAD H low, in turn, forces REF SRT L high. This causes the R35 RC network to begin charging ($8\ \mu\text{s}$ RC time). Note that the R34 RC network is inhibited because ST ECC INIT L holds it low. REF SRT L high also sets the Refresh Request flip-flop and clocks the address counter (LA02-LA13). When RMW 150 L goes true it prepares the resetting of the MBSY flip-flop. RMW 200 L enables RST REF L, resetting the Refresh Cycle flip-flop. RMW 150 L then goes high, clocking the MBSY flip-flop low.

When the R35 RC network charges to the high threshold of the E113 NOR gate input, the Refresh Request flip-flop is reset, initiating another stage of the ECC initialization routine. At the end of 4096 such stages, the entire memory will have been loaded with zeros and the appropriate check bit patterns.

When the ECC initialization cycle starts, BBM RESET A L clears the 4-bit counter E123 (sheet 5), which forms the upper bits of the refresh address counter. BBM RESET AL then goes high shortly after power up, enabling the counter. At the end of 4096 memory cycles, when the 12-bit address counter is reset to zero, LA13 H goes low clocking E123 once, causing OVFLW L to go high. After the second set of 4096 memory cycles, when LA13 H goes low again, the counter on E123 increments, causing OVFLW L to go low. The negative input OR gate E126, pin 11, then goes high, clocking the ECC INIT flip-flop (E118, sheet 3) low, and ending the ECC INIT cycle. When ECC INIT L and H are disabled, the refresh RC network (R34) is enabled, and the memory functions normally, responding to control signals initiated by a bus master. The entire ECC initialization process requires less than 70 ms. Note that during ECC INIT the memory asserts BUS AC LO.

6.7 MEMORY CYCLE CONFLICTS

A memory cycle cannot be initiated if one is already in progress. MSYN H will have no effect on the MF11S-K memory if MBSY L is low, disabling the 13 input NAND gate, E117 (sheet 1).

If a memory data cycle is in progress and the refresh RC network times out, initiating a refresh request, the refresh circuit will remain disabled until the end of the memory data cycle. The RC network, when charged, will reset the Refresh Request flip-flop, generating REF REQ L and H during a memory data cycle, but MBSY L will again be true, disabling NAND gate E110 at pin 13 (sheet 1). Then, when MBSY L is disabled at the end of the memory data cycle, the presence of REF REQ H will cause E110, pin 11, to go low, initiating a refresh cycle.

6.8 BATTERY SUPPORT MODE OPERATION

When power is shut down on a PDP-11 system that includes an MF11S-K memory with a battery backed up regulator, the regulator supplies the +5 V necessary to operate the refresh circuitry both on the control module and the array modules. It also supplies the $\pm 12\text{ V}$ for the MOS arrays. Integrated circuits that will function in this mode are identified with an asterisk on the schematic drawings.

CHAPTER 7

CSR FUNCTION AND LOGIC

7.1 GENERAL

The CSR controls the memory diagnostic modes and manipulates and stores error information as well. Thereby, it gives the user access to the memory that he must have for troubleshooting and programming purposes.

The CSR address will normally be 772136. A pair of jumpers allows the option of choosing address 772134 (Table 7-1).

Table 7-1 CSR Address Modification

Jumper Installed	CSR Address Selected
W1	772136
W2	772134

This allows the user to have two controllers on the same system. They would, of course, have to be in two separate backplanes. Note that these addresses are the two highest addresses of the parity module (M7850). The CSR can be addressed even if the memory is busy, i.e., finishing a data cycle or performing a refresh cycle. Contents are not changed on a refresh cycle or with battery backup master reset. Figure 7-1 shows the bit allocation of the CSR.

On power up, all bits except CSR bits 11–5 are cleared to zeros. All used bits can be written and read from the Unibus, with the unused bits (12 and 14) being read as zeros.

Note that pressing the start button will enable BUS INIT, clearing the CSR (except bits 11–5). Pressing continue will not clear the CSR.

7.2 WRITING TO THE CSR

CSR bits can be written from the bus master by placing the 1 or 0 desired on the appropriate Unibus data line. Assume, for example, that the user wishes to set CSR bit 0 to a logic 1 and places a logic 1 on Unibus data bit 0 line. DI 00 H goes high and, when CSR ADD SEL H and MSYN H qualify the NAND gate E119, pin 8, CSR SEL TIM L becomes true, enabling SSYN (sheets 10, 2). As Unibus line C1 is also a logic 1 (indicating that a write is to be performed), WRT CK H goes high, clocking each bit in the CSR, and causing CSR 00 H to become true.

7.3 READING THE CSR

When the CSR address is placed on the Unibus address lines and decoded by the CSR address decoder circuit (sheet 10), CSR ADD SEL L causes the CSR/data multiplexers to select the A inputs. Figure 7-2 shows a 4-bit slice of this circuit. The truth table (Table 7-2) below shows the selection process.

15	DOUBLE ERROR
14	NOT USED
13	SET INHIBIT MODE
12	NOT USED
11	A17 OR CHECK BIT T
10	A16 OR CHECK BIT 32
9	A15 OR CHECK BIT 16
8	A14 OR CHECK BIT 8
7	A13 OR CHECK BIT 4
6	A12 OR CHECK BIT 2
5	A11 OR CHECK BIT 1
4	SINGLE ERROR
3	INHIBIT MODE 0 PROTECTS 1ST 16K POINTER 1 PROTECTS 2ND 16K
2	DIAGNOSTIC CHECK
1	DISABLE ERROR CORRECTION
0	DOUBLE ERROR INDICATION ENABLE

NOTE:
IF DIAGNOSTIC CHECK
BIT IS SET THEN
CHECK BITS ARE ALWAYS
STORED IN CSR ON
DATI CYCLE TO MEMORY.
IF NOT SET THAN ADDRESS IS
STORED ON DOUBLE ERROR
ONLY ON DATI OR
DATIP CYCLE.

11-5395

Figure 7-1 CSR Bit Allocation

DATA BIT 00

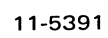


Figure 7-2 CSR/Data Multiplexer, a 4-Bit Slice

Table 7-2 CSR/Data Multiplexer (74157)

Inputs G	SEL	Outputs Y
L	L	A
L	H	B
H	X	L

With SSYN L true, CSR bits 0–15 are gated to the Unibus data lines.

7.4 CSR BIT FUNCTIONS

A discussion of the individual CSR bits follows.

7.4.1 Double Error Indication Enable (CSR Bit 0)

If a double error occurs on a DATI or DATIP cycle to the memory and CSR bit 0 is set, then BUS PBL will be asserted on the Unibus at the same time as the data. Bit 0 is reset by BUS INIT L.

7.4.2 Disable Error Correction Mode (CSR Bit 1)

If CSR bit 1 is set, the syndrome bit latches are never enabled on any type of cycle to memory. Thus, the error correction circuits are disabled and no single-bit error correction or double-error detection will occur. Correct check bits are still written into memory, however. This is a diagnostic aid to allow writing and reading data from memory without interference from the error correction logic.

Also, this is a means of clearing a soft double error in memory. Note that a soft double error may be caused by the occurrence of one hard error and one soft error, or two soft errors within a memory word (a hard double error cannot be cleared). The disable error correction bit is set and the appropriate word in memory is written. No double error is sensed on the read portion of the read-modify-write cycle because the syndrome latches are disabled. On the write portion, the new check bits are generated on whatever data is in the MDR and are not corrected when written into memory. The next read to that address with ECC enabled will not show any errors.

No double-error or single-error information is logged in the CSR having this mode enabled. This bit is reset by BUS INIT L.

CSR 01 H high will qualify ECC DIS L and H if the inhibit mode is not active (INH MODE L must be high) (Figure 7-3). ECC DIS L then disables the signal STROBE SYN H (E111, pin 6 low), so that the syndrome latches cannot be clocked.

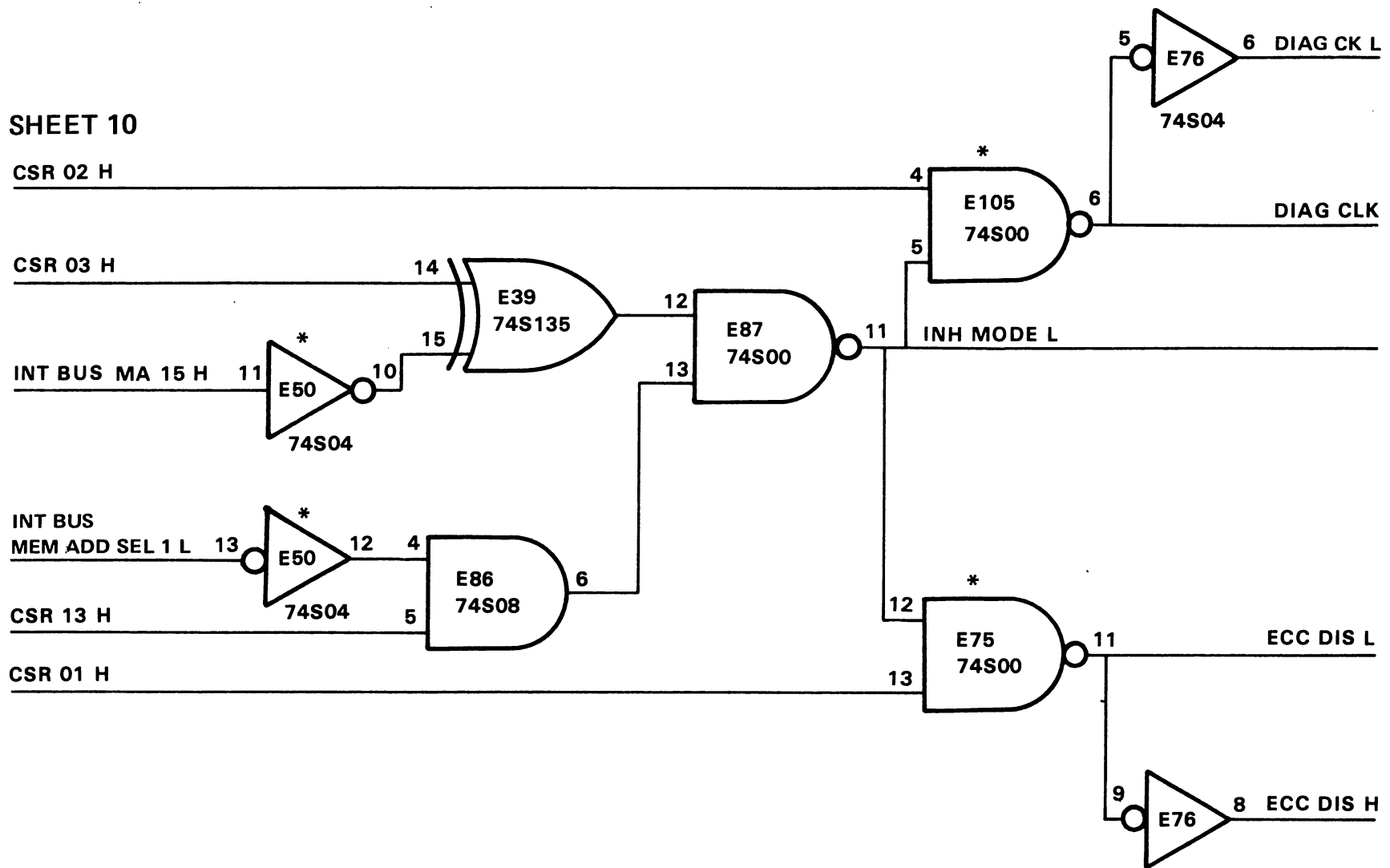
7.4.3 Diagnostic Check Mode (CSR Bit 2)

CSR bit 2 is reset by BUS INIT. The diagnostic check mode allows a means of writing data stored in CSR bits 11–5 into the MOS RAM chips used for check bit storage. A DATO cycle to memory is used for this. The cycle is always the shorter write cycle in this mode instead of the read-modify-write cycle. Since the check bits to be written are already in the CSR, it is not necessary to generate them with a read-modify-write cycle.

If the INH MODE L signal is false, CSR 02 H qualifies DIAG CK L and H, disabling DR TIM CK L, but enabling DR TIM DIAG CK L (sheet 13). DR TIM DIAG CK L, in turn, enables CSR bits 11–5 onto the internal memory bus check bit lines (Figure 7-4). Notice that the seven pairs of 74LS240 drivers function as a multiplexer.

This mode also allows a means of reading data stored in the check bit storage into CSR bits 11–5. A DATI cycle to memory is used for this.

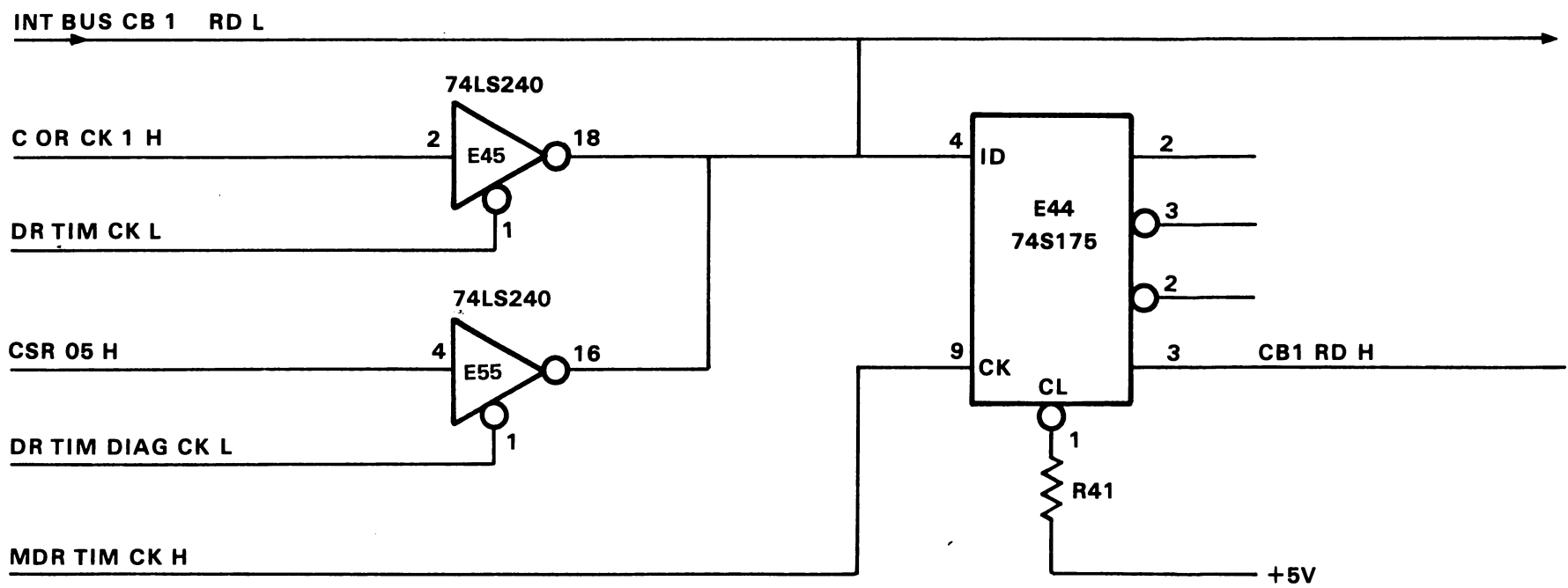
SHEET 10



11-5400

Figure 7-3 Generation of ECC DIAG CK L and ECC DIS L Signals

SHEET 13



11-5399

Figure 7-4 CSR/Check Bit Multiplexer and Check Bit Register

Operation in the diagnostic check mode, therefore, allows both an integrity check on the check bit storage chips and a check on the error correction logic. With a data field of all 1s, the check bits can be set so that they change bit 0 from a 1 to a 0. This can be repeated on each bit. The data can then be complemented and the test repeated.

For example, the check bit pattern generated on a data pattern of all 0s will be 0111111 (where CT is 0). If the user alters the check bit pattern to read 1100111, the error correction circuitry should detect an error in bit 0 of the double word (Table 7-3). In order to implement this example, the user should perform a DATO to the CSR, writing the 1100111 (starting with CT) pattern into bits 11–5 of the CSR (note that CT corresponds to CSR bit 11), and writing a 1 into CSR bit 2 (the diagnostic check bit) (Table 7-3). With the CSR thus set up, the user should perform several DATO cycles to memory, writing 0s into several consecutive locations.

Table 7-3 Data Modification Through the Check Bits

Check Bit Pattern	CT	C32	C16	C8	C4	C2	C1
Generated on all 0s data	0	1	1	1	1	1	1
Imposed check bit pattern	1	1	0	0	1	1	1

The diagnostic check bit (CSR bit 2) should then be set to 0, with a DATO to the CSR. When the user subsequently initiates DATI cycles to the same memory locations, the error correction logic should invert bit 0 of the data, placing the corrected data on the Unibus. Notice that bit 0 will be inverted only on every other word, because no correction will take place on bit 16 of the double word.

If a double error occurs in this mode (with CSR bit 1 = 0) the D ERR bit in the CSR is set, but the check bits read from memory are stored in CSR bits 11–5 and not the D ERR address bits.

DIAG CK H controls the select inputs of the two 2:1 multiplexer chips (E72, E85). When true, DIAG CK H selects the B inputs, the outputs of the seven check bit register latches, gating them to the CSR input pins (bits 11–5).

When TIM 550 H goes true and is ANDed with LC1 L (high), the resulting high signal is gated through the B side of the multiplexer (E72). It is then inverted to clock the seven check bits into the multiplexer with storage (sheet 9).

7.4.4 Inhibit Mode Pointer (CSR Bit 3)

CSR bit 3 is reset by BUS INIT. The inhibit mode pointer works in conjunction with the set inhibit mode (bit 13). When bit 13 is set to a 1, a 16K portion of memory is inhibited from operating in the ECC disable mode or diagnostic check mode. The inhibit mode pointer indicates which 16K portion is being inhibited; i.e., if bit 3 = 0, the first 16K of memory is inhibited. If bit 3 = 1, the second 16K of memory is inhibited. With bit 13 set to a 0, bit 3 becomes inoperative.

Bit 3, in conjunction with bit 13, therefore, allows a 16K portion of memory to always have ECC coverage. The system diagnostic can reside in this protected portion of memory and can disable ECC and/or run the diagnostic check mode in the rest of memory without itself becoming vulnerable to single errors.

If address bits MA 16 and MA 17 are low (first 32K), the INT BUS MA 15 H signal controls the selection of the 16K segment to be addressed. MA 15 H is inverted and Exclusive ORed with CSR 03 H (Figure 7-3).

An example of the functioning of the circuit follows. If the first array module is selected (INT BUS MEM ADD SEL 1 L true) and CSR bit 13 is set, INH MODE L will be true when INT BUS MA 15 H is true and CSR 03 H is true. Such a condition inhibits the DIAG CK L and H signals when a location in the second 16K of memory is addressed, protecting the second 16K addresses.

7.4.5 Single Error (CSR Bit 4)

On a DATI or DATIP cycle to memory, if a single error occurs, bit 4 is set. An examination of the CSR can thus be performed to see if a single error has occurred. This bit is cleared by BUS INIT L.

Notice that LC1 L must be high (read cycle) in order for SERR H to set CSR bit 4 when TIM 550 H goes true (sheets 9 and 10).

7.4.6 Address and Check Bit Storage (CSR Bits 11-5)

CSR bits 11-5 are not cleared by BUS INIT L or on +5 VBB power up.

Address Storage (DIAG CK Bit 2 = 0, ECC Disable Bit 1 = 0)

If a double error occurs on a DATI or DATIP cycle, then address bits A17-A11 are stored in these bits. This locates the double error within a 1K segment of memory.

Check Bit Storage (Diag CK Bit 2 = 1)

During a diagnostic check mode, CSR bits 11-5 are used to store the check bits to be written into memory or the check bits read from memory. If a double error occurs in the diagnostic mode, and the ECC Disable bit (CSR bit 1) equals 0, then the check bits are stored in the CSR together with the double-error bit.

7.4.7 Set Inhibit Mode (CSR Bit 13)

CSR bit 13 is cleared by BUS INIT L. When set to a logic 0, it allows the diagnostic check mode and/or ECC disable mode to operate over the entire installed memory.

When bit 13 is set to a logic 1, it enables the INH MODE POINTER to inhibit either the first or second 16K portion of memory from ever going into the diagnostic check or ECC disable mode (Figure 7-3).

7.4.8 Double Error (Bit 15)

On a DATI or DATIP (ECC disable bit 1 equals 0), CSR bit 15 is set if a double error occurs. The upper address bits A17 - A11 are stored in CSR bits 11-5 (DIAG CK bit 2 = 0) and will point to the 1K segment of memory that was addressed when the double error occurred. If DIAG CK bit 2 = 1, then the check bits read from memory are stored in CSR bits 11-5. Bit 15 also energizes an LED for a visual indication of the error. This bit is cleared by BUS INIT L. Notice, however, that although bit 15 and the LED will be cleared by BUS INIT L, the double error to which it refers will not be cleared. See Paragraph 9.5 for the procedure used to clear a double error.

CHAPTER 8

INSTALLATION OF THE MF11S-K MEMORY

8.1 GENERAL

Since the nine slot backplane, DD11-K, has been designed specifically for the MF11S-K, the backplane specifications should be examined thoroughly before configuration and power application.

8.2 DD11-K BACKPLANE SLOT ALLOCATION

The M7984 array module will fit in slots 7 through 4 of the DD11-K backplane. The M7983 controller, however, must be placed in slot 8. The array slots are dedicated according to memory size. The first 32K of memory must go in slot 7, the second in slot 6, the third in slot 5, and the fourth in slot 4. Slot 1 must be used for the Unibus cable-in jumper. Slot 9 must contain either a Unibus cable out jumper or a terminator. Figure 8-1 shows the DD11-K backplane slot allocation.

The internal memory bus runs on the A and B connectors to slots 8 through 4 (Figure 8-2).

While all of the slots are available as small peripheral controller slots, if the MF11S-K memory is not present, care must be used in slot allocation with or without the presence of MF11S-K memory modules. Hex SPC modules can be installed but power and ground pins must be compatible (see appendix). Slots 2 and 3 are pinned according to the modified Unibus configuration on connectors A and B. Some single module core and MOS memories could be plugged into these slots if no MF11S-K memory is installed in the backplane.

MF11S-K memories and other memory types are mutually exclusive with respect to the backplane. The MF11S-K requires ± 12 V where the MS11-E through J series of MOS memories requires ± 15 V and core memories require +20 V.

After the backplane has been configured with the MF11S-K modules and Unibus jumpers (or jumper and terminator), the slots that remain can be used for any SPC control module that picks up Unibus signals on connectors C, D, E, and F. Slots that are unused altogether should contain bus grant cards.

NOTE

**Be sure to remove the NPG wire on the backplane
when installing an NPG option in any SPC slot.**

The backplane power harness will plug into any power distribution board slot.

8.3 MF11S-K OPTIONS

The options available in the MF11S-K memory are listed below.

8.3.1 MF11S-K (32K MOS System Complete)

This option contains the following:

- One M7983 controller
- One M7984 32K × 16 array module
- One DD11-K backplane with appropriate power harness
- One M9202 Unibus jumper
- Seven bus grant cards
- Print set
- User's manual
- Diagnostic DZMML

NOTE

An additional letter at the end of the option name specifies the appropriate power harness depending on the box in which the backplane is installed; i.e., the MF11S-KK comes with the DD11-KK power harness for the BA11-K 10-1/2 inch box. The MF11S-KF comes with the DD11-KF power harness for the BA11-F 21 inch box.

8.3.2 MS11-KA (32K × 16 MOS Array Module)

This option contains the following:

One M7984-AA 32K × 16 MOS array module.

NOTE

M7984-AA = M7984-AB = M7984-AC = M7984-AD = M7984-AE, etc.

The MS11-KA can be replaced by an MS11-KE. The latter option contains faster access time MOS chips. Using this option does not, however, reduce system access time.

The letter *A* designates the memory module size (32K × 16 bits). The second letter identifies the vendor of the MOS chips used on the array.

8.3.3 Options Required Per Storage Capacity

Storage Capacity Options Required

32K × 16	One MF11S-K
64K × 16	One MF11S-K One MS11-KA or MS11-KE
96K × 16	One MF11S-K Two MS11-KA or MS11-KE
128K × 16	One MF11S-K Three MS11-KA or MS11-KE

Figure 8-3 shows a fully configured MF11S-K 128K memory.

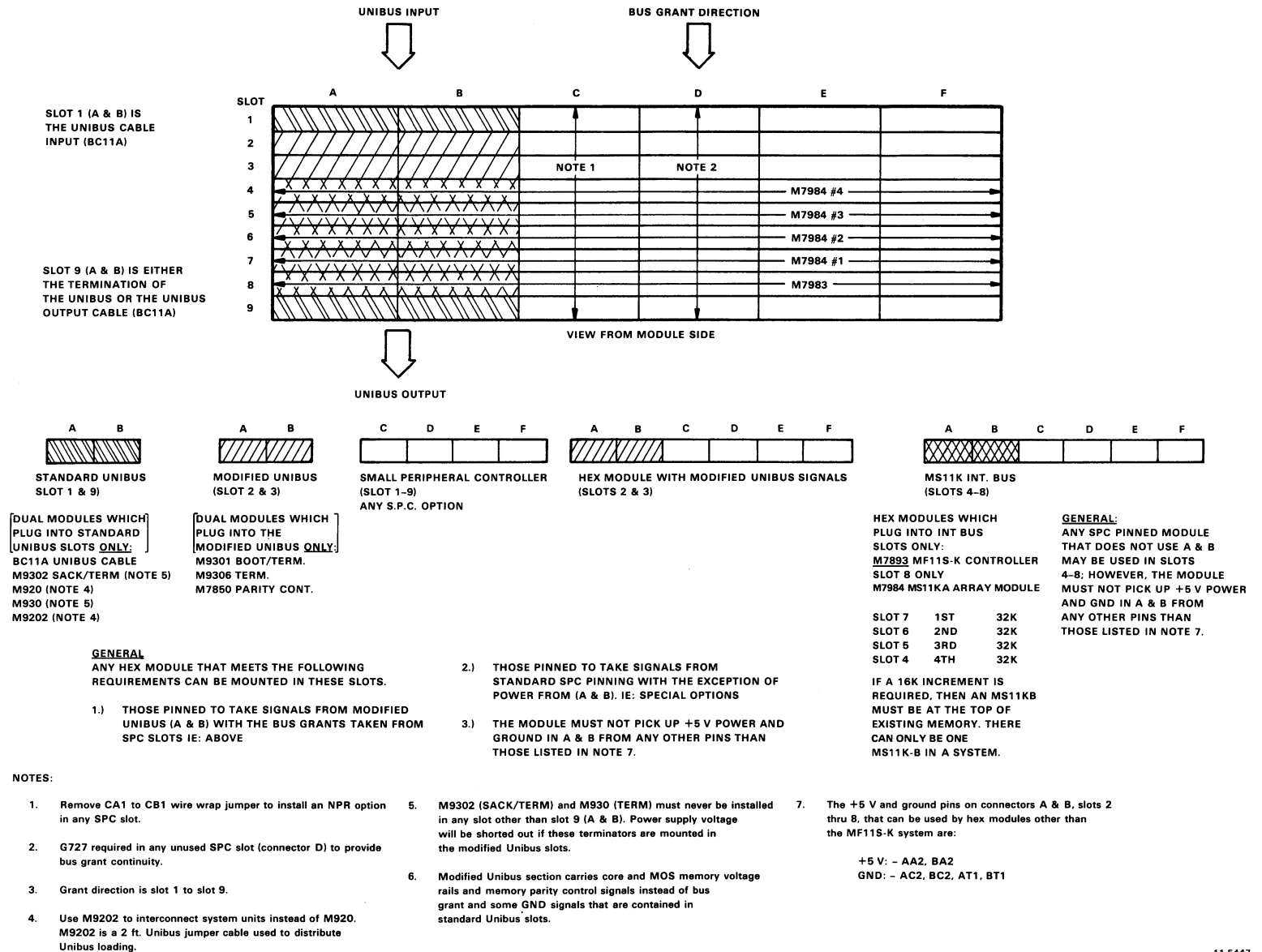
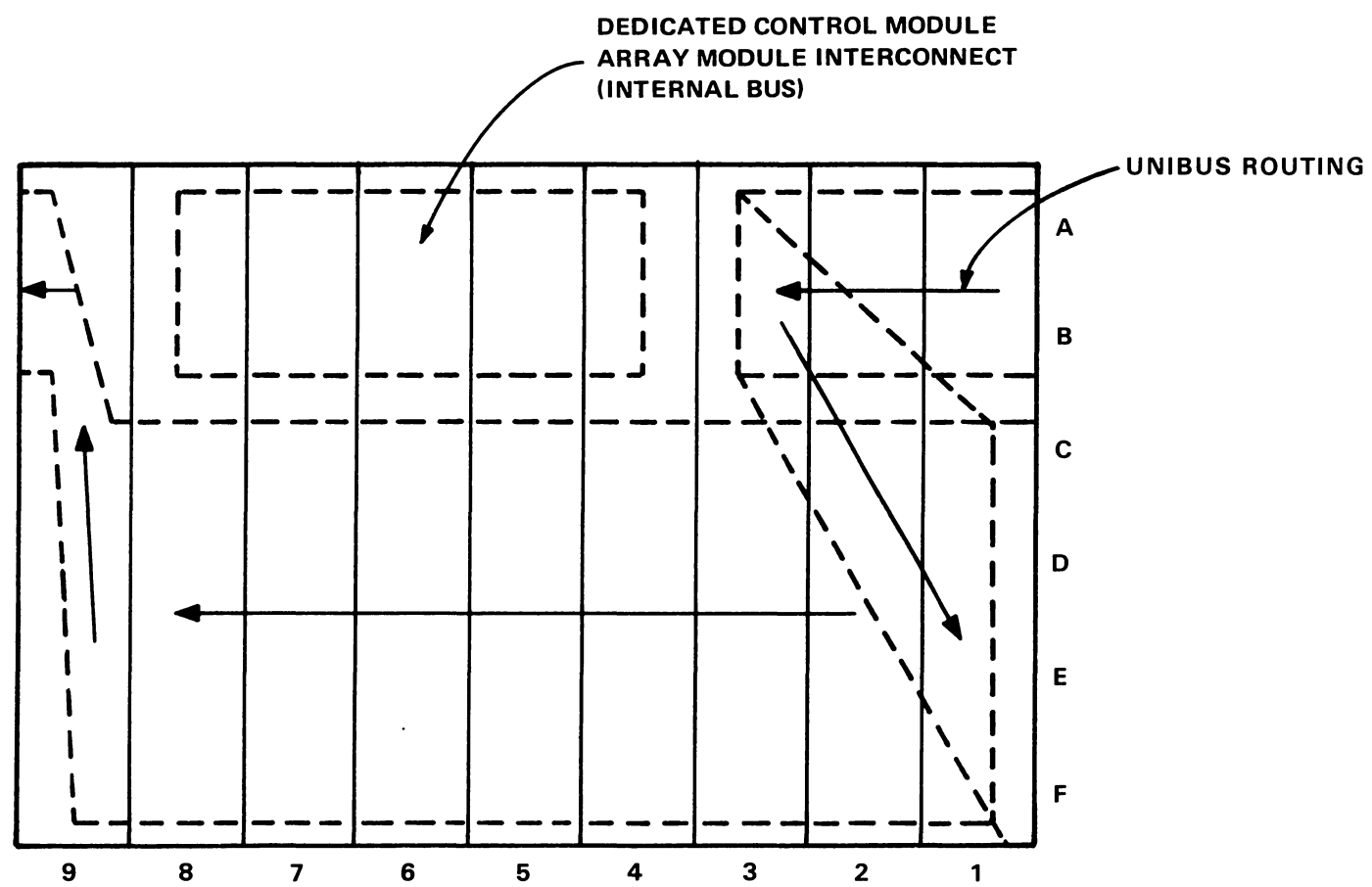


Figure 8-1 DD11-L Backplane Utilization



NOTE:
 Routing from connectors AB → CDEF is staggered
 to reduce wire bundling. Critical signals are on twisted pair.

11-5444

Figure 8-2 DD11-K Backplane Unibus Routing

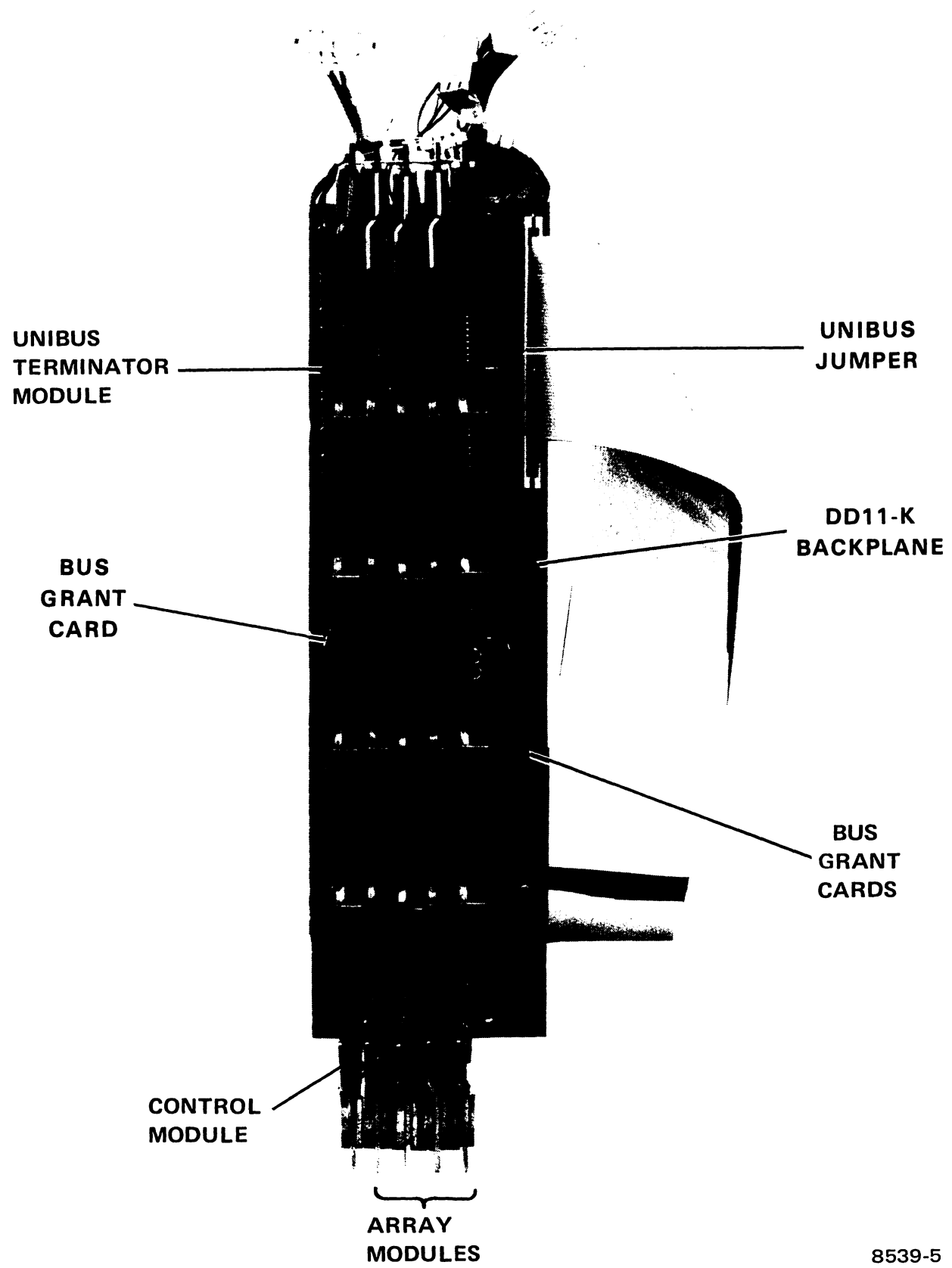


Figure 8-3 Fully Configured DD11-K Backplane

8.4 MIXING THE MF11S-K AND OTHER MEMORIES

Other memories can be used in the address space both above and below the MF11S-K. These other memories, whether core or MOS, must be installed in another system box because of the power supply restrictions mentioned in Paragraph 8.2. The MF11S-K requires ± 12 V.

The address of the lowest location in the MF11S-K is controlled by four microswitches located on the M7983 controller (Paragraph 5.4.1 and Table 5-1). The highest address is a function of the number of array modules used.

8.4.1 Address Space Above MF11S-K

There are no restrictions on putting other memories in the address space above the MF11S-K.

8.4.2 Address Space Below MF11S-K

Other Memory Below MF11S-K	Max MF11S-K Size
8K→ 32K	96K
40K→ 64K	64K
72K→ 96K	32K

For a full 128K system, other types of memories may, in some cases, be placed in the address space above the MF11S-K.

8.5 SUPPLY VOLTAGES

Check the +5 V and ± 12 V levels on the backplane before installing modules. When system power can be applied, the voltage level on the +12 V line on the array module should be adjusted at the power supply to provide the correct level.

8.6 FIRST TIME START-UP

The following procedure should be followed for first time start up of the MF11S-K memory system upon installation.

1. Ensure that all power is removed from the memory, including battery power.
2. Apply power.
3. Load MAINDEC-11-DZMML-A, the MF11S-K system diagnostic program.
4. Run DZMML for two complete passes (with the console switch register set at zeros).
5. Run DZMML for two complete passes with single errors enabled (bit 11 on the console switch register set). There must be no single errors for installation. However, after installation, single errors are allowable and are not considered faults.

CHAPTER 9

TROUBLESHOOTING THE MF11S-K

9.1 GENERAL

The information in this chapter is designed to supplement the technician's knowledge of the MF11S-K by suggesting possible courses of action for troubleshooting the memory. These suggestions are based on the assumption that a system fault has been traced to the MF11S-K memory by system troubleshooting procedures. We also assume that the MF11S-K begins at address 0. If any other starting address is used, the operator should modify the following procedures as appropriate.

Two main categories of problems may be encountered when using the system diagnostic (DZMML) for fault isolation. If the diagnostic will not load properly, then proceed to Paragraph 9.1 and the flowchart shown in Figure 9-1. If it is possible to load the diagnostic, then proceed by utilizing the error printout and the DZMML listing.

9.2 ECC INITIALIZATION

Before attempting any troubleshooting, power down and up to force ECC initialization. If batteries are on the system, they must be turned on after power has been restored. If the batteries are not turned off initially, the memory will not perform ECC initialization.

9.3 PROCEDURE TO ISOLATE FAULTS THAT PREVENT LOADING DIAGNOSTICS

9.3.1 Array Module Swap

If the system has more than one array module, exchange the one in slot 7 with any other array and try loading the program again. If only one array is used, proceed to troubleshoot according to the no load fault isolation flowchart (Figure 9-1).

It is important to make sure that all power to the memory is off before attempting to remove any of the modules. System power should be removed by throwing the power switch on the front panel. If a backup battery option is included in the system, however, power will still be applied to each of the modules in the MF11S-K system. The backup battery should be turned off, disabling the H7850 regulator. Note that the green LEDs on the array modules indicate the status of power to the memory.

9.3.2 Initial Check

Load address 000000 via the switch register or input device and examine the contents of the location. If you are unable to load the address (i.e., an improper address is displayed), then check BUS AC LO L (E122-13). This should be a logic high. If BUS AC LO L is low it indicates that the ECC INIT flip-flop (E118) did not reset. If address 000000 can be loaded, the CSR should be examined. The CSR logic and storage elements are entirely on the control module. Therefore, if the CSR is addressable and returns SSYN, but address 000000 does not return SSYN, it is likely that a fault exists in the address logic.

If SSYN is returned when both address 000000 and the CSR are addressed, bits 0, 1, 2, and 13 of the CSR should be examined. If they are not equal to zero, check to see whether the CSR is reset on power up.

9.3.3 Timing Check

Disable refresh by grounding REF IN H (E102-5), ground the SSYN flip-flop data input (E120-12), and ground MSYN L (E124-7). Check the SSYN flip-flop clock (E120-11), which should be clocking in 700 ns cycles. If it is not, check MEM GO L input conditions (E117), which all should be high. Proceed by checking the timing signals from delay lines DL1 and DL2.

9.3.4 SSYN Check

Ground MSYN L (E124-7). The SSYN flip-flop clear line (E120-13) should be high. Ground CSR SEL TIM L (E120-10). BUS SSYN L (E122-1) should be low.

9.3.5 CSR Address Decode

Load CSR address (772136) and check CSR ADD SEL H (E92-13) to see that it is enabled.

9.3.6 ECC Initialization Check

Load and examine the following consecutive locations in memory: 0, 2, 4, 6, 10, and 12. Note the data pattern displayed at each location. If the data equals all 0s or is a specific pattern (i.e., the same bits in each location equal 1s), there may be a double bit error. If a random pattern exists, the refresh cycle logic should be checked.

9.3.7 Refresh Cycle Check

Check the Refresh Cycle flip-flop, which should reset every 25 μ s. Check the refresh address counter (E80, E123). Addresses should be incrementing. Internal bus signals RAS TIM L (E1-4) and CAS TIM L (E1-6) should be asserted at the refresh rate.

9.3.8 ECC Initializaton Cycle

Perform the following operations to run a continuous ECC initialization cycle.

- Assert DC LO by grounding E124-11.
- Power up.
- Check to see that ECC INIT H (E118-5) is high and that BBM RESET A L (E129-8) is low.
- Ground E126-13 to inhibit overflow.
- Remove the ground from E124-11.

The ECC initialization cycle should now run continuously, then, check the following circuits.

- Internal bus data equals 0.
- Check bit data equals 0111111, where CT is 0.
- The write timing logic, write byte signals, and DR and MDR timing signals should be enabled every 8 μ s.

9.3.9 Double-Bit Error Indication

Load and examine the CSR (772136). If bit 15 is high, a double error is indicated. Error correction should be disabled.

9.3.10 Disable Error Correction

Load CSR (address 772136) and set CSR 01 H (disable ECC). Deposit and examine 1s in the following locations: 0, 2, 4, 6, 10, and 12. If the data in all locations equal 1s, the ECC initialization should be checked. If the data does not equal 1s, a bit check should be made.

9.3.11 Bit Check

If a single-bit error was observed in locations 0, 2, 4, 6, 10, and 12, then the following circuits should be checked: the output of the double word multiplexer to the drivers (E34, E65, E73, and E51), and the receiver to MDR signals (E24). If a single-bit error occurred in alternate locations, check the MDR and the double word multiplexer input (E24, E34).

9.3.12 No Double Error

Deposit and examine 1s in locations 0, 2, 4, 6, 10 and 12. If the data does not equal 1s, examine the CSR for a double error indication (Paragraph 9.3.9). If bit 15 of the CSR is high, the ECC logic is probably not faulty. If low, disable error correction.

9.3.13 Error Before ECC

Array module signals should be checked. Some checking may be accomplished in a refresh cycle or ECC initialization cycle (Paragraph 9.3.8). If all appear to be correct, perform the toggle in memory test.

9.3.14 Data Equals 1s

If the data in Paragraph 9.3.12 equals 1s, deposit and examine 0s in locations 0, 2, 4, 6, 10, and 12. If the data read back is 0s, perform the data shorts check. If the data does not equal 0s, disable the ECC logic as in Paragraph 9.3.10. Then, deposit and examine 0s as before. If the data does not equal 0s, perform the bit check. If the data does equal 0s, run the continuous ECC initialization cycle.

9.3.15 Data Shorts Check

Using memory location 000000, check for data line shorts by depositing and examining successively the following data words; 000001, 000002, 000004, 000010, 000020, 000040, 000100, 000200, 000400, 001000, 002000, 004000, 010000, 020000, 040000, 100000. If no problems are found, check the address circuitry.

9.3.16 Address Circuits Check

To check the address circuits, proceed as follows.

1. Deposit data word 000000 in the following locations: 000000, 000002, 000400, 001000, 002000, 004000, 010000, 020000.
2. Deposit 777777 in location 000000.
3. Examine location 000002. The data should be 000000 as deposited in Step 1. If the data is 777777, the currently set address bit is stuck low or high, or shorted to a previous address bit.
4. Deposit 777777 in location 000002.
5. Examine location 000004. The data should be 000000, as deposited in Step 1. If the data is 777777, the currently set address bit is stuck low or high, or shorted to a previous address bit.
6. Carry on the sequence begun in Step 2 (i.e., location 000004 is next).

9.3.17 Toggle In Memory Test

This test writes 0s, writes 1s, reads 1s, writes 0s, and reads 0s in a given location. It then decrements the address and repeats the above process over a given address range.

Load the program starting at address 100000. Set the top address to 100000 and the bottom address to 0. This will check memory over the first 16K. If this test is successful, load the program starting at address 0. Set the top address to 177776. Set the bottom address to 100000. This will check memory over the second 16K, where the absolute loader will reside.

R0 = Highest Address
R1 = Lowest Address

```

0    012700      MOV #TOP ADDRESS, R0
2    TOP ADDRESS
4    012701      MOV #LOW ADDRESS, R1
6    LOW ADDRESS
10   005040      A:  CLR - (R0)
12   005110      COM (R0)
14   022710      CMP #177777, (R0)
16   177777
20   001005      BNE B
22   005110      COM (R0)
24   001003      BNE B
26   020001      CMP R0, R1
30   001365      BNE A
32   000000      HALT;                ;test complete
34   000000      B:  HALT;                ;error

```

If no error is found, the program stops at location 32. If an error occurs, the program stops at location 34 and the failing address is contained in R0. Check the CSR (772136) to see if DERR (bit 15) is set. The address contained in bits 11–5 of the CSR should match bits 15–9 of R0. If only one array is used, the bad 8K segment (if an array is the problem) can be hardware jumpered to the top of the memory leaving a continuous 24K system (Paragraph 9.7). Repeat the test. If no error is encountered, load the diagnostic and run.

9.4 CLEARING A DOUBLE ERROR

If the MF11S-K error correction logic detects a double error in a given memory location, the controller will inhibit subsequent write operations to that location. Therefore, it is necessary that the user fully understand the methods available for the correction of a double error.

First, the ECC initialization routine will clear the double error by writing zeros and appropriate check bits into all memory locations. The user need only disable the backup battery, power down the system, and then power up in order to enable the ECC initialize routine. It is not necessary to determine the location of the double error to perform this routine. However, since the ECC initialization routine will wipe out whatever programs are stored in the memory, this method may not always be appropriate.

Second, the user can set bit 1 (Disable Error Correction bit) of the CSR by performing a DATO to the CSR. This will disable the error correction logic. The user can then write the data desired into the location containing the double error. Paragraph 7.4.2 explains the logic involved. The user may subsequently enable the error correction logic with a DATO to the CSR.

Note that the memory will function like a standard MOS memory with the Disable Error Correction bit enabled. The user may find it useful to implement this mode in order to run memory diagnostic programs that are written for use with standard memories.

The user can also disable the ECC logic by grounding pin 4 or 5 of E82 (sheet 7) inhibiting the clocking of the syndrome latches.

9.5 FORCING AN INTERNAL WRITE

The user can force the memory to perform an internal write cycle whenever it would normally perform a read-modify-write cycle by grounding pin 10 of E84 (sheet 2). This mode may be useful if, for troubleshooting purposes, it is necessary to write to memory without modifying the check bits stored with the location addressed.

9.6 MOS CHIP REPLACEMENT

If the user wishes to replace any of the MOS chips on an array module, he should make sure that his replacement is identical to the other MOS chips on the module with respect to vendor and part number. Note that MOS chips of different vendors may be used on separate modules within one system, however.

9.7 HARDWARE REMOVAL OF ONE 8K MEMORY SEGMENT

If a fault can be isolated to one of the 4K rows of MOS chips on an array module, it is possible to disable that row while still maintaining the use of the other address space on the module. Proper placement of jumpers W1-W5 will allow for continuous memory from 0-24K on the array module. The user should install the jumper in the appropriate configuration as shown in Figure 9-2. If two or more array modules are used in the system, the module with the row of disabled RAM chips must be placed at the top of memory.

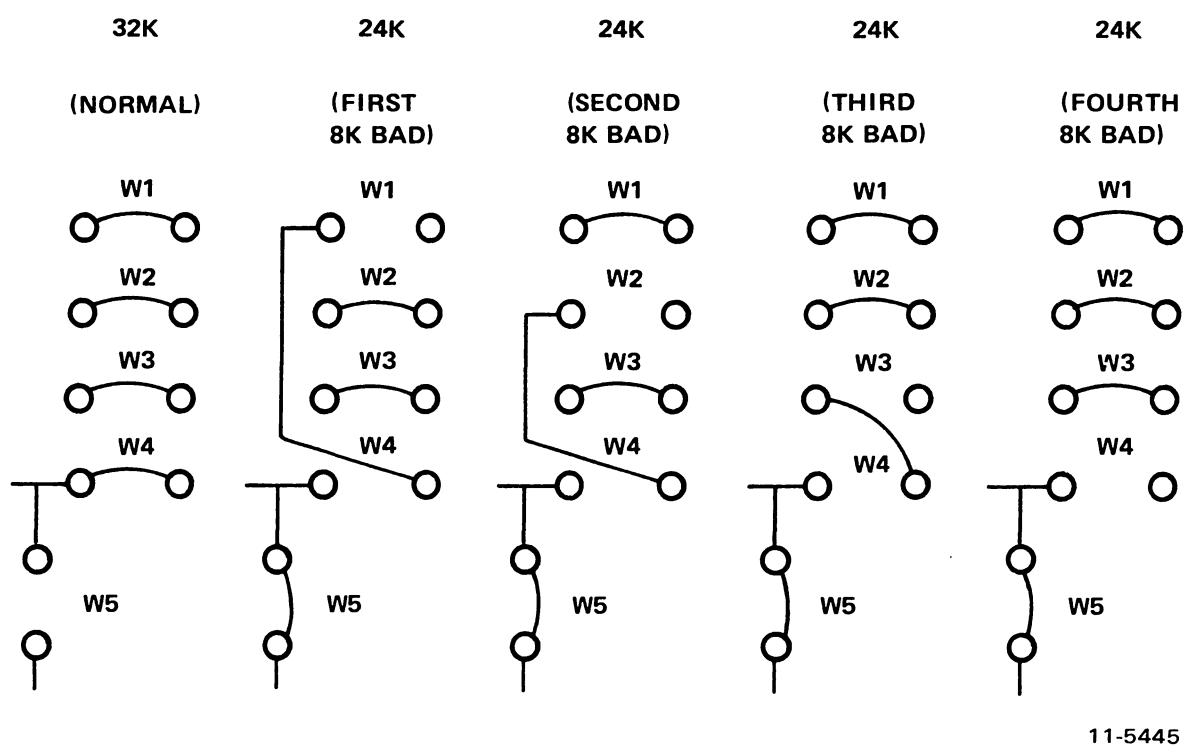


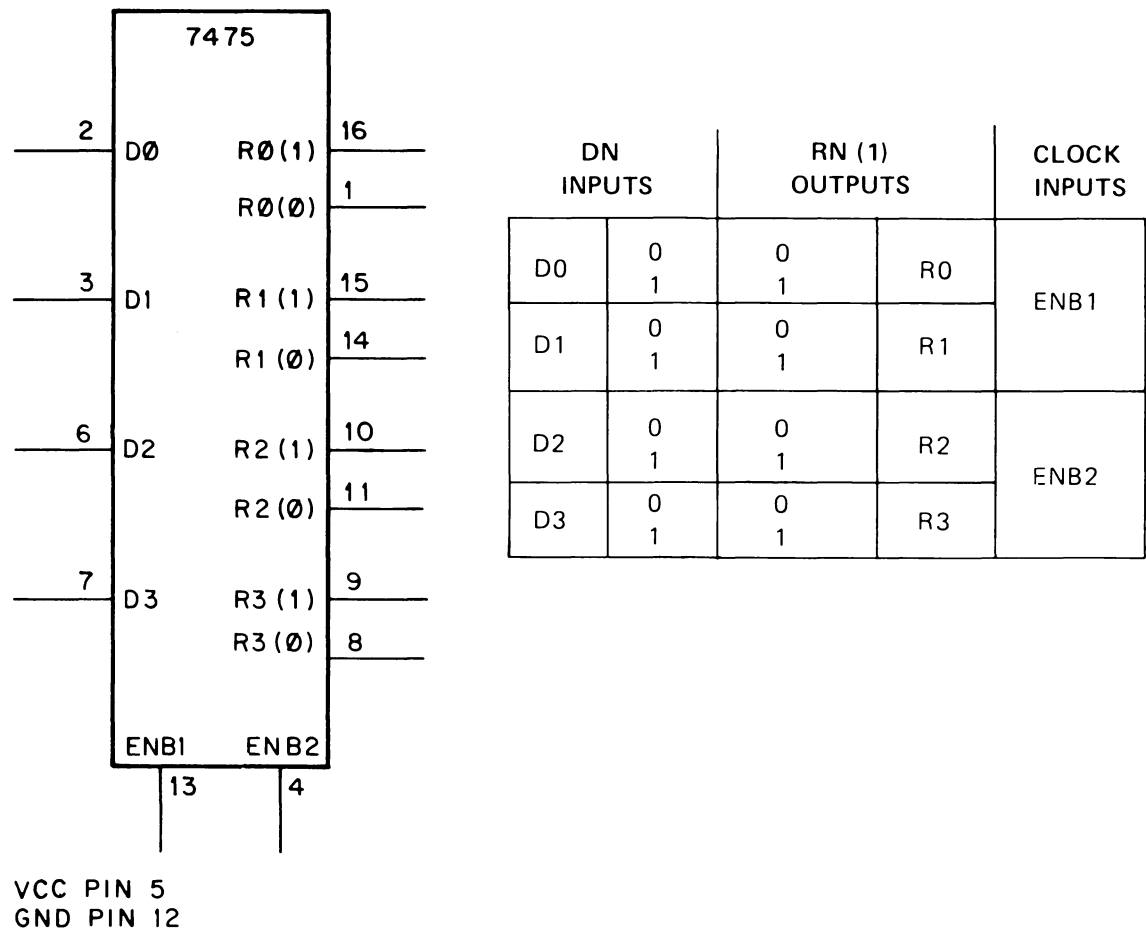
Figure 9-2 Array Module Jumper Configuration

APPENDIX A IC DESCRIPTIONS

This appendix contains descriptions of some of the ICs used in the MF11S-K logic. Only those ICs of an unusual nature are described; the more common types, i.e., NAND gates and inverters, should be familiar to the reader.

7475 4-BIT BISTABLE LATCH

The 7475 latches are used for temporary storage of binary information. Information present at a data (D) input is transferred to the R output when the clock is high, and the R output will follow the data input as long as the clock remains high. When the clock goes low, the information present at the data input at the time of the transition is retained at the R output until the clock is permitted to go high. Input ENB1 is the clock input for data inputs D0 and D1. ENB2 is the clock input for data inputs D2 and D3.

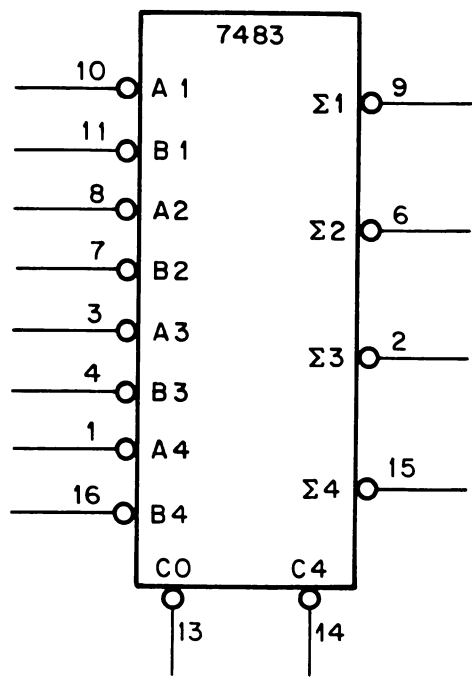


NOTE:
1. RN(0) Outputs = inverted RN(1) outputs.
2. ENB1 and ENB2 clock on negative going edge.

IC-7475

7483 4-BIT BINARY ADDER

The 7483 Binary Adder adds two 4-bit binary numbers. The sum outputs are provided for each bit and the resultant carry is obtained from the C₄ output.

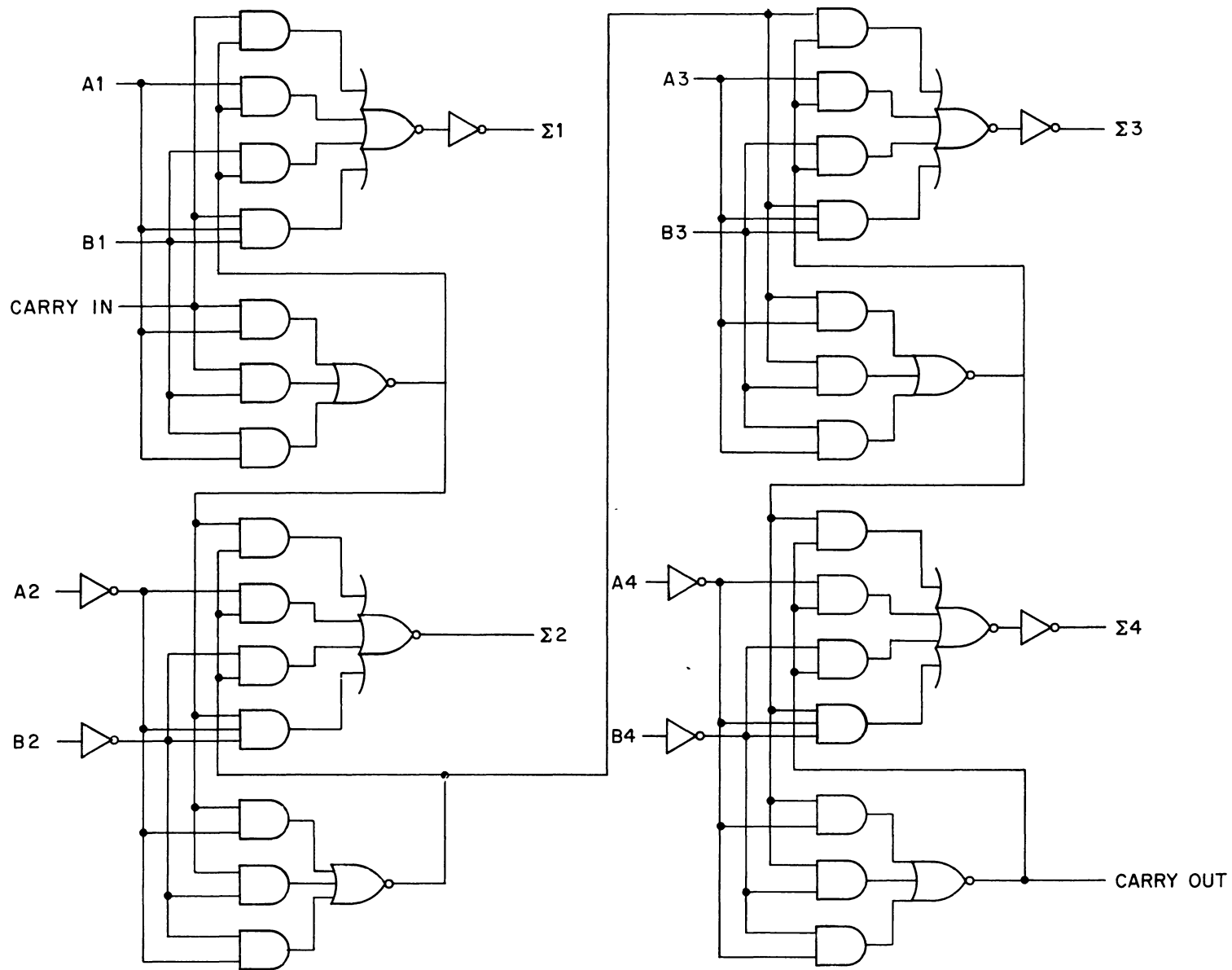


				C ₀
	A ₄	A ₃	A ₂	A ₁
+	B ₄	B ₃	B ₂	B ₁
	C ₄	Σ ₄	Σ ₃	Σ ₂
				Σ ₁

VCC = PIN 5
GND = PIN 12

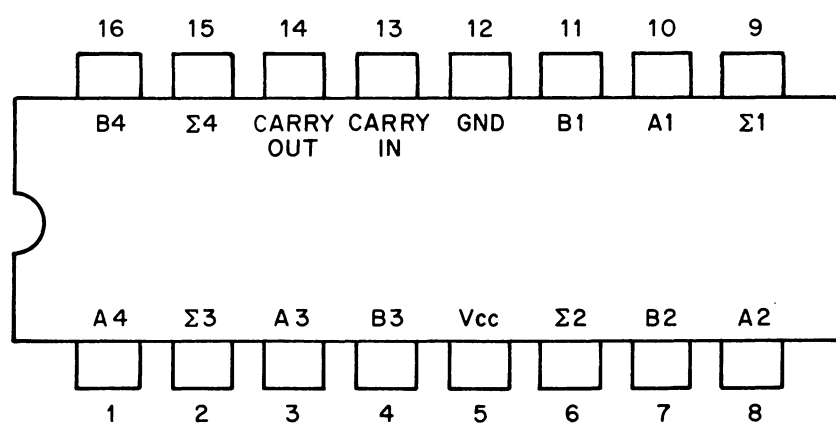
Note: If cascaded, C₀ = C₄ from preceding adder and C₄ = C₀ from succeeding adder.

IC-7483



INPUT				OUTPUT					
				WHEN $C_0 = 0$		WHEN $C_0 = 0$		WHEN $C_0 = 0$	
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
A_3	B_3	A_4	B_4	Σ_3	Σ_4	C_4	Σ_3	Σ_4	C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

LOGIC DIAGRAM

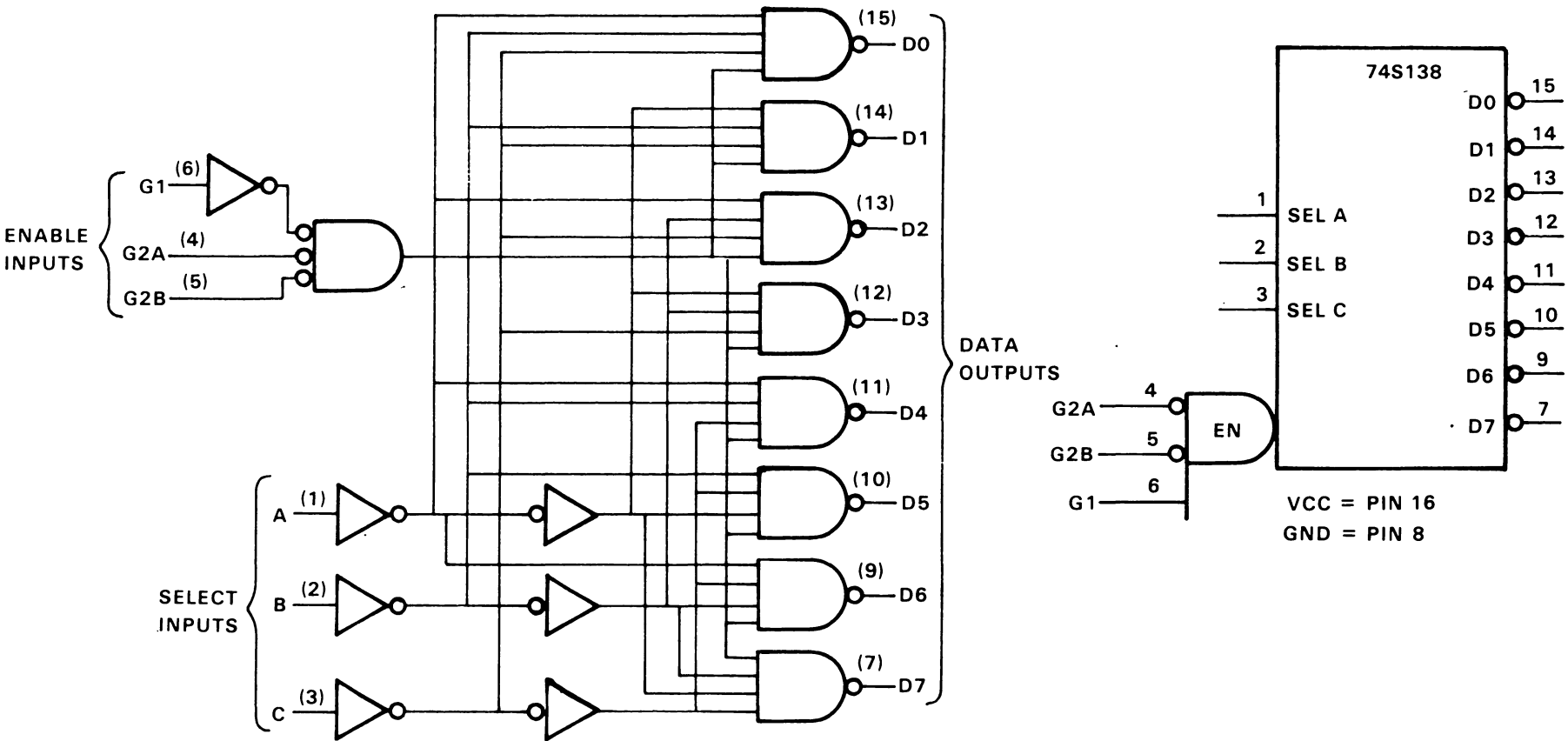


PIN LOCATOR
(TOP VIEW OF IC)

NOTE 1: Input conditions at A_1 , A_2 , B_1 , B_2 , and C_0 are used to determine outputs Σ_1 and Σ_2 , and the value of the internal carry C_2 . The values at C_2 , A_3 , B_3 , A_4 , and B_4 , are then used to determine outputs Σ_3 , Σ_4 , and C_4 .

IC-0093

74138 DECODER/DEMULTIPLEXER



FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2 *	C	B	A	D0	D1	D2	D3	D4	D5	D6	D7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

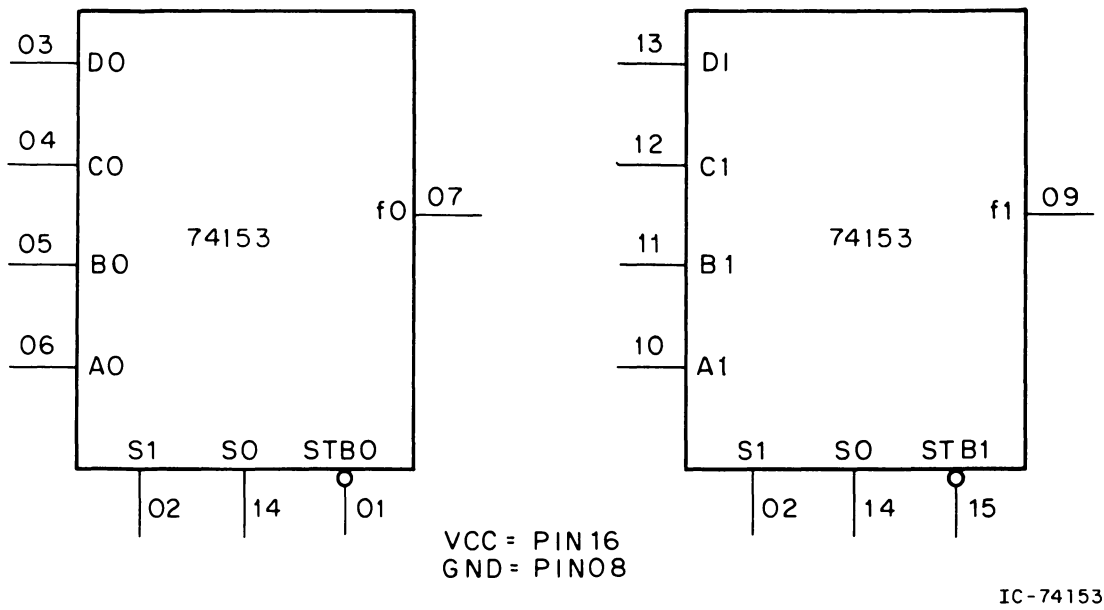
* G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

74153 DUAL 4-LINE-TO-1-LINE MULTIPLEXER

ADDRESS INPUTS		DATA INPUTS				STROBE OUTPUT	
S1	S0	A	B	C	D	STB	f
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

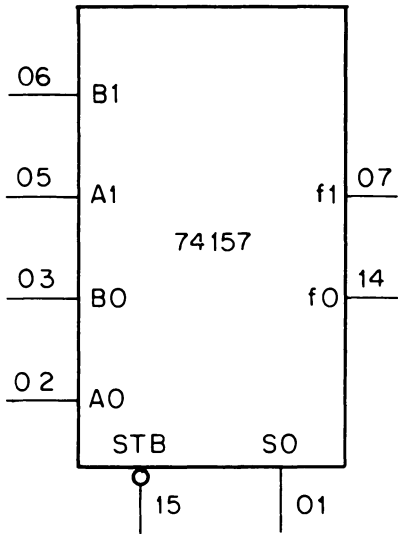
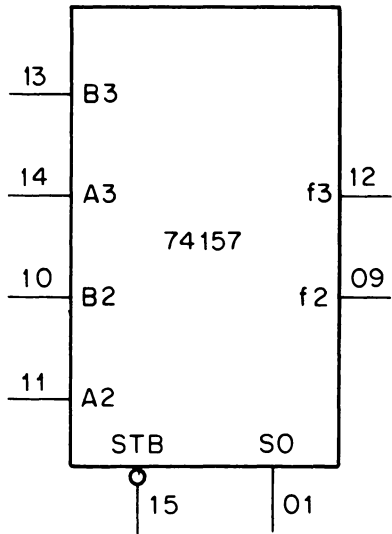
Address inputs S0 and S1 are common to both sections.
H = high level, L = low level, X = irrelevant.



74157 QUAD 2 TO 1 MULTIPLEXER

INPUTS				OUTPUT
STB	S0	A	B	f
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant.



VCC=PIN 16
GND=PIN 08

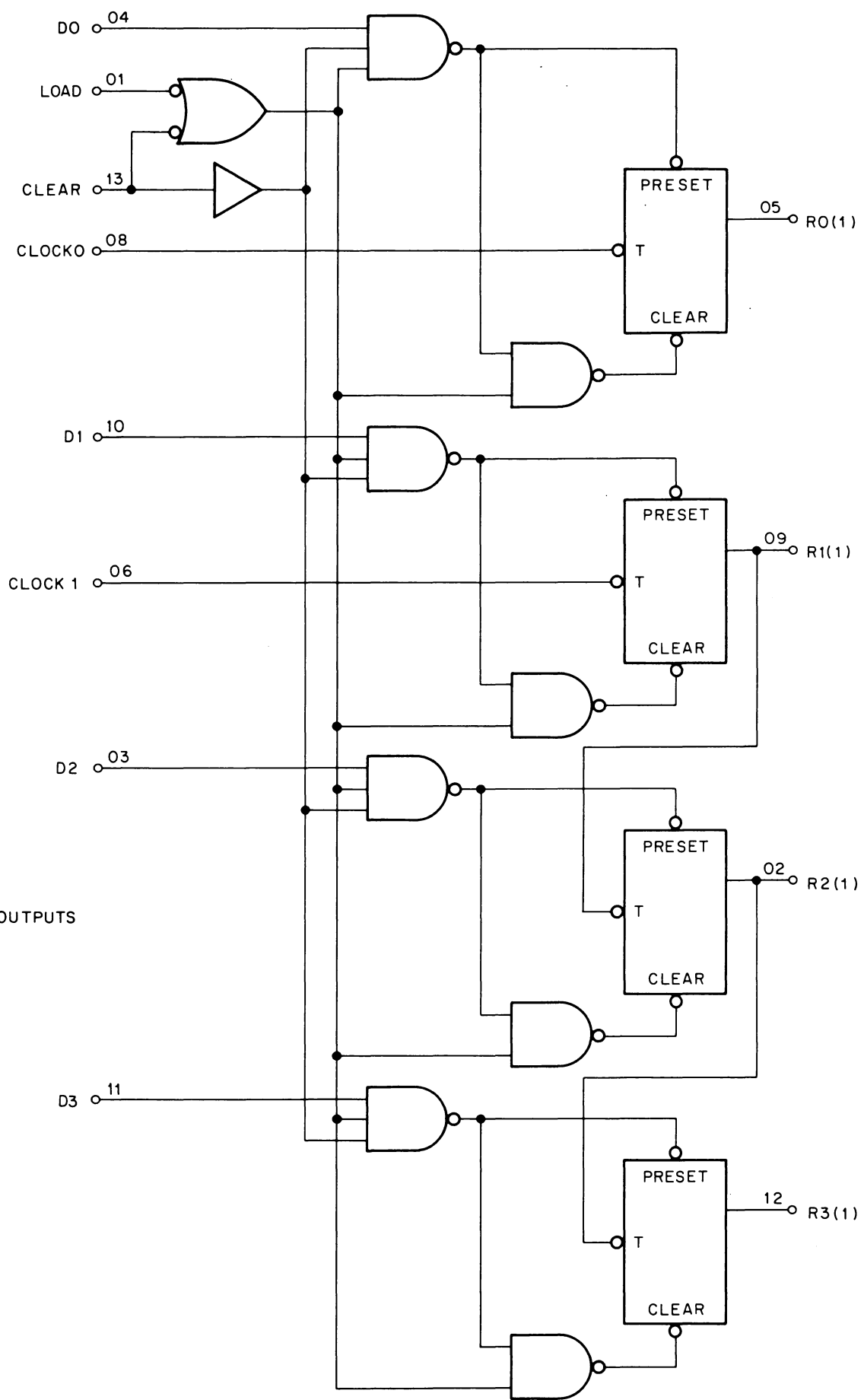
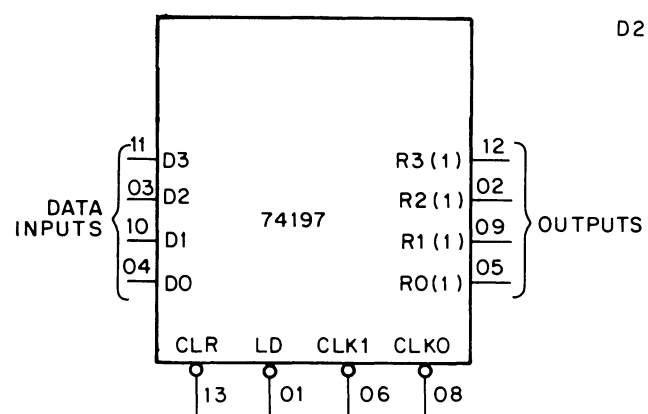
IC-74157

74197 4 Bit Counter

74197
TRUTH TABLE

COUNT	OUTPUT			
CLOCK 1 INPUT	R3 (1)	R2 (1)	R1 (1)	R0 (1)
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

RO (1) connected to CLOCK 2 input.



IC - 74197

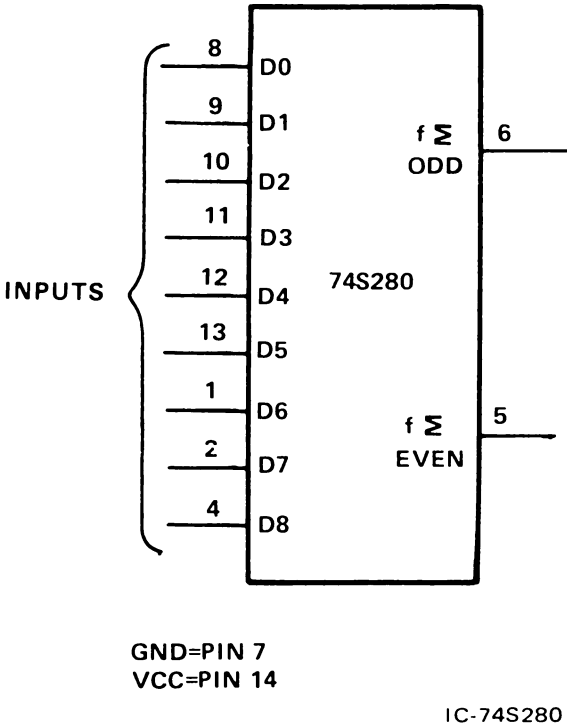
TYPE 74S280 9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

This IC gives a high logic level on the ODD output and a low logic level on the even output when there are an odd number of “1s” or high levels on the nine input pins. The converse is true for an even number of “1s” on the nine input pins.

Function Table

Number of Inputs (A-1) That are High	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

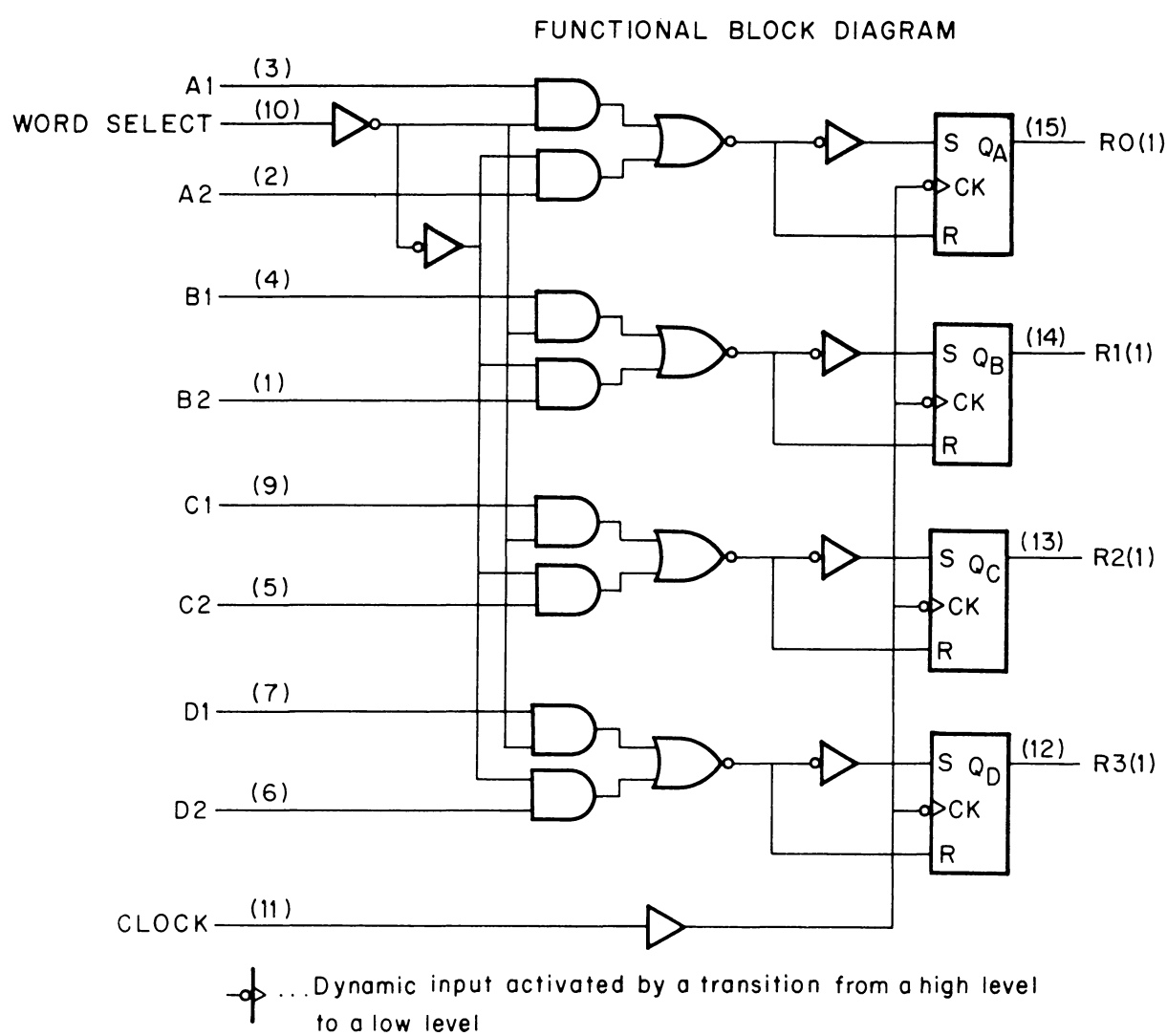
H = High Level
L = Low Level



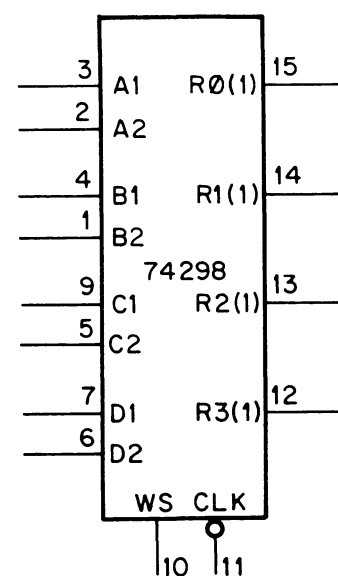
74298 QUAD 2-INPUT MULTIPLEXER

The 74298 multiplexers select one of two four-bit data sources and stores the data synchronously with the system clock.

When the WORD SELECT input (pin 10) is low, word 1 (A1, B1, C1, and D1) is applied to the flip-flops. When the WORD SELECT input is high, word 2 (A2, B2, C2, and D2) is applied to the flip-flops. The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.



IC-74298B



GND = PIN 8
VCC = PIN 16

IC-74298A

APPENDIX B SIGNAL NAME GLOSSARY

Many signal mnemonics are self-explanatory. Some, which may not be, are listed below.

B.1 CONTROL MODULE

Signal	Location	Description
ADD TIM H	E126-3 Sheet 2	Latch Unibus address signals at address time
BBM RESET B L	E127-11 Sheet 3	Battery backup mode reset, clears the CSR (except bits 5-11)
BBM RESET A L	E129-8 Sheet 3	Battery backup mode reset, sets the ECC INIT flip-flop
BUS PB L	E122-4 Sheet 10	Parity error, notification to CPU
COLAD H	E105-11 Sheet 1	Column address selection signal
CB 32 RD H	E41-6 Sheet 13	Check bit 32 read from array
CK 32 GEN H	E36-3 Sheet 6	Check bit 32 generated on MDR data
COR CK 32 H	E47-3 Sheet 8	Check bit 32 to be written into memory, having been corrected
COR D 00 L	E68-15 Sheet 8	Command to correct error in bit 00 of word requested on a read
CSR SEL TIM L	E119-8 Sheet 10	Timing generated when the CSR is selected
DAT IN TIM H	E101-8 Sheet 2	Enables data into data latches during a write cycle
DERR H	E101-11 Sheet 8	Double error

DIAG CK H	E76-6 Sheet 10	Set during the diagnostic check mode
DR TIM 0 L	E40-3 Sheet 13	Enable byte 0 data drivers to array
ECC DIS H	E76-8 Sheet 10	ECC logic disabled
ECC INIT GO L	E112-10 Sheet 1	Refresh override during ECC INIT, selects address counter/latch during ECC INIT, and refresh address counter during refresh
ECC INIT L	E118-6 Sheet 3	Set during ECC initialize on power up
ER BTW H	E66-13 Sheet 8	Error in byte(s) to be written
ER H BYT L	E66-11 Sheet 8	Error in high byte of word requested on a read cycle
ER L BYT L	E66-12 Sheet 8	Error in low byte of word requested on a read cycle
ER SIG H	E105-3 Sheet 8	Error signal
INH U4 L	E113-15 Sheet 5	Inhibit upper 4K of memory, I/O page is addressed
INT BUS CAS TIM L	E1-6 Sheet 1	Column address select time
INT BUS CS TIM L	E75-8 Sheet 1	Chip select
INT BUS RAS TIM L	E1-4 Sheet 1	Row address select time
MA16 H	E20-2 Sheet 5	Modified address bit 16
MBSY L	E117-11 Sheet 1	Memory busy
MDR TIM 0 L	E2-3 Sheet 13	Clock byte 0 data from array or data latches into MDR
MEM GO L	E117-9 Sheet 1	Initiate memory cycle
OVFLW L	E123-5 Sheet 5	Overflow signal at end of ECC INIT

REF REQ H	E110-12 Sheet 3	Refresh request
REF SRT L	E103-8 Sheet 3	Reset refresh timing
RFCY (1) H	E106-9 Sheet 3	Refresh cycle in progress
RST REF L	E128-8 Sheet 3	Reset Refresh cycle flip-flop
RMW WR H	E96-5 Sheet 13	Write portion of read-modify-write
SERR H	E76-2 Sheet 8	Single error
ST DB ERR H	E86-3 Sheet 9	Strobe if double error is present
ST ECC INIT H	E127-3 Sheet 3	Start ECC initialization cycle
SYN 32 H	E46-3 Sheet 7	Syndrome bit 32
TIM RMW H	E104-5 Sheet 2	Read-modify-write timing start
WRT CK H	E127-6 Sheet 10	Clock when writing data from Unibus into CSR
B.2 ARRAY MODULE		
DR DIS H	E48-8 Sheet 1	Inhibit enable data bit outputs from array to internal memory bus
FNGP1 L	Sheet 1	Signifies a fully populated array card with 4K chips (not used in MF11S-K)
RAS LA	E90-4 Sheet 2	Row address select MOS RAM, row A

APPENDIX C

SIGNAL NAMES WITH PIN LISTS

Table C-1 Internal Memory Bus Signals

Signal Name	Array Module Pin	Control Module Pin	Definition
DB00 RDL	BJ2	BJ2	32 data lines for the four read bytes.
DB01 RDL	BK2	BK2	
DB02 RDL	BJ1	BJ1	
DB03 RDL	BF2	BF2	
DB04 RDL	BR2	BR2	
DB05 RDL	BR1	BR1	
DB06 RDL	BP2	BP2	
DB07 RDL	BP1	BP1	
DB08 RDL	AF1	AF1	
DB09 RDL	AD1	AD1	
DB10 RDL	AB1	AB1	
DB11 RDL	AA1	AA1	
DB12 RDL	AU2	AU1	
DB13 RDL	AT2	AT1	
DB14 RDL	AR2	AR1	
DB15 RDL	AN1	AN1	
DB16 RDL	BH2	BH2	
DB17 RDL	BH1	BH1	
DB18 RDL	BF1	BF1	
DB19 RDL	BE1	BE1	
DB20 RDL	BU1	BU1	
DB21 RDL	BT2	BT2	
DB22 RDL	BS2	BS2	
DB23 RDL	BS1	BS1	
DB24 RDL	AL1	AL1	
DB25 RDL	AK2	AK2	
DB26 RDL	AJ1	AJ1	
DB27 RDL	AH2	AH2	
DB28 RDL	BD2	BD2	
DB29 RDL	BB2	BB2	
DB30 RDL	BC1	BC1	
DB31 RDL	AP2	AP2	

Table C-1 Internal Memory Bus Signals (Cont)

Signal Name	Array Module Pin	Control Module Pin	Definition
CB1 RDL	BM2	BM2	7 check bit lines for error correction code.
CB2 RDL	BL1	BL1	
CB4 RDL	BL2	BL2	
CB81 RDL	BK1	BK1	
CB16 RDL	BV2	BV2	
CB32 RDL	BV1	BV1	
CBT RDL	BU2	BU2	
AO H	AK1	AK1	6 multiplexed address lines used for row, column and refresh addresses.
A1 H	AH1	AH1	
A2 H	AF2	AF2	
A3 H	AJ2	AJ2	
A4 H	AV1	AV1	
A5 H	AP1	AP1	
WR BYT O H	BE1	BE1	4 write byte select lines. All writing is done on a byte basis.
WR BYT 1 H	BB1	BB1	
WR BYT 2 H	BM1	BA1	
WR BYT 3 H	AV1	AV1	
ADD SEL 1 L		AE2	4 memory select lines Line 1 goes to pin AE2 on the slot dedicated to the first 32K, Line 2 to pin AE2 on the slot dedicated to the second 32K etc.
ADD SEL 2 L		BN1	
ADD SEL 3 L		BN2	
ADD SEL 4 L		BM1	
ADD MEM SEL L	AE2		
REF CY(1) L	AE1	AE1	1 line which overrides the RAS row decode and MEM SEL signals when a refresh cycle takes place.
RAS TIM L	AS2	AS2	1 line for the Row Address Strobe timing.
CAS TIM L	AM1	AM1	1 line for the column Address Strobe timing.
MEM PRES L	BA2	BA2	One line to signal the controller that the addressed slot contains an array module.

Table C-1 Internal Memory Bus Signal (Cont)

Signal Name	Array Module Pin	Control Module Pin	Definition
MOD A14 H MOD A15 H	AD2 AC1	AD2 AC1	2 lines to be decoded for selection of the addressed row of MOS chips on the array module.
DR EN L	AM2	AM2	1 line to enable the tristate data drivers on the array module when data is read from the array.
WR TIM L	AN2	AN2	1 line to enable the WRITE BYTE signals to the array.
CS TIM L	AL2	AL2	1 line to time the chip select signals to the array.

Table C-2 Standard and Modified Unibus Pen Assignments

Pin	Standard Signal	Modified Signal	Pin	Standard Signal	Modified Signal	Pin	Standard Signal	Modified Signal
AA1	INIT L	INIT L	AP1	GROUND	P0*	BH1	A01 L	A01 L
AA2	+5 V	+5 V	AP2	BBSY L	BBSY L	BH2	A00 L	A00 L
AB1	INTR L	INTR L	AR1	GROUND	BAT BACKUP +15 V	BJ1	A03 L	A03 L
AB2	GROUND	TEST POINT	AR2	SACK L	SACK L	BJ2	A02 L	A02 L
AC1	D00 L	D00 L	AS1	GROUND	BAT BACKUP +15 V	BK1	A05 L	A05 L
AC2	GROUND	GROUND	AS2	NPR L	NPR L	BK2	A04 L	A04 L
AD1	D02 L	D02 L	AT1	GROUND	GROUND	BL1	A07 L	A07 L
AD2	D01 L	D01 L	AT2	BR7 L	BR7 L	BL2	A06 L	A06 L
AE1	D04 L	D04 L	AU1	NPG H	+20 V	BM1	A09 L	A09 L
AE2	D03 L	D03 L	AU2	BR6 L	BR6 L	BM2	A08 L	A08 L
AF1	D06 L	D06 L	AV1	BG7 H	+20 V	BN1	A11 L	A11 L
AF2	D05 L	D05 L	AV2	GROUND	+20 V	BN2	A10 L	A10 L
AH1	D08 L	D08 L	BA1	BG6 H	SPARE	BP1	A13 L	A13 L
AH2	D07 L	D07 L	BA2	+5 V	+5 V	BP2	A12 L	A12 L
AJ1	D10 L	D10 L	BB1	BG5 H	SPARE	BR1	A15 L	A15 L
AJ2	D09 L	D09 L	BB2	GROUND	TEST POINT	BR2	A14 L	A14 L
AK1	D12 L	D12 L	BC1	BR5 L	BR5 L	BS1	A17 L	A17 L
AK2	D11 L	D11 L	BC2	GROUND	GROUND	BS2	A16 L	A16 L
AL1	D14 L	D14 L	BD1	GROUND	BAT BACKUP +5 V	BT1	GROUND	GROUND
AL2	D13 L	D13 L	BD2	BR4 L	BR4 L	BT2	C1 L	C1 L
AM1	PA L	PA L	BE1	GROUND	INT SSYN*	BU1	SSYN L	SSYN L
AM2	D15 L	D15 L	BE2	BG4 H	PAR: DET*	BU2	C0 L	C0 L
AN1	GROUND	P1*	BF1	ACLO L	ACLO L	BV1	MSYN L	MSYN L
AN2	PB L	PB L	BF2	DCLO L	DCLO L	BV2	GROUND	-5 V

*Pins used by parity control module.

Table C-3 Array Module Pin List

Pin	Signal Name	Pin	Signal Name
AA1	DB11 RD L	BE1	WR BYTE 0 H
AA2	+5 V	BE2	DB19 RD L
AB1	DB10 RD L	BF1	DB18 RD L
AB2	MEM PRES L	BF2	DB03 RD L
AC1	MODA 15 H	BH1	DB17 RD L
AC2	GND	BH2	DB16 RD L
AD1	DB09 RD L	BJ1	DB02 RD L
AD2	MODA 14 H	BJ2	DB00 RD L
AE1	REFCY (1) L	BK1	CB8 RD L
AE2	ADD MEM SEL L	BK2	DB01 RD L
AF1	DB08 RD L	BL1	CB2 RD L
AF2	A2 H	BL2	CB4 RD L
AH1	A1 H	BM1	WR BYTE 2 H
AH2	DB17 RD L	BM2	CB 1 RD L
AJ1	DB26 RD L		
AJ2	A3 H	BP1	DB07 RD L
AK1	A0 H	BP2	DB06 RD L
AK2	DB25 RD L	BR1	DB05 RD L
AL1	DB24 RD L	BR2	DB04 RD L
AL2	CS TIM L	BS1	DB23 RD L
AM1	CAS TIM L	BS2	DB22 RD L
AM2	DR EN L	BT1	GND
AN1	DB 15 RD L	BT2	DB21 RD L
AN2	WR TIM L	BU1	DB20 RD L
AP1	A5 H	BU2	CBT RD L
AP2	DB31 RD L	BV1	CB32 RD L
AR1	+12 BAT	BV2	CB16 RD L
AR2	DB14 RD L	CA1	NPG S0
AS1	-12 BAT	CB1	NPG OUT
AS2	RAS TIM L	CC2	-5 V ZENER GND
AT1	GND	CE1	-5 V TP
AT2	DB13 RD L	CK1	FNGP 1 L
AU1	+12 BAT	CV1	BUS AC LO
AU2	DB12 RD L	DA2	+5 V
AV1	WR BYT 3 H	DK2	BG7 S0
AV2	A 4 H	DL2	BG7 OUT
BB1	WR BYTE 1 H	DM2	BG6 S0
BB2	DB29 RD L	DN2	BG5 OUT
BC1	DB30 RD L	DP2	BG5 S0
BC2	GND	DR2	BG5 OUT
BD1	+5 BAT	DS2	BG4 S0
BD2	DB28 RD L	DT2	BG4 OUT

Table C-4 Control Module Pin List

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
AA1	DB11 RD L	BH1	DB 17 RD L	CT2	D 03 L
AA2	+5 V	BH2	DB 16 RD L	CU1	D 02 L
AB1	DB10 RD L	BJ1	DB 02 RD L	CV1	D 06 L
AB2	MEM PRES L	BJ2	DB 00 RD L	DA2	+5 V
AC1	MODA 15 H	BK1	CB8 RD L	DC2	GND
AC2	GND	BK2	DB 01 RD L	DK2	BG 7 S0
AD1	DB09 RD L	BL1	CB2 RD L	DL1	INIT L
AD2	MOD A 14 H	BL2	CBL RD L	DL2	BG 7 OUT
AE1	REF CYC (1) L	BM1	ADD MEM SEL 4 L	DM2	BG 6 S0
AE2	ADD MEM SEL 1 L	BM2	CB1 RD L	DN2	BG 6 OUT
AF1	DB08 RD L	BN1	ADD MEM SEL 2 L	DP2	BG 5 S0
AF2	A2 H	BN2	ADD MEM SEL 3 L	DR2	BG 5 OUT
AH1	A1 H	BP1	DB 07 RD L	DS1	REF LOW TP
AH2	DB27 RD L	BP2	DB 06 RD L	DS2	BG 4 S0
AJ1	DB26 RD L	BR1	DB 05 RD L	DT1	GND
AJ2	A3 H	BR2	DB 04 RD L	DT2	BG4 OUT
AK1	A0 H	BS1	DB 23 RD L	EA2	+5 V
AK2	DB25 RD L	BS2	DB 22 RD L	EC1	A12 L
AL1	DB24 RD L	BT1	GND	EC2	GND
AL2	CS TIM L	BT2	DB 21 RD L	ED1	A17 L
AM1	CAS TIM L	BU1	DB 20 RD L	ED2	A15 L
AM2	DR EN L	BU2	CBT RD L	EE1	MSYN L
AN1	DB15 RD L	BV1	CB32 RD L	EE2	A16 L
AN2	WR TIM L	BV2	CB16 RD L	EF1	A02 L
AP1	A5 H	CA1	NPG S0	EF2	C1 L
AP2	DB31 RD L	CA2	5 V	EH1	A01 L
AR2	DB14 RD L	CB1	NPG OUT	EH2	A00 L
AS2	RAS TIM L	CC2	GND	EJ1	SSYN L
AT1	GND	CD2	D 15 L	EJ2	CO L
AT2	DB13 RD L	CE2	D 14 L	EK1	A14 L
AU2	DB12 RD L	CE2	D 13 L	EK2	A13 L
AV1	WR BYTE 3 H	CA1	D 11 L	EL1	A11 L
AV2	A4 H	CH2	D 12 L	EN2	A08 L
BA1	WR BYTE 2 H	CJ2	D 10 L	EP1	A10 L
BA2	5 V	CK2	D 09 L	EP2	A07 L
BB1	WR BYTE 1 H	CL2	D 08 L	ER1	A09 L
BB2	DB 29 RD L	CM2	D 07 L	ET1	GND
BC1	DB 30 RD L	CN1	DC LO	EU1	A06 L
BC2	GND	CN2	D 04 L	EU2	A04 L
BD1	+5 V BAT	CP2	D 05 L	EV1	A05 L
BD2	DB 28 RD L	CR2	D 01 L	EV2	A03 L
BE1	WR BYTE 0 H	CS1	PB L	FA1	+5 V
BE2	DB 19 RD L	CS2	D 00 L	FC2	GND
BF1	DB 18 RD L	CT1	GND	FT1	GND
BF2	DB 03 RD L				

Reader's Comments

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgment is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

What features are most useful? _____

What faults or errors have you found in the manual? _____

Does this manual satisfy the need you think it was intended to satisfy? _____

Does it satisfy *your* needs? _____ Why? _____

☐ Please send me the current copy of the *Technical Documentation Catalog*, which contains information on the remainder of DIGITAL's technical documentation.

Name _____	Street _____
Title _____	City _____
Company _____	State/Country _____
Department _____	Zip _____

Additional copies of this document are available from:

Digital Equipment Corporation
444 Whitney Street
Northboro, Ma 01532
Attention: Communications Services (NR2/M15)
Customer Services Section

Order No. _____

Please cut along this line.

Fold Here

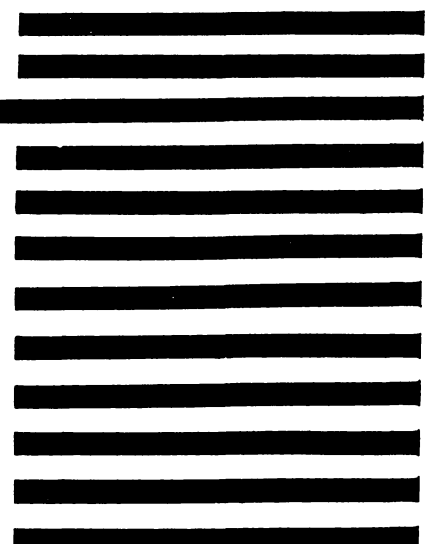
Do Not Tear - Fold Here and Staple

**FIRST CLASS
PERMIT NO. 33
MAYNARD, MASS.**

**BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF MAILED IN THE UNITED STATES**

Postage will be paid by:

**Digital Equipment Corporation
Technical Documentation Department
Maynard, Massachusetts 01754**



digital

digital equipment corporation

Printed in U.S.A.