

DMP-11,  
DMR11, M8207

M8207 STATIC DIAG  
CZDMQEO

AH-E229E-MC  
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MAY 1983  
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The main body of the document is a large grid of approximately 15 columns and 25 rows of small, dense text. Each cell in the grid contains a small diagram or data block, likely representing a static diagnostic for a specific component or circuit. The text is too small to be legible, but the layout is highly structured and repetitive.

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IDENTIFICATION  
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PRODUCT CODE: AC-E228E-MC  
PRODUCT NAME: CZDMQEO MB207 STATIC DIAG #2  
PRODUCT DATE: OCTOBER 1982  
MAINTAINER: DIAGNOSTICS MERRIMACK  
AUTHOR: ED BADGER

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## 1.0 INTRODUCTION

### 1.1 PROGRAM ABSTRACT

THIS DIAGNOSTIC WAS DESIGNED TO TEST OUT THE M8200, M8204, OR M8207 MICROPROCESSOR. IT IS THE SECOND OF TWO DIAGNOSTICS FOR THESE OPTIONS.

THE PROGRAM WAS IMPLEMENTED USING THE DIAGNOSTIC SUPERVISOR.

THROUGH DIALOGUE WITH THE OPERATOR, THE PROGRAM WILL ALLOW MODIFICATION OF DEVICE PARAMETERS, SUCH AS UNIBUS ADDRESS, VECTOR ADDRESS, AND PROCESSOR TYPE.

### 1.2 REVISION HISTORY

THIS DIAGNOSTIC WAS REVISED FOR THE FOLLOWING REASONS

- REV A - ORIGINAL RELEASE
- REV B - CORRECT AN ERROR TYPEOUT IN TEST 26, CORRECT TIME DEPENDENT CODE IN TEST 20, CORRECT MACHINE DEPENDENT CODE IN TEST 37
- REV C - FIX NECESSARY FOR DMP MICROCODE CHANGE. MICROCODE CHANGE CAUSED TEST 43 TO FAIL
- REV D - NEW MICROCODE CAUSED ERRONEOUS DATA TO REMAIN IN HIGH BYTE OF R5 IN TEST 40.
- REV E - CHANGED TEST 26 AT THE REQUEST OF MANUFACTURING. THIS CHANGE WILL ALLOW TESTING OF BITS 4 AND 5 IN IBUS\*(<13> (PC BITS 12 AND 13). THE DIAGNOSTIC ORIGINALLY ONLY TESTED A 12 BIT PC. THIS DID NOT EFFECT THE DMR; HOWEVER THE DMP-YA DOES USE A 14 BIT PC. THE CHANGE WAS PROPOSED BY MARTY DIMUZIO OF AUGUSTA MANUF.

### 1.3 HARDWARE INTRODUCTION

THE M820X MICROPROCESSOR USES AN EIGHT BIT DATA PATH WITH A SIXTEEN BIT INSTRUCTION MEMORY. THE INSTRUCTION MEMORY AND DATA MEMORY ARE TWO SEPARATE MEMORIES. THE MICROPROCESSOR IS DESIGNED FOR MOVING DATA AT HIGH RATES TO WORK AS A HIGH SPEED LINK BETWEEN PROCESSORS WHEN USED WITH A LINE UNIT. THE M8200 AND M8207 HAVE PROM INSTRUCTION MEMORIES. THE M8204 HAS WRITEABLE CONTROL STORE. THE MEMORY SIZES BETWEEN ALL THREE PROCESSORS VARY ALSO.

## 2.0 HARDWARE REQUIREMENTS

THE FOLLOWING HARDWARE IS REQUIRED TO RUN THE M8207 LOGIC TESTS:

PDP-11/04,05,10,20,30,34,35,40,45,50,60, OR 70  
16K MEMORY  
CONSOLE TERMINAL

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### 3.0 PRELIMINARY PROGRAM REQUIREMENTS

THE PROCESSOR AND MEMORY SHOULD BE THOROUGHLY TESTED PRIOR TO RUNNING THIS DIAGNOSTIC.

### 4.0 GENERAL PROGRAM CONSIDERATIONS

#### 4.1 DIAGNOSTIC SUPERVISOR

THIS PROGRAM IS COMPATIBLE WITH THE STANDALONE DIAGNOSTIC SUPERVISOR, AND MUST BE LOADED TO BE CO-RESIDENT WITH THE SUPERVISOR, OR BE PREVIOUSLY COMBINED WITH THE SUPERVISOR AND LOADED AS A SINGLE FILE. IN EITHER CASE, THE COMBINED PROGRAM WILL NOT EXCEED 16K OF MEMORY.

#### 4.2 EXECUTION TIME

THE TOTAL TIME REQUIRED TO RUN THE M8207 STATIC TESTS IS ABOUT 120 SECONDS PER PASS FOR EACH UNIT.

#### 4.3 XXDP+

THIS PROGRAM MAY BE LOADED UNDER XXDP+, AND MAY BE RUN IN DUMP MODE OR CHAIN MODE.

#### 4.4 ACT/SLIDE

THIS PROGRAM MAY BE LOADED UNDER ACT OR SLIDE AND MAY BE RUN IN DUMP MODE OR CHAIN MODE.

#### 4.5 APT

THIS PROGRAM MAY BE LOADED BY THE APT SYSTEM (INCLUDING APT-RD) AND RUN IN PROGRAM MODE OR SCRIPT MODE.

#### 4.6 MEMORY MANAGEMENT

MEMORY MANAGEMENT IS NOT UTILIZED IN THIS PROGRAM. IF IT IS INSTALLED, IT IS DISABLED BY THE PROGRAM.

#### 4.7 MEMORY PARITY OPTION

IF PARITY MEMORY IS INSTALLED, MEMORY PARITY TRAPS ARE DISABLED BY THE PROGRAM.

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#### 4.8 ERROR LOGGING

THE NUMBER OF ERRORS WHICH HAVE OCCURRED ON EACH DEVICE UNDER TEST SINCE THE LAST START OR RESTART COMMAND IS KEPT IN AN ERROR LOG. THIS LOG MAY BE PRINTED BY USING THE "PRINT" COMMAND (SEE SECTION 6.3.8).

#### 5.0 PROGRAM LOAD MEDIA

THIS PROGRAM CAN BE LOADED FROM PAPER TAPE USING THE ABSOLUTE LOADER OR FROM ACT, SLIDE, OR APT SYSTEMS, OR FROM ANY MEDIA SUPPORTED BY XXDP+. WHEN USING THE PAPER TAPE ABSOLUTE LOADER, THE PROGRAM SHOULD BE LOADED FIRST, FOLLOWED BY THE DIAGNOSTIC SUPERVISOR. WHEN USING XXDP+, THE DIAGNOSTIC SUPERVISOR SHOULD BE LOADED FIRST, FOLLOWED BY THE DIAGNOSTIC PROGRAM.

#### 6.0 OPERATING INSTRUCTIONS

##### 6.1 LOADING AND STARTING PROCEDURES

###### 6.1.1 LOADING PROCEDURES

THIS PROGRAM MAY BE LOADED FROM PAPER TAPE USING THE ABSOLUTE LOADER. IT MAY ALSO BE LOADED FROM ANY XXDP+ LOAD MEDIA. WHEN LOADED UNDER XXDP+, THE DIAGNOSTIC SUPERVISOR WILL BE LOADED AUTOMATICALLY.

###### 6.1.2 STARTING PROCEDURES

THE PROGRAM STARTS AT LOCATION 200. USE STANDARD DEC PROCEDURES TO START THE PROGRAM.

###### 6.1.3 STEPS FOR QUICK AND SIMPLE EXECUTION

THE DIAGNOSTIC CAN BE EXECUTED STANDALONE UNDER XXDP+ WITHOUT READING THE REMAINDER OF THIS DOCUMENT, AS FOLLOWS:

- A) LOAD AND START DIAGNOSTIC USING RUN COMMAND
- B) RECEIVE DIAGNOSTIC SUPERVISOR PROMPT (DR>)
- C) ENTER STA<CR>
- D) ANSWER HARDWARE AND SOFTWARE QUESTIONS
- E) GET END OF PASS MESSAGES OR ERROR MESSAGES
- F) TO END EXECUTION, ENTER CONTROL/C

##### 6.2 INITIAL DIALOGUE

AFTER THE PROGRAM AND THE SUPERVISOR ARE LOADED AND THE PROGRAM IS STARTED, THE FOLLOWING IDENTIFICATION IS TYPED:

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DRS LOADED  
DIAG. RUN-TIME SERVICES  
CZDMQ-D-0  
MB207 DIAG. #2 OF 2  
UNIT IS MB200,MB204,OR MB207  
DR>

THE OPERATOR THEN PROCEEDS BY TYPING ONE OR MORE OF THE  
COMMANDS DESCRIBED IN THE FOLLOWING SECTION 6.3.(FOR MORE  
DETAILED INFORMATION, REFER TO THE DIAGNOSTIC SUPERVISOR  
FUNCTIONAL SPECIFICATION).

6.3 PROGRAM OPTIONS

6.3.1 START COMMAND

\*\*\*\*\*  
STA(RT)/TESTS:<TEST-LIST>/PASS:<PASS-CNT>/FLAGS:  
<FLAG-LIST>/EOP:<INCR>  
\*\*\*\*\*

6.3.1.1 TESTS SWITCH (/TESTS:<TEST-LIST>)

<TEST-LIST> IS A SEQUENCE OF DECIMAL NUMBERS (1:2 ETC.) OR  
RANGES OF DECIMAL NUMBERS (1-5:8-10 ETC.) THAT SPECIFY THE  
TESTS TO BE EXECUTED. THE NUMBERS ARE SEPARATED BY COLONS.  
THE NUMBERS RANGE FROM 1 TO THE LARGEST TEST NUMBER IN THE  
DIAGNOSTIC. THEY MAY BE SPECIFIED IN ANY ORDER. TESTS WILL  
BE EXECUTED IN NUMERICAL ORDER REGARDLESS OF THE ORDER OF  
SPECIFICATION. THE DEFAULT IS TO EXECUTE ALL TESTS. ON  
THIS AND ALL SWITCHES, THE ANGLE BRACKETS <> ARE PUNCTUATION  
USED IN THE DEFINITION ONLY, AND ARE NOT TO BE TYPED BY THE  
OPERATOR. SEE EXAMPLE AT END OF 6.3.1.5.

6.3.1.2 PASS SWITCH (/PASS:<PASS-CNT>)

<PASS-CNT> IS A DECIMAL NUMBER INDICATING THE DESIRED NUMBER  
OF PASSES. A PASS IS DEFINED AS THE EXECUTION OF THE FULL  
DIAGNOSTIC (ALL SELECTED TESTS) AGAINST ALL UNITS SUBMITTED.  
THE DEFAULT IS NON-ENDING EXECUTION. IN THIS CASE EXIT FROM  
THE PROGRAM IS ACCOMPLISHED EITHER BY TYPING A CONTROL/C OR  
BY OCCURANCE OF AN ERROR WITH THE HALT ON ERROR FLAG BEING  
SET. THE EXIT IS A RETURN TO COMMAND MODE. SEE EXAMPLE AT  
END OF 6.3.1.5.

6.3.1.3 FLAGS SWITCH (/FLAGS:<FLAG-LIST>)

<FLAG-LIST> IS A SEQUENCE OF ELEMENTS OF THE FORM <FLAG>,  
<FLAG=1>, OR <FLAG=0>, SEPARATED BY COLONS, WHERE <FLAG> HAS  
ONE OF THE FOLLOWING VALUES:

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HOE HALT ON ERROR, CAUSING COMMAND MODE TO BE  
ENTERED WHEN AN ERROR IS ENCOUNTERED  
LOE LOOP ON ERROR, CAUSING THE DIAGNOSTIC TO LOOP  
CONTINUOUSLY WITHIN THE SMALLEST DEFINED BLOCK  
OF CODING (SEGMENT, SUBTEST, OR TEST) CONTAIN-  
ING THE ERROR  
IER INHIBIT ERROR REPORTING  
IBE INHIBIT BASIC ERROR REPORTS  
IXE INHIBIT EXTENDED ERROR REPORTS  
PRI DIRECT ALL MESSAGES TO A LINE PRINTER  
PNT PRINT NUMBER OF TEST BEING EXECUTED  
BOE BELL ON ERROR  
UAM RUN IN UNATTENDED MODE, BYPASSING MANUAL  
INTERVENTION TESTS  
ISR INHIBIT STATISTICAL REPORTS  
IDU INHIBIT DROPPING OF UNITS BY DIAGNOSTIC  
LOT LOOP ON TEST

THE FLAGS NAMED OR EQUATED TO 1 ARE SET, THOSE EQUATED TO 0  
ARE CLEARED. A FLAG NOT SPECIFIED IS CLEARED. IF THE FLAGS  
SWITCH IS NOT GIVEN ALL FLAGS ARE CLEARED. SEE EXAMPLE AT  
END OF 6.3.1.5.

#### 6.3.1.4 END OF PASS SWITCH (/EOP:<INCR>)

<INCR> IS A DECIMAL NUMBER INDICATING HOW OFTEN (IN TERMS OF  
PASSES) IT IS DESIRED THAT THE END OF PASS MESSAGE BE  
PRINTED. THE DEFAULT IS AT THE END OF EVERY PASS. SEE  
EXAMPLE AT END OF 6.3.1.5.

#### 6.3.1.5 EFFECT OF START COMMAND

THE EFFECT OF THE START COMMAND IS TO INITIATE THE HARDWARE  
PARAMETER DIALOGUE, THE SOFTWARE PARAMETER DIALOGUE, AND  
THEN THE DIAGNOSTIC TESTS THEMSELVES.

THE HARDWARE PARAMETER DIALOGUE COMMENCES WITH THE QUESTION  
"# UNITS?" TO WHICH THE OPERATOR REPLIES WITH A DECIMAL  
NUMBER N FROM 1 TO 16. THE TERM "UNIT" REFERS TO THE DEVICE  
TO WHICH THIS SERIES OF DIAGNOSTICS IS DEDICATED. FOLLOWING  
THIS ARE THE QUESTIONS WHEREBY THE P-TABLES THEMSELVES WILL  
BE BUILT. EACH P-TABLE IS A CORE-RESIDENT TABLE CONTAINING  
ALL THE HARDWARE INFORMATION FOR ONE UNIT. THE OPERATOR  
MUST SUPPLY N (NUMBER OF UNITS) VALUES FOR EACH QUESTION.  
HE MAY DO THIS BY GIVING ONE ANSWER TO EACH QUESTION (IN  
WHICH CASE THE SERIES OF QUESTIONS WILL BE POSED N TIMES) OR  
BY GIVING N VALUES, SEPARATED BY COMMAS, TO EACH QUESTION  
(SERIES WILL BE POSED ONCE). EACH QUESTION IS FOLLOWED BY  
THE RESPONSE RADIX (D FOR DECIMAL, B FOR BINARY, O FOR  
OCTAL, L FOR YES/NO) IN PARENTHESES AND THE DEFAULT VALUE  
AFTER THE PARENTHESES.

FOLLOWING THE HARDWARE QUESTIONS ARE THE SOFTWARE QUESTIONS



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TO BUILD THE SOFTWARE TABLES, WHICH DEFINE THE MODE (QUICK VERIFY ETC.) THAT THE DIAGNOSTIC WILL EXECUTE IN.

WHEN THE QUESTION "# UNITS?" IS ANSWERED, MEMORY STORAGE IS ALLOCATED FOR THE P-TABLES, AND IF THERE IS NOT ENOUGH TO ACCOMMODATE THEM THE MESSAGE "TOO MANY UNITS" IS ISSUED. IN THIS CASE THE DIAGNOSTIC MUST BE EXECUTED MORE THAN ONCE TO TEST ALL UNITS.

EXAMPLE:

STA/TESTS:1:2-4:6:8-10/PASS:3/FLAGS:IER:HOE=1:UAM:LOE

THIS COMMAND WILL CAUSE THREE PASSES TO BE MADE, EACH PASS CONSISTING OF TESTS 1,2,3,4,6,8,9, AND 10 EXECUTED AGAINST ALL UNITS. THERE IS NO DIFFERENCE BETWEEN SAYING <FLAG> AND SAYING <FLAG=1>. THE NOTATION <FLAG=0> IS MEANINGFUL ONLY ON A COMMAND OTHER THAN START TO CLEAR A FLAG THAT WAS PREVIOUSLY SET. NOTE THAT ON ALL COMMANDS ONLY THE FIRST THREE LETTERS ARE SCANNED.

### 6.3.2 RESTART COMMAND

```
*****  
RES(TART)/TESTS:<TEST-LIST>/PASS:<PASS-CNT>/FLAGS:  
  <FLAG-LIST>/UNITS:<UNIT-LIST>  
*****
```

#### 6.3.2.1 TESTS, PASS, AND FLAGS SWITCHES

<TEST-LIST>, <PASS-CNT>, AND <FLAG-LIST> ARE AS IN THE START COMMAND.

#### 6.3.2.2 UNITS SWITCH (/UNITS:<UNIT-LIST>)

<UNIT-LIST> IS A SEQUENCE OF DECIMAL NUMBERS (0,1 ETC.) OR RANGES OF DECIMAL NUMBERS (0-5, 8-10 ETC.) THAT SPECIFY THE UNITS TO BE TESTED. THE NUMBERS ARE SEPARATED BY COLONS. THE NUMBERS MAY RANGE FROM 0 THRU N-1 (N IS THE NUMBER OF UNITS SPECIFIED IN THE PREVIOUS START COMMAND). THE NUMBER INDICATES THE POSITION OF THE P-TABLE AS THE DATA WAS ENTERED DURING THE HARDWARE DIAGLOGUE. THE UNITS WHICH ARE SELECTED MUST NOT HAVE BEEN DROPPED BY THE DROP COMMAND. SEE THE DISCUSSION OF ADD AND DROP COMMANDS BELOW. DEFAULT IS TO TEST ALL UNITS WHICH HAVE NOT BEEN DROPPED BY A DROP COMMAND.

#### 6.3.2.3 EFFECT OF RESTART COMMAND

THE RESTART COMMAND DIFFERS FROM THE START COMMAND IN THAT THE P-TABLES FROM THE PREVIOUS START COMMAND (THERE MUST HAVE BEEN ONE) ARE USED, INSTEAD OF NEW ONES BEING BUILT.

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THE UNITS SWITCH GIVES THE ABILITY TO SELECT A SUBSET OF THESE. THE SOFTWARE DIALOGUE MAY OPTIONALLY BE REEXECUTED (OPERATOR WILL BE ASKED). THE COMMAND CAN BE USED AFTER COMMAND MODE HAS BEEN REENTERED IN ANY OF THE THREE NORMAL WAYS: A) THE REQUESTED NUMBER OF PASSES HAVE BEEN MADE. B) AN ERROR WAS ENCOUNTERED WITH THE HALT ON ERROR FLAG SET. C) A CONTROL/C WAS ENTERED BY THE OPERATOR.

6.3.3 CONTINUE COMMAND

\*\*\*\*\*  
CON(TINUE)/PASS:<PASS-CNT/FLAGS:<FLAG-LIST>  
\*\*\*\*\*

6.3.3.1 PASS SWITCH (/PASS:<PASS-CNT>)

<PASS-CNT> IS SAME AS IN START COMMAND, BUT THE DEFAULT IS THE UNSATISFIED PASS-CNT FROM THE PREVIOUS START OR RESTART. IF NONE REMAINS, THE DEFAULT IS NON-ENDING EXECUTION.

6.3.3.2 FLAG SWITCH (/FLAGS:<FLAG-LIST>)

<FLAG-LIST> IS SAME AS IN START COMMAND, BUT UNSPECIFIED FLAGS RETAIN THEIR CURRENT VALUE.

6.3.3.3 EFFECT OF CONTINUE COMMAND

CONTINUE MUST FOLLOW A START OR RESTART, AND COMMAND MODE MUST HAVE BEEN ENTERED DUE TO A HALT ON ERROR OR A CONTROL/C. THE EFFECT OF THE COMMAND IS TO GO TO THE BEGINNING OF THE TEST THAT WAS BEING EXECUTED WHEN THE HALT OR CONTROL/C TOOK PLACE. SOFTWARE DIALOGUE MAY OPTIONALLY BE REEXECUTED. HARDWARE PARAMETERS MAY NOT BE CHANGED.

6.3.4 PROCEED COMMAND

\*\*\*\*\*  
PRO(CEED)/FLAGS:<FLAG-LIST>  
\*\*\*\*\*

6.3.4.1 FLAGS SWITCH (/FLAGS:<FLAG-LIST>)

<FLAG-LIST> IS AS IN THE START COMMAND, BUT UNSPECIFIED FLAGS RETAIN THEIR CURRENT VALUE.

6.3.4.2 EFFECT OF PROCEED COMMAND

PROCEED MUST FOLLOW A START, RESTART, OR CONTINUE. COMMAND MODE MUST HAVE BEEN ENTERED VIA A HALT ON ERROR. THE EFFECT OF THE COMMAND IS TO BEGIN EXECUTION AT THE LOCATION

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FOLLOWING THE ERROR CALL. NEITHER HARDWARE NOR SOFTWARE  
PARAMETERS MAY BE ALTERED.

6.3.5 ADD COMMAND

\*\*\*\*\*  
ADD/UNITS:<UNIT-LIST>  
\*\*\*\*\*

6.3.5.1 UNITS SWITCH (/UNITS:<UNIT-LIST>

<UNIT-LIST> IS AS IN THE RESTART COMMAND.

6.3.5.2 EFFECT OF ADD COMMAND

THE UNITS SPECIFIED ARE ADDED TO THE TEST SEQUENCE. EACH  
UNIT MUST HAVE A P-TABLE IN MEMORY DUE TO AN EARLIER  
HARDWARE DIALOGUE. THIS COMMAND MUST BE FOLLOWED BY A  
RESTART OR CONTINUE. THE UNITS SWITCH MUST BE SPECIFIED.  
THE ADD COMMAND IS MEANINGFUL ONLY FOR UNITS THAT WERE  
PREVIOUSLY DROPPED.

6.3.6 DROP COMMAND

\*\*\*\*\*  
DRO(P)/UNITS:<UNIT-LIST>  
\*\*\*\*\*

6.3.6.1 UNITS SWITCH (/UNITS:<UNIT-LIST>)

<UNIT-LIST> IS AS IN THE RESTART COMMAND.

6.3.6.2 EFFECT OF DROP COMMAND

THE UNITS SPECIFIED WILL BE DROPPED FROM TESTING. THE UNITS  
WILL BE RESELECTED ONLY BY THE EXECUTION OF AN ADD OR START  
COMMAND. THE UNITS SWITCH MUST BE ENTERED. THIS COMMAND  
MUST BE FOLLOWED BY A RESTART OR A CONTINUE COMMAND.

6.3.7 PRINT COMMAND

\*\*\*\*\*  
PRI(NT)  
\*\*\*\*\*

6.3.7.1 EFFECT OF PRINT COMMAND

THE TOTAL NUMBER OF ERRORS FOR EACH UNIT SINCE THE LAST

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START OR RESTART COMMAND ARE PRINTED. THE ISR (INHIBIT STATISTICAL REPORTING) FLAG IS CLEARED.

6.3.8 DISPLAY COMMAND

\*\*\*\*\*  
DIS(PLAY)/UNITS:<UNIT-LIST>  
\*\*\*\*\*

6.3.8.1 UNITS SWITCH (/UNITS:<UNIT-LIST>)

<UNIT-LIST> IS AS IN THE RESTART COMMAND.

6.3.8.2 EFFECT OF DISPLAY COMMAND

THE HARDWARE P-TABLES FOR ALL UNITS UNDER TEST ARE PRINTED OUT IN THE FORMAT IN WHICH THEY WERE ENTERED. ANY UNITS THAT WERE DROPPED BY THE OPERATOR "DROP" COMMAND ARE SO DESIGNATED.

6.3.9 FLAGS COMMAND

\*\*\*\*\*  
FLA(GS)  
\*\*\*\*\*

6.3.9.1 EFFECT OF FLAGS COMMAND

THE CURRENT SETTINGS OF ALL FLAGS ARE PRINTED.

6.3.10 ZFLAGS COMMAND

\*\*\*\*\*  
ZFL(AGS)  
\*\*\*\*\*

6.3.10.1 EFFECT OF ZFLAG COMMAND

ALL FLAGS ARE CLEARED.

6.3.11 CONTROL CHARACTERS

A CONTROL C (C) ENTERED DURING THE EXECUTION OF A DIAGNOSTIC CAUSES A RETURN TO COMMAND MODE.

A CONTROL Z (Z) ENTERED DURING ONE OF THE THREE OPERATOR DIALOGUES- INITIAL DIALOGUE (SEE 6.2), HARDWARE DIALOGUE (SEE 6.3.1.5), OR SOFTWARE DIALOGUE (SEE 6.3.1.5) CAUSES THE

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DEFAULTS TO BE TAKEN FOR THE REMAINDER OF THAT DIALOGUE.

A CONTROL O (O) ENTERED DURING THE EXECUTION OF A DIAGNOSTIC CAUSES ALL TELETYPE OUTPUT TO BE SURPRESSED FOR THE REM' DER OF THE DIAGNOSTIC OR UNTIL ANOTHER O IS TYPED, WHICH RESTORES NORMAL TELETYPE OUTPUT.

### 6.3.12 HARDWARE PARAMETERS

THE FOLLOWING QUESTIONS WILL BE ASKED ON A START COMMAND. THE VALUE LOCATED TO THE LEFT OF THE QUESTION MARK IS THE DEFAULT VALUE THAT WILL BE TAKEN ON A CARRIAGE RETURN RESPONSE.

1. WHICH MICRO-CPU? (0= M8200, 4= M8204, 7= M8207) (0) 7?

2. MICRO-CPU CSR ADDRESS: (0) 160170?

THIS IS THE ADDRESS AT WHICH THE CSR REGISTERS (SEI 0) RESIDE ON THE UNIBUS. THE ALLOWABLE RANGE IS 160000-177776 (OCTAL), AND THE DEFAULT IS 160170.

3. MICRO-PROCESSOR RUN SWITCH-TYPE 1 IF ON, IF OFF: (0) 0?

THE RUN SWITCH IS E28, SWITCH 7 ON THE M8207. MORE TESTS CAN BE PERFORMED IF THE RUN SWITCH IS OFF. YOU MAY GENERATE AN ERROR IF YOU ANSWER THIS QUESTION WRONG.

### 6.3.13 SOFTWARE PARAMETERS

NO SOFTWARE PARAMETER QUESTIONS ARE ASKED BY PART 2 OF THE STATIC LOGIC TESTS.

### 6.3.14 EXTENDED DISCUSSION OF P-TABLE DIALOGUE

THE FULL CAPABILITY OF THE HARDWARE DIALOGUE IS REVEALED BY THE FOLLOWING DISCUSSION OF WHAT HAPPENS INTERNALLY.

AS SOON AS THE QUESTION "# UNITS?" IS ANSWERED (WITH THE NUMBER N, SAY) SPACE IN CORE IS ALLOCATED FOR N P-TABLES. ALL OF THE P-TABLES ARE OF THE SAME FORMAT, AND THERE IS A ONE-TO ONE CORRESPONDENCE BETWEEN THE HARDWARE PARAMETER QUESTIONS AND THE SLOTS IN THE P-TABLE FORMAT.

ON THE FIRST TRIP THRU THE QUESTIONS, ALL OF THE SLOTS IN ALL OF THE P-TABLES ARE FILLED. IF THE OPERATOR TYPES IN LESS THAN N EXPLICIT VALUES IN RESPONSE TO A PARTICULAR QUESTION, THESE VALUES ARE PLACED IN THE P-TABLES (ONE VALUE GOING INTO THE PROPER SLOT OF EACH P-TABLE BEGINNING WITH THE FIRST P-TABLE) UNTIL THE STRING OF VALUES IS EXHAUSTED.

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THE LAST VALUE IN THE STRING BECOMES THE NEW DEFAULT AND IS USED TO FILL THAT SLOT IN THE REMAINING P-TABLES.

ON SUBSEQUENT TRIPS THRU THE QUESTIONS, THE SAME PROCESS IS CARRIED OUT, EXCEPT THAT THE EARLIEST P-TABLE NOT TO HAVE RECEIVED AN EXPLICIT VALUE IN ANY OF ITS SLOTS NOW ASSUMES THE ROLE THAT TABLE NUMBER ONE PLAYED IN THE FIRST TRIP.

THE SERIES OF QUESTIONS IS REISSUED UNTIL AT LEAST ONE QUESTION HAS RECEIVED N EXPLICIT VALUES FROM THE OPERATOR.

IN GIVING A STRING OF VALUES, COMMAS WITHOUT INTERVENING VALUES MAY BE USED TO INDICATE A REPETITION OF THE LAST NAMED VALUE.

A STRING OF VALUES MAY BE GIVEN AS A RANGE (6-10 FOR EXAMPLE). IF THE VALUES REPRESENT PURE NUMERICAL DATA, THIS SAMPLE RANGE TRANSLATES TO THE STRING 6,7,8,9,10 (AN INCREMENT OF 1). IF THE VALUES ARE ADDRESSES, THE SAMPLE RANGE TRANSLATES TO THE STRING 6,8,10 (AN INCREMENT OF 2).

NOW LET US SEE HOW WE COULD USE THESE CAPABILITIES TO CONSTRUCT A SET OF P-TABLES. ASSUME THAT WE HAVE 16 UNITS, AND THAT THERE ARE THREE HARDWARE PARAMETERS FOR EACH (THREE SLOTS IN THE P-TABLE, THREE HARDWARE QUESTIONS IN THE DIALOGUE). LET THE DESIRED VALUE FOR THE FIRST PARAMETER BE THE NUMBER 75 FOR ALL 16 TABLES. LET THE DESIRED VALUE FOR THE SECOND PARAMETER BE EQUAL TO THE UNIT NUMBER (0,1,2,...,15) EXCEPT FOR UNIT 12, WHICH SHOULD RECEIVE THE VALUE 11. LET THE DESIRED VALUE FOR THE THIRD PARAMETER BE THE NUMBER 76 FOR THE FIRST 7 UNITS AND THE NUMBER 77 FOR THE LAST 9 UNITS.

THE FOLLOWING DIALOGUE WOULD ACCOMPLISH THIS GOAL:

# UNITS (D) ? 16

UNIT 1  
<QUESTION 1> ? 75  
<QUESTION 2> ? 0-6  
<QUESTION 3> ? 76

UNIT 21  
<QUESTION 1> ?  
<QUESTION 2> ? 7-11,,13-15  
<QUESTION 3> ? 77

THE FIRST TIME THE SERIES IS ASKED, SLOT ONE RECEIVES A 75 IN ALL 16 TABLES. SLOT TWO RECEIVES THE VALUES 0,1,2,...,6 IN TABLES 0 THRU 6 AND A CONSTANT 6 IN TABLES 7 THRU 15. SLOT THREE RECEIVES A CONSTANT 76 IN ALL 16 TABLES.

THE SECOND TIME THRU THE SERIES, TABLES 16 THRU THE END ARE GOING TO BE AFFECTED (NOTE THAT THIS PIECE OF INFORMATION IS PRINTED OUT FOR THE OPERATOR IN THE FORM "UNIT xx" AT THE BEGINNING OF EACH SERIES). QUESTION 1 IS RESPONDED TO

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BY A <CR>, SO SLOT ONE STAYS AT CONSTANT 75 IN TABLES 7 THRU 15, SINCE NO NEW EXPLICIT VALUES ARE TYPED IN. SLOT TWO GETS THE VALUES 7,8,9,10,11 IN TABLES 7 THRU 11, AND GETS A 11 IN SLOT 12, AND GETS THE VALUES 13,14,15 IN TABLES 13 THRU 15. SLOT THREE GETS THE VALUE 77 IN TABLES 7 THRU 15.

THE DIALOGUE IS TERMINATED WHEN THE SOFTWARE RECOGNIZES THAT 16 EXPLICIT VALUES HAVE BEEN GIVEN FOR AT LEAST ONE QUESTION (NAMELY QUESTION 2).

7.0 TEST DESCRIPTIONS

\*\*\*\*\* TEST 1 \*\*\*\*\*  
\*VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS  
\*DOES NOT CAUSE A TIME OUT TRAP  
\*\*\*\*\*

\*\*\*\*\* TEST 2 \*\*\*\*\*  
\*TEST OF BR RIGHT SHIFT  
\*VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION  
\*SHIFTS THE RESULTING BR DATA RIGHT ONCE.  
\*\*\*\*\*

\*\*\*\*\* TEST 3 \*\*\*\*\*  
\*IOP CRAM WRITE/READ TEST  
\*FLOAT A 1 THROUGH EACH CRAM LOCATION  
\*\*\*\*\*

\*\*\*\*\* TEST 4 \*\*\*\*\*  
\*IOP CRAM WRITE/READ TEST  
\*FLOAT A 0 THROUGH EACH CRAM LOCATION  
\*\*\*\*\*

\*\*\*\*\* TEST 5 \*\*\*\*\*  
\*IOP CRAM DUAL ADDRESSING TEST  
\*WRITE EACH ADDRESS INTO ITSELF, READ EACH  
\*ADDRESS TO VERIFY CORRECT ADDRESSING  
\*\*\*\*\*

\*\*\*\*\* TEST 6 \*\*\*\*\*  
\*IOP MAIN MEMORY TEST  
\*FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS  
\*\*\*\*\*

\*\*\*\*\* TEST 7 \*\*\*\*\*  
\*IOP MAIN MEMORY TEST  
\*FLOAT A 0 THROUGH ALL MAIN MEMORY LOCATIONS  
\*\*\*\*\*

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\*\*\*\*\* TEST 8 \*\*\*\*\*  
\*IOP MAIN MEMORY DUAL ADDRESSING TEST  
\*LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS  
\*READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING  
\*\*\*\*\*

\*\*\*\*\* TEST 9 \*\*\*\*\*  
\*IOP MAR TEST  
\*PERFORM DUAL ADDRESSING TEST  
\*USING MAR AUTO-INC FEATURE  
\*\*\*\*\*

\*\*\*\*\* TEST 10 \*\*\*\*\*  
\*IOP (CRAM) ODT BITS TEST  
\*LOAD MAR WITH A 0 INC MAR UNTIL IT OVERFLOWS  
\*VERIFY THAT IBUS\* 10 BITS IS SET ONLY WHEN MAR BIT 8 IS A ONE  
\*AND THAT IBUS\* 10 BIT6 IS SET ON MAR OVERFLOW  
\*\*\*\*\*

\*\*\*\*\* TEST 11 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.  
\*PERFORM THE JUMP INSTRUCTION  
\*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE CRAM PC IS CORRECT. IF THE CRAM PC IN NOT RIGHT,  
\*THEN PORT4 CONTAINS A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 12 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.  
\*PERFORM THE JUMP INSTRUCTION  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 13 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.  
\*SET THE C BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATJON IT IS AT. THIS INSTRUCITON LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL



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\*THEN PORT4 WILL CONTAIN A 37.  
\*\*\*\*\*

\*\*\*\*\* TEST 14 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.  
\*SET THE Z BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 15 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BRO SET MICRO-PROCESSOR INSTRUCTION.  
\*SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN THE PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 16 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.  
\*SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 17 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.  
\*SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 18 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.  
\*SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION

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\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 19 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON C BIT CLEAR MICRO-PROCESSOR INSTRUCTION.  
\*SET THE C BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 20 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON Z BIT CLEAR MICRO-PROCESSOR INSTRUCTION.  
\*CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 21 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BRO CLEAR MICRO-PROCESSOR INSTRUCTION.  
\*CLEAR THE BRO BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 22 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BR1 CLEAR MICRO-PROCESSOR INSTRUCTION.  
\*CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
\*THEN PORT4 WILL CONTAIN A 37  
\*\*\*\*\*

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\*\*\*\*\* TEST 23 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BR4 CLEAR MICRO-PROCESSOR INSTRUCTION.  
\*CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT  
\*THEN PORT4 CONTAINS A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 24 \*\*\*\*\*  
\*CRAM TEST OF JUMP(I) ON BR7 CLEAR MICRO-PROCESSOR INSTRUCTION.  
\*CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION.  
\*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
\*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT  
\*THEN PORT4 CONTAINS A 37  
\*\*\*\*\*

\*\*\*\*\* TEST 25 \*\*\*\*\*  
\*  
\*MAIN MEMORY PAGE DUAL ADDRESS TEST.  
\*IN THIS TEST WE WILL VERIFY THAT PAGES DO  
\*NOT DUAL ADDRESS. THIS TEST IS DIFFERENT FROM THE  
\*PREVIOUS DUAL ADDRESS TESTS IN THAT THE OTHER  
\*TEST REALLY DIDN'T CHECK PAGE DUAL ADDRESSING  
\*\*\*\*\*

\*\*\*\*\* TEST 26 \*\*\*\*\*  
\*  
\*JUMP FIELD,PAGE TEST  
\*  
\*IN THIS TEST WE WILL MAKE SURE A JUMP FIELD INSTRUCTION  
\*WORKS. TO DO THIS, WE'LL PUT THE DESIRED PAGE, FIELD  
\*INFORMATION IN IBUS<13> THEN ISSUE A JUMP FIELD  
\*THEN WE'LL READ PC REG. AND VERIFY.  
\* REV. E - CHANGE TO TEST BITS 4 & 5 (PC BITS 12 & 13)  
\*  
\*\*\*\*\*

\*\*\*\*\* TEST 27 \*\*\*\*\*  
\*  
\*JUMP TEST, JUMP ALWAYS, JUMP CHANGE FIELD  
\*  
\*IN THIS TEST, WE WILL CHECK THE ABILITY OF THE  
\*MICRO-PROCESSOR TO JUMP (BRANCH AND ALWAYS INSTRUCTION)  
\*TO LOCATIONS, FIELDS FROM OTHER LOCATIONS FIELDS.  
\*WE ALREADY KNOW THAT THE BRANCH INSTR WORKS FROM  
\*OTHER TEST. PROCEDURE:

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*      1.  START ADDR 0, FIELD 0
*      2.  **CALCULATE NEW ADDR, FIELD VIA INC.
*      3.  CAUSE JUMP (BRANCH) TO NEW ADDRESS
*      4.  READ PC FROM IBUS*12 AND IBUS*13
*      5.  REPEAT STEP 2-4 256.TIMES
*
*      TO CALCULATE NEW ADDRESS:
*      1.  INC LOW BYTE OF ADDRESS FOR PC ADDRESS 0-7
*      2.  INC LOW BYTE OF N ADDRESS FOR PC ADDRESS 8-11
*          BITS REPRESENTED AS BITS 0-3.  WHEN 0-3 OVERFLOWS,
*          RESTARTS AT ZERO.
*          NET RESULT IS JUMPS FROM:
*          FIELD,PAGE                                LOC
*          0                                           0
*          1                                           1
*          2                                           2
*          3                                           3
*          10                                          7
*          11                                          11
*          :10
*          17                                          377
*.....

```

\*\*\*\*\* TEST 28 \*\*\*\*\*

```

*
*JUMP TEST, JUMP ALWAYS, JUMP CHANGE FIELD
*
*IN THIS TEST, WE WILL CHECK THE ABILITY OF THE
*MICRO-PROCESSOR TO JUMP (BRANCH AND ALWAYS INSTRUCTION)
*TO LOCATIONS, FIELDS FROM OTHER LOCATIONS FIELDS.
*WE ALREADY KNOW THAT THE BRANCH INSTR WORKS FROM
*OTHER TESTS.
*          PROCEDURE:
*      1.  START ADDR 0, FIELD 0
*      2.  **CALCULATE NEW ADDR, FIELD VIA DEC.
*      3.  CAUSE JUMP (BRANCH) TO NEW ADDRESS
*      4.  READ PC FROM IBUS*12 AND IBUS*13
*      5.  REPEAT STEP 2-4 256.TIMES
*
*      TO CALCULATE NEW ADDRESS:
*      1.  DEC LOW BYTE OF ADDRESS FOR PC ADDRESS 0-7
*      2.  DEC LOW BYTE OF N ADDRESS FOR PC ADDRESS 8-11
*          BITS REPRESENTED AS BITS 0-3.  WHEN 0-3 OVERFLOWS,
*          RESTARTS AT ZERO
*          NET RESULT IS JUMPS FROM:
*          FIELD,PAGE                                LOC:
*          0                                           0
*          17                                          377
*          16                                          376
*          15                                          375
*          :10
*          00                                          000
*.....

```

\*\*\*\*\* TEST 29 \*\*\*\*\*

CZDMQE M8207 STATIC DIAG. #2  
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PROGRAM DOCUMENT

1041  
1042  
1043  
1044  
1045  
1046  
1047  
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1051  
1052  
1053  
1054  
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1057  
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1096

\*  
\*IN THIS TEST WE'LL VERIFY THAT THE Z BIT CAN BE READ FROM  
\*IBUS\* <13>. WE ALREADY KNOW THAT THE Z BIT WORKS PROPERLY,  
\*ALL WE WANT TO KNOW HERE IS THAT IT CAN BE READ.  
\*\*\*\*\*

\*\*\*\*\* TEST 30 \*\*\*\*\*

\*  
\*IN THIS TEST WE'LL VERIFY THAT THE C BIT CAN BE READ FROM  
\*IBUS\* <13>. WE ALREADY KNOW THAT THE C BIT WORKS PROPERLY  
\*ALL WE WANT TO KNOW HERE IS THAT IT BE READ.  
\*\*\*\*\*

\*\*\*\*\* TEST 31 \*\*\*\*\*

\*TEST OF PROGRAM CLOCK BIT  
\*DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET  
\*WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS,  
\*AND THEN SETS SOME TIME LATER  
\*\*\*\*\*

\*\*\*\*\* TEST 32 \*\*\*\*\*

\*FORCE POWER FAIL TEST  
\*SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24  
\*GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS  
\*BLOCKED FROM GETTING TO THE M8200,4,7 DURING THE POWER FAIL  
\*\*\*\*\*

\*\*\*\*\* TEST 33 \*\*\*\*\*

\*MICRO-PROCESSOR NOISE TEST  
\*WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN  
\*TO THE IBUS\* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM  
\*THEN GO BACK AND READ THE DATA PATTERNS TO VERIFY THAT  
\*READING AND WRITING OF OTHER LOCATIONS AND REGISTERS  
\*DID NOT CHANGE THE DATA.  
\*\*\*\*\*

\*\*\*\*\* TEST 34 \*\*\*\*\*

\*THIS TEST IS DESIGNED TO MAKE SURE THAT A NODST INSTRUCTION  
\*DOES NOT WRITE INTO PORT B OF THE MULTI PORT RAM.  
\*TO DO THIS, WE'LL PUT A 125 INTO INDAT2, THEN WE'LL PUT A  
\*125 INTO BOTH SP1 AND BR. LAST WE'LL DO A NODST BR, SUBOC, SP1  
\*IF THERE IS A WRITE INTO PORTB, INADT2 WILL CONTAIN A 377  
\*\*\*\*\*

\*\*\*\*\* TEST 35 \*\*\*\*\*

\*  
\*EXTENDED CRAM TEST FOR M8206. IN THIS TEST WE WILL LOAD DATA  
\*THROUGHOUT THE CRAM (TEST DATA IS JUST 4K OF DIAG. CODE) AND

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1097  
1098  
1099  
1100  
1101  
1102  
1103  
1104  
1105  
1106  
1107  
1108  
1109  
1110  
1111  
1112  
1113  
1114  
1115  
1116  
1117  
1118  
1119  
1120  
1121  
1122  
1123  
1124  
1125  
1126  
1127  
1128  
1129  
1130  
1131  
1132  
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1152

\*THEN READ IT BACK AND VERIFY THAT IT IS CORRECT  
\*\*\*\*\*

\*\*\*\*\* TEST 36 \*\*\*\*\*

\*  
\*THIS TEST LOADS MICRO-CODE INTO A M8206 MCPU THEN EXECUTES IT.  
\*THE MICRO-CODE IS DESIGNED TO WRITE ALL ONES INTO THE SEL REGS.  
\*  
\*\*\*\*\*

\*\*\*\*\* TEST 37 \*\*\*\*\*

\*  
\*NEGATIVE ADDRESS TEST.  
\* IN THIS TEST, WE'LL MAKE SURE THAT THE M8207  
\* DOES NOT RESPOND TO AN ADDRESS THAT ISN'T ASSIGNED  
\* TO IT  
\*  
\*\*\*\*\*

\*\*\*\*\* TEST 38 \*\*\*\*\*

\*  
\*BYTE ADDRESSING TEST  
\* HERE, WE'RE GOING TO MAKE SURE THAT WE CAN  
\* WRITE INTO ONLY A HIGH OR LOW BYTE OF THE MCPU.  
\*  
\*\*\*\*\*

\*\*\*\*\* TEST 39 \*\*\*\*\*

\*  
\*IN THIS TEST WE'RE GOING TO MAKE SURE THAT THE PC  
\*REG COUNTS UP PROPERLY. THE PC REG SHOULD INCREMENT  
\*ONCE AFTER EACH INSTRUCTION.  
\*  
\*\*\*\*\*

\*\*\*\*\* TEST 40 \*\*\*\*\*

\*  
\*IN THIS TEST WE'LL MAKE SURE THAT 'BRANCH FIELD H' DOESN'T  
\*GET STUCK HIGH.  
\*FIRST WE'LL CLEAR THE PC HIGH REG. THEN WE'LL DO A BRANCH INSTR  
\*WITH BAB BITS 11+12 SET. IF PCR BITS 8+9 SET THEN WE'LL KNOW  
\*WE WERE SUCCESSFUL IF PCR BITS 8+9 FAIL TO SET, WE'LL KNOW  
\*THAT THE MAX SELECTED THE WRONG INPUT TO BE CLOCKED INTO THE PCR.  
\*\*\*\*\*

\*\*\*\*\* TEST 41 \*\*\*\*\*

\*  
\*IN THIS TEST WE'RE GOING TO MAKE SURE THAT ONLY SPO  
\*IS SELECTED FOR SOURCE WHEN THE DESTINATION  
\*IS THE OUTBUS

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1153  
1154  
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1189  
1190  
1191  
1192  
1193  
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1197  
1198  
1199  
1200  
1201  
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1204  
1205  
1206  
1207  
1208

\*FIRST WE'LL WRITE EACH SP ADDR INTO ITSELF THEN WE'LL  
\*MOV SP TO OBUS4. THAT SHOULD SELECT  
\*SP ADDRESS 0. IF ANY OTHER DATA SHOWS UP, WE'LL  
\*BLAME IT ON THE SELECTION OF A DIFFERENT SCRATCH PAD.  
\*\*\*\*\*

\*\*\*\*\* TEST 42 \*\*\*\*\*

\*  
\*IN THIS TEST WE ARE GOING TO MAKE SURE THAT THE  
\*SIGNAL 'MOV INST H' (AND ITS ASSOC. TRIS) DOESN'T GET  
\*STUCK HIGH. IN ORDER TO DO THIS WE'LL CLEAR THE PC HIGH REG  
\*PUT KNOWN DATA IN THE BREG AND SP1 THEN WE'LL BRANCH  
\*WITH CROM BITS 0-3 SET AS WELL AS CROM BIT 9 WITH CROM BITS 8 AND 11 CLEAR.  
\*IF 'MOV INST H' GETS STUCK HIGH, THE PC REG HIGH WILL GET LOADED  
\*WITH THE CONTENTS OF THE ALU  
\*\*\*\*\*

\*\*\*\*\* TEST 43 \*\*\*\*\*

\*TEST THAT MASTER CLEAR, CLEARS BITS IN THE NPR CONTROL REGISTER AND  
\*MICROPROCESSOR MISCELLANEOUS REGISTER-FIRST WE'LL SET THE  
\*PRIORITY UP SO THAT WHEN WE SET THE BUS REQUEST BIT THAT IT WON'T BUG US  
\*THEN WE'LL SET ALL THE BITS IN BOTH REGS EXCEPT THE  
\*NPR REQUEST. WE'LL LOOK TO SEE THAT ALL GOT SET, NEXT  
\*WE'LL DO A MASTER CLEAR AND BE SURE THAT THEY ALL CLEAR.  
\*\*\*\*\*

8.0 ERROR INFORMATION

8.1 ERROR REPORTING

ERRORS ARE REPORTED BY THE PROGRAM AS THEY OCCUR (IF NOT  
INHIBITED). THE REPORT CONFORMS TO THE DIAGNOSTIC SUPERVISOR  
ERROR REPORT FORMAT, AND CONSISTS OF A DESCRIPTION OF THE  
ERROR, THE TEST NUMBER, SUBTEST NUMBER, PC OF THE ERROR  
CALL, DEVICE ADDRESS, AND BASIC AND EXTENDED ERROR  
INFORMATION.

THE FOLLOWING EXAMPLES PROVIDE TYPICAL ERROR REPORTS:

CZDMQ DVC FTL ERR 00045 TST 027 SUB 000 PC:022572

MASTER CLEAR FAILED TO CLEAR PC REG, CONTENTS=000624  
CZDMQ DVC FTL ERR 00015 TST 042 SUB 000 PC:027234

UNIT=00, FAILING UNIT ADDRESS=16017C  
JUMP TEST ERROR  
FROM ADDR TO ADDR BAD ADDR  
000402 000000 000114

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1234

FOR ALL OTHER ERRORS, THE REPORT MAY BE MORE EXTENSIVE AND  
REQUIRE ADDITIONAL DATA TO BE REPORTED.

9.0 HISTORY

- MODIFIED AUGUST 1980 FOR THE FOLLOWING REASONS:

- 1) CANCEL DEPO CZDMQA1
- 2) CANCEL DEPO CZDMQA2
- 3) DETECT BAD TIMING ON INTERNAL CLOCK.

- MODIFIED JULY 1981 TO FIX TEST 43 MAR BITS IN IBUS\* 10.

- MODIFIED JANUARY 1982

- 1) ERRONEOUS DATA WAS NOT CLEARED IN HIGH BYTE OF REGISTER 5  
IN TEST 40.  
FIX: CHANGE B!C #374,R5 TO BIC #17774,R5.

a



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L 2

SEQ 24

1235  
1236  
1237  
1238  
1239

2

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.TITLE CZDMQEO MB207 STATIC DIAG #2  
. =2000

1240  
1241  
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1270  
1271

002000

002000

002000

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000000  
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000000  
000000  
000000  
000000

.MCALL SVC  
SVC

; INITIALIZE SUPERVISOR MACROS

BGNMOD CZDMQ

\$LSTIN= 0  
\$LSTTAG= 0  
SVCINS= 0 ; LIST INSTRUCTIONS, SHIFTED RIGHT  
SVCTST= 0 ; LIST TEST TAGS, SHIFTED RIGHT  
SVCSUB= 0 ; LIST SUBTEST TAGS, SHIFTED RIGHT  
SVCGBL= 0 ; LIST GLOBAL TAGS, SHIFTED RIGHT  
SVCTAG= 0 ; LIST OTHER TAGS, SHIFTED RIGHT

: CHANGE THE VALUES OF THE SVC... SYMBOLS TO BE ZERO IF YOU WISH  
: TO ALIGN THE MACRO CALLS AND THEIR EXPANSIONS. CHANGE THE  
: SYMBOLS TO BE MINUS-ONE TO NOT LIST THE EXPANSIONS. YOU MAY  
: CHANGE THE SYMBOLS AT ANY POINT IN YOUR PROGRAM.

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1272		
1273		
1274		
1275		
1276		
1277		
1278	002000	
1279		
1280		
1281	002000	
1282	002000	
1283	002000	103
1284	002001	132
1285	002002	104
1286	002003	115
1287	002004	121
1288	002005	000
1289	002006	000
1290	002007	000
1291	002010	
1292	002010	104
1293	002011	
1294	002011	060
1295	002012	
1296	002012	000000
1297	002014	
1298	002014	000360
1299	002016	
1300	002016	027344
1301	002020	
1302	002020	000000
1303	002022	
1304	002022	002262
1305	002024	
1306	002024	000000
1307	002026	
1308	002026	030144
1309	002030	
1310	002030	000000
1311	002032	
1312	002032	000000
1313	002034	
1314	002034	000000
1315	002036	
1316	002036	000000
1317	002040	
1318	002040	002132
1319	002042	
1320	002042	000000
1321	002044	
1322	002044	000000
1323	002046	
1324	002046	000000
1325	002050	
1326	002050	003
1327	002051	003

```

.SBTTL PROGRAM HEADER
:++
: THE PROGRAM HEADER IS THE INTERFACE BETWEEN
: THE DIAGNOSTIC PROGRAM AND THE SUPERVISOR.
:--

        POINTER BGNAU,BGNDU

        HEADER CZDMQ,D,0,240,0
LSNAME:: :DIAGNOSTIC NAME
        .ASCII /C/
        .ASCII /Z/
        .ASCII /D/
        .ASCII /M/
        .ASCII /Q/
        .BYTE 0
        .BYTE 0
        .BYTE 0
LSREV:: :REVISION LEVEL
        .ASCII /D/
LSDEPO:: :0
        .ASCII /O/
LSUNIT:: :NUMBER OF UNITS
        .WORD 0
LSTIML:: :LONGEST TEST TIME
        .WORD 240.
LSHPCP:: :POINTER TO H.W. QUES.
        .WORD LSHARD
LSSPCP:: :POINTER TO S.W. QUES.
        .WORD 0
LSHPTP:: :PTR. TO DEF. H.W. PTABLE
        .WORD LSHW
LSSPTP:: :PTR. TO S.W. PTABLE
        .WORD 0
LSLADP:: :DIAG. END ADDRESS
        .WORD L$LAST
LSSTA:: :RESERVED FOR APT STATS
        .WORD 0
LSCO:: :
        .WORD 0
LSDTYP:: :DIAGNOSTIC TYPE
        .WORD 0
LSAPT:: :APT EXPANSION
        .WORD 0
LSDTP:: :PTR. TO DISPATCH TABLE
        .WORD L$DISPATCH
LSPRIO:: :DIAGNOSTIC RUN PRIORITY
        .WORD 0
LSENV1:: :FLAGS DESCRIBE HOW IT WAS SETUP
        .WORD 0
LSEXP1:: :EXPANSION WORD
        .WORD 0
LSMREV:: :SVC REV AND EDIT #
        .BYTE C$REVISION
        .BYTE C$EDIT

```

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1328	002052		L\$EF::		;DIAG. EVENT FLAGS
1329	002052	000000		.WORD 0	
1330	002054	000000		.WORD 0	
1331	002056		L\$SPC::		
1332	002056	000000		.WORD 0	
1333	002060		L\$DEVP::		; POINTER TO DEVICE TYPE LIST
1334	002060	002730		.WORD L\$DVTYP	
1335	002062		L\$REPP::		;PTR. TO REPORT CODE
1336	002062	000000		.WORD 0	
1337	002064		L\$EXP4::		
1338	002064	000000		.WORD 0	
1339	002066		L\$EXP5::		
1340	002066	000000		.WORD 0	
1341	002070		L\$AUT::		;PTR. TO ADD UNIT CODE
1342	002070	012144		.WORD L\$AU	
1343	002072		L\$DUT::		;PTR. TO DROP UNIT CODE
1344	002072	012140		.WORD L\$DU	
1345	002074		L\$LUN::		;LUN FOR EXERCISERS TO FILL
1346	002074	000000		.WORD 0	
1347	002076		L\$DESP::		;POINTER TO DIAG. DESCRIPTION
1348	002076	002312		.WORD L\$DESC	
1349	002100		L\$LOAD::		;GENERATE SPECIAL AUTOLOAD EMT
1350	002100	104035		EMT E\$LOAD	
1351	002102		L\$ETP::		;POINTER TO ERRtbl
1352	002102	000000		.WORD 0	
1353	002104		L\$ICP::		;PTR. TO INIT CODE
1354	002104	011340		.WORD L\$INIT	
1355	002106		L\$CCP::		;PTR. TO CLEAN-UP CODE
1356	002106	012134		.WORD L\$CLEAN	
1357	002110		L\$ACP::		;PTR. TO AUTO CODE
1358	002110	012042		.WORD L\$AUTO	
1359	002112		L\$PRT::		;PTR. TO PROTECT TABLE
1360	002112	002122		.WORD L\$PROT	
1361	002114		L\$TEST::		;TEST NUMBER
1362	002114	000000		.WORD 0	
1363	002116		L\$DLY::		;DELAY COUNT
1364	002116	000000		.WORD 0	
1365	002120		L\$HIME::		;PTR. TO HIGH MEM
1366	002120	000000		.WORD 0	
1367					
1368					
1369	002122		L\$PROT::	BGNPROT	
1370	002122			.WORD -1	
1371	002122	177777		.WORD -1	
1372	002124	177777		.WORD -1	
1373	002126	177777		.WORD -1	
1374	002130			ENDPROT	
1375					

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DISPATCH TABLE

.SBTTL DISPATCH TABLE

:/ THE DISPATCH TABLE CONTAINS THE STARTING ADDRESS OF EACH TEST.  
:/ IT IS USED BY THE SUPERVISOR TO DISPATCH TO EACH TEST.

1376  
1377  
1378  
1379  
1380  
1381  
1382  
1383 002130  
1384 002130 000053  
1385 002132  
1386 002132 012146  
1387 002134 012256  
1388 002136 012422  
1389 002140 012552  
1390 002142 012712  
1391 002144 013154  
1392 002146 013356  
1393 002150 013570  
1394 002152 014112  
1395 002154 014470  
1396 002156 014736  
1397 002160 015202  
1398 002162 015432  
1399 002164 015676  
1400 002166 016142  
1401 002170 016406  
1402 002172 016652  
1403 002174 017116  
1404 002176 017362  
1405 002200 017642  
1406 002202 020122  
1407 002204 020376  
1408 002206 020654  
1409 002210 021130  
1410 002212 021404  
1411 002214 021576  
1412 002216 021744  
1413 002220 022322  
1414 002222 022560  
1415 002224 022774  
1416 002226 023210  
1417 002230 023452  
1418 002232 024044  
1419 002234 025116  
1420 002236 025216  
1421 002240 025364  
1422 002242 026042  
1423 002244 026202  
1424 002246 026310  
1425 002250 026446  
1426 002252 026544  
1427 002254 026644  
1428 002256 026770  
1429  
1430  
1431

DISPATCH 43  
.WORD 43  
LSDISPATCH: :  
.WORD T1  
.WORD T2  
.WORD T3  
.WORD T4  
.WORD T5  
.WORD T6  
.WORD T7  
.WORD T8  
.WORD T9  
.WORD T10  
.WORD T11  
.WORD T12  
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.WORD T43

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DISPATCH TABLE

D 3

SEQ 29

1432  
1433  
1434

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DEFAULT HARDWARE P-TABLE

1435  
1436  
1437  
1438  
1439  
1440  
1441  
1442  
1443  
1444 002260  
1445 002260 C00013  
1446 002262  
1447 002262  
1448 002262 000007  
1449 002264 160170  
1450 002266 000300  
1451 002270 005000  
1452 002272 000003  
1453 002274 000056  
1454 002276 000000  
1455 002300 000000  
1456 002302 000000  
1457 002304 000004  
1458  
1459  
1460 002306 000000  
1461  
1462 002310  
1463 002310

.SBTTL DEFAULT HARDWARE P-TABLE

:/ THE DEFAULT HARDWARE P-TABLE CONTAINS DEFAULT VALUES OF  
:/ THE TEST-DEVICE PARAMETERS. THE STRUCTURE OF THIS TABLE  
:/ IS IDENTICAL TO THE STRUCTURE OF THE RUN-TIME P-TABLE.

.ENABL AMA  
BGNHW DFPTBL  
.WORD L10001-LSHW/2  
LSHW::  
DFPTBL::  
.WORD 7 :MICRO-CPU TYPE.  
.WORD 160170 :M8200,4,7 CRS ADDRESS  
.WORD 300 :M8200,4,7 VECTOR ADDRESS  
.WORD 5000 :INTERRUPT PRIORITY LEVEL  
.WORD 3 :LINE UNIT TYPE  
.WORD 56 :SWITCH PACK #1 (DDCMP LINE #)  
.WORD 0 :SWITCH PACK #2 (BM873 BOOT ADDRESS)  
.WORD 0 :SWITCH PACK #3  
.WORD 0 :TEST CONNECTOR INSTALLED FLAG  
.WORD 4 :CONTAINS BAUD RATE 4=56K BAUD DEFAULT  
:0=2.4K , 1=4.8K , 2=9.6K , 3=19.2K , 4 56K  
:5=250K , 6=500K , 7=1 MEG BAUD  
.WORD 0 :0=RUN SW OFF, 1=SW ON  
ENDHW  
L10001:

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SOFTWARE P-TABLE

1464  
1465  
1466  
1467  
1468  
1469  
1470  
1471 002310  
1472 002310 000000  
1473 002312  
1474 002312  
1475  
1476  
1477 002312  
1478 002312  
1479  
1480  
1481  
1482  
1483  
1484

.SBTTL SOFTWARE P-TABLE

:/  
:/ THE SOFTWARE P-TABLE CONTAINS THE VALUES OF THE PROGRAM  
:/ PARAMETERS THAT CAN BE CHANGED BY THE OPERATOR.  
:/

BGNSW SFPTBL  
.WORD L10002-L\$SW/2

L\$SW::  
SFPTBL::

ENDSW  
L10002:



CZDMQEO M8207 STATIC DIAG #2  
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SOFTWARE P-TABLE

1485  
1486  
1487  
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1491  
1492  
1493  
1494  
1495  
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1497  
1498  
1499  
1500  
1501  
1502  
1503  
1504  
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1539  
1540

002312

.SBTTL GLOBAL EQUATES SECTION

:/  
:/ THE GLOBAL EQUATES SECTION CONTAINS PROGRAM EQUATES THAT  
:/ ARE USED IN MORE THAN ONE TEST.  
:/

EQUALS

: BIT DEFINITIONS

BIT15== 100000  
BIT14== 40000  
BIT13== 20000  
BIT12== 10000  
BIT11== 4000  
BIT10== 2000  
BIT09== 1000  
BIT08== 400  
BIT07== 200  
BIT06== 100  
BIT05== 40  
BIT04== 20  
BIT03== 10  
BIT02== 4  
BIT01== 2  
BIT00== 1  
BIT9== BIT09  
BIT8== BIT08  
BIT7== BIT07  
BIT6== BIT06  
BIT5== BIT05  
BIT4== BIT04  
BIT3== BIT03  
BIT2== BIT02  
BIT1== BIT01  
BIT0== BIT00

: EVENT FLAG DEFINITIONS  
: EF32:EF17 RESERVED FOR SUPERVISOR TO PROGRAM COMMUNICATION

EF.START== 32. : START COMMAND WAS ISSUED  
EF.RESTART== 31. : RESTART COMMAND WAS ISSUED

CZDMQEO MB207 STATIC DIAG #2  
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GLCBL EQUATES SECTION

: CONTINUE COMMAND WAS ISSUED  
: A NEW PASS HAS BEEN STARTED  
: A POWER-FAIL/POWER-UP OCCURRED

1541 000036  
1542 000035  
1543 000034  
1544  
1545  
1546  
1547  
1548 000340  
1549 000300  
1550 000240  
1551 000200  
1552 000140  
1553 000100  
1554 000040  
1555 000000  
1556  
1557  
1558  
1559 000004  
1560 000010  
1561 000020  
1562 000040  
1563 000100  
1564 000200  
1565 000400  
1566 001000  
1567 002000  
1568 004000  
1569 010000  
1570 020000  
1571 040000  
1572 100000  
1573  
1574  
1575  
1576  
1577  
1578  
1579  
1580  
1581  
1582

EF.CONTINUE== 30.  
EF.NEW== 29.  
EF.PWR== 28.

: PRIORITY LEVEL DEFINITIONS

PRI07== 340  
PRI06== 300  
PRI05== 240  
PRI04== 200  
PRI03== 140  
PRI02== 100  
PRI01== 40  
PRI00== 0

: OPERATOR FLAG BITS

EVL== 4  
LOT== 10  
ADR== 20  
IDU== 40  
ISR== 100  
UAM== 200  
BOE== 400  
PNT== 1000  
PRI== 2000  
IXE== 4000  
IBE== 10000  
IER== 20000  
LOE== 40000  
HOE== 100000

: \*\*\*\*\*  
: \* PROGRAM EVENT FLAG DEFINITIONS  
: \*\*\*\*\*

CZDMQEO M8207 STATIC DIAG #2  
CZDMQE.P11 30-SEP-82 15:35

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GLOBAL DATA SECTION

1583				
1584				
1585				
1586				
1587				
1588				
1589				
1590				
1591				
1592				
1593	002312			
1594	002312			
1595	002312	034115	030062	020067
1596	002320	044504	043501	020056
1597	002326	031043	047440	020106
1598	002334	000062		
1599				
1600				
1601				
1602				
1603				
1604	002336	000000		
1605	002340	000000		
1606				
1607				
1608				
1609				
1610	002342	000000		
1611	002344	000000		
1612	002346	000000		
1613	002350	000000		
1614	002352	000000		
1615	002354	000000		
1616	002356	000000		
1617	002360	000000		
1618	002362	000000		
1619	002364	000000		
1620	002366	000000		
1621	002370	000000		
1622	002372	000001		
1623	002374	000000		
1624	002376	000001		
1625	002400	000001		
1626	002402	000001		
1627	002404	000001		
1628	002406	000000		
1629	002410	000000		
1630	002412	000000		
1631	002414	000000		
1632	002416	000000		
1633	002420	000000		
1634	002422	000000		
1635	002424	000000		
1636	002426	000000		
1637	002430	000000		
1638	002432	000000		

```

.SBTTL GLOBAL DATA SECTION
:
://////
:/ THE GLOBAL DATA SECTION CONTAINS DATA THAT ARE USED
:/ IN MORE THAN ONE TEST.
://////
:*****
:* STORAGE FOR DEVICE REGISTERS
:*****
:
:   DESCRIPT      <M8207 DIAG. #2 OF 2>
L$DESC::
:   .ASCIZ /M8207 DIAG. #2 OF 2/
:
:   .EVEN
:*****
:* PROGRAM CONTROL PARAMETERS
:*****
:
:   NEXT: .WORD 0           ;ADDRESS OF NEXT TEST TO BE EXECUTED
:   LOCK: .WORD 0           ;ADDRESS FOR LOCK CURRENT DATA
:*****
:* MISCELLANEOUS STORAGE
:*****
:
:   LOGDEV: .WORD 0           ;LOGICAL DEVICE NUMBER
:   PSTACK: .WORD 0           ;BASE LEVEL PROGRAM STACK POINTER
:   SUBRPC: .WORD 0           ;PC OF SUBR CALL FOR ERROR REPORTS
:   ERRFLG: .WORD 0           ;SUBROUTINE ERROR FLAG
:   RETADR: .WORD 0           ;SUBR ERROR RETURN ADDRESS
:   STRTSW: .WORD 0           ;SWITCHES AT START OF PROGRAM
:   STAT: .WORD 0             ;KM STATUS WORD STORAGE
:   CLKX: .WORD 0
:   MASKX: .WORD 0
:   SAVSP: .WORD 0           ;STACK POINTER STORAGE
:   SAVPC: .WORD 0           ;PROGRAM COUNTER STORAGE
:   ZERO: .WORD 0
:   ONE: .WORD 1
:   MEMLIM: .WORD 0           ;HIGHEST LOCATION FOR NPR'S
:   KMACTV: .BLKW 1           ;M8200,4,7 SELECTED ACTIVE
:   KMNUM: .BLKW 1           ;OCTAL NUMBER OF M8200,4,7'S
:   SAVACT: .BLKW 1           ;ORIGINAL ACTIVE DEVICES
:   SAVNUM: .BLKW 1           ;WORKABLE NUMBER
:   FLAG: .WORD 0            ;SCRATCH STORAGE
:   RUN: .WORD 0             ;POINTER TO RUNNING DEVICES
:   FADR: .WORD 0
:   WTYPE: .WORD 0           ;M82XX NUMBER FOR TYPE OF MICO-CPU
:   $REG5: .WORD 0           ;STORAGE USED FOR ERROR MSG DATA
:   $REG4: .WORD 0
:   $REG3: .WORD 0
:   $REG2: .WORD 0
:   $REG1: .WORD 0
:   $REG0: .WORD 0
:   TYPE: .WORD 0           ;=0 FOR DMP,=1 FOR M8206

```

CZDMQEO MB207 STATIC DIAG #2  
CZDMQE.P11 30-SEP-82 15:35

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GLCBL DATA SECTION

1639 002434 000000  
1640 002436 003777  
1641 002440 000000  
1642 002442 000000  
1643 002444 000000  
1644 002446 000000  
1645 002450 000000  
1646 002452 000000  
1647 002454 000000  
1648 002456 000000  
1649 002460 000000  
1650 002462 000000  
1651 002464 000000  
1652 002466 000000  
1653 002470 000000  
1654 002472 000000  
1655

MRO: .WORD 0 :MEMLOC USED INSTEAD OF RO.  
MEMSZ: .WORD 3777 :INDICATES MEMORIE SIZE, LAST ADDR.  
TEMP: .WORD 0  
\$TEMPO: .WORD 0  
\$TMP0: .WORD 0  
\$GDADR: .WORD 0 :CONTAINS ADDRESS OF 'GOOD' DATA  
\$BDADR: .WORD 0 :CONTAINS ADDRESS OF 'BAD' DATA  
\$GDDAT: .WORD 0 :CONTAINS 'GOOD' DATA  
\$BDDAT: .WORD 0 :CONTAINS 'BAD' DATA  
 :RESERVED--NOT TO BE USED  
FTIME: .WORD 0  
SAVE4: .WORD 0  
SAVE6: .WORD 0  
RUNB: .WORD 0 :0= RUN OFF, 1= RUN SW ON  
RUNINH: .WORD 0 :0=RUN SW OFF, 1=RUN SW ON

1656  
1657  
1658  
1659 002474 000  
1660 002476 000  
1661 002476 000  
1662 002477 000  
1663  
1664  
1665

\*\*\*\*\*  
: \* PROGRAM CONTROL FLAGS  
\*\*\*\*\*  
INIFLG: .BYTE 0 :PROGRAM INITIALIZING FLAG  
 :EVEN  
LOKFLG: .BYTE 0 :LOCK ON CURRENT TEST FLAG  
QV.FLG: .BYTE 0 :QUICK VERIFY FLAG  
 :EVEN

1666  
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1674  
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1680  
1681  
1682  
1683

\*\*\*\*\*  
: \* DEFINITION OF M8200,4,7 STATUS WORDS - STAT1,STAT2,STAT3  
\*\*\*\*\*  
: \*  
: \* STAT1 - BITS 00-08 IS M8200,4,7 VECTOR ADDRESS  
: \* BIT15=1 LINE UNIT IS AN M8203  
: \* BIT14=0 NO TEST CONNECTOR(S) USED  
: \* BIT14=1 M-XXX TEST CONNECTOR WILL BE USED  
: \* BIT13=0 LINE UNIT IS AN M8201  
: \* BIT13=1 LINE UNIT IS AN M8202  
: \* BIT12=1 N) LINE UNIT  
: \* BITS 09-11 IS M8200,4,7 PRIORITY LEVEL  
: \*  
: \* STAT2 - LOW BYTE IS SWITCH PACK #1 (DDCMP LINE NUMBER)  
: \* HIGH BYTE IS SWITCH PACK #2 (BM873 BOOT ADDRESS)  
: \*  
: \* STAT3 - BIT0=1 DO FREE RUNNING TESTS ON M8200,4,7  
\*\*\*\*\*

1684 002500 000000  
1685 002502 000000  
1686 002504 000000  
1687  
1688  
1689  
1690  
1691 002506 000000  
1692 002510 000000  
1693 002512 000000  
1694 002514 000000

STAT1: .WORD 0  
STAT2: .WORD 0  
STAT3: .WORD 0  
\*\*\*\*\*  
: \* POINTERS TO M8200,4,7 VECTORS AND REGISTERS  
\*\*\*\*\*  
KMRVEC: 0 :POINTER TO M8200,4,7 RCV INTRPT VECTOR  
KMRLVL: 0 :POINTER TO M8200,4,7 RCV INTRPT SERVICE PS  
KMTVEC: 0 :POINTER TO M8200,4,7 TX INTRPT VECTOR  
KMTLVL: 0 :POINTER TO M8200,4,7 TX INTRPT SERVICE PS

CZDMQEO M8207 STATIC DIAG #2  
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GLOBAL DATA SECTION

1695 002516 000000  
1696 002520 000000  
1697 002522 000000  
1698 002524 000000  
1699 002526 000000  
1700  
1701  
1702  
1703 002530  
1704  
1705  
1706 002530 000100  
1707 002730  
1708  
1709  
1710  
1711  
1712  
1713  
1714

KMCSR: 0 : POINTER TO M8200,4,7 CONTROL STATUS REGISTER  
KMCSRH: 0 : POINTER TO M8200,4,7 CONTROL STATUS REGISTER HIGH BYTE  
KMCTL: 0 : POINTER TO M8200,4,7 CONTROL OUT REGISTER  
KMP04: 0 : POINTER TO M8200,4,7 PORT REGISTER - SEL4  
KMP06: 0 : POINTER TO M8200,4,7 PORT REGISTER - SEL6

::\*\*\*\*\* PRIMARY REG ADRS STORAGE FOR THIS UNIT \*\*\*\*\*  
: THESE LOCATIONS WILL BE LOADED FOR THE CURRENT UNIT, IN INIT CODE  
REGADR:

::\*\*\*\*\* STACK USED FOR SUBROUTINE LINKAGE \*\*\*\*\*  
.BLKW 100  
SSTACK:

CZDMQEO M8207 STATIC DIAG #2  
CZDMQE.P11 30-SEP-82 15:35

MACY11 30A(1052) 18-OCT-82 15:30 PAGE 38  
GLCBAL TEXT SECTION

1715  
1716  
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002730			
002730			
002730	034115	030062	026060
002736	034115	030062	026064
002744	051117	046440	031070
002752	033460	000	
	002756		

```

.SBTTL GLOBAL TEXT SECTION
:XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
:Z THE GLOBAL TEXT SECTION CONTAINS FORMAT STATEMENTS,
:Z MESSAGES, AND ASCII INFORMATION THAT ARE USED IN
:Z MORE THAN ONE TEST.
:XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
:*****
: * NAMES OF DEVICES SUPPORTED BY PROGRAM
:*****
DEV TYP <M8200,M8204,OR M8207>
LSDVTYP::
.ASCIZ /M8200,M8204,OR M8207/

.EVEN

:
: FORMAT STATEMENTS USED IN PRINT CALLS
:

```

CZDMQEO MB207 STATIC DIAG #2  
CZDMQE.P11 30-SEP-82 15:35

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GLCBAL SUBROUTINES

1744  
1745  
1746  
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1750  
1751  
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1755  
1756  
1757  
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.SBTTL GLOBAL SUBROUTINES

:/ THE GLOBAL SUBROUTINES ARE CALLED BY MORE THAN ONE TEST

-----  
: MACRO'S NEEDED TO CALL SUBROUTINES  
-----

.MACRO POPSP2  
22626  
.ENDM

CZDMQEO M8207 STATIC DIAG #2  
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GLCBAL SUBROUTINES

1759  
1760  
1761  
1762  
1763



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GLCBAL SUBROUTINES

1764  
1765  
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1775  
1776  
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1785  
1786  
1787  
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1789

:/   
:/ THE GLOBAL SUBROUTINES ARE CALLED BY MORE THAN ONE TEST   
:/

:-  
: MACRO'S NEEDED TO CALL SUBROUTINES  
:-

.MACRO K4ONLY ?N2  
CMP MEMSZ,#2000  
BNE N2  
EXIT TST  
.ENDM  
.MACRO ED\$CALL XY  
.LIST  
:\*\*\*\*\* TEST 'XY' \*\*\*\*\*  
.NLIST  
.ENDM  
.MACRO BADHEAD  
.RADIX 10  
ED\$CALL \T\$TESTNUM+1  
.RADIX 8  
.ENDM

CZDMQEO M8207 STATIC DIAG #2  
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GLCBAL SUBROUTINES

```

1790 .MACRO MYINT
1791 .LIST
1792 MOV KMCSR,R1 ;RECORD DEVICE ADDR.
1793 .NLIST
1794 .ENDM
1795
1796 .MACRO MACEX ?N2
1797 .LIST
1798 ;DO NOT DO TEST IF M8200
1799 .NLIST
1800 TST TYPE
1801 BNE N2
1802 EXIT TST
1803 N2:
1804 .ENDM MACEX
1805 .MACRO MACEX2 ?N2
1806 .LIST
1807 ;DO NOT DO TEST IF M8200
1808 .NLIST
1809 CMP WTYPE,#0
1810 BNE N2
1811 EXIT TST
1812 N2:
1813 .ENDM MACEX2
1814 .MACRO K4ONLY ?N2
1815 .LIST
1816 ;DO NOT DO TEST IF M8200, OR M8204
1817 .NLIST
1818 CMP MEMSZ,#2000
1819 BNE N2
1820 EXIT TST
1821 N2:
1822 ;NOTE THIS TEST IS ONLY DESIGNED FOR 4K MODULE.
1823 .ENDM
1824
1825 .MACRO CLRMAR
1826 ROMCLK
1827 004000
1828 .ENDM CLRMAR
1829 .MACRO ROMCLK
1830 .LIST
1831 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
1832 .NLIST
1833 .ENDM
1834
1835 .MACRO SROMCLK
1836 .LIST
1837 JSR R5,.SROMCLK
1838 .NLIST
1839 .ENDM
1840 .MACRO SKIP06 NNN
1841 .LIST
1842 ;GOTO 'NNN' IF M8206
1843 .NLIST
1844 CMP WTYPE,#6 ;SEE IF M8206
1845 BEQ NNN

```

CZDMQEO MB207 STATIC DIAG #2  
CZDMQE.P11 30-SEP-82 15:35

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GLOBAL SUBROUTINES

```

1846 .ENDM
1847 .MACRO SKIP07 NNN
1848 .LIST
1849 :GOTO 'NNN' IF MB207
1850 .NLIST
1851 CMP WTYPE,#7 ;SEE IF MB200,4,7
1852 BEQ NNN
1853 .ENDM
1854 .MACRO SKIP04 NNN
1855 .LIST
1856 :GOTO 'NNN' IF MB204
1857 .NLIST
1858 CMP WTYPE,#4 ;SEE IF MB204
1859 BEQ NNN
1860 .ENDM
1861 .MACRO MSTCLR
1862 JSR R5, .MSTCLR ;CLEAR MB200,4,7
1863 .ENDM
1864
1865 002756 .MSTCLR:
1866 002756 112777 000100 177534 MOVB #BIT6,@KMCSRH ;SET INST.
1867 002764 142777 000300 177526 BICB #BIT6!BIT7,@KMCSRH
1868 002772 000205 RTS R5
1869
1870 002774 000024 PATCH: .BLKW 20. ;PATCH AREA.
1871
1872
1873
1874 003044 ENDBUG:
1875 : UNSAFE TO PATCH ANY OTHER AREA.
1876 003044 .ROMCLK:
1877 003044 000240 NOP
1878 003046 000240 NOP
1879 003050 152777 000002 177442 .REGT: BISB #BIT1,@KMCSRH
1880 003056 012577 177444 MOV (R5)+,@KMP06
1881 003062 152777 000003 177430 BISB #BIT1!BIT0,@KMCSRH
1882 003070 142777 000007 177422 BICB #BIT2!BIT1!BIT0,@KMCSRH
1883 003076 000205 RTS R5
1884
1885 003100 .SROMCLK:
1886 003100 000240 NOP
1887 003102 022737 000006 002414 CMP #6,WTYPE
1888 003110 001357 BNE .REGT
1889 003112 152777 000002 177400 BISB #BIT1,@KMCSRH
1890 003120 012577 177402 MOV (R5)+,@KMP06
1891 003124 000240 NOP
1892 003126 000240 NOP
1893 003130 142777 000007 177362 BICB #7,@KMCSRH
1894 003136
1895 003136 152777 000001 177354 1$: BISB #BIT0,@KMCSRH ;STEP INSTR.
1896 003144 142777 000007 177346 BICB #BIT2!BIT1!BIT0,@KMCSRH
1897 003152 000240 NOP
1898 003154 000240 NOP
1899 003156 152777 000002 177334 2$: BISB #2,@KMCSRH
1900 003164
1901 003164 000205 RTS R5

```

CZDMQEO M8207 STATIC DIAG #2  
CZDMQE.P11 30-SEP-82 15:35

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GLCBAL SUBROUTINES

```

1902 003166          CLRALL:
1903                ;CLEAR C & Z BITS AND BR
1904 003166          ROMCLK
1905 003166 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1906 003172 000400          400          ;0 TO BR
1907 003174          ROMCLK
1908 003174 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1909 003200 063220          63220         ;SP(0) TO BR
1910 003202          ROMCLK
1911 003202 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1912 003206 060400          60400         ;BR,SP(0) + BR
1913 003210          SR0MCLK
1914 003210 004537 003100 JSR   R5,,SR0MCLK
1915 003214 000000          0
1916 003216 000207          RTS    PC
1917
1918 003220          SETBR0:
1919                ;SETS BR0 BIT
1920 003220          ROMCLK
1921 003220 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1922 003224 000401          401          ;1 TO BR
1923 003226 000207          RTS    PC
1924
1925 003230          SETBR1:
1926                ;THIS SUBROUTINE SETS BR1 BIT
1927
1928 003230          ROMCLK          ;NEXT WORD IS INSTRUCTION
1929 003230 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1930 003234 000402          000402         ;BR_002
1931 003236 000207          RTS    PC
1932
1933 003240          SETBR4:
1934                ;THIS SUBROUTINE SETS BR4 BIT
1935
1936 003240          ROMCLK          ;NEXT WORD IS INSTRUCTION
1937 003240 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1938 003244 000420          420
1939 003246 000207          RTS    PC
1940
1941 003250          SETBR7:
1942                ;THIS SUBROUTINE SETS BR7 BIT
1943
1944 003250          ROMCLK          ;NEXT WORD IS INSTRUCTION
1945 003250 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1946 003254 000600          600
1947 003256 000207          RTS    PC
1948
1949 003260          SETC:
1950                ;THIS SUBROUTINE SETS THE C BIT
1951
1952 003260          ROMCLK          ;NEXT WORD IS INSTRUCTION
1953 003260 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1954 003264 000777          000777         ;BR 377
1955 003266          ROMCLK          ;NEXT WORD IS INSTRUCTION
1956 003266 004537 003044 JSR   R5,,ROMCLK      ;CLOCK INSTRUCTION
1957 003272 063220          063220         ;SP(0)_BR

```

CZDMQEO M8207 STATIC DIAG #2  
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GLCBAL SUBROUTINES

```

1958 003274          ROMCLK          :NEXT WORD IS INSTRUCTION
1959 003274 004537 003044 JSR      R5,ROMCLK      :CLOCK INSTRUCTION
1960 003300 060400          060400          :BR SP(0)+BR
1961 003302          SRMCLK          :NOW WE MUST CLOCK THE BITS INTO IBUS <13>
1962 003302 004537 003100 JSR      R5,.SRMCLK
1963 003306 000000          0
1964 003310 000207          RTS      PC
1965
1966 003312          SETZ:
1967          :THIS SUBROUTINE SETS THE Z BIT
1968
1969 003312          ROMCLK          :NEXT WORD IS INSTRUCTION
1970 003312 004537 003044 JSR      R5,ROMCLK      :CLOCK INSTRUCTION
1971 003316 000777          000777          :BR 377
1972 003320          SRMCLK          :NOW CLOCK THE BITS INTO IBUS<13>
1973 003320 004537 003100 JSR      R5,.SRMCLK
1974 003324 000777          0777
1975 003326 000207          RTS      PC
1976
1977 003330          RAMDAT:
1978          :THIS SUBROUTINE LOADS R4 WITH THE LOWEST
1979          :8 BITS OF THE CRAM PC.
1980
1981 003330 005004          CLR      R4
1982 003332 017605 000000 MOV      @ (SP),R5      :GOOD DATA
1983 003336 062716 000002 ADD      #2,(SP)       :ADJUST STACK
1984 003342          SKIP06 1$      :IF M8206,WE'LL GET PC A DIFFERENT WAY.
1985          :GOTO 1$ IF M8206
1986 003352          SKIP07 1$      :IF M8200,4,7 WE'LL GET PC A DIFFERENT WAY.
1987          :GOTO 1$ IF M8207
1988 003362 005011          CLR      (R1)          :CLEAR BIT10
1989 003364 052711 000400 BIS      #BIT8,(R1)    :CLOCK INSTRUCTION IN CRAM THAT
1990          :JUMPED TO, IT LOADS BR WITH IT
1991 003370 005011          CLR      (R1)          :CLR BIT8
1992 003372          ROMCLK          :NEXT WORD IS INSTRUCTION
1993 003372 004537 003044 JSR      R5,ROMCLK      :CLOCK INSTRUCTION
1994 003376 061225          061225          :MOV BR TO PORT 5
1995 003400 116104 000005 MOVB     5(R1),R4      :PUT 'FOUND' IN R4
1996 003404 000207          RTS      PC          :RETURN
1997
1998 003406          1$:
1999 003406 004537 003044 ROMCLK          :READ PC LOW REG DIRECTLY.
2000 003412 121244          JSR      R5,ROMCLK      :CLOCK INSTRUCTION
2001 003414 116104 000004 MOVB     4(R1),R4      :IBUS* <12> TO PORT 4
2002 003420 000207          RTS      PC          :PUT INTO R4
2003          :EXIT
2004 003422          WROM:
2005          :THIS SUBROUTINE WRITES THE ROMMAP INTO THE CRAM
2006
2007          :
2008          :
2009 003422          BIT      #BIT15,STAT1 :BE SURE M8200,4,7 HAS CRAM
2010          BEG      2$          :SKIP IF NO CRAM
2011          SKIP07 2$
2012          :GOTO 2$ IF M8207
2013 003432 005000          CLR      R0          :R0=CRAM ADDRESS
2014 003434 012702 012146 MOV      #ROMMAP,R2    :R2 POINTS TO ROMMAP
2015 003440 012711 002000 1$: MOV      #BIT10,(R1) :SET ROM0

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GLOBAL SUBROUTINES

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2014 003444 010061 000004      MOV      R0,4(R1)      ;LOAD CRAM ADDRESS
2015 003450 012261 000006      MOV      (R2)+,6(R1)  ;LOAD WORD TO BE WRITTEN
2016 003454 052711 020000      BIS      #BIT13,(R1) ;WRITE IT!
2017 003460 005200                INC      R0            ;NEXT ADDRESS
2018 003462 023700 002436      CMP      MEMSZ,R0     ;DONE YET?
2019 003466 001364                BNE     1$            ;BR IF NO
2020 003470 005011                CLR     (R1)         ;CLEAR SEL0
2021 003472 000207                RTS     PC           ;RETURN
2022
2023 003474                MEMSET:
2024                ;THIS SUBROUTINE LOADS CRAM WITH SPECIAL INSTRUCTIONS
2025                ;FOR THE CRAM JUMP TEST. ALL CRAM LOCATIONS ARE LOADED
2026                ;WITH INSTRUCTIONS THAT MOVE A 37 TO THE BR, EXCEPT THE
2027                ;FOLLOWING CRAM ADDRESSES: 0,1,4,7,525,1777. THESE LOCATIONS
2028                ;CONTAIN INSTRUCTIONS WHICH LOAD THE BR WITH THE LOWEST
2029                ;8 BITS OF THAT CRAM ADDRESS.
2030
2031 003474                SKIP07 3$           ;IF M8200,4,7 CAN'T WRITE CRAM!
2032                ;GOTO 3$ IF M8207
2033 003504 005000                CLR     R0           ;R0 = CRAM ADDRESS
2034 003506 012711 002000      1$:  MOV     #BIT10,(R1) ;SET ROMO
2035 003512 010061 000004      MOV     R0,4(R1)    ;LOAD CRAM ADDRESS
2036 003516 012761 000437 000006      MOV     #437,6(R1) ;LOAD INSTRUCTION
2037 003524 052711 020000      BIS     #BIT13,(R1) ;WRITE INSTRUCTION IN CRAM
2038 003530 005200                INC     R0           ;NEXT ADDRESS
2039 003532 023700 002436      CMP     MEMSZ,R0    ;DONE YET?
2040 003536 001363                BNE     1$           ;BR IF NO
2041 003540 005000                CLR     R0           ;INDEX REGISTER
2042 003542 012711 002000      2$:  MOV     #BIT10,(R1) ;SET ROMO
2043 003546 016061 003602 000004      MOV     CRAM(R0),4(R1) ;LOAD CRAM ADDRESS IN SEL4
2044 003554 016061 003616 000006      MOV     INSTU(R0),6(R1) ;LOAD INSTRUCTION TO BE WRITTEN
2045 003562 052711 020000      BIS     #BIT13,(R1) ;WRITE CRAM!
2046 003566 005720                TST     (R0)+        ;NEXT
2047 003570 022700 000014      CMP     #14,R0      ;DONE YET?
2048 003574 001362                BNE     2$           ;BR IF NO
2049 003576 005011                CLR     (R1)         ;CLEAR ALL BITS
2050 003600 000207                3$:  RTS     PC           ;RETURN
2051
2052 003602 000000 000001 000004      CRAMA: .WORD 0,1,4,7,1777,525
2053 003610 000007 001777 000525
2054
2055 003616 000400                INSTU: 000400        ;BR_0
2056 003620 000401                ;BR_1
2057 003622 000404                ;BR_4
2058 003624 000407                ;BR_7
2059 003626 000777                ;BR_377
2060 003630 000525                ;BR_125
2061
2062
2063                ;ROUTINE TO SAVE GENERAL REGISTERS FOR ERROR ROUTINE.
2064                ;CALL = JSR PC,SV05
2065 003632 010537 002416      SV05: MOV     R5,$REG5
2066 003636 010437 002420      MOV     R4,$REG4
2067 003642 010337 002422      MOV     R3,$REG3
2068 003646 010237 002424      MOV     R2,$REG2
2069 003652 010137 002426      MOV     R1,$REG1

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2070	003656	013737	002434	002430	MOV	MRO,\$REGO
2071	003664	000207			RTS	PC
2072						
2073						

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GLCGBAL ERROR REPORT SECTION

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003666 047045 047445 022466  
003674 032123 047445 022466  
003702 032123 047445 022466  
003710 000116  
003712 047045 047445 022466  
003720 033523 047445 022466  
003726 000116  
003730 047045 047445 022466  
003736 030523 022460 031517  
003744 051445 022464 032117  
003752 047045 000  
003755 045 022516 031517  
003762 051445 022467 031517  
003770 047045 000  
003773 045 022516 033117  
004000 051445 022465 033117  
004006 051445 022463 033117  
004014 047045 000  
004017 045 022516 051101  
004024 043505 051511 042524  
004032 020122 042101 051104  
004040 051505 020123 051105  
004046 047522 026122 042101  
004054 051104 051505 020123  
004062 020075 047445 022466  
004070 026101 047125 052111  
004076 036440 022440 031117  
004104 000  
004105 045 022516 020101  
004112 051503 020122 044510  
004120 044107 041040 052131  
004126 020105 047507 020124  
004134 051127 052111 042524  
004142 020116 047111 047524  
004150 047440 020116 020101  
004156 047514 020127 054502  
004164 042524 054040 042506  
004172 000122  
004174 047045 040445 041440  
004202 051123 046040 053517  
004210 041040 052131 020105  
004216 047507 020124 051127  
004224 052111 042524 020116  
004232 047111 047524 047440  
004240 020116 020101 044510

.SBTTL GLOBAL ERROR REPORT SECTION

:/ THE GLOBAL ERROR REPORT SECTION CONTAINS ERROR MESSAGES  
:/ THAT ARE USED IN MORE THAN ONE TEST.  
:/

TFM1: .ASCIZ /%N%06%54%06%54%04%N/

TFM2: .ASCIZ /%N%03%57%03%N/

TFM3: .ASCIZ /%N%03%510%03%54%04%N/

TFM4: .ASCIZ /%N%03%57%03%N/

TFM5: .ASCIZ /%N%06%55%06%53%06%N/

TFM36: .ASCIZ /%N%AREGISTER ADDRESS ERROR,ADDRESS = %06%A,UNIT = %02%/

TFM41: .ASCIZ /%N%A CSR HIGH BYTE GOT WRITTEN INTO ON A LOW BYTE XFER/

TFM42: .ASCIZ /%N%A CSR LOW BYTE GOT WRITTEN INTO ON A HIGH BYTE XFER/



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2130	004246	044107	041040	052131	
2131	004254	020105	043130	051105	
2132	004262	000			
2133	004263	045	022516	047101	TFM40: .ASCIZ /%N%ANEG ADDR TEST DUAL ADDR ERROR-BAD ADDR = %06/
2134	004270	043505	040440	042104	
2135	004276	020122	042524	052123	
2136	004304	042040	040525	020114	
2137	004312	042101	051104	042440	
2138	004320	051122	051117	041055	
2139	004326	042101	040440	042104	
2140	004334	020122	020075	047445	
2141	004342	000066			
2142	004344	040445	051440	051103	TFM43: .ASCIZ /%A SCRATCH PAD %03%A DUAL ADDRESS ERROR WITH SP%02/
2143	004352	052101	044103	050040	
2144	004360	042101	022440	03517	
2145	004366	040445	042040	040525	
2146	004374	020114	042101	051104	
2147	004402	051505	020123	051105	
2148	004410	047522	020122	044527	
2149	004416	044124	051440	022520	
2150	004424	031117	000		
2151	004427	045	022524	052101	TFM44: .ASCIZ /%T%ATHE MAR REG, CONTENTS= %06/
2152	004434	042510	046440	051101	
2153	004442	051040	043505	020054	
2154	004450	047503	052116	047105	
2155	004456	051524	020075	047445	
2156	004464	000066			
2157	004466	052045	040445	044124	TFM45: .ASCIZ /%T%ATHE PC REG, CONTENTS= %06/
2158	004474	020105	041520	051040	
2159	004502	043505	020054	047503	
2160	004510	052116	047105	051524	
2161	004516	020075	047445	000066	
2162	004524	047045	040445	047516	TFM45A: .ASCII /%N%ANOTE: THIS ERROR MAY BE FALSELY GENERATED IF THE/
2163	004532	042524	020072	044124	
2164	004540	051511	042440	051122	
2165	004546	051117	046440	054501	
2166	004554	041040	020105	040506	
2167	004562	051514	046105	020131	
2168	004570	042507	042516	040522	
2169	004576	042524	020104	043111	
2170	004604	052040	042510		
2171	004610	047045	040445	052522	.ASCIZ /%N%ARUN BIT (SW7 OF E28) IS ON/
2172	004616	020116	044502	020124	
2173	004624	051450	033527	047440	
2174	004632	020106	031105	024470	
2175	004640	044440	020123	047117	
2176	004646	000			
2177	004647	045	047101	051120	TFM46: .ASCIZ "%ANPR/MISC REGS DATA FAILURE, GOOD =%06%A, BAD -%06"
2178	004654	046457	051511	020103	
2179	004662	042522	051507	042040	
2180	004670	052101	020101	040506	
2181	004676	046111	051125	026105	
2182	004704	043440	047517	020104	
2183	004712	022475	033117	040445	
2184	004720	020054	040502	020104	
2185	004726	022475	033117	000	

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2186	004733	045	050101	020103	TFM47:	.ASCIZ	''%APC INCR. INCORRECT: S/B= %C6%A ; WAS = %06''
2187	004740	047111	051103	020056			
2188	004746	047111	047503	051122			
2189	004754	041505	035124	051440			
2190	004762	041057	020075	047445			
2191	004770	022466	020101	020073			
2192	004776	040527	020123	020075			
2193	005004	047445	000066				
2194	005010	040515	052123	051105	TMMC:	.ASCIZ	/MASTER CLEAR FAILED TO CLEAR /
2195	005016	041440	042514	051101			
2196	005024	043040	044501	042514			
2197	005032	020104	047524	041440			
2198	005040	042514	051101	000040			
2199	005046	047045	052045	047045	FM1:	.ASCIZ	/XNXTXN/
2200	005054	000					
2201							
2202							
2203							
2204	005055	000			EM0:	.ASCIZ	//
2205	005056	051103	046501	042040	EM1:	.ASCIZ	/CRAM DATA ERROR/
2206	005064	052101	020101	051105			
2207	005072	047522	000122				
2208	005076	051103	046501	042040	EM2:	.ASCIZ	/CRAM DUAL ADDRESSING ERROR/
2209	005104	040525	020114	042101			
2210	005112	051104	051505	044523			
2211	005120	043516	042440	051122			
2212	005126	051117	000				
2213	005131	112	046525	020120	EM3:	.ASCIZ	/JUMP ERROR/
2214	005136	051105	047522	000122			
2215	005144	051103	046501	045040	EM4:	.ASCIZ	/CRAM JUMP TEST FAULT/
2216	005152	046525	020120	042524			
2217	005160	052123	043040	052501			
2218	005166	052114	000				
2219	005171	111	050117	046440	EM5:	.ASCIZ	/IOP MAIN MEMORY TEST/
2220	005176	044501	020116	042515			
2221	005204	047515	054522	052040			
2222	005212	051505	000124				
2223	005216	047511	020120	040515	EM6:	.ASCIZ	/IOP MAR TEST/
2224	005224	020122	042524	052123			
2225	005232	000					
2226	005233	102	020122	044522	EM7:	.ASCIZ	/BR RIGHT SHIFT ERROR/
2227	005240	044107	020124	044123			
2228	005246	043111	020124	051105			
2229	005254	047522	000122				
2230	005260	040515	020122	052504	EM10:	.ASCIZ	/MAR DUAL ADDRESSING ERROR/
2231	005266	046101	040440	042104			
2232	005274	042522	051523	047111			
2233	005302	020107	051105	047522			
2234	005310	000122					
2235	005312	052512	050115	043040	EM11:	.ASCIZ	/JUMP FIELD ERROR/
2236	005320	042511	042114	042440			
2237	005326	051122	051117	000			
2238	005333	112	046525	020120	EM12:	.ASCIZ	/JUMP TEST ERROR/
2239	005340	042524	052123	042440			
2240	005346	051122	051117	000			
2241	005353	103	047117	044504	EM16:	.ASCIZ	/CONDITION CODE TESTING,Z & C/

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2242	005360	044524	047117	041440	
2243	005366	042117	020105	042524	
2244	005374	052123	047111	026107	
2245	005402	020132	020046	000103	
2246	005410	046103	041517	020113	EMB1: .ASCIZ /CLOCK TIME TOO FAST/
2247	005416	044524	042515	052040	
2248	005424	047517	043040	051501	
2249	005432	000124			
2250	005434				EM35:
2251	005434	047506	041522	020105	EM17: .ASCIZ /FORCE POWER FAIL ERROR/
2252	005442	047520	042527	020122	
2253	005450	040506	046111	042440	
2254	005456	051122	051117	000	
2255	005463	111	052502	025123	EM27: .ASCIZ 'IBUS* WRITE/READ ERROR'
2256	005470	053440	044522	042524	
2257	005476	051057	040505	020104	
2258	005504	051105	047522	000122	
2259					
2260	005512	041111	051525	047457	EM29: .ASCIZ 'IBUS/OBUS WRITE/READ ERROR'
2261	005520	052502	020123	051127	
2262	005526	052111	027505	042522	
2263	005534	042101	042440	051122	
2264	005542	051117	000		
2265					
2266	005545	120	046507	041440	EMB50: .ASCIZ 'PGM CLOCK WOULD NOT CLEAR'
2267	005552	047514	045503	053440	
2268	005560	052517	042114	047040	
2269	005566	052117	041440	042514	
2270	005574	051101	000		
2271	005577	120	046507	041440	EMB51: .ASCIZ 'PGM CLOCK WOULD NOT SET'
2272	005604	047514	045503	053440	
2273	005612	052517	042114	047040	
2274	005620	052117	051440	052105	
2275	005626	000			
2276	005627	045	022516	025101	STM: .ASCIZ '%NZ*****'
2277	005634	025052	025052	025052	
2278	005642	025052	025052	025052	
2279	005650	025052	025052	025052	
2280	005656	025052	025052	025052	
2281	005664	025052	025052	025052	
2282	005672	025052	025052	025052	
2283	005700	025052	025052	025052	
2284	005706	025052	025052	025052	
2285	005714	025052	025052	025052	
2286	005722	000			
2287	005723	000			DH0: .ASCIZ //
2288					
2289					
2290	005724	054105	042520	052103	DH1: .ASCIZ /EXPECTED FOUND ADDRESS/
2291	005732	042105	020040	047506	
2292	005740	047125	020104	040440	
2293	005746	042104	042522	051523	
2294	005754	000			
2295	005755	105	050130	041505	DH2: .ASCIZ /EXPECTED FOUND/
2296	005762	042524	020104	043040	
2297	005770	052517	042116	000	

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2298 005775 106 047522 020115 DH3: .ASCIZ /FROM ADDR TO ADDR BAD ADDR/  
 2299 006002 042101 051104 020040  
 2300 006010 047524 040440 042104  
 2301 006016 020122 041040 042101  
 2302 006024 040440 042104 000122

2303  
 2304  
 2305 .EVEN  
 2306  
 2307

2308  
 2309

2310 :-----  
 : MACRO'S NEEDED TO REPORT ERRORS  
 :-----

2311  
 2312

2313 .MACRO MDT1  
 2314 PRINTB #TFM1,\$REG2,\$REG4,\$REG0  
 2315 .ENDM

2316 .MACRO MDT2  
 2317 PRINTB #TFM1,\$REG5,\$REG4,\$REG2  
 2318 .ENDM  
 2319

2320 .MACRO MDT3  
 2321 PRINTB #TFM2,\$REG5,\$REG4  
 2322 .ENDM  
 2323

2324 .MACRO MDT4  
 2325 PRINTB #TFM3,\$REG5,\$REG4,FLAG  
 2326 .ENDM  
 2327

2328 .MACRO MDT5  
 2329 PRINTB #TFM3,\$REG5,\$REG4,\$REG2  
 2330 .ENDM  
 2331

2332 .MACRO MDT0  
 2333 .ENDM

2334 .MACRO MDT6  
 2335 PRINTB #TFM4,\$REG2,\$REG4  
 2336 .ENDM  
 2337

2338 .MACRO MDT7  
 2339 PRINTB #TFM4,\$REG5,\$REG4  
 2340

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2341  
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ENDM  
.MACRO MDT8  
PRINTB #TFM5,FADR,\$REG5,\$REG4  
.ENDM

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GLOBAL ERROR REPORT SECTION

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2346  
2347

.MACRO	SMD	ERRNN	ERNB	ERHM	ERFM
	BGNMSG	ERR'ERRNN			

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2348				PRINTB	#FM1,#EM'ERNB
2349				PRINTB	#FM1,#DH'ERHM
2350				MDT'ERFM	
2351				PRINTB	#STM
2352				ENDMSG	
2353				.ENDM	
2354				.MACRO	ERROR ECB
2355				JSR	PC,SVOS
2356				ERRDF	'ECB',EMO,ERR'ECB'
2357				.ENDM	
2358					
2359					
2360					
2361					
2362	006032			ERR1::	\$MD 1,1,1,1
2363	006032				
2364	006032	012746	005C56	MOV	#EM1,-(SP)
2365	006036	012746	005046	MOV	#FM1,-(SP)
2366	006042	012746	000002	MOV	#2,-(SP)
2367	006046	010600		MOV	SP,RO
2368	006050	104414		TRAP	C\$PNTB
2369	006052	062706	000006	ADD	#6,SP
2370	006056	012746	005724	MOV	#DH1,-(SP)
2371	006062	012746	005046	MOV	#FM1,-(SP)
2372	006066	012746	000002	MOV	#2,-(SP)
2373	006072	010600		MOV	SP,RO
2374	006074	104414		TRAP	C\$PNTB
2375	006076	062706	000006	ADD	#6,SP
2376	006102	013746	002430	MOV	\$REG0,-(SP)
2377	006106	013746	002420	MOV	\$REG4,-(SP)
2378	006112	013746	002424	MOV	\$REG2,-(SP)
2379	006116	012746	003666	MOV	#TFM1,-(SP)
2380	006122	012746	000004	MOV	#4,-(SP)
2381	006126	010600		MOV	SP,RO
2382	006130	104414		TRAP	C\$PNTB
2383	006132	062706	000012	ADD	#12,SP
2384	006136	012746	005627	MOV	#STM,-(SP)
2385	006142	012746	000001	MOV	#1,-(SP)
2386	006146	010600		MOV	SP,RO
2387	006150	104414		TRAP	C\$PNTB
2388	006152	062706	000004	ADD	#4,SP
2389	006156			L10003:	
2390	006156	104423		TRAP	C\$MSG
2391	006160			ERR2::	\$MD 2,2,1,1
2392	006160				
2393	006160	012746	005076	MOV	#EM2,-(SP)
2394	006164	012746	005046	MOV	#FM1,-(SP)
2395	006170	012746	000002	MOV	#2,-(SP)
2396	006174	010600		MOV	SP,RO
2397	006176	104414		TRAP	C\$PNTB
2398	006200	062706	000006	ADD	#6,SP
2399	006204	012746	005724	MOV	#DH1,-(SP)
2400	006210	012746	005046	MOV	#FM1,-(SP)
2401	006214	012746	000002	MOV	#2,-(SP)
2402	006220	010600		MOV	SP,RO
2403	006222	104414		TRAP	C\$PNTB

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2404	006224	062706	000006	ADD	#6,SP
2405	006230	013746	002430	MOV	\$REG0,-(SP)
2406	006234	013746	002420	MOV	\$REG4,-(SP)
2407	006240	013746	002424	MOV	\$REG2,-(SP)
2408	006244	012746	003606	MOV	#TFM1,-(SP)
2409	006250	012746	000004	MOV	#4,-(SP)
2410	006254	010600		MOV	SP,RO
2411	006256	104414		TRAP	C\$PNTB
2412	006260	062706	000012	ADD	#12,SP
2413	006264	012746	005627	MOV	#STM,-(SP)
2414	006270	012746	000001	MOV	#1,-(SP)
2415	006274	010600		MOV	SP,RO
2416	006276	104414		TRAP	C\$PNTB
2417	006300	062706	000004	ADD	#4,SP
2418	006304				
2419	006304	104423		L10004: TRAP	C\$MSG
2420	006306			\$MD	3,1,1,2
2421	006306			ERR3::	
2422	006306	012746	005056	MOV	#EM1,-(SP)
2423	006312	012746	005046	MOV	#FM1,-(SP)
2424	006316	012746	000002	MOV	#2,-(SP)
2425	006322	010600		MOV	SP,RO
2426	006324	104414		TRAP	C\$PNTB
2427	006326	062706	000006	ADD	#6,SP
2428	006332	012746	005724	MOV	#DH1,-(SP)
2429	006336	012746	005046	MOV	#FM1,-(SP)
2430	006342	012746	000002	MOV	#2,-(SP)
2431	006346	010600		MOV	SP,RO
2432	006350	104414		TRAP	C\$PNTB
2433	006352	062706	000006	ADD	#6,SP
2434	006356	013746	002424	MOV	\$REG2,-(SP)
2435	006362	013746	002420	MOV	\$REG4,-(SP)
2436	006366	013746	002416	MOV	\$REG5,-(SP)
2437	006372	012746	003666	MOV	#TFM1,-(SP)
2438	006376	012746	000004	MOV	#4,-(SP)
2439	006402	010600		MOV	SP,RO
2440	006404	104414		TRAP	C\$PNTB
2441	006406	062706	000012	ADD	#12,SP
2442	006412	012746	005627	MOV	#STM,-(SP)
2443	006416	012746	000001	MOV	#1,-(SP)
2444	006422	010600		MOV	SP,RO
2445	006424	104414		TRAP	C\$PNTB
2446	006426	062706	000004	ADD	#4,SP
2447	006432			L10005: TRAP	C\$MSG
2448	006432	104423		\$MD	4,3,2,3
2449	006434			ERR4::	
2450	006434				
2451	006434	012746	005131	MOV	#EM3,-(SP)
2452	006440	012746	005046	MOV	#FM1,-(SP)
2453	006444	012746	000002	MOV	#2,-(SP)
2454	006450	010600		MOV	SP,RO
2455	006452	104414		TRAP	C\$PNTB
2456	006454	062706	000006	ADD	#6,SP
2457	006460	012746	005755	MOV	#DH2,-(SP)
2458	006464	012746	005046	MOV	#FM1,-(SP)
2459	006470	012746	000002	MOV	#2,-(SP)



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2460	006474	010600		MOV	SP,RO
2461	006476	104414		TRAP	C\$PNTB
2462	006500	062706	000006	ADD	#6,SP
2463	006504	013746	002420	MOV	\$REG4,-(SP)
2464	006510	013746	002416	MOV	\$REG5,-(SP)
2465	006514	012746	003712	MOV	#TFM2,-(SP)
2466	006520	012746	000003	MOV	#3,-(SP)
2467	006524	010600		MOV	SP,RO
2468	006526	104414		TRAP	C\$PNTB
2469	006530	062706	000010	ADD	#10,SP
2470	006534	012746	005627	MOV	#STM,-(SP)
2471	006540	012746	000001	MOV	#1,-(SP)
2472	006544	010600		MOV	SP,RO
2473	006546	104414		TRAP	C\$PNTB
2474	006550	062706	000004	ADD	#4,SP
2475	006554				
2476	006554	104423		L10006:	TRAP C\$MSG

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 GLCBAL ERROR REPORT SECTION

2477	006556		
2478	006556		
2479	006556	012746	005144
2480	006562	012746	005046
2481	006566	012746	000002
2482	006572	010600	
2483	006574	104414	
2484	006576	062706	000006
2485	006602	012746	005755
2486	006606	012746	005046
2487	006612	012746	000002
2488	006616	010600	
2489	006620	104414	
2490	006622	062706	000006
2491	006626	013746	002420
2492	006632	013746	002416
2493	006636	012746	003712
2494	006642	012746	000003
2495	006646	010600	
2496	006650	104414	
2497	006652	062706	000010
2498	006656	012746	005627
2499	006662	012746	000001
2500	006666	010600	
2501	006670	104414	
2502	006672	062706	000004
2503	006676		
2504	006676	104423	

ERR5::	\$MD	5,4,2,3
	MOV	#EM4,-(SP)
	MOV	#FM1,-(SP)
	MOV	#2,-(SP)
	MOV	SP,R0
	TRAP	C\$PNTB
	ADD	#6,SP
	MOV	#DH2,-(SP)
	MOV	#FM1,-(SP)
	MOV	#2,-(SP)
	MOV	SP,R0
	TRAP	C\$PNTB
	ADD	#6,SP
	MOV	\$REG4,-(SP)
	MOV	\$REG5,-(SP)
	MOV	#TFM2,-(SP)
	MOV	#3,-(SP)
	MOV	SP,R0
	TRAP	C\$PNTB
	ADD	#10,SP
	MOV	#STM,-(SP)
	MOV	#1,-(SP)
	MOV	SP,R0
	TRAP	C\$PNTB
	ADD	#4,SP
L10007:	TRAP	C\$MSG

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2505	006700		
2506	006700		
2507	006700	012746	005171
2508	006704	012746	005046
2509	006710	012746	000002
2510	006714	010600	
2511	006716	104414	
2512	006720	062706	000006
2513	006724	012746	005724
2514	006730	012746	005046
2515	006734	012746	000002
2516	006740	010600	
2517	006742	104414	
2518	006744	062706	000006
2519	006750	013746	002406
2520	006754	013746	002420
2521	006760	013746	002416
2522	006764	012746	003730
2523	006770	012746	000004
2524	006774	010600	
2525	006776	104414	
2526	007000	062706	000012
2527	007004	012746	005627
2528	007010	012746	000001
2529	007014	010600	
2530	007016	104414	
2531	007020	062706	000004
2532	007024		
2533	007024	104423	
2534	007026		
2535	007026		
2536	007026	012746	005216
2537	007032	012746	005046
2538	007036	012746	000002
2539	007042	010600	
2540	007044	104414	
2541	007046	062706	000006
2542	007052	012746	005724
2543	007056	012746	005046
2544	007062	012746	000002
2545	007066	010600	
2546	007070	104414	
2547	007072	062706	000006
2548	007076	013746	002424
2549	007102	013746	002420
2550	007106	013746	002416
2551	007112	012746	003730
2552	007116	012746	000004
2553	007122	010600	
2554	007124	104414	
2555	007126	062706	000012
2556	007132	012746	005627
2557	007136	012746	000001
2558	007142	010600	
2559	007144	104414	
2560	007146	062706	000004

ERR6::	SMD	6,5,1,4
	MOV	#EM5,-(SP)
	MOV	#FM1,-(SP)
	MOV	#2,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#6,SP
	MOV	#DH1,-(SP)
	MOV	#FM1,-(SP)
	MOV	#2,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#6,SP
	MOV	FLAG,-(SP)
	MOV	\$REG4,-(SP)
	MOV	\$REG5,-(SP)
	MOV	#TFM3,-(SP)
	MOV	#4,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#12,SP
	MOV	#STM,-(SP)
	MOV	#1,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#4,SP
L10010:	TRAP	C\$MSG
ERR7::	SMD	7,6,1,5
	MOV	#EM6,-(SP)
	MOV	#FM1,-(SP)
	MOV	#2,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#6,SP
	MOV	#DH1,-(SP)
	MOV	#FM1,-(SP)
	MOV	#2,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#6,SP
	MOV	\$REG2,-(SP)
	MOV	\$REG4,-(SP)
	MOV	\$REG5,-(SP)
	MOV	#TFM3,-(SP)
	MOV	#4,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#12,SP
	MOV	#STM,-(SP)
	MOV	#1,-(SP)
	MOV	SP,RO
	TRAP	C\$PNTB
	ADD	#4,SP

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2561	007152		
2562	007152	104423	
2563	007154		
2564	007154		
2565	007154	012746	005233
2566	007160	012746	005046
2567	007164	012746	000002
2568	007170	010600	
2569	007172	104414	
2570	007174	062706	000006
2571	007200	012746	005755
2572	007204	012746	005046
2573	007210	012746	000002
2574	007214	010600	
2575	007216	104414	
2576	007220	062706	000006
2577	007224	013746	002420
2578	007230	013746	002416
2579	007234	012746	003712
2580	007240	012746	000003
2581	007244	010600	
2582	007246	104414	
2583	007250	062706	000010
2584	007254	012746	005627
2585	007260	012746	000001
2586	007264	010600	
2587	007266	104414	
2588	007270	062706	000004
2589	007274		
2590	007274	104423	
2591	007276		
2592	007276		
2593	007276	012746	005260
2594	007302	012746	005046
2595	007306	012746	000002
2596	007312	010600	
2597	007314	104414	
2598	007316	062706	000006
2599	007322	012746	005755
2600	007326	012746	005046
2601	007332	012746	000002
2602	007336	010600	
2603	007340	104414	
2604	007342	062706	000006
2605	007346	013746	002420
2606	007352	013746	002424
2607	007356	012746	003755
2608	007362	012746	000003
2609	007366	010600	
2610	007370	104414	
2611	007372	062706	000010
2612	007376	012746	005627
2613	007402	012746	000001
2614	007406	010600	
2615	007410	104414	
2616	007412	062706	000004

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L10011:
          TRAP      C$MSG
          $MD       10,7,2,3
ERR10::
          MOV       #EM7,-(SP)
          MOV       #FM1,-(SP)
          MOV       #2,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #6,SP
          MOV       #DH2,-(SP)
          MOV       #FM1,-(SP)
          MOV       #2,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #6,SP
          MOV       $REG4,-(SP)
          MOV       $REG5,-(SP)
          MOV       #TFM2,-(SP)
          MOV       #3,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #10,SP
          MOV       #STM,-(SP)
          MOV       #1,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #4,SP

L10012:
          TRAP      C$MSG
          $MD       11,10,2,6
ERR11::
          MOV       #EM10,-(SP)
          MOV       #FM1,-(SP)
          MOV       #2,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #6,SP
          MOV       #DH2,-(SP)
          MOV       #FM1,-(SP)
          MOV       #2,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #6,SP
          MOV       $REG4,-(SP)
          MOV       $REG2,-(SP)
          MOV       #TFM4,-(SP)
          MOV       #3,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #10,SP
          MOV       #STM,-(SP)
          MOV       #1,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #4,SP

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2617	007416		
2618	007416	104423	
2619	007420		
2620	007420		
2621	007420	012746	005233
2622	007424	012746	005046
2623	007430	012746	000002
2624	007434	010600	
2625	007436	104414	
2626	007440	062706	000006
2627	007444	012746	005755
2628	007450	012746	005046
2629	007454	012746	000002
2630	007460	010600	
2631	007462	104414	
2632	007464	062706	000006
2633	007470	013746	002420
2634	007474	013746	002416
2635	007500	012746	003755
2636	007504	012746	000003
2637	007510	010600	
2638	007512	104414	
2639	007514	062706	000010
2640	007520	012746	005627
2641	007524	012746	000001
2642	007530	010600	
2643	007532	104414	
2644	007534	062706	000004
2645	007540		
2646	007540	104423	
2647	007542		
2648	007542		
2649	007542	012746	005260
2650	007546	012746	005046
2651	007552	012746	000002
2652	007556	010600	
2653	007560	104414	
2654	007562	062706	000006
2655	007566	012746	005755
2656	007572	012746	005046
2657	007576	012746	000002
2658	007602	010600	
2659	007604	104414	
2660	007606	062706	000006
2661	007612	013746	002420
2662	007616	013746	002416
2663	007622	012746	003712
2664	007626	012746	000003
2665	007632	010600	
2666	007634	104414	
2667	007636	062706	000010
2668	007642	012746	005627
2669	007646	012746	000001
2670	007652	010600	
2671	007654	104414	
2672	007656	062706	000004

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L10013:
ERR12::
TRAP      C$MSG
SMD       12,7,2,7
MOV       #EM7,-(SP)
MOV       #FM1,-(SP)
MOV       #2,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #6,SP
MOV       #DH2,-(SP)
MOV       #FM1,-(SP)
MOV       #2,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #6,SP
MOV       $REG4,-(SP)
MOV       $REG5,-(SP)
MOV       #TFM4,-(SP)
MOV       #3,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #10,SP
MOV       #STM,-(SP)
MOV       #1,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #4,SP

L10014:
ERR13::
TRAP      C$MSG
SMD       13,10,2,3
MOV       #EM10,-(SP)
MOV       #FM1,-(SP)
MOV       #2,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #6,SP
MOV       #DH2,-(SP)
MOV       #FM1,-(SP)
MOV       #2,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #6,SP
MOV       $REG4,-(SP)
MOV       $REG5,-(SP)
MOV       #TFM2,-(SP)
MOV       #3,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #10,SP
MOV       #STM,-(SP)
MOV       #1,-(SP)
MOV       SP,R0
TRAP      C$PNTB
ADD       #4,SP

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2673	007662		
2674	007662	104423	
2675	007664		
2676	007664		
2677	007664	012746	005312
2678	007670	012746	005046
2679	007674	012746	000002
2680	007700	010600	
2681	007702	104414	
2682	007704	062706	000006
2683	007710	012746	005755
2684	007714	012746	005046
2685	007720	012746	000002
2686	007724	010600	
2687	007726	104414	
2688	007730	062706	000006
2689	007734	013746	002420
2690	007740	013746	002424
2691	007744	012746	003755
2692	007750	012746	00C003
2693	007754	010600	
2694	007756	104414	
2695	007760	062706	000010
2696	007764	012746	005627
2697	007770	012746	000001
2698	007774	010600	
2699	007776	104414	
2700	010000	062706	000004
2701	010004		
2702	010004	104423	

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L10015:
          TRAP      C$MSG
          SMD       14,11,2,6
ERR14::
          MOV       #EM11,-(SP)
          MOV       #FM1,-(SP)
          MOV       #2,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #6,SP
          MOV       #DH2,-(SP)
          MOV       #FM1,-(SP)
          MOV       #2,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #6,SP
          MOV       $REG4,-(SP)
          MOV       $REG2,-(SP)
          MOV       #TFM4,-(SP)
          MOV       #3,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #10,SP
          MOV       #STM,-(SP)
          MOV       #1,-(SP)
          MOV       SP,R0
          TRAP      C$PNTB
          ADD       #4,SP
L10016:
          TRAP      C$MSG

```

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GLCBL ERROR REPORT SECTION

2703	010006		
2704	010006		
2705	010006	012746	005333
2706	010012	012746	005046
2707	010016	012746	000002
2708	010022	010600	
2709	010024	104414	
2710	010026	062706	000006
2711	010032	012746	005775
2712	010036	012746	005046
2713	010042	012746	000002
2714	010046	010600	
2715	010050	104414	
2716	010052	062706	000006
2717	010056	013746	002420
2718	010062	013746	002416
2719	010066	013746	002412
2720	010072	012746	003773
2721	010076	012746	000004
2722	010102	010600	
2723	010104	104414	
2724	010106	062706	000012
2725	010112	012746	005627
2726	010116	012746	000001
2727	010122	010600	
2728	010124	104414	
2729	010126	062706	000004
2730	010132		
2731	010132	104423	
2732	010134		
2733	010134		
2734	010134	012746	005353
2735	010140	012746	005046
2736	010144	012746	000002
2737	010150	010600	
2738	010152	104414	
2739	010154	062706	000006
2740	010160	012746	005755
2741	010164	012746	005046
2742	010170	012746	000002
2743	010174	010600	
2744	010176	104414	
2745	010200	062706	000006
2746	010204	013746	002420
2747	010210	013746	002416
2748	010214	012746	003755
2749	010220	012746	000003
2750	010224	010600	
2751	010226	104414	
2752	010230	062706	000010
2753	010234	012746	005627
2754	010240	012746	000001
2755	010244	010600	
2756	010246	104414	
2757	010250	062706	000004
2758	010254		

```

ERR15:: $MD 15,12,3,8
MOV #EM12,-(SP)
MOV #FM1,-(SP)
MOV #2,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #6,SP
MOV #DH3,-(SP)
MOV #FM1,-(SP)
MOV #2,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #6,SP
MOV $REG4,-(SP)
MOV $REG5,-(SP)
MOV FADR,-(SP)
MOV #TFM5,-(SP)
MOV #4,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #12,SP
MOV #STM,-(SP)
MOV #1,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #4,SP

L10017: TRAP C$MSG
$MD 16,16,2,7

ERR16:: MOV #EM16,-(SP)
MOV #FM1,-(SP)
MOV #2,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #6,SP
MOV #DH2,-(SP)
MOV #FM1,-(SP)
MOV #2,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #6,SP
MOV $REG4,-(SP)
MOV $REG5,-(SP)
MOV #TFM4,-(SP)
MOV #3,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #10,SP
MOV #STM,-(SP)
MOV #1,-(SP)
MOV SP,RO
TRAP C$PNTB
ADD #4,SP

L10020:

```

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GLCBAL ERROR REPORT SECTION

2759 010254 104423  
2760

TRAP C\$MSG



2761  
2762 010256  
2763 010256  
2764 010256 012746 005434  
2765 010262 012746 005046  
2766 010266 012746 000002  
2767 010272 010600  
2768 010274 104414  
2769 010276 062706 000006  
2770 010302 012746 005723  
2771 010306 012746 005046  
2772 010312 012746 000002  
2773 010316 010600  
2774 010320 104414  
2775 010322 062706 000006  
2776 010326 012746 005627  
2777 010332 012746 000001  
2778 010336 010600  
2779 010340 104414  
2780 010342 062706 000004  
2781 010346  
2782 010346 104423  
2783 010350  
2784 010350  
2785 010350 012746 005512  
2786 010354 012746 005046  
2787 010360 012746 000002  
2788 010364 010600  
2789 010366 104414  
2790 010370 062706 000006  
2791 010374 012746 005755  
2792 010400 012746 005046  
2793 010404 012746 000002  
2794 010410 010600  
2795 010412 104414  
2796 010414 062706 000006  
2797 010420 013746 002420  
2798 010424 013746 002416  
2799 010430 012746 003712  
2800 010434 012746 000003  
2801 010440 010600  
2802 010442 104414  
2803 010444 062706 000010  
2804 010450 012746 005627  
2805 010454 012746 000001  
2806 010460 010600  
2807 010462 104414  
2808 010464 062706 000004  
2809 010470  
2810 010470 104423  
2811 010472  
2812 010472  
2813 010472 012746 005434  
2814 010476 012746 005046  
2815 010502 012746 000002  
2816 010506 010600

ERR17:: \$MD 17,17,0,0  
MOV #EM17,-(SP)  
MOV #FM1,-(SP)  
MOV #2,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #6,SP  
MOV #DH0,-(SP)  
MOV #FM1,-(SP)  
MOV #2,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #6,SP  
MOV #STM,-(SP)  
MOV #1,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #4,SP  
L10021: TRAP C\$MSG  
\$MD 29,29,2,3  
ERR29:: MOV #EM29,-(SP)  
MOV #FM1,-(SP)  
MOV #2,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #6,SP  
MOV #DH2,-(SP)  
MOV #FM1,-(SP)  
MOV #2,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #6,SP  
MOV \$REG4,-(SP)  
MOV \$REG5,-(SP)  
MOV #TFM2,-(SP)  
MOV #3,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #10,SP  
MOV #STM,-(SP)  
MOV #1,-(SP)  
MOV SP,RO  
TRAP C\$PNTB  
ADD #4,SP  
L10022: TRAP C\$MSG  
\$MD 35,35,2,3  
ERR35:: MOV #EM35,-(SP)  
MOV #FM1,-(SP)  
MOV #2,-(SP)  
MOV SP,RO

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GLOBAL ERROR REPORT SECTION

2817	010510	104414		TRAP	C\$PNTB
2818	010512	062706	000006	ADD	#6,SP
2819	010516	012746	005755	MOV	#DH2,-(SP)
2820	010522	012746	005046	MOV	#FM1,-(SP)
2821	010526	012746	000002	MOV	#2,-(SP)
2822	010532	010600		MOV	SP,R0
2823	010534	104414		TRAP	C\$PNTB
2824	010536	062706	000006	ADD	#6,SP
2825	010542	013746	002420	MOV	\$REG4,-(SP)
2826	010546	013746	002416	MOV	\$REG5,-(SP)
2827	010552	012746	003712	MOV	#TFM2,-(SP)
2828	010556	012746	000003	MOV	#3,-(SP)
2829	010562	010600		MOV	SP,R0
2830	010564	104414		TRAP	C\$PNTB
2831	010566	062706	000010	ADD	#10,SP
2832	010572	012746	005627	MOV	#STM,-(SP)
2833	010576	012746	000001	MOV	#1,-(SP)
2834	010602	010600		MOV	SP,R0
2835	010604	104414		TRAP	C\$PNTB
2836	010606	062706	000004	ADD	#4,SP
2837	010612				
2838	010612	104423		L10023: TRAP	C\$MSG
2839					
2840	010614			BGNMSG	ERR36
2841	010614			ERR36::	
2842	010614			PRINTB	#STM
2843	010614	012746	005627	MOV	#STM,-(SP)
2844	010620	012746	000001	MOV	#1,-(SP)
2845	010624	010600		MOV	SP,R0
2846	010626	104414		TRAP	C\$PNTB
2847	010630	062706	000004	ADD	#4,SP
2848	010634			ENDMSG	
2849	010634			L10024:	
2850	010634	104423		TRAP	C\$MSG
2851					
2852	010636			BGNMSG	ERR40
2853	010636			ERR40::	
2854	010636			PRINTF	#TFM40,R2
2855	010636	010246		MOV	R2,-(SP)
2856	010640	012746	004263	MOV	#TFM40,-(SP)
2857	010644	012746	000002	MOV	#2,-(SP)
2858	010650	010600		MOV	SP,R0
2859	010652	104417		TRAP	C\$PNTF
2860	010654	062706	000006	ADD	#6,SP
2861	010660			PRINTB	#STM
2862	010660	012746	005627	MOV	#STM,-(SP)
2863	010664	012746	000001	MOV	#1,-(SP)
2864	010670	010600		MOV	SP,R0
2865	010672	104414		TRAP	C\$PNTB
2866	010674	062706	000004	ADD	#4,SP
2867	010700			ENDMSG	
2868	010700			L10025:	
2869	010700	104423		TRAP	C\$MSG
2870	010702			BGNMSG	ERR41
2871	010702			ERR41::	
2872	010702			PRINTF	#TFM41

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 CZDMQE.P11 30-SEP-82 15:35 GLOBAL ERROR REPORT SECTION

2873	010702	012746	004105		MOV	#TFM41,-(SP)
2874	010706	012746	000001		MOV	#1,-(SP)
2875	010712	010600			MOV	SP,R0
2876	010714	104417			TRAP	C\$PNTF
2877	010716	062706	000004		ADD	#4,SP
2878	010722			PRINTB	#STM	
2879	010722	012746	005627		MOV	#STM,-(SP)
2880	010726	012746	000001		MOV	#1,-(SP)
2881	010732	010600			MOV	SP,R0
2882	010734	104414			TRAP	C\$PNTB
2883	010736	062706	000004		ADD	#4,SP
2884	010742			ENDMSG		
2885	010742			L10026:		
2886	010742	104423			TRAP	C\$MSG
2887	010744			BGNMSG	ERR42	
2888	010744			ERR42::		
2889	010744			PRINTF	#TFM42	
2890	010744	012746	004174		MOV	#TFM42,-(SP)
2891	010750	012746	000001		MOV	#1,-(SP)
2892	010754	010600			MOV	SP,R0
2893	010756	104417			TRAP	C\$PNTF
2894	010760	062706	000004		ADD	#4,SP
2895	010764			PRINTB	#STM	
2896	010764	012746	005627		MOV	#STM,-(SP)
2897	010770	012746	000001		MOV	#1,-(SP)
2898	010774	010600			MOV	SP,R0
2899	010776	104414			TRAP	C\$PNTB
2900	011000	062706	000004		ADD	#4,SP
2901	011004			ENDMSG		
2902	011004			L10027:		
2903	011004	104423			TRAP	C\$MSG
2904						
2905	011006			BGNMSG	ERR43	
2906	011006			ERR43::		
2907	011006			PRINTF	#TFM43,R5,R4	
2908	011006	010446			MOV	R4,-(SP)
2909	011010	010546			MOV	R5,-(SP)
2910	011012	012746	004344		MOV	#TFM43,-(SP)
2911	011016	012746	000003		MOV	#3,-(SP)
2912	011022	010600			MOV	SP,R0
2913	011024	104417			TRAP	C\$PNTF
2914	011026	062706	000010		ADD	#10,SP
2915	011032			PRINTB	#STM	
2916	011032	012746	005627		MOV	#STM,-(SP)
2917	011036	012746	000001		MOV	#1,-(SP)
2918	011042	010600			MOV	SP,R0
2919	011044	104414			TRAP	C\$PNTB
2920	011046	062706	000004		ADD	#4,SP
2921	011052			ENDMSG		
2922	011052			L10030:		
2923	011052	104423			TRAP	C\$MSG
2924	011054			BGNMSG	ERR44	
2925	011054			ERR44::		
2926	011054			PRINTF	#TFM44,#TMMC,R4	
2927	011054	010446			MOV	R4,-(SP)
2928	011056	012746	005010		MOV	#TMMC,-(SP)

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GLOBAL ERROR REPORT SECTION

2929	011062	012746	004427		MOV	#TFM44,-(SP)
2930	011066	012746	000003		MOV	#3,-(SP)
2931	011072	010600			MOV	SP,R0
2932	011074	104417			TRAP	C\$PNTF
2933	011076	062706	000010		ADD	#10,SP
2934	011102			PRINTB	#STM	
2935	011102	012746	005627		MOV	#STM,-(SP)
2936	011106	012746	000001		MOV	#1,-(SP)
2937	011112	010600			MOV	SP,R0
2938	011114	104414			TRAP	C\$PNTB
2939	011116	062706	000004		ADD	#4,SP
2940	011122			ENDMSG		
2941	011122			L10031:		
2942	011122	104423			TRAP	C\$MSG
2943	011124			BGNMSG	ERR45	
2944	011124			ERR45::		
2945	011124			PRINTF	#TFM45,#TMMC,R4	
2946	011124	010446			MOV	R4,-(SP)
2947	011126	012746	005010		MOV	#TMMC,-(SP)
2948	011132	012746	004466		MOV	#TFM45,-(SP)
2949	011136	012746	000003		MOV	#3,-(SP)
2950	011142	010600			MOV	SP,R0
2951	011144	104417			TRAP	C\$PNTF
2952	011146	062706	000010		ADD	#10,SP
2953	011152			PRINTB	#TFM45A	
2954	011152	012746	004524		MOV	#TFM45A,-(SP)
2955	011156	012746	000001		MOV	#1,-(SP)
2956	011162	010600			MOV	SP,R0
2957	011164	104414			TRAP	C\$PNTB
2958	011166	062706	000004		ADD	#4,SP
2959	011172			PRINTB	#STM	
2960	011172	012746	005627		MOV	#STM,-(SP)
2961	011176	012746	000001		MOV	#1,-(SP)
2962	011202	010600			MOV	SP,R0
2963	011204	104414			TRAP	C\$PNTB
2964	011206	062706	000004		ADD	#4,SP
2965	011212			ENDMSG		
2966	011212			L10032:		
2967	011212	104423			TRAP	C\$MSG
2968	011214			BGNMSG	ERR46	
2969	011214			ERR46::		
2970	011214			PRINTF	#TFM46,\$GDDAT,R4	
2971	011214	010446			MOV	R4,-(SP)
2972	011216	013746	002452		MOV	\$GDDAT,-(SP)
2973	011222	012746	004647		MOV	#TFM46,-(SP)
2974	011226	012746	000003		MOV	#3,-(SP)
2975	011232	010600			MOV	SP,R0
2976	011234	104417			TRAP	C\$PNTF
2977	011236	062706	000010		ADD	#10,SP
2978	011242			PRINTB	#STM	
2979	011242	012746	005627		MOV	#STM,-(SP)
2980	011246	012746	000001		MOV	#1,-(SP)
2981	011252	010600			MOV	SP,R0
2982	011254	104414			TRAP	C\$PNTB
2983	011256	062706	000004		ADD	#4,SP
2984	011262			ENDMSG		

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GLOBAL ERROR REPORT SECTION

2985	011262			L10033:	
2986	011262	104423		TRAP	C\$MSG
2987					
2988	011264			BGNMSG	ERR47
2989	011264			ERR47::	
2990	011264			PRINTF	#TFM47,R5,R4
2991	011264	010446		MOV	R4,-(SP)
2992	011266	010546		MOV	R5,-(SP)
2993	011270	012746	004733	MOV	#TFM47,-(SP)
2994	011274	012746	000003	MOV	#3,-(SP)
2995	011300	010600		MOV	SP,R0
2996	011302	104417		TRAP	C\$PNTF
2997	011304	062706	000010	ADD	#10,SP
2998	011310			PRINTB	#STM
2999	011310	012746	005627	MOV	#STM,-(SP)
3000	011314	012746	000001	MOV	#1,-(SP)
3001	011320	010600		MOV	SP,R0
3002	011322	104414		TRAP	C\$PNTB
3003	011324	062706	000004	ADD	#4,SP
3004	011330			ENDMSG	
3005	011330			L10034:	
3006	011330	104423		TRAP	C\$MSG
3007					

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REPORT CODING SECTION

3008  
3009  
3010

.SBTTL REPORT CODING SECTION

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REPORT CODING SECTION

3011

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REPORT CODING SECTION

3012  
3013  
3014  
3015  
3016 011332  
3017 011332  
3018  
3019  
3020 011332  
3021 011332 000167  
3022 011334 000000  
3023

: THE REPORT CODING SECTION CONTAINS THE  
: "PRINTS" CALLS THAT GENERATE STATISTICAL REPORTS.  
:--

LSRPT:: BGNRPT  
  
EXIT RPT  
.WORD JSJMP  
.WORD L10035-2-.



CZDMQEO MB207 STATIC DIAG #2  
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REPORT CODING SECTION

3024  
3025 011336  
3026 011336  
3027 011336 104425  
3028

L10035: ENDRPT  
TRAP (SRPT

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REPORT CODING SECTION

3029  
3030

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REPORT CODING SECTION

3031  
3032

CZLMQEO MB207 STATIC DIAG #2  
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INITIALIZE SECTION

3033

.SBTTL INITIALIZE SECTION

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INITIALIZE SECTION

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3034
3035
3036
3037
3038
3039
3040 011340
3041 011340
3042
3043
3044 011340 012705 002730
3045
3046 011344 010637 002344
3047 011350 005737 002462
3048 011354 001011
3049 011356 013737 000004 002464
3050 011364 013737 000006 002466
3051 011372 012737 000001 002462
3052 011400 013737 002464 000004
3053 011406 013737 002466 000006
3054
3055
3056 011414
3057 011414 012700 000040
3058 011420 104447
3059 011422
3060 011422 103414
3061
3062 011424
3063 011424 012700 000035
3064 011430 104447
3065 011432
3066 011432 103410
3067
3068 011434
3069 011434 012700 000036
3070 011440 104447
3071 011442
3072 011442 103576
3073
3074 011444
3075 011444 012700 000037
3076 011450 104447
3077 011452
3078 011452 103003
3079
3080 011454
3081
3082 011454 012737 177777 002342
3083
3084
3085
3086
3087 011462
3088 011462 005237 002342
3089 011466 023737 002342 002012

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```

:////////////////////
:/ THE INITIALIZE SECTION CONTAINS THE CODING THAT IS PERFORMED
:/ AT THE BEGINNING OF EACH PASS.
:////////////////////

      BGNINIT
LSINIT:

:INITIALIZE SUBROUTINE STACK
      MOV      #SSTACK,R5
:STORE BASE LEVEL PROGRAM STACK POINTER
      MOV      SP,PSTACK
      TST      FTIME
      BNE      1$
      MOV      @#4,SAVE4
      MOV      @#6,SAVE6
      MOV      #1,FTIME
1$:    MOV      SAVE4,@#4
      MOV      SAVE6,@#6

:SEE IF PROGRAM JUST STARTED, BR IF YES
      READEF   #EF.START
      MOV      #EF.START,R0
      TRAP     C$REFG
      BCOMPLETE NEWST
      BCS      NEWST
:SEE IF THIS IS A NEW PASS, BR IF YES
      READEF   #EF.NEW
      MOV      #EF.NEW,R0
      TRAP     C$REFG
      BCOMPLETE NEWST
      BCS      NEWST
:SEE IF PROGRAM WAS JUST CONTINUED
      READEF   #EF.CONTINUE
      MOV      #EF.CONTINUE,R0
      TRAP     C$REFG
      BCOMPLETE ENDIT
      BCS      ENDIT
:SEE IF PROGRAM JUST RESTARTED, BR IF NOT
      READEF   #EF.RESTART
      MOV      #EF.RESTART,R0
      TRAP     C$REFG
      BNCOMPLETE GETPRM
      BCC      GETPRM

NEWST:
:RESET LOGICAL DEVICE TO -1
      MOV      #-1,LOGDEV

:GET UNIBUS ADRS, VECTOR, PRIORITY LEVEL, LINE UNIT,SWITCH
:PACKS, TEST CONNECTOR INFO. FOR THIS M8200,4,7 (CURRENT LOGICAL
:DEVICE).
GETPRM:
      INC      LOGDEV
      CMP      LOGDEV,LSUNIT

```

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INITIALIZE SECTION

3090	011474	002367			BGE	NEWST
3091	011476				GPHARD	LOGDEV,R1
3092	011476	013700	002342		MOV	LOGDEV,R0
3093	011502	104442			TRAP	C\$GPHRD
3094	011504	010001			MOV	R0,R1
3095	011506				BNCOMPLETE	GETPRM
3096	011506	103365			BCC	GETPRM
3097	011510	012137	002414		MOV	(R1)+,WTYPE
3098						
3099	011514	011137	002516		:GET ADDRESS OF	M8200,4,7
3100					MOV	(R1),KMCSR
3101	011520	011137	002520		:GET POINTER TO	M8200,4,7 CSR HI BYTE
3102	011524	005237	002520		MOV	(R1),KMCSRH
3103					INC	KMCSRH
3104	011530	011137	002522		:GET POINTER TO	M8200,4,7 CTL OUT REG
3105	011534	062737	000002	002522	MOV	(R1),KMCTL
3106					ADD	#2,KMCTL
3107	011542	011137	002524		:GET POINTER TO	M8200,4,7 PORT REG - SEL 4
3108	011546	062737	000004	002524	MOV	(R1),KMPO4
3109					ADD	#4,KMPO4
3110	011554	012137	002526		:GET POINTER TO	M8200,4,7 PORT REG - SEL 6
3111	011560	062737	000006	002526	MOV	(R1)+,KMPO6
3112					ADD	#6,KMPO6
3113	011566	011137	002506		:GET POINTER TO	RCV VECTOR
3114					MOV	(R1),KMRVEC
3115	011572	011137	002510		:GET POINTER TO	RCV PRIORITY LEVEL
3116	011576	062737	000002	002510	MOV	(R1),KMRLVL
3117					ADD	#2,KMRLVL
3118	011604	011137	002512		:GET POINTER TO	TX VECTOR
3119	011610	062737	000004	002512	MOV	(R1),KMTVEC
3120					ADD	#4,KMTVEC
3121	011616	011137	002514		:GET POINTER TO	TX PRIORITY LEVEL
3122	011622	062737	000006	002514	MOV	(R1),KMTLVL
3123					ADD	#6,KMTLVL
3124	011630	016137	000020	002472	:PUT VECTOR INTO	STAT1
3125	011636	012137	002500		MOV	20(R1),RUNINH
3126					MOV	(R1)+,STAT1
3127	011642	052137	002500		:PUT PRIORITY INTO	STAT1
3128					BIS	(R1)+,STAT1
3129	011646	005711			:SEE IF NO LINE	UNIT, SET BIT IF YES
3130	011650	001004			TST	(R1)
3131	011652	052737	010000	002500	BNE	50000\$
3132	011660	000416			BIS	#BIT12,STAT1
3133	011662				BR	4\$
3134					50000\$:	
3135	011662	021127	000001		:SEE IF M8201	LINE UNIT, SET BIT IF YES
3136	011666	001001			CMR	(R1),#1
3137	011670	000412			BNE	50001\$
3138	011672				BR	4\$
3139					50001\$:	
3140	011672	021127	000002		:SEE IF M8202	LINE UNIT, SET BIT IF YES
3141	011676	001004			CMR	(R1),#2
3142	011700	052737	020000	002500	BNE	50002\$
3143	011706	000403			BIS	#BIT13,STAT1
3144	011710				BR	4\$
3145					50002\$:	
					:SET BIT FOR	M8203 LINE UNIT

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```

3146 011710 052737 100000 002500      BIS      #BIT15,STAT1
3147 011716
3148
3149 011716 056137 000006 002500      4$:
;SET BIT IN STAT1 FOR TEST CONNECTOR
3150 011724 062701 000002      BIS      6(R1),STAT1
3151
3152 011730 012137 002502      ADD      #2,R1
;SET SWITCH PACK #1 IN STAT2 LOW BYTE
3153
3154 011734 111137 002503      MOV      (R1)+,STAT2
;SET SWITCH PACK #2 IN STAT2 HIGH BYTE
3155
3156
3157
3158 011740 000240      ;INCREMENT LOGICAL UNIT (DEVICE) NUMBER
3159 011742 000240      :
;      INC      LOGDEV
3160
3161 011744 012737 002000 002436      MOV      #2000,MEMSZ
3162 011752 005037 002432      CLR      TYPE
3163 011756 123727 002414 000000      CMPB    WTYPE,#0
3164 011764 001425      BEQ      ENDIT
3165 011766 123727 002414 000004      CMPB    WTYPE,#4      *MC?
3166 011774 001004      BNE      5$
3167 011776 012737 000001 002432      MOV      #1,TYPE
3168 012004 000415      BR      ENDIT
3169 012006 012737 007777 002436 5$:      MOV      #7777,MEMSZ
3170 012014 123727 002414 000006      CMPB    WTYPE,#6
3171 012022 001003      BNE      7$
3172 012024 012737 000001 002432      MOV      #1,TYPE
3173 012032 013737 002472 002470 7$:      MOV      RUNINH,RUNB
3174 012040
3175 012040 6$:
3176 012040      ENDIT:
3177 012040      L10036:  ENDINIT
3178 012040 104411      TRAP    C$INIT
3179
3180      .EVEN
3181 012042      BGNAUTO
3182 012042      L$AUTO::
3183
3184 012042 013701 002516      ;DEVICE DOES NOT HAVE A "READY"
3185 012046 012705 000004      MOV      KMCSR,R1      ;R1 CONTAINS BASE M8200,4,7 ADDRESS
3186 012052 012737 012104 000004      MOV      #4,R5      ;4 REGISTERS TO BE TESTED
3187 012060 012737 000240 000006      MOV      #2$,4      ;SET OUT TIMEOUT TRAP
3188 012066 005711      MOV      #240,6      ;LEVEL 7
3189 012070 000240      1$:      TST      (R1)      ;REFERENCE DEVICE REGISTERS
3190 012072 062701 000002      NOP
3191 012076 005305      ADD      #2,R1      ;NEXT REGISTER
3192 012100 001372      DEC      R5      ;DEC REGISTER COUNT
3193 012102 000405      BNE      1$      ;BR IF NOT LAST REGISTER
3194
3195 012104 062706 000004      2$:      ADD      #4,SP
3196 012110      DODU    LOGDEV
3197 012110 013700 002342      MOV      LOGDEV,R0
3198 012114 104451      TRAP    C$DODU
3199
3200 012116 013737 002464 000004 3$:      MOV      SAVE4,4
3201 012124 013737 002466 000006      MOV      SAVE6,6
    
```

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INITIALIZE SECTION

3202 012132  
3203 012132  
3204 012132 104461 .  
3205

L10037: ENDAUTO  
TRAP CSAUTO



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CLEANUP CODING SECTION

3206  
3207  
3208  
3209  
3210  
3211  
3212  
3213 012134  
3214 012134  
3215 012134  
3216 012134 104433  
3217  
3218 012136  
3219 012136  
3220 012136 104412  
3221  
3222  
3223  
3224  
3225

.SBTTL CLEANUP CODING SECTION

:/  
:/ THE CLEANUP CODING SECTION CONTAINS THE CODING THAT IS PERFORMED  
:/ AT THE END OF EACH PASS.  
:/

BGNCLN  
L\$CLEAN: :  
BRESET  
TRAP C\$RESET  
  
ENDCLN  
L10040: :  
TRAP C\$CLEAN

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DRCP UNIT SECTION

3226  
3227  
3228  
3229  
3230  
3231  
3232  
3233 012140  
3234 012140  
3235  
3236 012140  
3237 012140 104433  
3238 012142  
3239 012142  
3240 012142 104453  
3241  
3242  
3243  
3244  
3245

```
.SBTTL DROP UNIT SECTION
://////
:/ THE DROP-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE
:/ TO NO LONGER BE TESTED.
://////
          BGNDU
L$DU::
:ISSUE UNIBUS RESET TO CLEAN UP
          BRESET
          TRAP   C$RESET
          ENDDU
L10041:
          TRAP   C$DU
```

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ADD UNIT SECTION

3246  
3247  
3248  
3249  
3250  
3251  
3252  
3253  
3254  
3255  
3256  
3257  
3258  
3259  
3260  
3261  
3262  
3263  
3264

012144  
012144  
012144  
012144  
012144 104452

.SBTTL ADD UNIT SECTION  
:////////////////////  
:// THE ADD-UNIT SECTION CONTAINS THE CODING THAT CAUSES A DEVICE  
:// TO BE (A) TESTED FOR THE FIRST TIME, OR (B) RESUMED IN TESTING. IF  
:// 'EF.AUN!' IS SET, THE UNIT WILL BE TESTED AS A NEW UNIT.  
:////////////////////  
L\$AU:: BGNU  
L10042: ENDAU  
TRAP C\$AU

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HARDWARE TESTS

.SBTTL HARDWARE TESTS

;START OF CODE BLOCK WHICH IS USED AS DATA  
ROMMAP:

3265  
3266  
3267  
3268  
3269  
3270 012146  
3271  
3272 012146  
3273  
3274  
3275  
3276 012146  
3277  
3278  
3279 012146  
3280 012146  
3281 012146 013701 002516  
3282 012152 012705 000004  
3283 012156 012737 012214 000004  
3284 012164 012737 000240 000006  
3285 012172 005711  
3286 012174 000240  
3287 012176  
3288 012176 104410  
3289 012200 000054  
3290 012202 062701 000002  
3291 012206 005305  
3292 012210 001370  
3293 012212 000410  
3294  
3295 012214 062706 000004  
3296 012220  
3297 012224 104455  
3298 012226 000044  
3299 012230 005055  
3300 012232 010614  
3301  
3302 012234 013737 002464 000004  
3303 012242 013737 002466 000006  
3304 012250  
3305 012250 104410  
3306 012252 000002  
3307  
3308 012254  
3309 012254  
3310 012254 104401  
3311  
3312  
3313  
3314 012256  
3315  
3316  
3317  
3318  
3319 012256  
3320

BADHEAD  
:\*\*\*\*\* TEST 1 \*\*\*\*\*  
:•VERIFY THAT REFERENCING UNIBUS DEVICE REGISTERS  
:•DOES NOT CAUSE A TIME OUT TRAP  
BADHEAD  
:\*\*\*\*\* TEST 1 \*\*\*\*\*

BGNTST  
T1::

MOV KMCSR,R1 ;R1 CONTAINS BASE MB200,4,7 ADDRESS  
MOV #4,R5 ;4 REGISTERS TO BE TESTED  
MOV #2\$,4 ;SET OUT TIMEOUT TRAP  
MOV #240,6 ;LEVEL 7  
TST (R1) ;REFERENCE DEVICE REGISTERS  
NOP  
ESCAPE TST  
TRAP C\$ESCAPE  
.WORD L10043-  
ADD #2,R1 ;NEXT REGISTER  
DEC R5 ;DEC REGISTER COUNT  
BNE 1\$ ;BR IF NOT LAST REGISTER  
BR 3\$

2\$:

ADD #4,SP  
ERROR 36 ;TIME OUT ERROR  
TRAP C\$ERDF  
.WORD 36  
.WORD EMO  
.WORD ERR36

3\$:

MOV SAVE4,4  
MOV SAVE6,6  
ESCAPE TST  
TRAP C\$ESCAPE  
.WORD L10043-

ENDTST  
L10043:

TRAP C\$E1ST

.EVEN

BADHEAD  
:\*\*\*\*\* TEST 2 \*\*\*\*\*  
:•TEST OF BR RIGHT SHIFT  
:•VERIFY THAT A DEST OF BR RSH (011) OF A MICRO-INSTRUCTION  
:•SHIFTS THE RESULTING BR DATA RIGHT ONCE.  
BADHEAD  
:\*\*\*\*\* TEST 2 \*\*\*\*\*

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```

3321
3322 012256
3323 012256
3324
3325 012256
3326 012262 013701 002516
3327 012266 005011
3328 012270 012705 052525
3329 012274 010561 000004
3330 012300
3331 012300 004537 003044
3332 012304 120500
3333 012306
3334 012306 004537 003044
3335 012312 061620
3336 012314
3337 012314 004537 003044
3338 012320 061225
3339 012322 006005
3340 012324 005004
3341 012326 116104 000005
3342 012332 120504
3343 012334 001410
3344 012336
3345 012342 104455
3346 012344 000014
3347 012346 005055
3348 012350 007420
3349
3350 012352
3351 012352 104410
3352 012354 000044
3353 012356
3354 012356
3355 012356 004537 003044
3356 012362 061620
3357 012364
3358 012364 004537 003044
3359 012370 061225
3360 012372 006005
3361 012374 116104 000005
3362 012400 120504
3363 012402 001406
3364 012404
3365 012410 104455
3366 012412 000014
3367 012414 005055
3368 012416 007420
3369
3370 012420
3371 012420
3372 012420
3373 012420 104401
3374
3375 012422
3376

```

```

BGNTST
12::
MSTCLR
MOV KMCSR,R1
CLR (R1)
MOV #52525,R5
MOV R5,4(R1)
ROMCLK
JSR R5,,ROMCLK
120500
ROMCLK
JSR R5,,ROMCLK
061620
ROMCLK
JSR R5,,ROMCLK
061225
ROR R5
CLR R4
MOVB 5(R1),R4
CMPB R5,R4
BEQ 1$
ERROR 12
TRAP C$ERDF
.WORD 12
.WORD EMC
.WORD ERR12
ESCAPE TST
TRAP C$ESCAPE
.WORD L10044-.
1$:
ROMCLK
JSR R5,,ROMCLK
061620
ROMCLK
JSR R5,,ROMCLK
061225
ROR R5
MOVB 5(R1),R4
CMPB R5,R4
BEQ 2$
ERROR 12
TRAP C$ERDF
.WORD 12
.WORD EMC
.WORD ERR12
2$:
ENDTST
L10044:
TRAP C$ETST
BADHEAD
:..... TEST 3 .....

```

```

;R1 CONTAINS BASE MB200,4,7 ADDRESS
;MASTER CLEAR MB200,4,7
;R1 = MB200,4,7 BASE ADDRESS
;CLEAR SEL0
;START WITH 125
;PORT4 125
;NEXT WORD IS INSTRUCTION
;CLOCK INSTRUCTION
;PORT4 TO BR-REG
;NEXT WORD IS INSTRUCTION
;CLOCK INSTRUCTION
;BR RSH BR, SHIFT BR RIGHT
;NEXT WORD IS INSTRUCTION
;CLOCK INSTRUCTION
;PORT5 BR
;R5 = "EXPECTED"
;R4 = "FOUND"
;DID BR SHIFT RIGHT ONCE?
;BR IF YES
;BR RIGHT SHIFT ERROR
;SHOULD BE 52
;NEXT WORD IS INSTRUCTION
;CLOCK INSTRUCTION
;BR RSH BR, SHFT BR RIGHT AGAIN
;NEXT WORD IS INSTRUCTION
;CLOCK INSTRUCTION
;PORT5 BR
;R5 = "EXPECTED"
;R4 = "FOUND"
;DID BR SHIFT RIGHT?
;BR IF YES
;BR RIGHT SHIFT ERROR
;S/B 25

```

```

3377                                     : *IOP CRAM WRITE/READ TEST
3378                                     : *FLOAT A 1 THROUGH EACH CRAM LOCATION
3379 012422                               BADHEAD
3380                                     : ***** TEST 3 *****
3381
3382 012422                               BGNTST
3383 012422                               T3::
3384 012422
3385                                     MACEX
3386 012430 104432                       : DO NOT DO TEST IF M8200
3387 012432 000116                       TRAP C$EXIT
3388 012434                               .WORD L10045-.
3389 012434 013701 002516               MYINT
3390                                     MOV KMCSR,R1                               :RECORD DEVICE ADDR.
3391 012440 005037 002434               CLR MRO                               :R1 CONTAINS BASE M3200,4,7 ADDRESS
3392 012444 012702 000001               MOV #1,R2                               :MRO = CRAM ADDRESS
3393 012450                               ADR4:
3394 012450                               ADR5:
3395 012450 104404                       BGNSEG
3396 012452 012711 002000               TRAP C$BSEG
3397 012456 013761 002434 000004       3$: MOV #BIT10,(R1)                       :SET ROMO
3398 012464 010261 000006               MOV MRO,4(R1)                          :WRITE ADDRESS TO SEL4
3399 012470 052711 020000               MOV R2,6(R1)                            :LOAD SEL6 WITH WRITE DATA
3400 012474 016104 000006               BIS #BIT13,(R1)                         :WRITE SEL6 INTO CRAM
3401 012500 020204 000006               MOV 6(R1),R4                            :READ CRAM INTO "FOUND"
3402 012502 001410                       CMP R2,R4                               :IS DATA CORRECT?
3403 012504                               BEQ 4$                                   :BR IF OK
3404 012510 104455                       ERROR 1                                  :ERROR
3405 012512 000001                       TRAP C$ERDF
3406 012514 005055                       .WORD 1
3407 012516 006032                       .WORD EMO
3408 012520                               .WORD ERR1
3409 012520 104410                       ESCAPE SEG
3410 012522 000002                       TRAP C$ESCAPE
3411 012524                               .WORD 10000$-.
3412 012524                               4$: ENDSEG
3413 012524 104405                       10000$: TRAP C$ESEG
3414 012526 000241                       CLC                                       :CLEAR CARRY
3415 012530 006102                       ROL R2                                   :SHIFT WRITE DATA
3416 012532 001346                       BNE ADR5                                  :BSR IF NOT DONE THIS ADDRESS
3417 012534 005237 002434 002434       INC MRO                                   :BUMP TO NEXT CRAM ADDRESS
3418 012540 023737 002436 002434       CMP MEMSZ,MRO                             :DONE YET?
3419 012546 001336                       BNE ADR4                                  :BR IF NO
3420 012550                               5$:
3421 012550                               ENDTST
3422 012550                               L10045:
3423 012550 104401                       TRAP C$ETST
3424
3425 012552                               BADHEAD
3426                                     : ***** TEST 4 *****
3427                                     : *IOP CRAM WRITE/READ TEST
3428                                     : *FLOAT A 0 THROUGH EACH CRAM LOCATION
3429 012552                               BADHEAD
3430                                     : ***** TEST 4 *****
3431
3432 012552                               BGNTST

```

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```

3433 012552
3434 012552
3435
3436 012560 104432
3437 012562 000126
3438 012564
3439 012564 013701 002516
3440 012570
3441 012574 005037 002434
3442 012600 012702 000001
3443 012604
3444 012604
3445 012604 104404
3446 012606 005102
3447 012610 012711 002000
3448 012614 013761 002434 000004
3449 012622 010261 000006
3450 012626 052711 020000
3451 012632 016104 000006
3452 012636 020204
3453 012640 001410
3454 012642
3455 012646 104455
3456 012650 000001
3457 012652 005055
3458 012654 006032
3459 012656
3460 012656 104410
3461 012660 000002
3462 012662
3463 012662
3464 012662 104405
3465 012664 005102
3466 012666 000241
3467 012670 006102
3468 012672 001344
3469 012674 005237 002434
3470 012700 023737 002436 002434
3471 012706 001334
3472 012710
3473 012710
3474 012710
3475 012710 104401
3476
3477 012712
3478
3479
3480
3481
3482 012712
3483
3484
3485 012712
3486 012712
3487 012712
3488

```

```

T4::
MACEX
;DO NOT DO TEST IF M8200
TRAP C$EXIT
.WORD L10046-.
MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
MSTCLR ;MASTER CLEAR M8200,4,7
CLR MRO ;MRO = CRAM ADDRESS
MOV #1,R2 ;R2 = WRITE DATA

BGNSEG
TRAP C$BSEG
COM R2 ;MAKE IT A FLOATING ZERO
MOV #BIT10,(R1) ;SET ROMO
MOV MRO,4(R1) ;WRITE ADDRESS TO SEL4
MOV R2,6(R1) ;LOAD SEL6 WITH WRITE DATA
BIS #BIT13,(R1) ;WRITE SEL6 INTO CRAM
MOV 6(R1),R4 ;READ CRAM INTO "FOUND"
CMP R2,R4 ;IS DATA CORRECT?
BEQ 4$ ;BR IF OK
ERROR 1 ;ERROR
TRAP C$ERDF
.WORD 1
.WORD EMO
.WORD ERR1
ESCAPE SEG
TRAP C$ESCAPE
.WORD 10000$-.

4$:
10000$:
TRAP C$ESEG
COM R2 ;BACK TO FLOATING ONE
CLC ;CLEAR CARRY
ROL R2 ;SHIFT WRITE DATA
BNE ADR2 ;BR IF NOT DONE THIS ADDRESS
INC MRO ;BUMP TO NEXT CRAM ADDRESS
CMP MEMSZ,MRO ;DONE YET?
BNE ADR1 ;BR IF NO

5$:
ENDTST
L10046:
TRAP C$ETST

BADHEAD
;***** TEST 5 *****
;•IOP CRAM DUAL ADDRESSING TEST
;•WRITE EACH ADDRESS INTO ITSELF, READ EACH
;•ADDRESS TO VERIFY CORRECT ADDRESSING
BADHEAD
;***** TEST 5 *****

BGNTST
T5::
MACEX
;DO NOT DO TEST IF M8200

```

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3489	012720	104432			TRAP	C\$EXIT		
3490	012722	000230			.WORD	L10047-		
3491	012724				MYINT			
3492	012724	013701	002516		MOV	KMCSR,R1		:RECORD DEVICE ADDR.
3493								:R1 CONTAINS BASE M8200,4,7 ADDRESS
3494	012730				MSTCLR			:MASTER CLEAR M8200,4,7
3495	012734	005037	002434		CLR	MRO		:MRO =CRAM ADDRESS
3496	012740				BGNSEG			
3497	012740	104404			TRAP	C\$BSEG		
3498	012742	013702	002434	1\$:	MOV	MRO,R2		:SAVE R2 FOR TYPEOUT
3499	012746	012711	002000		MOV	#BIT10,(R1)		:SET ROMO
3500	012752	013761	002434	000004	MOV	MRO,4(R1)		:WRITE ADDRESS TO SEL4
3501	012760	013761	002434	000006	MOV	MRO,6(R1)		:LOAD SEL6 WITH WRITE DATA
3502	012766	052711	020000		BIS	#BIT13,(R1)		:WRITE CRAM
3503	012772				SKIP06	15\$		:IF M8206,SKIP NEXT INSTR.
3504					:GOTO	15\$ IF M8206		
3505	013002	005061	000006		CLR	6(R1)		:CLEAR SEL 6
3506	013006			15\$:				
3507	013006	016104	000006		MOV	6(R1),R4		:SHOULD READ BACK OWN ADDRESS
3508	013012	023704	002434		CMP	MRO,R4		:IS DATA CORRECT?
3509	013016	001410			BEQ	2\$		:BR IF YES
3510	013020				ERROR	1		:DATA ERROR
3511	013024	104455			TRAP	C\$ERDF		
3512	013026	000001			.WORD	1		
3513	013030	005055			.WORD	EMO		
3514	013032	006032			.WORD	ERR1		
3515	013034				ESCAPE	SEG		
3516	013034	104410			TRAP	C\$ESCAPE		
3517	013036	000002			.WORD	10000\$-		
3518	013040			2\$:	ENDSEG			
3519	013040			10000\$:				
3520	013040	104405			TRAP	C\$ESEG		
3521	013042				BGNSEG			
3522	013042	104404			TRAP	C\$BSEG		
3523	013044	005237	002434		INC	MRO		:BUMP TO NEXT ADDRESS
3524	013050	023737	002436	002434	CMP	MEMSZ,MRO		:DONE WRITING YET?
3525	013056	001331			BNE	1\$		:BR IF NO
3526	013060	005037	002434		CLR	MRO		:RESTART AT ADDRESS 0
3527	013064	013702	002434	3\$:	MOV	MRO,R2		:SAVE R2 FOR TYPEOUT
3528	013070	012711	002000		MOV	#BIT10,(R1)		:SET ROMO
3529	013074	013761	002434	000004	MOV	MRO,4(R1)		:SEL4 = CRAM ADDRESS
3530	013102	016104	000006		MOV	6(R1),R4		:READ CRAM INTO "FOUND"
3531	013106	023704	002434		CMP	MRO,R4		:IS DATA CORRECT?
3532	013112	001411			BEQ	4\$		:BR IF YES
3533	013114				ERROR	2		:DUAL ADDRESSING ERROR
3534	013120	104455			TRAP	C\$ERDF		
3535	013122	000002			.WORD	2		
3536	013124	005055			.WORD	EMO		
3537	013126	006160			.WORD	ERR2		
3538	013130				ESCAPE	SEG		
3539	013130	104410			TRAP	C\$ESCAPE		
3540	013132	000002			.WORD	10001\$-		
3541	013134				ENDSEG			
3542	013134			10001\$:				
3543	013134	104405			TRAP	C\$ESEG		
3544	013136			4\$:				:LOOP TO 3\$ IF SW09=1



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3545	013136	005237	002434		INC	MRO	:BUMP TO NEXT ADDRESS
3546	013142	023737	002436	002434	CMP	MEMSZ,MRO	:DONE WRITING YET?
3547	013150	001345			BNE	3\$	:BR IF NO
3548	013152						
3549	013152						
3550	013152						
3551	013152	104401			TRAP	C\$ETST	
3552							
3553							
3554	013154						
3555							
3556							
3557							
3558	013154						
3559							
3560							

5\$:  
ENDTST  
L10047:

BADHEAD  
:\*\*\*\*\* TEST 6 \*\*\*\*\*  
:\*IOP MAIN MEMORY TEST  
:\*FLOAT A 1 THROUGH ALL MAIN MEMORY LOCATIONS  
BADHEAD  
:\*\*\*\*\* TEST 6 \*\*\*\*\*

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3561	013154					BGNTST				
3562	013154					T6::				
3563	013154						MYINT			
3564	013154	013701	002516				MOV	KMCSR,R1		:RECORD DEVICE ADDR.
3565										:R1 CONTAINS BASE M8200,4,7 ADDRESS
3566	013160						MSTCLR			:MASTER CLEAR M8200,4,7
3567	013164	005037	002406				CLR	FLAG		:START WITH ADDRESS 0
3568	013170	012737	000001	002434	1\$:		MOV	#1,MRO		:START WITH BIT 0
3569	013176	042737	003777	013232	65\$:		BIC	#3777,66\$		:CLEAR ADDRESS FIELD OF INSTRUCTION

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3570 013204 042737 000037 013240 BIC #37,68\$ ;CLEAR ADDRESS FIELD OF INSTRUCTION

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3571	013212	153737	002406	015252		BISB	FLAG,66\$	:ADD ADDRESS TO INSTRUCTION?
3572	013220	153737	002407	013240		BISB	FLAG+1,68\$	:ADD ADDRESS TO INSTRUCTION
3573	013226					ROMCLK		:NEXT WORD IS INSTRUCTION,
3574	013226	004537	003044			JSR	R5,.ROMCLK	:CLOCK INSTRUCTION
3575	013232	010000			66\$:	010000		
3576	013234					ROMCLK		
3577	013234	004537	003044			JSR	R5,.ROMCLK	:CLOCK INSTRUCTION
3578	013240	004000			68\$:	004000		:LOAD MAR HI
3579	013242	013761	002434	000004		MOV	MRO,4(R1)	:WRITE PATTERN IN PORT4
3580	013250					ROMCLK		:NEXT WORD IS INSTRUCTION,
3581	013250	004537	003044			JSR	R5,.ROMCLK	:CLOCK INSTRUCTION
3582	013254	122500				122500		:MOVE PORT4 TO MEMORY
3583	013256					ROMCLK		:NEXT WORD IS INSTRUCTION,
3584	013256	004537	003044			JSR	R5,.ROMCLK	:CLOCK INSTRUCTION
3585	013262	040620				040620		:MOVE MEMORY TO BR
3586	013264					ROMCLK		:NEXT WORD IS INSTRUCTION,
3587	013264	004537	003044			JSR	R5,.ROMCLK	:CLOCK INSTRUCTION
3588	013270	061225				61225		:MOVE BR TO PORT5
3589	013272	013705	002434			MOV	MRO,R5	:PUT 'EXPECTED' IN R5
3590	013276	116104	000005			MOVB	5(R1),R4	:PUT 'FOUND' IN R4
3591	013302	120504				CMPB	R5,R4	:DATA CORRECT?
3592	013304	001410				BEQ	67\$	:BR IF YES
3593	013306					ERROR	6	:DATA ERROR
3594	013312	104455				TRAP	C\$ERDF	
3595	013314	000006				.WORD	6	
3596	013316	005055				.WORD	EMO	
3597	013320	006700				.WORD	ERR6	
3598	013322					ESCAPE	TST	
3599	013322	104410				TRAP	C\$ESCAPE	
3600	013324	000030				.WORD	L10050-	
3601	013326				67\$:			:SW09=1?
3602	013326	000241				CLC		:CLEAR CARRY
3603	013330	106137	002434			ROLB	MRO	:SHIFT BIT IN MRO
3604	013334	001320				BNE	65\$	:DONE IF MRO=0
3605	013336					BREAK		
3606	013336	104422				TRAP	C\$BRK	
3607	013340	005237	002406			INC	FLAG	:NEXT ADDRESS
3608	013344	023737	002436	002406		CMP	MEMSZ,FLAG	:LAST ADDRESS?
3609	013352	001306				BNE	1\$	:BR IF NO
3610	013354				2\$:			
3611	013354				ENDTST			
3612	013354				L10050:			
3613	013354	104401				TRAP	C\$ETST	
3614								
3615	013356					BADHEAD		
3616						:***** TEST 7 *****		
3617						:*IOP MAIN MEMORY TEST		
3618						:*FLOAT A 0 THROUGH ALL MAIN MEMORY LOCATIONS		
3619	013356					BADHEAD		
3620						:***** TEST 7 *****		
3621								
3622	013356				BGNTST			
3623	013356				T7::			
3624	013356					MYINT		
3625	013356	013701	002516			MOV	KMCSR,R1	:RECORD DEVICE ADDR.
3626								:R1 CONTAINS BASE M8200,4,7 ADDRESS

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3627 013362          MSTCLR          :MASTER CLEAR MB200,4,7
3628 013366 005037 002406          CLR          FLAG          :START WITH ADDRESS 0
3629 013372 012737 000001 002434 1$: MOV          #1,MRO        :START WITH BIT 0
3630 013400 005137 002434          COM          MRO         :CHANGE TO FLOATING 0
3631 013404 042737 003777 013440 64$: BIC          #3777,66$    :CLEAR ADDRESS FIELD OF INSTRUCTION
3632 013412 042737 000037 013446 65$: BIC          #37,68$     :CLEAR ADDRESS FIELD OF INSTRUCTION
3633 013420 153737 002406 013440          BISB         FLAG,66$     :ADD ADDRESS TO INSTRUCTION
3634 013426 153737 002407 013446          BISB         FLAG+1,68$  :ADD ADDRESS TO INSTRUCTION
3635 013434          ROMCLK          :NEXT WORD IS INSTRUCTION,
3636 013434 004537 003044          JSR          R5, .ROMCLK  :CLOCK INSTRUCTION
3637 013440 010000          66$: 010000          :LOAD MAR LO WITH ADDRESS IN FLAG
3638 013442          ROMCLK          :NEXT WORD IS INSTRUCTION,
3639 013442 004537 003044          JSR          R5, .ROMCLK  :CLOCK INSTRUCTION
3640 013446 004000          68$: 004000          :LOAD MAR HI
3641 013450 013761 002434 000004          MOV          MRO,4(R1)    :WRITE PATTERN IN PORT4
3642 013456          ROMCLK          :NEXT WORD IS INSTRUCTION,
3643 013456 004537 003044          JSR          R5, .ROMCLK  :CLOCK INSTRUCTION
3644 013462 122500          :MOVE PORT4 TO MEMORY
3645 013464          ROMCLK          :NEXT WORD IS INSTRUCTION,
3646 013464 004537 003044          JSR          R5, .ROMCLK  :CLOCK INSTRUCTION
3647 013470 040620          :MOVE MEMORY TO BR
3648 013472          ROMCLK          :NEXT WORD IS INSTRUCTION,
3649 013472 004537 003044          JSR          R5, .ROMCLK  :CLOCK INSTRUCTION
3650 013476 061225          :MOVE BR TO PORT5
3651 013500 013705 002434          MOV          MRO,R5      :PUT 'EXPECTED' IN R5
3652 013504 116104 000005          MOVB         5(R1),R4    :PUT 'FOUND' IN R4
3653 013510 120504          CMPB         R5,R4      :DATA CORRECT?
3654 013512 001406          BEQ          67$        :BR IF YES
3655 013514          ERROR          6          :DATA ERROR
3656 013520 104455          TRAP         C$ERDF
3657 013522 000006          .WORD        6
3658 013524 005055          .WORD        EMO
3659 013526 006700          .WORD        ERR6
3660 013530          67$: ESCAPE TST
3661 013530 104410          TRAP         C$ESCAPE
3662 013532 000034          .WORD        L10051-
3663 013534 005137 002434          COM          MRO         :CHANGE TO FLOATING 1
3664 013540 000241          CLC          :CLEAR CARRY
3665 013542 106137 002434          ROLB         MRO        :SHIFT BIT IN MRO
3666 013546 001314          BNE         64$        :DONE IF MRO=0
3667 013550          BREAK
3668 013550 104422          TRAP         C$BRK
3669 013552 005237 002406          INC          FLAG        :NEXT ADDRESS
3670 013556 023737 002436 002406          CMP          MEMSZ,FLAG  :LAST ADDRESS?
3671 013564 001302          BNE         1$        :BR IF NO
3672 013566          2$:
3673 013566          ENDTST
3674 013566          L10051:
3675 013566 104401          TRAP         C$ETST
3676
3677 013570          BADHEAD
3678          :***** TEST 8 *****
3679          :*IOP MAIN MEMORY DUAL ADDRESSING TEST
3680          :*LOAD EACH MEMORY LOCATION WITH ITS OWN ADDRESS
3681          :*READ BACK EACH LOCATION TO VERIFY CORRECT ADDRESSING
3682 013570          BADHEAD

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3739 014022 004000      8$: 004000      ;LOAD MAR HI
3740 014024      ROMCLK      ;NEXT WORD IS INSTRUCTION,
3741 014024 004537 003044 JSR      R5,.ROMCLK      ;CLOCK INSTRUCTION
3742 014030 040620      040620      ;MOVE MEMORY TO THE BR
3743 014032      ROMCLK      ;NEXT WORD IS INSTRUCTION,
3744 014032 004537 003044 JSR      R5,.ROMCLK      ;CLOCK INSTRUCTION
3745 014036 061225      61225      ;MOV BR TO PORT5
3746 014040 010205      MOV      R2,R5      ;PJT 'EXPECTED' IN R5
3747 014042 116104 000005 MOVB     5(R1),R4      ;PUT 'FOUND' IN R4
3748 014046 120504      CMPB     R5,R4      ;DATA CORRECT?
3749 014050 001406      BEQ      6$      ;BR IF YES
3750 014052      ERROR      6      ;ADDRESSING ERROR
3751 014056 104455      TRAP     C$ERDF      .
3752 014060 000006      .WORD    6
3753 014062 005055      .WORD    EMO
3754 014064 006700      .WORD    ERR6
3755 014066      6$: ESCAPE TST
3756 014066 104410      TRAP     C$ESCAPE
3757 014070 000020      .WORD    L10052-.
3758 014072      BREAK
3759 014072 104422      TRAP     C$BRK
3760 014074 005237 002406 INC      FLAG      ;NEXT ADDRESS
3761 014100 023737 002436 002406 CMP      MEMSZ,FLAG ;IS IT THE LAST
3762 014106 001325      BNE      4$      ;BR IF NO
3763 014110      9$:
3764 014110      ENDTST
3765 014110      L10052:
3766 014110 104401      TRAP     C$ETST
3767
3768 014112      BADHEAD
3769      ;***** TEST 9 *****
3770      ;*IOP MAR TEST
3771      ;*PERFORM DUAL ADDRESSING TEST
3772      ;*USING MAR AUTO-INC FEATURE
3773 014112      BADHEAD
3774      ;***** TEST 9 *****
3775
3776 014112      BGNTST
3777 014112      T9::
3778 014112      K4ONLY      ;FOR 4K CPUS ONLY.
3779      ;DO NOT DO TEST IF M8200, OR M8204
3780 014122 104432      TRAP     C$EXIT
3781 014124 000342      .WORD    L10053-.
3782 014126      MYINT
3783 014126 013701 002516 MOV      KMCSR,R1      ;RECORD DEVICE ADDR.
3784      ;R1 CONTAINS BASE M8200,4,7 ADDRESS
3785 014132      MSTCLR      ;MASTER CLEAR M8200,4,7
3786 014136 005002      CLR      R2      ;START WITH A ZERO
3787 014140 013703 002436 MOV      MEMSZ,R3      ;GET MEMORY SIZE
3788 014144 005203      INC      R3      ;STOP ADDR=MEMSZ+1
3789 014146      ROMCLK      ;NEXT WORD IS INSTRUCTION,
3790 014146 004537 003044 JSR      R5,.ROMCLK      ;CLOCK INSTRUCTION
3791 014152 010000      010000      ;LOAD MAR WITH A ZERO
3792 014154      CLRMAR
3793 014154 004537 003044 JSR      R5,.ROMCLK      ;CLOCK INSTRUCTION
3794 014162 010261 000004 1$: MOV      R2,4(R1)      ;WRITE DATA TO PORT4

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3795	014166			ROMCLK		:NEXT WORD IS INSTRUCTION,
3796	014166	004537	003044	JSR	R5, .ROMCLK	:CLOCK INSTRUCTION
3797	014172	136500		136500		:MEM PORT4, AUTO-INC MAR
3798	014174	005202		INC	R2	:INCREMENT DATA
3799	014176	020302		CMP	R3,R2	:DONE YET?
3800	014200	001370		BNE	1\$	:BR IF NO
3801	014202	005002		CLR	R2	:RESTART WITH A ZERO
3802	014204			ROMCLK		:NEXT WORD IS INSTRUCTION,
3803	014204	004537	003044	JSR	R5, .ROMCLK	:CLOCK INSTRUCTION
3804	014210	010000		010000		:LOAD MAR WITH A ZERO
3805	014212			CLRMAR		
3806	014212	004537	003044	JSR	R5, .ROMCLK	:CLOCK INSTRUCTION
3807	014220					
3808	014220			2\$:		
3809	014220	004537	003100	SROMCLK		:NEXT WORD IS INSTRUCTION,
3810	014224	055224		JSR	R5, .SROMCLK	
3811	014226	010205		055224		:MOVE MEM TO PORT4
3812	014230	116104	000004	MOV	R2,R5	:PUT 'EXPECTED' IN R5
3813	014234	120504		MOV	4(R1),R4	:PUT 'FOUND' IN R4
3814	014236	001406		CMPI	R5,R4	:DATA CORRECT?
3815	014240			BEQ	3\$	:BR IF YES
3816	014244	104455		ERROR	11	:MAR ERROR
3817	014246	000013		TRAP	C\$ERDF	
3818	014250	005055		.WORD	11	
3819	014252	007276		.WORD	EMO	
3820	014254			.WORD	ERR11	
3821	014254	004537	003100	3\$:	SROMCLK	
3822	014260	000000		JSR	R5, .SROMCLK	
3823	014262	005004		0		:DUMP NOP INSTR. TO CLK AUTO INC IN MAR.
3824	014264			CLR	R4	
3825	014264	004537	003044	ROMCLK		:READ IBUS* <15> (MAR HIGH)
3826	014270	121325		JSR	R5, .ROMCLK	:CLOCK INSTRUCTION
3827				121325		:MAR HIGH _POT 5
3828	014272			ROMCLK		:READ IBUS* <14> (MAR LOW)
3829	014272	004537	003044	JSR	R5, .ROMCLK	:CLOCK INSTRUCTION
3830	014276	121304		121304		
3831	014300	016104	000004	MOV	4(R1),R4	:ADD TO MAR HIGH.
3832	014304	042704	160000	BIC	#160000,R4	
3833	014310	005202		INC	R2	
3834	014312	020237	002436	CMP	R2, MEMSZ	
3835	014316	001002		BNE	35\$	
3836	014320	052702	010000	BIS	#10000,R2	:IF AT HIGH LIMIT,ADD IN OVERFLOW BIT.
3837	014324			35\$:		
3838	014324	020204		CMP	R2,R4	:ADDR. OK?
3839	014326	001406		BEQ	4\$	
3840	014330			ERROR	11	:ERROR MAR ADDR. BAD IN IBUS <14>AND <15>
3841	014334	104455		TRAP	C\$ERDF	
3842	014336	000013		.WORD	11	
3843	014340	005055		.WORD	EMO	
3844	014342	007276		.WORD	ERR11	
3845						:EXPECTED (R4) IS COMBINATION OF
3846						:IBUS* <14> AND <15>
3847	014344			4\$:		
3848	014344			ESCAPE	TST	
3849	014344	104410		TRAP	C\$ESCAPE	
3850	014346	000120		.WORD	L10053-	



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3851 014350          BREAK
3852 014350 104422  TRAP      C$BRK
3853 014352 032702 010000 BIT      #10000,R2      ;DONE YET?
3854 014356 J01720  BEQ      2$
3855
3856                ;*THIS SECTION OF CODE ADDED TO MAKE SURE
3857                ;*THAT MASTER CLEAR, CLEARS THE MAR
3858                ;*
3859
3860 014360          SKIP06 40$
3861                ;GOTO 40$ IF M8206
3862 014370 005737 002470 TST     RUNB
3863 014374 001034      BNE     40$
3864 014376 005737 002472 TST     RUNINH
3865 014402 001031      BNE     40$
3866 014404 052711 040000 BIS     #40000,(R1)   ;SET MASTER CLEAR
3867 014410 005011      CLR     (R1)        ;CLEAR MASTER CLEAR
3868 014412          ROMCLK      ;WE MUST FIRST CLOCK
3869 014412 004537 003044 JSR     R5,.,ROMCLK  ;CLOCK INSTRUCTION
3870 014416 121325      121325  ;THE MAR LATCH REGS
3871 014420          ROMCLK      ;BEFORE WE CAN READ THEM
3872 014420 004537 003044 JSR     R5,.,ROMCLK  ;CLOCK INSTRUCTION
3873 014424 121304      121304
3874 014426          ROMCLK      ;READ IBUS* <15> PUT IN PORT5
3875 014426 004537 003044 JSR     R5,.,ROMCLK  ;CLOCK INSTRUCTION
3876 014432 121325      121325  ;MAR HIGH
3877 014434          ROMCLK      ;READ IBUS* <14>, PUT IN PORT4
3878 014434 004537 003044 JSR     R5,.,ROMCLK  ;CLOCK INSTRUCTION
3879 014440 121304      121304  ;MAR LOW
3880 014442 005002      CLR     R2          ;EXPECT MAR CLEAR
3881 014444 016104 000004 MOV     = 4(R1),R4   ;READ PORTS 4&5. THEY CONTAIN
3882                ;THE CONTENTS OF THE MAR
3883                ;MASTER CLEAR SHOULD HAVE
3884                ;CLEARED THE MAR
3885                ;BRANCH END TST IF CLEAR
3886 014450 001406      BEQ     40$
3887 014452          ERROR     44
3888 014456 104455      TRAP    C$ERDF
3889 014460 000054      .WORD  44
3890 014462 005055      .WORD  EMO
3891 014464 011054      .WORD  ERR44
3892 014466          40$:
3893 014466          ENDTST
3894 014466          L10053:
3895 014466 104401      TRAP    C$ETST
3896
3897 014470          BADHEAD
3898                ;***** TEST 10 *****
3899                ;*JOP (CRAM) ODT BITS TEST
3900                ;*LOAD MAR WITH A 0 INC MAR UNTIL IT OVERFLOWS
3901                ;*VERIFY THAT IBUS* 10 BITS IS SET ONLY WHEN MAR BIT 8 IS A ONE
3902                ;*AND THAT IBUS* 10 BIT6 IS SET ON MAR OVERFLOW
3903 014470          BADHEAD
3904                ;***** TEST 10 *****
3905
3906 014470          BGN1ST

```

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```

3907 014470          T10::
3908 014470          MACEX
3909                ;DO NOT DO TEST IF M8200
3910 014476 104432   TRAP C$EXIT
3911 014500 000234   .WORD L10054-.
3912 014502          MYINT
3913 014502 013701 002516 MOV KMCSR,R1
3914                ;RECORD DEVICE ADDR.
3915 014506          MSTCLR          ;R1 CONTAINS BASE M8200,4,7 ADDRESS
3916 014512 005002   CLR R2          ;MASTER CLEAR M8200,4,7
3917 014514          ROMCLK          ;R2=SAME AS MAR CONTENTS
3918 014514 004537 003044 JSR R5,ROMCLK  ;NEXT WORD IS INSTRUCTION,
3919 014520 010000   010000          ;CLOCK INSTRUCTION
3920 014522          15:          ;MAR_0
3921 014522          ROMCLK          ;NEXT WORD IS INSTRUCTION,
3922 014522 004537 003044 JSR R5,ROMCLK  ;CLOCK INSTRUCTION
3923 014526 121204   121204          ;PORT4=IBUS*10
3924 014530 005005   CLR R5          ;R5='EXPECTED'
3925 014532 032702 000400 BIT #BIT8,R2   ;IS BIT8 SET IN MAR?
3926 014536 001402   BEQ .+6          ;BR IF NO
3927 014540 012705 000040 MOV #BIT5,R5   ;IF YES THEN SET BITS
3928 014544 016104 000004 MOV 4(R1),R4   ;R4='FOUND'
3929 014550 042704 177637 BIC #177637,R4 ;CLEAR UNWANTED BITS
3930 014554 020504   CMP R5,R4      ;BITS 5&6 SHOULD BE CLEAR
3931 014556 001410   BEQ 15$          ;BR IF OK
3932 014560          ERROR 7          ;ERROR BITS 5&6 NOT CLEAR
3933 014564 104455   TRAP C$ERDF
3934 014566 000007   .WORD 7
3935 014570 005055   .WORD EMO
3936 014572 007026   .WORD ERR7
3937 014574          ESCAPE TST
3938 014574 104410   TRAP C$ESCAPE
3939 014576 000136   .WORD L10054-.
3940 014600          15$:
3941 014600          ROMCLK          ;NEXT WORD IS INSTRUCTION,
3942 014600 004537 003044 JSR R5,ROMCLK  ;CLOCK INSTRUCTION
3943 014604 014000   014000          ;INC MAR
3944 014606 005202   INC R2          ;BUMP MEM ADDRESS
3945 014610 022702 002000 CMP #2000,R2   ;OVERFLOWED YET?(OVFL PAGE BITS).
3946 014614 001342   BNE 15$          ;BR IF NO
3947 014616          ROMCLK          ;NEXT WORD IS INSTRUCTION,
3948 014616 004537 003044 JSR R5,ROMCLK  ;CLOCK INSTRUCTION
3949 014622 121204   121204          ;PART4 IBUS* 10
3950 014624 012705 000100 MOV #BIT6,R5   ;R5='EXPECTED'
3951 014630 016104 000004 MOV 4(R1),R4   ;R4='FOUND'
3952 014634 042704 177627 BIC #177627,R4 ;CLEAR UNWANTED BITS
3953 014640 020504   CMP R5,R4      ;BIT6 SHOULD BE SET
3954 014642 001406   BEQ 17$          ;BR IF OK
3955 014644          ERROR 7          ;ERROR, BIT6 NOT SET
3956 014650 104455   TRAP C$ERDF
3957 014652 000007   .WORD 7
3958 014654 005055   .WORD EMO
3959 014656 007026   .WORD ERR7
3960 014660          17$:
3961 014660 004537 003044 ROMCLK          ;NEXT WORD IS INSTRUCTION,
3962 014664 010000   JSR R5,ROMCLK  ;CLOCK INSTRUCTION

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3963 014666 ROMCLK ;NEXT WORD IS INSTRUCTION,
3964 014666 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
3965 014672 004000 004000 ;MAR HI 0
3966 014674 ROMCLK ;NEXT WORD IS INSTRUCTION,
3967 014674 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
3968 014700 121204 121204 ;PORT4 IBUS= 10
3969 014702 005005 CLR R5 ;R5='EXPECTED'
3970 014704 016104 000004 MOV 4(R1),R4 ;R4='FOUND'
3971 014710 042704 177637 BIC #177637,R4 ;CLEAR UNWANTED BITS
3972 014714 020504 CMP R5,R4 ;BITS 5&6 SHOULD BE CLEAR
3973 014716 001406 BEQ 2$ ;BR IF OK
3974 014720 ERROR 7 ;ERROR 5&6 NOT BOTH CLEAR
3975 014724 104455 TRAP C$ERDF
3976 014726 000007 .WORD 7
3977 014730 005055 .WORD EMO
3978 014732 007026 .WORD ERR7
3979 014734
3980 014734
3981 014734
3982 014734 104401 2$:
3983 ENDTST
3984 014736 L10054: TRAP C$ETST
3985 BADHEAD
3986 ***** TEST 11 *****
3987 ;*CRAM TEST OF JUMP(I) NEVER MICRO-PROCESSOR INSTRUCTION.
3988 ;*PERFORM THE JUMP INSTRUCTION
3989 ;*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
3990 ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
3991 ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
3992 ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
3993 ;*THE CRAM PC IS CORRECT. IF THE CRAM PC IS NOT RIGHT,
3994 ;*THEN PORT4 CONTAINS A 37
3995 BADHEAD
3996 ***** TEST 1: *****
3997
3998
3999
4000
4001 014746 SKIP04 10$
4002 014746 ;GOTO 10$ IF M8204
4003 014750 104432 EXIT TST ;CAN'T DO IF ROM,4k
4004 014752 000230 TRAP C$EXIT
4005 014752 10$: .WORD L10055-.
4006 014752 013701 002516 MYINT
4007 MOV KMCSR,R1 ;RECORD DEVICE ADDR.
4008 ;R1 CONTAINS BASE M8200,4,7 ADDRESS
4009 ;MASTER CLEAR M8200,4,7
4010 014762 MSTCLR
4011 014762 104404 BGNSEG
4012 014764 004737 003474 TRAP C$BSEG
4013 014770 004737 003166 JSR PC,MEMSET ;SET MEM AND RAM
4014 014774 JSR PC,CLRALL ;CLEAR ALL CONDITIONS
4015 014774 004537 003100 SROMCLK ;NEXT WORD IS INSTRUCTION,
4016 015000 100400 JSR R5,.SROMCLK
4017 015002 SROMCLK ;START AT ROM PC=0
4018 015002 004537 003100 JSR R5,.SROMCLK ;NEXT WORD IS INSTRUCTION,

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4019	015006	114377		114377!<400*0>	:JUMP TO ROM PC OF 1777
4020	015010	004737	003330	JSR PC,RAMDAT	:R4=(CRAM PC (LSB 8 BITS)
4021	015014	000001		1	:EXPECTED DATA
4022	015016	120504		CMPB R5,R4	:IS ROM PC CORRECT?
4023	015020	001406		BEQ 28	:BR IF NO
4024	015022			ERROR 5	:ERROR, CRAM PC IS WRONG
4025	015026	104455		TRAP C\$ERDF	
4026	015030	000005		.WORD 5	
4027	015032	005055		.WORD EMO	
4028	015034	006556		.WORD ERR5	
4029	015036			ESCAPE SEG	
4030	015036	104410		TRAP C\$ESCAPE	
4031	015040	000002		.WORD 10000\$-	
4032	015042			ENDSEG	
4033	015042				
4034	015042	104405		TRAP C\$ESEG	
4035	015044			BGNSEG	
4036	015044	104404		TRAP C\$BSEG	
4037	015046	004737	003166	JSR PC,CLRALL	:CLEAR ALL CONDITIONS
4038	015052			SROMCLK	:NEXT WORD IS INSTRUCTION.
4039	015052	004537	003100	JSR R5,.SROMCLK	
4040	015056	100403		100403	:START AT ROM PC=3
4041	015060			SROMCLK	:NEXT WORD IS INSTRUCTION.
4042	015060	004537	003100	JSR R5,.SROMCLK	
4043	015064	100000		100000!<400*0>	:JUMP TO ROM PC OF 0
4044	015066	004737	003330	JSR PC,RAMDAT	:R4=(CRAM PC (LSB 8 BITS)
4045	015072	000004		4	:EXPECTED DATA
4046	015074	120504		CMPB R5,R4	:IS ROM PC CORRECT?
4047	015076	001406		BEQ 48	:BR IF YES
4048	015100			ERROR 5	:ERROR, CROM PC IS WRONG
4049	015104	104455		TRAP C\$ERDF	
4050	015106	000005		.WORD 5	
4051	015110	005055		.WORD EMO	
4052	015112	006556		.WORD ERR5	
4053	015114			ESCAPE SEG	
4054	015114	104410		TRAP C\$ESCAPE	
4055	015116	000002		.WORD 10001\$-	
4056	015120			ENDSEG	
4057	015120				
4058	015120	104405		TRAP C\$ESEG	
4059	015122			BGNSEG	
4060	015122	104404		TRAP C\$BSEG	
4061	015124	004737	003166	JSR PC,CLRALL	:CLEAR ALL CONDITINS
4062	015130			SROMCLK	:NEXT WORD IS INSTRUCTION.
4063	015130	004537	003100	JSR R5,.SROMCLK	
4064	015134	100406		100406	:START AT ROM PC=6
4065	015136			SROMCLK	:NEXT WORD IS INSTRUCTION.
4066	015136	004537	003100	JSR R5,.SROMCLK	
4067	015142	104125		104125!<400*0>	:JUMP TO ROM PC OF 525
4068	015144	004737	003330	JSR PC,RAMDAT	:R4=(CRAM PC (LSB 8 BITS)
4069	015150	000007		7	:EXPECTED DATA
4070	015152	120504		CMPB R5,R4	:IS ROM PC CORRECT?
4071	015154	001406		BEQ 68	:BR IF YES
4072	015156			ERROR 5	:ERROR, CRAM PC IS WRONG
4073	015162	104455		TRAP C\$ERDF	
4074	015164	000005		.WORD 5	

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4075 015166 005055  
 4076 015170 006556  
 4077 015172  
 4078 015172 104410  
 4079 015174 000002  
 4080 015176  
 4081 015176  
 4082 015176 104405  
 4083 015200  
 4084 015200  
 4085 015200 104401  
 4086  
 4087 015202  
 4088  
 4089  
 4090  
 4091  
 4092  
 4093  
 4094  
 4095  
 4096  
 4097 015202  
 4098  
 4099  
 4100 015202  
 4101 015202  
 4102 015202  
 4103  
 4104 015212 104432  
 4105 015214 000214  
 4106 015216  
 4107 015216 013701 002516  
 4108  
 4109 015222  
 4110 015226 004737 003474  
 4111 015232  
 4112 015232 104404  
 4113 015234  
 4114 015234 004537 003100  
 4115 015240 100400  
 4116 015242  
 4117 015242 004537 003100  
 4118 015246 114777  
 4119 015250 004737 003330  
 4120 015254 000377  
 4121 015256 120504  
 4122 015260 001406  
 4123 015262  
 4124 015266 104455  
 4125 015270 000005  
 4126 015272 005055  
 4127 015274 006556  
 4128 015276  
 4129 015276 104410  
 4130 015300 000002

```

6$: .WORD EMO
     .WORD ERR5
     ESCAPE SEG
     TRAP C$ESCAPE
     .WORD 10002$-.
     ENDSEG

10002$: TRAP C$ESEG

ENDTST
L10055: TRAP C$ETST

BADHEAD
:***** TEST 12 *****
:*CRAM TEST OF JUMP(I) ALWAYS MICRO-PROCESSOR INSTRUCTION.
:*PERFORM THE JUMP INSTRUCTION
:*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
:*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
:*THEN PORT4 WILL CONTAIN A 37
BADHEAD
:***** TEST 12 *****

BGNTST
T12::
MACEX2 ;DON'T DO IF M8200
:DO NOT DO TEST IF M8200
TRAP C$EXIT
.WORD L10056-.
MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
;R1 CONTAINS BASE M8200,4,7 ADDRESS
;MASTER CLEAR M8200,4,7
;SET MEM AND RAM

1$: MSTCLR
JSR PC,MEMSET
BGNSEG
TRAP C$BSEG ;NEXT WORD IS INSTRUCTION.
SROMCLK R5,.SROMCLK ;START AT ROM PC=0
100400 ;NEXT WORD IS INSTRUCTION.
SROMCLK R5,.SROMCLK
JSR 114377!<400*1> ;JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
377 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 2$ ;BR IF YES
ERROR 5 ;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5

2$: ESCAPE SEG
TRAP C$ESCAPE
.WORD 10000$-.

```

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4131 015302  
4132 015302  
4133 015302 104405  
4134 015304  
4135 015304 104404  
4136 015306  
4137 015306 004537 003100  
4138 015312 100403  
4139 015314  
4140 015314 004537 003100  
4141 015320 100400  
4142 015322 004737 003330  
4143 015326 000000  
4144 015330 120504  
4145 015332 001406  
4146 015334  
4147 015340 104455  
4148 015342 000005  
4149 015344 005055  
4150 015346 006556  
4151 015350  
4152 015350 104410  
4153 015352 000002  
4154 015354  
4155 015354  
4156 015354 104405  
4157 015356  
4158 015356 104404  
4159 015360  
4160 015360 004537 003100  
4161 015364 100406  
4162 015366  
4163 015366 004537 003100  
4164 015372 104525  
4165 015374 004737 003330  
4166 015400 000125  
4167 015402 120504  
4168 015404 001406  
4169 015406  
4170 015412 104455  
4171 015414 000005  
4172 015416 005055  
4173 015420 006556  
4174 015422  
4175 015422 104410  
4176 015424 000002  
4177 015426  
4178 015426  
4179 015426 104405  
4180 015430  
4181 015430  
4182 015430 104401  
4183  
4184 015432  
4185  
4186

```

ENDSEG
10000$: TRAP C$ESEG
        BGNSEG
        TRAP C$BSEG
        SROMCLK ;NEXT WORD IS INSTRUCTION,
        JSR R5,.SROMCLK
        100403 ;START AT ROM PC=3
        SROMCLK ;NEXT WORD IS INSTRUCTION,
        JSR R5,.SROMCLK
        100000!<400*1> ;JUMP TO ROM PC OF 0
        JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
        0 ;EXPECTED DATA
        CMPB R5,R4 ;IS ROM PC CORRECT?
        BEQ 4$ ;BR IF YES
        ERROR 5 ;ERROR, CRAM PC IS WRONG
        TRAP C$ERDF
        .WORD 5
        .WORD EMO
        .WORD ERR5
4$: ESCAPE SEG
        TRAP C$ESCAPE
        .WORD 10001$-.
        ENDSEG
10001$: TRAP C$ESEG
        BGNSEG
        TRAP C$BSEG
        SROMCLK ;NEXT WORD IS INSTRUCTION,
        JSR R5,.SROMCLK
        100406 ;START AT ROM PC=6
        SROMCLK ;NEXT WORD IS INSTRUCTION,
        JSR R5,.SROMCLK
        104125!<400*1> ;JUMP TO ROM PC OF 525
        JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
        125 ;EXPECTED DATA
        CMPB R5,R4 ;IS ROM PC CORRECT?
        BEQ 6$ ;BR IF YES
        ERROR 5 ;ERROR, CRAM PC IS WRONG
        TRAP C$ERDF
        .WORD 5
        .WORD EMO
        .WORD ERR5
6$: ESCAPE SEG
        TRAP C$ESCAPE
        .WORD 10002$-.
        ENDSEG
10002$: TRAP C$ESEG
ENDTST
L10056: TRAP C$ETST
BADHEAD
***** TEST 13 *****
:CRAM TEST OF JUMP(1) ON C BIT SET MICRO-PROCESSOR INSTRUCTION.

```

```

4187
4188
4189
4190
4191
4192
4193
4194 015432
4195
4196
4197 015432
4198 015432
4199 015432
4200
4201 015442 104432
4202 015444 000230
4203 015446
4204 015446 013701 002516
4205
4206 015452
4207 015456 004737 003474
4208 015462
4209 015462 104404
4210 015464 004737 003260
4211 015470
4212 015470 004537 003100
4213 015474 100400
4214 015476
4215 015476 004537 003100
4216 015502 115377
4217 015504 004737 003330
4218 015510 000377
4219 015512 120504
4220 015514 001406
4221 015516
4222 015522 104455
4223 015524 000005
4224 015526 005055
4225 015530 006556
4226 015532
4227 015532
4228 015532 104410
4229 015534 000002
4230 015536
4231 015536
4232 015536 104405
4233 015540
4234 015540 104404
4235 015542 004737 003260
4236 015546
4237 015546 004537 003100
4238 015552 100403
4239 015554
4240 015554 004537 003100
4241 015560 101000
4242 015562 004737 003330

```

```

; *SET THE C BIT, PERFORM THE JUMP INSTRUCTION.
; *VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
; *IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
; *BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
; *THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
; *THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
; *THEN PORT4 WILL CONTAIN A 37
BADHEAD
; ***** TEST 13 *****

BGNTST
T13::
MACEX2
; DON'T DO IF M8200
; DO NOT DO TEST IF M8200
TRAP C$EXIT
; R1 CONTAINS BASE M8200,4,7 ADDRESS
; MASTER CLEAR M8200,4,7
; SET MEM AND RAM
; RECORD DEVICE ADDR.
; R1 CONTAINS BASE M8200,4,7 ADDRESS
; SET MEM AND RAM
; SET THE C BIT
; NEXT WORD IS INSTRUCTION,
; START AT ROM PC=0
; NEXT WORD IS INSTRUCCION,
; JUMP TO ROM PC OF 1777
; R4=CRAM PC (LSB 8 BITS)
; EXPECTED DATA
; IS ROM PC CORRECT?
; BR IF YES
; ERROR, CRAM PC IS WRONG
; LOOP TO 1$ IF SW09=1
; ESCAPE SEG
; R4=CRAM PC (LSB 8 BITS)
; SET THE C BIT
; NEXT WORD IS INSTRUCTION,
; START AT ROM PC=3
; NEXT WORD IS INSTRUCTION,
; JUMP TO ROM PC OF 0
; R4=CRAM PC (LSB 8 BITS)

```

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4243 015566 000000      0
4244 015570 120504      CMPB    R5,R4      ;EXPECTED DATA
4245 015572 001406      BEQ     4$         ;IS ROM PC CORRECT?
4246 015574      ERROR   5         ;BR IF YES
4247 015600 104455      TRAP   C$ERDF     ;ERROR, CRAM PC IS WRONG
4248 015602 000005      .WORD  5
4249 015604 005055      .WORD  EMO
4250 015606 006556      .WORD  ERR5
4251 015610      4$:           ;LOOP TO 3$ IF SW09=1
4252 015610      ESCAPE SEG
4253 015610 104410      TRAP   C$ESCAPE
4254 015612 000002      .WORD  10001$-.
4255 015614      ENDSEG
4256 015614      10001$:
4257 015614 104405      TRAP   C$ESEG
4258 015616      BGNSEG
4259 015616 104404      TRAP   C$BSEG
4260 015620 004737 003260      JSR    PC,SETC    ;SET THE C BIT'
4261 015624      SROMCLK          ;NEXT WORD IS INSTRUCTION,
4262 015624 004537 003100      JSR    R5,..SROMCLK
4263 015630 100406      100406          ;START AT ROM PC=6
4264 015632      SROMCLK          ;NEXT WORD IS INSTRUCTION,
4265 015632 004537 003100      JSR    R5,..SROMCLK
4266 015636 105125      104125!<400*2> ;JUMP TO ROM PC OF 525
4267 015640 004737 003330      JSR    PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
4268 015644 000125      125            ;EXPECTED DATA
4269 015646 120504      CMPB    R5,R4      ;IS ROM PC CORRECT?
4270 015650 001406      BEQ     6$         ;BR IF YES
4271 015652      ERROR   5         ;ERROR, CRAM PC IS WRONG
4272 015656 104455      TRAP   C$ERDF
4273 015660 000005      .WORD  5
4274 015662 005055      .WORD  EMO
4275 015664 006556      .WORD  ERR5
4276 015666      6$:           ESCAPE SEG
4277 015666 104410      TRAP   C$ESCAPE
4278 015670 000002      .WORD  10002$-.
4279 015672      ENDSEG
4280 015672      10002$:
4281 015672 104405      TRAP   C$ESEG
4282 015674      ENDTST
4283 015674      L10057:
4284 015674 1044^1      TRAP   C$ETST
4285
4286 015676      BADHEAD
4287      ;***** TEST 14 *****
4288      ;*CRAM TEST OF JUMP(1) ON Z BIT SET MICRO-PROCESSOR INSTRUCTION.
4289      ;*SET THE Z BIT, PERFORM THE JUMP INSTRUCTION.
4290      ;*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
4291      ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
4292      ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
4293      ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
4294      ;*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
4295      ;*THEN PORT4 WILL CONTAIN A 37
4296 015676      BADHEAD
4297      ;***** TEST 14 *****
4298

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4299 015676
4300 015676
4301 015676
4302
4303 015706 104432
4304 015710 000230
4305 015712
4306 015712 013701 002516
4307
4308 015716
4309 015722 004737 003474
4310 015726
4311 015726 104404
4312 015730 004737 003312
4313 015734
4314 015734 004537 003100
4315 015740 100400
4316 015742
4317 015742 004537 003100
4318 015746 115777
4319 015750 004737 003330
4320 015754 000377
4321 015756 120504
4322 015760 001406
4323 015762
4324 015766 104455
4325 015770 000005
4326 015772 005055
4327 015774 006556
4328 015776
4329 015776 104410
4330 016000 000002
4331 016002
4332 016002
4333 016002 104405
4334 016004
4335 016004 104404
4336 016006 004737 003312
4337 016012
4338 016012 004537 003100
4339 016016 100403
4340 016020
4341 016020 004537 003100
4342 016024 101400
4343 016026 004737 003330
4344 016032 000000
4345 016034 120504
4346 016036 001406
4347 016040
4348 016044 104455
4349 016046 000005
4350 016050 005055
4351 016052 006556
4352 016054
4353 016054 104410
4354 016056 000002

BGNTST
T14::
MACEX2
;DO NOT DO TEST IF M8200
TRAP C$EXIT
.WORD L10060-.
MYINT
MOV KMCSR,R1
;RECORD DEVICE ADDR.
;R1 CONTAINS BASE M8200,4,7 ADDRESS
;MASTER CLEAR M8200,4,7
;SET MEM AND RAM

1$:
BGNSEG
JSR PC,MEMSET
TRAP C$BSEG
JSR PC,SETZ
;SET THE Z BIT'
;NEXT WORD IS INSTRUCTION,
SROMCLK
JSR R5, .SROMCLK
100400
;START AT ROM PC=0
SROMCLK
JSR R5, .SROMCLK
114377! <400*3>
;JUMP TO ROM PC OF 1777
JSR PC,RAMDAT
;R4=CRAM PC (LSB 8 BITS)
377
;EXPECTED DATA
CMPB R5,R4
;IS ROM PC CORRECT?
BEQ 2$
;BR IF YES
ERROR 5
;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5
2$:
ESCAPE SEG
TRAP C$ESCAPE
.WORD 10000$-.
ENDSEG

10000$:
TRAP C$ESEG
BGNSEG
TRAP C$BSEG
JSR PC,SETZ
;SET THE Z BIT'
;NEXT WORD IS INSTRUCTION,
SROMCLK
JSR R5, .SROMCLK
100403
;START AT ROM PC=3
SROMCLK
;NEXT WORD IS INSTRUCTION,
JSR R5, .SROMCLK
100000! <400*3>
;JUMP TO ROM PC OF 0
JSR PC,RAMDAT
;R4=CRAM PC (LSB 8 BITS)
0
;EXPECTED DATA
CMPB R5,R4
;IS ROM PC CORRECT?
BEQ 4$
;BR IF YES
ERROR 5
;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5
4$:
ESCAPE SEG
TRAP C$ESCAPE
.WORD 10001$-.

```

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HARDWARE TESTS

4355 016060  
4356 016060  
4357 016060 104405  
4358 016062  
4359 016062 104404  
4360 016064 004737 003312  
4361 016070  
4362 016070 004537 003100  
4363 016074 100406  
4364 016076  
4365 016076 004537 003100  
4366 016102 105525  
4367 016104 004737 003330  
4368 016110 000125  
4369 016112 120504  
4370 016114 001406  
4371 016116  
4372 016122 104455  
4373 016124 000005  
4374 016126 005055  
4375 016130 006556  
4376 016132  
4377 016132 104410  
4378 016134 000002  
4379 016136  
4380 016136  
4381 016136 104405  
4382 016140  
4383 016140  
4384 016140 104401  
4385  
4386 016142  
4387  
4388  
4389  
4390  
4391  
4392  
4393  
4394  
4395  
4396 016142  
4397  
4398  
4399 016142  
4400 016142  
4401 016142  
4402  
4403 016152 104432  
4404 016154 000230  
4405 016156  
4406 016156 013701 002516  
4407  
4408 016162  
4409 016166 004737 003474  
4410 016172

```

10001$: ENDSEG
TRAP C$ESEG
BGNSEG
TRAP C$BSEG
JSR PC,SETZ ;SET THE Z BIT
SROMCLK ;NEXT WORD IS INSTRUCTION,
JSR R5,.SROMCLK
100406 ;START AT ROM PC=6
SROMCLK ;NEXT WORD IS INSTRUCTION,
JSR R5,.SROMCLK
104125!<400*3> ;JUMP TO ROM PC OF 525
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
125 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 6$ ;BR IF YES
ERROR 5 ;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5
6$: ESCAPE SEG
TRAP C$ESCAPE
.WORD 10002$-.
ENDSEG
10002$: TRAP C$ESEG
ENDTST
L10060: TRAP C$ETST

BADHEAD
:***** TEST 15 *****
:*CRAM TEST OF JUMP(1) ON BRO SET MICRO-PROCESSOR INSTRUCTION.
:*SET THE BRO BIT, PERFORM THE JUMP INSTRUCTION.
:*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PCRT4. IF THIS DATA IS CORRECT
:*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
:*THEN PORT4 WILL CONTAIN A 37
BADHEAD
:***** TEST 15 *****

BGNTST
T15:: MACEX2 ;DON'T DO IF M8200.
;DO NOT DO TEST IF M8200
TRAP C$EXIT
.WORD L10061-.
MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
;R1 CONTAINS BASE M8200.4,7 ADDRESS
MSTCLR ;MASTER CLEAR M8200.4,7
JSR PC,MEMSET ;SET MEM AND RAM

1$:

```

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4411	016172			BGNSEG		
4412	016172	104404		TRAP	C\$BSEG	
4413	016174	004737	003220	JSR	PC,SETBRO	:SET THE BRO BIT'
4414	016200			SROMCLK		:NEXT WORD IS INSTRUCTION.
4415	016200	004537	003100	JSR	R5, SROMCLK	
4416	016204	100400		100400		:START AT ROM PC=0
4417	016206			SROMCLK		:NEXT WORD IS INSTRUCTION.
4418	016206	004537	003100	JSR	R5, SROMCLK	
4419	016212	116377		114377!<400*4>		:JUMP TO ROM PC OF 1777
4420	016214	004737	003330	JSR	PC, RAMDAT	:R4=CRAM PC (LSB 8 BITS)
4421	016220	000377		377		:EXPECTED DATA
4422	016222	120504		CMPB	R5,R4	:IS ROM PC CORRECT?
4423	016224	001406		BEQ	2\$	:BR IF YES
4424	016226			ERROR	5	:ERROR, CRAM PC IS WRONG
4425	016232	104455		TRAP	C\$ERDF	
4426	016234	000005		.WORD	5	
4427	016236	005055		.WORD	EMO	
4428	016240	006556		.WORD	ERR5	
4429	016242			2\$: ESCAPE	SEG	
4430	016242	104410		TRAP	C\$ESCAPE	
4431	016244	000002		.WORD	10000\$-	
4432	016246			ENDSEG		
4433	016246			10000\$: TRAP	C\$ESEG	
4434	016246	104405		BGNSEG		
4435	016250			TRAP	C\$BSEG	
4436	016250	104404		JSR	PC,SETBRO	:SET THE BRO BIT'
4437	016252	004737	003220	SROMCLK		:NEXT WORD IS INSTRUCTION.
4438	016256			JSR	R5, SROMCLK	
4439	016256	004537	003100	100403		:START AT ROM PC=3
4440	016262	100403		SROMCLK		:NEXT WORD IS INSTRUCTION.
4441	016264			JSR	R5, SROMCLK	
4442	016264	004537	003100	100000!<400*4>		:JUMP TO ROM PC OF 0
4443	016270	102000		JSR	PC, RAMDAT	:R4=CRAM PC (LSB 8 BITS)
4444	016272	004737	003330	0		:EXPECTED DATA
4445	016276	000000		CMPB	R5,R4	:IS ROM PC CORRECT?
4446	016300	120504		BEQ	4\$	:BR IF YES
4447	016302	001406		ERROR	5	:ERROR, CRAM PC IS WRONG
4448	016304			TRAP	C\$ERDF	
4449	016310	104455		.WORD	5	
4450	016312	000005		.WORD	EMO	
4451	016314	005055		.WORD	ERR5	
4452	016316	006556		4\$: ESCAPE	SEG	
4453	016320			TRAP	C\$ESCAPE	
4454	016320	104410		.WORD	10001\$-	
4455	016322	000002		ENDSEG		
4456	016324			10001\$: TRAP	C\$ESEG	
4457	016324			BGNSEG		
4458	016324	104405		TRAP	C\$BSEG	
4459	016326			JSR	PC,SETBRO	:SET THE BRO BIT'
4460	016326	104404		SROMCLK		:NEXT WORD IS INSTRUCTION.
4461	016330	004737	003220	JSR	R5, SROMCLK	
4462	016334			100406		:START AT ROM PC=6
4463	016334	004537	003100	SROMCLK		:NEXT WORD IS INSTRUCTION.
4464	016340	100406		JSR	R5, SROMCLK	
4465	016342					
4466	016342	004537	003100			

4467 016346 106125  
 4468 016350 004737 003330  
 4469 016354 000125  
 4470 016356 120504  
 4471 016360 001406  
 4472 016362  
 4473 016366 104455  
 4474 016370 000005  
 4475 016372 005055  
 4476 016374 006556  
 4477 016376  
 4478 016376 104410  
 4479 016400 000002  
 4480 016402  
 4481 016402  
 4482 016402 104405  
 4483 016404  
 4484 016404  
 4485 016404 104401  
 4486  
 4487 016406  
 4488  
 4489  
 4490  
 4491  
 4492  
 4493  
 4494  
 4495  
 4496  
 4497 016406  
 4498  
 4499  
 4500 016406  
 4501 016406  
 4502 016406  
 4503  
 4504 016416 104432  
 4505 016420 000230  
 4506 016422  
 4507 016422 013701 002516  
 4508  
 4509 016426  
 4510 016432 004737 003474  
 4511 016436  
 4512 016436  
 4513 016436 104404  
 4514 016440 004737 003230  
 4515 016444  
 4516 016444 004537 003100  
 4517 016450 100400  
 4518 016452  
 4519 016452 004537 003100  
 4520 016456 116777  
 4521 016460 004737 003330  
 4522 016464 000377

```

104125!<400*4>      :JUMP TO ROM PC OF 525
JSR      PC,RAMDAT  :R4=CRAM PC (LSB 8 BITS)
125      :EXPECTED DATA
CMPB     R5,R4      :IS ROM PC CORRECT?
BEQ      6$         :BR IF YES
ERROR    5          :ERROR, CRAM PC IS WRONG
TRAP     C$ERDF
.WORD    5
.WORD    EMO
.WORD    ERR5
6$:      ESCAPE SEG
TRAP     C$ESCAPE
.WORD    10002$-.
ENDSEG
10002$: TRAP     C$ESEG
ENDTST
L10061: TRAP     C$ETST

BADHEAD
:***** TEST 16 *****
:*CRAM TEST OF JUMP(I) ON BR1 SET MICRO-PROCESSOR INSTRUCTION.
:*SET THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.
:*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
:*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
:*THEN PORT4 WILL CONTAIN A 37
BADHEAD
:***** TEST 16 *****

BGN1ST
T16::
MACEX2      :DON'T DO IF M8200.
:DO NOT DO TEST IF M8200
TRAP     C$EXIT
.WORD    L10062-.
MYINT
MOV       KMCSR,R1      :RECORD DEVICE ADDR.
:R1 CONTAINS BASE M8200,4,7 ADDRESS
MSTCLR
JSR      PC,MEMSET     :MASTER CLEAR M8200,4,7
:SET MEM AND RAM
1$:
BGNSEG
TRAP     C$BSEG
JSR      PC,SETBR1     :SET THE BR1 BIT'
SROMCLK  :NEXT WORD IS INSTRUCTION,
JSR      R5,.,SROMCLK
100400     :START AT ROM PC=0
SROMCLK  :NEXT WORD IS INSTRUCCION,
JSR      R5,.,SROMCLK
114377!<400*5>      :JUMP TO ROM PC OF 1777
JSR      PC,RAMDAT    :R4=CRAM PC (LSB 8 BITS)
377      :EXPECTED DATA

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4523	016466	120504		CMPB	R5,R4		:IS ROM PC CORRECT?
4524	016470	001406		BEQ	2\$		:BR IF YES
4525	016472			ERROR	5		:ERROR, CRAM PC IS WRONG
4526	016476	104455		TRAP	C\$ERDF		
4527	016500	000005		.WORD	5		
4528	016502	005055		.WORD	EMO		
4529	016504	006556		.WORD	ERR5		
4530	016506		2\$:	ESCAPE	SEG		
4531	016506	104410		TRAP	C\$ESCAPE		
4532	016510	000002		.WORD	10000\$-		
4533	016512			ENDSEG			
4534	016512		10000\$:				
4535	016512	104405		TRAP	C\$ESEG		
4536	016514			BGNSEG			
4537	016514	104404		TRAP	C\$BSEG		
4538	016516	004737	003230	JSR	PC,SETBR1		:SET THE BR1 BIT'
4539	016522			SROMCLK			:NEXT WORD IS INSTRUCTION,
4540	016522	004537	003100	JSR	R5, .SROMCLK		
4541	016526	100403		100403			:START AT ROM PC=3
4542	016530			SROMCLK			:NEXT WORD IS INSTRUCTION,
4543	016530	004537	003100	JSR	R5, .SROMCLK		
4544	016534	102400		100000!<400*5>			:JUMP TO ROM PC OF 0
4545	016536	004737	003330	JSR	PC,RAMDAT		:R4=CRAM PC (LSB 8 BITS)
4546	016542	000000		0			:EXPECTED DATA
4547	016544	120504		CMPB	R5,R4		:IS ROM PC CORRECT?
4548	016546	001406		BEQ	4\$		:BR IF YES
4549	016550			ERROR	5		:ERROR, CRAM PC IS WRONG
4550	016554	104455		TRAP	C\$ERDF		
4551	016556	000005		.WORD	5		
4552	016560	005055		.WORD	EMO		
4553	016562	006556		.WORD	ERR5		
4554	016564		4\$:	ESCAPE	SEG		
4555	016564	104410		TRAP	C\$ESCAPE		
4556	016566	000002		.WORD	10001\$-		
4557	016570			ENDSEG			
4558	016570		10001\$:				
4559	016570	104405		TRAP	C\$ESEG		
4560	016572			BGNSEG			
4561	016572	104404		TRAP	C\$BSEG		
4562	016574	004737	003230	JSR	PC,SETBR1		:SET THE BR1 BIT'
4563	016600			SROMCLK			:NEXT WORD IS INSTRUCTION,
4564	016600	004537	003100	JSR	R5, .SROMCLK		
4565	016604	100406		100406			:START AT ROM PC=6
4566	016606			SROMCLK			:NEXT WORD IS INSTRUCTION,
4567	016606	004537	003100	JSR	R5, .SROMCLK		
4568	016612	106525		104125!<400*5>			:JUMP TO ROM PC OF 525
4569	016614	004737	003330	JSR	PC,RAMDAT		:R4=CRAM PC (LSB 8 BITS)
4570	016620	000125		125			:EXPECTED DATA
4571	016622	120504		CMPB	R5,R4		:IS ROM PC CORRECT?
4572	016624	001406		BEQ	6\$		:BR IF YES
4573	016626			ERROR	5		:ERROR, CRAM PC IS WRONG
4574	016632	104455		TRAP	C\$ERDF		
4575	016634	000005		.WORD	5		
4576	016636	005055		.WORD	EMO		
4577	016640	006556		.WORD	ERR5		
4578	016642		6\$:	ESCAPE	SEG		

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4579 016642 104410  
4580 016644 000002  
4581 016646  
4582 016646  
4583 016646 104405  
4584 016650  
4585 016650  
4586 016650 104401  
4587  
4588 016652  
4589  
4590  
4591  
4592  
4593  
4594  
4595  
4596  
4597  
4598 016652  
4599  
4600  
4601 016652  
4602 016652  
4603 016652  
4604  
4605 016662 104432  
4606 016664 000230  
4607 016666  
4608 016666 013701 002516  
4609 016672  
4610 016676 004737 003474  
4611 016702  
4612 016702  
4613 016702 104404

TRAP C\$ESCAPE  
.WORD 10002\$-.  
ENDSEG  
10002\$: TRAP C\$ESEG  
ENDTST  
L10062: TRAP C\$ETST  
BADHEAD  
:\*\*\*\*\* TEST 17 \*\*\*\*\*  
:\*CRAM TEST OF JUMP(I) ON BR4 SET MICRO-PROCESSOR INSTRUCTION.  
:\*SET THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.  
:\*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION  
:\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
:\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
:\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
:\*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL  
:\*THEN PORT4 WILL CONTAIN A 37  
BADHEAD  
:\*\*\*\*\* TEST 17 \*\*\*\*\*  
BGNTST  
T17:: MACEX2 :DON'T DO IF M8200.  
:DO NOT DO TEST IF M8200  
TRAP C\$EXIT  
.WORD L10063-.  
MYINT  
MOV KMCSR,R1 :RECORD DEVICE ADDR.  
MSTCLR :MASTER CLEAR M8200,4,7  
JSR PC,MEMSET :SET MEM AND RAM  
1\$:  
BGNSEG  
TRAP C\$BSEG

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4614 016704 004737 003240  
4615 016710  
4616 016710 004537 003100  
4617 016714 100400  
4618 016716  
4619 016716 004537 003100

JSR PC,SETBR4 ;SET THE BR4 BIT'  
SROMCLK ;NEXT WORD IS INSTRUCTION,  
JSR R5,.SROMCLK  
100400 ;START AT ROM PC=0  
SROMCLK ;NEXT WORD IS INSTRUCION,  
JSR R5,.SROMCLK

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4620 016722 117377  
4621 016724 004737 003330

114377!<400\*6>  
JSR PC, RAMDAT

:JUMP TO ROM PC OF 1777  
:R4=(RAM PC (LSB 8 BITS))



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4622 016730 000377  
4623 016732 120504

377  
CMPB R5,R4

:EXPECTED DATA  
:IS ROM PC CORRECT?

0

J 9

SEQ 113

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4624 016734 001406

BEQ 28

;BR IF YES

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4625 016736  
4626 016742 104455  
4627 016744 000C05  
4628 016746 005055  
4629 016750 006556

ERROR 5  
TRAP C\$ERDF  
.WORD 5  
.WORD EMO  
.WORD ERR5

;ERROR, CRAM PC IS WRONG

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4630 016752  
4631 016752 104410  
4632 016754 000002  
4633 016756  
4634 016756  
4635 016756 104405  
4636 016760  
4637 016760 104404  
4638 016762 004737 003240  
4639 016766  
4640 016766 004537 003100  
4641 016772 100403  
4642 016774  
4643 016774 004537 003100  
4644 017000 103000  
4645 017002 004737 003330  
4646 017006 000000  
4647 017010 120504  
4648 017012 001406  
4649 017014  
4650 017020 104455  
4651 017022 000005  
4652 017024 005055  
4653 017026 006556  
4654 017030  
4655 017030 104410  
4656 017032 000002  
4657 017034  
4658 017034  
4659 017034 104405  
4660 017036  
4661 017036 104404  
4662 017040 004737 003240  
4663 017044  
4664 017044 004537 003100  
4665 017050 100406  
4666 017052  
4667 017052 004537 003100  
4668 017056 107125  
4669 017060 004737 003330  
4670 017064 000125  
4671 017066 120504  
4672 017070 001406  
4673 017072  
4674 017076 104455  
4675 017100 000005  
4676 017102 005055  
4677 017104 006556  
4678 017106  
4679 017106 104410  
4680 017110 000002  
4681 017112  
4682 017112  
4683 017112 104405  
4684 017114  
4685 017114

2\$: ESCAPE SEG  
TRAP C\$ESCAPE  
.WORD 10000\$-  
ENDSEG  
10000\$: TRAP C\$ESEG  
BGNSEG  
TRAP C\$BSEG  
JSR PC,SETBR4  
SROMCLK R5,.SROMCLK  
JSR R5,.SROMCLK  
100403  
SROMCLK R5,.SROMCLK  
100000!<400\*6>  
JSR PC,RAMDAT  
0  
CMPB R5,R4  
BEQ 4\$  
ERROR 5  
TRAP C\$ERDF  
.WORD 5  
.WORD EMO  
.WORD ERR5  
4\$: ESCAPE SEG  
TRAP C\$ESCAPE  
.WORD 10001\$-  
ENDSEG  
10001\$: TRAP C\$ESEG  
BGNSEG  
TRAP C\$BSEG  
JSR PC,SETBR4  
SROMCLK R5,.SROMCLK  
JSR R5,.SROMCLK  
100406  
SROMCLK R5,.SROMCLK  
104125!<400\*6>  
JSR PC,RAMDAT  
125  
CMPB R5,R4  
BEQ 6\$  
ERROR 5  
TRAP C\$ERDF  
.WORD 5  
.WORD EMO  
.WORD ERR5  
6\$: ESCAPE SEG  
TRAP C\$ESCAPE  
.WORD 10002\$-  
ENDSEG  
10002\$: TRAP C\$ESEG  
ENDTST  
L10063:

;SET THE BR4 BIT'  
;NEXT WORD IS INSTRUCTION,  
;START AT ROM PC=3  
;NEXT WORD IS INSTRUCTION,  
;JUMP TO ROM PC OF 0  
;R4=CRAM PC (LSB 8 BITS)  
;EXPECTED DATA  
;IS ROM PC CORRECT?  
;BR IF YES  
;ERROR, CRAM PC IS WRONG  
;SET THE BR4 BIT'  
;NEXT WORD IS INSTRUCTION,  
;START AT ROM PC=6  
;NEXT WORD IS INSTRUCTION,  
;JUMP TO ROM PC OF 525  
;R4=CRAM PC (LSB 8 BITS)  
;EXPECTED DATA  
;IS ROM PC CORRECT?  
;BR IF YES  
;ERROR, CRAM PC IS WRONG

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4686 017114 104401 TRAP C$ETST
4687
4688 017116 BADHEAD
4689 ;***** TEST 18 *****
4690 ;*CRAM TEST OF JUMP(1) ON BR7 SET MICRO-PROCESSOR INSTRUCTION.
4691 ;*SET THE BR7 BIT, PERFORM THE JUMP INSTRUCTION.
4692 ;*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
4693 ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
4694 ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
4695 ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
4696 ;*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
4697 ;*THEN PORT4 WILL CONTAIN A 37
4698 017116 BADHEAD
4699 ;***** TEST 18 *****
4700
4701 017116 BGNTST
4702 017116 T18::
4703 017116
4704
4705 017126 104432 MACEX2 ;DON'T DO IF M8200.
4706 017130 000230 ;DO NOT DO TEST IF M8200
4707 017132 .WORD L10064-. TRAP C$EXIT
4708 017132 013701 002516 MYINT .WORD L10064-.
4709 MOV KMCSR,R1 ;RECORD DEVICE ADDR.
4710 017136 ;R1 CONTAINS BASE M8200,4,7 ADDRESS
4711 017142 004737 003474 MSTCLR ;MASTER CLEAR M8200,4,7
4712 017146 1$: JSR PC, MEMSET ;SET MEM AND RAM
4713 017146 104404 BGNSEG
4714 017150 004737 003250 TRAP C$BSEG
4715 017154 JSR PC, SETBR7 ;SET THE BR7 BIT'
4716 017154 004537 003100 SROMCLK ;NEXT WORD IS INSTRUCTION,
4717 017160 100400 JSR R5, .SROMCLK
4718 017162 100400 ;START AT ROM PC=0
4719 017162 004537 003100 SROMCLK ;NEXT WORD IS INSTRUCTION,
4720 017166 117777 JSR R5, .SROMCLK
4721 017170 004737 003330 114377! <400*7> ;JUMP TO ROM PC OF 1777
4722 017174 000377 JSR PC, RAMDAT ;R4=CRAM PC (LSB 8 BITS)
4723 017176 120504 377 ;EXPECTED DATA
4724 017200 001406 CMPB R5,R4 ;IS ROM PC CORRECT?
4725 017202 BEQ 2$ ;BR IF YES
4726 017206 104455 ERROR 5 ;ERROR, CRAM PC IS WRONG
4727 017210 000005 TRAP C$ERDF
4728 017212 005055 .WORD 5
4729 017214 006556 .WORD EMO
4730 017216 2$: ESCAPE SEG .WORD ERR5
4731 017216 104410 TRAP C$ESCAPE
4732 017220 000002 .WORD 10000$-.
4733 017222 ENDSEG
4734 017222
4735 017222 104405 10000$: TRAP C$ESEG
4736 017224 BGNSEG
4737 017224 104404 TRAP C$BSEG
4738 017226 004737 003250 JSR PC, SETBR7 ;SET THE BR7 BIT'
4739 017232 SROMCLK ;NEXT WORD IS INSTRUCTION,
4740 017232 004537 003100 JSR R5, .SROMCLK
4741 017236 100403 ;START AT ROM PC=3

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4742 017240
4743 017240 004537 003100
4744 017244 103400
4745 017246 004737 003330
4746 017252 000000
4747 017254 120504
4748 017256 001406
4749 017260
4750 017264 104455
4751 017266 000005
4752 017270 005055
4753 017272 006556
4754 017274
4755 017274 104410
4756 017276 000002
4757 017300
4758 017300
4759 017300 104405
4760 017302
4761 017302 104404
4762 017304 004737 003250
4763 017310
4764 017310 004537 003100
4765 017314 100406
4766 017316
4767 017316 004537 003100
4768 017322 107525
4769 017324 004737 003330
4770 017330 000125
4771 017332 120504
4772 017334 001406
4773 017336
4774 017342 104455
4775 017344 000005
4776 017346 005055
4777 017350 006556
4778 017352
4779 017352 104410
4780 017354 000002
4781 017356
4782 017356
4783 017356 104405
4784 017360
4785 017360
4786 017360 104401
4787
4788 017362
4789
4790
4791
4792
4793
4794
4795
4796
4797

SROMCLK
JSR R5,.SROMCLK ;NEXT WORD IS INSTRUCTION,
100000!<400*7> ;JUMP TO ROM PC OF 0
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
0 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 4$ ;BR IF YES
ERROR 5 ;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5
4$: ESCAPE SEG
TRAP C$ESCAPE
.WORD 10001$-.
ENDSEG
10001$: TRAP C$ESEG
BGNSEG
TRAP C$BSEG
JSR PC,SETBR7 ;SET THE BR7 BIT
SROMCLK ;NEXT WORD IS INSTRUCTION,
JSR R5,.SROMCLK
100406 ;START AT ROM PC=6
SROMCLK ;NEXT WORD IS INSTRUCTION,
JSR R5,.SROMCLK
104125!<400*7> ;JUMP TO ROM PC OF 525
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
125 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 6$ ;BR IF YES
ERROR 5 ;ERRCR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5
6$: ESCAPE SEG
TRAP C$ESCAPE
.WORD 10002$-.
ENDSEG
10002$: TRAP C$ESEG
ENDTST
L10064: TRAP C$ETST

BADHEAD
:***** TEST 19 *****
:*CRAM TEST OF JUMP(I) ON C BIT CLEAR MICRO-PROCESSOR INSTRUCTION.
:*SET THE C BIT, PERFORM THE JUMP INSTRUCTION.
:*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
:*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
:*THEN PORT4 WILL CONTAIN A 37

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4798 017362  
4799  
4800  
4801 017362  
4802 017362  
4803 017362  
4804  
4805 017372 104432  
4806 017374 000244  
4807 017376  
4808 017376 013701 002516  
4809 017402  
4810 017406 004737 003474  
4811 017412  
4812 017412 104404  
4813 017414 004737 003260  
4814 017420 004737 003166  
4815 017424  
4816 017424 004537 003100  
4817 017430 100400  
4818 017432  
4819 017432 004537 003100  
4820 017436 115377  
4821 017440 004737 003330  
4822 017444 000001  
4823 017446 120504  
4824 017450 001406  
4825 017452  
4826 017456 104455  
4827 017460 000005  
4828 017462 005055  
4829 017464 006556  
4830 017466  
4831 017466 104410  
4832 017470 000002  
4833 017472  
4834 017472  
4835 017472 104405  
4836 017474  
4837 017474 104404  
4838 017476  
4839  
4840 017506 004737 003166  
4841 017512  
4842 017512 004537 003100  
4843 017516 100403  
4844 017520  
4845 017520 004537 003100  
4846 017524 101000  
4847 017526 004737 003330  
4848 017532 000004  
4849 017534 120504  
4850 017536 001406  
4851 017540  
4852 017544 104455  
4853 017546 000005

```

BADHEAD
:***** TEST 19 *****

BGNTST
T19::
MACEX2 ;DON'T DO IF M8200.
;DO NOT DO TEST IF M8200
TRAP C$EXIT
.WORD L10065-.
MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
MSTCLR ;MASTER CLEAR M8200,4,7
JSR PC,MEMSET ;SET MEM AND RAM
1$: BGNSEG
TRAP C$BSEG
JSR PC,SETC
JSR PC,CLRALL
SR0MCLK ;NEXT WORD IS INSTRUCTION,
JSR R5,.SR0MCLK
100400 ;START AT ROM PC=0
SR0MCLK ;NEXT WORD IS INSTRUCION,
JSR R5,.SR0MCLK
114377!<400*2> ;JUMP TO ROM PC OF 1777
JSR PC,RAMDAT ;R4=CRAM PC (LSB 8 BITS)
1 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 2$ ;BR IF YES
ERROR 5 ;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5
.WORD EMO
.WORD ERR5
2$: ESCAPE SEG
TRAP C$ESCAPE
.WORD 10000$-.
ENDSEG
10000$: TRAP C$ESEG
BGNSEG
TRAP C$BSCC
SKIP06 6$
;GOTO 6$ IF M8206
JSR PC,CLRALL ;CLEAR ALL CONDITIONS
SR0MCLK ;NEXT WORD OF INSTRUCTION
JSR R5,.SR0MCLK
100403 ;START AT ROM PC=3
SR0MCLK ;NEXT WORD OF INSTRUCTION
JSR R5,.SR0MCLK
100000!<400*2> ;JUMP TO ROM PC OF 0
JSR PC,RAMDAT ;R4=CRAM PC(LSB 8 BITS)
4 ;EXPECTED DATA
CMPB R5,R4 ;IS ROM PC CORRECT?
BEQ 4$ ;BR IF YES
ERROR 5 ;ERROR, CRAM PC IS WRONG
TRAP C$ERDF
.WORD 5

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4854 017550 005055      .WORD  EMO
4855 017552 006556      .WORD  ERR5
4856 017554             4$:  ESCAPE  SFG
4857 017554 104410      TRAP   C$ESCAPE
4858 017556 000002      .WORD  10001$-.
4859 017560             ENDSEG
4860 017560             10001$:
4861 017560 104405      TRAP   C$ESEG
4862 017562             BGNSEG
4863 017562 104404      TRAP   C$BSEG
4864 017564 004737 003166  JSR    PC,CLRALL           ;CLEAR ALL CONDITIONS
4865 017570             SROMCLK           ;NEXT WORD IS INSTRUCTION,
4866 017570 004537 003100  JSR    R5,..SROMCLK
4867 017574 100406             100406           ;START AT ROM PC=6
4868 017576             SROMCLK           ;NEXT WORD IS INSTRUCTION,
4869 017576 004537 003100  JSR    R5,..SROMCLK
4870 017602 105125             104125:<400*2>       ;JUMP TO ROM PC OF 525
4871 017604 004737 003330  JSR    PC,RAMDAT         ;R4=CRAM PC (LSB 8 BITS)
4872 017610 000007             7                ;EXPECTED DATA
4873 017612 120504             CMPB   R5,R4           ;IS ROM PC CORRECT?
4874 017614 001406             BEQ   6$              ;BR IF YES
4875 017616             ERROR  5                ;ERROR, CRAM PC IS WRONG
4876 017622 104455      TRAP   C$ERDF
4877 017624 000005      .WORD  5
4878 017626 005055      .WORD  EMO
4879 017630 006556      .WORD  ERR5
4880 017632             6$:  ESCAPE  SEG
4881 017632 104410      TRAP   C$ESCAPE
4882 017634 000002      .WORD  10002$-.
4883 017636             ENDSEG
4884 017636             10002$:
4885 017636 104405      TRAP   C$ESEG
4886 017640             ENDTST
4887 017640             L10065:
4888 017640 104401      TRAP   C$ETST
4889 017642             BADHEAD
4890 017642             :***** TEST 20 *****
4891 017642             :*CRAM TEST OF JUMP(I) ON Z BIT CLEAR MICRO-PROCESSOR INSTRUCTION.
4892 017642             :*CLEAR THE Z BIT, PERFORM THE JUMP INSTRUCTION.
4893 017642             :*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
4894 017642             :*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
4895 017642             :*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
4896 017642             :*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
4897 017642             :*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
4898 017642             :*THEN PORT4 WILL CONTAIN A 37
4899 017642             BADHEAD
4900 017642             :***** TEST 20 *****
4901 017642             BGNST
4902 017642             T20::
4903 017642             MACEX2           ;DON'T DO IF M8200.
4904 017642             :DO NOT DO TEST IF M8200
4905 017642             TRAP   C$EXIT
4906 017642             .WORD  L10066-.
4907 017652 104432      MYINT
4908 017654 000244
4909 017656

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4910	017656	013701	002516	MOV	KMCSR,R1				
4911	017662			MSTCLR					;RECORD DEVICE ADDR.
4912	017666	004737	003474	JSR	PC,MEMSET				;MASTER CLEAR M8200,4,7
4913	017672			1\$:	BGNSEG				;SET MEM AND RAM
4914	017672	104404		TRAP	C\$BSEG				
4915	017674	004737	003312	JSR	PC,SETZ				
4916	017700	004737	003166	JSR	PC,CLRALL				; CLEAR CONDITION CODES ;*** BO
4917	017704			SROMCLK					;NEXT WORD IS INSTRUCTION,
4918	017704	004537	003100	JSR	R5,.SROMCLK				
4919	017710	100400		100400					;START AT ROM PC=0
4920	017712			SROMCLK					;NEXT WORD IS INSTRUCTION,
4921	017712	004537	003100	JSR	R5,.SROMCLK				
4922	017716	115777		114377!<400*3>					;JUMP TO ROM PC OF 1777
4923	017720	004737	003330	JSR	PC,RAMDAT				;R4=CRAM PC (LSB 8 BITS)
4924	017724	000001		1					;EXPECTED DATA
4925	017726	120504		CMPB	R5,R4				;IS ROM PC CORRECT?
4926	017730	001406		BEQ	2\$				;BR IF YES
4927	017732			ERROR	5				;ERROR, CRAM PC IS WRONG
4928	017736	104455		TRAP	C\$ERDF				
4929	017740	000005		.WORD	5				
4930	017742	005055		.WORD	EMO				
4931	017744	006556		.WORD	ERR5				
4932	017746			2\$:	ESCAPE SEG				
4933	017746	104410		TRAP	C\$ESCAPE				
4934	017750	000002		.WORD	10000\$-				
4935	017752			ENDSEG					
4936	017752			10000\$:					
4937	017752	104405		TRAP	C\$ESEG				
4938	017754			BGNSEG					
4939	017754	104404		TRAP	C\$BSEG				
4940	017756			SKIP06	6\$				
4941				:GOTO 6\$ IF M8206					
4942	017766	004737	003166	JSR	PC,CLRALL				;CLEAR ALL CONDITIONS
4943	017772			SROMCLK					;NEXT WORD IS INSTRUCTION,
4944	017772	004537	003100	JSR	R5,.SROMCLK				
4945	017776	100403		100403					;START AT ROM PC=3
4946	020000			SROMCLK					;NEXT WORD IS INSTRUCTION,
4947	020000	004537	003100	JSR	R5,.SROMCLK				
4948	020004	101400		100000!<400*3>					;JUMP TO ROM PC OF 0
4949	020006	004737	003330	JSR	PC,RAMDAT				;R4=CRAM PC (LSB 8 BITS)
4950	020012	000004		4					;EXPECTED DATA
4951	020014	120504		CMPB	R5,R4				;IS ROM PC CORRECT?
4952	020016	001406		BEQ	4\$				;BR IF YES
4953	020020			ERROR	5				;ERROR, CRAM PC IS WRONG
4954	020024	104455		TRAP	C\$ERDF				
4955	020026	000005		.WORD	5				
4956	020030	005055		.WORD	EMO				
4957	020032	006556		.WORD	ERR5				
4958	020034			4\$:	ESCAPE SEG				
4959	020034	104410		TRAP	C\$ESCAPE				
4960	020036	000002		.WORD	10001\$-				
4961	020040			ENDSEG					
4962	020040			10001\$:					
4963	020040	104405		TRAP	C\$ESEG				
4964	020042			BGNSEG					
4965	020042	104404		TRAP	C\$BSEG				

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4966 020044 004737 003166      JSR    PC,CLRALL      ;CLEAR ALL CONDITIONS
4967 020050                    SRMCLK                ;NEXT WORD IS INSTRUCTION,
4968 020050 004537 003100      JSR    R5,.SRMCLK
4969 020054 100406                    100406                ;START AT ROM PC=6
4970 020056                    SRMCLK                ;NEXT WORD IS INSTRUCTION,
4971 020056 004537 003100      JSR    R5,.SRMCLK
4972 020062 105525                    104125!<400*3>      ;JUMP TO ROM PC OF 525
4973 020064 004737 003330      JSR    PC,RAMDAT      ;R4=CRAM PC (LSB 8 BITS)
4974 020070 000007                    7                    ;EXPECTED DATA
4975 020072 120504                    CMPB   R5,R4          ;IS ROM PC CORRECT?
4976 020074 001406                    BEQ    6$             ;BR IF YES
4977 020076                    ERROR   5              ;ERROR, CRAM PC IS WRONG
4978 020102 104455                    TRAP   C$ERDF
4979 020104 000005                    .WORD  5
4980 020106 005055                    .WORD  EMO
4981 020110 006556                    .WORD  ERR5
4982 020112                    6$:  ESCAPE  SEG
4983 020112 104410                    TRAP   C$ESCAPE
4984 020114 000002                    .WORD  10002$-.
4985 020116                    ENDSEG
4986 020116                    10002$:
4987 020116 104405                    TRAP   C$ESEG
4988 020120                    ENDTST
4989 020120                    L10066:
4990 020120 104401                    TRAP   C$ETST
4991
4992 020122                    BADHEAD
4993                    ;***** TEST 21 *****
4994                    ;*CRAM TEST OF JUMP(1) ON BRO CLEAR MICRO-PROCESSOR INSTRUCTION.
4995                    ;*CLEAR THE BRO BIT, PERFORM THE JUMP INSTRUCTION.
4996                    ;*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
4997                    ;*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
4998                    ;*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
4999                    ;*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
5000                    ;*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
5001                    ;*THEN PORT4 WILL CONTAIN A 37
5002 020122                    BADHEAD
5003                    ;***** TEST 21 *****
5004
5005 020122                    BGNTST
5006 020122                    T21::
5007 020122
5008                    MACEX2                    ;DON'T DO IF M8200.
5009 020132 104432                    ;DO NOT DO TEST IF M8200
5010 020134 000240                    TRAP   C$EXIT
5011 020136                    .WORD  L10067-.
5012 020136 013701 002516                    MYINT
5013 020142                    MOV    KMCSR,R1      ;RECORD DEVICE ADDR.
5014 020146 004737 003474                    MSTCLR                ;MASTER CLEAR M8200,4,7
5015 020152                    JSR    PC,MEMSET      ;SET MEM AND RAM
5016 020152 104404                    1$:  BGNSEG
5017 020154 004737 003166                    TRAP   C$BSEG
5018 020160                    JSR    PC,CLRALL      ;CLEAR ALL CONDITIONS
5019 020160 004537 003100                    SRMCLK                ;NEXT WORD IS INSTRUCTION,
5020 020164 100400                    JSR    R5,.SRMCLK
5021 020166                    100400                ;START AT ROM PC=0
                    SRMCLK                ;NEXT WORD IS INSTRUCTION,

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5022	020166	004537	003100	JSR	R5, .SROMCLK	
5023	020172	116377		114377!	<400*4>	: JUMP TO ROM PC OF 1777
5024	020174	004737	003330	JSR	PC, RAMDAT	: R4=CRAM PC (LSB 8 BITS)
5025	020200	000001		1		: EXPECTED DATA
5026	020202	120504		CMPB	R5, R4	: IS ROM PC CORRECT?
5027	020204	001406		BEQ	2\$	: BR IF YES
5028	020206			ERROR	5	: ERROR, CRAM PC IS WRONG
5029	020212	104455		TRAP	C\$ERDF	
5030	020214	000005		.WORD	5	
5031	020216	005055		.WORD	EMO	
5032	020220	006556		.WORD	ERR5	
5033	020222			2\$:	ESCAPE SEG	
5034	020222	104410		TRAP	C\$ESCAPE	
5035	020224	000002		.WORD	10000\$-	
5036	020226			10000\$:	ENDSEG	
5037	020226					
5038	020226	104405		TRAP	C\$ESEG	
5039	020230			BGNSEG		
5040	020230	104404		TRAP	C\$BSEG	
5041	020232			SKIP06	6\$	
5042				:GOTO	6\$ IF M8206	
5043	020242	004737	003166	JSR	PC, CLRALL	: CLEAR ALL CONDITIONS
5044	020246			SROMCLK		: NEXT WORD IS INSTRUCTION,
5045	020246	004537	003100	JSR	R5, .SROMCLK	
5046	020252	100403		100403		: START AT ROM PC-3
5047	020254			SROMCLK		: NEXT WORD IS INSTRUCTION,
5048	020254	004537	003100	JSR	R5, .SROMCLK	
5049	020260	102000		100000!	<400*4>	: JUMP TO ROM PC OF 0
5050	020262	004737	003330	JSR	PC, RAMDAT	: R4=CRAM PC (LSB 8 BITS)
5051	020266	000004		4		: EXPECTED DATA
5052	020270	120504		CMPB	R5, R4	: IS ROM PC CORRECT?
5053	020272	001406		BEQ	4\$	: BR IF YES
5054	020274			ERROR	5	: ERROR, CRAM PC IS WRONG
5055	020300	104455		TRAP	C\$ERDF	
5056	020302	000005		.WORD	5	
5057	020304	005055		.WORD	EMO	
5058	020306	006556		.WORD	ERR5	
5059	020310			4\$:	ESCAPE SEG	
5060	020310	104410		TRAP	C\$ESCAPE	
5061	020312	000002		.WORD	10001\$-	
5062	020314			10001\$:	ENDSEG	
5063	020314					
5064	020314	104405		TRAP	C\$ESEG	
5065	020316			BGNSEG		
5066	020316	104404		TRAP	C\$BSEG	
5067	020320	004737	003166	JSR	PC, CLRALL	: CLEAR ALL CONDITIONS
5068	020324			SROMCLK		: NEXT WORD IS INSTRUCTION,
5069	020324	004537	003100	JSR	R5, .SROMCLK	
5070	020330	100406		100406		: START AT ROM PC=6
5071	020332			SROMCLK		: NEXT WORD IS INSTRUCTION,
5072	020332	004537	003100	JSR	R5, .SROMCLK	
5073	020336	106125		104125!	<400*4>	: JUMP TO ROM PC OF 525
5074	020340	004737	003330	JSR	PC, RAMDAT	: R4=CRAM PC (LSB 8 BITS)
5075	020344	000007		7		: EXPECTED DATA
5076	020346	120504		CMPB	R5, R4	: IS ROM PC CORRECT?
5077	020350	001406		BEQ	6\$	: BR IF YES

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```

5078 020352          ERROR 5          ;ERROR, CRAM PC IS WRONG
5079 020356 104455  TRAP  C$ERDF
5080 020360 000005  .WORD 5
5081 020362 005055  .WORD EMO
5082 020364 006556  .WORD ERR5
5083 020366          6$: ESCAPE SEG
5084 020366 104410  TRAP  C$ESCAPE
5085 020370 000002  .WORD 10002$-.
5086 020372          ENDSEG
5087 020372          10002$:
5088 020372 104405  TRAP  C$ESEG
5089 020374          ENDTST
5090 020374          L10067:
5091 020374 104401  TRAP  C$ETST
5092
5093 020376          BADHEAD
5094          :***** TEST 22 *****
5095          :*CRAM TEST OF JUMP(I) ON BR1 CLEAR MICRO-PROCESSOR INSTRUCTION.
5096          :*CLEAR THE BR1 BIT, PERFORM THE JUMP INSTRUCTION.
5097          :*VERIFY THE JUMP DID OCCUR BY CLOCKING THE INSTRUCTION
5098          :*IN THE LOCATION IT IS AT. THIS I STRUCTION LOADS THE
5099          :*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
5100          :*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
5101          :*THE JUMP WAS SUCCESSFUL, IF THE JUMP WAS UNSUCCESSFUL
5102          :*THEN PORT4 WILL CONTAIN A 37
5103 020376          BADHEAD
5104          :***** TEST 22 *****
5105
5106 020376          BGNST
5107 020376          T22::
5108 020376
5109          MACEX2          ;DON'T DO IF M8200.
5110 020406 104432  :DO NOT DO TEST IF M8200
5111 020410 000240  TRAP  C$EXIT
5112 020412          .WORD L10070-.
5113 020412 013701 002516  MYINT
5114 020416          MOV  KMCSR,R1          ;RECORD DEVICE ADDR.
5115 020422 004737 003474  MSTCLR          ;MASTER CLEAR M8200,4,7
5116 020426          JSR  PC, MEMSET          ;SET MEM AND RAM
5117 020426 104404          1$: BGNSEG
5118 020430 004737 003166  TRAP  C$BSEG
5119 020434          JSR  PC, CLRALL          ;CLEAR ALL CONDITIONS
5120 020434 004537 003100  SROMCLK          ;NEXT WORD IS INSTRUCTION.
5121 020440 100400          JSR  R5, .SROMCLK
5122 020442          100400          ;START AT ROM PC=0
5123 020442 004537 003100  SROMCLK          ;NEXT WORD IS INSTRUCTION.
5124 020446 116777          JSR  R5, .SROMCLK
5125 020450 004737 003330  114377!<400*5>          ;JUMP TO ROM PC OF 1777
5126 020454 000001          JSR  PC, RAMDAT          ;R4=CRAM PC (LSB 8 BITS)
5127 020456 120504          1          ;EXPECTED DATA
5128 020460 001406          CMPB R5,R4          ;IS ROM PC CORRECT?
5129 020462          BEQ  2$          ;BR IF YES
5130 020466 104455          ERROR 5          ;ERROR, CRAM PC IS WRONG
5131 020470 000005  TRAP  C$ERDF
5132 020472 005055  .WORD 5
5133 020474 006556  .WORD EMO
                    .WORD ERR5

```

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5134 020476  
5135 020476 104410  
5136 020500 000002  
5137 020502  
5138 020502  
5139 020502 104405  
5140 020504  
5141 020504 104404  
5142 020506  
5143  
5144 020516 004737 003166  
5145 020522  
5146 020522 004537 003100  
5147 020526 100403  
5148 020530  
5149 020530 004537 003100  
5150 020534 102400  
5151 020536 004737 003330  
5152 020542 000004  
5153 020544 120504  
5154 020546 001406  
5155 020550  
5156 020554 104455  
5157 020556 000005  
5158 020560 005055  
5159 020562 006556  
5160 020564  
5161 020564 104410  
5162 020566 000002  
5163 020570  
5164 020570  
5165 020570 104405  
5166 020572  
5167 020572 104404  
5168 020574 004737 003166  
5169 020600  
5170 020600 004537 003100  
5171 020604 100406  
5172 020606  
5173 020606 004537 003100  
5174 020612 106525  
5175 020614 004737 003330  
5176 020620 000007  
5177 020622 120504  
5178 020624 001406  
5179 020626  
5180 020632 104455  
5181 020634 000005  
5182 020636 005055  
5183 020640 006556  
5184 020642  
5185 020642 104410  
5186 020644 000002  
5187 020646  
5188 020646  
5189 020646 104405

```

2$:  ESCAPE SEG
      TRAP C$ESCAPE
      .WORD 10000$-.
      ENDSEG
10000$:
      TRAP C$ESEG
      BGNSEG
      TRAP C$BSEG
      SKIP06 6$
      :GOTO 6$ IF #B206
      JSR PC,CLRALL          ;CLEAR ALL CONDITIONS
      SROMCLK                ;NEXT WORD IS INSTRUCTION,
      JSR R5,.,SROMCLK
      100403                  ;START AT ROM PC=3
      SROMCLK                ;NEXT WORD IS INSTRUCTION,
      JSR R5,.,SROMCLK
      100000!<400*5>         ;JUMP TO ROM PC OF 0
      JSR PC,RAMDAT          ;R4=CRAM PC (LSB 8 BITS)
      4                       ;EXPECTED DATA
      CMPB R5,R4             ;IS ROM PC CORRECT?
      BEQ 4$                 ;BR IF YES
      ERROR 5                ;ERROR, CRAM PC IS WRONG
      TRAP C$ERDF
      .WORD 5
      .WORD EMO
      .WORD ERR5
4$:  ESCAPE SEG
      TRAP C$ESCAPE
      .WORD 10001$-.
      ENDSEG
10001$:
      TRAP C$ESEG
      BGNSEG
      TRAP C$BSEG
      JSR PC,CLRALL          ;CLEAR ALL CONDITIONS
      SROMCLK                ;NEXT WORD IS INSTRUCTION,
      JSR R5,.,SROMCLK
      100406                  ;START AT ROM PC=6
      SROMCLK                ;NEXT WORD IS INSTRUCTION,
      JSR R5,.,SROMCLK
      104125!<400*5>         ;JUMP TO ROM PC OF 525
      JSR PC,RAMDAT          ;R4=CRAM PC (LSB 8 BITS)
      7                       ;EXPECTED DATA
      CMPB R5,R4             ;IS ROM PC CORRECT?
      BEQ 6$                 ;BR IF YES
      ERROR 5                ;ERROR, CRAM PC IS WRONG
      TRAP C$ERDF
      .WORD 5
      .WORD EMO
      .WORD ERR5
6$:  ESCAPE SEG
      TRAP C$ESCAPE
      .WORD 10002$-.
      ENDSEG
10002$:
      TRAP C$ESEG

```

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5190 020650  
5191 020650  
5192 020650 104401  
5193  
5194 020652  
5195  
5196  
5197  
5198  
5199  
5200  
5201  
5202 020652 020652  
5203  
5204  
5205 020654  
5206  
5207

ENDTST  
L10070:  
TRAP C\$ETST

BADHEAD  
:\*\*\*\*\* TEST 23 \*\*\*\*\*  
:\*CRAM TEST OF JUMP(1) ON BR4 CLEAR MICRO-PROCESSOR INSTRUCTION.  
:\*CLEAR THE BR4 BIT, PERFORM THE JUMP INSTRUCTION.  
:\*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION  
:\*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE  
:\*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT  
:\*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT  
  
:\*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT.  
:\*THEN PORT4 CONTAINS A 37  
BADHEAD  
:\*\*\*\*\* TEST 23 \*\*\*\*\*

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5208	020654		
5209	020654		
5210	020654		
5211			
5212	020664	104432	
5213	020666	000240	
5214	020670		
5215	020670	013701	002516
5216	020674		
5217	020700	004737	003474
5218	020704		
5219	020704	104404	
5220	020706	004737	003166
5221	020712		
5222	020712	004537	003100
5223	020716	100400	
5224	020720		
5225	020720	004537	003100
5226	020724	117377	
5227	020726	004737	003330

```

BGNTST
T23::
MACEX2
:DO NOT DO TEST IF M8200 :DON'T DO IF M8200.
TRAP C$EXIT
.WORD L10071-.
MYINT
MOV KMCSR,R1 :RECORD DEVICE ADDR.
MSTCLR :MASTER CLEAR M8200,4,7
JSR PC,MEMSET :SET MEM AND RAM
1$: BGNSEG
TRAP C$BSEG
JSR PC,CLRALL :CLEAR ALL CONDITIONS
SROMCLK :NEXT WORD IS INSTRUCTION.
JSR R5,.SROMCLK
100400 :START AT ROM PC=0
SROMCLK :NEXT WORD IS INSTRUCTION.
JSR R5,.SROMCLK
114377!<400*6> :JUMP TO ROM PC OF 1777
JSR PC,RAMDAT :R4=(RAM PC (LSB 8 BITS)

```

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```

5228 020732 000001          1          ;EXPECTED DATA
5229 020734 120504          CMPB    R5,R4          ;IS ROM PC CORRECT?
5230 020736 001406          BEQ     2$            ;BR IF YES
5231 020740                ERROR    5              ;ERROR, CRAM PC IS WRONG
5232 020744 104455          TRAP   C$ERDF
5233 020746 000005          .WORD  5
5234 020750 005055          .WORD  EMO
5235 020752 006556          .WORD  ERR5
5236 020754                2$:  ESCAPE  SEG
5237 020754 104410          TRAP   C$ESCAPE
5238 020756 000002          .WORD  10000$-.
5239 020760                ENDSEG
5240 020760                10000$:
5241 020760 104405          TRAP   C$ESEG
5242 020762                BGNSEG
5243 020762 104404          TRAP   C$BSEG
5244 020764                SKIP06 6$
5245                ;GOTO 6$ IF M8206
5246 020774 004737 003166    JSR    PC,CLRALL      ;CLEAR ALL CONDITIONS
5247 021000                SROMCLK
5248 021000 004537 003100    JSR    R5,..SROMCLK  ;NEXT WORD IS INSTRUCTION,
5249 021004 100403                100403
5250 021006                SROMCLK
5251 021006 004537 003100    JSR    R5,..SROMCLK  ;START AT ROM PC=3
5252 021017 103000                100000!<400*6> ;NEXT WORD IS INSTRUCTION,
5253 021014 004737 003330    JSR    PC,RAMDAT     ;JUMP TO ROM PC OF 0
5254 021020 000004                4              ;R4=CRAM PC (LSB 8 BITS)
                    ;EXPECTED DATA

```



5

L 10

SEQ 128

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5255 021022 120504  
5256 021024 001406

CMPB R5,R4  
BEQ 48

:IS ROM PC CORRECT?  
:BSR IF YES

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5257 021026  
5258 021032 104455  
5259 021034 000005  
5260 021036 005055  
5261 021040 006556

ERROR 5  
TRAP C\$ERDF  
.WORD 5  
.WORD EMO  
.WORD ERR5

:ERROR, CRAM PC IS WRONG

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5262 021042  
5263 021042 104410  
5264 021044 000002  
5265 021046  
5266 021046  
5267 021046 104405  
5268 021050  
5269 021050 104404  
5270 021052 004737 003166  
5271 021056  
5272 021056 004537 003100  
5273 021062 100406  
5274 021064  
5275 021064 004537 003100  
5276 021070 107125  
5277 021072 004737 003330  
5278 021076 000007  
5279 021100 120504  
5280 021102 001406  
5281 021104  
5282 021110 104455  
5283 021112 000005  
5284 021114 005055  
5285 021116 006556  
5286 021120  
5287 021120 104410  
5288 021122 000002  
5289 021124  
5290 021124  
5291 021124 104405  
5292 021126  
5293 021126  
5294 021126 104401  
5295  
5296 021130  
5297  
5298  
5299  
5300  
5301  
5302  
5303  
5304  
5305  
5306 021130  
5307  
5308  
5309 021130  
5310 021130  
5311 021130  
5312  
5313 021140 104432  
5314 021142 000240  
5315 021144  
5316 021144 013701 002516  
5317 021150

```

4$:  ESCAPE SEG
     TRAP  C$ESCAPE
     .WORD 10001$-.
     ENDSEG
10001$:
      TRAP  C$ESEG
      BGNSEG
      TRAP  C$BSEG
      JSR   PC,CLRALL          ;CLEAR ALL CONDITIONS
      SROMCLK          ;NEXT WORD IS INSTRUCTION,
      JSR   R5,.SROMCLK
      100406          ;START AT ROM PC=6
      SROMCLK          ;NEXT WORD IS INSTRUCTION,
      JSR   R5,.SROMCLK
      104125!<400*6> ;JUMP TO ROM PC OF 525
      JSR   PC,RAMDAT        ;R4=CRAM PC (LSB 8 BITS)
      7                ;EXPECTED DATA
      CMPB  R5,R4           ;IS ROM PC CORRECT?
      BEQ   6$             ;BR IF YES
      ERROR 5                ;EPROR, CRAM PC IS WRONG
      TRAP  C$ERDF
      .WORD 5
      .WORD EMO
      .WORD ERR5
6$:  ESCAPE SEG
     TRAP  C$ESCAPE
     .WORD 10002$-.
     ENDSEG
10002$:
      TRAP  C$ESEG
ENDTST
L10071:
      TRAP  C$ETST

BADHEAD
:***** TEST 24 *****
:*CRAM TEST OF JUMP(1) ON BR7 CLEAR MICRO-PROCESSOR INSTRUCTION.
:*CLEAR THE BR7 BIT, PERFORM THE JUMP INSTRUCTION.
:*VERIFY THE JUMP DID NOT OCCUR BY CLOCKING THE INSTRUCTION
:*IN THE LOCATION IT IS AT. THIS INSTRUCTION LOADS THE
:*BR WITH THE LOWEST 8 BITS OF THE CRAM PC. AT THIS POINT
:*THE BR DATA IS MOVED TO PORT4. IF THIS DATA IS CORRECT
:*THE CRAM PC IS CORRECT, IF THE CRAM PC IS NOT RIGHT.
:*THEN PORT4 CONTAINS A $7
BADHEAD
:***** TEST 24 *****

BGNTST
T24::
      MACEX2          ;DON'T DO IF M8200.
      ;DO NOT DO TEST IF M8200
      TRAP  C$EXIT
      .WORD L10072-.
      MYINT
      MOV   KMCSR,R1          ;RECORD DEVICE ADDR.
      MSTCLR          ;MASTER CLEAR M8200,4,7

```

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5318 021154 004737 003474
5319 021160
5320 021160 104404
5321 021162 004737 003166
5322 021166
5323 021166 004537 003100
5324 021172 100400
5325 021174
5326 021174 004537 003100
5327 021200 117777
5328 021202 004737 003330
5329 021206 000001
5330 021210 120504
5331 021212 001406
5332 021214
5333 021220 104455
5334 021222 000005
5335 021224 005055
5336 021226 006556
5337 021230
5338 021230 104410
5339 021232 000002
5340 021234
5341 021234
5342 021234 104405
5343 021236
5344 021236 104404
5345 021240
5346
5347 021250 004737 003166
5348 021254
5349 021254 004537 003100
5350 021260 100403
5351 021262
5352 021262 004537 003100
5353 021266 103400
5354 021270 004737 003330
5355 021274 000004
5356 021276 120504
5357 021300 001406
5358 021302
5359 021306 104455
5360 021310 000005
5361 021312 005055
5362 021314 006556
5363 021316
5364 021316 104410
5365 021320 000002
5366 021322
5367 021322
5368 021322 104405
5369 021324
5370 021324 104404
5371 021326 004737 003166
5372 021332
5373 021332 004537 003100

1$: JSR PC, MEMSET ;SET MEM AND RAM
    BGNSEG
    TRAP C$BSEG
    JSR PC, CLRALL ;CLEAR ALL CONDITIONS
    SROMCLK ;NEXT WORD IS INSTRUCTION,
    JSR R5, .SROMCLK
    100400 ;START AT ROM PC=0
    SROMCLK ;NEXT WORD IS INSTRUCTION,
    JSR R5, .SROMCLK
    114377!<400*7> ;JUMP TO ROM PC OF 1777
    JSR PC, RAMDAT ;R4=CRAM PC (LSB 8 BITS)
    1 ;EXPECTED DATA
    CMPB R5, R4 ;IS ROM PC CORRECT?
    BEQ 2$ ;BR IF YES
    ERROR 5 ;ERROR, CRAM PC IS WRONG
    TRAP C$ERDF
    .WORD 5
    .WORD EMO
    .WORD ERR5

2$: ESCAPE SEG
    TRAP C$ESCAPE
    .WORD 10000$-.
    ENDSEG

10000$: TRAP C$ESEG
    BGNSEG
    TRAP C$BSEG
    SKIP06 6$
    ;GOTO 6$ IF M8206
    JSR PC, CLRALL ;CLEAR ALL CONDITIONS
    SROMCLK ;NEXT WORD IS INSTRUCTION,
    JSR R5, .SROMCLK
    100403 ;START AT ROM PC=3
    SROMCLK ;NEXT WORD IS INSTRUCTION,
    JSR R5, .SROMCLK
    100000!<400*7> ;JUMP TO ROM PC OF 0
    JSR PC, RAMDAT ;R4=CRAM PC (LCB 8 BITS)
    4 ;EXPECTED DATA
    CMPB R5, R4 ;IS ROM PC CORRECT?
    BEQ 4$ ;BR IF YES
    ERROR 5 ;ERROR, CRAM PC IS WRONG
    TRAP C$ERDF
    .WORD 5
    .WORD EMO
    .WORD ERR5

4$: ESCAPE SEG
    TRAP C$ESCAPE
    .WORD 10001$-.
    ENDSEG

10001$: TRAP C$ESEG
    BGNSEG
    TRAP C$BSEG
    JSR PC, CLRALL ;CLEAR ALL CONDITIONS
    SROMCLK ;NEXT WORD IS INSTRUCTION,
    JSR R5, .SROMCLK

```

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5374 021336 100406          100406          ;START AT ROM PC=6
5375 021340          SR0MCLK          ;NEXT WORD IS INSTRUCTION,
5376 021340 004537 003100  JSR      R5,.SR0MCLK
5377 021344 107525          104125!<400*7>      ;JUMP TO ROM PC OF 525
5378 021346 004737 003330  JSR      PC,RAMDAT   ;R4=CRAM PC (LSB 8 BITS)
5379 021352 000007          7                ;EXPECTED DATA
5380 021354 120504          CMPB     R5,R4      ;IS ROM PC CORRECT?
5381 021356 001406          BEQ     6$         ;BR IF YES
5382 021360          ERROR     5        ;ERROR, CRAM PC IS WRONG
5383 021364 104455          TRAP    C$ERDF
5384 021366 000005          .WORD  5
5385 021370 005055          .WORD  EMO
5386 021372 006556          .WORD  ERR5
5387 021374          6$:  ESCAPE  SEG
5388 021374 104410          TRAP    C$ESCAPE
5389 021376 000002          .WORD  10002$-.
5390 021400          ENDSEG
5391 021400          10002$:
5392 021400 104405          TRAP    C$ESEG
5393 021402          ENDTST
5394 021402          L10072:
5395 021402 104401          TRAP    C$ETST
5396
5397 021404          BADHEAD
5398          ;***** TEST 25 *****
5399          ;*
5400          ;*MAIN MEMORY PAGE DUAL ADDRESS TEST.
5401          ;*IN THIS TEST WE WILL VERIFY THAT PAGES DO
5402          ;*NOT DUAL ADDRESS. THIS TEST IS DIFFERENT FROM THE
5403          ;*PREVIOUS DUAL ADDRESS TESTS IN THAT THE OTHER
5404          ;*TEST REALLY DIDN'T CHECK PAGE DUAL ADDRESSING
5405 021404          BADHEAD
5406          ;***** TEST 25 *****
5407
5408 021404          BGNTST
5409 021404          T25::
5410 021404          K4ONLY          ;FOR 4K CPUS ONLY.
5411          ;DO NOT DO TEST IF M8200, OR M8204
5412 021414 104432          TRAP    C$EXIT
5413 021416 000156          .WORD  L10073-.
5414 021420          MYINT
5415 021420 013701 002516  MOV     KMCSR,R1    ;RECORD DEVICE ADDR.
5416 021424          MSTCLR
5417 021430 005002          CLR R2
5418 021432 042737 000037 021456 1$: BIC #37,2$      ;R2 WILL BE PAGE #
5419 021440 050237 021456  BIS R2,2$        ;CLEAR UNUSED BITS
5420 021444          ROMCLK          ;ADD CURRENT PAGE MARKER.
5421 021444 004537 003044  JSR     R5,.ROMCLK ;SET ADDR D
5422 021450 010000          10000          ;CLOCK INSTRUCTION
5423 021452          ROMCLK          ;OF PAGE X
5424 021452 004537 003044  JSR     R5,.ROMCLK ;CLOCK INSTRUCTION
5425 021456 004000          2$: 4000        ;THIS LOCATION MODIFIED BY LOST
5426          ;FEW INSTRUCTIONS
5427 021460 010261 000004  MOV R2,4(R1)      ;PUT PAGE # INTO PART 4
5428 021464          ROMCLK          ;CLOCK PART 4 INTO MEMORY
5429 021464 004537 003044  JSR     R5,.ROMCLK ;CLOCK INSTRUCTION

```

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```

5430 021470 122500          122500          ;WHOSE PAGE # IS IN R2
5431 021472 005202          INC R2          ;UPDATE PAGE #
5432 021474 032702 000020  BIT #20,R2     ;DONE ALL PAGES?
5433 021500 001754          BEQ 1$         ;NO-DO NEXT ONE
5434
5435
5436
5437
5438
5439
5440 021502 005002          CLR R2          ;R2 STILL HAS PAGE NUMBER
5441
5442 021504 042737 000037 021522 3$:  BIC #37,4$
5443 021512 050237 021522  BIC R2,4$
5444 021516          ROMCLK          ;LOAD PAGE NUMBER
5445 021516 004537 003044  JSR R5,.ROMCLK ;CLOCK INSTRUCTION
5446 021522 004000          4$: 4000
5447 021524          ROMCLK          ;MOVE MEM TO PART 4
5448 021524 004537 003044  JSR R5,.ROMCLK ;CLOCK INSTRUCTION
5449 021530 041224          041224
5450 021532 116104 000004  MOVB 4(R1),R4  ;"FOUND"
5451 021536 110205          MOVB R2,R5     ;"EXPECTED"
5452 021540 120504          CMPB R5,R4     ;ADDRESS PROBLEM?
5453 021542 001406          BEQ 5$
5454
5455 021544          ERROR 13      ;PAGE ADDRESSING ERROR IN MAIN
5456 021550 104455          TRAP C$ERDF
5457 021552 000015          .WORD 13
5458 021554 005055          .WORD EMO
5459 021556 007542          .WORD ERR13
5460
5461
5462
5463
5464 021560          5$:  ESCAPE TST
5465 021560 104410          TRAP C$ESCAPE
5466 021562 000012          .WORD L10073-.
5467 021564 005202          INC R2
5468 021566 032702 000020  BIT #20,R2     ;UPDATE PAGE ADDRESS
5469 021572 001744          BEQ 3$         ;ALL DONE?
5470
5471 021574          ENDTST
5472 021574          L10073:
5473 021574 104401          TRAP C$ETST
5474
5475
5476 021576          BADHEAD
5477          ;***** TEST 26 *****
5478          ;*
5479          ;*JUMP FIELD,PAGE TEST
5480          ;*
5481          ;*IN THIS TEST WILL MAKE SURE A JUMP FIELD INSTRUCTION
5482          ;*WORKS. TO DO THIS, WE'LL PUT THE DESIRED PAGE, FIELD
5483          ;*INORMATION IN IBUS* <13> THEN ISSUE A JUMP FIELD
5484          ;*THEN WE'LL READ PC REG. AND VERIFY.
5485          ;** REV. E - CHANGE TO TEST BITS 4 & 5 (PC BITS 12 & 13)

```

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```

5486 021576          RADHEAD
5487                ;***** TEST 26 *****
5488
5489 021576          BGNTST
5490 021576          T26::
5491 021576
5492                K4ONLY                ;FOR 4K CPUS ONLY
5493 021606 104432    ;DO NOT DO TEST IF M8200, OR M8204
5494 021610 000132    TRAP C$EXIT
5495 021612          .WORD L10074-.
5496 021612 013701 002516 MYINT
5497 021616          MOV KMCSR,R1                ;RECORD DEVICE ADDR.
5498                MSTCLR
5499 021622 005002    CLR R2                ;R2 TO CONTAIN FIELD #
5500
5501
5502
5503 021624 042737 000077 021642 1$: BIC #77,2$    ;CLEAR ANY JUNK (REV E - CHANGE TO 77)
5504 021632 050237 021642          BIS R2,2$    ;SET FIELD # INTO INSTR.
5505
5506 021636          ROMCLK                ;CLOCK FIELD BITS INTO BREG.
5507 021636 004537 003044          JSR R5,,ROMCLK ;CLOCK INSTRUCTION
5508 021642 000400          2$: 000400          ;CONTAINS FIELD,PAGE BITS
5509 021644          ROMCLK                ;XFERR BREG INTO IBUS* <13>
5510 021644 004537 003044          JSR R5,,ROMCLK ;CLOCK INSTRUCTION
5511 021650 061233          061233
5512 021652          SRMCLK                ;GET INSTRUCTION CLOCKED.
5513 021652 004537 003100          JSR R5,,SRMCLK
5514 021656 100000          100000          ;BAS FORM FOR JUM FIELD INSTR.
5515
5516
5517 021660 142761 000002 000001 BICB #BIT1,1(R1) ;CLEAR ROMI
5518 021666          ROMCLK                ;CLOCK NEXT INSTR.
5519 021666 004537 003044          JSR R5,,ROMCLK ;CLOCK INSTRUCTION
5520 021672 121264          121264          ;MOVE IBUS* TO PORT 4
5521 021674 116104 000004          MOVB 4(R1),R4 ;GET IT.
5522 021700 042704 177700          BIC #^C<77>,R4 ;(REV E - CHANGE TO 77)
5523 021704 120402          CMPB R4,R2 ;FIELD OK?
5524 021706 001407          BEQ 3$ ;IF OK GO AHEAD
5525 021710 010205          MOV R2,R5
5526 021712          ERROR 14                ;CHANGE FIELD INSTRUCTION ;*** B0
5527 021716 104455          TRAP C$ERDF
5528 021720 000016          .WORD 14
5529 021722 005055          .WORD EMO
5530 021724 007664          .WORD ERR14
5531
5532                ;FAILED. FOR FIELD,PAGE INDICATES
5533                ;BY "EXPECTED" BITS 0,1,2,3 OF
5534                ;EXPECTED REPRESENT FIELD BITS.
5534 021726          3$: ESCAPE TST
5535 021726 104410          TRAP C$ESCAPE
5536 021730 000012          .WORD L10074-.
5537
5538
5539 021732 005202          INC R2                ;UPDATE TO NEXT FIELD
5540 021734 032702 000100          BIT #100,R2 ;DONE ALL FIELDS? (REV E - CHANGE TO 100)
5541 021740 001731          BEQ 1$

```

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5542  
5543 021742  
5544 021742  
5545 021742 104401  
5546  
5547 021744

ENDTST  
L10074:

TRAP CSETST

BADHEAD

:\*\*\*\*\* TEST 27 \*\*\*\*\*

:\*JUMP TEST, JUMP ALWAYS, JUMP CHANGE FIELD

:\*IN THIS TEST, WE WILL CHECK THE ABILITY OF THE  
:\*MICRO PROCESSOR TO JUMP (BRANCH & ALWAYS INSTRUCTION)  
:\*TO LOCATIONS, FIELDS FROM OTHER LOCATIONS FIELDS.  
:\*WE ALREADY KNOW THAT THE BRANCH INSTR WORKS FROM  
:\*OTHER TEST.

PROCEDURE:

1. START ADDR 0, FIELD 0
2. \*\*CALCULATE NEW ADDR, FIELD VIA INC.
3. CAUSE JUMP (BRANCH) TO NEW ADDRESS
4. READ PC FROM IBUS\*12 AND IBUS\*13
5. REPEAT STEP 2-4 256.TIMES

TO CALCULATE NEW ADDRESS:

1. INC LOW BYTE OF ADDRESS FOR PC ADDRESS 0-7
  2. INC LOW BYTE OF NADDRESS FOR PC ADDRESS 8-11  
BITS REPRESENTED AS BITS 0-3. WHEN 0-3 OVERFLOWS,  
RESTARTS AT ZERO.
- NET RESULT IS JUMPS FROM:

FIELD,PAGE	LOC
0	0
1	1
2	2
3	3
10	7
11	11
:10	:
17	377

BADHEAD

:\*\*\*\*\* TEST 27 \*\*\*\*\*

5548  
5549  
5550  
5551  
5552  
5553  
5554  
5555  
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5557  
5558  
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5577  
5578  
5579 021744  
5580  
5581  
5582 021744  
5583 021744  
5584 021744  
5585 021744 013701 002516  
5586 021750  
5587  
5588 021760 104432  
5589 021762 000336  
5590 021764  
5591  
5592 021770 012737 000000 002406  
5593  
5594  
5595  
5596 021776 012702 000000  
5597

T27::

BGNTST

MYINT  
MOV KMCSR,R1 ;RECORD DEVICE ADDR.  
K4ONLY ;4K CPUS ONLY.  
:DO NOT DO TEST IF M8200, OR M8204  
TRAP C\$EXIT  
.WORD L10075-.  
MSTCLR

MOV #0, FLAG ;FLAG TO REPRESENT  
;FIELD,PAGE  
;TO VARIE STARTING PAGE,FIELD,  
;CHANGE #0 PORTION OF INSTR.  
MOV #0, R2 ;R2 TO CONTAIN JUMPED  
;TO CHANGE STARTING IMM ADDR.,



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 CZDMQE.P11 30-SEP-82 15:35 HARDWARE TESTS

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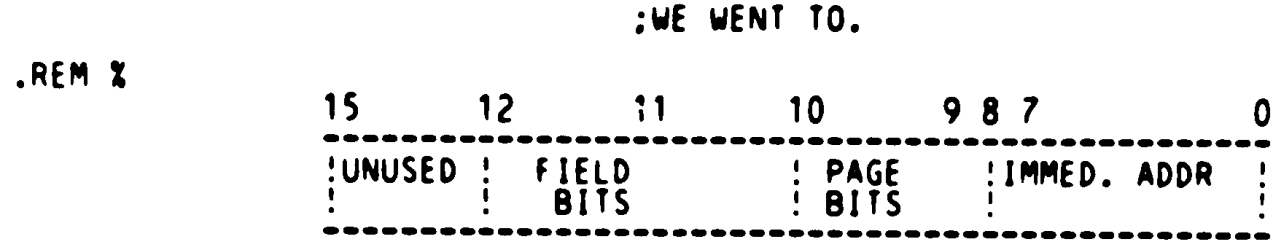
5598
5599 022002 012737 000000 002412      MOV    #0, FADR      ;VARIE #0 PORTIONS OF INSTR.
5600                                ;LOOP HERE          ;ADDRESS
5601 022010
5602 022010 042737 000017 022050 1$:   BIC #17,2$          ;CLEAR JUNK FROM FIELD
5603                                ;PORTION OF CHANGE FIELD INSTR
5604 022016 013700 002406      MOV FLAG,R0          ;INORDER TO INC, DEC FIELD,PAGE
5605 022022 042700 177760      BIC #^C<17>,R0
5606 022026 050037 022050      BIS R0,2$           ;NOW POSITION IN INSTR.
5607 022032 042737 077777 022064      BIC #077777,3$     ;NOW FOR IMMED. BR INSTR.
5608 022040 050237 022064      BIS R2,3$           ;NOW ADD IMMEDIATE ADDR
5609
5610
5611
5612 022044
5613 022044 004537 003044      ROMCLK
5614 022050 000400 2$:   JSR    R5,.ROMCLK   ;CLOCK INSTRUCTION
5615 022052      000400          ;MOVE PAGE, FIELD # TO BREG.
5616 022052 004537 003044      ROMCLK
5617 022054 061233 61233   JSR    R5,.ROMCLK   ;CLOCK INSTRUCTION
5618 022060      061233          ;MOV    BREG TO PC HIGH REG.
5619 022060 004537 003100      SROMCLK
5620 022064 100000 3$:   JSR    R5,.SROMCLK
5621      100000          ;NOW CLOCK IT IN BY JMP FIELD INSTR.
5622 022066
5623 022066 004537 003044      ROMCLK
5624 022072 121265 121265   JSR    R5,.ROMCLK   ;READ PC REG HI
5625 022074      121265          ;CLOCK INSTRUCTION
5626 022074 004537 003044      ROMCLK
5627 022100 121244 121244   JSR    R5,.ROMCLK   ;READ PC REG LOW
5628      121244          ;CLOCK INSTRUCTION
5629 022102 016104 000004      MOV 4(R1),R4
5630 022106 042704 170000      BIC #170000,R4
5631      ;READ PC REG (NOW IN SEL 4)
5632 022112 013705 022050      MOV 2$,R5           ;STRIP FOR ONLY PAGE, FIELD BITS.
5633 022116 000305
5634 022120 042705 170377      SWAB R5
5635 022124 050205 170377      BIC #170377,R5
5636 022126      ;NOW FROM ADDR WE WANTED TO
5637      SKIP06 5$      ;JUMP TO
5638 022136 105205 5$:   ;GOTO 5$ IF M8206
5639 022140      INCB  R5      ;CLEAR JUNK
5640      ;ADD IMMED ADDR
5641      ;UPDATE ADDR. EXPECTED SENCE THE READ
5642 022140 020504
5643 022142 001406
5644 022144      ;OF THE IBUS <13> INC THE PC.
5645 022150 104455
5646 022152 000017
5647 022154 005055
5648 022156 010006
5649
5650
5651
5652
5653

```

;JUMP GO OK?  
 ;YEA, CONTINUES  
 ;FAILED TO JUMP PROPERLY.  
 ;"FROM ADDR" REPRESENTS  
 ;THE ADDRESS WE STARTED AT  
 ;"TO ADDR" REPRESENTS WHERE  
 ;WE EXPECTED TO JUMP TO,  
 ;"BAD ADDR" REPRESENTS WHERE

5654  
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5705  
5706  
5707  
5708  
5709

022160  
022160 104410  
022162 000136  
022164 010437 002412  
022170 005237 002406  
022174 105202  
022176 001304  
  
  
  
  
  
  
  
  
  
  
022200  
  
  
022210 005737 002470  
022214 001041  
022216 005737 002472  
022222 001036  
022224 052711 040000  
022230 105761 000001  
022234 042711 040000  
  
  
022240  
022240 004537 003044  
022244 121265  
022246  
022246 004537 003044  
022252 121244



:THIS IS A PICTURE OF THE P.C. REG.  
BITS 0-7 ARE IN IBUS\*  
BITS 8-11 ARE IN IBUS\*  
THEY GOT CLOCK IN THERE VIA JUMPS TAKEN  
THE FIELD BITS  
ARE IN BIT POSITION 0,1 OF THE INSTRUCTION AT 2\$.

3\$ WAS THE JUMP ALWAYS INSTRUCTION. THE IMMED. ADDR.  
WAS IN 0-7 OF THE JUMP INSTR. THE PAGE BITS,  
PC REG BITS 8,9, WERE IN BITS 11,12 OF THE INSTR.  
JUMP INSTRUCTIONS HAVE BEEN CHECKED OUT  
BEFORE, SO THE IMPORTANT THING TO REMEMBER TO  
WATCH IS THE "FROM ADDR", "TO ADDR"

%

4\$:

ESCAPE TST  
TRAP C\$ESCAPE  
.WORD L10075-  
MOV R4,FADR  
INC FLAG ;UPDATE PAGE,FIELD  
INCB R2 ;UPDATE IMMED. ADDR  
BNE 1\$ ;LOOP IF NOT DONE.

\*  
\*CHECK HERE TO SEE IF MASTER CLEAR CLEARS P.C. REG  
\*

SKIP06 40\$  
:GOTO 40\$ IF M8206  
TST RUNB  
BNE 40\$  
TST RUNINH  
BNE 40\$  
BIS #40000,(R1) ;SET MASTER CLEAR  
TSTB 1(R1)  
BIC #40000,(R1)

:TO RUN THIS SECTION OF CODE YOU MUST TURN SW7 OF SWITCH PACK #E28  
:OFF SO THAT M8207 NOT SELFSTARTING.

ROMCLK ;WE MUST FIRST CLOCK  
JSR R5,..ROMCLK ;CLOCK INSTRUCTION  
121265 ;THE PC LATCH REGS  
ROMCLK ;BEFORE WE CAN READ THEM  
JSR R5,..ROMCLK ;CLOCK INSTRUCTION  
121244

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```

5710 022254 ROMCLK ;REG PC REG HI, PUT IN PORT5
5711 022254 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
5712 022260 121265 121265
5713
5714 022262 ROMCLK ;REG PC REG LOW, PUT IN PORT4
5715 022262 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
5716 022266 121244 121244
5717 022270 005005 CLR R5 ;EXPECT ZERO
5718 022272 016104 000004 MOV 4(R1),R4 ;READ PC REG FROM PORT 4&5
5719 022276 042704 170003 BIC #170003,R4
5720 022302 001406 BEQ 40$ ;IF CLEARED, EXIT
5721 ;NOTE WE ALSO CLEARED BIT 1 OF THE
5722 ;PC REG, BECAUSE AFTER THE MASTER
5723 ;CLEAR, WE DID TWO INSTRUCTIONS TO
5724 ;READ IT, THUS CAUSING THE PC REG
5725 ;TO GET BUMPED.
5726
5727 022304 ERROR 45 ;MASTER CLEAR FAILED TO CLEAR
5728 022310 104455 TRAP C$ERDF
5729 022312 000055 .WORD 45
5730 022314 005055 .WORD EMO
5731 022316 011124 .WORD ERR45
5732 ;PC REG
5733 022320 40$:
5734 022320 ENDTST
5735 022320 L10075:
5736 022320 104401 TRAP C$ETST
5737 022322 BADHEAD
5738 ;***** TEST 28 *****
5739 ;
5740 ;JUMP TEST, JUMP ALWAYS, JUMP CHANGE FIELD
5741 ;
5742 ;*IN THIS TEST, WE WILL CHECK THE ABILITY OF THE
5743 ;*MICRO PROCESSOR TO JUMP (BRANCH & ALWAYS INSTRUCTION)
5744 ;*TO LOCATIONS, FIELDS FROM OTHER LOCATIONS FIELDS.
5745 ;*WE ALREADY KNOW THAT THE BRANCH INSTR WORKS FROM
5746 ;*OTHER TEST. PROCEDURE:
5747 ; 1. START ADDR 0, FIELD 0
5748 ; 2. **CALCULATE NEW ADDR, FIELD VIA DEC,
5749 ; 3. CAUSE JUMP (BRANCH) TO NEW ADDRESS
5750 ; 4. READ PC FROM IBUS*12 AND IBUS*13
5751 ; 5. REPEAT STEP 2-4 256.TIMES
5752 ;
5753 ;TO CALCULATE NEW ADDRESS:
5754 ; 1. DEC LOW BYTE OF ADDRESS FOR PC ADDRESS 0-7
5755 ; 2. DEC LOW BYTE OF NADDRESS FOR PC ADDRESS 8-11
5756 ; BITS REPRESENTED AS BITS 0-3. WHEN 0-3 OVERFLOWS,
5757 ; RESTARTS AT ZERO.
5758 ; NET RESULT IS JUMPS FROM:
5759 ; FIELD,PAGE LOC
5760 ; 0 0
5761 ; 17 377

```

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```

5762          : *                16                376
5763          : *                15                375
5764          : *                :TO                :
5765          : *                00                000
5766          : *
5767 022322    : BADHEAD
5768          : ***** TEST 28 *****
5769          :
5770 022322    : BGNTST
5771 022322    T28: :
5772 022322    : MYINT
5773 022322 013701 002516 : MOV KMCSR,R1 ;RECORD DEVICE ADDR.
5774 022326    : K4ONLY ;4K CPUS ONLY.
5775          : ;DO NOT DO TEST IF M8200, OR M8204
5776 022336 104432 : TRAP C$EXIT
5777 022340 000216 : .WORD L10076-.
5778 022342    : MSTCLR
5779          :
5780 022346 012737 000000 002406 : MOV #0, FLAG ;FLAG TO REPRESENT
5781          : ;FIELD,PAGE
5782          : ;TO VARIE STARTING PAGE,FIELD,
5783          : ;CHANGE #0 PORTION OF INSTR.
5784 022354 012702 000000    : MOV #0, R2 ;R2 TO CONTAIN JUMPED
5785          : ;TO CHANGE STARTING IMM ADDR.,
5786          : ;VARIE #0 PORTIONS OF INSTR.
5787 022360 012737 000000 002412 : MOV #0, FADR ;ADDRESS
5788          : ;LOOP HERE
5789 022366    T1S: :
5790 022366 042737 000017 022426 : BIC #17,2$ ;CLEAR JUNK FROM FIELD
5791          : ;PORTION OF CHANGE FIELD INSTR
5792 022374 013700 002406    : MOV FLAG,R0 ;INORDER TO INC, DEC FIELD,PAGE
5793 022400 042700 177760    : BIC #^C<17>,R0
5794 022404 050037 022426    : BIS R0,2$ ;NOW POSITION IN INSTR.
5795 022410 042737 077777 022442 : BIC #077777,3$ ;NOW FOR IMMED. BR INSTR.
5796 022416 050237 022442    : BIS R2,3$ ;NOW ADD IMMEDIATE ADDR
5797          :
5798          :
5799          :
5800 022422    : ROMCLK
5801 022422 004537 003044    T2S: : JSR R5,..ROMCLK ;CLOCK INSTRUCTION
5802 022426 000400    : 000400 ;MOVE PAGE,FIELD # TO BREG.
5803 022430    : ROMCLK
5804 022430 004537 003044    : JSR R5,..ROMCLK ;CLOCK INSTRUCTION
5805 022434 061233    : 61233 ;MOV BREG TO PC HIGH REG.
5806 022436    : SROMCLK
5807 022436 004537 003100    T3S: : JSR R5,..SROMCLK
5808 022442 100000    : 100000 ;NOW CLOCK IT IN BY JMP FIELD INSTR.
5809          :
5810 022444    : ROMCLK
5811 022444 004537 003044    : JSR R5,..ROMCLK ;READ PC REG HI
5812 022450 121265    : 121265 ;CLOCK INSTRUCTION
5813 022452    : ROMCLK
5814 022452 004537 003044    : JSR R5,..ROMCLK ;READ PC REG LOW
5815 022456 121244    : 121244 ;CLOCK INSTRUCTION
5816          :
5817 022460 016104 000004    : MOV 4(R1),R4 ;READ PC REG (NOW IN SEL 4)

```

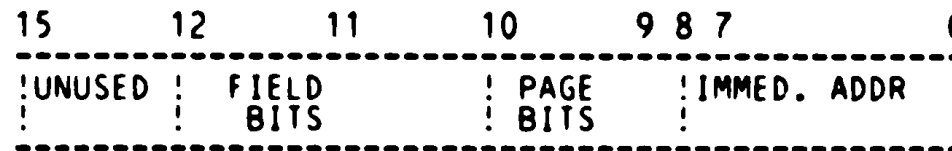
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```

5818 022464 042704 170000          BIC    #170000,R4          ;STRIP FOR ONLY PAGE,FIELD BITS.
5819                                     ;
5820 022470 013705 022426          MOV 2$,R5                ;NOW FROM ADDR WE WANTED TO
5821 022474 000305                   SWAB R5                  ;JUMP TO
5822 022476 042705 170377          BIC #170377,R5          ;CLEAR JUNK
5823 022502 050205                   BIS R2,R5                ;ADD IMMED ADDR
5824 022504                                     ;
5825                                     ;
5826 022514 105205                   INCB  R5                  ;UPDATE ADDR. EXPECTED SENSE THE READ
5827 022516          5$:                                     ;OF THE IBUS <13> INC THE PC.
5828                                     ;
5829                                     ;
5830 022516 020504                   CMP R5,R4                ;JUMP GO OK?
5831 022520 001406                   BEQ 4$                   ;YEA, CONTINUES
5832 022522                   ERROR 15                 ;FAILED TO JUMP PROPERLY.
5833 022526 104455                   TRAP  C$ERDF
5834 022530 000017                   .WORD 15
5835 022532 005055                   .WORD EMO
5836 022534 010006                   .WORD ERR15
5837                                     ;
5838                                     ;"FROM ADDR" REPRESENTS
5839                                     ;THE ADDRESS WE STARTED AT
5840                                     ;"TO ADDR" REPRESENTS WHERE
5841                                     ;WE EXPECTED TO JUMP TO,
5842                                     ;"BAD ADDR" REPRESENTS WHERE
5843                                     ;WE WENT TO.
5844                                     ;
5845          .REM %
5846                                     ;
5847                                     ;
5848                                     ;
5849                                     ;
5850                                     ;
5851                                     ;
5852                                     ;
5853                                     ;
5854                                     ;
5855                                     ;
5856                                     ;
5857                                     ;
5858                                     ;
5859                                     ;
5860                                     ;
5861                                     ;
5862                                     ;
5863                                     ;
5864                                     ;
5865                                     ;
5866                                     ;
5867 022536          4$:          ESCAPE TST
5868 022536 104410          TRAP  C$ESCAPE
5869 022540 000016          .WORD L10076-
5870 022542 010437 002412          MOV R4,FADR
5871 022546 005337 002406          DEC FLAG
5872 022552 105302          DECB R2
5873 022554 001304          BNE 1$
                                     ;UPDATE PAGE,FIELD
                                     ;UPDATE IMMED. ADDR
                                     ;LOOP IF NOT DONE.

```



;THIS IS A PICTURE OF THE P.C. REG.  
 BITS 0-7 ARE IN IBUS\* <12>  
 BITS 8-11 ARE IN IBUS\* <13>  
 THEY GOT CLOCK IN THERE VIA JUMPS TAKEN  
 THE FIELD BITS  
 ARE IN BIT POSITION 0,1 OF THE INSTRUCTION AT 2\$.  
  
 3\$ WAS THE JUMP ALWAYS INSTRUCTION. THE IMMED. ADDR.  
 WAS IN 0-7 OF THE JUMP INSTR. THE PAGE BITS,  
 PC REG BITS 8,9, WERE IN BITS 11,12 OF THE INSTR.  
 JUMP INSTRUCTIONS HAVE BEEN CHECKED OUT  
 BEFORE, SO THE IMPORTANT THING TO REMEMBER TO  
 WATCH IS THE "FROM ADDR", "TO ADDR"

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5874
5875
5876 022556
5877 022556
5878 022556 104401
5879 022560
5880
5881
5882
5883
5884
5885
5886 022560
5887
5888
5889 022560
5890 022560
5891 022560
5892
5893 022570 104432
5894 022572 000200
5895 022574
5896 022600
5897 022600 013701 002516
5898 022604 004737 003166
5899 022610
5900 022610 004537 003044
5901 022614 121264
5902 022616 116104 000004
5903 022622 042704 177477
5904 022626 012705 000000
5905 022632 120405
5906 022634 001410
5907 022636
5908 022642 104455
5909 022644 000020
5910 022646 005055
5911 022650 010134
5912
5913 022652
5914 022652 104410
5915 022654 000116
5916 022656 004737 003312
5917 022662
5918 022662 004537 003044
5919 022666 121264
5920
5921 022670 016104 000004
5922 022674 042704 177477
5923 022700 012705 000200
5924 022704 120405
5925 022706 001410
5926 022710
5927 022714 104455
5928 022716 000020
5929 022720 005055

ENDTST
L10076:
TRAP C$ETST
BADHEAD
:***** TEST 29 *****
:*
:* IN THIS TEST WE'LL VERIFY THAT THE Z BIT CAN BE READ FROM
:* IBUS* <13>. WE ALLREADY KNOW THAT THE Z BIT WORKS PROPERLY,
:* ALL WE WANT TO KNOW HERE IS THAT IT CAN BE READ.
:*
BADHEAD
:***** TEST 29 *****

T29::
BGNTST
K4ONLY
:DO NOT DO TEST IF M8200, OR M8204 :M8206 & M8207 ONLY!
TRAP C$EXIT
.WORD L10077-.
MSTCLR
MYINT
MOV KMCSR,R1 :RECORD DEVICE ADDR.
JSR PC,CLRALL :CLR CONDITION CODES.
ROMCLK :NOW READ IBUS* <15>PUT IN PORT 4
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121264
MOVB 4(R1),R4 :READ IT FROM PORT 4
BIC #177477,R4 :STRIP ANY JUNK,C&Z BITS 6,7
MOV #0,R5 :EXPECT IT CLEAR
CMPB R4,R5 :OK?
BEQ 1$
ERROR 16 :FAILURE OF Z&C TO BE CLEAR.
TRAP C$ERDF
.WORD 16
.WORD EMO
.WORD ERR16

1$:
ESCAPE TST
TRAP C$ESCAPE
.WORD L10077-.
JSR PC,SETZ :SET Z BIT.
ROMCLK :NOW GO BACK AND CHECK Z BIT SET.
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121264
MOV 4(R1),R4 :GET INFO.
BIC #^C<300>,R4 :STRIP FOR C&Z BITS.
MOV #200,R5 :EXPECT ONLY Z BIT SET.
CMPB R4,R5 :SET OK?
BEQ 2$
ERROR 16 :Z BIT FAILED TO SET PROPERLY.
TRAP C$ERDF
.WORD 16
.WORD EMO

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5930 022722 010134          .WORD   ERR16
5931
5932 022724          ESCAPE  TST
5933 022724 104410        TRAP   C$ESCAPE
5934 022726 000044        .WORD   L10077-.
5935 022730 004737 003166 2$:   JSR   PC,CLRALL          ;NOW TRY TO CLEAR Z BIT.
5936 022734          ROMCLK
5937 022734 004537 003044  JSR   R5,.ROMCLK      ;CLOCK INSTRUCTION
5938 022740 121264        JSR   121264
5939 022742 016104 000004  MOV   4(R1),R4
5940 022746 042704 177477  BIC   #^C<300>,R4      ;STRIP FOR C&Z BITS
5941 022752 001407        BEQ   3$                ;IF ZERO,WE'RE OK
5942 022754 005005        CLR   R5                ;ELSE REPORT ERROR
5943 022756          ERROR  16          ;Z BIT FAILED TO CLEAR PROPERLY.
5944 022762 104455        TRAP   C$ERDF
5945 022764 000020        .WORD   16
5946 022766 005055        .WORD   EMO
5947 022770 010134        .WORD   ERR16
5948 022772          3$:
5949 022772          ENDTST
5950 022772          L10077:
5951 022772 104401        TRAP   C$ETST
5952          ;FINDFAST
5953 022774          BADHEAD
5954          ;***** TEST 30 *****
5955          ;*
5956          ;* IN THIS TEST WE'LL VERIFY THAT THE C BIT CAN BE READ FROM
5957          ;* IBUS*<13>. WE ALLREADY KNOW THAT THE C BIT WORKS PROPERLY,
5958          ;* ALL WE WANT TO KNOW HERE IS THAT IT CAN BE READ.
5959          ;*
5960 022774          BADHEAD
5961          ;***** TEST 30 *****
5962
5963 022774          T30::
5964 022774          BGNTST
5965 022774          K4ONLY          ;M8206 &M8207 ONLY!
5966          ;DO NOT DO TEST IF M8200, OR M8204
5967 023004 104432        TRAP   C$EXIT
5968 023006 000200        .WORD   L10100-.
5969 023010          MSTCLR
5970 023014          MYINT
5971 023014 013701 002516  MOV   KMCSR,R1          ;RECORD DEVICE ADDR.
5972 023020 004737 003166  JSR   PC,CLRALL        ;CLR CONDITION CODES.
5973 023024          ROMCLK          ;NOW READ IBUS*<13>PUT IN PORT 4
5974 023024 004537 003044  JSR   R5,.ROMCLK      ;CLOCK INSTRUCTION
5975 023030 121264        JSR   121264
5976 023032 116104 000004  MOVB  4(R1),R4          ;READ IT FROM PORT 4
5977 023036 042704 177477  BIC   #177477,R4      ;STRIP ANY JUNK,C&Z BITS 6,7
5978 023042 012705 000000  MOV   #0,R5            ;EXPECT IT CLEAR
5979 023046 120405        CMPB  R4,R5            ;OK?
5980 023050 001410        BEQ   1$
5981 023052          ERROR  16          ;FAILURE OF Z&C TO BE CLEAR.
5982 023056 104455        TRAP   C$ERDF
5983 023060 000020        .WORD   16
5984 023062 005055        .WORD   EMO
5985 023064 010134        .WORD   ERR16

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5986
5987 023066          ESCAPE TST
5988 023066 104410   TRAP  C$ESCAPE
5989 023070 000116   .WORD L10100-
5990 023072 004737 0032b0 1$: JSR  PC,SETC          ;SET C BIT.
5991 023076          ROMCLK          ;NOW GO BACK AND CHECK C BIT SET.
5992 023076 004537 003044 JSR  R5,.ROMCLK      ;CLOCK INSTRUCTION
5993 023102 121264   121264
5994 023104 016104 000004 MOV  4(R1),R4        ;GET INFO.
5995 023110 042704 177477 BIC  #^C<300>,R4    ;STRIP FOR C&Z BITS.
5996 023114 012705 000100 MOV  #100,R5        ;EXPECT ONLY C BIT SET.
5997 023120 120405   CMPB R4,R5          ;SET OK?
5998 023122 001410   BEQ  2$
5999 023124          ERROR  16          ;C BIT FAILED TO SET PROPERLY.
6000 023130 104455   TRAP C$ERDF
6001 023132 000020   .WORD 16
6002 023134 005055   .WORD EMO
6003 023136 010134   .WORD ERR16
6004
6005 023140          ESCAPE TST
6006 023140 104410   TRAP  C$ESCAPE
6007 023142 000044   .WORD L10100-
6008 023144 004737 003166 2$: JSR  PC,CLRALL        ;NOW TRY TO CLEAR C BIT.
6009 023150          ROMCLK          ;CLOCK INSTRUCTION
6010 023150 004537 003044 JSR  R5,.ROMCLK
6011 023154 121264   121264
6012 023156 016104 000004 MOV  4(R1),R4
6013 023162 042704 177477 BIC  #^C<300>,R4    ;STRIP FOR C&Z BITS
6014 023166 001407   BEQ  3$            ;IF ZERO,WE'RE OK
6015 023170 005005   CLR  R5            ;ELSE REPORT ERROR
6016 023172          ERROR  16          ;C BIT FAILED TO CLEAR PROPERLY.
6017 023176 104455   TRAP C$ERDF
6018 023200 000020   .WORD 16
6019 023202 005055   .WORD EMO
6020 023204 010134   .WORD ERR16
6021 023206          3$:
6022 023206          L10100:
6023 023206          ENDTST
6024 023206 104401   TRAP  C$SETST
6025 023210          BADHEAD
6026          ;***** TEST 31 *****
6027          ;*TEST OF PROGRAM CLOCK BIT
6028          ;*DO A MASTER CLEAR, VERIFY THAT PROGRAM CLOCK IS SET
6029          ;*WRITE PROGRAM CLOCK BIT TO A ONE, VERIFY THAT IT CLEARS.
6030          ;*AND THEN SETS SOME TIME LATER
6031 023210          BADHEAD
6032          ;***** TEST 31 *****
6033
6034 023210          BGNTST
6035 023210          T31::
6036 023210          MYINT
6037 023210 013701 002516 MOV  KMCSR,R1        ;RECORD DEVICE ADDR.
6038 023214          MSTCLP          ;MASTER CLEAR M8200,4,7
6039 023220 005037 002440 CLR  TEMP            ;PREPARE FOR
6040 023224 005037 002444 CLR  $TMP0           ;DELAY
6041 023230 012761 000020 000004 1$: MOV #20,4(R1)        ;LOAD PORT 4

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6042	023236	152761	000002	000001	BISB	#BIT1,1(R1)	:SET ROMI
6043	023244	012761	121111	000006	MOV	#121111,6(R1)	:SEL6 INSTRUCTION
6044	023252	152761	000003	000001	BISB	#BIT1!BIT0,1(R1)	:SET CLOCK BIT
6045	023260	012761	121224	000006	MOV	#121224,6(R1)	:LOAD NEXT INSTRUCTION
6046	023266	152761	000003	000001	BISB	#BIT1!BIT0,1(R1)	:READ CLOCK BIT
6047	023274	142761	030001	000001	BICB	#BIT!BIT0,1(R1)	:CLEAR MAINT BITS
6048	023302	016104	000004		MOV	4(R1),R4	:PUT 'FOUND' IN R4
6049	023306	005037	002452		CLR	\$GDDAT	:PUT 'EXPECTED' IN \$GDDAT
6050	023312	123704	002452		CMPB	\$GDDAT,R4	:IS PGM CLOCK CLEAR?
6051	023316	001406			BEQ	2\$	
6052	023320	013702	002452		MOV	\$GDDAT,R2	
6053	023324				ERRDF	50,EMB50	:ERROR, PGM CLOCK IS NOT CLEAR
6054	023324	104455			TRAP	C\$ERDF	
6055	023326	000062			.WORD	50	
6056	023330	005545			.WORD	EMB50	
6057	023332	000000			.WORD	0	
6058	023334			2\$:			
6059	023334				ROMCLK		:NEXT WORD IS INSTRUCTION,
6060	023334	004537	003044		JSR	R5,.ROMCLK	:CLOCK INSTRUCTION
6061	023340	121224			121224		:PORT4 LUI1
6062	023342	122761	000020	000004	CMPB	#20,4(R1)	:IS PGM CLOCK SET?
6063	023350	001420			BEQ	3\$	:BR IF YES
6064	023352	005237	002440		INC	TEMP	:INCREMENT DELAY
6065	023356	005537	002444		ADC	\$TMPO	:INCREMENT DELAY
6066	023362	022737	000006	002444	CMP	#6,\$TMPO	:IS DELAY DONE
6067	023370	001361			BNE	2\$	:BR IF NO
6068	023372	012702	000006		MOV	#6,R2	
6069	023376	013704	002444		MOV	\$TMPO,R4	
6070	023402				ERRDF	51,EMB51	:ERROR PGM CLOCK NOT SET
6071	023402	104455			TRAP	C\$ERDF	
6072	023404	000063			.WORD	51	
6073	023406	005577			.WORD	EMB51	
6074	023410	000000			.WORD	0	
6075	023412			3\$:			
6076							
6077	023412	122737	000007	002414	CMPB	#7,WTYPE	: ONLY DO NEXT TEST IF MB207
6078	023420	001013			BNE	4\$	: EXIT IF NOT.
6079							
6080	023422	005737	002444		TST	\$TMPO	: IF ANY LARGE COUNT, WE'RE OK
6081	023426	001010			BNE	4\$	: THEN EXIT
6082							
6083	023430	042737	000007	002440	BIC	#7,TEMP	: CLEAR OUT ANY SMALL COUNT
6084	023436	001004			BNE	4\$	: IF LARGE COUNT LEFT OVER, WE'RE OK.
6085							
6086	023440				ERRDF	100,EMB1	: ERROR
6087	023440	104455			TRAP	C\$ERDF	
6088	023442	000144			.WORD	100	
6089	023444	005410			.WORD	EMB1	
6090	023446	000000			.WORD	0	
6091							: TIME TOO SHORT FOR CLOCK. MUST BE
6092							: DEFECTIVE CAPACITOR IN TIMEING CIRCUIT.
6093	023450			4\$:			
6094							
6095	023450			ENDTST			
6096	023450			L10101:			
6097	023450	104401			TRAP	C\$ETST	

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6098
6099 023452
6100
6101
6102
6103
6104
6105
6106
6107 023452
6108
6109
6110 023452
6111 023452
6112 023452
6113 023452 104433
6114 023454
6115 023454 013701 002516
6116
6117 023460
6118 023464 005037 002440
6119 023470 013737 000024 002444
6120 023476 013746 000024
6121 023502 012737 023564 000024
6122 023510 012761 000002 000004
6123 023516 012711 001000
6124 023522 012761 121111 000006
6125 023530 012711 005400
6126 023534 005237 002440
6127 023540 001375
6128 023542
6129 023546
6130 023552 104455
6131 023554 000021
6132 023556 005055
6133 023560 010256
6134 023562 000445
6135 023564 012737 023602 000024 1$:
6136 023572 010637 023600
6137 023576 000000
6138 023600 000000 2$:
6139 023602 013706 023600 3$:
6140 023606 012737 024002 000024
6141 023614 005037 024000
6142 023620 005237 024000 12$:
6143 023624 001375
6144
6145
6146 023626
6147 023630 013701 002516
6148 023634 012637 000024
6149 023640 023737 002444 000024
6150 023646 001413
6151 023650
6152 023654 104455
6153 023656 000021

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BADHEAD
:***** TEST 32 *****
:*FORCE POWER FAIL TEST
:*SET FORCE POWER FAIL BIT VERIFY THAT PROCESSOR TRAPS TO 24
:*GOING DOWN AND COMING UP. VERIFY ALSO THAT BUS INIT WAS
:*BLOCKED FROM GETTING TO THE M8200,4,7 DURING THE POWER FAIL
:*THIS TEST WILL TAKE LONGER THAN 2 SECONDS TO RUN. THIS TEST
:*SHOULD NOT BE RUN IF YOU HAVE VOLATILABLE MEMORY IN YOUR SYSTEM.
BADHEAD
:***** TEST 32 *****

BGNTST
T32::

BRESET
TRAP C$RESET ;STALL FOR TIME
MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
;R1 CONTAINS BASE M8200,4,7 ADDRESS
MSTCLR ;MASTER CLEAR M8200,4,7
CLR TEMP ;PREPARE FOR DELAY
MOV @#24,$TMP0 ;SAVE POWER FAIL ADDRESS
MOV @#24,-(SP) ;STORE POWER FAIL ADDRESS
MOV #1$,@#24 ;SET U FOPR FORCE POWER FAIL
MOV #2,4(R1) ;LOAD PORT4
MOV #BIT9,(R1) ;SET ROMI
MOV #12111,6(R1) ;LOAD INSTRUCTION
MOV #BIT9!BIT8!BIT11,(R1) ;CLOCK INSTRUCTION
INC TEMP ;WAIT FOR POWER FAIL
BNE 5$ ;BR IF DELAY NOT DONE
MSTCLR
ERROR 17 ;ERROR, NO POWER FAIL
TRAP C$ERDF
.WORD 17
.WORD EMO
.WORD ERR17
BR 4$
MOV #3$,@#24 ;POWER UP ADDRESS
MOV SP,2$ ;STORE STACK
HALT ;WAIT FOR POWER UP SEQUENCE
0
MOV 2$,SP ;RESTORE STACK
MOV #10$,@#24 ;PUT IN CASE OF FALSE POWER-UP.
CLR 11$
INC 11$ ;STALL ON POWER UP.
BNE 12$ ;WAIT HERE IF BAD,WILL POWER OUT OF HERE.
;ELSE PROCEED.

POPSP2 ;POP STACK TWICE2
MOV KMCSR,R1
MOV (SP)+,@#24 ;RESTORE TRUE POWER FAIL ADDRESS
CMP $TMP0,@#24 ;IS IT CORRECT?
BEQ 4$ ;BR IF YES
ERROR 17 ;ERROR, STACK IS INCORRECT
TRAP C$ERDF
.WORD 17

```

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6154 023660 005055      .WORD  EMO
6155 023662 010256      .WORD  ERR17
6156 023664 013737 002444 000024  MOV  $TMP0,@#24      ;RESTORE TRUE POWER FAIL ADDRESS
6157 023672 013706 002344  MOV  PSTACK,SP      ;RESTORE STACK
6158 023676 032711 004000 4$:  BIT  #BIT11,(R1)    ;BIT11 STILL SET?
6159 023702 001016      BNE   7$
6160 023704 005737 002470      TST  RUNB
6161 023710 001013      BNE   7$
6162 023712 011104      MOV  (R1),R4
6163 023714 012705 004000  MOV  #BIT11,R5
6164 023720      ERROR 35      ;OAC FAILED
6165 023724 104455      TRAP C$ERDF
6166 023726 000043      .WORD 35
6167 023730 005055      .WORD  EMO
6168 023732 010472      .WORD  ERR35
6169
6170
6171
6172 023734      EXIT  TST
6173 023734 104432      TRAP C$EXIT
6174 023736 000104      .WORD L10102-
6175 023740 012711 003000 7$:  MOV  #BIT9:BIT10,(R1) ;SEL6 = MAINT IR
6176 023744 012705 121111  MOV  #12111,R5      ;R5 = EXPECTED
6177 023750 016104 000006  MOV  6(R1),R4      ;R4 = FOUND
6178 023754 020504      CMP  R5,R4          ;MAINT IR SHOULD = 12111
6179 023756 001431      BEQ  6$             ;BR IF OK
6180 023760      MSTCLR
6181 023764      ERROR 35      ;IF = 0 THEN BUS INIT WAS
6182 023770 104455      TRAP C$ERDF
6183 023772 000043      .WORD 35
6184 023774 005055      .WORD  EMO
6185 023776 010472      .WORD  ERR35
6186
6187
6188
6189 024000 000000 11$: .WORD 0      ;TEMP COUNT FOR STALL ON POWER UP.
6190
6191 024002 052711 040000 10$: BIS  #BIT14,(R1) ;CLR THE THING SO IT CAN'T ASSIRT AC LOW
6192
6193 024006      MSTCLR
6194 024012      ERROR 17      ;ERROR GLIP GAVE US SECOUND UNEXPECTED
6195 024016 104455      TRAP C$ERDF
6196 024020 000021      .WORD 17
6197 024022 005055      .WORD  EMO
6198 024024 010256      .WORD  ERR17
6199
6200
6201 024026 062706 000004      ADD  #4,SP
6202 024032 012637 000024      MOV  (SP)+,@#24
6203 024036
6204 024042
6205 024042
6206 024042 104401 6$:  ENDTST
6207 024042      L10102: TRAP C$ETST
6208
6209 024044      BADHEAD

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6210 :***** TEST 33 *****
6211 :*MICRO-PROCESSOR NOISE TEST
6212 :*WRITE ALL ZERO'S THEN ALL ONE'S THEN A DATA PATTERN
6213 :*TO THE IBUS* AND IBUS REGISTERS AND TO THE SP AND MAIN MEM
6214 :*THEN GO BACK AND READ THE DATA PATERNS TO VERIFY THAT
6215 :*READING AND WRITING OF OTHER LOCATIONS AND REGISTERS
6216 :*DID NOT CHANGE THE DATA.
6217 024044 BADHEAD
6218 :***** TEST 33 *****
6219
6220 024044 BGNTST
6221 024044 T33::
6222 024044
6223 024044 013701 002516 MYINT
6224 024050 MOV KMCSR,R1 ;RECORD DEVICE ADDR.
6225 024054 005002 MSTCLR ;MASTER CLEAR M8200,4,7
6226 024056 042737 000017 024104 1$: CLR R2 ;R2 IS INDEX REGISTER
6227 024064 156237 025100 024104 BIC #17,2$ ;CLEAR ADDRESS FIELD
6228 024072 116261 025106 000004 BISB 30$(R2),2$ ;ADD IBUS* REG ADDRESS TO INSTRUCTION
6229 024100 MOVB 31$(R2),4(R1) ;LOAD PORT4
6230 024100 004537 003044 ROMCLK ;NEXT WORD IS INSTRUCTION,
6231 024104 121100 2$: JSR R5,..ROMCLK ;CLOCK INSTRUCTION
6232 024106 005202 INC R2 ;WRITE IBUS* REGISTER
6233 024110 022702 000005 CMP #5,R2 ;INC INDEX REGISTER
6234 024114 001360 BNE 1$ ;DONE YET?
6235 024116 005002 CLR R2 ;BR IF NO
6236 024120 042737 000017 024166 3$: BIC #17,4$ ;R2 IS IBUS REGISTER ADDRESS
6237 024126 042737 000017 024202 BIC #17,5$ ;CLEAR ADDRESS FIELD OF INSTRUCTIONS
6238 024134 042737 000017 024214 BIC #17,6$
6239 024142 050237 024166 BIS R2,4$ ;ADD IBUS REG ADDRESS TO INSTRUCTION
6240 024146 050237 024202 BIS R2,5$
6241 024152 050237 024214 BIS R2,6$
6242 024156 105061 000004 CLRB 4(R1) ;CLEAR PORT4
6243 024162 ROMCLK ;NEXT WORD IS INSTRUCTION,
6244 024162 004537 003044 JSR R5,..ROMCLK ;CLOCK INSTRUCTION
6245 024166 122100 4$: MOVB #377,4(R1) ;WRITE 0 TO IBUS REG
6246 024170 112761 000377 000004 ROMCLK ;LOAD PORT4
6247 024176 004537 003044 JSR R5,..ROMCLK ;NEXT WORD IS INSTRUCTION,
6248 024176 122100 5$: JSR 122100 ;CLOCK INSTRUCTION
6249 024202 110261 000004 MOVB R2,4(R1) ;WRITE ALL ONES TO IBUS REG
6250 024210 ROMCLK ;LOAD PORT4
6251 024210 004537 003044 JSR R5,..ROMCLK ;NEXT WORD IS INSTRUCTION,
6252 024214 122100 6$: JSR 122100 ;CLOCK INSTRUCTION
6253 024216 005202 INC R2 ;WRITE ITS OWN ADDRESS TO IBUS REG
6254 024220 022702 000010 CMP #10,R2 ;NEXT ADDRESS
6255 024224 001335 BNE 3$ ;DONE YET?
6256 024226 005002 CLR R2 ;BR IF NO
6257 024230 042737 000017 024276 7$: BIC #17,8$ ;START AT SP ADDRESS 0
6258 024236 042737 000017 024312 BIC #17,9$ ;CLEAR ADDRESS FIELD
6259 024244 042737 000017 024324 BIC #17,10$
6260 024252 050237 024276 BIS R2,8$ ;ADD ADDRESS TO INSTRUCTION
6261 024256 050237 024312 BIS R2,9$
6262 024262 050237 024324 BIS R2,10$
6263 024266 105061 000004 CLRB 4(R1) ;CLEAR PORT4
6264 024272 ROMCLK ;NEXT WORD IS INSTRUCTION,
6265

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6266	024272	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6267	024276	123100			8\$:	123100		:WRITE ZERO TO SP
6268	024300	112761	000377	000004		MOVB	#377,4(R1)	:LOAD PORT4
6269	024306					ROMCLK		:NEXT WORD IS INSTRUCTION,
6270	024306	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6271	024312	123100			9\$:	123100		:WRITE ALL ONES TO SP
6272	024314	110261	000004			MOVB	R2,4(R1)	:LOAD PORT4
6273	024320					ROMCLK		:NEXT WORD IS INSTRUCTION,
6274	024320	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6275	024324	123100			10\$:	123100		:WRITE SP ADDRESS TO ITSELF
6276	024326	005202				INC	R2	:NEXT SP ADDRESS
6277	024330	022702	000020			CMP	#20,R2	:DONE YET?
6278	024334	001335				BNE	7\$	:BR IF NO
6279	024336	005002				CLR	R2	:R2 = ,AOM ,E, ADDRESS
6280	024340					ROMCLK		:NEXT WORD IS INSTRUCTION,
6281	024340	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6282	024344	010000				010000		:MAR - 0
6283	024346					ROMCLK		
6284	024346	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6285	024352	004000				4000		
6286	024354	105061	000004		11\$:	CLRB	4(R1)	:CLEAR PORT4
6287	024360					ROMCLK		:NEXT WORD IS INSTRUCTION,
6288	024360	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6289	024364	122500				122500		:WRITE ZEROS TO MEM
6290	024366	112761	000377	000004		MOVB	#377,4(R1)	:LOAD PORT4
6291	024374					ROMCLK		:NEXT WORD IS INSTRUCTION,
6292	024374	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6293	024400	122500				122500		:WRITE ONES TO MEM
6294	024402	110261	000004			MOVB	R2,4(R1)	:LOAD PORT4
6295	024406					ROMCLK		:NEXT WORD IS INSTRUCTION,
6296	024406	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6297	024412	136500				136500		:WRITE TO MEM IT OWN ADDRESS
6298	024414	005202				INC	R2	:NEXT MEM ADDRESS
6299	024416	022702	001000			CMP	#1000,R2	:DONE YET?
6300	024422	001354				BNE	11\$	:BR IF NO
6301								
6302								
6303								:NOW GO BACK AND READ EVERYTHIN
6304	024424					ROMCLK		:NEXT WORD IS INSTRUCTION,
6305	024424	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6306	024430	010000				010000		:MAR 0
6307	024432					ROMCLK		:NEXT WORD IS INSTRUCTION,
6308	024432	004537	003044			JSR	R5,,ROMCLK	:CLOCK INSTRUCTION
6309	024436	004000				4000		:MAR HI - 0 (M8200,4,7 ONLY)
6310								:WOULD BE CRAM CODE
6311	024440	005737	002432			IST	TYPE	
6312	024444	001452				BEQ	40\$	
6313	024446	005005				CLR	R5	:R5 IS INDEX REGISTER
6314	024450	042737	000360	024512	12\$:	BIC	#360,13\$	:CLEAR ADDRESS FIELD
6315	024456	116502	025100			MOVB	30\$(R5),R2	:R2 = IBUS* ADDRESS
6316	024462	010203				MOV	R2,R3	:PUT IBUS* ADDRESS IN R3
6317	024464	006303				ASL	R3	:SHIFT ADDRESS TO BITS 4-7
6318	024466	006303				ASL	R3	
6319	024470	006303				ASL	R3	
6320	024472	006303				ASL	R3	
6321	024474	050337	024512			BIS	R3,13\$	:ADD ADDRESS TO INSTRUCTION

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6322	024500	116537	025106	002452		MOVB	31\$(R5),%GDDAT	;%GDDAT = 'EXPECTED'
6323	024506					ROMCLK		;%NEXT WORD IS INSTRUCTION,
6324	024506	004537	003044			JSR	R5,ROMCLK	;%CLOCK INSTRUCTION
6325	024512	121004			13\$:	121004		;%PORT4 - IBUS* REGISTER
6326	024514	016104	000004			MOV	4(R1),R4	;%R4 = 'FOUND'
6327	024520	123704	002452			CMPB	%GDDAT,R4	;%IBUS* CONTENTS OK?
6328	024524	001416				BEQ	20\$	;%BR IF YES
6329	024526	010237	002434			MOV	R2,MRO	
6330	024532	105037	002453			CLRB	%GDDAT+1	
6331	024536	013705	002452			MOV	%GDDAT,R5	
6332	024542					ERROR	29	;%IBUS* DATA ERROR
6333	024546	104455				TRAP	C\$ERDF	
6334	024550	000035				.WORD	29	
6335	024552	005055				.WORD	EMO	
6336	024554	010350				.WORD	ERR29	
6337	024556					ESCAPE	TST	
6338	024556	104410				TRAP	C\$ESCAPE	
6339	024560	000334				.WORD	L10103-	
6340	024562	005205			20\$:	INC	R5	;%INC COUNTER
6341	024564	022705	000005			CMP	#5,R5	;%DONE YET?
6342	024570	001327				BNE	12\$	;%BR IF NO
6343								
6344	024572				40\$:			
6345						;END CRAM,GENERAL TESTS		
6346								
6347	024572	005002				CLR	R2	;%R2 = IBUS REG ADDRESS
6348	024574	042737	000360	024630	14\$:	BIC	#360,15\$	;%CLEAR ADDRESS FIELD OF INSTRUCTION
6349	024602	010203				MOV	R2,R3	;%R3 = IBUS ADDRESS
6350	024604	006303				ASL	R3	;%SHIFT ADDRESS TO BITS 4-7
6351	024606	006303				ASL	R3	
6352	024610	006303				ASL	R3	
6353	024612	006303				ASL	R3	
6354	024614	050337	024630			BIS	R3,15\$	;%ADD ADDRESS TO INSTRUCTION,
6355	024620	010237	002452			MOV	R2,%GDDAT	;%GDDAT = 'EXPECTED'
6356	024624					ROMCLK		;%NEXT WORD IS INSTRUCTION,
6357	024624	004537	003044			JSR	R5,ROMCLK	;%CLOCK INSTRUCTION
6358	024630	021004			15\$:	021004		;%PORT4 - IBUS REG
6359	024632	016104	000004			MOV	4(R1),R4	;%IBUS = 'FOUND'
6360	024636	123704	002452			CMPB	%GDDAT,R4	;%IBUS CONTENTS OK?
6361	024642	001410				BEQ	21\$	;%BR IF YES
6362	024644	013705	002452			MOV	%GDDAT,R5	
6363	024650					ERROR	29	;%IBUS DATA ERROR
6364	024654	104455				TRAP	C\$ERDF	
6365	024656	000035				.WORD	29	
6366	024660	005055				.WORD	EMO	
6367	024662	010350				.WORD	ERR29	
6368	024664	005202			21\$:	INC	R2	;%NEXT IBUS REGISTER
6369	024666	022702	000010			CMP	#10,R2	;%DONE YET?
6370	024672	001340				BNE	14\$	;%BR IF NO
6371	024674	005002				CLR	R2	;%R2 = SP ADDRESS
6372	024676	042737	000017	024714	16\$:	BIC	#17,17\$	;%CLEAR ADDRESS FIELD OF INSTRUCTION
6373	024704	050237	024714			BIS	R2,17\$	;%ADD ADDRESS TO INSTRUCTION
6374	024710					ROMCLK		;%NEXT WORD IS INSTRUCTION,
6375	024710	004537	003044			JSR	R5,ROMCLK	;%CLOCK INSTRUCTION
6376	024714	040600			17\$:	040600		;%BR - SP
6377	024716	010237	002452			MOV	R2,%GDDAT	;%GDDAT = 'EXPECTED'

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6378	024722			ROMCLK						:NEXT WORD IS INSTRUCTION, ROMCLK PC-5304
6379	024722	004537	003044	JSR	R5,ROMCLK					:CLOCK INSTRUCTION
6380	024726	061224		061224						:PORT4 BR
6381	024730	016104	000004	MOV	4(R1),R4					:R4 = 'FOUND'
6382	024734	123704	002452	CMPB	\$GDDAT,R4					:SP CONTENTS OK?
6383	024740	001412		BEQ	22\$					:BR IF YES
6384	024742	013705	002452	MOV	\$GDDAT,R5					
6385	024746			ERROR	7					:SP DATA ERROR
6386	024752	104455		TRAP	C\$ERDF					
6387	024754	000007		.WORD	7					
6388	024756	005055		.WORD	EMO					
6389	024760	007026		.WORD	ERR7					
6390	024762			ESCAPE	TST					
6391	024762	104410		TRAP	C\$ESCAPE					
6392	024764	000130		.WORD	L10103-					
6393	024766	005202		22\$: INC	R2					:NEXT SP LOCATION
6394	024770	022702	000020	CMP	#20,R2					:DONE YET?
6395	024774	001340		BNE	16\$					:BR IF NO
6396	024776	005002		CLR	R2					:R2 = MEMORY ADDRESS
6397	025000			ROMCLK						:NEXT WORD IS INSTRUCTION,
6398	025000	004537	003044	JSR	R5,ROMCLK					:CLOCK INSTRUCTION
6399	025004	010000		010000						:MAR 0
6400	025006			ROMCLK						:NEXT WORD IS INSTRUCTION,
6401	025006	004537	003044	JSR	R5,ROMCLK					:CLOCK INSTRUCTION
6402	025012	004000		4000						:MAR HI 0 (MB200,4,7 OR FAMILY ONLY)
6403	025014	010237	002452	18\$: MOV	R2,\$GDDAT					:\$GDDAT = 'EXPECTED'
6404	025020			ROMCLK						:NEXT WORD IS INSTRUCTION,
6405	025020	004537	003044	JSR	R5,ROMCLK					:CLOCK INSTRUCTION
6406	025024	055224		055224						:PORT4 MAIN MEM
6407	025026	016104	000004	MOV	4(R1),R4					:R4 = 'FOUND'
6408	025032	123704	002452	CMPB	\$GDDAT,R4					:MAIN MEM CONTENTS OK?
6409	025036	001412		BEQ	23\$					:BR IF YES
6410	025040	013705	002452	MOV	\$GDDAT,R5					
6411	025044			ERROR	6					:MAIN MEM DATA ERROR
6412	025050	104455		TRAP	C\$ERDF					
6413	025052	000006		.WORD	6					
6414	025054	005055		.WORD	EMO					
6415	025056	006700		.WORD	ERR6					
6416	025060			ESCAPE	TST					
6417	025060	104410		TRAP	C\$ESCAPE					
6418	025062	000032		.WORD	L10103-					
6419	025064	005202		23\$: INC	R2					:NEXT MEM ADDRESS
6420	025066	022702	001000	CMP	#1000,R2					:DONE YET?
6421	025072	001350		BNE	18\$					:BR IF NO
6422	025074			EXIT	TST					
6423	025074	104432		TRAP	C\$EXIT					
6424	025076	000016		.WORD	L10103-					
6425	025100	000	002	003 30\$: .BYTE	0,2,3,5,10					
6426	025103	005	010							
6427										
6428		025106		.EVEN						
6429	025106	001	003	004 31\$: .BYTE	1,3,4,6,10					
6430	025111	006	010							

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6431
6432          025114          .EVEN
6433
6434 025114          ENDTST
6435 025114          L10103:
6436 025114 104401          TRAP      C$ETST
6437
6438 025116          BADHEAD
6439          :***** TEST 34 *****
6440          :* THIS TEST IS DESIGNED TO MAKE SURE THAT A NODST INSTRUCTION
6441          :* DOES NOT WRITE INTO PORT B OF THE MULTIPOINT RAM.
6442          :* TO DO THIS, WE'LL PUT A 125 INTO INDAT2, THEN WE'LL PUT A
6443          :* 125 INTO BOTH SP1 AND BR. LAST WE'LL DO A NODST BR, SUBOC, SP1
6444          :* IF THERE IS A WRITE INTO PORTB, INDAT2 WILL CONTAIN A 377.
6445 025116          BADHEAD
6446          :***** TEST 34 *****
6447
6448 025116          BGN1ST
6449 025116          T34::
6450 025116
6451 025116 013701 002516          MYINT
6452 025122          MOV      KMCSR,R1          ;RECORD DEVICE ADDR.
6453 025122 004537 003044          ROMCLK
6454 025126 000525          JSR      R5,,ROMCLK          ;CLOCK INSTRUCTION
6455 025130          00525          ;PUT A 125 INTO BRG.
6456 025130 004537 003044          ROMCLK
6457 025134 062221          JSR      R5,,ROMCLK          ;CLOCK INSTRUCTION
6458 025136          062221          ;NOW INTO 0IDAT2
6459 025136 004537 003044          ROMCLK
6460 025142 063221          JSR      R5,,ROMCLK          ;CLOCK INSTRUCTION
6461 025144          63221          ;NOW INTO SP1
6462 025144 004537 003044          ROMCLK
6463 025150 060361          JSR      R5,,ROMCLK          ;CLOCK INSTRUCTION
6464          060361          ;NOW THE 'NODST BR,SUBOC,SP1'
6465          ;THE NODST SHOULD NOT MODIFY INDAT2!
6466 025152          ROMCLK
6467 025152 004537 003044          JSR      R5,,ROMCLK          ;CLOCK INSTRUCTION
6468 025156 020420          020420          ;PUT CONTENT OF INDAT2 IN BRG.
6469
6470 025160          ROMCLK
6471 025160 004537 003044          JSR      R5,,ROMCLK          ;CLOCK INSTRUCTION
6472 025164 061220          061220          ;PUT BRG INTO BSEL0
6473
6474 025166 111104          MOVB     (R1),R4          ;SEE WHAT CAME BACK.
6475 025170 012705 000125          MOV      #125,R5          ;SHOULD BE 125 IF 377 CAME BACK.
6476          ;YOU CAN BET THAT THE 'NODST' WROTE
6477          ;INTO THE MULTIPOINT RAM! WATCH SIGNAL
6478          ; 'D1 WRITE OUT L'
6479
6480 025174 020405          CMP      R4,R5          ;NOW LOOK.
6481 025176 001406          BEQ     10$
6482
6483 025200          ERROR 7
6484 025204 104455          TRAP   C$ERDF
6485 025206 000007          .WORD 7
6486 025210 005055          .WORD EMO

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6487 025212 007026          .WORD  ERR7
6488
6489 025214          10$:
6490 025214          ENDTST
6491 025214          L10104:
6492 025214 104401      TRAP  C$ETST
6493
6494 025216          BADHEAD
6495          :***** TEST 35 *****
6496          :*
6497          :* EXTENDED CRAM TEST FOR M8206. IN THIS TEST WE WILL LOAD DATA
6498          :* THROUGHOUT THE CRAM (TEST DATA IS JUST 4K OF DIAG. CODE) AND
6499          :* THEN READ IT BACK AND VERIFY THAT IT IS CORRECT.
6500 025216          BADHEAD
6501          :***** TEST 35 *****
6502
6503 025216          BGNTST
6504 025216          T35::
6505 025216          SKIP06 10$          ;DO TEST ONLY IF IT IS A M8206
6506          :GOTO 10$ IF M8206
6507 025226          EXIT  TST          ;OTHERWISE,SKIP TEST.
6508 025226 104432      TRAP  C.EXIT
6509 025230 000132      .WORD  L10105-.
6510
6511 025232          10$:  MYINT
6512 025232 013701 002516  MOV  KMCSR,R1          ;RECORD DEVICE ADDR.
6513
6514 025236 012702 012146  MOV  #ROMMAP,R2       ;GET ADDR. OF LIST.
6515
6516 025242 012711 002000  MOV  #2000,(R1)       ;SET TO WRITE DATA.
6517 025246 005003      CLR  R3               ;CRAM ADDR ZERO.
6518
6519 025250 010361 000004  15$:  MOV  R3,4(R1)       ;SET ADDR.
6520 025254 012261 000006  MOV  (R2)+,6(R1)      ;WRITE DATA.
6521
6522 025260 020337 002436  CMP  R3,MEMSZ         ;DONE WHOLE CRAM?
6523 025264 001402      BEQ  20$             ;YES,EXIT THIS LOOP.
6524 025266 005203      INC  R3              ;NO,UPDAT ADDR.
6525 025270 000767      BR   15$
6526 025272 005003      20$:  CLR  R3              ;NOW WE WILL READ BACK,STARTING AT
6527          :CRAM ADDR. ZERO.
6528 025274 012705 012146  MOV  #ROMMAP,R5       ;GET ADDR. LIST OF DATA
6529
6530 025300 010361 000004  30$:  MOV  R3,4(R1)       ;SET ADDR.
6531
6532 025304 011502      MOV  (R5),R2          ;PUT EXPECTED INTO R2
6533 025306 016104 000006  MOV  6(R1),R4         ;READ ACCUAL
6534 025312 020204      CMP  R2,R4           ;EQUAL?
6535 025314 001411      BEQ  40$             ;YES,CONTINUE.
6536 025316 010300      MOV  R3,R0
6537
6538 025320          ERROR  1          ;ERROR CRAM DATA TEST,DATA
6539 025324 104455      TRAP  C$ERDF
6540 025326 000001      .WORD  1
6541 025330 005055      .WORD  EMO
6542 025332 006032      .WORD  ERR1
    
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6543                                     ;READ NOT DATA THAT WAS WRITTEN.
6544
6545 025334                               ESCAPE TST
6546 025334 104410                       TRAP C$ESCAPE
6547 025336 000024                       .WORD L10105-
6548 025340 020337 002436               40$: CMP R3, MEMSZ
6549 025344 001002                       BNE 50$                                     ;ALL DONE?
6550
6551 025346                               EXIT TST
6552 025346 104432                       TRAP C$EXIT
6553 025350 000012                       .WORD L10105-
6554
6555 025352 005203                       50$: INC R3                                     ;UPDATE ADDR.
6556 025354 062705 000002               ADD #2, R5
6557 025360 000747                       BR 30$
6558
6559 025362                               ENDTST
6560 025362                               L10105:
6561 025362 104401                       TRAP C$ETST
6562
6563
6564 025364                               BADHEAD
6565                                     ;***** TEST 36 *****
6566                                     ;*
6567                                     ;* THIS TEST LOADS MICRO-CODE INTO A M8206 MCPU THEN EXECUTES IT.
6568                                     ;* THE MICRO CODE IS DESIGNED TO WRITE ALL ONES INTO THE SEL REGS.
6569                                     ;* THIS TEST IS ONLY PERFORMED ON AN M8206.
6570 025364                               BADHEAD
6571                                     ;***** TEST 36 *****
6572
6573 025364                               BGNTST
6574 025364                               T36::
6575
6576 025364                               SKIP06 1$                                     ;ONLY DO THIS TEST IF M8206
6577                                     ;GOTO 1$ IF M8206
6578 025374                               EXIT TST
6579 025374 104432                       TRAP C$EXIT
6580 025376 000442                       .WORD L10106-
6581
6582 025400                               1$: MYINT
6583 025400 013701 002516               MOV KMCSR, R1                                     ;RECORD DEVICE ADDR.
6584
6585 025404 004537 026006               JSR R5, LOADER                                     ;LOAD THE MICRO CODE
6586
6587 025410 000777                       777
6588 025412 061220                       ;MOVE #377, BRG
6589 025414 061222                       ;MOVE BRG, BSEL0
6590 025416 061223                       ;MOVE BRG, BSEL2
6591 025420 061224                       ;MOVE BRG, BSEL3
6592 025422 061225                       ;MOVE BRG, BSEL4
6593 025424 061226                       ;MOVE BRG, BSEL5
6594 025426 061227                       ;MOVE BRG, BSEL6
6595 025430 123000                       ;MOVE BRG, BSEL7
6596 025432 101410                       ;MOVE BSEL0, SPO
6597                                     ;BRANCH BACK ONE UNTIL <>377
6598 025434 000400                       400

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6599	025436	061220		61220		:MOVE BRG,BSELO
6600	025440	061222		61222		:MOVE BRG,BSEL2
6601	025442	061223		61223		:MOVE BRG,BSEL3
6602	025444	061224		61224		:MOVE BRG,BSEL4
6603	025446	061225		61225		:MOVE BRG,BSEL5
6604	025450	061226		61226		:MOVE BRG,BSEL6
6605	025452	061227		61227		:MOVE BRG,BSEL7
6606	025454	123000		123000		:MOVE BSELO,SPO
6607	025456	104022		104022		:BRANCH BACK ONE LOCATION.
6608	025460	177777		177777		
6609						
6610	025462	012711	040000	MOV	#040000,(R1)	:INITIALIZE MCPU
6611	025466	012711	100000	MOV	#100000,(R1)	:START CPU.
6612						
6613	025472	012700	000062	MOV	#50.,R0	:THE CYCLE TIME ON THE M8206 IS
6614						:200NS. WE ARE ASKING THE MCPU TO
6615						:DO 8 INSTRUCTIONS. WE'LL DELAY
6616						:100 PDP11 INSTRUCTIONS
6617						:THIS REALLY SHOULD BE PLENTY OF TIME.
6618						
6619	025476	005300		20\$: DEC	R0	
6620	025500	001376		BNE	20\$	
6621						
6622	025502	005005		CLR	R5	:JUST FOR TYPEOUT.
6623	025504	012705	000377	MOV	#377,R5	:EXPECT 377
6624	025510	111104		MOVB	(R1),R4	:READ MCPU
6625	025512	120405		CMPB	R4,R5	:SEE IF OK.
6626	025514	001410		BEG	30\$	
6627						
6628	025516			ERROR	29	:ERROR! MCPU WAS TO WRITE ALL
6629	025522	104455		TRAP	C\$ERDF	
6630	025524	000035		.WORD	29	
6631	025526	005055		.WORD	EMO	
6632	025530	010350		.WORD	ERR29	
6633						:ONES INTO BSELO,BUT INSTEAD FAILED.
6634	025532			ESCAPE	TST	
6635	025532	104410		TRAP	C\$ESCAPE	
6636	025534	000304		.WORD	L10106-	
6637						
6638	025536	012705	177777	30\$: MOV	#177777,R5	:EXPECT ALL ONES
6639	025542	016104	000002	MOV	2(R1),R4	:RECIEVED
6640	025546	020405		CMP	R4,R5	:RECIEVE OK?
6641	025550	001410		BEG	40\$	
6642						
6643	025552			ERROR	29	:ERROR! MCPU WAS TO WRITE ALL ONES
6644	025556	104455		TRAP	C\$ERDF	
6645	025560	000035		.WORD	29	
6646	025562	005055		.WORD	EMO	
6647	025564	010350		.WORD	ERR29	
6648						:INTO BSEL 2&3
6649						
6650	025566			ESCAPE	TST	
6651	025566	104410		TRAP	C\$ESCAPE	
6652	025570	000250		.WORD	L10106-	
6653						
6654	025572	016104	000004	40\$: MOV	4(R1),R4	:READ BSEL 4&5

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6655	025576	020405				CMP	R4,R5			
6656	025600	001410				BEQ	50\$			;READ OK?
6657										
6658	025602					ERROR	29			
6659	025606	104455				TRAP	C\$ERDF			;ERROR! FAILED TO WRITE BSEL \$85
6660	025610	000035				.WORD	29			
6661	025612	005055				.WORD	EMO			
6662	025614	010350				.WORD	ERR29			
6663										; TO ALL ONES.
6664	025616					ESCAPE	TST			
6665	025616	104410				TRAP	C\$ESCAPE			
6666	025620	000220				.WORD	L10106-			
6667										
6668	025622	016104	000006		50\$:	MOV	6(R1),R4			;READ BSEL 687
6669	025626	020405				CMP	R4,R5			;READ OK?
6670	025630	001410				BEQ	60\$			
6671										
6672	025632					ERROR	29			
6673	025636	104455				TRAP	C\$ERDF			;ERROR! FAILED TO WRITE BSEL 687
6674	025640	000035				.WORD	29			
6675	025642	005055				.WORD	EMO			
6676	025644	010350				.WORD	ERR29			
6677										; TO ALL ONES.
6678	025646					ESCAPE	TST			
6679	025646	104410				TRAP	C\$ESCAPE			
6680	025650	000170				.WORD	L10106-			
6681	025652	105011			60\$:	CLRB	(R1)			;SIGNAL MCPU TO WRITE ALL ZEROS.
6682	025654	005005				CLR	R5			;EXPECT TO READ ALL ZEROS.
6683										
6684	025656	005034				CLR	R4			
6685	025660	111104				MOVB	(R1),R4			;READ BSELO
6686	025662	001410				BEQ	70\$			;EXPECT ZERO.
6687										
6688	025664					ERROR	29			;MCPU FAILED TO CLEAR BSELO
6689	025670	104455				TRAP	C\$ERDF			
6690	025672	000035				.WORD	29			
6691	025674	005055				.WORD	EMO			
6692	025676	010350				.WORD	ERR29			
6693										
6694	025700					ESCAPE	TST			
6695	025700	104410				TRAP	C\$ESCAPE			
6696	025702	000136				.WORD	L10106-			
6697	025704	016104	000002		70\$:	MOV	2(R1),R4			;READ BSEL 283
6698	025710	001410				BEQ	80\$			;IF ZERO,OK
6699										
6700	025712					ERROR	29			;MCPU FAILED TO CLEAR BSEL 283
6701	025716	104455				TRAP	C\$ERDF			
6702	025720	000035				.WORD	29			
6703	025722	005055				.WORD	EMO			
6704	025724	010350				.WORD	ERR29			
6705	025726					ESCAPE	TST			
6706	025726	104410				TRAP	C\$ESCAPE			
6707	025730	000110				.WORD	L10106-			
6708	025732				80\$:					
6709	025732	016104	000004			MOV	4(R1),R4			;READ BSEL 485
6710	025736	001410				BEQ	90\$			

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6711
6712 025740          ERROR 29          ;MCPU FAILED TO CLEAR BSEL 485
6713 025744 104455   TRAP  C$ERDF
6714 025746 000035   .WORD 29
6715 025750 005055   .WORD EMO
6716 025752 010350   .WORD ERR29
6717 025754          ESCAPE TST
6718 025754 104410   TRAP  C$ESCAPE
6719 025756 000062   .WORD L10106-.
6720 025760
6721 025760 016104 000006 90$: MOV 6(R1),R4          ;READ BSEL 687
6722 025764 001406   BEQ 95$
6723
6724 025766          ERROR 29          ;MCPU FAILED TO CLEAR BSEL 687
6725 025772 104455   TRAP  C$ERDF
6726 025774 000035   .WORD 29
6727 025776 005055   .WORD EMO
6728 026000 010350   .WORD ERR29
6729
6730 026002          95$: EXIT TST
6731 026002 104432   TRAP  C$EXIT
6732 026004 000034   .WORD L10106-.
6733
6734
6735
6736          ;LOADER  SUBROUTINE USED BY THIS TEST TO LOAD MICRO CODE INTO A M8206
6737          ;
6738
6739 026006 012711 002000  LOADER: MOV #2000,(R1)
6740
6741 026012 005000          CLR R0
6742
6743 026014 010061 000004 10$: MOV R0,4(R1)          ;SET ADDR.
6744 026020 005200          INC R0
6745 026022 011561 000006  MOV (R5),6(R1)          ;WRITE MICRO CODE.
6746 026026 022527 177777  CMP (R5)+,#177777      ;SEE IF TERM.
6747 026032 001370          BNE 10$
6748 026034 005011          CLR (R1)
6749 026036 000205          RTS R5
6750
6751 026040          ENDTST
6752 026040          L10106: TRAP C$ETST
6753 026040 104401
6754
6755 026042          BADHEAD
6756          ;***** TEST 37 *****
6757          ;
6758          ;*NEGATIVE ADDRESS TEST.
6759          ;* IN THIS TEST, WE'LL MAKE SURE THAT THE M8207
6760          ;* DOES NOT RESPOND TO AN ADDRESS THAT ISN'T ASSIGNED
6761          ;* TO IT
6762          ;*
6763 026042          BADHEAD
6764          ;***** TEST 37 *****
6765
6766 026042          BGN1ST

```

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6767 026042          137::
6768 026042
6769 026042 013701 002516      MYINT
6770                                MOV      KMCSR,R1          ;RECORD DEVICE ADDR.
6771 026046 012711 000641      MOV      #641,(R1)        ;PUT A DEFINITE PATTERN IN MCPU.
6772 026052 012737 026130 000004  MOV      #20$,@#4        ;SET UP FOR TRAPS FROM NON-EX.
6773 026060 005037 000006      CLR      @#6
6774 026064 012702 160000      MOV      #160000,R2      ;GET STARTING ADDRESS.
6775
6776 026070 022712 000641      10$:    CMP      =641,(R2)    ;SEE IF CONTENTS OF THE ADDRESS
6777                                ;POINTED TO BY R2 EQUALS THE CONTENTS
6778                                ;OF THE MCPU CSR
6779 026074 001420      BEQ      40$
6780
6781 026076 062702 000002      15$:    ADD      #2,R2          ;UPDATE ADDRESS.
6782 026102 020227 177700      CMP      R2,#17770C      ;DONE? ;80
6783 026106 001370      BNE      10$            ;NO-LOOP
6784
6785 026110 013737 002464 000004 17$:    MOV      SAVE4,@#4        ;RESTORE TRAP CATCHER
6786 026116 013737 002466 000006  MOV      SAVE6,@#6        ;FROM VALUES SAVED BY INIT SECTION
6787 026124      EXIT      TST          ;EXIT, ALL DONE
6788 026124 104432      TRAP    C$EXIT
6789 026126 000052      .WORD  L10107-.
6790
6791 026130 062706 000004      20$:    ADD      #4,SP          ;SAVE FPOM TRAP
6792 026134 000760      BR       15$            ;LOOP
6793
6794 026136      40$:    ;*OH NO, WE MAY HAVE A DUAL ADDRESS PROBLEM!
6795
6796 026136 012711 000174      MOV      #174,(R1)       ;WRITE NEW PATTERN IN MCPU CSR
6797 026142 022712 000174      CMP      #174,(R2)       ;DID NEW PATTERN SHOW UP IN ADDR?
6798 026146 001403      BEQ      60$
6799
6800 026150 012711 000641      50$:    MOV      #641,(R1)       ;PUT OLD PATTERN BACK IN MCPU CSR.
6801 026154 000750      BR       15$            ;LOOP
6802
6803 026156 020102 60$:    CMP      R1,R2          ;IS THIS THE MCPU ADDRESS?
6804 026160 001773      BEQ      50$            ;YES-NO ERROR
6805
6806 026162      ERROR  40              ;DUAL ADDRESS ERROR
6807 026166 104455      TRAP    C$ERDF
6808 026170 000050      .WORD  40
6809 026172 005055      .WORD  EMO
6810 026174 010636      .WORD  ERR40
6811 026176 000744      BR       17$
6812
6813 026200      L10107:  ENDTST
6814 026200
6815 026200 104401      TRAP    C$ETST
6816
6817 026202      BADHEAD
6818      ;***** TEST 38 *****
6819      ;
6820      ;*BYTE ADDRESSING TEST
6821      ;* HERE, WE'RE GOING TO MAKE SURE THAT WE CAN
6822      ;* WRITE INTO ONLY A HIGH OR LOW BYTE OF THE MCPU.

```

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```

6823
6824 026202
6825
6826
6827 026202
6828 026202
6829 026202
6830 026202 013701 002516
6831 026206 005061 000002
6832 026212 112761 177777 000002
6833
6834 026220 032761 177400 000002
6835 026226 001410
6836
6837 026230
6838 026234 104455
6839 026236 000051
6840 026240 005055
6841 026242 010702
6842 026244
6843 026244 104410
6844 026246 000040
6845
6846 026250 005051 000002
6847 026254 112761 177777 000003
6848 026262 032761 000377 000002
6849 026270 001406
6850
6851 026272
6852 026276 104455
6853 026300 000052
6854 026302 005055
6855 026304 010744
6856
6857
6858 026306
6859 026306
6860 026306
6861 026306 104401
6862
6863 026310
6864
6865
6866
6867
6868
6869
6870 026310
6871
6872
6873 026310
6874 026310
6875 026310
6876
6877 026320
6878 026320 104432

```

```

: *
BADHEAD
: ***** TEST 38 *****
:
T38::
BGNTST
MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
CLR 2(R1) ;CLEAR CSR
MOVB #-1,2(R1) ;WRITE ALL ONES INTO LOW BYTE
;OF CSR
BIT #177400,2(R1) ;SEE IF HIGH BYTE GOT WRITTEN
BEQ 10$
ERROR 41 ;HIGH BYTE GOT WRITTEN INTO ON A LOW BYTE
TRAP C$ERDF
.WORD 41
.WORD EMO
.WORD ERR41
ESCAPE TST ;OPERATION
TRAP C$ESCAPE
.WORD L10110-.
10$:
CLR 2(R1)
MOVB #-1,3(R1) ;WRITE INTO HIGH BYTE
BIT #377,2(R1) ;SEE IF LOW BYTE GOT WRITTEN
BEQ 20$
ERROR 42 ;LOW BYTE GOT WRITTEN INTO ON A
TRAP C$ERDF
.WORD 42
.WORD EMO
.WORD ERR42
;HIGH BYTE OPERATION.
20$:
L10110:
ENDTST
TRAP C$ETST
BADHEAD
: ***** TEST 39 *****
: *
: *IN THIS TEST WE'RE GOING TO MAKE SURE THAT THE PC
: *REG COUNTS UP PROPERLY. THE PC REG SHOULD INCREMENT
: *ONCE AFTER EACH INSTRUCTION.
: *
BADHEAD
: ***** TEST 39 *****
:
T39::
BGNTST
SKIP07 10$ ;ONLY DO IF M8207
;GOTO 10$ IF M8207
EXIT TST
TRAP C$EXIT

```

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```

6879 026322 000122          .WORD  L10111-.
6880
6881 026324          10$:  MYINT
6882 026324 013701 002516    MOV    KMCSR,R1          ;RECORD DEVICE ADDR.
6883 026330          MSTCLR
6884 026334          ROMCLK
6885 026334 004537 003044    JSR    R5,.ROMCLK      ;CLOCK INSTRUCTION
6886 026340 000400          400
6887 026342          ROMCLK
6888 026342 004537 003044    JSR    R5,.ROMCLK      ;CLOCK INSTRUCTION
6889 026346 061233          61233
6890 026350          SROMCLK
6891 026350 004537 003100    JSR    R5,.SROMCLK
6892 026354 100000          100000
6893 026356 012705 000001    MOV    #1,R5           ;START AT ZERO
6894
6895 026362          20$:  ROMCLK          ;READ PC HIGH REG.
6896 026362 004537 003044    JSR    R5,.ROMCLK      ;CLOCK INSTRUCTION
6897 026366 121265          121265
6898
6899 026370          ROMCLK          ;READ PC LOW REG.
6900 026370 004537 003044    JSR    R5,.ROMCLK      ;CLOCK INSTRUCTION
6901 026374 121244          121244
6902 026376 016104 000004    MOV    4(R1),R4        ;GET WHOLE PICTURE
6903 026402 042704 170000    BIC    #170000,R4
6904 026406 020405          CMP    R4,R5           ;INCREMENT OK?
6905 026410 001410          BEQ    30$
6906
6907 026412          ERROR  47          ;PC FAILED TO INCREMENT PROPERLY
6908 026416 104455          TRAP  C$ERDF
6909 026420 000057          .WORD  47
6910 026422 005055          .WORD  EMO
6911 026424 011264          .WORD  ERR47
6912
6913
6914 026426          ESCAPE  TST          ;SHOULD INCREMENT BY ONE
6915 026426 104410          TRAP  C$ESCAPE        ;FOR EACH INSTRUCTION.
6916 026430 000014          .WORD  L10111-.
6917
6918 026432 062705 000002    30$:  ADD    #2,R5          ;UPDATE EXPECTED ADDRESS BY 2.
6919 026436 020527 000777    CMP    R5,#777
6920 026442 001347          BNE    20$
6921
6922 026444          L10111:  ENDTST
6923 026444          TRAP  C$ETST
6924 026444 104401
6925
6926 026446          BADHEAD
6927          :***** TEST 40 *****
6928          :
6929          :*IN THIS TEST WE'LL MAKE SURE THAT 'BRANCH FIELD H' DOESN'T
6930          :*GET SUCH HIGH.
6931          :*FIRST WE'LL CLEAR THE PC HIGH REG. THEN WE'LL DO A BRANCH INSTR
6932          :*WITH BAB BITS 11&12 SET. IF PCR BITS 8&9 SET THEN WE'LL KNOW
6933          :*WE WERE SUCCESSFUL IF PCR BITS 8&9 FAIL TO SET, WE'LL KNOW
6934          :*THAT THE MUX SELECTED THE WRONG INPUT TO BE CLOCKED INTO THE PCR.

```



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6935
6936 026446
6937
6938
6939 026446
6940 026446
6941 026446
6942
6943 026456
6944 026456 104432
6945 026460 000062
6946
6947 026462
6948 026462 013701 002516
6949 026466
6950
6951 026472
6952 026472 004537 003044
6953 026476 114400
6954
6955 026500
6956 026500 004537 003044
6957 026504 121265
6958
6959 026506 116105 000005
6960 026512 112704 000003
6961 026516 042705 177774
6962 026522 020405
6963 026524 001406
6964
6965 026526
6966 026532 104455
6967 026534 000017
6968 026536 005055
6969 026540 010006
6970
6971
6972 026542
6973 026542
6974 026542
6975 026542 104401
6976
6977 026544
6978
6979
6980
6981
6982
6983
6984
6985
6986
6987 026544
6988
6989
6990 026544

;*
BADHEAD
:***** TEST 40 *****
BGNTST
T40:: SKIP07 10$ ;ONLY DO IF M8207
;GOTO 10$ IF M8207
EXIT TST
TRAP CSEX!T
.WORD L10112-.
10$: MYINT ;INITIALIZE PARAMETERS
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
MSTCLR ;CLEAR DEVICE.
ROMCLK ;DO A 'BRANCH ALWAYS' WITH
JSR R5,ROMCLK ;CLOCK INSTRUCTION
114400 ;BAB BITS 11&12 SET THIS SHOULD CLOCK
;THESE BITS INTO BITS 8&9 OF THE PCR.
ROMCLK ;NOW READ THE PCR HIGH
JSR R5,ROMCLK ;CLOCK INSTRUCTION
121265 ;AND PUT INTO PORTS.
;REG. BR NO CLK OF BAB BITS
;READ THE PCR.
MOV# 5(R1),R5 ;EXPECT BITS 8,9 TO BE SET.
MOV# 3,R4 ;STRIP ANY JUNK
BIC #177774,R5 ;OK?
CMP R4,R5
BEQ 20$
ERROR 15 ;'BRANCH FIELD H' STUCK HIGH OR
TRAP C$ERDF
.WORD 15
.WORD EMO
.WORD ERR15
;OTHER PROBLEM IN THIS AREA.
20$:
L10112: ENDTST
TRAP C$ETST
BADHEAD
:***** TEST 41 *****
;*
;IN THIS TEST WE'RE GOING TO MAKE SURE THAT ONLY SPO
;IS SELECTED FOR SOURCE WHEN THE DESTINATION
;IS THE OUTBUS
;FIRST WE'LL WRITE EACH SP ADDR$ INTO ITSELF THEN WE'LL
;MOV SP TO OBUS4. THAT SHOULD SELECT
;SP ADDRESS 0. IF ANY OTHER DATA SHOWS UP, WE'LL
;BLAME IT ON THE SELECTION OF A DIFFERENT SCRATCH PAD.
BADHEAD
:***** TEST 41 *****
BGN!ST

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VRG0182

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6991 026544
6992 026544
6993 026544 013701 002516
6994 026550 005005
6995
6996 026552 042737 000017 026574 10$: BIC #17,20$ ;STRIP SP ADDR FIELD FROM INSTR
6997 026560 010551 000004 ;MOV R5,4(R1) ;PUT SP ADDR INTO PORT4.
6998 026564 050537 026574 ;BIS R5,20$ ;ADD SP ADDR TO INSTR.
6999 026570
7000 026570 004537 003044 ;ROMCLK ;CLOCK INSTRUCTION
7001 026574 123100 20$: JSR R5,.ROMCLK ;WRITE TO SP
7002 026576 005205 ;INC R5 ;UPDATE ADDRESS
7003 026600 120527 000020 ;CMPB R5,#20 ;IF NOT THROUGH, REPEAT.
7004 026604 001362 ;BNE 10$
7005
7006 026606
7007 026606 004537 003044 ;ROMCLK ;NOW MOV SPO TO OBUS* PORT4
7008 026612 061204 ;JSR R5,.ROMCLK ;CLOCK INSTRUCTION
7009 026614 116104 000004 ;MOV#B 4(R1),R4 ;READ PORT4 IT S/B ZERO
7010 026620 001410 ;BEQ 30$
7011 026622 012705 000000 ;MOV #0,R5
7012 026626 ;ERROR 43 ;SPO NOT SELECTED FOR SOURCE-SEE
7013 026632 104455 ;TRAP C$ERDF
7014 026634 000053 ;.WORD 43
7015 026636 005055 ;.WORD EMO
7016 026640 011006 ;.WORD ERR43
7017
7018 ;DISCUSSION IN HEADER.
7019 026642
7020 026642
7021 026642 104401 30$: ENDTST
7022 ;L10113: TPAP C$ETST
7023 026644
7024 ;BADHEAD
7025 ;***** TEST 42 *****
7026 ;*
7027 ;*IN THIS TEST WE ARE GOING TO MAKE SURE THAT THE
7028 ;*SIGNAL 'MOV INST H' (AND ITS ASSOC. TRIBS) DOESN'T GET
7029 ;*STUCK HIGH. IN ORDER TO DO THIS WE'LL CLEAR THE PC HIGH REG
7030 ;*PUT KNOWN DATA IN THE BREG AND SP1 THEN WE'LL A BRANCH
7031 ;*WITH CROM BITS 0-3 SET AS WELL AS CROM BIT 9 WITH CROM BITS 8 AND 11 CLEAR.
7032 ;*IF 'MOV INST H' GETS STUCK HIGH, THE PC REG HIGH WILL GET LOADED
7033 ;*WITH THE CONTENTS OF THE ALU
7034 ;BADHEAD
7035 ;***** TEST 42 *****
7036 026644
7037 026644
7038 026644 142$: BGNTST
7039 ;SKIP07 10$ ;ONLY DO IF M8207
7040 026654 ;GOTO 10$ IF M8207
7041 026654 104432 ;EXIT TST ;ELSE EXIT
7042 026656 000110 ;TRAP C$EXIT
7043 ;.WORD L10114-.
7044 026660 10$: MYINT ;DO INITIAL TEST SET-UP.
7045 026660 013701 002516 ;MOV KMCSR,R1 ;RECORD DEVICE ADDR.
7046 026664 ;MSTCLR ;DO A MASTER CLEAR.
    
```

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7047 026670 005737 002470          TST      RUNB
7048 026674 001034          BNE      20$
7049
7050          :TO RUN THIS SECTION OF CODE YOU MUST TURN SW7 OF SWITCH PACK #E28
7051          :OFF SO THAT M8207 NOT SELFSTARTING.
7052
7053 026676 012761 000002 000004    MOV      #2,4(R1)          :PUT A 2 INTO SP1
7054 026704          ROMCLK          :PORT4 TO SCRATCH PAD 1
7055 026704 004537 003044          JSR      R5,,ROMCLK       :CLOCK INSTRUCTION
7056 026710 123101          123101
7057 026712 012761 000004 000004    MOV      #4,4(R1)
7058 026720          ROMCLK
7059 026720 004537 003044          JSR      R5,,ROMCLK       :CLOCK INSTRUCTION
7060 026724 123100          123100
7061 026726          ROMCLK          :NOW DO A BRANCH ON C-BIT SET
7062 026726 004537 003044          JSR      R5,,ROMCLK       :CLOCK INSTRUCTION
7063 026732 141201          141201          :BASED ON SP CONTENTS
7064          :OK-WHAT WE ARE REALLY
7065          :INTERESTED IN IS SEEING IF THE
7066          :PC HIGH REG GETS LOADED WITH
7067          :THE CONTENTS OF THE ALU (2)
7068          :IF THIS OCCURS, WE CAN PROBABLY
7069          :SAY THAT 'MOV INSTR' REMAINED
7070          :HIGH.
7071 026734          ROMCLK          :READ PC HIGH, PUT INTO PORTS
7072 026734 004537 003044          JSR      R5,,ROMCLK       :CLOCK INSTRUCTION
7073 026740 121265          121265
7074 026742 116104 000005          MOV      5(R1),R4        :READ PC REG HIGH FROM PORT
7075 026746 001407          BEQ      20$             :SHOULD BE CLEAR
7076 026750 005005          CLR      R5
7077
7078 026752          ERROR      15          :ERROR-PC REG HIGH S/B CLEAR-SEE HEADER
7079 026756 104455          TRAP     C$ERDF
7080 026760 000017          .WORD   15
7081 026762 005055          .WORD   EMO
7082 026764 010006          .WORD   ERR15
7083
7084          :DISCUSSION.
7085 026766          20$:
7086 026766          L10114:
7087 026766          ENDTST
7088 026766 104401          TRAP     C$ETST
7089
7090 026770          BADHEAD
7091          :***** TEST 43 *****
7092          :*TEST THAT MASTER CLEAR, CLEARS BITS IN THE NPR CONTROL REGISTER AND
7093          :*MICROPROCESSOR MISCELLANEOUS REGISTER-FIRST WE'LL SET THE
7094          :*PRIORITY UP SO THAT WHEN WE SET THE BUS REQUEST BIT THAT IT WON'T BUG US
7095          :*THEN WE'LL SET ALL THE BITS IN BOTH REGS EXCEPT THE
7096          :*NPR REQUEST. WE'LL LOOK TO SEE THAT ALL GOT SET, NEXT
7097          :*WE'LL DO A MASTER CLEAR AND BE SURE THAT THEY ALL
7098          :*CLEAR.
7099 026770          BADHEAD
7100          :***** TEST 43 *****
7101
7102 026770          BGN1ST

```

CZDMQEO M8207 STATIC DIAG #2  
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HARDWARE TESTS

```

7103 026770
7104 026770
7105 026770 013701 002516
7106 026774
7107 027000
7108 027000 012700 000340
7109 027004 104441
7110 027006 012761 177777 003004
7111 027014 042761 000002 000004
7112 027022
7113 027022 004537 003044
7114 027026 121111
7115 027030 042761 000400 000004
7116 027036
7117 027036 004537 003044
7118 027042 121130
7119 027044
7120 027044 004537 003044
7121 027050 121225
7122
7123 027052
7124 027052 004537 003044
7125 027056 121204
7126 027060 012737 146636 002452
7127 027066 016104 000004
7128 027072 042704 030140
7129 027076 023704 002452
7130 027102 001410
7131 027104
7132 027104 104433
7133 027106
7134 027112 104455
7135 027114 000056
7136 027116 005055
7137 027120 011214
7138
7139 027122
7140 027122 104406
7141
7142 027124 152761 000100 000001 10$:
7143 027132 142761 000300 000001
7144
7145 027140
7146 027140 004537 003044
7147 027144 121225
7148
7149 027146
7150 027146 004537 003044
7151 027152 121204
7152 027154 016104 000004
7153 027160 005037 002452
7154 027164 042704 010140
7155 027170 001407
7156
7157 027172
7158 027176 104455

```

T43::

```

MYINT
MOV KMCSR,R1 ;RECORD DEVICE ADDR.
MSTCLR
SETPRI #PRI07 ;DON'T ALLOW INTERRUPTS.
MOV #PRI07,R0
TRAP C$SPRI
MOV #-1,4(R1) ;DATA TO BE SET
BIC #2,4(R1) ;DON'T SET AC LOW!
ROMCLK
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121111 ;PUT INTO MISC REG.
BI #400,4(R1) ;DON'T SET NPR BIT
ROMCLK
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121130 ;PUT INTO NPR REG
ROMCLK
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121225 ;MOV MISC REG (11) TO PORT5
ROMCLK
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121204 ;MOVE NPR REG (10) TO PORT4
MOV #146636,$GDDAT ;EXPECT ALL TO SET
MOV 4(R1),R4 ;READ WHAT HAPPEN
BIC #030140,R4 ;MASK UNUSED BITS
CMP $GDDAT,R4 ;DID ALL BITS GET SET?
BEQ 10$ ;YES CONTINUE.
BRESET
TRAP C$RESET
ERROR 46 ;SO SORT OF PROBLEM SETTING BITS
TRAP C$ERDF
.WORD 46
.WORD EMO
.WORD ERR46
;IN THE NPR AND/OR MISC REG.
CKLOOP
TRAP C$CLP1
BISB #100,1(R1) ;SET MASTER CLEAR
BICB #300,1(R1) ;CLEAR MASTER CLEAR
ROMCLK
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121225 ;MOV MISC REG (11) TO PORT5
ROMCLK
JSR R5,.ROMCLK ;CLOCK INSTRUCTION
121204 ;MOV NPR REG (10) TO PORT4
MOV 4(R1),R4 ;READ RESULTS
CLR $GDDAT ;EXPECT ZERO
BIC #010140,R4 ;MASK UNUSED BITS
BEQ 20$ ;IF ALL ZERO, EVERYTHING COOL.
ERROR 46 ;MASTER CLEAR FAILED TO CLEAR
TRAP C$ERDF

```

CZDMQEO MB207 STATIC DIAG #2 MACY11 30A(1052) 18-OCT-82 15:30 PAGE 165  
 CZDMQE.P11 30-SEP-82 15:35 HARDWARE TESTS

```

7159 027200 000056 .WORD 46
7160 027202 005055 .WORD EMO
7161 027204 011214 .WORD ERR46
7162 ;SOME BITS IN THE NPR AND/OR MISC REGS.
7163 027206 CKLOOP
7164 027206 104406 TRAP C$CLP1
7165
7166 027210 20$:
7167 027210 012761 000014 000004 MOV #14,4(R1) ;NOW WE ARE GOING TO TRY TO
7168 027216 027216 004537 003044 ROMCLK #14,4(R1) ;SET THE EXT BITS (16&17) IN THE NPR REG.
7169 027216 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
7170 027222 121110 121110 ROMCLK ;IF MASTER CLEAR FAILED TO CLEAR ITSELF
7171 027224 004537 003044 JSR R5,.ROMCLK ;THEN WE WILL BE UNABLE TO SET
7172 027224 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
7173 027230 121205 121205 ROMCLK ;THESE BITS
7174 027232 116104 000005 MOVB 5(R1),R4 ;READ REG
7175 027236 042704 000140 BIC #140,R4 ;MASK UNUSED BITS
7176 027242 012737 000014 002452 MOV #14,$GDDAT ;STORE GOOD
7177 027250 023704 002452 CMP $GDDAT,R4 ;DID BITS SET?
7178 027254 001407 BEQ 30$ ;YES-CONTINUE
7179
7180 027256 ERROR 46 ;MASTER CLEAR FAILED TO CLEAR
7181 027262 104455 TRAP C$ERDF
7182 027264 000056 .WORD 46
7183 027266 005055 .WORD EMO
7184 027270 011214 .WORD ERR46
7185 ;ITSELF, THUS PROHIBITING US FROM
7186 ;FURTHER SETTING BITS IN THE NPR REG.
7187 027272 CKLOOP
7188 027272 104406 TRAP C$CLP1
7189
7190 027274 30$:
7191 027274 104433 BRESET ;NOW WE'LL SEE IF A BUS RESET CLEARS
7192 TRAP C$RESET ;THESE BITS.
7193 027276 005737 002470 TST RUNB ;CAN'T DO THIS
7194 027302 001016 BNE 40$ ;TEST IF RUN SW SET.
7195 027304 ROMCLK
7196 027304 004537 003044 JSR R5,.ROMCLK ;CLOCK INSTRUCTION
7197 027310 121204 121204 ROMCLK ;READ MISC REG
7198 027312 116104 000004 MOVB 4(R1),R4
7199 027316 001410 BEQ 40$ ;IF ZERO-END TST
7200
7201 027320 005037 002452 CLR $GDDAT ;S/B ZERO
7202
7203 027324 ERROR 46 ;BUS RESET FAILED TO CLEAR NPR REG
7204 027330 104455 TRAP C$ERDF
7205 027332 000056 .WORD 46
7206 027334 005055 .WORD EMO
7207 027336 011214 .WORD ERR46
7208 ;MASTER CLEAR WAS ABLE TO LOOK TO THE
7209 ;CIRCUITRY THAT CONVERTS BUS INIT
7210 ;TO "CLEAR"
7211
7212 027340 40$:
7213 027340 ENDTST
7214 027340 L10115:
    
```

J 13

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SEQ 165

7215 027340 104401

TRAP C\$ETST

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HARDWARE PARAMETER CODING SECTION

.SBTTL HARDWARE PARAMETER CODING SECTION

7216  
7217  
7218  
7219  
7220  
7221  
7222  
7223  
7224  
7225  
7226  
7227  
7228  
7229 027342  
7230 027342 000016  
7231 027344  
7232  
7233 027344  
7234 027344 000032  
7235 027346 027400  
7236 027350 000007  
7237 027352 000000  
7238 027354 000007  
7239 027356  
7240 027356 001031  
7241 027360 027452  
7242 027362 160000  
7243 027364 177776  
7244  
7245  
7246  
7247  
7248  
7249  
7250 027366  
7251 027366 012032  
7252 027370 030050  
7253 027372 000007  
7254 027374 000000  
7255 027376 000001  
7256 027400  
7257  
7258 027400  
7259  
7260 027400 044127 041511 020110  
7261 027406 044515 051103 026517  
7262 027414 050103 037525 024040  
7263 027422 036460 034115 030062  
7264 027430 026060 036464 034115  
7265 027436 030062 026064 036467  
7266 027444 034115 030062 000067  
7267 027452 044515 051103 026517  
7268 027460 050103 020125 041440  
7269 027466 051123 040440 042104  
7270 027474 042522 051523 035040  
7271 027502 000040

:/ THE HARDWARE PARAMETER CODING SECTION CONTAINS MACROS  
:/ THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES. THE  
:/ MACROS ARE NOT EXECUTED AS MACHINE INSTRUCTIONS BUT ARE  
:/ INTERPRETED BY THE SUPERVISOR AS DATA STRUCTURES. THE  
:/ MACROS ALLOW THE SUPERVISOR TO ESTABLISH COMMUNICATIONS  
:/ WITH THE OPERATOR.

BGNHRD  
.WORD L10116-L\$HARD/2  
L\$HARD::  
GPRMD WPM,0,0,7,0,7,YES  
.WORD T\$CODE  
.WORD WPM  
.WORD 7  
.WORD T\$LLOLIM  
.WORD T\$HILIM  
GPRMA ADDRES,2,0,160000,177776,YES  
.WORD T\$CODE  
.WORD ADDRES  
.WORD T\$LLOLIM  
.WORD T\$HILIM  
GPRMA VECTOR,4,0,0,674,YES  
GPRMD PRIRTY,6,0,7000,4,7,YES  
GPRMD LNUNIT,10,0,3,0,3,YES  
GPRMD SWPAC1,12,0,377,0,377,YES  
GPRMD SWPAC2,14,0,377,0,377,YES  
GPRMD LOOPBK,16,0,40000,0,1,YES  
GPRMD ISRUN,24,0,7,0,1,YES  
.WORD T\$CODE  
.WORD ISRUN  
.WORD 7  
.WORD T\$LLOLIM  
.WORD T\$HILIM  
ENDHRD  
.EVEN  
L10116:  
WPM: .ASCIZ 'WHICH MICRO-CPU? (0=M8200,4=M8204,7=M8207'  
ADDRES: .ASCIZ /MICRO-CPU CSR ADDRESS : /

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HARDWARE PARAMETER CODING SECTION

7272	027504	044515	051103	026517	VECTOR: .ASCIZ /MICRO-CPU VECTOR ADDRESS : /
7273	027512	050103	020125	042526	
7274	027520	052103	051117	040440	
7275	027526	042104	042522	051523	
7276	027534	035040	000040		
7277	027540	044515	051103	026517	PRIRTY: .ASCIZ /MICRO-CPU PRIORITY LEVEL : /
7278	027546	050103	020125	051120	
7279	027554	047511	044522	054524	
7280	027562	046040	053105	046105	
7281	027570	035040	000040		
7282	027574	044127	041511	020110	LNUNIT: .ASCIZ /WHICH LINE UNIT (0-3)? 0=NONE,1=M8201,2=M8202,3=M8203 : /
7283	027602	044514	042516	052440	
7284	027610	044516	020124	030050	
7285	027616	031455	037451	030040	
7286	027624	047075	047117	026105	
7287	027632	036461	034115	030062	
7288	027640	026061	036462	034115	
7289	027646	030062	026062	036463	
7290	027654	034115	030062	020063	
7291	027662	020072	000		
7292	027665	123	044527	041524	SWPAC1: .ASCIZ /SWITCH PACK #1 (DDCMP LINE #) : /
7293	027672	020110	040520	045503	
7294	027700	021440	020061	042050	
7295	027706	041504	050115	046040	
7296	027714	047111	020105	024443	
7297	027722	035040	000040		
7298	027726	053523	052111	044103	SWPAC2: .ASCIZ /SWITCH PACK #2 (BM873 BOOT ADR) : /
7299	027734	050040	041501	020113	
7300	027742	031043	024040	046502	
7301	027750	033470	020063	047502	
7302	027756	052117	040440	051104	
7303	027764	020051	020072	000	
7304	027771	127	046111	020114	LOOPBK: .ASCIZ /WILL TEST CONNECTOR(S) BE USED ? 0=NO,1=YES : /
7305	027776	042524	052123	041440	
7306	030004	047117	042516	052103	
7307	030012	051117	051450	020051	
7308	030020	042502	052440	042523	
7309	030026	020104	020077	036460	
7310	030034	047516	030454	054475	
7311	030042	051505	035040	000040	
7312	030050	044515	051103	026517	ISRUN: .ASCIZ 'MICRO-PROCESSOR RUN SWITCH TYPE 0 IF OFF, 1 IF ON :'
7313	030056	051120	041517	051505	
7314	030064	047523	020122	052522	
7315	030072	020116	053523	052111	
7316	030100	044103	020040	054524	
7317	030106	042520	030040	044440	
7318	030114	020106	043117	026106	
7319	030122	030440	044440	020106	
7320	030130	047117	035040	000	
7321					
7322		030136			.EVEN
7323					
7324					
7325					
7326					
7327					



CZDMQEO M8207 STATIC DIAG #2  
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HARDWARE PARAMETER CODING SECTION

7328

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SOFTWARE PARAMETER CODING SECTION

.SBTTL SOFTWARE PARAMETER CODING SECTION

:/ THE SOFTWARE PARAMETER CODING SECTION CONTAINS MACROS  
:/ THAT ARE USED BY THE SUPERVISOR TO BUILD P-TABLES. THE  
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:/ WITH THE OPERATOR.

7329  
7330  
7331  
7332  
7333  
7334  
7335  
7336  
7337  
7338  
7339  
7340  
7341 030136  
7342 030136 000000  
7343 030140  
7344  
7345  
7346 030140  
7347  
7348 030140  
7349  
7350  
7351  
7352  
7353  
7354  
7355  
7356  
7357 030140  
7358  
7359 030140 000000  
7360 030142 000000  
7361 030144  
7362  
7363 000001

BGNSFT  
.WORD L10117-L\$SOFT/2  
L\$SOFT::  
  
ENDSFT  
.EVEN  
L10117:  
  
.EVEN  
  
LASTAD  
.EVEN  
.WORD 0  
.WORD 0  
L\$LAST::  
  
.END







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 CZDMQE.P11 30-SEP-82 15:35 CROSS REFERENCE TABLE -- USER SYMBCLS

ERR15	010006	G	2704#	5648	5836	6969	7082												
ERR16	010134	G	2733#	5911	5930	5947	5985	6003	6020										
ERR17	010256	G	2763#	6133	6155	6198													
ERR2	006160	G	2392#	3537															
ERR29	010350	G	2784#	6336	6367	6632	6647	6662	6676	6692	6704	6716	6728						
ERR3	006306	G	2421#																
ERR35	010472	G	2812#	6168	6185														
ERR36	010614	G	2841#	3300															
ERR4	006434	G	2450#																
ERR40	010636	G	2853#	6810															
ERR41	010702	G	2871#	6841															
ERR42	010744	G	2888#	6855															
ERR43	011006	G	2906#	7016															
ERR44	011054	G	2925#	3891															
ERR45	011124	G	2944#	5731															
ERR46	011214	G	2969#	7137	7161	7184	7207												
ERR47	011264	G	2989#	6911															
ERR5	006556	G	2478#	4028	4052	4076	4127	4150	4173	4225	4250	4275	4327	4351	4375				
			4428	4452	4476	4529	4553	4577	4629	4653	4677	4729	4753	4777	4829				
			4855	4879	4931	4957	4981	5032	5058	5082	5133	5159	5183	5235	5261				
			5285	5336	5362	5386													
ERR6	006700	G	2506#	3597	3659	3721	3754	6415											
ERR7	007026	G	2535#	3936	3959	3978	6389	6487											
EVL =	000004	G	1559#																
ESEND =	002100		1250#																
ESLOAD =	000035		1250#	1350															
FADR	002412		1630#	2719	5599*	5682*	5787*	5870*											
FLAG	002436		1628#	2519	3567*	3571	3572	3607*	3608	3628*	3633	3634	3669*	3670	3691*				
			3692	3695	3696	3725*	3726	3729*	3730	3733	3760*	3761	5592*	5604	5683*				
			5780*	5792	5871*														
FM1	005046		2199#	2365	2371	2394	2400	2423	2429	2452	2458	2480	2486	2508	2514				
			2537	2543	2566	2572	2594	2600	2622	2628	2650	2656	2678	2684	2706				
			2712	2735	2741	2765	2771	2786	2792	2814	2820								
F TIME	002462		1650#	3047	3051*														
F\$AU =	000015		1250#	3255	3257														
F\$AUTO =	000020		1250#	3182	3203														
F\$BGN =	000040		1250#	1256	1370	2363	2392	2421	2450	2478	2506	2535	2564	2592	2620				
			2648	2676	2704	2733	2763	2784	2812	2841	2853	2871	2888	2906	2925				
			2944	2969	2989	3017	3023	3041	3182	3214	3234	3255	3280	3288	3305				
			3309	3323	3351	3372	3383	3386	3395	3409	3422	3433	3436	3445	3460				
			3474	3486	3489	3497	3516	3522	3539	3550	3562	3599	3612	3623	3661				
			3674	3686	3723	3756	3765	3777	3780	3849	3894	3907	3910	3938	3981				
			3998	4002	4010	4030	4036	4054	4060	4078	4084	4101	4104	4112	4129				
			4135	4152	4158	4175	4181	4198	4201	4209	4228	4234	4253	4259	4277				
			4283	4300	4303	4311	4329	4335	4353	4359	4377	4383	4400	4403	4412				
			4430	4436	4454	4460	4478	4484	4501	4504	4513	4531	4537	4555	4561				
			4579	4585	4602	4605	4613	4631	4637	4655	4661	4679	4685	4702	4705				
			4713	4731	4737	4755	4761	4779	4785	4802	4805	4812	4831	4837	4857				
			4863	4881	4887	4904	4907	4914	4933	4939	4959	4965	4983	4989	5006				
			5009	5016	5034	5040	5060	5066	5084	5090	5107	5110	5117	5135	5141				
			5161	5167	5185	5191	5209	5212	5219	5237	5243	5263	5269	5287	5293				
			5310	5313	5320	5338	5344	5364	5370	5388	5394	5409	5412	5465	5472				
			5490	5493	5535	5544	5583	5588	5620	5735	5771	5776	5868	5877	5890				
			5893	5914	5933	5950	5964	5967	5988	6006	6023	6035	6096	6111	6173				
			6206	6221	6338	6391	6417	6423	6435	6449	6491	6504	6508	6546	6552				
			6560	6574	6579	6635	6651	6665	6679	6695	6706	6718	6731	6752	6767				



CZDMQEO MB207 STATIC DIAG #2 MACY11 30A(1052) 18-OCT-82 15:30 PAGE 177  
CZDMQE.P11 30-SEP-82 15:35 CRCSS REFERENCE TABLE -- USER SYMBOLS

FSTEST= 000001	1250#	3281	3309	3324	3372	3384	3422	3434	3474	3487	3550	3563	3612
	3624	3674	3687	3765	3778	3894	3908	3981	3999	4084	4102	4181	4199
	4283	4301	4383	4401	4484	4502	4585	4603	4685	4703	4785	4803	4887
	4905	4989	5007	5090	5108	5191	5210	5293	5311	5394	5410	5472	5491
	5544	5584	5735	5772	5877	5891	5950	5965	6023	6036	6096	6112	6206
	6222	6435	6450	6491	6505	6560	6575	6752	6768	6814	6829	6860	6875
	6923	6941	6974	6992	7020	7038	7087	7104	7214				
	3078	3087#	3096										
GETPRM 011462	1250#												
GSCNTO= 000200	1250#												
GSDLM= 000372	1250#												
GSDISP= 000003	1250#												
GSEXCP= 000400	1250#												
GSMLI= 000002	1250#												
GSLOLI= 000001	1250#												
GSNO = 000000	1250#												
GSOFFS= 000400	1250#	7234	7240	7251									
GSOFSI= 000376	1250#	7234	7240	7251									
GSPRMA= 000001	1250#	7240											
GSPRMD= 000002	1250#	7234	7251										
GSPRML= 000000	1250#												
GSRADA= 000140	1250#												
GSRADB= 000000	1250#												
GSRADD= 000040	1250#												
GSRADL= 000120	1250#												
GSRADO= 000020	1250#	7234	7240	7251									
GSXFER= 000004	1250#												
GSYES = 000010	1250#	7234	7240	7251									
HELP = 000000	1241#	1280	1369	1430	1739	3019	3024						
HUL = 100000 G	1572#												
IBE = 010000 G	1569#												
IDU = 000040 G	1562#												
IER = 020000 G	1570#												
INIFLG 002474	1659#												
INSTU 003616	2044	2055#											
ISR = 000100 G	1563#												
ISRUN 030050	7252	7312#											
IXE = 004000 G	1568#												
ISAU = 000041	1250#	3255#	3259#										
ISAUTO= 000041	1250#	3182#	3205#										
ISCLN = 000041	1250#	3214#	3221#										
ISDU = 000041	1250#	3234#	3241#										
ISHRD = 000041	7230#	7259#											
ISINIT= 000041	1250#	3041#	3179#										
ISMOD = 000040	1250#	1256#											
ISMSG = 000041	1250#	2363#	2391#	2392#	2420#	2421#	2449#	2450#	2477#	2478#	2505#	2506#	2534#
	2535#	2563#	2564#	2591#	2592#	2619#	2670#	2647#	2648#	2675#	2676#	2703#	2704#
	2732#	2733#	2760#	2763#	2783#	2784#	2811#	2812#	2839#	2841#	2851#	2853#	2870#
	2871#	2881#	2888#	2904#	2906#	2924#	2925#	2943#	2944#	2968#	2969#	2987#	2989#
	3007#												
ISPROT= 000040	1250#	1370#											
ISP*AB= 000041	1250#												
ISPR = 000041	1250#												
ISRPT = 000041	1250#	3017#	3028#										
ISSEG = 000041	1250#	3280	3323	3383	3395#	3409	3414#	3433	3445#	3460	3465#	3486	3497#
	3516	3521#	3522#	3539	3544#	3562	3623	3686	3777	3907	3998	4010#	4030
	4035#	4036#	4054	4057#	4060#	4078	4083#	4101	4112#	4129	4134#	4135#	4152





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CRCSS REFERENCE TABLE -- USER SYMBOLS

LSACP	002110	G	1357#		
LSAPT	002036	G	1315#		
LSAU	012144	G	1342	3255#	
LSAUT	002070	G	1341#		
LSAUTO	012042	G	1358	3182#	
LSCCP	002106	G	1355#		
LSCLEA	012134	G	1356	3214#	
LSCO	002032	G	1311#		
LSDEPO	002011	G	1293#		
LSDESC	002312	G	1348	1594#	
LSDESP	002076	G	1347#		
LSDEVP	002060	G	1333#		
LSDISP	002132	G	1318	1385#	
LSDLY	002116	G	1363#		
LSDTP	002040	G	1317#		
LSDTYP	002034	G	1313#		
LSDU	012140	G	1344	3234#	
LSDUT	002072	G	1343#		
LSDVTY	002730	G	1334	1727#	
LSEF	002052	G	1328#		
LSENV1	002044	G	1321#		
LSETP	002102	G	1351#		
LSEXP1	002046	G	1323#		
LSEXP4	002064	G	1337#		
LSEXP5	002066	G	1339#		
LSHARD	027344	G	1300	7230	7231#
LSHIME	002120	G	1365#		
LSHPCP	002016	G	1299#		
LSHPTP	002022	G	1303#		
LSHW	002262	G	1304	1445	1446#
LSICP	002104	G	1353#		
LSINIT	011340	G	1354	3041#	
LSLADP	002026	G	1307#		
LSLAST	030144	G	1308	7361#	
LSLOAD	002100	G	1349#		
LSLUN	002074	G	1345#		
LSMREV	002050	G	1325#		
LSNAME	002000	G	1282#		
LSPRIO	002042	G	1319#		
LSPROT	002122	G	1360	1370#	
LSPRT	002112	G	1359#		
LSREPP	002062	G	1335#		
LSREV	002010	G	1291#		
LSRPT	011332	G	3017#		
LSOFT	030140	G	7342	7343#	
LSSPC	002056	G	1331#		
LSSPCP	002020	G	1301#		
LSPTP	002024	G	1305#		
LSSTA	002030	G	1309#		
LSW	002312	G	1472	1473#	
LSTEST	002114	G	1361#		
LSTIML	002014	G	1297#		
LSUNIT	002012	G	1295#	3089	
L10001	002310		1445	1463#	
L10002	002312		1472	1478#	
L10003	006156		2389#		

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CROSS REFERENCE TABLE -- USER SYMBOLS

L10004	006304	2418#		
L10005	006432	2447#		
L10006	006554	2475#		
L10007	006676	2503#		
L10010	007024	2532#		
L10011	007152	2561#		
L10012	007274	2589#		
L10013	007416	2617#		
L10014	007540	2645#		
L10015	007662	2673#		
L10016	010004	2701#		
L10017	010132	2730#		
L10020	010254	2758#		
L10021	010346	2781#		
L10022	010470	2809#		
L10023	010612	2837#		
L10024	010634	2849#		
L10025	010700	2868#		
L10026	010742	2885#		
L10027	011004	2902#		
L10030	011052	2922#		
L10031	011122	2941#		
L10032	011212	2966#		
L10033	011262	2985#		
L10034	011330	3005#		
L10035	011336	3022	3026#	
L10036	012040	3177#		
L10037	012132	3203#		
L10040	012136	3219#		
L10041	012142	3239#		
L10042	012144	3257#		
L10043	012254	3289	3304	3309#
L10044	012420	3352	3372#	
L10045	012550	3387	3422#	
L10046	012710	3437	3474#	
L10047	013152	3490	3550#	
L10050	013354	3600	3612#	
L10051	013566	3662	3674#	
L10052	014110	3724	3757	3765#
L10053	014466	3781	3850	3894#
L10054	014734	3911	3939	3981#
L10055	015200	4003	4084#	
L10056	015430	4105	4181#	
L10057	015674	4202	4283#	
L10060	016140	4304	4383#	
L10061	016404	4404	4484#	
L10062	016650	4505	4585#	
L10063	017114	4606	4685#	
L10064	017360	4706	4785#	
L10065	017640	4806	4887#	
L10066	020120	4908	4989#	
L10067	020374	5010	5090#	
L10070	020650	5111	5191#	
L10071	021126	5213	5293#	
L10072	021402	5314	5394#	
L10073	021574	5413	5466	5472#



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		4420	4444	4468	4521	4545	4569	4621	4645	4669	4721	4745	4769	4821
		4847	4871	4923	4949	4973	5024	5050	5074	5125	5151	5175	5227	5253
		5277	5328	5354	5378									
REGADR	002530	1703#												
RETADR	002352	1614#												
ROMMAP	012146	2012	3270#	6514	6528									
RUN	002410	1629#												
RUNB	002470	1653#	3173*	3862	5693	6160	7047	7193						
RUNINH	002472	1654#	3124*	3173	3864	5695								
SAVACT	002402	1626#												
SAVE4	002464	1651#	3049*	3052	3200	3302	6785							
SAVE6	002466	1652#	3050*	3053	3201	3303	6786							
SAVNUM	002404	1627#												
SAVPC	002366	1620#												
SAVSP	002364	1619#												
SETBRO	003220	1918#	4413	4437	4461									
SETBR1	003230	1925#	4514	4538	4562									
SETBR4	003240	1933#	4614	4638	4662									
SETBR7	003250	1941#	4714	4738	4762									
SETC	003260	1949#	4210	4235	4260	4813	5990							
SETZ	003312	1966#	4312	4336	4360	4915	5916							
SFPTBL	002312	1474#												
SSTACK	002730	1707#	3044											
STAT	002356	1616#												
STAT1	002500	1684#	3125*	3127*	3131*	3142*	3146*	3149*						
STAT2	002502	1685#	3152*	3154*										
STAT3	002504	1686#												
STM	005627	2276#	2384	2413	2442	2470	2498	2527	2556	2584	2612	2640	2668	2696
		2725	2753	2776	2804	2832	2843	2862	2879	2896	2916	2935	2960	2979
		2999												
STRTSW	002354	1615#												
SUBRPC	002346	1612#												
SVCGBL=	000000	1250#	1256	1263#	1282	1283	1291	1292	1293	1294	1295	1296	1297	1298
		1299	1300	1301	1302	1303	1304	1305	1306	1307	1308	1309	1310	1311
		1312	1313	1314	1315	1316	1317	1318	1319	1320	1321	1322	1323	1324
		1325	1326	1328	1329	1331	1332	1333	1334	1335	1336	1337	1338	1339
		1340	1341	1342	1343	1344	1345	1346	1347	1348	1349	1350	1351	1352
		1353	1354	1355	1356	1357	1358	1359	1360	1361	1362	1363	1364	1365
		1366	1370	1371	1385	1386	1446	1447	1448	1473	1474	1475	1594	1595
		1727	1728	2363	2364	2392	2393	2421	2422	2450	2451	2478	2479	2506
		2507	2535	2536	2564	2565	2592	2593	2620	2621	2648	2649	2676	2677
		2704	2705	2733	2734	2763	2764	2784	2785	2812	2813	2841	2842	2853
		2854	2871	2872	2888	2889	2906	2907	2925	2926	2944	2945	2969	2970
		2989	2990	3017	3018	3041	3042	3182	3183	3214	3215	3234	3235	3255
		3256	7231	7232	7343	7344	7361#	7362						
SVCINS=	000000	1250#	1260#	1283	1284	1285	1286	1287	1288	1289	1290	1291	1292	1293
		1294	1295	1296	1297	1298	1299	1300	1301	1302	1303	1304	1305	1306
		1307	1308	1309	1310	1311	1312	1313	1314	1315	1316	1317	1318	1319
		1320	1321	1322	1323	1324	1325	1326	1327	1328	1329	1330	1331	1332
		1333	1334	1335	1336	1337	1338	1339	1340	1341	1342	1343	1344	1345
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		1359	1360	1361	1362	1363	1364	1365	1366	1367	1384	1385	1386	1387
		1388	1389	1390	1391	1392	1393	1394	1395	1396	1397	1398	1399	1400
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		1414	1415	1416	1417	1418	1419	1420	1421	1422	1423	1424	1425	1426
		1427	1428	1429	1445	1446	1472	1473	1595	1599	1600	172R	1732	1733

2364	2365	2366	2367	2368	2369	2370	2371	2372	2373	2374	2375	2376
2377	2378	2379	2380	2381	2382	2383	2384	2385	2386	2387	2388	2389
2390	2391	2393	2394	2395	2396	2397	2398	2399	2400	2401	2402	2403
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2498	2499	2500	2501	2502	2503	2504	2505	2507	2508	2509	2510	2511
2512	2513	2514	2515	2516	2517	2518	2519	2520	2521	2522	2523	2524
2525	2526	2527	2528	2529	2530	2531	2532	2533	2534	2536	2537	2538
2539	2540	2541	2542	2543	2544	2545	2546	2547	2548	2549	2550	2551
2552	2553	2554	2555	2556	2557	2558	2559	2560	2561	2562	2563	2565
2566	2567	2568	2569	2570	2571	2572	2573	2574	2575	2576	2577	2578
2579	2580	2581	2582	2583	2584	2585	2586	2587	2588	2589	2590	2591
2593	2594	2595	2596	2597	2598	2599	2600	2601	2602	2603	2604	2605
2606	2607	2608	2609	2610	2611	2612	2613	2614	2615	2616	2617	2618
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2646	2647	2649	2650	2651	2652	2653	2654	2655	2656	2657	2658	2659
2660	2661	2662	2663	2664	2665	2666	2667	2668	2669	2670	2671	2672
2673	2674	2675	2677	2678	2679	2680	2681	2682	2683	2684	2685	2686
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2714	2715	2716	2717	2718	2719	2720	2721	2722	2723	2724	2725	2726
2727	2728	2729	2730	2731	2732	2734	2735	2736	2737	2738	2739	2740
2741	2742	2743	2744	2745	2746	2747	2748	2749	2750	2751	2752	2753
2754	2755	2756	2757	2758	2759	2760	2764	2765	2766	2767	2768	2769
2770	2771	2772	2773	2774	2775	2776	2777	2778	2779	2780	2781	2782
2783	2785	2786	2787	2788	2789	2790	2791	2792	2793	2794	2795	2796
2797	2798	2799	2800	2801	2802	2803	2804	2805	2806	2807	2808	2809
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2837	2838	2839	2843	2844	2845	2846	2847	2848	2850	2851	2855	2856
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2873	2874	2875	2876	2877	2878	2879	2880	2881	2882	2883	2884	2886
2887	2890	2891	2892	2893	2894	2895	2896	2897	2898	2899	2900	2901
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2919	2920	2921	2923	2924	2927	2928	2929	2930	2931	2932	2933	2934
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2951	2952	2953	2954	2955	2956	2957	2958	2959	2960	2961	2962	2963
2964	2965	2967	2968	2971	2972	2973	2974	2975	2976	2977	2978	2979
2980	2981	2982	2983	2984	2986	2987	2991	2992	2993	2994	2995	2996
2997	2998	2999	3000	3001	3002	3003	3004	3006	3007	3021	3022	3023
3027	3028	3057	3058	3059	3060	3061	3063	3064	3065	3066	3067	3069
3070	3071	3072	3073	3075	3076	3077	3078	3079	3092	3093	3094	3095
3096	3097	3178	3179	3197	3198	3199	3204	3205	3216	3217	3220	3221
3237	3238	3240	3241	3258	3259	3288	3289	3290	3297	3298	3299	3300
3301	3305	3306	3307	3310	3311	3345	3346	3347	3348	3349	3351	3352
3353	3365	3366	3367	3368	3369	3373	3374	3386	3387	3388	3395	3396
3404	3405	3406	3407	3408	3409	3410	3411	3413	3414	3423	3424	3436
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3465	3475	3476	3489	3490	3491	3497	3498	3511	3512	3513	3514	3515
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CRSS REFERENCE TABLE -- USER SYMBOLS

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3668	3669	3675	3676	3718	3719	3720	3721	3722	3723	3724	3725	3751
3752	3753	3754	3755	3756	3757	3758	3759	3760	3766	3767	3780	3781
3782	3816	3817	3818	3819	3820	3841	3842	3843	3844	3845	3849	3850
3851	3852	3853	3888	3889	3890	3891	3892	3895	3896	3910	3911	3912
3933	3934	3935	3936	3937	3938	3939	3940	3956	3957	3958	3959	3960
3975	3976	3977	3978	3979	3982	3983	4002	4003	4004	4010	4011	4025
4026	4027	4028	4029	4030	4031	4032	4034	4035	4036	4037	4049	4050
4051	4052	4053	4054	4055	4056	4058	4059	4060	4061	4073	4074	4075
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4113	4124	4125	4126	4127	4128	4129	4130	4131	4133	4134	4135	4136
4147	4148	4149	4150	4151	4152	4153	4154	4156	4157	4158	4159	4170
4171	4172	4173	4174	4175	4176	4177	4179	4180	4182	4183	4201	4202
4203	4209	4210	4222	4223	4224	4225	4226	4228	4229	4230	4232	4233
4234	4235	4247	4248	4249	4250	4251	4253	4254	4255	4257	4258	4259
4260	4272	4273	4274	4275	4276	4277	4278	4279	4281	4282	4284	4285
4303	4304	4305	4311	4312	4324	4325	4326	4327	4328	4329	4330	4331
4333	4334	4335	4336	4348	4349	4350	4351	4352	4353	4354	4355	4357
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4384	4385	4403	4404	4405	4412	4413	4425	4426	4427	4428	4429	4430
4431	4432	4434	4435	4436	4437	4449	4450	4451	4452	4453	4454	4455
4456	4458	4459	4460	4461	4473	4474	4475	4476	4477	4478	4479	4480
4482	4483	4485	4486	4504	4505	4506	4513	4514	4526	4527	4528	4529
4530	4531	4532	4533	4535	4536	4537	4538	4550	4551	4552	4553	4554
4555	4556	4557	4559	4560	4561	4562	4574	4575	4576	4577	4578	4579
4580	4581	4583	4584	4586	4587	4605	4606	4607	4613	4614	4626	4627
4628	4629	4630	4631	4632	4633	4635	4636	4637	4638	4650	4651	4652
4653	4654	4655	4656	4657	4659	4660	4661	4662	4674	4675	4676	4677
4678	4679	4680	4681	4683	4684	4686	4687	4705	4706	4707	4713	4714
4726	4727	4728	4729	4730	4731	4732	4733	4735	4736	4737	4738	4750
4751	4752	4753	4754	4755	4756	4757	4759	4760	4761	4762	4774	4775
4776	4777	4778	4779	4780	4781	4783	4784	4786	4787	4805	4806	4807
4812	4813	4826	4827	4828	4829	4830	4831	4832	4833	4835	4836	4837
4838	4852	4853	4854	4855	4856	4857	4858	4859	4861	4862	4863	4864
4876	4877	4878	4879	4880	4881	4882	4883	4885	4886	4888	4889	4907
4908	4909	4914	4915	4928	4929	4930	4931	4932	4933	4934	4935	4937
4938	4939	4940	4954	4955	4956	4957	4958	4959	4960	4961	4963	4964
4965	4966	4978	4979	4980	4981	4982	4983	4984	4985	4987	4988	4990
4991	5009	5010	5011	5016	5017	5029	5030	5031	5032	5033	5034	5035
5036	5038	5039	5040	5041	5055	5056	5057	5058	5059	5060	5061	5062
5064	5065	5066	5067	5079	5080	5081	5082	5083	5084	5085	5086	5088
5089	5091	5092	5110	5111	5112	5117	5118	5130	5131	5132	5133	5134
5135	5136	5137	5139	5140	5141	5142	5156	5157	5158	5159	5160	5161
5162	5163	5165	5166	5167	5168	5180	5181	5182	5183	5184	5185	5186
5187	5189	5190	5192	5193	5212	5213	5214	5219	5220	5232	5233	5234
5235	5236	5237	5238	5239	5241	5242	5243	5244	5258	5259	5260	5261
5262	5263	5264	5265	5267	5268	5269	5270	5282	5283	5284	5285	5286
5287	5288	5289	5291	5292	5294	5295	5313	5314	5315	5320	5321	5333
5334	5335	5336	5337	5338	5339	5340	5342	5343	5344	5345	5359	5360
5361	5362	5363	5364	5365	5366	5368	5369	5370	5371	5383	5384	5385
5386	5387	5388	5389	5390	5392	5393	5395	5396	5412	5413	5414	5456
5457	5458	5459	5460	5465	5466	5467	5473	5474	5493	5494	5495	5527
5528	5529	5530	5531	5535	5536	5537	5545	5546	5588	5589	5590	5645
5646	5647	5648	5649	5680	5681	5682	5728	5729	5730	5731	5732	5736
5737	5776	5777	5778	5833	5834	5835	5836	5837	5868	5869	5870	5878

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5879	5893	5894	5895	5908	5909	5910	5911	5912	5914	5915	5916	5927
5928	5929	5930	5931	5933	5934	5935	5944	5945	5946	5947	5948	5951
5952	5967	5968	5969	5982	5983	5984	5985	5986	5988	5989	5990	6000
6001	6002	6003	6004	6006	6007	6008	6017	6018	6019	6020	6021	6024
6025	6054	6055	6056	6057	6058	6071	6072	6073	6074	6075	6087	6088
6089	6090	6091	6097	6098	6113	6114	6130	6131	6132	6133	6134	6152
6153	6154	6155	6156	6165	6166	6167	6168	6169	6173	6174	6175	6182
6183	6184	6185	6186	6195	6196	6197	6198	6199	6207	6208	6333	6334
6335	6336	6337	6338	6339	6340	6364	6365	6366	6367	6368	6386	6387
6388	6389	6390	6391	6392	6393	6412	6413	6414	6415	6416	6417	6418
6419	6423	6424	6425	6436	6437	6484	6485	6486	6487	6488	6492	6493
6508	6509	6510	6539	6540	6541	6542	6543	6546	6547	6548	6552	6553
6554	6561	6562	6579	6580	6581	6629	6630	6631	6632	6633	6635	6636
6637	6644	6645	6646	6647	6648	6651	6652	6653	6659	6660	6661	6662
6663	6665	6666	6667	6673	6674	6675	6676	6677	6679	6680	6681	6689
6690	6691	6692	6693	6695	6696	6697	6701	6702	6703	6704	6705	6706
6707	6708	6713	6714	6715	6716	6717	6718	6719	6720	6725	6726	6727
6728	6729	6731	6732	6733	6753	6754	6788	6789	6790	6807	6808	6809
6810	6811	6815	6816	6838	6839	6840	6841	6842	6843	6844	6845	6852
6853	6854	6855	6856	6861	6862	6878	6879	6880	6908	6909	6910	6911
6912	6915	6916	6917	6924	6925	6944	6945	6946	6966	6967	6968	6969
6970	6975	6976	7013	7014	7015	7016	7017	7021	7022	7041	7042	7043
7079	7080	7081	7082	7083	7088	7089	7108	7109	7110	7132	7133	7134
7135	7136	7137	7138	7140	7141	7158	7159	7160	7161	7162	7164	7165
7181	7182	7183	7184	7185	7188	7189	7191	7192	7204	7205	7206	7207
7208	7215	7216	7230	7231	7234	7235	7236	7237	7238	7239	7240	7241
7242	7243	7244	7251	7252	7253	7254	7255	7256	7257	7258	7342	7343
7347	7348	7358	7359	7360	7361							
1250#	1262#											
1250#	1264#	1463	1464	1478	1479	2389	2390	2418	2419	2447	2448	2475
2476	2503	2504	2532	2533	2561	2562	2589	2590	2617	2618	2645	2646
2673	2674	2701	2702	2730	2731	2758	2759	2781	2782	2809	2810	2837
2838	2847	2850	2868	2869	2885	2886	2902	2903	2922	2923	2941	2942
2966	2967	2985	2986	3005	3006	3026	3027	3177	3178	3203	3204	3219
3220	3234	3240	3257	3258	3309	3310	3372	3373	3412	3413	3422	3423
3463	3464	3474	3475	3519	3520	3542	3543	3550	3551	3612	3613	3674
3675	3765	3766	3894	3895	3981	3982	4033	4034	4057	4058	4081	4082
4084	4085	4132	4133	4155	4156	4178	4179	4181	4182	4231	4232	4256
4257	4280	4281	4283	4284	4332	4333	4356	4357	4380	4381	4383	4384
4433	4434	4457	4458	4481	4482	4484	4485	4534	4535	4558	4559	4582
4583	4585	4586	4634	4635	4658	4659	4682	4683	4685	4686	4734	4735
4758	4759	4782	4783	4785	4786	4834	4835	4860	4861	4884	4885	4887
4888	4936	4937	4962	4963	4986	4987	4989	4990	5037	5038	5063	5064
5087	5088	5090	5091	5138	5139	5164	5165	5188	5189	5191	5192	5240
5241	5266	5267	5290	5291	5293	5294	5341	5342	5367	5368	5391	5392
5394	5395	5472	5473	5544	5545	5735	5736	5877	5878	5950	5951	6023
6024	6096	6097	6206	6207	6435	6436	6491	6492	6560	6561	6752	6753
6814	6815	6860	6861	6923	6924	6974	6975	7020	7021	7087	7088	7214
7215	7258	7259	7348	7349								
1250#	1261#	3280	3281	3323	3324	3383	3384	3433	3434	3486	3487	3562
3563	3623	3624	3686	3687	3777	3778	3907	3908	3998	3999	4101	4102
4198	4199	4300	4301	4400	4401	4501	4502	4602	4603	4702	4703	4802
4803	4904	4905	5006	5007	5107	5108	5209	5210	5310	5311	5409	5410
5490	5491	5583	5584	5771	5772	5890	5891	5964	5965	6035	6036	6111
6112	6221	6222	6449	6450	6504	6505	6574	6575	6767	6768	6828	6829
6874	6875	6940	6941	6991	6992	7037	7038	7103	7104			

SVCSUB= 000C00  
SVCTAG= 000000

SVCTST= 000000



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SV05	003632	2065#	3297	3345	3365	3404	3455	3511	3534	3594	3656	3718	3751	3816
		3841	3888	3933	3956	3975	4025	4049	4073	4124	4147	4170	4222	4247
		4272	4324	4348	4372	4425	4449	4473	4526	4550	4574	4626	4650	4674
		4726	4750	4774	4826	4852	4876	4928	4954	4978	5029	5055	5079	5130
		5156	5180	5232	5258	5282	5333	5359	5383	5456	5527	5645	5728	5833
		5908	5927	5944	5982	6000	6017	6130	6152	6165	6182	6195	6333	6364
		6386	6412	6484	6539	6629	6644	6659	6673	6689	6701	6713	6725	6807
		6838	6852	6908	6966	7013	7079	7134	7158	7181	7204			
SWPAC1	027665	7292#												
SWPAC2	027726	7298#												
S&LSYM=	010000	1250#	1464#	1479#	2390#	2419#	2448#	2476#	2504#	2533#	2562#	2590#	2618#	2646#
		2674#	2702#	2731#	2759#	2782#	2810#	2838#	2850#	2869#	2886#	2903#	2923#	2942#
		2967#	2986#	3006#	3027#	3178#	3204#	3220#	3240#	3258#	3310#	3373#	3395#	3423#
		3445#	3475#	3497#	3522#	3551#	3613#	3675#	3766#	3895#	3982#	4010#	4036#	4060#
		4085#	4112#	4135#	4158#	4182#	4209#	4234#	4259#	4284#	4311#	4335#	4359#	4384#
		4412#	4436#	4460#	4485#	4513#	4537#	4561#	4586#	4613#	4637#	4661#	4686#	4713#
		4737#	4761#	4786#	4812#	4837#	4863#	4888#	4914#	4939#	4965#	4990#	5016#	5040#
		5066#	5091#	5117#	5141#	5167#	5192#	5219#	5243#	5269#	5294#	5320#	5344#	5370#
		5395#	5473#	5545#	5736#	5878#	5951#	6024#	6097#	6207#	6436#	6492#	6561#	6753#
		6815#	6861#	6924#	6975#	7021#	7088#	7215#	7259#	7349#				
TEMP	002440	1641#	6039*	6064*	6083*	6118*	6126*							
TFM1	003666	2085#	2379	2408	2437									
TFM2	003712	2089#	2465	2493	2579	2663	2799	2827						
TFM3	003730	2092#	2522	2551										
TFM36	004017	2103#												
TFM4	003755	2096#	2607	2635	2691	2748								
TFM40	004263	2133#	2856											
TFM41	004105	2113#	2873											
TFM42	004174	2123#	2890											
TFM43	004344	2142#	2910											
TFM44	004427	2151#	2929											
TFM45	004466	2157#	2948											
TFM45A	004524	2162#	2954											
TFM46	004647	2177#	2973											
TFM47	004733	2186#	2993											
TFM5	003773	2099#	2720											
TMMC	005010	2194#	2928	2947										
TYPE	002432	1638#	3162*	3167*	3172*	3386	3436	3489	3910	6311				
T\$ARGC=	000001	1283#	1284#	1285#	1286#	1287#	1288#	2364#	2369	2370#	2375	2376#	2383	2384#
		2388	2393#	2398	2399#	2404	2405#	2412	2413#	2417	2422#	2427	2428#	2433
		2434#	2441	2442#	2446	2451#	2456	2457#	2462	2463#	2469	2470#	2474	2479#
		2484	2485#	2490	2491#	2497	2498#	2502	2507#	2512	2513#	2518	2519#	2526
		2527#	2531	2536#	2541	2542#	2547	2548#	2555	2556#	2560	2565#	2570	2571#
		2576	2577#	2583	2584#	2588	2593#	2598	2599#	2604	2605#	2611	2612#	2616
		2621#	2626	2627#	2632	2633#	2639	2640#	2644	2649#	2654	2655#	2660	2661#
		2667	2668#	2672	2677#	2682	2683#	2688	2689#	2695	2696#	2700	2705#	2710
		2711#	2716	2717#	2724	2725#	2729	2734#	2739	2740#	2745	2746#	2752	2753#
		2757	2764#	2769	2770#	2775	2776#	2780	2785#	2790	2791#	2796	2797#	2803
		2804#	2808	2813#	2818	2819#	2824	2825#	2831	2832#	2836	2843#	2847	2855#
		2860	2862#	2866	2873#	2877	2879#	2883	2890#	2894	2896#	2900	2908#	2914
		2916#	2920	2927#	2933	2935#	2939	2946#	2952	2954#	2958	2960#	2964	2971#
		2977	2979#	2983	2991#	2997	2999#	3003						
T\$CODE=	012032	7234#	7240#	7251#										
T\$ERRN=	000056	1250#	3298#	3346#	3366#	3405#	3456#	3512#	3535#	3595#	3657#	3719#	3752#	3817#
		3842#	3889#	3934#	3957#	3976#	4026#	4050#	4074#	4125#	4148#	4171#	4223#	4248#
		4273#	4325#	4349#	4373#	4426#	4450#	4474#	4527#	4551#	4575#	4627#	4651#	4675#

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	4727#	4751#	4775#	4827#	4853#	4877#	4929#	4955#	4979#	5030#	5056#	5080#	5131#
	5157#	5181#	5233#	5259#	5283#	5334#	5360#	5384#	5457#	5528#	5646#	5729#	5834#
	5909#	5928#	5945#	5983#	6001#	6018#	6055#	6072#	6088#	6131#	6153#	6166#	6183#
	6196#	6334#	6365#	6387#	6413#	6485#	6540#	6630#	6645#	6660#	6674#	6690#	6702#
	6714#	6726#	6808#	6839#	6853#	6909#	6967#	7014#	7080#	7135#	7159#	7182#	7205#
TSEXCP= 000000	7234#	7239	7240#	244	7251#	7256							
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	3661#	3723#	3756#	3849#	3910#	3938#	4002#	4030#	4054#	4078#	4104#	4129#	
	4152#	4175#	4201#	4228#	4253#	4277#	4303#	4329#	4353#	4377#	4403#	4430#	4454#
	4478#	4504#	4531#	4555#	4579#	4605#	4631#	4655#	4679#	4705#	4731#	4755#	4779#
	4805#	4831#	4857#	4881#	4907#	4933#	4959#	4983#	5009#	5034#	5060#	5084#	5110#
	5135#	5161#	5185#	5212#	5237#	5263#	5287#	5313#	5338#	5364#	5388#	5412#	5465#
	5493#	5535#	5588#	5680#	5776#	5868#	5893#	5914#	5933#	5967#	5988#	6006#	6173#
	6338#	6391#	6417#	6423#	6508#	6546#	6552#	6579#	6635#	6651#	6665#	6679#	6695#
	6706#	6718#	6731#	6788#	6843#	6878#	6915#	6944#	7041#				
TSGMAN= 000000	1250#												
TSMILI= 000001	7234#	7238	7240#	7243	7251#	7255							
TSLAST= 000001	1250#	7359#											
TSLOLI= 000000	7234#	7237	7240#	7242	7251#	7254							
TSLSYM= 010000	1250#	1464	1479	2390	2419	2448	2476	2504	2533	2562	2590	2618	2646
	2674	2702	2731	2759	2782	2810	2838	2850	2869	2886	2903	2923	2942
	2967	2986	3006	3027	3178	3204	3220	3240	3258	3310	3373	3423	3475
	3551	3613	3675	3766	3895	3982	4085	4182	4284	4384	4485	4586	4686
	4786	4888	4990	5091	5192	5294	5395	5473	5545	5736	5878	5951	6024
	6097	6207	6436	6492	6561	6753	6815	6861	6924	6975	7021	7088	7215
	7259	7349											
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	2447#	2450#	2475#	2478#	2503#	2506#	2532#	2535#	2561#	2564#	2589#	2592#	2617#
	2620#	2645#	2648#	2673#	2676#	2701#	2704#	2730#	2733#	2758#	2763#	2781#	2784#
	2809#	2812#	2837#	2841#	2849#	2853#	2868#	2871#	2885#	2888#	2902#	2906#	2922#
	2925#	2941#	2944#	2966#	2969#	2985#	2989#	3005#	3017#	3026#	3041#	3177#	3182#
	3203#	3214#	3219#	3234#	3239#	3255#	3257#	3281#	3309#	3324#	3372#	3384#	3395#
	3412#	3422#	3434#	3445#	3463#	3474#	3487#	3497#	3519#	3522#	3542#	3550#	3563#
	3612#	3624#	3674#	3687#	3765#	3778#	3894#	3908#	3981#	3999#	4010#	4033#	4036#
	4057#	4060#	4081#	4084#	4102#	4112#	4132#	4135#	4155#	4158#	4178#	4181#	4199#
	4209#	4231#	4234#	4256#	4259#	4280#	4283#	4301#	4311#	4332#	4335#	4356#	4359#
	4380#	4383#	4401#	4412#	4433#	4436#	4457#	4460#	4481#	4484#	4502#	4513#	4534#
	4537#	4558#	4561#	4582#	4585#	4603#	4613#	4634#	4637#	4658#	4661#	4682#	4685#
	4703#	4713#	4734#	4737#	4758#	4761#	4782#	4785#	4803#	4812#	4834#	4837#	4860#
	4863#	4884#	4887#	4905#	4914#	4936#	4939#	4962#	4965#	4986#	4989#	5007#	5016#
	5037#	5040#	5063#	5066#	5087#	5090#	5108#	5117#	5138#	5141#	5164#	5167#	5188#
	5191#	5210#	5219#	5240#	5243#	5266#	5269#	5290#	5293#	5311#	5320#	5341#	5344#
	5367#	5370#	5391#	5394#	5410#	5472#	5491#	5544#	5584#	5735#	5772#	5877#	5891#
	5950#	5965#	6023#	6036#	6096#	6112#	6206#	6222#	6435#	6450#	6491#	6505#	6560#
	6575#	6752#	6768#	6814#	6829#	6860#	6875#	6923#	6941#	6974#	6992#	7020#	7038#
	7087#	7104#	7214#	7230#	7257#	7342#	7347#						
TSNSO = 000000	1256#												
TSNS1 = 000005	1370#	1375	1445#	1463	1472#	1478	2363#	2389	2392#	2418	2421#	2447	2450#
	2475	2478#	2503	2506#	2532	2535#	2561	2564#	2589	2592#	2617	2620#	2645
	2648#	2673	2676#	2701	2704#	2730	2733#	2758	2763#	2781	2784#	2809	2812#
	2837	2841#	2849	2853#	2868	2871#	2885	2888#	2902	2906#	2922	2925#	2941
	2944#	2966	2969#	2985	2989#	3005	3017#	3026	3041#	3177	3182#	3203	3214#
	3219	3234#	3239	3255#	3257	3281#	3309	3324#	3372	3384#	3422	3434#	3474
	3487#	3550	3563#	3612	3624#	3674	3687#	3765	3778#	3894	3908#	3981	3999#
	4084	4102#	4181	4199#	4283	4301#	4383	4401#	4484	4502#	4585	4603#	4685

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CROSS REFERENCE TABLE -- USER SYMBOLS

	4703#	4785	4803#	4887	4905#	4989	5007#	5090	5108#	5191	5210#	5293	5311#
	5394	5410#	5472	5491#	5544	5584#	5735	5772#	5877	5891#	5950	5965#	6023
	6036#	6096	6112#	6206	6222#	6435	6450#	6491	6505#	6560	6575#	6752	6768#
	6814	6829#	6860	6875#	6923	6941#	6974	6992#	7020	7038#	7087	7104#	7214
	7230#	7257	7342#	7347									
T\$NS2 = 000003	3395#	3412	3445#	3463	3497#	3519	3522#	3542	4010#	4033	4036#	4057	4060#
	4081	4112#	4132	4135#	4155	4158#	4178	4209#	4231	4234#	4256	4259#	4280
	4311#	4332	4335#	4356	4359#	4380	4412#	4433	4436#	4457	4460#	4481	4513#
	4534	4537#	4558	4561#	4582	4613#	4634	4637#	4658	4661#	4682	4713#	4734
	4737#	4758	4761#	4782	4812#	4834	4837#	4860	4863#	4884	4914#	4936	4939#
	4962	4965#	4986	5016#	5037	5040#	5063	5066#	5087	5117#	5138	5141#	5164
	5167#	5188	5219#	5240	5243#	5266	5269#	5290	5320#	5341	5344#	5367	5370#
	5391												
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T\$SAVL= 177777	1250#												
T\$SEGL= 177777	1250#	3395#	3410	3412#	3414	3445#	3461	3463#	3465	3497#	3517	3519#	3521
	3522#	3540	3542#	3544	4010#	4031	4033#	4035	4036#	4055	4057#	4059	4060#
	4079	4081#	4083	4112#	4130	4132#	4134	4135#	4153	4155#	4157	4158#	4176
	4178#	4180	4209#	4229	4231#	4233	4234#	4254	4256#	4258	4259#	4278	4280#
	4282	4311#	4330	4332#	4334	4335#	4354	4356#	4358	4359#	4378	4380#	4382
	4412#	4431	4433#	4435	4436#	4455	4457#	4459	4460#	4479	4481#	4483	4513#
	4532	4534#	4536	4537#	4556	4558#	4560	4561#	4580	4582#	4584	4613#	4632
	4634#	4636	4637#	4656	4658#	4660	4661#	4680	4682#	4684	4713#	4732	4734#
	4736	4737#	4756	4758#	4760	4761#	4780	4782#	4784	4812#	4832	4834#	4836
	4837#	4858	4860#	4862	4863#	4882	4884#	4886	4914#	4934	4936#	4938	4939#
	4960	4962#	4964	4965#	4984	4986#	4988	5016#	5035	5037#	5039	5040#	5061
	5063#	5065	5066#	5085	5087#	5089	5117#	5136	5138#	5140	5141#	5162	5164#
	5166	5167#	5186	5188#	5190	5219#	5238	5240#	5242	5243#	5264	5266#	5268
	5269#	5288	5290#	5292	5320#	5339	5341#	5343	5344#	5365	5367#	5369	5370#
	5389	5391#	5393										
T\$SEKO= 010002	3395#	3410	3412#	3445#	3461	3463#	3497#	3517	3519	3522#	3540	3542	4010#
	4031	4033	4036#	4055	4057	4060#	4079	4081	4112#	4170	4132	4135#	4153
	4155	4158#	4176	4178	4209#	4229	4231	4234#	4254	4256#	4259	4278	4280#
	4311#	4330	4332	4335#	4354	4356#	4359#	4378	4380	4412#	4431	4433	4436#
	4455	4457	4460#	4479	4481	4513#	4532	4534	4537#	4556	4558#	4561#	4580
	4582	4613#	4632	4634	4637#	4656	4658	4661#	4680	4682#	4713#	4732	4734#
	4737#	4756	4758	4761#	4780	4782	4812#	4832	4834	4837#	4851	4860	4863#
	4882	4884	4914#	4934	4936	4939#	4960	4962	4965#	4984	4986	5016#	5035
	5037	5040#	5061	5063	5066#	5085	5087	5117#	5136	5138#	5141#	5162	5164#
	5167#	5186	5188	5219#	5238	5240	5243#	5264	5266	5269#	5288	5290	5320#
	5339	5341	5344#	5365	5367	5370#	5389	5391					
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	4198#	4300#	4400#	4501#	4602#	4702#	4802#	4904#	5006#	5107#	5209#	5310#	5409#
	5490#	5583#	5771#	5890#	5964#	6035#	6111#	6221#	6449#	6504#	6574#	6767#	6828#
	6874#	6940#	6991#	7037#	7103#								
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T\$TAGN= 010120	1250#	1370#	1445#	1472#	2363#	2392#	2421#	2450#	2478#	2506#	2535#	2564#	2592#
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	3434#	3487#	3563#	3624#	3687#	3778#	3908#	3999#	4102#	4199#	4301#	4401#	4502#
	4603#	4703#	4803#	4905#	5007#	5108#	5210#	5311#	5410#	5491#	5584#	5772#	5891#
	5965#	6036#	6112#	6222#	6450#	6505#	6575#	6768#	6829#	6875#	6941#	6992#	7038#
	7104#	7230#	7342#										
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	1398#	1399#	1400#	1401#	1402#	1403#	1404#	1405#	1406#	1407#	1408#	1409#	1410#
	1411#	1412#	1413#	1414#	1415#	1416#	1417#	1418#	1419#	1420#	1421#	1422#	1423#

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1424#	1425#	1426#	1427#	1428#	1429#	1463#	1478#	2389#	2418#	2447#	2475#	2503#
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2868#	2885#	2902#	2922#	2941#	2966#	2985#	3005#	3021#	3022#	3026#	3177#	3203#
3219#	3239#	3257#	3288#	3289#	3305#	3306#	3309#	3351#	3352#	3372#	3386#	3387#
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3517#	3519#	3539#	3540#	3542#	3550#	3599#	3600#	3612#	3661#	3662#	3674#	3723#
3724#	3756#	3757#	3765#	3780#	3781#	3849#	3850#	3894#	3910#	3911#	3938#	3939#
3981#	4002#	4003#	4030#	4031#	4033#	4054#	4055#	4057#	4078#	4079#	4081#	4084#
4104#	4105#	4129#	4130#	4132#	4152#	4153#	4155#	4175#	4176#	4178#	4181#	4201#
4202#	4228#	4229#	4231#	4253#	4254#	4256#	4277#	4278#	4280#	4283#	4303#	4304#
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4534#	4555#	4556#	4558#	4579#	4580#	4582#	4585#	4605#	4606#	4631#	4632#	4634#
4655#	4656#	4658#	4679#	4680#	4682#	4685#	4705#	4706#	4731#	4732#	4734#	4755#
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4860#	4881#	4882#	4884#	4887#	4907#	4908#	4933#	4934#	4936#	4959#	4960#	4962#
4983#	4984#	4986#	4989#	5009#	5010#	5034#	5035#	5037#	5060#	5061#	5063#	5084#
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6695#	6696#	6706#	6707#	6718#	6719#	6731#	6732#	6752#	6788#	6789#	6814#	6843#
6844#	6860#	6878#	6879#	6915#	6916#	6923#	6944#	6945#	6974#	7020#	7041#	7042#
7087#	7214#	7234#	7240#	7251#	7257#	7347#						
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4198#	4287#	4297#	4300#	4387#	4397#	4400#	4488#	4498#	4501#	4589#	4599#	4602#
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6501#	6504#	6565#	6571#	6574#	6756#	6764#	6767#	6818#	6825#	6828#	6864#	6871#
6874#	6927#	6937#	6940#	6978#	6988#	6991#	7024#	7034#	7037#	7091#	7100#	7103#
7362#												
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2440#	2445#	2448#	2455#	2461#	2468#	2473#	2476#	2483#	2489#	2496#	2501#	2504#
2511#	2517#	2525#	2530#	2533#	2540#	2546#	2554#	2559#	2562#	2569#	2575#	2582#
2587#	2590#	2597#	2603#	2610#	2615#	2618#	2625#	2631#	2638#	2643#	2646#	2653#
2659#	2666#	2671#	2674#	2681#	2687#	2694#	2699#	2702#	2709#	2715#	2723#	2728#
2731#	2738#	2744#	2751#	2756#	2759#	2768#	2774#	2779#	2782#	2789#	2795#	2802#
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2882#	2886#	2893#	2899#	2903#	2913#	2919#	2923#	2932#	2938#	2942#	2951#	2957#
2963#	2967#	2976#	2982#	2986#	2996#	3002#	3006#	3027#	3058#	3064#	3070#	3076#
3073#	3178#	3198#	3204#	3216#	3220#	3237#	3240#	3258#	3288#	3297#	3305#	3310#
3345#	3351#	3365#	3373#	3386#	3395#	3404#	3409#	3413#	3423#	3436#	3445#	3455#
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3594#	3599#	3606#	3613#	3656#	3661#	3668#	3675#	3718#	3723#	3751#	3756#	3759#
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3982#	4002#	4010#	4025#	4030#	4034#	4036#	4049#	4054#	4058#	4060#	4073#	4078#
4082#	4085#	4104#	4112#	4124#	4129#	4133#	4135#	4147#	4152#	4156#	4158#	4170#
4175#	4179#	4182#	4201#	4209#	4222#	4228#	4232#	4234#	4247#	4253#	4257#	4259#

TEST= 00053

TESTM= 17777

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	4272	4277	4281	4284	4303	4311	4324	4329	4333	4335	4348	4353	4357
	4359	4372	4377	4381	4384	4403	4412	4425	4430	4434	4436	4449	4454
	4458	4460	4473	4478	4482	4485	4504	4513	4526	4531	4535	4537	4550
	4555	4559	4561	4574	4579	4583	4586	4605	4613	4626	4631	4635	4637
	4650	4655	4659	4661	4674	4679	4683	4686	4705	4713	4726	4731	4735
	4737	4750	4755	4759	4761	4774	4779	4783	4786	4805	4812	4826	4831
	4835	4837	4852	4857	4861	4863	4876	4881	4885	4888	4907	4914	4928
	4933	4937	4939	4954	4959	4963	4965	4978	4983	4987	4990	5009	5016
	5029	5034	5038	5040	5055	5060	5064	5066	5079	5084	5088	5091	5110
	5117	5130	5135	5139	5141	5156	5161	5165	5167	5180	5185	5189	5192
	5212	5219	5232	5237	5241	5243	5258	5263	5267	5269	5282	5287	5291
	5294	5313	5320	5333	5338	5342	5344	5359	5364	5368	5370	5383	5388
	5392	5395	5412	5456	5465	5473	5493	5527	5535	5545	5588	5645	5680
	5728	5736	5776	5833	5868	5878	5893	5908	5914	5927	5933	5944	5951
	5967	5982	5988	6000	6006	6017	6024	6054	6071	6087	6097	6113	6130
	6152	6165	6173	6182	6195	6207	6333	6338	6364	6386	6391	6412	6417
	6423	6436	6484	6492	6508	6539	6546	6552	6561	6579	6629	6635	6644
	6651	6659	6665	6673	6679	6689	6695	6701	6706	6713	6718	6725	6731
	6753	6788	6807	6815	6838	6843	6852	6861	6878	6908	6915	6924	6944
	6966	6975	7013	7021	7041	7079	7088	7109	7132	7134	7140	7158	7164
	7181	7188	7191	7204	7215								
TSTSTS= 000001	1250#	3281#	3324#	3384#	3434#	3487#	3563#	3624#	3687#	3778#	3908#	3999#	4102#
	4199#	4301#	4401#	4502#	4603#	4703#	4803#	4905#	5007#	5108#	5210#	5311#	5410#
	5491#	5584#	5772#	5891#	5965#	6036#	6112#	6222#	6450#	6505#	6575#	6768#	6829#
	6875#	6941#	6992#	7038#	7104#								
TSSAU = 010042	3255#	3257											
TSSAUT= 010037	3182#	3203											
TSSCLE= 010040	3214#	3219											
TSSDU = 010041	3234#	3239											
TSSHAR= 010116	7230#	7258											
TSSHW = 010001	1445#	1463											
TSSINI= 010036	3041#	3177											
TSSMSG= 010034	2363#	2389	2392#	2418	2421#	2447	2450#	2475	2478#	2503	2506#	2532	2535#
	2561	2564#	2589	2592#	2617	2620#	2645	2648#	2673	2676#	2701	2704#	2730
	2733#	2758	2763#	2781	2784#	2809	2812#	2837	2841#	2849	2853#	2868	2871#
	2E	2888#	2902	2906#	2922	2925#	2941	2944#	2966	2969#	2985	2989#	3005
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TSSRPT= 010035	3017#	3021	3026										
TSSSEG= 010002	3395#	3409	3412#	3445#	3460	3463#	3497#	3516	3519#	3522#	3539	3542#	4010#
	4030	4033#	4036#	4054	4057#	4060#	4078	4081#	4112#	4129	4132#	4135#	4152
	4155#	4158#	4175	4178#	4209#	4228	4231#	4234#	4253	4256#	4259#	4277	4280#
	4311#	4329	4332#	4335#	4353	4356#	4359#	4377	4380#	4412#	4430	4433#	4436#
	4454	4457#	4460#	4478	4481#	4513#	4531	4534#	4537#	4555	4558#	4561#	4579
	4582#	4613#	4631	4634#	4637#	4655	4658#	4661#	4679	4682#	4713#	4731	4734#
	4737#	4755	4758#	4761#	4779	4782#	4812#	4831	4834#	4837#	4857	4860#	4863#
	4881	4884#	4914#	4933	4936#	4939#	4959	4962#	4965#	4983	4986#	5016#	5034
	5037#	5040#	5060	5063#	5066#	5084	5087#	5117#	5135	5138#	5141#	5161	5164#
	5167#	5185	5188#	5219#	5237	5240#	5243#	5263	5266#	5269#	5287	5290#	5320#
	5338	5341#	5344#	5364	5367#	5370#	5388	5391#					
TSSSOF= 010117	7342#	7348											
TSSSW = 010002	1472#	1478											
TSSTES= 010115	3281#	3288	3305	3309	3324#	3351	3372	3384#	3386	3422	3434#	3436	3474
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	4181	4199#	4201	4283	4301#	4303	4383	4401#	4403	4484	4502#	4504	4585
	4603#	4605	4685	4703#	4705	4785	4803#	4805	4887	4905#	4907	4989	5007#

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		5009	5090	5108#	5110	5191	5210#	5212	5293	5311#	5313	5394	5410#	5412	
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		5877	5891#	5893	5914	5933	5950	5965#	5967	5988	6006	6023	6036#	6096	
		6112#	6173	6206	6222#	6338	6391	6417	6423	6435	6450#	6491	6505#	6508	
		6546	6552	6560	6575#	6579	6635	6651	6665	6679	6695	6706	6718	6731	
		6752	6768#	6788	6814	6829#	6843	6860	6875#	6878	6915	6923	6941#	6944	
		6974	6992#	7020	7038#	7041	7087	7104#	7214						
T1	012146	G	1386	3280#											
T10	014470	G	1395	3907#											
T11	014736	G	1396	3998#											
T12	015202	G	1397	4101#											
T13	015432	G	1398	4198#											
T14	015676	G	1399	4300#											
T15	016142	G	1400	4400#											
T16	016406	G	1401	4501#											
T17	016652	G	1402	4602#											
T18	017116	G	1403	4702#											
T19	017362	G	1404	4802#											
T2	012256	G	1387	3323#											
T20	017642	G	1405	4904#											
T21	020122	G	1406	5006#											
T22	020376	G	1407	5107#											
T23	020654	G	1408	5209#											
T24	021130	G	1409	5310#											
T25	021404	G	1410	5409#											
T26	021576	G	1411	5490#											
T27	021744	G	1412	5583#											
T28	022322	G	1413	5771#											
T29	022560	G	1414	5890#											
T3	012422	G	1388	3383#											
T30	022774	G	1415	5964#											
T31	023210	G	1416	6035#											
T32	023452	G	1417	6111#											
T33	024044	G	1418	6221#											
T34	025116	G	1419	6449#											
T35	025216	G	1420	6504#											
T36	025364	G	1421	6574#											
T37	026042	G	1422	6767#											
T38	026202	G	1423	6828#											
T39	026310	G	1424	6874#											
T4	012552	G	1389	3433#											
T40	026446	G	1425	6940#											
T41	026544	G	1426	6991#											
T42	026644	G	1427	7037#											
T43	026770	G	1428	7103#											
T5	012712	G	1390	3486#											
T6	013154	G	1391	3562#											
T7	013356	G	1392	3623#											
T8	013570	G	1393	3686#											
T9	014112	G	1394	3777#											
UAM	= 000200	G	1564#												
VECTOR	027504		7272#												
WPM	027400		7235	7260#											
WROM	003422		2004#												
WTYPE	002414		1631#	1887	1986	1988	2011	2033	3097*	3163	3170	3505	3862	4001	
			4104	4201	4303	4403	4504	4605	4705	4805	4840	4907	4942	5009	5043

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	5110	5144	5212	5246	5313	5347	5638	5693	5826	6077	6507	6578	6877
	5110	5144											
	6943	7040											
X\$ALWA= 000000	1250#												
X\$FALS= 000040	1250#												
X\$OFFS= 000400	1250#												
X\$TRUE= 000020	1250#												
ZERO 002370	1621#												
\$BDADR 002450	1645#												
\$BDDAT 002454	1647#												
\$GDADR 002446	1644#												
\$GDDAT 002452	1646#	2972	6049*	6050	6052	6322*	6327	6330*	6331	6355*	6360	6362	6377*
	6382	6384	6403*	6408	6410	7126*	7129	7153*	7176*	7177	7201*		
\$LSTIN= 000000	1258#												
\$LSTIA= 000000	1259#												
\$REG0 002430	1637#	2070*	2376	2405									
\$REG1 002426	1636#	2069*											
\$REG2 002424	1635#	2068*	2378	2407	2434	2548	2606	2690					
\$REG3 002422	1634#	2067*											
\$REG4 002420	1633#	2066*	2377	2406	2435	2463	2491	2520	2549	2577	2605	2633	2661
	2689	2717	2746	2797	2825								
\$REG5 002416	1632#	2065*	2436	2464	2492	2521	2550	2578	2634	2662	2718	2747	2798
	2826												
\$TEMPO 002442	1642#												
\$TMPO 002444	1643#	6040*	6065*	6066	6069	6080	6119*	6149	6156				
. = 030144	1241#	1624#	1625#	1626#	1627#	1660#	1706#	1732#	1870#	3022	3289	3306	3352
	3387	3410	3437	3461	3490	3517	3540	3600	3662	3724	3757	3781	3850
	3911	3926	3939	4003	4031	4055	4079	4105	4130	4153	4176	4202	4229
	4254	4278	4304	4330	4354	4378	4404	4431	4455	4479	4505	4532	4556
	4580	4606	4632	4656	4680	4706	4732	4756	4780	4806	4832	4858	4882
	4908	4934	4960	4984	5010	5035	5061	5085	5111	5136	5162	5186	5202
	5213	5238	5264	5288	5314	5339	5365	5389	5413	5466	5494	5536	5589
	5681	5777	5869	5894	5915	5934	5968	5989	6007	6174	6339	6392	6418
	6424	6428#	6432#	6509	6547	6553	6580	6636	6652	6666	6680	6696	6707
	6719	6732	6789	6844	6879	6916	6945	7042	7322#				
.MSTCL 002756	1865#	3326	3441	3495	3567	3628	3691	3786	3916	4009	4110	4207	4309
	4409	4510	4610	4711	4810	4912	5014	5115	5217	5318	5417	5498	5591
	5779	5896	5970	6039	6118	6129	6181	6194	6204	6225	6884	6950	7047
	7107												
.REGT 003050	1879#	1888											
.ROMCL 003044	1876#	1905	1908	1911	1921	1929	1937	1945	1953	1956	1959	1970	1993
	1999	3331	3334	3337	3355	3358	3574	3577	3581	3584	3587	3636	3639
	3643	3646	3649	3698	3701	3705	3708	3711	3735	3738	3741	3744	3790
	3793	3796	3803	3806	3825	3829	3869	3872	3875	3878	3918	3922	3942
	3948	3961	3964	3967	5421	5424	5429	5445	5448	5507	5510	5519	5613
	5616	5623	5626	5705	5708	5711	5715	5801	5804	5811	5814	5900	5918
	5937	5974	5992	6010	6060	6230	6244	6248	6252	6266	6270	6274	6281
	6284	6288	6292	6296	6305	6308	6324	6357	6375	6379	6398	6401	6405
	6453	6456	6459	6462	6467	6471	6885	6888	6896	6900	6952	6956	7000
	7007	7055	7059	7062	7072	7113	7117	7120	7124	7146	7150	7169	7172
	7196												
.SROMC 003100	1885#	1914	1962	1973	3809	3821	4015	4018	4039	4042	4063	4066	4114
	4117	4137	4140	4160	4163	4212	4215	4237	4240	4262	4265	4314	4317
	4338	4341	4362	4365	4415	4418	4439	4442	4463	4466	4516	4519	4540
	4543	4564	4567	4616	4619	4640	4643	4664	4667	4716	4719	4740	4743
	4764	4767	4816	4819	4842	4845	4866	4869	4918	4921	4944	4947	4968
	4971	5019	5022	5045	5048	5069	5072	5120	5123	5146	5149	5170	5173





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BADHEA	1785#	3272	3276	3314	3319	3375	3379	3425	3429	3477	3482	3554	5558	3615	3619
	3677	3682	3768	3773	3897	3903	3984	3994	4087	4097	4184	4194	4286	4296	4386
	4396	4487	4497	4588	4598	4688	4698	4788	4798	4890	4900	4992	5002	5093	5103
	5194	5205	5296	5306	5397	5405	5476	5486	5547	5579	5737	5767	5879	5886	5953
	5960	6025	6031	6099	6107	6209	6217	6438	6445	6494	6500	6564	6570	6755	6763
	6817	6824	6863	6870	6926	6936	6977	6987	7023	7033	7090	7099			
BAMPL	1#	1250#	3059	3065	3071										
BERROR	1#	1250#													
BGNAU	1#	1250#	3254												
BGNAUT	1#	1250#	3181												
BGNCLN	1#	1250#	3213												
BGNDU	1#	1250#	3233												
BGNHRD	1#	1250#	7229												
BGNHW	1#	1250#	1444												
BGNINI	1#	1250#	3040												
BGNMOD	1#	1250#	1255												
BGNMSG	1#	1250#	2363	2392	2421	2450	2478	2506	2535	2564	2592	2620	2648	2676	2704
	2733	2763	2784	2812	2840	2852	2870	2887	2905	2924	2943	2968	2988		
BGNPRO	1#	1250#	1369												
BGNPTA	1#	1250#													
BGNRPT	1#	1250#	3016												
BGNSEG	1#	1250#	3394	3444	3496	3521	4009	4035	4059	4111	4134	4157	4208	4233	4258
	4310	4334	4358	4411	4435	4459	4512	4536	4560	4612	4636	4660	4712	4736	4760
	4811	4836	4862	4913	4938	4964	5015	5039	5065	5116	5140	5166	5218	5242	5268
	5319	5343	5369												
BGNSET	1#	1250#													
BGNSFT	1#	1250#	7341												
BGNSRV	1#	1250#													
BGNSUB	1#	1250#													
BGNSW	1#	1250#	1471												
BGNTST	1#	1250#	3279	3322	3382	3432	3485	3561	3622	3685	3776	3906	3997	4100	4197
	4299	4399	4500	4601	4701	4801	4903	5005	5106	5208	5309	5408	5489	5582	5770
	5889	5963	6034	6110	6220	6448	6503	6573	6766	6827	6873	6939	6990	7036	7102
			3077	3095											
BNCOMP	1#	1250#													
BNERRR	1#	1250#													
BREAK	1#	1250#	3605	3667	3758	3851									
BRESET	1#	1250#	3215	3236	6112	7131	7190								
CKLOOP	1#	1250#	7139	7163	7187										
CLOCK	1#	1250#													
CLOSE	1#	1250#													
CLRMAR	1825#	3792	3805												
CLRVEC	1#	1250#													
COMMEN	1#	1250#													
DELAY	1#	1250#													
DESCRI	1#	1250#	1593												
DEVTYP	1#	1250#	1726												
DISPAT	1#	1250#	1383												
DISPLA	1#	1250#													
DOCLN	1#	1250#													
DODU	1#	1250#	3196												
DORPT	1#	1250#													
EDSCAL	1780#	3273	3277	3315	3320	3376	3380	3426	3430	3478	3483	3555	3559	3616	3620
	3678	3683	3769	3774	3898	3904	3985	3995	4088	4098	4185	4195	4287	4297	4387
	4397	4488	4498	4589	4599	4689	4699	4789	4799	4891	4901	4993	5003	5094	5104
	5195	5206	5297	5307	5398	5406	5477	5487	5548	5580	5738	5768	5880	5887	5954
	5961	6026	6032	6100	6108	6210	6218	6439	6446	6495	6501	6565	6571	6756	6764



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CROSS REFERENCE TABLE -- MACRO NAMES

GETBYT	1#	1250#																		
GETPRI	1#	1250#																		
GETWOR	1#	1250#																		
GMANIA	1#	1250#																		
GMANID	1#	1250#																		
GMANIL	1#	1250#																		
GPHARD	1#	1250#	3091																	
GPRMA	1#	1250#	7239																	
GPRMD	1#	1250#	7233	7250																
GPRML	1#	1250#																		
HEADER	1#	1250#	1281																	
INLOOP	1#	1250#																		
IOSETU	1#	1250#																		
IOSTAR	1#	1250#																		
KT11	1#	1250#																		
K4ONLY	1775#	1814#	3778	5410	5491	5586	5774	5891	5965											
LASTAD	1#	1250#	7357																	
MACEX	1796#	3384	3434	3487	3908															
MACEX2	1805#	4102	4199	4301	4401	4502	4603	4703	4803	4905	5007	5108	5210	5311						
MANUAL	1#	1250#																		
MDTO	2333#	2776																		
MDT1	2313#	2376	2405																	
MDT2	2317#	2434																		
MDT3	2321#	2463	2491	2577	2661	2797	2825													
MDT4	2325#	2519																		
MDT5	2329#	2548																		
MDT6	2335#	2605	2689																	
MDT7	2339#	2633	2746																	
MDT8	2342#	2717																		
MEMORY	1#	1250#																		
MSTCLR	1861#	3325	3440	3494	3566	3627	3690	3785	3915	4008	4109	4206	4308	4408	4509					
	4609	4710	4809	4911	5013	5114	5216	5317	5416	5497	5590	5778	5895	5969	6038					
	6117	6128	6180	6193	6203	6224	6883	6949	7046	7106										
MYINT	1790#	3388	3438	3491	3563	3624	3687	3782	3912	4005	4106	4203	4305	4405	4506					
	4607	4707	4807	4909	5011	5112	5214	5315	5414	5495	5584	5772	5896	5970	6036					
	6114	6222	6450	6511	6582	6768	6829	6881	6947	6992	7044	7104								
MSBYTE	1#	1250#	1282#	1288	1289	1290														
MSCHEC	1#	1250#	3021#	3386#	3436#	3489#	3780#	3910#	4002#	4104#	4201#	4303#	4403#	4504#	4605#					
	4705#	4805#	4907#	5009#	5110#	5212#	5313#	5412#	5493#	5588#	5776#	5893#	5967#	6173#	6423#					
	6508#	6552#	6579#	6731#	6788#	6878#	6944#	7041#												
MSCNTO	1#	1250#	7234#	7240#	7251#															
MSCOUN	1#	1250#	2364#	2370#	2376#	2384#	2393#	2399#	2405#	2413#	2422#	2428#	2434#	2442#	2451#					
	2457#	2463#	2470#	2479#	2485#	2491#	2498#	2507#	2513#	2519#	2527#	2536#	2542#	2548#	2556#					
	2565#	2571#	2577#	2584#	2593#	2599#	2605#	2612#	2621#	2627#	2633#	2640#	2649#	2655#	2661#					
	2668#	2677#	2683#	2689#	2696#	2705#	2711#	2717#	2725#	2734#	2740#	2746#	2753#	2764#	2770#					
	2776#	2785#	2791#	2797#	2804#	2813#	2819#	2825#	2832#	2843#	2855#	2862#	2873#	2879#	2890#					
	2896#	2908#	2916#	2927#	2935#	2946#	2954#	2960#	2971#	2979#	2991#	2999#								
MSDATA	1#	1250#	1282#	1291	1293	1295	1297	1299	1301	1303	1305	1307	1309	1311	1313					
	1315	1317	1319	1321#	1323	1325	1328	1331	1333	1335	1337	1339	1341	1343	1345					
	1347	1349	1351	1353	1355	1357	1359	1361	1363	1365	1594#	1727#								
MSDECR	1#	1250#	1375#	1463#	1478#	2389#	2418#	2447#	2475#	2503#	2532#	2561#	2589#	2617#	2645#					
	2673#	2701#	2730#	2758#	2781#	2809#	2837#	2849#	2868#	2885#	2902#	2922#	2941#	2966#	2985#					
	3005#	3026#	3177#	3203#	3219#	3239#	3257#	3309#	3372#	3412#	3422#	3463#	3474#	3519#	3542#					
	3550#	3612#	3674#	3765#	3894#	3981#	4033#	4057#	4081#	4084#	4132#	4155#	4178#	4181#	4231#					
	4256#	4280#	4283#	4332#	4356#	4380#	4383#	4433#	4457#	4481#	4484#	4534#	4558#	4582#	4585#					
	4634#	4658#	4682#	4685#	4734#	4758#	4782#	4785#	4834#	4860#	4884#	4887#	4936#	4962#	4986#					

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	4989#	5037#	5063#	5087#	5090#	5138#	5164#	5188#	5191#	5240#	5266#	5290#	5293#	5341#	5367#
	5391#	5394#	5472#	5544#	5735#	5877#	5950#	6023#	6096#	6206#	6435#	6491#	6560#	6752#	6814#
	6860#	6923#	6974#	7020#	7087#	7214#	7257#	7347#							
MSDEFA	1#	1250#	7234#	7240#	7251#										
MSENDE	1#	1250#	1463#	1478#	2389#	2418#	2447#	2475#	2503#	2532#	2561#	2589#	2617#	2645#	2673#
	2701#	2730#	2758#	2781#	2809#	2837#	2849#	2868#	2885#	2902#	2922#	2941#	2966#	2985#	3005#
	3026#	3177#	3203#	3219#	3239#	3257#	3309#	3372#	3412#	3422#	3463#	3474#	3519#	3542#	3550#
	3612#	3674#	3765#	3894#	3981#	4033#	4057#	4081#	4084#	4132#	4155#	4178#	4181#	4231#	4256#
	4280#	4283#	4332#	4356#	4380#	4383#	4433#	4457#	4481#	4484#	4534#	4558#	4582#	4585#	4634#
	4658#	4682#	4685#	4734#	4758#	4782#	4785#	4834#	4860#	4884#	4887#	4930#	4962#	4986#	4989#
	5037#	5063#	5087#	5090#	5138#	5164#	5188#	5191#	5240#	5266#	5290#	5293#	5341#	5367#	5391#
	5394#	5472#	5544#	5735#	5877#	5950#	6023#	6096#	6206#	6435#	6491#	6560#	6752#	6814#	6860#
MSERRI	6923#	6974#	7020#	7087#	7214#	7257#	7347#								
	1#	1250#	3297#	3345#	3365#	3404#	3455#	3511#	3534#	3594#	3656#	3718#	3751#	3816#	3841#
	3888#	3933#	3956#	3975#	4025#	4049#	4073#	4124#	4147#	4170#	4222#	4247#	4272#	4324#	4348#
	4372#	4425#	4449#	4473#	4526#	4550#	4574#	4626#	4650#	4674#	4726#	4750#	4774#	4826#	4852#
	4876#	4928#	4954#	4978#	5029#	5055#	5079#	5130#	5156#	5180#	5232#	5258#	5282#	5333#	5359#
	5383#	5456#	5527#	5645#	5728#	5833#	5908#	5927#	5944#	5982#	6000#	6017#	6054#	6071#	6087#
	6130#	6152#	6165#	6182#	6195#	6333#	6364#	6386#	6412#	6484#	6539#	6629#	6644#	6659#	6673#
MSESCA	6689#	6701#	6713#	6725#	6807#	6838#	6852#	6908#	6966#	7013#	7079#	7134#	7158#	7181#	7204#
	1#	1250#	3288#	3289	3305#	3306	3351#	3352	3409#	3460#	3516#	3539#	3599#	3600	3661#
	3662	3723#	3724	3756#	3757	3849#	3850	3938#	3939	4030#	4054#	4078#	4129#	4152#	4175#
	4228#	4253#	4277#	4329#	4353#	4377#	4430#	4454#	4478#	4531#	4555#	4579#	4631#	4655#	4679#
	4731#	4755#	4779#	4831#	4857#	4881#	4933#	4959#	4983#	5034#	5060#	5084#	5135#	5161#	5185#
	5237#	5263#	5287#	5338#	5364#	5388#	5465#	5466	5535#	5536	5680#	5681	5868#	5869	5914#
	5915	5933#	5934	5988#	5989	6006#	6007	6338#	6339	6391#	6392	6417#	6418	6546#	6547
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CROSS REFERENCE TABLE -- MACRO NAMES

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CROSS REFERENCE TABLE -- MACRO NAMES

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CRSS REFERENCE TABLE -- MACRO NAMES

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4223	4224	4225	4247#	4248	4249	4250	4272#	4273	4274	4275	4303#	4324#	4325	4326	
4327	4348#	4349	4350	4351	4372#	4373	4374	4375	4403#	4425#	4426	4427	4428	4449#	

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CROSS REFERENCE TABLE -- MACRO NAMES

4450	4451	4452	4473#	4474	4475	4476	4504#	526#	4527	4528	4529	4550#	4551	4552	
4553	4574#	4575	4576	4577	4605#	4626#	4627	4628	4629	4650#	4651	4652	4653	4674#	
4675	4676	4677	4705#	4726#	4727	4728	4729	4750#	4751	4752	4753	4774#	4775	4776	
4777	4805#	4826#	4827	4828	4829	4852#	4853	4854	4855	4876#	4877	4878	4879	4907#	
4928#	4929	4930	4931	4954#	4955	4956	4957	4978#	4979	4980	4981	5009#	5029#	5030	
5031	5032	5055#	5056	5057	5058	5079#	5080	5081	5082	5110#	5130#	5131	5132	5133	
5156#	5157	5158	5159	5180#	5181	5182	5183	5212#	5232#	5233	5234	5235	5258#	5259	
5260	5261	5282#	5283	5284	5285	5313#	5333#	5334	5335	5336	5359#	5360	5361	5362	
5383#	5384	5385	5386	5412#	5456#	5457	5458	5459	5493#	5527#	5528	5529	5530	5588#	
5645#	5646	5647	5648	5728#	5729	5730	5731	5776#	5833#	5834	5835	5836	5893#	5908#	
5909	5910	5911	5927#	5928	5929	5930	5944#	5945	5946	5947	5967#	5982#	5983	5984	
5985	6000#	6001	6002	6003	6017#	6018	6019	6020	6054#	6055	6056	6057	6071#	6072	
6073	6074	6087#	6088	6089	6090	6130#	6131	6132	6133	6152#	6153	6154	6155	6165#	
6166	6167	6168	6173#	6182#	6183	6184	6185	6195#	6196	6197	6198	6333#	6334	6335	
6336	6364#	6365	6366	6367	6386#	6387	6388	6389	6412#	6413	6414	6415	6423#	6484#	
6485	6486	6487	6508#	6539#	6540	6541	6542	6552#	6579#	6629#	6630	6631	6632	6644#	
6645	6646	6647	6659#	6660	6661	6662	6673#	6674	6675	6676	6689#	6690	6691	6692	
6701#	6702	6703	6704	6713#	6714	6715	6716	6725#	6726	6727	6728	6731#	6788#	6807#	
6808	6809	6810	6838#	6839	6840	6841	6852#	6853	6854	6855	6878#	6908#	6909	6910	
6911	6944#	6966#	6967	6968	6969	7013#	7014	7015	7016	7041#	7079#	7080	7081	7082	
7134#	7135	7136	7137	7158#	7159	7160	7161	7181#	7182	7183	7184	7204#	7205	7206	
7207	7234#	7240#	7251#	7359	7360										
MSXFER	1#	1250#													
OPEN	1#	1250#													
POINTE	1#	1250#	1278												
POPSP2	1756#	6146													
PRINTB	1#	1250#	2364	2370	2376	2384	2393	2399	2405	2413	2422	2428	2434	2442	2451
	2457	2463	2470	2479	2485	2491	2498	2507	2513	2519	2527	2536	2542	2548	2556
	2565	2571	2577	2584	2593	2599	2605	2612	2621	2627	2633	2640	2649	2655	2661
	2668	2677	2683	2689	2696	2705	2711	2717	2725	2734	2740	2746	2753	2764	2770
	2776	2785	2791	2797	2804	2813	2819	2825	2832	2842	2861	2878	2895	2915	2934
	2953	2959	2978	2998											
PRINTF	1#	1250#	2854	2872	2889	2907	2926	2945	2970	2990					
PRINTS	1#	1250#													
PRINTX	1#	1250#													
READBU	1#	1250#													
READEF	1#	1250#	3056	3062	3068	3074									
RFLAGS	1#	1250#													
ROMCLK	1829#	1904	1907	1910	1920	1928	1936	1944	1952	1955	1958	1969	1992	1998	3330
	3333	3336	3354	3357	3573	3576	3580	3583	3586	3635	3638	3642	3645	3648	3697
	3700	3704	3707	3710	3734	3737	3740	3743	3789	3793	3795	3802	3806	3824	3828
	3868	3871	3874	3877	3917	3921	3941	3947	3960	3963	3966	5420	5423	5428	5444
	544X	5506	5509	5518	5612	5615	5622	5625	5704	5707	5710	5714	5800	5803	5810
	5813	5899	5917	5936	5973	5991	6009	6059	6229	6243	6247	6251	6265	6269	6273
	6280	6283	6287	6291	6295	6304	6307	6323	6356	6374	6378	6397	6400	6404	6452
	6455	6458	6461	6466	6470	6884	6887	6895	6899	6951	6955	6999	7006	7054	7058
	7061	7071	7112	7116	7119	7123	7145	7149	7168	7171	7195				
SETPRI	1#	1250#	7107												
SETVEC	1#	1250#													
SKIP04	1854#	3999													
SKIP06	1840#	1984	3503	3860	4838	4940	5041	5142	5244	5345	5636	5691	5824	6505	6576
SKIP07	1847#	1986	2009	2031	6875	6941	7038								
SLASH	1#	1250#													
SROMCL	1835#	1913	1961	1972	3808	3820	4014	4017	4038	4041	4062	4065	4113	4116	4136
	4139	4159	4162	4211	4214	4236	4239	4261	4264	4313	4316	4337	4340	4361	4364
	4414	4417	4438	4441	4462	4465	4515	4518	4539	4542	4563	4566	4615	4618	4639

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CROSS REFERENCE TABLE -- MACRO NAMES

	4642	4663	4666	4715	4718	4739	4742	4763	4766	4815	4818	4841	4844	4865	4868
	4917	4920	4943	4946	4967	4970	5018	5021	5044	5047	5068	5071	5119	5122	5145
	5148	5169	5172	5221	5224	5247	5250	5271	5274	5322	5325	5348	5351	5372	5375
	5512	5618	5806	6890											
STARS	1#	1250#													
SVC	1#	1248#	1249												
XFER	1#	1250#	3021#	3386#	3436#	3489#	3780#	3910#	4002#	4104#	4201#	4303#	4403#	4504#	4605#
	4705#	4805#	4907#	5009#	5110#	5212#	5313#	5412#	5493#	5588#	5776#	5893#	5967#	6173#	6423#
	6508#	6552#	6579#	6731#	6788#	6878#	6944#	7041#							
XFERF	1#	1250#													
XFERT	1#	1250#													
\$MD	2346#	2352	2391	2420	2449	2477	2505	2534	2563	2591	2619	2647	2675	2703	2732
	2762	2783	2811												

. ABS. 030144 000

ERRORS DETECTED: 0

CZDMQE.BIN,CZDMQE.SEQ/SOL/CRF/NL:TOC=SVC34R.MLB,CZDMQE.P11  
RUN-TIME: 40 49 5 SECONDS  
RUN-TIME RATIO: 300/95=3.1  
CORE USED: 21K (41 PAGES)