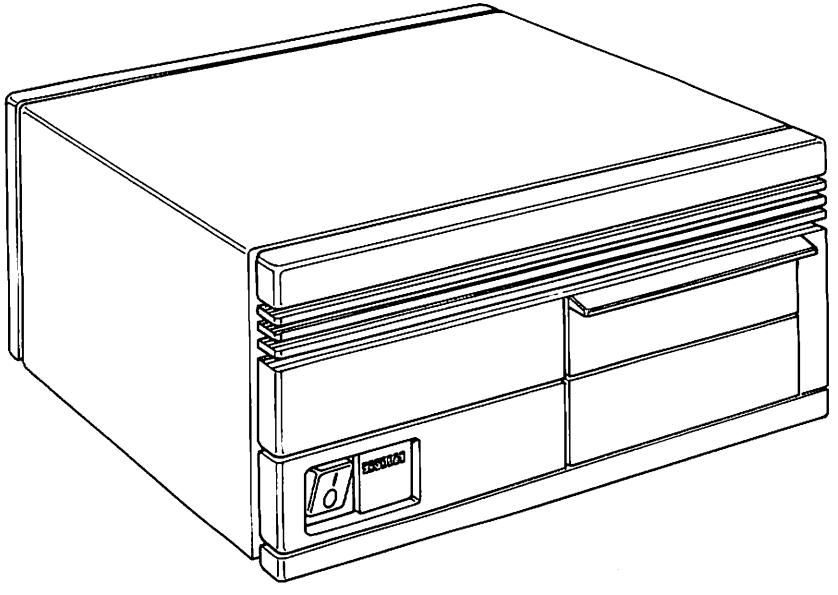
VAXstation 2000 and MicroVAX 2000 Technical Manual Addendum: DHT32 Asynchronous Serial Line Option

Order Number EK-ASYNC-IM-001



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Tables

1 Introduction

The DHT32 serial line option adds eight serial lines to the MicroVAX 2000 system. The serial lines are implemented with a DHU style interface and support data lead (no modem control) type serial lines.

The DHT32 option consists of a controller module, a driver/receiver module and cables.

2 Physical Description

This section describes the DHT32 option and tell how it interfaces with the MicroVAX 2000 system unit.

2.1 DHT32 Controller Module

The DHT32 controller module is a two-layer printed circuit board measuring 26.42 centimeters (10.4 inches) by 19.31 centimeters (7.6 inches), and weighing 297.67 grams (10.5 ounces). It connects to the MicroVAX 2000 system module by way of two 40-pin connectors (J3 and J4, on the DHT32 controller module connect to J8 and J11, respectively, on the system module). All power, ground, and data/address lines come through these connectors. In addition, there is a 34-pin connectors (J1) which connect to the driver/receiver module. The driver/receiver module receives its power and data lines through this connector, so the system module is actually supplying the power for the entire DHT32 option.

2.2 DHT32 Driver/Receiver Module

The DHT32 driver/receiver module is a four-layer printed circuit board measuring 8.13 centimeters (3.20 inches) by 13.21 centimeters (5.20 inches), and weighing 99.23 grams (3.5 ounces). It is mounted in the expansion adapter with a 34-pin ribbon cable that connects connector J2 (on the driver/receiver module) to the controller module's connector J1. Connector J1 on the driver/receiver module is used with an eight line cable concentrator to connect to terminals or other peripherals.

2.3 Electrical Characteristics

The power for the DHT32 controller module and the driver/receiver module is supplied by the MicroVAX 2000 system module through connectors J3 and J4 on the controller module. The controller module's power requirements are listed as follows.

- +12 volts at 700 mA maximum
- −12 volts at 120 mA maximum
- +5 volts at 1.5 A maximum

2.4 Environmental Specifications

The DHT32 asynchronous serial line option environmental specifications are listed in Table 1, Table 2, and Table 3. Refer to Table 1 for storage conditions, Table 2 for operating conditions, and Table 3 for nonoperating conditions.

Table 1: Storage Conditions

Parameter	Range
Temperature range	5 °C (41 °F) to 50 °C (122 °F)
Relative humidity	10% to 95% (noncondensing)
Maximum wet bulb temperature	32 °C (90 °F)
Maximum dew point	2 °C (36 °F)
Altitude	2400 m (8000 feet) at 36 °C (96 °F)

Table 2: Operating Conditions

Parameter	Range
Temperature range	10 °C (50 °F) to 40 °C (104 °F)
Temperature change rate	11 °C (20 °F) degree/hour maximum
Relative humidity	10% to 90% (noncondensing, no diskette)
	20% to 80% (diskette in use)
Maximum wet bulb temperature	28 °C (82 °F)
Minimum dew point	2 °C (36 °F)
Altitude	2400 m (8000 feet) at 36 °C (96 °F)
Heat dissipation	17.4 watts maximum

Table 3: Nonoperating Conditions

Parameter	Range
Temperature range	-40 °C (-40 °F) to 66 °C (151 °F)
Relative humidity	95% at 66 °C (151 °F) (may condense)
Maximum wet bulb temperature	28 °C (82 °F)
Minimum dew point	2 °C (36 °F)
Altitude	4900 m (16000 feet)

3 Controller Module Input/Output Connectors

Connectors J3 and J4 on the controller module share data/address lines, control lines, and several power and ground lines with connectors J8 and J11, respectively, on the system module. The signals on connectors J3 and J4 are listed in Table 4.

Table 4: Controller Module Connectors J3 and J4

Pin	Signal	Pin	Signal
J3-1	+5 volts	J4-1	GND
J3-2	+5 volts	J4-2	GND
J3-3	+12 volts	J4-3	BDAL31 H
J3-4	-12 volts	J4-4	BDAL30 H
J3-5	GND	J4-5	BDAL29 H
J3-6	BCLKO H	J4-6	BDAL28 H
J3-7	BRESET L	J4-7	BDAL27 H
J3-8	BVAS L	J4-8	BDAL26 H
J3-9	VDS L	J4-9	BDAL25 H
J3-10	BWRITE L	J4-10	BDAL24 H
J3-11	N/C	J4-11	BDAL23 H
J3-12	N/C	J4-12	BDAL22 H
J3-13	GND	J4-13	GND
J3-14	GND	J4-14	GND
J3-15	CAS3 L	J4-15	BDAL21 H
J3-16	CAS2 L	J4-16	BDAL20 H
J3-17	CAS1 L	J4-17	BDAL19 H
J3-18	CAS0 L	J4-18	BDAL18 H
J3-19	N/C	J4-19	BDAL17 H
J3-20	N/C	J4-20	BDAL16 H
J3-21	N/C	J4-21	BDAL15 H
J3-22	N/C	J4-22	BDAL14 H
J3-23	OPTROMENA L	J4-23	BDAL13 H

Table 4 (Cont.): Controller Module Connectors J3 and J4

Pin	Signal	Pin	Signal
J3-24	OPTVIDENA L	J4-24	BDAL12 H
J3-25	OPTIRQ L	J4-25	BDAL11 H
J3-26	OPTEOF L	J4-26	BDAL10 H
J3-27	GND	J4-27	GND
J3-28	GND	J4-28	GND
J3-29	INTENA L	J4-29	BDAL09 H
J3-30	SCYC/IAD2 H	J4-30	BDAL08 H
J3-31	DCYC/IAD1 H	J4-31	BDAL07 H
J3-32	STFH/IAD0 H	J4-32	BDAL06 H
J3-33	N/C	J4-33	BDAL05 H
J3-34	GND	J4-34	BDAL04 H
J3-35	N/C	J4-35	BDAL03 H
J3-36	GND	J4-36	BDAL02 H
J3-37	N/C	J4-37	BDAL01 H
J3-38	GND	J4-38	BDAL00 H
J3-39	OPT_PRESENT L	J4-39	GND
J3-40	+5 volts	J4-40	GND

Connector J1 on the controller module connects the controller module, channel numbers 0 through 7, to the driver/receiver module. Connector J2 is not used on this module. The signals on connector J1 are listed in Table 5.

Table 5: Controller Module Connector J1

Pin	Signal	Pin	Signal
J1-1	BSDO 7 H	J1-18	-12 volts
J1-2	+5 volts	J1-19	N/C
J1-3	BSDO 6 H	J1-20	BSDI 7 H
J1-4	GND	J1-21	GND
J1-5	BSDO 5 H	J1-22	BSDI 6 H
J1-6	GND	J1-23	GND
J1-7	BSDO 4 H	J1-24	BSDI 5 H
J1-8	GND	J1-25	GND
J1-9	BSDO 3 H	J1-26	BSDI 4 H
J1-10	GND	J1-27	GND
J1-11	BSDO 2 H	J1-28	BSDI 3 H
J1-12	GND	J1-29	GND
J1-13	BSDO 1 H	J1-30	BSDI 2 H
J1-14	GND	J1-31	GND
J1-15	BSDO 0 H	J1-32	BSDI 1 H
J1-16	+12 volts	J1-33	GND
J1-17	N/C	J1-34	BSDI 0 H

4 Functional Description

The functional description of the DHT32 option and its registers is described in the following sections.

4.1 Overview of the Controller Module

The DHT32 controller module implements a DHU compatible device on the MicroVAX 2000 system unit. The major features of the module are listed as follows.

- Eight data lead only serial lines at independent baud rates up to 38400 bits per second.
- Two hundred and fifty six character input FIFO buffer with programmable hold-off timer.
- Sixty four character per line output FIFO buffer.

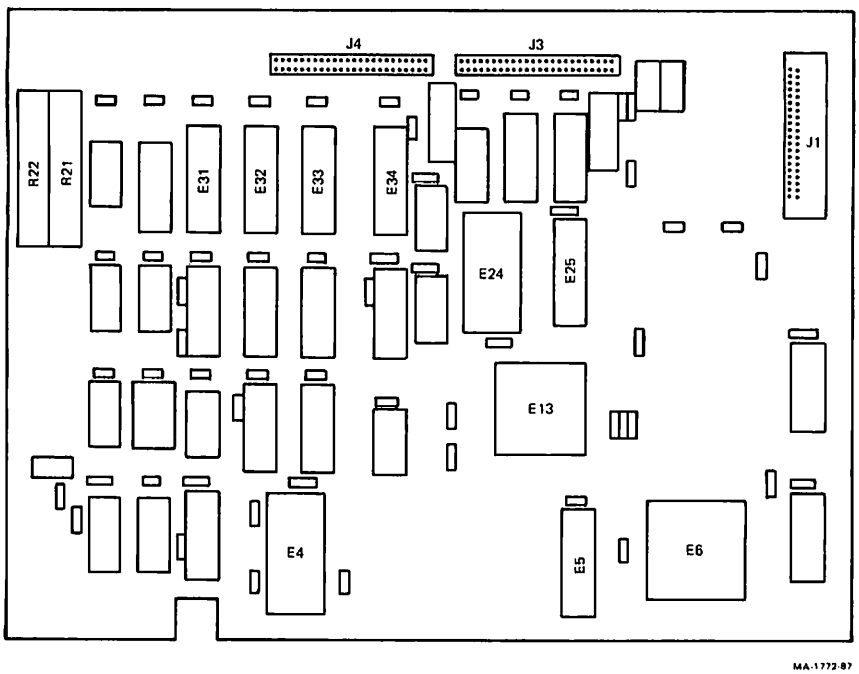
The major differences between the DHT32 controller module (DHU implemetation) and the other DHU-like products are listed below.

- The module has eight versus sixteen serial lines.
- The module has no output direct memory access (DMA) support.
- The module has no modem control.

These lines connect to terminals or other peripherals by way of a driver/receiver module mounted in the MicroVAX 2000 expansion adapter. The driver/receiver module converts TTL levels from the main controller to DEC423 levels for transmission outside of the enclosure. Passive devices for added electrostatic discharge (ESD) and electrical overstress (EOS) protection are also resident on this board.

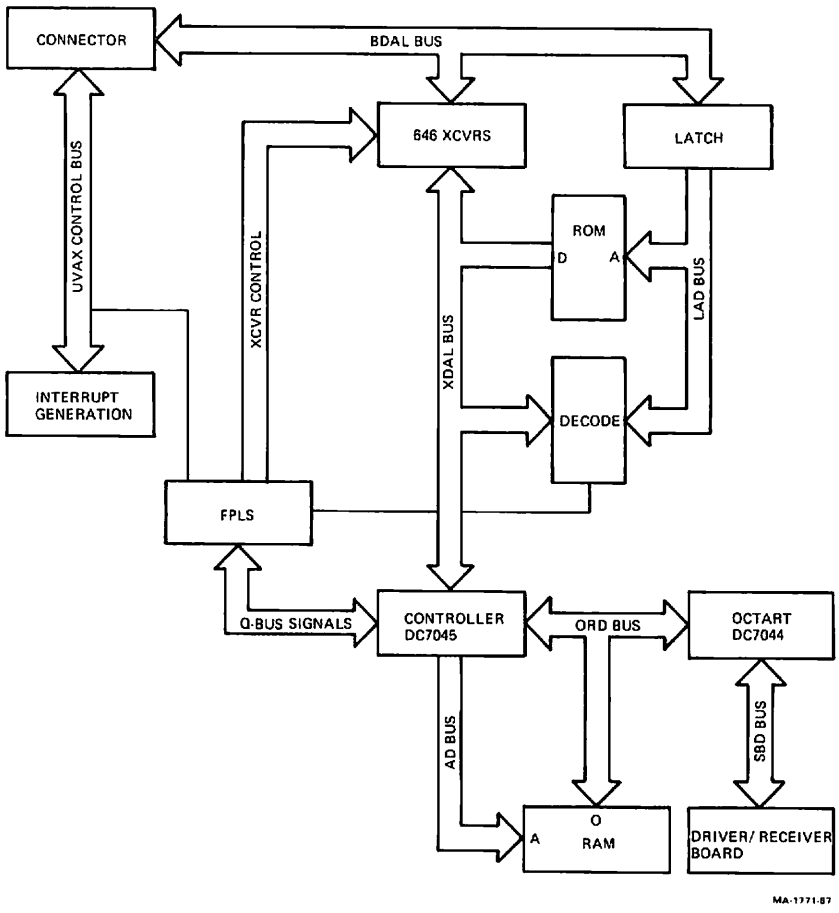
The controller module layout is shown in Figure 1.

Figure 1: DHT32 Controller Module Layout



A block diagram of the DHT32 option is shown in Figure 2.

Figure 2: DHT32 Option Block Diagram



4.2 Interrupts

The receiver interrupt is enabled by setting bit 0 in the video select register (VDCSEL). This bit selects the interrupt source for vector 244h as the DHT32 controller module. The other bits in this register should always be written to 0.

Two interrupts are used for program control of the DHT32 controller module. Refer to Table 6 below.

Table 6: Interrupts

Interrupt	Vector	Source Mask Bit
VF	244h	Receive FIFO not empty
VS	248h	Transmit FIFO empty

NOTE: *The video select register address is 2008.000E (hexadecimal).*

The receiver interrupt is qualified on the module by any value that was programmed into the hold-off timer for receive interrupts. This concept is explained in Section 4.4.

4.3 Registers

All registers on the controller module are word addressable. They should not be addressed as longwords. Table 7 briefly describes the registers.

Table 7: Registers

Register	CSR Address (hexadecimal)	Type
Control and status (SLU_CSR)	3800.0000	r/w*
Receive buffer (SLU_RBUF)	3800.0002	ro*
Receive timer (SLU_RTIM) † §	3800.0002	wo*
Line parameter (SLU_LPR) ‡	3800.0004	r/w
Transmit FIFO data (SLU_DATA) ‡	3800.0006	wo

*Read/write = r/w; write only = wo; read only = ro

§Able to be read/written as a single byte only or as part of the word it is in.

†Available only when SLU_CSR [0:3] equal 0.

‡A separate register is available for each line based on the value of SLU_CSR [0:3].

Table 7 (Cont.): Registers

Register	CSR Address (hexadecimal)	Type
Transmit FIFO size (SLU_DATA) ‡ §	3800.0006	wo
Line status (SLU_STAT) ‡ §	3800.0007	ro
Line control (SLU_CNTL) ‡	3800.0008	r/w
Not used ‡ ®	3800.000A	r/w
Transmit enable ‡	3800.000C	r/w
Not used ‡ ®	3800.000E	r/w

®Not used on this module. These registers are normally used to implement DMA output transfers and are listed here only because they appear in the address space.

§Able to be read/written as a single byte only or as part of the word it is in.

‡A separate register is available for each line based on the value of SLU_CSR [0:3].

Registers are accessed by instructions which use the register address as a source or destination. However, before multiple registers are accessed, the channel number should be written to the CSR address (3800.0000). For example the following I/O commands would be executed to read the line status register of channel number 3.

```
MOVB   #CHAN,@#CSR      ;WRITE CHANNEL NUMBER TO CSR
MOV    @#CSR+6,R0       ;READ THE LINE STATUS REGISTER
```

Example:

```
CHAN = 0er00011(b)

where
        e = the R.IE bit
        r = the RESET bit
  0011(b) = channel number 3
```

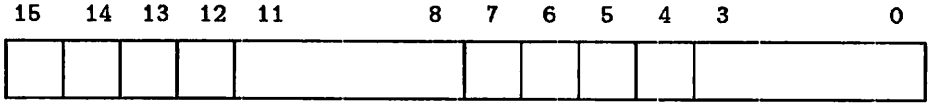
CSR + 6 addresses a block of 16 line status registers, only eight of which are used. The DHT32 hardware indexes this address by three, thereby selecting line status register of channel number 3.

4.4 Control And Status Register

Figure 3 shows the bits in the control and status register (SLU_CSR).

Figure 3: Control And Status Register

Address : 3800.0000



Data Bit	Definition
<15> (RO)	Tranmitter ready (T.RDY). Set this bit when a tranmit FIFO becomes empty. This bit is cleared by reading the register or setting the RESET bit.
<14> (RW)	Transmit interrupt enable (T.IE). When this bit is set, an interrupt is generated to the system at vector address 248h whenever the T.RDY bit becomes set. Clear by writing to 0. Setting the RESET bit has no effect on this bit.
<13> (RO)	Diagnostic failure (D.FAIL). When this bit is set and the RESET bit is clear, a failure has been detected by internal module diagnostics. The bit is set if the RESET bit is set and cleared after internal diagnostics have run successfully.
<12> (RO)	Not used. This bit is not used on the serial option card and should be ignored by system software.
<11:8> (RO)	Transmit line number (T.LINE). These bits hold the line number that caused the T.RDY bit to set. The bits are only valid while T.RDY is set. Clear by setting the RESET bit.
<7> (RO)	Receiver done (R.DON). This bit is set when receive FIFO data is available. This bit is set by setting the RESET bit since diagnostic information is left in the receive FIFO. This bit is only cleared when the FIFO is empty.
<6> (RW)	Receiver interrupt enable (R.IE). Setting this bit enables a receive interrupt to the system at vector address 244h. An interrupt occurs under the following conditions: • R.IE is set and a character is placed into an empty FIFO. • R.IE is changed from a 0 to a 1 while the FIFO is not empty.

Both of the above conditions are subject to the delay specified in the hold-off timer in register SLU_RTIM. The enable is cleared by writing to 0. Setting the RESET bit does not affect this bit.

Data Bit	Definition
<5> (RW)	Reset (RESET). Setting this bit causes the module to reset itself and run the internal diagnostics. The bit stays set while the diagnostics are running. This bit should not be written to a 1 when it is already set. Clear by completion of diagnostics. (See Section 5.3 for the status of all bits after a successful reset.)
<4> (RW)	Diagnostic skip (D.SKP). When this bit is set at the same time as the RESET bit, the reset and diagnostic time is shortened. This allows fast reseting of the module.
<3:0> (RW)	Line select number (L.SEL). This field is used to select which line the SLU_LPR, SLU_DATA, SLU_SIZE, SLU_STAT, and SLU_CNTL registers represent. Additionally, when these bits are all zero, the SLU_RTIM value may be set. Only lines zero through seven are valid on the serial option card. Any data written to registers outside that range cause unpredictable results.

NOTES: *To enable receive interrupts from the serial option card, bit 0 of the video select register (VDCSEL) should be set to 1.*

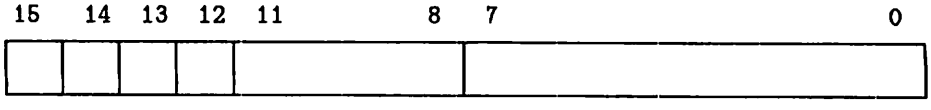
Since the state of the transmit ready bit is cleared on any read of the register, the software must use only word or byte write instructions and not read-modify-write instructions when accessing the register.

4.5 Receive Buffer Register

Figure 4 shows the bits in the receive buffer register (SLU_RBUF).

Figure 4: Receive Buffer Register

Address : 3800.0002



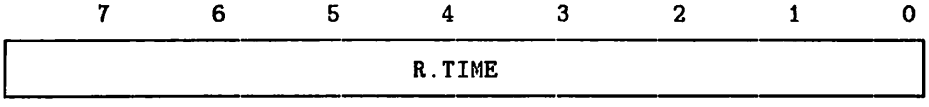
Data Bit	Definition
<15> (RO)	Data valid (D. VAL). This bit is set whenever the receive FIFO is not empty. The bit is set by RESET since diagnostic information is left in the FIFO.
<14> (RO)	Over-run error (O.ERR). This bit is set if a character is received on the indicated line (R.LINE) and the FIFO for that line if full or an error occured while receiving a character. If this bit is set along with F.ERR and P.ERR then the R.DATA field contains diagnostic information.
<13> (RO)	Framing error (F.ERR). This bit is set if there was a framing error (no stop) on receiving the character. If this bit is set along with O.ERR and P.ERR then the R.DATA field contains diagnostic information. A break detected on the indicated line appears as a framing error with a null (all zero) data field.
<12> (RO)	Parity error (P.ERR). This bit is set if parity is enabled for the line and the parity of the character received is incorrect. If this bit is set along with O.ERR and F.ERR then the R.DATA field contains diagnostic information.
<11:8> (RO)	Receive line (R.LINE). These bits form the binary value of the line number for which the data in the word is valid. (Even though there is room for 16 lines, only lines zero through seven are considered valid.)
<7:0> (RO)	Received data (R.DATA). These bits contain the data received for the indicated line. If the error bits (O.ERR, P.ERR and F.ERR) are all clear, then the data is valid. If any one of the bits are set, then the data is invalid due to the condition specified by that bit (with the exception of F.ERR; see that bit's documentation). If all the error bits are set, then the word contains diagnostic information in the R.DATA field. (See Section 5 for a description of the diagnostic codes.)

4.6 Receive Timer Register

Figure 5 shows the bits in the receive timer register (SLU_RTIM).

Figure 5: Receive Timer Register

Address : 3800.0002



Data Bit	Definition
<7:0> (WO)	Receiver time delay (R.TIME). When the L.SEL bits in SLU_CSR are all 0, a byte written to this address sets the value of an interrupt holdoff timer for receive character interrupts. The following table shows the various programmed values and the response of the option card.

The value is set to 1 by setting the RESET bit.

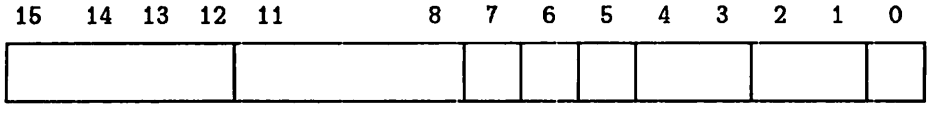
Value	Interrupt Requested
0	The receive FIFO becomes three quarters (48 characters full). This could take an infinite amount of time.
1	Immediate interrupt. The interrupt is requested as soon as the FIFO is not empty.
2 to 255	An interrupt is requested after the first character is received and the number of milliseconds equal to the value written have passed.

4.7 Line Parameter Register

The line parameter register (SLU_LPR) is used to program the characteristics for each of the eight lines of the DHT32 option. The line parameter register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 6 shows the bits in the line parameter register.

Figure 6: Line Parameter Register

Address : 3800.0004



<15:12> (RW) Transmit speed (T.SPEED). These bits are used to set the transmit speed of the selected line. See Table 8 for the baud rates that correspond to the values for the field. The field is set to 1101 (9600 baud) by setting the RESET bit.

<11:8> (RW) Receive speed (R.SPEED). These bits are used to set the receive speed of the selected line. See Table 8 for the baud rates that correspond to the values for the field. The field is set to 1101 (9600 baud) by setting the RESET bit.

<7> (RW) Stop code (S.CODE). This bit defines the length of the transmitted stop bit. If S.CODE is set to 0, then one stop bit is always sent. If S.CODE is set to 1, the two stop bits are sent for 6, 7, and 8-bit characters and one and one-half stop bits for 5-bit characters. Setting the RESET bit sets S.CODE to 0.

<6> (RW) Even parity select (E.PAR). This bit selects the sense of the character parity (if enabled by P.ENA). If set to 1, then even parity is expected. If set to 0, then odd parity is expected. Setting the RESET bit sets E.PAR to 0.

<5> (RW) Parity enable (P.ENA). This bit enables the detection and transmission of character parity. If set to 1, then parity is enabled for the line. If set to 0, parity is disabled for the line. Setting the RESET bit clears this bit.

<4:3> (RW) Character length (C.LEN). These bits define the number of bits that make up each character. The bits do not include the start, stop or parity bits. The following information shows the character length for each of the field settings.

Value	Bits Per Character
00	5
01	6
10	7
11	8

Setting the RESET bit causes this field to be set to 11 (8 bits per character).

Data Bit	Definition
<2:1> (RW)	Diagnostic control (DIAG). These bits control the state of the internal diagnostics on the option. If both bits are set to 0, then the background diagnostics only reports the status when an error is detected. If the bits are set to 01, then the background program runs and reports the status whether or not an error is detected. Once these bits are set to 01, no other bits should be changed in this register until that code is cleared to 0. See Section 5 for more information.
<0> (RW)	Disable XON and XOFF reporting (D.XRPT). This bit is used to control whether or not XON and XOFF characters are saved in the receive FIFO. If this bit is 0, then XON and XOFF characters are saved. If this bit is 1 and the transmit auto flow control (T.AUTO) bit in the line control register (SLU_CNTL) is set, then XON and XOFF characters are not saved in the FIFO. Setting the RESET bit clears this bit.

Table 8 defines the binary codes used to select the transmit and receive data rates for the controller module.

Table 8: Binary Codes Used to Select Baud Rates

Value	Baud Rate
0000	50
0001	75
0010	110
0011	134.5
0100	150
0101	300
0110	600

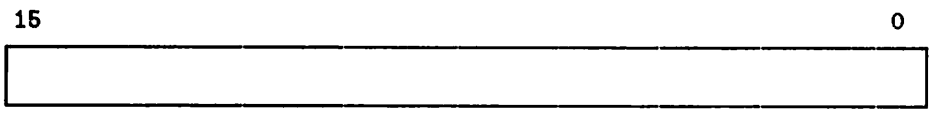
Table 8 (Cont.): Binary Codes Used to Select Baud Rates

Value	Baud Rate
0111	1200
1000	1800
1001	2000
1010	2400
1011	4800
1100	7200
1101	9600
1110	19200
1111	38400

4.8 Transmit FIFO Data Register

The Transmit FIFO data register (SLU_DATA) sends characters out the desired line. The Transmit FIFO data register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 7 shows the bits in the transmit FIFO data register.

Figure 7: Transmit FIFO Data Register

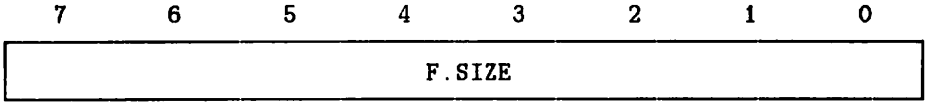


Data Bit	Definition
<15:0> (WO)	Transmit data (T.DATA). The transmit data field programs the data to be sent out the selected line. If a byte write is performed to the register, only the data in the low byte is placed in the transmit FIFO. If a word write is performed to the register, then two characters are placed in the FIFO. First the low byte is placed in the FIFO, then the high byte. Setting the RESET bit clears this register.

4.9 Transmit FIFO Size Register

The transmit FIFO size register (SLU_SIZE) is used to determine the amount of available space in the transmit FIFO for the selected line. The transmit FIFO size register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 8 shows the bits in the transmit FIFO size register.

Figure 8: Transmit FIFO Size Register



Data Bit	Definition
<7:0> (RO)	FIFO space available (F.SIZE). This field is used to indicate the number of entries left in the transmit FIFO for the selected line. The available size ranges from 0 to 64 characters. Setting the RESET bit sets this field to 40h (64 entries are available).

4.10 Line Status Register

The line status register (SLU_STAT) is used to read the status of the modem control signals on the module. While modem control is not used, the status bits are set to indicate to DHU compatible software that no modem control exists. This register must be read (as a word) along with the FIFO size register. It is documented here at its byte position.

The line status register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 9 shows the bits in the line status register.

Figure 9: Line Status Register

Address : 3800.0007

7	6	5	4	3	2	1	0
DSR	0	RI	DCD	CTS	0	M.STA	1

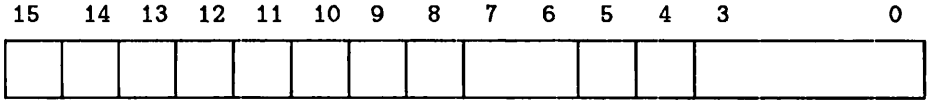
Data Bit	Definition
<7> (R0)	Data set ready (DSR) bit. Not implemented. Always read as 0.
<6> (R0)	Not implemented. Always read as 0.
<5> (R0)	Ring indicator (RI) bit. Not implemented. Always read as 0.
<4> (R0)	Data carrier detect (DCD) bit. Not implemented. Always read as 0.
<3> (R0)	Clear to send (CTS) bit. Not implemented. Always read as 0.
<2> (R0)	Not implemented. Always read as 0.
<1> (R0)	Modem status (M.STAT) bit. This bit is used to indicate if modem support is available for the selected line. No modem support is available at all on the option so this bit will always read as 1.
<0> (R0)	Not implemented. Always read as 1.

4.11 Line Control Register

The line control register (SLU_CNTL) is used to control miscellaneous line interface functions. The line control register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 10 shows the bits in the line control register.

Figure 10: Line Control Register

Address : 3800.0008



Data Bit	Definition
<15> (RO)	Not implemented. Always read as 0.
<14> (RO)	Not implemented. Always read as 0.
<13> (RO)	Not implemented. Always read as 0.
<12> (RW)	Request to send (RTS) bit. Not used on module. Setting or clearing this bit has no effect.
<11> (RO)	Not implemented. Always read as 0.
<10> (RO)	Not implemented. Always read as 0.
<9> (RW)	Data terminal ready (DTR) bit. Not used on module. Setting or clearing this bit has no effect.
<8> (RW)	Link type (L.TYPE). This bit is used to inform the controller module of a modem attached to the selected line. Since modem control is not supported on the DHT32 option, this bit should always be left cleared. Setting the bit should have no effect on the controller function.
<7:6> (RW)	Maintainance mode (MAINT). These bits are used to control the maintainance features incorporated into the module. A 2-bit value is used to place the module in one of four operating states. The values and the corresponding states are as follows.

Value	Operating State
00	Normal operating state.
01	Automatic echo mode. The data received on the selected line is sent back out the corresponding transmit line (even if T.ENA is cleared). The normal internal receive/transmit path is used and the characters are saved in the receive FIFO. The receive line must be enabled and no data placed into the FIFO by the user is transmitted. The baud rate selected for the receiver is used for both transmit and receive.
10	Local loopback. The data sent out the transmit channel is looped back to the receive channel even if the receiver enable is clear. The transmitter enable must be set (T.ENA), any data received at this time is ignored, and the output line is held in the mark condition. The baud rate selected for the transmitter is used for both transmit and receive.
11	Remote loopback. The data received is retransmitted at the receiving baud rate. The data is not saved in the FIFO and the transmit enable is ignored. The receive enable must be set.

Setting the RESET bit causes these bits to be set to 00 (normal operating mode).

Data Bit	Definition
<5> (RW)	Force transmit XOFF (F.XOFF). This bit is used to send an XOFF before any other character in the FIFO. If this bit stays set, an XOFF is sent after every other character received on that line. When the bit is cleared (after being set), an XON character is sent unless the receiver auto flow control (R.AUTO) is enabled and the FIFO is three-quarters full.
<4> (RW)	Tranmitter auto flow control (T.AUTO). This bit is used to control the controller module's response to valid flow control characters received on a line. When the bit is set, a received XOFF character causes the transmisson to stop until an XON character is received. The T.ENA bit is actually cleared and set by this action so host software can override this action. To completely disable a channel both this bit and the T.ENA bit must be cleared. Setting the RESET bit causes this bit to clear.
<3> (RW)	Transmit break (BREAK). This bit is used to assert a break condition on the selected channel. The condition is held until the bit is cleared. Setting the RESET bit causes this bit to clear.

Data Bit	Definition
<2> (RW)	Receive line enable (R.ENA). This bit is used to enable and disable the receiving of data on the selected line. This bit is set to enable a line. Setting the RESET bit clears this bit.
<1> (RW)	Receiver auto flow control (R.AUTO). This bit is used to control the flow of characters into the receive FIFO. An XOFF character is sent to any line that has this bit set when the receive FIFO become three-quarters full. An XON character is then sent when the FIFO becomes less than half full. Setting the RESET bit clears this bit.
<0> (RW)	Transmit abort (T.ABT). This bit is used to flush all characters from the transmit FIFO for a line. A few characters may be sent after the bit is set. When the FIFO is cleared, the T.RDY bit is set and, if enabled, an interrupt is requested. Setting the RESET bit clears this bit.

4.12 Transmit Enable Register

The transmit enable register (SLU_TXA) is used to enable data transmission on the selected line. Extreme care must be taken when setting the enable bit in this register. While the other bits in the register are not used, setting certain bits could hang up the controller module. Only the most significant bit of this register should ever be changed.

The transmit enable register for the appropriate line can be selected by setting the line value in the L.SEL field of the control and status register. Figure 11 shows the bits in the transmit enable register.

Figure 11: Transmit Enable Register

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Address : 3800.000C
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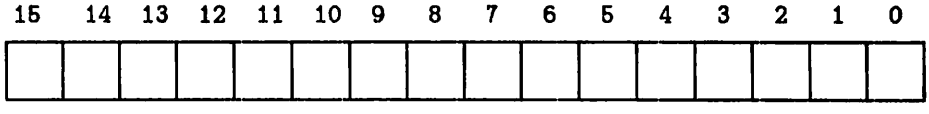

Data Bit	Definition
<15> (RW)	Transmitter enable (T.ENA). This bit is used to enable and disable the transmission of characters on the selected line. When this bit is set, the controller module transmits all characters placed in the FIFO. When cleared, the controller module only transmits flow control characters that are generated by the controller module (if enabled by the user). To completely stop character transmission on a line, both the T.AUTO bit and the T.ENA bit should be cleared. Setting the RESET bit sets this bit.
<14:8> (RO)	Not implemented. Always read as 0.
<7> (RW)	Do not set. Setting this bit hangs up the controller module. Setting the RESET bit clears the bit.
<6> (RO)	Not implemented. Always read as 0.
<5:0> (RO)	Not used. Always set to 0.

5 Internal Diagnostics

The DHT32 option has two levels of internal diagnostics: self-test and background test.

5.1 Self-Test

The DHT32 option self-test runs when the system powers-up and each time the RESET bit is set without the D.SKP bit being set. The diagnostic leaves 8 bytes of data in the receive FIFO. When the reset bit is cleared by the option and the T.RDY bit is set, the D.FAIL bit indicates whether any of the data bytes in the FIFO contain error information. After setting the RESET bit, the user waits for the bit to clear before doing anything else with the option.

The self-test can take up to two seconds to run. The user should not manipulate the option in any way during this time.

5.1.1 Self-Test Codes

The 8 data bytes that we referred to in Section 5.1 are placed in the FIFO. The line number field (R.LINE) is used to determine the sequence of the byte. Sequence numbers 0 through 7 are returned in the FIFO along with the following possible error codes in the data field (R.DATA). The self-test error codes are referenced in Table 9.

Table 9: Self-Test Error Codes

Octal Code	Hex Code	Definition
201	81	Self-test null (filler byte)
203	83	Self-test skipped
211	89	Low octart error
213	8B	High octart error
225	95	RAM error

When the test is complete, 6 data bytes and 2 bytes of ROM version code are left in the FIFO. Null codes are used whenever there is no error to report. An error-free test returns six null codes and two version bytes. If the test is skipped, six test skipped codes are returned instead of the null codes.

5.2 Background Test

A background test program continuously runs in the DHT32 option. If an error is detected, the octal code 307 is placed in the FIFO along with the setting of all the error bits (O.ERR, F.ERR, and P.ERR) and the clearing of the line number field (R.LINE). If all the error bits are set the software signals that a problem exists with the module.

The user can cause the background test to explicitly place a code into the receive FIFO by setting the diagnostic bit (DIAG). When the test is complete, the DIAG bit is cleared and either the octal code 307 is placed in the FIFO to indicate an error or the octal code 305 is placed in the FIFO to indicate normal operation.

5.3 Reset State

This section summarizes the reset information that is available individually for each of the sections above. After system power-up or setting the RESET bit (and waiting for it to clear), a successful (no errors detected) reset leaves the controller module in the following state.

- Eight bytes of diagnostic data are in the FIFO.
- The diagnostic failure bit is clear.
- The transmit baud rate for each line is set to 9600 and is enabled.
- The receive baud rate for each line is set to 9600 and is disabled.
- Each line is set for 8 data bits, one stop bit, and odd parity but with parity disabled.
- Transmit and receive auto flow control are disabled for all lines.
- Normal operational mode is set in the maintainance bits.
- No space (break) condition is asserted on any line.

5.4 ROM Option

The ROM option for the DHT32 controller module resides in address range 2014.0000 to 2015.FFFC (hexadecimal).