DataGeneral

TECHNICAL STATEMENT

LISTING

068-001662-00

PROGRAM

CS30 LOGIC TEST

TAPE

097-001662-00

ABSTRACT

THE CS30 LOGIC TEST IS A MAINTENANCE PROGRAM DESIGNED TO TEST THE MICRONOVA CPU. IT IS A FUNCTIONAL TEST OF THE LOGIC USED TO IMPLEMENT THE MICRONOVA INSTRUCTION SET.

NOTICE

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01
02
03
04
05              ;*****************************************************************
06              ;
07              ; NAME: CS30LGCT.TX                        PART NUMBER: 097-001662
08              ;
09              ;
10              ; DESCRIPTION: CS30 LOGIC TEST
11              ;
12              ; REVISION HISTORY:
13              ;
14              ;       REV.            DATE
15              ;       00              04/13/79
16              ;
17              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1979
18              ; ALL RIGHTS RESERVED.
19              ;*****************************************************************
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01
02              ;1.     PROGRAM NAME
03              ;       CS30LGCT.SR
04              ;
05              ;2.     REVISION HISTORY
06              ;       REV.            DATE            COMMENT
07              ;
08              ;2.1    00              04/13/79        ORIGINAL RELEASE
09              ;
10              ;3.     MACHINE REQUIREMENTS (MINIMUM)
11              ;3.1            MICRO NOVA PROCESSOR
12              ;3.2            4K READ/WRITE MEMORY
13              ;3.3            CONSOLE DEVICE
14              ;3.4            DISKETTE DRIVE OR PAPER TAPE READER
15              ;
16              ;4.     TEST REQUIREMENTS (MAXIMUM)
17              ;4.1            602 MICRONOVA PROCESSOR (MAXIMUM
18              ;               CONFIGURATION)
19              ;4.2            4K USER RAM & 47(OCTAL) WORDS MAPPED RAM.
20              ;4.3            CONSOLE DEVICE
21              ;4.4            DISKETTE DRIVE
22              ;
23              ;5.     SUMMARY
24              ;5.1            THE CS30 LOGIC TEST IS A MAINTENANCE
25              ;               PROGRAM DESIGNED TO TEST THE MICRO NOVA
26              ;               CENTRAL PROCESSING UNIT.  IT IS A FUNCTIONAL
27              ;               TEST OF THE LOGIC USED TO IMPLEMENT THE
28              ;               MICRO NOVA INSTRUCTION SET.  INCLUDED ALSO
29              ;               IS A MINIMUM LEVEL TEST OF THE CPU
30              ;               I/O INSTRUCTIONS, TELETYPE I/O, AND
31              ;               PROGRAM INTERRUPT.
32              ;
33              ;6.     RESTRICTIONS
34              ;6.1            IF A MICRO NOVA 602 IS UNDER TEST
35              ;               AND THERE IS NOT ENOUGH MAPPED
36              ;               MEMORY (47 OCTAL LOCATIONS) TO TEST
37              ;               TRAP INSTRUCTIONS, THOSE INSTRUCTIONS
38              ;               WILL NOT BE TESTED WITHOUT OPERATOR
39              ;               INTERVENTION (SEE PARA 11.6.6).
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!0003 .MAIN
01                      ;
02                      ;7.     PROGRAM DESCRIPTION/THEORY OF OPERATION.
03                      ;7.1            THIS PROGRAM IS A COLLECTION OF SMALL
04                      ;               TESTS, EACH TEST IN SEQUENCE BASED
05                      ;               ON PREVIOUS TESTS WORKING AND
06                      ;               DESIGNED TO TEST AS SMALL AN
07                      ;               ADDITIONAL PIECE OF THE LOGIC AS
08                      ;               POSSIBLE.  AFTER THE ENTIRE INSTRUCTION
09                      ;               SET HAS BEEN VERIFIED SPECIALLY DESIGNED
10                      ;               TESTS ARE PERFORMED TO CHECK
11                      ;               IDIOSYNCRACIES OF THE MICRO NOVA PROCESSOR.
12                      ;
13                      ;8.     OPERATING MODES/SWITCH SETTINGS.
14                      ;
15                      ;9.     OPERATING PROCEDURE/OPERATOR INPUT
16                      ;9.1            VERIFY THAT THE MICRO NOVA WILL PERFORM
17                      ;               ALL CONSOLE FUNCTIONS. (I.E. EXAMINE/
18                      ;               EXAMINE NEXT, DEPOSIT/DEPOSIT NEXT,
19                      ;               EXAMINE/DEPOSIT AC'S.)
20                      ;9.2            LOAD THE TEST PROGRAM VIA THE BINARY
21                      ;               LOADER OR DIAGNOSTIC OPERATING SYSTEM.
22                      ;9.3            NORMAL STARTING ADDRESS IS 200.
23                      ;9.4            OPTIONAL STARTING ADDRESSES ARE:
24                      ;               170     START WITHOUT CAT/KITTEN
25                      ;               171     START WITH CAT/KITTEN (CAT/KITTEN
26                      ;                       MUST HAVE BEEN PREVIOUSLY LOADED.)
27                      ;9.5            IF NOT AN AUTO-START FROM DIAGNOSTIC
28                      ;               OPERATING SYSTEM THE MACHINE SHOULD
29                      ;               HALT AT LOCATION 503.  THIS VERIFIES
30                      ;               CPU CAN HALT IF THERE IS AN
31                      ;               ERROR.  PROCEED BY TYPING A "P".
32                      ;               PROCESSOR SHOULD CONTINUE TO RUN
33                      ;               WITHOUT HALTING.
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!0004 .MAIN
01                      ;
02                      ;10.    PROGRAM OUTPUT/ERROR DESCRIPTION.
03                      ;10.1           MICRO NOVA 601 CPU OUTPUTS 60
04                      ;               "RUBOUTS" THEN PRINTS "PASS" FOR
05                      ;               THE INITIAL RUN.  THE TEST SHOULD
06                      ;               CONTINUE TO LOOP WITH THE OUTPUTS
07                      ;               AT A SLOWER RATE.
08                      ;10.2           MICRO NOVA 602 CPU OUTPUTS
09                      ;               THE PRINTOUT OF "PASS"  AND
10                      ;               60 "RUBOUTS" ENSUE.
11                      ;10.3           IF CAT/KITTEN IS RUNNING WITH THE
12                      ;               PROGRAM AN "S", INDICATING START, WILL
13                      ;               BE OUTPUTTED AFTER THE INITIAL PASS
14                      ;               IS COMPLETE.  PERIODICALLY A "P" WILL BE
15                      ;               OUTPUTTED INDICATING THAT THE CAT/KITTEN
16                      ;               TEST IS PASSING.
17                      ;               NOTE: MAP AND I/O INTERRUPT TESTING IS
18                      ;               NOT PERFORMED WHILE CAT/KITTEN IS RUNNING.
19                      ;10.4           DETECTED ERRORS WILL CAUSE THE
20                      ;               PROGRAM TO DO A PROCESSOR HALT.
21                      ;
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!0005 .MAIN
01              ;11.    DEBUG HELP
02              ;11.1           RECORD THE STATE OF THE PROCESSOR AND
03              ;               REGISTERS AT THE TIME THE HALT OCCURS.
04              ;               CONSULT THE LISTING AT THE ADDRESS OF
05              ;               THE ERROR HALT FOR PROBABLE CAUSES
06              ;               OF THE FAILURE.
07              ;11.2           CONSTRUCT A LOOP THAT WILL REPEAT THE
08              ;               FAILURE AND SCOPE AS REQUIRED.
09              ;11.3           THE SUBTEST COUNTER
10              ;               AT LOCATION TSN?M SHOULD BE EXAMINED
11              ;               FOR POSSIBLE PROGRAM FLOW ERRORS.
12              ;11.4           MACROS USED IN THIS PROGRAM WITH
13              ;               THEIR FUNCTION ARE:
14              ;11.4.1                 CHANGE - JSR TO CHNG IF NOT FIRST PASS.
15              ;11.4.2                 ADDTO - BIT ADD OPERATION
16              ;11.4.3                 LDATI - LOAD ACCUMULATOR COMBINATIONS
17              ;11.4.4                 SWPTS - SWAP FUNCTION
18              ;11.4.5                 STTST - MOVE TO AND FROM STACK
19              ;11.4.6                 PSPT - PUSH AND POP ACCUMULATORS
20              ;11.4.7                 IOTS1 - DIA AC,CPU & DIB AC,CPU
21              ;11.4.8                 IOTS2 - FALSE DEVICE CODES
22              ;11.5           SUBROUTINES USED IN THIS PROGRAM WITH
23              ;               THEIR FUNCTIONS ARE:
24              ;11.5.1                 CHNG - MODIFY SOURCE AND DESTINATION OF
25              ;                              SPECIFIED ALC INSTRUCTIONS.
26              ;11.5.2                 ENTER AND CYCLE - SUBTEST ITERATION
27              ;                                         CONTROL
28              ;11.5.3                 MPLD - LOADS SPECIFIED INSTRUCTIONS INTO
29              ;                              MAPPED RAM
30              ;11.6           SEQUENCE OF TESTING AND PROGRAM FLOW.
31              ;11.6.1                 BASIC ARITHMETIC AND LOGIC INSTRUCTIONS
32              ;                       ARE BUILT UPON TO FULLY TEST SKIPS,
33              ;                       SHIFTS, CARRY, AND NO LOADS.
34              ;                       THE ORDER OF TESTING IS ADC, COM,
35              ;                       MOV, ADD, AND, INC, NEG, SUB.
36              ;11.6.2                 BASIC MEMORY REFERENCE INSTRUCTIONS ARE
37              ;                       TESTED THEN BUILT UPON TO INCLUDE
38              ;                       VARIOUS INDEX AND INDIRECTS.
39              ;                       THE ORDER OF TESTING IS LDA, STA,
40              ;                       ISZ, DSZ, JMP, AND JSR INSTRUCTIONS.
41              ;11.6.3                 VARIOUS INDEX, INDIRECT, AUTO INC/DEC,
42              ;                       AND INDIRECT AND AUTO INC/DEC CHAINS.
43              ;11.6.4                 STACK OPERATIONS ARE THEN TESTED,
44              ;                       MOVE TO AND FROM STACK AND FRAME
45              ;                       POINTERS, POP AND PUSH ACCUMULATORS,
46              ;                       SAVE, RETURN, STACK OVERFLOW.
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!0006 .MAIN
01              ;11.6.5                 REAL TIME CLOCK IS TESTED AND
02              ;                       IT IS DETERMINED HERE IF A 602
03              ;                       PROCESSOR IS UNDER TEST.  IF A 601
04              ;                       IS BEING TESTED THEN THE "TRPSW" IS
05              ;                       CLEARED.
06              ;11.6.6                 THE "TRPSW" IS EXAMINED FOR A 0 OR 1
07              ;                       TO ALLOW EXECUTION OF TRAP INSTRUCTIONS.
08              ;                       NOTE: WHEN PIN 2 OF A 602 IS NOT SELECT-
09              ;                       ED AND THERE IS NOT ENOUGH MAPPED RAM
10              ;                       TO TEST TRAPS (OUTPUT "B") A LOOP SHOULD
11              ;                       BE CONSTRUCTED AND THESE TESTS SHOULD
12              ;                       BE RUN SEPARATELY.
13              ;11.6.7                 CONSTANT MULTIPLY/DIVIDE ARE FOLLOWED
14              ;                       BY 100 ITERATIONS OF RANDOM TESTS.
15              ;11.6.8                 FIRST PASS THROUGH LOGIC TESTS IS
16              ;                       ACKNOWLEDGED AND THE PREM MACRO
17              ;                       IS CALL TO SIZE MEMORY, SET UP
18              ;                       POINTERS TO I/O MODULE & CAT/KITTEN,
19              ;                       CHECK MODE OF OPERATION & SET PROPER
20              ;                       STATUS BITS.
21              ;11.6.9                 KATSW IS NOW EXAMINED TO DETERMINE
22              ;                       IF I/O AND MAP TESTS ARE OMITTED TO
23              ;                       ALLOW CAT/KITTEN TO RUN PROPERLY.
24              ;                       IF THE ENTIRE PROGRAM HAS COMPLETED
25              ;                       ONE PASS AND KATSW IS LOADED THEN
26              ;                       THE LOGIC TESTS WILL BE REPEATED WHILE
27              ;                       CAT/KITTEN IS RUNNING.
28              ;11.6.10                CPU AND I/O INSTRUCTIONS ARE NOW
29              ;                       TESTED.  CPU SKIPS, NIO, READS, INTA,
30              ;                       MSKO, INTEN, DEVICE CODES, MNRST.
31              ;11.6.11                TTO IS SIZED FOR AND, IF THERE,
32              ;                       THE INTERRUPT HANDLER FUNCTIONS
33              ;                       TESTED ARE MSKO, INTEN, INTA, INTDS.
34              ;11.6.12                MAIN PROGRAM IS NOW COMPLETE.
35              ;                       THE POS?T MACRO IS CONSULTED
36              ;                       TO DETERMINE IF SIXTY PASSES HAVE
37              ;                       BEEN ACCOMPLISHED.  IF NOT THEN THE
38              ;                       PROGRAM IS RESTARTED.  IF SUFFICIENT
39              ;                       PASSES HAVE BEEN COMPLETED THEN DEPENDING
40              ;                       ON THE TRPSW A SPECIAL SKIP TEST
41              ;                       AND THE PRINT OUT OF "PASS" IS
42              ;                       EXECUTED NOW OR AFTER MAP INSTRUCTION
43              ;                       ARE TESTED.
44              ;11.6.13                IF 602 IS DISCOVERED WITH MAXIMUM
45              ;                       CONFIGURATION THEN MAP INSTRUCTIONS
46              ;                       TESTED ARE MAP CHANGE PENDING (MAP 1)
47              ;                       WITH LDA, STA, JMP, & JSR.
48              ;                       BREAKPOINT (MAP 0), RESET (MAP 2), SKIP
49              ;                       ON DEVICE CODE 01, INTERRUPTS, MAP TRAP,
50              ;                       ECLIPSE VECTOR (DIBP 0,CPU), REAL
51              ;                       TIME CLOCK, AND MNRST IN MAP.
52              ;                       REFER TO PARAGRAPH 10.2 FOR THE
53              ;                       APPROPRIATE OUTPUTS OF THESE TESTS.
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!0007 .MAIN
01                ;11.6.14                A CARRIAGE RETURN AND "PASS" IS
02                ;                       NOW PRINTED TO THE CONSOLE.  VARIOUS
03                ;                       WAIT LOOPS IN THE TTO AND XOR'S
04                ;                       ARE PERFORMED.
05                ;11.6.15                DTOS IS NOW MONITORED TO DETERMINE IF
06                ;                       CAT/KITTEN SHOULD BE STARTED, OR IF
07                ;                       SUFFICIENT PASSES HAVE BEEN COMPLETED
08                ;                       TO SATISFY ITS REQUIREMENT.
09                ;
10                ;12.     SPECIAL NOTES/SPECIAL FEATURES.
11                ;12.1           IF THE PROGRAM WAS LOADED FROM
12                ;               DTOS WITH CAT/KITTEN IT WILL
13                ;               RUN IT IN THE BACKGROUND AFTER
14                ;               ONE PASS OF USING THE TTY
15                ;               INTERRUPTS.  THE PROGRAM WILL RUN
16                ;               MUCH SLOWER ALLOWING THE CAT/KITTEN
17                ;               AMPLE TIME TO COMPLETE A PASS.
18                ;12.2           AFTER THE INITIAL PASS THROUGH THE
19                ;               LOGIC TESTS THE SOURCE AND DESTINATION
20                ;               OF SOME ALC AND TRAP INSTRUCTIONS
21                ;               ARE CONTINUOUSLY INCREMENTED TO TEST
22                ;               ALL COMBINATIONS.  THEREFORE SOME CODE
23                ;               MAY NOT MATCH THE LISTING.  CONSULT
24                ;               THE MICRONOVA INSTRUCTION REFERENCE CARD FOR
25                ;               PROPER INTERPRETATION OF THESE INSTRUCTIONS.
26                ;
27                ;13.     RUNTIME
28                ;13.1           THE APPROXIMATE RUNTIME FOR THE FIRST
29                ;               TWO PASSES WITH 601 CPU = 1 MIN 40 SEC,
30                ;               602 CPU = 1 MIN 10 SEC.
31                ;13.2           THE APPROXIMATE TIME FOR COMPLETION OF THE
32                ;               FIRST CAT/KITTEN PASS WITH 601 CPU = 3 MIN
33                ;               30 SEC, 602 CPU = 3 MIN 20 SEC.

**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
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