PRELIMINARY

Diablo Systems Incorporated

Series 10 Flexible · Disk Drive

Model 12

Maintenance Manual

81803P APRIL 1976

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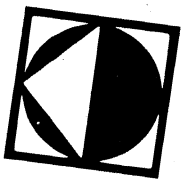

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WARRANTY

The Diablo Series 10, Model 12 Flexible-Disk Drive is warranted against defects in materials and workmanship for 1 year from the date of shipment. Any questions with respect to the warranty should be taken up with your Diablo Sales Representative.

All requests for repairs should be directed to the Diablo Repair Depot in your area. This will assure you the fastest possible service.

PREFACE

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Publication No. 81803P – First Edition

Printed in the U.S.A.

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SECTION 1

GENERAL INFORMATION

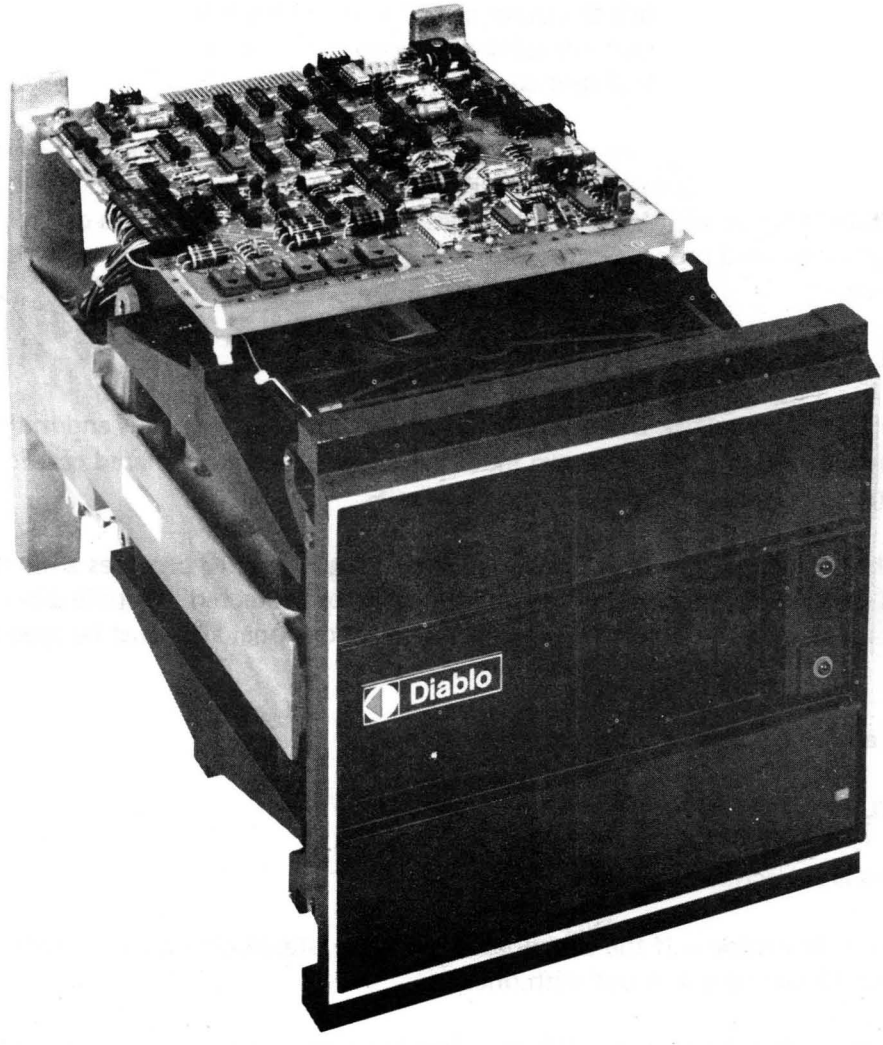


Figure 1-1 MODEL 12 FLEXIBLE-DISK DRIVE

1.1 INTRODUCTION

The Diablo Series 10, Model 12 Flexible-Disk Drive is a compact, reliable direct access storage device utilizing two interchangeable flexible-disk cartridges as storage media. Data is magnetically recorded on and read from the ferro-oxide surfaces of the disk cartridges. Up to 3.1 million bits of data may be stored on the recording surfaces of either flexible disk, providing a total on-line storage capacity of 6.2 million bits with a data transfer rate of 250 thousand bits per second.

The Model 12 has a recording density of 48 tracks-per-inch and 3200 bits-per-inch. This permits its use in an IBM 3740 Data Entry System and allows disk interchangeability with IBM 3740 Diskette Input/Output units. Using the IBM 3740 data format, up to 1.94 million bits of data may be recorded on a single cartridge.

Design flexibility permits the Model 12 to also be used in non-IBM compatible configurations. For these applications, the data format must be determined by the user.

The dual cartridge configuration of the Model 12 provides the storage capacity of two single-disk drives, but requires less space and cost less than two single drives. An operator can load or unload either one of the two cartridges while the other continues to operate (as indicated by an illuminated light emitting diode). This feature permits subsequent work to be set up without disturbing present work flow, thereby increasing throughtput capability.

Simplicity, built-in dependability, low maintenance requirements, and cost-effectiveness make the Model 12 an ideal device for a broad range of system applications requiring low cost data storage. The drive is ideally suited for use with intelligent terminals, mini or large scale data communications systems, small business systems, word processors, point-of-entry systems, error logging systems, and microprogram loading operations.

1.2 GENERAL DESCRIPTION

The basic Model 12 Flexible-Disk Drive consists of a pair of read/write heads and multiplexed read/write channel, two head loading mechanisms, two index sensing circuits and a shared cartridge drive system, head positioning mechanism and track ØØ sensing circuit.

In addition to the basic drive functions identified above, the Model 12 provides a number of special features such as hard sector interface, write inhibit on "write protected" flexible disks, data/clock separation with missing clock detection. These features are optional and must be specified at the time of order.

Note: Hard and soft sectors are defined in Section 4.

1.3 OPTIONAL FEATURES

Optional features are described below:

1. **Data Clock Separator** – If the user does not have a data/clock separator within his control unit, the Model 12 can be purchased with one.

2. **Sector/Index Mark Separator** – Distinguishes, on a sectored disk, the sector from index holes and sends them out on appropriate I/O lines. Electronics include sector detection and separation logic which permits use of hard sectors in record formatting. When enabled, this feature provides the user with up to 32 sector pulses for each revolution of the selected disk.

3. **Write Protect** – Provides the sensing apparatus to detect the Write Protect hole in the diskette cartridge which then flags the user of such feature and inhibits any Write operation from taking place.

Note: When only one or two of the above options are desired, the user will receive all three.

4. **Mounting Tray** – A tray is available for 19-inch rack mounting of one or two drives with sufficient room for power supplies.

5. **Diskette Storage** – A storage box is available that fits into the mounting tray, in the place of one drive, for storage of disketts only.

Signal and power cables are normally provided by the user to connect the drive to the host system. The user supplies the selection, control, data formatting and power requirements of the drive. Cable and connector requirements are defined in Section 2.

1.4 PERFORMANCE CHARACTERISTICS AND FEATURES

Performance characteristics and features are given below.

1.4.1 Storage Medium

Type	IBM diskette or equivalent, or hard sector disk (32 sector holes maximum)
Number of Tracks	77
Tracks Per Inch	48
Track-to-Track Spacing	0.508mm (.020 inch)

1.4.2 Recording Technology

Recording Mode	Frequency Modulation (FM)
Method	Contact Recording
Bit Density (inner track)	3200 bits-per-inch
Transfer rate	250,000 bits-per-second
Maximum Capacity (Unformatted)	
Drive	6.2 Megabits
Disk	3.1 Megabits
Track	41 Kilobits

1.4.3 Disk Speed

Rotational Speed	360 RPM ±3%
Rotational Time	166.7 Milliseconds
Average Latency	83.3 Milliseconds

1.4.4 Head Positioning (Access) Time

Head Positioning	10 Milliseconds (track-to-track)
Settling Time	10 Milliseconds (after last track)
Head Loading Time	40 Milliseconds

1.4.5 Physical Characteristics

Height	220mm (8.66 inches)
Width	220mm (8.66 inches)
Depth (including front panel)	368mm (14.49 inches)
Weight (Approximate)	6.8kgs (15 pounds)

1.4.6 Environmental Characteristics

1.4.6.1 Operating Mode

Temperature	15.5° to 38°C (60° to 100°F)
Maximum Rate of Change	8.3°C (15°F) per hour
Relative Humidity	20% to 80% at 29.4°C (85°F) noncondensing

1.4.6.2 Non-Operating Mode

Temperature	−40° to 54°C (−40° to 130°F)
Maximum Relative Humidity	90% noncondensing

1.4.7 Power Requirements

DC Voltage	+24 Vdc ±10% at 2.5A maximum
	+5 Vdc ±5% at 2.5A maximum
AC Voltage (standard)	115 Vac 60Hz at 0.4A maximum
(optional)	115 Vac 50Hz or 230 Vac 50Hz

SECTION 2

INSTALLATION AND OPERATION

2.1 INSTALLATION

A Model 12 Disk Drive may be mounted in a standard 19 inch rack or in a desk-top manner. Diablo offers a tray, Part No. 45028, which fits in a 19 inch rack, easing the user installation.

When the desk-top unit is selected, a front panel with a flange is installed on the drive. When the unit is rack mounted, the disk doors may be either in the vertical or horizontal plane.

The 19 inch rack mounting tray comes with separate installation instructions. In addition, the tray has sufficient room for mounting two drives, or one drive and a disk storage compartment. The rear of the tray has ample room for power supplies. The tray has internal slides for easy access and maintenance.

2.2 INTERCONNECTING CABLES

The Model 12 requires three external cables; one interface cable, one DC power cable, and one AC power cable. The I/O cable is connected via the printed circuit board edge connector. The DC power cable is connected to the printed circuit board at plug P1. The AC power cable is connected to a mating female receptacle in one of the drives rear support legs.

2.2.1 Cable Connectors Parts Description

Connectors used are as follows:

1. I/O connector; Diablo Part No. 10817-50, 3M Part No. 3415-0000, and includes both the connector housing and pins.

2. DC power connector; connector housing, Diablo Part No. 10872-04, Molex Part No. 09-05-3041; female connector pins, Diablo Part No. 10873, Molex Part No. 08-50-0106.

3. AC power connector; connector housing, Diablo Part No. 10920-03, Molex Part No. 19-09-1032; female connector pins, Diablo Part No. 10834-01, Molex Part No. 02-09-1103.

2.2.2 Connector Pin Assignments

Connector pin assignments can be found in Section 3, Interface Information and Section 7, Wiring Diagram.

2.2.3 Cable Recommendations

2.2.3.1 DC Cable

A Model 12 drive requires +5 volts at 2.5 Amperes and +24 volts at 2.5 Amperes. The cable wire size should be 16 AWG or larger. Cable length should be sufficient to allow a service loop, but should not exceed 12 feet in length.

2.2.3.2 AC Cable

Any 3-wire AC Cable, 18 AWG or larger is sufficient. Maximum length should not exceed 12 feet.

2.2.3.3 I/O Cable

For the Model 12 I/O Cable Diablo recommends a 50-conductor flat ribbon cable of 28 AWG stranded wires and a characteristic impedance is about 100 ohms. The length of cable should not exceed 12 feet. This allow ample room if more than one Model 12 is to be daisy chained.

Diablo offers a cable assembly, Part No. 45037-XX (XX = length in inches), which includes a 50-conductor flat cable with a connector at the disk drive end. In addition, a kit is available, Part No. 45146, which contains AC and DC connectors with pins, and an I/O connector.

2.3 TERMINATION

Signal lines carrying pulses will cause reflections if not properly terminated. Input lines to the Model 12 are terminated into a 180/390 Ohm resistor network. The Model 12 output lines are open collector circuits requiring termination on the host systems line receivers. Diablo recommends 180/390 Ohm termination (see Figure 2-1).

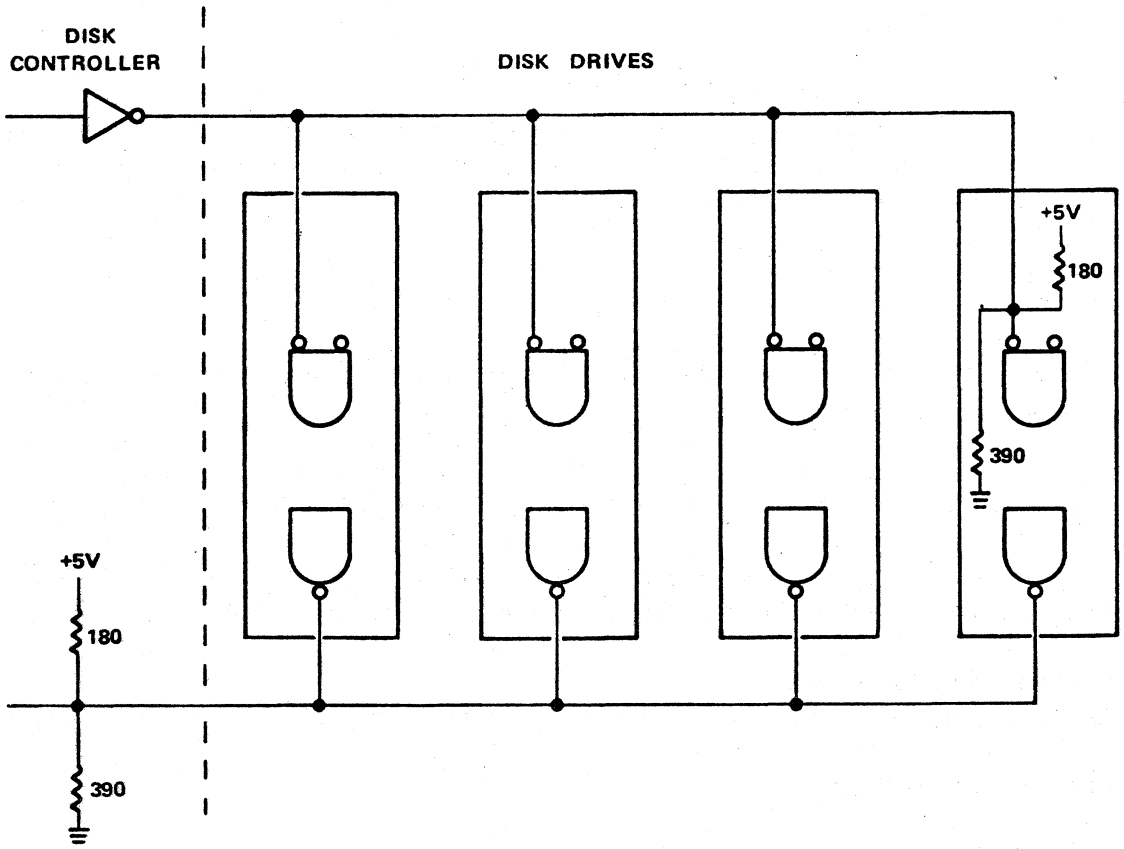


Figure 2-1 TYPICAL TERMINATION CIRCUITS

2.4 DAISY CHAIN

When more than one Model 12 Disk Drive is to be placed on the I/O Cable, the last drive on the chain should be terminated. Each Model 12 is supplied from the factory with a terminating resistor network, mounted on the PC board in an I.C. socket at location E15. It is up to the user to remove the terminating resistor network from each drive not requiring one.

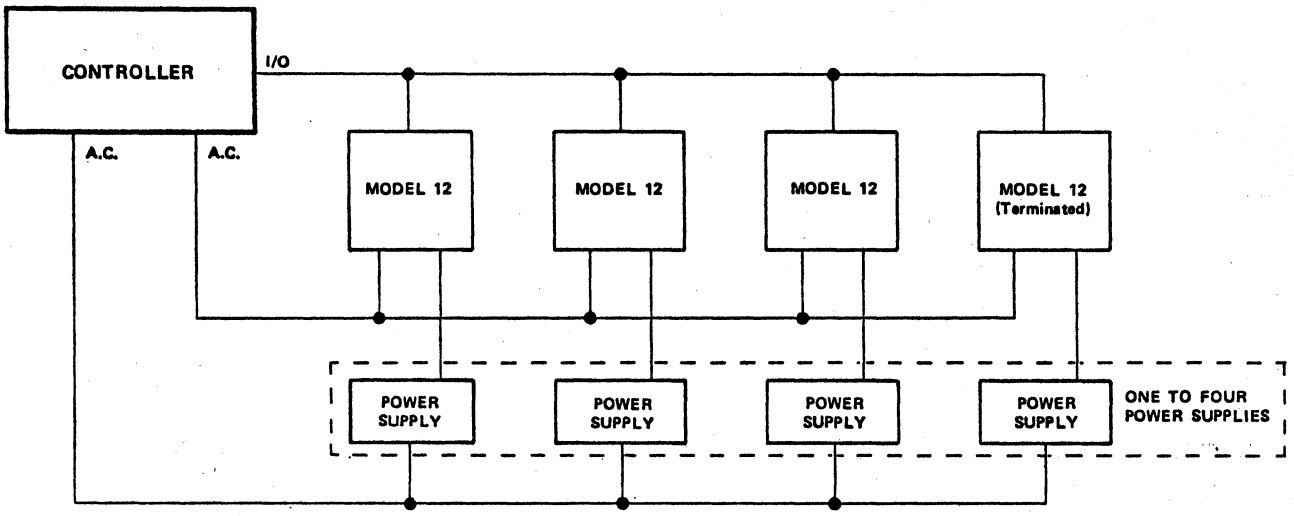


Figure 2-2 TYPICAL INTERCONNECTING DIAGRAM

2.5 SYSTEM INTERCONNECTION

Figure 2-2 illustrates a typical scheme for connecting up to four Model 12 Disk Drives to a Controller. It is up to the user to provide power supplies for each or all drives. I/O Cable length should not exceed 12 feet from the Controller to the last (terminated) drive on the chain.

2.6 UNIT SELECT LINES

When a Model 12 is shipped from the factory, its Select Line jumper is soldered into the "1" position. This is the proper position for systems using only one drive. If the drive is to be installed daisy-chain, the jumper must be changed to reflect the position within the chain. The Unit Select jumper is located on the PCB to the left of the I/O connector when looking at the drive from the rear with the PCB on top.

2.7 INDEX OR SECTOR SELECTION

Depending on how the user ordered the Model 12, Index or Sector mode jumpers are installed at the factory. Jumper selection is located on the PCB, to the right of the I/O edge connector when looking at the rear of the drive with the PCB on top.

2.8 CONTROLS AND INDICATORS

The Model 12 has only two indicators located on the front panel. The indicators are of the Light Emiting Diode (LED) type which are visable at distances of 10 feet from the front of the drive.

The appropriate 'Busy' LED is on when a disk is installed and up to speed, the drive is selected, and disk is selected. Both LED's should never be on at the same time. When looking at the drive from the front, with the doors horizontal and the PCB on top, the upper LED indicates the 'B' side and the lower LED the 'A' side.

2.9 OPERATION

With power and I/O Cables attached and Select and Index/Sector jumpers in the correct position, apply power to the drive. The disk hubs will turn and the drive is ready for operation.

Open both doors and insert appropriate flexible-disk media into the front panel slots. Media must be

inserted with its label toward the PCB (normally up). Close the doors as far as possible. The drive is now ready for selection by the Controller for normal seek, read and write functions.

Each disk may be removed by an operator and another installed when the appropriate busy indicator is off. A disk should not be removed while the busy LED is on as data transfer may be interrupted.

Note: The Model 12 may be ordered without any options. This is an Index only drive without a Data/Clock Separator or Write Protect. If the drive is ordered with one option, such as Write Protect, then Sector and the Data/Clock Separator are included.

If any of the drives output lines are not used, the user should terminate them to prevent possible line noise.

SECTION 3

INTERFACE INFORMATION

3.1 GENERAL

This section provides a detailed description of the electrical interface functions of the Model 12 Flexible-Disk Drive. Included are line definitions, cable and connector specifications, line driver and receiver information, termination data and interface timing requirements.

The interface requirements of the Model 12 are divided into two categories: Power and Signal.

3.2 POWER INTERFACE

The power interface consists of one AC power cable and one DC power cable. These cables are normally supplied by the host system.

3.2.1 AC Power

The Model 12 requires 115Vac 60Hz or 50Hz for operation of its spindle motor. A 230Vac 50Hz option is also available. A nylon receptacle (Diablo Part No. 10920-03 or equivalent) must be used on the host system to connect to the AC plug mounted in the rear casting of the drive. The middle pin of this plug is chassis ground.

3.2.2 DC Power

The Model 12 operates on +24Vdc and +5Vdc. The DC power cable plugs into connector J1, located at the rear area of the PC Board. A nylon connector (Diablo Part No. 10872-04, is used on the drive end of the DC Power Cable.

Listed below are the pin numbers and power levels of the DC power cable.

Pin No. (J1)	Power Level	Wire Size
1	+24Vdc Return	18 AWG
2	+24Vdc	18 AWG
3	+5Vdc	18 AWG
4	+5Vdc Return	18 AWG

+5Vdc operates the logic family used while +24Vdc operates the stepper motor and supplies the voltage for the read/write channel.

3.3 INPUT/OUTPUT SIGNAL INTERFACE

The I/O signal cable provides the lines to control the Model 12 and transfer data to and from the drive. Twelve input lines and twelve output lines are included in the I/O cable.

Note: Input signals are defined as those received by the drive from the user and output signals are those transmitted from the drive to the user.

Each signal line is paired with a separate return line and all lines in the signal interface are digital (TTL) compatible. The characteristic impedance of the input signal lines is approximately 100 Ohms.

3.3.1 I/O Cable Connector Requirements

The I/O signals are connected to the drive through a PC board edge connector located on the rear area of the Model 12 PC board. A flat cable connector (Diablo Part No. 10817-50 or equivalent) which has 25 dual readout contacts on .100 inch centers is required for the drive end of the cable. The same type connector is recommended for the user end of the cable. Connector pin assignments for the I/O signal cable are provided below.

Note: Input and output voltages are 0.0V to 0.4V relative low (LO) active and 2.4V to 5.5V relative high (HI) inactive.

Pin	Signal	Direction
2	–Unit Select 4	Input
4	–Unit Select 3	Input
6	–Unit Select 2	Input
8	–Unit Select 1	Input
10	–Read Data	Output
12	–Read Clock	Output
14	–Missing Clock Pulse	Output
16	–Write Protect	Output
18	–Write Gate	Input
20	–Head Load A	Input
22	–Head Load B	Input
24	–Step	Input
26	–Ready A	Output
28	–Ready B	Output
30	–Index A	Output
32	–Index B	Output
34	–Sector A	Output
36	–Sector B	Output
38	–Track 00	Output
40	–F.M. Data	Output
42	–Select Disk B	Input
44	–Write Data	Input
46	–Low Current	Input
48	–Seek In	Input
50	+5V	Output

Note: A schematic diagram of the I/O cable appears in Section 7 of this manual.

3.3.2 Signal Definitions

The I/O signals are defined in the following paragraphs. The sign proceeding each signal name indicates the polarity of that signal in its active state.

3.3.2.1 Input Signals

1. **–Unit Select 1, 2, 3, 4** – These four lines are jumper selected in each drive. The jumper must be installed in each drive to reflect the desired position in a string of drives. The four

select lines allow a maximum of four drives to be daisy chained.

2. **–Write Gate** – This signal enables data to be written on the disk, which is controlled to the appropriate disk by the –Select Disk 'B' signal. –Write Data should follow the enabling of Write Gate or the disk will be erased with only Write Gate active. Tunnel erase current is controlled internally in the drive by Write Gate.

3. **–Head Load A** – This signal allows the 'A' side R/W head to come into contact with the disk on side 'A'. The 'A' side Ready signal must be active as well as the unit being selected.

4. **–Head Load B** – This signal works the same as the 'A' side except that all references are made to the 'B' side.

5. **–Step** – This signal is a LO pulse which, when active, causes the R/W heads to move one track. The negative going leading edge of each pulse latches the direction information and excutes the step. The direction signal should remain stable for 100 nanoseconds prior to the leading edge of the step pulse. The maximum step rate is 10 milliseconds per track with a 10 millisecond settling time after completion of the last step.

6. **–Select Disk B** – This line enables the 'B' side read/write electronics for operation on the disk. When this line is HI, the 'A' side read/write electronics is enabled.

7. **–Write Data** – This is a series of LO pulses which represents the data to be written on the selected disk in an F.M. (double frequency) encoded manner. Encoding data in double frequency is the users responsibility. Pulse width is 1 ± 0.8 microsecond. The leading edge of the LO pulse causes a flex reversal on the media. Clock pulses should appear every 4 microseconds for a transfer rate of 250 Kilobits per second. Data pulses should follow clock pulses by 2 microseconds.

8. **–Low Current** – This line changes the amount of write current flowing through the R/W Head. The line is LO when at or higher than track 43 and in a "Write Data" condition. It is the host systems' responsibility to monitor this line.

9. **–Seek In** – This signal controls the direction of head (positioner) travel. When LO and the drive is selected, the travel is in, toward the center of the disk. When HI and selected, travel is away from the center.

3.3.2.2 Output Signals

1. **–Read Data (Optional)** – This signal represents separated data bits that are recorded on the selected disk. Each recorded data bit is represented by a LO pulse whose width is 500 ± 200 nanoseconds.

2. **–Read Clock (Optional)** – This signal represents the separated clock bits that are recorded on the selected disk. Each recorded clock bit is represented by a LO pulse whose width is 500 ± 200 nanoseconds.

3. **–Missing Clock Pulse (Optional)** – This signal identifies dropped clocks on the disk which

are coded to provide Index/Sector information (IBM format address marks).

4. **–Write Protect (Optional)** – This LO signal indicated to the user that a "read only" cartridge is installed in the selected disk position and that the Write Gate function is therefore disabled.

5. **–Ready A** – This signal goes LO when disk 'A' is in place and is up to speed. Disk speed is monitored and aftertwo revolutions at the proper speed, this signal becomes active.

6. **–Ready B** – This signal is identical to –Ready A except reference is made to disk 'B'.

7. **–Index A** – This signal is provided by disk 'A' once each revolution to indicate the beginning of data on each track. It is used as a reference when unrecorded disks are being written on.

8. **–Index B** – This signal is identical to –Index A except that disk 'B' is referenced.

9. **–Sector A (Optional)** – This signal is provided by disk 'A' at the beginning of each sector of a sectored data disk. The number of sectors on a disk is determined by the media; typical is 8, 16 or 32. This means that for each revolution of the disk, 8, 16, or 32 sector pulses would occur. This signal is LO active with a duration of 0.3 ± 0.1 millisecond.

10. **–Sector B (Optional)** – This line is identical to –Sector A except that reference is made to disk 'B'.

11. **–Track 00** – This signal goes LO to indicate that the R/W heads are psotioned over the outermost data track on the disk.

12. **–F.M. Data** – This signal represents the recorded clock and data bits and is sent to the user in the same interleaved sequence in which they were received during the write operation. Signal pulse width is 500 ± 200 nanoseconds.

Note: The optional signal lines should be monitored only if the options are used. Random signals may be present on the lines when options are not used.

3.3.3 Line Drivers and Receivers

Control, data and timing information is exchanged between the Model 12 and the user system via standard line driver and receiver circuits. Commercially available integrated circuit packages are utilized for both line drivers and receivers to simplify the control unit interface design. An example of the typical line driver/receiver circuits is shown in Figure 3-1.

3.3.3.1 Line Drivers

A standard type 7438 integrated circuit package is used for all line driver applications. The output stage of this circuit is an open collector transistor. The line driver is capable of current sinking 40 milliamps in the LO (active) condition at 0.5V maximum.

The user must provide signal line termination in his system. Recommended values are 180 Ohms to +5V and 390 Ohms to ground.

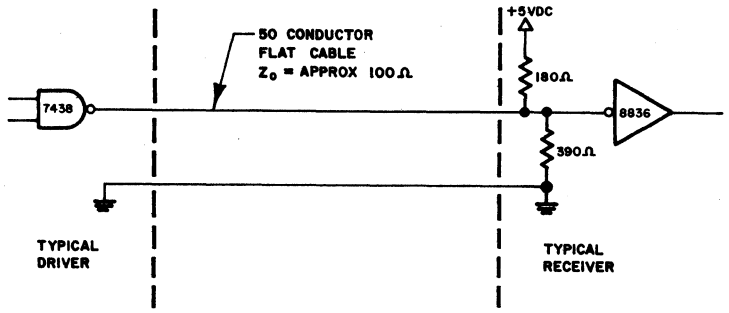


Figure 3-1 TYPICAL LINE DRIVER/RECEIVER CIRCUITS

3.3.3.2 Line Receivers

A type 8836 receiver integrated circuit gate, together with its input terminating network is used for line receiver applications. The terminating network consists of 180 Ohms to +5V and 390 Ohms to ground.

3.3.4 Termination

A single ended line scheme is used for the interface signal cable. For this reason, all lines should be terminated at the receiving end to assure satisfactory noise immunity.

Note: A line terminator must be installed in any single drive, or in the last drive of a multiple drive system.

3.3.5 Interface Timing

The following paragraphs define timing characteristics of the Model 12 interface. Timing information is provided for the five operations that involve drive/control unit communication:

1. Application of power to the drive.
2. Seek operations.
3. Write operations.
4. Read operations.
5. Index/Sector pulse generation.

Details regarding the use of Index and Sector pulses for record formatting are provided in Section 4.

3.3.5.1 Power Application

AC and DC power may be applied to the drive in any sequence. However, both must be on before the drive can indicate a ready condition to the host system.

After power is applied, the drive starts testing the rotational speed of either or both cartridges.

Note: For speed monitoring of either cartridge location, a cartridge must be installed in that location.

Approximately 1 second after power is applied, the speed monitoring circuits will condition the disk

ready status gate for either or both cartridges. This delay period includes sufficient time for the spindle to reach 80% of its rotational speed before enabling index/sector counter. After two index pulses have been counted (approximately .332 second at an RPM greater than 340) the Ready Status gate is conditioned to indicate that the spindle has stabilized at its normal operating speed.

3.3.5.2 Seek Operations

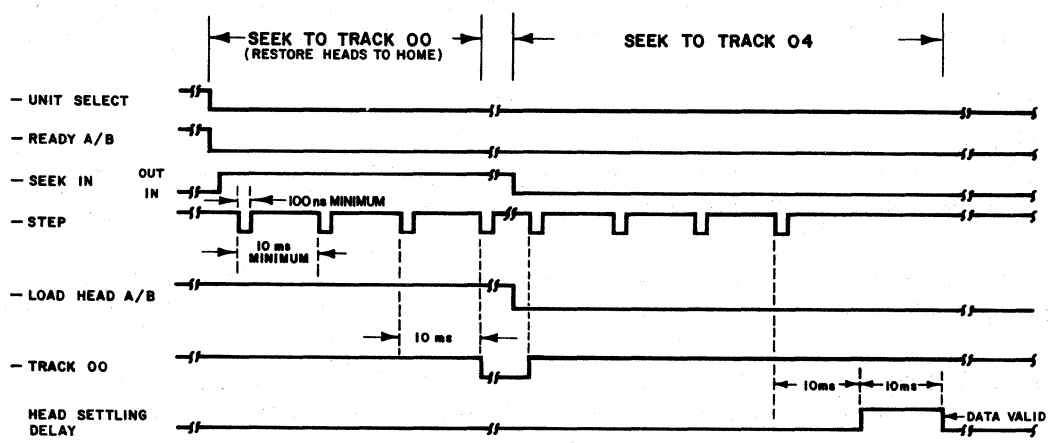


Figure 3-2 SEEK TIMING

Figure 3-2 illustrates the interface timing for seek operations. Following drive selection, the control unit sets the appropriate signal level on the –Seek In line (LO for seeks to higher track addresses; HI for seeks to lower track addresses). The –Seek In line must be valid for 100 nanoseconds prior to the leading edge of the first –Step pulse. The leading edge of each –Step pulse latches the seek direction information and causes the head position actuator to move the heads one track increment. The drives' maximum step rate of 10 milliseconds per track requires that the period between –Step pulses be no less than 10 milliseconds. A 10 millisecond head settling period is required after the last –Step pulse before initiating a read or write operation.

Note: Seek operations can be executed with the heads loaded. However, to prolong head and media life, it is recommended that the heads be unloaded during extended periods when no commands are issued to the drive. The time required to load the heads is 40 milliseconds.

3.3.5.3 Write Operation

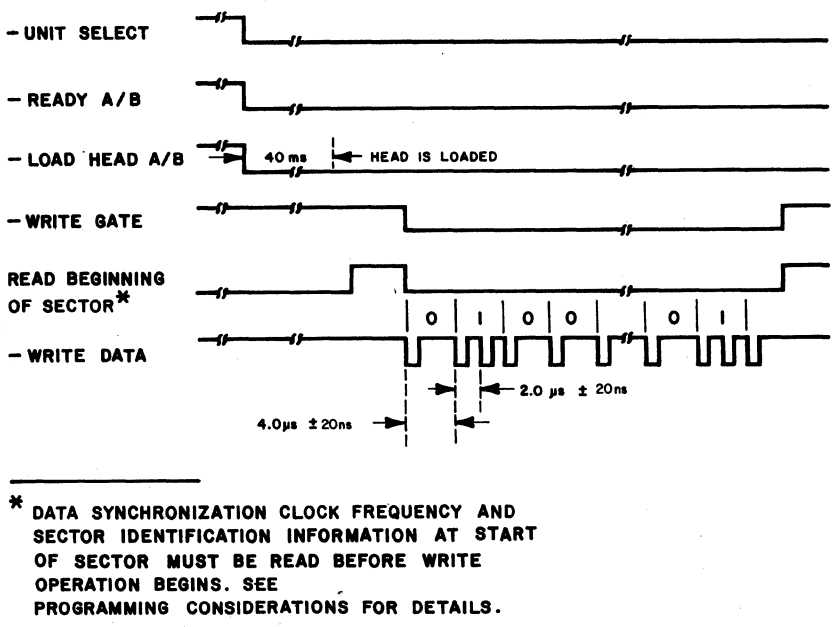


Figure 3-3 WRITE CLOCK AND DATA PULSE TIMING

Figure 3-3 shows the timing requirements for write clock and data pulses.

A Write operation can begin when the heads are loaded, the appropriate head is selected and the specified sector is detected. If hard sectoring is employed, sector detection can be performed during head loading. Detection of soft sectors requires the selected head to read address marks. For this reason, the heads must be loaded before sector detection can be performed.

As soon as the specified sector is identified, the control unit should activate –Write Gate. This enables the Write drivers for the selected head to respond to write clock and data pulses. The control unit may send its first clock pulse on the –Write Data line as soon as –Write Gate is issued.

Note: The first pulse (clock or data) may or may not be recoverable depending on where it occurs in relation to the leading edge of the –Write Gate signal and to the previously recorded data.

The period from the leading edge of one clock pulse to the next must be 4.0 microseconds ± 20 nanoseconds. The leading edge of each data pulse must occur 2.0 microseconds ± 100 nanoseconds after the leading edge of the preceding clock pulse.

A delay circuit in the drive controls tunnel erase current in the selcted head, turning erase on 200 microseconds after –Write Gate becomes active, and keeping erase active for 600 microseconds (nominal) after –Write Gate goes false.

3.3.5.4 Read Operation

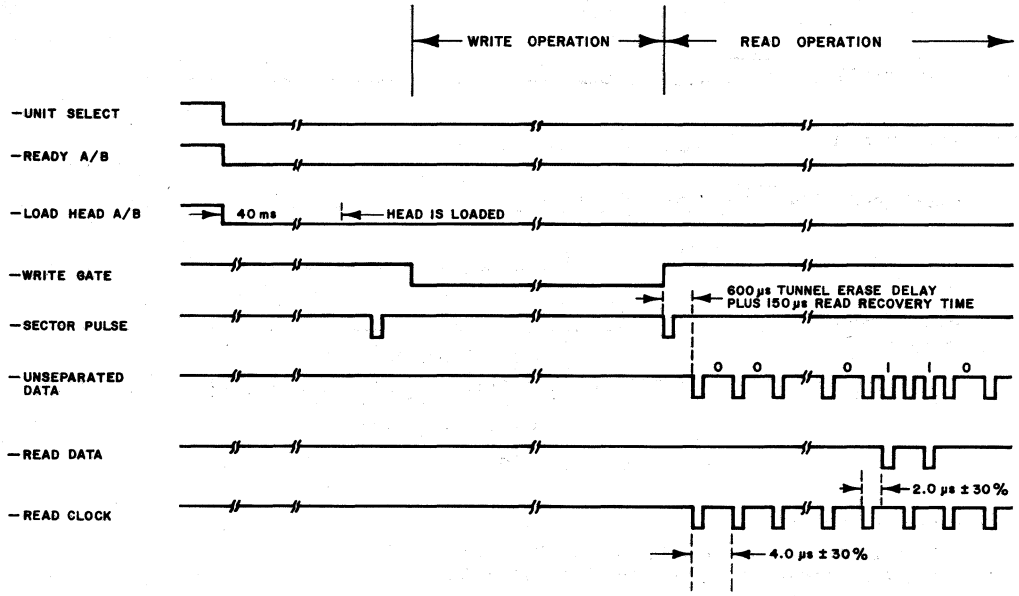


Figure 3-4 READ CLOCK AND DATA PULSE TIMING

Figure 3-4 illustrates the timing characteristics of read clock and data pulses.

A selected R/W head is enabled for reading whenever –Write Gate is inactive. This assumes that the control unit has varified that the associated disk is in the ready state and has loaded the R/W heads.

When a read operation follows a write operation, the read data will not be valid until approximately 750 microseconds after –Write Gate goes false. This time includes 600 microseconds for tunnel erase delay plus 150 microseconds for read channel recovery time.

When the drive's read channel is enabled, heads are loaded and the selected head is in a valid record field, digital read clock and data pulses appear on the –Read Clock and –Read Data lines. Clock pulses occur 4.0 microseconds ± 30% apart and data pulses follow the preceding clock pulses by 2.0 microseconds ± 30%. These timing tolerances are caused by pattern sensitive bit shift.

Note: These timing relationships are the same for both separated and unseparated data.

In systems using soft sector record formatting, the pulses provided on the –Missing Clock line maintain a delayed clock frequency established by the clock pulses on the –Read Clock line.

3.3.5.5 Index/Sector Timing

Figure 3-5 shows the timing characteristics of the index and sector pulses as they appear at the drive interface.

When the spindle is rotating at its operating speed, an index pulse is generated every 166.7 milliseconds ± 3%. The width of each index pulse is 0.3 ± 0.1 millisecond.

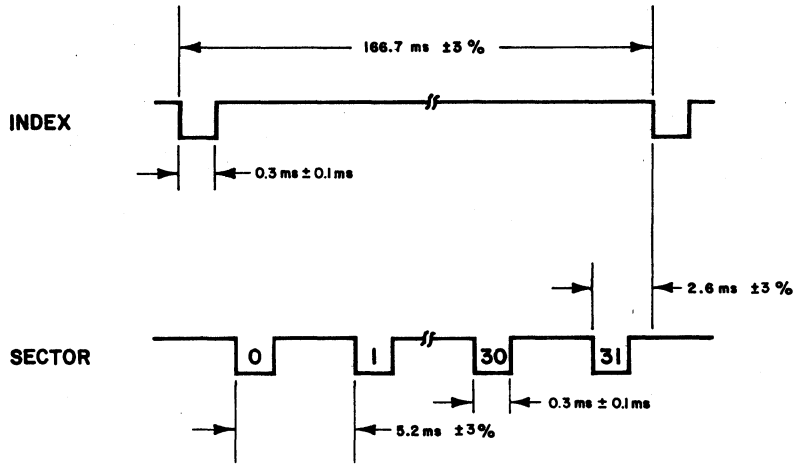


Figure 3-5 INDEX/SECTOR PULSE TIMING

In systems using hard sector record formats, up to 32 sector pulses are issued between index pulses. The sector pulses occur at regular intervals and have individual pulse widths of 0.3 ± 0.1 millisecond.

SECTION 4

DISK FORMATTING

4.1 GENERAL

Specific requirements for the organization of data on a disk vary considerably from one application to another. For this reason, each user must be responsible for establishing the data record format when implementing a Model 12 Flexible-Disk Drive.

This section does provide, however, certain general guidelines for planning the record format. It presents this information in two categories; one concerning requirements imposed by the IBM 3740 Data Entry System, and the other covering both hard and soft sector formats in non-IBM compatible systems.

4.2 IBM COMPATIBILITY

4.2.1 General Data Organization

In the IBM 3740 Data Entry System, each disk contains one index track (addesss 00), 73 record tracks (addresses 01 through 73), two alternate tracks (addresses 74 and 75) and a spare (address 76). Each track is divided into 26 sectors containing from 1 to 128 characters in EBCDIC. The organization of sectors on a track is determined logically (soft sectoring) rather than mechanically (hard sectoring). The data records may be logically organized into data sets, with up to 19 data sets residing on a single flexible disk (volume).

4.2.1.1 Index Track (00)

Each Sector on the index contains 80 characters.

Sector 1	80 Blanks	(Initialized as Hex 40)
Sector 2	80 Blanks	(Initialized as Hex 40)
Sector 3		
Character 1	Machine Test Character	(Initialized as Hex 40)
Character 2-80	Blanks	(Initialized as Hex 40)
Sector 4	80 Blanks	(Initialized as Hex 40)
Sector 5-26	Error Track Map	(See Paragraph 4.3.2)

4.2.1.2 Record Tracks (01-73)

These are the tracks normally used for storing the user records.

4.2.1.3 Alternate Tracks (74 and 75)

These tracks are used as record tracks when any of the regular record tracks are unusable. Their use is defined in the Error Track Map (sector 5 of track 00).

4.2.1.4 Spare Track (76)

This track is not used in the present 3740 System.

4.2.2 Record Format

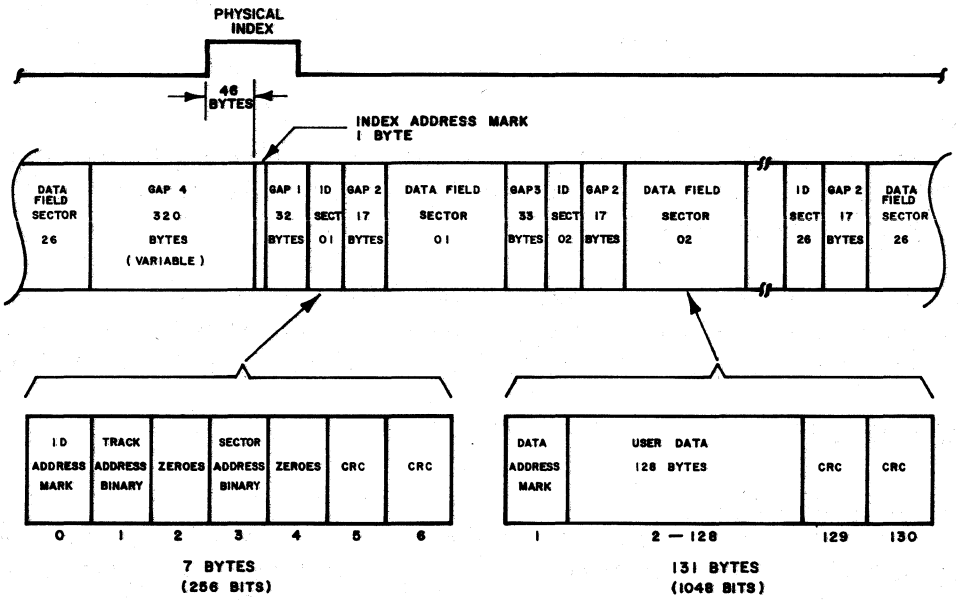


Figure 4-1 IBM TRACK FORMAT

The principal characteristics of the record format are shown in Figure 4-1. These characteristics are defined in the following subsections.

4.2.2.1 Gaps

These are track segments that contain only clock bits. They serve as buffer zones between adjacent fields to permit one field to be rewritten without affecting the adjacent fields. There are four different types of gaps, each of a different length.

1. Gap 1 (Post Index Gap)
   This gap separates the index address mark and the ID address mark for sector 1. It is always 32 bytes in length.

2. Gap 2 (ID field and the data field)
   Its nominal length is 17 bytes, but may vary slightly as a result of updating the data field.

3. Gap 3 (Data Gap)
   This gap separates the data field and the following ID field. Its nominal length is 33 bytes, but may vary slightly as a result of updating and adjacent data field.

4. Gap 4 (Pre-Index Gap)
   This gap separates the data field in sector 26 from the index address mark. Its nominal length is 320 bytes, but may vary as a result of disk speed and write frequency tolerances as well as of updating the sector 26 data field.

4.2.2.2 Address Marks

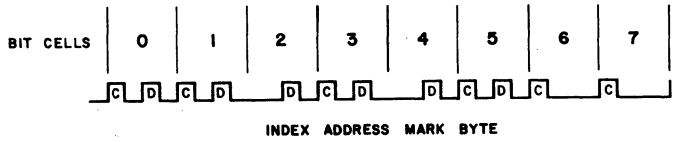
These areas contain unique bit patterns of one byte each. They identify the beginning of ID and data fields and are used to synchronize data deserializing circuitry with the first byte of ID or data.

Address mark bit patterns are unique because specified clock bits are deleted from their bit cells. All other bytes in the record are required to have clock bits in every bit cell.

There are four different types of address marks.

1. Index Address Mark

   This address mark is located a fixed number of bytes ahead of the first record in the track. Its bit pattern is illustrated in Figure 4-2.

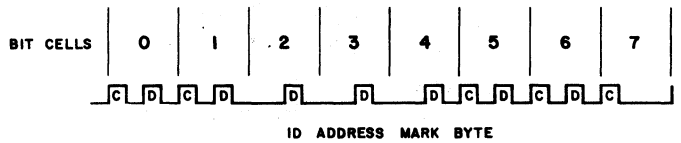


	BINARY VALUE	HEX VALUE
DATA BITS	1 1 1 1 1 1 0 0	F C
CLOCK BITS	1 1 0 1 0 1 1 1	D 7

Figure 4-2 INDEX ADDRESS MARK BIT PATTERN

2. ID Address Mark

   This address mark precedes each ID field on the track. Its bit pattern is illustrated in Figure 4-3.

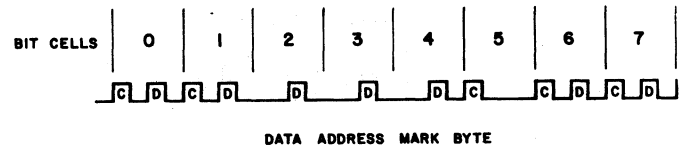


	BINARY VALUE	HEX VALUE
DATA BITS	1 1 1 1 1 1 1 0	F E
CLOCK BITS	1 1 0 0 0 1 1 1	C 7

Figure 4-3 ID ADDRESS MARK BIT PATTERN

3. Data Address Mark

   This address mark precedes each non-deleted data field on the track. Its bit pattern is illustrated in Figure 4-4.

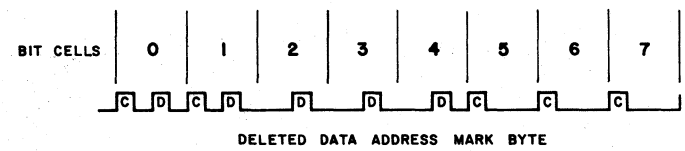


	BINARY VALUE	HEX VALUE
DATA BITS	1 1 1 1 1 0 1 1	F B
CLOCK BITS	1 1 0 0 0 1 1 1	C 7

Figure 4-4 DATA ADDRESS MARK BIT PATTERN

4. Deleted Data Address Mark

   This address mark precedes each deleted data field on the track. Its bit pattern is illustrated in Figure 4-5.



	BINARY VALUE	HEX VALUE
DATA BITS	1 1 1 1 1 0 0 0	F 8
CLOCK BITS	1 1 0 0 0 1 1 1	C 7

Figure 4-5 DELETED DATA ADDRESS MARK BIT PATTERN

4.2.2.3 Cyclic Redundancy Check (CRC)

Every ID and data field on the track has a pair of CRC bytes appended to it. These bytes, which are generated as the field is written, represent a cyclic permutation of all the data bits in the field, from bit 0 of the address mark to bit 7 of the last byte in the field (excluding the CRC bytes).

The cyclic permutation is the remainder that results from dividing the data bits (represented as an algebraic polynomial) by a generator polynomial G (X). The polynomial used in the 3740 system is $G(X) = X^{16} + X^{12} + X^5 + 1$.

4.2.3 Error Track Map

Sector 5	Position 1-5:	ERMAP Position 6-80 blanks (Hex 40) If a bad data track is found on the disk, an alternate track may be substituted.
	Positions 7 and 8 indicate first bad track number. Alternate track 74 will be used in its place.	
	Position 9 must contain a Hex 00.	
Sector 6	80 blanks (Hex 40) Volume Label	
	Position 1-4:	Vol 1 (Initialized VOL 1. Required for 3740 system.)
	Position 5-10:	Volume ID: (initialized on IBM Diskette as IBMIRD)
		The volume ID may be changed by the system user.
	Position 11:	Accessibility — any non-blank character means disk is not accessible. (Initialized as a blank character, Hex 40. This is rarely used in the 3740 system.)
	Positions 12-76:	Blanks (Hex 40)
	Position 77,78:	Sector Sequence information (Initialized as Hex 40). This allows for initializing nonsequential sectors on a track. For example: a 02 in these positions will sequence the sectors: 1, 3, 5, 7, . . . etc. The sector sequence information characters provide for inter-leaving of sectors, allowing for increased system throughput in special applications.

Section 6 (Continued)	Position 79:	Blank
	Position 80:	W (Initialized as W, required by 3740 system.)
Sectors 8-26	Data Set Labels	Data Set Labels define logical boundaries of data. Up to 19 data sets may be defined on a diskette volume.
	Position 1-4:	Header Sector 8 is initialized as HDR1. (Initialized Sector 9 through 26 contain deleted records with DDR1 in Position 1-4.)
	Position 5:	Blank or Reserved (Initialized Hex 40)
	Position 6-13:	Data Set Name: May be user defined. (Initialized Sectors 9 through 26 contain records with the sector number recorded in positions 10-11.)
	Position 14-24:	Reserved or blank (Initialized as Hex 40 in positions 14-24)
	Position 25-27:	Logical Record length (maximum 128) Record length must be equal to 080 on the 3742 or greater than 000, less than 128 on the 3741 or on the 3742 with 128 feature. (Initialized as 080)
	Position 28:	Reserved or blank (Initialized as Hex 40)
	Position 29-33:	Beginning of Extent (BOE). Identifies address of first sector of a data set. Positions 29 and 30 contain track number, position 31 must be 0, position 32 and 33 contain sector number. (Initialized Sector 8 has 01001 in position 29-33, Sector 9-26 has 74001.
	Position 34:	Reserved or blank (Initialized as Hex 40)
	Position 35-39:	End of Extent: Identifies the address of last sector reserved for data set. (Initialized with 73026 in position 35-39 for Sector 8-26)
	Position 40:	Reserved or blank (Initialized Hex 40)

Sectors 8-26 (Continued)	Position 41:	Bypass data set: If this field contains a B, then 3747 data convertor will ignore data set. If field contains a blank, then data set will be processed. (Initialized as a blank Hex 40)
	Position 42:	Accessibility Field must contain a blank for processing in data set. (Initialized as blank Hex 40)
	Position 43:	Data Set Write Protect If field is blank, then reading and writing in data set is permitted. If field contains a P, the data set is write protected.
	Position 44:	Reserve or blank
	Position 45:	Multivolume indicator: A blank indicates data set is not continued on or from another diskette volume. A C indicates a data set is continued on another diskette and an L indicates this diskette to be the last on which the data set resides. (Initialized as a blank Hex 40)
	Position 46-72:	Reserved or blank (Initialized Hex 40)
	Position 73:	Verify Mark: A V in this field indicates the data set has been verified. (Initialized as blank Hex 40)
	Position 74:	End of Data: Indicates the address of next unused sector of data set. (Initialized in Sector 8 as 01001) (Sectors 9-26 initialized as 74001)
	Position 80:	Reserved or blank

4.3 NON-IBM SYSTEMS

In applications other than the IBM 3740 Data Entry System, the user has great flexibility in the organization of data records within each track. Either hard sectoring or soft sectoring or a combination of the two may be used.

Note: For a combination scheme, the hard sectors may be subdivided by logic in the control unit to develop additional sector locations.

4.3.1 Hard Sectoring

Hard sectored disks typically have up to 32 evenly spaced sector holes at the same radius as the index hole.

These holes are used as mechanical references for locating anywhere from 2 to 32 sectors in each track.

Formatting of the disk is the organized placement of data zones and guard zones in each sector, and the placement of clock pulses and/or data within these zones. The data zones are the zones where data is to be recorded or read. To provide reliable recovery of data, these data zones must contain a constant number of data cells, even in the presence of disk speed variation and other tolerances. The guard zones are variable in length, and ensure a constant number of data cells in each data zone by absorbing variations in sector time.

Each guard zone is a series of recorded clock pulses. The guard zone is recorded at the beginning and ending of each data zone and is normally defined as a preamble (when at the beginning of the data zone) and as a postamble (when at the end of the data zone). The length of each guard zone must be adequate to allow for a reliable reading of each data zone even under worst-case conditions of all tolerances. Factors contributing to the required allowances for system tolerances include physical separation of the sector holes, sector jitter, disk rotational speed variations, write clock frequency, read amplifier recover time, and variations in the transducers and their associated circuitry.

Each data zone typically contains synchronizing, header, data and check information. A guard zone and a data zone are defined as a sector, and typically are recorded by a combination of hardware and software control.

Minimum requirements for formatting a 32 sector flexible disk are illustrated in Figure 4-6.

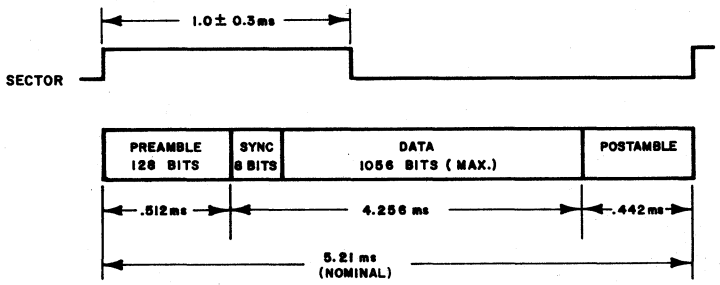
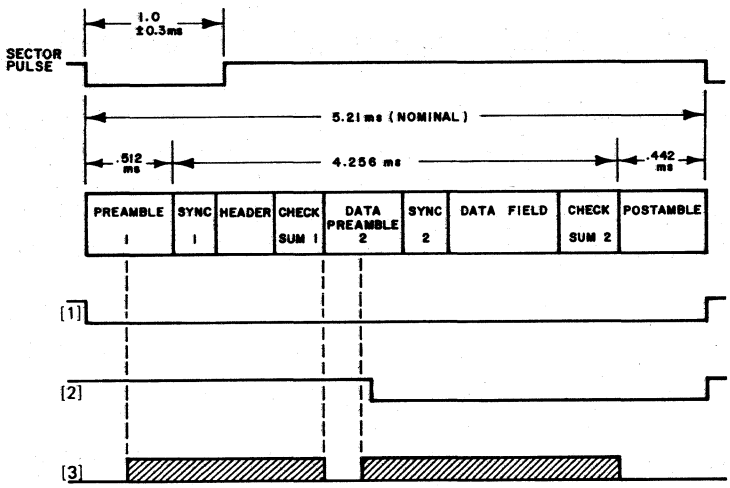


Figure 4-6 BASIC 32 SECTOR RECORD FORMAT

If the user intends to use a more sophistricated method of search and record verification, and if data integrity is highly ciritical, a typical sector mark format such as that shown in Figure 4-7 is recommended.



[1] During Write Format operation, controller activates –WRITE GATE line at leading edge of Sector Mark '0'.

[2] During Write Data operation, controller must not activate –WRITE GATE line until 11 byte/word times (352 microseconds) after the last bit of previous field. This delay period plus the 200 microsecond Erase Gate turn-on delay in the drive compensates for the R/W head tunnel erase delay, thus preventing previously recorded information (e.g., header, check sum, etc.) from being erased.

[3] During Read Data operation, controller should not enable Read Data from Model 12 until one-half way through the Preamble field. This ensures reading a zero field for data separator synchronization.

Figure 4-7 TYPICAL DETAILED 32 SECTOR RECORD FORMAT

The fields shown in this format are defined as follows:

1. **Preamble 1** – This field consits of a series of clock bits with no data bits. This pattern is necessary to permit a clear distinction between the preamble and the subsequent information field. The clock pattern also provides a time base for data synchronization circuits in the host system when the Unseparated Data option is used.

   The length of Gap 1 must be sufficient to provide for the following factors:

   (a) Time for the control unit to receive a sector pulse, compare the new sector address, and determine if this is the desired sector for the read or write operation.

   (b) Allow for read channel recovery time following a write operation.

   (c) Allow for jitter of the leading edge of the sector pulse. Jitter is caused by mechanical tolerances in the sector holes as well as electrical tolerance of the index/sector detector.

   (d) Allow for the ±3% speed variation of the disk.

   (e) If Unseparated Data option is used, allow synchronization time for the read detection circuits. Frequency stabilization and clock time must be precisely established before data may be recovered.

2. **Sync 1** – This area identifies the transition from the preamble to the header field. Sync 1 should consist of a known bit pattern (e.g., 00110011, etc.). The control unit searches for this pattern after enabling the read circuits while still in the preamble.

3. **Header** – The Header field will normally contain the following:

   (a) Track address of the record.

   (b) Sector number.

   This information is normally used in the control unit to compare with the track and sector that were addressed by the controller.

4. **Check Sum 1** – This is a bit check character generated in the controller as the header field is written, and then written immediately after the header. As the header is read at a later time, a check sum is generated within the controller, then compared with the sum recorded. If the check sums compare, the field is assumed to have been read without error.

5. **Data Preamble** – This is an optional field of all clock bits that function as a preamble to the data field. It is used in system applications when a virgin disk surface is initialized (to write all headers) only on the first pass. On subsequent data write operations the header field is not rewritten. When this field is not used, the header and data field are rewritten during subsequent data write operations.

6. **Sync 2** – Sync 2 is a known bit pattern, and is generally a different bit pattern from Sunc 1. Regardless of the pattern chosen, significance to the control unit is: the next bit read will be the first bit of the data field.

7. **Data** – The data field is the user's information storage area. For fixed record length recording, the data field preamble, Sync 2, and entire data field must be written each time the field is changed, since the check sum must be recorded at the end of the data field.

8. **Check Sum 2** – This field is generated within the controller as the data is written, and the check sum is written immediately after the data field. The check sum will be generated in the control unit by the same logic that generated Check Sum 1 for the header. As the data field is being read, the same logic will generate a new check sum on the bits being read. At the end of the data field, the generated check sum will be held and compared with Check Sum 2 when it is read. Since each data field contains a fixed number of bits, a counter may be incremented by each clock pulse to determine the end of the data field. If the sum generated as data is read compares with Check Sum 2, the data is assumed to have been read without error.

9. **Postamble** – This field is recorded immediately after the data check sum. It usually contains only clock bits, but may contain data bits if desired. Writing the postamble continues until the next sector mark pulse is received by the controller. The postamble provides for allowable disk rotational speed variation, write/erase gap placement, and write clock frequency variations.

4.3.2 Soft Sectoring

The format considerations for soft sector data records are for the most part the same as those for hard sector data records, with two significant differences.

1. Hard sector records are limited to a uniform length that is the same for all sectors. Record lengths in a soft sector system can vary from sector to sector and can be changed through programming efforts without modifying hardware design.

2. Soft sector formats require a unique bit pattern at the beginning of each sector to identify the leading edge of the sector. This information is readily recognized by the control unit as the start of a sector.

The task of indicating the start of sector is typically performed by a unique bit pattern called an address mark. This address mark cannot be duplicated by any legitimate sequence of data bit cells.

To render the address mark unique, certain prescribed clock bits must be deleted from the bit pattern when the address mark is written.

During subsequent read operations, the control unit tests the read data for this pattern and, recognizing it, synchronizes the read logic.

The drive's read channel includes an optional missing clock circuit, which detects any deletions of clock bits and generates a substitute clock pulse for each missing clock bit. These are sent to the control unit on a separate line for use in maintaining data synchronization.

4.3.3 Typical Read/Write Operations

This section summarizes typical Write Format, Write Data and Read Data operations with respect to the basic record format shown in Figure 4-7.

4.3.3.1 Write Format Operation

Before using a virgin disk for data storage, a write format operation should be performed to write header information in each sector of all tracks. This is referred to as initialization. Typical steps of the write format operation are summarized below.

1. Detect leading edge of sector mark '0'.

2. Enable Write Gate (See Item (1) in Figure 4-7.

3. Write Preamble 1 (zeros pattern).

4. Write Sync 1, typically 03_{16} or 03_{8}.

5. Write Header and Check Sum 1.

6. Write Preamble 2, zeros pattern.

7. Write Sync 2, Data Field and Check Sum 2. Typically, a zero's pattern or Header/Check Sum 1 information will be written in the Data Field during format operations. Sync 2 is typically 03_{16} or 03_{8}.

8. Write Postamble, zero's pattern until the leading edge of the next sector mark is detected.

9. During format operations Write Gate would not be disabled until the last sector of that particular track is formatted. Each sector would follow the same format, with only Header and Check Sum 1

information changing. This same track should be read on the next revolution to verify a proper formatting operation. Timing considerations would be identical to a Read Data operation.

4.3.3.2 Write Data Operation

A write data operation permits the user to store data in the data fields in each sector of an initialized disk. Typical steps of this routine are listed below.

1. Detect the leading edge of the desired sector mark.
2. Wait for one-half of Preamble 1 and enable Read Gate (Item (3) in Figure 4-7).
3. Read zero's preamble to synchronize data separator circuit.
4. Read Sync 1 and Header/Check Sum 1 to verify that the correct sector has been found.
5. Inhibit Read Data input to controller after last bit of Check Sum 1.
6. Wait 11 byte/word times (352 microseconds) then enable Write Gate (Item (2) in Figure 4-7).
7. Write Preamble 2, Zero's pattern.
8. Write Sync 2.
9. Write Data Field/Check Sum 2.
10. Disable Write Gate at the leading edge of the next sector mark.

4.3.3.3 Read Data Operation

Typical steps of a read operation are as follows:

1. Detect the leading edge of the desired sector mark.
2. Wait for one-half of Preamble 1 and enable Read Gate (Item (3) in Figure 4-7).
3. Read zero's preamble to synchronize Data Separator circuit.
4. Read Sync 1, Header/Check Sum 1 to verify that the correct sector has been found.
5. Inhibit Read Data input to controller after last bit of Check Sum 1.
6. Wait for one-half of Preamble 2, then enable Read Data (Item (3) in Figure 4-7).
7. Read zero's preamble to sync Data Separator circuit.
8. Read Sync 2, Data Field/Check Sum 2.
9. Inhibit Read Data input to controller.

SECTION 5

THEORY OF OPERATION

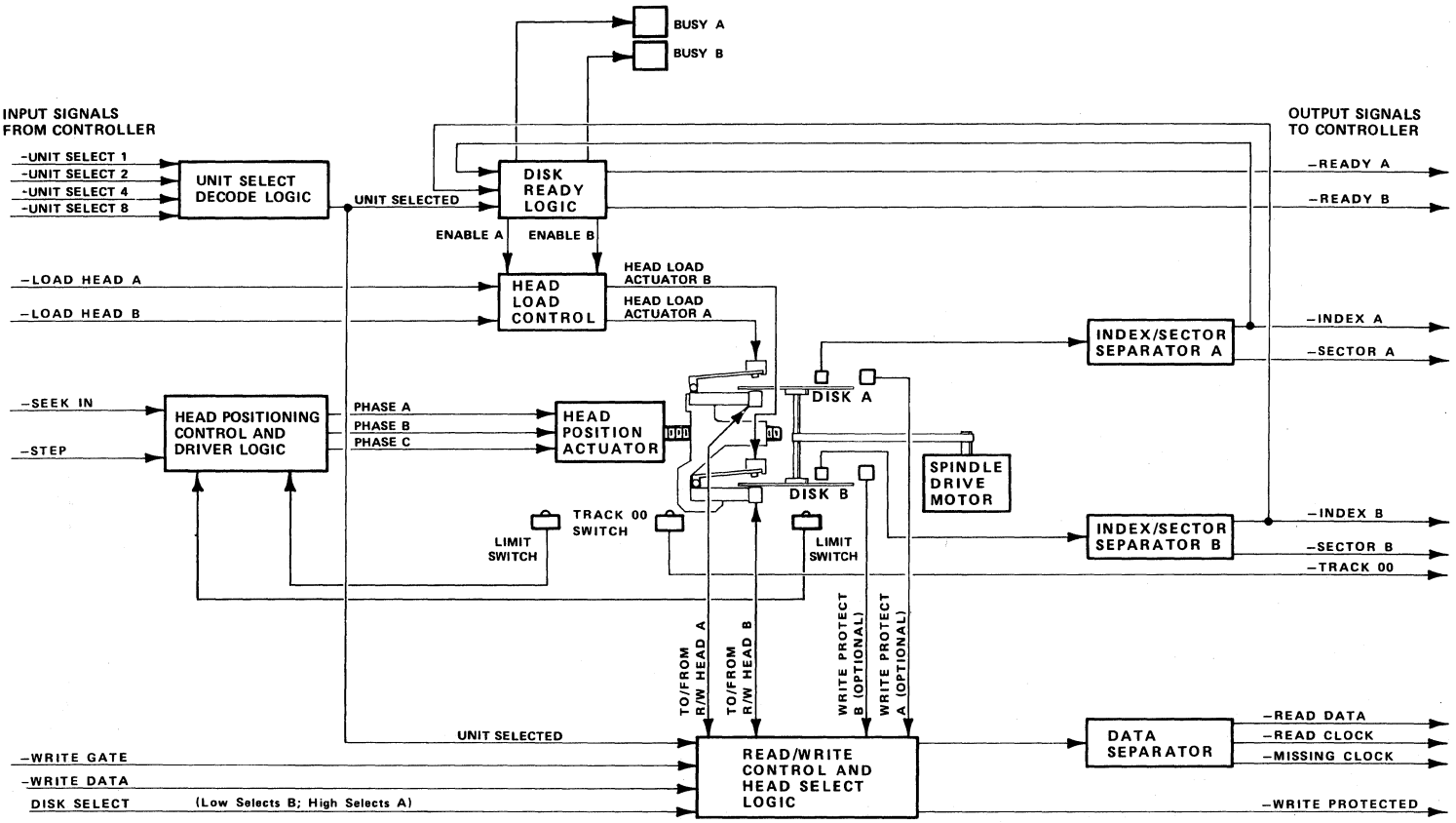


Figure 5-1 MODEL 12 BLOCK DIAGRAM

5.1 GENERAL

This section gives both functional and detailed circuit descriptions of the Model 12 electronics. The functional description does not cover the drive-to-controller interface. This information is presented in Section 3 of this manual.

5.2 FUNCTIONAL DESCRIPTION

Each Diablo Model 12 Flexible-Disk Drive performs the following basic functions:

1. Receives and interprets control information and write data from the host system.
2. Simultaneously positions a pair of Read/Write heads to a new track location.
3. Writes data on or reads data from the selected track under the control of the host system.
4. Transmits data, status and timing signals to the host system.

The drive also performs other functions, such as head loading and track 00 sensing, in support of these

basic activities. All the major functional elements that comprise the Model 12 are illustrated in Figure 5-1 and are listed below:

1. A drive system for rotating two flexible-disk cartridges.
2. Two Read/Write Head Assemblies.
3. Two head loading assemblies.
4. A head positioning mechanism.
5. A track 00 sensing circuit.
6. Two index/sector sensing circuits.
7. Two Write Protect sensing circuits (optional).
8. All associated digital and analog electronics.

5.2.1 Spindle Drive System

The spindle drive assembly consists of two drive hubs mounted on opposite ends of a single drive shaft. The drive shaft extends through the base plate.

The spindle is rotated at 360 RPM (nominal) by an AC motor, using a belt/pulley drive system. The spindle drive motor can be factory equipped for 50 Hz or 60 Hz power by fitting it with an appropriate drive pulley at the time of order.

When a cartridge access door is closed, with a disk inserted, an associated disk centering cone is automatically pressed into the center hole of the disk. The cone assures disk-to-spindle concentricity, while holding the disk clamped against the drive hub. The centering cone is disengaged when the disk cartridge access door is opened. The two cartridge compartments have independent centering cone mechanisms.

5.2.2 Head Loading

The R/W heads are designed to operate in direct contact with the disk surface. This enhances read and write performance by maximizing signal transfer.

Each R/W head is loaded against its disk on command from the control unit. When a cartridge is installed and the disk is rotating at its operating speed, an enable signal from the control unit will cause the associated R/W head to be loaded. A separate head load enable is used for each disk to permit independent loading of the two heads.

Figure 5-2 illustrates the head loading mechanism. When the controller issues the head load enable signal, two pressure pads are brought to bear against the back of the disk. Pad 'A' settles and cleans the disk and pad 'B' applies head load pressure.

The heads are unloaded from both disks whenever the control unit removes the head load enable, a DC power failure occurs, disk speed falls below the minimum operating threshold, or when the cartridge access door is opened.

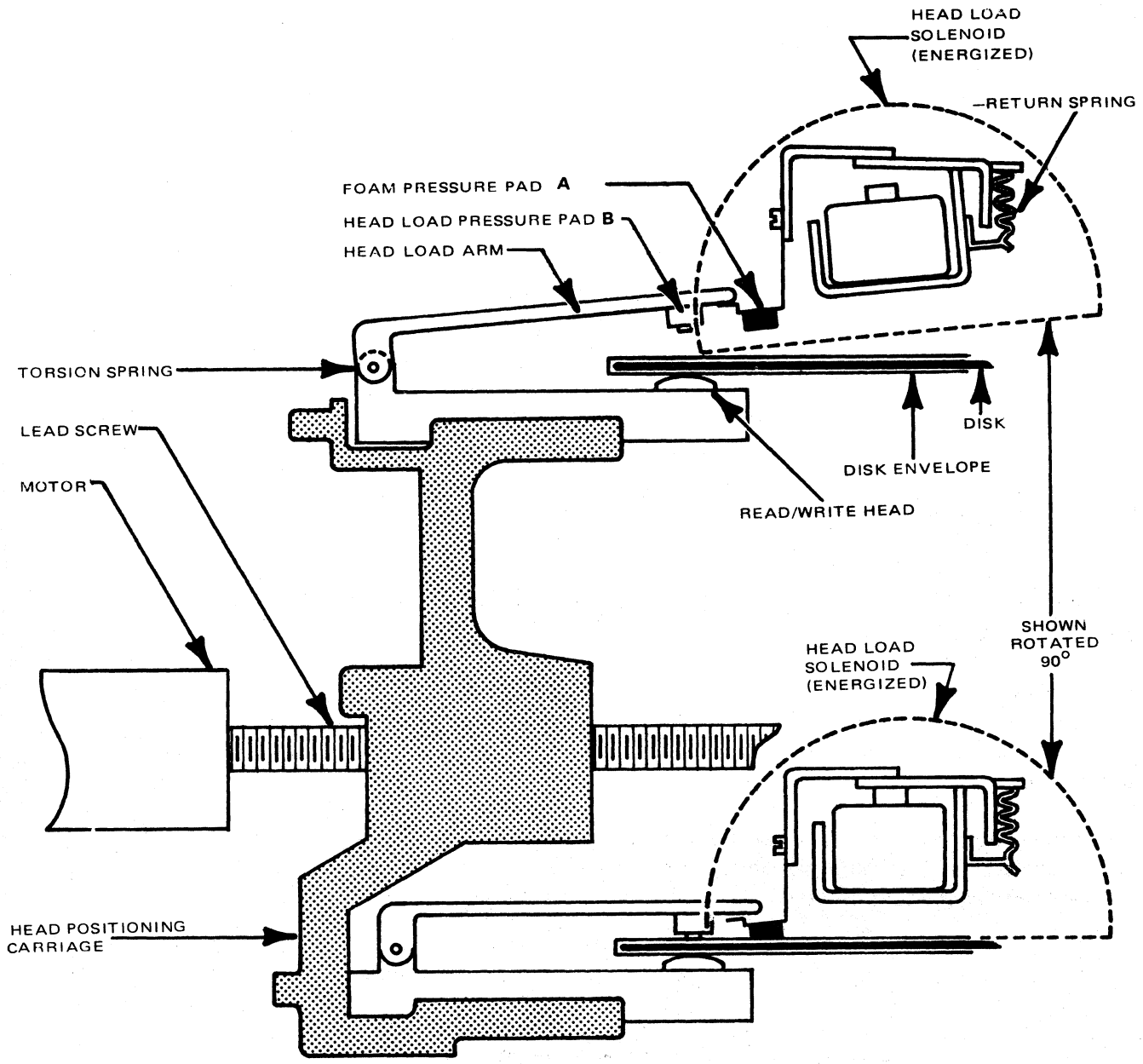


Figure 5-2 HEAD LOAD MECHANISM

When either cartridge access door is opened, the index sensing circuit detects no more index marks. Approximately one disk revolution later, disk speed monitoring logic in the drive determines that the speed of the disk has dropped below the minimum operating threshold and the head is unloaded.

5.2.3 Head Positioning

The two R/W head assemblies are mounted on a carriage which is driven by a head position actuator. The head position actuator moves the R/W heads toward or away from the disk center in one track increments.

The head position actuator consists of a stepper motor and a leadscrew. The stepper motor rotates

the leadscrew clockwise or counterclockwise in 90° increments. Each 90° of rotation corresponds to .508mm (.020 inch) of linear travel, which is equal to the track-to-track spacing.

Direction control and step commands for the stepper motor are provided by the host system.

Note: Continual seeks from track 00 to track 76 to track 00 without read/write operations will make the stepper motor housing hot to the touch.

5.2.4 Index/Sector Sensing

A pair of LED-photo transistor circuits detect the index holes in the two disks. If the hard sector feature is employed, these circuits also detect sector holes in the disks. The output of each detector circuit consists of a series of analog pulses, which are converted to digital (TTL Level) pulses. With the hard sector feature, separation logic in the drive separates each index pulse from the series and forwards the index and sector pulses to the control unit on different interface lines. Each revolution of a hard sector disk produces up to 32 sector pulses and one index pulse.

Note: The number of sectors is determined by the using system, the drive options, and type of disk used.

If the drive is operating in an IBM 3740 Data Entry System, the sector output is disabled by a jumper selection in the drive logic.

5.2.5 Ready Status

Disk speed monitoring logic in the drive tests the period between index pulses to determine whether or not disk speed is above the minimum operating threshold. Separate speed monitoring circuits are provided for each disk.

When the selected disk is rotating at the specified speed (166.7ms per revolution), a Ready Status signal for that disk is sent to the control unit. This ready condition is also used as an internal qualifier for the head load circuits and the index and sector output drivers.

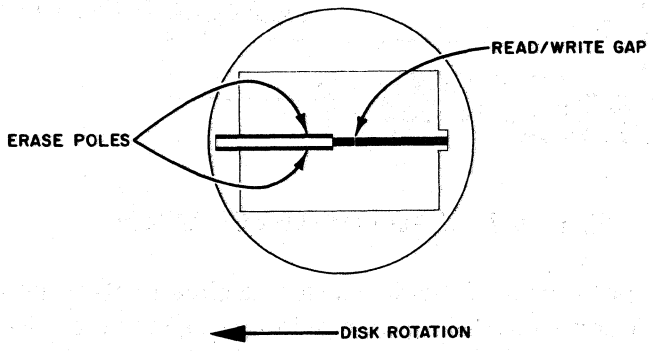


Figure 5-3 READ/WRITE HEAD STRUCTURE

5.2.6 Read/Write Heads and Electronics

Information is recorded on and read from the flexible disks by a pair of ceramic/ferrite read/write heads. The R/W head assemblies include tunnel erase poles for side trimming the data tracks. See Figure 5-3. These erase poles narrow each track to 0.012 inch. This provides sufficient separation between tracks to

compensate for the minor head positioning tolerance that is characteristic of interchangeable disk systems.

The drives head select and read/write functions are controlled through a pair of interface lines disignated "Disk Select B" and "Write Gate".

Note: Details regarding all interface lines are provided in Section 3 of this manual.

One head or the other is enabled according to the logic level present on Disk Select B. If Write Gate is active, the selected head is enabled for writing; otherwise, it is enabled for reading.

The Write logic converts clock and data pulses received from the control unit into current reversals in the read/write head. These are recorded on the disk surface as a series of polarity reversals, with the same timing relationships as the original clock/data pulses.

In the read mode (Write Gate is inactive), the read/write head transforms these polarity reversals into a read signal. This signal, consisting of a series of analog pulses, it applied to the drive's read channel.

The read channel amplifies the raw read signal, filters attendant noise and converts each analog pulse into a TTL-compatible digital pulse.

In the final stages of the read channel, the data and clock pulses are demultiplexed and forwarded to the control unit on separate lines (Read Data and Read Clock) if the data/clock separator is implemented. In the standard drive the data and clock pulses are sent to the control unit serially, just as they had been received from the control unit.

The read channel also provides the control unit with a pulse output designated Missing Clock. A pulse is sent to the control unit on this line each time the read channel detects a gap in the stream of Read Clock outputs. See Figure 5-4.

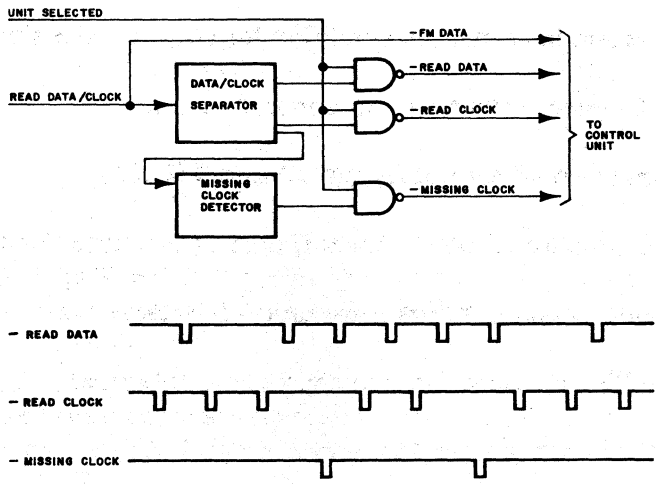


Figure 5-4 SAMPLE READ DATA/CLOCK/MISSING CLOCK OUTPUT

Note: The user is expected to delete predetermined clock pulses from the address mark sigments of the write data when soft sectoring is used. These missing clocks assure that the address mark bit patterns are absolutely unique. Details regarding this use of missing clocks are provided in Section 4, Disk Formatting.

5.2.7 Write Protect Option

The Write function may be disabled for either or both disks by implementing the drive's Write Protect sensing circuits. These circuits consist of two LED-photo transistor detectors, one for each disk cartridge. If a disk is Write Protected, the associated detector senses a write protect feature on the disk's envelope. An internal signal generated by the sensor circuit then disables the write current path whenever the disk is selected for a Write operation. The drive also issues a Write Protect status signal to the control unit whever a protected disk is selected.

5.2.8 Track 00 Sensor

A switch, which is mounted on the baseplate, provides a "home position" signal when the R/W heads are located at Track 00. This signal is forwarded to the control unit, where it is used as a head position reference.

5.2.9 Front and Rear Limit Sensors

Two switches, which are mounted on the baseplate, limit head carriage travel in either direction due to improper positioning commands from the control unit. If a limit switch is made the direction of carriage travel is reversed.

5.3 CIRCUIT DESCRIPTIONS

The following paragraphs provide electrical characteristics and circuit descriptions for circuits found on the Model 12 PC Board. The functions described are as follows:

Note: Side A = Lower disk and
Side B = Upper disk.

1. On both sides A and B, detect index marks and provide index signals to the interface. For hard sectoring, detect sector marks and separate sector and index signals.

2. Generate ready status and indicate busy condition for both A and B sides.

3. Provide stepper motor drive current for appropriate stepping.

4. Provide the head load solenoid current for both A and B sides.

5. Detect Write Protect condition on both A and B sides and inhibits "Write" when appropriate.

6. Provide gating to input and output lines when unit is selected.

7. Provide "Write" and "Erase" current to the appropriate R/W head.

8. Select appropriate R/W head, process the readback signal and generate F.M. data pulses.

9. Decode F.M. data pulses, provide separated data and clock pulses and detect absence of clocks.

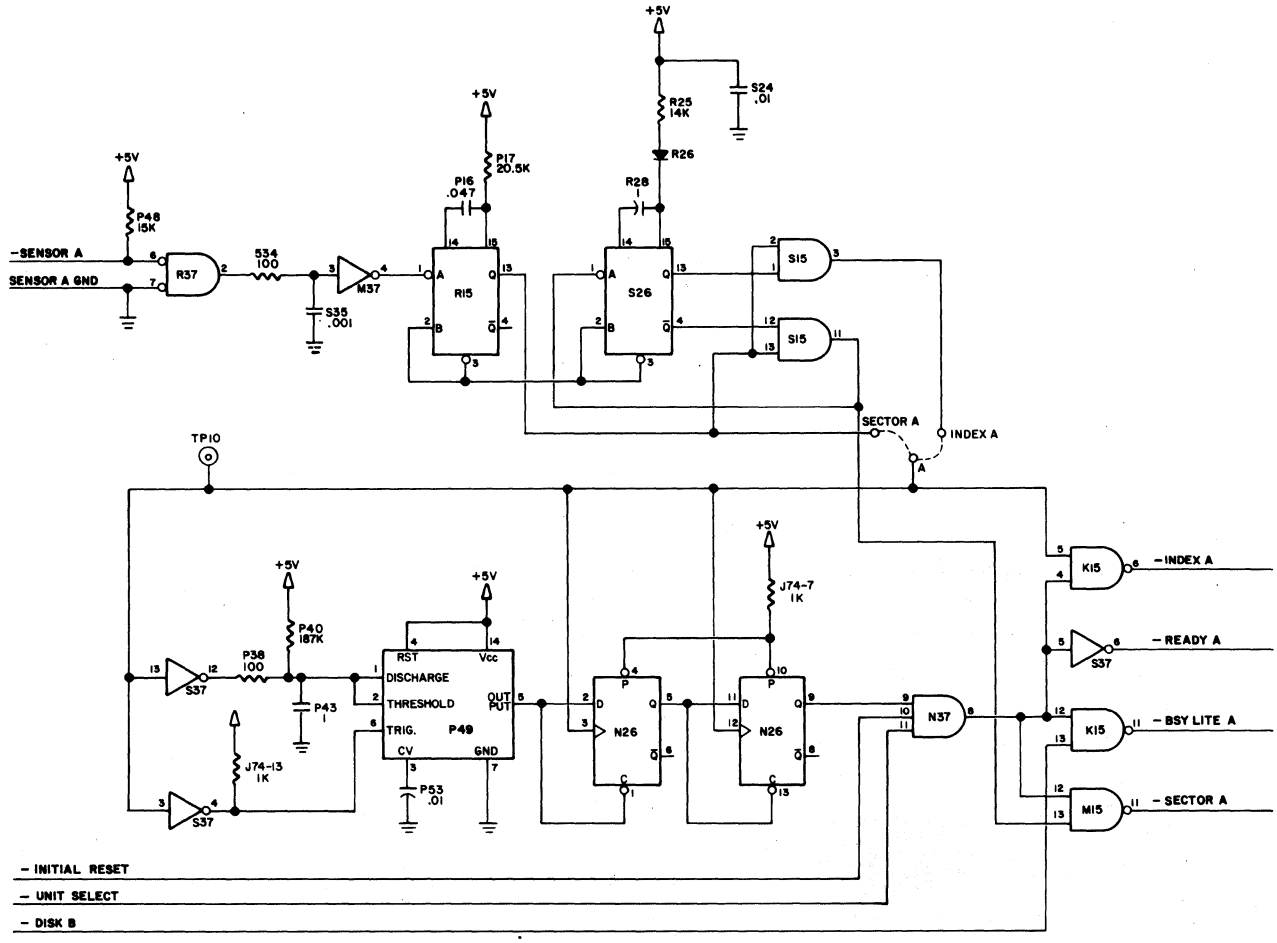


Figure 5-5 INDEX/SECTOR MARK-STATUS DETECTION AND BUSY INDICATION (SIDE A)

5.3.1 Index and Sector Mark Detection

The index and sector holes on a diskette are detected by a phototransistor towards which a beam of light from an infrared LED is aimed.

Refer to Figure 5-5. Due to the opaqueness of the diskette, the phototransistor has little light incident on it and is therefore cut off. Its collector is pulled up to +5V through a 15K resistor (P48).

As the diskette rotates, the index/sector holes permit the LED light beam to reach the phototransistor, turning it on, and pulling the collector LO. This LO (–Sensor A) to fed to an 8836 line receiver (R37-6).

Due to the slow transition period of the –Sensor A signal (about 400μsec) the output of the receiver is filtered and buffered by a Schmidt trigger inverter circuit (S34, S35 and M37) to obtain a clean TTL signal.

On the negative going edge of the inverter output (M37-4) a one-shot (R15) is triggered. The output

of the one-shot (R15-13) is the sector/index signal with a duration of 280 ± 80μsec.

For soft sector diskettes, only index signals are generated. This is accomplished by installing a jumper from "Index A" to "A". This bypasses index/sector separation circuitry.

With hard sector diskettes, index and sector pulses are generated by installing a jumper from "Sector A" to "A". Index/sector separation is accomplished by examining for an index pulse occurance with a "window" period of 3.67 ± 0.8msec after each sector pulse. The one-shot that sets up the window (S26) is inhibited from retriggering during that period.

Separated sector pulses are gated to I/O pin 34 when the unit is selected, has ready status, and the initial reset period is over.

Index pulses are gated out to I/O pin 30 when the unit is selected, has ready status, and the initial reset period is over.

The index signals are brought out to test points (TP10, A side and TP11, B side) for both hard and soft sectored drives.

Note: The index/sector separation scheme implies and requires that the index hole be located in relation to the preceding sector hole, less than 2.6msec away. (This is approximately 0.15 inch from leading edge to leading edge of the holes.) This applies irrespective of the number of sector holes and their location on the disk.

5.3.2 Ready Status Detection and Busy Indication

A "Ready" status is generated if index pulses occur at periods of less than 175msec for at least two revolutions of the disk.

See Figure 5-5. A timer (P49) is used to test the ready condition. During index, a 1μF capacitor (P43) is discharged. After index, the capacitor is allowed to charge through 187K resistor (P40) to +5V. At the leading edge of the next index pulse, the charged voltage level of the capacitor is examined. If the level has exceeded the threshold level of the timer, index pulses are judged to occur at periods greater than 175msec. The output of the timer is then set LO, clearing two "D" type flip-flops (N26) to inhibit the ready condition. The capacitor is discharged again and the cycle repeats.

When the charged voltage level of the capacitor, examined at every index signal, is below the threshold voltage of the timer, the output of the timer goes HI. The HI is transferred across the "D" type flip-flops on the succeeding two index pulses, to set the ready condition. Thus, at the end of two revolutions of the disk, i.e. two index pulses, the ready condition is gated to the interface, (I/O pin 26) when the unit is selected, and the initial reset period is over.

A busy indication is provided on the front panel when ready status exists on the side (A or B) that is selected by the host system.

Notes: (1) The busy light does not indicate actual operations of Ready, Write or Seek, but only that a Read/Write operation may be in progress.

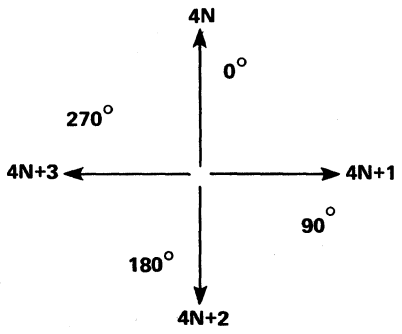
(2) "Ready" is a status indication. If Ready status is not present, only index and sector signals are not gated to the I/O outputs. Read, Write, and Seek operations are not

inhibited. Also, while Read and Write operations require index signals, a seek operation does not.

(3) "Ready" status is not an RPM indicator and can not detect a disk overspeed condition. It serves only to indicate disk rotation, and indirectly, that doors are closed and the diskette is engaged and rotating without excessive slippage.

5.3.3 Stepper Motor Drive Circuitry

The stepper motor is a four phase permanent magnet type. The four stable (detent) positions of the motor for different phases are shown in Figure 5-6.



TRACK POSITION (Stable)	SHAFT POSITION	PHASES ENERGIZED A	B	C	D
4N	0°	OFF	OFF	ON	ON
4N+1	90°	ON	OFF	OFF	ON
4N+2	180°	ON	ON	OFF	OFF
4N+3	270°	OFF	ON	ON	OFF

NOTES:
1) N = 0, 1, 2, - - - 18.
2) 0° – Track positions 0, 4, 8, 12, - - - 72, 76.
3) Track-to-track spacing is .020" or 90° rotation of lead screw.

Figure 5-6 STEPPER MOTOR PHASES

Refer to Figure 5-7. At power on, the initial Reset one-shot (K37) is fired and its output (K37-12) clears the two "D" type flip-flops (M59) making –A (M59-5) and –D (M59-9) LO. Base bias is now provided to two motor drive transistors (N75 and P75). Also at power on, detent one-shot (K37) is fired, turning on transistor (M75).

Phases "A" and "D" of the stepper motor are energized. If the motor were positioned at 4N, 4N+1, or 4N+2, it moves to, or stays at, the 4N+1 position. The motor may or may not move from the 4N+3 position to 4N+1. However, the first following step will move the stepper to the proper position.

The D-inputs to the flip-flops (M59-2 and M59-12) represent the next active state of phases A and D, clocked in on the leading edge of –Step command.

(Next –A State) : (Present –B State) + (Seek In)
(Next –D State) : (Present –A State) + (Seek In)

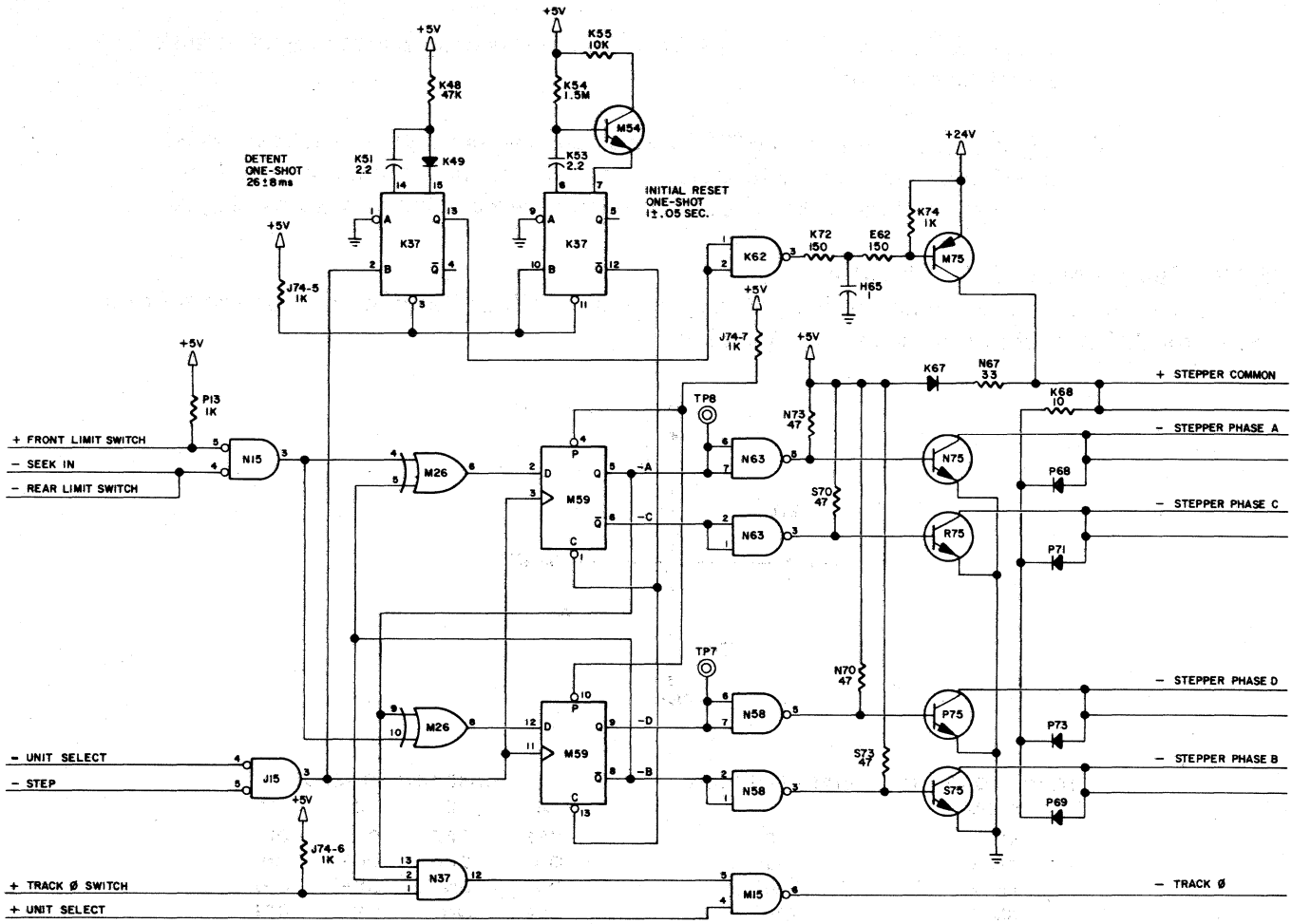


Figure 5-7 STEPPER MOTOR DRIVE CIRCUITRY AND TRACK 00 INDICATION

At the leading edge of –Step command, the detent one-shot (K37) is fired for 26 ± 8msec. The gate output (K62-3) goes low, turning transistor (M75) on. The next phase states are also clocked into flip-flops (M59) whose outputs turn on the appropriate driver transistors (N75, R75, P75, S75). 24Vdc is now applied to the appropriate phases and the stepper motor steps. If step commands follow within the detent one-shot period (but greater than 10msec), the one-shot is retriggered, the following phase states are clocked in, and successive stepping occurs.

When the detent one-shot times out after the last step pulse, transistor (M75), deprived of base forward bias, turns off. R-C network (K72, H65) is used to slow the turn-off speed of the transistor. Holding current is now provided from +5Vdc to the stepper motor through a resistor (N67) and a diode (K67).

5.3.4 Track 00 Indication

Refer to Figure 5-7. Closure of the track 00 switch is gated (N37) with the –A and –B outputs of the "D" flip-flops (M59-5, M59-8) to indicate track 00 to the interface. This gating with –A and –B makes the adjustment of the track 00 switch non-critical.

5.3.5 Front and Rear End-Stop Protection

To prevent the R/W head carriage from trying to move beyond its physical limits, front and rear limit switches have been provided.

When the rear limit switch is closed, the –Seek In signal is pulled low. A Step command pulse will now step the positioner inward (toward the spindle).

The +Front Limit Switch signal is gated with –Seek in (OR-gate function) so that when the front limit switch is closed, a step command will step the positioner outward (away from the spindle).

5.3.6 Head Load Solenoid Operation

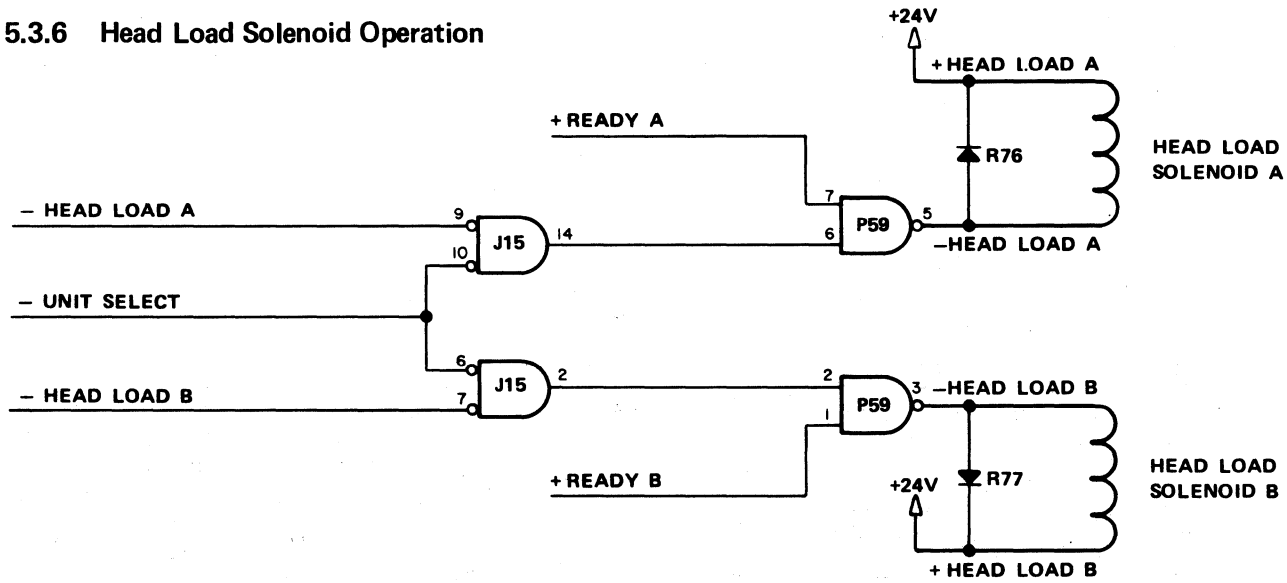


Figure 5-8 HEAD LOAD SOLENOID CIRCUITS

Refer to Figure 5-8. For a R/W head to be loaded requires that the unit be selected and that head load and ready signals be active.

To energize the solenoid, the gate outputs (P59-5, P59-3) are pulled low, drawing current from +24Vdc through the appropriate solenoid.

5.3.7 Write Protect Detection

Write Protect detection is similar to detection of index marks. See Figure 5-9. A write protected diskette has a hole in the disk envelope. LED light shining through the hole turns on a phototransistor, pulling its collector LO, indicating a write protected condition. This write protected condition is gated through, if that disk is selected, to the interface (H15-3). Also, the output of a gate (B26-5) is forced HI, preventing transistor (A25) from turning on and thus inhibiting write or erase current.

5.3.8 Daisy-Chain Capability

Signals are gated to the twelve interface output lines only if the unit is selected, to permit daisy-chaining of up to four units. The units are identified by installation of a jumper wire in one of the four 'Unit Select' locations on the PC Board.

Seek, write and head load functions are inhibited until the unit is selected (–Step, –Write Gate, –Head Load A and –Head Load B are gated on Unit Select). However, if one of the units head carriage has been

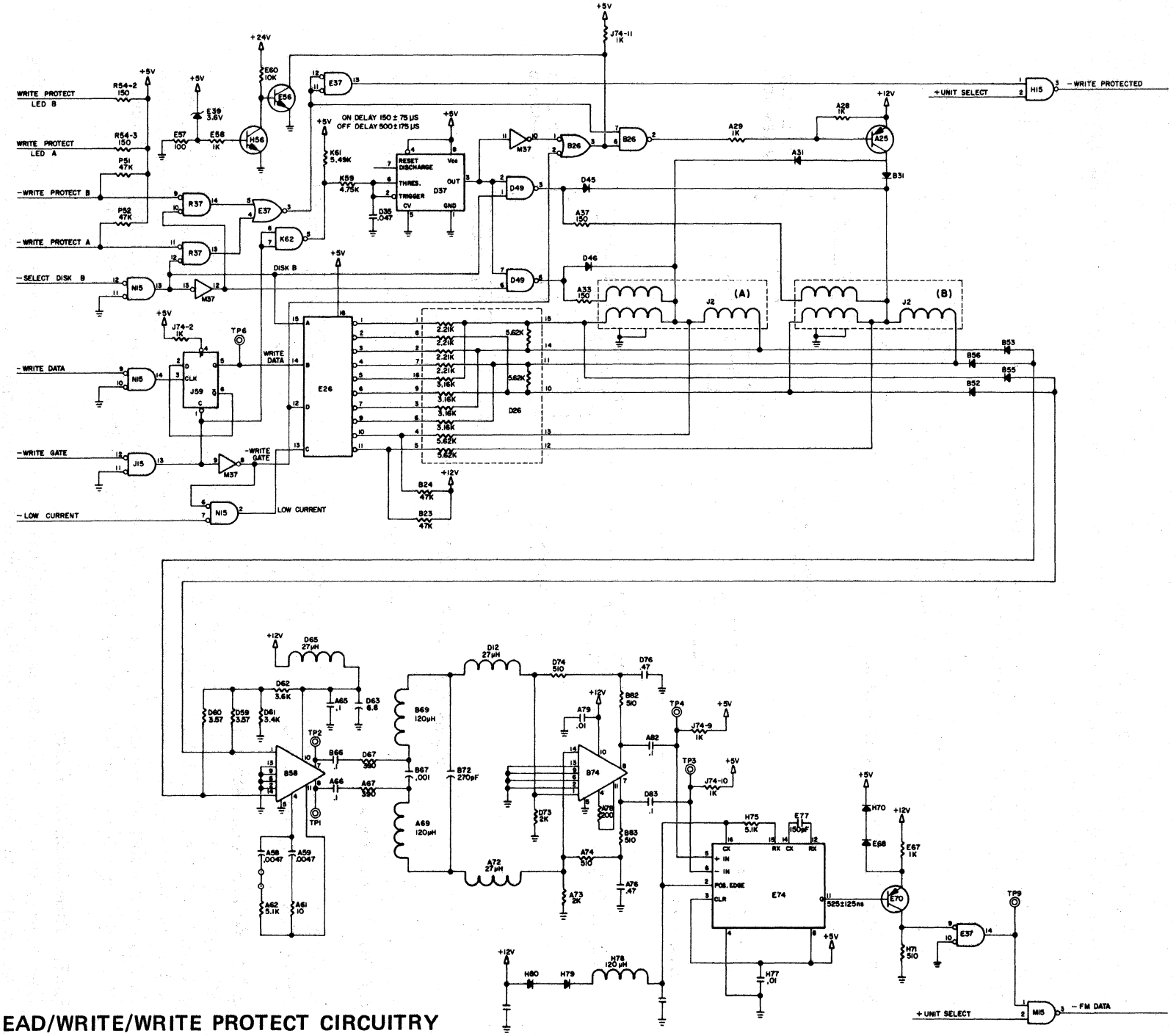


Figure 5-9 READ/WRITE/WRITE PROTECT CIRCUITRY

mispositioned by the controller, and the rear limit switch is made, all of the –Seek In inputs on the buss are pulled low. A step command, to any unit, will result in a forward seek only (toward the spindle) until the mispositioning is corrected.

5.3.9 Write Circuitry

Refer to Figure 5-9. When –Write Gate goes LO, the unit is selected, and a Write Protect condition is not present,, transistor (A25) is turned on. This provides approximately 11 volts to the center tap of both Read/Write heads.

A timer circuit (D37) is designed to provide an output which follows Write Gate (J15-13), delayed, on the leading edge by 150 ± 50 microseconds and on the trailing edge by 500 ± 175 microseconds. This delayed Write Gate output is Erase Gate, and is required due to the physical separation of write and erase poles on the R/W head.

Erase current of approximately 75ma is enabled for Head A by Erase Gate and $\overline{\text{Select Disk B}}$, and for Head B by Erase Gate and Select Disk B.

This selection of the Write current and appropriate R/W head are set by the input lines to a ONE to TEN decoder (E26). Refer to Figure 5-10. The inputs to the decoder are + Disk B (N15-13), + Write Data (J59-5), + Low Current (N15-2) and –Write Gate (M37-8).

Write current is approximately 7 ma peak-to-peak with –Low current LO and 10ma peak-to-peak with –Low current HI.

Figure 5-11 is a flow diagram of a Write operation with disk B selected.

5.3.10 Read Circuitry

Refer to Figure 5-9. Head selection is made by the status of the input lines to the one-to-ten Decoder (E26). When Write Gate is false, Write Data and Low Current inputs to the decoder are also forced LO. The state of +Disk B input determines if E26-10 or E26-11 is pulled LO.

The selected head center top voltage is about 6 volts and the unselected head center top voltage is about 12 volts. The recovered signals are 3mV peak-to-peak maximum. The first gain stage (B58) performs differentiation of the signal placing the recovered information, contained in the signal peaks, into the signal baseline crossovers. Phase compensation is also provided to compensate for pulse pairing of the read-back signal. Gain is about 40 for 1F and 70 for 2F. The output of the first gain stage is a four pole Bissel (linear phase) filter to reduce the high noise components.

The second gain stage (B74) amplifies and acts as a limiter. Gain is approximately 70.

The baseline crossovers are now detected by a bidirectional one-shot (E74-5 and E74-6) and pulses of 525 ± 125ns duration are generated (E74-11).

The read signal circuitry operates from ground to +12 volts. The pulses generated by the bidirectional one-shot are voltage translated by transistor (E70) and gate (E37). The output (M15-3) is –F.M. Data.

5.3.11 Data and Clock Separation, Detection of Missing Clocks

Data separation is accomplished by a two time constant technique that recognizes the conditions for pulse pairing and shortens the data window accordingly.

1 TO 10 DECODER (E-26)

A = Disk B

B = Write Data

C = Low Current

D = Write Gate

1. Select Disk B with J59 Set: (Write Mode)

A	B	C	D	1	2	3	4	5	6	7	8	9	10	11
H	H	L	L	H	H	H	L	H	H	H	H	H	H	H

2. Select Disk B with J59 Reset: (Write Mode)

A	B	C	D	1	2	3	4	5	6	7	8	9	10	11
H	L	L	L	H	L	H	H	H	H	H	H	H	H	H

3. Select Disk A with J59 Set: (Write Mode)

A	B	C	D	1	2	3	4	5	6	7	8	9	10	11
L	H	L	L	H	H	L	H	H	H	H	H	H	H	H

4. Select Disk A with J50 Reset: (Write Mode)

A	B	C	D	1	2	3	4	5	6	7	8	9	10	11
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H

5. Select Disk B: (Read Mode)

A	B	C	D	1	2	3	4	5	6	7	8	9	10	11
H	L	L	H	H	H	H	H	H	H	H	H	H	H	L

6. Select Disk A: (Read Mode)

A	B	C	D	1	2	3	4	5	6	7	8	9	10	11
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H

Figure 5-10 DECODER INPUTS/OUTPUTS

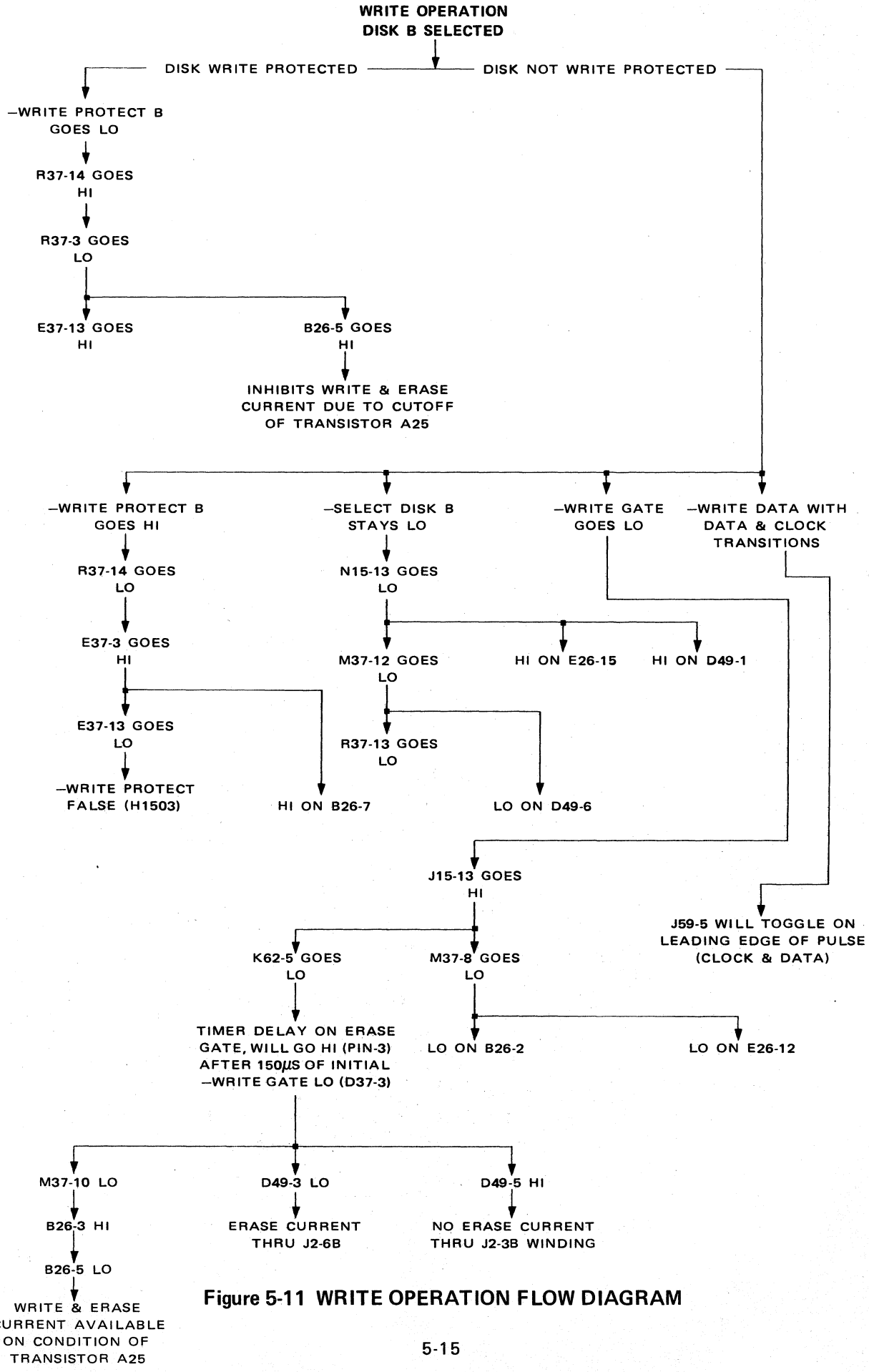


Figure 5-11 WRITE OPERATION FLOW DIAGRAM

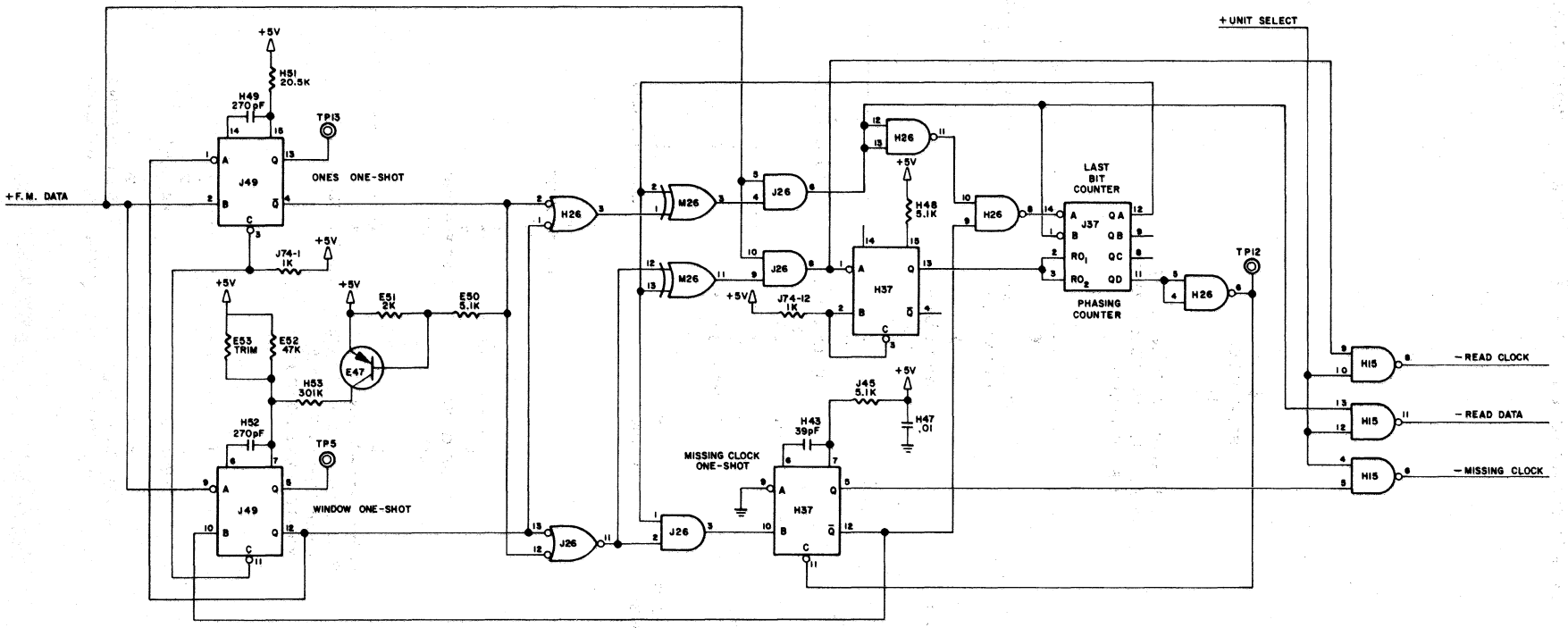


Figure 5-12 DATA/CLOCK SEPARATOR AND MISSING CLOCKS CIRCUITS

Refer to Figure 5-12. Each FM data pulse triggers (or retriggers) the window one-shot (J49-5). The output state of the one-shot (J49-12) and the last bit counter (J37-12) open the appropriate clock window (M26-11) or data window (M26-3). Each clock bit recognized in the clock window is gated out as —Read Clock, resets the last bit counter, and closes the clock window on its trailing edge. Each data bit recognized in the data window is gated out as —Read Data, and on its trailing edge, sets the last bit counter and closes the data window.

A ONES one-shot is fired on the leading edge of FM Data, if the last bit was a "one", for a period of 1.8 ±0.4 μs. During this period transistor (E47) is turned on, shunting the window one-shot timing resistors (E52/53) and thus shortening the window one-shot period by 250 ±150ηs.

The ONES one-shot output also serves as a masking function, permitting the window one-shot to time out before the FM data pulses trailing edge occurs.

If the Last Bit Counter is set, indicating that the last pulse was a data pulse, and no other FM data pulse has been detected for the period of the window one-shot, then, when the one-shot times out, Missing Clock one-shot (H37-5) is fired for a period of 180 ±80ηs. The pulse is gated out (H15-6) as —Missing Clock. On the trailing edge of +Missing Clock, the Last Bit Counter (J37) is reset, opening the data window.

With only data pulses and no clock pulses to reset the phasing counter, the counter counts up. On the fourth data bit, the missing clock one-shot (H37-5) is held cleared, inhibiting the next missing clock. The Last Bit Counter is thus not reset, and the next bit is detected as clock, thereby rephasing the clock and data windows.

5.4 TEST POINTS

Seventeen test points are provided on the PC Board to aid in the troubleshooting of circuits. Three test points, TP15 through TP17, are labeled GND to provide oscilloscope probe grounding points.

The functions of test points TP1 through TP14 are as follows:

1. TP1 and TP2 — Read channel first gain stage differential ouputs. The amplified and differentiated read signals can be examined at these test points in differential mode.

2. TP3 and TP4 — Read channel bidirectional one-shot inputs. Read signals from the outputs of the second gain stage can be examined at these test points in differential mode.

3. TP 5 — Window one-shot output in Data/Clock separator circuit. The window one-shot triggers and retriggers on FM Data pulses. The one-shot time period, in conjuction with +FM data pulses at TP9, should be examined and the trim resistor (E53) should be selected so that the time period from the leading edge of FM Data pulse to the trailing edge of window one-shot is a period of 3.0 ±0.1μs. (See Figure 5-13)

4. TP6 — Write Data. Double frequency encoded write data pulses can be examined at this test point.

5. TP7 — Stepper Motor, Phase 'D' state. If this signal is HI, Phase 'D' is inactive and Phase 'B' is active. When LO, Phase 'D' is active and Phase 'B' is inactive.

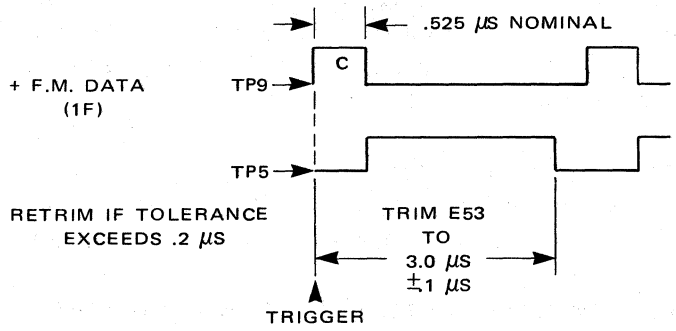


Figure 5-13 WINDOW ONE-SHOT TIMING

6. TP8 – Stepper Motor, Phase 'A' state. This point will be HI if Phase 'A' is inactive and Phase 'C' is active, and LO if Phase 'A' is active and Phase 'C' inactive.

7. TP9 – +FM Data. The signal at this point will be a stream of clock and data pulses (TTL levels) when a head is selected, Write Gate is HI, and the head is loaded on a recorded media.

8. TP10 – +Index 'A'. This signal is a pulse with a period of 280 ±80µs every revolution (167ms nominally) of the diskette installed in Side 'A'.

9. TP11 – +Index 'B'. This signal is a pulse with a period of 280 ±80µs every revolution of the diskette installed in Side 'B'.

SECTION 6

MAINTENANCE

6.1 GENERAL

The Diablo Series 10, Model 12 Disk Drive is designed to be as maintenance free as possible. All components are used well below their design limits, and all moving parts are controlled electronically.

6.2 MAINTENANCE PHILOSOPHY

The objective of maintenance is to provide maximum utilization of the machine with minimum down time. Unless a preventive maintenance operation increases drive availability, it is unnecessary. Properly functioning equipment is best left alone. In the event of a problem, isolated to the drive, field maintenance philosophy is "on-line diagnosis; rapid off-line repair; and on-line check-out". Should a repair become necessary, the design of the drive's modular parts assures a quick return to service.

The semi-annual preventive maintenance session on the Model 12 is a visual inspection. Do not alter any adjustment on equipment that is performing at a satisfactory level.

6.2.1 Visual Inspection

Visually inspect the drive for corrosion, dirt, wear, loose wiring connectors, hardware, heads, etc. Noting these items and taking appropriate action will result in minimizing if not preventing future down-time altogether.

6.2.2 Cleaning

Cleanliness is important in disk storage devices. Flexible-disk drives are no exception. Slight accumulations of dust, dirt, or other deposits on read/write heads can result in failures to the drive or to the media being used in the drive.

Cleanliness and care in handling the flexible disk media is also important. Damage to the disk can occur from finger prints, exposure to sunlight, magnatized objects, severe bending, dirt, dust, oil, etc. Therefore, it is important that the disks be returned to their jackets and stored in a safe place, such as their shipping container or equivalent.

Note: Incorrect operating procedures, faulty programing, damaged media and "soft errors" caused by airborn contaminants, random electrical nose, and other external causes can produce errors falsely attributed to drive failure or misadjustment. Unless visual inspection of the drive discloses an obvious misalignment or broken part, attempt to repeat the fault with the original diskette, then attempt to duplicate the fault on a second diskette.

6.3 PREVENTIVE MAINTENANCE

Operating the Model 12 Flexible-Disk Drive in a normal office environment on a one-shift basis generates a need for preventive maintenance at a six-month interval. Operating the drive in a high dust/dirt environment will shorten the preventive maintenance interval.

6.3.1 Preventive Maintenance Action

Preventive maintenance actions recommended are shown in Table 6-1.

TABLE 6-1

PREVENTIVE MAINTENANCE — 6 MONTH INTERVAL

AREA	ACTION
Read/Write Heads	Clean and inspect for scratches and build-up of oxide. Clean with 91% isoprophyl alcohol (or equivalent) using a lint free wiper to remove any residue. For best results, complete removal of all contamination is necessary.
Carriage Lead Screw and Guide Rods	Clean and inspect. If mispositioning occurs on long seeks, relubrication will usually correct the problem. Oil lightly with Diablo #70655 oil. See caution note below.
Spindle Assembly/Cone Area	Clean and inspect. Remove particles, as required, using adhesive tape.
Base Plate and Doors	Clean and inspect for loose hardware.

[CAUTION]

Do not over Lubricate. Oil is needed only on the head carriage lead screw and guide rods, and only in small quantities. Over lubrication will cause contamination in the drive and of the media.

6.4 DIAGNOSTIC TECHNIQUES

The simple design of the Model 12 PCB assembly levels itself to easy diagnosis of suspected trouble areas.

6.4.1 Error Analysis and Data Collection

Disk system problems are frequently resolved by analyzing error patterns.

To obtain an error pattern, a comprehensive record of troubles must be maintained and analyzed. The following error patterns may appear:

1. Errors which transfer from drive to drive with a particular disk — suspect the disk cartridge.
2. Errors occuring in several disk drives associated with a particular control unit — suspect the control unit.
3. Errors occuring on several disk cartridges written on one disk drive — suspect the disk drive unit.
4. A read error may have been created when the data was written.

A system of disk identification and error data collection is encouraged.

6.4.2 Visual Analysis

Inspect the disk and disk drive for dirt or clumps of oxide when data handling problems occur. Dirt

and oxide can usually be removed by wiping the area with a clean lint-free wiper moistened with 91% isopropyl alcohol.

Do not attempt to use a damaged disk or read/write head to recover data. A practice of this kind will result in compounding the problems. It is much better to replace a defective cartridge than to attempt to use it in another drive, which may result in damage to the second drive.

6.4.3 Troubleshooting

The following simplified procedures should be used to determine whether the Model 12 is malfunctioning or whether the malfunction is being caused by some other reason. During the warranty period, additional troubleshooting or repair should not be performed. Diablo Customer Service should be contacted for servicing assistance, instructions, or for return of the unit to the nearest Repair Depot.

When an operating difficulty is encountered, check the software in the controlling system, the diskette, and the operating system control inputs to the Model 12.

Verify the following:

1. That power and I/O cable connections are made properly.

2. The unit select jumper is installed in the correct position.

3. With a test disk installed, monitor that Index/Sector is operating at TP10 for 'A' and TP11 for 'B', and at the I/O connector, Pin-30 for –Index A, Pin-34 for –Sector A, Pin-32 for –Index B and Pin-36 for –Sector B. Index pulses occur once every 166.7 milliseconds. Pulse width is 0.3 millisecond.

   Note: Without Index/Sector, data handling is not possible.

4. A ready signal is presented to the interface after three revolutions of the disk at Pin-26 for –Ready A and Pin-28 for –Ready B.

5. State Register, TP7 and TP8, should have level changes when Step pulses are initiated from the Controller. During this time the carriage should be moving either forward or reverse.

6. That head loading (either A or B) occurs within 40 milliseconds after the command is received from the Controller. Verify as follows:

   a) Insert a head alignment disk or a pre-written disk with data written on track 00.
   b) Initiate a Restore Command to position the carriage to track 00.
   c) Sync a scope on head load input line, interface Pin-20 for –Head Load A or Pin-22 for –Head Load B and set the time base for 10MS/div.
   d) Connect scope channels A and B to TP1 and TP2 (Read Data). Set the scope inputs to Add and invert one input.
   e) Energize the head load solenoid and observe the Read signal. It should be at full amplitude within 35 milliseconds.

      Note: If the Read signal occurs beyond 40 milliseconds, the head load solenoid should be replaced.

7. That a read channel operates, load both heads A and B. Swap head connectors and do a read operation on both sides. This can also be done to verify that both heads are functional. Be sure to return the head connectors to their proper location.

8. That a write operation can take place. Write a known data pattern onto either side. If an error occurs, it will be detected on the next revolution by doing a read operation, commonly called a "Write Check". If an error is present, a write/read operation should be attempted on another track to determine if the media or the drive is failing. If the error persists, the disk should be swapped and the above procedure repeated. If the failure still exists, consider the drive defective. If the failure disappears, consider the original disk defective and discard it.

6.4.4 Field Service Alignment Disk

An alignment disk for the Model 12 should contain the following information:

1. IBM format on track 00.
2. A sector burst pattern on tracks 01 and 76.
3. Head alignment lobe pattern on track 38.
4. 2F data on track 75.

6.4.5 Field Service Aids

Field Service Aids covering a variety of operating and service problems are regularly prepared and distributed by Diablo Customer Service.

6.5 REMOVAL, REPLACEMENT AND ADJUSTMENT OF SUBASSEMBLIES

The following paragraphs cover field service replacement of subassemblies for the Model 12. Refer to Figures 6-1a and 6-1b for locations of major assemblies.

Note: If any problems occur in the stepper motor/carriage area of the drive, it should be returned to Diablo Customer Service for repair.

6.5.1 Tools and Test Equipment Required

The following tools and test equipment are required to perform corrective maintenance on the Model 12.

1. Oscilloscope, Vbw 15MHz, Vds 100mV/cm, Sweep Speed 50ηs/cm.
2. Soft sectored, IBM compatable formatted disketts and/or hard sectored disketts with 32 sector holes.
3. Alignment diskette.
4. Deep socket driver, 7.0mm.
5. Combination off-set open and box wrench, 10.0mm.
6. Open end wrench, 8.0mm.
7. Allen hex drivers, 1.5mm, 2.0mm, 2.5mm and 3.0mm.
8. Torque wrench, with a 4 inch ounce sitting, able to accept a screw driver bit.
9. Snap Ring pliers.

Note: The paragraphs below follows the sequence suggested for disassembly of the drive. A complete disassembly is seldom required, however, and since the design of the drive lends itself well to partial disassembly for servicing major assemblies, the user may excerpt only those portions of this sequence of immediate interest. Power should be off and power and I/O cables disconnected.

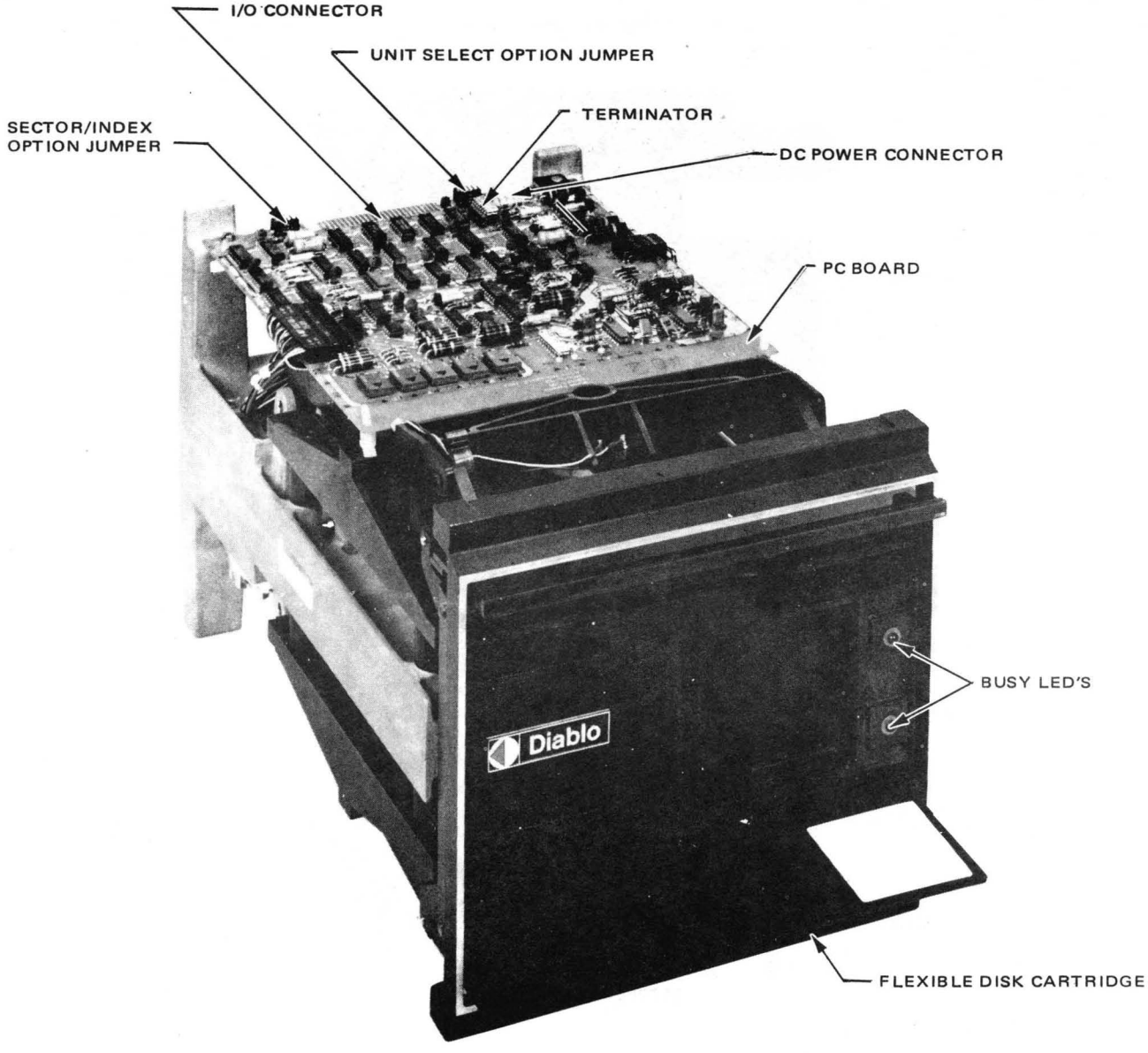


Figure 6-1a MAJOR ASSEMBLY LOCATIONS

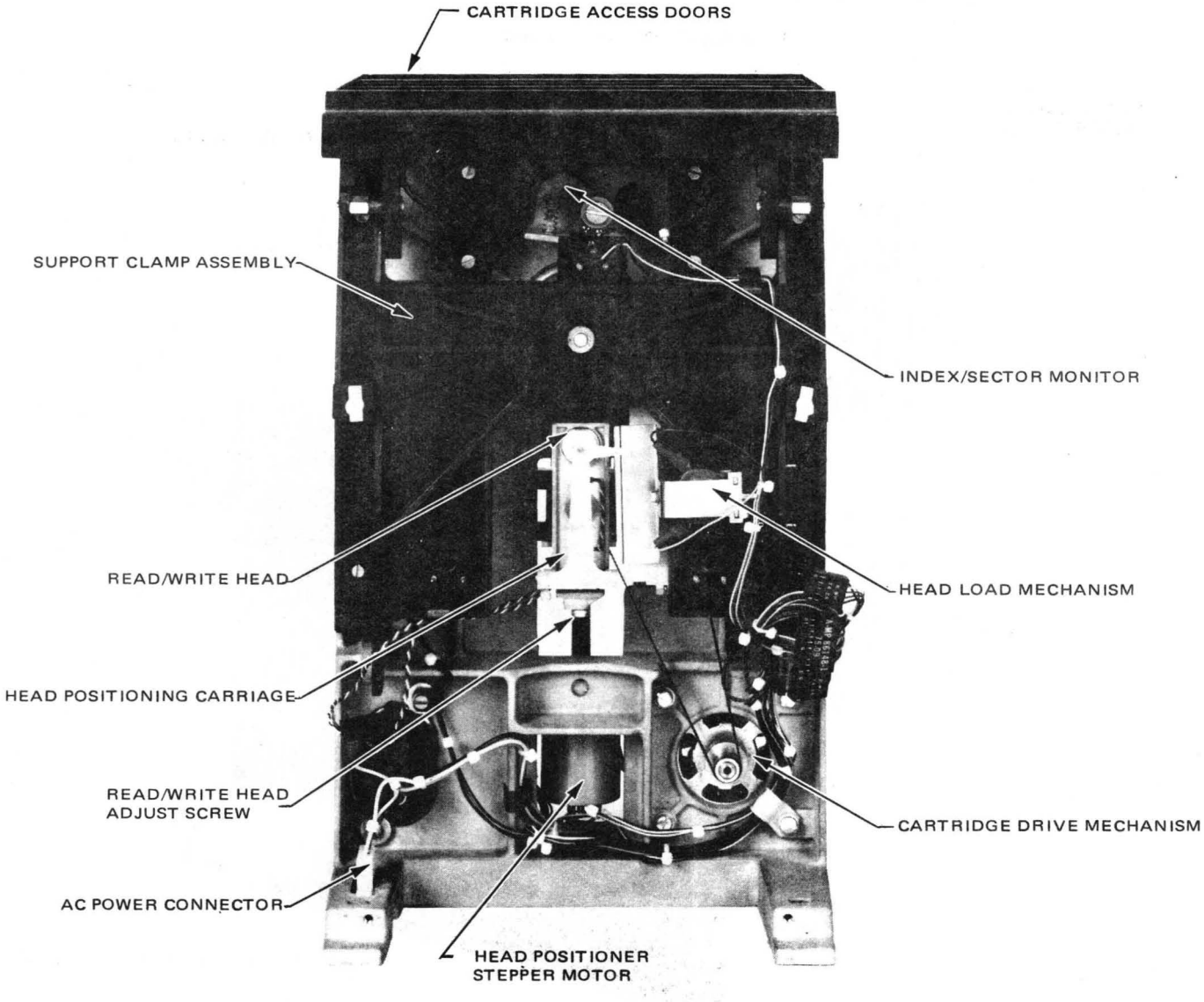


Figure 6-1b MAJOR ASSEMBLY LOCATIONS

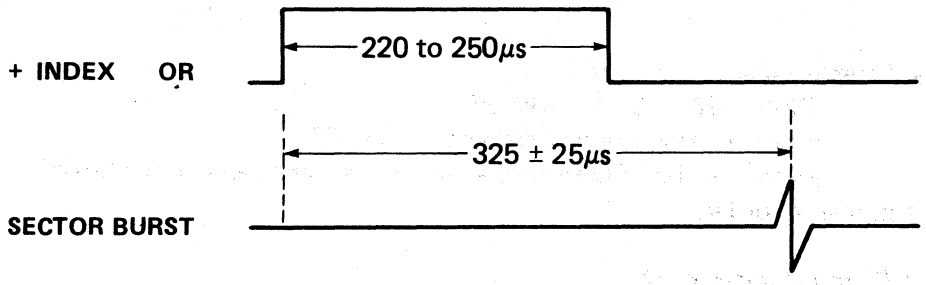


Figure 6-4 SECTOR BURST TIMING

6.5.4.1 Index/Sector Sensor Alignment (Index Burst)

1. Connect the unit to power and a controller.
2. Install an alignment disk in the side to be checked.
3. Set up and connect a scope as follows:

   a) 'Add' mode with channel 'B' inverted and AC coupling on both channels.
   b) Set both channels to 100mv/div.
   c) Set the time base to 50μs/div.
   d) Attach Channel 'A' probe to Index 'A' (TP-10) or Index 'B' (TP-11).
   e) Attach Channel 'B' probe to TP-1.
   f) Sync the scope on Channel 'A', Index, and adjust sync as necessary.

4. Seek to track 01 and observe the Sector Burst signal. It should be similar to Figure 6-4.
5. The burst pulse should occur 325 ±25μs after the leading edge of Index.
6. If adjustment is necessary, loosen the lock-nut and adjust the slotted screw until the burst pulse is at 325 ±25μs. Tighten the lock-nut and recheck the timing.
7. Seek to track 76 and observe the burst pulse. it should be within ±25μs of the timing at track 01.
8. Move Channel 'B' probe to TP-2 and observe that the burst pulse is approximately the same amplitude as at TP-1.

6.5.5 Head Load Solenoid Replacement — Side 'A'

This piece is best replaced as an assembly.

1. Remove the hub clamp assembly (refer to Section 6.5.3).
2. Remove the wiring from the Head Load Bracket assembly.
3. Remove the two screws securing the assembly to the main casting.
4. Install the new assembly in reverse order.

Note: The 'B' side Head Load Solenoid is mounted on the 'B' side Hub Clamp assembly.

6.5.5.1 Head Load Solenoid Adjustment

1. Install a disk in the unit and energize the Solenoid being adjusted.
2. Insert a .010 inch gage between the ridge on the Head Load Bail and the Head Load Pressure Arm (part of the carriage assembly).
3. Loosen the screw on the solenoid bail and adjust for .010 inch clearance over entire working area of the disk.
4. Tighten the bail screw and recheck the clearance.

6.5.2 PC Board Replacement

1. Remove plugs P2A, P2B, P3, P4 and P5.
2. Remove two screws securing the rear corners of the PCB.
3. Lift the front corners of the PCB from the clamp posts and remove the board.
4. Replace in reverse order.

6.5.3 Support Clamp Replacement

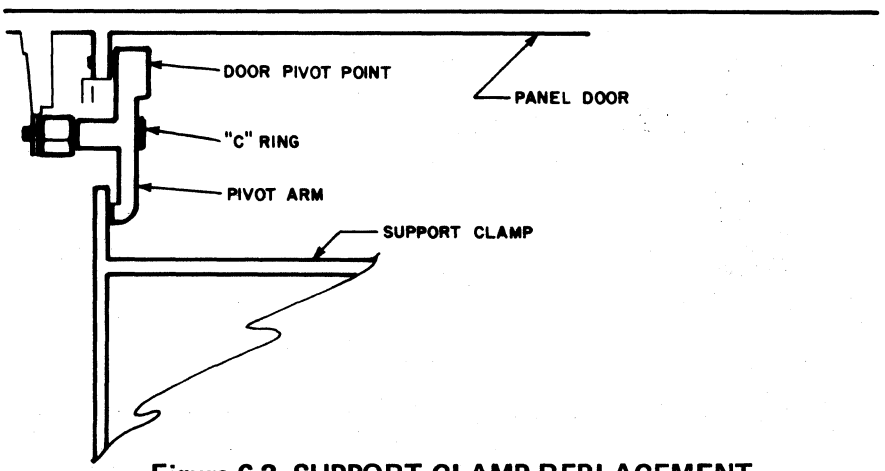


Figure 6-2 SUPPORT CLAMP REPLACEMENT

Refer to Figure 6-2.

1. With snap-ring pliers, remove the 'C' rings from the left and right door pivot arms.
2. Remove the pivot arms.
3. Make a wiring diagram of wires connected to the support clamp assembly, then, remove the wires.
4. Compress the rear pivot arms of the support clamp and lift the assembly from the drive.
5. Replace in reverse order.

6.5.4 Index/Sector Sensor Assembly Replacement

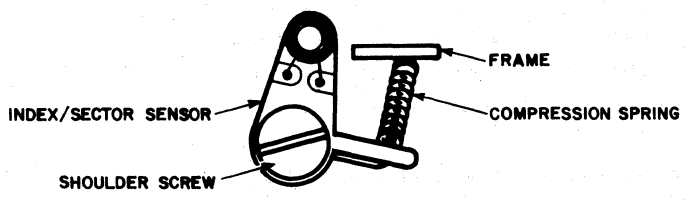


Figure 6-3 INDEX/SECTOR SENSOR ASSEMBLY REPLACEMENT

Refer to Figure 6-3.

1. Carefully remove the shoulder screw securing the Index/Sector Sensor assembly to the frame so that the compression spring does not get away.
2. Remove the wires from the old and connect to the new assembly.
3. Install the spring and compress it sufficiently for easy installation over the adjustment screw.
4. Install and secure the shoulder screw.

6.5.6 Spindle Drive Belt Replacement

1. Slip the belt off of the spindle motor pulley.
2. Open the 'B' side door, to raise the Hub Clamp, and slip the belt out of the unit.
3. Install the new belt in reverse order, turning the pulley several times to center the belt.

6.5.7 Spindle Motor Replacement

1. Be sure the AC power cable is disconnected.
2. Remove the rubber boot on the starting capacitor and disconnect two wires leading to the motor.
3. Remove one wire from the AC connector, which goes to the motor.
4. Remove the drive belt from the motor pulley.
5. Remove the four screws securing the motor to the main casting and remove the motor assembly and from the unit.
6. Remove the pulley from the old motor and place it on the new one, flush with the top of the motor shaft.
7. Install the new motor in reverse order.

6.5.8 Read/Write Head Replacement

1. Disconnect the appropriate head connector.
2. Remove the cable tie that holds both head leads.
3. Loosen the set-screw at the rear of the carriage.
4. Remove the head hold-down screw and leaf spring.
5. Back off on the head adjustment screw and lift the head assembly up and away from the carriage.
6. Place the new head assembly on the carriage and start the adjustment screw into the housing.
7. Install the head hold-down screw and leaf spring. Tighten this screw until the adjustment screw turns with 4 inch ounces of torque.

6.5.8.1 Read/Write Head Alignment

1. Apply power to the drive, insert an alignment disk, and insure Write Protect is on.
2. Set up an oscilloscope as follows:

    a) ADD mode with Channel 'B' inverted and AC coupling on both channels.
    b) Set both Channels to 100mv/div and the time base to 20ms/div.

3. Connect Channel 'A' to TP1 and Channel 'B' to TP2 and trigger on Index (TP10 or TP11).
4. Seek to track 38.
5. Carefully turn the adjusting screw at the rear of the carriage until "cats eyes" of equal amplitude are seen (See Figure 6-5).
6. Back-off on the adjusting screw 1/4 turn to remove pressure on the head holder and tighten the set screw.

[CAUTION]

Do not over-tighten the set screw, only make it snug, over-tightening will strip the threads.

7. Seek to track 39 then back to track 38 and check that A1=A2. Seek to track 37 then back to track 38 and again check that A1=A2. If a difference of greater than ±5% is noted, readjustment is necessary.

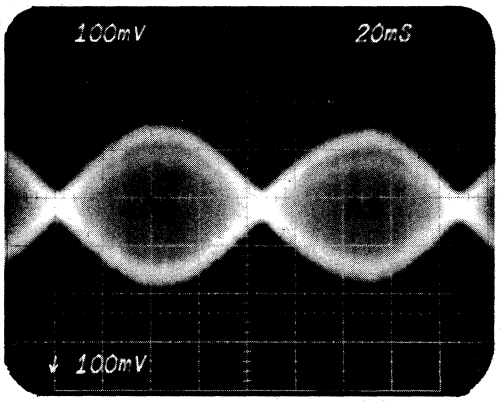


Figure 6-5 READ/WRITE HEAD PROPERLY ADJUSTED (A1=A2)

6.5.8.2 Track 00 Alignment

1. Maintain the same scope set-up as was used for R/W Head alignment.
2. Insert an alignment disk in side 'A'.
3. Perform an incremental forward seek until the head alignment pattern, Figure 6-5, is displayed. This will position the R/W Heads over track 38.
4. Change the scope time base to 50μs/div and display Index 'A' (TP10).
5. Seek 37 increments in reverse. The Sector burst should be displayed indicating that the R/W heads are now over track 01.
6. The Track 00 switch should just "make" at track 01.
7. Attach a scope probe and display M15-6 (—track 00). Trigger on this channel.
8. Seek one more step in reverse to track 00. —Track 00 signal should now be LO.

Note: The Track 00 switch should be in the position shown in Figure 6-6.

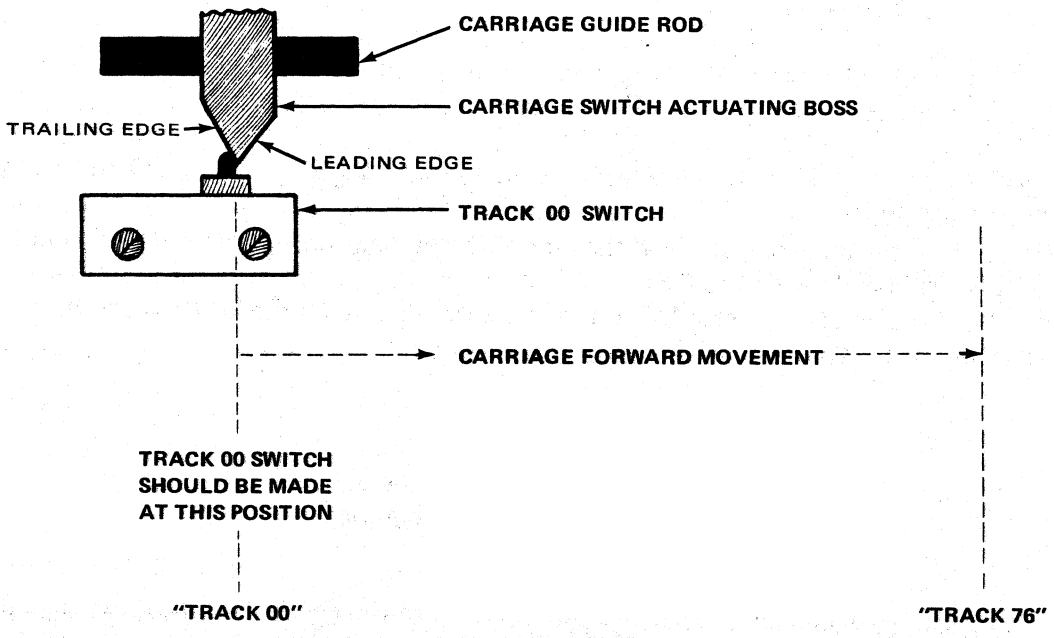


Figure 6-6 TRACK 00 SWITCH ADJUSTMENT

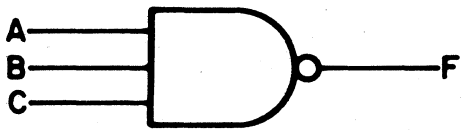
SECTION 7

REFERENCE DIAGRAMS

7.1 GENERAL

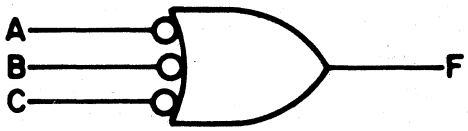
Diablo Systems reference diagrams are primarily intended for use by field service personnel as troubleshooting aids and by system design engineers as sources of design theory information. As such, the first responsibility of a set of reference diagrams is to illustrate a design's principles of operation. Diablo Systems logic diagrams emphasize the functions performed by the logic elements in a design rather than the kinds of devices used to implement the function. For example, a NAND gate may appear on a Diablo System logic diagram as either a positive logic AND function with the output inverted (NAND) or as a negative logic OR function with the inputs inverted (NOR).

AND Function



(Positive Logic NAND)

OR Function



(Negative Logic NOR)

A	B	C	F
L	L	L	H
H	L	L	H
L	H	L	H
H	H	L	H
L	L	H	H
H	L	H	H
L	H	H	H
H	H	H	L

L = Relative low
H = Relative high

This practice runs contrary to some logic drawing standards, which require the use of the NAND symbol for both functions. But, in Diablo Systems diagrams, different symbols are used to distinguish between the two functions because the functional elements of a design are considered to be more relevant to the design theory than symbolic representation of the kinds of devices used.

This functional approach to logic symbology is basic to the logic documentation conventions employed by Diablo Systems. The conventions that govern logic symbology and signal nomenclature are explained below. Other information concerning drawing standards that may help the reader interpret Diablo Systems logic diagrams is also included.

7.2 SIGNAL NOMENCLATURE

The active level of each logic signal is assigned a descriptive name. A signal is considered active when it either causes or represents some logic event that is significant to the progress of an operation. Consequently, the name given a signal usually provides one of two kinds of information:

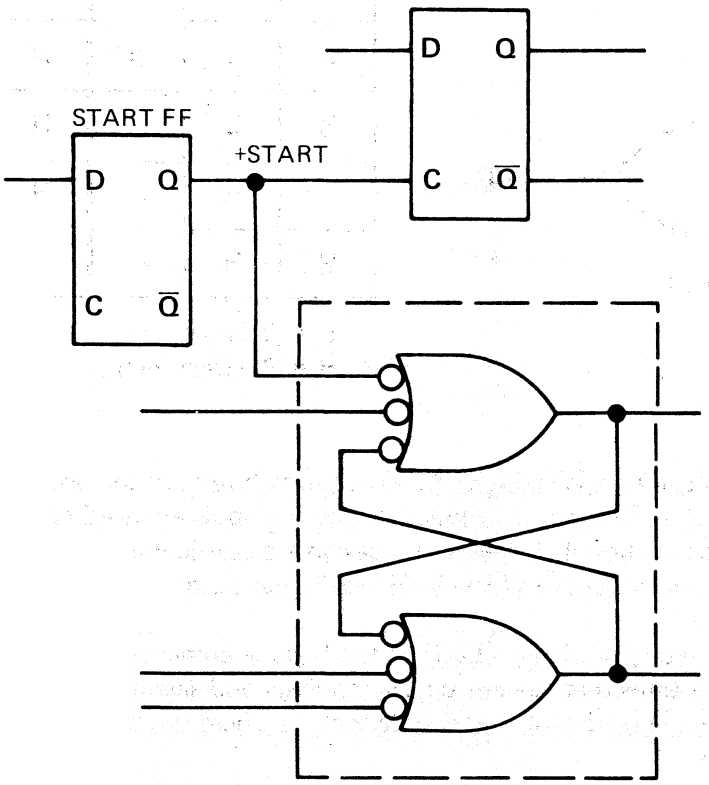
1. Describes the effect that signal's active level has on the logic it feeds; for example, "-- LOAD 'XXX' BUFFER" is the name of the signal that clocks data into the 'XXX' buffer.

2. Represents a condition or event that develops elsewhere in the logic; for example, "-- 'XXX' READY" is the name of the signal that is active whenever the 'XXX' logic is able to accept a new command.

A + or – sign precedes each signal name is identify which of the two voltage levels used in the logic system is considered to be that signal's active level. The + sign represents the relatively higher logic level, and the – sign the relatively lower level. This means relatively higher or lower with respect to each other; the signs do not indicate signal polarity with respect to ground.

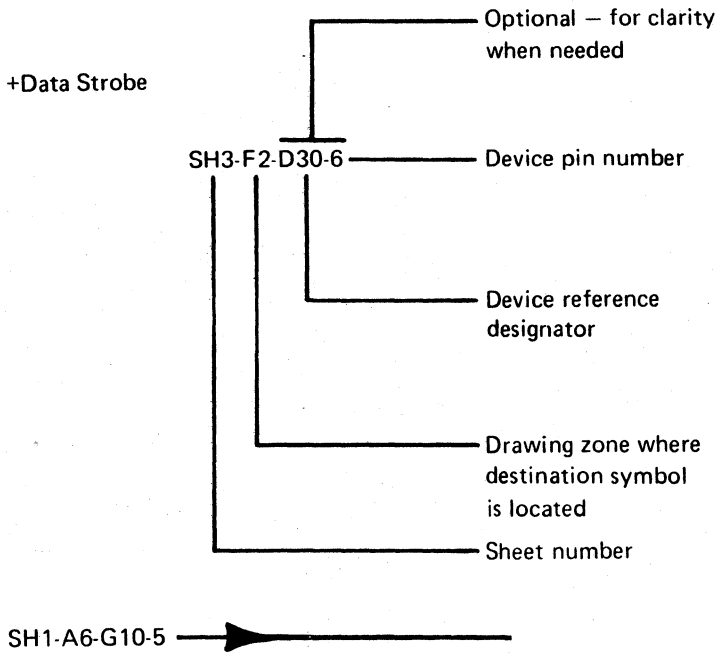
The actual voltage levels represented by the signs will depend on the logic family being used. For example, in TTL circuits, the signal identified by "-- 'XXX' READY" is active when it is at 0 volts (nominal) and inactive at +4 volts (nominal).

Sometimes a signal serves as the input to both positive and negative logic elements. Ordinarily in such cases, the sign preceeding the signal name agrees with the active level indicated at the output of the logic element that produced the signal. An example of this is illustrated by the following sketch.



7.3 INTERPAGE REFERENCING

When a circuit diagram requires more than one page, an interpage reference scheme is used on the points on each diagram page where the signal lines enter and leave the page. The reference scheme used includes the following information.



7.4 LOGIC SYMBOLOGY

The logic function symbols used in Diablo Systems logic diagrams conform closely to those set forth in MIL-STD-806.

Most small scale integration (SSI) circuits are represented by function symbols.

Medium scale integration (MSI) devices, such as shift registers and read-only memories (ROM), may be represented by rectangles with functional labels.

Since both positive and negative logic conventions can appear in a single set of diagrams, the unfilled circle negation symbol specified by MIL-STD-806 is used to distinguish between low-true and high-true signals.

A circle drawn at an input to a symbol indicates that the input is active at its relatively lower potential. The absence of a circle at an input means that the input is logically active at its relatively higher potential. The presence or absence of a circle at a symbol output has similar meaning for the active level of that output.

Usually, all logic symbols are drawn with inputs on the left and outputs on the right. Some device symbols (e.g. one-shots, J-K flip-flops) show some inputs and other external connections on the top and/or bottom of the symbol for clarity. Also, drawing layout restrictions occasionally requires that some symbols be drawn with a vertical orientation so that signal flow through them is from top to bottom. However, logic

symbols are never drawn with inputs on the right side or outputs on the left; nor are they drawn with inputs and outputs on the same side.

The component identifiers used on Diablo Systems logic diagrams, such as "flip-flop G23" is the grid coordinate code for locating that component on its printed circuit board. Textual reference to a device, such as a flip-flop will usually further identify the device by its output erminal number, particularly where a multi device component is involved.

TABULATION CHART				
ASSEMBLY NO.	DRIVE MOTOR		CAPACITOR	
45000-01	115VAC, 50/60Hz	45058	5.0 μF	10242-50
45000-02	230VAC, 50Hz	45062	2.5 μF	10242-25
45000-03	115VAC, 50/60 Hz	45058	5.0 μF	10242-50
45000-04	230VAC, 50Hz	45062	2.5 μF	10242-25

DRIVE MOTOR ASSEMBLY
45018-XX
SEE TABULATION CHART

M1
DRIVE MOTOR
BLK
BLU
TERM. B
TERM. A
CAP
P6
BLK
GRN
BLK/YEL
1
2
3
A/C POWER SUPPLY

BRACKET & PHOTO TRANSISTOR ASSY 45019-02
WRITE PROTECT SENSOR A
SUPPORT CLAMP ASSY BOTTOM 45020-04
WRITE PROTECT LED A

PHOTO TRANSISTOR ASSY 45005
WRITE PROTECT SENSOR B
SUPPORT CLAMP ASSY TOP 45020-03
WRITE PROTECT LED B

PHOTO TRANSISTOR ASSY 45005
SENSOR B
SUPPORT CLAMP ASSY TOP 45020-01,-03
LED B
SOLENOID B ASSY 45014

PHOTO TRANSISTOR ASSY 45005
SENSOR A
SUPPORT CLAMP ASSY BOTTOM, 45020-02,-04
LED A
SOLENOID A ASSY 45014

FRONT PANEL ASSY
45006-XX (RACK MTG)
45026-XX (DESK TOP)
LED B
LED A

FRONT LIMIT SWITCH
REAR LIMIT SWITCH
TRACK Ø SWITCH
NO
C
NC
BLK

CARRIAGE ASSY 45010
STEPPER MOTOR ASSY 45016-XX
M2

ORN	WRITE PROTECT LED A		P3 3A	J3 3A
BLK	WRITE PROTECT LED A RETURN		3B	3B
YEL	-WRITE PROTECT SENSOR A		4A	4A
BLK	-WRITE PROTECT SENSOR A RETURN		4B	4B
	SPARE		5A	5A
	SPARE		5B	5B
BRN	WRITE PROTECT LED B		1A	1A
BLK	WRITE PROTECT LED B RETURN		1B	1B
RED	-WRITE PROTECT SENSOR B		2A	2A
BLK	-WRITE PROTECT SENSOR B RETURN		2B	2B

HARNESS ASSY WRITE PROTECT 45035

YEL	+ LED (SENSOR B)	P4 5A	10A
BLK	LED (SENSOR B) RETURN	5B	10B
GRY	+ HEAD LOAD SOLENOID B	9B	14B
GRY	- HEAD LOAD SOLENOID B	9A	14A
RED	- SENSOR B	3A	8A
BLK	SENSOR B RETURN	3B	8B
GRN	+ LED (SENSOR A)	6A	11A
BLK	LED (SENSOR A) RETURN	6B	11B
ORN	- SENSOR A	4A	9A
BLK	SENSOR A RETURN	4B	9B
WHT	+ HEAD LOAD SOLENOID A	10B	15B
WHT	- HEAD LOAD SOLENOID A	10A	15A
BLU	+ BUSY LITE B	7A	12A
BLK	- BUSY LITE B	7B	12B
VIO	+ BUSY LITE A	8A	13A
BLK	- BUSY LITE A	8B	13B
WHT	+ FRONT LIMIT SWITCH	1A	6A
GRY	- REAR LIMIT SWITCH	1B	6B
BLK	TRACK Ø COMMON	2B	7B
BRN	+ TRACK Ø SWITCH	2A	7A

MAIN HARNESS ASSY 45034

BLK	+ STEPPER COMMON	P5 1A	16A
RED	- STEPPER PHASE B	3A	18A, 18B
YEL	- STEPPER PHASE D	5A	20A, 16B
BRN	- STEPPER PHASE A	2A	17A, 19B
BLK	+ STEPPER COMMON	5B	20B
ORN	STEPPER PHASE C	4A	19A, 17B

+5V ISOLATED POWER
GROUND
- SEEK IN
GROUND
- LOW CURRENT
GROUND
- WRITE DATA
GROUND
- SELECT DISK B
GROUND
F.M. DATA
GROUND
TRACK Ø
GROUND
- SECTOR B
GROUND
- SECTOR A
GROUND
- INDEX B
GROUND
- INDEX A
GROUND
- READY B
GROUND
- READY A
GROUND
- STEP
GROUND
- HEAD LOAD B
GROUND
- HEAD LOAD A
GROUND
- WRITE GATE
GROUND
- WRITE PROTECTED
GROUND
- MISSING CLOCK
GROUND
- READ CLOCK
GROUND
- READ DATA
GROUND
- UNIT SELECT 1
GROUND
- UNIT SELECT 2
GROUND
- UNIT SELECT 3
GROUND
- UNIT SELECT A
GROUND
50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
I/O

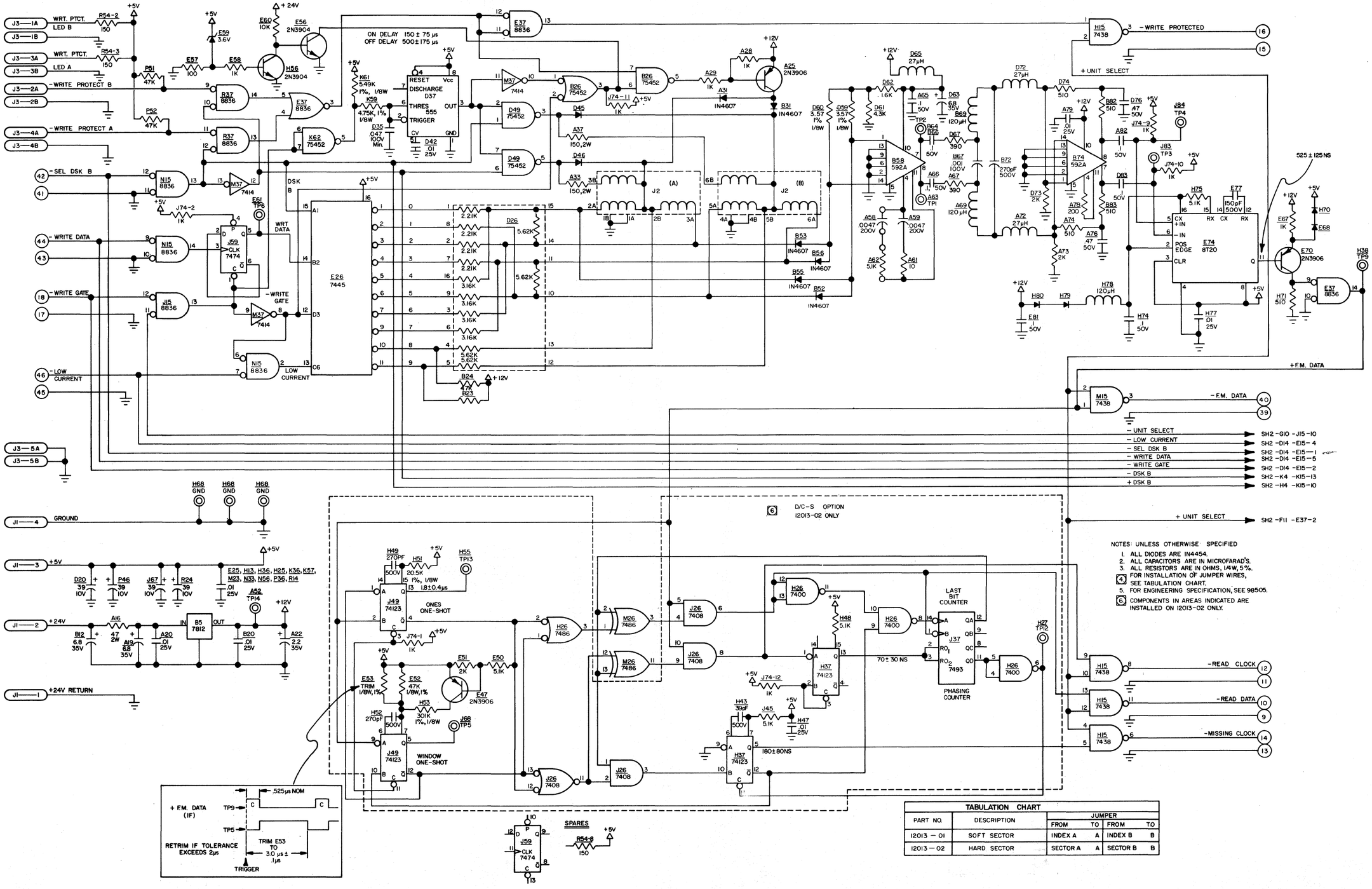
P.C.B. ASSEMBLY
12013-XX

J1 P1
4 4 GROUND
3 3 + 5V
2 2 + 24V
1 1 + 24V RETURN
DC POWER SUPPLY

J2 P2-A
3B 3B RED ERASE
1A 1A
3A 3A BLK READ/WRITE
1B 1B
2B 2B GRN
2A 2A WHT COMMON
READ/WRITE
CARRIAGE ASSY 45010
BOTTOM HEAD SUPPORT ASSY 45011-02

P2-B
6B 3B RED ERASE
4A 1A
6A 3A BLK READ/WRITE
4B 1B
5B 2B GRN
5A 2A WHT COMMON
READ/WRITE
CARRIAGE ASSY 45010
TOP HEAD SUPPORT ASSY 45011-01

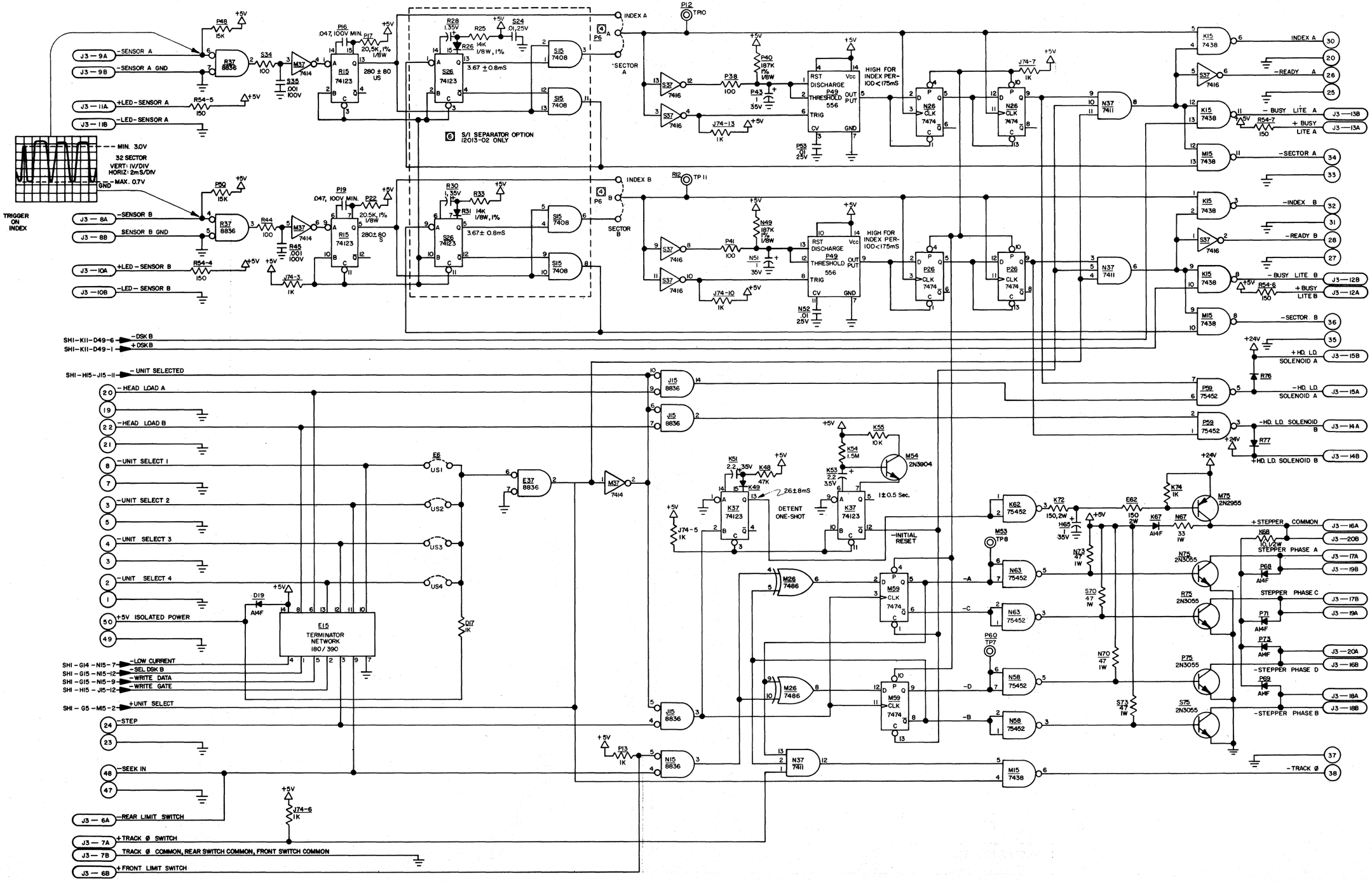
MODEL 12
WIRING DIAGRAM



TABULATION CHART					
PART NO.	DESCRIPTION	JUMPER			
		FROM	TO	FROM	TO
12013 — 01	SOFT SECTOR	INDEX A	A	INDEX B	B
12013 — 02	HARD SECTOR	SECTOR A	A	SECTOR B	B

NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL DIODES ARE IN4454.
2. ALL CAPACITORS ARE IN MICROFARAD'S.
3. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
4. FOR INSTALLATION OF JUMPER WIRES, SEE TABULATION CHART.
5. FOR ENGINEERING SPECIFICATION, SEE 98505.
6. COMPONENTS IN AREAS INDICATED ARE INSTALLED ON 12013-02 ONLY.

12013-XX
MODEL 12 SCHEMATIC DIAGRAM
Sheet 1 of 2



 # 12013-XX
MODEL 12 SCHEMATIC DIAGRAM
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