APPLICATIONS OF ANALOG STORAGE TECHNIQUES FOR HYBRID COMPUTATION

ABSTRACT: A discussion of analog storage techniques is presented. The general requirements, including a description of available devices, a summary of techniques for their use, and some applications susceptible to solution with analog storage, are treated as a unified whole. Of primary concern will be point storage, with standard integrator amplifiers utilizing normal mode control relays--the so-called "track-hold" storage devices with high-speed electronic mode switches--and, to a smaller extent, capacitor storage and mechanical switching type devices. The use of this equipment for performing the functions of switching, storage, counting, and gating at normal and high solution speeds will be discussed from the point of view of both operational requirements and applications for real time, repetitive, and sequential calculations.

INTRODUCTION

The concept of point storage or "sample and hold" for the solution of problems on the analog computer is not new to the field. In the early fifties, a good deal of study was devoted to the storage requirements for solution of partial differential equations (1), and, since that time, a number of analog problems have required and have been solved by the use of storage devices (2, 3, 4, 5). In general, these have been specific applications requiring specific equipment for solution. As the range of storage-type applications broadens, it seems advantageous to present the subject of analog storage as a separate and unified whole.

In the past, analog storage has been accomplished primarily through the use of electrical capacitors, either as passive network devices without amplifiers (e.g., SADSAC computer (6)), or with the standard analog computer integrator amplifier. In some cases, it has been desirable to digitize the information and store it by means of magnetic tape, core, or drum, such as in the SIMULAG Unit produced by Electronic Associates. The choice of a storage device will obviously depend upon the particular application, the number of points that must be stored, the speed of solution, and the economics governing available equipment. For a few points, amplifier storage on a "track-hold" integrator in a normal general purpose analog computer proves to be the simplest to implement. Whether one amplifier per point is expensive or not will depend upon the size of the computer available. When a number of points (several functions, for example) must be stored, it may be necessary to use banks of capacitors and mechanical switching. When several hundred points must be stored, digital means such as the Serial Memories in the EAI HYDAC* Computers, must be utilized.

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I-a: Storage Controlled by Computer Mode. In the solution of problems covering a number of decades of change for an important variable, it is sometimes necessary after an initial operate time, to place the entire computer in the HOLD mode, rescale the problem, and then continue the solution by returning the entire computer to the OPERATE mode. Thus, the entire computer is made to perform as a storage device. It "tracks" or follows the calculated variables during the initial operate time, "stores" the last calculated values of the variables while the computer is in the HOLD mode, and then uses the stored values for completion of the solution during the second operate interval. Somewhat the same technique is used for sequential calculations, such as in the design calculations for component compositions in a distillation column (EXAMPLE II). In this case, rebalance circuits are used to solve the column steady-state equations for selected input conditions, with one or more of the variables being stored at the conclusion of the operate cycle. These stored values are then used as inputs to the same rebalance circuits to generate a solution for the next plate in the column. This general technique of equipment sharing allows the same computer components to be used in a sequential manner until the problem is completed.

In both of these problem examples, storage amplifiers were controlled, i.e. changed, from track-to-store or store-to-track, directly from the computer mode control busses. Thus, by definition, a "storage" amplifier stores during the time that the computer is in the OPERATE mode; a "tracking" amplifier tracks during the time that the computer is in the OPERATE mode. Typical behavior for this type of operation is shown in Figure 1(a) for a tracking amplifier, and in Figure 1(b) for a storage amplifier.

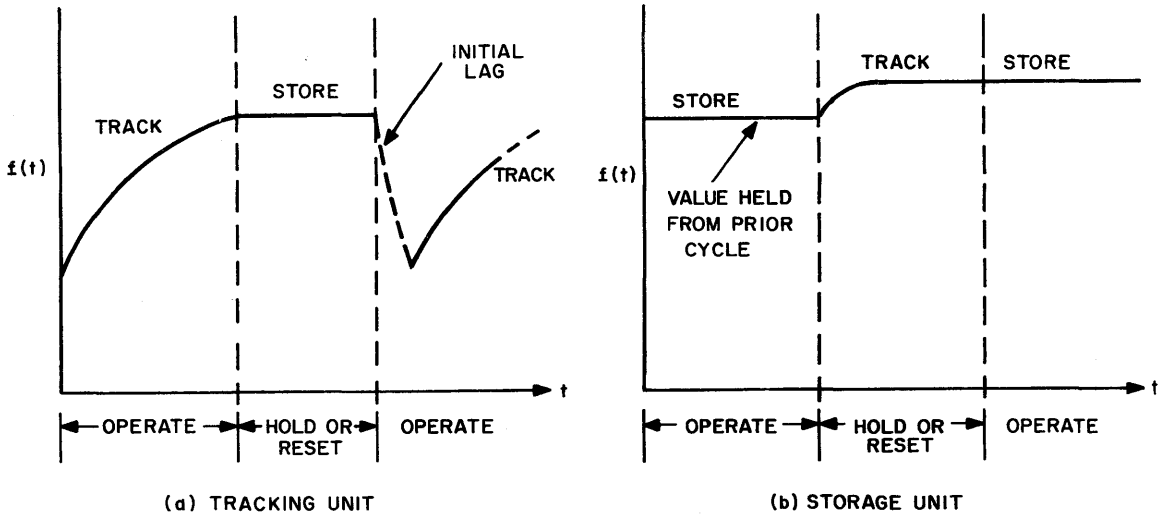


Figure 1: Computer-Mode-Controlled Storage. During the operate cycle the tracking amplifier follows a varying voltage, f(t), that is generated in the computer; the storage amplifier simultaneously holds a constant value of voltage from the previous cycle. At the conclusion of the operate cycle, when the computer is placed in the HOLD mode, the tracking amplifier immediately stores the last value of f(t). At the same time, the storage amplifier becomes operative and tracks to the value of voltage at its input. Since this voltage is most often a constant, the storage amplifier is shown in Ib as reaching and staying at this value during the hold time. Placing the computer in IC mode has no effect on the operation of the amplifiers. When the computer is again placed in OPERATE, the storage amplifier stores the constant it has picked up, and the tracking amplifier begins following f(t) again. There is a short lag before the tracking amplifier can reach the value of f(t) depending on the difference between the initial and final values of the function.

I-b: Comparator-Controlled Storage. The second type of storage amplifier required is one that changes from track-to-store or store-to-track during an operate cycle, being controlled by a comparator or another decision device rather than by computer mode. Data-fitting problems and curve-storage problems are typical examples of this use of storage. The behavior of a comparator-controlled track-store unit is shown in Figure 2.

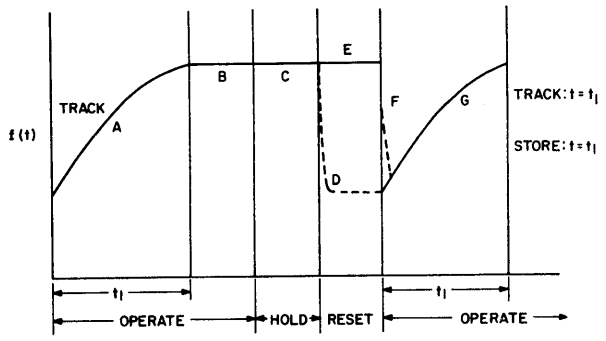


Figure 2: Comparator-Controlled Storage. At the beginning of the operate cycle, the control or decision device compares t (generated as a ramp function) with t_1 and puts the track-store amplifier into the track mode. The output is, therefore, the tracked value of the function f(t), shown as Curve A. When $t=t_1$, a control signal from the decision device reverses the mode of the track-store amplifier and it holds the value of f(t) at t_1. This value is held during the remainder of the operate time (Curve B) and during the hold time (Curve C). If the computer is placed in IC at this point, two possible methods of operation arise from the fact that the amplifier generating the time ramp must reset to zero in preparation for the next operate cycle; 1) the time ramp is reset and, as soon as t becomes less than t_1, the storage amplifier returns to the track mode and immediately picks up the I.C. of f(t) as shown by the dotted Curve D, or 2) a latch voltage is applied to the decision device after the initial operate time. This latch controls the track-store amplifier unit during both the hold and reset periods, and drops to zero when the computer is again placed in the OPERATE mode. Curve E shows a latched track-store output and Curve F shows the short lag period when the tracking amplifier is picking up the function again. Curve G is the tracked value of f(t) during cycle 2.

The comparator-controlled track-store unit can operate in either mode at any time, depending on the control device signal. Thus, a complementary "store-track" unit could be used which would operate from the same decision device as that for Figure 2, but which would store when $t \leq t_1$. The use of such a complementary storage unit will become more obvious shortly.

I-c: Track-Store Combined Memory. The series connection of a tracking unit feeding a storage unit is one of the most useful combinations of storage devices. In high-speed repetitive operation, it is a virtual necessity if a stored quantity is to be used in the system calculations. Operation of track-store combinations in series will allow use of a stored value from several cycles back. This is demonstrated in Figure 3 where f(t) is the function being tracked in the n^{th} cycle, $f(t)_{n-1}$ is the stored value from the previous cycle, $f(t)_{n-2}$ from 2 cycles back, etc.

I-d: Counting Circuits: One of the obvious requirements for iterative or sequential operation is a counting circuit. Not only does this provide a knowledge of the operation or solution at its various points, but it also acts as a logic device, triggering comparators to change circuitry and allowing recycle after the correct number of iterations. For example, in a distillation calculation according to the McCabe-Thiele method, the circuit must be changed at the feed plate to generate a new operating line for the stripping section. This is accomplished by having a counting circuit which keeps count of every plate as the calculation is made, and changes the circuitry automatically when the feed plate is passed. The same counter would be used to determine the last plate in the column, and to either stop the computer or repeat the calculation from the first plate.

In most of the problems involving serial-type analog solution, a counting circuit of some type will usually be found to be necessary.

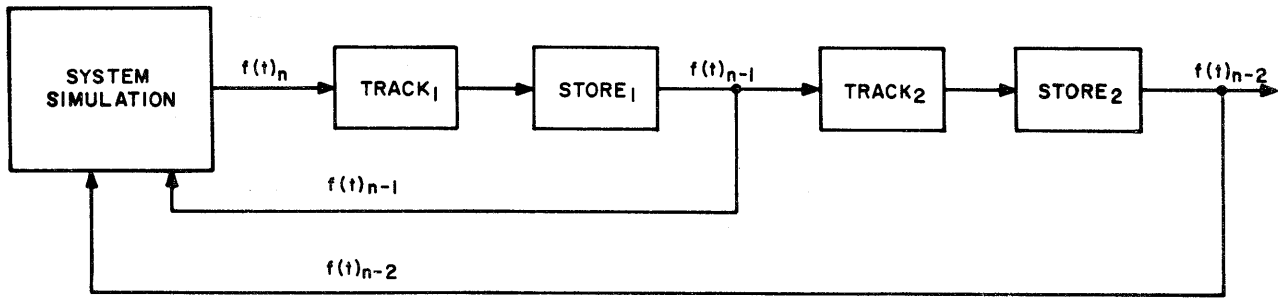


Figure 3: Series Connection of Track-Store Units. All units operate under computer mode control. During the operate cycle, the storage amplifiers remain constant and feed their values, $f(t)_{n-1}$ and $f(t)_{n-2}$, into the system. The first tracking amplifier follows $f(t)_n$ and the second $f(t)_{n-1}$. At the conclusion of the operate time, the modes reverse on the track-store units and information is passed forward regarding cycle n and n-1. Upon returning to operate and cycle n+1, the two storage amplifiers again become constant with the proper values from the last two runs.

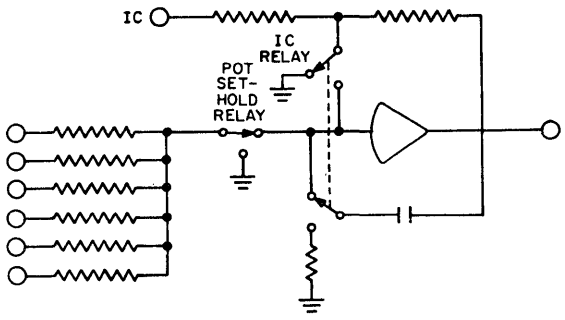
I-e: Curve Storage and Interpolation. For the serial solution of partial differential equations on the analog computer, one or more entire solution curves must be stored and fed back into the computation during the following computing cycle. The need for accurate curve storage in these problems is essential since, for many systems, any error in the stored curve will become a slightly larger error in the new curve being generated. The amplification of error will cause the solution either to arrive at a constant but stable error, or to diverge from its correct value with each additional cycle in the computation. Since the combination of precision, high speed, and continuous curve storage is not available, the problem is resolved by the use of multiple point storage and subsequent interpolation. But this practical approach necessarily imposes limitations on the computation.

To obtain an accurate solution to a problem involving curve storage, a multitude of points must be used along with an adequate, and sometimes elegant, method of interpolation. Sample-hold storage under such circumstances becomes extremely expensive in terms of amplifier requirements. On the other hand, approximate curve storage limits the number of steps in a serial computation to the point where parallel computation may be more feasible. These limitations on available curve storage techniques must be taken into consideration when preparing a serial computation for the analog computer.

II-a: General. The equipment required to perform each of the storage functions listed in Section I differs somewhat depending upon the solution speeds utilized. The availability of the mode relays on each integrator amplifier allows individual amplifier control in real-time operation. This, and the fact that mechanical relay comparators may be used, somewhat reduces the equipment requirement from that necessary in high-speed operation. However, the advantages that are gained by using high-speed operation, where possible, far outweigh the equipment differential in most cases. The following discussion is, therefore, intended for those situations in which real-time storage is required (or is combined with high-speed operations to obtain multiple-speed operation), or where high-speed equipment is not available.

II-b: Review of Real-Time Integrator Operation. Implementing storage with real-time equipment implies proper use of the relays associated with each integrating amplifier. By way of review, Figure 4 shows the operation of the mode control relays on a 231R integrator. The relay contacts in Figure 4a are shown in the so-called "normal" (deactivated coil) position. These relays operate on a pulse-decay system in which a + 90 volt pulse decays to 21 volts for activating the coil, and a zero pulse rises to 21 volts for deactivating the coil. The 21 volt holding voltage keeps the relay in either position following the pulse and is used to speed up relay throw-time and cut down transient effects. The circuits shown in Figures 5 and 6 illustrate two methods for control of individual integrator modes. These pulse generating circuits are easy to assemble and, with variations, will satisfy a variety of control requirements.

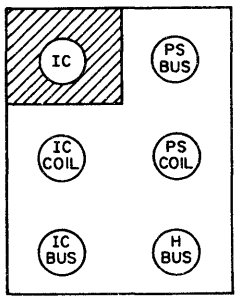
II-c: Computer-Mode Controlled. Representative circuits are shown in Figures 7 and 8. The real-time tracking memory circuit shown in Figure 7a consists of a high-gain lag-circuit around a normal integrator (the IC relay must be disabled to allow the integrator to store when the computer is in the IC mode). This circuit will track an input voltage within about 50 milliseconds. If input frequencies are higher, a 0.01 microfarad capacitor can be used to speed up the tracking. An alternate circuit for high-speed tracking is shown in Figure 7b. This circuit will track an input within about 15 milliseconds. Control is obtained (IC relay deactivated) with a pulse circuit from a control voltage, t, switched when the computer is placed in the IC mode.



4a:

MODE	POT SET-HOLD RELAY	IC RELAY
POT SET	ACTIVATED	ACTIVATED
INITIAL CONDITION	ACTIVATED	ACTIVATED
HOLD	ACTIVATED	DEACTIVATED
OPERATE	DEACTIVATED	DEACTIVATED

4b:



4c:

Figure 4: 231R Amplifier Schematic, Operation and Relay Terminations. (a) Amplifier Schematic; (b) Mode Relay Operation; (c) Relay Terminations. (Relays shown in Normal or deactivated position.)

The storage memory (Figure 8) consists of an input to the IC of a normal integrator and the connection of the hold bus to the IC coil. When the computer is in operate, this amplifier will store because there are no inputs to change its value. When the computer is in the HOLD or IC mode, the amplifier tracks the voltage at the initial condition input.

II-d: Comparator-Controlled Real Time Memory. The circuit for real-time memory under comparator control (Figure 9) takes the same form as that shown in Figure 7b for the mode-controlled memory. Here, the control voltage, t, is generated in the problem solution. The pulse circuit is arranged so that for tracking operation, the IC relay is acti-

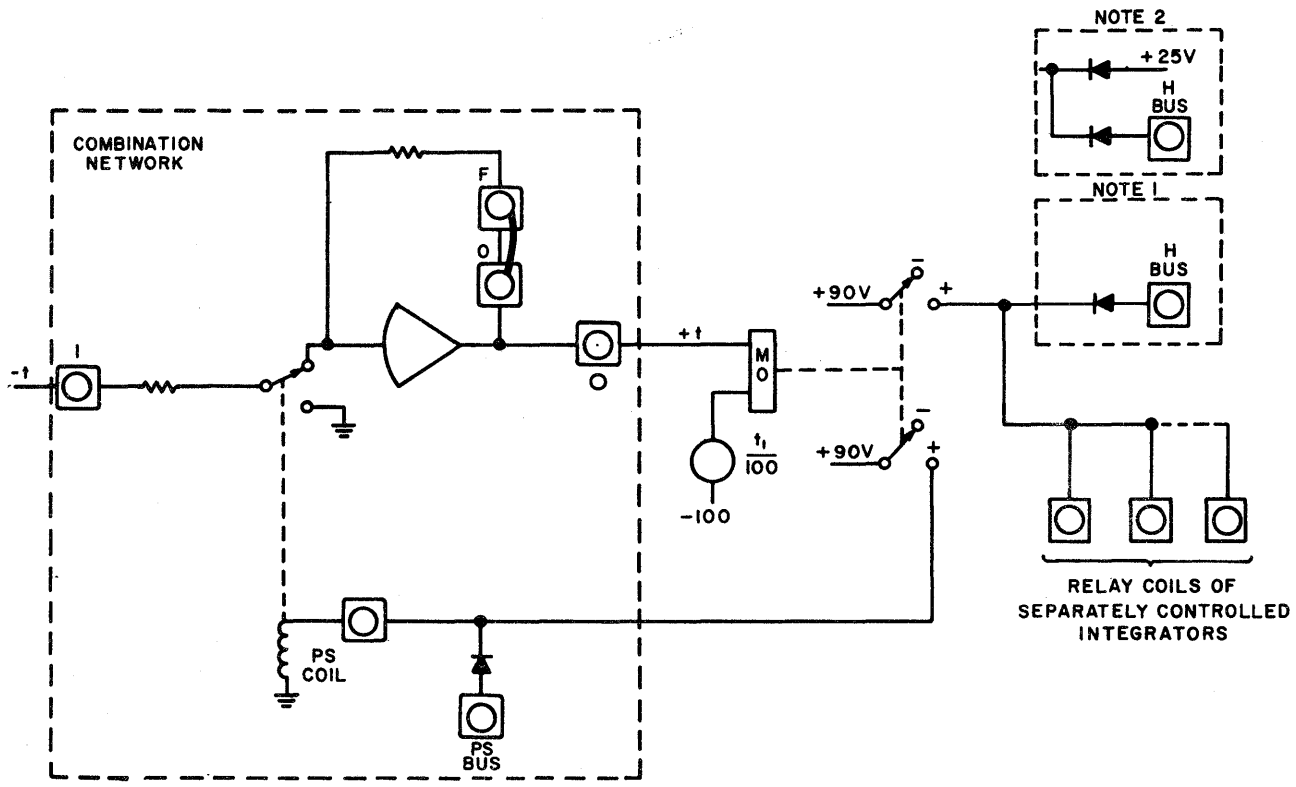


Figure 5: Mode Relay Pulse Generating Circuit. Note 1: Placing integrators into HOLD from OPERATE. Note 2: Placing Integrators into OPERATE from HOLD. The number of integrators that can be switched is limited to eight when the HD6008 patch cord diode is used.

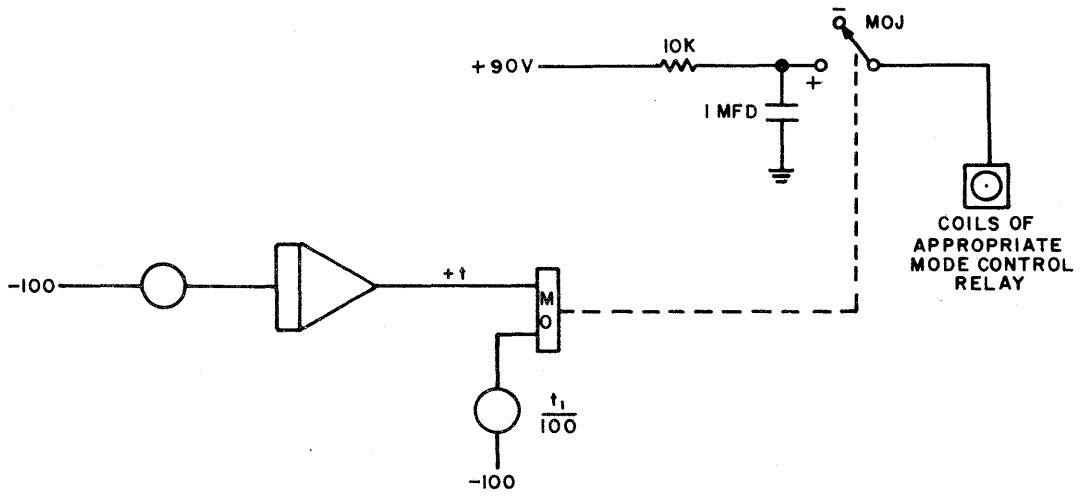


Figure 6: Mode Relay Pulse Circuit. An RC time constant of 10^{-2} seconds and 1 microfarad of capacitance will provide sufficient current to quickly throw the relays for a single amplifier. For example, four relay coils would require a pulse circuit consisting of a 4 microfarad capacitor and a 2500 ohm resistor. These values are approximate and substitutions easily made.

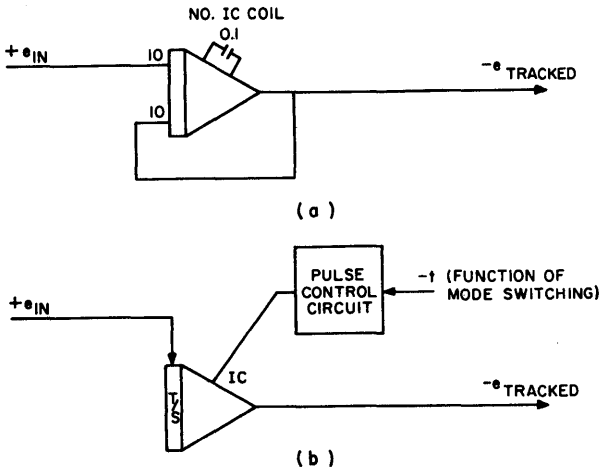


Figure 7: Real-Time Tracking Amplifier Controlled by Computer Mode. (a) High-Gain Lag-Circuit; (b) Fast "Reset" Circuit.

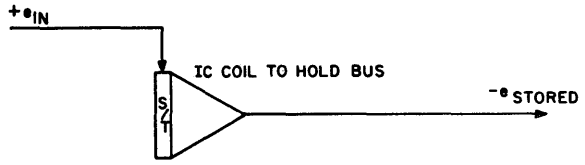


Figure 8: Real-Time Storage Amplifier Controlled by Computer Mode.

vated by a + 90 volt pulse followed by a + 21 volt holding voltage. Storage operation (IC relay deactivated) is obtained by interrupting the + 21 volt holding voltage for a period of approximately 20 milliseconds.

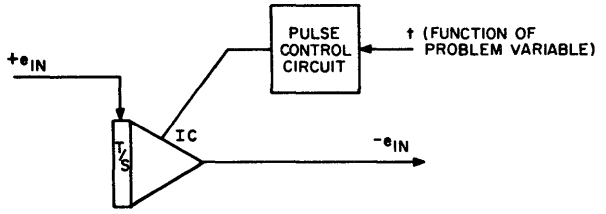


Figure 9: Real-Time Memory Amplifier Controlled by Comparator.

A logic circuit that can be used in place of the comparator is the so-called "bang-bang amplifier, a high-gain, feedback-limited amplifier as shown in Figure 10. A basic limitation is that one bang-bang amplifier can only supply enough current to drive two relay coils, whereas the voltage-pulse circuits can drive a larger number of coils.

II-e: Track-Store Combined Memory. When the computer is to be switched among all three modes (OPERATE-HOLD-IC), a track-store combination must be used for effective storage. Figure 11 shows a circuit for the computer-mode-controlled operation.

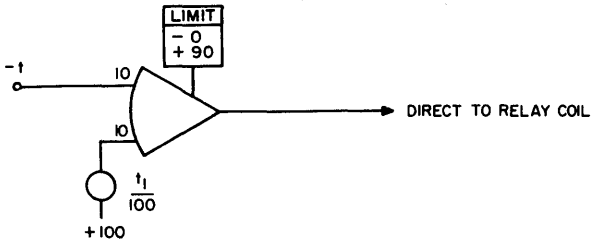


Figure 10: Bang-Bang Amplifier for Driving Relay Coils. As $t \geq t_1$, the amplifier bangs from its negative zero limit to a + 90 volts which is sufficient to activate the coil directly.

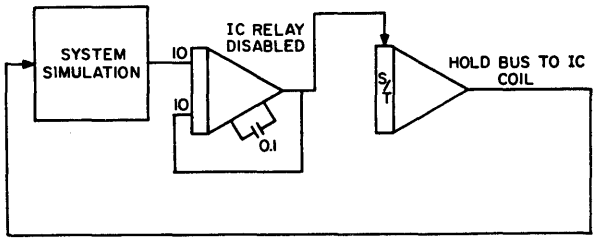


Figure 11: Real-Time Combined Track-Store Memory Circuit.

II-f: Counting Circuit. For a simple counting system in which no repetitive operation is required, a single integrator circuit as shown in Figure 12 will suffice. At the expense of an additional amplifier, a more adaptable counting circuit can be constructed which can also be used for repetitive operation.

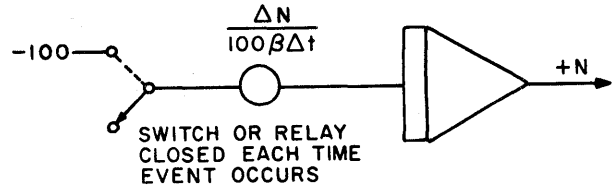


Figure 12: Simple Counting Circuit for Real-Time Operation.

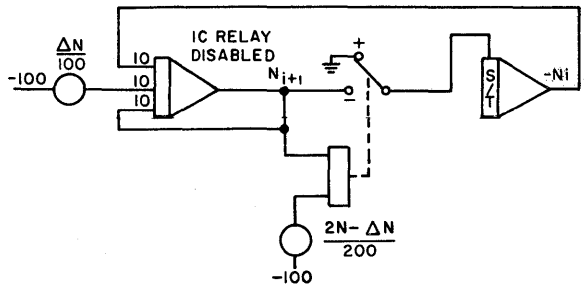


Figure 13: Two Amplifier Counting Circuit. In the first operate cycle, the tracking amplifier assumes the value of ΔN. Since relay arm MOJ is in the negative position, this value is stored by the storage amplifier during the reset time. During the next operate cycle voltage $-N_i$ is added to $-\Delta N$ to obtain $+N_{i+1}$ on the output of the tracking amplifier. The accumulation continues until $N_{i+1} \geq 100 - \frac{\Delta N}{2}$, the value on the comparator which determines the number of counts before restarting.

II-g: Curve Storage and Interpolation. For real-time curve storage, track-store amplifiers are too expensive, equipmentwise, to be useful for any but trivial problems. On the other hand, very simple schemes of multiple-point storage which use stepping switches and passive capacitors for a memory have proven successful. One such technique was devised to solve a set of partial differential equations in which three curves remain in storage while a fourth was being stored and a fifth was being read into the computer (3). Figures 14 through 17 present a brief summary of the circuits required. This technique requires only three amplifiers for storage and interpolation of a complete curve. More sophisticated switching arrangements and interpolation schemes (for instance, parabolic) would allow use of many more points, and would yield a smoother and more accurate curve reproduction. Whether or not this is justified is a function of the problem and the available equipment.

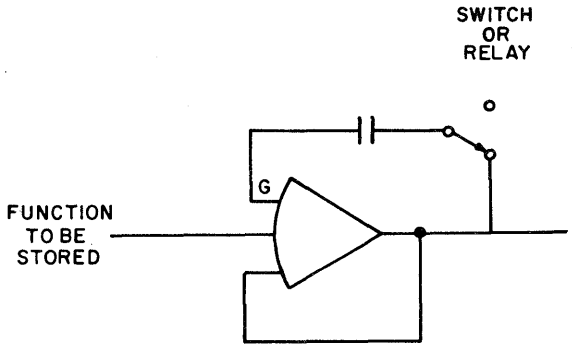


Figure 14: Multiple-Point Tracking Amplifier. A voltage to be stored is read from an amplifier output by charging a capacitor placed in the feedback of a tracking amplifier. When the capacitor is switched out of the feedback at some instance of time, it remains charged to the value of the voltage to be stored.

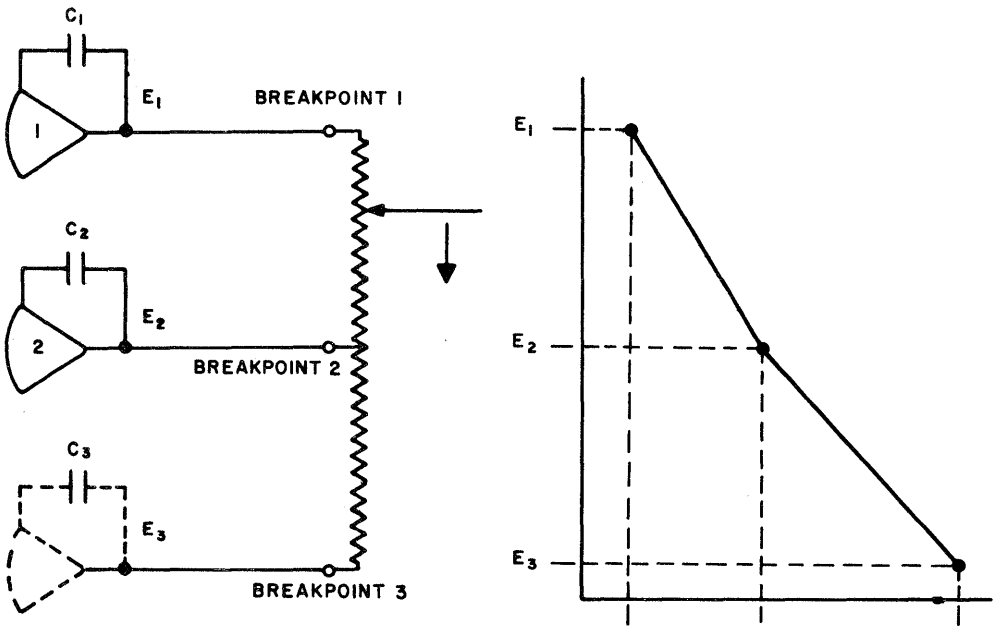


Figure 15: Multiple-Point Readout Circuit. A capacitor charged to the value of a voltage to be stored can be switched into the feedback of a high-gain amplifier whose output will then assume the value of the stored voltage. When amplifiers with output voltages corresponding to values on a stored function are connected to two adjacent taps of a padded servo potentiometer, linear interpolation is obtained as the potentiometer arm is swept from one tap to another.

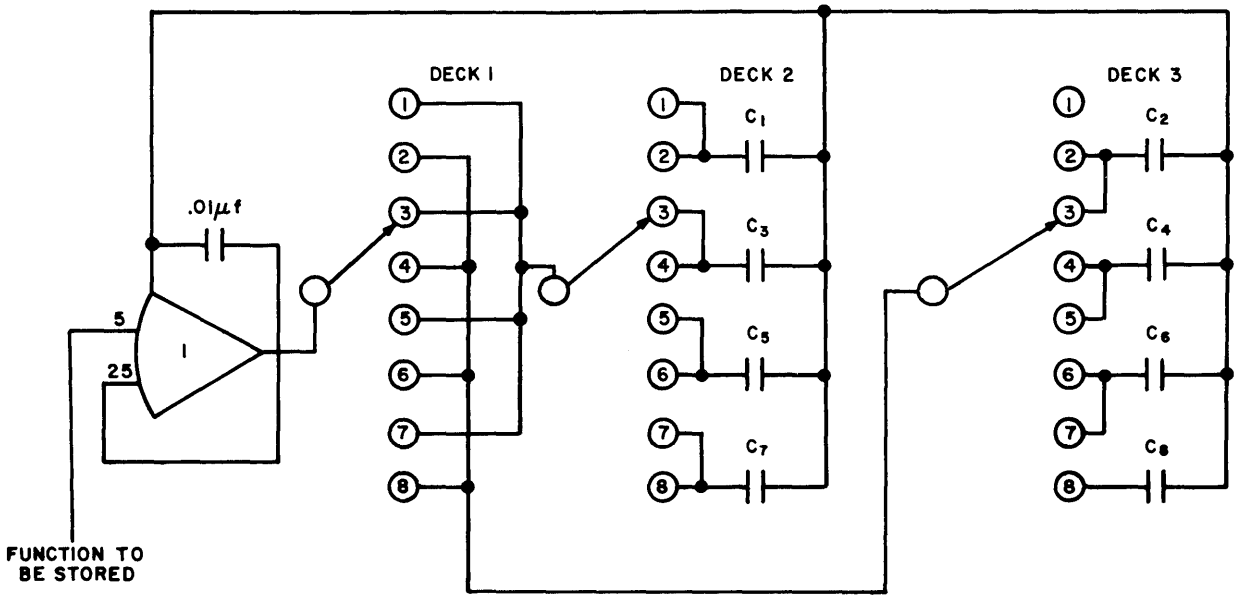


Figure 16: Multiple-Point Storage Circuit. Switching circuits connect appropriate storage capacitors to a high-gain amplifier for storage of voltages corresponding to points on a stored function.

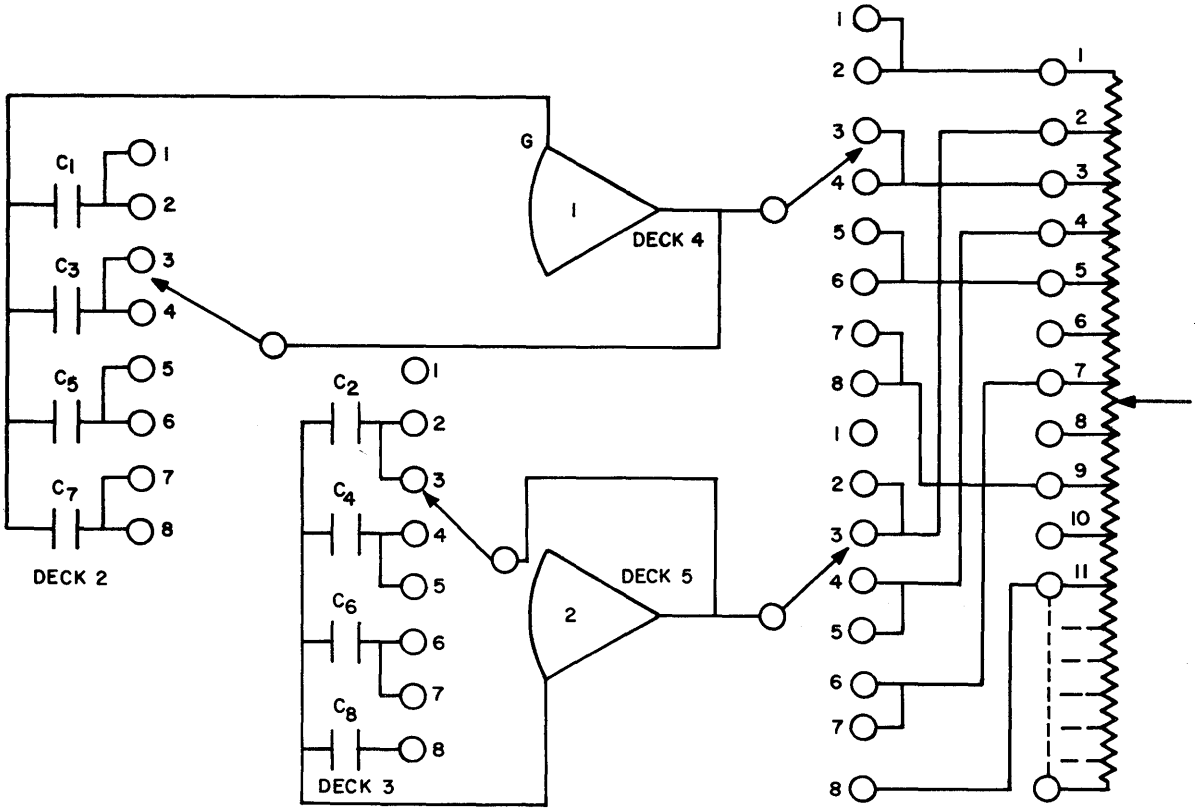


Figure 17: Multiple-Point Storage Readout Circuit. A function with any number of straight-line approximations up to the total available taps on a pot padder (17) can be obtained with only two readout amplifiers. Values on the curve between stored points are linearly interpolated due to the resistance of the servo multiplier potentiometer and the voltage gradient between taps.

SECTION III: HIGH-SPEED REPETITIVE OPERATION EQUIPMENT AND TECHNIQUES

III-a: General. The advent of accurate, high-speed repetitive operation equipment has made possible many new techniques and applications for the analog computer. Data- and curve-fitting problems, boundary value problems, statistical studies, and the general problem area of model building by visual means have reduced trial and error work on the computer to a considerable extent.

At the same time, the use of repetitive operation requires several equipment changes in the standard analog computer. It is no longer possible to use the electromechanical devices such as servo-multipliers, relay comparators, and the normal computer mode control relays commonly associated with the computer. These devices must be replaced by electronic equipment. In the same sense, requirements for operation of track and store memory become more stringent. Tracking times and switching times must be in the range of microseconds. Provisions must also be made for a simple method of returning to real-time operation since most final results will be plotted on an x-y plotter.

A brief review of the equipment necessary for high-speed repetitive operation and for track-store at these speeds is essential. In particular, the following units and ideas must be defined:

Rep-Op Drive (Master Drive): This unit produces a square wave voltage signal that drives the repetitive operation mode switches. When the voltage is negative, the computer is placed in the OPERATE mode; when positive, the computer is in the IC mode (See Figure 18). There is no HOLD mode, as such, in repetitive operation; this is the function of track-store units.

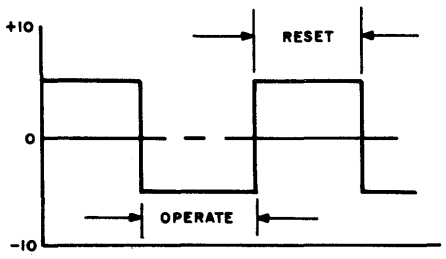


Figure 18: Repetitive Operation Master Drive Signal. Operate time is variable from 10 milliseconds to 80 milliseconds. Reset time for normal operation is 10 milliseconds. Thus, repetitive rates from 10 to 50 cycles per second can be obtained.

Track-Store Master Drive: This device accepts the rep-op drive signal as an input and converts it, by means of suitable shaping and an adjustable time delay, into a bi-polar square wave for controlling track-store units under computer control. A negative voltage occurring when the computer is in the OPERATE mode is used to control a track-store amplifier; a positive voltage occuring when the computer is in the OPERATE mode is used to control a store-track amplifier.

Electronic Control Comparator: This component provides a means of controlling a track-store amplifier from problem variables. Operation is such that when the sum of the two voltage inputs to the comparator is negative, the "track" output (labeled "-" in Figure 20) is negative and the store output is positive (labeled "+" in Figure 20). When the voltage summation becomes positive, the comparator output state reverses.

Comparator Latch Input: In addition to the two normal signal inputs, a third comparator "latching" input is provided to allow a control voltage (either from mode control signals or from problem variables) to be used to insure a desired state of comparator output. The latch signal necessary is approximately ±5 volts, and is only used for overriding the other inputs after a condition is met. A positive latch signal produces a positive signal at the comparator "+" output and a negative signal at the comparator "-" output. A negative latch signal reverses the polarity of the comparator outputs. Note that the latch termination is not a precision input, and should be coupled through a diode so as to insure that the comparator sensitivity is not affected.

Track-and-Hold Gate: This unit performs the switching functions required for track and store operations, and is essentially a precision electronic ON-OFF switch with its mode being determined by the polarity of the voltage applied to its switch input, SW.

Microstore Module: For programming flexibility, the Electronic Comparator and Track-and-Hold Gate described above have been combined into a modular group whose patch panel layout is shown in Figure 19. A simplified schematic of the switching actions, and the associated circuitry for a high-speed track-store amplifier are shown in Figure 20 along with the computer symbol used.

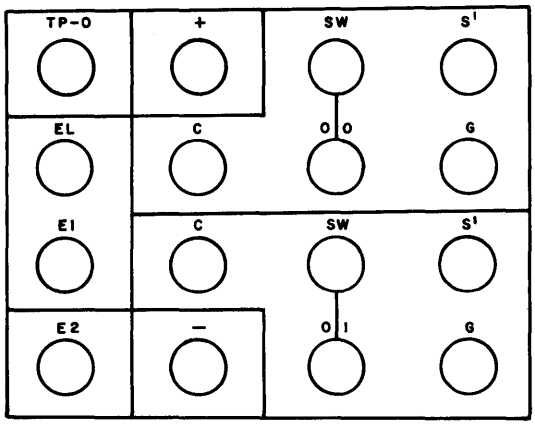


Figure 19: Patch Panel Terminations for Track-Store Unit. Two Track-Hold Gates and one Electronic Comparator are terminated in a single patching area. The two normal comparator inputs are labeled E1 and E2; the latch input E_L. Termination "TP" is a tie point to simplify patching when several gates are to be operated from the same control input. The comparator output appears in the second column and, as shown, represents the polarity of the control voltage when the sum of the voltage inputs to the comparator are negative. For normal track-and-store operation, the amplifier output is patched to C, the summing junction to S', and the grid to G.

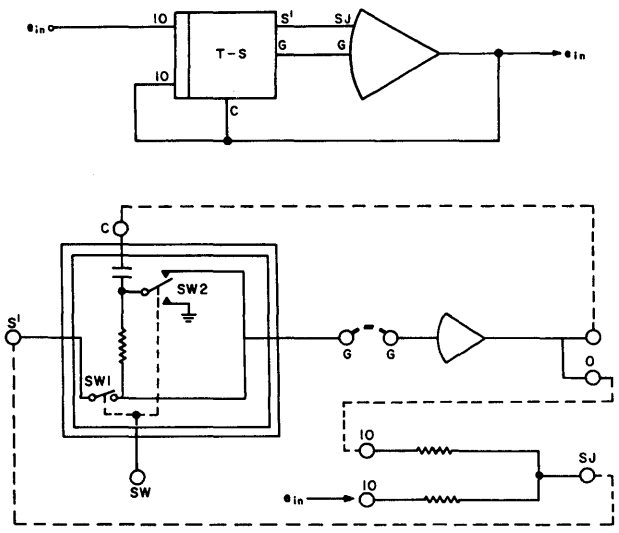


Figure 20: Repetitive Operation Track-Store Unit. (a) Simplified schematic of the Track-Store Unit – the unit is capable of accepting multiple inputs which enter the amplifier summing network on gains of 10 as does the feedback connection around the amplifier. The two switches are "down" for track operation; "up" for store operation. (b) Computer symbol for Track-Store Unit.

Electronic Switch: One advantage of the modular arrangement is that it is possible to utilize the Track-and-Hold Gates as an electronic switch. Using two gates without the capacitor feedback, and an amplifier with 100K input and feedback resistors, a solid-state switch may be realized for either repetitive or real-time operation. Figure 22 shows the connections required for simulating a single-pole, double-throw switch in one of two operating conditions, i.e., selector or distributor (Figure 21).

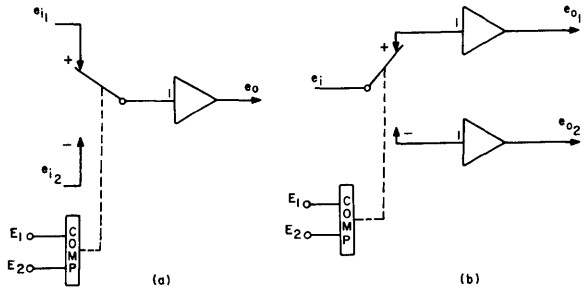


Figure 21: Simulation of SPDT Switch with a Track-Hold Gate. (a) Selector Operation; (b) Distributor Operation.

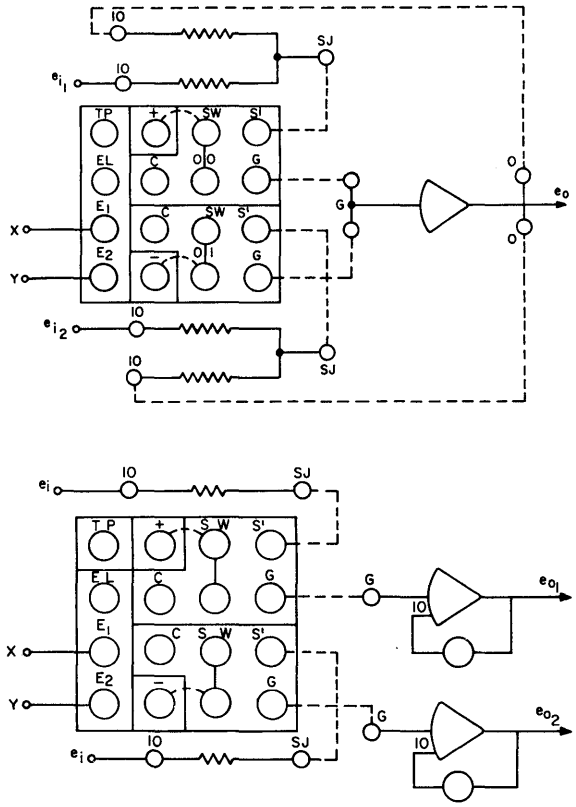


Figure 22: Patching Connection for Simulation of SPDT Switch. (a) Selector Operation. If $x + y > 0$, $e_o = -e_{i_1}$. If $x + y < 0$, $e_o = -e_{i_2}$. (b) Distributor Operation. Since the Track-Hold Gate is not in the amplifier feedback path, a reduced gain will result because the diode gate is not a perfect short-circuit when conducting. This error can be largely compensated for by a potentiometer in the feedback path of the amplifier. However, since the effective resistance of the gate is nonlinear, the gain can be made correct at one particular input level, but will be slightly in error for other input levels.

III-b: Computer-Mode Controlled Track-Store. To obtain computer-mode control of the track-store amplifiers, the "track" (negative signal in OPERATE mode") output of the Track-Store Master Drive is connected to the SW connection of the gate, and the S', G, and C connections made to an external amplifier. If the complementary store-track operation is desired, the "store" (positive signal in OPERATE mode) output of the drive is connected to the SW termination.

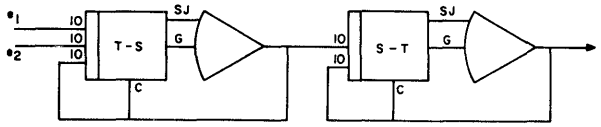


Figure 23: Mode-Controlled Track-Store Combination. Two inputs are being summed in the Track-Store (T - S) unit and fed to the Store-Track (S - T) unit.

III-c: Comparator-Controlled Track-Store. The normal comparator signal inputs are entered at the E_{in} terminations, while the outputs of the comparator connect to the SW terminations for control of the Track-Hold gates. The remaining connections are the same as those for computer-mode control. The computer symbols are shown in Figure 24.

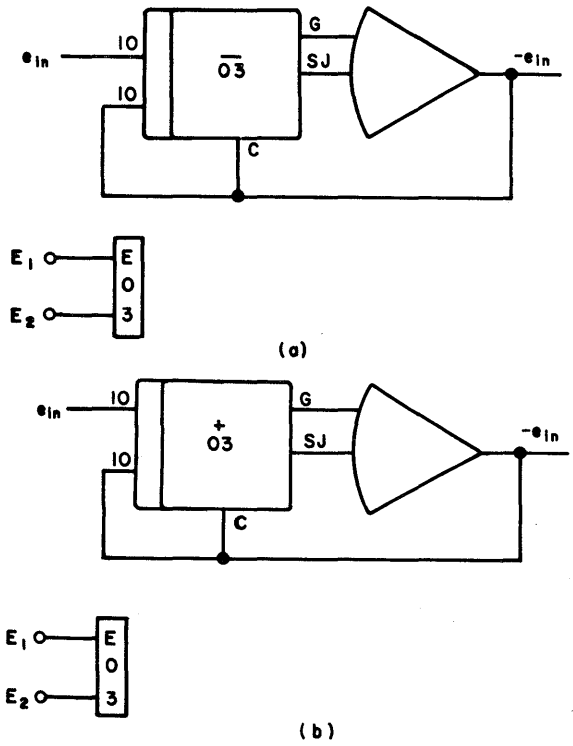


Figure 24: Comparator-Controlled Track-Store Combination. (a) Amplifier tracks when the sum of the inputs to the comparator is negative (minus sign in gating block). (b) Amplifier tracks when the sum of the inputs to the comparator is positive (positive sign in gating block).

III-d: Track-Store Combined Memory. In high-speed repetitive operation, it is usually necessary to have a track-store combination memory in order to use stored values from one cycle to the next. This can be accomplished quite simply by the series connection of track-store and store-track amplifiers for either method of control (Figures 23 and 24). In data-fitting problems, however, it is not always necessary to use the rapid reset qualities of the track-store amplifier. For these types of problems, the use of the latch voltage permits substitution of a normal integrator for the storage unit, thus halving the equipment requirement of track-store modules. This can be seen by the simple example shown in Figure 2. If the tracked voltage (curve A) is held during reset by latching the comparator, its value (curve E) can be used as the initial condition on a normal integrator. The circuit diagram for such a combined memory is shown in Figure 25.

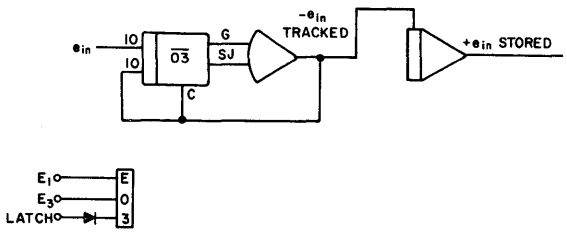


Figure 25: Circuit for Track-Store Combined Memory Under Comparator Control.

III-e: Counting Circuit (Accumulating Circuit). The counting or accumulator circuit for repetitive operation is the same as the real time accumulator with the exception of the reset-to-zero circuit. For high speed operation, this function is performed by a gate placed in the feedback of the storage amplifier as indicated by the electronic switch (ES) symbol in Figure 26.

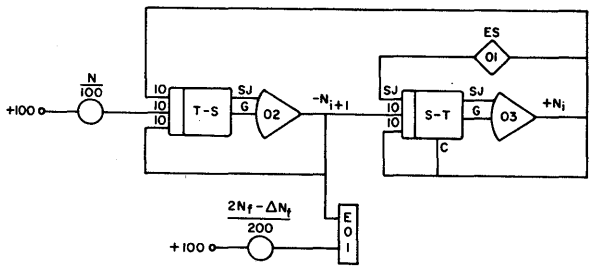


Figure 26: Counting Circuit Using Track-Store Units. The operation of this circuit follows closely that of the real time counter (Figure 13).

III-f: Curve Storage and Interpolation. As previously pointed out, curve storage with analog memory devices requires many amplifiers and a good interpolation scheme to achieve satisfactory results. The basic approach is to use multiple track-store amplifiers under comparator control, and to sample the value of the function at the desired points. Aside from the equipment requirements, this is easily accomplished. The problem arises in the interpolation between the points, especially when, as in a serial computation, the stored curves are being used to generate new curves in each cycle. Some simplified schemes have been used, but even at their best, care must be taken to avoid a large number of serial steps.

If the curve to be stored is a function of the independent variable and if its general shape is known, a Newton Forward Difference approximation can be tried. For the case of a polynomial, this would be:

$$f(t) = a + bt + c\frac{t(t-1)}{2!} + dt\frac{(t-1)(t-2)}{3!} + \cdots\cdots$$

For the case of an exponential curve, the equation would be:

$$f(t) = a + be^{-t} + ce^{-t(t-1)} + de^{-t(t-1)(t-2)} + \cdots$$

Consider the case of the polynomial, and take the derivatives with respect to time.

$$f'(t) = b + \frac{c}{2}(2t-1) + \frac{d}{6}(3t^2 - 6t + 2) + \cdots\cdots$$

$$f''(t) = c + \frac{d}{6}(6t-6) + \cdots\cdots$$

$$f'''(t) = d$$

The initial conditions (t=0) are:

$$f(0) = a$$

$$f'(0) = \frac{c}{2} + \frac{d}{3}$$

$$f''(0) = c - d$$

$$f'''(0) = d$$

The general technique in applying this difference formula is to take the value of f(t) at four evenly spaced points in time, store them, algebraically calculate the values of constants a, b, c, d, and then solve the preceding four equations with their appropriate initial conditions. This procedure is shown schematically in Figure 27.

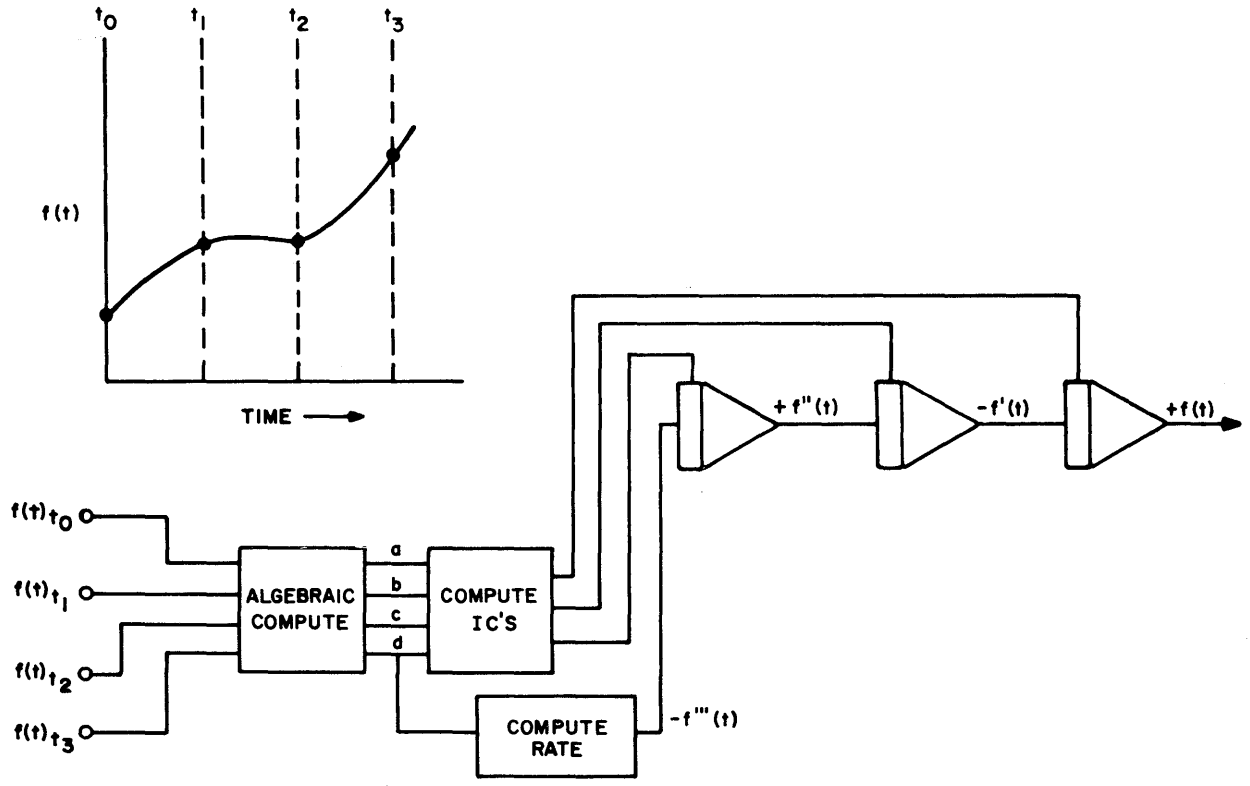


Figure 27: Schematic of Newton Forward Difference Interpolation Scheme.

The values of a, b, c, and d are obtained by solving the polynomial at the various points; t_0, t_1, t_2, and t_3.

$a = f(t)_{t=0}$

$b = f(t)_{t=t_1} - f(t)_{t=0}$

$c = f(t)_{t=t_2} - 2\,f(t)_{t=t_1} + f(t)_{t=0}$

$d = f(t)_{t=t_3} - 3\,f(t)_{t=t_2} + 3\,f(t)_{t=t_1} - f(t)_{t=0}$

The circuit diagram for this system is shown in Figure 28.

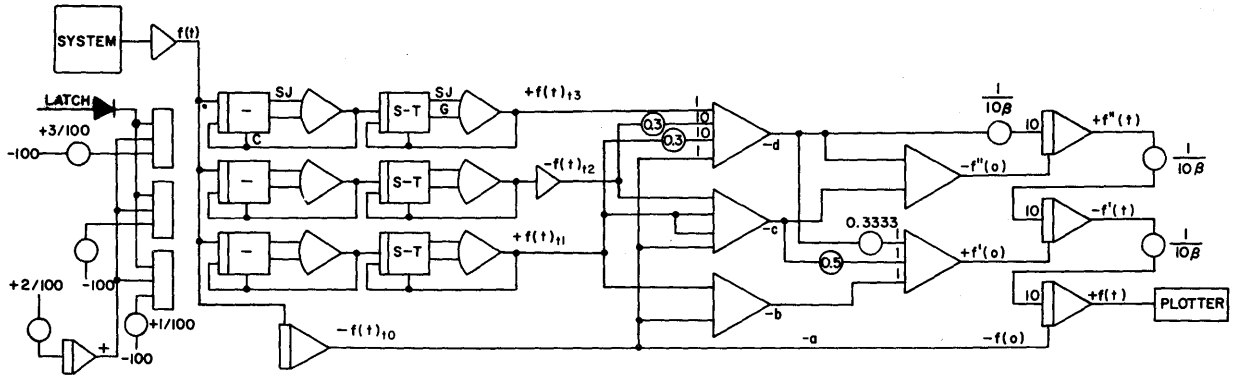


Figure 28: Circuit for Newton Forward Difference Interpolation. Four storage points are used; initial condition constant.

SECTION IV: THE MEMORY LOGIC GROUP EXPANSION

IV-a: General. Multi-speed operation, or the ability to operate individual integrators or groups of integrators at different time scales, is a natural extension of the concept of high-speed repetitive operation. Add to this the ability to perform the functions of analog storage, logic switching, gating, and counting--all at repetitive operation speeds--and the analog computer becomes capable of even more advanced solution techniques. Sequential and/or iterative solution schemes become both practical and economical, opening additional problem areas to solution by the analog computer.

Although the concept of multi-speed operation does not introduce any mathematical functions not possible with a standard analog computer, it does introduce ideas and components new to analog computation. In addition to the obvious stringent requirements placed on switching devices, the introduction of logic components forces a consideration of the "interface" between analog signals on the one hand, and the binary logic signals on the other. On the one side of the interface, electronic comparators serve to convert the sign of analog voltages to binary levels for the performance of logic operations. These logic levels, in turn, are converted to analog signals by electronic switches capable of changing the modes of integrators from IC to OPERATE, Track-to-Store or Store-to-Track operation, by gating analog signals from one source to another, or by operating relays at slower rates. To further isolate the two types of signals and increase the programming flexibility, all logic signals are terminated on a separate, removable patch panel while analog signals are terminated on the standard analog panel. Such a system allows an almost unlimited flexibility in the control of the operation of analog components.

Effective multi-speed operation of the analog computer thus requires the following functions:

Integrator Time Scales: Any one of 6 different time scales, over a range of from 10 seconds to 100 microseconds, can be selected for integrators by a combination of patching and pushbutton control. Each integrator may be operated at a different time scale, but all can be speeded up by a factor of from 10 to 1000 by pushbutton. Pushbutton control can be applied to all integrators simultaneously, or individually to three sectors. Since the feedback capacitors are paralled, speedup of the time scale can be performed during a run without loss of signal. Patching terminations for the control of a single integrator are shown in Figure 29.

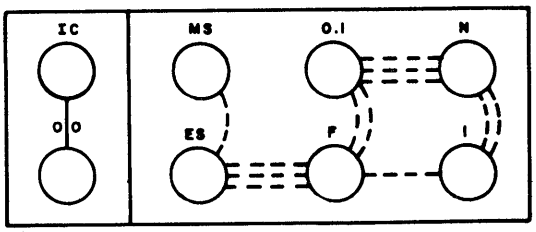


Figure 29: Patching Terminations for Control of Integrator Time Scales. Logic signals serving as drive-input to the electronic mode switch are patched to the IC terminations (the switch is conducting, i.e., Track mode when the signal applied is high). If an integrator is patched along the single dashed line, its "Fast" time scale will be .1 sec; if patched along the double lines, its "Fast" time will be 0.1 sec; if patched along the triple lines, its "Fast" time will be 10 msec..

Analog-to-Logic Conversion: Electronic comparators convert the sign of analog voltages to logic levels suitable for use to drive integrator switches, relays, D/A switches, latches on other comparators, and AND gates. Dual analog inputs appear on the analog board while outputs appear in complementary logic form on the logic patch panel. Inputs to Track-and-Store gates are terminated adjacent to comparators associated with MICROSTORE units; relay driver inputs, adjacent to comparators terminated in the normal comparator area of the analog panel. Latch inputs are also provided, capable of overriding the analog signals, so that the comparator output state can be controlled from logic signals.

Electronic Mode Control: The operating modes of individual integrators can be controlled from logic signals by means of control terminations on the logic patch panel. This is in addition to the normal relay

mode control. When the electronic switching is selected, a high (binary ONE) logic signal will place the integrator in the IC (Track) mode.

Assigned Track-and-Store Amplifiers: Patching terminations appear on the logic patch panel to permit assigned summing amplifiers to be converted to track-and-store amplifiers. Logic inputs allow control of their mode of operation, i.e., track or store. Normal summer operation is not affected when they are not being used as track-store units.

Digital/Analog Switches: These components provide a means for switching analog inputs to amplifiers under control of logic signals. Each unit consists of a series-connected, gain 10 resistor and an electronic switch terminated on the analog patch panel. A high signal to the switch input located on the logic patch panel causes a voltage patched to the series resistor to be switched to the input of an amplifier, when the switched end is patched to the amplifier summing junction.

Relay Coils: Drive inputs located on the logic patch panel permit logic signals to be used to control the position of like-numbered DPDT relay contacts terminated in the normal comparator area of the analog patch panel. A high logic signal to the drive input causes the relay contacts to throw to the "+" position on the analog panel.

Mode Relay Drivers: Drive inputs on the logic patch panel permit logic signals to be used to produce a voltage on the analog patch panel capable of driving up to ten (10) regular mode control relays. A high signal produces a 90 volt pulse returning to 21 volts; a low signal returns the control voltage to zero.

Timers: A basic 10 KC square wave is provided for use to determine the basic interval from which synchronous signals for control of integrator switches and logic programs can be derived. When a Repetitive Operation Display Unit is provided, synchronized square waves of 250, 500, and 2500 cps are also available.

Counter Drivers: A Master Drive and a Slave Drive are provided, each capable of generating rectangular waves with controlled duration of each state. Complementary outputs are provided which are capable of driving all the electronically-switched integrators. Each counter can provide a change of state after 1 to 999 counts, then a change to the opposite state after 1 to 999 counts, alternating from then on. Initialization and reset of counters, and outputs to either state can be accomplished as a function of other logic signals by appropriate patching.

AND Gates: These gates are provided with from two to four inputs and with complementary outputs. Each gate is capable of performing the fundamental logical multiplication operation, i.e., when all inputs are high, or unconnected, the output will be high. Conversely, if any of the inputs are low, then the output will be low.

Programmers symbols for the units described above are shown in Figure 30.

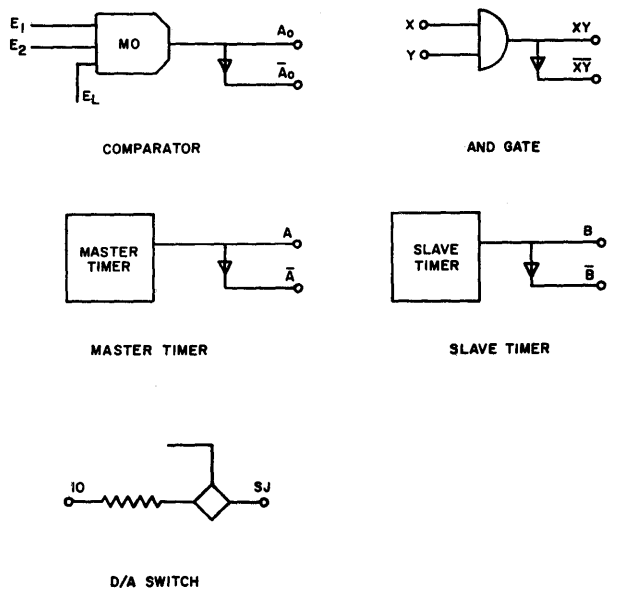


Figure 30: Computer Symbols for Multi-Speed Operation Components.

IV-b: Computer-Mode-Controlled Track-Store. MICROSTORE units are connected as described in Section III-b, except that switch inputs are driven from complementary output signals of the Master or Slave Timer Drivers (A or B in Figure 30). Assigned Track-Store amplifiers are connected by grounding the numbered tan terminals on the logic patch panel. Switch inputs are the same as for the MICROSTORE units. The complementary mode of integrator operation can be obtained easily for any integrator by applying the proper state of the output of the Master or Slave Timer Drivers to the drive input of its high-speed electronic switch (the electronic switch has to be activated and a suitable time scale selected by patching). Thus, by omitting rate inputs to the integrator, it can be used to track-and-store or store-and-track a signal applied to the normal IC termination.

IV-c: Comparator-Controlled Track-Store. Connections are the same as for mode-controlled track-and-store or store-and-track operation, except that the switch inputs are driven from the

comparator logic output signals. The normal comparator signal inputs are entered at the E_{in} terminations on the analog patch panel. The computer symbols for the MICROSTORE units are the same as those shown in Figure 24. The symbols for the assigned track-store amplifiers and complementary integrators are shown in Figure 31.

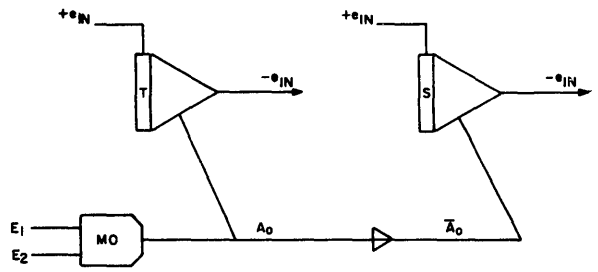


Figure 31: Combined Track-Store Memory Under Comparator Control Using Electronically Switched Integrators.

IV-d: Track-Store Combined Memory. Combined memory is easily accomplished by the series connection of track-store and store-track units for either method of control. The same comments made in Section III-d regarding the use of the comparator latch inputs also apply here. Note that comparator latching is performed much more easily and with greater flexibility with the conveniently available logic signals.

IV-e: Counting Circuit. While it is possible to assemble counting or accumulator circuits in the manner described in Section III-e and illustrated in Figure 26, a much more satisfactory arrangement is to use the Master and Slave Counters provided with the Memory and Logic System. For example, the Slave Counter might be set up to count the number of OPERATE cycles generated by the Master Counter and, at the conclusion of the number of cycles determined by the thumbwheel controls of the Slave Counter, a logic signal could be generated which is used to force the output of the Master Counter to a desired state, thereby interrupting or suspending the cycling of the computer between modes.

IV-f: Curve Storage and Interpolation. The comments made in Section III-f also apply to curve storage and interpolation with multi-speed operation. Note, however, that the availability of logic capability, combined with the flexibility of the system provided for multi-speed operation, permits the implementation of a variety of interpolation schemes.

SECTION V: SOME GENERAL APPLICATIONS OF ANALOG STORAGE

V-a: General. In a certain sense, there is no such thing as an "area of application" for storage devices anymore than there is an "area of application" for multiplication devices, functions generators, etc. They are simply the tools--the components in the computer--that permit solution of a problem. On the other hand, high-speed storage has opened up some areas of application of the analog computer that were not considered feasible before, and that will undoubtedly expand in use as newer and faster equipment is developed. Some of the areas in which storage is required or advantageous are summarized in this section.

V-b: Data- and Curve-Fitting Problems. When experimental data has been gathered on a process, and a set of mechanisms has been proposed, there are still several choices left to the analyst as to how he might best match the model and the data. The three most common methods are:

(1) Visual matching in high-speed repetitive operation with manual adjustment of parameters.

(2) Minimizing or maximizing some criterion by manual adjustment of parameters.

(3) Using a criterion as above, with automatic parametric changes.

The choice of a particular technique will depend upon the nature of the problem, the amount of data (number of points or curves), and the number of unknown parameters. For a large quantity of data and many parameters, visual matching, at least initially, is the most profitable and requires the least equipment. Expansion to include some form of error criterion (e.g., least squares, or minimum $\int|\varepsilon|$ is quite easy when complete curves are available, since these may be placed on a DFG, continuously compared with the model curves, and the error criterion displayed as an output.

When the input information is a series of points, track-store units are employed to pick off the computer points for comparison. By using the latch input to comparators in these cases, only one amplifier is required for each point as seen in Example I. For many points, however, this is expensive in amplifier requirements. It is advisable, therefore, to consider drawing continuous curves from a number of points and representing them on a DFG whenever possible.

The techniques for making automatic parametric changes are also more powerful when the experimental data are a continuous curve. Most of the work in this area, however, has been done with sampled-data systems since the iteration techniques have been developed primarily for digital computer users. For such cases, the computer model curve is tracked, the proper point stored and compared with the experimental datum point, the error criterion evaluated, and the adjustment made in one (or sometimes more) of the parameters. This is continued in a repetitive manner until the error criterion is satisfied.

Most of the techniques for evaluating the error criterion and making changes in the parameters also involve use of track-store units. These will be seen more thoroughly in future discussion of automatic parameter evaluation techniques.

V-c: Boundary Value Problems. Another class of problems that are often extremely important are those in which an initial condition must be guessed until a boundary condition is matched. The problem here is quite similar to the data-fitting situation already discussed, and the choice of manual or automatic techniques for solution is the same, except that an initial condition, rather than a problem parameter, is varied until the error is zero. The use of a track-store memory, together with a simple iteration technique, does not usually require much equipment and represents a powerful tool for such problems.

V-d: Stagewise Calculations. Many of the separation operations in chemical engineering are calculated in a serial or stage-wise manner. Here, the results of one calculation are required as inputs to the next calculation but the equations remain

essentially the same. Typical of such processes are steady-state distillation calculations by the McCabe-Thiele or similar methods. On top of the basic calculation is often imposed the complexity of multi-component systems, and trial and error "guess-the-overhead-composition-and-see-if-the-bottoms-make-an-overall-material-balance" computations. The use of real-time storage with the analog computer for multi-component distillation calculations is in the literature (2). The extension to high-speed repetitive operation is a natural step, as seen in the simple binary problem of Example II.

A word of caution should be given about the number of steps employed in a serial calculation with the analog computer. In the distillation example, the term (L/V) appears as a multiplier N times, where N is the number of plates. This is equivalent to $(L/V)^N$, and represents a source of increasing error in the computation. For even a 0.1% error in the value of (L/V), there will be an error of 10% at the end of 100 plates. Consequently, every means must be taken to insure accuracy in such calculations, and if possible, reduce the number of steps.

V-e: Serial Solution of Partial Differential Equations. Example III demonstrates the use of real-time storage for serial solution of the partial differential equations for composition transients in a fixed-bed ion exchange process. Various papers are also available describing techniques for high-speed serial solution of the thermal diffusion equation when the boundary conditions have been simplified. Most of these problems are characterized by their high degree of non-linearity, and consequent high non-linear equipment requirements when parallel solution is attempted. In these situations, serial solution presents a very attractive possibility; the repetition of circuitry is traded for a single basic circuit together with storage and interpolation requirements. The accuracy problems inherent in curve generation from point storage must be considered, but the overall approach is certainly desirable and necessary, in some cases, and represents an area in which storage can be used to good advantage.

V-f: Multi-speed Computer Operation. A new field of application of the analog computer is in the area of multi-speed operation. While the range of usefulness of this concept is largely unexplored, there is no question that it will be expanded in the future. For such situations, many kinds of storage, operating at different solution times, will be required for conversion from one time domain to another.

V-g: Optimization Techniques. Various kinds of storage are required for process optimization techniques, whether "on-line" in a plant or as a computation tool. The use of track-store memory for automatic parameter evaluation in model building has already been mentioned; a natural extension of the same idea is that of model optimization by automatic techniques in which process variables (temperature, pressure, etc.) are varied to satisfy an economic criterion. Both of these require simple point storage.

EXAMPLE I: Data-Fitting by Least-Squares Error.

The results of a laboratory experiment yield the value of a function y(t) at several points in time, t_i, as follows:

$$t_o = 0 \quad ; \quad y_o = 0$$

$$t_1 = 0.25 \; ; \; y_1 = 49.23$$

$$t_2 = 0.50 \; ; \; y_2 = 28.58$$

$$t_3 = 0.75 \; ; \; y_3 = 19.56$$

$$t_4 = 1.00 \; ; \; y_4 = 12.85$$

A mechanism has been proposed such that $y_{(t)}$ can be described as the difference between two exponential decays:

$$y = A\,(e^{-at} - e^{-bt})$$

where the value of A is known and constants "a" and "b" are the unknown parameters. It is desired to evaluate "a" and "b" such that $\Sigma_i |E|^2$ is a minimum, where $E = y(t)_1 - y(t)_{experimental}$. A suggested circuit diagram is shown in Figure 32.

At the upper left in the circuit is the system circuit describing y(t) according to the assumed model. This value is fed into a series of 4 track-store circuits and compared with the experimental values of $y(t)_i$. The output errors are squared and summed in amplifier #07. Since, at the beginning of the operate cycle, all of these units are tracking, the errors E_i^2 and ΣE_i^2 will be large; hence amplifier #07 must be limited. At time t_1, the first track-store gate will lock on E_1 at time t_2, on E_2, etc. until, at the end of the operate cycle, we have the correct value of ΣE_i^2. The function switch around amplifier #07 allows the operator:

(1) In the "L" position, to obtain "ball-park" values of the parameters.

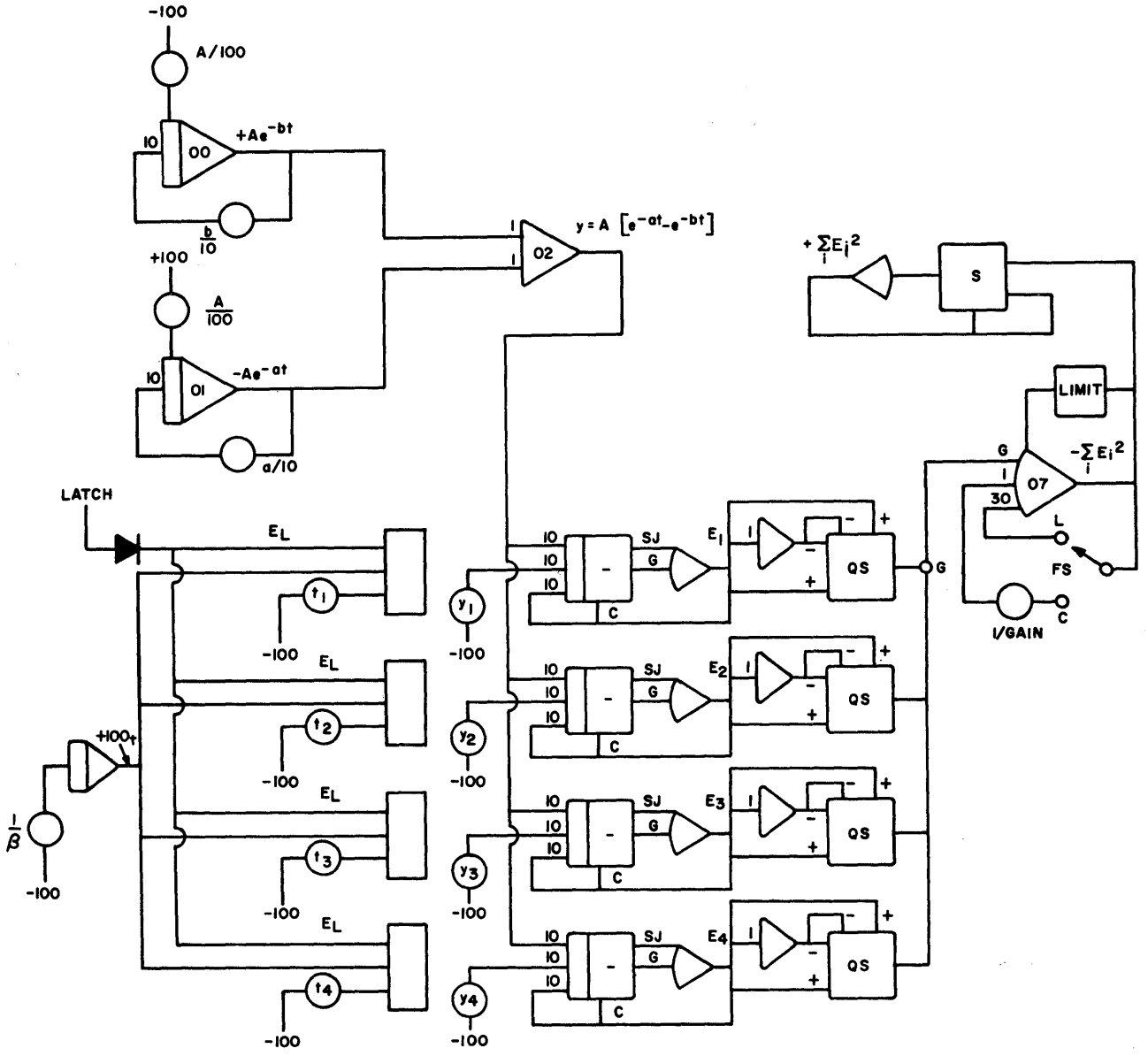


Figure 32: Circuit Diagram for Performing Data-Fitting by Least-Square Error.

(2) In the "C" position, to amplify the least-square error output when the values of "a" and "b" are nearly correct.

Following amplifier #07 is a store-track amplifier which will hold the value of the sum of square errors from the last cycle. Since this unit will track during the IC mode, the four comparator-controlled track-store gates must be kept in the "store" position until the next operate cycle begins. This is accomplished by the latching circuit on the comparators. The visual display of the least-square error line permits rapid and accurate data-fitting.

EXAMPLE II: Binary Non-Ideal Fractional Distillation.

Saturated liquid feed, containing 50 mole percent of the light component, is fractionated in a column containing 80 theoretical plates. The overhead contains 98 mole percent of the light component at a recovery of 95 percent. Assuming constant molal overflow, calculate the reflux requirement.

For the total theoretical plates given, the calculation procedure will be to guess a reflux rate and calculate down from the overhead composition ($x_D = y_1$) until the bottom (n = 80) tray is passed.

The change in the material balance will be automatically switched in when the feed tray is passed, i.e., when $x_n = x_f$. The calculated x_W bottoms composition is compared with the value obtained by overall material balances, and the difference displayed. A new value of reflux rate is then chosen until x_W is correct.

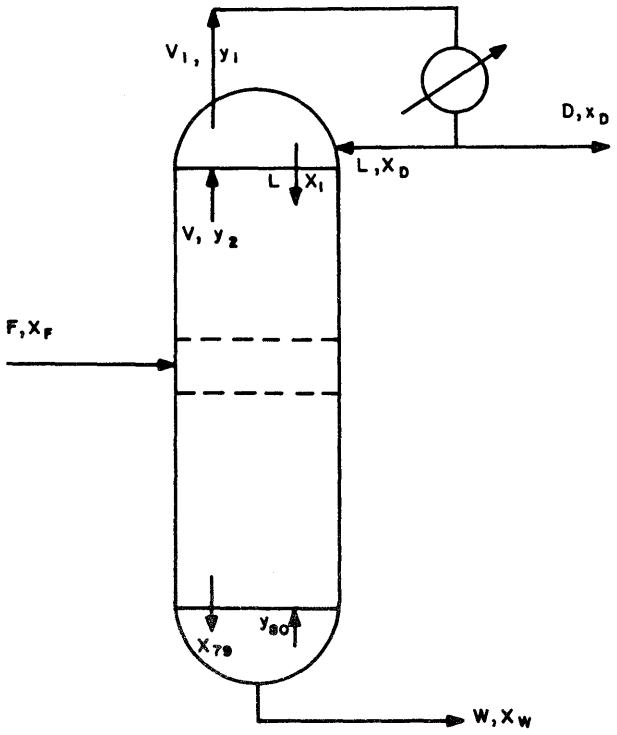


Figure 33: Schematic Diagram of Distillation Column.

Summary of Equations

Equilibrium:

$$y_n = \frac{\alpha x_n}{1 + (\alpha - 1) x_n}$$

$\alpha = \alpha(x_n)$ a function easily obtained once the components are specified.

Define

$$K(x_n) = \frac{\alpha}{1 + (\alpha - 1) x_n}$$

Then

$$y_n = K(x_n) \cdot x_n$$

Material Balance Equations

Top of Column (total condenser)

$$\frac{dx_1}{d\theta} = \frac{1}{K(x_1)} \left[\frac{L}{V} x_D + \frac{D}{V} x_D \right] - x_1$$

Plate "n" (above feed)

$$\frac{dx_n}{d\theta} = \frac{1}{K(x_n)} \left[\frac{L}{V} x_{n-1} + \frac{D}{V} x_D \right] - x_n$$

Feed Plate

$$\frac{dx_{f+1}}{d\theta} = \frac{1}{K(x_{f+1})} \left[\frac{L}{V} x_f - \frac{W}{V} x_w \right] - x_{f+1}$$

Plate "N" (below feed)

$$\frac{dx_N}{d\theta} = \frac{1}{K(x_N)} \left[\frac{L}{V} x_{N-1} - \frac{W}{V} x_w \right] - x_N$$

The circuit required for solving the material balance and equilibrium equations for a single tray, plus the necessary storage amplifiers for the sequential calculation of the total number of trays, is shown in Figure 35. Figure 34 shows a special circuit used to generate the equilibrium function. Additional accuracy is obtained by approximating the function with a straight line and adding to this a calculated error term represented on a DFG.

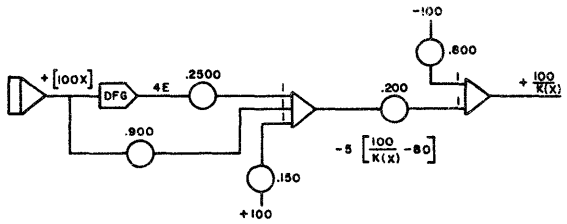


Figure 34: Special Circuit for Generating Equilibrium Function.

EXAMPLE III: Analog/Digital Memory Applied to Fixed-Bed Transients*

A digital memory channel is a device that will store a set of numbers. For analog solution of certain types of problems (i.e., partial differential equations), these numbers can represent successive values of a time variable as illustrated in Figure 36. The original function c(t), shown as a solid curve in Figure 36, could be reproduced with satisfactory accuracy by linearly interpolating between the stored numbers n_1, n_2, etc.

*This problem was performed by Mr. Roger Franks of the Systems Eng. Section, ESD, E.I. DuPont & Co., and is reproduced with their permission.

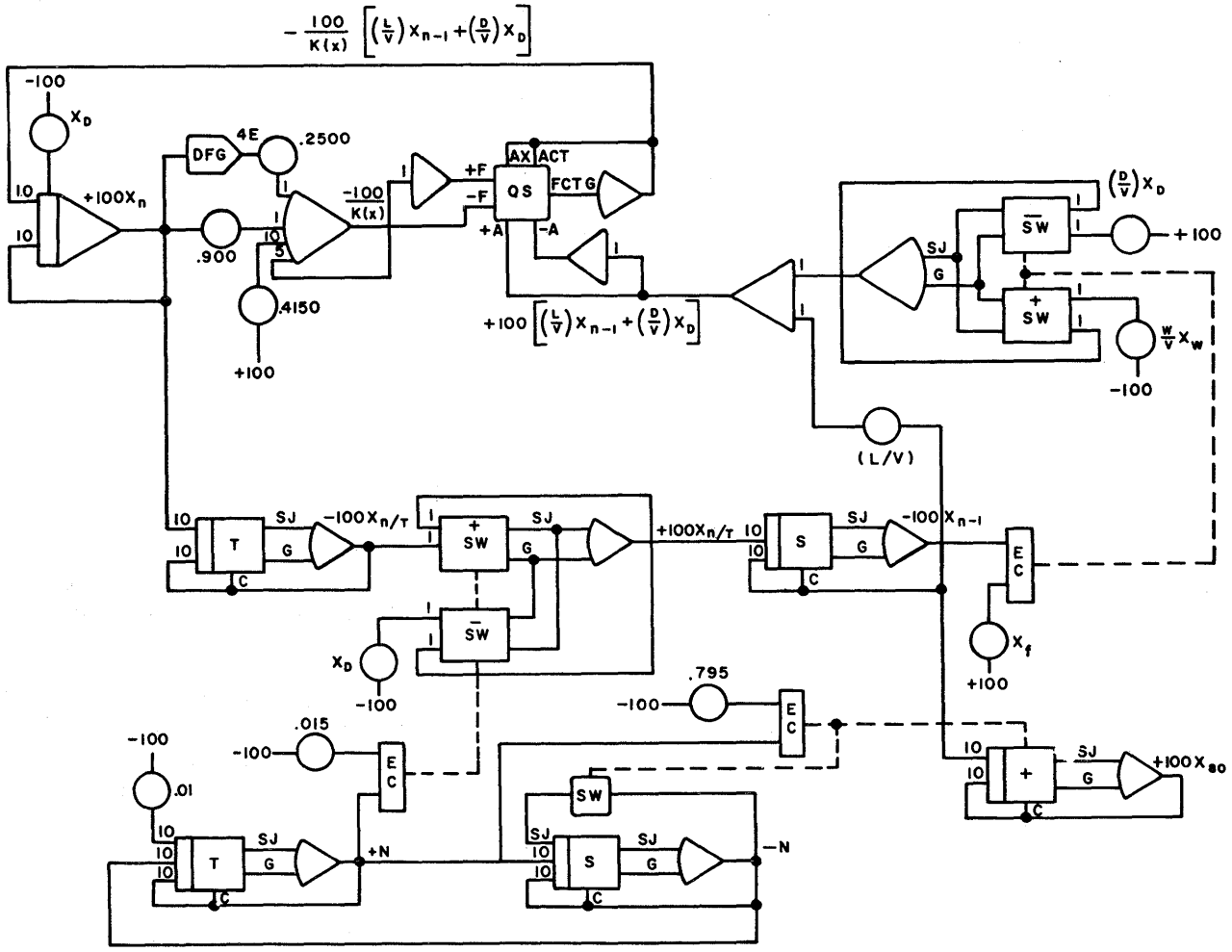


Figure 35: Circuit for Steady State Calculation of Binary Distillation.

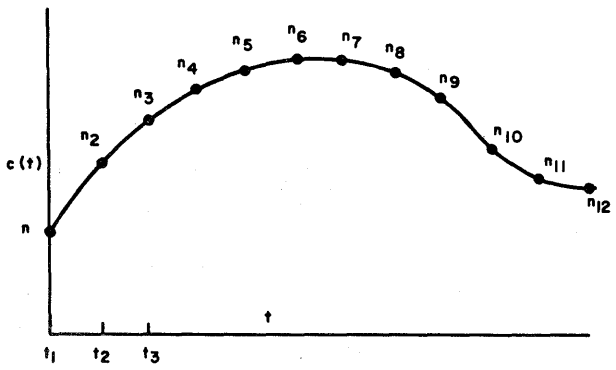


Figure 36: Sampled Points in Time.

For such solution schemes, the memory channel receives two signals from the analog computation circuits, namely, a time voltage and the time dependent value c(t). At preselected values of time (t_1, t_2, etc.), the memory will store the successive values of c(t). At the end of the solution run, it should be possible to drive the memory channel with t (starting from t = 0) and reproduce the linearly interpolated function c(t). In other words, this is the definition of an automatically-set function generator. A more generally useful memory for analog computation has the capability of storing a new function while at the same time reproducing a previously stored function (Figure 27).

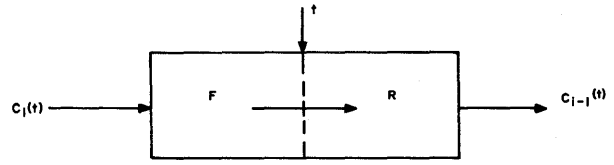


Figure 37: Functional Diagram of a Combined Memory. Such a memory would consist of two parts, a forward (F) and reverse (R) memory. The former stores the current result, $c_i(t)$, while the latter reproduces the previous result, $c_{i-1}(t)$. Transfer of $c_i(t)$ from the forward to reverse memory can take place any time after $c_{i-1}(t)$ has been used.

The greatest value of such a device is where it is necessary to use the results of a previous computation for a new computation, requiring rapid storage and reproduction of a function. The technique is applicable to a number of problems in chemical engineering, and especially to composition transients through fixed beds (Kinetics, absorption, adsorption, diffusion, heat transfer, etc.).

A typical example is a fixed-bed ion exchange process (Figure 38), where a solution containing a component A is passed through a fixed resin bed

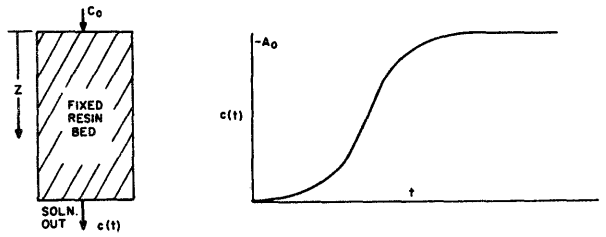


Figure 38: Fixed-Bed Ion Exchange Process.

that will absorb the A component until the resin absorption capacity is exhausted. At this time, the effluent solution concentration of A will start to increase up to the maximum inlet concentration A_o. A mathematical model programmed for computer solution allows an investigation of the effect of varying the system parameters such as solution flow rate, bed depth, resin properties, etc..

Equations: The complete system is mathematically defined as a set of partial differential equations with three independent variables: time, axial length (down the column), and radial length (diffusion into the resin bed). Considering an incremental length of the column, ΔZ, the conservation equation for the solution can be written as:

$$f_V \Delta Z \frac{dC_n}{dt} = S(C_{n-1} - C_n) - aD_L (C_n - C_n^*)$$

and for the resin particle diffusion (See Figure 40)

$$\Delta V_{Rn} \frac{d\phi_n}{dt} = D_R \left(\frac{\phi_{n-1} - \phi_n}{\Delta r}\right) + \frac{\phi_{n+1} - \phi_n}{\Delta r}$$

Interface equilibrium is defined as

$$C^* = f(\phi^*)$$

Where

For solution

S = Flow Rate

C = Concentration

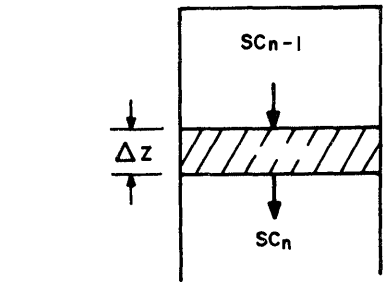


Figure 39: Unit Cross Section of Ion Exchange Column.

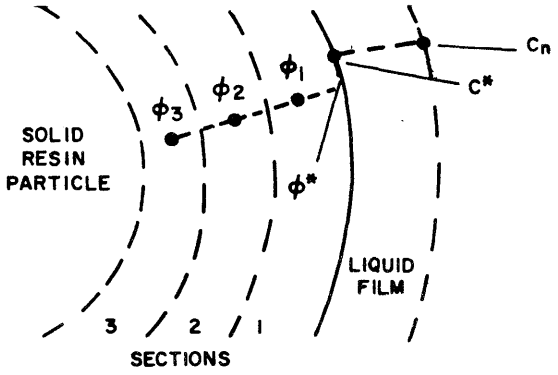


Figure 40: Resin Particle Diffusion.

f_V = Void Fraction

D_L = Diffusion Coefficient

a = Surface in ΔZ

Z = Column Length

For Resin

R = Radius of Particle

ϕ = Concentration

V_{Rn} = Part Volumn

D_R = Diffusion Coefficient Slice.

The analog program for one axial slice, ΔZ, and ten (10) radial segments is shown in Figure 41. The overall solution scheme for ten (10) axial segments is shown in Figure 42. Since 11 integrators are required for each axial slice, a total of 110 integrators would be required for the entire bed, which requires a rather large computer.

Referring to Figure 42, it will be seen that since the program in each axial slice block is the same for all blocks, and since there is only one signal,

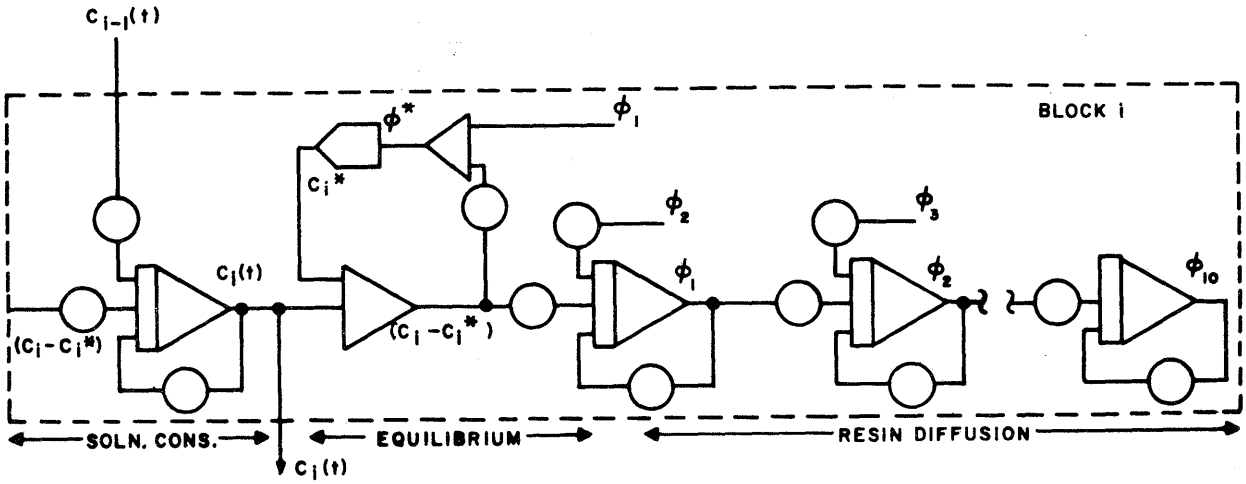


Figure 41: Analog Program for One Axial Slice of Ion Exchange Column Representation.

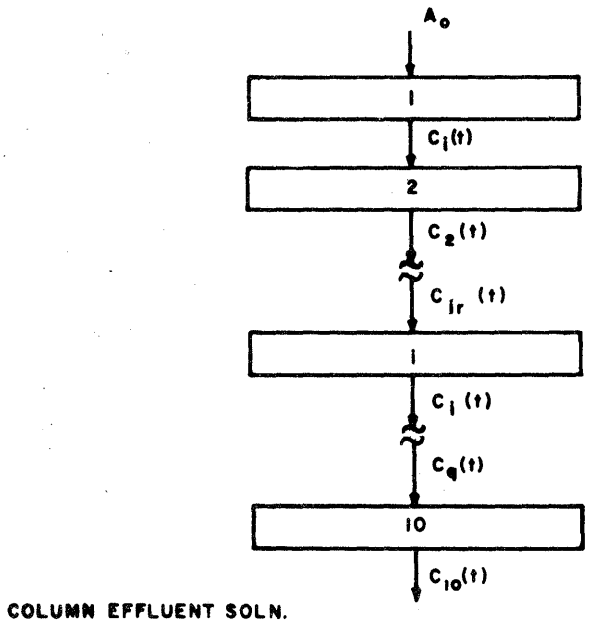


Figure 42: Overall Solution Scheme for Fixed-Bed Ion Exchange Process.

Figure 43: Solution Scheme for Fixed-Bed Ion Exchange Process Using Memory.

c(t), passing forward to each block, the entire computation could be made by programming just one block and passing the result of the computation, $c_1(t)$, to a memory channel. Resetting the analog circuits and starting again with this stored signal as the driving function, a new signal, $c_2(t)$, is produced which is in turn stored and used again; and so on. (See Figure 43).

A typical result for an ion exchange column is shown in Figure 44.

This method would only require 11 integrators plus the integrators required for the memory channel. The main disadvantage of the method is that more time is needed to complete each run since the entire bed has to be computed serially, slice by slice. On the other hand, the method reduces considerably the amount of computation equipment required--in this case, a 75% reduction of integrators and a 90% reduction in non-linear equipment.

Figures 45 and 46 show two schemes for a practical memory channel that can be put together for the analog computer, using components already available, except the second example which uses a stepping switch but eliminates 17 relays and amplifiers. The memory channel consists simply of a set of sample-clamp circuits operated sequentially by

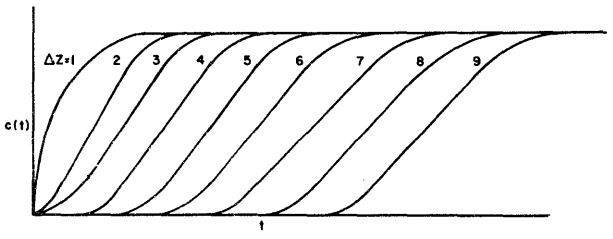


Figure 44: Typical Results of Ion Exchange Column Calculation.

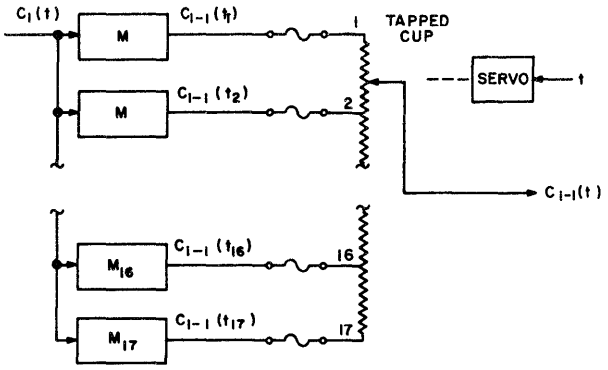


Figure 45: Memory Channel Interpolation Scheme Employing Servo-Multiplier Tapped Potentiometer.

either operational relays or a stepping switch. In both cases, the forward memory consists of a bank of condensers, while the reverse memory are the integrators. The linear interpolation is obtained by connecting the output of the integrators to the taps of a servo potentiometer, and driving the servo by the time signal, t. As soon as the servo potentiometer arm has passed a given segment, the forward memory capacitor can be discharged into the integrator. This double action explains the cross connection in the stepping switch bank and the double set of relay contacts in the relay-type memory.

Both memories are programmed to be entirely automatic, such as cycling through each run, resetting, lifting and lowering the plotter pen on each run and so on (circuits not shown in Figures 45 and 46).

EXAMPLE IV: Multi-speed Operation as Applied to Control of a Chemical Reactor.

A typical example of the use of multi-speed operation is the study of the control characteristics of a tubular chemical reactor (Figure 47). Fluids or gases are reacting while flowing rapidly through the reactor, and the input flow rates and reactor temperature are adjusted as functions of the outlet concentration of some constituent.

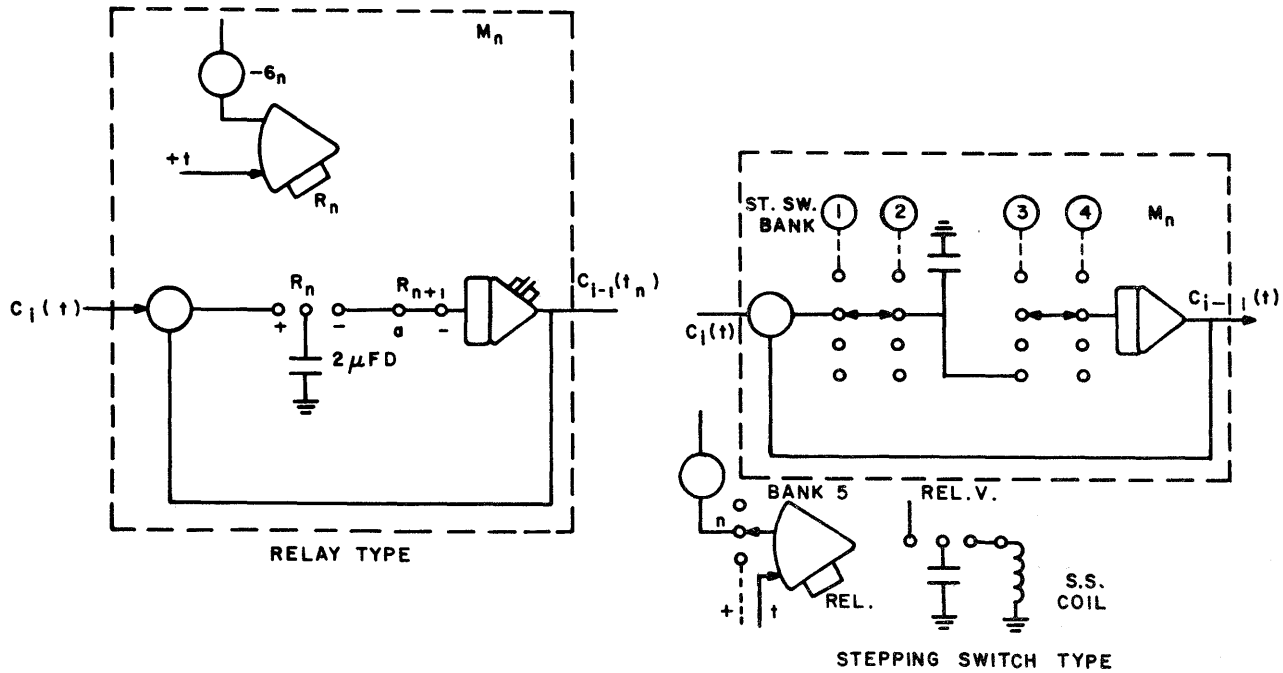


Figure 46: Storage Channel Employing Special Switching Circuits. Messrs. W.S. Sloan and D.N. Miller (E.I. DuPont deNemours and Co.), by their interest in this approach, have stimulated its development. The assistance of R.W. McClure and the Louviers Analog Maintenance Staff in the development of the device is gratefully acknowledged.

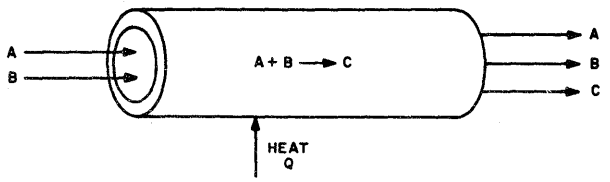


Figure 47: Schematic Diagram of Tubular Chemical Reactor.

The reaction rate differential equations must be solved for a small volume of gas with certain inlet or initial conditions, to determine the outlet state of that typical volume of gas. If the conditions outside of the reactor are to be solved in real time, the behavior of that typical volume of gas moving down the tube must be computed in a shorter time interval compared with the time required for the controllers or inlet conditions to make a significant change. Thus, the reaction rate equations are solved at high speed, with the fast time, τ, related to distance, x, along the reactor by the gas velocity. $V = x/\tau$. The outlet conditions are sampled after each calculation and smoothed to form the inputs to the controllers which are simulated in real time. The solution scheme used is illustrated by the diagram of Figure 48.

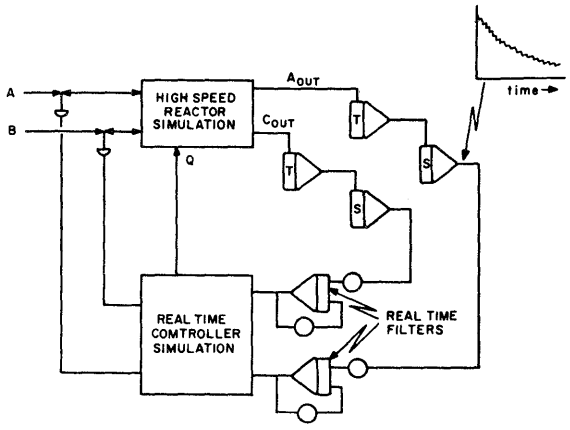


Figure 48: Solution Scheme for Investigation of Control Performance of Tubular Chemical Reactor Utilizing Multi-Speed Computer Operation.

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