EAI®

ELECTRONIC ASSOCIATES, INC. *West Long Branch, New Jersey*

SINE COSINE DIODE FUNCTION GENERATORS MODELS 16.313 & 16.314

Publ. No. D800 2005 0A

PRINTED IN U.S.A.

November 1964

NOTICE

In order to enable us to process your requests for spare parts and replacement items quickly and efficiently, we request your conformance with the following procedure:

1. Please specify the type number and serial number of the basic unit as well as the identification of the part when inquiring about replacement items as potentiometer assemblies or cups, relays, transformers, precision resistors, etc.

2. When inquiring about items as servo multipliers, resolvers, networks, cables, potentiometer expansions, etc., please specify the serial numbers of the major equipment with which the units are to be used, such as: Console Type 231R, Amplifier Group Type 4.028, serial #000, etc. If at all possible, please include the purchase order or the EAI project number under which the equipment was originally procured.

Your cooperation in supplying the required information will facilitate the processing of your requests and aid in assuring that the correct items are supplied.

It is the policy of Electronic Associates, Inc. to supply equipment patterned as closely as possible to the individual requirements of the individual customer. This is accomplished, without incurring the prohibitive costs of custom design, by substituting new components, modifying standard components, etc., wherever necessary to expedite conformance with requirements. As a result, this instruction manual, which has basically been written to cover standard equipment, may not entirely concur in its content with the equipment supplied. It is felt, however, that a technically qualified person will find the manual a fully adequate guide in understanding, operating, and maintaining the equipment actually supplied.

Electronic Associates, Inc. reserves the right to make changes in design, or to make additions to or improvements in its product without imposing any obligation upon itself to install them on products previously manufactured.

Printed in U.S.A.

M226

SALES OFFICES

EASTERN REGIONAL OFFICE
Long Branch, New Jersey
Telephone: Area Code 201
229–1100
TWX-LG BR 201-222-2795
Cable-PACE Long Branch, N.J.

R & D & SPECIAL PRODUCT SALES
Long Branch, New Jersey
Telephone: Area Code 201
229–1100
TWX-LG BR 201-222-2795
Cable-PACE Long Branch, N.J.

PARTS SALES
Long Branch, New Jersey
Telephone: Area Code 201
229–1100
TWX-LG BR 201-222-2795
Cable-PACE Long Branch, N.J.

N.Y. DISTRICT OFFICE
111 Main Street
P.O. Box 218
North Syracuse, N.Y.
Telephone: Area Code 315
GL8-2188

NORTHEAST DISTRICT OFFICE
711 Main Street
Waltham, Massachusetts
Telephone: Area Code 617
TWinbrook 9-0420

CENTRAL REGIONAL OFFICE
101 South Pine Street
Mount Prospect, Illinois
Telephone: Area Code 312
CLearbrook 5-6070
TWX-ARL HTS 3315

SOUTHWESTERN REGIONAL OFFICE
108 Prentice Bldg.
Dallas 6, Texas
Telephone: Area Code 214
EMerson 1-6165

WESTERN REGIONAL OFFICE
1500 East Imperial Highway
El Segundo, California
Telephone: Area Code 213
EAstgate 2-3124
TWX 213-322-2144

SAN FRANCISCO DISTRICT OFFICE
4151 Middlefield Road
Palo Alto, California
Telephone: Area Code 415
321–0363
TWX: 415 492–9211

EUROPEAN CONTINENTAL REGIONAL OFFICE
Centre International, 22nd Floor
Place Rogier, Brussels 1, Belgium
Cable: PACEBELG Brussels
Telephone: Brussels 18-40-04
Telex: 2.21-106

SOUTHEASTERN DISTRICT OFFICE
7902 Old Georgetown Road
Bethesda 14, Maryland
Telephone: Area Code 301
652-3625
652-3626

EAI–ELECTRONIC ASSOCIATES GMBH
Martinstrasse, 14
Aachen, W. Germany
Telephone: 26041

UK & SCANDINAVIAN REGIONAL OFFICE
Electronic Associates, Ltd.
Burgess Hill
Sussex, England
Telephone: Burgess Hill (Sussex) 5101–5
Cable-LONPACE
Telex: 87183

EAI–ELECTRONIC ASSOCIATES SARL
11, rue du Faubourg Poissonniere,
Paris 9, France
Telephone: PRO 93-69

AUSTRALIAN REGIONAL OFFICE
EAI-Electronic Associates, Pty., Ltd.
87 Alexander Street
Crows Nest
Sydney, N.S.W.
Australia
Telephone: 43-1557
Cable-PACEAUS, Sydney

MANUFACTURING PLANTS

ELECTRONIC ASSOCIATES, INC.
Manufacturing Division
Long Branch, New Jersey

ELECTRONIC ASSOCIATES, LTD.
Burgess Hill
Sussex, England

CUSTOMER SERVICE

SERVICE ENGINEERING
Long Branch, New Jersey
Telephone: Area Code 201
229–1100
TWX-LG BR 201-222-2795
Cable-PACE Long Branch, N.J.

COMPUTATION CENTERS

EAI COMPUTATION CENTER AT LOS ANGELES, INC.
1500 East Imperial Highway
El Segundo, California
Telephone: Area Code 213
EAstgate 2–3220

UK COMPUTATION CENTER
Electronic Associates, Ltd.
Burgess Hill
Sussex, England
Telephone: Burgess Hill (Sussex) 5101–5
Cable – LONPACE
Telex: 87183

EUROPEAN COMPUTATION CENTER
Centre International, 22nd Floor
Place Rogier, Brussels 1, Belgium
Cable: PACEBELG Brussels
Telephone: Brussels 18-40-04
Telex: 2.21-106

EAI RESEARCH AND COMPUTATION DIVISION
Integrated Controls Department
4151 Middlefield Road
Palo Alto, California

PRINCETON COMPUTATION CENTER
P.O. Box 582
Princeton, New Jersey
Telephone: Area Code 609
WAlnut 4-2900

MANUAL REVISION NOTICE*

ELECTRONIC ASSOCIATES INC.
LONG BRANCH NEW JERSEY

PAGE	ITEM / PARA	REVISION
		In order to standardize terminal designations the patch blocks for the Sine Cosine Diode Function Generators Models 16.313 and 16.314 have been relettered. During the transition period the B_1, B_2 and B_2' designations may appear as S_1, S_2 and S_2'. The functions of these terminals are identical in either case.

DATE	MANUAL TITLE	REVISION NOTICE
11/18/64	SINE COSINE DIODE FUNCTION GENERATORS MODELS 16.313 and 16.314	NO. 64-45 SH. 1 OF 1 SH.

* THIS MANUAL REVISION NOTICE IS ISSUED TO INCORPORATE IMPROVEMENTS OR CHANGES OF ROUTINE OR MINOR NATURE IN THE SUBJECT MANUAL.

CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

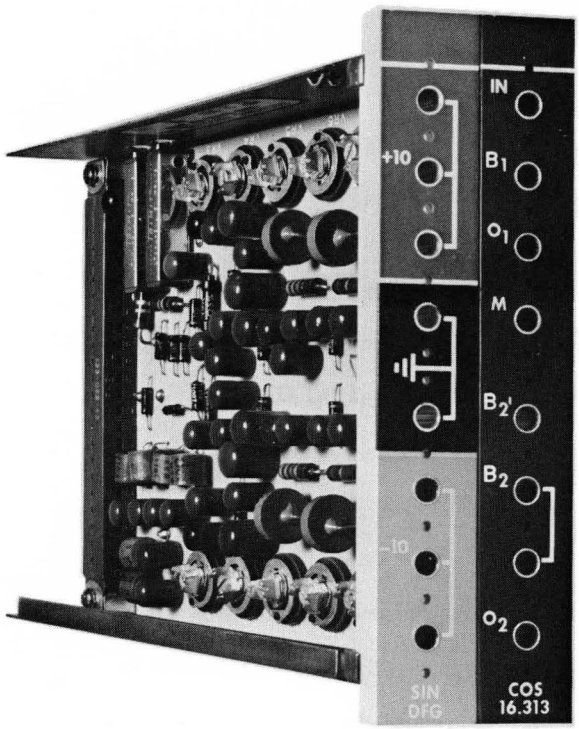


Figure 1. Sine-Cosine DFG, Model 16.313

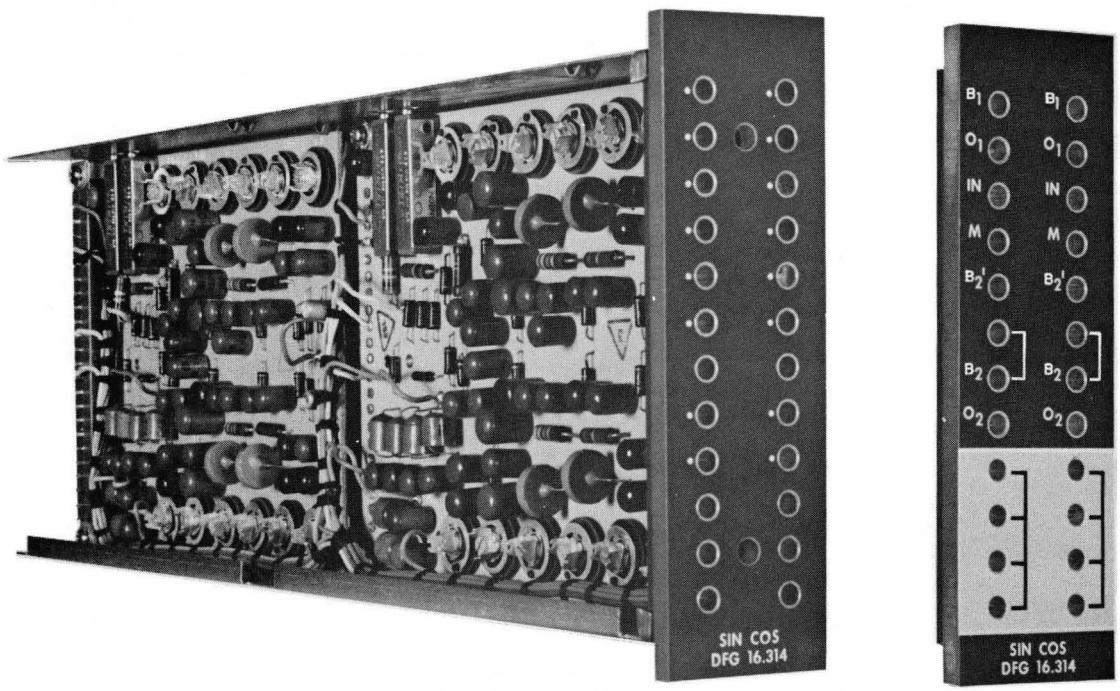


Figure 2. Sine-Cosine DFG, Model 16.314

CHAPTER I

INTRODUCTION

1. GENERAL

The Electronic Associates, Inc., Models 16.313 and 16.314, (Figures 1 and 2) Sine-Cosine Diode Function Generators (DFG) are non-linear fixed function generators designed for use with the EAI TR-20 and TR-48 General Purpose Analog Computers.

The Model 16.313 performs one conversion and the 16.314 performs two conversions of angular data to the sine or ± cosine functions within a range of ±180°.

2. FIXED DFG'S AND SHAPING NETWORK

Two similar DFG's, which together form a sine generator, are employed as the feedback elements of a computing amplifier permitting either positive or negative inputs to yield a sine function within the range ±90°. A shaping network, employed as a feedback element of a second computing amplifier, used in conjunction within both DFG's, extends their range to ±180°.

3. MODEL DIFFERENCES

The Model 16.313 DFG is designed for use with the TR-20 while the Model 16.314, Dual DFG is designed for use with the TR-48 General Purpose Analog Computer.

4. MATHEMATICAL OPERATIONS

The 16.313 and 16.314 DFG's will approximate the curves of any one of the following trigometric functions with 7 segments per quadrant.

a. Sine ±180°
b. - Cosine ±180°
c. + Cosine ±180°
d. Sine ±90°

The sine-cosine DFG can also be used in conjunction with multipliers to perform both polar-to-rectangular and rectangular-to-polar conversions.

5. PATCH BLOCK

Complete flexibility in the use of the DFG is provided by their integral patch blocks. Interconnections between the DFG's junction terminations (B1 and B2) and output terminations (01 and 02) on the patch block and their corresponding computing amplifiers are made by either bottle plugs and/or patch cords.

Each of the modes of mathematical operation described in Paragraph 4 of this chapter can be uniquely selected by patching the appropriate reference supply (either -10v, 0v, or +10v) to termination M. The input ramp is patched to termination IN.

CHAPTER II

TECHNICAL DATA

1. SPECIFICATIONS

Input Scaling (±10V Maximum = ±180°)

Sine Mode	18°/V (.0555V/Degree)
Cosine Mode	18°/V (.0555V/Degree)

Output Scaling (±10V Maximum)

Sine Mode	$\pm 10 \sin \frac{\pi X}{10}$
Cosine Mode	$\pm 10 \cos \frac{\pi X}{10}$

Accuracy

Static Error ..... Any Point Within ±180° (Any of the Three Modes)

Ambient Temperature Varying Between 12°C and 50°C:

Typical	±.2% (40MV) of Full Scale
Maximum	±.25% (50MV) of Full Scale

Ambient Temperature Varying Between ±5°C:

Typical	±.1% (20MV) of Full Scale
Maximum	±.15% (30MV) of Full Scale

Dynamic Error - Small Signal (With 6.282 Dual DC Amplifier):

Phase Shift (Typical)	5° at 1000 CPS
Peaking Within the Band Pass (Typical)	5% at 4000 CPS
Frequency Response (Typical)	3 db Down at >12K CPS

Zero Error - Less than 1MV (For Zero Input)

Noise (Any of the Three Modes)

Typical	5MV Peak-to-Peak
Maximum	10MV Peak-to-Peak

Stability Against Oscillations

The effective capacity of the generator on the summing junction is approximately 100 pf. For ±10v input each amplifier will stand (without oscillating);

.03 μF on the Output

.005 μF on the Summing Junction

2. POWER SUPPLY REQUIREMENTS

+15V	4.5 MA
+10V	2.2 MA
-10V	2.2 MA
-15V	4.5 MA

3. DIMENSIONS

a. Model 16.313

Width	1-1/2 Inches
Height	5 Inches
Length	6-1/2 Inches

b. Model 16.314

Width	1-7/16 Inches
Height	4-7/16 Inches
Length	12-1/2 Inches

4. UNIT LOCATION

a. Model 16.313

Located in adjacent position pair 17 and 18 on the TR-20.

b. Model 16.314

Located in slot 2 of module areas 4 and 6 and any of the comparator positions on the TR-48.

CHAPTER III

OPERATION PROCEDURES

1. GENERAL

As mentioned in Chapter I, Paragraph 5, each operating mode is uniquely selected by a single bottle plug, or patch cord, on the patch block.

Since the sine-cosine DFG is a fixed function generator the setting-up, or checking of the sine ±90° DFG's can be regarded as a maintenance procedure rather than an operating procedure. The setting-up procedures are described in Chapter V, Paragraph 4. Once set up however, the DFG's should require little attention.

The operating procedures are, as a result, very simple. To change from a selected trigonometric function, once patched, requires altering the input to terminal M.

2. SINE ±180° AND ± COSINE ±180° MODES

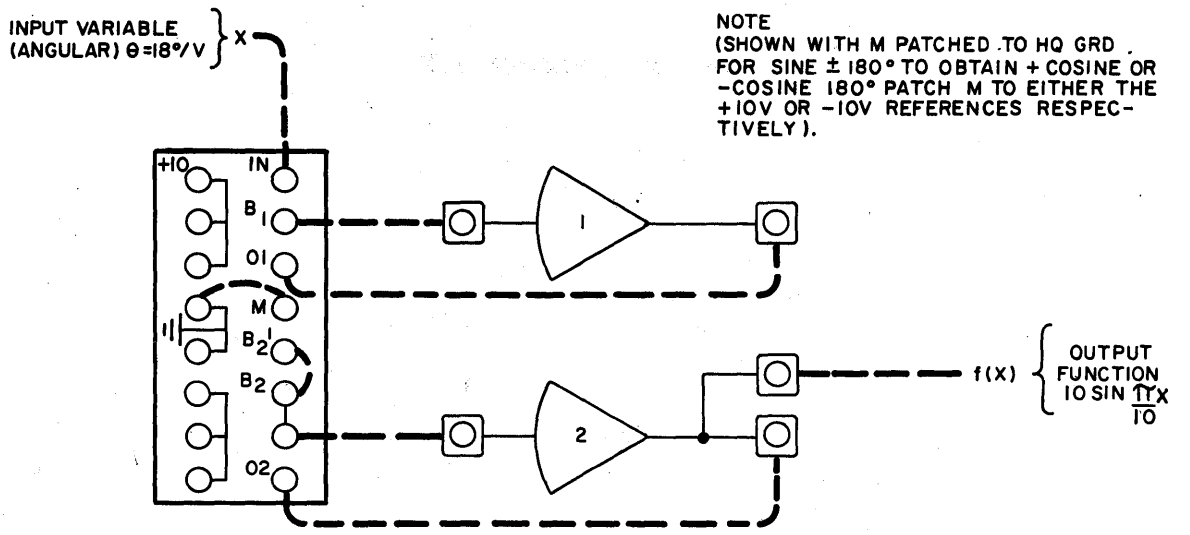
The sine and cosine modes require a suitable configuration of inter-connections (see patch block layout Figure 3) between the following elements:

(1) Computing amplifier -1 used in conjunction with the shaping network; terminals B1 (input) and 01 (output).

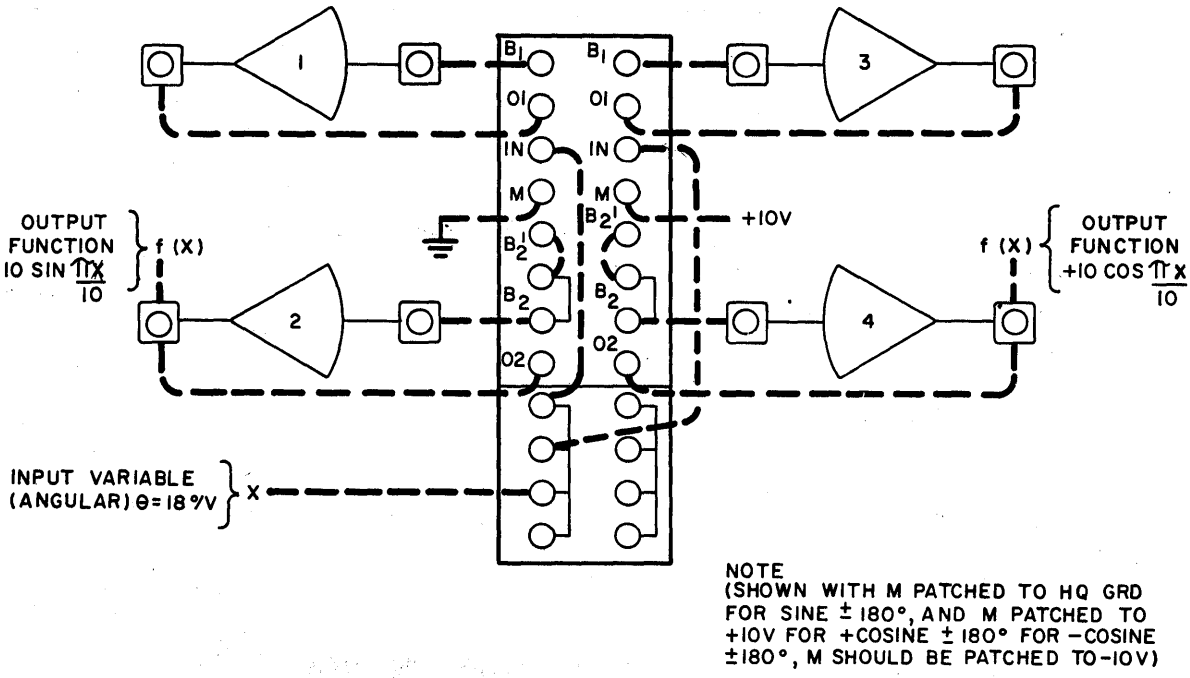
(2) Computing amplifier -2 used in conjunction with the sine generator (fixed DFG's sine ±90°), terminals B2 (input) and 02 (output).

(3) The shaping network output (B2') and sine generator input (B2).

The sine ±180° mode is illustrated in Figure 3 with the input to M at 0 volt (HQ GND) (for use with Model 16.313 only).



a. SINE OR COSINE ± 180° FOR MODEL 16.313



b. SINE ±180° AND +COSINE ±180° FOR MODEL 16.314

Figure 3. Patch Block Layout

a. Scaling

In the sine ±180° mode, the input voltage X represents an angle θ with a scaling of 18°/v (.0555v/degree); the output voltage Y equals 10 Sine $\frac{\pi X}{10}$ for values of X between ±10 volts. For example, if X = +2.5 volts, representing an angle θ of 45°, the corresponding output voltage is:

$$\left(10 \text{ Sine}(180)\frac{2.5}{10}\right)$$
$$= 10 \text{ Sine } 45$$
$$= 7.07 \text{ Volts}$$

The scaling for each of three modes is shown in Table 1.

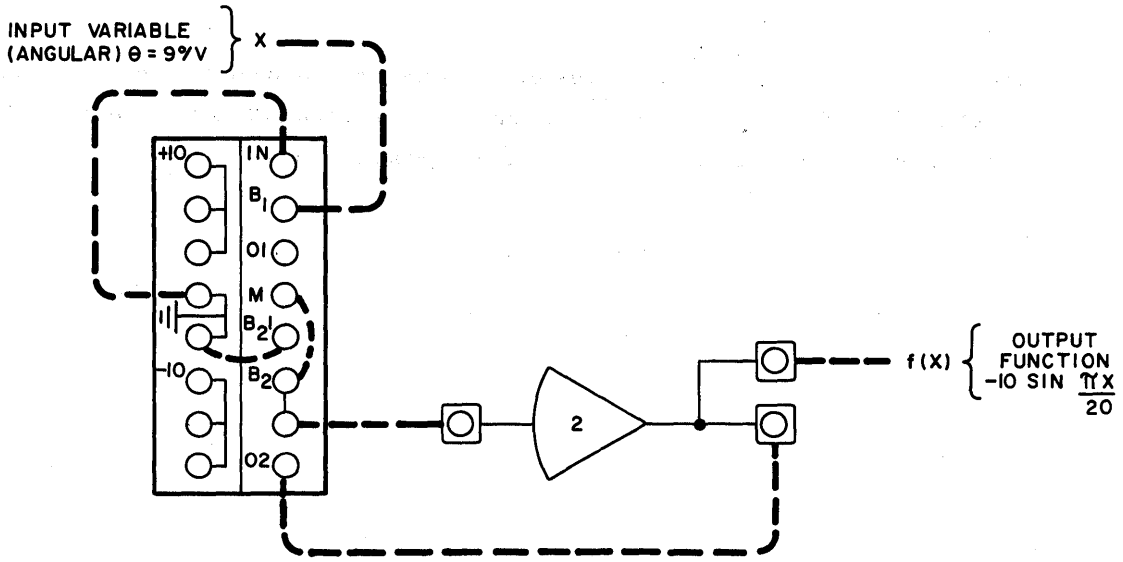
TABLE 1. Scaling

Mode Selection		Input Voltage		Output Voltage
Function	M	Range	IN (X)	
Sine	0V (HQ GND)	±10V (±180°)	.0555V/Degree	$10 \text{ Sin } \frac{\pi X}{10}$
+ Cosine	+10V Ref.	±10V (±180°)	.0555V/Degree	$10 \text{ Cos } \frac{\pi X}{10}$
- Cosine	-10V Ref.	±10V (±180°)	.0555V/Degree	$-10 \text{ Cos } \frac{\pi X}{10}$

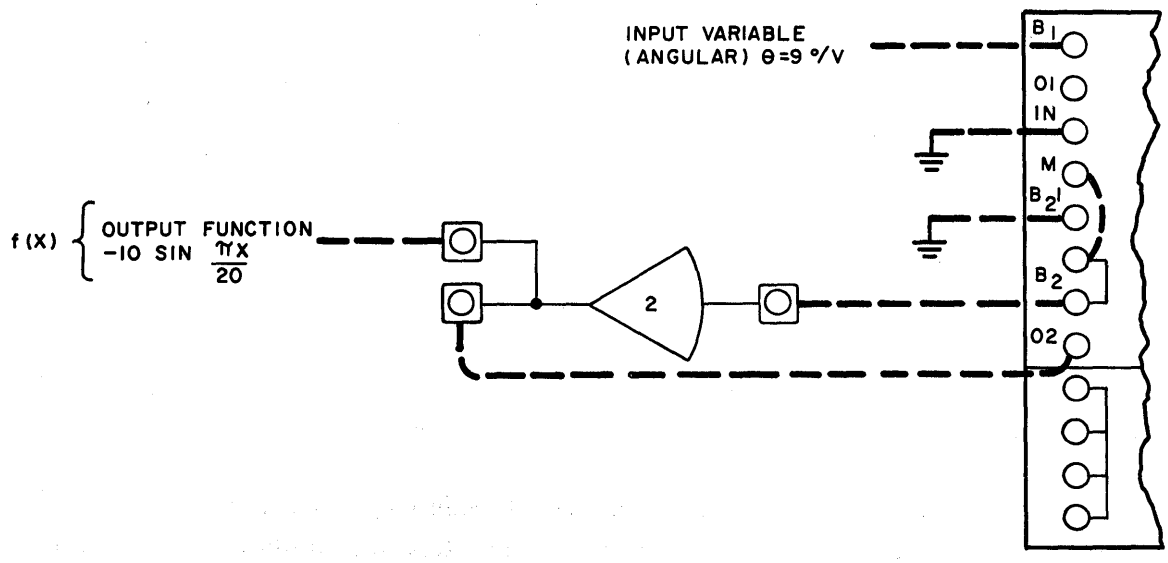
3. SINE ±90° MODE

If operation is restricted to the sine ±90° only the sine generator is required. To generate the sine ±90° the patching configuration must be as shown in Figure 4.

It should be observed that in the configuration shown in Figure 4, which requires only one computing amplifier, input IN and M do not perform the same functions as illustrated in Figure 3. Input IN is patched to HQ GND and input M is patched to input (B2) of the computing amplifier; the configuration is completed by patching B2' to HQ GRD and feeding the input variable X into B1. The need for this particular configuration, which is a circuit convenience, is described in Chapter V, Paragraph 4.



a. SINE ± 90° FOR MODEL 16.313



b. SINE ± 90° FOR MODEL 16.314

Figure 4. Patch Block Layout for Sine ±90°

a. Scaling

In the sine ±90° mode, the input voltage X represents an angle θ with a scaling of 9°/v (.111v/ degree); the output voltage Y equals -10 Sine $\frac{\pi X}{20}$ for values of X between ±10 volts. For example, if X = +5.0 volts, representing an angle θ of -45°, the corresponding output voltage is:

$$(-10 \text{ Sine } 180)\ \frac{5}{20}$$
$$= -10 \text{ Sine } 45$$
$$= -7.07\text{V}$$

4. POLAR-TO-RECTANGULAR CONVERSION

The sine-cosine DFG can be used in conjunction with either a quarter-square multiplier or a servo-mechanical multiplier to perform polar-to-rectangular conversion (termed forward resolution).

In polar-to-rectangular conversion the relation between the polar coordinates (R, θ) and the rectangular coordinates (X, Y) is given by the following equations:

$$X = R \text{ Cosine } \theta \quad (1)$$
$$Y = R \text{ Sine } \theta \quad (2)$$

The trigonometric relationship between these sets of coordinates is shown in Figure 5.

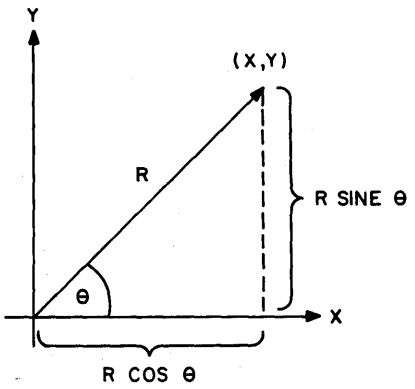


Figure 5. Relationship of Polar-to-Rectangular Coordinates

The sine and cosine functions of polar coordinate θ are multiplied by polar coordinate R to obtain products R sine θ and R cosine θ representing rectangular coordinates Y and X respectively.

The basic circuit for deriving Equations (1) and (2) is shown in Figure 6.

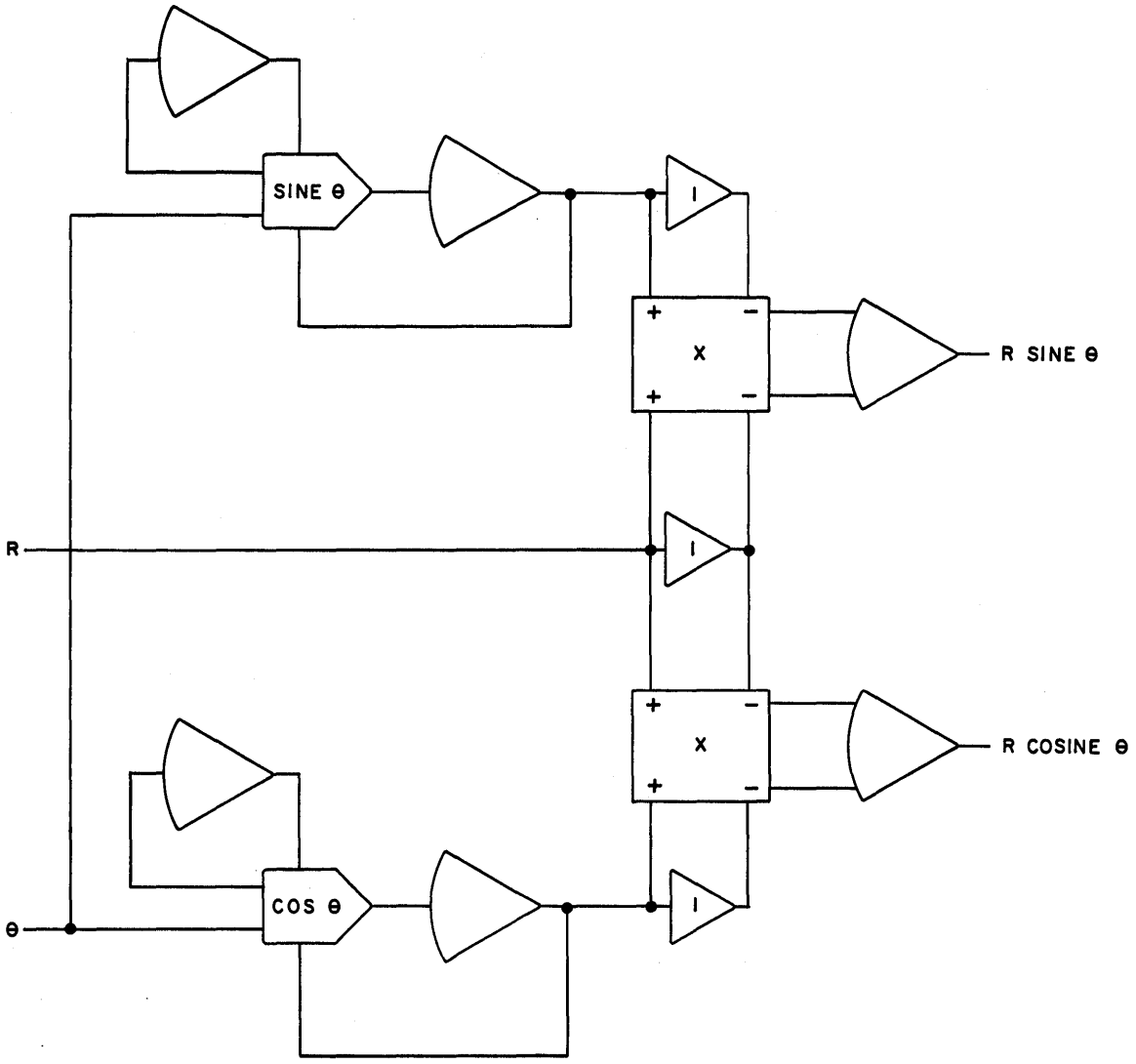
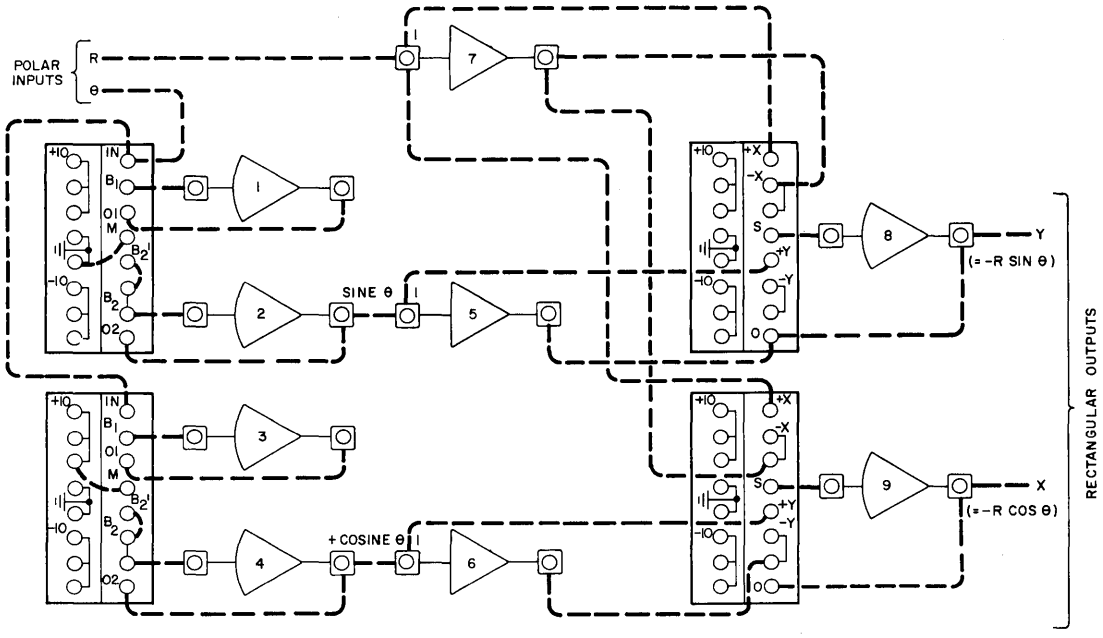
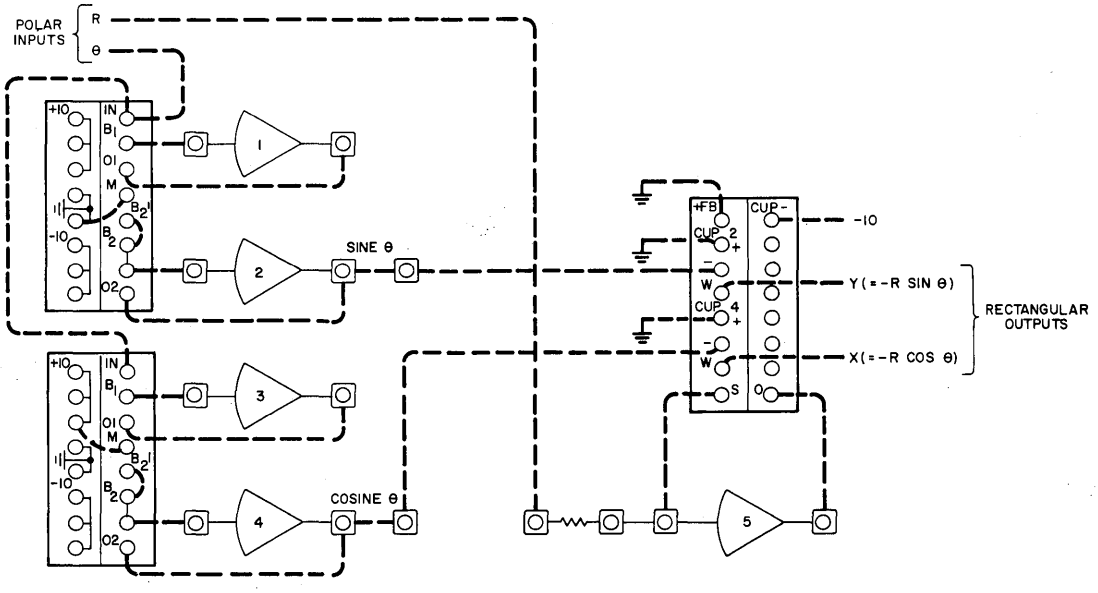


Figure 6. Basic Circuit for Polar-to-Rectangular Equations

Forward resolution using the quarter-square multiplier and servo-mechanical multiplier methods is described with reference to Figures 7 and 8.

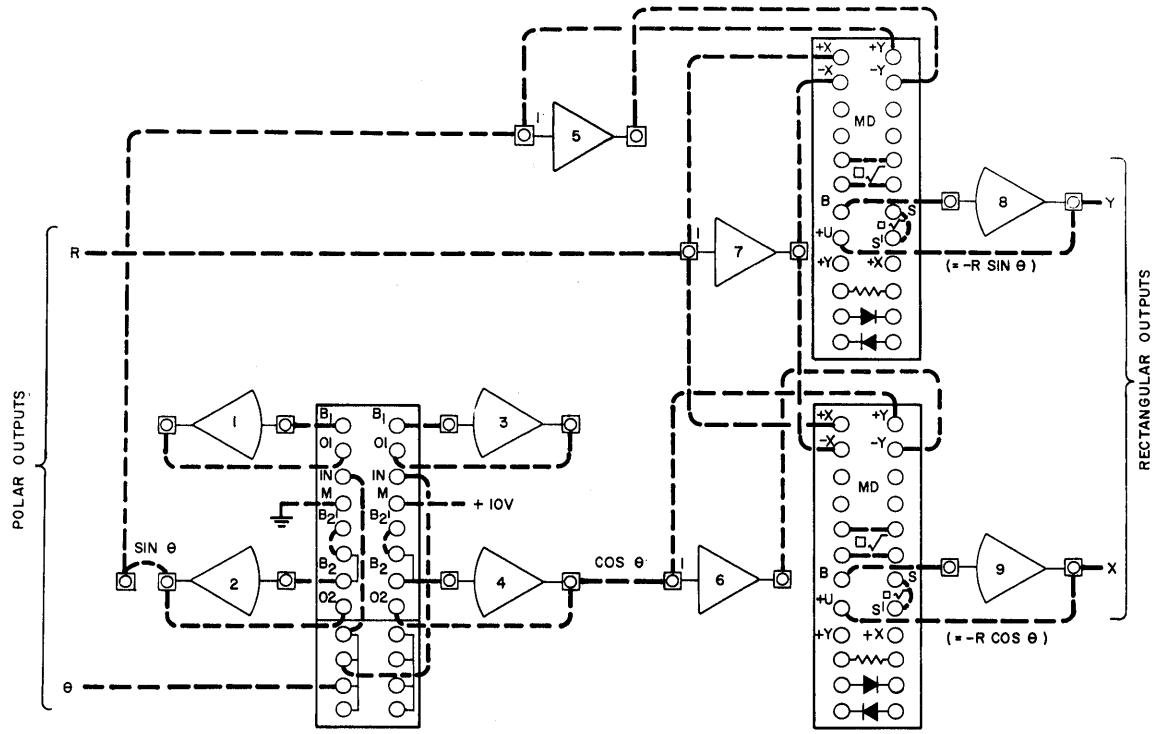


a. USING QUARTER-SQUARE MULTIPLIER

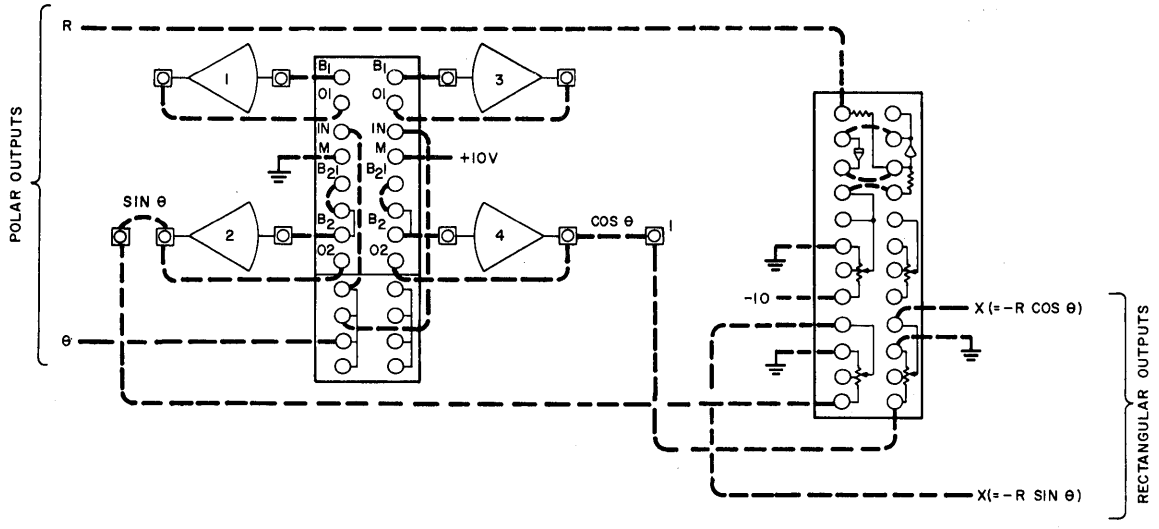


b. USING SERVO-MECHANICAL MULTIPLIER

Figure 7. Patch Block Layout (Forward Resolution) (Model 16.313 Only)



a. USING QUARTER-SQUARE MULTIPLIER



b. USING SERVO-MECHANICAL MULTIPLIER

Figure 8. Patch Block Layout (Forward Resolution) (Model 16.314 Only)

a. Quarter-Square Multiplier Method

Polar coordinate θ is applied concurrently to two sine-cosine DFG's, Figures 7a or 8a, patched in the sine ±180° and +cosine ±180° modes; polar coordinate R is applied concurrently to two quarter-square multipliers. Outputs sine θ from the DFG's are multiplied by R to produce, at the output of the appropriate quarter-square multiplier, -R sine θ (computing amplifier-8) and -R cosine θ (computing amplifier-9) representing rectangular coordinates Y and X respectively.

Sine θ, cosine θ, polar coordinate R and their inverses, provided by unity-gain computing amplifiers 5, 6, and 7 respectively, must be patched as shown to obtain the sign conventions -R sine θ (Y) and -R cosine θ (X).

b. Servo-Mechanical Multiplier Method

When forward resolution is required at frequencies and accuracies that do not exclude the servo-mechanical multiplier method the configuration illustrated in Figures 7b and 8b, can be used.

A comparison of Sections a and b of Figure 7 and 8 indicates that the methods of generating sine θ and cosine θ are identical.

Polar coordinate R is applied to the multiplier computing amplifier. Outputs sine θ and cosine θ, from the DFG's are multiplied by R to produce, at the wiper of the appropriate cup, -R sine θ and -R cosine θ representing rectangular coordinates Y and X respectively.

Both multipliers must be patched for two-quadrant operation as shown. (Note that R must be restricted to positive values only.) Although not shown in Figures 7b or 8b it is important to connect the cup wipers into equal load resistors (preferably 100K ohms) in order to obtain accurate operation.

5. RECTANGULAR-TO-POLAR CONVERSION

Again, the sine-cosine DFG can be used in conjunction with either a quarter-square multiplier, or a servo-mechanical multiplier to perform polar-to-rectangular conversion (termed inverse resolution).

In rectangular-to-polar conversion the relation between the rectangular coordinates (X, Y) and the corresponding polar coordinates (R, θ) is given by the following equations:

$$R = \sqrt{X^2 + Y^2}$$

$$\theta = \tan^{-1} Y/X$$

The non-linear operations of squaring, extraction of square-root, division and production of the inverse tangent in solving these equations would result in a rather complex configuration of computing elements. However, each equation defining polar coordinates R, θ can be rewritten in a simpler form.

Equation $R = \sqrt{X^2 + Y^2}$ becomes:

$$R^2 = X\,(R \text{ Cosine } \theta) + Y\,(R \text{ Sine } \theta)$$

Then, dividing by R:

$$R = X \text{ Cosine } \theta + Y \text{ Sine } \theta \qquad (3)$$

Equation $\theta = \tan^{-1} \frac{Y}{X}$ becomes

$$\tan \theta = \frac{Y}{X}$$

$$\frac{\text{Sine } \theta}{\text{Cosine } \theta} = \frac{Y}{X}$$

Then, cross multiplying by X and Y:

$$X \text{ Sine } \theta = Y \text{ Cosine } \theta, \text{ or} \qquad (4)$$

$$X \text{ Sine } \theta - Y \text{ Cosine } \theta = 0$$

The sine and cosine functions of θ are multiplied by rectangular coordinates X and Y to obtain products X sine θ, X cosine θ, Y sine θ, and Y cosine θ used in deriving Equations (3) and (4). The basic circuit for deriving Equations (3) and (4) is shown in Figure 9.

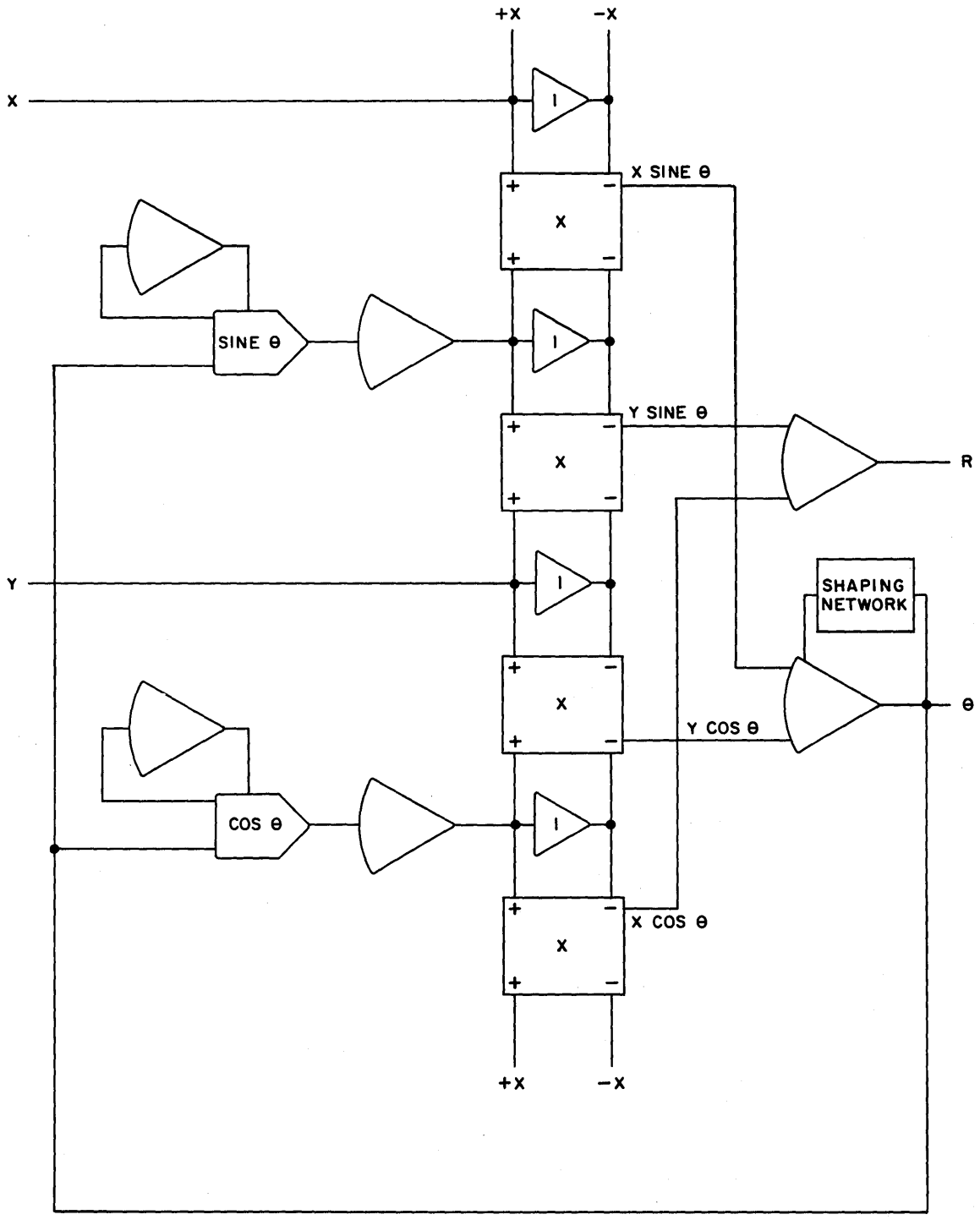


Figure 9. Basic Circuit for Rectangular-to-Polar Equations

Inverse resolution using the quarter-square multiplier and servo-mechanical multiplier methods are described with reference to Figures 10, 11, 12, and 13.

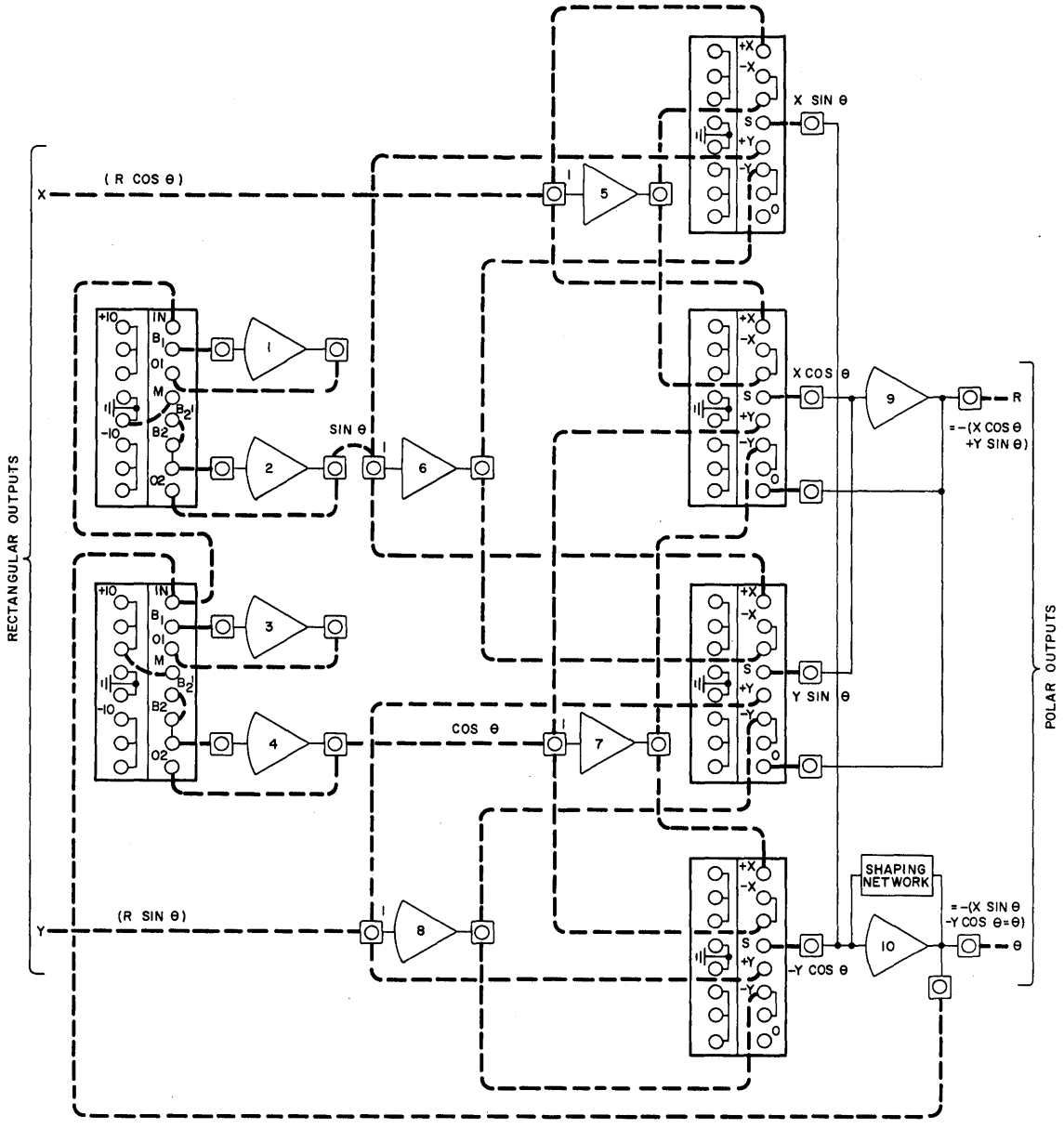


Figure 10. Patch Block Layout (Inverse Resolution) (Model 16.313 Only)

a. Quarter-Square Multiplier Method

A comparison of Figures 8 and 10 indicates a similarity in the method of deriving sine θ and cosine θ. There is however an essential difference in that with forward resolution input θ is available directly in the problem and with inverse resolution it is not.

Rectangular coordinates X and Y are each applied concurrently to two quarter-squre multipliers. Outputs sine θ and cosine θ from the DFG's are multiplied by X and Y to produce, at the output of the appropriate quarter-square multiplier, X sine θ, X cosine θ, Y sine θ and -Y cosine θ.

Outputs X sine θ and -Y cosine θ are summed by computing amplifier-10; the amplifier output, which represents polar coordinate θ, is also fed back to both DFG's. The correct value for θ is obtained implicitly by utilizing the high gain of amplifier-10, together with its shaping network, which provides an output voltage (corresponding to θ) to satisfy the equation X sine θ - Y cosine θ = 0) (or X sine θ = Y cosine θ).

Once the feedback loop is established polar coordinate R is produced, at the output of computing amplifier-9, by summing X cosine θ and Y sine θ.

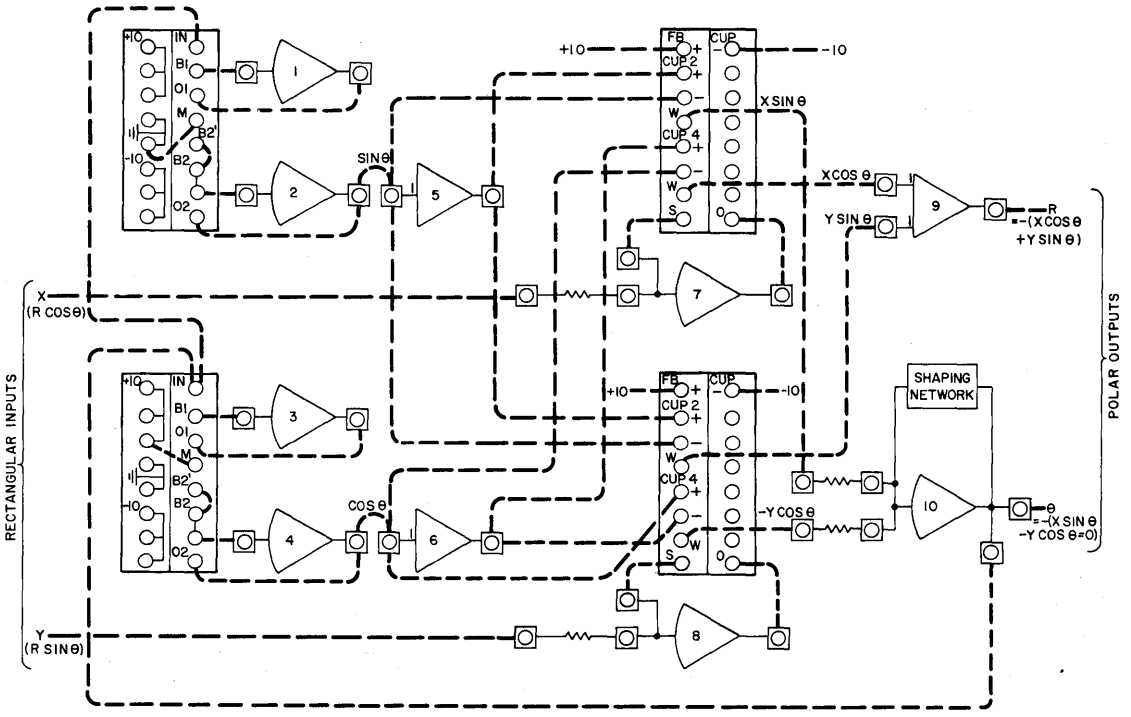


Figure 11. Patch Block Layout (Inverse Resolution) (Model 16.313 Only)

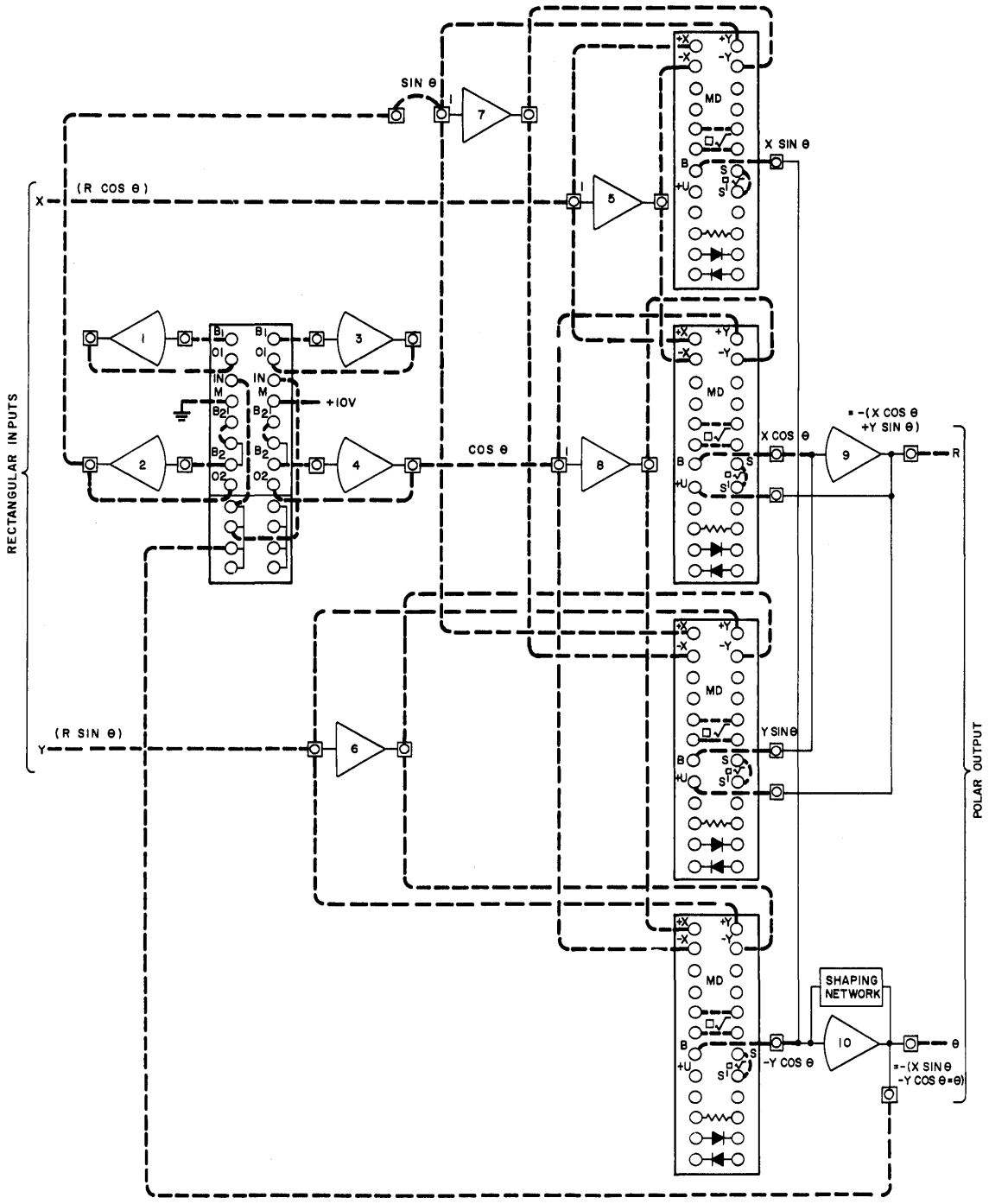


Figure 12. Patch Block Layout (Inverse Resolution) (Model 16.314 Only)

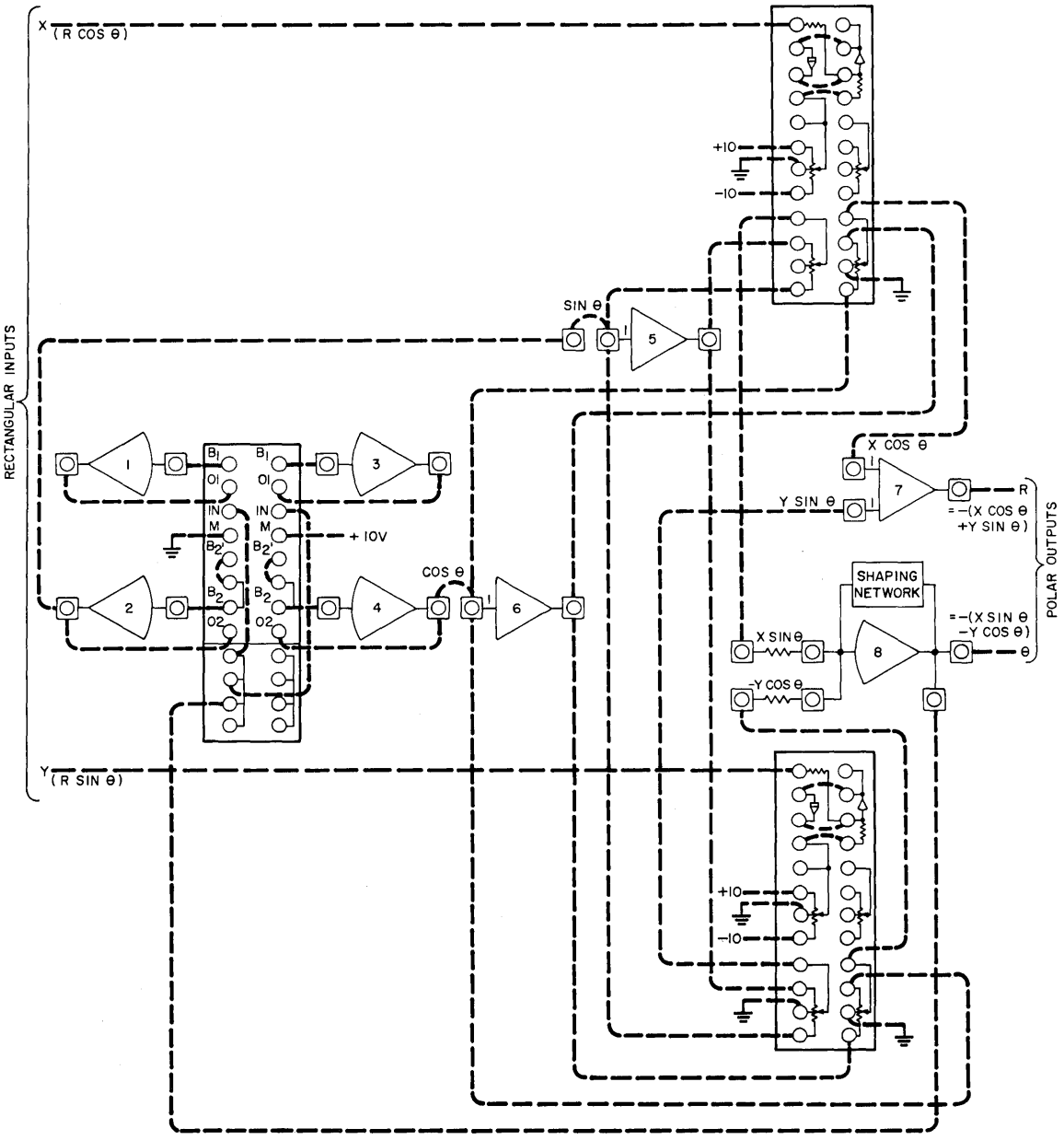


Figure 13. Patch Block Layout (Inverse Resolution) (Model 16.314 Only)

b. Servo-Mechanical Multiplier Method

When frequency considerations permit, the configurations illustrated in Figures 11 and 13 can be used.

The method of generating sine θ and cosine θ is identical to the method previously described in Chapter III, Paragraph 5*a*.

Rectangular coordinates X and Y are each applied to a servo-mechanical multiplier. Outputs sine θ and cosine θ from the DFG's are multiplied by X and Y to produce, at the wiper of the appropriate cup, X sine θ, X cosine θ, Y sine θ and -Y cosine θ.

The method of deriving polar coordinates (R, θ) is otherwise identical to quarter-square method. All four multipliers must be patched for four-quadrant operation as shown.

It should be observed that in Figures 10 and 12 input resistors are not required for computing amplifiers-9 and 10 since they are driven from a current source. Input resistors are, however, required for the corresponding amplifiers illustrated in Figures 11 and 13 since they are driven from voltage sources. Feedback paths are provided from the output of amplifier-9 to the appropriate quarter-square multiplier to obtain the correct scaling for R.

CHAPTER IV

CIRCUIT DESCRIPTION

1. GENERAL

The sine-cosine generator is described in this section in several stages. A simplified description, with reference to Figure 14 is followed by a more detailed description with reference to Figures 14 to 18.

2. SIMPLIFIED DESCRIPTION

The sine-cosine generator shown in Figure 14 consists of two amplifier circuits; each circuit performs an unique function.

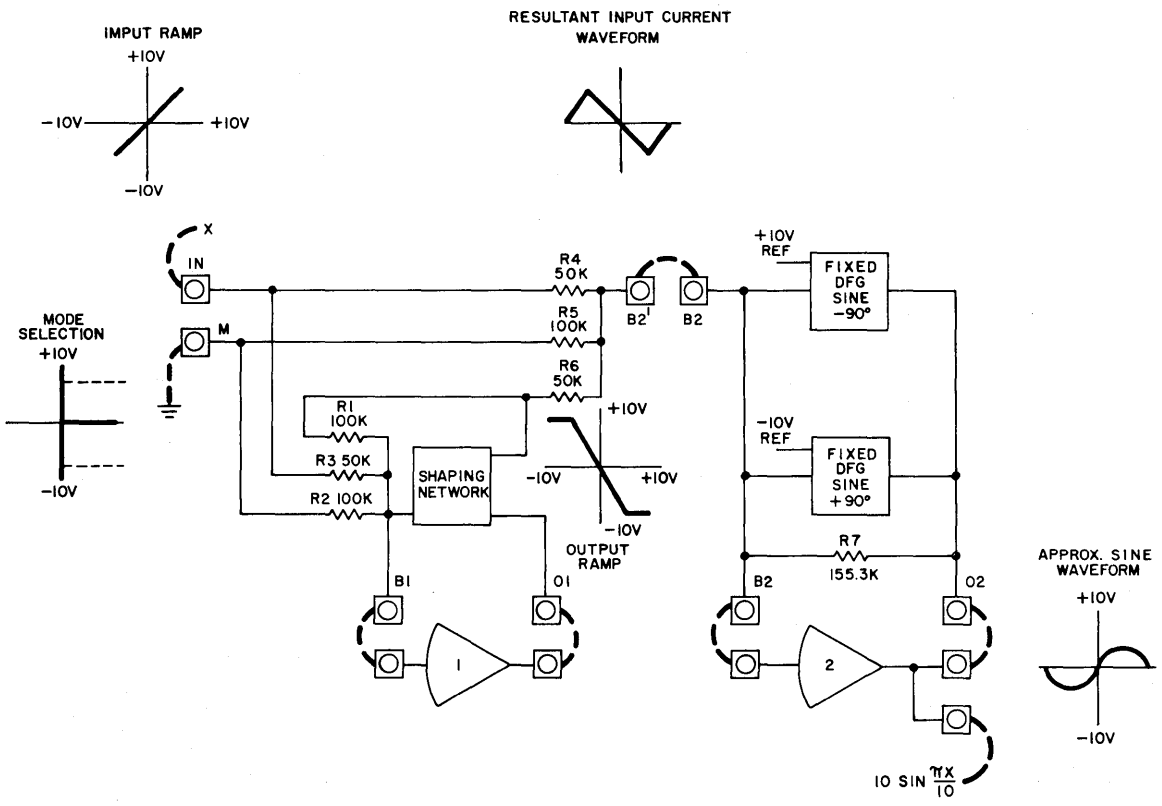


Figure 14. Simplified Schematic

Amplifier-1, together with its summing resistor network R1 to R3 and the shaping network, forms a computing amplifier circuit in which the change in output voltage is equal to twice the magnitude of the input voltage but of opposite sign.

The mode control voltage, applied through M to the input resistor R2, is at HQ GRD selecting the sine ±180° mode as shown.

From the output of amplifier-1 the feedback path is completed through the shaping network (containing a diode bridge and limiting circuits) to R1.

An input ramp waveform increasing with time from -10 volts through 0 volt to +10 volts is applied, as θ, through IN to input resistor R3. The consequent output ramp waveform, from the shaping network, limits at +10 volts as the input ramp decreases from -10 volts to -5 volts, then decreases from +10 volts to -10 volts, at twice the slope of the input ramp, and finally limits at -10 volts as the input ramp increases from +5 volts to +10 volts.

Amplifier-2, together with its summing resistor network R4 to R6 and fixed DFG sine -90° and fixed DFG sine +90°, forms the second computing amplifier circuit. The fixed DFG sine -90° and fixed DFG sine +90° (containing resistor networks with biased diodes) are in parallel with feedback resistor R7.

The input ramp and shaping network output ramp waveforms are applied to input resistors R4 and R6 respectively, while the mode control voltage is applied to input resistor R5. The slope of the resultant input current waveform appearing at the summing junction (B2), is twice that of the input ramp waveform.

As the resultant input current to B2 increases from zero in a positive direction the output from amplifier-2 overcomes the predetermined reverse biases applied to the six resistor-diodes networks in the fixed DFG sine -90°; as each diode conducts (termed breakpoint occurrence) in turn, precision resistors are switched-in in parallel with R7, decreasing the output slope from amplifier-2 until, at -10 volt output, it is approximately zero.

Conversely, as the resultant input current decreases to zero, the reverse biases are re-applied to the six diodes in turn, producing a consequent increase in slope until, finally, R7 only is in the feedback path.

Similarly, the six diodes in the fixed DFG sine +90° conduct in turn and then cut off in turn as the resultant input current increases from zero in a negative direction and then decreases again to zero.

In this manner the output function 10 sin $\pi X/10$ is approximated, from 0 to ±180° in a series of straight-line segments as the resistor-diode networks in the fixed DFG's are switched in and out of the circuit.

3. DETAILED DESCRIPTION

The detailed description augments the generalized circuit concepts previously described under Simplified Description, Paragraph 2 of this chapter and introduces various supplementary circuit features (see Schematic C36,132XS). Circuit operation in each of the three modes is described with reference to the waveforms illustrated in Figures 16, 17, and 18.

The areas enclosed within dashed lines on Schematic C36,132XS illustrate the resistor-diode networks which are within the corresponding blocks shown in Figure 14. The operation of the shaping network and fixed DFG sine -90° is also described.

a. Shaping Network

The shaping network bridge circuit is formed from diodes CR3, CR5, CR6, and CR8; the bridge input (junction CR3 and CR6) is fed directly from the output of amplifier-1 while its output (junction CR5 and CR8) is applied concurrently to R2 and R48 on the appropriate summing resistor networks.

The output from the bridge which follows the output from amplifier-1 (within the range ±10 volts), is limited at +10 volts or -10 volts when either diode (CR7 or CR4 respectively) conducts; adjustment of the +10 volts or -10 volts limiting value is controlled by VR1 or VR2 respectively. When either diode conducts the feedback path from the output of amplifier-1 to R2 is broken; the output from amplifier-1 then rises toward +15 volts or -15 volts until clamped at +12 volts or -12 volts when either diode (CR1 or CR2 respectively) conducts.

Operation of the shaping network is best considered under three different conditions.

Assume first that the following initial circuit conditions exist.

(1) The DFG is operating in the sine ±180° mode with M patched to HQ GRD.

(2) The input ramp applied to IN is at zero volt.

(3) The output from amplifier-1 is approximately zero.

(4) The output from the bridge is at zero volts.

If, then the input ramp increases from zero toward -10 volts the circuit conditions are modified as follows:

(1) As the input ramp increases from zero to -5 volts, the output from amplifier-1 increases positively, driving the bridge output from zero to +10 volts at twice the slope of the input ramp.

(2) When the input ramp reaches -5 volts the outputs from both the amplifier and bridge will be +10 volts and with, say, a 0.6 volt drop across CR6 the junction of CR6 and CR8 is at +10.6 volts, forward biasing CR7. Diode CR7 conducts and clamps the junction of CR6 and CR8 at +10.6 volts; the junction CR5 and CR8 (the bridge output) will be limited at +10 volts. Since the shaping network output is limited at +10 volts, breaking the feedback path, the output from amplifier-1 will rise sharply toward +15 volts, reverse biasing CR6 (its anode is clamped at +10.6 volts). As the summing junction (B1) is maintained at virtual ground, the output from amplifier-1 will, however, only rise until the junction of R4 and R49 rises to approximately +0.6 volts, forward biasing CR1; when CR1 conducts, the output from amplifier-1 is clamped at approximately +12 volts.

(3) During the excursion of the input ramp between -5 volts and -10 volts the output from amplifier-1 remains at approximately +12 volts; the shaping network output remains firmly at +10 volts.

Conversely, if the input ramp increases from zero toward +10 volts the circuit conditions are modified as follows:

(a) Between zero and +5 volts the output from amplifier-1 increases negatively driving the bridge output from zero to -10 volts at twice the slope of the input ramp; then at +5 volts.

(b) The bridge output is limited at -10 volts when diode CR4 conducts; diodes CR3 cuts off and the output from amplifier-1 rises sharply toward -15 volts until clamped at -12 volts when diode CR2 conducts.

b. Fixed DFG Sine -90°

Basically, the technique of function approximation employed in the DFG is to generate a sequence of straight-line segments which approximate the curve of the sine function to the required tolerance. The accuracy of the approximation is dependent upon the number of straight-

line segments used; in this instance 7 segments, including the initial slope, are used. Each of the straight-line segments, the breakpoints of which are adjustable but having fixed slope, are fitted together by the DFG to form an approximation to the desired function.

Curve fitting is accomplished by straight-line segments between selected points which lie above the curve; the points at which these changes of slope occur, to approximate the start of the next straight-line segment, are termed breakpoints. The maximum error between the actual curve and each linear approximation is minimized by arranging the breakpoints to be closely spaced where the function is changing slope rapidly and widely spaced where the slope is nearly constant.

In the DFG the slope of each straight-line segment is less than the slope of the theoretical sine curve; the error is controlled by arranging each breakpoint to occur 16 mv above the corresponding point on the theoretical sine curve. The straight-line segment between two consecutive breakpoints, (which lie above the theoretical sine curve) intersects the curve twice. This is shown in somewhat exaggerated form, in Figure 15. The approximation of each segment to the curve is further aided by the curvature of the diode characteristics. The fixed DFG sine -90° is formed from six similarly biased resistor-diode networks. Diodes CR10 to CR14 conduct in turn, switching their corresponding precision resistor into the feedback loop, as the output (02) voltage overcomes the bias (or breakpoint) voltage applied to each diode. The bias voltage applied to each diode is adjustable over a small range by its corresponding set-up potentiometer (VR3 to VR8), to ensure that its breakpoint occurs correctly 16 mv above the associated point on the theoretical sine curve.

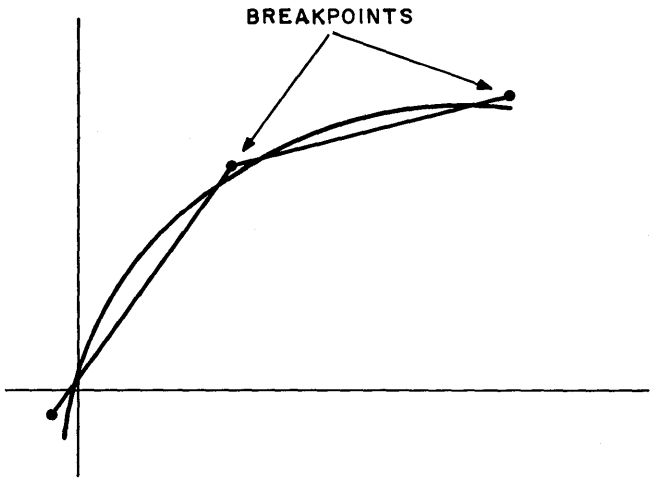


Figure 15. Plotting Between Breakpoints

Some practical limitations exist however in clearly establishing the exact point at which each diode will conduct. To simplify the setting-up procedure and ensure that each diode breakpoint occurs at the correct value, an input voltage is selected mid-way between the desired breakpoint voltage of the selected diode and the desired breakpoint voltage of the next diode in the sequence. The potentiometer associated with the selected diode is then adjusted until the required output from amplifier-2 is obtained. (This technique is described further under Fixed DFG Sine ±90° Adjustments, Chapter V, Paragraph 4.)

In the following description it is assumed that the DFG breakpoints are set up to occur at the values stated in the Table 6 in Chapter V, Paragraph 4. To assist in the description however, the breakpoint voltage of each diode, and the corresponding approximated sine function, at the output of amplifier-2, are shown in Table 2 below.

TABLE 2. Fixed DFG Sine -90° Input and Output Voltages

Input		Diode	Output Voltage (02) Amplifier-2 (10 Sine $\frac{\pi X}{20}$)
Voltage	Degrees (θ = 9°/V)		
+1.9V	17°6'	CR9	-2.94V
+3.6V	32°24'	CR10	-5.36V
+5.1V	45°54'	CR11	-7.18V
+6.4V	57°36'	CR12	-8.44V
+7.9V	71°6'	CR13	-9.46V
+9.2V	82°48'	CR14	-9.92V

A graphical representation of input voltage versus output voltage, for the fixed DFG sine -90°, is illustrated in Figure 22. The points marked "breakpoint occurrence" indicate the output voltages (02) at which diodes CR9 to CR14 conduct; points denoted "potentiometer set-up point" indicate the corresponding input voltages at which potentiometers VR3 to VR8 are adjusted to ensure correct breakpoint occurrence, of diodes CR9 to CR14 respectively.

The breakpoint at which each diode conducts is shown to occur at particular value of input voltage, a convenience previously assumed in the simplified description. Since, however, the summing junction (B2) is maintained at virtual ground it is the corresponding change in output from amplifier-2 which causes the appropriate diode to conduct.

As an example of DFG operation consider that the following initial circuit conditions exist.

(1) The input voltage to amplifier-2 is at zero.

(2) The output voltage from amplifier-2 (02) is also at zero.

If then the input increases from zero towards +10 volts the circuit conditions are modified as follows:

(1) As the input voltage increases from zero to approximately +1.9 volts the output from amplifier-2 increases from zero toward -10 volts at an initial slope determined solely by the value of R9.

(2) When the input voltage reaches +1.9 volts the corresponding output from amplifier-2 (-2.94 volts) overcomes the bias applied to diode CR9. When diode CR9 conducts, switching precision resistors R10 and R11 in parallel with R9, the output slope from amplifier-2 will, in consequence alter; the output will continue at this slope until the input voltage reaches approximately +3.6 volts (-5.36 volts corresponding output voltage) when diode CR10 conducts.

(3) Diodes CR11 to CR14 will conduct in turn as the output voltage reaches the values listed in Table 1.

It should be noted that the resistor-diode networks are all similar with the exception of the first (least positive) and the sixth (most positive) breakpoint diode circuits CR9 and CR14 respectively.

In the first breakpoint circuit resistors R12 and R51 act as a voltage divider in the feedback loop. The breakpoint of diode CR9 switches in this divider together with precision resistors R10 and R11.

The sixth breakpoint occurs when the input reaches +9.2 volts, switching in resistor R23, a very low feedback resistor (1.5K). If only R23 was in the feedback circuit R24 and VR8 would be lower in value imposing a heavy current drain on the +10 volt reference supply. However, with a constant voltage drop of 6.8 volts across Zener diode CR15 a further voltage drop of only 2.6 volts is required across R23 to overcome the bias applied to CR14. In this instance with the output from amplifier-2 at -9.9 volts, and with voltage drops of 6.8 volts and 2.6 volts across CR15 and R23 respectively, the junction of R22 and R23 will be approximately -0.5 volts causing diode CR14 to conduct.

c. Sine ±180°

The sine mode is obtained by patching M to 0 volt. The shaping network, in conjunction with amplifier-1, permits the range of the sine generator (used in conjunction with amplifier-2) to be increased from ±90° to ±180°. Figure 16 illustrates the resultant waveforms from the shaping network and sine generator (output from amplifier-2) when placed in the sine mode.

Assume a gradient voltage from -10 volts to +10 volts is applied to input IN (waveform a); this ramp covers the full range of the sine mode from -180° to +180°.

The ramp input is applied to the summing resistor network associated with amplifier-1; the output from amplifier-1 (waveform b), shown to be limited at approximately +12 volts (input ramp -10 volts to -5 volts) and -12 volts (input ramp range +5 volts to +10 volts), decreases at twice the slope of the input ramp from +10 volts to -10 volts (input ramp range -5 volts to +5 volts).

The output from the shaping network (the dashed form of waveform b), which is driven by the output from amplifier-1, is limited at +10 volts and -10 volts when the input ramp is within the ranges -10 volts to -5 volts and +5 volts to +10 volts respectively.

Waveforms a and b, which are applied to the "gain-of-two" inputs on the summing network associated with amplifier-2, generate the resultant input current waveform c (or 2a + 2b). Waveform c is shown to increase at twice the slope of the input ramp (between the ranges -10 volts to -5 volts and +5 volts to +10 volts) and decrease at the same slope as the output ramp (between the range -5 volts to +5 volts of the input ramp).

Waveform d illustrates the output of amplifier-2; it represents the sine function 10 Sine $\pi X/10$ with a range -180° to +180°.

d. + Cosine ±180°

The positive cosine mode is obtained by patching M to the +10 volt reference supply. Figure 17 illustrates the resultant waveforms from the shaping network and sine generator when placed in the positive cosine mode.

The +10 volts at M, applied to a unity gain input on the summing network associated with amplifier-1, when summed with the input ramp produces a consequent offset of -12 volts at the output of amplifier-1 (or -10 volts at the shaping network output) shifting waveform b 90° to the left (compare Figures 16 and 17).

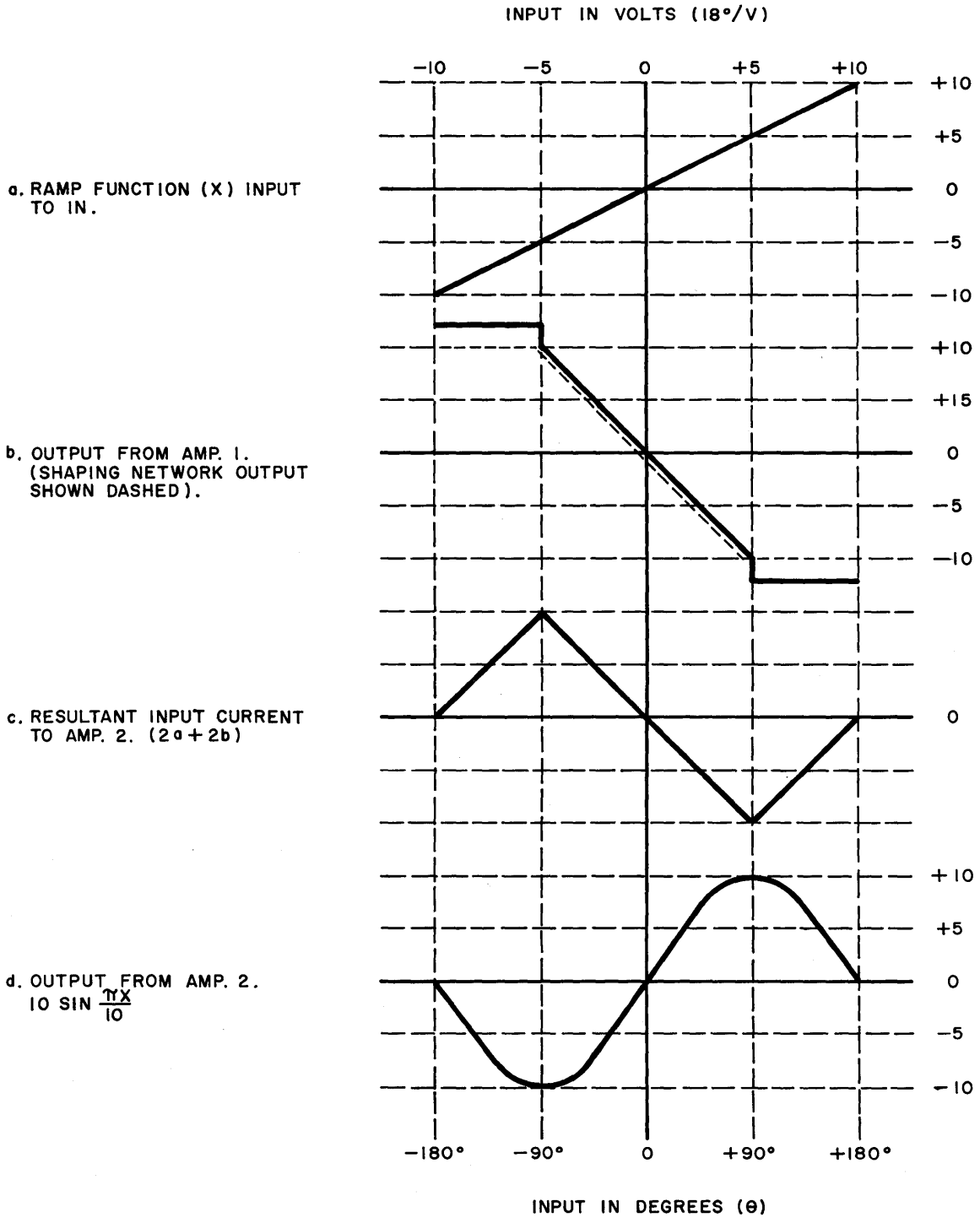


Figure 16. Sine Mode Waveforms

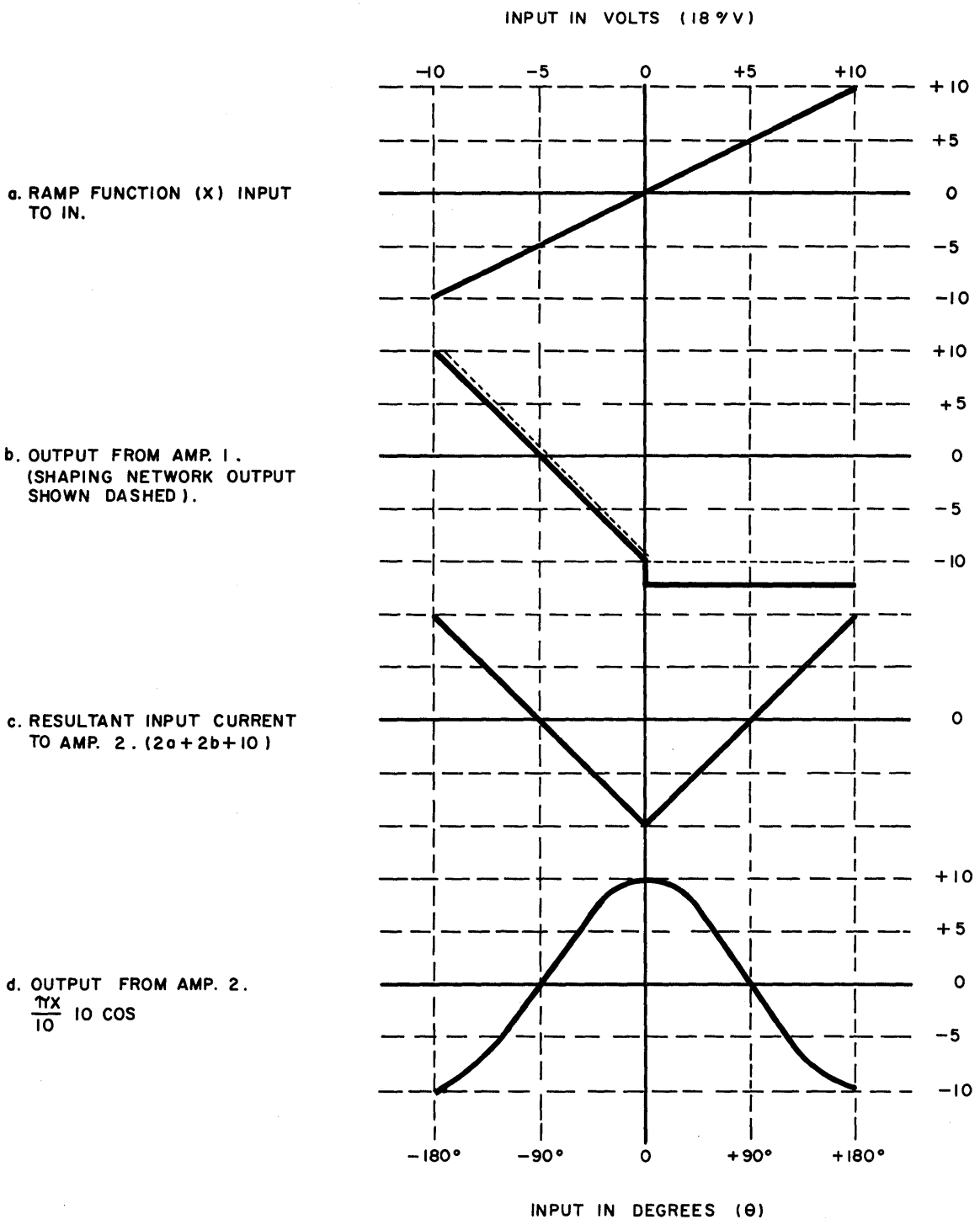


Figure 17. +Cosine Mode Waveforms

The +10 volts at M, applied to a unity gain input on the summing network associated with amplifier-2, when summed with waveforms a and b (2a + 2b + 10) generates the resultant input current waveform (c) applied to the summing junction (B2) of amplifier-2.

Waveform d illustrates the output of amplifier-2; it represents the positive cosine function 10 Cosine $\pi X/10$ with a range -180° to +180°.

e. - Cosine ±180°

The negative cosine mode is obtained by patching M to the -10 volt reference supply. Figure 18 illustrates the resultant waveforms from the shaping network and sine generator when placed in the negative cosine mode.

Similarly to the positive cosine mode the -10 volts applied to M produces an offset of +12 volts at the output of amplifier-1 shifting waveform b 90° to the right (compare Figures 16 and 18); the resultant input current waveform c (2a + 2b - 10) is applied to summing junction (B2) of amplifier-2.

Waveform d illustrates the output of amplifier-2; it represents the negative cosine function -10 Cosine $\pi X/10$ with range -180° to +180°.

f. Temperature Compensation

The forward voltage drop across the breakpoint diodes decreases with increasing ambient temperature resulting in a lower forward bias, hence a lower breakpoint voltage.

Thermistors have been employed in the biasing circuits to compensate for changes in ambient temperature. If, for example, an increase in ambient temperature is detected by RT1 the decreased voltage drop across RT1 will result in increased breakpoint voltages for diodes CR9 to CR11. Similarly, RT2 compensates for diodes CR12 and CR13; Zener diode CR15 compensates for CR14.

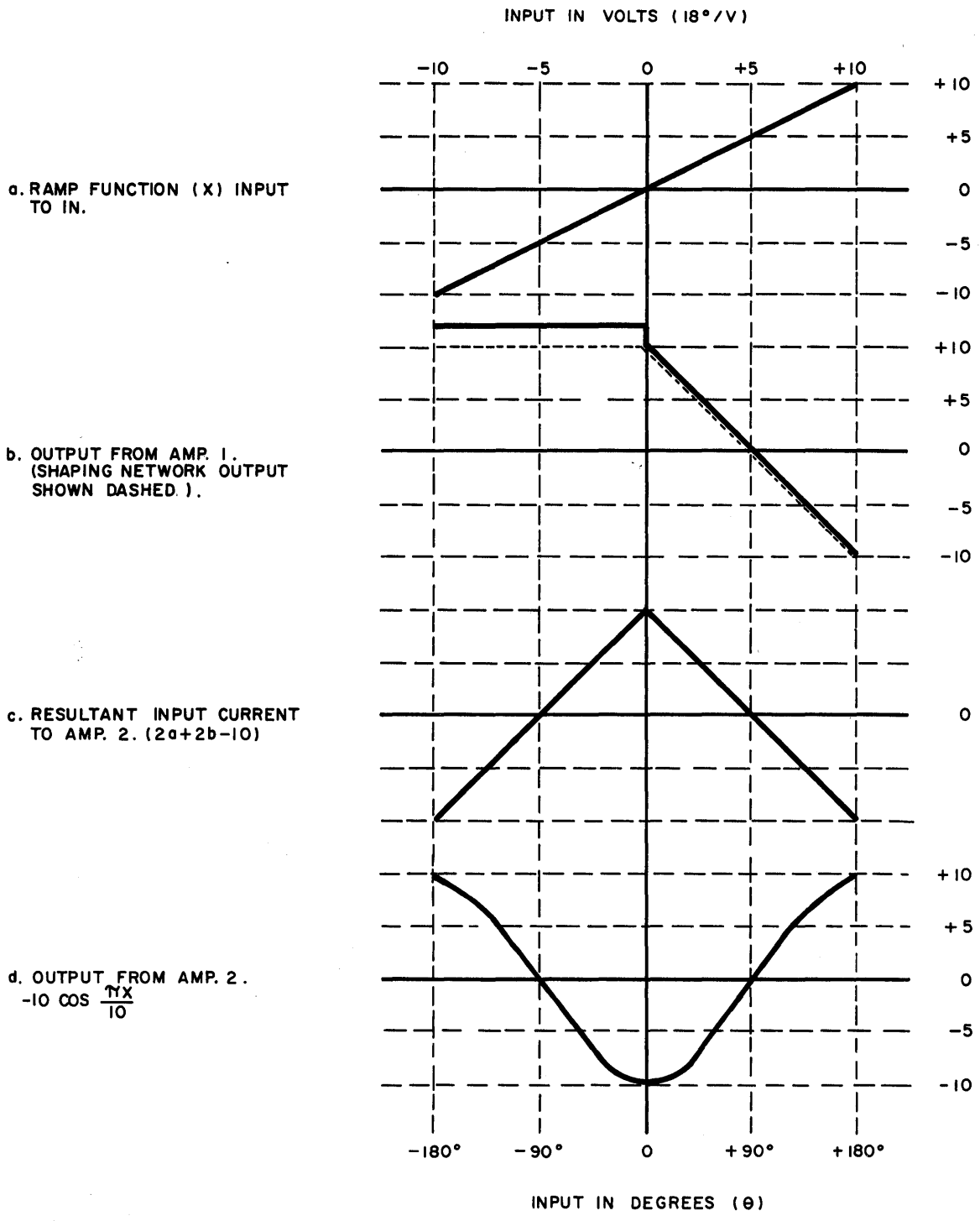


Figure 18. -Cosine Mode Waveforms

CHAPTER V

MAINTENANCE

1. GENERAL

The maintenance procedures described in this section consist of a number of tests and adjustments which can be performed on the DFG to ensure correct operation and anticipate impeding failure. The tests are:

1. Operational Checks
2. Shaping Network Adjustments
3. Fixed DFG Sine ±90° Adjustment

If any adjustments are necessary as a result of these tests the DFG should be mounted on the service shelf accompanying the computer.

2. OPERATIONAL CHECKS

The sine ±180° mode and ± cosine ±180° mode should each be checked by:

1. Applying a series of known inputs to IN (sine -180°).
2. Measuring the corresponding actual output voltage with a null potentiometer and microammeter, or an electronic digital voltmeter.

If the maximum difference (or error) between the actual output voltage and the theoretical output voltage exceeds ±25 mv (at ambient temperature) the adjustments of the shaping network and/or fixed DFG sine ±90° should be checked.

a. Sine ±180°

To check the sine ±180° mode proceed as follows:

1. Patch the sine-cosine DFG in the sine mode as shown in Figure 3 with M = 0 volt.
2. Apply in turn the voltages listed in Tables 3 and 4 first as positive inputs to IN (sine +180°), then as negative inputs to IN (sine -180°).
3. Check the actual output voltage corresponding to each of these input voltages against the theoretical output voltages listed. They should be within ±25 mv.

TABLE 3. Sine Mode Check Voltages
$\theta = 0°$ to $90°$

Input		Theoretical Output Volts
Volts (X)	Degrees (θ)	10 Sine $\frac{\pi X}{10}$
0	0	0
0.4	7.2	1.25
0.8	14.4	2.49
1.0	18.0	3.09
1.2	21.6	3.68
1.6	28.8	4.82
1.8	32.4	5.36
2.0	36.0	5.88
2.4	43.2	6.85
2.5	45.0	7.07
2.7	48.6	7.50
3.0	54.0	8.09
3.2	57.6	8.44
3.4	61.2	8.76
3.8	68.4	9.30
4.0	72.0	9.51
4.2	75.6	9.69
4.4	79.2	9.82
4.6	82.8	9.92
4.8	86.4	9.98
5.0	90.0	10.00

TABLE 4. Sine Mode Check Voltages
$\theta = 90°$ to $180°$

Input		Theoretical Output Volts
Volts (X)	Degrees (θ)	10 Sine $\frac{\pi X}{10}$
5.0	90	10.0
5.2	93.6	9.98
5.4	97.2	9.92
5.6	100.8	9.82
5.8	104.4	9.69
6.0	108.0	9.51
6.2	111.6	9.30
6.6	118.8	8.76
6.8	122.4	8.44
7.2	129.6	7.71
7.4	133.2	7.29
7.6	136.8	6.85
8.0	144.0	5.88
8.2	147.6	5.36
8.8	158.4	3.68
8.9	160.2	3.39
9.0	162.0	3.09
9.4	169.2	1.87
10.0	180.0	0.00

Note: Maximum allowable error is less then ±25 mv in all cases.

b. + Cosine ±180°

To check the + cosine ±180° mode proceed as follows:

(1) Patch the sine-cosine DFG in the + cosine mode as shown in Figure 3 with M = +10 volts.

(2) Apply in turn the voltages listed in Tables 5 and 6 first as positive inputs to IN (+ cosine +180°) then as negative inputs to IN (+ cosine -180°).

(3) Check the actual output voltages corresponding to each of these input voltages against the theoretical output voltages listed. They should be within ±25 mv.

TABLE 5. + Cosine Mode Check Voltages
$\theta = 0°$ to 90°

Input		Theoretical Output Volts
Volts (X)	Degrees (θ)	+10 Sine $\frac{\pi X}{10}$
0	0	10.0
0.2	3.6	9.98
0.4	7.2	9.92
0.6	10.8	9.82
0.8	14.4	9.69
1.0	18.0	9.51
1.2	21.6	9.30
1.6	28.8	8.76
2.0	36.0	8.09
2.4	43.2	7.29
2.6	46.8	6.85
3.0	54.0	5.88
3.2	57.6	5.36
3.4	61.2	4.82
3.8	68.4	3.68
4.0	72.0	3.09
4.2	75.6	2.49
4.6	82.8	1.25
5.0	90.0	0.00

TABLE 6. + Cosine Mode Check Voltages
$\theta = 90°$ to 180°

Input		Theoretical Output Volts
Volts (X)	Degrees (θ)	+10 Cos $\frac{\pi X}{10}$
5.0	90.0	0.00
5.4	97.2	1.25
5.8	104.4	2.49
6.0	108.0	3.09
6.2	111.6	3.68
6.6	118.8	4.82
6.8	122.4	5.36
7.0	126.0	5.88
7.4	133.2	6.85
7.6	136.8	7.29
8.0	144.0	8.09
8.2	147.6	8.44
8.4	151.2	8.76
8.8	158.4	9.30
9.0	162.0	9.51
9.2	165.6	9.69
9.4	169.2	9.82
9.6	172.8	9.92
10.0	180.0	10.00

Note: Maximum allowable error is less than ±25 mv in all cases.

c. - Cosine ±180°

To check the - cosine ±180° mode proceed as follows:

(1) Patch the sine-cosine DFG in the - cosine mode as shown in Figure 3 with M = -10 volts.

(2) Apply in turn the voltages listed in Tables 5 and 6 first as positive inputs to IN (- cosine +180°) then as negative inputs IN (- cosine -180°).

(3) Check the actual output voltage corresponding to each of these input voltages against the theoretical output voltage listed. They should be within ±25 mv.

3. SHAPING NETWORK ADJUSTMENTS

For the locations of the various potentiometers used in setting up the shaping network and sine generators see Figure 19. Before performing any shaping network or sine generator adjustments it is important that the reference supplies are accurately balanced.

To adjust the balance of the +10 volt and -10 volt reference supplies see either the TR-20 or the TR-48 Maintenance handbooks.

To adjust the shaping network limiting circuits of either the Model 16.313 or 16.314, Sine-Cosine DFG's, patch the units as shown in Figures 20 and 21 respectively. Omit the link from the output of the integrator to IN, and proceed as follows:

(1) Patch the -10 volt reference directly to IN.

(2) Set switch S1 to the TEST position.

(3) Adjust VR1 (see Figure 19) until a reading of 0.000 volt is obtained on the meter.

(4) Replace the -10 volt reference supply applied to IN with the +10 volt reference supply and adjust VR2 until a reading of 0.000 volt is obtained on the meter.

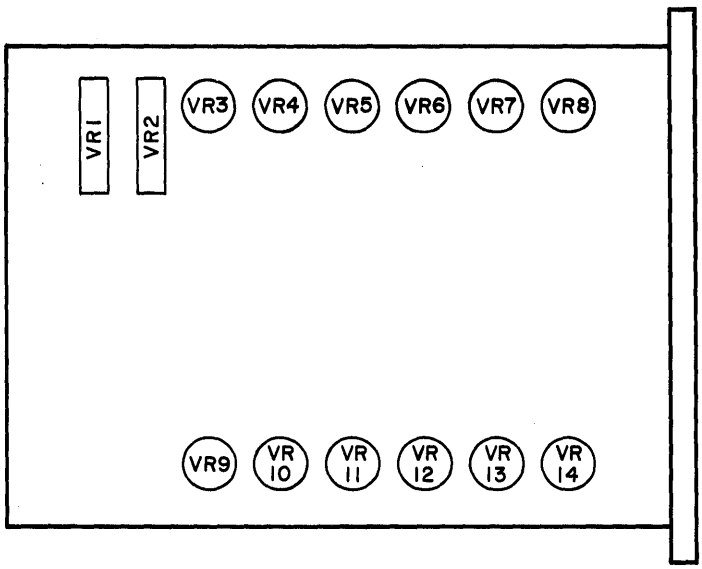
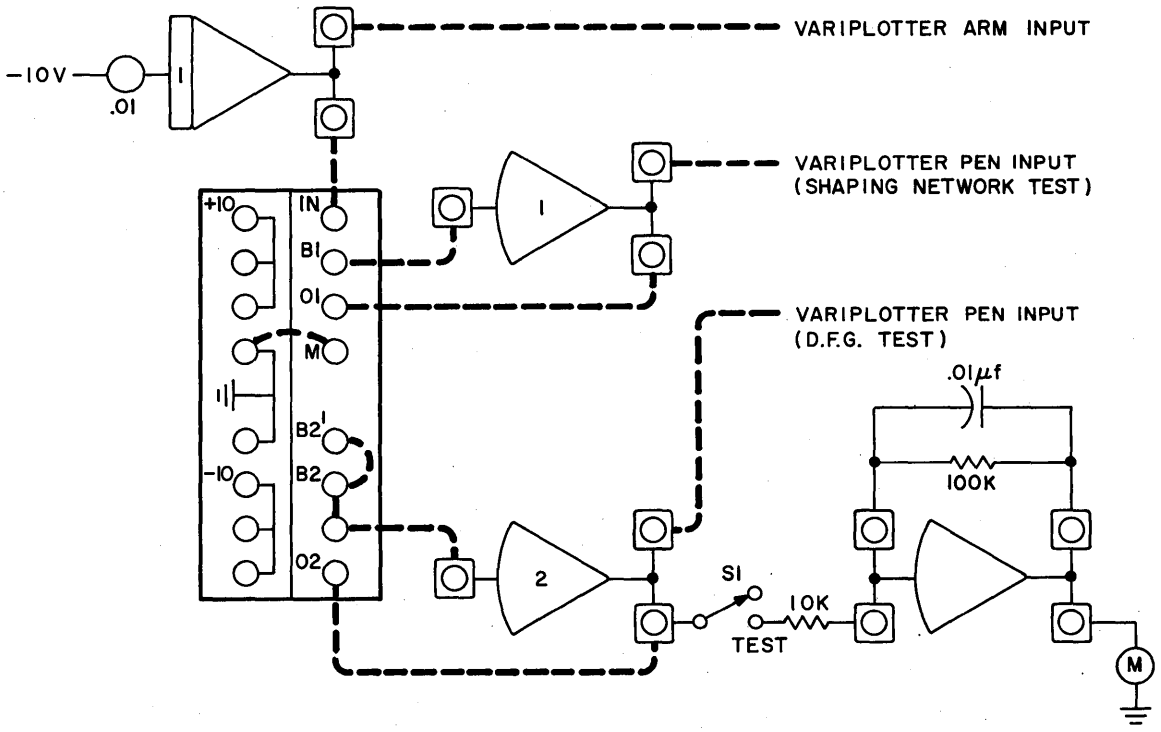
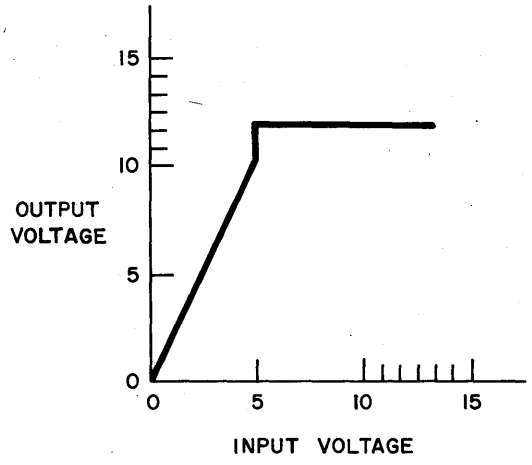


Figure 19. Potentiometer Location

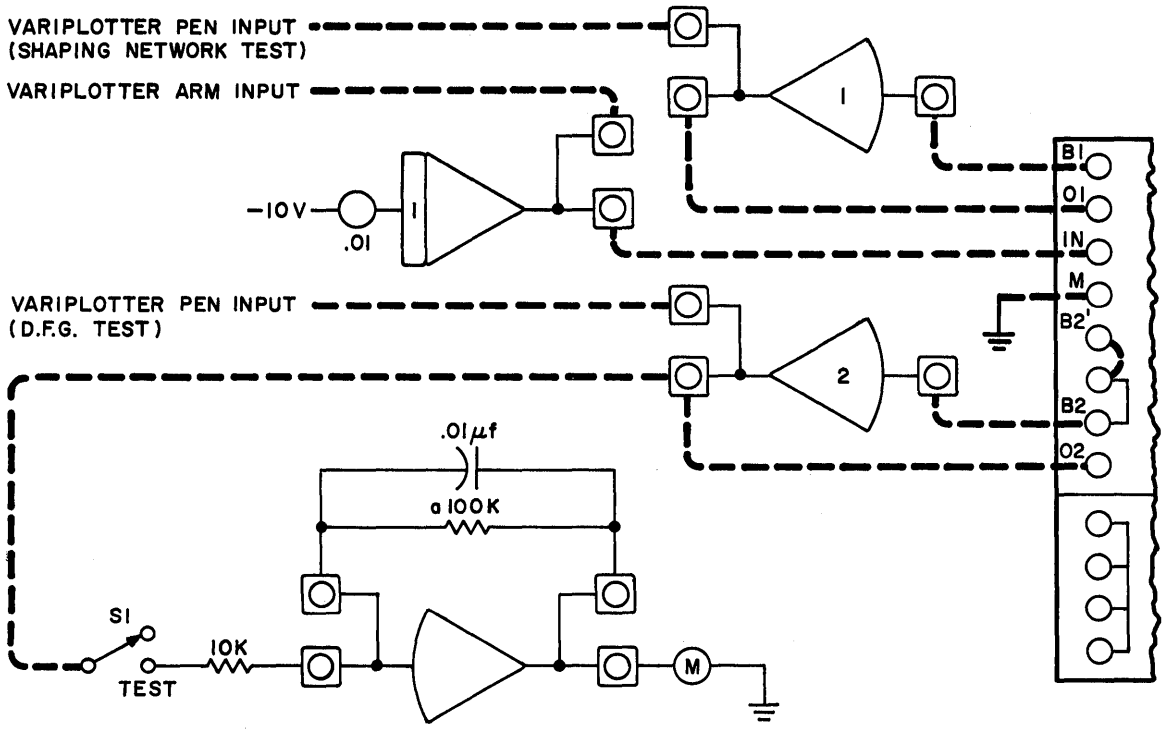


a. PATCHING DIAGRAM
(SHAPING NETWORK TEST)

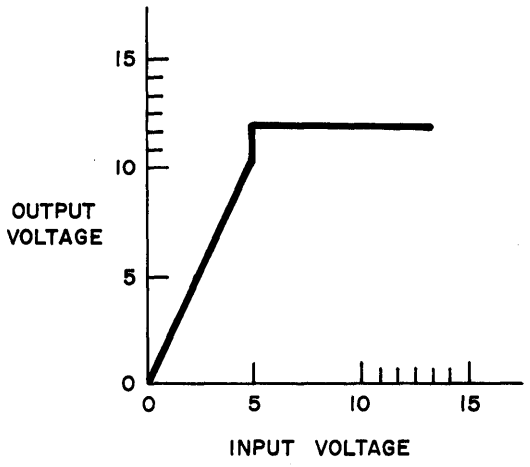


b. SHAPING AMPLIFIER WAVEFORM.

Figure 20. Shaping Network, Test Circuit (Model 16.313 Only)



a. PATCHING DIAGRAM
(SHAPING NETWORK TEST)



b. SHAPING AMPLIFIER WAVEFORM.

Figure 21. Shaping Network, Test Circuit (Model 16.314 Only)

With the DFG still patched for the previous step check the adjustment of the shaping network by plotting the curve shown in Figures 20b or 21b using an EAI 1110 VARIPLOTTER®, Model 99.656. Proceed as follows:

(1) Patch the output from the integrator to IN and the ARM INPUT on the VARIPLOTTER.

(2) Patch the output from amplifier-1 to the PEN INPUT on the VARIPLOTTER.

(3) Set the VARIPLOTTER PEN SCALE and ARM SCALE controls to a suitable volts/inch scaling.

(4) Press the computer OPERATE button and trace out the curve shown in Figures 20b or 21b on the VARIPLOTTER.

(5) Replace the -10 volt reference supply applied to the integrator attenuator with the +10 volt reference supply and repeat Step (4). The curve will be reversed.

4. FIXED DFG SINE ±90° ADJUSTMENTS

Figure 22 illustrates the approximation of the sine function from 0 to -90° using seven straight-line segments. The points marked "breakpoint occurrence" on the diagram indicate the potentials at which diodes CR9 to CR14 conduct and switch in precision resistors in the feedback system of amplifier-2 (Figure 23). The points denoted as "potentiometer set-up points" indicate the potentials at which potentiometers VR3 to VR8 are adjusted to assure proper breakpoint occurrence.

To adjust the breakpoint for the fixed DFG sine -90° proceed as follows:

(1) Patch the sine-cosine DFG as shown in Figure 23.

(2) Turn potentiometers VR3 to VR8 fully counter-clockwise.

(3) Set the attenuator to obtain each of the input voltages listed in Table 7 and apply in turn to M1. The inversion through the unity gain amplifier-1 must be observed.

(4) Adjust the corresponding breakpoint potentiometer to obtain the output voltages listed.

As an example of how the sine function is obtained consider a voltage of +5 volts (-45°) to be applied to M1. Breakpoint diodes CR9 and CR10 both conduct, decreasing the slope of amplifier-2 thus generating -7.07 volts or sine -45° (see Figure 22).

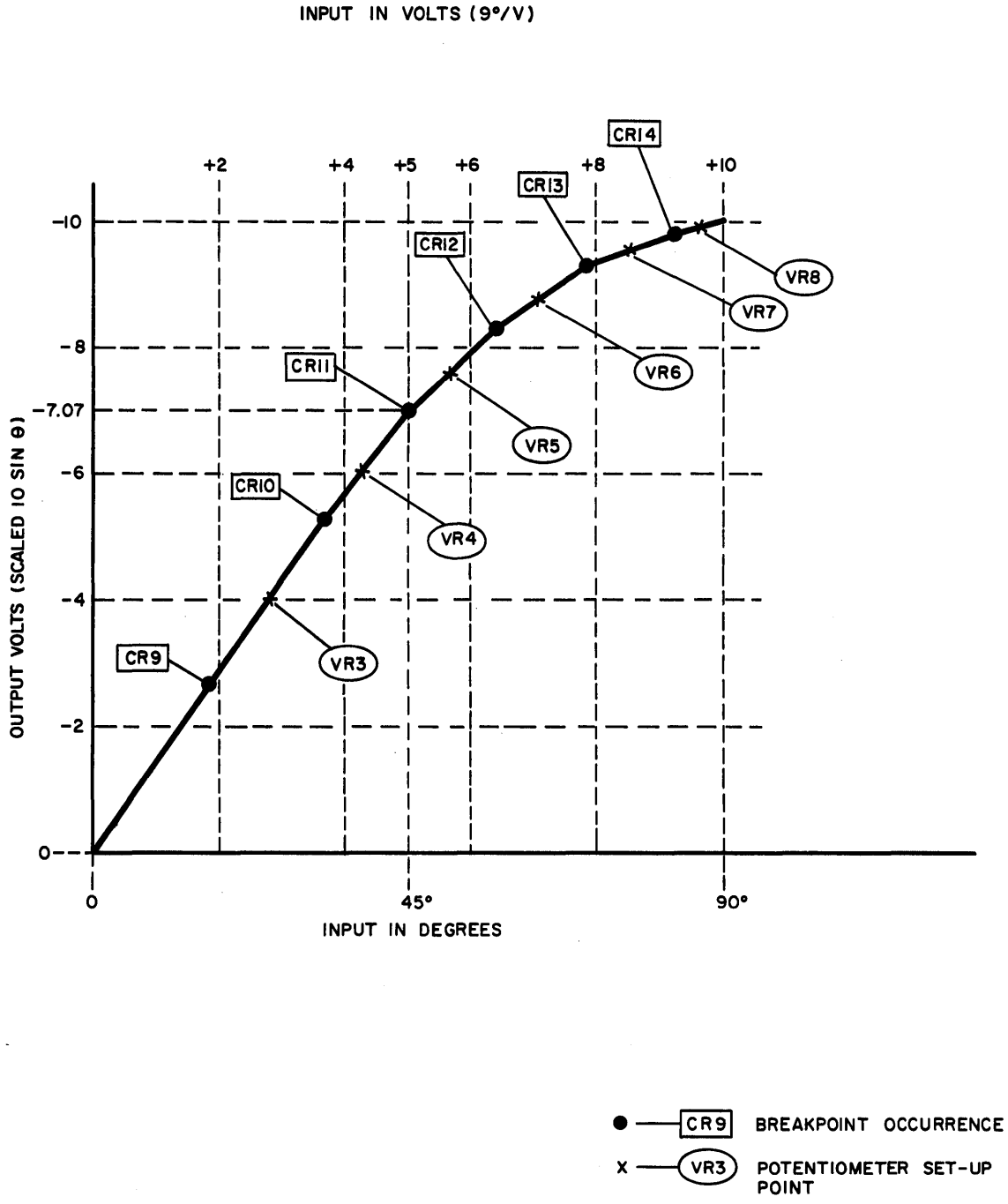
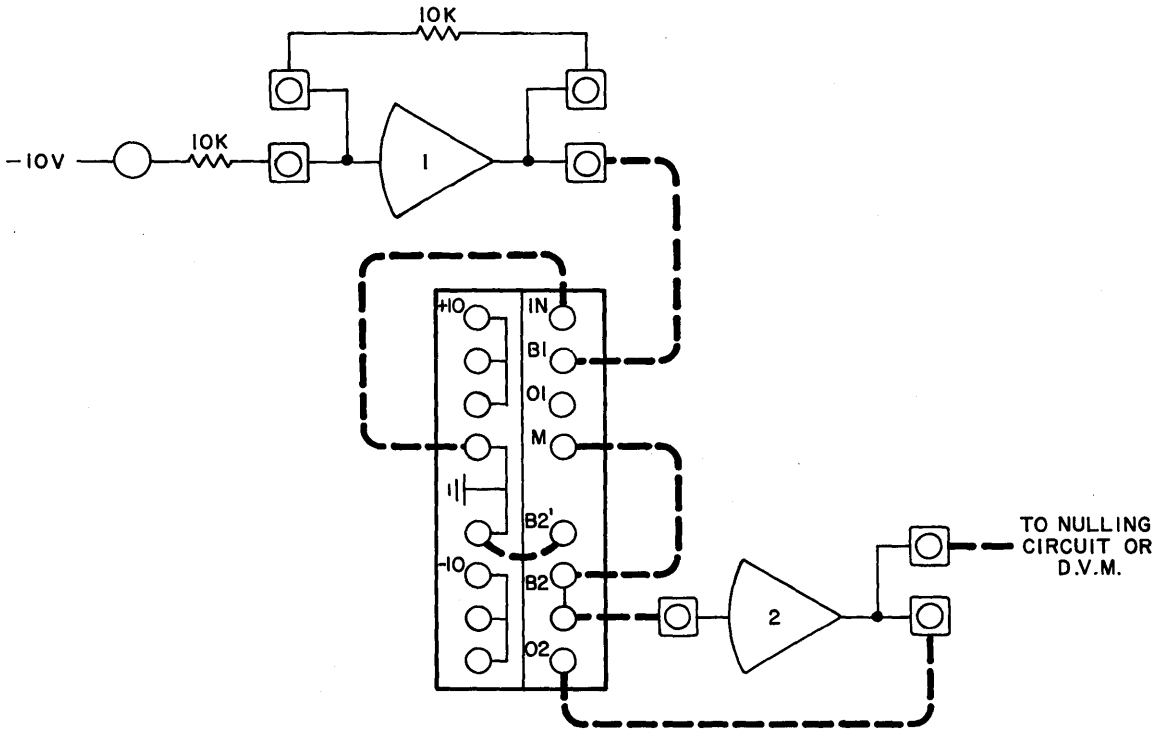
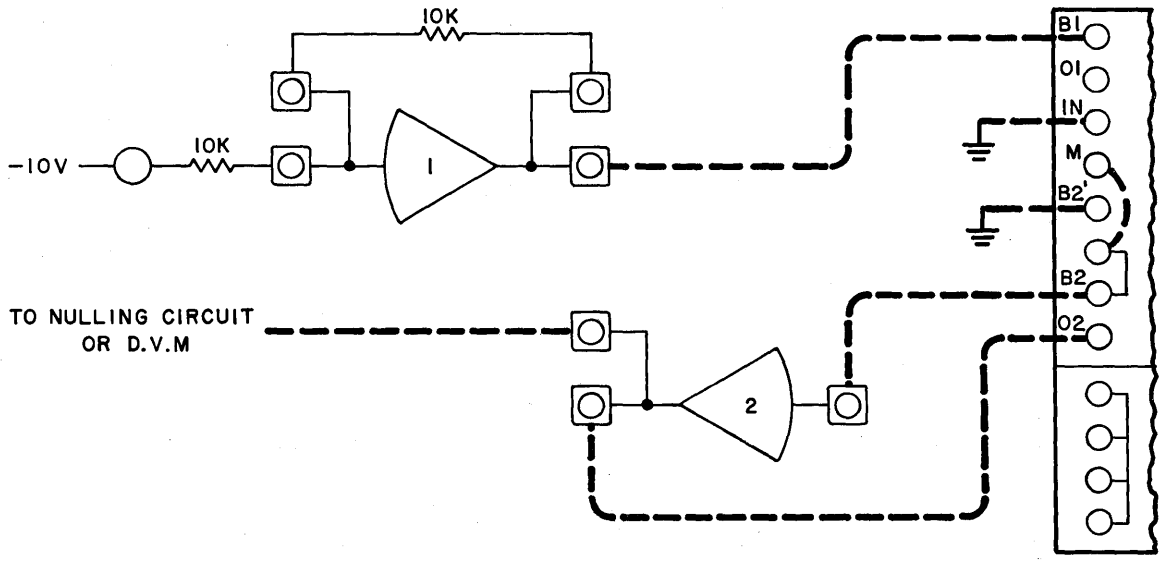


Figure 22. DFG Test Circuit



a. SINE ±90° PATCHING FOR MODEL 16.313



b. SINE ±90° PATCHING FOR MODEL 16.314

Figure 23. Sine ±90° Test Circuit

TABLE 7. Breakpoint Setting Fixed DFG Sine -90°

Input Voltage (M1)	Breakpoint		Output Voltage
	Diode	Potentiometer	
+2.88	CR9	VR3	-4.36
+4.39	CR10	VR4	-6.35
+5.77	CR11	VR5	-7.86
+7.24	CR12	VR6	-9.06
+8.49	CR13	VR7	-9.71
+9.53	CR14	VR8	-9.96

To adjust the breakpoints for the fixed DFG sine +90° proceed as follows:

(1) Repeat Steps (1) to (4) replacing the -10 volt reference supply applied to the attenuator with the +10 volt reference supply and adjust breakpoint potentiometers VR9 to VR13 (having previously set them fully counter-clockwise) to obtain the output voltages listed in Table 8.

TABLE 8. Breakpoint Setting Fixed DFG Sine +90°

Input Voltage (M1)	Breakpoint		Output Voltage
	Diode	Potentiometer	
-2.88	CR16	VR9	+4.36
-4.39	CR17	VR10	+6.35
-5.77	CR18	VR11	+7.86
-7.24	CR19	VR12	+9.06
-8.49	CR20	VR13	+9.71
-9.53	CR21	VR14	+9.96

To check the breakpoint adjustments of the Model 16.314,DFG in the sine ±90° mode use the patching shown in Figure 23b. By applying the input to M, the 100K resistor (R3) becomes the input resistor for amplifier-2 thus altering the input scaling to 9°/volts. To complete the test configuration the output of the bridge rectifier (junction of CR5 and CR8) is connected to ±GRD. Proceed with Step (1).

(1) Patch the output from the integrator to IN and to the ARM INPUT on the VARIPLOTTER.

(2) Patch the output from amplifier-2 to the PEN INPUT on the VARIPLOTTER.

(3) Set the VARIPLOTTER PEN SCALE and ARM SCALE controls to a suitable volts/inch scaling.

(4) Patch the DFG in the sine mode as shown with M = 0 volt.

(5) Press the computer OPERATE button and check that the VARIPLOTTER plots the curve shown in Figure 16d.

(6) Repeat Step (5) with the DFG patched in the + cosine mode (M = +10 volts) and - cosine mode (M = -10 volts) and check that the VARIPLOTTER plots the curves in Figures 17d and 18d respectively.

APPENDIX I

REPLACEABLE PARTS LISTS

SINE-COSINE DIODE FUNCTION GENERATORS, MODELS 16.313 AND 16.314

This appendix contains a Replaceable Parts List for the equipment described in this manual. In each case, a brief description of the part is listed. Where applicable, a reference symbol (schematic designation) is included. To enable a particular sheet to be readily located, an index precedes the individual replaceable parts lists.

The category column in the parts list indicates the availability of each listed part so that a replacement part can be obtained as quickly as possible. The components in category A are standard electronic items that are usually available from any commercial electronic supplier. In order to expedite obtaining items of this nature, it is suggested that they be purchased from a local source whenever possible. If necessary these parts may be ordered from EAI.

The parts in category B are components that are available only from EAI. When ordering items of this type, please specify the type number and serial number of the basic unit in which the part is located, as well as the part identification.

PLEASE NOTE THAT EAI RESERVES THE RIGHT TO MAKE PART SUBSTITUTIONS WHEN REQUIRED. IN ALL CASES EAI GUARANTEES THAT THESE SUBSTITUTIONS ARE ELECTRICALLY AND PHYSICALLY COMPATIBLE WITH THE ORIGINAL COMPONENT.

INDEX

ITEM	REF. DESIG.	DESCRIPTION	EAI NO.	*CAT.
1	CR1-14,16-21	Diode: Hughes HS1007E	Order by Description	B
2	CR15,22	Diode, Silicon: Zener, 6.8V ±5%; Brush ZB	Order by Description	B
3	R1,2,3	Resistor, Fixed, Wirewound, Precision: 99,900 ohms ±0.1% Padded to 100,000 ohms +0% -.02% Per EAI Standards.	Order by Description	B
4	R4,7	Resistor, Fixed, Composition: 15K ohms ±5%, 1/4W.	625 153 0	A
5	R5,8	Resistor, Fixed, Wirewound, Precision: 6,000 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
6	R6,49	Resistor, Fixed, Composition: 10K ohms ±5%, 1/2W	626 103 0	A
7	R9	Resistor, Fixed, Wirewound, Precision: 155,300 ohms ±.1%, 1/4W; McMurdo PB Type	Order by Description	B
8	R10,28	Resistor, Fixed, Wirewound, Precision: 13,150 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
9	R11,29	Resistor, Fixed, Wirewound, Precision: 101,420 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
10	R12,30	Resistor, Fixed, Wirewound, Precision: 237,700 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
11	R13,31	Resistor, Fixed, Wirewound, Precision: 258,000 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
12	R14,33	Resistor, Fixed, Wirewound, Precision: 350,100 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
13	R15,34	Resistor, Fixed, Wirewound, Precision: 43,000 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
14	R16,35	Resistor, Fixed, Wirewound, Precision: 480,000 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
15	R17,36	Resistor, Fixed, Wirewound, Precision: 257,000 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
16	R18,37	Resistor, Fixed, Wirewound, Precision: 119,000 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B

*NOTE: THE CATEGORY COLUMN IS DESIGNED TO INDICATE AVAILABILITY OF PARTS.
A - INDICATES PARTS THAT SHOULD BE PURCHASED LOCALLY.
B - INDICATES PARTS THAT SHOULD BE PURCHASED FROM EAI.

DATE 7 / 10 / 64

UNIT TITLE
SINE-COSINE
DIODE FUNCTION GENERATOR

MODEL NO.
16.313 Sh. 1 of 3 Sh.

ITEM	REF. DESIG.	DESCRIPTION	EAI NO.	*CAT.
17	R19,38	Resistor, Fixed, Wirewound, Precision: 356,000 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
18	R20,39	Resistor, Fixed, Wirewound, Precision: 204,000 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
19	R21,40	Resistor, Fixed, Wirewound, Precision: 240,000 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
20	R22,42	Resistor, Fixed, Wirewound, Precision: 55,980 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
21	R23,44	Resistor, Fixed, Wirewound, Precision: 1,506 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
22	R24,45	Resistor, Fixed, Wirewound, Precision: 4,200 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
23	R25,43	Resistor, Fixed, Wirewound, Precision: 60,000 ohms ±1%, 1/4W; McMurdo PB Type	Order by Description	B
24	R26,41	Resistor, Fixed, Composition: 3.3K ohms ±10%, 1/2W	626 332 1	A
25	R27,46	Resistor, Fixed, Composition: 2.7K ohms ±10%, 1/2W	626 272 1	A
26	R32,47,48	Resistor, Fixed, Wirewound, Precision: 49,950 ohms ±0.1%, Padded to 50,000 ohms +0.0% -0.02%	Order by Description	B
27	R50,51	Resistor, Fixed, Wirewound, Precision: 30,000 ohms ±0.1%, 1/4W; McMurdo PB Type	Order by Description	B
28	RT1-4	Thermistor: 1,000 ohms S.T.C. Type K13	Order by Description	B
29	VR1,2	Resistor, Variable: 5,000 ohms ±10%; Bourne Trimit 275	Order by Description	B
30	VR3,9	Resistor, Variable: 10,000 ohms ±20%; Plessey Type G	Order by Description	B
31	VR4,5,10, 11	Resistor, Variable: 47,000 ohms ±20%; Plessey Type G	Order by Description	B
32	VR6,12	Resistor, Variable: 27,000 ohms ±20%; Plessey Type G	Order by Description	B

*NOTE: THE CATEGORY COLUMN IS DESIGNED TO INDICATE AVAILABILITY OF PARTS.
A - INDICATES PARTS THAT SHOULD BE PURCHASED LOCALLY.
B - INDICATES PARTS THAT SHOULD BE PURCHASED FROM EAI.

DATE 7 / 10 /64

UNIT TITLE
SINE-COSINE
DIODE FUNCTION GENERATOR

MODEL NO.
16.313 Sh.2 of 3 Sh.

ITEM	REF. DESIG.	DESCRIPTION	EAI NO.	*CAT.
33	VR7,13	Resistor, Variable: 4,700 ohms ±20%; Plessey Type G	Order by Description	B
34	VR8,14	Resistor, Variable: 2,700 ohms ±20%; Plessey Type G	Order by Description	B

*NOTE: THE CATEGORY COLUMN IS DESIGNED TO INDICATE AVAILABILITY OF PARTS.
A - INDICATES PARTS THAT SHOULD BE PURCHASED LOCALLY.
B - INDICATES PARTS THAT SHOULD BE PURCHASED FROM EAI.

DATE 7/ 10/ 64

UNIT TITLE
SINE-COSINE
DIODE FUNCTION GENERATOR

MODEL NO.
16,313 Sh.3 of 3 Sh.

APPENDIX II

DRAWINGS

SINE-COSINE DIODE FUNCTION GENERATORS, MODELS 16.313 AND 16.314

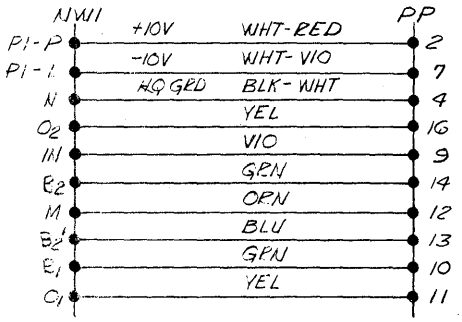
This appendix contains necessary schematics and wiring diagrams of equipment described in this manual. To facilitate locating a particular sheet, an index is provided that lists the model number of each unit or component, the type of drawings, and the associated drawing number. The drawings are bound into the manual in the order listed under the index Drawing Number column.

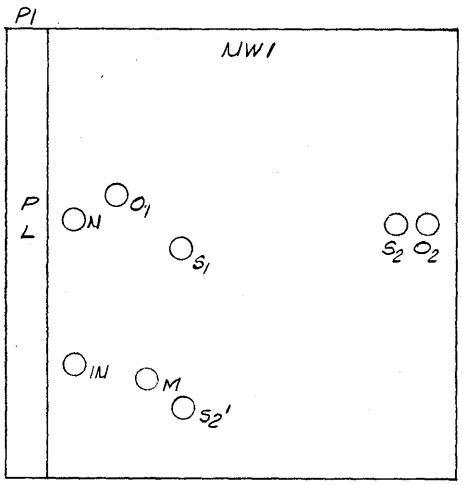
EAI drawings are prepared in accordance with standard drafting practices for electro-mechanical and electronic equipment. All symbols are in accordance with current government standards.

INDEX

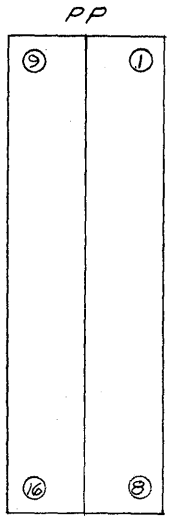
Unit or Component	Type of Drawing	Drawing Number
Sine-Cosine DFG	Wiring Schematic	A016 313 0W C36, 132XS
Sine-Cosine DFG	Wiring	C016 314 0W

NOTES:
UNLESS OTHERWISE SPECIFIED,
1. ALL WIRES TO BE #22 PHU
2. ALL JUMPERS TOBE #22 PHU.
3. WIRES TO RUN THROUGH #4 GRAY TUBING (EAI # 976 009 0) ON COPPER SIDE OF NW1. GRAY TUBING TO BE 3" LONG.



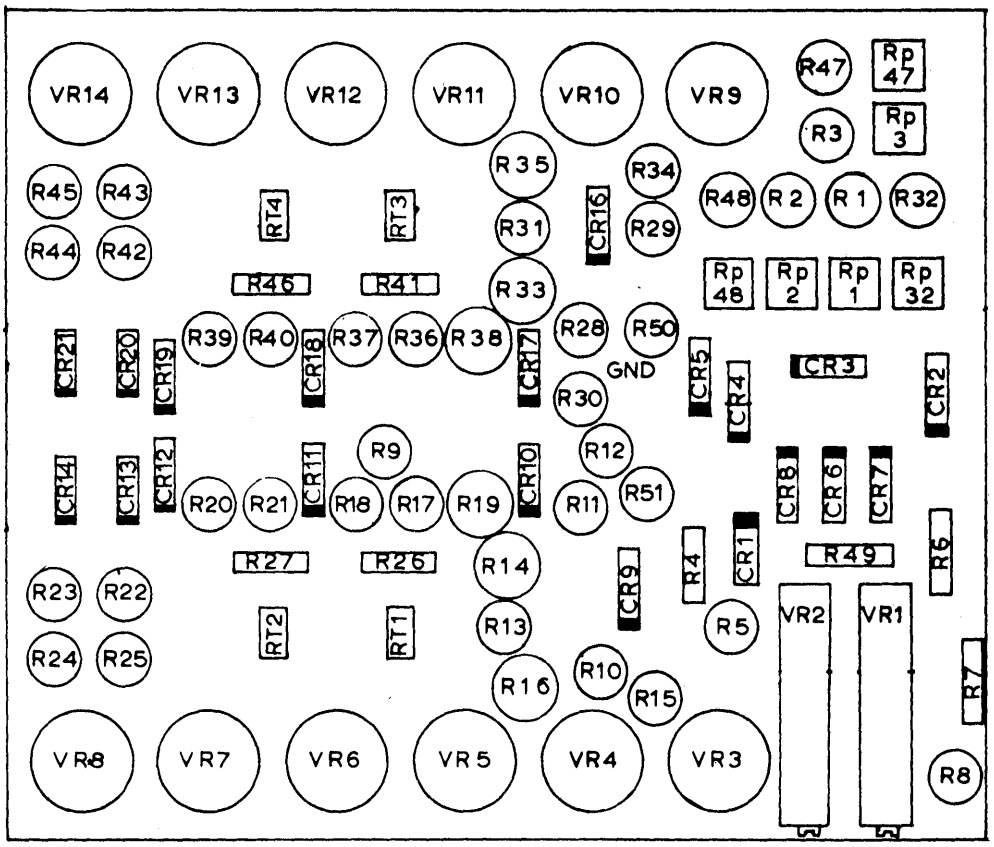


NOTE:
S_1 & S_2 ARE EQUIV. TO B_1 & B_2

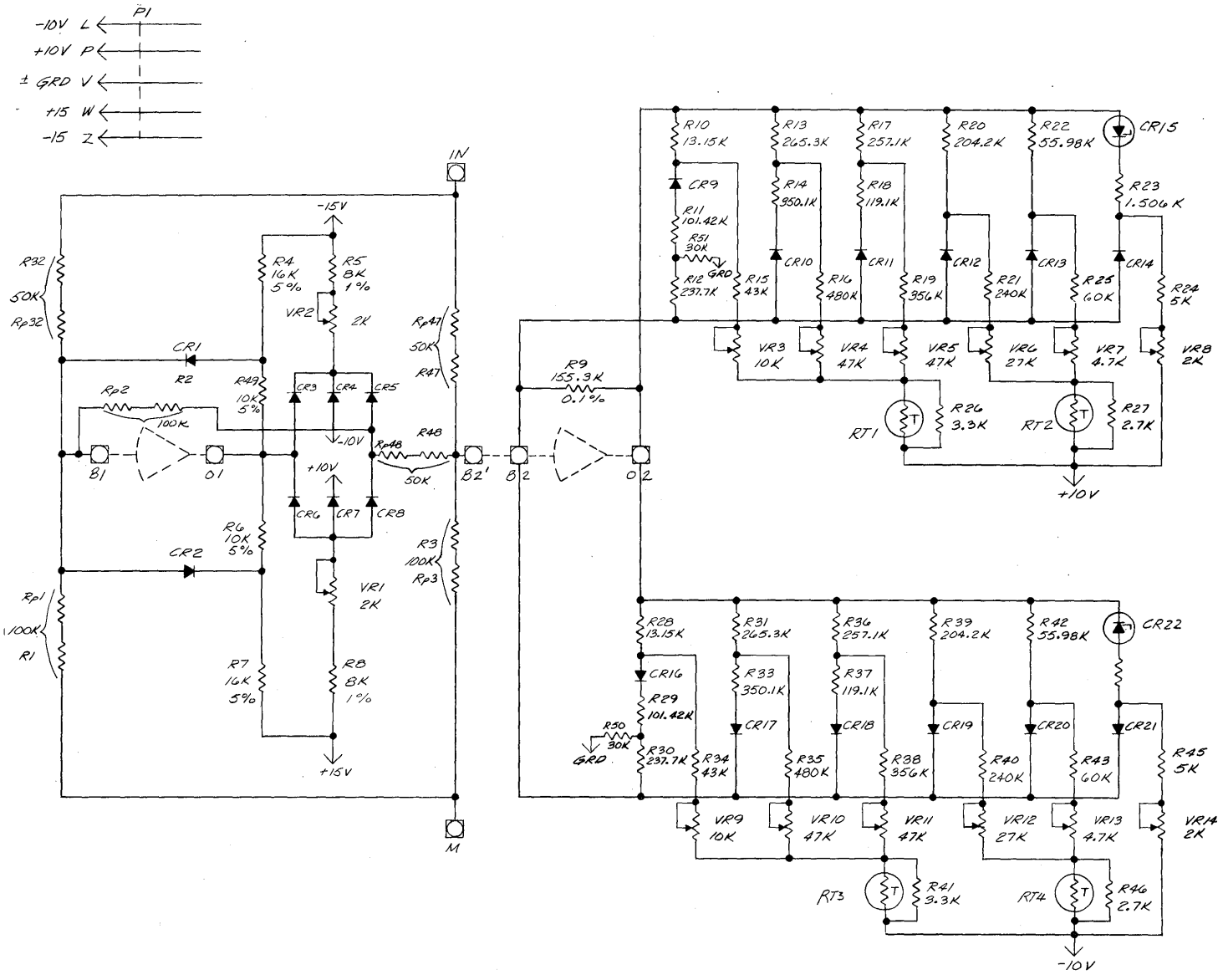


REAR VIEW

ELECTRONIC ASSOCIATES, INC. LONG BRANCH, NEW JERSEY	
WIRING SINE - COS D F G (TR-20)	
SHT. NO.	
SIZE	
REV. NO.	
PROJECT 19098	B 016 313 0W
SHEET / OF / SHEETS	

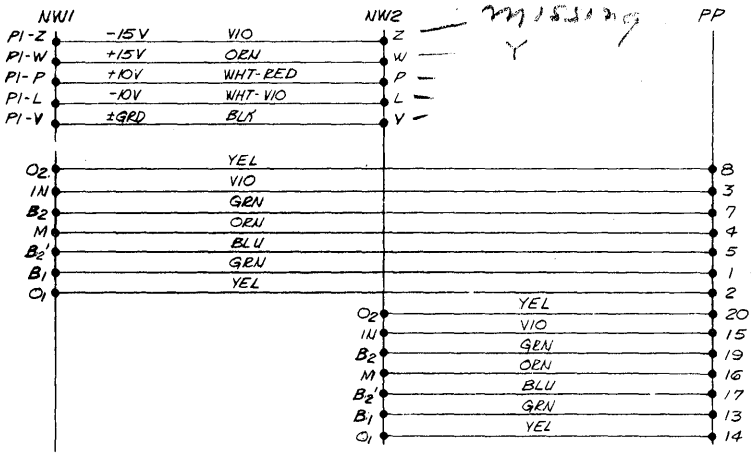


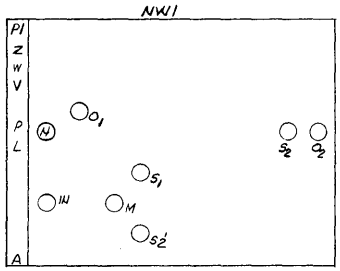
1016.005 Card Assembly Sine-Cosine DFG, Component Location Diagram

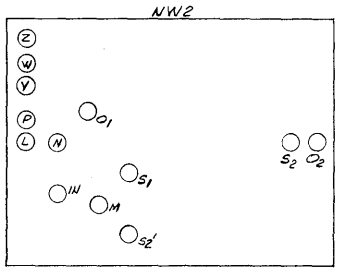


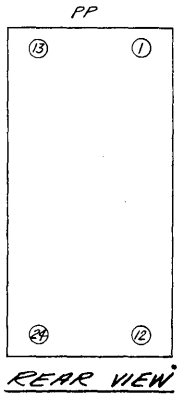
ELECTRONIC ASSOCIATES, INC. LONG BRANCH, NEW JERSEY	
SCHEMATIC SINE-COSINE DIODE FUNCTION GENERATOR (TR-48)	
SHT. NO.	
SIZE	
REV. NO.	
PROJECT 19098	C 36, 132 X5
SHEET 1 OF 1 SHEETS	

NOTES:
UNLESS OTHERWISE SPECIFIED,
1. ALL WIRES TO BE #22 PHU
2. ALL JUMPER TO BE #22 SD-BUS
3. SEE A 018 752 0P FOR HARNESS ASSEMBLY.









NOTE
1. S_1 & S_2 ARE EQUIV. TO B_1 & B_2

ELECTRONIC ASSOCIATES, INC. LONG BRANCH, NEW JERSEY	
WIRING SWE-COS DFG (TR-48)	
SHT. NO.	
SIZE	
REV. NO.	
PROJECT /9098	C 016 314 0W
SHEET / OF / SHEETS	