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SANTA ANA, CALIFORNIA

EECO "T-SERIES"
Germanium
TRANSISTOR
PLUG-IN CIRCUITS

SPECIFICATION SHEETS

FOR

"T-SERIES"

GERMANIUM TRANSISTOR

PLUG-IN CIRCUITS

A fully compatible family
of circuits

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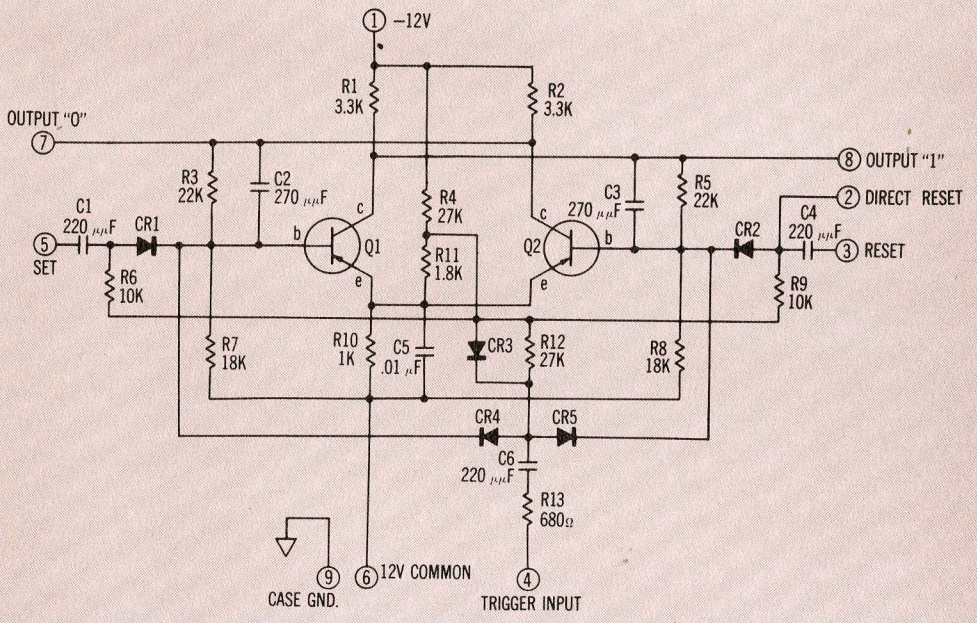
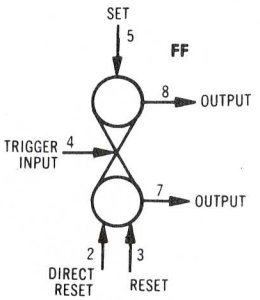


"T-SERIES"
Germanium
TRANSISTOR PLUG-IN CIRCUITS

RST FLIP-FLOP



T-101

CIRCUIT DESCRIPTION

The T-101 is an RST Flip-Flop for general application. It uses two Germanium PNP transistors. Saturated operation of the transistors is employed at the sacrifice of higher-speed operation to obtain maximum independence of transistor parameter variations and to provide maximum stability and reliability.

The T-101 can be triggered in either of two modes:

1. In the T (trigger or binary) mode, each input pulse changes the state of the flip-flop. Standard operating range is 0 to 250 kc.
2. a) In the RS (reset and set) mode, a pulse on the Set input will change output "0" to the "1" condition (−3 volts), and the "1" to the "0" condition (−11 volts). Subsequent set pulses will have no effect.
   b) The inverse is true for the Reset input.
   c) The direct reset input is for use when several flip-flops are to be reset in synchronism as when a dc reset generator is used.
   d) The standard operating range in the RS mode is 0 to 300 kc.

All inputs are diode isolated.

ELECTRICAL SPECIFICATIONS

Input:

General Range: 5½ to 9 volts between 0.2 and 1 microsecond rise time.

Inputs Available: Set, Reset, Trigger, and DC Reset.

Signal Frequency Range: 0 to 250 kc in T mode; 0 to 300 kc in RS mode (with alternate pulses applied to R and S inputs). In the T mode, input signals to 400 kc are permissible with lighter loading, e.g., one emitter follower on each output and a minimum input of 7 volts at 0.4 microsecond rise time.

Minimum Input Amplitude (R, S, or T input): The T-101 will *not* trigger on a positive-going pulse of 1½ volts or less, regardless of rise time. The T-101 will *always* operate on a positive-going pulse of 5½ volts or greater at a rise time of 1 microsecond or faster.

Maximum Input Amplitude: 9 volts peak.

Rise Time: 0.2 to 1.0 microsecond. (Rise = positive-going; fall = negative-going.)

Duty Cycle: Above 150 kc, in the RS mode, input signal pulse widths should be restricted to allow 5½ microseconds recovery time on each input.

Output:

Outputs Available: Two, of opposite polarity: "0" output and "1" output.

Amplitude: 8-volt level shift from −11 volts dc to −3 volts dc nominal.

Rise Time: 0.8 microsecond nominal under typical load.

Fall Time: Approximately 1½ microseconds.

Loading:

Typical load is a paralleled combination of 1 flip-flop, 1 emitter follower, 1 indicator, and 50 μμf capacitance to ground.

Maximum resistive loading is:
0.2 ma to a positive source.
1.0 ma to a negative source.

Power Required:

−12 volts dc at 4 ma. Pin 1 to be negative with respect to pin 6.

Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	Direct reset
3	Reset
4	Trigger
5	Set
6	12-volt common
7	Output "0"
8	Output "1"
9	Case ground

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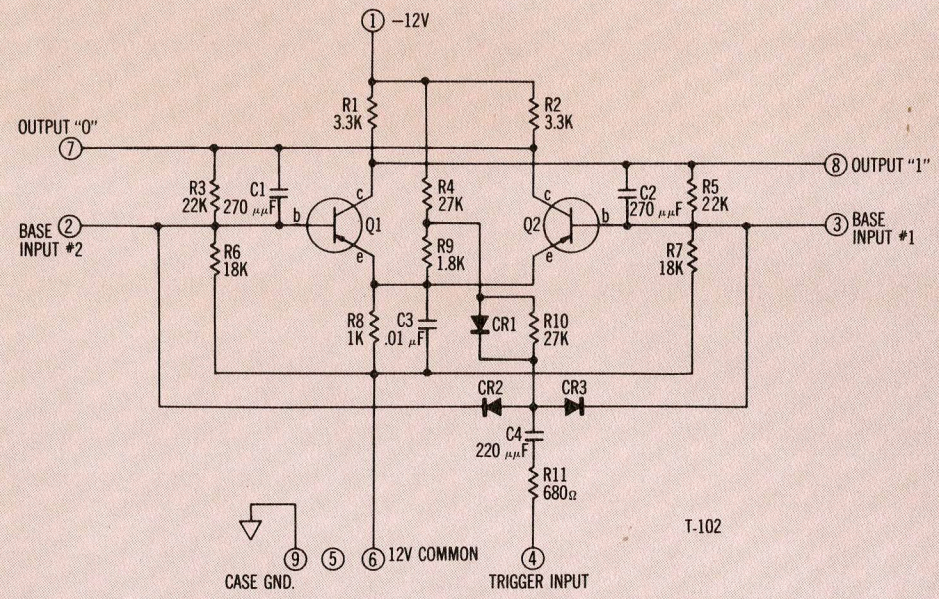
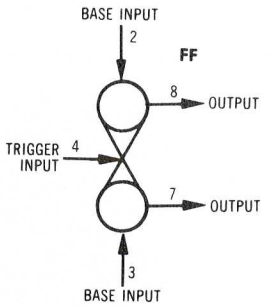


Note: Q1, Q2-type 2N269

"T-SERIES"
Germanium
TRANSISTOR PLUG-IN CIRCUITS
T FLIP-FLOP



T-102

CIRCUIT DESCRIPTION

The T-102 is a "T" Flip-Flop very similar to the general purpose T-101. It differs in that the diode-isolated set and reset inputs have been eliminated and replaced with a direct connection to the base of each transistor. For applications where a flip-flop will be used only with a binary or trigger input, a substantial cost saving is permitted.

The T-102 is basically intended to be triggered in the T (trigger or binary) mode, where each input pulse changes the state of the flip-flop. Standard operating range is 0 to 250 kc.

The units can be used in set and reset operation where external circuitry contains the proper input circuit permitting set and reset connections to be made directly to the transistor base. In this mode, the maximum frequency is 300 kc.

ELECTRICAL SPECIFICATIONS

Input:

Trigger Input (pin 4):

General Range: 5½ to 9 volts between 0.2 and 1 microsecond rise time.

Signal Frequency Range: 0 to 250 kc. In the T mode, input signals to 400 kc are permissible with lighter loading, e.g., one emitter follower on each ouput and a minimum input of 7 volts at 0.4 microsecond rise time.

Minimum Input Amplitude: The T-102 will *not* trigger on a positive-going pulse of 1½ volts or less, regardless of rise time.

Maximum Input Amplitude (9 volts peak): The T-102 will *always* operate on any positive-going pulse of 5½ volts or greater at a rise time of 1 microsecond or faster.

Rise Time: 0.2 to 1.0 microsecond.

Base Input (pins 2 and 3):

The minimum pulse amplitude for base input should change from a nominal −3.5-volt dc level to a −1.0-volt dc level. Other conditions consistent with triggered input specifications listed above with a frequency range of 0 to 300 kc.

Output:

Outputs Available: Two, of opposite polarity: "0" output and "1" output.

Amplitude: 8-volt level shift from −11 volts dc to −3 volts dc nominal.

Rise Time: 0.8 microsecond nominal under typical load.

Fall Time: Approximately 1½ microseconds. (Rise = positive-going; fall = negative-going.)

Loading:

Typical load is a paralleled combination of 1 flip-flop, 1 emitter follower, 1 indicator, and 50 μμf capacitance to ground.

Maximum resistive loading is:

0.2 ma to a positive source.

1.0 ma to a negative source.

Power Required:

−12 volts dc at 4 ma. Pin 1 to be negative with respect to pin 6.

Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	Base No. 2
3	Base No. 1
4	Trigger input
5	Unused
6	12-volt common
7	Output "0"
8	Output "1"
9	Case ground

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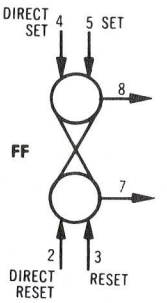
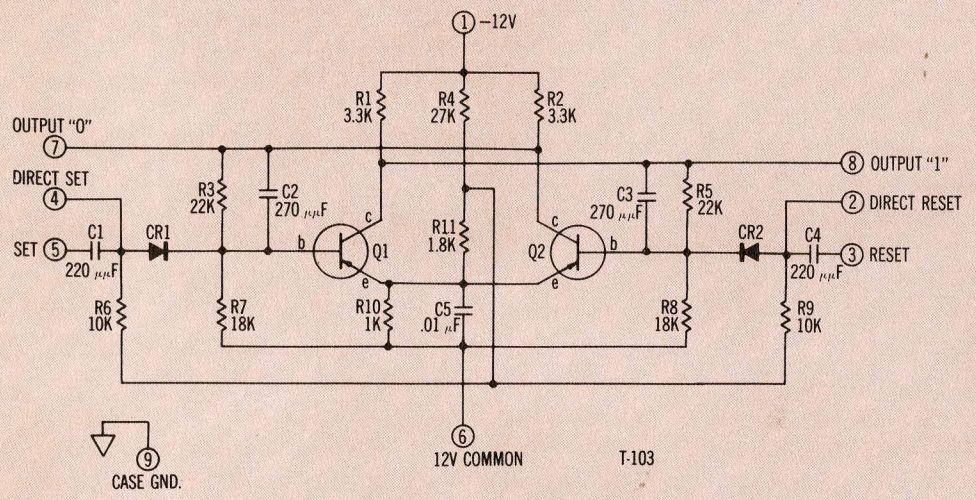
RS FLIP-FLOP



T-103



Note: Q1, Q2-type 2N269

CIRCUIT DESCRIPTION

The T-103 is an RS Flip-Flop very similar to the general purpose T-101. It differs in that the binary or trigger input has been deleted with a substantial reduction in cost for applications where that input is not used. A direct set input has been added. Typical use for the T-103 would be for storage, memory, pulse width generation, or scanning.

The T-103 can be triggered in either the R or S (Reset and Set) modes, directly or through internally contained capacitors.

1. a) A pulse on the set input will change Output "0" to the "1" condition (−3 volts), and Output "1" to the "0" condition (−11 volts). There will be no change for a set input if the flip-flop is already in this condition.
   b) The inverse is true for the Reset input.
   c) The direct reset and direct set are for use when several flip-flops are to be set and reset in synchronism as when a dc reset generator is used.
2. The standard operating range for the T-103 is 0 to 300 kc.

ELECTRICAL SPECIFICATIONS

Input:
- General Range: 5½ to 9 volts between 0.2 and 1 microsecond rise time.
- Inputs Available: Set, Reset, Direct Set, and Direct Reset.
- Signal Frequency Range: 0 to 300 kc with separate pulses applied to R and S inputs.
- Minimum Input Amplitude: The T-103 will *not* trigger on a positive-going pulse of 1½ volts or less, regardless of rise time.
  The T-103 will *always* operate on any positive-going pulse of 5½ volts or greater at a rise time of 1 microsecond or faster.
- Maximum Input Amplitude: 9 volts peak.
- Rise Time: 0.2 to 1.0 microsecond. (Rise = positive-going; fall = negative-going.)
- Duty Cycle: Above 150 kc, in the RS mode, input signal pulse widths should be restricted to allow 5½ microseconds recovery time on each input.

Output:
- Outputs Available: Two, of opposite polarity: "0" output and "1" output.
- Amplitude: 8-volt level shift from −11 volts dc to −3 volts dc nominal.
- Rise Time: 0.8 microsecond nominal under typical load.
- Fall Time: Approximately 1½ microseconds.

Loading:
- Typical load is a paralleled combination of 1 flip-flop, 1 emitter follower, 1 indicator, and 50 μμf capacitance to ground.
- Maximum resistive loading is:
  0.2 ma to a positive source.
  1.0 ma to a negative source.

Power Required:
- −12 volts dc at 4 ma. Pin 1 to be negative with respect to pin 6.
- Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	Direct reset
3	Reset
4	Direct set
5	Set
6	12-volt common
7	Output "0"
8	Output "1"
9	Case ground

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"T-SERIES"
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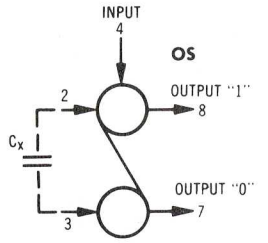
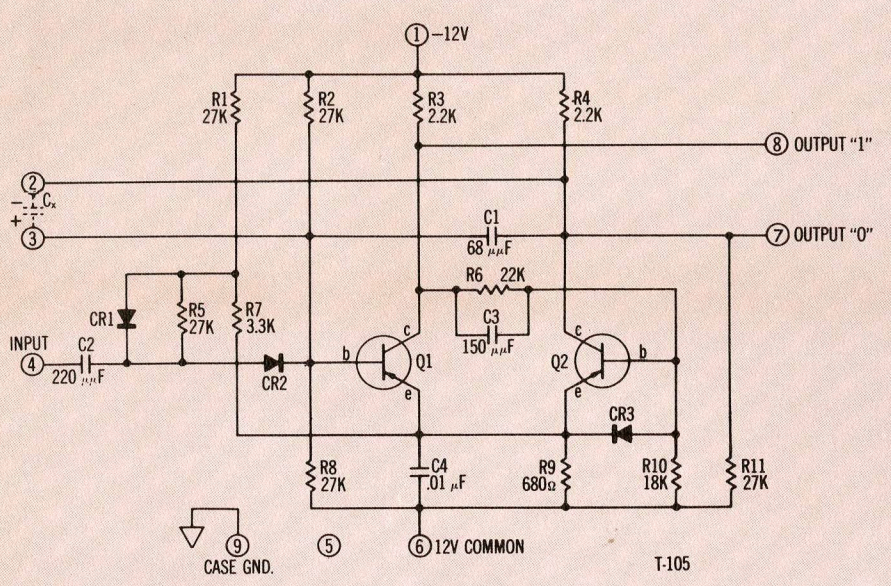
ONE-SHOT MULTIVIBRATOR



T-105



Note: Q1, Q2-type 2N269

CIRCUIT DESCRIPTION

The T-105 is a transistor One Shot for general application. It uses two PNP germanium transistors in saturated operation to obtain maximum independence of transistor parameter variations and therefore maximum stability and reliability. Typical uses for the T-105 include pulse width generation, time delay, and temporary digit storage.

The T-105 is triggered by a positive pulse or positive-going input step. Two outputs (rectangular pulses of opposite polarity) are available. Pulse widths from 2 microseconds ($C_x = 0$) to 50 milliseconds ($C_x = 2.5$ μf approximately) are obtainable at duty cycles up to 75%. For greater widths up to one second, electrolytic capacitors can be used if correct polarity is observed.

ELECTRICAL SPECIFICATIONS

Input:

Signal Frequency Range: 0 to 250 kc.

Trigger Input Amplitude (pin 4):

a) The T-105 will *not* trigger on a positive input pulse of 1.5 volts or less, regardless of rise time.

b) The T-105 will *always* operate on a positive input pulse of 5 volts with a rise time of 1 microsecond.

c) Sensitivity is correspondingly greater for sharper rise times.

d) Maximum trigger input is 9 volts peak.

e) Rise time range is from 0.2 microsecond to 1.0 microsecond.

Output:

Outputs Available: Two of opposite polarity: "0" output (pin 7), "1" output (pin 8).

Amplitude: 8 volts level shift from −11 volts dc to −3 volts dc.

Rise Time: 0.4 microsecond nominal under typical load.

Fall Time: Output "1": 1.5 microsecond nominal; output "0": Nominally 20% of pulse duration.

Pulse Duration: The duration of the output pulse is primarily determined by an external capacitor connected between pins 2 and 3. The relation between capacity and duration is given by:

$$C_x = 50\,(t - 2)$$

where t is in microseconds, C_x is in μμf.

The minimum pulse duration is 2 microseconds with no external capacitor used. The maximum pulse duration is 1 second with $C_x = 50$ μf.

Duty Cycle: 75% maximum.

Loading:

A typical load for the "0" output (pin 7) is 2 flip-flops for frequencies up to 125 kc and 1 flip-flop from 125 kc to 250 kc. A typical load for the "1" output (pin 8) is 2 flip-flops for all frequencies.

Power Required:

−12 volts dc at 5 ma. Pin 1 to be negative with respect to pin 6.

Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	External capacitor negative
3	External capacitor positive
4	Input
5	Unused
6	12-volt common
7	Output "0"
8	Output "1"
9	Case ground

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"T-SERIES"
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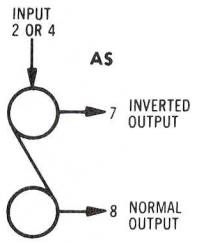
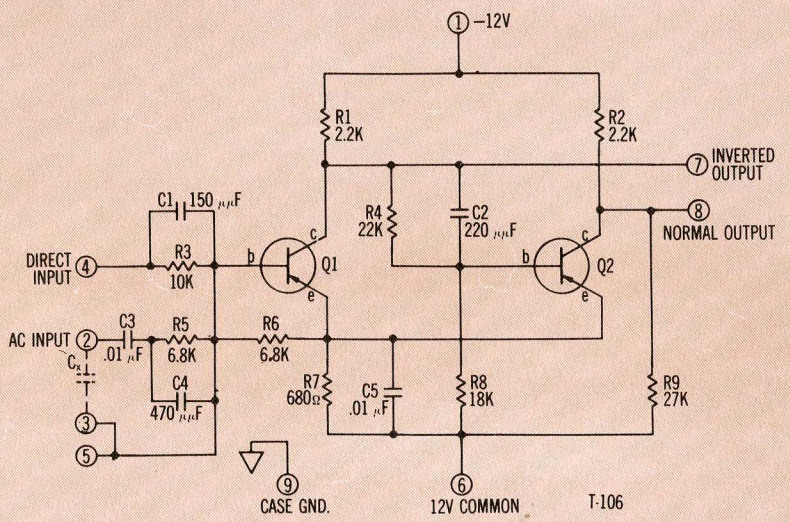
TRANSISTOR PLUG-IN CIRCUITS
SQUARING AMPLIFIER



T-106



Note: Q1, Q2-type 2N269

CIRCUIT DESCRIPTION

The T-106 general-purpose Squaring Amplifier is typically used for such purposes as waveform restoration, signal level shifting, "Not" circuits, squaring sinusoidal or nonrectangular inputs, pulse amplification, and dc level detecting. Two outputs are available, (a normal and an inverted output), both of which are rectangular waveforms of opposite polarities.

The unit is a modified Schmidt Trigger which remains in one output state until the input exceeds the trigger level. At this time the output levels switch to the opposite condition.

The trigger level is adjustable. Without external connection (pin 5 floating), the threshold level is −2.5 volts dc. Suitable bias connected to pin 5 will establish different trigger levels to fit various applications. For example, in a system using our standard signal levels of −3 and −11 volts, a threshold of −6.5 volts could be desired to permit the T-106 to function as a "Not" circuit or signal restorer. The −6.5-volt threshold occurs when pin 5 is connected to our standard +12-volt dc supply through a 47,000-ohm resistor.

ELECTRICAL SPECIFICATIONS

Input:

Direct Input (pin 4): Signal must shift above and below the threshold level (−2.5 volts dc) by +½ volt and −2½ volts dc, which would be a dc level shift from −2 volts dc to −5 volts dc. A signal possessing this minimum level excursion can be shifted to encompass the desired range by suitable biasing on pin 5 (i.e., by connecting an external resistor to ±12 volts dc).

AC Input (pin 2): 4 volts peak-to-peak sine wave minimum.

Operating Frequency Range: 0 to 500 kc (pin 4); 50 to 500 kc (pin 2).

Sine Wave Inputs: For lower than 50 kc, use pin 2 and add an external capacitor across pins 2 and 3.

Output:

Normal Output (pin 8): Rectangular signals of 8 volts peak-to-peak amplitude. Levels are −11 volts dc and −3 volts dc.

Rise Time Normal Output: 0.6 microsecond under maximum loaded conditions.

Inverted Output (pin 7): Rectangular signal of 8 volts peak-to-peak amplitude. Levels are −11 volts dc and −3 volts dc.

Rise Time Inverted Output: 0.8 microsecond under maximum loaded conditions.

Loading:

Typical, up to 2 paralleled flip-flop inputs.

Power Required:

−12 volts dc at 4 ma. Pin 1 to be negative with respect to pin 6.

Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	AC (capacitor-coupled) input
3	Tie point for external capacitor for sine frequencies below 50 kc
4	Direct input
5	Level adjusting bias
6	12-volt common
7	Inverted output
8	Normal output
9	Case ground

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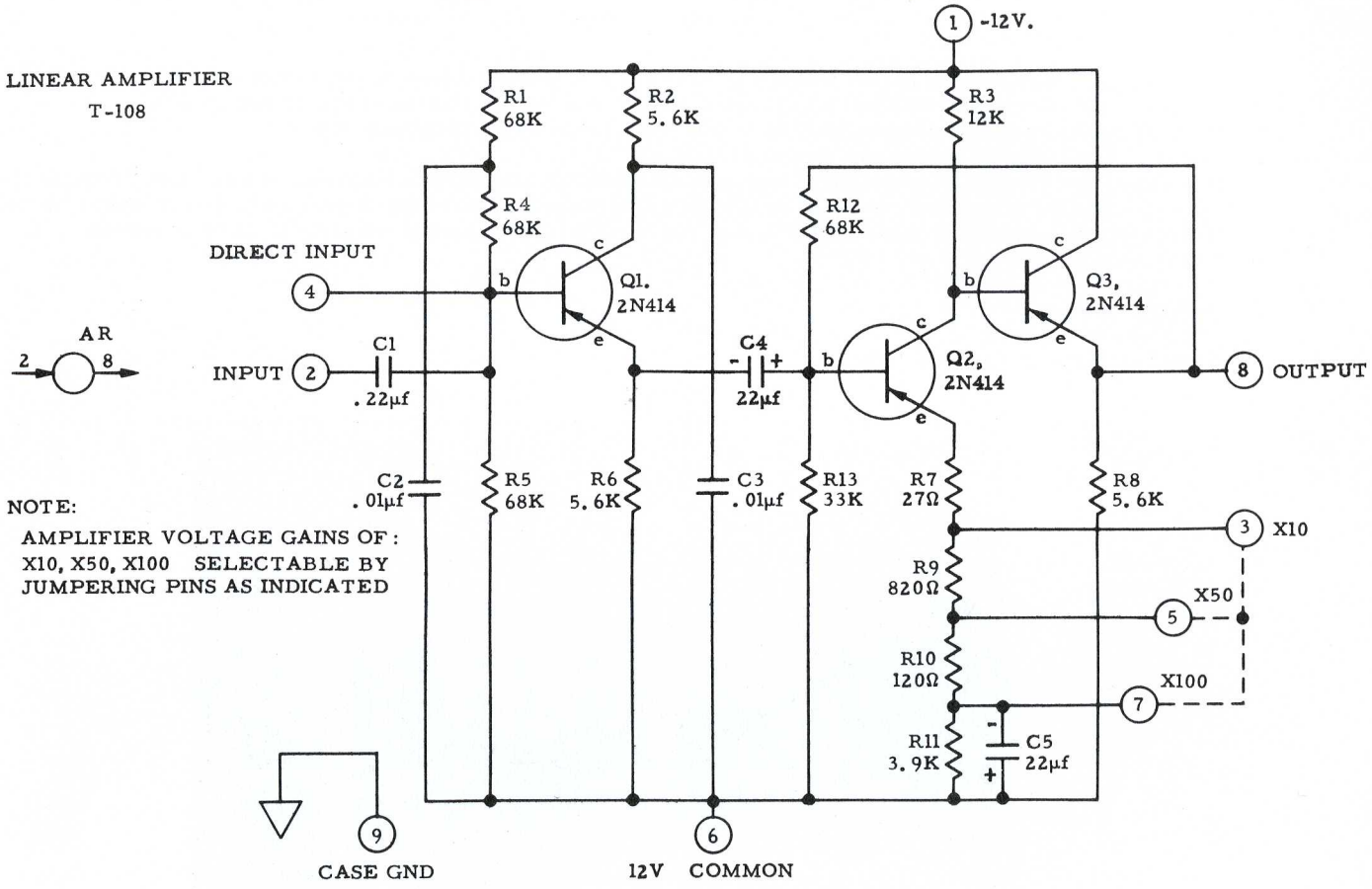


GENERAL

This unit is a transistorized assembly containing three germanium transistors in a linear amplifier circuit. The purpose is to increase the amplitude of small input signals. Both A.C. and D.C. feedback are incorporated for stability of operation.

Inputs can be sine waves, square waves, pulses or any complex wave forms provided the frequency components of the signal are within the response range of the amplifier.

Inputs can be derived from a variety of external sources including voltage pickups and low level transducers. Signals as small as 50 mv PP can be amplified to a 5 V PP level.

Features include high input impedance, low output impedance, three selectable fixed gains, provisions for obtaining any intermediate gain by use of external resistors and provisions for extending low frequency response by use of external capacitors.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

ELECTRICAL SPECIFICATIONS

A. Input:
1. Signal Frequency Range: 20 cps to 800 kc sine wave. Low frequency limit is extended when using large external capacitors.
2. Amplitude Range: 5 mv to 0.6 V PP depending upon gain, for linear operation.
3. Maximum Amplitude: 12 V PP.
4. Input Impedance: Better than 13KΩ at 1 kc at any gain. See chart for limits of input impedance versus frequency.
5. Wave Form: Sinusoidal, or complex if the frequency components are within response range of the amplifier.

OVER

B. Output:

1. Type: One emitter follower output. D.C. level is -6.5 V D.C. nominal.
2. Phase: Output signal is inverted (180°) relative to input.
3. Amplitude: 6 V peak to peak maximum undistorted.
4. Gain: Any of three voltage gains may be obtained by jumpering socket pins as indicated below:

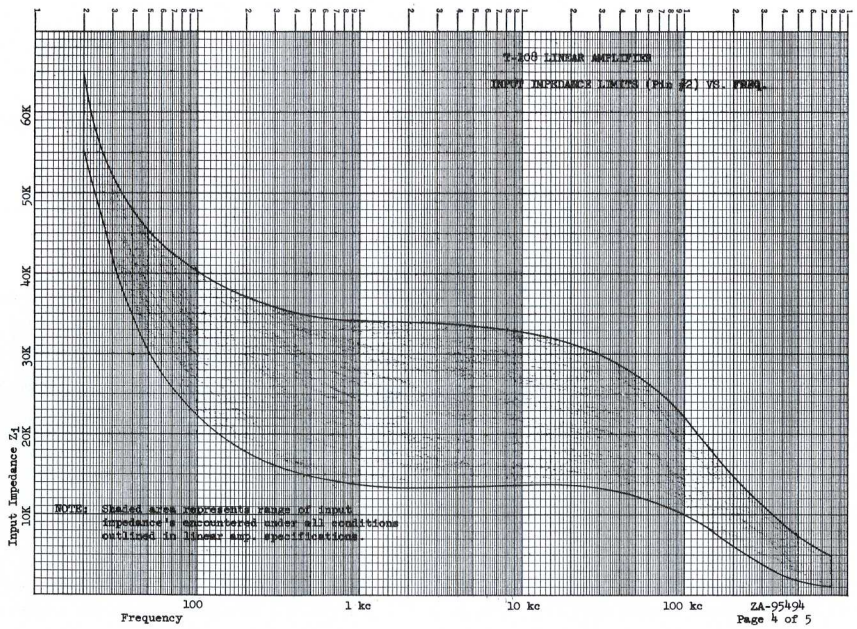
Selected Gain	Pins Jumpered
10	None
50	3 and 5
100	3 and 7

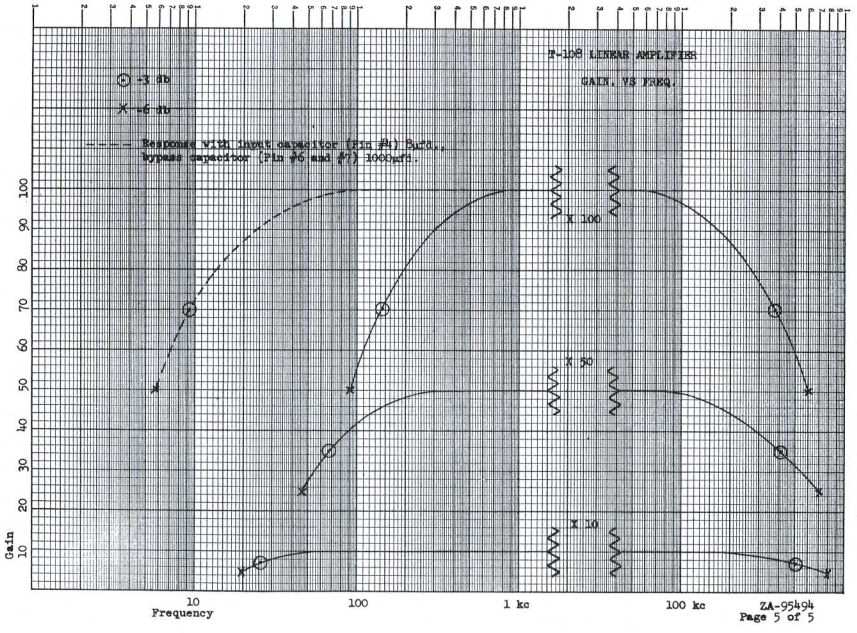
Variable gain may be obtained by connecting the arm of a potentiometer to Pin #7 and one end to Pin #3. Fixed intermediate gains may be obtained by connecting a suitable resistor between Pin #3 and Pin #7.

5. Output Impedance: 150Ω nominal at 1 kc. 350Ω nominal at upper frequency limit.
6. Loads: Typical load is a squaring amplifier unit.
7. Response: The frequency response at each gain is shown on gain versus frequency chart. Low frequency response may be extended (shown only for gain of 100) by using large external input capacitor to direct input (Pin #4) and by adding external capacitor between Pin #6 and Pin #7. Correct capacitor polarity must be observed.
8. Random Output Noise: 20 mv PP.

C. Power Requirements:

1. -12 V DC at 2.5 ma.
2. **Supply voltage tolerance: ± 10%.**





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"T-SERIES"
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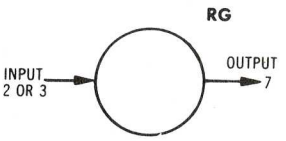
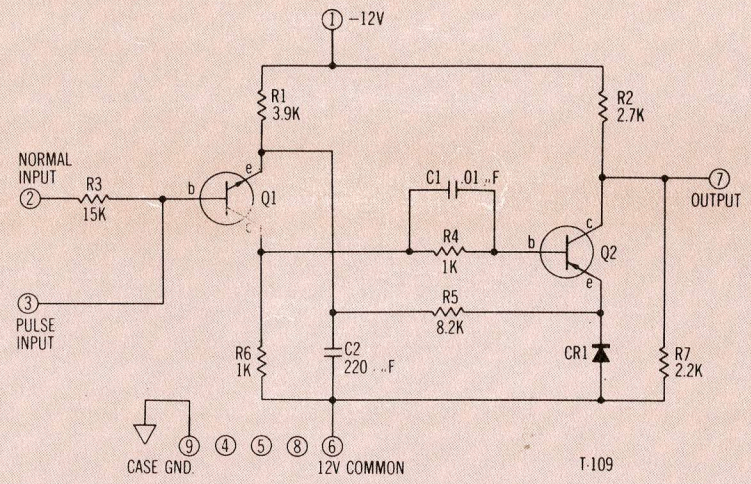
TRANSISTOR PLUG-IN CIRCUITS
RESET GENERATOR



T-109



Note: Q1-type 2N438; Q2-type 2N269

CIRCUIT DESCRIPTION

The T-109 is a transistorized DC Reset Generator for the purpose of resetting up to 15 flip-flops. For the duration of an applied input signal all flip-flops are continuously held in the reset condition and cannot be triggered in any manner. Upon removal of the input signal, all flip-flops are immediately allowed to respond to their normal input signals.

The standard input is an 8-volt dc signal such as would be obtained from a flip-flop, a one-shot, or a gate. Pulse resetting may also be employed.

ELECTRICAL SPECIFICATIONS

Input:

- Minimum Input Amplitude: 4 volts dc level shift from −8 volts dc to −4 volts dc.
- Maximum Input Voltage: Between −12 and zero volts dc.
- Maximum Reset Rate: 250 kc.
- Pulse Input: For optional operation with pulse inputs, a minimum positive-going 5-volt peak-to-peak pulse should be applied to pin 3 through a suitable capacitor and a 47,000-ohm resistor connected from pin 3 to pin 6.
- Input Impedance: Greater than 15,000 ohms (pin 2).

Output (pin 7):

- DC Level Shift: From a nominal −5 volts dc to −0.3 volts dc. The exact value of the most negative level is determined by the number of flip-flop loads. It is −5 volts dc unloaded and approximately −4 volts dc loaded with 15 flip-flops.
- Duration: From 1 microsecond minimum to dc.
- Rise Time: 0.5 microsecond nominally.
- Fall Time: 0.5 microsecond nominally.

Loading:

- Up to a maximum of 15 flip-flops.

Power Required:

- −12 volts dc at 3 ma quiescent; 7 ma during reset period. Pin 1 to be negative with respect to pin 6.
- Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	Normal input
3	Pulse input
4	Unused
5	Unused
6	12-volt common
7	Output
8	Unused
9	Case ground

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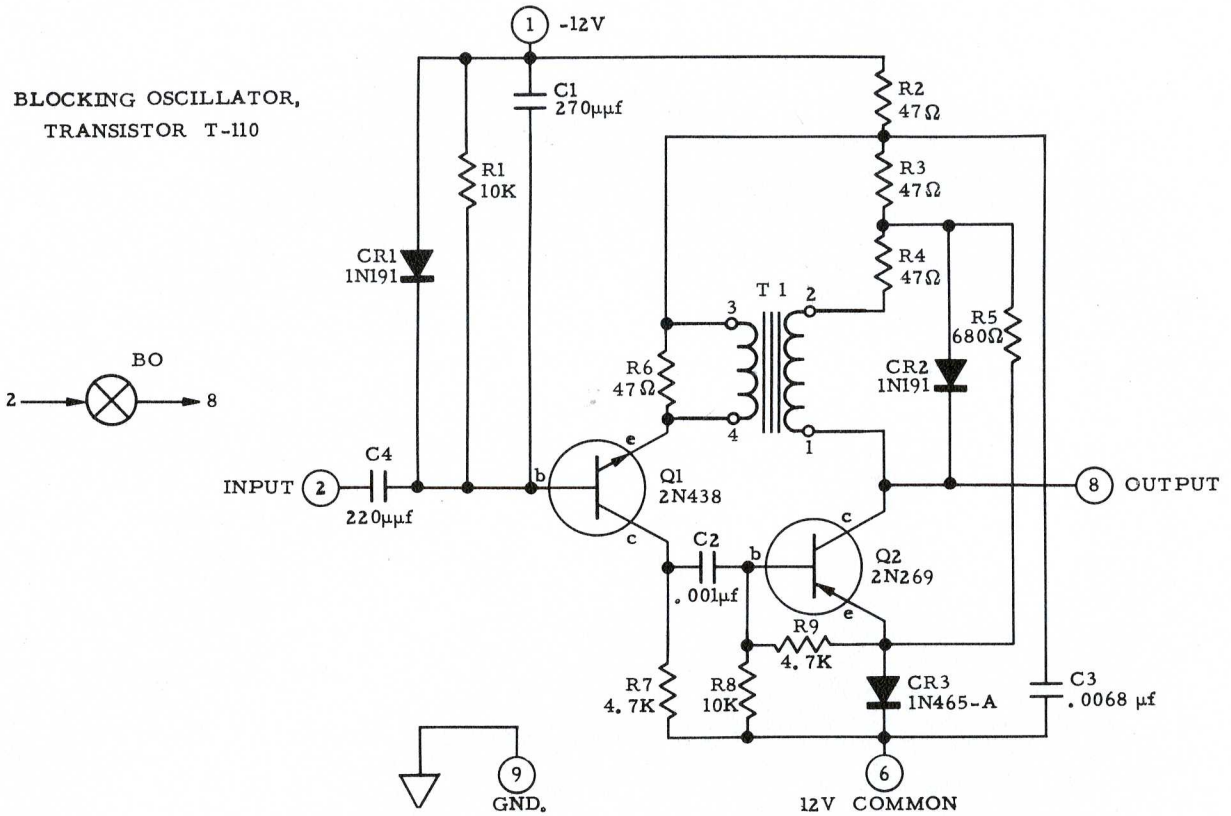
BLOCKING OSCILLATOR,
TRANSISTOR T-110



GENERAL

This is a Transistorized Blocking Oscillator assembly containing two germanium transistors in a monostable circuit. The purpose of this unit is to provide a sharp, standard pulse capable of driving a heavy load.

This assembly is contained in a cylindrical plug-in package which inserts in a standard 9-pin miniature tube socket.

ELECTRICAL SPECIFICATIONS

A. Input: (Pin #2)
   1. Signal Frequency Range: 0 to 250 kc.
   2. Trigger Input Amplitude: Circuit will <u>always</u> operate on any positive-going pulse of 5.5 volts or greater, at a rise time up to 1 μsec.
      Circuit will <u>not</u> trigger on any positive-going pulse of 1.5 volts or less, regardless of rise time.
   3. Maximum Trigger Input Amplitude: 9 volts peak.
   4. Rise Time: 0.1 μsec. to 1.0 μsec.
   5. Input Impedance: 220μμf capacitive, maximum.

B. Output: (Pin #8)
   1. Amplitude: 7.5 V to 8 V P-P unloaded, depending on frequency.
   2. Polarity: Positive.
   3. Output Levels: unloaded
      Upper Level, -3 VDC nominal.
      Lower Level, -10.5 VDC to -11 VDC depending on frequency.
   4. Rise Time: 0.1 μsec. to 0.8 μsec. depending on capacitive load.
   5. Duration: 1.0 μsec. nominal.
   6. Capacitive Load: Up to 20 paralleled Flip-Flop inputs.
   7. Resistive Load: 5KΩ to ground maximum.
      500Ω to -12 V maximum.

C. Power Requirements:
   1. -12 VDC at 12 ma quiescent, 55 ma peak. Pin #1 negative with respect to Pin #6.
   2. Supply Voltage Tolerance: ± 10%.

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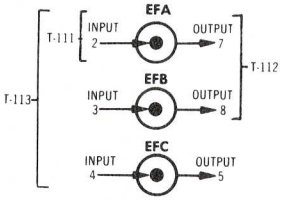
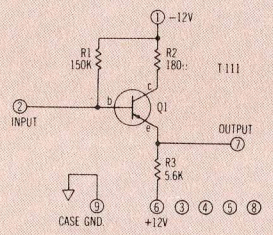
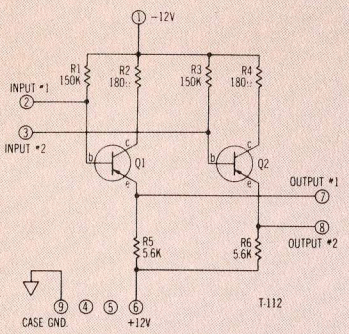
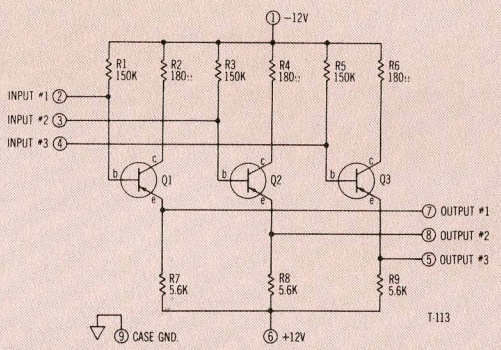
"T-SERIES"
Germanium
TRANSISTOR PLUG-IN CIRCUITS
PNP EMITTER FOLLOWERS



T-111, T-112, T-113







Note: Q1, Q2, Q3-type 2N414

CIRCUIT DESCRIPTION

The T-111, T-112, and T-113 are arrangements of the same basic PNP Emitter Follower. Circuit details and performance are identical. The T-111 contains a single emitter follower. The T-112 contains two independent emitter followers, while the T-113 contains three independent emitter followers.

This series of emitter followers is used to provide current gain and circuit isolation, as well as to increase the load-driving capacity of an input signal. Probably the most general application is for operating into dc logic.

The PNP Emitter Follower has a minimum output impedance for negative-going signals. If minimum output impedance is needed for positive-going signals, the NPN Emitter Followers, T-114, T-115, or T-116, should be considered.

ELECTRICAL SPECIFICATIONS

Input:

- Signal Frequency Range: 0 to 250 kc. (Frequency range can be extended to 500 kc with slightly reduced signal.)
- Signal Amplitude: The standard input is an 8-volt dc level shift within the range of −11 volts dc to −3 volts dc, such as from a flip-flop, one shot, etc. The maximum range is from zero volts to −12 volts dc.
- Input Impedance: Nominally 50,000 ohms under loaded conditions.
- Input Circuit Differentiation: Can be accomplished in a conventional fashion with a series capacitor and a resistor returned to a bias of proper value to establish the quiescent output voltage. Definite care should be taken to keep operating conditions within the maximum signal amplitude allowed.

Output:

- Amplitude: Equal to input signal. Level shift is ¼ volt in the positive direction.
- Rise Time: Not deteriorated by more than a nominal 0.2 microsecond referred to input.
- Output Impedance: 150 ohms for a negative-going signal; 5,600 ohms maximum for a positive-going signal.

Loading:

- Resistance: 3,300 ohms to ±12 volts, maximum resistive load for a signal shift of −3 to −11 volts dc.
- Capacitance: 600 $\mu\mu$f maximum capacity to ground, or three paralleled flip-flops. When operating into pure capacitive loads, connect a 5,600-ohm external resistor from output to +12-volt supply.

Power Required (each Emitter Follower):

+12 volts dc at 3.9 to 11 ma, and −12 volts dc at 3.9 to 11 ma, depending on load. Pin 1 to be 24 volts negative with respect to pin 6.

Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	T-111
1	−12 volts dc
2	Input
3	Unused
4	Unused
5	Unused
6	+12 volts dc
7	Output
8	Unused
9	Case ground

Pin No.	T-112
1	−12 volts dc
2	Input No. 1
3	Input No. 2
4	Unused
5	Unused
6	+12 volts dc
7	Output No. 1
8	Output No. 2
9	Case ground

Pin No.	T-113
1	−12 volts dc
2	Input No. 1
3	Input No. 2
4	Input No. 3
5	Output No. 3
6	+12 volts dc
7	Output No. 1
8	Output No. 2
9	Case ground

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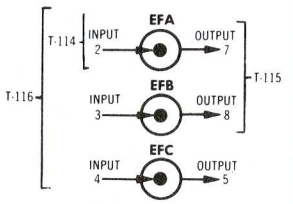
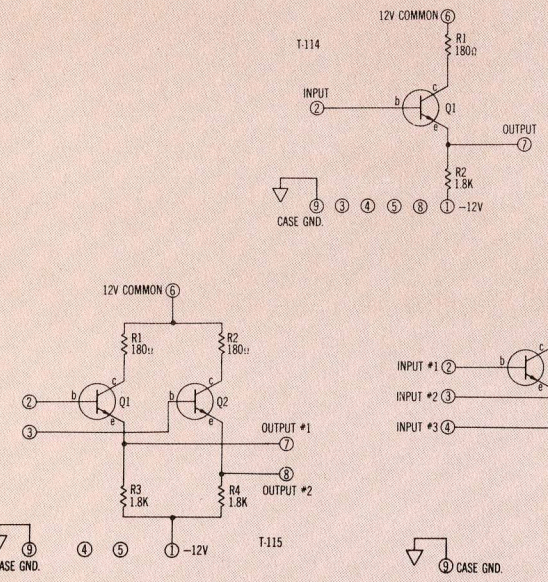
"T-SERIES"

Germanium TRANSISTOR PLUG-IN CIRCUITS

NPN EMITTER FOLLOWERS



T-114, T-115, T-116



Note: Q1, Q2, Q3 - type 2N438

CIRCUIT DESCRIPTION

The T-114, T-115, and T-116 are arrangements of the same basic NPN Emitter Follower. Circuit details and performance are identical. The T-114 contains a single emitter follower. The T-115 contains two independent emitter followers, while the T-116 contains three independent emitter followers.

This series of emitter followers is used to provide current gain and circuit isolation, as well as to increase the load-driving capacity of an input signal. Probably the most general application is for driving capacitive loads such as multiple flip-flops or one shots. NPN Emitter Followers should *not* be used for operating into dc logic.

The NPN Emitter Follower has a minimum output impedance for positive-going signals. If minimum output impedance is needed for negative-going signals, the PNP Emitter Followers, T-111, T-112, or T-113, should be considered.

ELECTRICAL SPECIFICATIONS

Input:

Signal Frequency Range: 0 to 250 kc. (Frequency range can be extended to 500 kc with slightly reduced signal.)

Signal Amplitude: The standard input is an 8-volt dc level shift within the range of −11 volts dc to −3 volts dc. The maximum range is from zero volts to −12 volts dc.

Input Impedance: Nominally 30,000 ohms under loaded conditions.

Input Circuit Differentiation: Can be accomplished in a conventional fashion with a series capacitor and a resistor returned to a bias of proper value to establish the quiescent output voltage. Definite care should be taken to keep operating conditions within the maximum signal amplitude allowed.

Output:

Amplitude: Equal to input signal. Level shift is ¼ volt in the negative direction.

Rise Time: Normally not deteriorated by more than 0.1 microsecond referred to input.

Output Impedance: 150 ohms for a positive-going signal; 1,800 ohms maximum for a negative-going signal.

Loading:

Either 600 $\mu\mu$f maximum capacity to ground or four flip-flops. (Greater capacitive loads may be imposed when correspondingly poorer rise times are allowable. Maximum should not exceed 5000 $\mu\mu$f.

Power Required: (each Emitter Follower):

−12 volts at 1 to 7 ma, depending on load. Pin 1 to be negative with respect to pin 6.

Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	T-114
1	−12 volts dc
2	Input
3	Unused
4	Unused
5	Unused
6	12-volt common
7	Output
8	Unused
9	Case ground

Pin No.	T-115
1	−12 volts dc
2	Input No. 1
3	Input No. 2
4	Unused
5	Unused
6	12-volt common
7	Output No. 1
8	Output No. 2
9	Case ground

Pin No.	T-116
1	−12 volts dc
2	Input No. 1
3	Input No. 2
4	Input No. 3
5	Output No. 3
6	12-volt common
7	Output No. 1
8	Output No. 2
9	Case ground

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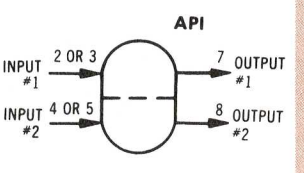
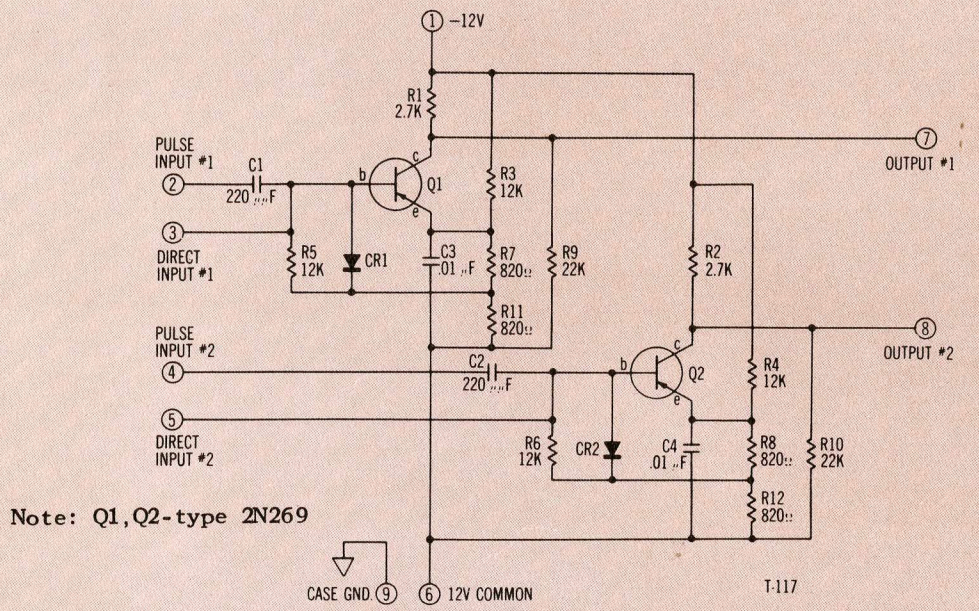
TRANSISTOR PLUG-IN CIRCUITS
PULSE INVERTER, DUAL



T-117



Note: Q1, Q2-type 2N269

CIRCUIT DESCRIPTION

The T-117 assembly contains two identical, independent Pulse Inverting Amplifiers. Each pulse inverter section produces a standard positive-going pulse of 1 to 2 microseconds duration for each negative-going input step. The input is shaped to produce an output of improved rise time and standard amplitude.

ELECTRICAL SPECIFICATIONS

Input (each Pulse Inverter section):

Amplitude:

a) Minimum input is a 5-volt negative pulse or step to pin 2 or 4 with a rise time of 1 microsecond.
b) Circuit will *not* respond to inputs of less than 1½ volts, regardless of rise time.

Rise Time (pin 2 or 4): Up to 1 microsecond at minimum input amplitude. More deteriorated rise times at correspondingly greater amplitudes may be regenerated.

Maximum Center Value Input Voltage (Quiescent Value):
±50 volts dc.

Maximum Operating Frequency: 250 kc.

Direct Input (pins 3 and 5): For signals of very poor rise time, use Direct Input with an external capacitor of suitable size.

Input Impedance: 220µµf capacitance (pins 2 and 4).

Output (each Pulse Inverter section):

Amplitude: 9 volts peak-to-peak (pins 7 and 8).

Polarity: Positive-going.

Output Levels: −11 volts dc and −2 volts dc nominal.

Rise Time: 0.4 microsecond nominal into a capacitive load of 470 µµf.

Duration: 1 to 2 microseconds, depending on input.

Loading:
Typical, up to 3 paralleled flip-flop inputs.

Power Required:
−12 volts dc at 5 ma. Pin 1 to be negative with respect to pin 6.
Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	Pulse input No. 1
3	Direct input No. 1
4	Pulse input No. 2
5	Direct input No.2
6	12-volt common
7	Output No. 1
8	Output No. 2
9	Case ground

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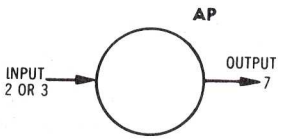
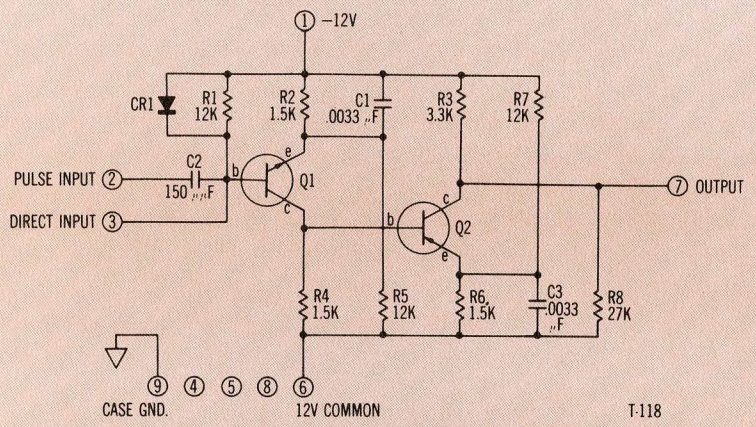
PULSE AMPLIFIER



T-118



Note: Q1-type 2N438; Q2-type 2N269

CIRCUIT DESCRIPTION

The T-118 is a Transistorized Pulse Amplifier used to produce standardized positive-going pulses with a duration of 0.5 to 1.0 microsecond and a sharp rise time. The input may be of deteriorated shape and low amplitude. The positive-going pulses result from an input of either a positive-going pulse or voltage step.

ELECTRICAL SPECIFICATIONS

Input:
- Amplitude:
  - a) Minimum input is a 4.7-volt positive pulse or step at 1 microsecond rise time (pin 2).
  - b) Circuit will *not* respond to inputs of less than 2.0 volts, regardless of rise time.
- Rise Time: From 0.2 to 1.0 microsecond.
- Maximum Operating Frequency: 250 kc.
- Direct Input (pin 3): For signals of very poor rise time, use Direct Input with an external capacitor of suitable size.
- Input Impedance: 150 μμf capacitance (pin 2).

Output:
- Amplitude: 8 volts peak-to-peak.
- Polarity: Positive-going.
- Output Levels: −11 volts dc and −3 volts dc nominal.
- Rise Time: 0.4 microsecond nominal loaded by flip-flops.
- Duration: 0.5 to 1.0 microsecond nominal.

Loading:
- Typical load is three flip-flops. For frequencies up to 125 kc loading may be four flip-flops.

Power Required:
- −12 volts dc at 2 ma quiescent, 10 ma peak. Pin 1 to be negative with respect to pin 6.
- Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin connections are arranged to permit convenient in-line wiring of power and ground connections.

Pin No.	
1	−12 volts dc
2	Pulse input
3	Direct input
4	Unused
5	Unused
6	12-volt common
7	Output
8	Unused
9	Case ground

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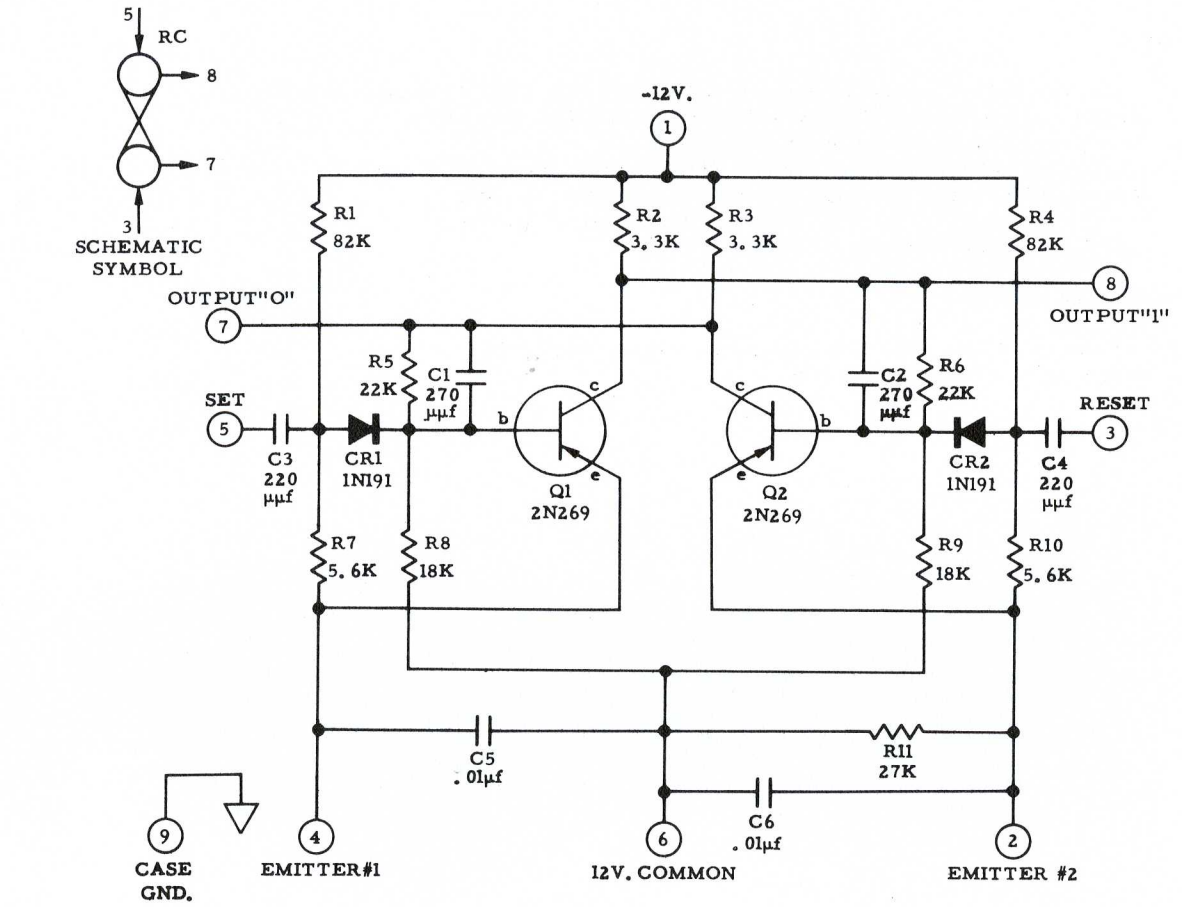
PLUG-IN CIRCUITS

RING COUNTER T-119



GENERAL

This unit is a transistorized ring counter element for assembly into ring counter and linear counter systems.

The circuit is specifically designed for unambiguous operation in counter applications. The circuit is basically a set-reset flip-flop with separate emitter connections made available for external connection to emitters of other Ring Counter units. Only one element in a ring counter configuration can be in the Binary "1" condition at any time. This feature makes it possible to assemble reliable counters of large numbers of digits.

By suitably combining these ring counter elements, counters of up to 200 digits are possible.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

ELECTRICAL SPECIFICATIONS

A. Reset Input: (Pin #3)

1. Signal Frequency Range: 0 to 250 kc.
2. Input Amplitude: Positive pulse of 6.5 volts minimum amplitude at 0.6 μsec. rise time. Ring counter will not respond to inputs of 1.5 volts or less, regardless of rise time.
3. Rise Time: 0.1 μsec. to 0.6 μsec.
4. Maximum Input Amplitude: 9 volts peak-to-peak.
5. Source: Reset input signals normally obtained from a pulse clock source such as Pulse Amplifier, Pulse Inverter, Blocking Oscillator, or NPN Emitter Follower.
6. Input Impedance: 220 μμfd. capacitive, maximum.

OVER

B. Set Input: (Pin #5)

1. Signal Frequency Range: 0 to 125 kc.
2. Input Amplitude: Square wave or positive pulse of 6.5 volts minimum amplitude at 0.8 μsec. rise time. Ring Counter will not respond to inputs of 1.5 volts or less regardless of rise time.
3. Rise Time: 0.1 μsec. to 0.6 μsec.
4. Maximum Input Amplitude: 9 volts peak-to-peak.
5. Source: The set input signal is normally supplied from the output of another Ring Counter element, or from a Flip-Flop.
6. Input Impedance: 220 μμfd. capacitive, maximum.

C. Output:

1. Type: 2 outputs of opposite polarity; "0" output, (Pin #7); "1" output, (Pin #8).
2. Amplitude: 8 V level shift from -11 V DC to -3 V DC, nominally.
3. Rise Time: 0.6 μsec. nominally under load.
4. Loads: Typical load is 1 set input to Ring Counter, plus 1 FF T input.
   Maximum Resistive Loading: .2 ma. to a positive source.
   1.0 ma. to a negative source.
5. Fall Time: Approximately 1.5 μsec.

D. Power Requirements:

1. -12 volts at 4 ma. Pin #1 negative with respect to Pin #6.
2. Supply voltage tolerance: ± 10%

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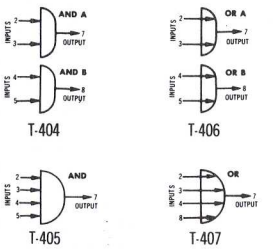
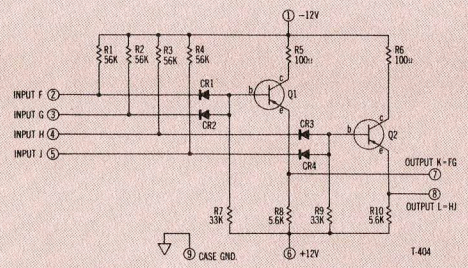
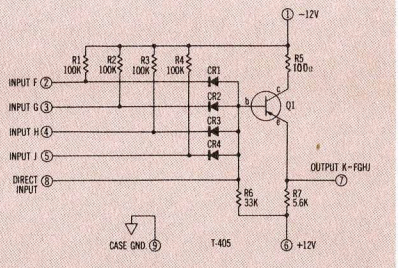
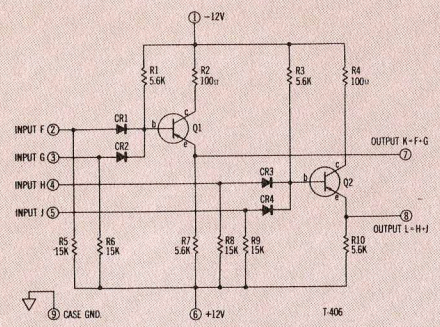
DC LOGIC



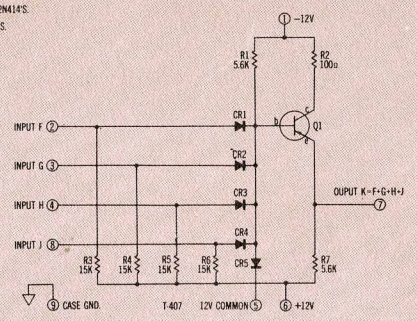
T-404, T-405, T-406, T-407







ALL TRANSISTORS ARE 2N414'S.
ALL DIODES ARE 1N191'S.



GENERAL

This group of logic circuits for the T-Series system has been developed on the principle that it contains an integral emitter follower on the output of each "And" or "Or" gate. This provides superior isolation and the ability to cascade logic in any combination. For example, the usual limitation that "Or" circuits cannot drive "And" circuits is overcome in this system.

The cost of adding the emitter follower to the logic is very small and can save substantial amounts in space and cost when compared to the use of external emitter followers to accomplish the same purpose.

Normally, our logic circuits are packaged in our standard 9-pin container. Complex logic, requiring more pin connections, will be produced with a 13-pin header with socket (T-906) supplied. The T-906 is a standard, generally available 14-pin miniature socket with pin 10 blocked to provide an orientation key.

CIRCUIT DESCRIPTION

Since individual needs for different logic equations vary widely, we believe it to be most efficient to furnish logic circuits to fit specific needs. Because of the basic simplicity of the theory and circuits involved, and because of our package design, we can produce units tailored to your specific needs at a cost favorably comparable to the cost of producing an equal number of standard items.

We are always very glad to produce single units or small quantities of new or special logic circuits. On initial small quantities, the price of the logic should be within 20% of a standard unit of roughly the same complexity, using components of the same general cost. If you do not find the circuits you need among the few examples shown here, please order or let us quote on the precise circuit you require. We can work either from schematic or logic formula.

Four standard D-C Logic circuits are shown here as typical examples:

Cat. No.	Circuit(s)	Formula
T-404	Two: 2-input "And"	K = FG, L = HJ
T-405	One: 4-input "And"	K = FGHJ
T-406	Two: 2-input "Or"	K = F + G, L = H + J
T-407	One: 4-input "Or"	K = F + G + H + J

ELECTRICAL SPECIFICATIONS

(These specifications apply to all units, unless otherwise indicated.)

Input:
- Frequency Range: 0 to 250 kc.
- Standard Signal Input: −3 to −11 volts.
- Input Impedance: Function of load and transistor beta.

Output:
- Amplitude: Essentially equal to input signal.
- Level Shift: T-404 and T-405, approximately +0.4 volt. T-406 and T-407, approximately +0.1 volt.
- Rise Time (Unloaded): Positive-going signal essentially equal to input signal rise time.
- Rise Time Degradation: Nominally 0.2 microsecond referred to input.

Loading:
- Maximum resistive load is determined by input level and allowable transistor dissipation at 65°C. For a typical signal input of −3 volts to −11 volts, maximum resistive load is 3,300 ohms to either plus or minus 12 volts.

Power Required:
- +12 volts dc at 3.9 to 11 ma, depending on load.
- −12 volts dc at 3.9 to 11 ma, depending on load.
- Pin 1 to be 24 volts negative with respect to pin 6.
- Supply voltage tolerance ±10%.

PIN CONNECTIONS

Pin No.	T-404 & T-406	T-405
1	−12 volts dc	−12 volts dc
2	Input F	Input F
3	Input G	Input G
4	Input H	Input H
5	Input J	Input J
6	+12 volts dc	+12 volts dc
7	Output K	Output K
8	Output L	Direct input
9	Case ground	Case ground

Pin No.	T-407
1	−12 volts dc
2	Input F
3	Input G
4	Input H
5	12-volt common
6	+12 volts dc
7	Output K
8	Input J
9	Case ground

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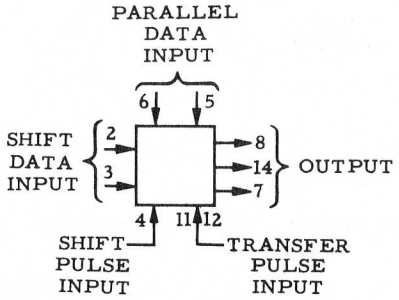
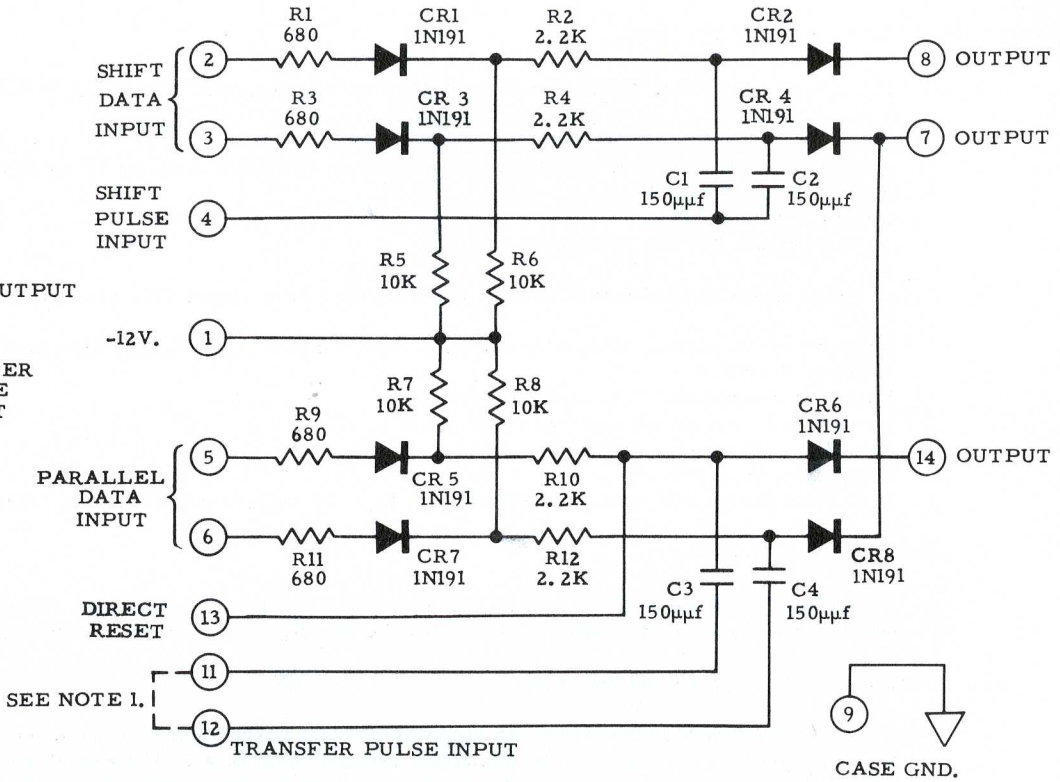
TRANSISTOR

PLUG-IN CIRCUITS

SHIFT REGISTER LOGIC,
DIODE T-600



SCHEMATIC SYMBOL



NOTES: 1. JUMPER USED WHEN DUAL INPUT PARALLEL DATA APPLIED.
2. KEYWAY LOCATION - PIN 10. (OMITTED FROM HEADER)

GENERAL

This unit is a Shift Register Logic element. It is used in conjunction with the T-102 Flip-Flop for assembly into shift register systems.

The circuit of this unit is a configuration of diode pulse gates arranged to transfer stored data from input flip-flops to an output flip-flop. Four pulse "And" gates and two pulse "Or" gates are contained in the circuit. Each pulse "And" gate permits an applied clock pulse to be transmitted through the gate when its control input signal is in the binary "1" state. The "Or" gates are pulse mixers.

A shift register system is composed of a series of alternate T-600 SR and T-102 FF units, one pair for each digit. Each flip-flop output supplies the control inputs (shift data input) for its associated shift register element. The outputs of each Shift Register element are applied to the set and reset base inputs of the succeeding flip-flop. Every applied clock shift pulse is gated to either the R or S base input of the succeeding flip-flop, depending on the state of the preceding flip-flop. In this way, data is shifted serially from digit to digit through the shift register.

Provision is made for parallel data transfer from a storage flip-flop in a second register. The circuitry for accomplishing this parallel read-in of data is identical to that used for shifting.

Simultaneous resetting of all shift register flip-flops may be accomplished by employing a Reset Generator T-106. This method of resetting clears the register in one clock time.

Four fundamental types of shift register configurations are possible with this unit. The first three differ mainly in the method of entering parallel data, and of clearing the shift register; the fourth is a special application:

(a) Parallel data can be entered into the shift register by gating both outputs of the storage flip-flop. The corresponding shift register flip-flop is forced into the same state by set-reset triggering. Clearing of the shift register is not required since data is entered into the register regardless of the prior state of the shift register flip-flop.

OVER

(b) Parallel data is entered by setting the shift register flip-flops. This method requires that the shift register be initially cleared before entering new data. Clearing is accomplished by shifting "zeros" through the register, which operation leaves all flip-flops in the reset state.

(c) This configuration is identical to "b" except that a Reset Generator T-109, is employed for clearing the register. All Flip-Flops are simultaneously reset.

(d) This Shift Register element is also used for Gray-to-Binary code conversion. Provision is made for this application by rearrangement of the internal gate circuitry of the Shift Register Logic, and by operating the flip-flops in R-S and T modes.

ELECTRICAL SPECIFICATIONS

A. Control Inputs: Shift Data Input (Pin #2 and Pin #3), and Parallel Data Input (Pin #5 and Pin #6)

1. Type: D.C. Level shift as obtained from flip-flop outputs.
2. Amplitude: Level shift of 8 volts amplitude, from -11 volts D.C. to -3 volts D.C., nominal.
3. Rise Time: 0.2 to 1.0 μsec.
4. Frequency: 0 to 125 kc.
5. Input Current: 0.9 ma to negative voltage.

B. Pulse Inputs: Shift Pulse Input (Pin #4), and Transfer Pulse Input (Pin #11 and Pin #12)

1. Type: Positive pulse. Normally obtained from a Pulse Amplifier, Pulse Inverter, Blocking Oscillator, or NPN Emitter Follower.
2. Minimum Amplitude: 7.5 volts peak-to-peak.
3. Maximum Amplitude: 9 volts peak-to-peak.
4. Rise Time: 0.4 μsec. or better.
5. Frequency: 0 to 250 kc.
6. Input Impedance: 300 μμfd. capacitive (Pin #4); 150 μμfd. capacitive (Pin #11); 150 μμfd. capacitive (Pin #12).

C. Reset Input: (Pin #13)

1. When Reset operation is used, a Reset Generator T-109 is connected to Pin #13. A resistor should be connected from Pin 13 to 12 V common. Value = $\frac{10,000}{n}$ where n is the number of SR elements.

D. Output: (Pin #7, Pin #8 and Pin #14)

1. Type: Three output connections for applying set and reset signals to base inputs of a T-102 Flip-Flop and one output for applying trigger signals into the direct trigger input of a T-102 Flip-Flop. Pulse signals are present on either Pin #7 or Pin #8. Pin #14 is used for Gray-to-Binary conversion only. For all other shift register applications Pin #14 is jumpered to Pin #8.

2. Polarity: Positive pulse.
3. Minimum Amplitude, Loaded: 2 volt pulse, level shift from -3.5 volts D.C. to -1.5 volts D.C.
4. Rise Time: Essentially equal to pulse input rise time (0.4 μsec. or better).
5. Duration: Nominally 0.75 μsec.
6. Load: Typical load is a direct base input of T-102 Flip-Flop or a direct trigger input of T-102 Flip-Flop.

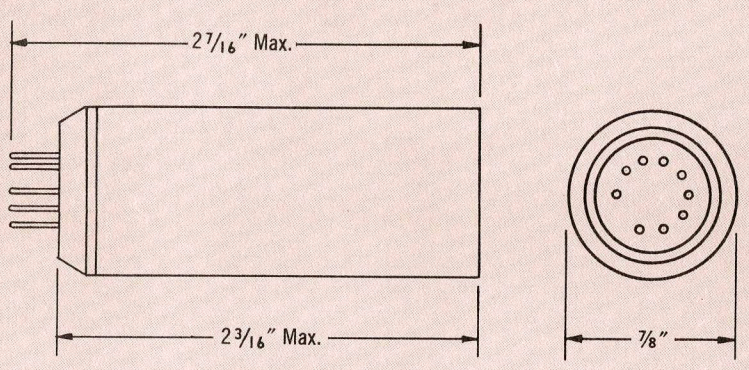
E. Power Requirements:

1. -12 volts at 1.8 ma. maximum. Pin #1 negative with respect to the 12 V common.
2. Supply voltage tolerance $\pm$ 10%.

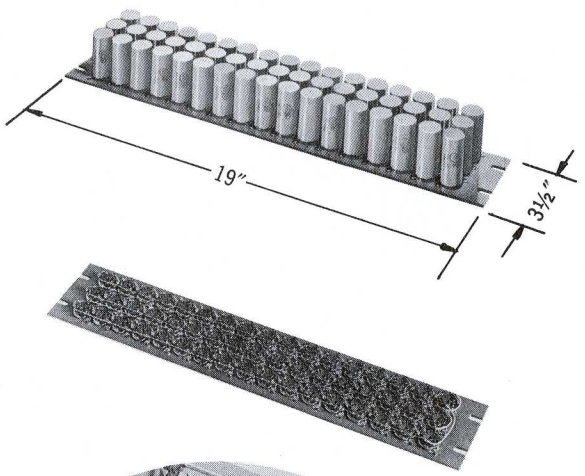
ENGINEERED ELECTRONICS COMPANY
506 EAST FIRST STREET • SANTA ANA, CALIFORNIA

"T-SERIES"
Germanium
TRANSISTOR PLUG-IN CIRCUITS

PHYSICAL SPECIFICATIONS



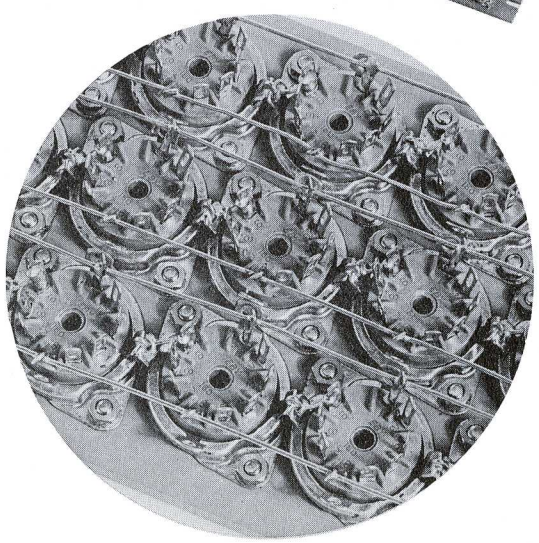
Maximum compactness is achieved by mounting units on 1-inch centers, as shown in this view of a standard 19" x 3½" panel, which contains a total of 51 "T-Series" circuits.



EECO "T-Series" Germanium Transistor Plug-in Circuit units are designed with compactness and reliable performance in mind. In the selection of parts and in the assembly techniques, every effort is made to maintain the highest quality of construction.

PHYSICAL SPECIFICATIONS:

Body: ⅞-inch diameter.
Seated height: 2 3/16 inches, maximum.
Over-all height 2 7/16 inches, maximum.
Mounting: On 1-inch centers, minimum.
Socket: Standard nine-pin miniature.
Weight: Less than 1 ounce.
Temperature Range: −45°C to +65°C.
Repairability: Case can be opened without special tools and without damage to the unit.
Sealing: Totally enclosed, using J-slot lock and locking ring.
Holddown: Will accept standard Jan 2⅜-inch tube shield and various other standard miniature tube-type holddown devices.
Pin Connections: Arranged to permit convenient in-line wiring of power and ground connections.
Finish: Gray baked enamel.



Rear view of panel, showing detail of convenient in-line wiring of power and ground connections made possible when sockets are consistently oriented to take advantage of standard arrangement of pin connections.

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OF CALIFORNIA)

TELEPHONE
Kimberley 7-5651

506 EAST FIRST STREET
SANTA ANA, CALIFORNIA

EECO "T-SERIES" *Germanium* TRANSISTOR PLUG-IN CIRCUITS

Prices effective May 1, 1958 and
subject to change without notice.

	1 - 9	10 - 24	25 - 49	50 - 99	100-199	200-499
T-104 Multivibrator	$ 32.25	$ 29.75	$ 27.95	$ 26.95	$ 26.15	$ 25.80
T-108 Linear Amplifier	43.10	39.60	36.25	34.15	32.05	31.45
T-110 Blocking Oscillator	54.35	49.35	43.20	41.50	37.80	37.15
T-119 Ring Counter	36.65	33.70	31.65	30.50	29.75	29.20
T-408 Pulse "And" Gate, dual	27.30	25.20	23.00	20.75	20.25	19.80
T-410 Pulse "And" Gate, dual	36.80	34.00	31.15	28.65	27.95	27.25
T-411 Pulse "And" Gate, multiple	46.40	42.75	39.45	38.20	37.00	36.40
T-412 Pulse Mixer Amplifier, multiple	47.75	44.00	40.50	39.20	38.15	37.40
T-600 Shift Register Logic diode	40.35	37.20	34.95	33.95	33.15	32.50
T-601 Pulse "And" Gate, multiple	65.90	60.75	55.75	53.75	51.75	50.35
T-602 Pulse Mixer Amplifier, multiple	66.60	61.35	56.20	54.40	52.85	51.75

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EECO "T-SERIES" *Germanium* TRANSISTOR PLUG-IN CIRCUITS

ADVANCE PRICE LIST

T-SERIES GERMANIUM PLUG-IN CIRCUITS
(Effective December 10, 1957)

	1-9	10-24	25-49	50-99	100-199	200-499
T-101 Flip Flop (RST)	42.85	39.50	37.10	36.10	35.20	34.65
T-102 Flip Flop (T)	33.70	31.10	29.20	28.40	27.75	27.35
T-103 Flip Flop (RS)	33.15	30.55	28.65	27.90	27.20	26.80
T-105 One Shot	34.75	32.05	30.15	29.30	28.60	27.95
T-106 Squaring Amplifier	26.10	24.05	22.55	21.95	21.40	21.05
T-109 Reset Generator	23.85	22.05	20.75	20.15	19.70	19.35
T-111 Emitter Follower, PNP	10.70	9.85	9.25	8.95	8.75	8.65
T-112 Emitter Follower, PNP, dual	15.85	14.60	13.70	13.35	13.00	12.70
T-113 Emitter Follower, PNP, triple	21.35	19.70	18.50	18.00	17.30	16.85
T-114 Emitter Follower, NPN	12.05	11.15	10.45	10.20	9.95	9.80
T-115 Emitter Follower, NPN dual	17.40	16.10	15.15	14.75	14.40	14.10
T-116 Emitter Follower, NPN, triple	23.40	21.70	20.45	19.90	19.30	18.90
T-117 Pulse Inverter	31.50	29.10	27.35	26.55	25.85	25.25
T-118 Amplifier	23.75	21.95	20.55	19.95	19.40	19.00
T-404 DC "AND" Gate (2 input), dual	30.95	28.60	26.30	25.60	24.90	24.30
T-405 DC "AND" Gate (4 input)	24.95	23.05	21.25	20.70	19.95	19.65
T-406 DC "OR" Gate (2 input), dual	30.95	28.60	26.30	25.60	24.90	24.30
T-407 DC "OR" Gate (4 input)	24.95	23.05	21.25	20.70	19.95	19.65

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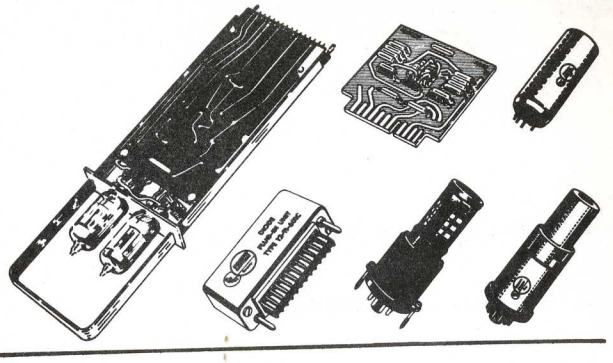


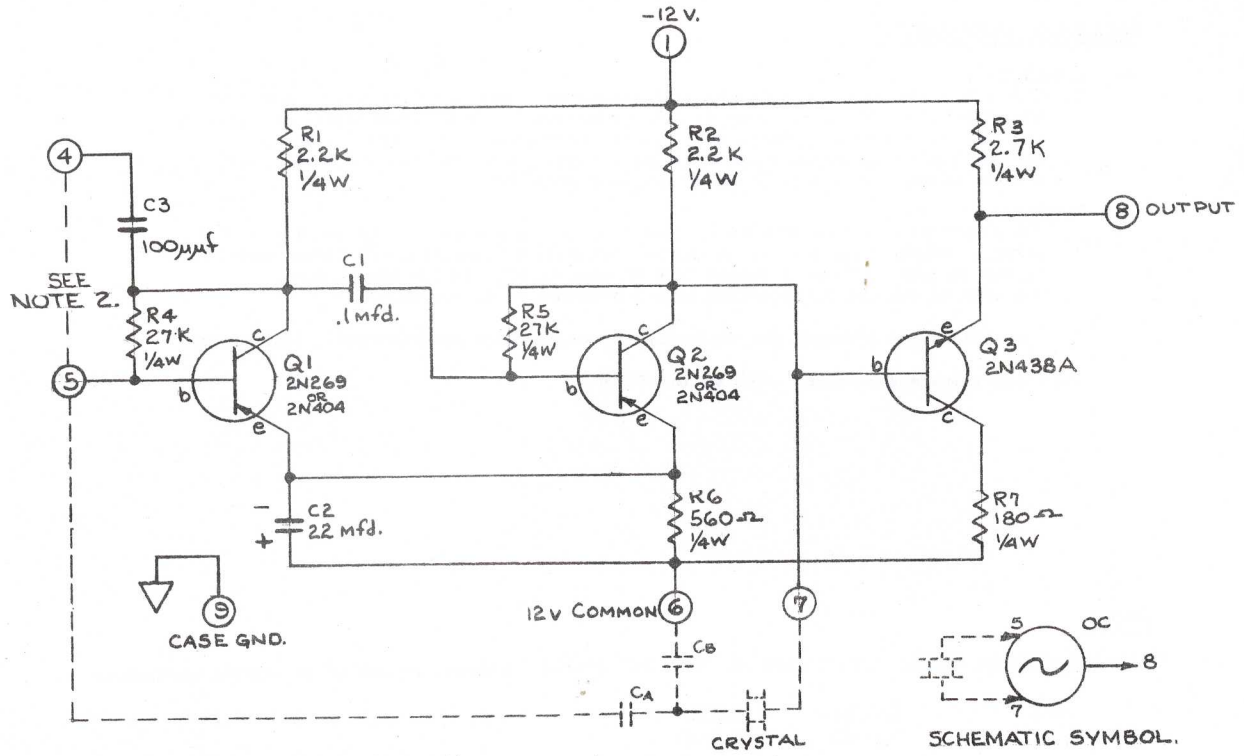
SUPPLEMENT TO CATALOG TR-758A

Effective 1 June 1959

The following listed circuits will be included in the forthcoming re-issue of our standard catalog. In the interim the specifications and schematics attached will serve as a supplement to the existing transistorized catalog TR-758A. The circuits listed below are standard catalog items and are stocked for immediate delivery.

	1-9	10-24	25-49	50-99	100-199	200-499
T-107 Crystal Oscillator (10-75 KC)	32.25	29.75	27.95	26.95	26.15	25.80
T-120 Relay Driver	27.40	25.45	24.00	21.85	18.95	18.70
T-121 Relay Driver	42.80	40.00	37.85	35.40	27.15	26.75
T-123 Regulator	19.05	17.75	16.75	16.35	13.60	13.40
T-127 Crystal Oscillator (75-250 KC)	38.25	35.40	33.35	32.50	31.70	31.25
T-128 Relay Driver (0-24 V)	24.90	23.05	21.75	19.65	17.70	17.45
T-129 Reset Generator	23.85	22.05	20.75	20.15	19.70	19.35
T-421 Two-Input "Exclusively Or" Gate	21.55	19.85	18.65	18.10	17.65	17.40
T-423 Dual two-input "Exclusively Or" Gate	36.75	33.80	31.75	30.90	30.15	29.70
T-424 Half Adder Subtractor	34.95	32.15	30.15	29.30	28.60	28.20
T-605 Shift Register Flip Flop	43.00	39.55	37.10	36.10	35.20	34.70
T-606 Shift Register Flip Flop	53.05	48.75	45.65	44.40	43.30	42.70
T-607 Triple, two-input Buffered "AND" Gate	24.80	22.90	21.45	20.90	20.40	20.15
T-608 Dual, three-input Buffered "AND" Gate	21.95	20.20	19.00	18.50	18.05	17.85
T-609 Dual, four-input Buffered "AND" Gate	25.80	23.80	22.35	21.75	21.25	20.95
T-610 Shift Register Flip Flop	46.70	42.95	40.30	39.15	38.20	37.70
T-612 Triple Pulse Gate	40.50	37.50	31.40	30.55	29.70	28.15
T-620 Three-input "AND" Circuit	33.10	30.60	28.80	27.90	27.20	26.80

	1-9	10-24	25-49	50-99	100-199	200-499
R-121 Miniature Minisig	7.55	7.10	6.75	6.75	6.75	6.60
R-221 Miniature Minisig	7.55	7.10	6.75	6.75	6.75	6.60
R-441 Germanium Incandescent Minisig	13.40	12.55	11.90	11.90	11.90	11.60



NOTE: 1. C_A & C_B USED TO TRIM FREQ ±.001%
SEE TABLE OF VALUES ZA-95491,
IF NO TRIM IS REQ. CONNECT CRYSTAL
BETWEEN PINS 5 & 7.
2. FOR 10KC TO 45KC, JUMPER PIN
4 TO PIN 5.
3. CASE OF Q3 TO BE INSULATED

SCHEMATIC, CRYSTAL OSC. T-107

I. GENERAL

This is a transistorized unit containing two germanium PNP transistors in a two stage saturated feedback amplifier and one germanium NPN transistor connected in emitter follower configuration. The output is a square wave at the crystal resonant frequency. Units are normally supplied without crystals, but may be supplied with crystals cut to specific frequencies. For maximum stability an oven may be supplied in which is mounted both the unit and the crystal.

The crystal is used in the series resonance mode for maximum stability. The crystal acts as the coupling impedance between the output of the second stage and the input to the first stage. Since a full 360° phase shift occurs through two cascaded common emitter transistor amplifiers, the circuit will oscillate at a frequency which experiences neither phase shift nor appreciable attenuation through the crystal. This frequency is the series resonant frequency of the crystal. The T-107 covers the frequency range of 10 kcs. to 75 kcs.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket. The crystal is connected externally. It is recommended that the crystal be mounted along side the electronic assembly in order to reduce shunt capacitance between the crystal leads.

II. ELECTRICAL SPECIFICATIONS

A. Output:
1. Frequency Range: 10 kcs. to 75 kcs. (For 10 kcs. to 45 kcs., jumper pin 4 to pin 5.)
2. Amplitude: 8 volts peak to peak, from -11 volts to -3 volts with respect to pin 6.
3. Stability: Frequency ±.005%, Amplitude ±10%. (Frequency Stability ±.0005% with crystal and electronic unit in oven.)
4. Output Impedance: 800 ohms.
5. Rise Time: .1 to 1.0 μsec.
6. Frequency Trimming: ±.001% of nominal crystal frequency. See Chart I.
7. Maximum DC Load: 2.7K to -12 V (at 71° C.).

B. Power Requirements:
1. -12 volts D.C. at 7.0 ma.
(800 ohm AC load)
2. Supply Voltage Tolerance: ± 10%.

MECHANICAL SPECIFICATIONS

A. Dimensions:
   1. The electronic unit (less crystal) is contained within a cylindrical package of 7/8 inch diameter by 2-7/16 inches long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.
   2. An oven can be purchased which contains a 9-pin socket for the electronic unit and a 2-pin socket for a type MC-6A or MC-13A crystal holder.

B. Mounting:
   1. The electronic unit is mounted by inserting into a standard 9-pin miniature tube socket. Where mechanical retention is required, a standard 2-3/8 inches noval tube shield is used. Either a J-slot type or snap-on type shield may be used.
   2. The oven is mounted by inserting into a standard octal socket.

C. Pin connections are arranged for minimum shunt capacitance across crystal connections.

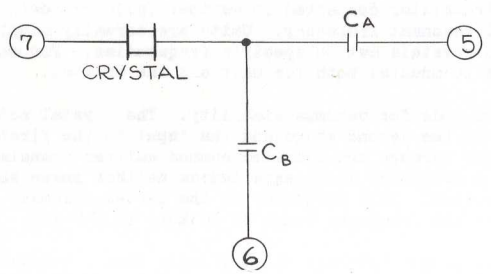
D. Operating Temperature Range: -54° C. to +71° C.

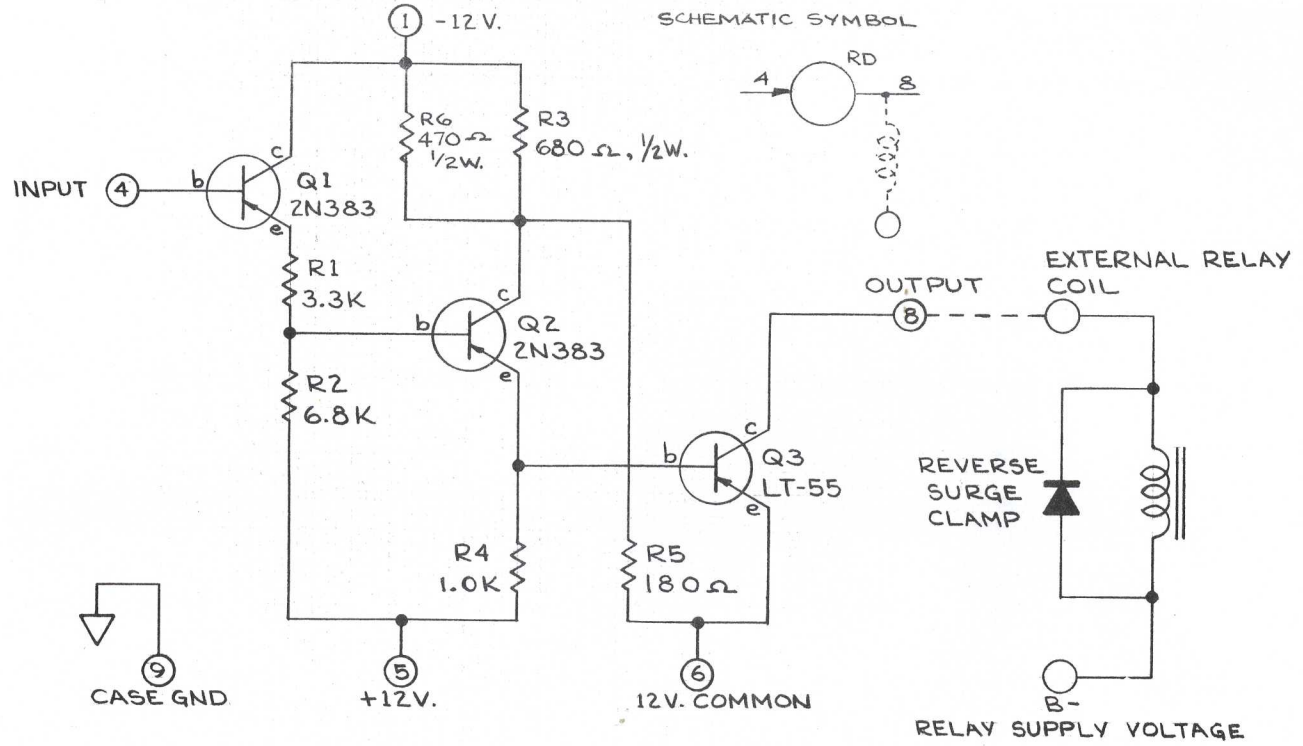
CHART I

FREQUENCY TRIMMING TABLE: CAPACITANCE VS. FREQUENCY CHANGE (typical, depending on crystal parameters).

ΔF (10^{-4}%)	Series C_A ($\mu\mu f$)	Shunt C_B ($\mu\mu f$)
+10	170	0
+5	400	0
+2	700	0
0	Jumper	0
-2	Jumper	160
-5	Jumper	300
-10	Jumper	500

C_A or C_B is added externally as indicated in the sketch below:

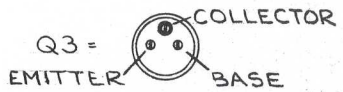




0 TO 48V. RELAY DRIVER T-120

2. ALL RESISTORS ARE 1/4W.
1. Q2 REQUIRES BIRTCHER RADIATOR No. 3AL-635.

NOTES, UNLESS OTHERWISE SPECIFIED:



I. GENERAL

This unit is a transistorized relay driver containing three germanium transistors. The purpose is to provide sufficient power to operate most of the general purpose relays now available. It may be operated directly from the T-Series digital units (Flip-Flop, One Shot, Squaring Circuits).

The assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:
1. Signal Frequency Range: 0 - 1 kc (for 400 ma resistive load). Max frequency with relay load depends on relay capabilities.
2. DC Signal Level to Actuate Relay: -11 V nominal.
3. DC Signal Level to Release Relay: -3 V nominal.
4. Input Impedance: 90 kΩ minimum.

B. Output:
1. Maximum output current available is dependant on the relay voltage used. See Chart I.
2. Absolute Maximum Output Current: 400 ma.
3. The relay driver must be protected against reverse surge voltages generated by the relay. Diode clamping may be used across the relay.

C. Power Required:
1. B+ +12V ±10% at 14 ma.
2. B- -12V ±10% at 30 ma to 45 ma, exclusive of relay current.
3. Relay Coil Supply Voltage: -48V absolute maximum.

III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot or a snap-on type shield may be used.

C. Pin connections are so arrangedthat power and grounds may be in-line wired.

D. Operating Temperature Range: -54° C. to +65° C. (may be operated at +71° C. for relay voltages up to 40V).

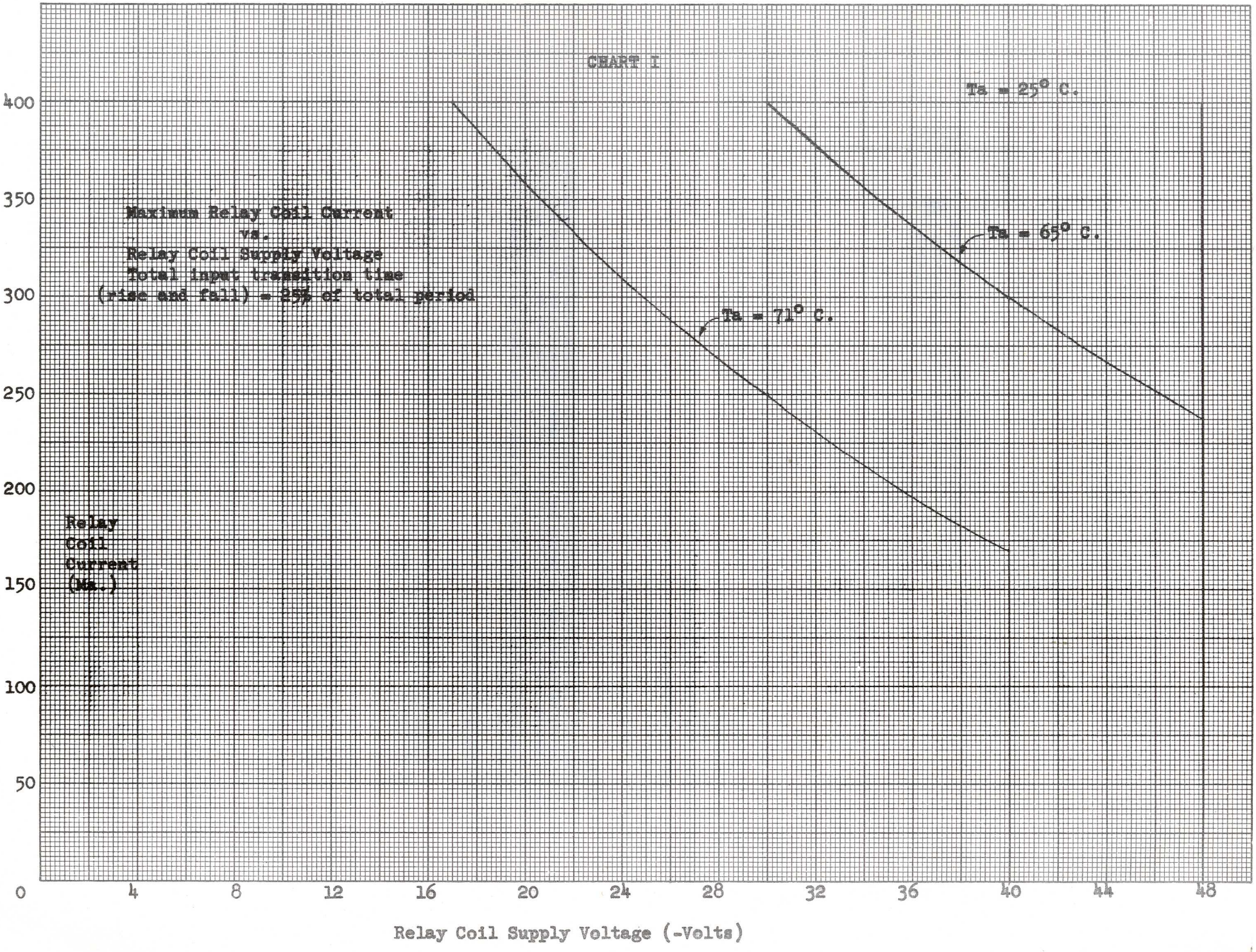
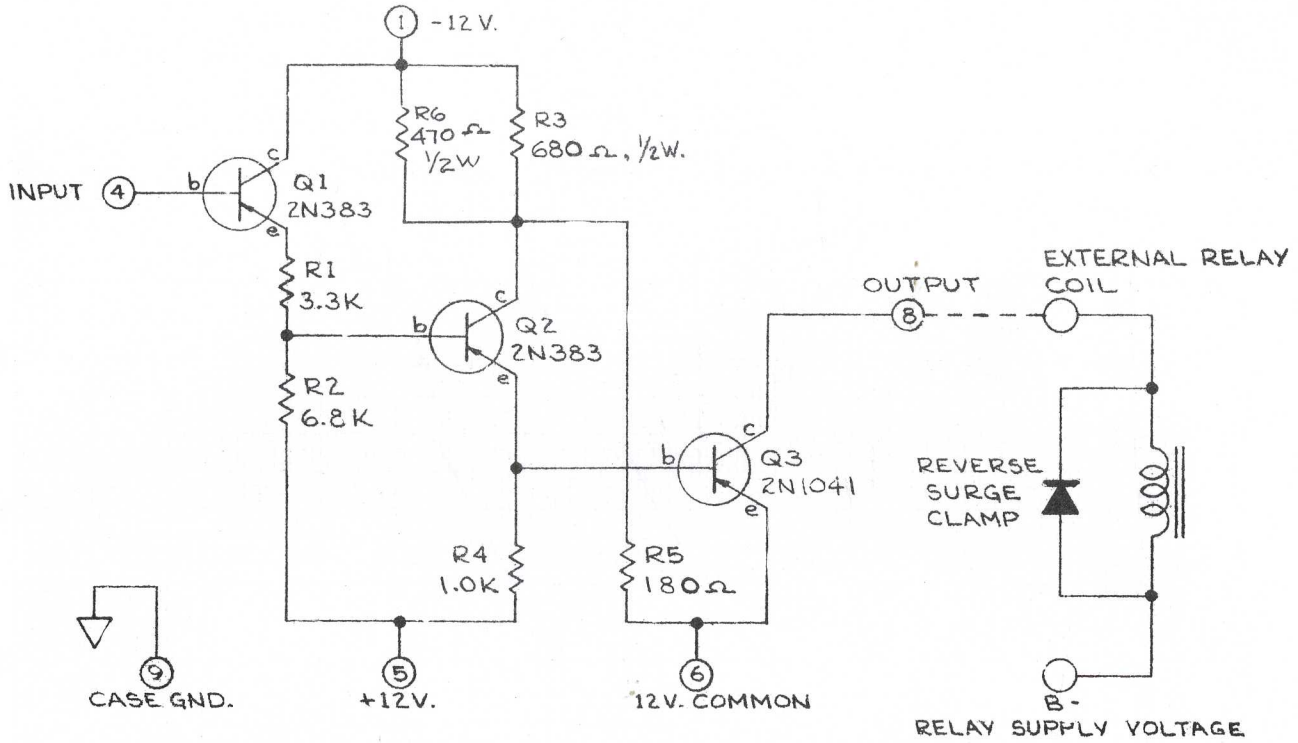


CHART I
Maximum Relay Coil Current
vs.
Relay Coil Supply Voltage
Total input transition time
(rise and fall) = 25% of total period
Ta = 25° C.
Ta = 65° C.
Ta = 71° C.
Relay
Coil
Current
(Ma.)
400
350
300
250
200
150
100
50
0
4
8
12
16
20
24
28
32
36
40
44
48
Relay Coil Supply Voltage (-Volts)



SCHEMATIC, 0-90v. RELAY DRIVER T-121

NOTES, UNLESS OTHERWISE SPECIFIED:

1. Q2&3 REQUIRE BIRTCHER RADIATORS No. 3AL-635.
2. ALL RESISTORS ARE 1/4 W.

I. GENERAL

This unit is a transistorized relay driver containing three germanium transistors. The purpose is to provide sufficient power to operate most of the general purpose relays now available. It may be operated directly from the T-Series digital units (Flip-Flop, One Shot, Squaring Circuits).

The assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:
1. Signal Frequency Range: 0 - 1 kc (for 400 ma resistive load). Max frequency with relay load depends on relay capabilities.
2. DC Signal Level to Actuate Relay: -11 V nominal.
3. DC Signal Level to Release Relay: -3 V nominal.
4. Input Impedance: 90 kΩ minimum.

B. Output:
1. Maximum output current available is dependant on the relay voltage used. See Chart I.
2. Absolute Maximum Output Current: 500 ma.
3. The relay driver must be protected against reverse surge voltages generated by the relay. Diode clamping may be used across the relay.

C. Power Required:
1. B+ +12V ±10% at 14 ma.
2. B- -12V ±10% at 30 ma to 45 ma, exclusive of relay current.
3. Relay Coil Supply Voltage: -90V absolute maximum.

III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot on a snap-on type shield may be used.

C. Pin connections are so arranged that power and grounds may be in-line wired.

D. Operating Temperature Range: -54° C. to +71° C.

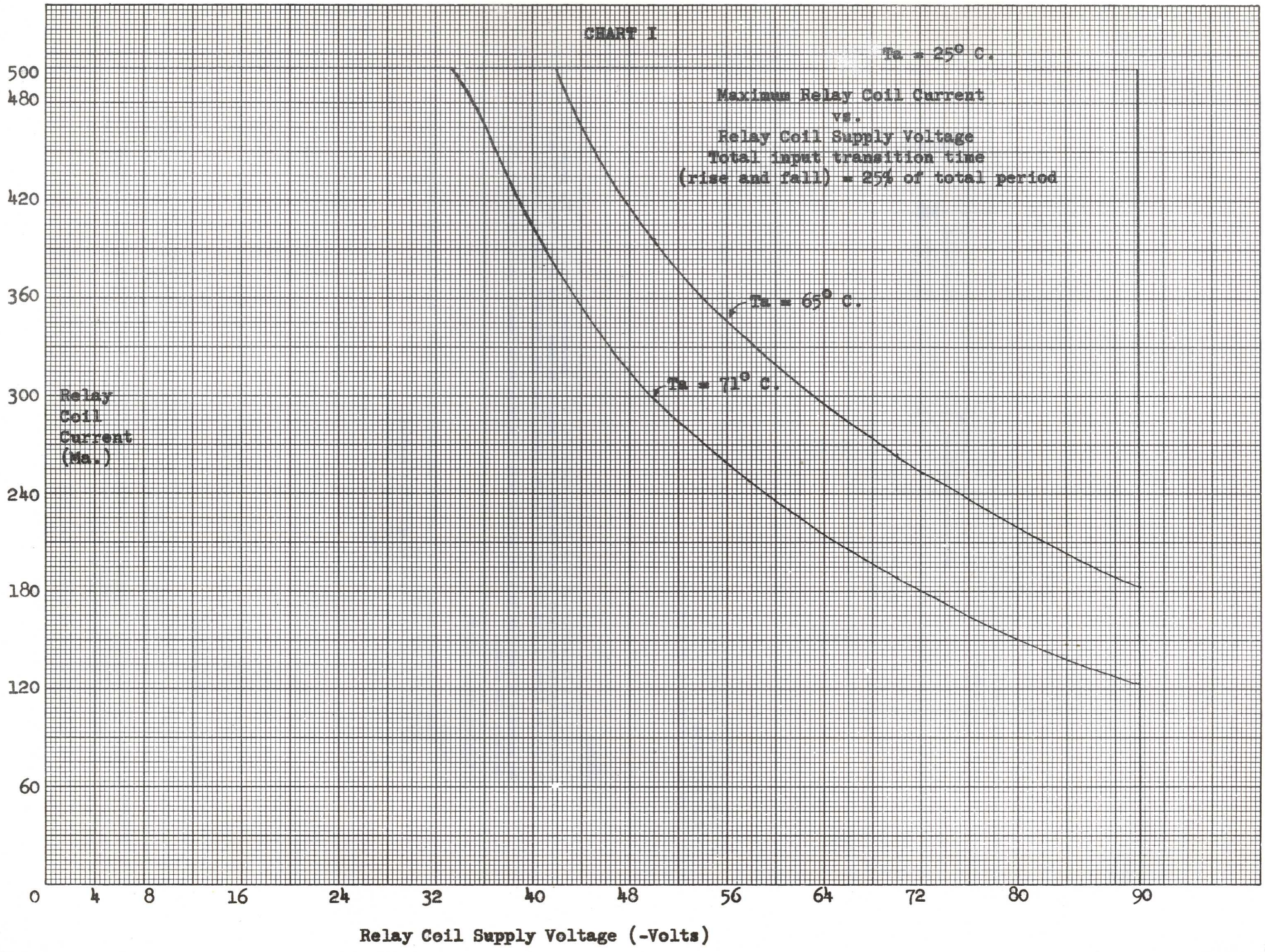
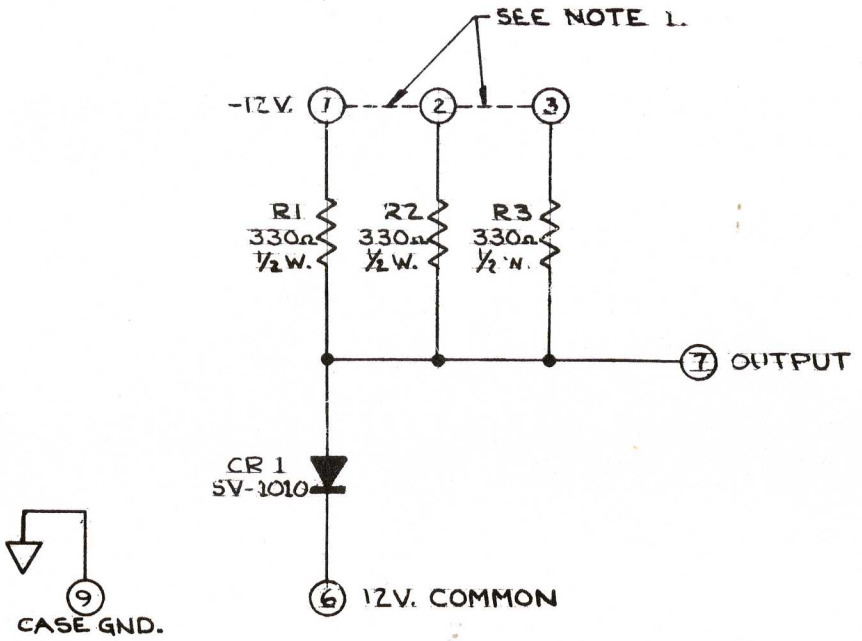


CHART I
Ta = 25° C.
Maximum Relay Coil Current
vs.
Relay Coil Supply Voltage
Total input transition time
(rise and fall) = 25% of total period
Ta = 65° C.
Ta = 71° C.
Relay
Coil
Current
(Ma.)
500
480
420
360
300
240
180
120
60
0
4
8
16
24
32
40
48
56
64
72
80
90
Relay Coil Supply Voltage (-Volts)



SCHEMATIC - -7.5 VOLT REGULATOR T-123

NOTE: 1. NO JUMPER; OUTPUT CURRENT 6 MA.
JUMPER 1 & 2; OUTPUT CURRENT 12 MA.
JUMPER 1, 2 & 3; OUTPUT CURRENT 18 MA.

I. GENERAL

The T-123 is a shunt type regulated negative 7.5 V supply. A medium power zener diode is used and yields a low output impedance and good regulation. Three ranges of regulated current are provided for by means of an external jumper.

II. ELECTRICAL SPECIFICATIONS

A. Input

The input to this device is -12 V regulated.

B. Output

1. Voltage level: -7.5 V ±1.0 V.

2. Regulated output current:

a. No jumper: 0 to 6 ma.

b. Jumper between pins 1 and 2: 12 ma.

c. Jumper between pins 1, 2, and 3: 18 ma.

3. Impedance: Approximately 10 ohms.

C. Power Requirements

1. -12 V:

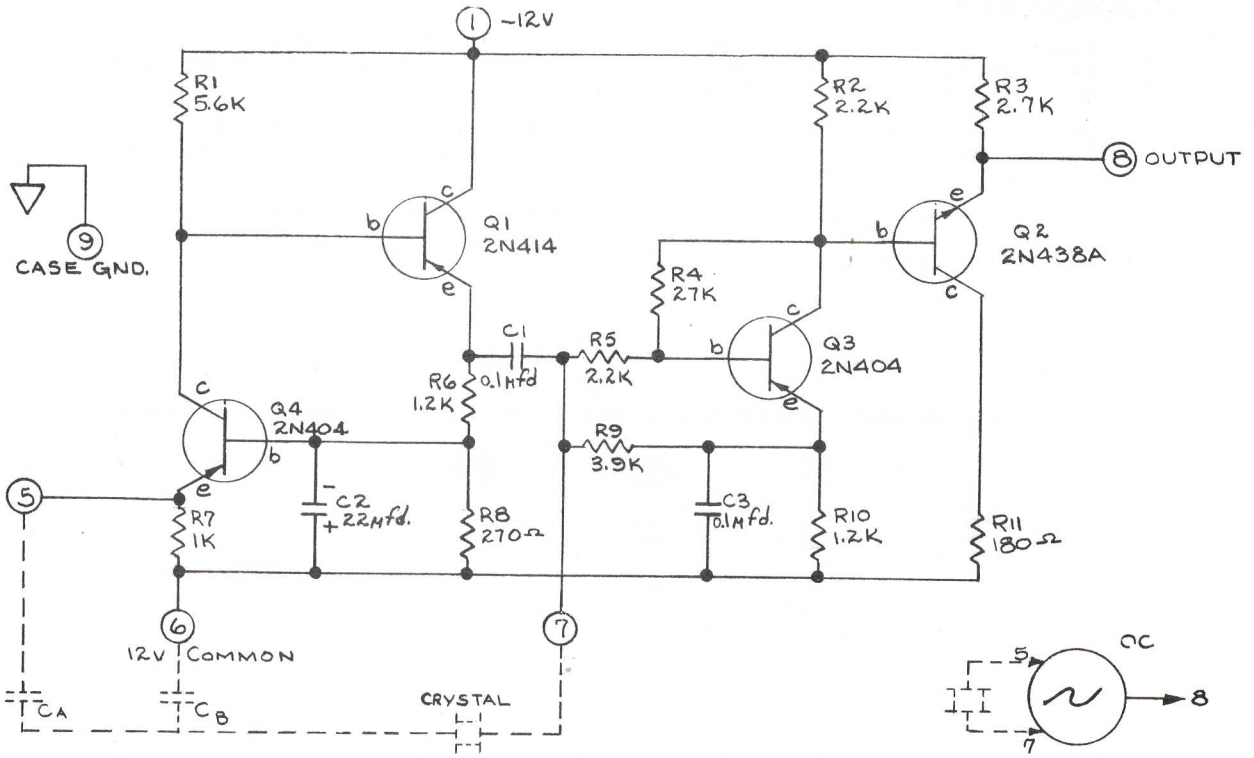
a. No jumper: 22 ma.

b. Jumper between pins 1 and 2: 44 ma.

II. ELECTRICAL SPECIFICATIONS CONTINUED

C. 1. c. Jumper between pins 1, 2, and 3: 66 ma.

2. Supply voltage tolerance: ±10%.



NOTE: 1. Q2 CASE TO BE INSULATED.
2. C_A & C_B USED TO TRIM FREQ. ±.001%; IF NO TRIM IS REQ. CRYSTAL TO BE CONNECTED BETWEEN PINS 5 & 7.
SEE CHART I FOR VALUES OF C_A & C_B

SCHEMATIC, CRYSTAL OSC. T-127

I. GENERAL

This is a transistorized unit containing two germanium PNP transistors as a butler crystal oscillator circuit, one germanium PNP transistor for squaring, and one germanium NPN transistor as emitter follower. The output is a square wave at the crystal resonant frequency. Units are normally supplied without crystals, but may be supplied with crystals cut to specific frequencies.

The crystal is used in the series-resonance mode for maximum stability. The crystal acts as the coupling impedance between the two stages of the butler circuit; one stage is common collector and the other stage is common base. Since 0° phase shift occurs through cascaded CC-CB stages, the circuit will oscillate at a frequency which experiences neither phase shift nor appreciable attenuation through the crystal. This frequency is the series-resonant frequency of the crystal. The T-127 covers the frequency range of 75 kcs to 250 kcs.

The assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket. The crystal is connected externally. It is recommended that the crystal be mounted along side the electronic assembly in order to reduce shunt capacitance between the crystal leads.

II. ELECTRICAL SPECIFICATIONS

A. Output:
1. Frequency Range: 75 kc to 250 kc.
2. Amplitude: 8 volts peak to peak, from -11 volts to -3 volts with respect to Pin #6.
3. Frequency Stability: ± .001% maximum, ±.0005% typical (under maximum combined variations of temperature, supply voltage and load; with crystal in oven).
4. Output Impedance: 1000 ohms (AC coupled).
5. Rise Time: 1.0 μsec. maximum, 0.4 μsec. typical.
6. Frequency Trimming: ± .001% of nominal crystal frequency. See Chart I.
7. Maximum DC Load: 2.7K to -12 V.

B. Power Requirements:
1. -12 volts D.C. at 10 ma (1000 ohm AC load).
2. Supply Voltage Tolerance: ± 10%

II. MECHANICAL SPECIFICATIONS

A. Dimensions: The electronic unit (less crystal) is contained within a cylindrical package of 7/8 inch diameter by 2-7/16 inches long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: The electronic unit is mounted by inserting into a standard 9-pin miniature tube socket. Where mechanical retention is required, a standard 2-3/8 inch noval tube shield is used. Either a J-slot type or snap-on type shield may be used.

C. Pin connections are arranged for minimum shunt capacitance across crystal connections.

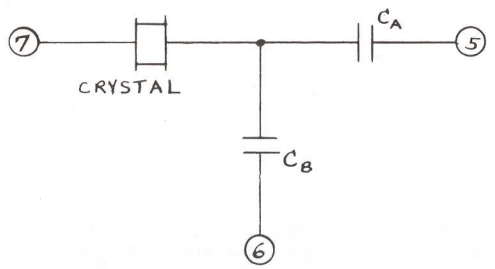
D. Operating Temperature Range: -54° C. to +71° C.

CHART I

FREQUENCY TRIMMING TABLE: CAPACITANCE VS. FREQUENCY CHANGE (typical depending on crystal parameters).

$\frac{\Delta F}{(\%)}$	Series $C_A(\mu f)$	Shunt $C_B(\mu f)$
+.0010	.003	0
+.0005	.007	0
.000	jumper	0
-.0005	jumper	.003
-.0010	jumper	.005

C_A or C_B is added externally as indicated in the sketch below:



Specification For Ordering Crystals (Monitor Products)

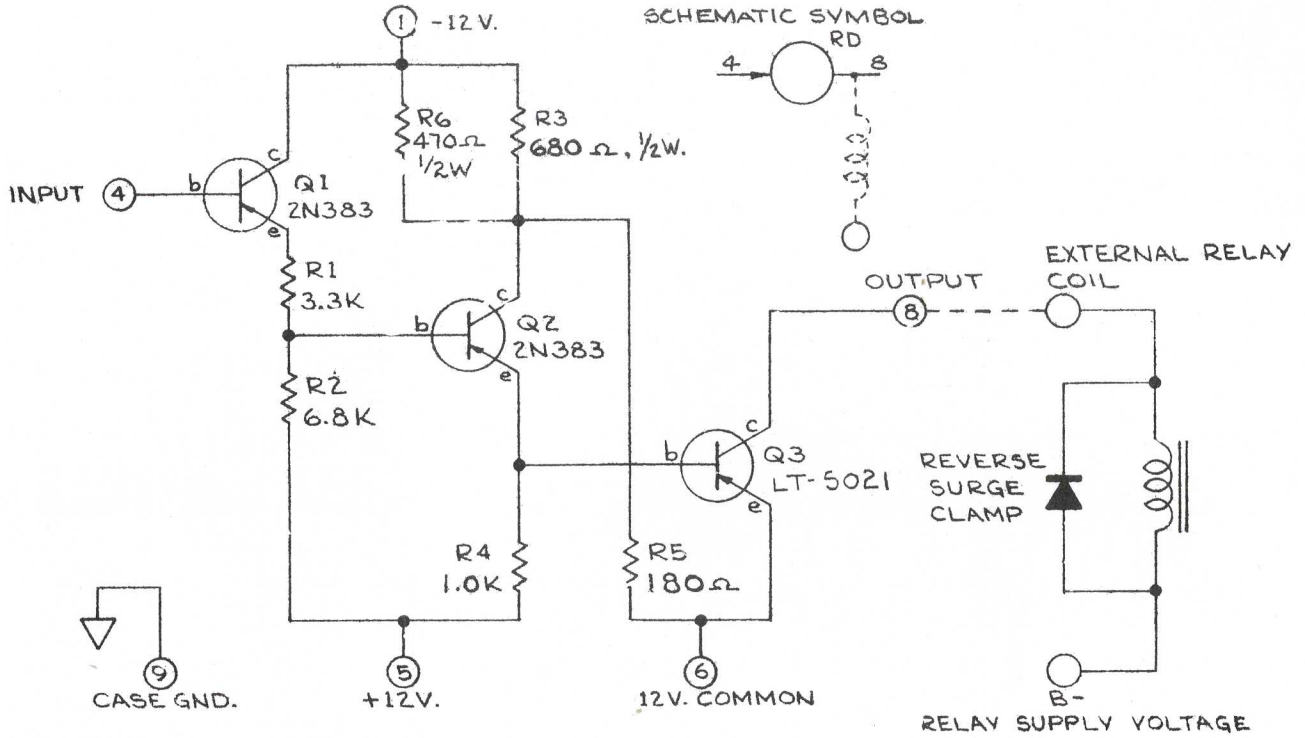
1. Series Resonant Operation
2. Drive Level: 2 mw
3. Maximum Motional Resistance: 2.5K-ohm.
4. Frequency: Customer specify (range: 75 kc to 250 kc).

* 5. Calibration Accuracy: ± .001%.

* 6. Drift: ± .0005% at 75° C. ± 5° C.

* 7. Holder Type: MC-131A (75 kc to 90 kc)
MC-13A (90 kc to 250 kc)

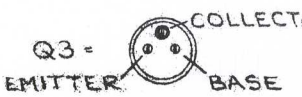
* Typical; can be changed to meet individual customer specification.



SCHEMATIC. 0-24v. RELAY DRIVER T-128

2. ALL RESISTORS ARE 1/4W.
1. Q2 REQUIRES BIRTCHER RADIATOR No. 3AL-635.

NOTES, UNLESS OTHERWISE SPECIFIED



I. GENERAL

This unit is a transistorized relay driver containing three germainum transistors. The purpose is to provide sufficient power to operate most of the general purpose relays now available. It may be operated directly from the T-Series digital units (Flip-Flop, One Shot, Squaring Circuits).

The assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:
1. Signal Frequency Range: 0 - 1 kc (for 400 ma resistive load). Max frequency with relay load depends on relay capabilities.
2. DC Signal Level to Actuate Relay: -11 V nominal.
3. DC Signal Level to Release Relay: -3 V nominal.
4. Input Impedance: 90 kΩ minimum.

B. Output:
1. Maximum output current available is dependant on the relay voltage used. See Chart I.
2. Absolute Maximum Output Current: 400 ma.
3. The relay driver must be protected against reverse surge voltages generated by the relay. Diode clamping may be used across the relay.

C. Power Required:
1. B+ +12V ±10% at 14 ma.
2. B- -12V ±10% at 30 ma to 45 ma, exclusive of relay current.
3. Relay Coil Supply Voltage: -24V absolute maximum.

III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot or a snap-on type shield may be used.

C. Pin connections are so arranged that power and grounds may be in-line wired.

D. Operating Temperature Range: -54° C. to +71° C.

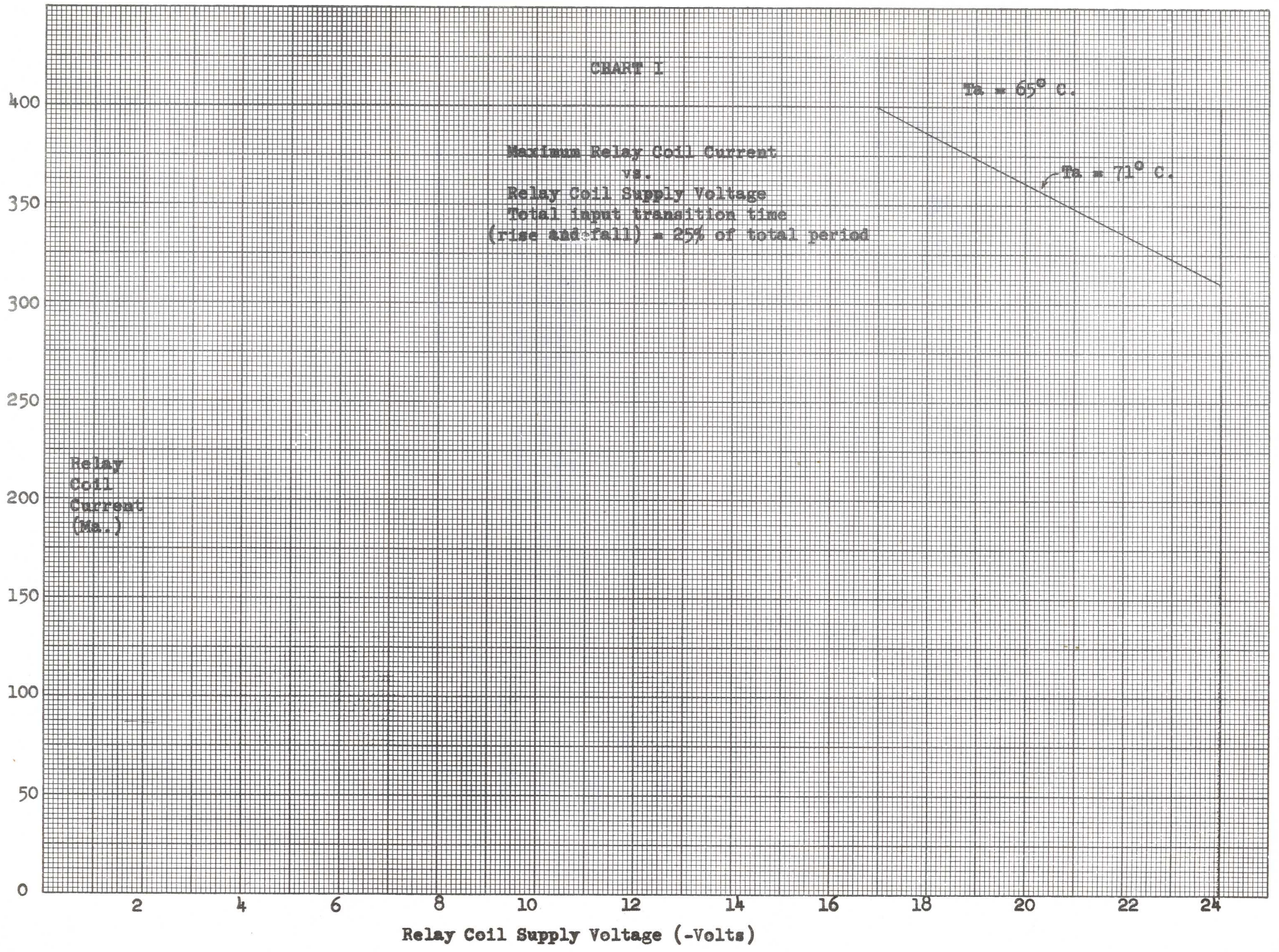
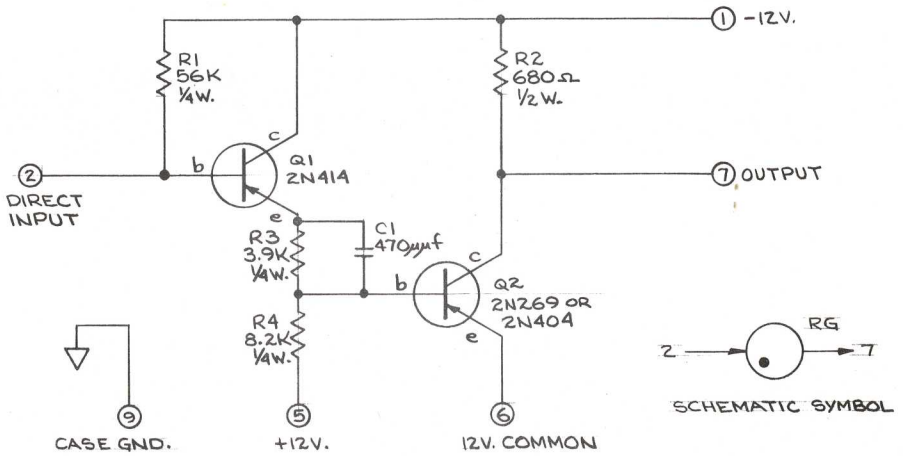


CHART I
Maximum Relay Coil Current
vs.
Relay Coil Supply Voltage
Total input transition time
(rise and fall) = 25% of total period
Ta = 65° C.
Ta = 71° C.
Relay
Coil
Current
(Ma.)
400
350
300
250
200
150
100
50
0
2
4
6
8
10
12
14
16
18
20
22
24
Relay Coil Supply Voltage (-Volts)



SCHEMATIC, RESET GENERATOR T-129

I. GENERAL

This is a transistorized D.C. Reset Generator for the purpose of resetting up to 6 decades. For the duration of an applied input signal all decades are continuously held in the reset condition. Upon removal of the input signal, all decades are immediately allowed to return to their normal operating condition. This reset generator is to be used when a negative pulse or level is required for resetting. If during reset the input to the decade is not gated and pluses are fed to the decade, the first stage N/2 in the decade will have an output, but this will not be coupled through the decade.

The standard input is an 8 V P-P signal such as would be obtained from a flip-flop, a one shot, or a gate. Pulse resetting may also be employed.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:
1. Minimum Input Amplitude: 5.5 VDC level shift of -9.5 VDC to -4 VDC.
2. Maximum Reset Rate: 50 kc.
3. For optional operation with pulse inputs, a 7 V PP minimum positive level shift with rise time up to 1 μs is applied to Pin #2 through a capacitor. A 470μμf capaciter is recommended for approximately 15 μs pulse output.
4. Input Impedance: Greater than 25K (Pin #2).
5. Maximum Input Amplitude: -12 VDC to 0 VDC.
6. Resetting is accomplished by a positive pulse or level shift.

B. Output:
1. D.C. level shift: 0 to -12 VDC (no load). Exact value of the lower level determined by number of decade loads. Lower level when operating into a maximum of 6 decades ≅ -4 VDC.
2. Duration: from 15 μsec. minimum to D.C.
3. Rise Time: .5 μsec. nominally (negative going).
4. Fall Time: 1 μsec. nominally (D.C. input), approximately 1/4 pulse width (A.C. input).

5. Load: Up to a maximum of 6 decades. When loaded with less than 3 decades insert 1K resistor in series with output.

C. Power Requirements:
1. -12 VDC at 20 ma. quiescent; 13 ma. maximum during reset period. Pin #1 negative with respect to Pin #6. +12 VDC at 1.5 ma. Pin #5 positive with respect to Pin #6.
2. Supply Voltage Tolerance: ± 10%.

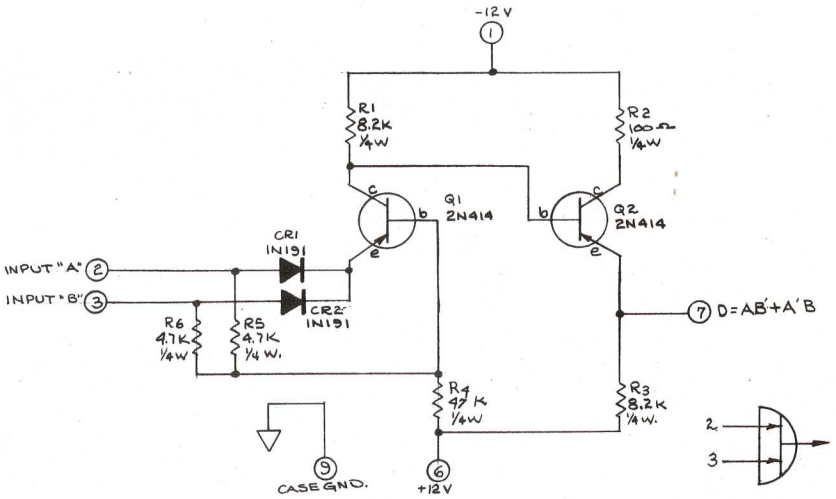
III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot type or a snap-on type shield may be used.

C. Pin connections are so arranged that power and grounds may be in-line wired.

D. Operating Temperature Range: -54° C. to +71° C.



2 INPUT "EXCLUSIVELY-OR" GATE T-421

I. GENERAL

This unit is an "exclusively-OR" gate containing two transistors and two diodes. The purpose of an "exclusively-OR" gate is to provide an output when one and only one input is present. The logic equation is as follows:

$$D = AB' + A'B$$

The circuit consists of a conventional "OR" gate whose output is supplied to the emitter of a transistor gate (Q_1). The base of the transistor is supplied by a summing network of which the summed voltage is a function of the number of OR-gate input signals which are OFF. When more than one input are ON, the summed voltage is sufficiently low to cut off the transistor gate.

If all but one of the inputs are held at -11 volts (OFF), the remaining input can be switched ON and OFF to produce a similar signal at the output. The output rise time is a function of the input rise time and the B of Q_1.

The circuit can also be used as a DC inverter by holding one input at -3 volts (ON) while a second input is switched ON and OFF by the signal which is to be inverted. The output rise time is now a function of the input fall time and the B of Q_1.

A recommended driving unit for each input is a T-111 PNP emitter follower.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:

Frequency Range: 0 to 250 kc.
Signal Driving Levels:
OFF (Binary "0") -11 volts at 1.7 ma to a positive source.
ON (Binary "1") -3 volts at 2.4 ma to a negative source.
Recommended Driving Unit:
PNP emitter follower (T-111)

B. Output:

Signal Levels: -3 to -11 volts.

Rise Time: .1 to 1.0 μsec. if input rise and fall times are less than 2 μsec.
Typical Load: One "OR" Gate and one "AND" Gate
Maximum Load at 71°C: 8K to +12 volts, 2K to ground, or 4.7K to -12 volts.

C. Power Required:
+12 volts DC at 4 ma.
-12 volts DC at 4 ma.
Supply Voltage Tolerance: ± 10%.

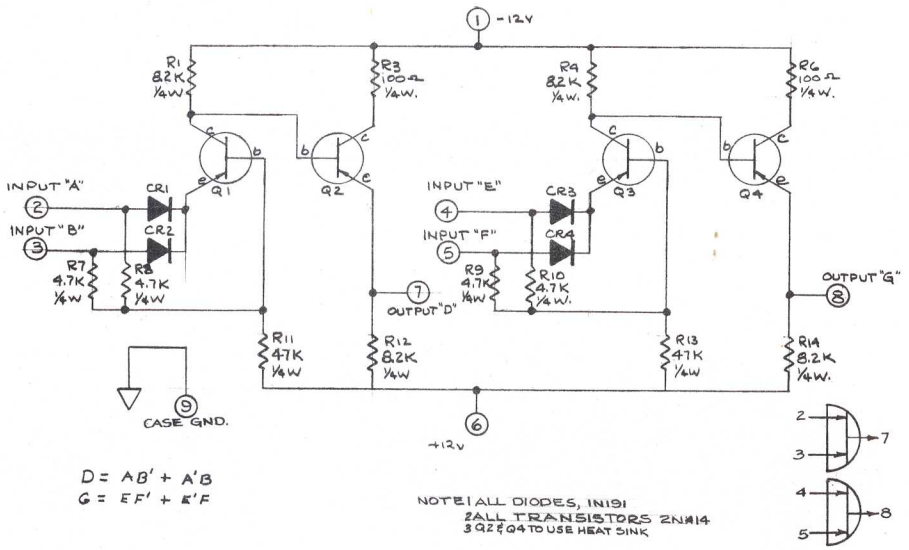
III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot or a snap-on type may be used.

C. Pin connections are so arranged that power and grounds may be in-line wired.

D. Operating Temperature Range: -54°C to +71°C



$D = AB' + A'B$

$G = EF' + E'F$

NOTE: 1 ALL DIODES, 1N191
2 ALL TRANSISTORS 2N414
3 Q2 & Q4 TO USE HEAT SINK

DUAL 2-INPUT, "EXCLUSIVELY-OR" GATE. T-423

I. GENERAL

This unit is a pair of "exclusively-OR" gates, (T-421), each containing two transistors and two diodes. The purpose of an "exclusively OR" gate is to provide an output when one and only one input is present. The logic equations are as follows:

$D = AB' + A'B$

$G = EF' + E'F$

Each circuit consists of a conventional OR gate whose output is supplied to the emitter of a transistor gate (Q_1). The base of the transistor is supplied by a summing network of which the summed voltage is a function of the number of OR-gate input signals which are OFF. When more than one input are ON, the summed voltage is sufficiently low to cut off the transistor gate.

If one input is held at -11 volts (OFF), the remaining input can be switched ON and OFF to produce a similar signal at the output. The output rise time is a function of the input rise time and the B of Q_1.

The circuit can also be used as a DC inverter by holding one input at -3 volts (ON) while a second input is switched ON and OFF by the signal which is to be inverted. The output rise time is now a function of the input fall time and the B of Q_1.

A recommended driving unit for each input is a T-111 PNP emitter follower.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:

Frequency Range: 0 to 250 kc.
Signal Driving Levels:
OFF (Binary "0") -11 volts at 1.7 ma to positive source.
ON (Binary "1") -3 volts at 2.4 ma to negative source.
Recommended Driving Unit: PNP emitter follower (T-111)

B. Output:

Signal Levels: -3 to -11 volts.

Rise Time: .1 to 1.0 μsec. if input rise and fall times are less than 2 μsec.
Typical Load: One "OR" gate and one "AND" gate on each output
Maximum Load at 71°C: 8K to +12 volts, 2K to ground, or 4.7K to -12 volts on each output.

C. Power Required

+12 volts DC at 8 ma.
-11 volts DC at 8 ma.
Supply Voltage Tolerance ± 10%.

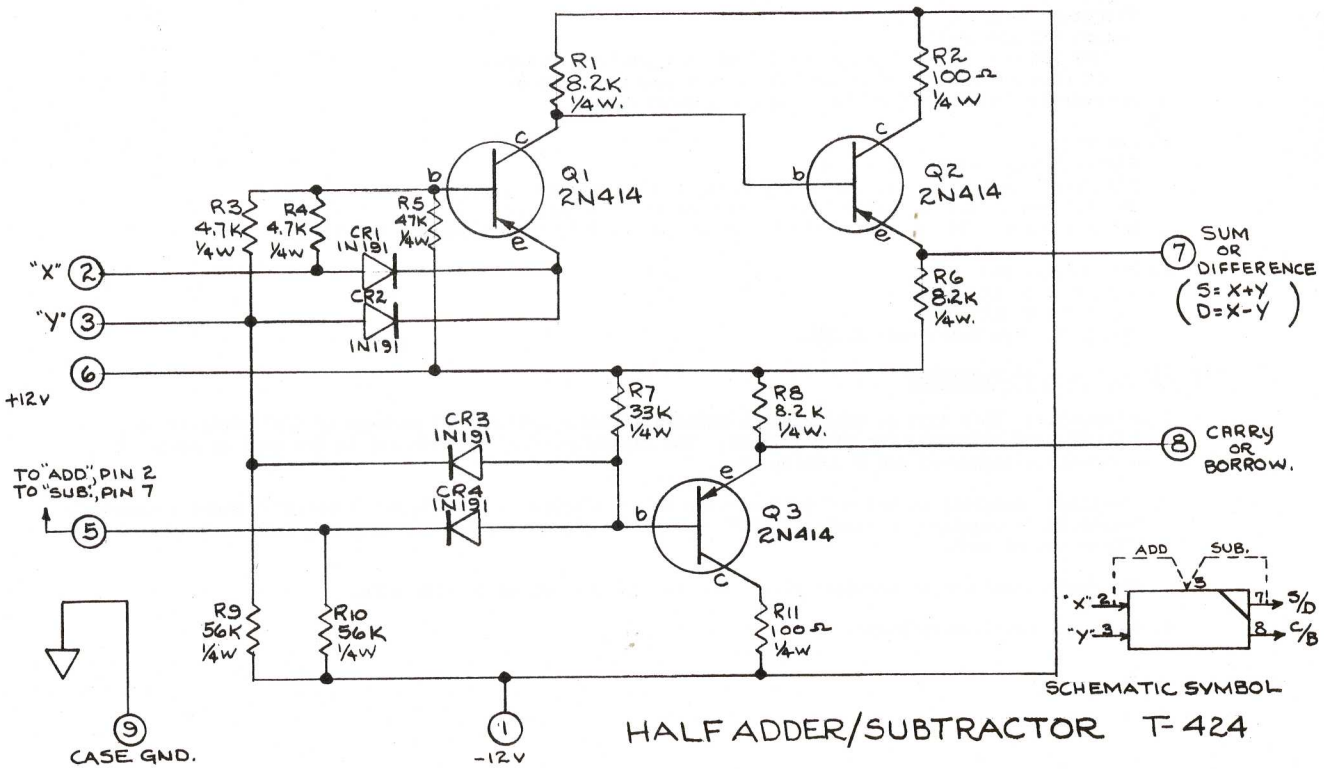
III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" moval tube shield is used. Either a J-slot or a snap-on shield may be used.

C. Pin connections are so arranged that power and grounds may be in-line wired.

D. Operating Temperature Range: -54°C to +71°C



HALF ADDER/SUBTRACTOR T-424

NOTE: USE HEAT SINK ON Q2 & Q3.

I. GENERAL

This is a transistorized assembly containing three PNP germanium transistors, two of which are emitter followers, and four germanium diodes. The unit can be used as a half-adder or a half-subtractor, depending on the connection of an external jumper.

The purpose of a half-adder is to provide sum (S) and carry (C) outputs from two single-digit inputs (X + Y). Full addition is performed when a third input, "carry" from adder of next lowest significant digit, is added to X + Y. Two half-adders and an "OR" gate make up a full-adder. See Truth Tables I and II on page 3.

The purpose of a half-subtractor is to provide difference (D) and borrow (B) outputs from two single-digit inputs (X - Y). Full subtraction is performed when a third input, "borrow" from subtractor of next lowest significant digit, is subtracted from X - Y. Two half-subtractors and an "OR" gate make up a full-subtractor. See Truth Tables III and IV on page 3.

The logic equations of a half-adder as derived from the truth table are as follows:

S (sum) = XY' + X'Y
C (carry) = XY

The logic equations of a half-subtractor as derived from the truth table are as follows:

D (difference) = XY' + X'Y
B (borrow) = DY

The sum and difference equations are exactly alike; thus, either can be performed by an "exclusively OR" gate. Carry and borrow equations have similar form but different inputs. Either can be performed by an "AND" gate if one of the inputs is connected to X for addition or to D for subtraction. (The other input is always connected to Y.)

The T-424 contains one "exclusively OR" gate and one "AND" gate. One of the "AND" gate inputs is terminated at Pin 5 which is jumpered to Pin 2 (X) for addition or Pin 7 (D) for subtraction.

This assembly is contained in a cylindrical plug-in package which inserts into a standard 9-pin miniature tube socket.

II. ELECTRICAL SPECIFICATIONS

A. Input:
Frequency Range: 0 to 250 kc.
Signal Driving Levels:
OFF (Binary "0") -11 volts at 2.5 ma to a positive source.
ON (Binary "1") -3 volts at 2.5 ma to a negative source.
Recommended Driving Unit: PNP emitter follower (T-112).

B. Output:
Signal Levels: -3 to -11 volts.
Rise Time .1 to 1.0 μsec depending on input rise and fall time.
Typical Load: One half-adder/subtractor and one "OR" gate.
Maximum Load: 8K to +12 volts, 2K to ground, or 4.7K to -12 volts. (at 71°C)

C. Power Required:
+12 volts DC at 8 ma.
-12 volts DC at 8 ma.
Supply Voltage Tolerance: ± 10%.

III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 9-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot or a snap-on type shield may be used.

C. Pin connections are so arranged that power and grounds may be in-line wired.

D. Operating Temperature Range: -54°C to +71° C.

Truth Table I - Half-Adder X + Y = S

X	0	0	1	1
Y	0	1	0	1
S	0	1	1	0
C	0	0	0	1

Truth Table II - Full-Adder X + Y + C = S

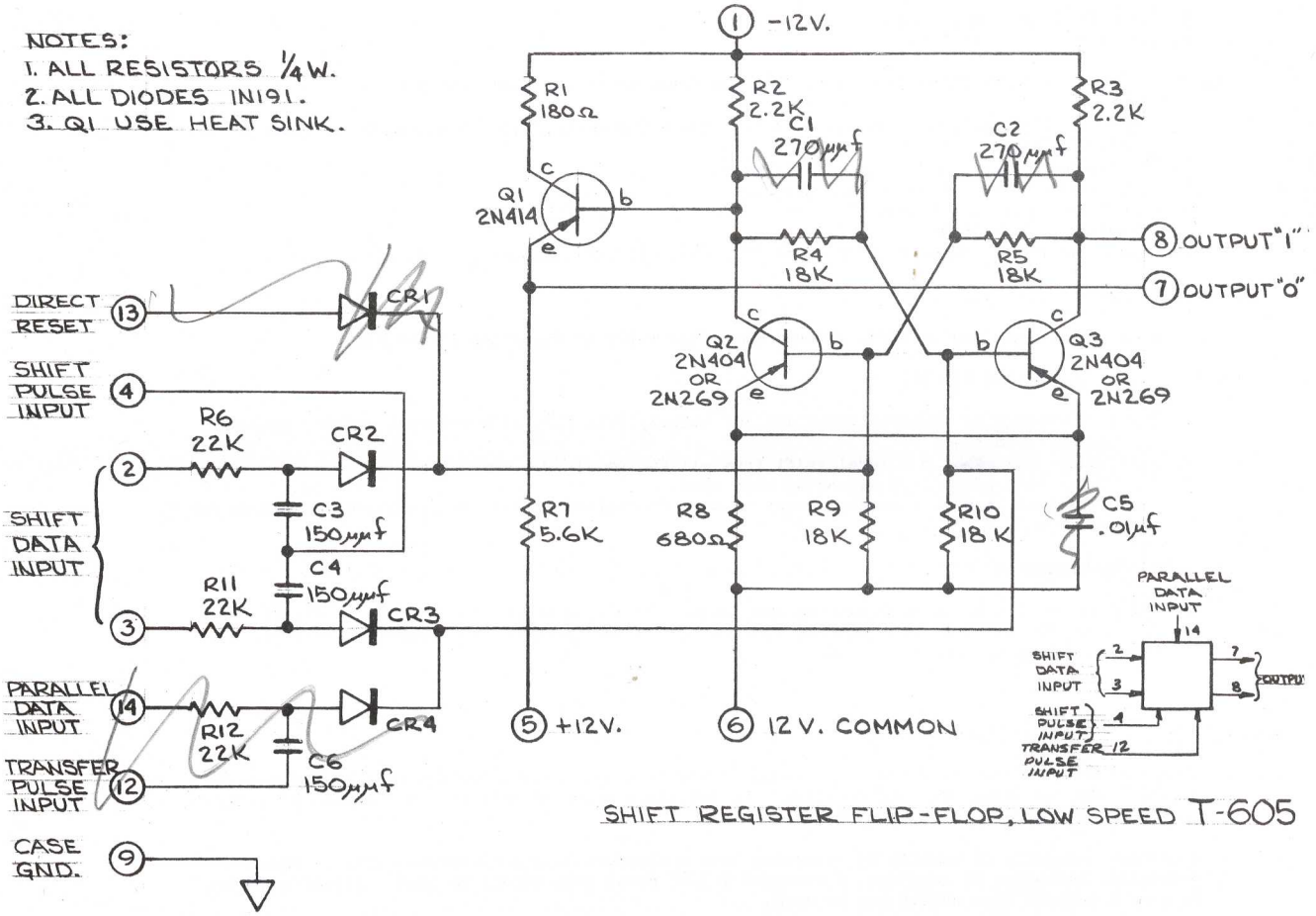
X	0	1	0	0	1	1	0	1
Y	0	0	1	0	1	0	1	1
C	0	0	0	1	0	1	1	1
S	0	1	1	1	0	0	0	1
C	0	0	0	0	1	1	1	1

Truth Table III - Half-Subtractor X - Y = D

X	0	1	0	1
Y	0	0	1	1
D	0	1	1	0
B	0	0	1	0

Truth Table IV - Full-Subtractor X - Y - B = D

X	0	1	0	0	1	1	0	1
Y	0	0	1	0	1	0	1	1
B	0	0	0	1	0	1	1	1
D	0	1	1	1	0	0	0	1
B	0	0	1	1	0	0	1	1



SHIFT REGISTER FLIP-FLOP, LOW SPEED T-605

I. GENERAL

This unit is a Shift Register Flip-Flop. It is used in assembling shift register systems.

The circuit of this unit is a configuration of diode pulse gates and a storage flip-flop arranged to transfer stored data from input shift registers to an output shift register. Three pulse "And" gates and one pulse "Or" gate are contained in the circuit. Each pulse "And" gate permits an applied clock pulse to be transmitted through the gate when its control input signal is in the binary "1" state. The "Or" gate is a pulse mixer.

A shift register system is composed of a series of T-605 SR units, one for each digit. Each shift register output supplies the control inputs (shift data input) for the next shift register element. Every applied clock shift pulse is gated to one side or the other of the internal storage flip-flop, depending upon the state of the preceeding shift register. In this way, data is shifted serially from digit to digit through the shift register.

Provision is made for parallel data transfer from a storage flip-flop in a second register. The circuitry for accomplishing this parallel read-in of data is identical to that used for shifting.

An internal emitter follower is included to facilitate direct loading of DC logic for parallel or serial output.

Parallel data is entered by setting the shift register flip-flops. This method requires that the shift register be initially cleared before entering new data. Clearing is accomplished by shifting "zeros" through the register or by employing a reset generator, T-109, for clearing in one clock time.

II. ELECTRICAL SPECIFICATIONS

A. Control Inputs: Shift Data Input (Pin #2 and Pin #3), and Parallel Data Input (Pin #14)

1. Type: D.C. Level shift as obtained from shift register or flip-flop outputs.
2. Amplitude: Level shift of 8 volts amplitude, from -11 volts DC to -3 volts DC, nominal.

3. Rise Time: 0.1 to 1.0 μsec.
4. Frequency: 0 to 12.5 kc.

B. Pulse Inputs: Shift Pulse Input (Pin #4), and Transfer Pulse Input (Pin #12)

1. Type: Positive pulse. Normally obtained from a Pulse Amplifier, Blocking Oscillator, or NPN Emitter Follower.
2. Minimum Amplitude: 6.0 volts peak-to-peak.
3. Maximum Amplitude: 9 volts peak-to-peak.
4. Rise Time: 0.1 to 1.0 μsec.
5. Frequency: 0 to 25 kc.
6. Input Impedance: 300μμfd. capacitive (Pin #4); 150μμfd. capacitive (Pin #12).

C. Reset Input: (Pin #13)

1. When reset operation is used, a Reset Generator T-109 is connected to Pin #13.

D. Output: (Pin #7 and Pin #8)

1. Type: 2 outputs of opposite polarity; "0" output, (Pin #7), with internal emitter follower; "1" output, (Pin #8).
2. Amplitude: Unloaded, 8 V level shift from -11 VDC to -3 VDC, nominally.
3. Rise Time: 0.2 μs to 1 μs depending upon load.
4. Load: Typical load is a control input to a shift register. Maximum resistive loading on Pin #7 is 3.3K to ± 12 V.

E. Power Requirements:

1. -12 volts at 8.9 to 16 ma depending upon load. Pin #1 negative with respect to Pin #6.
2. +12 volts at 3.9 to 11 ma depending upon load. Pin #5 positive with respect to Pin #6.
3. Supply Voltage Tolerance: ± 10%.

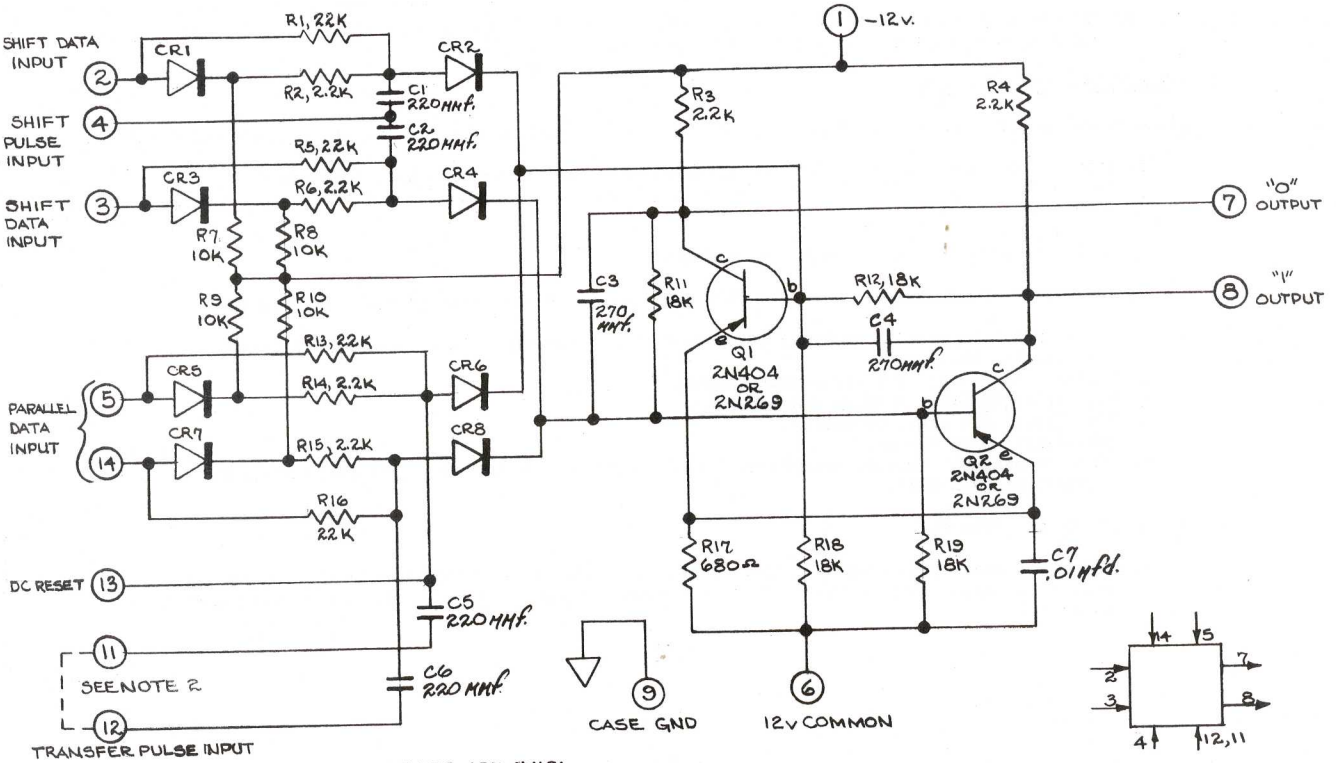
III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 14-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot type or a snap-on type shield may be used.

C. The location of Pin 10 is used for orientation.

D. Operating Temperature Range: -45° C. to +65° C.



NOTE: 1. ALL DIODES ARE IN191.
2. JUMPER USED WHEN DUAL INPUT PARALLEL DATA APPLIED
3. KEYWAY LOCATION, PIN 10.

MEDIUM SPEED SHIFT REGISTER FLIP-FLOP T-606

I. GENERAL

This unit is a Shift Register Flip-Flop. It is used in assembling shift register systems.

The circuit of this unit is a configuration of diode pulse gates and storage flip-flop arranged to transfer stored data from input flip-flops to an output shift register. Four Pulse "And" gates and two pulse "Or" gates are contained in the circuit. Each pulse "And" gate permits an applied clock pulse to be transmitted through the gate when its control signal is in the binary "1" state. The "Or" gates are pulse mixers.

A shift register system is composed of a series of T-606 shift register flip-flops, one for each digit. Each shift register output supplies the control inputs (shift data input) for the next shift register. Every applied clock shift pulse is gated to one base or the other of the internal storage flip-flop, depending on the state of the preceeding shift register. In this way, data is shifted serially from digit to digit through the shift register system.

Provision is made for parallel data trsnsfer from a storage flip-flop in a second register. The circuitry for accomplishing this parallel read-in of data is identical to that used for shifting.

Simultaneous resetting of all shift register flip-flops may be accomplished by employing a Reset Generator T-109. This method of resetting clears the register in one clock time.

Three fundamental types of shift register configurations are possible with this unit. They differ mainly in the method of entering parallel data, and of clearing the shift register.

(a) Parallel data can be entered into the shift register by gating <u>both</u> outputs of the parallel data storage flip-flop. The corresponding shift register flip-flop is forced into the same state by set-reset triggering. Clearing of the shift register is not required since data is entered into the register regardless of the prior state of the shift register flip-flop.

(b) Parallel data is entered by <u>setting</u> the shift register flip-flops. This method requires that the shift register be initially cleared before entering new data. Clearing is accomplished by shifting "zeros" through the register, which leaves all flip-flops in the reset state.

(c) This configuration is identical to "b" except that a Reset Generator T-109, is employed for clearing the register. All flip-flops are simultaneously reset.

II. ELECTRICAL SPECIFICATIONS

A. Control Inputs: Shift Data Input (Pin #2 and Pin #3), and Parallel Data Input (Pin #5 and Pin #14)

1. Type: D.C. level shift as obtained from a shift register or a flip-flop output.
2. Amplitude: Level shift of 8 volts amplitude, from -11 volts D.C. to -3 volts D.C., nominal.
3. Rise Time: 0.1 to 1.0 μsec.
4. Frequency: 0 to 125 kc.
5. Input Current: 0.9 ma to negative voltage.

B. Pulse Inputs: Shift Pulse Input (Pin #4), and Transfer Pulse Input (Pin #11 and Pin #12)

1. Type: Positive pulse. Normally obtained from a Pulse Amplifier, Blocking Oscillator, or NPN Emitter Follower.
2. Minimum Amplitude: 7.5 volts peak-to-peak.
3. Maximum Amplitude: 9 volts peak-to-peak.
4. Rise Time: 0.4 μsec. or better.
5. Frequency: 0 to 250 kc.
6. Input Impedance: 440μμf. capacitive (Pin #4); 220μμfd. capacitive (Pin #11); 220μμfd. capacitive (Pin #12).

C. Reset Input: (Pin #13).

1. When reset operation is used, a Reset Generator T-109 is connected to Pin #13. A resistor should be connected from Pin 13 to 12 V common. Value = $\frac{10,000}{n}$ where n is the number of SR elements.

D. Output: (Pin #7 and Pin #8)

1. Type: 2 outputs of opposite polarity; "0" output, (Pin #7); "1" output, (Pin #8).
2. Amplitude: 8 V level shift from -11 VDC to -3 VDC nominally.
3. Rise Time: 0.2 μs to 1.0 μs depending on load and input signal.
4. Loads: Typical load is a parallel combination of 1 control input to a shift register flip-flop, 1 flip-flop and 1 minisig indicator.
   Maximum resistive loading: for 1/2 V level shift, .2 ma to a positive source; 1 ma to a negative source.
   for 1 v level shift, 0.4 ma to a positive source; 2 ma to a negative source.
5. Fall Time: Approximately 2.0 μsec.

E. Power Requirements:

1. -12 volts at 6.6 ma maximum. Pin #1 negative with respect to the 12 V common.
2. Supply Voltage Tolerance: ± 10%.

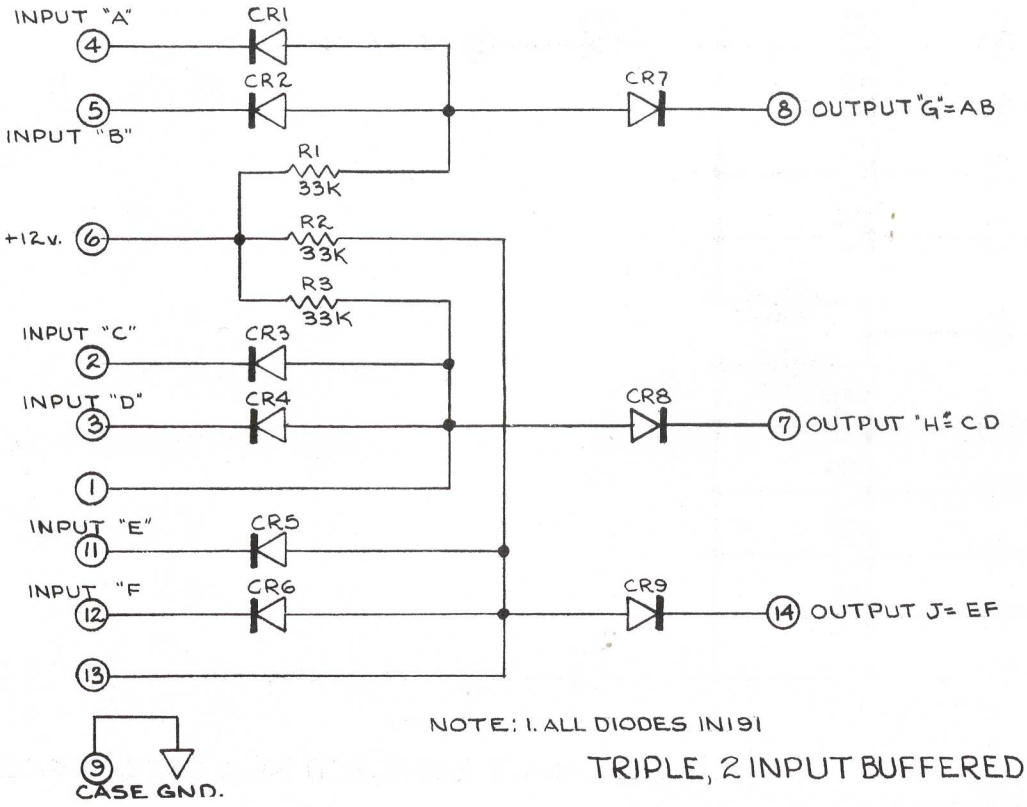
III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

B. Mounting: Assembly is mounted by inserting into a standard 14-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot type or a snap-on type shield may be used.

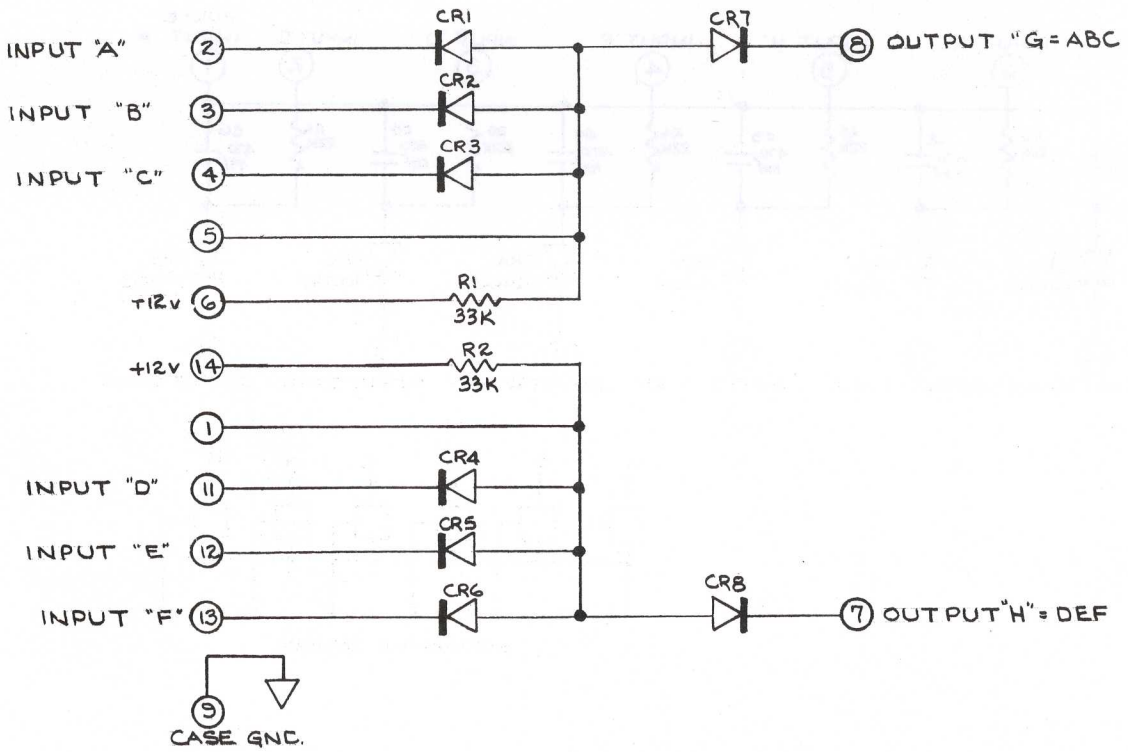
C. The location of Pin 10 is used for orientation.

D. Operating Temperature Range: -45° C. to +71° C.



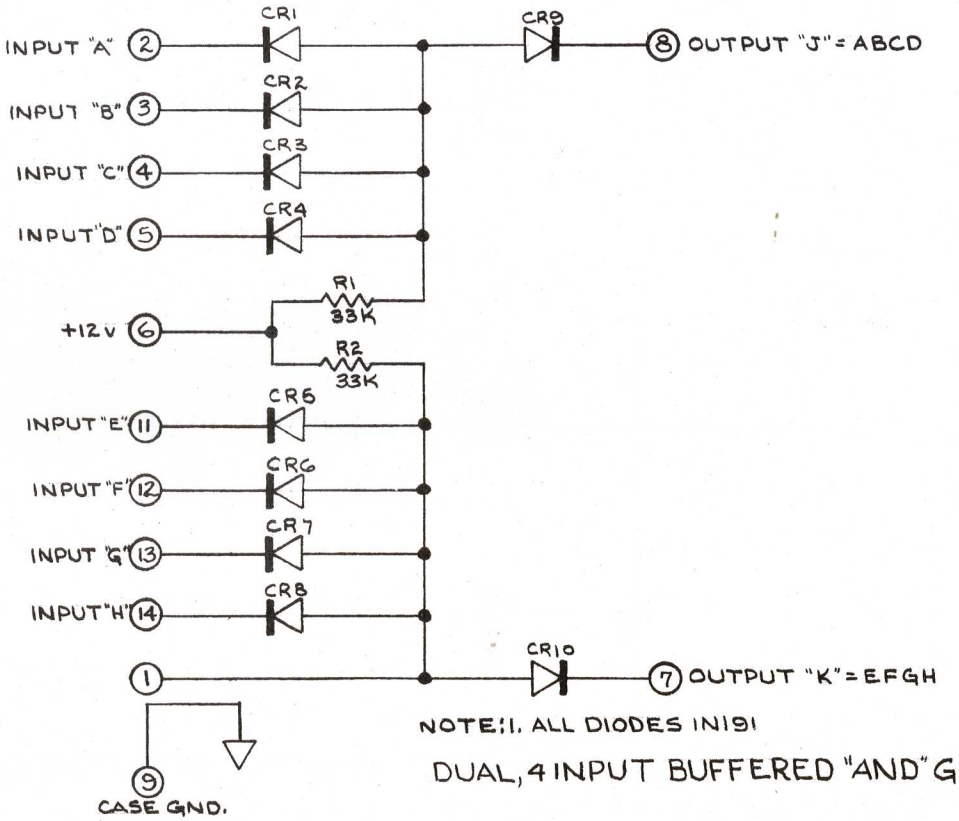
NOTE: 1. ALL DIODES IN191

TRIPLE, 2 INPUT BUFFERED "AND" GATE. T-607



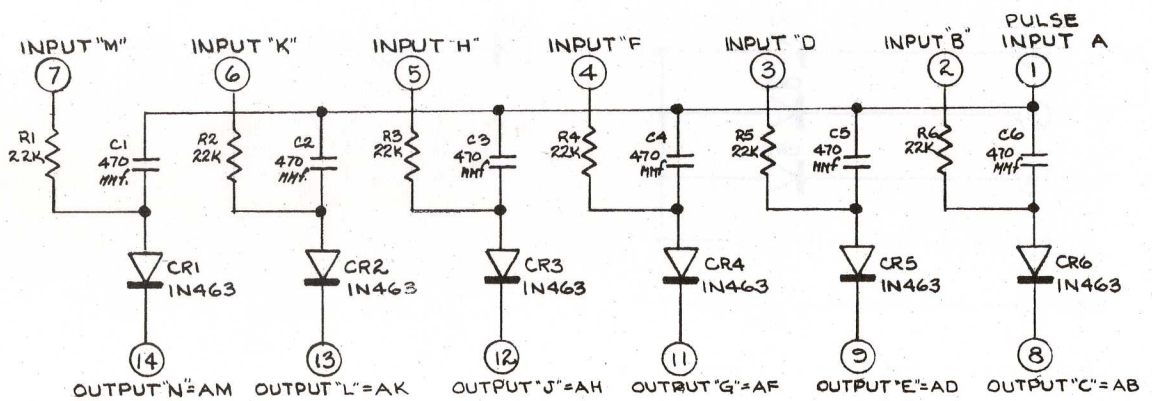
NOTE: 1. ALL DI ES IN191

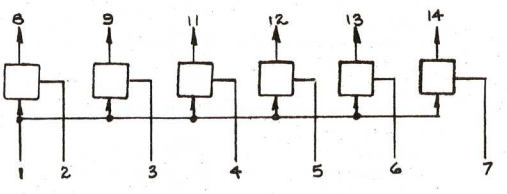
DUAL, 3 INPUT BUFFERED "AND" GATE T-608



NOTE: 1. ALL DIODES IN191

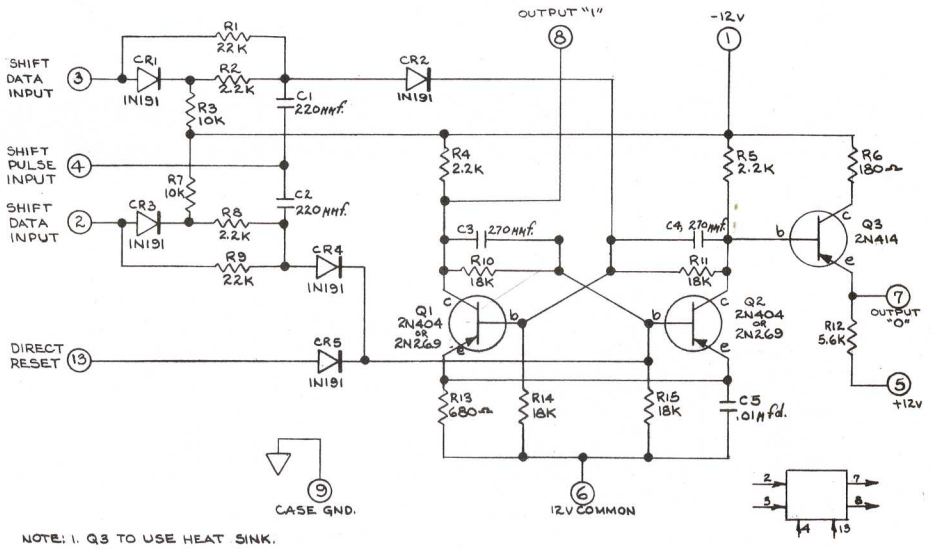
DUAL, 4 INPUT BUFFERED "AND" GATE T-609





SCHEMATIC SYMBOL

SCHEMATIC, MULTIPLE PULSE "AND" GATE. T-612



NOTE: 1. Q3 TO USE HEAT SINK.

SHIFT REGISTER FLIP-FLOP. T-610

I. GENERAL

This unit is a Shift Register Flip-Flop. It is used in assembling shift register systems for serial in and serial or parallel out operation.

The circuit of this unit is a configuration of diode pulse gates and a storage flip-flop arranged to transfer stored data from an input flip-flop to an output shift register. Two pulse "And" gates are contained in the circuit. Each pulse "And" gate permits an applied clock pulse to be transmitted through the gate when its control input signal is in the bimary "1" state.

A shift register system is composed of a series of T-610 SR units, one for each digit. Each shift register output supplies the control inputs (shift data input) for the next shift register element. Every applied clock shift pulse is gated to one side or the other of the internal storage flip-flop, depending upon the state of the preceeding shift register. In this way, data is shifted serially from digit to digit through the shift register.

An internal emitter follower is included to facilitate direct loading of DC logic for parallel or serial output.

II. ELECTRICAL SPECIFICATIONS

A. Control Inputs: Shift data input (Pin #2 and Pin #3)

1. Type: D.C. level shift as obtained from shift register or flip-flop outputs.
2. Amplitude: Level shift of 8 volts amplitude, from -11 volts DC to -3 volts DC, nominal.
3. Rise Time: 0.1 to 1.0 μsec.
4. Frequency: 0 to 125 kc.
5. Input Current: 0.9 ma to negative voltage.

B. Pulse Inputs: Shift pulse input (Pin #4)

1. Type: Positive pulse. Normally obtained from a Pulse Amplifier, Blocking Oscillator, or NPN Emitter Follower.

2. Minimum Amplitude: 7.5 volts peak-to-peak.
3. Maximum Amplitude: 9 volts peak-to-peak.
4. Rise Time: 0.4 μsec. or better.
5. Frequency: 0 to 250 kc.
6. Input Impedance: 440μμfd. capacitive.

C. Output: (Pin #7 and Pin #8)

1. Type: 2 outputs of opposite polarity; "0" output, (Pin #7), with internal emitter follower; "1" output, (Pin #8).
2. Amplitude: Unloaded, 8 V level shift from -11 VDC to -3 VDC, nominally.
3. Rise Time: 0.2 μs to 1 μs depending upon load.
4. Load: Typical load is a control input to a shift register. Maximum resistive loading on Pin #7 is 3.3K to ± 12 V.

D. Power Requirements:

1. -12 volts at 9.8 to 16.9 ma depending upon load. Pin +1 negative with respect to Pin #6.
2. +12 volts at 3.9 to 11 ma depending upon load. Pin #5 positive with respect to Pin #6.
3. Supply Voltage Tolerance: ± 10%.

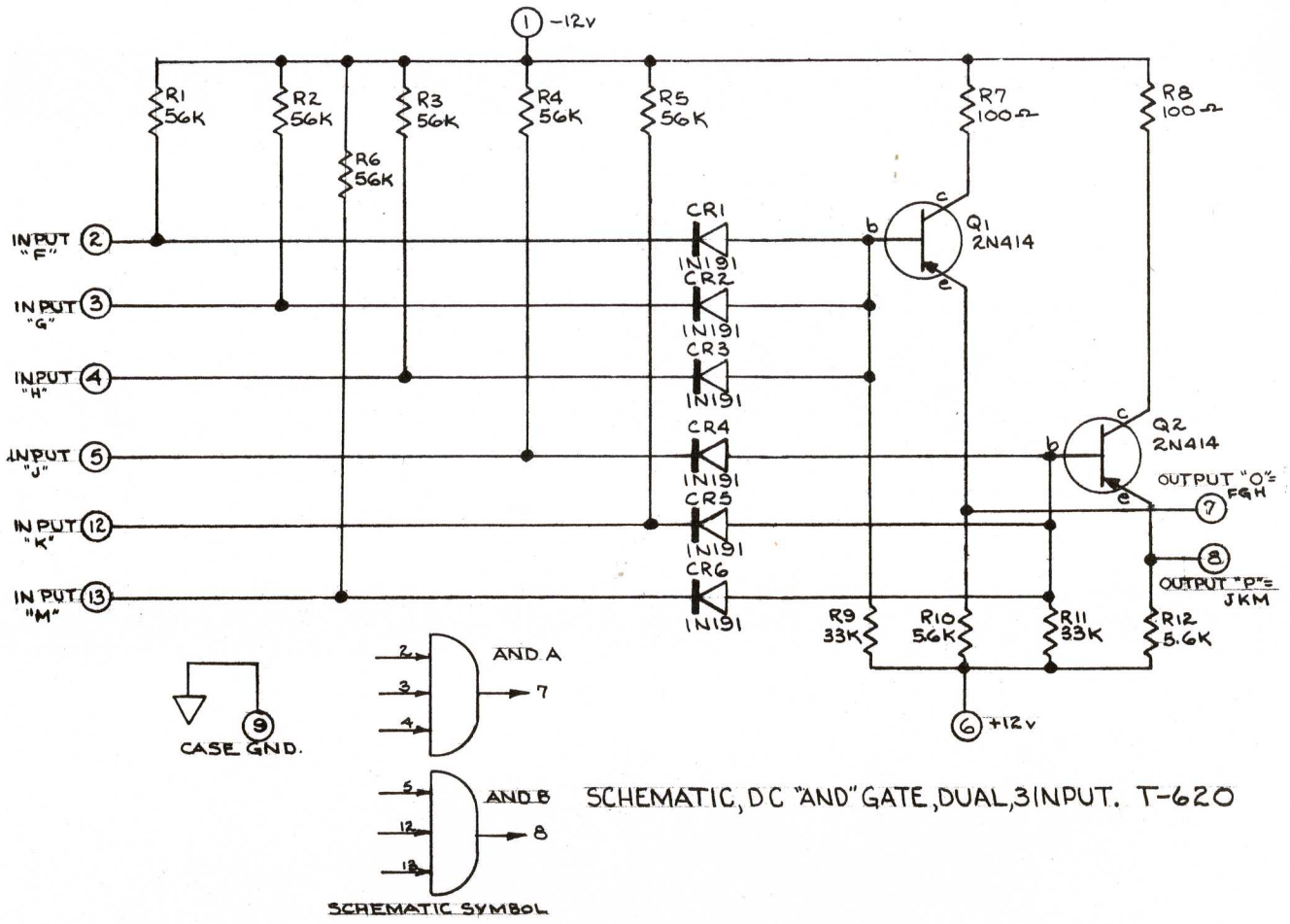
III. MECHANICAL SPECIFICATIONS

A. Dimensions: This unit is completely contained within a cylindrical package of 7/8" diameter by 2-7/16" long including the plug-in base. The removable cover is attached to the base by means of a bayonet arrangement and a locking ring.

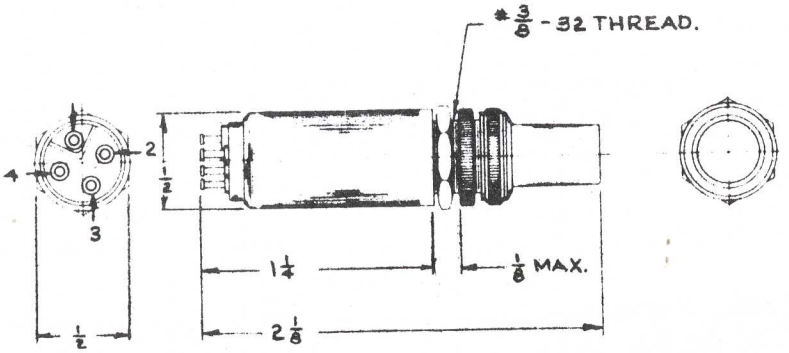
B. Mounting: Assembly is mounted by inserting into a standard 14-pin miniature socket. Where mechanical retention is required, a standard 2-3/8" noval tube shield is used. Either a J-slot type or a snap-on type shield may be used.

C. The location of Pin 10 is used for orientation.

D. Operating Temperature Range: -45° C. to +65° C.



SCHEMATIC, DC "AND" GATE, DUAL, 3 INPUT. T-620



I. GENERAL

The Minisig Indicator (R-121) is a high gain, transisterized neon indicator, useful for a visual display of various signal levels. The device is designed to accommodate small or medium amplitude signal excursions (3 volts peak-to-peak to 45 volts peak-to-peak or greater), and yields a visual indication for the most positive of two signal levels. The R-221 yields a visual indication for the most negative of two signal levels. A typical application of the device would be to indicate the static state of a flip-flop or other information storage element by a visual display.

II. ELECTRICAL SPECIFICATIONS

A. Input:

1. See Chart I for areas of operation.
2. Maximum loads imposed upon input signal:
   a. Neon on: -120μa.
   b. Neon off: > +35μa, the limit being determined by the lower operating point. See Chart I.
3. Maximum negative input is -50 volts.

B. Output:

A visual display is given for the most positive of two signal levels to the input of the R-121.

C. Power Requirements:

1. -100 volts at 0.7ma.
2. Bias voltage at 3.5 ma maximum (depending on input signal level and bias voltage). The voltage level is derived from Chart I.
3. Supply voltage tolerance: ± 5%.

III. MECHANICAL SPECIFICATIONS

A. Over-all Length: 2-19/32 inches.
B. Diameter: 1/2 inch.
C. Weight: 1/2 ounce (approximately).
D. Finish: Black anodized aluminum.
E. Lens: High impact Polystyrene.

IV. REFERENCES

A. Bill of Material: MA-95301
B. Schematic: SA-96300
C. Container Assembly: B-95963
D. Outline Drawing:

V. PIN CONNECTIONS

1. -100VDC
2. Signal Input
3. Bias Voltage (See Chart I)
4. Ground

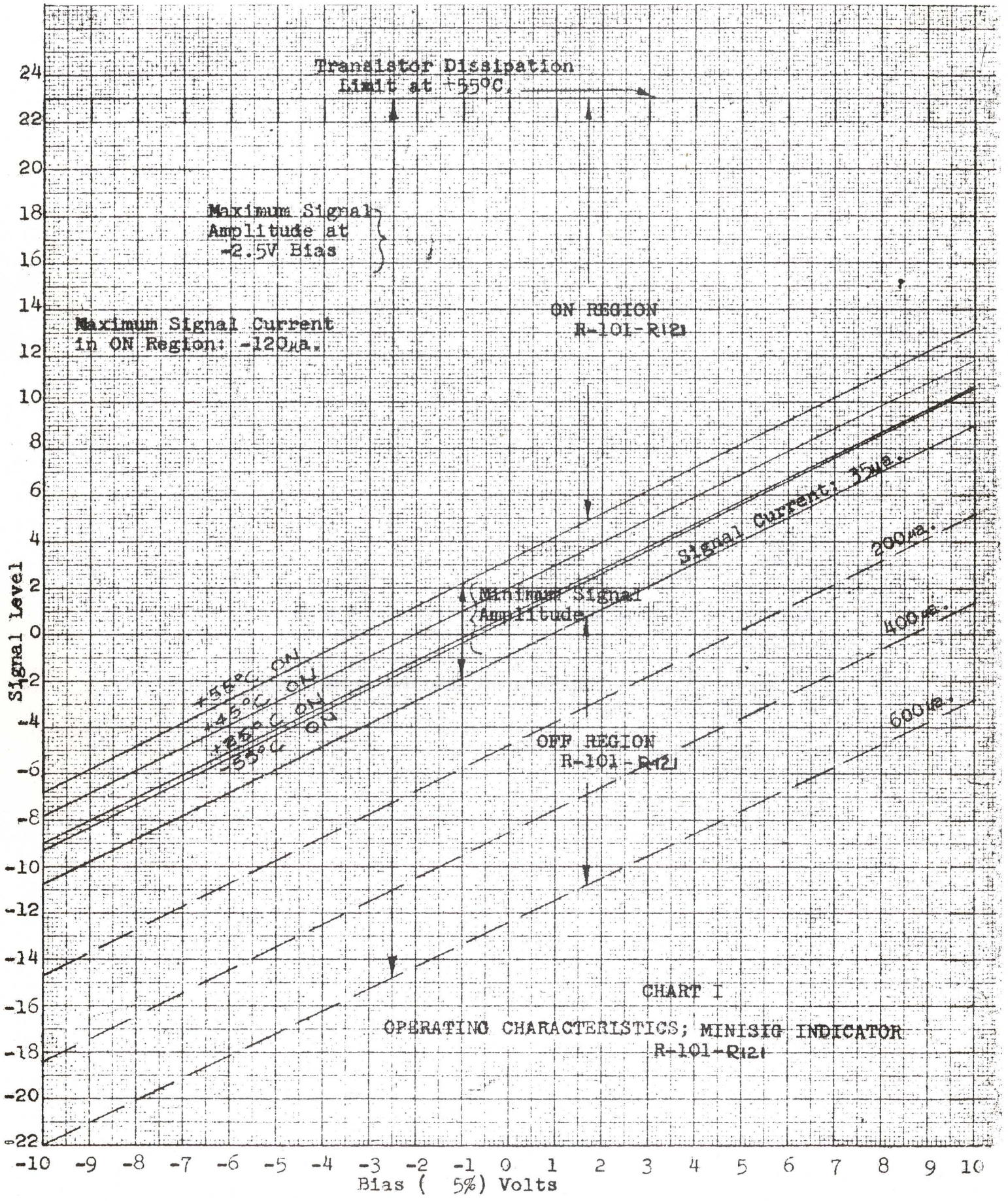
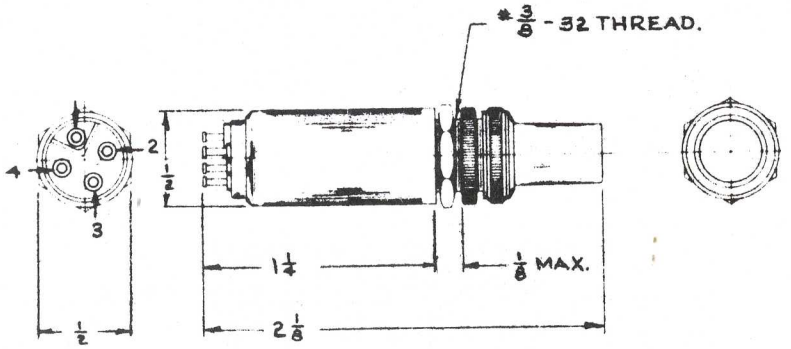


CHART I

OPERATING CHARACTERISTICS; MINISIG INDICATOR R-101-R121



I. GENERAL

The Minisig Indicator (R-221) is a high gain, transistorized neon indicator, useful for a visual display of various signal levels. The device is designed to accommodate small or medium amplitude signal excursions (4.0 volts peak-to-peak to 40 volts peak-to-peak or greater), and yields a visual indication for the most negative of two signal levels. The R-121 yields a visual indication for the most positive of two signal levels. A typical application of the device would be to indicate the static state of a flip-flop or other information storage element by a visual display.

II. ELECTRICAL SPECIFICATIONS

A. Input:

1. See Chart I for areas of operation.
2. Maximum loads imposed upon input signal:
   a. Neon on: >75μa, the limit being determined by the lower operating point.
   b. Neon off: -120μa.
3. Maximum negative input is -50 volts.

B. Output:

A visual display is given for the most positive of two signal levels to the input of the R-221.

C. Power Requirements:

1. -100 volts at 1.6 ma.
2. Bias voltage at 4 ma maximum (depending on input signal level and bias voltage). The voltage level is derived from Chart I.
3. Supply voltage tolerance: ± 5%.

III. MECHANICAL SPECIFICATIONS

A. Over-all Length: 2-19/32 inches.
B. Diameter: 1/2 inch.
C. Weight: 1/2 ounce (approximately).
D. Finish: Black anodized aluminum.
E. Lens: High impact Polystyrene.

IV. REFERENCES

A. Bill of Material: MA-96304
B. Schematic: SA-96303
C. Container Assembly: B-95963
D. Outline Drawing:

V. PIN CONNECTIONS

1. -100VDC
2. Signal Input
3. Bias Voltage (See Chart I)
4. Ground

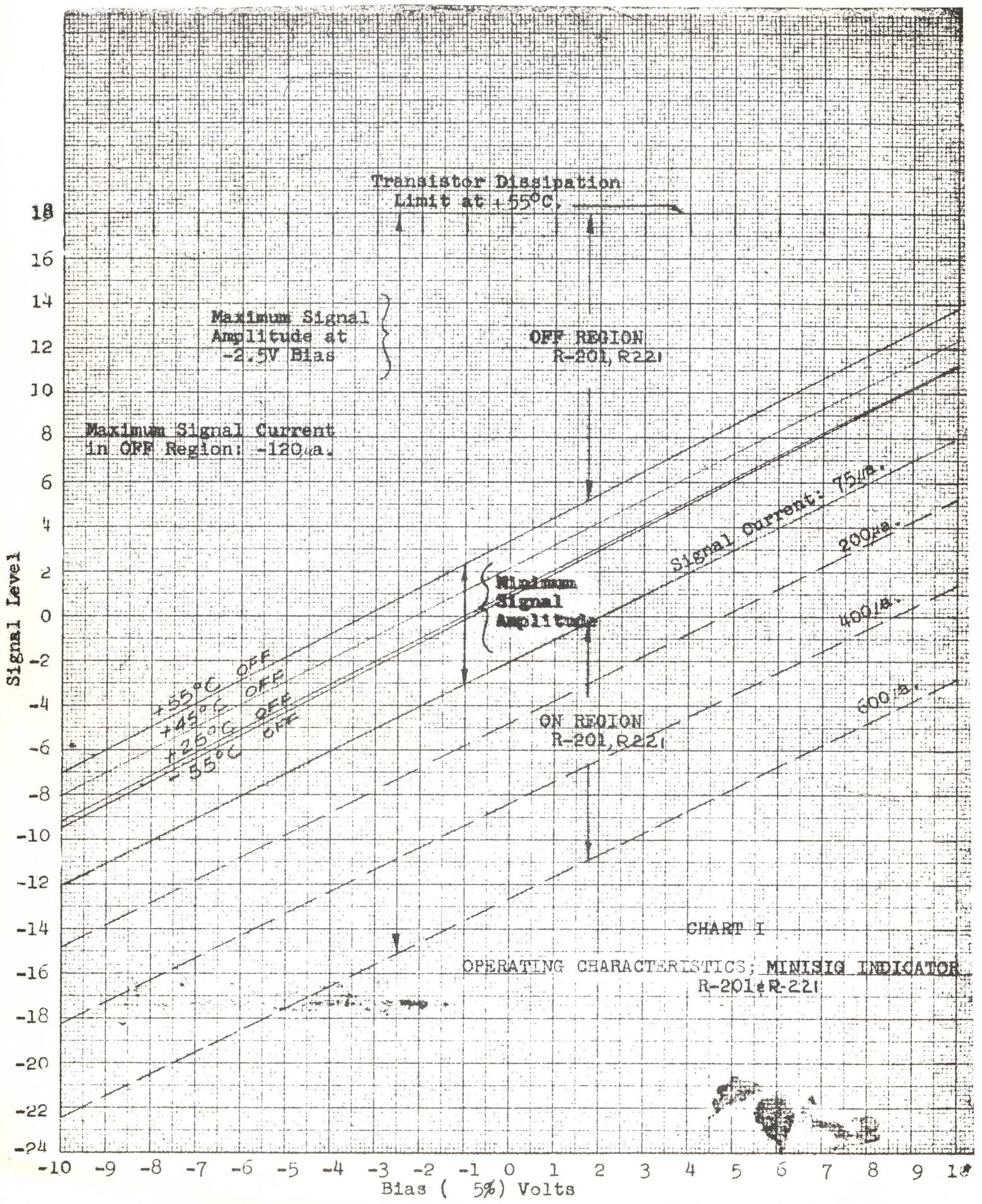
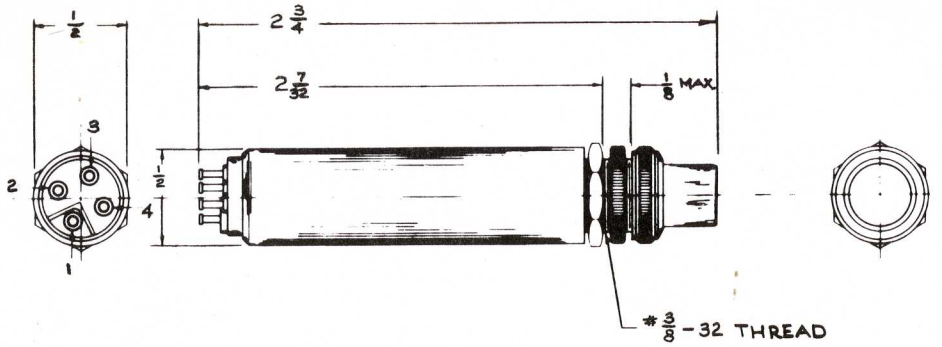


CHART I

OPERATING CHARACTERISTICS; MINISIG INDICATOR R-201 & R-221



I. GENERAL

The Lamp Minisig Indicator (R-441) is a high gain, transisterized. low voltage lamp indicator useful for a visual display of the T-Series signal levels. The circuit employs a low voltage incandescent lamp of high luminosity. The device yields a visual indication for the -11.0 V level. A typical application of the device would be to indicate the static state of a flip-flop or other information storage element by a visual display.

II. ELECTRICAL SPECIFICATIONS

A. Input:
   1. Amplitude: T-Series levels; -3.0 V, -11.0 V.
   2. Maximum load imposed upon input signal:
      a. Less than 0.1 ma. under normal conditions.

B. Output: A visual display is given for the -11.0 V level.

C. Power Requirements:

   1. +12.0 V at 1.6 ma.
   2. -12.0 V at 43.0 ma.
   3. Supply Voltage Tolerance: ± 10%.

III. MECHANICAL SPECIFICATIONS

A. Over-all Length: 2-19/32 inches.
B. Diameter: 1/2 inch.
C. Weight: 1/2 ounce (approximately).
D. Finish: Black anodized aluminum.
E. Lens: High impact polystyrene.

IV. REFERENCES

A. Bill of Material: MA-96182
B. Schematic: SA-96183
C. Container Assembly: 96200-4
D. Outline Drawing: A-96318
E. Application Chart: A-95578

V. PIN CONNECTIONS

1. -12.0 V.
2. Signal Input.
3. +12.0 V. (See chart)
4. Ground.