CHAPTER 6 Q10AD - A/D-D/A CONVERTER INTERFACE -

6.1. General

The Q10AD includes both an A/D converter and a D/A converter on one card, which is mounted in one of the option slots of the QX-10. Both of these devices can be used independently with the QX-10's software. The features of this card are described below.

(a) A/D converter

1) The A/D converter is equipped with 8 analog input channels, any one of which can be selected by command for input to the A/D converter.

2) Analog input signals in the range from -12 V to +12 V can be converted to digital data.

3) The maximum rate at which analog input signals can be sampled is 23.8 kHz; therefore, digital data can be obtained for analog signals with frequencies of up to 11.9 kHz.

4) Analog input signals are converted to 8-bit digital values in one of two selectable formats: offset binary or straight binary (described later).

(b) D/A converter

This converter outputs analog signals whose voltage varies according to the 8-bit digital data supplied from the QX-10 as follows:

Unipolar output: 0 V $\pm$10 mV to +5.1 V $\pm$10 mV
(Voltage changes by 20 mV for each change in the LSB of the digital value.)

Bipolar output : -5.1 V $\pm$10 mV to +5.1 V $\pm$10 mV
(Voltage changes by 40 mV for each change in the LSB of the digital value.)

6.2. I/O Map

The I/O map of the Q10AD changes according to the settings of jumpers J5A and J5B. At the time of shipment from the factory, jumper J5A is connected.
If jumper J5B is connected, "4" is added to all addresses indicated when jumper J5A is connected. Note that this will result in overlap with the I/O map for the Q10RS (RS-232C interface).
The I/O map is as indicated in the table below when jumper J5A is connected. Addresses indicated in parentheses apply when J5B is connected.

Address	Writes (OUT instruction)	Reads (IN instruction)
A0H (A4H)	Selects one of the analog channels for A/D conversion. Channels are selected by outputting the number of the desired channel to the data bus. The channel numbers are 0 to 7 (AIN0 - 7).	Inhibited.
A1H (A5H)	Executing an OUT instruction to this address starts A/D conversion. It does not matter what value is on the data bus.	Reads 8-bit data resulting from A/D conversion into the CPU.
A2H (A6H)	Writes digital values for D/A conversion. Writing data to this address latches the data and outputs the corresponding analog voltage to AOUT.	Inhibited.
A3H (A7H)	When the Q10AD is mounted in one of the option slots, a write to this address activates INTSL to generate an interrupt.	Reading this address inactivates INTSL (for acknowledgement). During A/D conversion, the D0 value on the data bus can be monitored to identify completion of A/D conversion (when D0 = 1).

6.3. A/D Converter

(a) A/D conversion procedures

A flow chart of A/D conversion procedures is shown in Fig. 6-1. These procedures are described below. (In the examples, it is assumed that jumper J5A is connected.)

1) Channel select

This step select one of the 8 analog input channels for A/D conversion. These 8 channels are designated AIN0 to AIN7, and the procedure for selecting one of these is to write the corresponding number to I/O address A0H. Once a channel has been selected, that channel is held until another channel selection is made; therfore, the channel selection need only be made once if only a certain channel is to be used. Further, channel AIN0 is selected by default upon reset.

Example: Selecting AIN3

```
LD A, 03H     ; LOAD CHANNEL NUMBER INTO A
OUT (0A0H), A; CHANNEL SELECT
```

2) Acquisition time (4 μs wait)

The sample holding circuit of the A/D converter is such that Max. 4 μs is required for the holding level of the output voltage to catch up when the input level changes from one sample to the next.

3) Start A/D conversion

A/D conversion is started by executing a Z-80 OUT instruction to write any data to I/O address 0A1H.

4) Detecting completion of A/D conversion

Completion of A/D conversion is detected either by interrupt or by monitoring the status of data bus bit D0.

i. Detection by interrupt

Depending on the jumper settings, the following interrupts become active when conversion is completed.

Jumper J3	Jumper J4A	Jumper J4B	Interrupt activated
o	x	x	INTSL
x	o	x	INTF1
x	x	o	INTF2
x	x	x	None

o: Jumper connected.
x: Jumper not connected.

Note: Do not connect more than one of these jumpers at a time.

ii. Detection by status

The status of conversion can be determined by reading I/O address 0A3H and checking the value of data bus bit D0.

D0 = 0: Conversion being performed.
D0 = 1: Conversion completed.

5) Read 8-bit data

The 8-bit digital value resulting from conversion of the analog input voltage can be determined by reading address 0A1H. The conversion format is determined by the setting of jumper J2 as follows:

i. Jumper J2 connected (offset binary format)

Bipolar analog input to A/D converter IC BA9101 is possible in the range from -2.55 V to +2.55 V. The digital value returned for -2.55 V is 00H, and that returned for +2.55 V is 0FFH. The LSB of the digital value output changes for each 20 mV shift in the analog input voltage.

ii. Jumper J2 disconnected (straight binary)

In this case, unipolar analog input to A/D converter IC BA9101 is possible in the range from 0 V to +5.1 V. The digital value returned for 0 V is 00H, and that returned for +5.1 V is 0FFH. The LSB of the digital value output changes with each 20 mV shift in the analog input voltage.

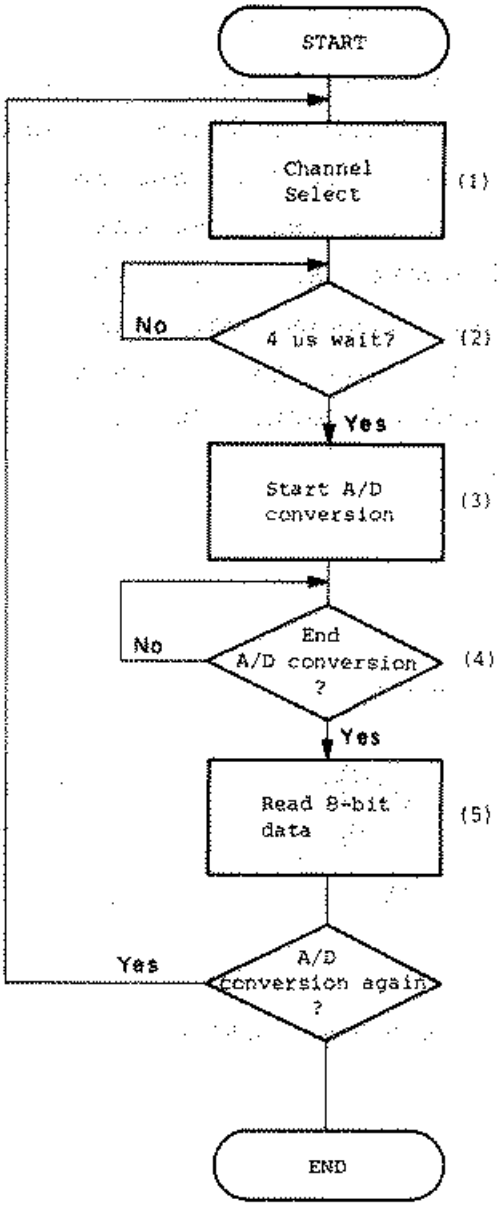

Fig. 6-1 Flow chart of A/D conversion

(b) Analog input channels AIN0 to AIN7

There are eight analog input channels, numbered AIN0 to AIN7, each of which is paired to GND. The settings of two DIP switches (SW1 and SW2) determine whether the input from the selected channel is fed directly to the A/D converter IC (BA9101) or to an operational amplifier (TL084A) which is used as a buffer to control the signal gain. In the latter case, input to the A/D converter IC is from the operational amplifier.
(See Fig. 6-2.)

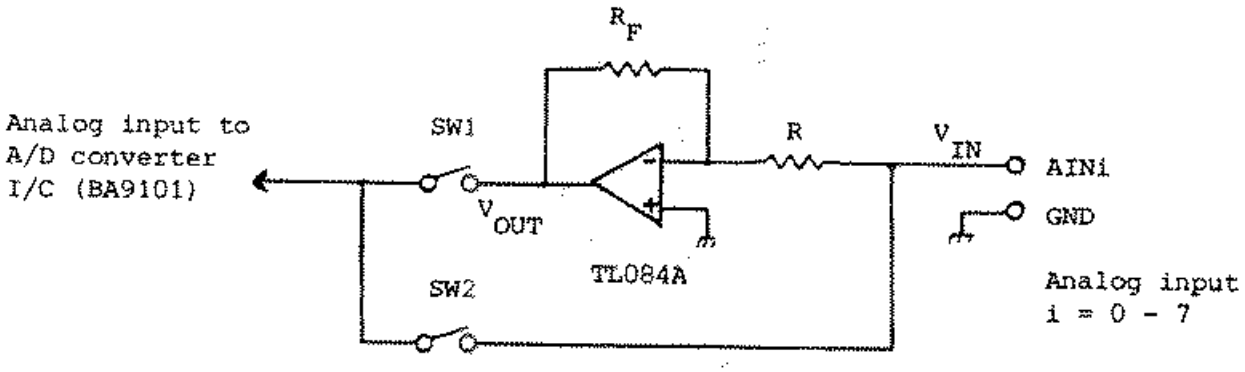

Fig. 6-2 Analog signal input stage

One or the other of these modes is selected as follows:

Mode 1: In this mode, SW1 is OFF and SW2 is ON, and the input signal voltage from channel AINi is fed directly to the A/D converter.

Mode 2: In this mode, SW1 is ON and SW2 is OFF, and the input gain from channel AINi is converted by operational amplifier TL0894A for input to the A/D converter.

When mode 2 is selected, the relationship between signal voltage V_{IN} and output voltage V_{OUT} after gain conversion is as indicated by the following expression.

$$V_{OUT} = - \frac{Rf}{R} V_{IN}$$

Thus, although the rated range of input voltages for the A/D converter IC (BA9101) is limited to 0 V to 5.1 V for direct binary conversion (or to -2.55 V to +2.55 V for binary offset conversion), selection of appropriate resistances makes it possible to increase the range to -12 V to +12 V by reducing the gain of the analog input signal. (The power supply voltage of the operational amplifier is +12 V.) In this case, it is necessary to note that the signal polarity is reversed and the amount of error increases as input levels approach 12 V.
Resistors R (R1 to R8) and Rf (R9 to R16) are not installed at the time of shipment from the factory, and must be installed by the user. See the schematic diagram for correspondence between the various channels and the resistors used for R and R_f.

The values used for R and R_f are primarily determined by the input offset current and the rated load of the operational amplifier.
The resistance of R should be in the range from 100 ohms to 10 kohms, and that of R_f should be in the range from 1 kohm to 1000 kohms.

Note: Do not set both DIP switches to ON simultaneously.

Correspondence between the bit numbers of the DIP switches and the analog input channels (AIN0 to AIN7) is shown in Table 6-1.
These bit numbers are printed on the circuit board.
These switches make it possible to determine the input mode for each channel independently.

Analog input channel	SW1 bit number	SW2 bit number
0	8	8
1	7	7
2	6	6
3	5	5
4	4	4
5	3	3
6	2	2
7	1	1

Table 6-1 Analog input channels and corresponding DIP switch bit numbers

(c) Internal reference voltage adjustment for A/D converter IC BA9101

The output voltage of A/D converter IC BA9101's internal reference voltage generator is adjusted by changing the setting of potentiometer VR3. Changing this setting adjusts the rate at which the least significant bit of the digital output data changes for shifts in the level of the analog voltage input to the A/D converter IC. See Fig. 6-3.

(d) Offset adjustment

Offset for the input voltage is adjusted by changing the setting of potentiometer VR2. See Fig. 6-4.

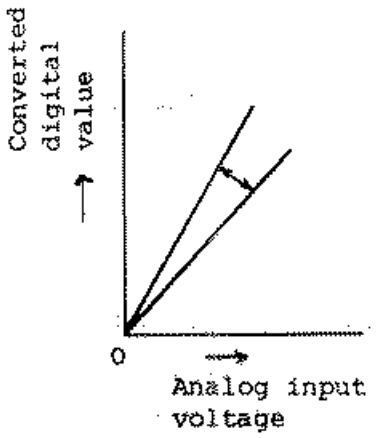

Fig. 6-3

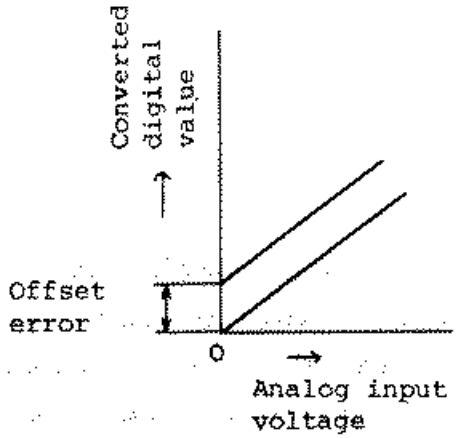

Fig. 6-4

(e) A/D conversion timing (A/D converter IC BA9101)

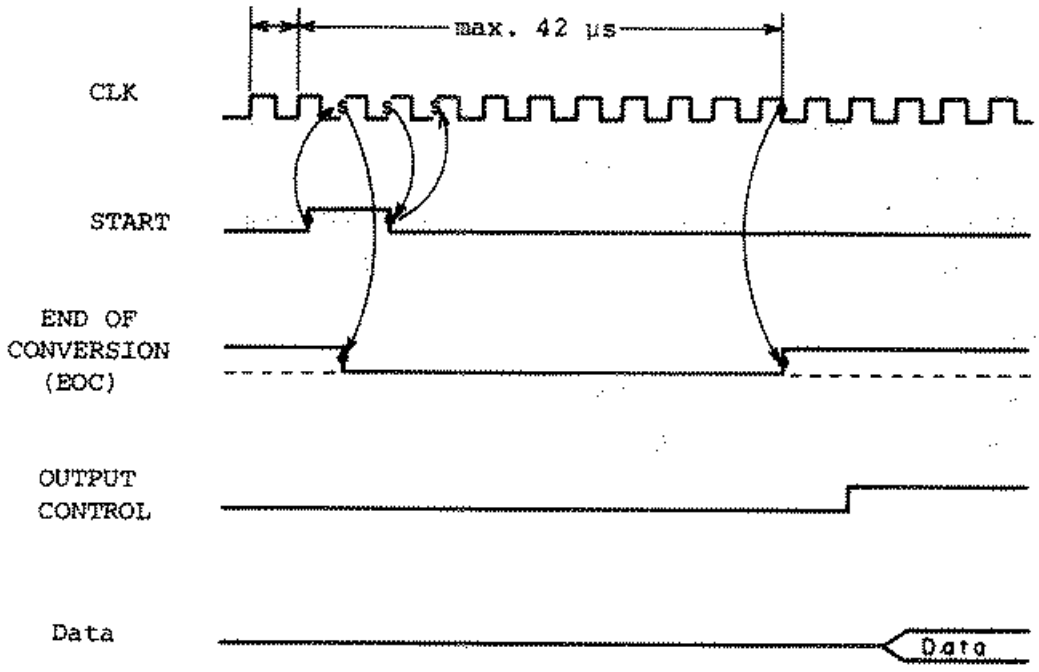

Fig. 6-5 A/D conversion timing chart

Conversion begins when EOC becomes "L" at the rising edge of the first CLK pulse after START becomes "H". EOC becomes "H" again (indicating that conversion has been completed) at the rising edge of the eighth CLK pulse after START drops back to "L". After the end of conversion, data is assured for a maximum of 220 ns after OUTPUT CONTROL rises.

(f) Sampling rate

As is indicated by the timing chart in (e) above, a maximum of 42 μs is required for one A/D conversion operation.

Sampling rate = 1/42 μs ≒ 23.8 kHz

Therefore, A/D conversion is possible for signals with frequencies up to 11.9 kHz even under the worst possible conditions.

(g) A/D converter linearity error

Although the LSB of the digital value produced by the A/D converter changes for each 20 mV change in the analog input voltage, it does not change at an accurate rate for variation in the analog input voltage within a certain range (which varies according to unit). Therefore, the digital values resulting from conversion do not precisely correspond to the analog input voltage. The maximum extent of this error is ±1 LSB.

(h) Procedure for adjusting the A/D converter

As shown in Table 6-2, the A/D converter should be adjusted so that digital values of 0, 1 and 254 are obtained for analog input voltages of 0 V, 20 mV and 5.08 V, respectively (during straight binary conversion). For offset binary conversion, adjust so that digital values of 0, 1 and 254 are obtained for analog voltages of -2.55 V, -2.53 V, respectively.

Type conversion	Analog input corresponding to 0	Analog input corresponding to 1	Analog input corresponding to 254
Straight binary	0 V	20 mV	5.08 V
Offset binary	-2.55 V	-2.53 V	+2.53 V

Table 6-2

Although the analog-digital characteristic can be adjusted based only on the two digital values 0 and 255, a line including error such as that indicated by B in Fig. 6-6 may result during straight binary conversion, even though the line indicated by A is ideal; therefore, the two point method is not recommended. The same applies to offset binary adjustment.

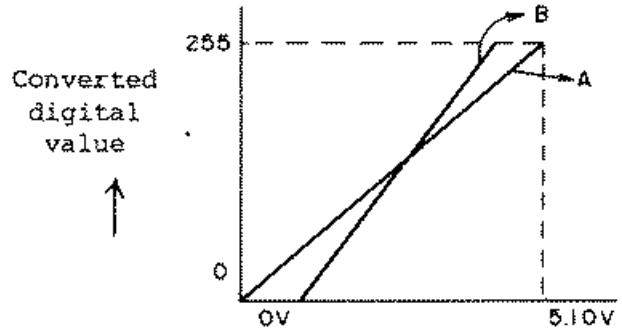

Fig. 6-6

6.4. D/A Converter

(a) Data is latched by outputting an 8-bit digital value to I/O address 0A2H (when jumper J5A is connected), then the corresponding analog voltage is output from AOUT. Whether the voltage output is bipolar or unipolar is determined by the setting of jumper J1A. Table 6-3 shows analog output voltages corresponding to digital values for both output formats.

Output format	Setting of J1A/B	Analog output for 00H	Analog output for 0FFH	Change in voltage for each change in LSB
Unipolar	A connected	0 V ±1.0 mV	+5.1 V ±10 mV	20 mV
Bipolar	B connected	-5.1 V ±10 mV	+5.1 V ±10 mV	40 mV

Table 6-3

Note: Jumper J1 A and B must not both be connected at the same time.

(b) Potentiometer VR1

VR1 controls the internal reference voltage of the D/A converter; this potentiometer is adjusted to bring the analog voltages resulting from D/A conversion into the ranges shown in Table 6-3.

(c) D/A converter error

When VR1 has been adjusted so that output voltages are in the ranges indicated in Table 6-3, analog output error will be less than the amount of change in voltage indicated for each change in the LSB of the digital value.

(d) Load

The maximum load which may be connected to the output terminal is 500 ohms.

6.5. Jumpers

Jumpers included on the option card are J1A, J1B, J2, J3, J4A, J4B and J5.

(a) J1A and J1B

These jumper determine whether the analog output resulting from D/A conversion is bipolar or unipolar. (See 6.4. "D/A Converter".)

(b) J2

This jumper sets the A/D converter for either bipolar or unipolar analog input. (See 5) "Reading data" in section 6.3. "A/D Converter".)

(c) J3, J4A and J4B

The settings of these jumpers determine which interrupt becomes active upon completion of A/D conversion. (See 4) "Detecting completion of A/D conversion" in section 6-3. "A/D Converter".)

(d) At the time of shipment from the factory, jumpers J1A, J2, J3 and J5A are connected.

6.6. DIP Switches

Two DIP switches, SW1 and SW2, are mounted on the option card. Turning the bits of these switches ON or OFF determines whether analog input from each of the 8 channels is input directly to the BA9101, or is buffered for input by operational amplifier TL084A. (See (b) of section 6.3. "A/D Converter".)
At the time of shipment from the factory, all bits of SW1 are set to OFF and all bits of SW2 are set to ON.

6.7. Potentiometers

Three potentiometers, VR1, VR2 and VR3, are mounted on the option card.

(a) VR1

This potentiometer controls the D/A converter's internal reference voltage.

(b) VR2

This potentiometer adjusts the A/D converter offset.

(c) VR3

This potentiometer controls the A/D converter's internal reference voltage.

* At the time of shipment from the factory, VR1 is adjusted so that unipolar characteristics are as shown in Table 6-3.

6.8. Resistors

Resistors R1 to R16 determine the gain of the operational amplifier. These resistors are not installed at the factory, and must be installed by the user.

6.9. Connector Pin Assignments

Pin numbers and signal names for the interface connector to the QX-10 are as shown in the table below.

Pin No.	Signal name	Function	Pin No.	Signal name	Function
1	GND	GND	20	AD7	Address bus 7
2	GND	GND	29	GND	GND
3	D0	Data bus 0	30	GND	GND
4	D1	Data bus 1	31	CLK	Clock
5	D2	Data bus 2	32	GND	GND
6	D3	Data bus 3	33	$\overline{\text{BSAK}}$	Bus acknowledge
7	D4	Data bus 4	34	$\overline{\text{IRD}}$	I/O read
8	D5	Data bus 5	35	$\overline{\text{IWR}}$	I/O write
9	D6	Data bus 6	40	INTF1	INTF1
10	D7	Data bus 7	41	INTF2	INTF2
13	AD0	Address bus 0	42	INTSL	INTSL
14	AD1	Address bus 1	43	+5 V	+5 V
15	AD2	Address bus 2	44	$\overline{\text{RESET}}$	Reset signal
16	AD3	Address bus 3	45	+5 V	+5 V
17	AD4	Address bus 4	46	+5 V	+5 V
18	AD5	Address bus 5	59	GND	GND
19	AD6	Address bus 6	60	GND	GND

6.10. External Interface

Pin numbers and corresponding signals for the analog output (AOUT) and analog input (AIN0 to AIN7) connector are as shown in the table below.

Pin No.	Signal	Function
1	AOUT	Analog signal output after D/A conversion
2	GND	Ground
3	AIN0	Analog input channel 0
4	GND	Ground
5	AIN1	Analog input channel 1
6	GND	Ground
7	AIN2	Analog input channel 2
8	GND	Ground
9	AIN3	Analog input channel 3
10	GND	Ground
11	AIN4	Analog input channel 4
12	GND	Ground
13	AIN5	Analog input channel 5
14	GND	Ground
15	AIN6	Analog input channel 6
16	GND	Ground
17	AIN7	Analog input channel 7
18	GND	Ground
19	GND	Ground
20	GND	Ground