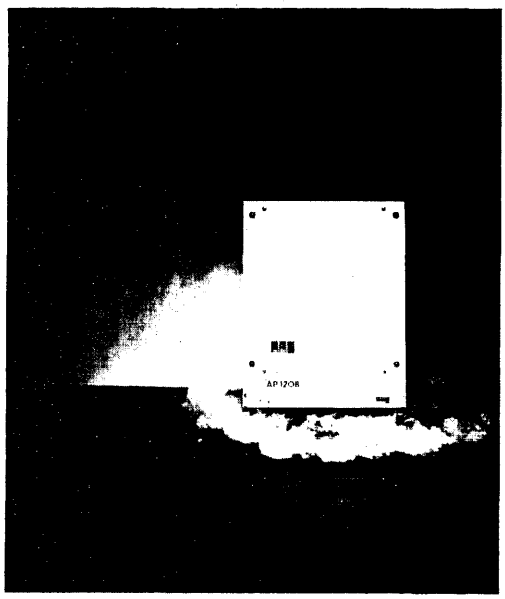
FLOATING POINT SYSTEMS, INC.

AP-120B

FLOATING POINT ARRAY PROCESSOR



FEATURES

- Fast Floating-point arithmetic -- 167ns
- Enhanced computing accuracy
- Powerful 64-bit instructions
- Multiple high-speed memories
- Numerous hardware registers
- Multiple data paths
- Overlap input/processing/output
- Efficient data width
- Intelligent interface
- Flexible format conversion
- DMA to Peripherals
- Reliable synchronous design
- Extensive software support
- High accuracy & range

DESCRIPTION

The AP-120B floating-point array processor gives a unique combination of computational capability to mini and maxi-computer systems. The high-speed, high-accuracy floating-point operations and programmability greatly increase system flexibility and throughput. Formatting hardware and interface logic provide full control of AP-120B and host interaction; an internal 38-bit floating-point format gives extra precision. Multiple accumulators, registers and data paths give ready access to data. Separate internal memories avoid accessing conflicts. A variety of mathematical functions and software packages allow the user to upgrade his existing computer system to handle heavy computational loads.

ARITHMETIC

The AP-120B performs floating-point arithmetic at maxi-computer speeds. Separate multiplier and adder units operate concurrently. The two-cycle pipelined adder completes a normalized, convergently rounded floating-point add (or subtract, fix, float, absolute value, logical And, Or, Equivalence) every 167ns. The three-cycle pipelined multiplier completes a normalized, convergently rounded floating-point multiply every 167ns.

Each unit detects overflow and underflow error conditions, forcing the result to the proper signed maximum value or zero, and setting the appropriate error flag.

ACCURACY

The floating-point adder and multiplier both contain special hardware to provide an extra cushion of accuracy for each computational step.

The adder has three extra bits (equal to 28 extra bits for normalized arguments) to preserve information shifted right during exponent alignment for use later during normalization and convergent rounding. The binary floating-point format further minimizes loss of resolution.

The multiplier computes the entire 56-bit fractional product, and then normalizes and convergently rounds to 28-bits.

Convergent rounding hardware in both arithmetic units rounds the normalized result up only when the remainder is greater than one half of the least significant bit. This causes the cumulative rounding error bias to converge toward zero.

INSTRUCTIONS

A single AP-120B instruction handles operations that would require several successive instructions on most computers. Each 64-bit instruction is divided into 10 powerful command fields, allowing a single instruction to perform a variety of tasks:

Floating-point add
Floating-point multiply
Fetch or store from Data memory
Read and store accumulators (two reads and two writes)
Conditional branching
Fetch from Table memory
Index register arithmetic

All transfers, computations, and memory accesses occur synchronously. No special programmed testing is needed to insure proper execution.

The AP-120B has three separate high-speed memories, each with dedicated controller logic. Multiple memories eliminate accessing conflicts, allow an optimal word length and cycle speed for each, and provide flexibility in configuring for specific applications.

Program Memory: 64-bit word size; 50ns cycle bipolar memory in 256 word increments. Addressable to 4K words.

Data Memory: 38-bits word size; either 167ns interleaved cycle MOS memory in 4K word increments, or 333ns interleaved cycle MOS memory in 8K word increments. Two parity bits are optional. Addressable to 1 Megawords.

Table Memory: 38-bit word size, 167ns cycle bipolar ROM in 512 word increments. Addressable to 64K words. Optional 167ns RAM table memory available in 1024 word increments up to 64K.

ACCUMULATORS AND REGISTERS

The AP-120B has 64 floating-point accumulators. Four accumulators are available during any instruction cycle; two as argument sources and two as result destinations.

The 16 integer index registers permit address calculations and loop overhead to occur concurrently with floating-point arithmetic. Data arrays may be indexed in either true or bit-reversed order.

DATA PATHS

Four separate 38-bit wide data paths into the floating-point adder and multiplier allow an uninterrupted flow of arguments for computation. Three additional data paths concurrently channel results back into accumulators or memory. This combination of multiple data paths allows sustained computational throughput, and avoids intermediate data moves. DMA cycle stealing allows overlapped data input, arithmetic processing, and data output.

DATA WIDTHS

Three distinct data widths are used to fit each particular data type: instructions, floating-point numbers and integers.

The 64-bit instruction word permits up to 10 different instructions to be programmed concurrently in a single 167ns processor cycle.

The 38-bit floating-point data word gives both extra computing accuracy and increased dynamic range over traditional 32-bit word lengths (8.1 vs 6.0 decimal digits, with a dynamic range of over 10^{+153}).

The 16-bit integer word allows direct memory addressing to 65,536 words; and to 1 million words with memory bank selection.

INTERFACE

An intelligent interface coordinates interaction between the AP-120B processor and the host computer.

The AP-120B electronic front panel gives the host computer access inside the AP-120B. The internal memories and registers may be examined and modified. A hardware break-point can be set to stop AP-120B execution at a selected program location or data address.

Programs may be single stepped for debugging purposes, with execution identical to free-running programs.

The interface provides four data transfer combinations between the two processors: host DMA to AP-120B DMA; Host DMA to AP-120B programmed I/O; host programmed I/O to AP-120B DMA; and host programmed I/O to AP-120B programmed I/O. Either the AP-120B or the host computer can control data transfers.

FORMAT CONVERSION

The formatting hardware in the AP-120B interface converts data "on-the-fly" during transfers between the AP-120B and host or peripherals. Four standard formats are automatically handled and many options are available.

Host Computer Format to AP-120B Format

16-bit integers	– 38-bit unnormalized floating point
32-bit integers	– 32-bit integers
IBM 360 floating point	– 38-bit normalized floating point
Host floating point	– 38-bit normalized floating point

On return of results to the host, any floating-point numbers that would be out of range for the target format are detected and forced to the proper signed maximum or zero, and indicator bits set.

PERIPHERALS

A separate programmed I/O and direct memory access bus is provided for peripheral devices (A/D converters, disks, tape drives, etc.) to be interfaced directly to the AP-120B. Up to 256 I/O device addresses can be accommodated.

RELIABILITY

A single master clock synchronizes processor actions in the AP-120B. There is no uncertainty caused by inter-element "hand-shaking", not variable phasing delays.

Timing allowances are designed to worst case temperature and voltage operating specifications – a full 50% safety margin in every cycle.

Units are tested as a functioning system at extremes of heat and supply voltage: a minimum of eight successful hours at high temperature, high voltage and again at low temperature, low voltage.

The high-speed Schottky MSI and LSI TTL logic is pre-conditioned and parametrically tested to eliminate "infant mortality".

COMPACT PACKAGING

The AP-120B is arithmetic power in a compact package. The chassis mounts in standard 19' rack and occupies 24½" of space, including a high-efficiency switching regulated power supply. Rugged mechanical design and moderate card size (10" x 15") maximize system integrity in the field.

SOFTWARE SUPPORT

An extensive package of library functions, vector and matrix subroutines, and signal processing algorithms is supplied with the AP-120B; all callable from the host computer's FORTRAN programs. A cross assembler, program linker, on-line debugger (using the electronic front panel) and software simulator aid in new program development.

ALGORITHM EXECUTION TIMES*

Multiply-add: 167ns
Complex multiply: 667ns

Algorithm	167ns memory	333ns memory
1024 pt real FFT	2.7 ms	4.2 ms
1024 pt complex FFT	4.8 ms	7.0 ms
8192 pt real FFT	26.1 ms	38.7 ms
1024 pt vector elem. by elem. mult.	0.52 ms	1.05 ms
1024 x 32 pt convolution	6.0 ms	6.5 ms
512 x 512 real 2 DIM FFT	1.55 sec	2.2 sec
1000 element vector square root	1.85 ms	1.85 ms

*Established by benchmarks at user installations.

SPECIFICATIONS

ARITHMETIC

Floating-point width: 38-bits
Floating-point adds: every 167ns, 333ns for completion
Floating-point multiples: every 167ns, 500ns for completion
Integer width: 16-bits
Integer arithmetic: 167ns

MEMORY

Cycle:	Program Memory, (bipolar RAM); Data Memory, 167ns interleaved or 333ns interleaved (MOS); Table Memory, 167ns (bipolar ROM).
Sizes:	Program Memory, increments of 256 words to 4K words; Data Memory, increments of 2K words (167ns) or 8K words (333ns) to 1 million words; Table Memory, increments of 512 words to 64K words.
Word Sizes:	Program Memory, 64-bits. Data Memory, 38-bits, plus two optional parity bits Table Memory, 38-bits.

REGISTERS

Floating-point Accumulators: 64
Index registers: 16
Subroutine return stack: 16

INPUT/OUTPUT

Direct memory access rate: Up to 3 million 38-bit words per second, depending upon the host computer.

Input/Output System, 38-bit word length, 256 devices addressable. An ancillary DMA port allows the AP-120B to communicate with other peripherals, such as disc memory A/D and D/A converters, etc.

ELECTRICAL

Power service: 105/125 at 20 amps or 188/228 Vac, or 210/250 Vac at 10 amps. 50/60 Hz. 50/400 Hz optional.

Power Dissipation with 512 words of Program Memory, 16K Data Memory, and 2K Table Memory; less than 1200 watts.

ENVIRONMENTAL

Temperature Range: 10 to 40°C operating

Relative humidity range: 0-90%
Ventilation: 8 push-pull fans.

PHYSICAL

Dimensions: 24½" H, 19" W, 20"-25" D
Weight: 88 pounds including power supplies

FLOATING POINT SYSTEMS, INC.

P.O. Box 23489, Portland, OR 97005
11000 S.W. 11th, Beaverton, OR 97223
(503) 641-3151, TLX: 360470, FLOATPOINT PTL

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