FUJITSU

M2622T/M2623T/M2624T

Intelligent Disk Drive
Engineering Specifications

41FH5066E . . . 01

REVISION RECORD

Edition	Date published	Revised contents
01	Oct., 1991	

Specification No.: 41FH5066E

FB118195

Comments concerning this manual should be addressed to one of the following addresses:

FUJITSU LIMITED
International Marketing
Marunouchi 1-6-1, Chiyoda-ku, Tokyo 100 JAPAN
TEL: 03-216-3211
FAX: 03-213-7174, 03-216-9353
TLX: J22833
Cable: "FUJITSU LIMITED TOKYO"

FUJITSU COMPUTER PRODUCTS
OF AMERICA, INC.
2904 Orchard Parkway, San Jose, California 95134-2029, U.S.A.
TEL: (1-408) 432-6333
FAX: 408-894-1709, 3908

FUJITSU CANADA, INC.
2800 Matheson Blvd. East, Mississauga
Ontario, L4W 4X5, CANADA
TEL: (1-416) 602-5454
FAX: 416-602-5457
TLX: 968132

FUJITSU EUROPE LIMITED
2, Longwalk Road, Stockly Park,
West Drayton, Middlesex UB11 1AB, ENGLAND
TEL: (44-81) 573-4444
FAX: 81-573-2643
TLX: 263871FEL SP G

FUJITSU DEUTSCHLAND GmbH
Rosenheimerstraße 145, D-8000 München 80, F.R. GERMANY
TEL: (49-89) 32378142
FAX: 89-32378102 or 3
TLX: 897106 FDG D

FUJITSU NORDIC AB
Torggatan 8, 171 54, Solna, SWEDEN
TEL: (46) 8-764-76-90
FAX: 8-28-03-45
TLX: 13411 FNAB S

FUJITSU ITALIA S.p.A.
Via Melchiorre Gioia, 8, 20124 Milano, ITALY
TEL: (39-2) 6572741
FAX: 2-6572257
TLX: 350142 FJITLY I

FUJITSU FRANCE S. A.
17, rue Olof Palme-94006 Créteil cedex, FRANCE
TEL: 33-1-43-99-40-00
FAX: 33-1-43-99-07-00
TLX: 262661

FUJITSU AUSTRALIA LIMITED
475 Victoria Avenue, Chatswood, N.S.W. 2067, AUSTRALIA
TEL: (61-2) 410-4555
FAX: 2-411-8603, 8362
TLX: 25233

FUJITSU HONG KONG LIMITED
R.M. 1831, Sun Hung Kai Centre, 30 Harbour Road,
HONG KONG
TEL: (852-5) 8915780
FAX: 5-742917
TLX: 62667

FUJITSU ESPAÑA, S.A.
Edificio Torre Europa, Paseo de la Castellana 95, Madrid 28046, SPAIN
TEL: (34-1) 581-8000
FAX: 1-581-8300
TLX: 23887

The contents of this manual are subject to change without prior notice.

This page is intentionally left blank.

LIST OF EFFECTIVE PAGES

PAGE	REV
Cover	01
Blank	—
i	01
ii	01
iii	01
iv	01
v	01
vi	01
vii	01
viii	01
ix	01
x	01
xi	01
xii	01
1-1	01
1-2	01
1-3	01
1-4	01
1-5	01
1-6	01
1-7	01
1-8	01
1-9	01
1-10	01
2-1	01
2-2	01
2-3	01
2-4	01
3-1	01
3-2	01
3-3	01
3-4	01
3-5	01
3-6	01
3-7	01
3-8	01
3-9	01
3-10	01
3-11	01
3-12	01
3-13	01
3-14	01
3-15	01
3-16	01
4-1	01
4-2	01
4-3	01
4-4	01
4-5	01
4-6	01
4-7	01

PAGE	REV
4-8	01
4-9	01
4-10	01
4-11	01
4-12	01
4-13	01
4-14	01
4-15	01
4-16	01
4-17	01
4-18	01
4-19	01
4-20	01
4-21	01
4-22	01
4-23	01
4-24	01
4-25	01
4-26	01
4-27	01
4-28	01
5-1	01
5-2	01
5-3	01
5-4	01
5-5	01
5-6	01
5-7	01
5-8	01
6-1	01
6-2	01
6-3	01
6-4	01
6-5	01
Blank	—
Reader Comment Card	—
Blank	—
Cover	01

PREFACE

This manual describes the M262xT, a 3.5-inch hard disk drive with a BUILT-IN controller that is compatible with the IBM PC-AT interface.

This manual explains, in detail, how to incorporate the magnetic disk drives into user systems.

This manual assumes that users have a basic knowledge of hard disk drives and their application in computer systems.

This manual consists of the following six chapters:

Chapter 1 DEVICE OVERVIEW

Chapter 2 DEVICE CONFIGURATION

Chapter 3 INSTALLATION CONDITIONS

Chapter 4 HOST INTERFACE

Chapter 5 DATA FORMAT

Chapter 6 OTHERS

In this manual, disk drives may be referred to as IDD, drives, or devices.

IBM PC-AT is a registered trademark of IBM (International Business Machines Corporation) of the United States of America.

This page is intentionally left blank.

LIABILITY EXCEPTION

"Disk drive defects" refers to defects that involve adjustment, repair, or replacement. Fujitsu is not liable for any other disk drive defects, such as those caused by user misoperation or mishandling, inappropriate operating environments, defects in the power supply or cable, problems of the host system, or other causes outside the disk drive.

This page is intentionally left blank.

CONTENTS

FIGURES

This page is intentionally left blank.

TABLES

This page is intentionally left blank.

CHAPTER 1 DEVICE OVERVIEW

1.1 Overview

The M262xT is a 3.5-inch hard disk drive with a BUILT-IN controller. The disk drive is compact and reliable, and is compatible with the IBM PC-AT interface.

1.2 Features

(1) Compact

A DC motor, directly coupled to the spindle, drives a disk of 95 mm diameter. The controller is mounted on the PCA of the disk drive, making the entire unit very compact.

(2) Large capacity

Although this device uses a 3.5-inch disk as the recording media, a maximum recording capacity of 608 MB (unformatted) is possible. This is achieved by dividing all cylinders into four areas to make the recording density the same for each area (constant-density recording).

(3) Connection to IBM PC-AT interface

With the BUILT-IN PC-AT interface compatible controller, the device can be connected to an extension slot of a personal computer via a simple adapter board. The adapter board consists of an address decoder and a driver/receiver (74LS244/245 or equivalent).

(4) 64-KB data buffer

The disk drive uses a 64-KB data buffer to transfer data between the host and the disk media.

In combination with the read-ahead cache system described in (5), the buffer contributes to efficient I/O processing.

(5) Read-ahead cache system

After the execution of a disk read command, the disk drive automatically reads the subsequent data block and writes it to the data buffer (read ahead operation). This cache system enables fast sequential data access. The next disk read command would normally cause another disk access. But, if the read ahead data corresponds to the data requested by the next read command, the data in the buffer can be transferred instead.

(6) High-speed transfer rate

The device uses a 30 MHz clock for data transfer to and from the host. Efficient buffer management enables high-speed data transfer at 3.7 MW/s.

The host must synchronize data transfer by sending the IORDY (I/O Channel Ready) signal to insert a WAIT state if the transfer rate is 3.7 MW/s or more.

(7) Error correction and retry by ECC

If a recoverable error occurs, the disk drive itself attempts error recovery. The seven-byte ECC has improved buffer error correction for correctable data errors.

(8) Self-diagnosis

The disk drive has a diagnostic function to check operation of the controller and disk drive. Executing the diagnostic command invokes self-diagnosis.

(9) High reliability

The head and positioner are completely sealed. Circulation and respiration filters clean the environment within the disk enclosure, improving device reliability and minimizing the risk of a head crash.

(10) Fast positioning

Use of a rotary voice coil motor in the head positioning mechanism greatly increases the positioning speed.

(11) Low power consumption and wide-ranging operating temperature

The disk drive consumes little power through the use of LSI devices and other techniques. The disk drive can be used over a wide temperature range (5°C to 45°C).

(12) Low noise and vibration

In Ready status, the noise of the disk drive is only about 43 dB (characteristic A). This makes the drive very suitable for office use.

The supporting mechanism features rubber mounts that prevent vibration from being transmitted outside.

1.3 Device Specifications

1.3.1 Device specifications

Table 1.1 Device specifications

Model		M2622T	M2623T	M2624T
Format capacity/drive (*1)		326.75 (MB)	420.16 (MB)	513.51 (MB)
Number of heads (data + servo)		7+1	9+1	11+1
Number of cylinders (user + CE + SA)		1429 + 1 + 5		
Recording method		1/7 RLL		
Track density		1,751 (TPI)		
Bit density		46,383 (BPI)		
Speed		4,400 ±0.5% (rpm)		
Average revolution wait time		6.82 (ms)		
Positioning time	Minimum	3 (ms)		
	Average	12 (ms)		
	Maximum	25 (ms)		
Start/stop time	Start	15 (s) or less		
	Stop	30 (s) or less		
Interface		PC-AT Maximum cable length; 0.5 (m)		
Data transfer rate	Disk drive	2.44 to 3.05 (MB/s)		
	Controller	3.7 (MW/s) Max.		
Theoretical data block length (fixed length)		512 (B)		
PC-AT command specifications		Compatible with PC-AT support command (considering ATA)		
Data buffer		64 (Kbytes), with read-ahead cache system		
Dimensions (h x d x w)		41.3 (mm) × 146.0 (mm) × 101.6 (mm)		
Weight		About 1.2 (kg)		

*1: Capacity when the disk drive is configured as follows:

M2622T : CYL 1013/ HD 10/ SCT /TRK 63
M2623T : CYL 1002/ HD 13/ SCT /TRK 63
M2624T : CYL 995/ HD 16/ SCT /TRK 63

1.3.2 Model and product number

Many types of disk drives are available for each model, varying mainly in the presence of a bezel (front panel) and types of mounting screws. Table 1.2 lists the model names and product numbers.

Table 1.2 Model names and product numbers

Model name	Total storage capacity (user area)	Bezel	Mounting screws	Product No.
M2622T	326.75 MB	Included	M3	B03B-7195-B304A
		Not included	M3	B03B-7195-B304A#P
		Included	#6-32UNC	B03B-7195-B304A#N
		Not included	#6-32UNC	B03B-7195-B304A#NP
M2623T	420.16 MB	Included	M3	B03B-7195-B305A
		Not included	M3	B03B-7195-B305A#P
		Included	#6-32UNC	B03B-7195-B305A#N
		Not included	#6-32UNC	B03B-7195-B305A#NP
M2624T	513.51 MB	Included	M3	B03B-7195-B306A
		Not included	M3	B03B-7195-B306A#P
		Included	#6-32UNC	B03B-7195-B306A#N
		Not included	#6-32UNC	B03B-7195-B306A#NP

1.3.3 Positioning time

Figure 1.1 graphs the positioning time.

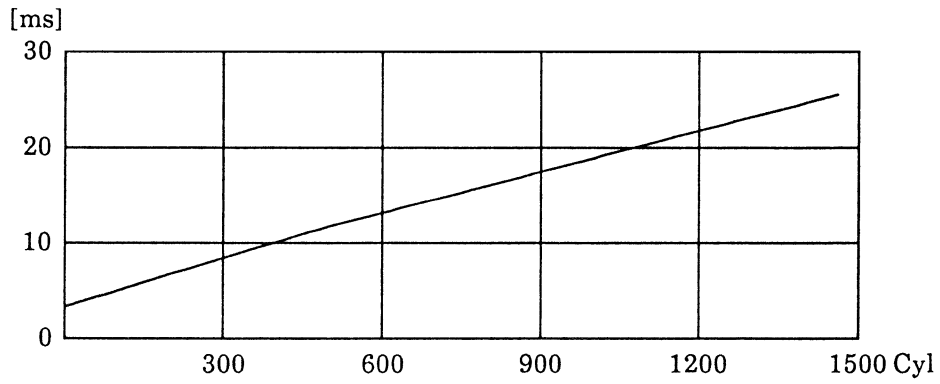


Figure 1.1 Positioning time

1.3.4 Typical start and stop times

The typical start time is 9 seconds or less. The typical stop time is 23 seconds or less.

1.4 Operating Conditions

Table 1.3 lists the environmental conditions.

Table 1.3 Environmental conditions

Item		Conditions
Operature (*1)	Operating ambient temperature	5°C to 45°C
	Stand-by ambient temperature	– 40°C to 60°C
	Operating disk enclosure surface temperature	60°C or less
	Operating disk enclosure surface temperature range	(Variable span) 55°C or less
	Slope	15°C/H or less
Humidity	Operating	20% to 80% RH
	Stand-by	5% to 95% RH
	Highest wet bulb temperature	29°C (no condensation)
Vibration resistance	Operating	0.5 G (5 to 250 Hz) or less
	Stand-by (*2)	2.0 G (5 to 250 Hz) or less
Physical shock	Operating	5 G (10 ms max.) or less
	Stand-by	50 G (10 ms max.) or less
Altitude	Operating	0 to 3,000 m above sea level
	Stand-by	0 to 12,000 m above sea level

*1: Details are described in Section 3.2.
*2: Power-off status after installation.

1.5 Power Supply Conditions

(1) Input power supply

	Voltage	Current	
		Peak	Average
+12V	+12V±5%	2.5 A	0.5 A
+5V	+5V±5%	———	0.8 A

The above voltage is measured at the receiving end (connector) of the disk drive.

(2) Ripple

+5V : 50mV$_{PP}$ or less
+12 V : 100 mV$_{PP}$ or less
High frequency noise : 100mV$_{PP}$ or less

(3) Current consumption (Typ.)

	Seek	W/R	Ready
+12V	0.6A	0.5A	0.45A
+5V	0.8A	0.8A	0.8A

(4) Power consumption (Typ.)

Seek	W/R	Ready
11W	10W	9.5W

(5) Current fluctuation (Typ.) at +12 V when power is turned on

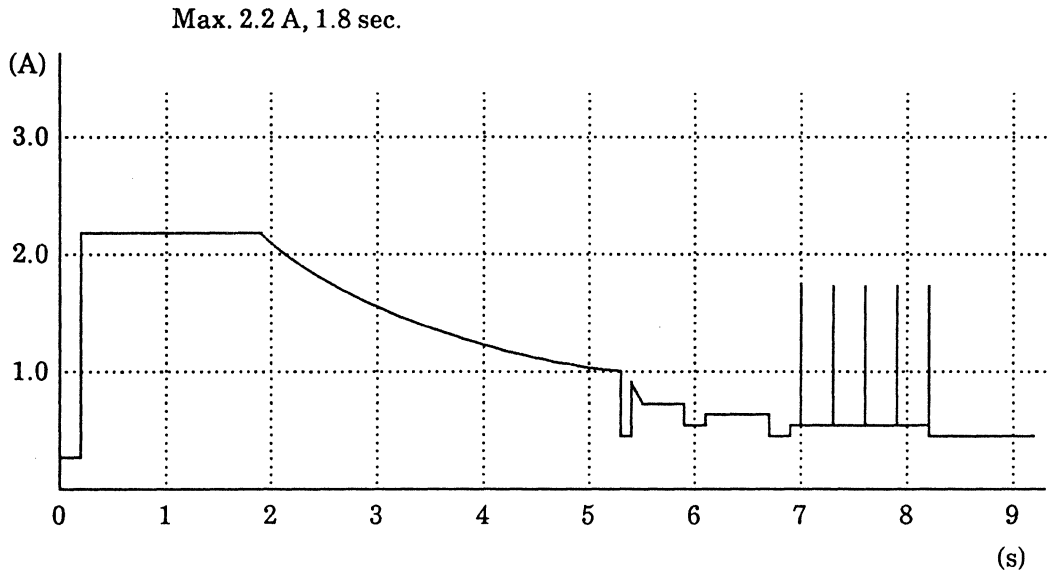


Figure 1.2 Current fluctuation (Typ.) at +12 V when power is turned on

(6) Power on/off sequence

The voltage detector circuit monitors +5 V and +12 V. The circuit does not allow a write signal if either voltage is abnormal. This prevents data from being destroyed and eliminates the need to be concerned with the power on/off sequence.

However, the +5 V and +12 V voltages must be turned on within three seconds or less. If the +12 V is turned on more than three seconds after the +5 V is turned on, an error is reported in Diagnostic mode (02H is set in the error register).

1.6 Reliability

(1) Mean time between failures (MTBF)

The mean time between failures (MTBF) is 200,000 H or more (operation: 24 hours/day, 7 days/week). This does not include failures occurring during the first three months after installation.

MTBF is defined as follows:

$$\text{MTBF} = \frac{\text{Total operation time in all fields}}{\text{number of device failures in all fields}} \text{ (H)}$$

*1: "Disk drive defects" refers to defects that involve repair, readjustment, or replacement. Disk drive defects do not include failures caused by external factors, such as damage caused by handling, inappropriate operating environments, defects in the power supply host system, or interface cable.

(2) Mean time to repair (MTTR)

The mean time to repair (MTTR) is 30 minutes or less, if repaired by a specialist maintenance staff member.

(3) Service life

In situations where management and handling are correct, the disk drive requires no overhaul for five years or 20,000 hours of operation, whichever occurs first.

(4) Data assurance in the event of power failure

Except for the data block being written to, the data on the disk media is assured in the event of any power supply abnormalities. This does not include power supply abnormalities during disk media initialization (formatting) or processing of defects (alternative block assignment).

1.7 Error Rate

Known defects, for which alternative blocks can be assigned, are not included in the error rate count below. It is assumed that the data blocks to be accessed are evenly distributed on the disk media.

(1) Unrecoverable read error

Read errors that cannot be recovered by eight read retries and ECC corrections shall occur no more than 10 times when reading data of 10^{15} bits.

Read retries are executed according to the disk drive's error recovery procedure, and include read retries accompanying head offset operations.

(2) Positioning error

Positioning (seek) errors that can be recovered by one retry shall occur no more than 10 times in 10^{7} seek operations.

1.8 Media Defects

Defective sectors are replaced with alternates when the disk is formatted prior to shipment from the factory (low level format). Thus, the host sees a defect-free device.

Alternate sectors are automatically accessed by the disk drive. The user need not be concerned with access to alternate sectors.

Chapter 6 describes the low level format at shipping.

CHAPTER 2 DEVICE CONFIGURATION

2.1 Device Configuration

Figure 2.1 shows the disk drive. The disk drive consists of a disk enclosure (DE), read/write preamplifier and controller PCA, and mounting brackets. The disk enclosure contains the disk media, heads, spindle motors, actuators, and a circulating air filter.

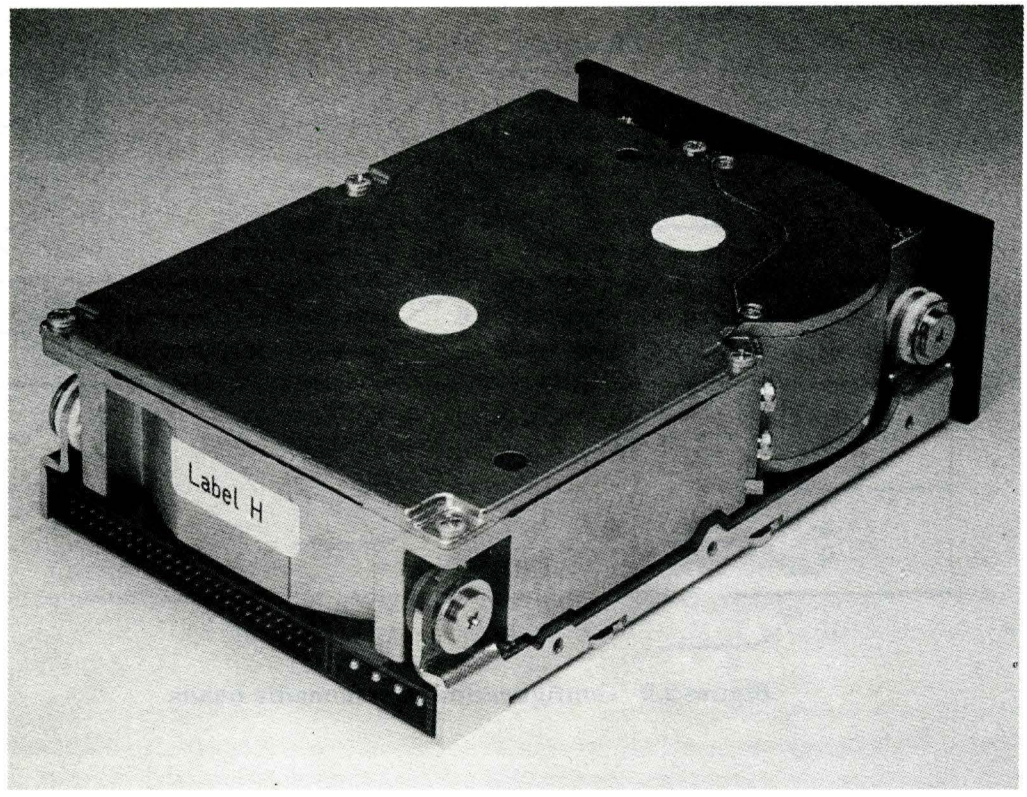


Figure 2.1 Disk drive

(1) Disk

The outer diameter of the disk is 95 mm. The inner diameter is 25 mm. The number of disks used varies with the model, as described below. The disks are rated at over 10,000 start/stop operations.

M2622T: 4 disks
M2623T: 5 disks
M2624T: 6 disks

(2) Head

The heads are of the contact start/stop (CSS) type. The head touches the disk surface while the disk is not rotating and automatically lifts when the disk starts.

Figure 2.2 illustrates the configuration of the disks and heads of each model. In Figure 2.2, the SR surface is a special servo surface containing servo information, necessary for controlling positioning and read/write. Numerals 0 to 10 indicate read/write heads and SR indicates the servo head.

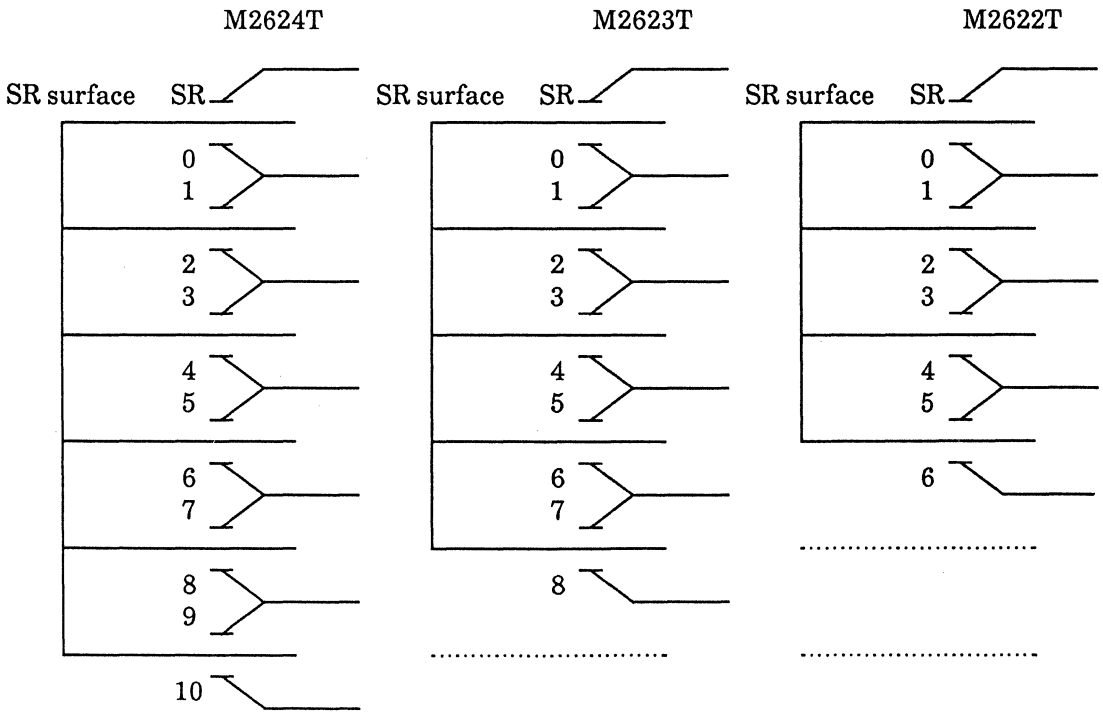


Figure 2.2 Configuration of disk media heads

(3) Spindle motor

The disks are rotated by a direct drive DC motor. The feedback circuit uses a Hall element to control the rotational speed. The speed is precisely maintained at 4400 rpm ±0.5%.

(4) Actuator

The actuator uses a revolving voice coil motor (VCM) structure which consumes low power and generates very little heat. The head assembly at the edge of the actuator arm is controlled and positioned by feedback of the servo information read by the servo head. If the power is not on or if the spindle motor is stopped, the head assembly stays in the specific CSS zone on the disk and is fixed by a mechanical lock.

(5) Air circulation system

The disk enclosure (DE) is sealed to prevent dust and dirt from entering. The disk enclosure features a closed loop air circulation system that relies on the blower effect of the rotating disk. This system continuously circulates the air through the circulation filter to maintain the cleanliness of the air within the disk enclosure. The disk enclosure also has a respiration filter to prevent load at the start of operation and to eliminate any difference in the inside and outside air pressures caused by changes in the ambient temperature.

(6) Read/write circuit

The read/write circuit uses a LSI chip for the head IC. It improves data reliability by preventing errors caused by external noise.

(7) Controller circuit

The controller circuit consists of an LSI chip to improve reliability. The high-speed microprocessor unit (MPU) achieves a high-performance AT controller.

2.2 System Configuration

Figure 2.3 diagrams a sample system configuration (connection of two units).

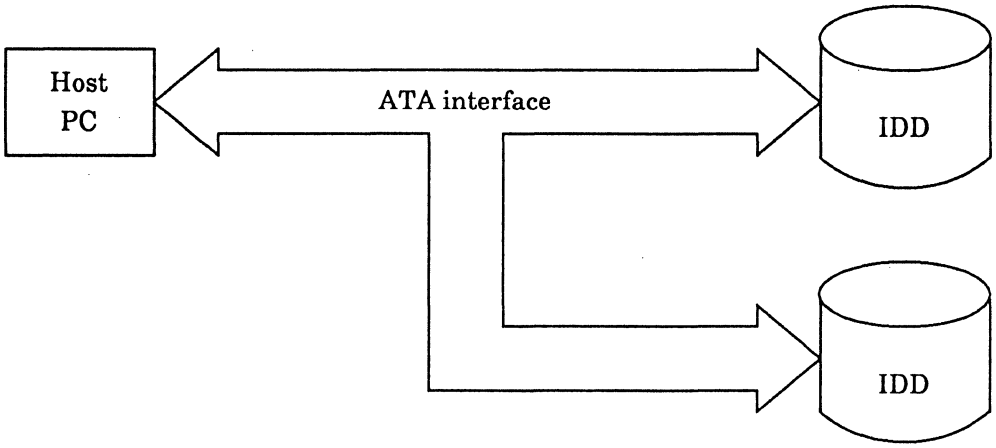


Figure 2.3 Sample system configuration (connection of two units)

Note:

To use a daisy chain configuration (2-drive system), the disk drives must be connected to an M261xT series machine or an ATA-compatible machine in principle. Operation can not be assured for daisy chain configurations with other machines.

CHAPTER 3 INSTALLATION CONDITIONS

3.1 Dimensions

Figures 3.1 and 3.2 illustrate the dimensions of the disk drive and positions of the mounting screw holes. All dimensions are in mm.

*1 Distance between screw holes for mounting to the bottom of unit.

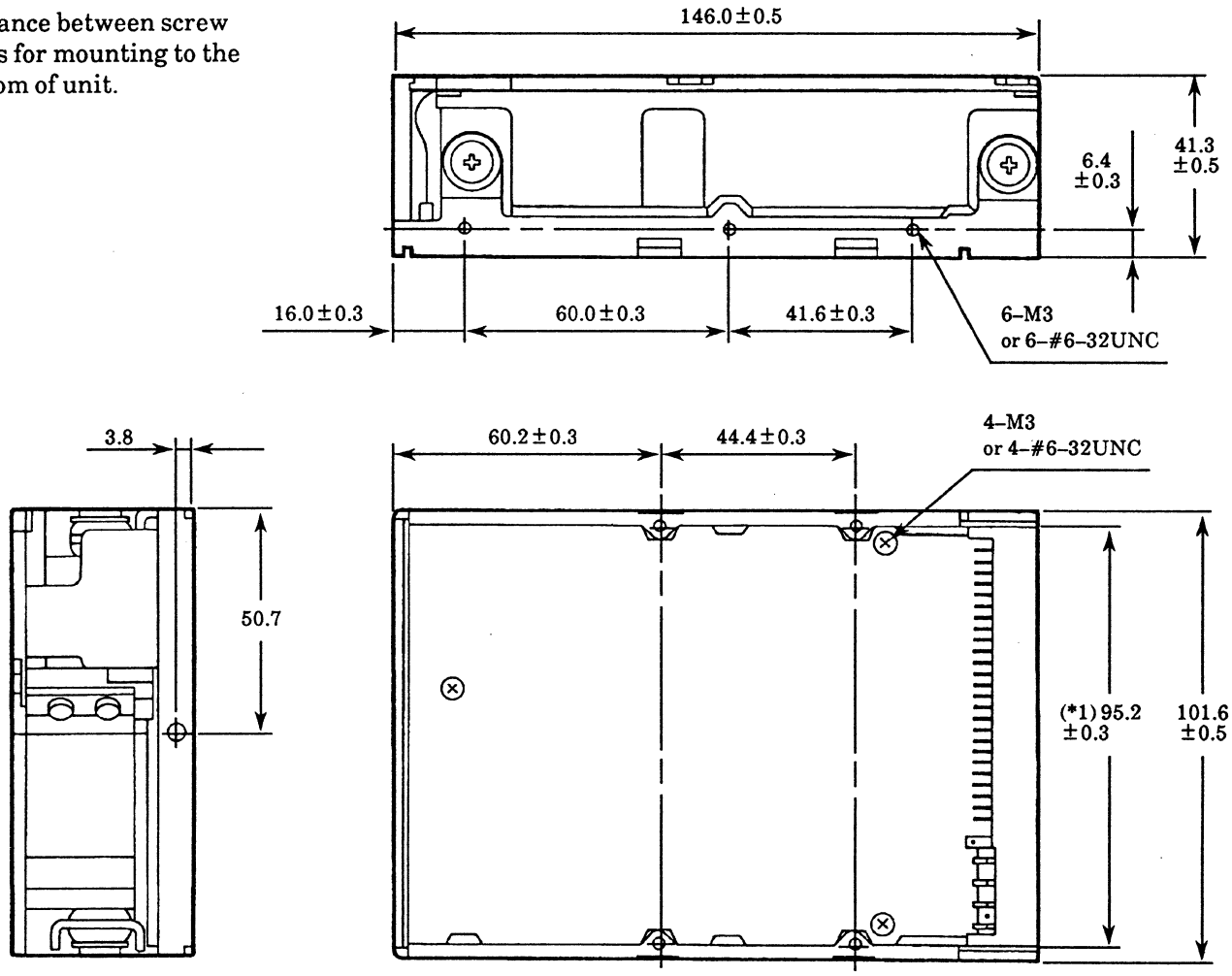


Figure 3.1 Dimensions without front panel

*1 Distance between screw holes for mounting to the bottom of unit.

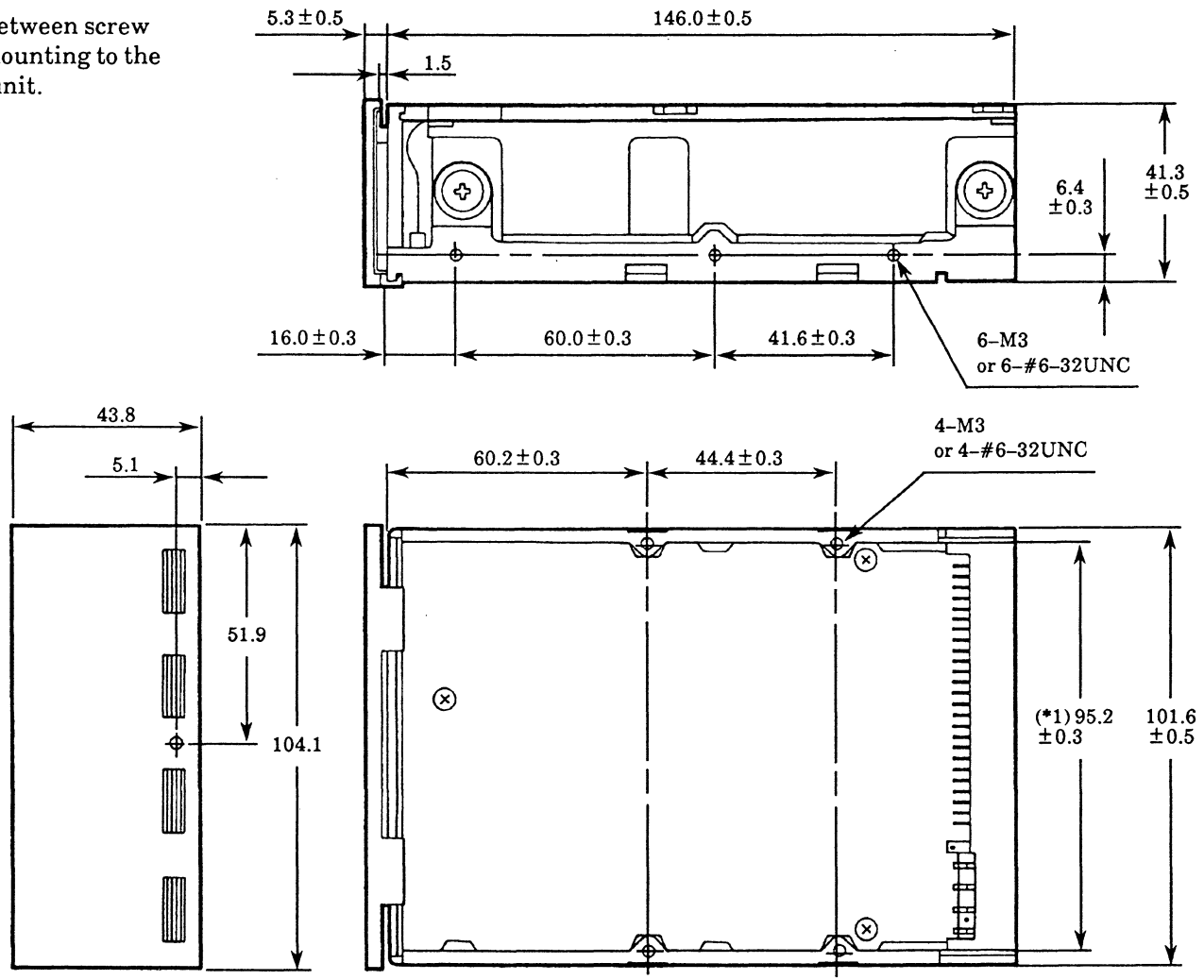
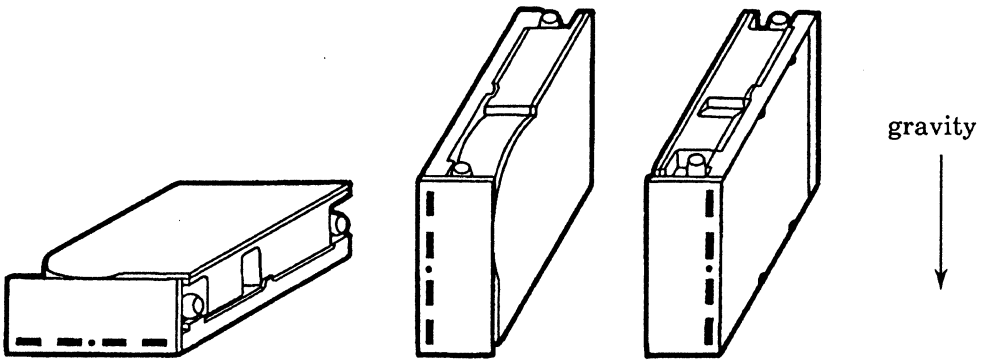


Figure 3.2 Dimensions with front panel

3.2 Mounting

(1) Orientation

Figure 3.3 illustrates the allowable orientations for the disk drive. The mounting angle can vary ±5° from the horizontal.



(a) Horizontal mounting (b) Vertical mounting (c) Vertical mounting

Figure 3.3 Orientation

(2) Frame

Figure 3.4 illustrates the structure of the frame.

The disk enclosure (DE) body is connected to signal ground (SG) and is electrically insulated from the disk drive mounting frame (frame ground: FG). Care must be taken to maintain the insulation after installing the disk drive.

Note:

In most cases, SG and FG are connected at a single point in the system. Therefore, when the disk drive is mounted, the insulation must be maintained as follows:

① To prevent the DE base from contacting the FG, use an embossed frame, as shown in Figure 3.4, or a similar frame that holds the disk drive at least 2.5 mm away from the system frame.

② As shown in Figure 3.4, be sure the mounting screws project no more than 4 mm from the outer surface of the disk drive mounting frame.

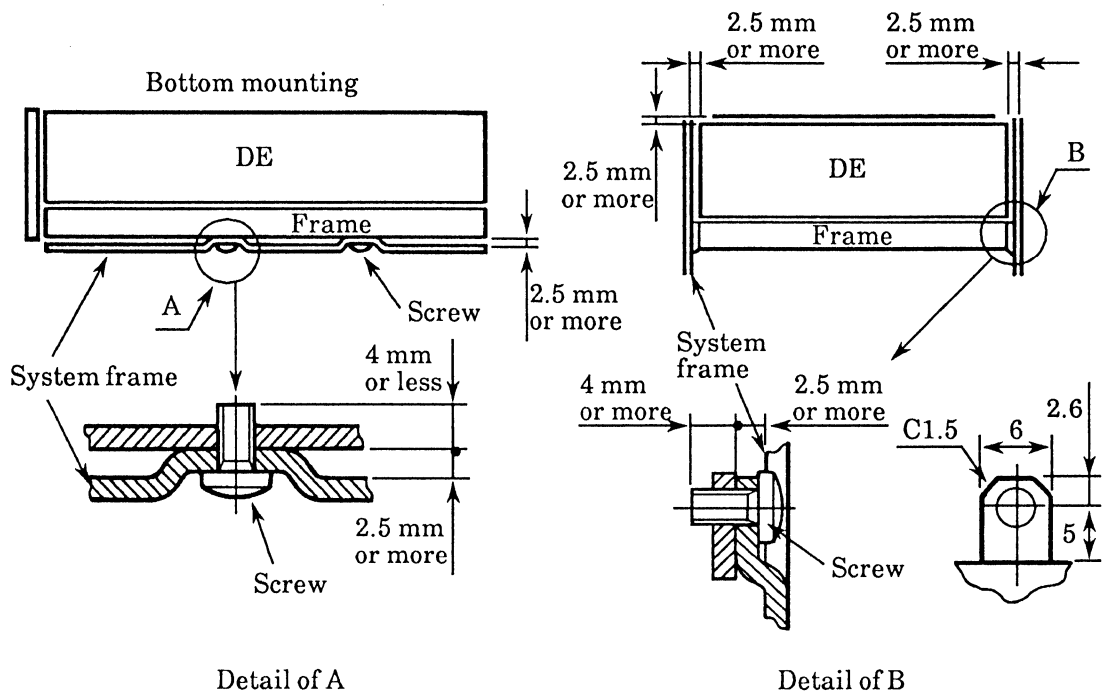


Figure 3.4 Frame structure

(3) Ambient temperature

The temperature conditions for a disk drive mounted in a cabinet refer to the ambient temperature at a point 3 cm from the disk drive. Pay attention to the air flow to prevent the DE surface temperature from exceeding 60°C.

Provide air circulation in the cabinet such that the PCA side, in particular, receives sufficient cooling. To check the cooling efficiency, measure the surface temperatures of the particular ICs listed below and the DE. Regardless of the ambient temperature, these surface temperatures must meet the standards listed in Table 3.1.

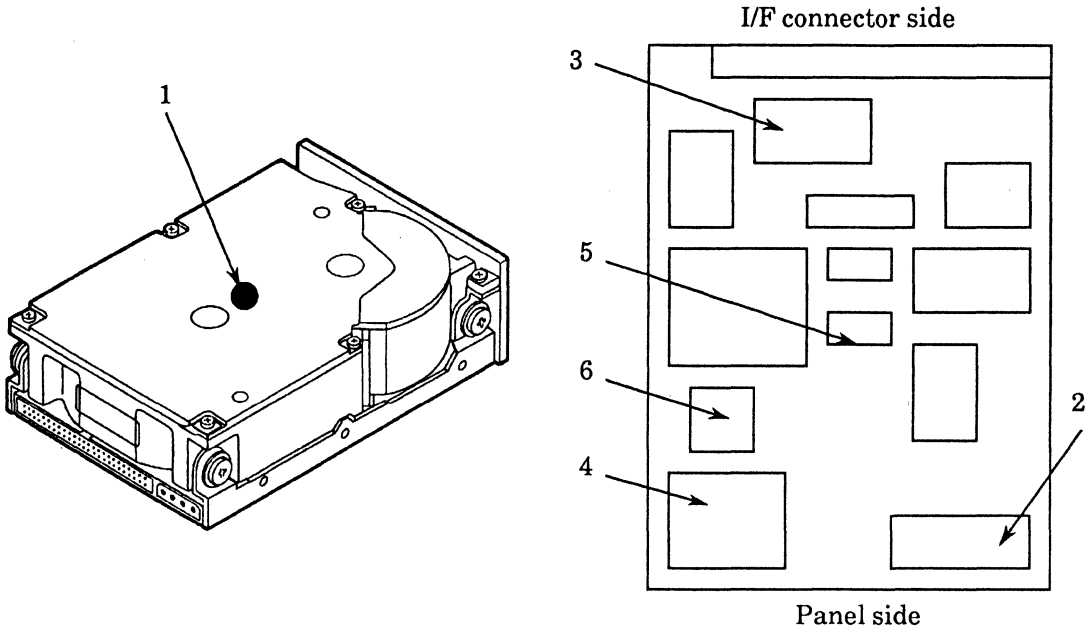


Figure 3.5 Surface temperature measurement points

Table 3.1 Surface temperature measurement points and standard values

No.	Measurement point	Temperature
1	Center of DE cover	60.0 °C
2	VCM driver radiator panel	70.0 °C
3	WS7010 (AT controller)	70.0 °C
4	SSI547 (pulse detector)	70.0 °C
5	SSI537 (encoder/decoder)	75.0 °C
6	Servo demodulator	80.0 °C

(4) Service area

Figure 3.6 shows how the drive must be accessed (service areas) during and after installation.

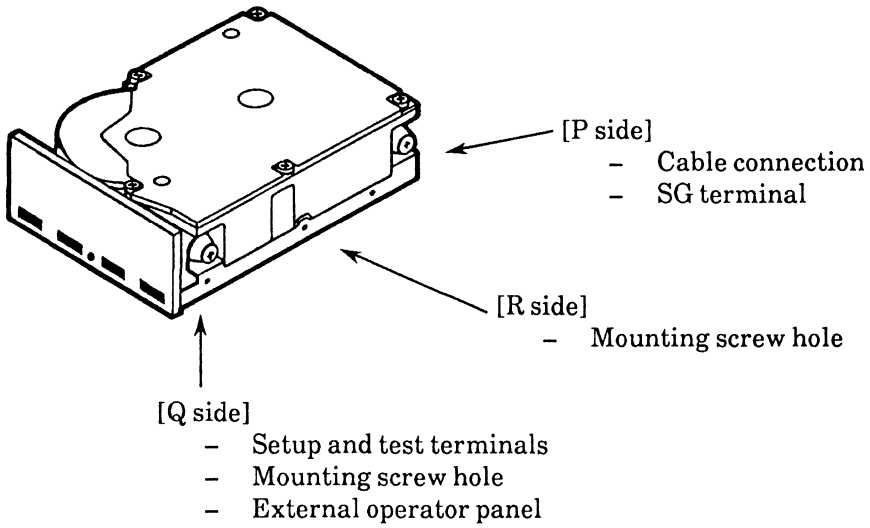


Figure 3.6 Service area

(5) External magnetic fields

Avoid mounting the disk drive near strong magnetic sources such as loud speakers. Ensure that the disk drive is not affected by external magnetic fields.

3.3 Cable Connections

3.3.1 Device connector

The disk drive has the connectors and terminals listed below for connecting external devices. Figure 3.7 shows the locations of these connectors and terminals.

- Power supply connector
- AT interface connector
- SG terminal
- External operator panel connector (LED)

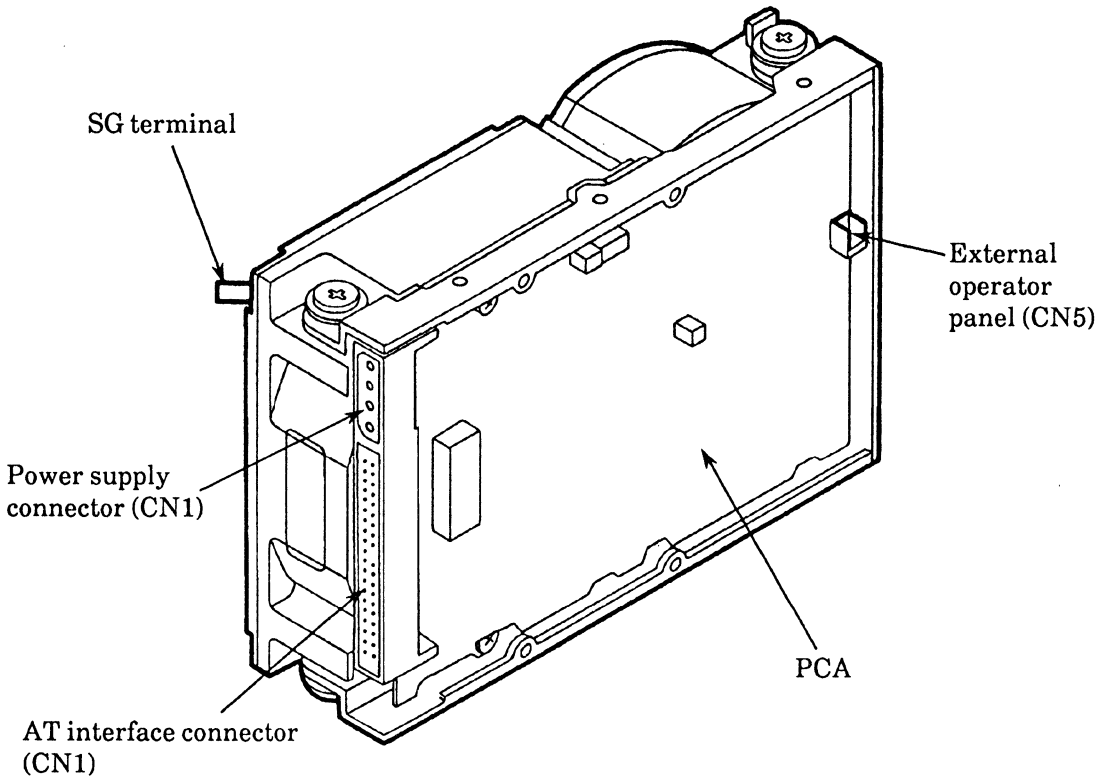


Figure 3.7 Connector locations

3.3.2 Cable connector specifications

Table 3.2 lists the recommended specifications for the cable connectors.

Table 3.2 Cable connector specifications

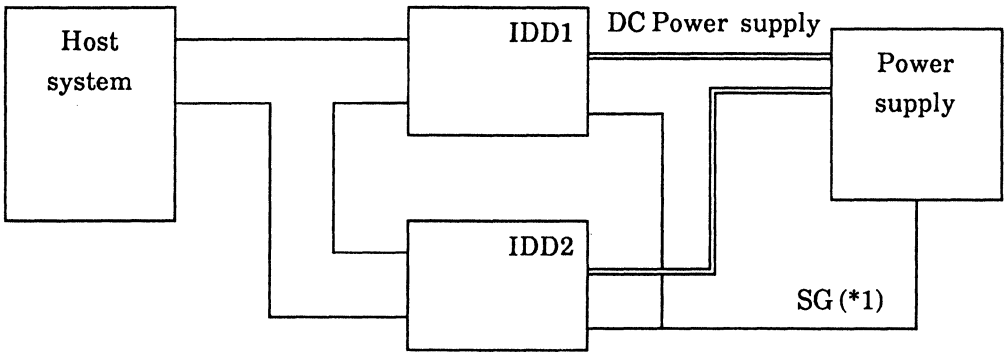
	Name	Model	Manufacturer
AT interface cable (40-pin, CN1)	Cable socket (closed-end type)	FCN-707B040-AU/B	Fujitsu
	Cable socket (through-end type)	FCN-707B040-AU/0	Fujitsu
	Signal cable	87711-004	DUPONT
		445-248-40	SPECTRS STRIP
Power supply cable (CN1)	Cable socket housing	1-480424-0	AMP
	Contact	170148-2	AMP
	Signal cable	86260-001 or equivalent	DUPONT
		AWG 18 to 24	
DC ground	Quick-connect receptable (FASTON)	62187-1	AMP
	Cable	AWG20	
External operator panel (CN5)	Cable socket housing	608283302815000	ELCO
	Contact	608283052330808 (wire:AWG24 to 30) 608283252330808 (wire:AWG32)	ELCO

Note:

The cable of twisted pairs and neighboring line separated individually is not allowed to use for the host interface cable. It is because that the location of signal lines in these cables is not fixed, and so the problem on the crosstalk among signal lines may occur.

3.3.3 Device connection

Figure 3.8 shows how to connect the devices.

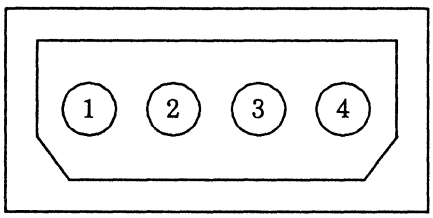


*1: Whether the SG is to be connected depends on the system, and should be evaluated for each system.

Figure 3.8 Cable connections

3.3.4 Power supply connectors

Figure 3.9 shows the pin assignment of the power supply connector.



(Viewed from cable side)

①	+12VDC
②	+12V RETURN
③	+5V RETURN
④	+5VDC

Figure 3.9 Power supply connector pins

3.4 SG Terminal

Figure 3.10 shows the SG terminal (quick-connect tab) for the DC ground.

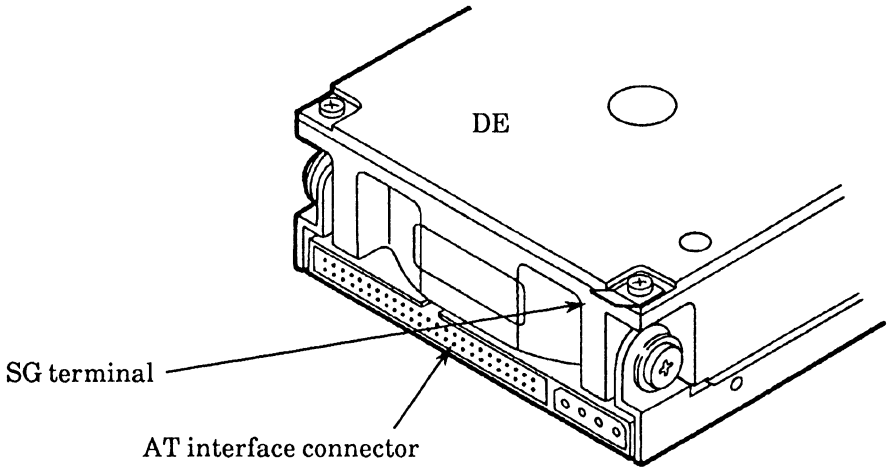
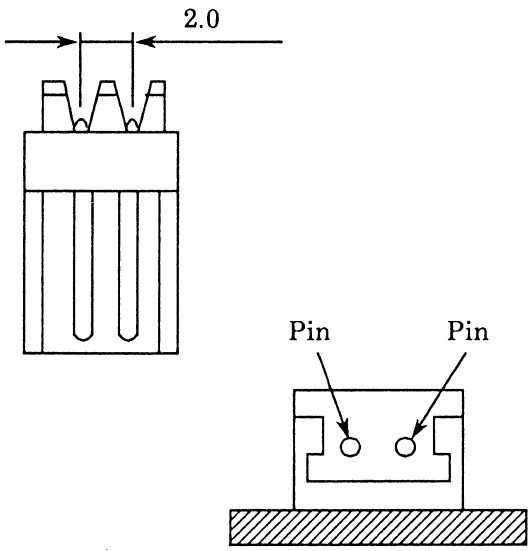


Figure 3.10 SG terminal

3.5 External Operator Panel Connector

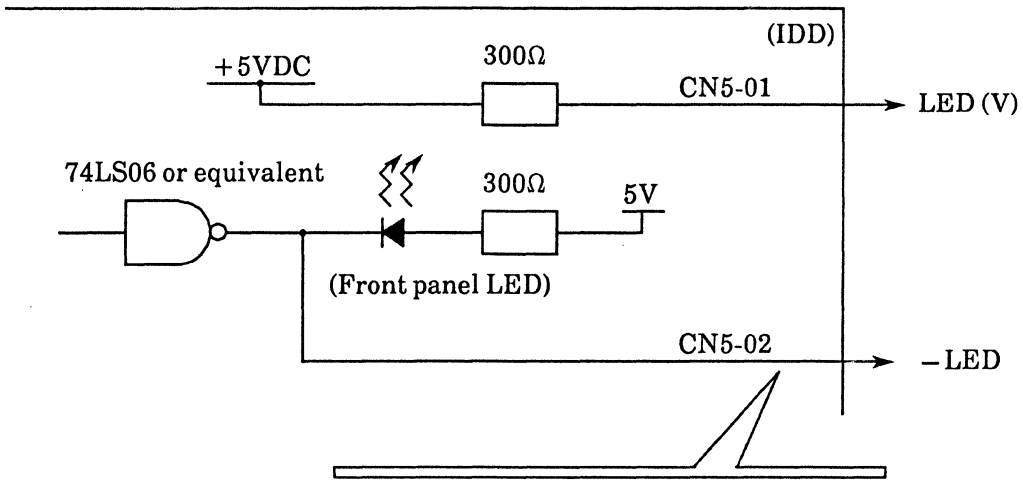
So that the front panel LEDs can be mounted externally, the disk drive has an external operator panel connector, shown in Figure 3.11.



CN5	
Pin	Signal
01	LED (V)
02	– LED

Figure 3.11 External operator panel connector

Figure 3.12 shows the electrical requirements for external LED. Output signals LED(V) and −LED are used to externally indicate the same information as the LEDs on the disk drive front panel.



Output level	Function
0 ~ 0.4 VDC (I_{OL} = 15 mA max.)	LED on
2.5 ~ 5.25 VDC	LED off

Figure 3.12 Electrical conditions of external LEDs

Notes:

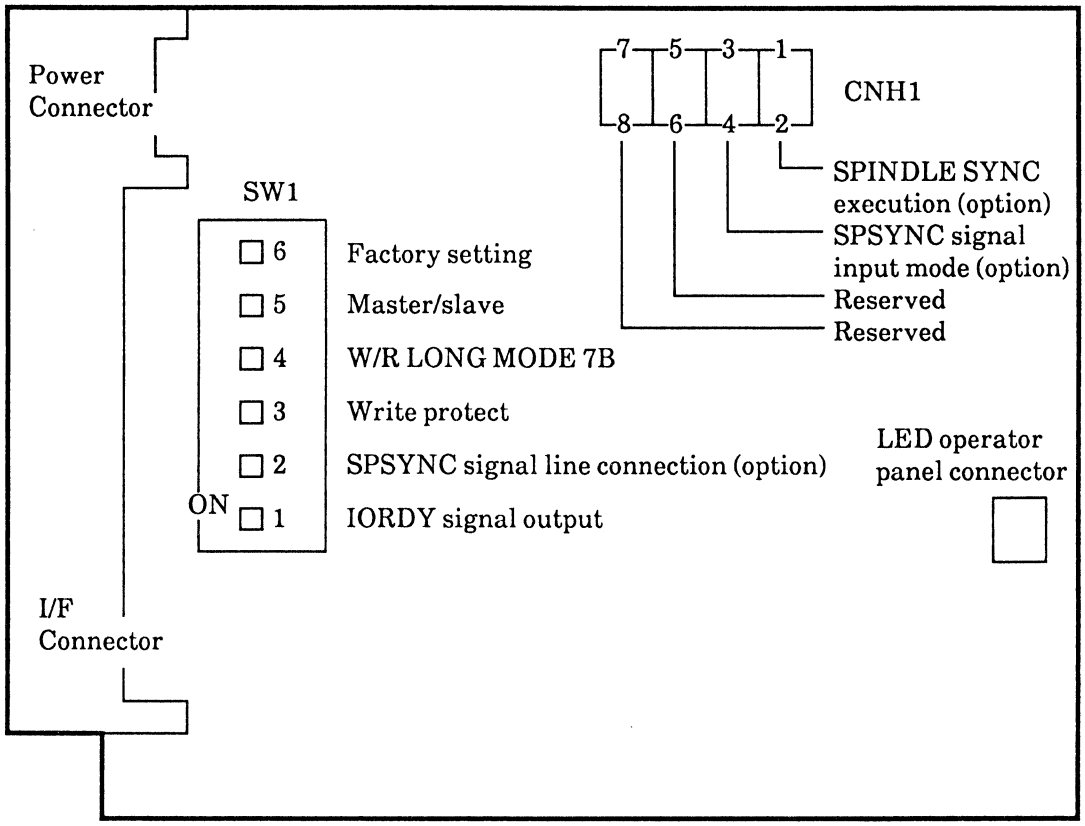
1. The external LED indication is the same as the LED indication on the front panel of the disk drive.

2. Do not connect any load other than external LEDs (satisfying the above electrical requirements) to the LED (V) and −LED terminals.

3.6 Switch Setup

3.6.1 Switch layout

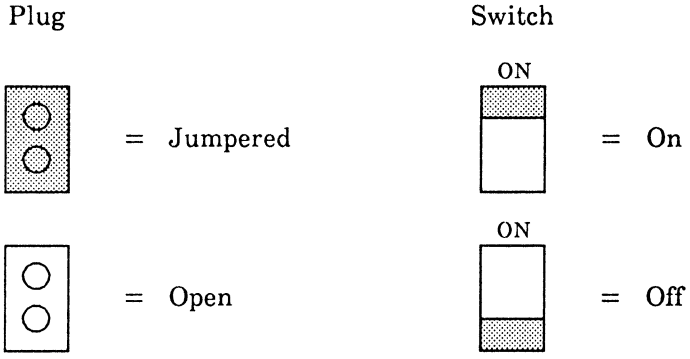
Figure 3.13 illustrates layout of the switch for mode setup.



*1: This figure may be changed without prior notice.

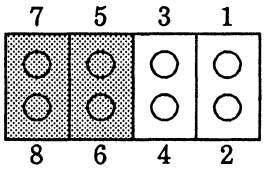
Figure 3.13 Mode setup switch layout

The description on the subsequent pages uses the following legend for the setup of, for example,CNH1 and SW1:



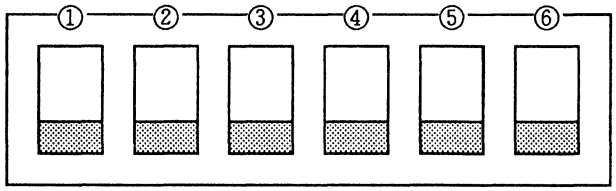
3.6.2 Standard factory setup

CNH1



1-2 open: Spindle Sync is not executed.
3-4 open: SPSYNC signal is in output mode.
5-6 jumper: Reserved
7-8 jumper: Reserved

SW1



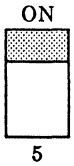
No.1 OFF: IORDY output is disabled.
No.2 OFF: SPSYNC line is disconnected.
No.3 OFF: Write protect is disabled.
No.4 OFF: Number of ECC bytes in LONG mode depends on command. (default: 4 bytes)
No.5 OFF: Master drive
No.6 OFF: For factory use

3.6.3 Mode setup

The following items must be set on the disk drive:

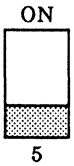
(1) Master drive/slave drive

SW1



Slave drive

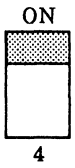
SW1



Master drive

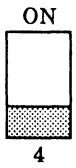
(2) 7-byte ECC in write/read LONG mode

SW1



Fixed 7-byte ECC

SW1

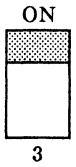


The number of ECC bytes in LONG mode is always 7 bytes regardless of the setup on the host.

The number of ECC bytes in LONG mode depends on the setup done with the SET FEATURES command. The default setup after power-on is 4 bytes.

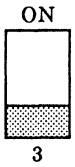
(3) Write protect

SW1



Write protect ON

SW1

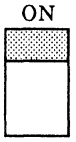


Write protect OFF

(4) Connection to the spindle synchronous signal line (option)

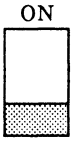
Specify whether to connect pin 28 of the HOST interface.

SW1



Connected to HOST interface

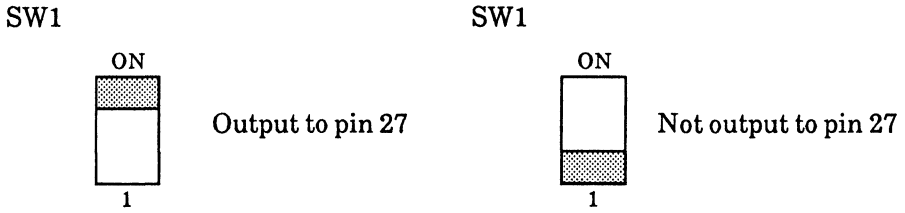
SW1



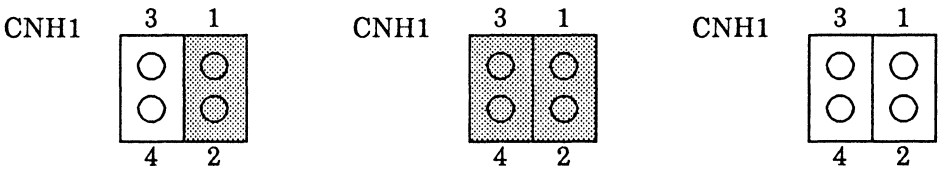
Not connected to HOST interface

(5) I/O channel ready signal output

Specify whether to output the IORDY signal to pin 27 of the HOST interface. When the data transfer rate of the host is very high (around 3.7 MW/s), the IORDY signal is output to synchronize data transfer by inserting wait states.



(6) SPINDLE SYNC operation and OUTPUT/INPUT mode of SPSYNC signal (option)



SPINDLE SYNC is performed and the SPSYNC signal is sent to the I/F 28 pin.
OUTPUT mode

SPINDLE SYNC is performed and the SPSYNC signal is received from the I/F 28 pin.
INPUT mode

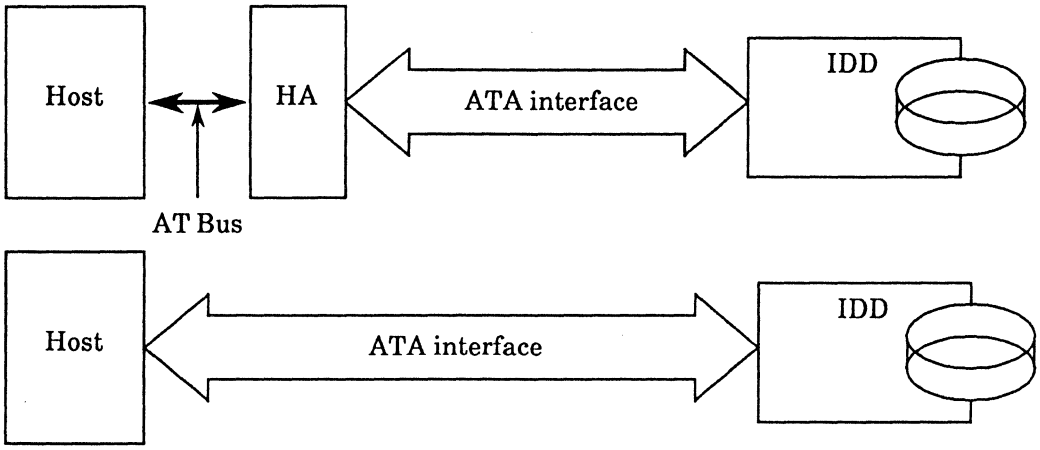
SPINDLE SYNC is not performed.

CHAPTER 4 HOST INTERFACE

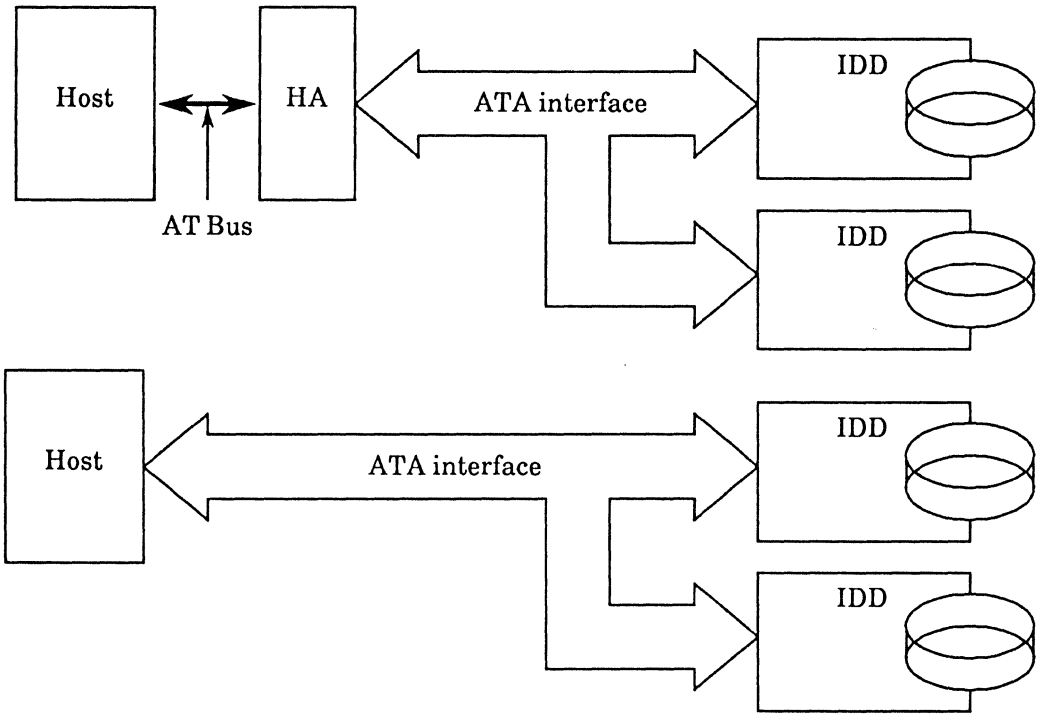
4.1 System Configuration

Figure 4.1 shows several sample system configurations.

(1) Single IDD connection



(2) Two-IDD connection



HA stands for host adapter (adapter board). A host adapter consists of an address decoder and driver/receiver (74LS244, 245, or equivalent).

Figure 4.1 System configuration

4.2 Interface Signal Names

Figure 4.2 diagrams the interface signal lines. Table 4.1 lists the connector pin assignment.

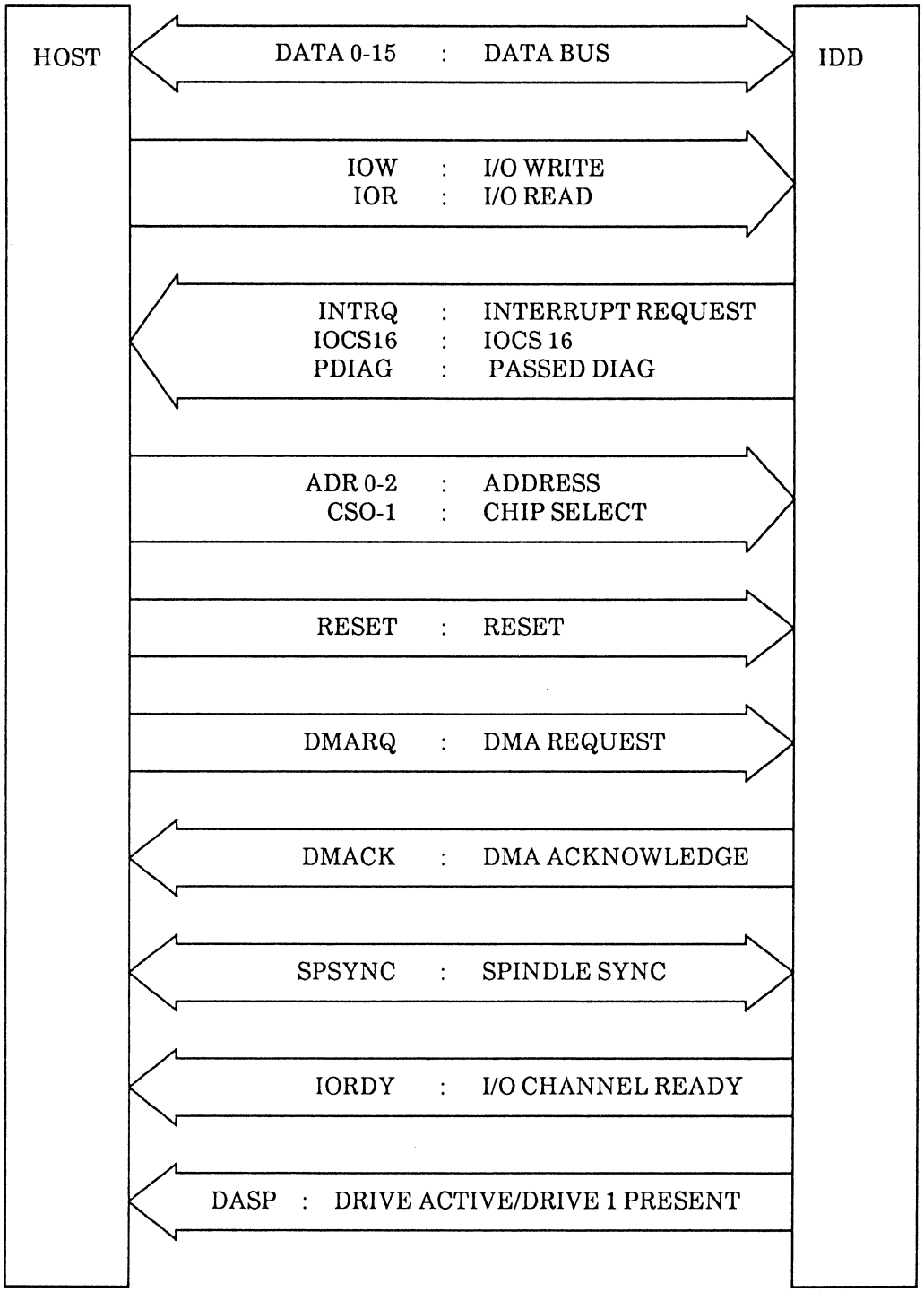


Figure 4.2 Interface signals

Table 4.1 Connector pin assignment

1	RESET–	2	GND
3	DATA7	4	DATA8
5	DATA6	6	DATA9
7	DATA5	8	DATA10
9	DATA4	10	DATA11
11	DATA3	12	DATA12
13	DATA2	14	DATA13
15	DATA1	16	DATA14
17	DATA0	18	DATA15
19	GND	20	KEY
21	DMARQ	22	GND
23	IOW–	24	GND
25	IOR–	26	GND
27	IORDY	28	SPSYNC (*1)
29	DMACK–	30	GND
31	INTRQ	32	IOCS16–
33	ADR1	34	PDIAG–
35	ADR0	36	ADR2
37	CS0–	38	CS1–
39	DASP–	40	GND

*1 : Option

[Signal name]	[I/O]	[Description]
RESET–	I	RESET signal from host system. Valid if low (min. 25μs).
DATA 0-15	I/O	16-bit bidirectional data bus between host and controller (HDC). I_{OL}=12 mA
IOW–	I	WRITE strobe signal. Host data items 0 to 15 are set in HDC register at rising edge of this signal. Valid if Low.
IOR–	I	READ strobe signal. If low, contents of HDC register are sent to bus of data items 0 to 15.
INTRQ	O	INTERRUPT signal for host system. Valid if high. This signal is reset when host system reads STATUS, sets a command, or makes DRQ inactive. This signal is a tristate output. I_{OL} = 12 mA
IOCS16–	O	This signal indicates that data is transferred as 16-bit data. Valid if low. Not output during DMA. This signal is an open collector output. I_{OL} = 12 mA
CS0–	I	CHIP SELECT signal decoding HOST address bus. If low, host can access registers 1F0H to 1F7H.
CS1–	I	CHIP SELECT signal decoding HOST address bus. If low, host can access registers 3F6H and 3F7H.
ADR 0-2	I	Address signal to select TASK FILE REGISTER.
KEY	–	Connector misinsertion prevention key –
PADIAG–	I/O	Signal to notify master that master has entered input mode (I), slave has entered output mode (O), and self-diagnosis of slave has ended normally in a daisy chain configuration. I_{OL} = 12 mA
IORDY	O	In data transfer between host and register IF0H, this signal is automatically set low to request host for WAIT state when the transfer rate approaches or exceeds 3.7 MW/s. This signal is a tristate output. I_{OL} = 12 mA
DASP–	I/O	Time-multiplexed signal. In a daisy chain configuration, the master enters input mode (I) and slave enters output mode (O). In other cases, this signal activates drive access LEDs. This signal is an open collector output. I_{OL} = 12 mA
DMARQ	O	DATA REQUEST signal to perform DMA transfer with host. This signal is a tristate output. I_{OL} = 12 mA
DMACK–	I	DATA ACKNOWLEDGE signal to perform DMA transfer with the host. A response to DMARQ from host.
SPSYNC	I/O	Reference signal to perform spindle synchronization. Jumpering CNH1 3 and 4 of mode setup switches starts input mode (I). Opening them starts output mode (O).

*1: I indicates that the direction is from host to drive. O indicates that the direction is from drive to host. I/O indicates bidirectional operations.

4.3 Task File Register

Host task files can be designated by CS0–, CS1–, and ADR 0 to 2 signals as described in Table 4.2.

Table 4.2 Task file register

CS0–	CS1–	ADR2	ADR1	ADR0	TASK FILE REGISTER		HOST I/O ADDRESS
					READ	WRITE	
0	1	0	0	0	Data Reg.	Data Reg.	$1F0_H$
0	1	0	0	1	Error Reg.	Features Reg.	$1F1_H$
0	1	0	1	0	Sector Count Reg.	Sector Count Reg.	$1F2_H$
0	1	0	1	1	Sector Number Reg.	Sector Number Reg.	$1F3_H$
0	1	1	0	0	Cylinder Low Reg.	Cylinder Low Reg.	$1F4_H$
0	1	1	0	1	Cylinder High Reg.	Cylinder High Reg.	$1F5_H$
0	1	1	1	0	SDH Reg.	SDH Reg.	$1F6_H$
0	1	1	1	1	Status Reg.	Command Reg.	$1F7_H$
1	0	1	1	0	Alt. Status Reg.	Device Control Reg	$3F6_H$
1	0	1	1	1	Drive Address Reg.	Not Used	$3F7_H$
1	1	X	X	X	No Operation	No Operation	———
0	0	X	X	X	Invalid Address	Invalid Address	———

*1: Data registers can be accessed in units of 16 bits of data, 0 to 15, for both read and write.

*2: Registers other than the data registers can be accessed in units of eight bits of data, 0 to 7, for both read and write.

*3: After the drive address register is read, only bit 7 becomes high impedance.

4.3.1 Data register (1F0H)

The data register is used to transfer data between the host and the buffer in response to read or write commands. This register consists of 16 bits and the host transfers data in PIO (programmed I/O) mode. However, to transfer ECC bytes in response to the R/W LONG command, only the low-order eight bits are used.

4.3.2 Error register (1F1H)

The error register stores the status of the executed instruction.

Except for the execution of self-diagnosis (DIAGNOSTIC), this register is valid only while the ERROR bit of the status register is set. During execution of DIAG, this register is valid regardless of the contents of the status register.

(1) During DIAG execution

01 : No Error Detected
02 : Formatter Device Error
03 : Sector Buffer Error
04 : Ecc Circuitry Error
05 : Controlling Microprocessor Error
06 : Drive 1 Failed (Slave Error)

If the drive is a two-unit system, the error indicated in the error register of the master side are valid. If an abnormality is detected on the slave side, "80H" is ORed with the above error is reported to the host. However, if the host selects the slave side, the host recognizes the slave error code only.

(2) Operation status

Bit 7 : A bad block was detected.
Bit 6: An uncorrectable ECC error was detected in the data portion during execution of the READ SECTOR(S) command. (UNCORRECTABLE ECC ERROR)
Bit 5 : Unused
Bit 4 : The target sector was not found. (ID NOT FOUND)
Bit 3 : Unused
Bit 2 : A command issued during a drive abnormality (such as NOT READY) was aborted. Or, an invalid command was received. (Aborted Command Error)
Bit 1 : The RECALIBRATE command was executed but cylinder 0 was not detected.
Bit 0 : The address mark of the data portion was not found. (DATA AM NOT FOUND)

4.3.3 Features register (1F1H)

Before the following commands are issued, a value corresponding to the target is set in the features register.

(1) SET FEATURES command

Specifies the drive modes: read-ahead cache enable/disable and the number of ECC transfer bytes for the execution of the READ/WRITE LONG command. For details, see Chapter 4, Subsection 4.3.9, "Command register".

(2) WRITE SAME command

Writes the data of one sector specified by the host into the user area. According to the contents of this register, the write target may be the specified area or the entire user area. For details, see Chapter 4, Subsection 4.3.9, "Command register".

4.3.4 Sector count register (1F2H)

This register contains the number of transfer sectors for instructions such as READ SECTOR or WRITE SECTOR. 0 indicates that 256 is specified.

4.3.5 Sector number register (1F3H)

The sector number register contains the address of the target start sector of an instruction. The valid range of values is from 01_H to the sector number specified by the SET PARAMETERS command.

4.3.6 Cylinder number register (1F4H, 1F5H)

The cylinder number register stores the address of the target start cylinder of an instruction.

4.3.7 Drive/head register (1F6H)

The drive/head register stores the device number of the disk to execute the command and the number of the first head to be accessed in correspondence to its bits.

Bit 7 : Always 1
Bit 6 : Always 0
Bit 5 : Always 1
Bit 4 : 0 : Disk drive 0
1 : Disk drive 1
Bit 3 : Head 2^3
Bit 2 : Head 2^2
Bit 1 : Head 2^1
Bit 0 : Head 2^0

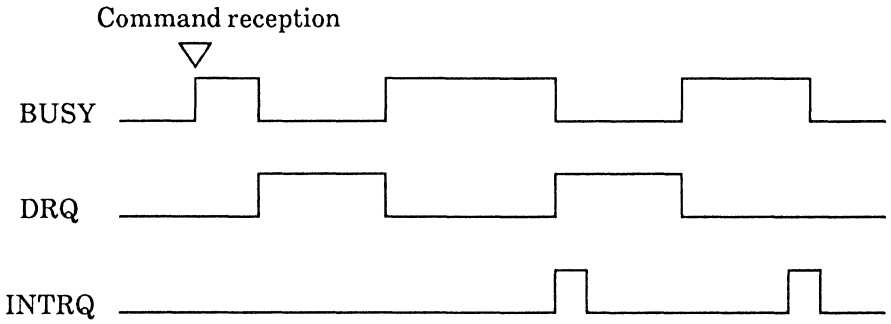
4.3.8 Status register (1F7H)

Bit 7 : BUSY
While this bit is set, access from the host to the task file register is inhibited. When this bit is set, the contents of status register are copied to all of registers $1F0_H$ to $1F6_H$ and $3F6_H$, which can be read from the host. The BUSY bit is set under the conditions below:

(1) The RESET– signal becomes active or the SRST bit of the device control register becomes "1".

(2) The host writes the command register. Figure 4.3 illustrates the relationship between the BUSY bit and the DATA REQUEST bit (DRQ) during multi sector read/write.

Example 1 : When two sectors are transferred because of a write command



Example 2 : When two sectors are transferred because of a read command

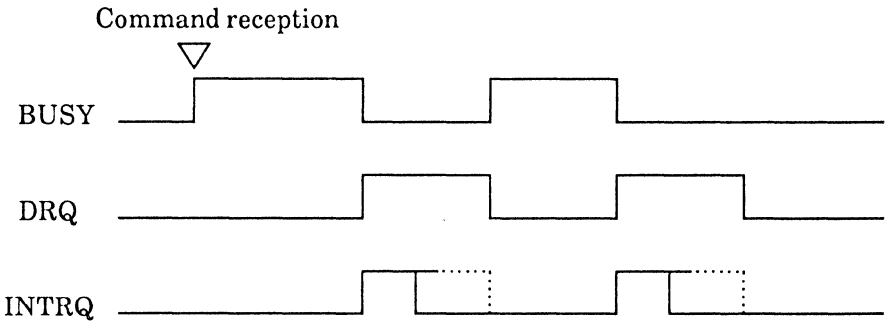


Figure 4.3 BUSY and DRQ timing

Bit 6 : DRIVE READY

"1" : The drive is ready.

Bit 5 : WRITE FAULT

"1" : Drive abnormality is detected.

Bit 4 : COMMAND COMPLETE

"1" : Active

Bit 3 : DATA REQUEST

"1" : Data of one sector can be transferred to the host.

Bit 2 : CORRECTED DATA

"1" : A correctable ECC error occurred and the data was corrected.

Bit 1 : INDEX

"1" : The INDEX signal from the drive is active. The active period is about 300 ns.

Bit 0 : ERROR

"1" : An error occurred during execution of an instruction.

The INTRQ signal is reset when this register is read.

4.3.9 Command register ($IF7_H$)

The command register contains the command to be executed by the controller. Table 4.3 lists the commands and necessary parameters. All operations start after the host sets valid parameters in other task file registers and writes a command in this register.

Table 4.3 Command register

Command name	Command code (bit)								Parameter used				
	7	6	5	4	3	2	1	0	FR	SC	SN	CY	SDH
RECALIBRATE	0	0	0	1	X	X	X	X	N	N	N	N	D
SEEK	0	1	1	1	X	X	X	X	N	N	N	Y	Y
READ SECTOR(S)	0	0	1	0	0	0	0	R	N	Y	Y	Y	Y
READ LONG	0	0	1	0	0	0	L	R	N	Y	Y	Y	Y
WRITE SECTOR(S)	0	0	1	1	0	0	0	R	N	Y	Y	Y	Y
WRITE LONG	0	0	1	1	0	0	L	R	N	Y	Y	Y	Y
READ VERIFY	0	1	0	0	0	0	0	R	N	Y	Y	Y	Y
FORMAT TRACK	0	1	0	1	0	0	0	0	N	N	N	Y	Y
EXECUTE DRIVE DIAGNOSTIC	1	0	0	1	0	0	0	0	N	N	N	N	*D
INITIALIZE DRIVE PARAMETERS	1	0	0	1	0	0	0	1	N	Y	N	N	Y
READ BUFFER	1	1	1	0	0	1	0	0	N	N	N	N	D
WRITE BUFFER	1	1	1	0	1	0	0	0	N	N	N	N	D
SET MULTIPLE MODE	1	1	0	0	0	1	1	0	N	Y	N	N	D
READ MULTIPLE	1	1	0	0	0	1	0	0	N	Y	Y	Y	Y
WRITE MULTIPLE	1	1	0	0	0	1	0	1	N	Y	Y	Y	Y
WRITE VERIFY	0	0	1	1	1	1	0	0	N	Y	Y	Y	Y
READ DMA	1	1	0	0	1	0	0	R	N	Y	Y	Y	Y
WRITE DMA	1	1	0	0	1	0	1	R	N	Y	Y	Y	Y
WRITE SAME	1	1	1	0	1	0	0	1	Y	Y	Y	Y	Y
IDENTIFY DRIVE	1	1	1	0	1	1	0	0	N	N	N	N	D
SET FEATURES	1	1	1	0	1	1	1	1	Y	N	N	N	D

The abbreviations used in Table 4.3 stand for the following:

FR	:	Features register ($1F1_H$)
SC	:	Sector count register ($1F2_H$)
SN	:	Sector number register ($1F3_H$)
CY	:	Cylinder number register ($1F4_H$, $1F5_H$)
SDH	:	Drive/head register ($1F6_H$)
L	:	1 : READ LONG or WRITE LONG command. Data transfer with the host is in the format of DATA (256 W) + ECC (7 B or 4 B). 0 : Data transfer with the host is in units of 256 W.
R	:	1 : Retry inhibited 0 : Retry enabled
Y	:	Valid parameters are necessary for command execution. For SDH, parameters of both DRIVE and HEAD must be set up.
N	:	The register value is ignored in command execution.
D	:	Only the DRIVE parameter is valid and the HEAD parameter is ignored.
*D	:	In a daisy chain configuration, both drives are executed regardless of the DRIVE parameter.
X	:	Don't care (Any value can be used.)

(1) RECALIBRATE (10_H)

The head seeks cylinder 0 (head 0). After command execution, the INTRQ signal becomes active.

(2) SEEK (70_H)

The specified cylinder is sought. After command execution, the INTRQ signal becomes active.

(3) READ SECTOR (S) ($2X_H$)

The specified cylinder is sought and the read operation starts from the specified head and sector.

If at least one sector of read data is stored in the buffer, the DRQ bit of the status register is set and data transfer to the host starts.

If a DATA ECC error occurs during a read operation, the error is automatically corrected and the corrected data is transferred to the host. If an uncorrectable error occurs, the sector data is also transferred to the host. However, processing of subsequent sectors is stopped and the cylinder, head, and sector position where the error occurred are written to each register of the host task file. Operation then ends.

If all read operations end without error, "00" is written to the sector count register. The end position is written to other task files.

(4) WRITE SECTOR(S) ($3X_H$)

The specified cylinder is sought and the write operation starts from the specified head and the sector.

When this command is received, the DRQ bit of the status register is immediately set and data transferred from the host is written to the buffer. If at least one sector of data is stored, writing to the drive starts.

If an error such as ID NOT FOUND occurs during a write operation, the processing of subsequent sectors is stopped and the cylinder, head, and sector position where the error are written to each register of the host task file. Operation then ends.

If all write operations end without error, "00" is written to the sector count register. The end position is written to other task files.

(5) FORMAT TRACK (50_H)

The specified cylinder is sought and one track of the specified head is formatted. After the command ends, the INTRQ signal becomes active.

Parameters for formatting are transferred as data of one sector from the host. The data consists of a word (two bytes) for each sector. The lower byte is selected from the four types below (sector conditions). The higher byte indicates the sector number.

00_H : Good sector
20_H : This sector was reassigned from the alternate area.
40_H : This sector was assigned to the alternate area.
80_H : Bad sector

Data is prepared for full length of a sector and the remaining area is padded with 00_H for transfer. (See Chapter 6, Subsection 6.2.2, "Reformatting".)

(6) READ VERIFY ($4X_H$)

In the same way as the READ SECTOR(S) command, the specified cylinder is sought and the read operation starts from the specified head and sector. The INTRQ signal is set after the command ends.

Unlike the READ SECTOR(S) command, data is not transferred to the host. If a DATA ECC error occurs during a read operation, correction is performed. If the error is correctable, the CORRECTED DATA bit of the status register is set. If the error is uncorrectable, the UNCORRECTABLE ECC ERROR bit of the error register is set.

(7) EXECUTE DRIVE DIAGNOSTIC (or DIAGNOSTIC) (90_H)

This command executes internal self-diagnosis. The results of the self-diagnosis are indicated by the ERROR register. If the system has two drives, the master drive reports the self-diagnosis execution results for both the master and slave to the host.

The master drive monitors the PDIAG– signal issued from the slave drive. If the PDIAG– signal is found to be low, the master drive assumes that the self-diagnosis of the slave drive ended normally.

The INTRQ signal is set when this command ends.

(8) INITIALIZE DRIVE PARAMETERS (or SET PARAMETERS) (91_H)

This command is used by the host to define the maximum head number of the drive and the number of sectors per track.

When this command ends, the INTRQ signal is set.

Valid registers

SECTOR COUNT register = Sectors/track
SDH register = Head/cylinder

(Example 1) When there are 16 heads and 63 sectors in the host setup
SECTOR COUNT register = $3F_H$
SDH register = XF_H (X: Drive number)

(9) WRITE BUFFER ($E8_H$)

Upon executing this command, the host can write any data to the buffer of the drive. When this command is executed, the DRQ bit and the INTRQ signal are set.

The buffer accessed with this command is the same as that accessed with the READ BUFFER command. The number of blocks is always 1.

The INTRQ signal is not set when this command ends.

(10) READ BUFFER ($E4_H$)

Upon executing this command, the host can read the data in the drive buffer. When this command is executed, the DRQ bit and the INTRQ signal are set.

The buffer accessed with this command is the same as that accessed with the WRITE BUFFER command. The number of blocks is always 1.

The INTRQ signal is not set when this command ends.

(11) READ LONG ($2X_H$)

This command is similar to the READ SECTOR(S) command, but reads not only data but also ECC from the drive and transfers them to the host. The number of ECC transfer bytes is specified by SW1-NO4 or the SET FEATURES command.

(12) WRITE LONG ($3X_H$)

This command is similar to the WRITE SECTOR(S) command, but writes not only data but also ECC transferred from the host to the drive.

The number of ECC transfer bytes is specified by SW1-NO4 or the SET FEATURES command.

The operating conditions of this command are as follows :

- READ LONG → WRITE LONG sequence
  (However, WRITE LONG can be executed in succession after READ LONG.)
- The specification of the address and the number of transfer blocks are the same in the above sequence.

If the above conditions are not satisfied, an Aborted Command error occurs.

(13) SET MULTIPLE MODE ($C6_H$)

This command validates the operation of the READ MULTIPLE and WRITE MULTIPLE commands. The valid block count is indicated by the SECTOR COUNT register ($1F2_H$). The valid values are decimal 2, 4, 6, 8, 16, and 32. If a block size other than the above is specified, an Aborted Command error ($1F1_H = 04_H$) occurs.

After power-on, hard reset, or soft reset, the READ MULTIPLE and WRITE MULTIPLE commands become invalid.

(14) READ MULTIPLE ($C4_H$)

Executing this command results in an Aborted Command error ($1F1_H = 04_H$) if the block size has not been set by the SET MULTIPLE MODE command. However, once the SET MULTIPLE MODE command is issued, this command remains valid until hard reset, or soft reset. When data is transferred to the host, the DRQ bit of the STATUS register is set and the INTRQ signal is set.

The number of transfer blocks is calculated by the block count ($1F2_H$) set by the SET MULTIPLE MODE command and the sector count ($1F2_H$) set by this command.

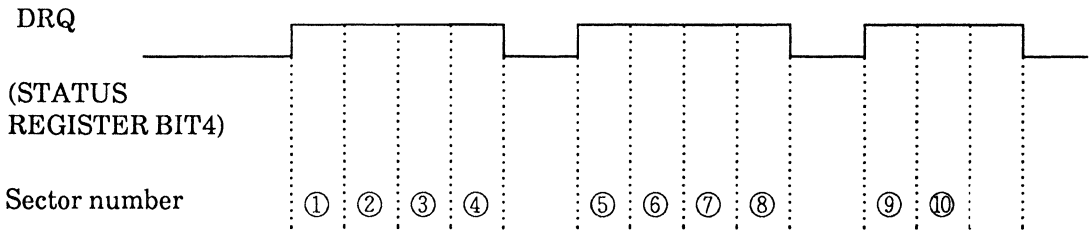
For example, if the block count is 4 and the sector count is 11, the transfer format is as follows:

Number of transfer blocks = INT {(sector count)/(block count)}
= INT (11/4)
= 2

However, this means that only eight sectors are transferred but the command requested that 11 sectors be transferred. The remaining three sectors must be transferred as one block. The calculation is as follows:

(Sector count) MOD (Block count)
= 11-4 * (INT 11/4)
= 11-8
= 3

Thus, to satisfy this command, two four-sector blocks must be transferred first and the remaining eight sectors must be transferred as one block.



If an error occurs, the error contents are reported to the host at the beginning of a block. If the DRQ is set, data is transferred correctly. For correctable ECC errors, data is normally transferred to the host. For other errors, command processing is stopped after processing of the faulty block ends.

(15) WRITE MULTIPLE ($C5_H$)

This command results in an Aborted command error ($1F1_H = 04_H$) if the block size is not set by the SET MULTIPLE MODE command. However, once the SET MULTIPLE MODE command is issued, this command remains valid until power-on, hard reset, or soft reset.

When a request for data is made to the host, the DRQ bit of the STATUS register is set.

The INTRQ signal is handled in the same way as the WRITE SECTOR(S) command.

The number of transfer blocks or remaining blocks is calculated in the same way as for the READ MULTIPLE command. If an error occurs in a sector in the block, processing of the sector is terminated and the INTRQ signal is set.

(16) READ DMA (CX_H)

Unlike ordinary PIO (programmed I/O), this command transfers data to and from the host using DMARQ (pin 21) and DMACK- (pin 29) of the INTERFACE signal. The DRQ bit is set during transfer, but the INTRQ signal is set once all transfer operations have been completed. Other operations are the same as those of the READ SECTOR(S) command. If an error occurs, the pertinent sector is not transferred and the INTRQ signal is set. Subsequent data is not transferred.

(17) WRITE DMA (CX_H)

Unlike ordinary PIO (programmed I/O), this command transfers data to and from the host using DMARQ (pin 21) and DMACK- (pin 29) of the INTERFACE signal. The DRQ bit is set during transfer, but the INTRQ signal is set once all transfer operations have been completed. Other operations are the same as those of the WRITE SECTOR(S) command. If an error occurs, the pertinent sector is not transferred and the INTRQ signal is set. Subsequent data is not transferred.

(18) WRITE VERIFY ($3C_H$)

This command performs READ VERIFY after performing WRITE SECTOR(S) processing. When the host issues the command, the DRQ bit is set and data is written. Then, READ VERIFY is performed with the BUSY bit set. Once this processing has been completed, the INTRQ signal is set and the command ends. Errors are handled in the same way as for the WRITE SECTOR(S) command.

(19) WRITE SAME ($E9_H$)

This command writes data of a sector specified by the host to a specified area, according to the value set in the FEATURES register (1F1H).

DRQ and INTRQ for transfer are the same as for the WRITE SECTOR(S) command. Errors are handled in the same way as the WRITE SECTOR(S) command.

If the value of the FEATURES register is other than 22_H or DD_H, this command results in an Aborted command error.

① When the FEATURES register value is 22_H

Data equal to the sector count is written from the specified cylinder, head, and sector according to the host parameters of $1F2_H$ to $1F6_H$.

② When the FEATURES register value is DD_H

Data is written to the entire user area. Only the device number of the disk is valid in the host parameters of $1F2_H$ to $1F6_H$.

If a write error occurs, the error contents are set in the $1F1_H$ register and the error location is set in registers $1F3_H$ to $1F6_H$ by a logical address (the parameter specified by the SET PARAMETERS command). The $1F2_H$ register is invalid.

(20) SET FEATURES (EF_H)

This command specifies the drive mode according to the FEATURES register value. The following modes can be specified:

44_H = ECC length for READ LONG/WRITE LONG of the vendor (M262xT is set as 7 bytes)
55_H = Read-ahead cache is disabled.
AA_H = Read-ahead cache is enabled.
BB_H = ECC length for READ LONG/WRITE LONG is set to 4 bytes.

After power-on, hard reset, or soft reset, the default settings are that the read-ahead cache is enabled and the ECC length is 4 bytes. INTRQ becomes active when this command ends.

INTRQ becomes active when this command ends.

If SW1-No.4 is on (long mode 7 bytes), the 44_H and BB_H modes are invalid and the number of ECC transfer bytes for the READ/WRITE LONG command execution is always 7 bytes.

(21) IDENTIFY DRIVE (or READ PARAMETERS) (EC_H)

The host uses this command to obtain parameters for the drive. When this command is issued, the drive parameters are prepared in the buffer and the DRQ but of the STATUS register and INTRQ signal are set. Then the host can read data of one sector from the drive.

The data format of the buffer is listed below.

		VALUE (HEX)
WORD 0	GENERAL CONFIGURATION	0c5a
WORD 1	NUMBER OF FIXED CYLINDERS	03f5 / 03ea / 03e3
WORD 2	RESERVED	0000
WORD 3	NUMBER OF HEADS	000a / 000d / 0010
WORD 4	NUMBER OF UNFORMATTED BYTES /PHYSICAL TRACK	936d
WORD 5	NUMBER OF UNFORMATTED BYTES / SECTOR	0251
WORD 6	NUMBER OF PHYSICAL SECTORS / TRACK	003f
WORD 7	RESERVED	0000
WORD 8	RESERVED	0000
WORD 9	RESERVED	0000
WORD 10~19	SERIAL NUMBER	Drive serial Number
WORD 20	BUFFER TYPE 0003 = DUAL PORTED, MULTI SECTOR BUFFER, CACHE	0003
WORD 21	CONTROLLER BUFFER SIZE IN 512 BYTE INCREMENTS	0080
WORD 22	NUMBER OF ECC BYTES TRANSFERRED ON LONG OPERATIONS	0004 / 0007
WORD 23~26	CONTROLLER FIRMWARE REVISION	*1
WORD 27~46	CONTROLLER MODEL NUMBER	*2
WORD 47	Bit7~0= MAXIMUM NUMBER OF SECTOR THAT CAN BE PER INTERRUPT ON READ AND WRITE MULTIPLE	0020
WORD 48	DOUBLE WORD-TRANSFER FLAG 0000 = CAN PERFORM DOUBLE WORD I / O	0001
WORD 49	CAPABILITIES BIT8~1 = DMA SUPPORTED	0100
WORD 50	RESERVED	0000
WORD 51	BIT15~8 = PIO DATA TRANSFER CYCLE TIMING MODE	0100
WORD 52	BIT15~8 = DMA DATA TRANSFER CYCLE TIMING MODE	0100
WORD 53~255	RESERVED	ALLO

*1 ..... Controller Firmware Rev. "WS-xx-xx"
*2 ..... Controller model name PB4-AT-xxh (X : Don't care)

Table 4.4 Command error contents

	ERROR REGISTER ($1FI_H$)						STATUS REGISTER ($1F7_H$)				
	BBK	UNC	IDNF	ABRT	TKONF	AMNF	DRDY	DWF	DSC	CORR	ERR
FORMAT TRACK			V	V			V	V	V		V
IDENTIFY DRIVE				V			V	V	V		V
INITIALIZE DRIVE PARAMETERS							V	V	V		
RECALIBATE				V	V		V	V	V		V
READ BUFFER				V			V	V	V		V
READ DMA	V	V	V	V		V	V	V	V	V	V
READ LONG	V	V	V	V		V	V	V	V		V
READ MULTIPLE	V	V	V	V		V	V	V	V	V	V
READ SECTOR(S)	V	V	V	V		V	V	V	V	V	V
READ VERIFY	V	V	V	V		V	V	V	V	V	V
SEEK			V	V			V	V	V		V
SET FEATURES				V			V	V	V		V
SET MULTIPLE MODE				V			V	V	V		V
WRITE BUFFER											
WRITE DMA	V		V	V			V	V	V		V
WRITE LONG	V		V	V			V	V	V		V
WRITE MULTIPLE	V		V	V			V	V	V		V
WRITE SAME	V		V	V			V	V	V		V
WRITE SECTOR(S)	V		V	V			V	V	V		V
WRITE VERIFY	V	V	V	V		V	V	V	V	V	V
INVALID COMMAND CODE				V			V	V	V		V

V = Valid

BBK	Bad Block Detected	(Bit 7)
UNC	Uncorrectable ECC Error	(Bit 6)
IDNF	ID Not Found	(Bit 4)
ABRT	Aborted Command	(Bit 2)
TRONF	Track 0 Not Found	(Bit 1)
AMNF	Address Mark Not Found	(Bit 0)
DRDY	Drive Ready	(Bit 6)
DWF	Drive Write Fault	(Bit 5)
DSC	Drive Seek Complete	(Bit 4)
CORR	Corrected Data	(Bit 2)
ERR	Error	(Bit 0)

For information about the DIAGNOSTIC command, see Subsection 4.3.2, "Error register."

4.3.10 Alternate status register (3F6H)

The alternate status register contains the same data as the STATUS register. It differs, however, in that the INTRQ signal is not reset when the host reads this register.

4.3.11 Device control register (3F6H)

The device control register is used to specify disk INTRQ and soft reset.

bit7 Unused
bit6 Unused
bit5 Unused
bit4 Unused
bit3 Unused
bit2 SOFT RESET
  1: Reset on (all circuits are reset while "1".)
  0: Reset off
bit1 HEAD DISK INTERRUPT DISABLE
  1: INTRQ DISABLE (The INTRQ signal output is high impedance.)
  0: INTRQ ENABLE
bit0 Unused

This register is cleared to 00H when the hardware reset signal RESET– becomes active.

4.3.12 Drive address register (3F7H)

The drive address register is used to select the head and drive.

bit7 Undefined (high impedance)
bit6 WRITE GATE
bit5 HEAD SELECT 2^3
bit4 HEAD SELECT 2^2
bit3 HEAD SELECT 2^1
bit2 HEAD SELECT 2^0
bit1 DRIVE SELECT 1
bit0 DRIVE SELECT 0

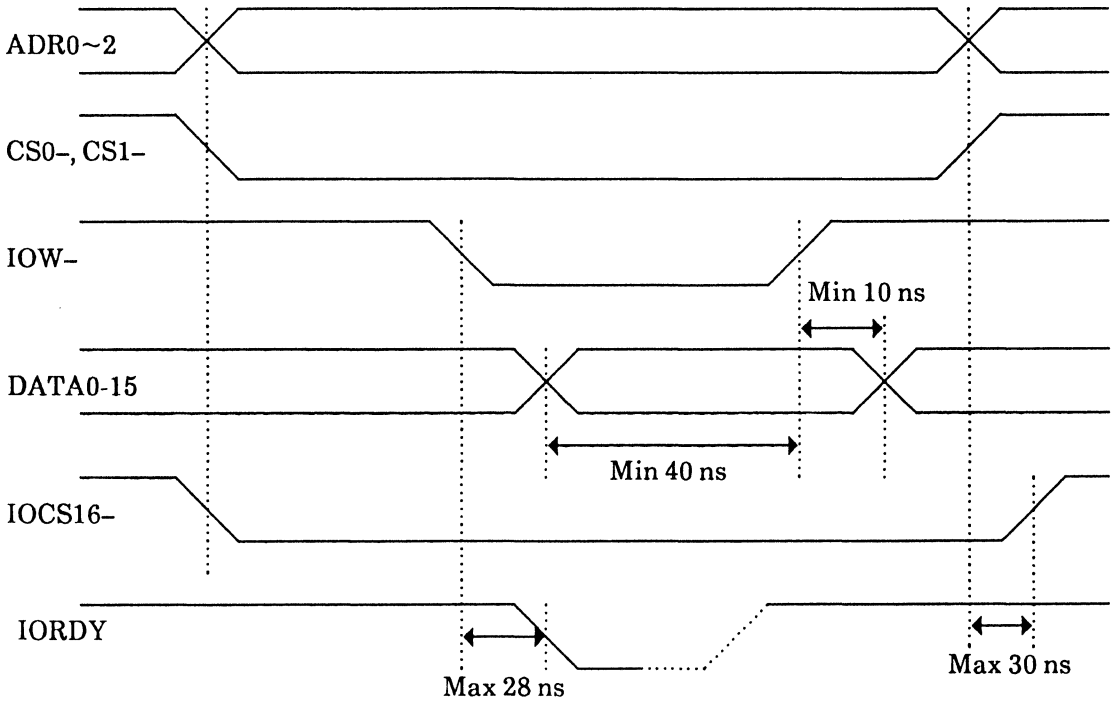
4.4 Host Interface Timing

On the device side, the interface signal driver is a 74LS244 or equivalent. The receiver is a 74LS245 or equivalent. The signal level is TTL-compatible.

Logical "1"	Logical "0"
2.0V(Min)	0.0V to 0.7V

4.4.1 PIO transfer

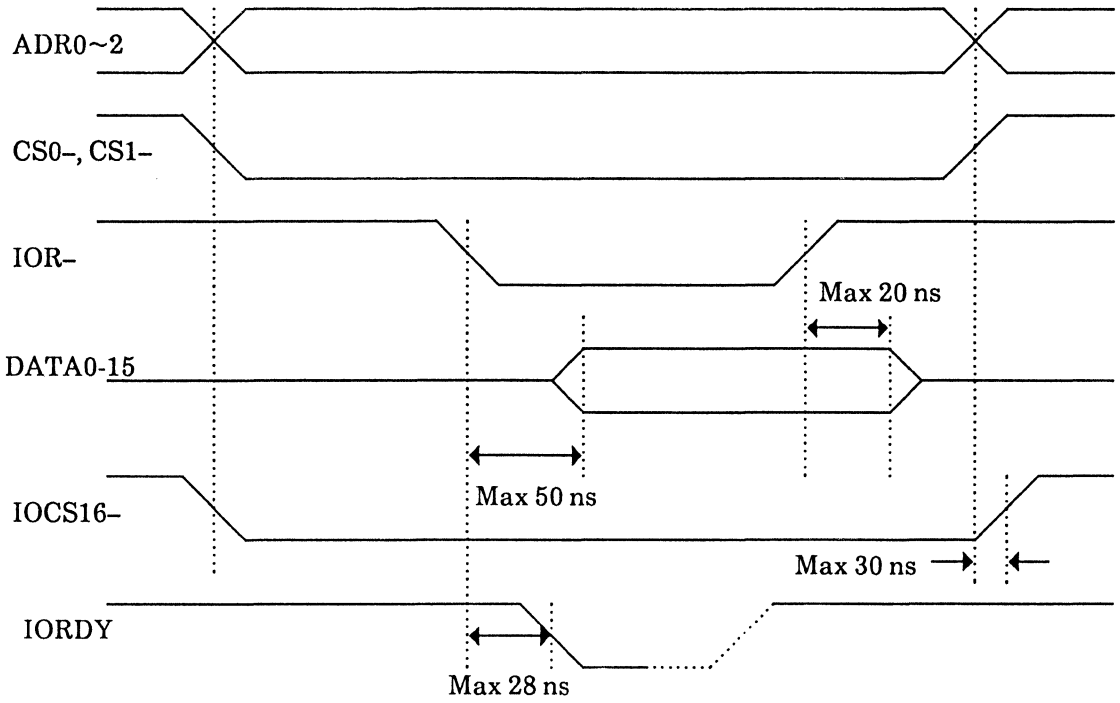
(1) Data write : When data is transferred from the host to the controller



*1: IOCS16- occurs only when the DATA register is accessed.

Figure 4.4.a Data write timing

(2) Data read : When data is transferred from the controller to the host

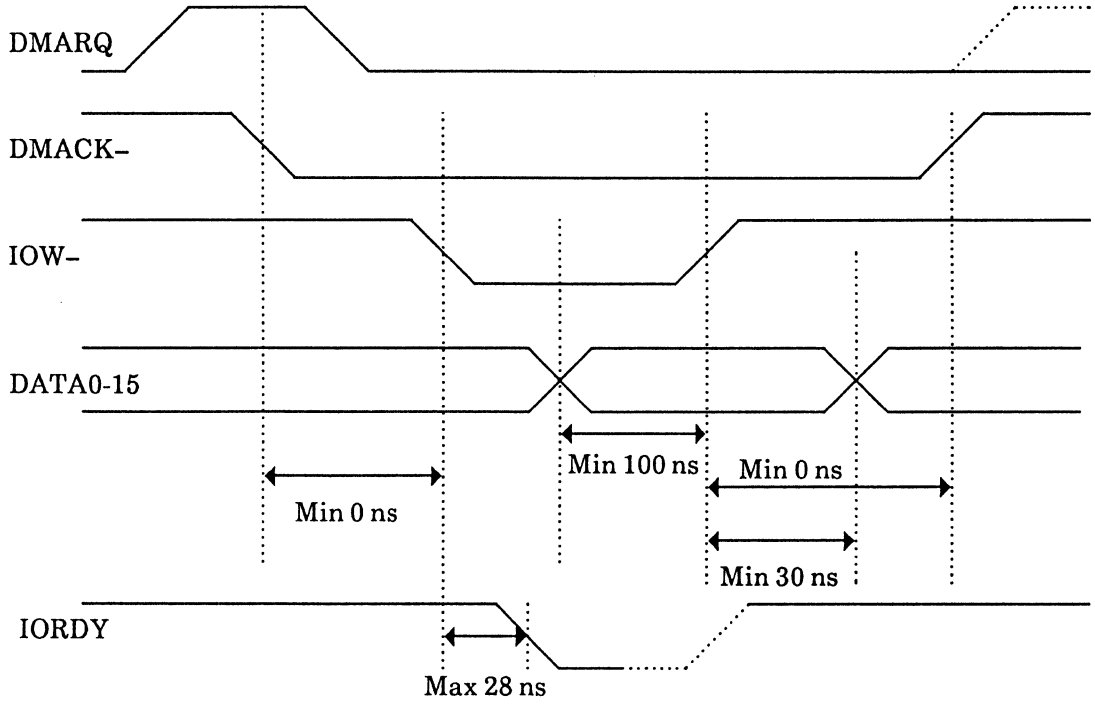


*1: IOCS16– occurs only when the DATA register is accessed.

Figure 4.4.b Data read timing

4.4.2 DMA transfer

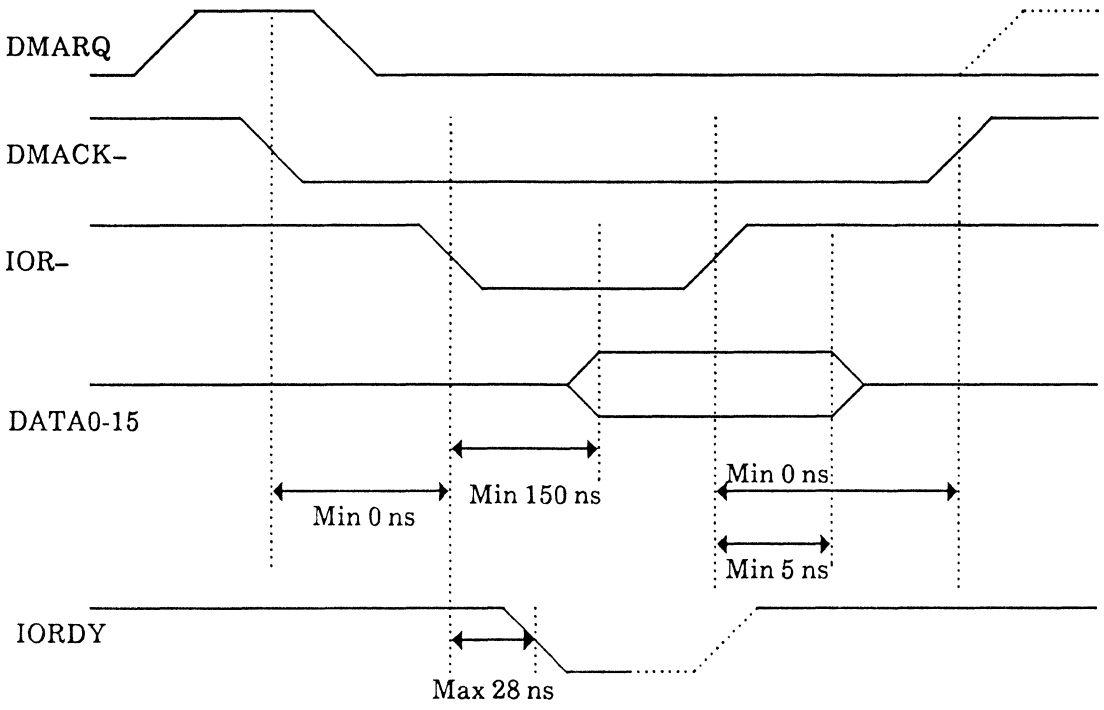
(1) Data write : When data is transferred from the host to the controller



*1 : IOCS16– does not change.

Figure 4.5.a Data write timing

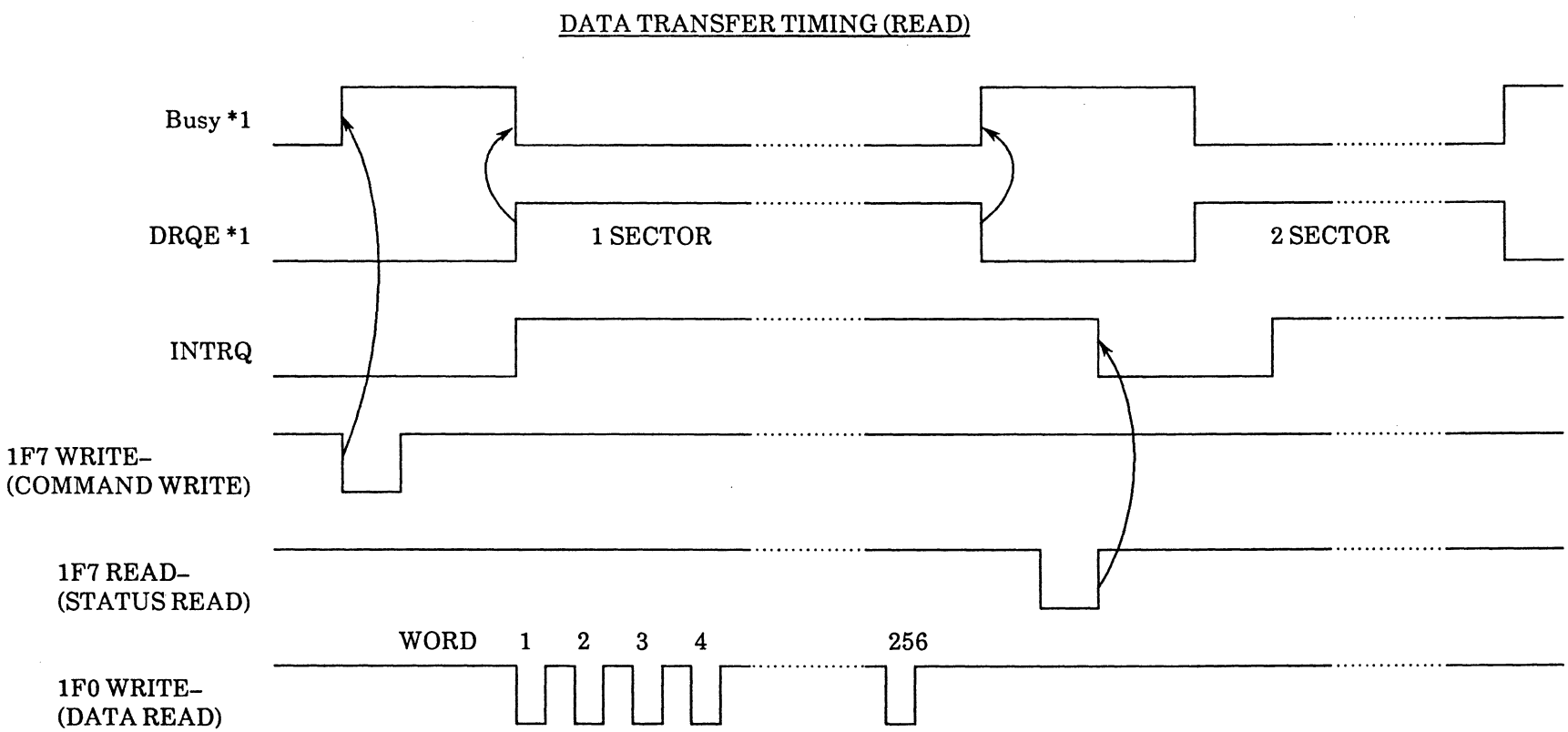
(2) Data read : When data is transferred from the controller to the host



*1 : IOCS16- does not change.

Figure 4.5.b Data read timing

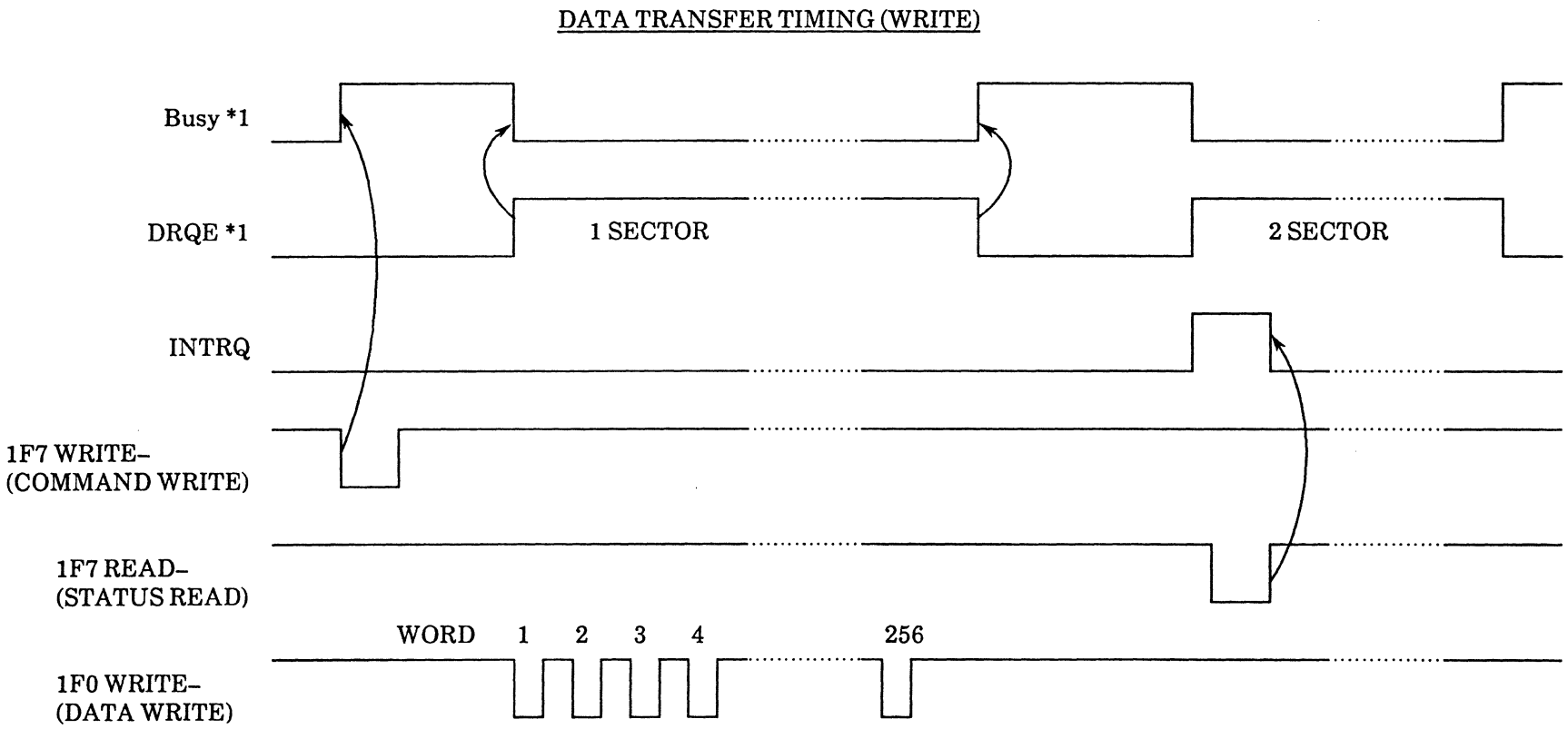
Reference example: IBM PC-AT BIOS



*1: BUSY and DRQE are bits in the 1F7H register.

Figure 4.6 Data transfer (read)

Reference example: IBM PC-AT BIOS



*1: BUSY and DRQE are bits in the 1F7H register.

Figure 4.7 Data transfer (write)

CHAPTER 5 DATA FORMAT

5.1 Data Space

5.1 Data Space

The disk drive manages the data storage area on the drive by classifying it into the following three types of data space:

① User space : Storage area for user data.
② CE space : Area reserved for specific purposes such as self-diagnosis
③ System space : Reserved area for disk drive

The user can explicitly access only the user space. The system space is accessed internally by the disk drive at power-on or during the processing of certain commands. It cannot be directly accessed by the user.

5.1.1 Cylinder configuration

The disk drive assigns three types of data space (user space, CE space, and system space) to each cylinder. Figure 5.1 shows the cylinder configuration. In addition to the logical configuration shown in the figure, the disk drive classifies all cylinders into four zones. Varying the recording density to make each zone the same permits an increase of the overall disk capacity.

(1) User space

The user space is used for user data. The data length of each sector in this space is always 512 bytes.

(2) CE space

The CE space is used for operations such as self-diagnosis. The data length of each sector is the same as that of the user space, 512bytes. The CE space always consists of one cylinder 1429 (595H), regardless of the device type.

(3) System space

The system space is dedicated to control. The data length of each sector is always 512 bytes. The system space always consists of five cylinders, 1430 (596H) to 1434 (59AH), regardless of the device type. The cylinder space contains the following information:

① Information on defects as delivered from factory (cylinder, track, sector shape) (P-LIST)
② Test information upon delivery from factory (factory information)
③ Control information (device information)
④ Defect management table

(4) Alternate cylinder

The alternate cylinder is used if a track has more than one defect.

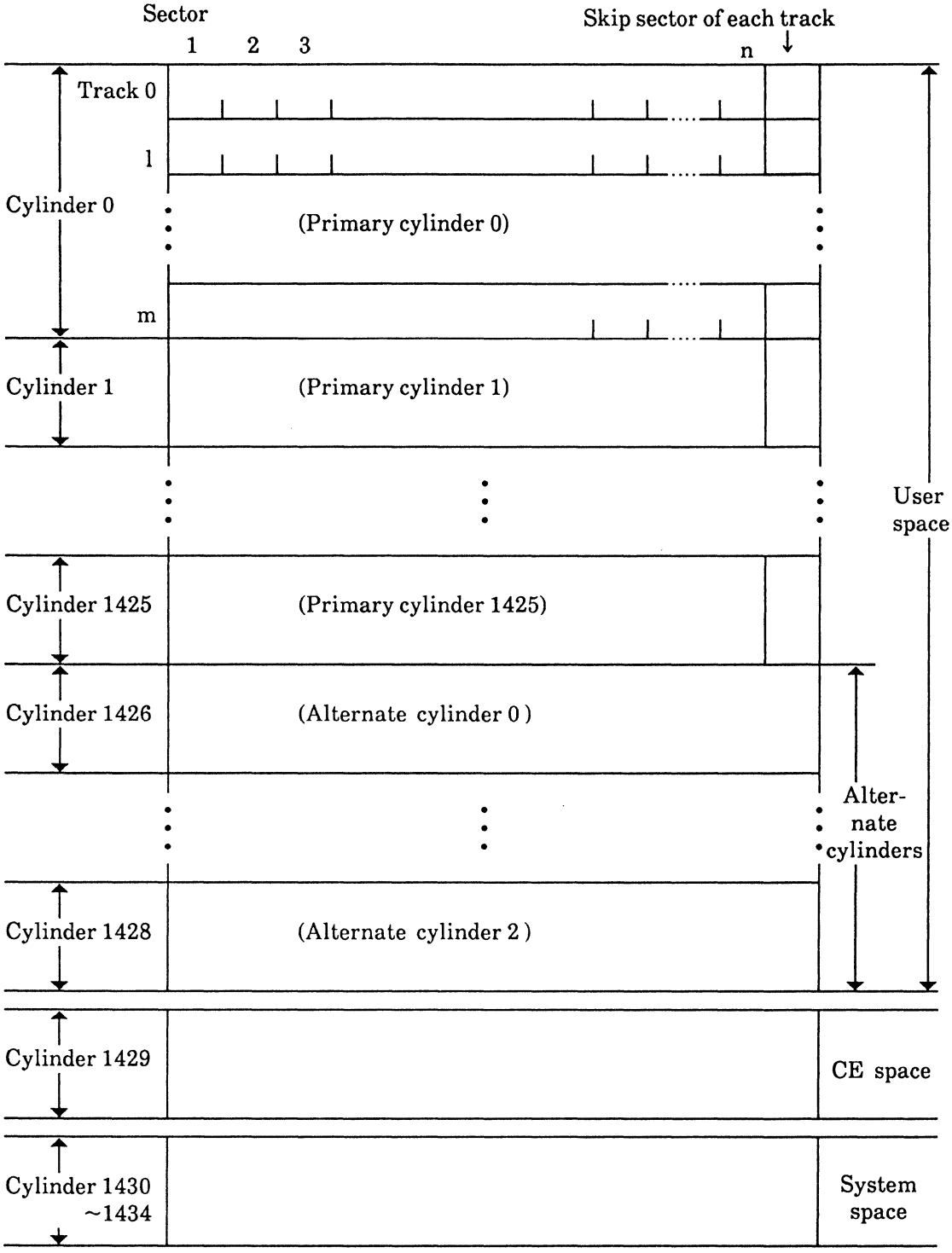


Figure 5.1 Cylinder configuration

5.1.2 Sector format

A sector on a track consists of an ID area, data area, and a gap area to separate the two. The format is 512 bytes / sector.

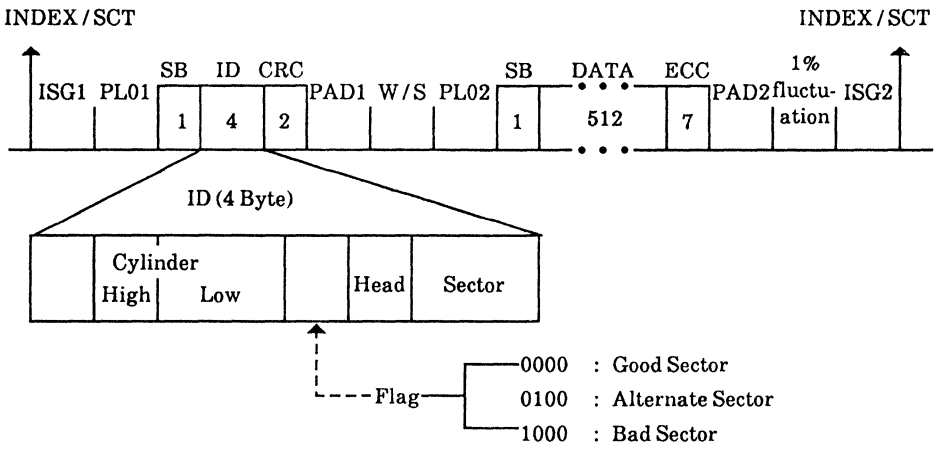


Figure 5.2 Sector format

Table 5.1 Sector format configuration

Logical data block length		512
Nominal physical sector length		594
Sector format	ISG1	24
	PL01	12
	SB	1
	ID	4
	CRC	2
	PAD1	2
	W/S	1
	PL02	12
	SB	1
	DATA	512
	ECC	7
	PAD2	4
	1% fluctuation	6
	ISG2	5~6

Unit : Byte

Each sector on a track consists of the following fields :

① ISG1, ISG2

These are inter-sector gap lengths. All "00" is written.

② PLO1, PLO2

All "00" of the specified byte length (12 bytes) required for PLO SYNC is written.

③ SB

The ID area and the data area of the sync byte are the same one-byte data of "FE".

④ ID

The ID area is four bytes and indicates the sector attribute and address information. Table 5.2 gives the ID area configuration.

⑤ CRC

CRC is the two-byte error detection code of the ID area. The generating function and the detection ability are as follows :

Generating function	:	$P = X^{16} + X^{12} + X^5 + 1$ Initial value "FF", sync byte "FE"
Detection	:	16-bit single burst max.

⑥ PAD1

PAD1 is a two-byte "00" pattern and guarantees the time immediately after CRC read to write splice.

⑦ W/S

W/S is the write gate switching area for write to the data area. When the disk is formatted, a one-byte "00" pattern is written.

⑧ DATA

The data area contains the data used for the read/write commands. The data area length is always 512 bytes. When the disk is formatted, a one-byte "00" pattern is written.

⑨ ECC

ECC is a seven-byte error detection/correction code for the data area. The generating function and the detection/correction ability are as follows :

Generating function : $P = X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^{8} + 1$

Initial value "FF", sync byte "FE"

Detection : 22-bit single burst max.

Correction : 11 bits max.

⑩ PAD2

PAD2 is a four-byte "00" pattern written when the disk is formatted or when the data area is written to. PAD2 assures the time immediately after ECC read to the write splice (write gate off).

⑪ 1% fluctuation

For write operations, the disk drive uses a self-regulating clock that is asynchronous with the servo clock. This prevents ISG2 from being overwritten because of lack of synchronization with the self-regulating clock if the disk revolution varies by more than 1%.

⑫ Physical sector length

The actual physical sector length cannot be obtained in integral values. The values are given below. This is a real value that is no greater than the nominal physical sector length and exceeds he nominal physical sector length minus 1.
Nominal physical sector length = 594 bytes

Table 5.2 ID area configuration

Byte	Bit	Name	Meaning
0	7	0	Reserved
	6	0	
	5	0	
	4	0	
	3	0	
	2	Cylinder 1024	Cylinder address
	1	" 512	
	0	" 256	
1	7	Cylinder 128	
	6	" 64	
	5	" 32	
	4	" 16	
	3	" 8	
	2	" 4	
	1	" 2	
	0	" 1	
2	7	Flag	FLAG (*1)
	6	Flag	FLAG (*1)
	5	0	
	4	0	
	3	Head 8	Head Number
	2	" 4	
	1	" 2	
	0	" 1	
3	7	Sector 128	Sector Number
	6	" 64	
	5	" 32	
	4	" 16	
	3	" 8	
	2	" 4	
	1	" 2	
	0	" 1	

*1 : This flag is written when the FORMAT TRACK command is executed and sector condition 80# or 40# is specified.

This page is intentionally left blank.

CHAPTER 6 MISCELLANEOUS INFORMATION

6.1 Disk Drive BIOS Specifications

The disk drive uses constant density recording technology (all cylinders are classified into four areas and the recording density varies in each area). The number of sectors per track varies with the area. Therefore, the disk drive constantly performs logical/physical translation (emulation) and the host must access the disk drive according to the BIOS specifications (logical parameters).

The number of sectors per track and the number of heads in the BIOS specifications are defined by the INITIALIZE DRIVE PARAMETERS (or SET PARAMETERS) command from the host.

Table 6.1 describes the BIOS specifications that allow the physical capacity of the disk drive to be used most effeciently. The disk drive has a low-level format with these parameters as shipped from the factory.

If able to change the fixed disk parameter table in the BIOS, the user can select parameters and incorporate them into the BIOS specifications. However, the selected parameters must satisfy the capacities listed in Table 6.1.

It is also possible to select items (within the capacity of Table 6.1) from the existing drive type table in the BIOS of the system. The disk drive operates as a device of the capacity of the selected drive type (parameter).

Table 6.1 BIOS specifications

	M2622T	M2623T	M2624T
Number of cylinders	1013	1002	995
Number of heads	10	13	16
Number of sectors / track	63	63	63
Format capacity	326.75MB	420.16MB	513.51MB

6.2 Low-Level Format

A low level format is a physical format. This is in contrast to high-level format "FORMAT C: (or D:)/S" executed as a DOS command.

6.2.1 Format when shipped

(1) BIOS specifications when formatting is executed

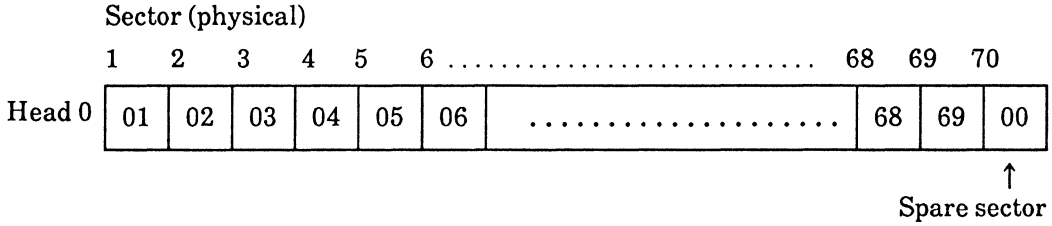
A low-level format is executed with the parameters listed in Table 6.1.

(2) Format contents

Defects (defective sectors) are replaced with alternate by utilizing one spare sector in each physical track and an alternate area (three cylinders). The disk is formatted such that defects are invisible to the host.

The example below shows the formatting of head 0 in zone 1. Numerals (01 to 69) are sector numbers written to the ID area.

① If there are no defective sectors on the target track



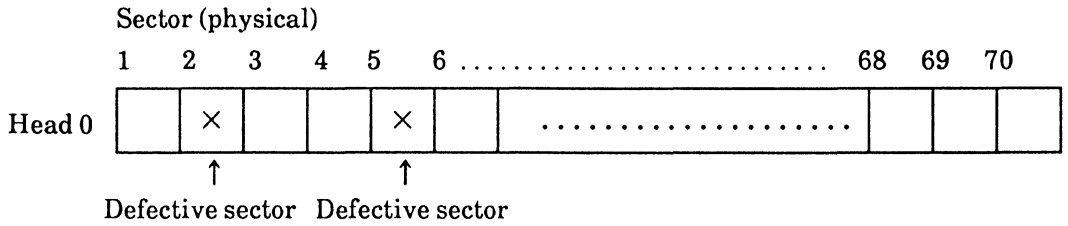
② If there is more than one defective sector on the target track

The defective sector having the lowest sector number is skipped. In other words, the defective sector is skipped, the sectors subsequent to the spare sector are shifted by one sector, and IDs are written.

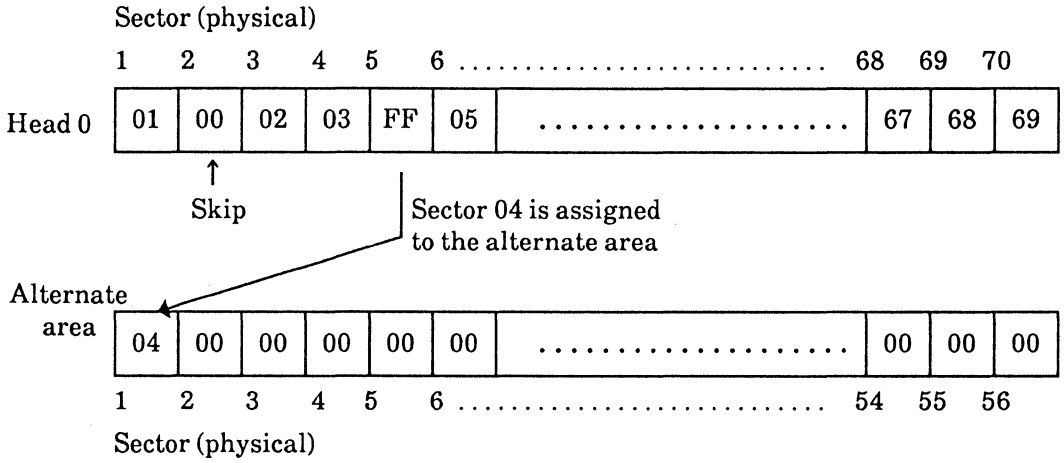
The second and subsequent defective sectors are assigned to alternate areas. This assignment is managed by the alternation management table generated on the SA cylinder.

In the example below, physical sectors 2 and 5 are defective:

a. Before formatting



b. After formatting



If the host executes a command to access sector 04 in the target track but fails to find sector 4, it then searches the alternation management table. Using the table, it accesses the alternate assignment destination.

6.2.2 Reformat

The FORMAT TRACK command reformats any sector of the disk drive formatted at the factory for additional alternation.

The FORMAT TRACK command executes a low level format in units of tracks for all sectors of a track specified by the INITIALIZE DRIVE PARAMETERS command.

However, if the disk drive is reformatted by the arbitrary number of sectors per track specified by the host, it only rewrites the ID area for the sector to which additional alternation is specified. Thus, the other sectors remain as is. (The cylinder, head, and sector written in the ID area are physical addresses.)

(1) Rules governing execution of low level format

① Defective sectors alternated during factory formatting cannot be made good by reformatting.

② The contents executed during reformat can be changed in later format execution according to the sector conditions described in (2), below. In other words, reformatting sectors of good to bad or bad to good is allowed.

If this is done, the P-List (defect information) of the SA cylinder is not updated. Therefore, if any sector is once formatted as bad, it is formatted as good in later formatting unless specified as bad again.

③ Transfer of a format parameter other than 1:1 interleave from the host results in an ABORTED COMMAND error (ERROR register bit 2 = 1).

(2) Sector conditions

The following four sector conditions can be specified:

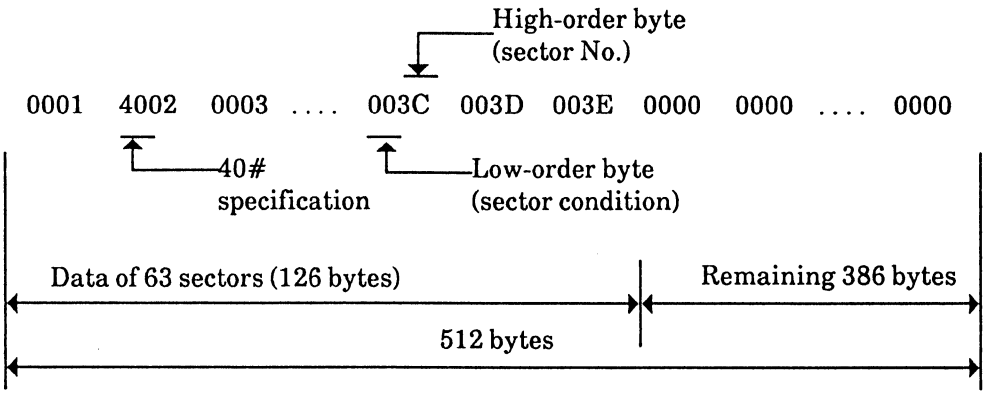
Sector condition	Contents of specification
00#	"Good" sector
20#	Reassigned from the alternate destination assigned.
40#	This sector is assigned to the alternate area.
80#	"Bad" sector (The bad sector flag is written in the ID area.)

(3) Format execution procedure

Follow the procedure below to execute reformatting.
Before formatting is executed, the number of sectors per track and the number of heads specified by the host must be defined by the INITIALIZE DRIVE PARAMETERS command.

① Specify the track address (cylinder and head).
↓
② Issue the FORMAT TRACK command.
↓
③ Transfer the format parameter.

This parameter is data of one sector (512 bytes) . The disk drive starts formatting after receiving the 512th byte.
The parameter data format is shown below.
In the example, there are 63 sectors per track and condition 40# is specified for sector No.02 (assigned to alternate area).
The parameter data is in word configuration for each sector. The high-order byte indicates the sector number and the low-order byte indicates the sector condition. The remaining portion, other than data on each sector, is filled with "0000."



If the defect information on the SA cylinder is destroyed by some cause, the disk drive reports an ABORTED COMMAND error upon receiving the FORMAT TRACK command.

FUJITSU COMPUTER PRODUCTS
OF AMERICA, INC.
2904 Orchard Parkway
San Jose, California 95134-2029, U.S.A.

FUJITSU COMPUTER PRODUCTS
OF AMERICA, INC.

Reader Comment Form

We would appreciate your comments and suggestions for improving this publication.

Publication No.	Rev. Letter	Title	Current Date

How did you use this publication?

☐ Learning ☐ Installing ☐ Sales
☐ Reference ☐ Maintaining ☐ Operating

Is the material presented effectively?

☐ Fully Covered ☐ Well Illustrated ☐ Well Organized ☐ Clean

What is your overall rating of this publication?

☐ Very Good ☐ Fair ☐ Very Poor
☐ Good ☐ Poor

What is your occupation?

Your other comments may be entered here. Please be specific and give page, paragraph and line number references where applicable.

Your Name & Return Address

Thank you for your interest. (Fold & fasten as shown on back, no postage needed if mailed in U.S.A.)

Tape Here Only

Fold

No Postage
Necessary
If Mailed
in the
United States

BUSINESS REPLY MAIL

First Class Permit # 7446 San Jose

Postage will be paid by Addressee

FUJITSU COMPUTER PRODUCTS
OF AMERICA, INC.
Technical Support Dept.
2904 Orchard Parkway
San Jose, California 95134-2029, U.S.A.

Fold

FUJITSU COMPUTER PRODUCTS
OF AMERICA, INC.

2904 Orchard Parkway, San Jose, California 95134-2029, U.S.A.
TEL: (1-408) 432-6333 FAX: 408-894-1709, 3908