GE PAC* 4020

COMPACT COMPUTER FOR PROCESS CONTROL

SYSTEM MANUAL

GENERAL ELECTRIC

*Reg. Trademark of General Electric Co.

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GENERAL ELECTRIC

PROCESS COMPUTER BUSINESS SECTION

PHOENIX, ARIZONA

CONTENTS

INTRODUCTION

SCOPE

This manual presents the specifications, internal organization, operation and machine-level programming characteristics of the GE/PAC 4020* central processor, bulk memories, peripheral devices, remotes and subsystems.

The machine-level programming information is included to help explain how the equipment works, not how it should be programmed. Virtually all the real-time and input-output functions required for process monitoring and control are implemented by calling sequences to the GE/PAC 4020 computer's Real-Time Operating System (RTOS), which differ from the machine-level formats in both scope and detail. This manual will refer to RTOS occasionally, in those situations in which RTOS software substantially enhances or adds to the features wired into the equipment.

For information on how to program the GE/PAC 4020 computer, please refer to the GE/PAC 4020 Programming Manual and to the detailed reference manuals on the languages (FORTRAN, PAL, TASC), operating systems and other useful programs.

FEATURES OF THE GE/PAC 4020 COMPUTER

Thanks to its monolithic integrated circuits and to its heritage from the GE 412 and the earlier members of the compatible GE/PAC 4000 process computer family, the GE/PAC 4020 computer combines high performance, high reliability, ease of programming and compactness. Its large command repertoire, long word, extensive input-output buffering, realistic process interface arrangements, and excellent safety characteristics offer unparalleled value for a wide variety of real-time applications. These features are aimed at reducing total project cost, not at reducing cost in one area at the expense of another.

The monolithic integrated circuits used in the GE/PAC 4020 computer reduce the number of active components, connections and wiring by a factor of five, improving system reliability. These circuits also greatly reduce the physical area required for a given function, improving noise rejection characteristics and permitting safe and solid operation at clock frequencies higher than those usable with conventional or hybrid circuits.

Accompanying the GE/PAC 4020 central processor is a full line of bulk memories, peripheral devices, process-oriented subsystems, and devices for remote communication and control, encompassing many application requirements.

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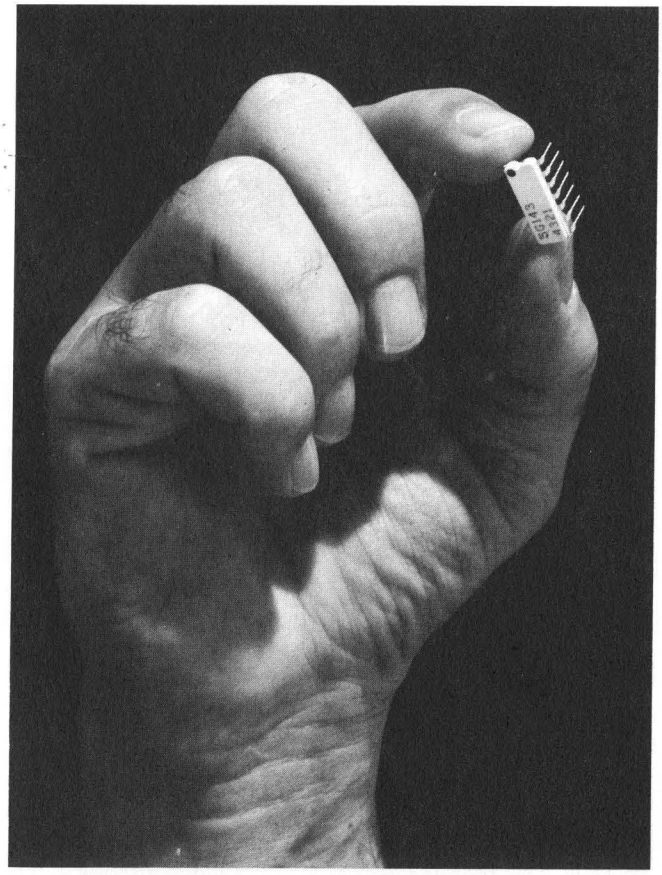
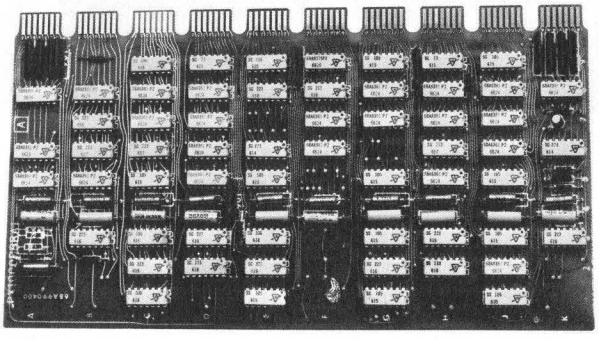


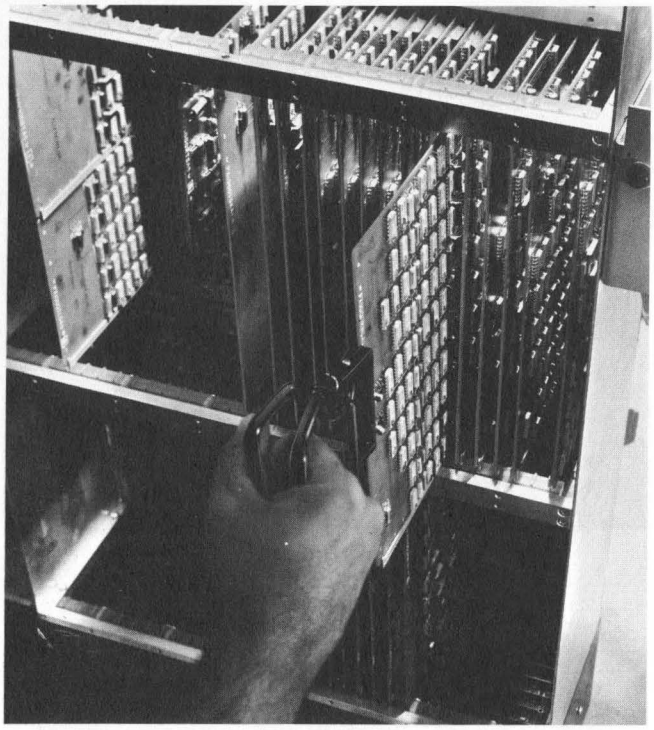


Related General Electric products include GE/MAC electronic process instrumentation, GE/TAC remote telemetering and supervisory control, GE X-Ray Emission Gages (XEG's) and other special sensors, Directo-Matic II wired-program analog and digital control equipment, GE 400 and 600-series scientific and data processing computer systems, GE datasets and microwave, GE Mark Century numerical control and the full line of GE electrical apparatus.

Software for the GE/PAC 4020 computer includes the Process Assembly Language (PAL), GE/PAC Process FORTRAN, the TASC control interpreter, the Real-Time and Free-Time Operating Systems, a full set of mathematical function subroutines, a Direct Digital Control package, numerous other specific application-oriented programs, the AID debugging program, and miscellaneous utility functions.

Unique features of the GE/PAC 4020 central processor include the TIM/TOM automatic input-output operations; Quadritect four-level core memory protection; and the use of quasi-instructions to encourage and make more efficient the use of floating-point arithmetic, circular lists, inverse to memory and other advanced operations. Additional features are its flexible and powerful memory addressing capabilities and both word-logical and bit-logical hardware.

Process-oriented features of special value include automatic prevention of analog scanner and output controller multiple selections, avoiding upsets to processes caused by computer failures; three stall alarms covering a wide range of possible software and hardware problems; over-temperature detection in the cabinetry and on the bulk and working memories; and analog and contact output devices with enough current and power capability to remove the requirement for interposing devices or circuits.



THE GE/PAC 4020 CENTRAL PROCESSOR

ORGANIZATION

The GE/PAC 4020 computer is a binary, fixed word length, single-address, highly parallel computer utilizing a parallel adder for arithmetic and word-logical functions and a serial adder for bit-logical functions. Figure 1 shows this processor's internal organization in a simplified manner.

Of the three input-output methods shown, the great majority of the work is done either by direct memory access or by the arithmetic unit channels via TIM/TOM. The channel to and from the "A" register exists mainly to provide compatibility with the GE/PAC 4040 computer and to drive the contact sensing subsystem.

Certain functions — primarily indexing and the secondary accumulator ("Q" location) — are performed by a combination of dedicated core locations and special control hardware, but are programmed just as if they were active-component registers.

REGISTER AND CONTROL FLIP-FLOP DESCRIPTIONS

Not counting the registers and other hardware used to implement its automatic program interrupt, TIM/TOM input-output or optional Quadritect memory protection features, the GE/PAC 4020 computer uses seven integrated circuit registers, eight special-purpose dedicated core locations and two full adders in executing programs:

A register (24 bits, including sign). This is the primary working register, involved in nearly all instructions and tests. "A" uses the serial full adder for bit operations and the parallel full adder for arithmetic and word-logical operations. "A" contains one of the two numbers involved in the elemental arithmetic operations and receives all or the most significant part of the result, except for division, after which "A" contains the remainder and "Q", the quotient.

Q location (24 bits, including sign). This special-purpose core location, 10_8 in all systems, supplemented by special hardware, acts as an extension of the "A" register during multiplication, division, double-length logical and arithmetic shifts, and double-length load, store, add and subtract operations.

P register (15 bits). This register contains the address from which the next instruction will be fetched. It works in conjunction with the parallel full adder and the "I" register to implement the GE/PAC computer's program control operations. The "P" register can address 32,768 core locations.

X locations (15 bits). These seven special-purpose core locations, $1 - 7_8$ in all systems, and their associated hardware facilitate processing tables of data by the method of automatic operand address modification and addressing memory beyond 16K. Five of the seven are available without restriction and are stored by software whenever an interrupt is acknowledged, along with "A", "Q", "P", and the states of several important flip-flops. The other two "X" locations are usable in special situations. The unusually large number of index locations reduces programming effort.

I register (25 bits). This register contains the instruction being executed and with the main adder computes and holds the actual, direct operand address (up to 32K) that results from the four primary memory addressing modes and their combinations.

J register (five bits). This register contains the lengths of shift instructions ($0-31_{10}$ places) and the count resulting from the bit-counting instructions. The contents of "J" can be transferred into any of the "X" locations by a single instruction, for further use.

B register (24 bits). This register acts as a buffer between the core registers, the arithmetic unit, and various input-output channels. It also assists in "Q" operations.

MAB (memory address buffer, 15 bits). This buffer consists of selection circuits and addresses both operands and instructions stored in up to 32K locations.

MDR (memory data register, 25 bits including parity). This register holds operands and instructions on their way to and from core.

In addition to these registers, adders and core locations, the GE/PAC 4020 computer employs four control flip-flops. The states of these flip-flops are stored in memory during interrupts or subroutine entries by the save place and branch (SPB) instruction and are reloaded by load place and restore (LPR).

Test flip-flop (TSTF). Numerous test instructions set or reset this flip-flop, which then controls the direction of conditional branches. Separating these functions allows very efficient testing and branching in the numerous situations where there are only two possible exits from a series of conditions being tested.

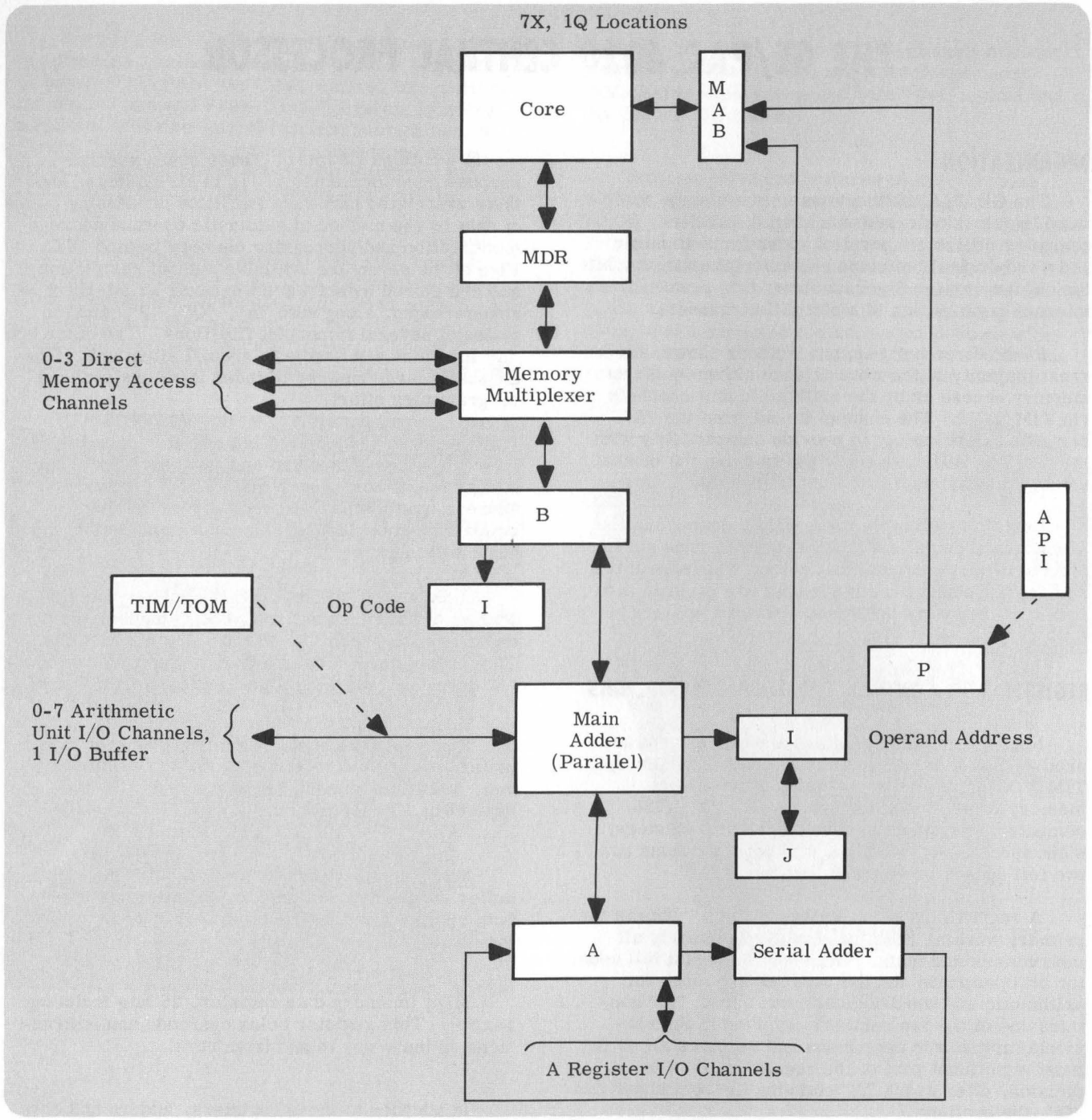


Figure 1
GE/PAC 4020 Computer Simplified Block Diagram

Overflow flip-flop (OVRF). Operations exceeding the capacity of the "A" register cause a carry to propagate into the sign bit position, setting this flip-flop. Examples are all arithmetic operations, whether fixed-point or floating-point, and arithmetic shifts. Floating-point underflow is detected by the floating-point quasi's; the result is replaced by zero.

Permit automatic interrupt flip-flop (PAIF). Actually two flip-flops, this function can permit all the interrupt levels, inhibit just the so-called "inhibitable" interrupts (IAI1), or inhibit all of them (IAI2). The first pulse reaching an inhibited portion of the API system will be stored in its flip-flop, but action will not be taken until a permit automatic interrupt (PAI) instruction enables the system again.

Trapping mode flip-flop (TMFF). This enables or disables the GE/PAC 4020 computer's Quadritect memory protection.

CORE MEMORY

General Characteristics and Operation

A coincident-current, three-wire magnetic core memory system is used in the GE/PAC 4020 computer, up to a maximum of 32,768 words.

Memory full-cycle time for the GE/PAC 4020 computer is 1.6 microseconds. The memory unit contains its own timing and control to enable external device controllers to share the core memory with the arithmetic unit, thereby reducing overall processing time.

Each word in the core memory contains 24 bits plus a parity bit. The parity circuitry generates an odd parity on the write cycle and checks on the read cycle for an odd total of "1's". The core word is restored as read, whether or not a parity error occurs.

Since 14 bits of each instruction are used for memory addressing, one instruction has direct access to 16,384 core locations and access to any of 32,768 locations by indexing or indirect addressing.

The numerous instructions that do not address memory use this field for microcoded elaborations on their basic operation code, device and channel selection, length of shift, or constants. This last use provides a form of "immediate mode" operation that saves both time and memory.

Memory Multiplexer

This device switches the core memory between the arithmetic unit and three channels to external controllers. The arithmetic unit is given lowest priority because it can always wait for access if necessary. The external controllers drive high data-rate devices such as bulk memories, data links to other computers, data acquisition for telemetering systems, and high-speed peripherals. For high-speed peripherals, up to eight controllers can share a single channel. Each can operate up to four devices, one at a time.

The memory multiplexer operates on a true cycle-stealing basis. Once any of the controllers has made several accesses to core to load its control words, it makes only one access (1.6 μs) for each succeeding operation. Even while cycles are being stolen in this manner, the arithmetic unit will continue to execute its current instruction, stopping only when it needs another access to core that cannot be granted at that instant.

Using these three cycle-stealing channels, the GE/PAC 4020 computer can communicate with a large number of high data-rate devices in the most efficient possible manner.

Dedicated Addresses

The following dedicated memory locations are typical of the GE/PAC 4020 computer, if the named function is provided. Also, all are addressable and usable with any GE/PAC command.

OCTAL	FUNCTION
00	Primary bulk storage pointer word
01 – 07	Index location words
10	Q location word
11 – 17	Additional bulk storage pointer words
20	Memory protect error exit location (SPB)
21	Memory protect, saved I-register word
22	Not dedicated
23	" "
24	API stall alarm error exit location
25	Not dedicated
26	" "
27	" "
30	" "
31 – 37	Common peripheral pointer words
40 – 77	Quasi instruction branch vectors
100 – 177	Memory protect status words
200 – 377	8 to 128 automatic program interrupt response locations. They may contain:
(variable)	(a) Transfers to driver programs (SPB, BRU) (b) Memory decrement and test (DMT) for timing, counting (c) Table I/O (TIM/TOM) control words for input-output (d) No operation (NOP)

Quadritect Memory Protection

This optional feature virtually assures that a new program being debugged on-line under the GE/PAC Free-Time System cannot interfere with running process programs, the Real-Time Operating System, the I/O equipment or any other part of the hardware, the software or the process.

Quadritect permits the identification of four possible types of protection for each 64-word block of core memory:

read, execute or write (anything allowable) -- 11

read or execute, but not write -- 01

read or write, but not execute -- 10

inaccessible (nothing allowable) -- 00

The instruction portions of the program being debugged will use as appropriate areas defined as 11 and 01; data portions, 10.

This status information is stored in up to 64 protect status words in core locations 100 - 177_8, each of which gives the status for eight 64-word blocks, or 512 words. Figure 2 shows their layout.

When Quadritect is enabled (by setting the trapping mode flip-flop with a special "OUT" command), special hardware immediately begins examining instruction operation codes and operand addresses and fetching from core into the protect status word register (PSWR) the status word describing the block being referenced. When a reference is attempted to a block not described by the present word, the relevant word is fetched. The status word address register keeps track of which 512-word block is covered by the word presently in the PSWR.

In no case is any instruction in a program being debugged allowed to execute I/O instructions, to prevent errors and conflicts with the Real-Time Operating System (RTOS). I/O calls to RTOS and certain other situations too complex to handle solely by hardware, are trapped, examined by software, and executed only if they reference I/O devices or subsystems specified by the programmer as allowable. This feature, combined with the Quadritect hardware, allows the programmer to check out his program's logic under severe restrictions, then gradually remove constraints as he identifies and corrects errors and progresses toward his goal — a correctly running program.

Attempted violations of Quadritect or the software restructions causes a branch to core location 20_8, which in turn transfers control to a diagnostic program. This program then turns off the offending program and prints out a summary of the attempted violation, to help the programmer diagnose and correct his error.

It is important to realize the Quadritect does require some software, is intended primarily for on-line debugging using the Free-Time System rather than for normal operations, and at any one instant can enforce only one of the four possible types of protection for each core block. If Quadritect were left enabled during normal operations, it could practically protect only those fixed areas (not subject to dynamic relocation) whose selected type of protection applied to all system programs.

In this Quadritect approach, GE offers flexible, in-depth protection useful when protection is really needed — during on-line debugging — rather than offering a modest level of protection active at all times and really adequate at no time.

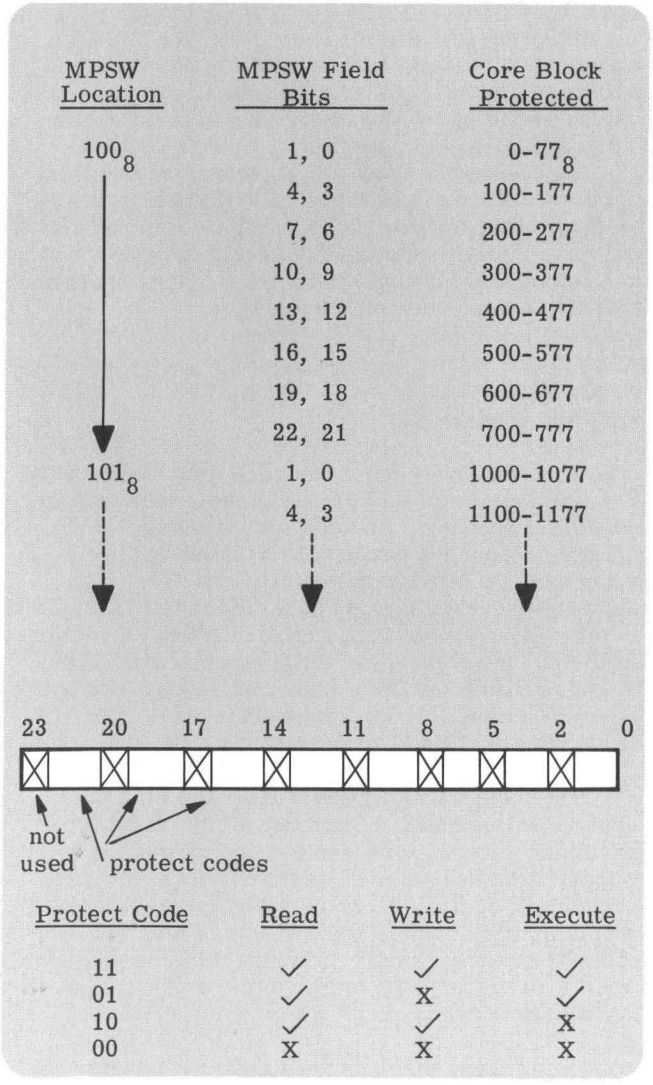


Figure 2
Memory Protect Status Words (MPSW)

ARITHMETIC UNIT

Commands

Major Types

The GE/PAC 4020 computer accepts two types of commands, wired and quasi. The first is executed without further references to memory, except for operands; the second causes an automatic entry and return from a subroutine. This feature saves programming effort, bulk memory and running time, since it allows the GE/PAC 4020 central processor to have a larger and richer command repertoire, to be essentially program-compatible with the earlier GE/PAC 4000 computers, and to offer the programmer such powerful features as circular list processing and floating-point arithmetic.

The total amount of core required for the entire GE/PAC 4020 quasi package is approximately 700 words, which includes floating-point arithmetic. This block of words is included in the 5-6,000 words generally considered as RTOS's core requirement.

The GE/PAC 4020 computer's command repertoire consists of 112 commands — 92 wired and 20 quasi's. There are 37 of these which reference memory — 21 wired and 16 quasi's — and 60 which represent unique and useful microcoded variations of three of the GE/PAC 4020 computer's 44 primary operation codes. Of the unused operation codes, three — 75, 76 and 77 — will cause quasi operation and can be used for special system instructions or macroinstructions.

Formats

Instructions

Although the PAL Assembler takes care of assembling operation codes, addresses and parameters into the following formats, it is occasionally desirable to know them when debugging.

In all the formats, bits 23-18 are either the sole operation code or the primary one. Bits 17-15 specify the index location (if any) whose contents will be added to bits 13-0 of the instruction before execution. While the primary use of this feature is automatic address modification of full operand instructions, it will also produce the stated result when used with other types of instructions.

Bits 14-0 vary in significance depending on the instruction type.

The GE/PAC 4020 central processor's full operand mode references memory either directly or relative to the instruction's location, depending on whether bit 14 is a zero or a one. The GE/PAC 4020 computer, like the rest of the GE/PAC 4000 series, uses relative addressing for locations within a program and direct addressing for fixed locations outside it. Then, whenever the Real-Time Operating System wants to bring a program from bulk memory into core and run it, RTOS only needs to find an area large enough without regard to its starting address, saving both running time and core. Since the internal memory references are relative to wherever the program happens to be, the program will still run correctly. This feature, called "dynamic relocatability", allows true multiprogramming.

The relative address may be positive or negative, as shown by bit 13. If bit 13 is a one, bits 12-0 contain the two's complement of the relative address.

Certain instructions, such as add constant to A (AKA) use the full operand format but carry their operands with them, in bits 13-0. A form of "immediate mode" addressing, this saves considerable memory and time when it is usable.

The second major format, called GEN 1, covers commands used for bit manipulation of the "A" register. Bits 14-5 are microcoded elaborations on the basic operation code for this format, 05, and bits 4-0 specify the particular bit position desired, counting down from left to right, or specify the length of shift. GEN 1 operations include right shifts, masking, testing, and counting.

GEN 2, distinguished from GEN 1 by its operation code, 25, is used for I/O operations involving the "A" register channels. Bits 14-12 are microcoding; bits 11-0 contain a device number. One instruction selects the device and transfers the data to or from it. A GE/PAC 4020 computer could address up to 2048 devices, if necessary.

GEN 3, 45, handles left shifts of A and left or right shifts of A and Q together. Bits 12-5 are microcoded; bits 4-0 specify the length of shift, $0\text{-}31_{10}$ positions.

The GE/PAC 4020 computer offers the two formats below for fixed-point arithmetic. The double-word format is seldom necessary and is used mainly for large accumulations.

Multiply develops a 46-bit plus sign product from two 23-bit plus sign factors, and divide develops a 23-bit plus sign quotient and a 23-bit plus sign remainder from a 46-bit plus sign dividend and a 23-bit plus sign divisor.

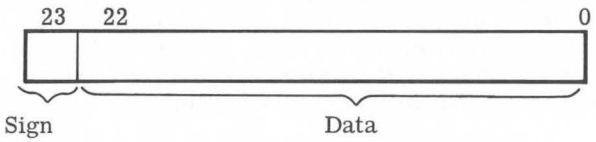
The fixed-point formats represent negative numbers in two's complement form. The double-word format ignores the second word's sign bit and uses the sign bit of the first word for the entire number.

	23 22 21 20 19 18	17 16 15	14 13	12 11 10 9 8 7 6 5 4 3 2 1 0
FULL OPERAND Hardware	OP	X	*	Y
GEN 1	000101	X	G	K
GEN 2	010101	X	S	D
GEN 3	100101	X	G	K

OP Instruction octal
X Index word address
* Relative addressing indicator
Y Operand address (a few instructions use Y as the operand; others use Y as the address of the operand)
G Micro-coded GEN 1 subcommand
K Bit position of A-register or length of shift
S GEN 2 subcommand
D I/O device address (bits 9, 10, 11 = 7/8 for high speed I/O)

GE/PAC 4020 Computer Instruction Formats

Single-word fixed-point

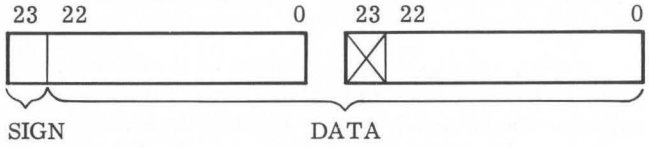


0 = +
1 = -

(Two's complement if negative)

Range: +8,388,607 to -8,388,608

Double-word fixed-point

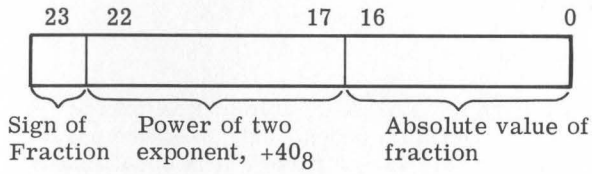


Range: +70,368,744,177,633 to -70,368,744,177,664

The GE/PAC 4020 computer's floating-point representation uses a sign and absolute value notation for the fractional part (mantissa) and an offset exponent for the characteristic. This is a self-normalizing floating-point, to preserve maximum precision without extra programming effort.

Two modes of floating-point arithmetic are available. The single-length mode is adequate for the simpler mathematical process and control relationships, since it provides 17 bits of precision, equivalent to about five decimal digits. The double-length mode is useful for more sophisticated models, linear programs, and other operations involving large matrices and provides about 11 digits. Both modes can be made available in the same central processor, selectable by the floating mode shift (FMS) command, though it remains the programmer's responsibility to use the modes and formats consistently and correctly. Accompanying this quasi package are fix and float conversion commands; they could be used with an FMS to convert between formats, or a new quasi could be written and assigned one of the unused quasi operation codes.

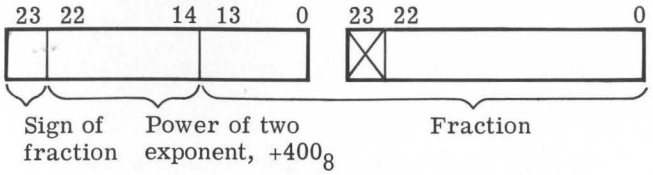
Single-word floating-point



0 = +
1 = -

Range (approximate): $\pm 2.15 \times 10^{\pm 9}$

Double-word floating-point



Range (approximate): $\pm 5.8 \times 10^{\pm 76}$

Memory Addressability

A single full operand instruction can address 16,384 words directly. In systems with more than 16K, direct addressing references the first 16K, in which the Real-Time Operating System subroutines and common data areas are generally found. In the relative mode, the GE/PAC 4020 computer can address any location within +8191 or -8192 locations of the instruction, regardless of memory size.

By using one of its seven index locations as a base address register, or by using its indirect load, store or branch instructions (LDI, STI, LPR), the computer can address any of its maximum 32,384 words of memory. The use of either mode for this purpose is rare, primarily because most instructions either reference locations within their own program (seldom as large as the 16K range available) or locations within the first 16K.

There are also available various interesting combinations of indexing and direct, indirect, relative, and "immediate mode" addressing. In the relative-indexed mode, the relative operation is carried out before the index location's contents are added.

Circular Lists

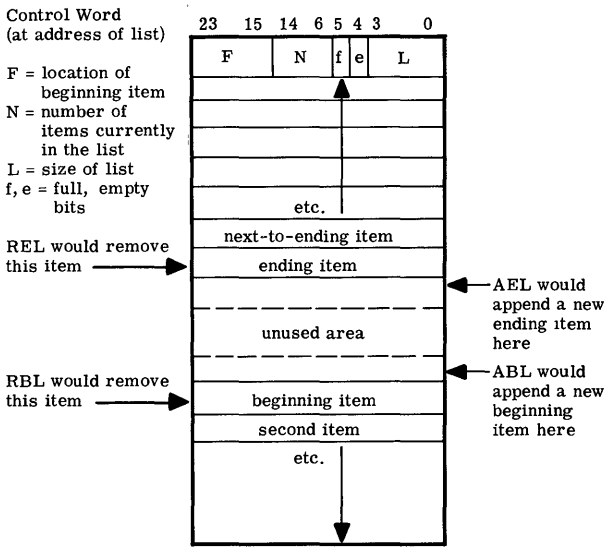
A circular list consists of a set of consecutive items contained within a fixed length block of memory. The first word of the block is a list control word. The size of the list must be a power of two, from one to eight.

Quasi-instructions append additional items to the beginning (ABL) or end (AEL) of the list and remove the beginning (RBL) or ending (REL) items. The address of the beginning and ending items changes as items are added and removed, as does the size of the unused area.

An item, when appended, becomes the new first or last item. The removal of an item forces the adjacent item to become the new beginning or ending item.

These lists are most useful for inter-program communication, since the appending and the removing programs can operate at different speeds and even at different times. Each program must know only the address of the control word. Each program must also incorporate logic to handle the "full" or "empty" conditions, depending on whether it is appending to or removing from the list.

Items processed through a list must either not require identification or must carry it with them; the usual implicit identification of its contents by an address does not pertain.



Circular Lists

Counting and Time Keeping

Any location in the GE/PAC 4020 computer's core memory can be used for counting external pulses, for maintaining a real-time or elapsed-time clock, or for program loop counting. The decrement memory and test (DMT) instruction, when used as an automatic program interrupt response command, acts as a one-instruction subroutine to accomplish this function.

When a pulse comes in, the DMT decrements a count preset into a designated core location. When the count passes from zero to minus one, the DMT generates an "echo" interrupt that notifies the relevant program to reset the count and take appropriate action.

The total time taken away from the running programs is only 4.8 μs per event counted, since none of the AU's contents are disturbed, although some additional time is required to store and reload registers and to run the response program when the count runs down and the "echo" is processed.

Another advantage of this approach is that counts are not lost when the a-c power voltage or frequency goes out of limits, since the core's contents are protected against this contingency.

CODE	NAME	EXECUTE TIME	ADDRESSING REL.	ADDRESSING INDEX	OCTAL CODE
ABL	Append Item to Beginning of List	*130.0	X	X	57x*Y
ABT	Abort	*** 8.5 & 26.5		X	25x3D
ACT	Activate Device	*** 8.5 & 26.5		X	25x1D
ADD	Add	3.2	X	X	11x*Y
ADO	Add One to Bit K	4.7		X	05x0700K
AEL	Append Item to End of List	*125.0	X	X	47x*Y
AKA	Add K to A	* 6.4		X	60x0K
ANA	AND to A	3.2	X	X	20x*Y
BRU	Branch unconditionally	1.6	X	X	14x*Y
BTR	Branch if TSTF Reset	1.6	X	X	30x*Y
BTS	Branch if TSTF Set	1.6	X	X	34x*Y
CBK	Change Bit	4.7		X	05x4700K
CLO	Count Least Significant Ones	4.7			05004137
CLZ	Count Least Significant Zeros	4.7			05070137
CMO	Count Most Significant Ones	4.7			05004237
CMZ	Count Most Significant Zeros	4.7			05070237
CPL	Complement A	4.7			05010000
DAD	Double Add	* 48.8	X	X	51x*Y
DLA	Double Left Arithmetic Shift	4.8 - 8.0		X	45x0644K
DLD	Double Length Load	* 25.6	X	X	41x*Y
DLL	Double Left Logical Shift	4.8 - 8.0		X	45x0720K
DMT	Decrement Memory and Test	4.8	X		060*Y
DRA	Double Right Arithmetic Shift	4.8 - 8.0		X	45x0440K
DRC	Double Right Circular Shift	4.8 - 8.0		X	45x0530K
DRL	Double Right Logical Shift	4.8 - 8.0		X	45x0430K
DST	Double Length Store	* 28.8	X	X	63x*Y
DSU	Double Subtract	* 42.4	X	X	61x*Y
DVD	Divide	13.7	X	X	65x*Y
ERA	Exclusive "OR" to A	3.2	X	X	10x*Y
FAD	Floating Add Single/Double	*203.0/295.0	X	X	70x*Y
FDV	Floating Divide Single/Double	*182.0/288.0	X	X	73x*Y
FIX	Fix Floating Number Single/Double	*111.0/112.0		X	74x0K
FLO	Float Fixed Number Single/Double	*123.0/145.0		X	74x2K
FMP	Floating Multiply Single/Double	*151.0/216.0	X	X	72x*Y
FMS	Floating-point Mode Shift	*208.0			74x3K
FSU	Floating Subtract Single/Double	*208.0/300.0	X	X	71x*Y
IAI1	Inhibit Automatic Interrupt	2.2			25030000
IAI2	Inhibit Automatic Interrupt	2.2			25040005
IBK	Isolate Bit K	4.7		X	05x0100K
IN	Input from Device D	*** 8.5 & 26.5		X	25x5D
INX	Increment Index	4.8	X	X	26x*K2
JCB	Jump Channel Busy	*** 8.5 & 26.5			25x6D4D
JDR	Jump if Device D Ready	*** 8.5 & 26.5		X	25x6D2D
JND	Jump if no Demand	2.2			25040000
JNE	Jump if Device D not in Error	*** 8.5 & 26.5		X	25x7D
JNO	Jump if No Overflow	2.2			25060000
JNP	Jump if No Parity Error	2.2			25070000
JNR	Jump if Device D not Ready	*** 8.5 & 26.5		X	25x6D
LBM	Load Bit Mask	4.7		X	05x6300K
LDA	Load A-Register	3.2	X	X	00x*Y
LDI	Load Indirect	* 35.1	X	X	52x*K
LDK	Load A with K	* 6.4	X	X	40x*Y
LDO	Load One into Bit K	4.7		X	05x0300K
LDP	Load Place	3.2	X	X	15x*Y
LDQ	Load Q-Location	4.8	X	X	42x*Y
LDX	Load Index Word	4.8	X	X	16x*Y
LDZ	Load Zeros into A	4.7			05000000
LMO	Load Minus One	4.7			05060000
LMR	Load API Mask Register #1	2.2			25000302
LMR2	Load API Mask Register #2	2.2			25000300
LPR	Load Place and Restore	3.2	X	X	35x*Y

CODE	NAME	EXECUTE TIME	ADDRESSING REL.	ADDRESSING INDEX	OCTAL CODE
LXC	Load Index with Count	4.8		X	17x00000
LXK	Load Index with K	3.2	X	X	07x*K
MAQ	Move A to Q	7.3			45004330
MPY	Multiply	8.9 - 12.1	X	X	55x*Y
NEG	Negate	4.7			05013000
NOP	No Operation	4.8			26200000
OOM	Operate on Memory	* 60.8	X	X	62x*Y
OPR	Operate Device D	*** 8.5 & 26.5		X	25x2D
ORA	OR to A	3.2	X	X	21x*Y
OUT	Output to Device D	*** 8.5 & 26.5		X	25x4D
PAI	Permit Automatic Interrupt	2.2			25020000
RBK	Reset Bit K	4.7		X	05x4500K
RBL	Remove Beginning Item from List	*122.0	X	X	56x*Y
RCS	Read Console Switches	2.2			25050000
REL	Remove End Item from List	*136.0	X	X	46x*Y
REV	Reset TSTF if Bit K is Even	4.7		X	05x7040K
RNZ	Reset TSTF if A≠0	4.7			05004470
ROD	Reset TSTF if Bit K is Odd	4.7		X	05x0440K
RST	Reset TSTF	4.7			05004737
SBK	Set Bit K	4.7		X	05x4600K
SEL	Select Device D	*** 8.5 & 26.5		X	25x0D
SET	Set TSTF	4.7			05004637
SEV	Set TSTF if Bit K is Even	4.7		X	05x7050K
SKA	Subtract K from A	* 6.4		X	50x0K
SLA	Shift Left Arithmetic	4.8 - 8.0		X	45x0204K
SLL	Shift Left Logical	4.8 - 8.0		X	45x0200K
SNZ	Set TSTF if A is NON-ZERO	4.7			05004570
SOD	Set TSTF if Bit K is Odd	4.7		X	05x0450K
SPB	Save Place and Branch	3.2	X	X	33x*Y
SRA	Shift Right Arithmetic	4.7		X	05x1404K
SRC	Shift Right Circular	4.7		X	05x0404K
SRL	Shift Right Logical	4.7		X	05x0004K
SSA	Set Stall Alarm	2.2			25010000
STA	Store A	3.2	X	X	32x*Y
STI	Store Indirect	* 40.9	X	X	53x*Y
STM	Set Trapping Mode Flip-flop	2.2			25000001
STQ	Store Q	6.4	X	X	44x*Y
STX	Store Index	6.4	X	X	06x*Y
SUB	Subtract	3.2	X	X	31x*Y
TER	Test Even and Reset Bit K	4.7		X	05x4560K
TES	Test Even and Set Bit K	4.7		X	05x4660K
TEV	Test Bit K Even	4.7		X	05x7070K
TNM	Test Not Minus One	4.7			05070770
TNZ	Test A≠0	4.7			05004770
TOD	Test Bit K Add	4.7		X	05x0470K
TOR	Test Odd and Reset Bit K	4.7		X	05x4570K
TOS	Test Odd and Set Bit K	4.7		X	05x4670K
TSC	Test and Shift Circular	4.7		X	05x0464K
TXH	Test Index High or Equal	4.7		X	24x0 - K
TZC	Test Zero and Complement	4.7			05064670
TZE	Test A Zero	4.7			05004670
XEC	Execute	1.6	X	X	04x*Y
**TIM/TOM	Table I/O	*** 12.7 & 30.7			

* = Relative Addressing

* = Extended function or "quasi" instructions. Index address modification adds 1.6 μs to stated execution times.

** = Not an instruction, a wired sequence.

*** = Selected by $K_3 = 7$ for high speed and $K_3 \neq 7$ for low speed.

Notes: Where two times are listed for one I/O instruction the smaller figure is for the high-speed I/O channel of the GE/PAC 4020 computer.

Where two times are listed for floating point instructions, the first is for single word; the second, for double word. K may range up to 31_{10} (five bits) on shifts and up to 4095_{10} (14 bits) on constants. Where K is greater than 7, add it (in octal) to the indicated code. Example: TSC 13_8 would be 05x04653.

For timing, the "event" counted is the passage of one cycle on the a-c power line — 16.67 ms on a 60-Hz system.

When the DMT is used as a program loop counter, the interrupt system is not involved. Instead, the DMT resets the test flip-flop when the count goes from zero to minus one. Advantages of using the DMT with the index locations for this purpose include speed and the fact that the X locations are saved automatically in the event that the program is interrupted or over-written.

Subroutine Linkage

A subroutine consists of a series of instructions to perform a given function required several times by one program or by several programs.

Relevant instructions include save place and branch (SPB) for subroutine entry and load place and restore (LPR) for return to the calling program.

In addition to the contents of "P", these two instructions also save and restore the contents of four important control flip-flops, shown in Figure 3.

The SPB stores this information in index location one and inhibits interrupts for one succeeding instruction. That instruction — the first of the subroutine — should store X1 in any other memory location. Then the LPR can refer to that location in exiting from the subroutine.

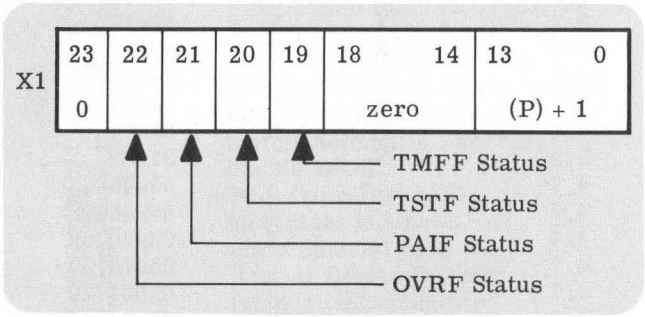


Figure 3
Storing, Reloading the Control Flip-lops

Logical Variables

Process control programs spend much of their time performing logical functions. The GE/PAC 4020 computer's capabilities include hardware to manipulate individual bits in a word (bit logic), count various configurations of ones and zeroes (a form of partial word logic) and perform four full-word logical instructions (AND, OR, Exclusive OR, and Complement). Many of these capabilities are carried into the GE/PAC Process FORTRAN language; all are reflected in PAL.

Thus, rather than wasting an entire word to store each logical variable, the GE/PAC 4020 computer can pack 24 into each word, with no additional running time or programming effort.

Operate on Memory

Inverse to memory operations are carried out by the operate on memory (OOM) quasi, which causes the memory location addressed by the OOM to act as the A register for the instruction immediately following the OOM. While this feature will not save running time, it will save memory and enhances compatibility between the GE/PAC 4020 computer and the earlier GE/PAC 4050, 4050-II and 4060 machines, which implement OOM as a wired instruction.

Execute

Operations involving double-indexing, indexing of otherwise non-indexable instructions, and execution of commands manufactured by a program are implemented in the GE/PAC 4020 computer by the execute (XEC) instruction. XEC fetches an instruction from the address given in its operand address field, executes it, then transfers control to the instruction following the XEC, not the instruction following the object instruction.

Automatic Program Interrupt (API)

This feature saves central processor time, permits faster response to critical external conditions, operates I/O devices and subsystems at full-rated speeds without special attention from the system's programs, and helps the software be certain that programs are run in the desired order of priority as time passes and system conditions change.

Each level of interrupt can recognize and retain either a momentary signal or a change-of-level signal. When the level is "permitted", program control will be transferred to a location unique for each level. What happens next depends on which instruction is stored at that location. The most frequently used response commands are:

Save Place and Branch (SPB). When a program is to run as a consequence of the interrupt, this instruction stores the P register and control flip-flop states of the running program and enters the response program (if it is always in core) or the real-time executive portion of RTOS (if the program may not be in core). It is the responsibility of the response program to save any registers it uses or disturbs and to reload them before returning to the interrupted program.

No Operation (NOP). This instruction is executed, but does nothing, after which control is returned to the interrupted program. Storing a NOP in its API response address is the way to inhibit an individual interrupt.

A Table Input to Memory (TIM) or Table Output from Memory (TOM) Control Word. To be described later in this manual, this is the computer's main I/O path to process subsystems and peripherals. It has a buffering capacity of 189 eight-bit characters and takes from the running program a total of 12.7 or 30.7 μs per word or character I/O operation, until the table becomes full or empty. Then the TIM/TOM hardware generates an "echo" interrupt, requiring registers to be stored and a driver program to be run to use the data or provide more.

Decrement Memory and Test (DMT). Described in the "Special Commands and Features" section of this manual, DMT provides a safe and efficient way to count events, real-time and elapsed real-time, and does not affect any of the programmable registers.

The total time a GE/PAC 4020 computer will require to respond to a "permitted" interrupt consists of the signal conditioning time constant required for noise suppression, approximately 0.5 μs for the API hardware itself to recognize an interrupt and generate an address for it, and the length of time until the program encounters and executes a wired, interruptible instruction.

Since program sequence or data might be lost if interrupts were permitted immediately after certain instructions (such as branches, bit-counting instructions, instructions which load or test the index locations, and instructions which permit or inhibit the API system itself), these instructions inhibit the API system long enough for the one following instructions to be executed, and are called "uninterruptible" instructions for this reason.

The API system is available in increments of eight levels from eight to 128 levels.

An optional mask register provides selective inhibiting or enabling of groups of four sequential levels. For a 128-level system, a 32-bit register is provided. It is loaded from the lowest-order 16 bits in the A register by load mask register commands (LMR and LMR2).

To prevent the possibility of a continuous loop of uninterruptible instructions effectively stalling the central processor, and to be sure interrupts are serviced in time, the computer optionally includes an API watchdog timer. The first of the two timers actually used to implement this function starts timing whenever a non-inhibitable interrupt is requested. If a permit automatic interrupt (PAI) instruction is not executed within one ms, program control is forced to core location 24_8, the beginning of a remedial program. The second timer performs a similar function for all interrupts, non-inhibitable and inhibitable, but uses a 30 ms period.

Implementing this useful option also requires the Quadritect memory protection option.

Figure 4 shows a typical set of API level assignments.

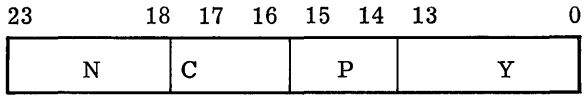
GE/PAC 4020 COMPUTER INPUT—OUTPUT

Direct Memory Access. The first of three types of I/O provisions handles such high data-rate devices as drum and disc bulk memories, other computers or data acquisition systems, and GE high-speed peripherals.

This I/O method operates in a true "cycle-stealing" mode, requiring just one core cycle (1.6 μs) to transfer a 24-bit word between the core and an external controller. The GE/PAC 4020 computer can have up to three direct access channels and in the case of high-speed peripherals, can drive more up to eight controllers with one of the channels, permitting a large number of very high-performance peripherals.

TIM/TOM. TIM and TOM stand for Table Input to Memory and Table Output from Memory. In this mode, portions of the AU not used between instructions are employed by the special-purpose TIM/TOM hardware to act as a controller between core memory, process I/O subsystems, and both low-speed and moderate-speed peripherals. The result combines economy and high speed; since no programmable registers are disturbed, it is not necessary to store and reload them. While TIM/TOM is somewhat slower than true cycle-stealing, it is more than adequate for the service and far faster than any other known I/O approach.

This feature also makes very efficient use of memory as well as CPU time, since it can pack and unpack one, two, three or four characters per 24-bit word, depending on the code required by the device or subsystem being driven. The table in memory can be up to 63 words long. TIM/TOM is not an instruction, but a hardware function activated by an interrupt. The interrupt response location holds a TIM/TOM control word which is modified as the operation proceeds. The control word contains a starting address, word count, and character packing instructions, as below:



N = 1's complement of the number of words to be manipulated

C = P, initially, and is incremented as each character is transferred

P = Packing Mode

00 = 4 char./word (6 bits/char.)
01 = 3 char./word (8 bits/char.)
10 = 2 char./word (12 bits/char.)
11 = 1 char./word (24 bits/char.)

Y = Starting Address minus 1

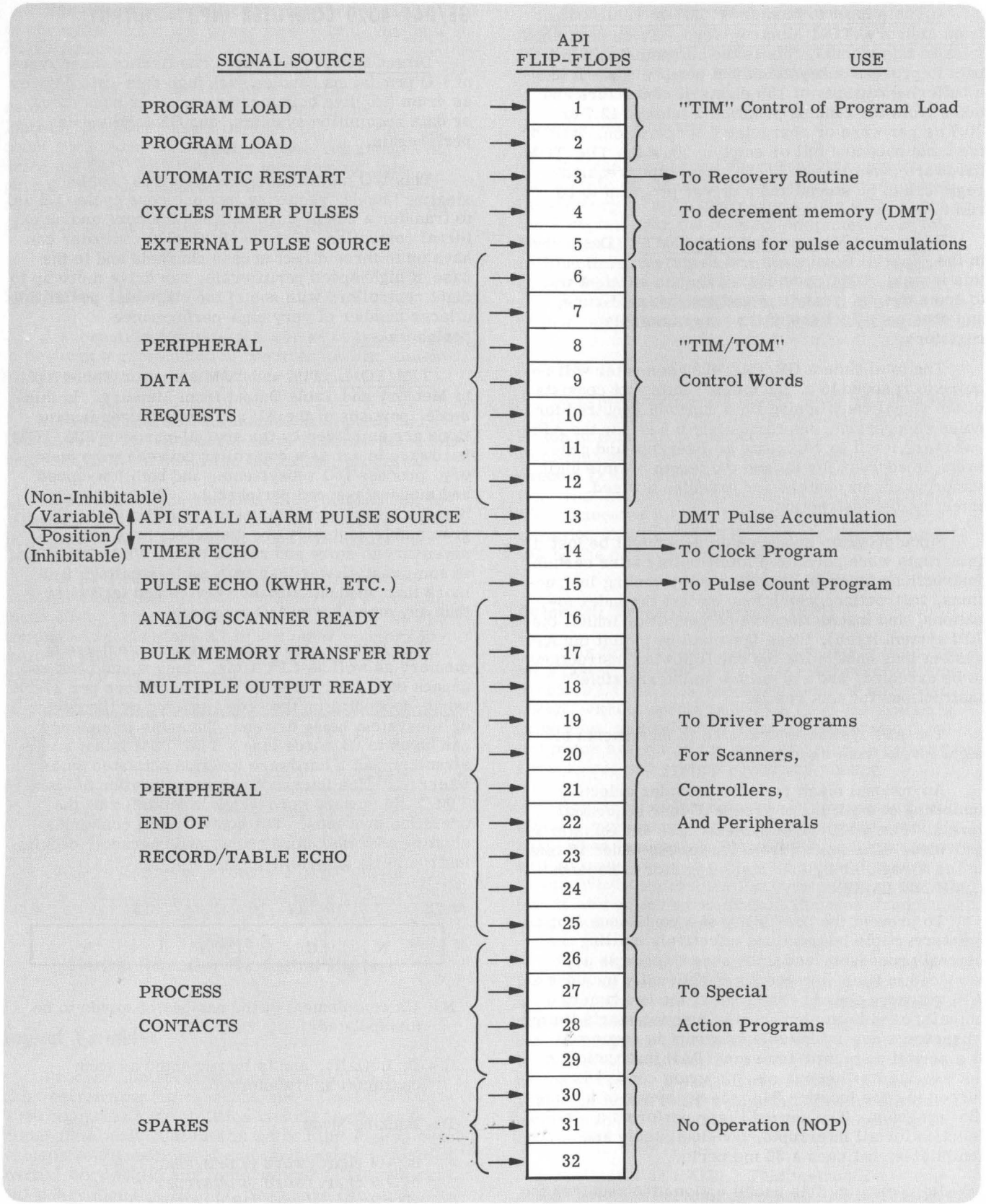


Figure 4
Typical Allocation of Inputs to API Module

Data flow for the TIM/TOM function is via the adder and B register, with the accumulator or A register always left undisturbed. The address is 14 bits, allowing data to be read into or written from the first 16K of core.

The word count (N) permits up to 63 words to be read or written in a block. This is equal to 252, 189, 126, or 63 characters depending on the packing mode used. The C and N fields are adjacent so a carry-out of the C field will cause the N field to increment, automatically counting both characters and words.

The TIM (input) function builds a word in memory character by character from an input device, using the following cycle:

1. Contents of the memory location go to the B register.
2. The B register is circularly shifted left by the number of bits in one character position (6, 8, 12 bits). It is not shifted if P = 11 (1 character/word.
3. A character is OR'ed into the least significant bits of the B register from the input device.
4. The contents of the B register are transferred back to memory.

This cycle is repeated for each character in the word. The B register is cleared between steps 1 and 2 before the first character is transferred. It is not cleared for the remaining characters in the word. When more than one character is packed into a word (P = 2, 3, or 4), the first character is in the most significant bits of the word and the last character is in the least significant bits. When only one character is in the word and it is less than 24 bits, it is right-justified in the word (positioned in the least significant bits).

When the N-field reaches 77_8, a second and separate (echo signal) interrupt occurs calling for program intervention. Any further attempt to exercise the TIM/TOM function on the same channel without updating the control word will result in a no operation.

The TOM (output) function operates similarly.

The TIM and TOM functions are initiated by an operate (OPR) instruction referencing the appropriate device or subsystem number. The A register must contain a special "medium enable" code at this time. Thereafter, A is not involved in any way. These functions are stopped by a "data termination code, handled the same way.

Using the A Register. The GE/PAC 4020 computer also has a communications channel connected with its A register, used mainly to drive the digital input scanner, which reads the states of contact closures in groups of 24. This subsystem is so fast that no waiting — and hence no buffers or interrupts — are necessary to use it. The contact sensing programs are generally written to read a group (with an IN command), process its information and store it if necessary.

Since the TIM or TOM operation modifies the control word, the driver program must re-initialize it.

Depending on where a subsystem's controller or a device's buffer is located physically with regard to the central processor, I/O operations will require either 8.5 (IN or OUT command) or 12.7 s. TIM/TOM functions are 26.5 or 30.7 s. Most process I/O subsystems require the extra time.

This mode is also useful when dealing with special I/O situations requiring such functions as selecting a device, activating it, operating it, or aborting its operation (also usable with direct-access controllers). GEN II commands perform these functions.

The Input/Output Buffer. The input/output buffer controls the operations of peripheral devices, allowing the central processor to continue other operations. High throughput rates are achieved by individual device character buffering and interrupts.

The basic characteristics of the I/O buffer are:

Offers a maximum of 16 channels, of which 7 may be used for input.

Operates peripherals in a record-oriented mode, for more accuracy and longer life.

Accommodates the American Standard Code for Information Interchange (ASCII).

Permits concurrent operation of all attached devices at their rated speeds through individual one-character buffers for each device.

The I/O buffer is the connecting link between the central processor and input/output devices: such as tape readers, tape punches, card readers, card punches, teletypewriters, output typewriters, I/O typewriters, line printers (300 LPM), and the Data-Edit Display (Local operation up to 1200 bps.)

Data-Edit Display (Local operation up to 1200 bps)

CHARACTER	CARD CODE	TELE-TYPE-WRITER	MED-SPEED LINE PRINTER	LONG CARRIAGE TYPER	SELECTRIC	HI-SPEED PRINTER	CHARACTER
A	12-1	X	X	X	X	X	A
B	12-2	X	X	X	X	X	B
C	12-3	X	X	X	X	X	C
D	12-4	X	X	X	X	X	D
E	12-5	X	X	X	X	X	E
F	12-6	X	X	X	X	X	F
G	12-7	X	X	X	X	X	G
H	12-8	X	X	X	X	X	H
I	12-9	X	X	X	X	X	I
J	11-1	X	X	X	X	X	J
K	11-2	X	X	X	X	X	K
L	11-3	X	X	X	X	X	L
M	11-4	X	X	X	X	X	M
N	11-5	X	X	X	X	X	N
O	11-6	X	X	X	X	X	O
P	11-7	X	X	X	X	X	P
Q	11-8	X	X	X	X	X	Q
R	11-9	X	X	X	X	X	R
S	0-2	X	X	X	X	X	S
T	0-3	X	X	X	X	X	T
U	0-4	X	X	X	X	X	U
V	0-5	X	X	X	X	X	V
W	0-6	X	X	X	X	X	W
X	0-7	X	X	X	X	X	X
Y	0-8	X	X	X	X	X	Y
Z	0-9	X	X	X	X	X	Z
0	0	X	X	X	X	X	0
1	1	X	X	X	X	X	1
2	2	X	X	X	X	X	2
3	3	X	X	X	X	X	3
4	4	X	X	X	X	X	4
5	5	X	X	X	X	X	5
6	6	X	X	X	X	X	6
7	7	X	X	X	X	X	7
8	8	X	X	X	X	X	8
9	9	X	X	X	X	X	9
Space		X	X	X	X	X	Space
.	12-3-8	X	X	X	X	X	.
,	0-3-8	X	X	X	X	X	,
+	12	X	X	X	X	X	+
-	11	X	X	X	X	X	-
*	11-4-8	X	X	X	X	X	*
/	0-1	X	X	X	X	X	/
=	3-8	X	X	X	X	X	=
(	0-4-8	X	X	X	X	X	(
)	12-4-8	X	X	X	X	X	)
$	11-3-8	X	X	X	X	X	$
"	4-8α	X	X	X	X		"
'		X	X		X		'
#		X	X		X	X	#
@	4-8α	X	X		X	X	@
&		X	X		X		&
%		X	X		X	X	%
?		X	X		X		?
!		X	X		X		!
_			X			X	_
>		X	X		X		>
<		X	X		X		<
[			X		X		[
]			X		X		]
:		X	X		X		:
;		X	X		X		;
\			X		X		\
↑		X	X		X		↑
←		X	X		X		←
Carriage ret		X		X	X		Carriage ret
Tab		X		X	X		Tab
Stop							Stop
Punch On							Punch On
Punch Off							Punch Off
Print Red				X	X		Print Red
Print Black				X	X		Print Black
Delete							Delete
WRU		X	Who are you?				
Tape		X	Tape On/Off				
Line Feed		X					
X Off		X	Reader Off				
EOT		X	End of Transmission				
RU		X	Are you?				
VT		X	Vertical Tab				
FORM		X	Form Feed				
RUBOUT		X	Cancel Tape Char				
RPT		X	Repeat				

α - on keyboard and card substitutes for "
character available = X

GE/PAC Peripheral Character Sets

Operation

Peripheral inputs and outputs are accomplished by TIM and TOM functions. The information flows by character between the arithmetic unit and the buffer. The data will consist of 7 to 12 bits, depending on the device to be used. All devices connected to the I/O buffer operate in a record format or are programmed in a record format. For example, the card reader always reads at least one entire card (unit record), and the paper tape reader continues reading until the "end of record" character is detected or until the TIM table fills up. The overall I/O capability of the computer is 50-60,000 characters per second.

Normally each channel will function using two interrupts, one to indicate "data ready", and the other "end of record" or "table full (or empty)".

Even parity is checked or added by the peripheral buffer for all devices except card readers, card punches, and typewriters, which do not use parity.

The size of the buffer register depends on the device. The card readers and card punches use 12-bit registers. All other devices have 8-bit registers.

The bits are transmitted in parallel from the arithmetic unit to the I/O buffer, and from the I/O buffer to the device, except for teletypewriters and the Data-Edit, which are bit serial. Also for the teletypewriter, the I/O buffer generates one bit to indicate a start of a character and two bits to indicate the end of a character.

Test lines enable the program to determine the status of any given channel. A "channel busy" line tells the program when the addressed channel is in use. A "data exchange ready" line tells the program when the addressed device wants data or when it has data ready to input. An error line informs the program of an error condition in the addressed device.

Computer-to-computer communication between I/O buffers is possible. An output control module and an input control module provide a 12-bit-parallel, medium-speed, computer-to-computer communication link. Communications are carried out via the TIM/TOM mode at transfer rates up to approximately 50-60,000 characters per second.

The I/O buffer has been designed to handle character-oriented I/O devices which send and receive data coded in ASCII. Devices which do not respond to ASCII may be used, but program translation is required.

Programming all I/O functions on the GE/PAC 4020 computer (except the DIC) can be done most efficiently and easily through calling sequences to RTOS. The programmer must specify only where to find the data and format descriptive words, which device is desired, and what to do if that device is bad or out of service. RTOS then handles all the I/O mechanics including stacking requests from one program or several for a particular device, recognizing and remembering peripheral failure and out of service conditions, performing code conversions, and using working alternative devices as required.

RTOS thus maximizes peripheral utilization, minimizes the possibility of loss of data, and eliminates the possibilities of peripheral conflicts and system "hang ups" due to failed devices.

Program Load. The Program Load permits an operator to "bootstrap" a loader subroutine into GE/PAC core memory from paper tape or cards, using the TIM feature.

Program load uses the two highest priority interrupt locations 000 and 001 (program interrupt locations 200_8 and 201_8) corresponding to a "primary" input device and a "secondary" input device. GE/PAC bootstrap input devices are:

Teletype ASR35

100 cps paper-tape reader

200 cps paper-tape reader

300 cpm card reader

The detailed procedure is:

Place the bootstrap card (tape) into the reader and ready so that: the card is in "load position"; or the tape is positioned so that a leader frame is under the read heads.

Place the computer in manual.

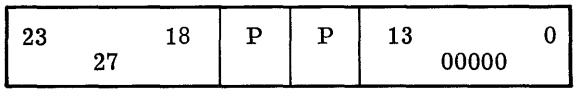
Push the program load button

Initialize the computer by pushing the on button. (This sets P = 0 and clears interrupts.)

Latch save P switch.

Store a "LDA 0" instruction in location 0.

Store a TIM control word in the chosen readers' API location (200_8 or 201_8).



Where P = 2 if cards

P = 0 if paper tape

Load the instruction "OPR Reader" (2502110D) into the B register.

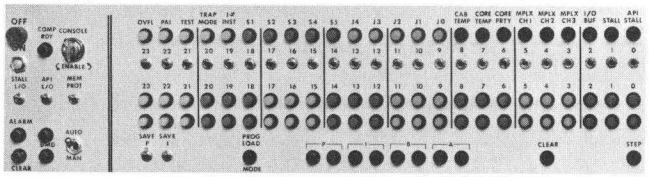
Load the medium enable code, 00000021, into the A register.

Place the computer in auto. (The card or tape will be read into locations 01_8 through 50_8).

Wait until the card (tape) is fully read, (i.e., the input device stops) then unlatch the Save P switch. (The computer will execute the program read from the card (tape).) Location 1 is the first instruction executed.

PROGRAMMING AND MAINTENANCE CONSOLE

The programming and maintenance console as shown below is an integral part of the central processor or, as an option, can be a plug-in portable unit when several central processors are used but only one console is required. This console allows the programmer and product service engineer to communicate with the computer in machine language and to step through programs.



Register Display P, I, B, or A

The 24 register displays are pushbutton momentary-type switch lights. These 24 switches operate in conjunction with the A, B, I or P register select switches. If A or B is selected, depressing any one of the 24 sets a one bit into that position of the register selected. These switches are enabled in the manual mode only. The entire register is cleared by depressing the "clear" switch. Individual reset is not provided.

Register Select P, I, B, A

The "P, I, B, and A" are momentary-type switch lights. Depressing one of these switches causes the respective light to glow and the associated register contents to be displayed in the 24 register display lights. Depressing any one of these four switches de-selects the others. These switches are enabled in the auto or manual modes.

Register Console Switches (RCS)

These 24 console switches are latching-type switches that operate in conjunction with the "read console switch" instruction.

Save—I

of the I-register cannot be changed. When unlocked off, the I-register functions normally. The Save-I function is enabled only in the auto or manual modes.

Save—P

The save-P-register switch is a latching type. When this switch is in the on position, the contents of the P register cannot be changed. The Save-P function is enabled only in the auto or manual modes.

Stall I/O

This switch functions only in the auto mode and disables or enables all stall functions in the system.

Step

The step button is a momentary pushbutton which steps the computer one instruction per depression. This function is enabled only in the manual mode. The step switch is disabled until the console is switched to Manual.

Console OFF (lockout) (Toggle Switch)

In the Console off mode all console functions except power off, RCS and demand are disabled.

Optional Console OFF (Toggle Switch)

The console off switch used on an optional console locks out all functions provided on the optional console. It is mounted near the parity lockout switch.

API Stall

The API stall indicator comes on when the API watchdog timer is allowed to run out. It is turned off by restarting the API watchdog timer.

CH1, CH2, CH3

The bulk storage indicators come on when the associated device produces an error condition. Example: drum, disc, etc.

Core Temp

The core temperature indicator comes on when the core stack temperature is not within the allowable operating range. Should a parity error be detected during this time, a normal shutdown sequence will occur.

Alarm/Clear

All error conditions displayed on the optional console are "OR'ed" in the arithmetic unit and a single line is sent into this error indicator, a backlighted pushbutton. Therefore, if the optional console is included in a system and one of the error indicators is turned ON, this error indicator is turned on too. The indicator and error condition, if applicable, can be cleared by depressing the switch.

J4 ◄——► J0

The contents of the J-counter are continuously displayed on the five J-counter indicators.

Memory Protect

The memory protect indicator comes on when a memory protect violation is encountered. The next instruction is executed from address 20_8. This indicator may be cleared when an SPB is executed that is in locations 20_8 or 24_8.

I = Instr

The I≠ INSTR indicator comes on at the completion of the multiply or divide or TIM/TOM operation. It is cleared during the execution of the next instruction. This indicator, when on, also implies that I-register (which normally contains the next instruction) does not contain the next instruction.

Ovfl

The overflow indicator comes on when an arithmetic overflow occurs. The OVFL is cleared by executing the JNO instruction, or the LPR if OVFL had been stored in its off condition.

Pai

The permit automatic interrupt indicator comes on when the PAI instruction is executed and indicates that the "inhibitable" interrupts are allowed.

Per Buf

The peripheral buffer indicator comes on when either a parity error or a deadman error has occurred on one of the devices attached to the peripheral buffer. It is cleared by depressing the alarm/clear button.

Cab Temp

The cabinet temperature indicator comes on when the cabinet temperature reaches its first preset limit. A shut down sequence occurs when: (1) The cabinet temperature reaches the second preset limit; (2) Either limit is reached and a stall alarm occurs. An external signal is available for system use.

Core Prty

The memory parity indicator comes on when a memory parity error occurs. Depressing the alarm/clear button turns off the indicator.

Seq. State #1, 2, 3, 4, 5

The five sequence states of the computer are displayed via the sequence state indicators. Sequence state 1 is displayed when the computer is halted and everything is normal.

Stall

The stall indicator comes on when the stall alarm timer is allowed to time out. It is turned off by depressing the alarm/clear button.

Test (TSTF)

The test indicator comes on when the Test Flip-Flop is set by instructions such as GEN 1, LPR or TXH. The test indicator is cleared by program depending on the instruction being executed, similar to its setting.

CONSOLE SWITCHES

API L/O

The API lockout switch is a latching-type. In the on position, it disables all interrupts from the API module. This function is enabled only in the auto and manual modes.

Auto/Man

The auto/manual switch is a latching-type. When locked in the on position the light glows and the computer is in the automatic mode. When unlocked, the computer is in the manual mode. This switch is disabled in the console off mode. When switched from manual to auto, AU timing starts.

Clear

The Clear pushbutton is a momentary zeroes type. When in the manual mode, Clear the entire register selected by the A or B switches. Clear is disabled in the auto mode.

DMD

The demand pushbutton is a momentary type. When it is depressed and released the demand flip-flop is set and the DMD light glows. When the JND command is executed the demand flip-flow is cleared and the indicator light is turned off.

Mem Prot L/O

The memory protect lockout is a latching-type switch. When in the on position it disables the memory protect function. This switch function is enabled only in the automatic or manual modes.

Off Switch

The off pushbutton is a momentary-type switch. When depressed, it turns off the power to the computer system. Provision is included on the console to make it difficult to turn off power accidentally.

ON/INT

The power on initialize momentary pushbutton maintains the power on condition. In addition, the pushbutton, when depressed, performs the initialize function in the manual mode. The computer is initialized when the power is turned on or is already on, and the power on switch is depressed to close the initialize contact.

Program Load

The program load pushbutton is a momentary-type switch. Program load is active in both the manual and auto modes.

Prty Stop

The parity stop toggle switch, when in the on or stop position, halts the computer upon completing an instruction in which a memory parity error is detected. The switch function is enabled at all times regardless of the setting of the auto man switch. The parity error must be cleared before the computer can be made to continue operation. This switch is mounted inside the cabinet.

DEVICE	MODE		
	AUTO	MAN	OFF
API Stall	I	I	I
CH1, CH2, CH3	I	I	I
Core Temp	I	I	I
Error	I/O	I/O	
J-Counter	I	I	I
Mem. Prot.	I	I	I
I ≠ Instr.	I	I	I
OVFL	I	I	I
PAI	I	I	I
PER. BUF.	I	I	I
CORE PRTY.	I	I	I
Seq. State	I	I	I
Stall	I	I	I
Trap'g Mode	I	I	I
API-L/O	O	O	
Auto	O	O	
Clear		O	I/O
DMD	I/O	I/O	
Mem. Prot. L/O	I/O	I/O	
Off	O	O	O
ON/INT	I	I/O	I
Prog. Load	O	O	
Prty. Stop	O	O	O
Reg. Display/Enter		I/O	
Reg. Select (P, I, B, A)		I/O	
Reg. (RCS) Console Switches	O	O	O
Save-I	O	O	
Save-P	O	O	
Stall L/O	O		
Step		O	

I = Indicate, O = Operate

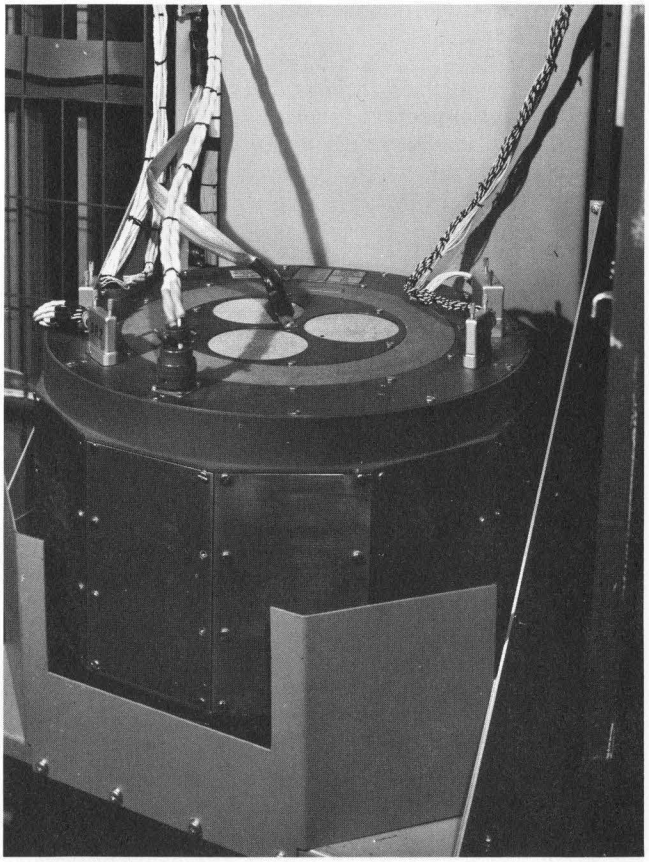
Modes in which Devices on Console Operate or Indicate

BULK MEMORY SUBSYSTEMS

DRUM

General Characteristics

The magnetic drum auxiliary memory provides non-destructive bulk storage. The drum capacity varies from 16,384 words to 262,144 words in increments of 8,192 words. The drum is composed of tracks, each containing 512 words. Each word consisting of 24 information bits, one parity bit and a three bit interword gap. The drum module contains the necessary read-write amplifiers, control logic and heads to enable reading and writing on the continuously rotating magnetic surface.



Checking and Protection

An odd parity bit is written with each word as it is transferred to the drum. Parity check is made on each word as it is transferred to or from the drum; a parity error signal is set if a parity error is detected. Parity is received from core and checked by hardware.

The write protect pinboard located in the drum cabinet provides selective drum memory protection in blocks of 4096 words. Figure 5 indicates details.

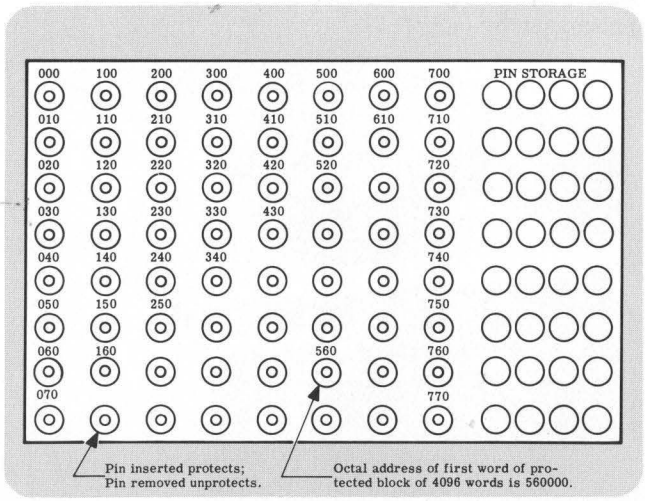


Figure 5
Drum Write Protect Pinboard

Overheat protection is provided by a single-throw double-pole temperature sensing switch which is incorporated in the drum cabinet. One contact is available to control a remote overtemperature indicating device and the other will trip the shutdown function in the computer power sequencer.

Control Word Formats

The location of the program or data on the drum is given by a block of three consecutive drum control words which are shown in Figure 6. These control words are located in core and contain the starting drum address, number of words to transfer (length of program or data) and starting core address. Bit 23 of the first drum control word is either set or reset depending on the direction of transfer.

To activate a drum transfer, place the location Y of the first drum control word in core memory location zero. Then call for an output to drum with an OUT instruction. The drum controller will perform a drum operation as specified by the control words.

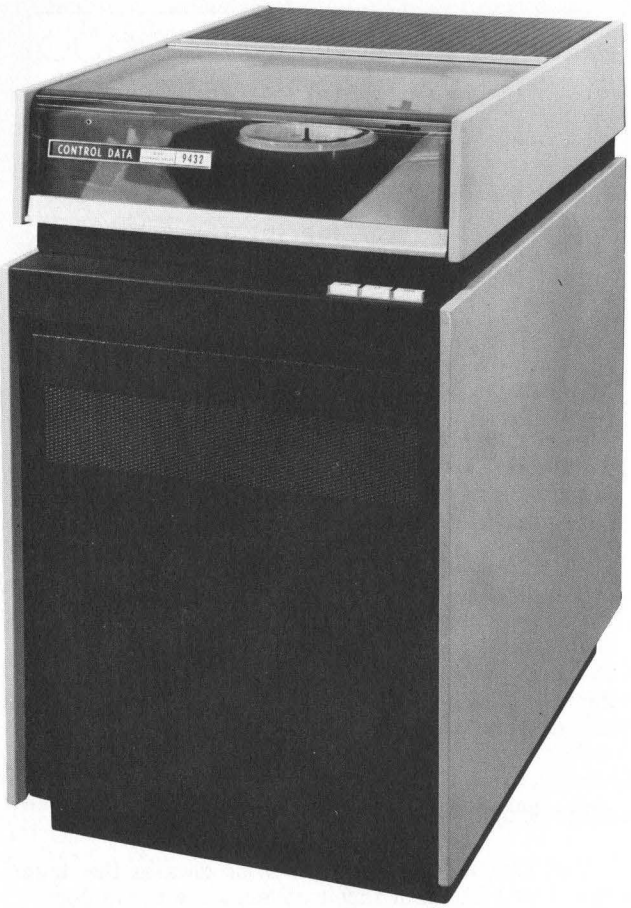
The time required to effect the transfer includes drum access time plus actual transfer time. For 60 Hz operation:

Access time variable -0 to 16.67 ms, average 8.3 ms

Transfer of 256 words per revolution

Transfer time 0.0650 ms per word

One to 16,384 words can be transferred by one drum transfer instruction. Each word takes one core memory cycle, or 1.6 μs of central processor time during drum transfer, slowing the central processor by only 2.5%.



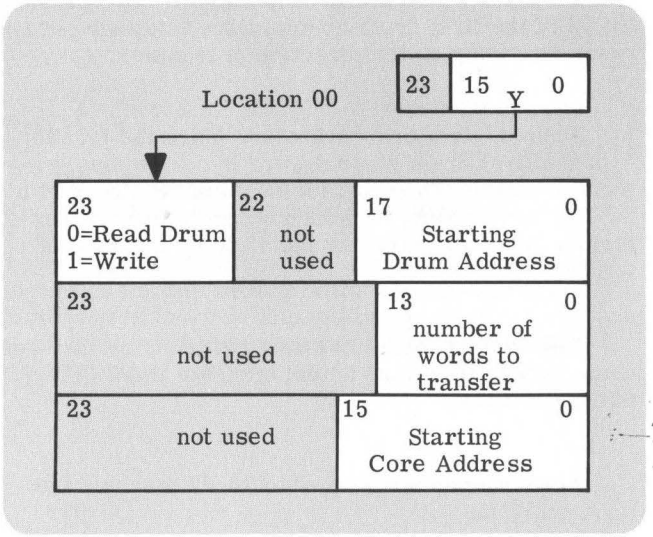


Figure 6
Drum Control Words

DISC

General Characteristics

The disc auxiliary memory provides non-destructive bulk storage. Disc memory consists of removable disc units and a controller which contains the necessary hardware to communicate directly to core memory. Each word consists of 24 information bits and one parity bit.

From one to four discs may be connected to a single controller.

Checking and Protection

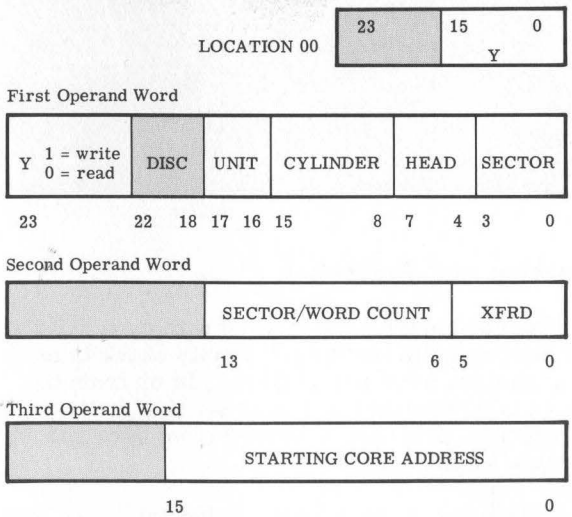
Odd parity is checked by hardware during disc read and write operations. Error indications are provided for illegal addressing, positioning error, and limit error.

Write protection is provided for each disc drive. When the write-protect function is activated, no program can inadvertently write on that disc pack.

Control Word Formats

To activate a disc transfer, first place the location Y of the first disc control word in core memory location zero. Then call for an output to disc utilizing an OUT instruction. This will cause the disc controller to fetch the contents Y from core memory location zero. The disc controller will perform a disc operation as specified by these control words.

From 1 to 16K words can be transferred from or to the disc for each programmed access. Transfer is direct to core memory at a rate of 1.2 million data bits per second. The central processor operates at 92% of rated speed while transfer is taking place.



Disc Control Words

PROGRAMMER INPUT-OUTPUT DEVICES

This section contains the specifications of the devices used for the basic programming functions of reading, printing, punching, input-output communications with the Real-Time Operating System, and interface with high-performance peripherals through the common peripheral interface.

READING DEVICES

Unless otherwise noted, all devices are suitable for reliable and accurate operation and long life in industrial environments.

GE/PAC 4000 Paper-Tape Reader

Speed

100 characters per second or 200 characters per second

Operational Modes

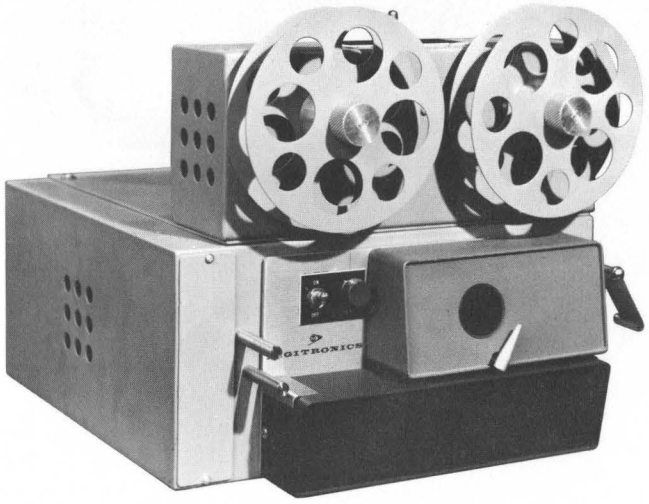
10 characters per inch. Demand read push-button. Operation up to 50 feet is standard and up to 2000 feet is optional. 100 ips rewind.

Checking features

Media presence check, tight tape indication, off-line check, parity check.

Spoolers

Both a supply reel and a take-up spooler are provided.



Simultaneous operation

The paper-tape reader can operate at full speed while other peripherals and/or the central processor are operating.

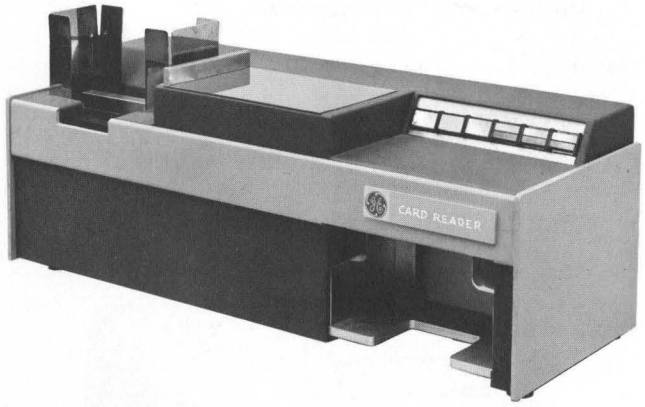
Physical specifications

14 inches wide
13 inches high
19 inches deep
Weight 43 lbs.

GE/PAC 4000 Card Reader

Speed

100, 200 or 300 cards per minute



Operation modes

80-column, 12-row cards

Cards may be read in Hollerith or binary modes

Operation up to 50 feet is standard and up to 2000 feet is optional

Operating features

Synchronized, optical reading mechanism assures accurate, reliable card reading.

Serial read, column-by-column, one card at a time or continuously under program control.

Checking features

Alert condition is signaled for input hopper empty, feed failure, card jam, stacker full, amplifier and photo cell operation.

Hopper Capacity

Input and output hopper -- Input hopper -- 500, Stacker - 750. Continuous loading and unloading.

Simultaneous operation

The card reader can operate at full speed while other peripherals and/or the processor are operating.

Environment

Temperature 65 to 85°F

Relative humidity 40 to 60% (cards limit)

Office environment

PRINTING DEVICES

Model 35 Teletyper

Type - RO

Receive-only (no keyboard)

Speed

10 characters per second

Type-carriage characteristics

Murray typeface

7.5 inch type line

6 lines per inch vertically

10 characters per inch

Optional automatic line feed and carriage return when end of line reached

Operation modes

Operation up to 50 feet standard and up to 2000 feet optional

Optional automatic answer back

Code

8-level ASCII (7 data, 1 even parity)

Paper-tape unit

Tape has 10 characters per inch

Model 33 Teletyper

Type RO

RO - Receive-Only (no keyboard)

Speed

10 characters per second

Type-carriage characteristics

Murray typeface

7.2 inch type line

6 lines per inch vertically

10 characters per inch

Optional automatic line feed and carriage return when end of line is reached

Operation modes

Operation up to 50 feet standard and up to 20 miles optional

Optional automatic answer back

Code

8-level ASCII (7 data, 1 even parity)

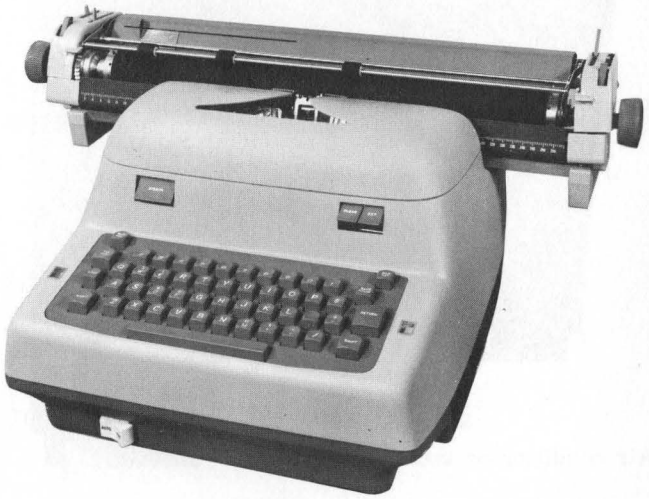
Paper-tape unit

Tape has 10 characters per inch

GE/PAC 4000 Output Typer

Speed

10 characters per second



Type style & size

Gothic

10 characters per inch (Micro-Gothic, 14, Optional)

6 lines per inch vertically

Operation modes

Operation up to 50 feet is standard and up to 2000 feet is optional.

Red-black ribbon feed is selectable under program control.

Pin feed platen standard. On-line and off-line operation.

Simultaneous operation

Typewriter can operate at full speed while other peripherals and/or the central processor are operating.

Physical Specifications

Carriage Length (inches)	Writing line -Pin Feed- (inches)	Width (inches)	Height (inches)	Depth (inches)	Weight (pounds)
12	8-7/8	28	14-1/4	17	67
20	16-27/32	44	14-1/4	17	71
30	26-1/2	64	14-1/4	17	84

The above carriage lengths are standard - others are optional.

GE/PAC 4000 High-Speed Output Typer

Speed

15.5 characters per second

Type style & size

Manifold 10 type

12 characters per inch

6 lines per inch vertically

Operation modes

Operation up to 50 feet is standard and up to 2000 feet is optional.

Red-black ribbon feed is selectable under program control.

On-line and off-line operation. Pin feed platen standard.

Simultaneous operation

Typewriter can operate at full speed while other peripherals and/or the central processor are operating.

Physical Specifications

21-3/4 inches wide

10 inches high

16 inches deep

weight 61 lbs.

Carriage - 11" or 15-1/2" with or without pin feed platen

Writing line 8" or 12-5/8" with pin feed platen

GE/PAC 4000 Printer

Speed

300 lines per minute alphanumeric

Line width

120 characters, 10 characters per inch

Vertical line spacing

6 lines per inch

Paper skipping

27-1/2 inches per second. After initiation of paper skip operation, printer may accept next print command.

Vertical format control

Control by command: single or top of page. Paper can be skipped to one of 8 lines defined on the Mylar* tape loop, or skipped to top of page.

Paper handling

Paper is contained under the printer. Completed forms stack onto a tray in back of the printer.

When removing paper, the print head is withdrawn from the platen by motor control.

*Reg. T.M. Dupont Co.

Paper specifications

Width: 3-inch minimum to 19-inch maximum. 22-inch fanfold forms. Prints original and up to 4 copies. Handles continuous tabulating card stock, single part.

Operation

Operation up to 50 feet is standard and up to 2000 feet is optional.

Checking features

Low paper, out of paper, hammer drive fuse failure

Buffer

120 character buffer holds print line data during printing.

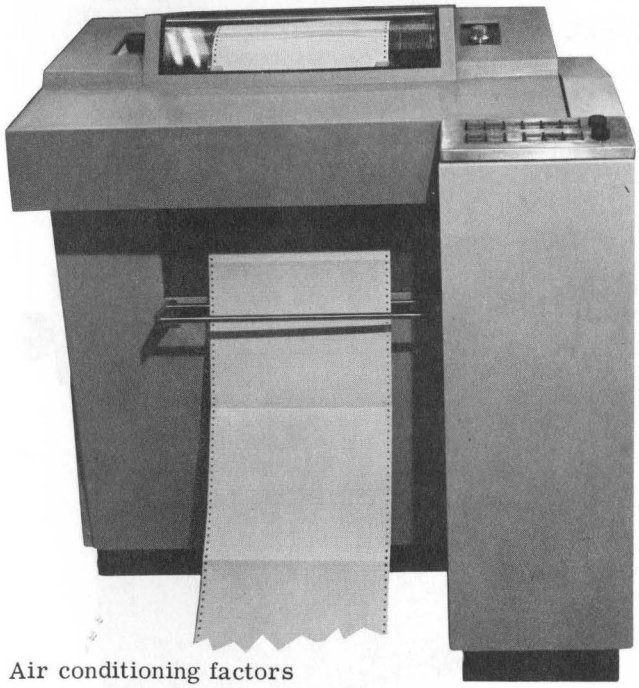
Physical specifications

48 inches high

33 inches deep

47 inches wide

Weight 700 lbs.



Air conditioning factors

4400 Btu/Hr. Cooling by non-removable fans circulating room air.

Environment

Temperature 65 to 85°F

Relative humidity 20 to 80%

Office environment

PUNCHING DEVICES

GE/PAC 4000 Paper Tape Punch

Speed

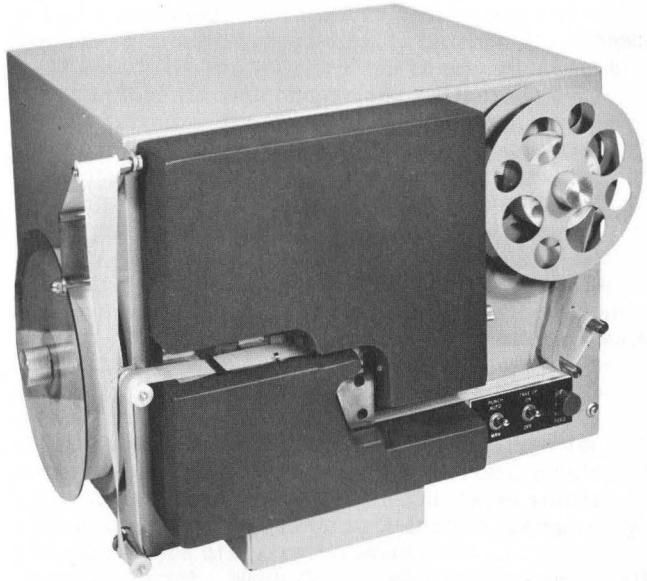
120 characters per second

Operation mode

8 channel, 1 inch wide paper or Mylar tape

10 characters per inch

Operation up to 50 feet is standard and up to 2000 feet is optional.



Simultaneous Operation

The paper-tape punch can operate at full speed while other peripherals and/or the central processor are operating.

Spoolers

Both a supply reel and a take-up spooler are provided.

Checking features

Media presence check

Parity check

Auto-off-manual control

Physical specifications

19 inches wide, 11 inches deep

13 inches high

Weight 50 lbs.

GE/PAC 4000 Card Punch

Speed

100 cards per minute

Operation modes

80-column, 12-row cards

Cards may be punched in Hollerith or binary modes. Operation up to 50 feet is standard and optionally up to 2000 feet.

Checking features

Alert condition is signaled when input hopper empty, output stacker full, chad box full, feed failure, or card jam.

Input/Output capacity

Input and output hopper - 800 cards. Continuous loading and unloading.

Simultaneous operation

The card punch can operate at full speed while other peripherals and/or the central processor are operating.

Physical specifications

48 inches high

33 inches deep

47 inches wide

Weight 700 lbs.

Air conditioning factors

4400 Btu/Hr. Cooling by non-removable fans circulating room air.

Environment

Temperature 65 to 85°F

Relative humidity 20 to 80%

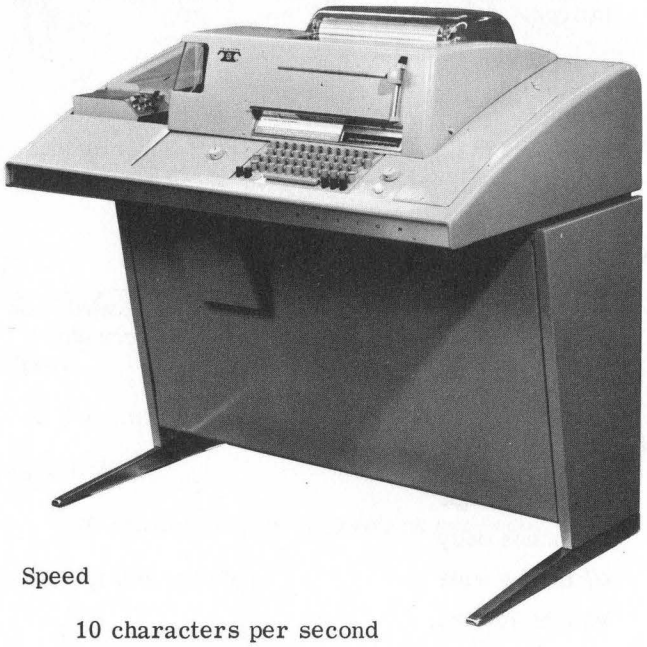
Office environment.

INPUT/OUTPUT TYPERS

Model 35 ASR Teletyper

Type - ASR

Automatic Send-Receive with paper tape punch and reader



Speed

10 characters per second

Type-carriage characteristics

Murray typeface

7.5-inch type line

6 lines per inch vertically

10 characters per inch (Optional * 12 characters per inch)

Optional * automatic line feed and carriage return when end of line reached

Operation modes

Full duplex (Optional ** half duplex)

4-row keyboard input

Operation up to 50 feet standard and up to 2000 feet optional

Character counter on keyboard of ASR model

Optional ** automatic answer back

Code

8-level ASCII (7 data, 1 even parity)

Paper-tape unit

Operates from keyboard or by computer

Tape has 10 characters per inch

Tape can be prepared off-line

GE/PAC 4000 I/O Typer

Speed

15.5 characters per second

Type style

Manifold 10 type

12 characters per inch

6 lines per inch vertically

Operation modes

Operation up to 50 feet is standard and up to 2000 feet is optional. Red-black ribbon feed is selectable under program control. Automatic alarm override for output. Multiple input typewriter capability. Input typing under RTOS program control.

Simultaneous operation

Typewriter can operate at full speed while other peripherals and/or the central processor are operating.

Physical specifications

21-3/4 inches wide

16 inches deep

*Options used when Teletypes used as I/O console for computer.
**Options not used when Teletype used as I/O console for computer.

Data-Edit Displays (CRT Operator's Stations)

The Data-Edit Display is an alpha-numeric input-output system which provides rapid communication with the GE/PAC 4020 computer from local or remote locations. It permits convenient single- or multiple-character editing in either the on-line or off-line mode. In case entire tables of data are to be replaced, the operator may call up the information in computer-stored format, go off line, enter the new data, go back on line and transmit the new data to the computer.

Used in the on-line mode, the Data-Edit Display allows: direct transmission, character-by-character, to the computer; receipt, storage, and presentation of responses. The Data-Edit Display consists of a controller, one or more memories, and one or more TV-type display terminals. Up to eight terminals per memory can communicate with the computer through the display controller. The display terminal consists of a television display screen and a keyboard. Each terminal may communicate with the computer through the controller by means of the keyboard. Keyboard entries are converted and stored in the memory of the controller. The coded characters in the memory are repetitively converted to TV video and, along with synchronized signals, are transmitted to the display screen. Selected portions of the stored information are transmitted on command to the computer either by direct connection or by the use of standard digital data sets. A variety of data line communication options is available, providing a range of data rates to fit various applications. The presentation on the display terminal is composed of up to 1196 characters and symbols, stored in the memory. The characters are arrayed in up to 26 lines of 46 characters each. With the use of special symbols, both horizontal and vertical lines can be generated on the displays.

The operator enters data by typing on the keyboard as an office typewriter. The characters and symbols are instantaneously displayed as they are typed. A special entry marker appears on the display to indicate the location of the next character to be entered. The marker automatically indexes with each character entry or may be manually spaced forward or backward, and up or down. It may be reset to the first character position on the page or textual line. In addition to providing repetitive character entry capability, the "repeat" key allows a continuous scanning movement of the marker. Changes or corrections are made by relocating the marker to the erroneous character and typing the correct one.

A "tab" key allows the operator to quickly and efficiently enter information into a manually composed or computer-stored format. Depressing the "tab" key causes the entry market to scan the display face until it finds a vertical line, where it stops. These vertical lines, which serve as tab-stop markers, can be positioned anywhere on the display surface by the operator or the computer. A "blink" feature permits emergency status or significant information to be emphasized. A single control operation erases the entire display.

The operator completes the composing, verifying, and correcting of the entry with the system off-line. When satisfied that the information is correct, the operator returns to the on-line mode, locates the market at the first character to be transmitted and depresses the transmit key. Successive characters are transmitted until the "end" symbol is encountered.

Responses from the computer are stored in the memory of the controller and immediately appear on the display.

Monolithic integrated circuits are used for the electronics. The American Standard Code for Information Interchange (ASCII) is the character code, and is transmitted bit serial at rates varying from 110 to 2400 bps, depending on the communication channel and controller options used.

When used in conjunction with a teletypewriter, the Data-Edit will produce hard copy of data displayed on the screen.

Closed-circuit TV and computer-produced data may be mixed on the same screen. The output signals from the camera are displayed on the same 525-line-per-inch TV screen used to display computer-produced, real-time data. Installing a signal mixer allows a choice of viewing closed-circuit TV only, a combination of data and closed-circuit TV, or process data alone.

The Data-Edit controller, if located near the computer, may be operated through the peripheral buffer; if remote, through data-sets over voice-grade channels.

The Data-Edit has two, three, or four memories per controller, and transmits in half-duplex or full-duplex mode at 100 or 1200 bps. Synchronous transmissions at 2000 or 2400 bps are also possible.

COMMON PERIPHERAL CONTROLLER

The common peripheral controller is designed to permit a GE/PAC computer to communicate with the following GE peripherals:

High-speed line printer	900/1200 lpm, 136 char. per line, buffered
High-speed card reader	900 cpm either binary or Hollerith
High-speed card punch	300 cpm either binary or Hollerith
Magnetic tape subsystem	Transfer rates of 7,500-120,000 char. per sec.
Disc storage subsystem	Capacities of 5,898,240 to 94.36 million characters. Transfer rate of 41,700 or 83,400 char. per second

Each common peripheral controller is expandable from one to four channels, where each channel interfaces to one of the above-listed subsystems. A program controlled switch allows the computer to switch from one channel to another. Therefore, only one channel may be in operation at any given time. Simultaneous operation may be achieved by using two or more common peripheral controllers. Up to eight common peripheral controllers may share one direct memory channel.

Features

The common peripheral controller checks for "odd ones" parity on all characters coming from the peripheral subsystems and will generate parity on all character transmissions to the peripheral subsystems. This is done by hardware in the common peripheral controller.

All input subsystems respond to a special signal called the program load signal. When a common peripheral subsystem is in the "ready" state and it receives this signal, it will respond by transmitting one record to the common peripheral controller.

Operation

The common peripheral controller utilizes four control words in memory. These words are shown in Figure 7. The pointer word is at a dedicated core location between 31_8 and 37_8. This address word gives the location Y of the first of the three control words.

The common peripheral controller contains the control, sequencing, buffering, and storage elements required to perform core memory to device storage data transfers and vica versa. An OUT instruction transfers the pointer word to the controller. After fetching the control words, the common peripheral controller transmits the proper commands to the peripheral. If data transfer is required, the unit initiates the data transfer sequence, controls the data word fetching from (or storage to) core memory, controls the data transmission, and terminates the operation when the designated number of words have been transferred. When terminating an operation the common peripheral controller stores 12 bits of status information into the pointer word location, and generates a ready signal interrupt to the central processor to request more data or a new instruction.

The common peripheral controllers also respond to the ACT (activate interrupt) and the ABT (abort) instructions, the latter to accomplish premature termination.

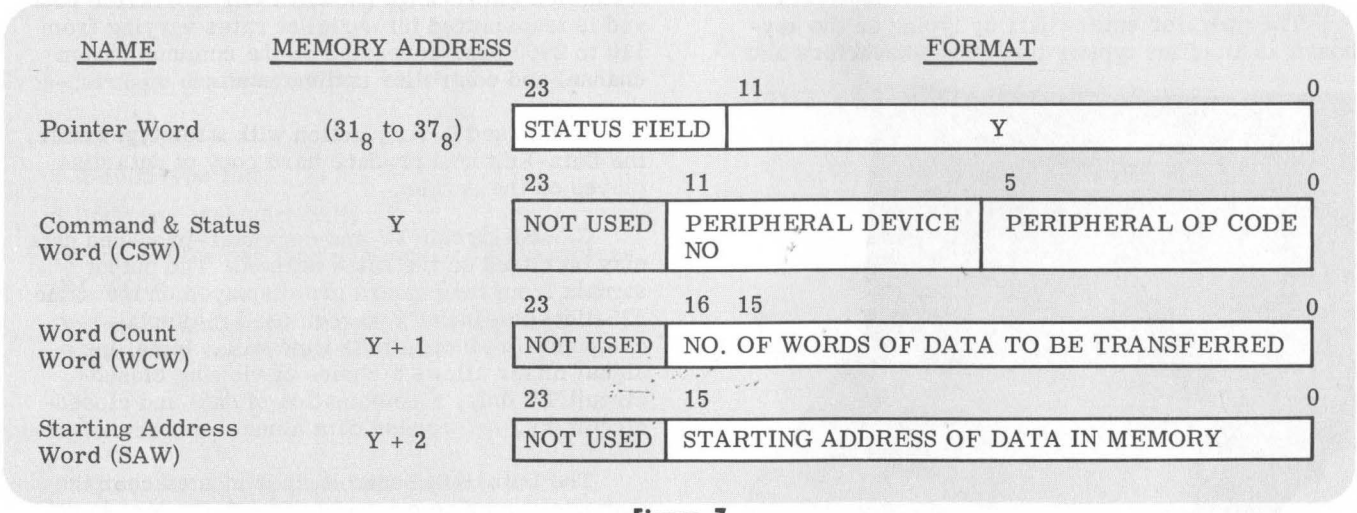


Figure 7
Common Peripheral Control Words

PROCESS INPUT-OUTPUT SUBSYSTEMS

ANALOG INPUT SCANNERS

Relay

The analog input scanner (AIS) accepts analog signals representing process variables and provides the computer with a digital representation of them. A useful concept is to think of the scanner as an automated, high-quality, high-speed digital voltmeter.

The AIS receives instructions from the central processor on which analog point to read, which gain and mode of operation to use. The scanner conditions the analog signal, selects the point by switching, amplifies the signal and converts the signal to a binary number. Figure 8 illustrates the configurations and major components of a typical system.

The basic analog scanner cycle requires 20 milliseconds, which includes relay switching time, amplifier settling time, and conversion time. The basic scan rate is therefore 50 points per second. Scan rates up to 165 points per second can be obtained by using the group scan mode of operation.

During the group mode of operation, two, four or eight points are selected simultaneously. A high-speed relay (group switch) then applies one of these signals at a time to the amplifier input. After sufficient settling time an analog-to-digital conversion is made, and the next point is selected. In the group mode of operation, all points within a group will be digitized using the same gain range.

Both two-wire and three-wire switching of analog input points are available. Three-wire switching permits the use of a guard system, allowing more accurate measurements where common-mode noise voltages are significant.

The amplifier performs the functions of isolation, common mode rejection, and amplification to a level suitable for the A/D converter. The amplifier has six input ranges; ±10, ±20, ±40, ±80, ±160 millivolts and ±10 volts, selectable under program control. Maximum allowable input voltage is 500 volts. Maximum common mode voltage is 250 volts peak (100 volts for multigroup systems). Common mode rejection ratio is 120 db, or 10^6, when using the optional three-wire switching.

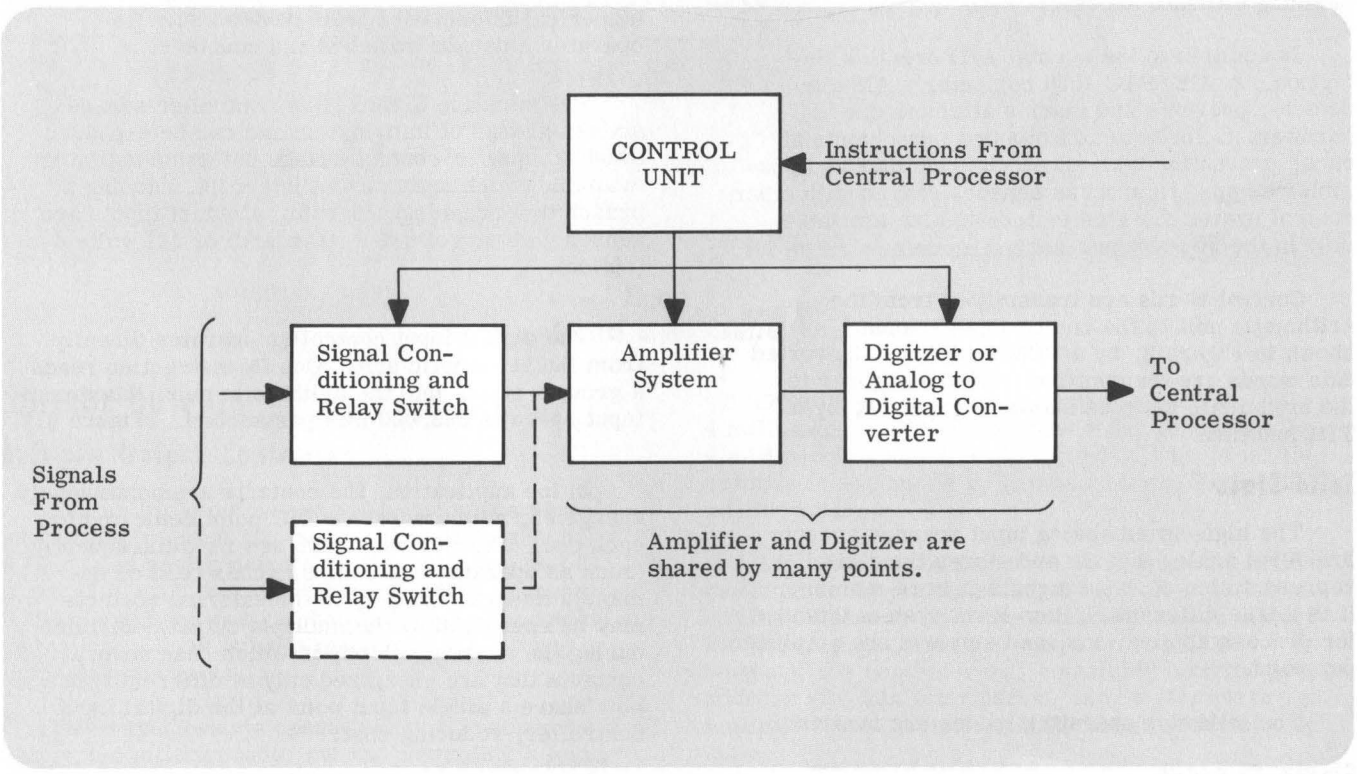


Figure 8
GE/PAC Analog Scanner System

Signal conditioning filters and attenuates the process instrument signals to one of the standard voltage ranges. A wide range of standard signal conditioning cards for attenuation, filtering, current inputs, resistance inputs (RTD bridges) and slide wires are available.

Thermocouple inputs require the use of thermocouple cold junction references. The temperature of the cold junction referenced is measured (rather than controlled). The correction for the cold junction temperature is made by the program. Open thermocouple detection is optional.

The RTOS software that drives the AIS has two features that increase its accuracy. The first is automatic (partial) compensation for thermal drifts, accomplished by taking a rolling average of the reading of a shorted input on each gain range and subtracting it from each process variable reading. The second feature, applicable to 50 point-per-second models only, is automatic gain changing, assuring that each variable is "tracked" and read at the highest possible gain and hence with the highest possible accuracy. This software then re-scales the reading just as if it were read at the nominal gain specified in the control word, so that calculation scaling is not affected.

The AIS hardware includes a voltage reference card, allowing periodic on-line calibration for gain (in addition to offset) by any functional programs desiring ultimate accuracy.

In addition to the normal A/D overflow detection, the GE/PAC 4020 computer's AIS also detects, prevents and alarms attempts due to hardware failures to address two input points at once, preventing both erroneous readings and possible "bumps" to process sensors shared with other control systems. This feature is also available only in the 50 point per-second models.

Control words are transmitted from the arithmetic unit to the analog input scanner, as shown in Figure 8, by a TOM function. Converted data words are transmitted from the scanner to the arithmetic unit, as shown in Figure 8, by a TIM function.

Solid-State

The high-speed analog input scanner accepts low-level analog signals and stores the digital representation of these signals in core memory. It is a true differential, low-level system intended for process applications, and employs one amplifier per point.

The following operating modes are available:

Single Channel

In this mode the computer instruction causes the system to enter the random scan mode, and will place one data word in core memory.

Sequential Scan

In this mode the computer instruction causes the system to enter the sequential scan mode, and will output sequentially the specified number of data words, commencing with the specified initial address.

The standard high-speed analog scanner, operating in the sequential scan mode, will scan up to 256 points at the rate of 40,000 analog points per second, with a resolution of 12 bits plus sign.

DIGITAL INPUT CONTROLLER

The GE/PAC digital input controller senses contact closures or logic level voltages. These are read into the arithmetic unit in groups of 23 bits, plus an additional validity bit taken directly from the power supply circuit breaker for detection of power supply failure and process wiring grounds, whether momentary or continuing.

The bits may be individual status bits, or may be coded in any manner, to be interpreted by the program. The digital input controller is used to read status information from devices such as limit switches, hot metal detectors, over-temperature switches, pressure switches, pushbuttons, alarm contacts, and shaft position encoders, and to read numerical information from devices such as operator's decade switches and counters.

The standard digital input controller senses sixteen groups of information and can be expanded to 64 groups. A contact change detection option is available which activates an interrupt, causing a branch to a scanning program. Contact inputs are sensed with 28 volts d-c (standard) or 125 volts d-c (option).

The digital input controller operates directly from the arithmetic unit. One IN instruction reads a group's status into the arithmetic unit. Maximum input speed is 883,000 bits per second. (Figure 9.)

In the application, the contacts are continuously energized, with a separate DIC point dedicated to each one. For devices which are read infrequently (such as operator's decade switches read on demand), the power supply to the external contacts may be energized by the multiple output controller during the sensing period, in which case several contacts that are energized only at different times may share a single input point at the digital input controller, reducing cost.

The digital input controller does not remember transient signals. Intermittent digital signals and digital information in the form of pulses are sensed by interrupt hardware rather than by the DIC.

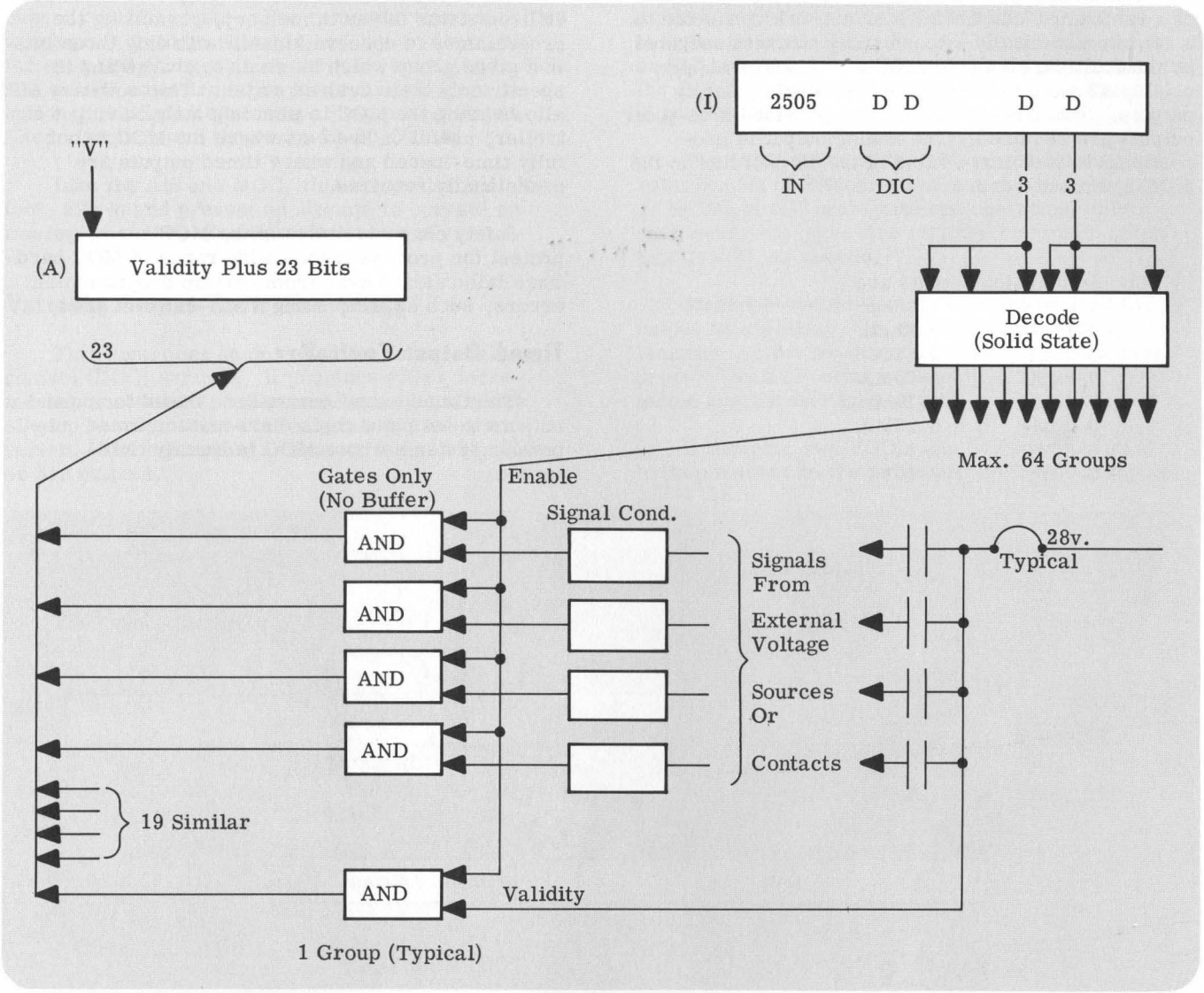


Figure 9
Digital Input Control

CONTROL OUTPUTS

Multiple Output Controller

The multiple output controller provides digital outputs in groups of 16, display outputs in groups of four, and analog outputs in groups of two (8-bit) or one (10-bit). Any combination up to 64 groups of the above functions can be handled by one output controller. Relay outputs may be either latched or momentary contacts.

The output relay's operating time is approximately 2.4 milliseconds, but the controller's logic allows 3.5 milliseconds for one operation plus 0.5 milliseconds for timer recovery. Thus, 250 multiple output operations per second are possible, or 4000 digital points per second.

Operating times are program selectable, either 4 milliseconds and 40 microseconds, or optionally, 4 milliseconds and 75 milliseconds. The 75 milliseconds is adjustable by hardware from 20 to 150 milliseconds.

After receipt of a control word from the arithmetic unit, the multiple output controller is entirely independent of the arithmetic unit and does its own timing. With the execution of a TOM function, the control word, containing both the group address and data information, is transferred to the multiple output register (MOR) from the arithmetic unit.

A special five-relay matrix is used for in-line decimal displays, energized by four bits in the MOC command word.

The analog generator or D/A converter consists of a resistance-current divider network connected to a set of magnetically latched relay contacts operated by the multiple output controller. A power supply, usually 42 volts or less, provides single polarity outputs. Two power supplies are provided if bi-polar outputs are required. The analog output is proportional to the binary value of the 16 data bits in the MOC command word.

Standard analog outputs are:

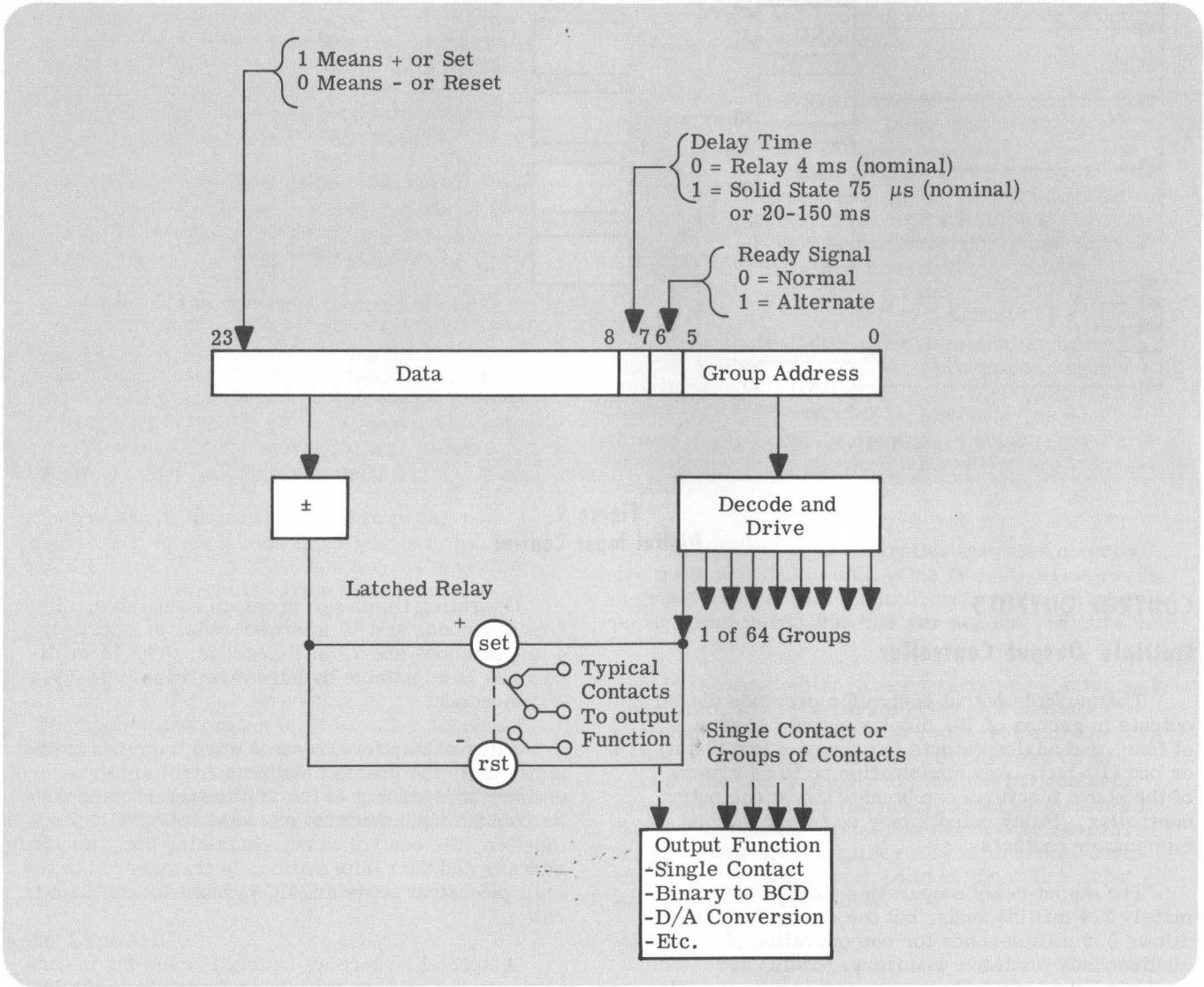
0-1MA	(Offset)
0-2MA	1-5MA
0-5MA	2-10MA
0-10MA	4-20MA
0-20MA	5-25MA
0-5V	1-5V
0-10V	2-10V

The RTOS software that actually drives the MOC utilizes status tables in memory, permitting the programmer to concern himself with only those bits in a given group which he wants to change and to specify only their desired states. This software also allows using the MOC to simulate a timed output controller, useful on systems where the MOC is not fully time-loaded and where timed outputs are occasionally required.

Safety characteristics of the MOC hardware protect the process from a wide range of MOC hardware failures and even from certain programming errors, such as addressing a non-existent group.

Timed Output Controller

The timed output controller is used for pulsed outputs to set point controllers and for timed outputs on systems whose MOC is heavily time-loaded.



Multiple Output Control

This controller operates one point at a time; its capacity is 128 points. The command word specifies which point is to be selected, an "up or down" bit for set point changes, and the pulse count (up to 255). The pulses come from the power line or from an optional oscillator operating at any pre-selected, fixed, frequency in the range 20-20,000 Hz.

Like the AIS and MOC, this controller will detect, alarm and prevent an attempt to operate an improper number of points simultaneously.

Variable Output Controller (VOC)

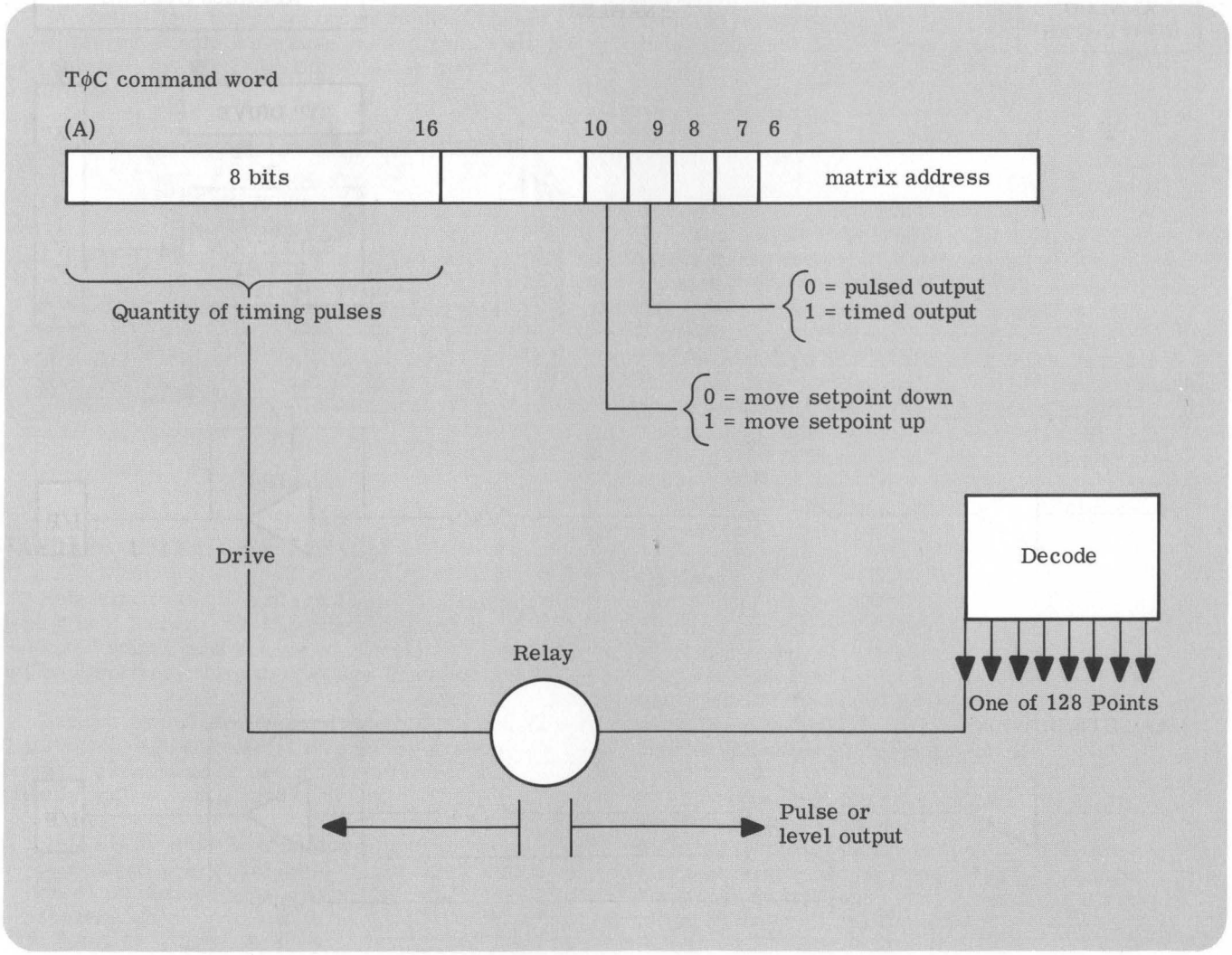
This controller is designed for direct digital control (DDC) service. It provides either incremental or absolute position analog outputs from a single, shared, solid-state digital-to-analog converter. The controller's capacity is 64, 128, 256 or 512 outputs.

Driven by a TOM function, the VOC receives a control word containing a 9-bit address, one bit to indicate incremental or absolute position output, and 12 bits of output value. If the output is absolute, the 12 bits represent its magnitude; if incremental, sign plus 11 bits.

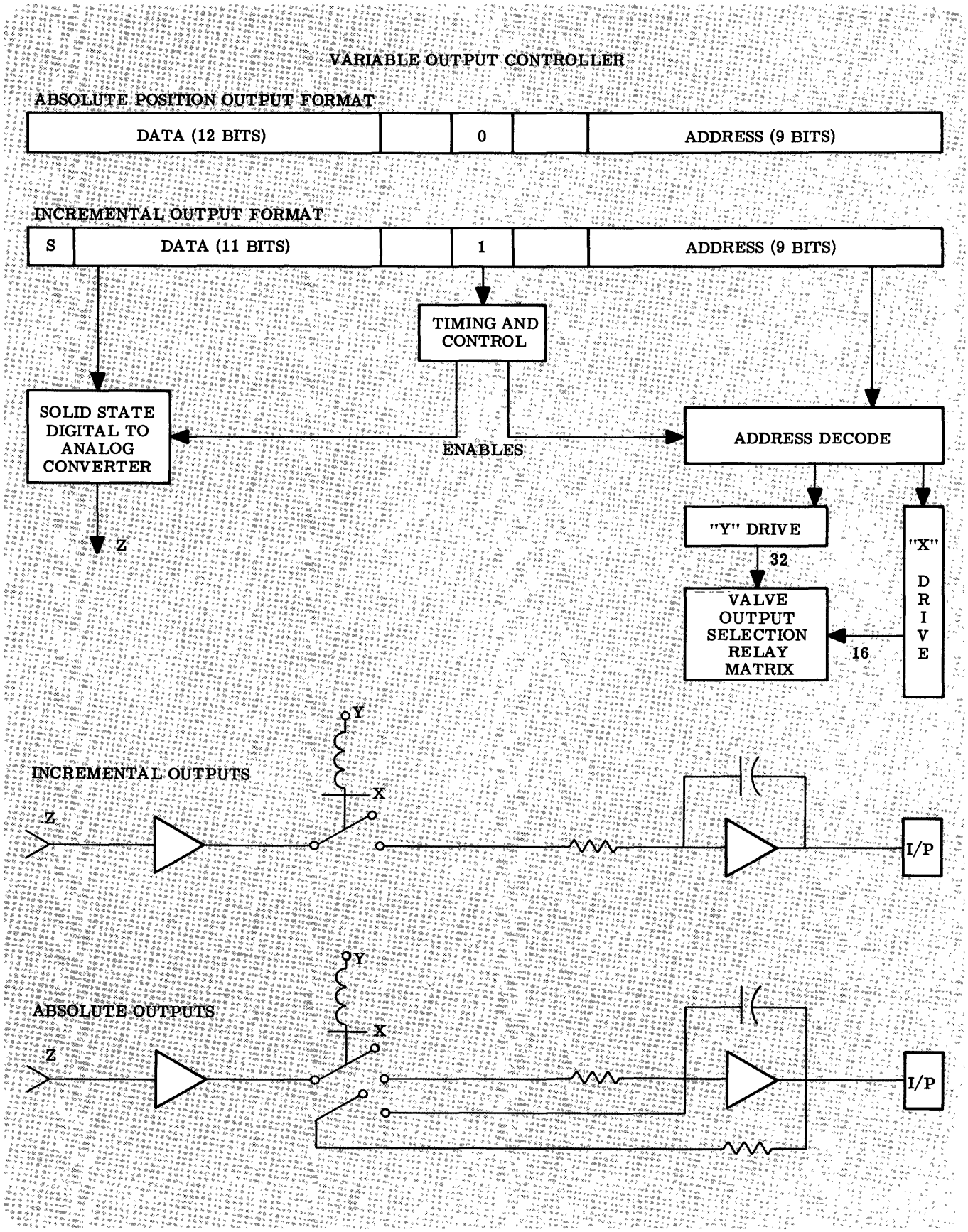
The VOC delivers up to 50 ma. d-c to a maximum burden of 300 ohms and can drive a set point up to 10% of full scale with one operation. Since each operation takes five ms, the maximum output rate is 200 per second.

Mercury-wetted-contact relays are used for output multiplexing, for maximum safety and isolation. Like the other GE/PAC 4020 computer process control output subsystems, the VOC is protected against multiple outputs.

If desired, two VOC's can be connected in a backup manner to the same GE/PAC 4020 computer.



Timed Output Controller


VARIABLE OUTPUT CONTROLLER
ABSOLUTE POSITION OUTPUT FORMAT
DATA (12 BITS)
0
ADDRESS (9 BITS)
INCREMENTAL OUTPUT FORMAT
S
DATA (11 BITS)
1
ADDRESS (9 BITS)
TIMING AND CONTROL
SOLID STATE DIGITAL TO ANALOG CONVERTER
ENABLES
ADDRESS DECODE
Z
"Y" DRIVE
32
"X" DRIVE
VALVE OUTPUT SELECTION RELAY MATRIX
16
INCREMENTAL OUTPUTS
Y
X
Z
I/P
ABSOLUTE OUTPUTS
Y
X
Z
I/P

PROCESS OPERATOR COMMUNICATIONS

SURVEY

Generally, process operators use special consoles for entering information into the computer and for requesting various special functions from it. These work out better than I/O typers because it is much easier to use them correctly.

The computer communicates with the operator by outputting on several electric typewriters. Usually, one typer is devoted to message and alarm print-outs and several more, to normal and special log print-outs of measured and calculated values. Occasionally, in installations involving multiple process units and a great deal of historical logging, a line printer at a central location will also be used, though even an electric typer can print information faster than most men can read it and act on it.

In applications where an operator must review a fair amount of data but where printed copies are not required, the GE Data-Edit Display may be preferable.

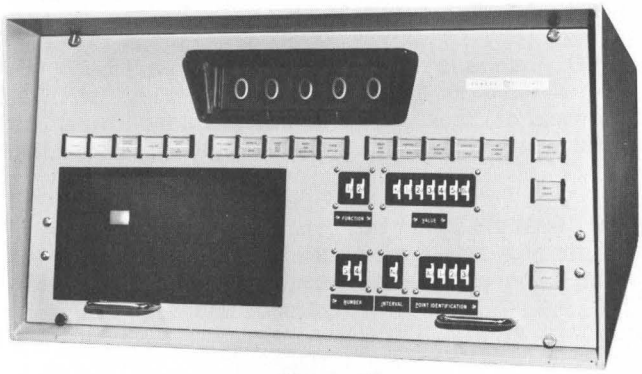


Figure 10

STANDARD OPERATOR'S CONSOLE

Referring to the console in Figure 10, the top display is a decimal, engineering units display of a selected point. Any sensor or calculated value may be displayed, through operator selection.

The top row of the "demand function" lights, (a 10 x 10 back-lighted matrix) is used for system alarms. These alarms are displayed in red and typically indicate such conditions as:

Stall Alarm - the light indicates that the computer is in a program loop, (stalled), or that a hardware failure has occurred to stop sequencing.

High Temperature - The light occurs when the cabinet temperature exceeds predetermined limits.

Peripheral Trouble - The light occurs if the computer tries to use a peripheral that will not operate.

Analog Check Point - The light occurs if the accuracy of reading a precision voltage is less than a predetermined value (0.1 to 0.2%).

Off Limits Alarm - The light occurs whenever a point is out of limits. As long as any values are in alarm, the alarm light will remain on.

The remaining rows of function lights are numbered by row and column, and contain a description of the function. For example, the third row and tenth column in Figure 10 is the "enter data" demand function, and is labeled as follows:

ENTER DATA	
10	FVMA

The operator determines the desired function and dials the function identification (10 in the above example) into the "function" thumb-wheel switches. The operator must then tell the computer what "value" is to be entered pertaining to what point ("point identification"), and what action is desired (storing) this value by dialing the appropriate thumb-wheel switches. Since the "enter data" function will change a location in memory, the "memory change" back-lighted pushbutton will light, reminding the operator that it must be pushed before the "action" pushbutton is activated. This is one of numerous safeguards.

Options

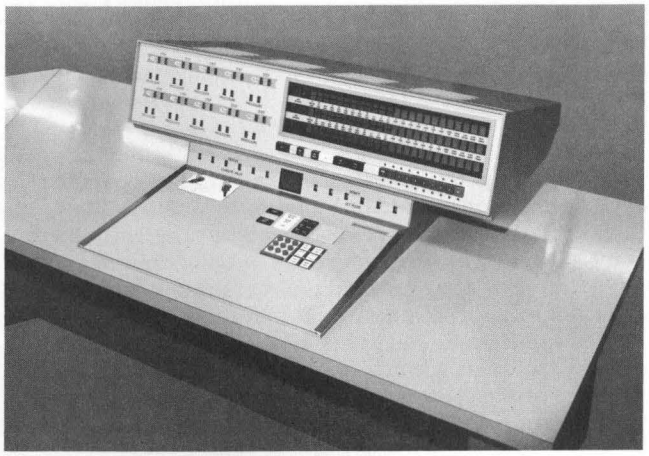
The standard GE/PAC 4000 console offers several options. In the examples above, the operator would have to select a demand function which would cause type-out of the point identification of the value being displayed. A second decimal display may be added for point identification.

Both the point identification and digital value displays may be eliminated, at the expense of operator inconvenience. In such a configuration, the operator would then be required to use demand functions and type-out in two steps to obtain identification of the point and its value.

The functional lights may be individually lighted according to the function selected on the function switch, or a single light behind all demand functions may be used. In either case, the demand functions lights are available in a wide range of color codes so that all summary functions can be one color, all limit functions another color, etc.

Also, audible alarms, (bells, buzzer, etc.) can be incorporated which sound with the activation of special alarm lights.

In some applications, a key-switch is desirable in place of the memory change pushbutton, to prohibit unauthorized changes. Such a key-switch may be substituted without changing the design or function of the console.



Special Operator's Consoles

Special operator consoles are provided where the standard consoles do not meet the requirements of the process control application.

REMOTES

COMMUNICATIONS COUPLER

The communications coupler adapts the standard GE/PAC input-output channels and control lines to the requirements of Bell System 103F, 201A and B, or 202C and D Data-Phone*s or other equivalent communication modems. Automatic dial-up and automatic-answering capabilities are not provided.

Communications Coupler Specifications

Operates simplex (two-wire, one-way) or half-duplex (two- or four-wire, two-way non-simultaneous transmission) over asynchronous and synchronous modems, and connects with them as specified in EIA RS-232-A. Two simplex modules will permit four-wire, full-duplex operation.

Provides asynchronous data rates of 150, 300, 600, 1200 or 1800 baud (bits/sec.) and synchronous rates of 2000 or 2400 baud. Rates are function of modems and lines used.

Receives data in parallel upon command (OUT instruction or TOM function) from computer and transmits serially, low order bit first, to modem; with start, parity, and stop bits added by coupler.

Collects data serially, low order bit first, from modem, checking start bit, parity, and stop bit, and transfers it to the computer upon command. (IN instruction or TIM function).

Provides signals for the API for finished transmitting and finished receiving. Provides status to the computer upon command for busy (either sending or receiving) and presence of parity and other errors on incoming data.

NOTE: All beginning-of-block, end-of-message, word or character counting and longitudinal error checks, when required, are generated by program.

Communications Coupler Wired Options

Minimum of five to a maximum of twenty-four bits of data, in one-bit increments.

Synchronous operation with local clock or modem clock or asynchronous with local clock.

Half-duplex, two- or four-wire; or simplex, transmit or receive.

*Trademark American Telephone & Telegraph Co.

Communications Coupler Jumper Board Options

Odd or even parity check and generate.

Optional speeds as above.

One, two, or three stop bits.

The communications coupler is used for transmission between the GE/PAC computer and the GE/PAC remote scanner, the Data-Edit CRT display and console, and remote computers including GE/PAC, Datanet 30, GE 100-Line, GE 400-Line, and GE 600-Line systems.

THE GE/PAC REMOTE SCANNER

The remote scanner provides the ability to monitor and control a process located at a distance from the computer, over voice-grade telephone lines, in conjunction with data sets and a GE/PAC communications coupler. The GE/PAC central processor can communicate with up to 16 remote scanners at different locations. The remote scanners may operate independently, or in a party-line mode, or in combinations of each with up to four per party line.

Input and output controllers are similar to those located at the central processor, except that the communications channel must be shared. Any or all of the following may be included:

Analog inputs, up to 512 points, 12 bits plus sign. (automatic group advance neither allowed nor useful)

Digital inputs, up to 64 groups, 11 bits plus validity, with or without change detection.

Multiple outputs up to 32 groups, 8 bits per group (analog output resolution limited)

Optionally, multiple outputs, up to 8 groups, 10 bits per group, for use with analog outputs of 10-bit resolution.

Timed outputs, up to 32 points, pulsed or timed, up to 63 counts.

Any of the standard GE/PAC peripherals which operate from the peripheral buffer, including I/O typewriter, but not including typed inputs from teletypewriter or other keyboards which do not have a locking feature. Peripheral ratings are reduced to 10 char. per second. (15 cps for GE/PAC I/O typer)

The remote scanner operates in half-duplex mode, (two-way, non-simultaneous transmission) at 1800 bits per second. Two pairs of Type 4B private phone lines are used with the data sets in order to eliminate turn-around time in the telephone lines and equipment.

In order to conserve line time, during the 20 ms delay for analog scanning, a digital input group with an address identical to the last 6 bits of the analog point address will be automatically transmitted to the central processor. Thus, the digital input function operates in two modes: with the analog input function, or independently.

For every request received by the remote scanner, the scanner will return one reply, except that analog input requests may return either one error replay or an analog reply plus a digital reply.

All output requests cause a non-data reply. All input requests cause a non-data error reply, or a data reply if the scanner detects no errors.

The remote scanner is controlled by the GE/PAC computer by transmitting 19 data bits from the arithmetic unit to the communications coupler, utilizing and OUT or TOM instruction. Bit patterns are shown in Figure 11.

By transmitting a request with bit #18, the repeat bit, set at "1", followed approximately 20 ms later (during which the request, less the repeat bit, is returned in reply) by a similar request with the repeat bit set at "0", the remote scanner may be required to do a complete bit-by-bit word check before acting on the request.

For maximum reliability, the repeat option should be used with output requests. Optimum performance with inputs is obtained by doing a complete check of two successive inputs within the central processor by program, rather than by using the hardware repeat function at the remote scanner.

Scan rates may be estimated for short lines (no repeater stations) by using 20 ms at the transmission time for one word. Thus, one output group may be energized or one input group read each 40 ms without repeat, or each 80 ms with the repeat option. In 30 ms, without repeat, one analog point and one digital group may be read. Overall scan rates vary with individual systems, depending on the mix of inputs and outputs, the number of remote scanners, and the number of voice-grade lines.

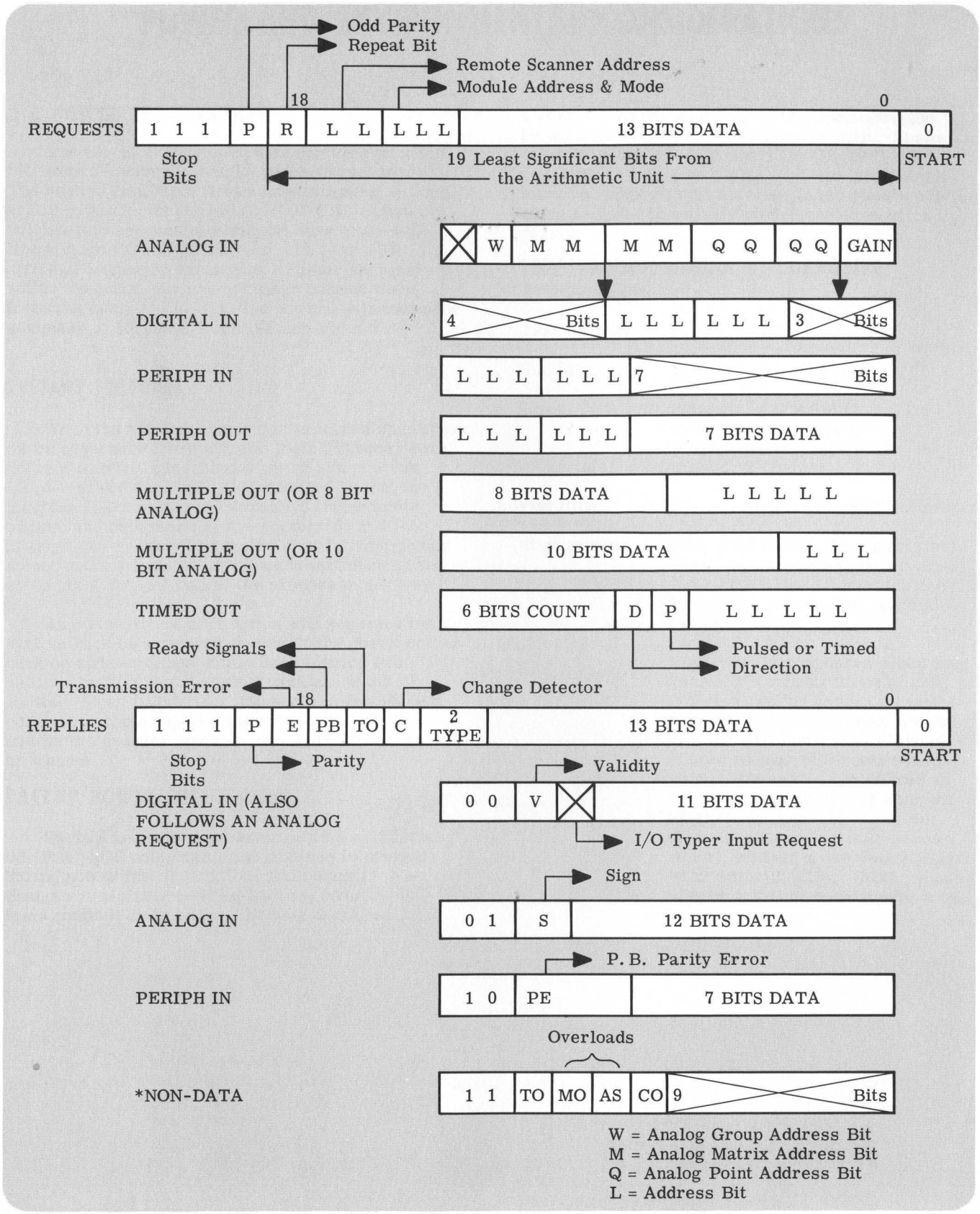


Figure 11
GE/PAC Remote Scanner Codes

*(Follows All Output Requests and all Error Transmissions.)

POWER AND ENVIRONMENTAL CONSIDERATIONS

A-C POWER REQUIREMENTS

The GE/PAC 4020 computer operates on a 115/230 volts a-c circuit, single-phase, three-wire. The central processor draws approximately 6.2 kva at 0.9 power factor. The GE/PAC 4020 computer will operate successfully despite slow + or -10% line voltage variations and + or -1% (+ or -3% optional) frequency variations. Faster changes within these limits and any change outside them, including complete loss of line power, will cause the computer to sequence itself off safely.

RESTART FEATURES

When the GE/PAC computer is turned on, turned off or sequences itself off, the logic voltages, core current source, internal a-c power and process I/O d-c power supplies are sequenced so that the machine is not damaged internally, the contents of core and bulk memory are protected, and the analog input scanner and multiple output distributor do not make erroneous or multiple operations, and so do not upset or "bump" the process in any way.

An automatic restart option will sequence the system back on and into program if the power comes back on and stabilizes within limits within two seconds to 10 minutes after it went off or out of limits. After 10 minutes, the process is assumed not to need the computer's services, though of course the process operator can start it up any time he wishes.

BACKUP POWER SUGGESTIONS

Backup a-c power is recommended only if the GE/PAC 4020 computer must continue to operate during power line fluctuations and outages. Although solid-state rectifier/battery/inverter systems continue to improve, the best operation from a reliability viewpoint to date has been provided by propane engine/motor/generator sets. In any event it is best not to connect the GE/PAC 4020 computer to a line supplying variable large motor loads but rather to get as close to the plant's primary a-c source as convenience and economics permit.

TEMPERATURE, HUMIDITY, CORROSIVE ATMOSPHERES

Temperature:	0-55°C
Humidity:	5-95%
Shock:	Shipping, 5 G's for 11 ms. on each of three mutually-perpendicular major axes. Installed, 2 G's.
Vibration:	5 to 55 cps at .015" displacement.
Atmosphere:	Dust from material such as steel scale, coal, cement, paper, and lint. (Particles 10 microns and larger are removed by internal air filters.)
	Corrosive atmospheres containing "normal" concentrations of salt, chlorine, sulfur gases, oil mist, and gas by-products from natural gas and coal furnaces. "Normal" concentrations of the more common contaminants are defined as not more than 10 ppm of chlorine (gas), hydrogen sulfide, sulfur dioxide and sulfuric acid (aerosol vapor), and not more than 0.1 ppm or chlorine dioxide. (Note: these are the lethal dose parameters for humans.)

ALPHABETICAL INDEX

The equipment described is compatible with the American Standard Code for Information Interchange (ASCII code). However, this does not imply full compatibility with other manufacturers' equipment using the ASCII code. In the construction of the equipment described, General Electric Company reserves the right to modify the design for reasons of improved performance and operational flexibility.

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PROCESS COMPUTER BUSINESS SECTION

PHOENIX, ARIZONA

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