Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
Device Channel Adapter (DCA)

No. 43A177862

L16-92 OKL BGE 2V TOS Total Pages 125 Page 1

REVISION RECORD

REVISION LETTER	DATE	PAGES AFFECTED	APPROVALS	AUTHORITY
A ISSUED	JAN 21 1970			
B Rev.	OCT 12 1971	Ret.& Rev.Sh. 1,4,11,24, 31,34,40,45,47,63,66,72, 77 & 90;Added Sh. 72.1; Rev.Sh.2,3,5,7-10,12,13, 15,16,23,25-30,32,33,41-44, 46,48,53,55,57-62,64,65, 67,69,74,76,78,80,83,101, 105,108,110,111,115-121	Oct. 6, 1971 CO ZEY-00-0067	

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)

(TABLE OF CONTENTS)

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)

TABLE OF CONTENTS
(continued)

TABLE OF CONTENTS
(Continued)

TABLE OF CONTENTS
(continued)

TABLE OF CONTENTS
(continued)

TABLE OF CONTENTS
(continued)

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)

1.0 GENERAL DESCRIPTION

This Engineering Product Specification, Part 1, describes the Device Channel Adapter (DCA) module used in DSS175/180 disc storage subsystems. It has been prepared in response to Large Systems Department Product Planning Functional Specifications, 69-003 and 69-008, and the DSS175/180 Subsystem EPS-1, 43A177861.

This specification encompasses the Device Channel Adapter (DCA), and the interface to the Device File Electronics (DFE). Of necessity, functions and specifications outside of the arbitrary hardware limits of the DCA (i.e., the 355, DFE, and Drives) are included in order to clarify the role of the DCA within the subsystem.

1.1 ELEMENTS OF THE SUBSYSTEM

The following diagram illustrates the relationships of the various elements of the subsystem, and the major logical divisions of the 355/DCA/DFE complex.

a) The 355 software functions as a primary controller (or sequencer) for the subsystem. As such, 355 software shall perform all functions which can be executed without exceeding the time constraints imposed on the 355/IOM and memory by the data transfer rate of the subsystem.

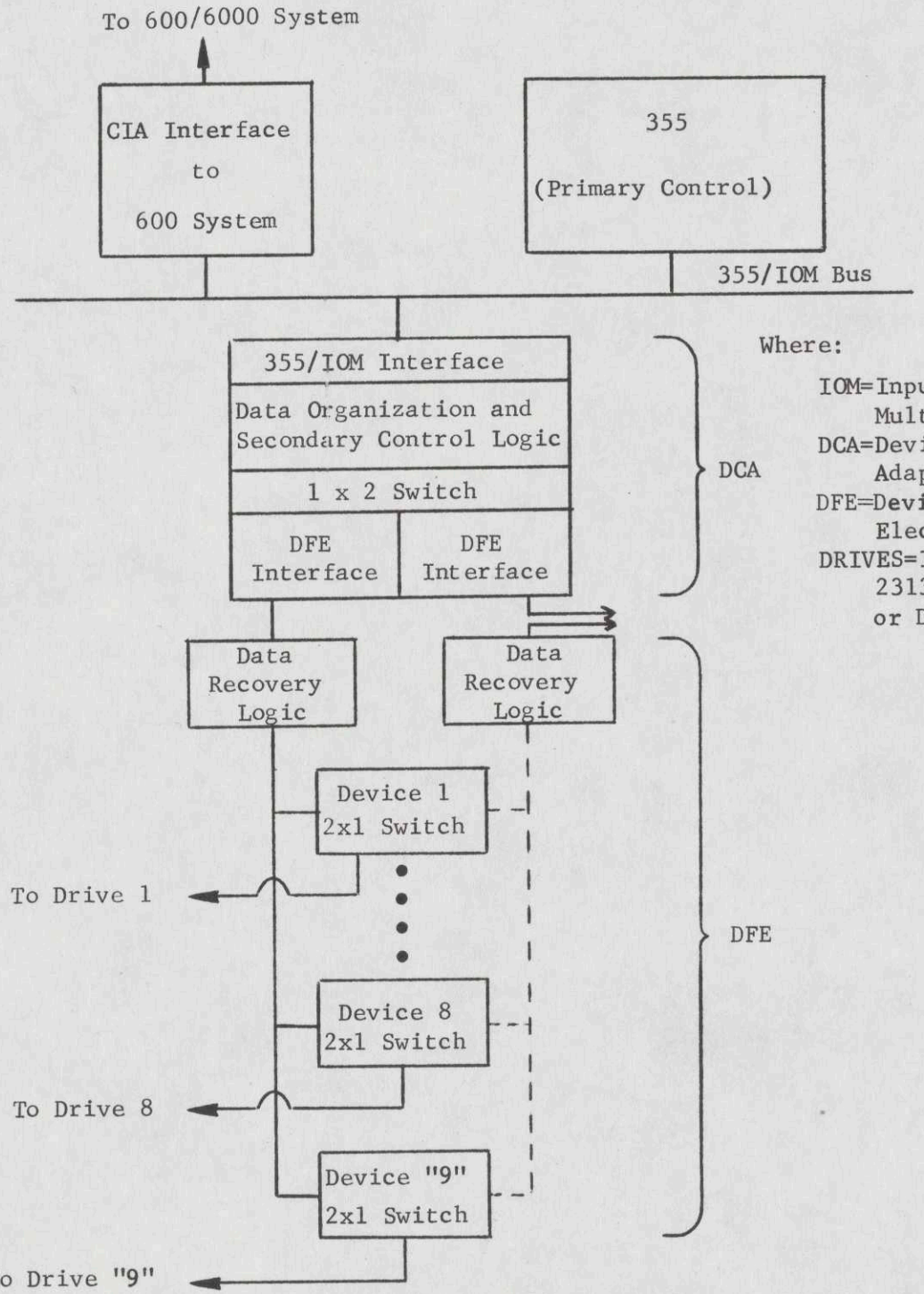
b) The subsystem will include a maximum of two DCA's (where both may be executing data transfer simultaneously), and four CIA's. The CIA's will operate in switched channel pairs with only one of each pair transferring data at any one time.

c) DCA channel adapters shall have priority over all other channel adapters connected to the 355/IOM.

d) Each DCA shall require no more than 5 MQX type boards.

e) The DCA shall perform those control functions which the 355 control software cannot execute because of insufficient response time. In addition, the DCA shall provide interfaces to the 355/IOM Bus and the DFE.

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)



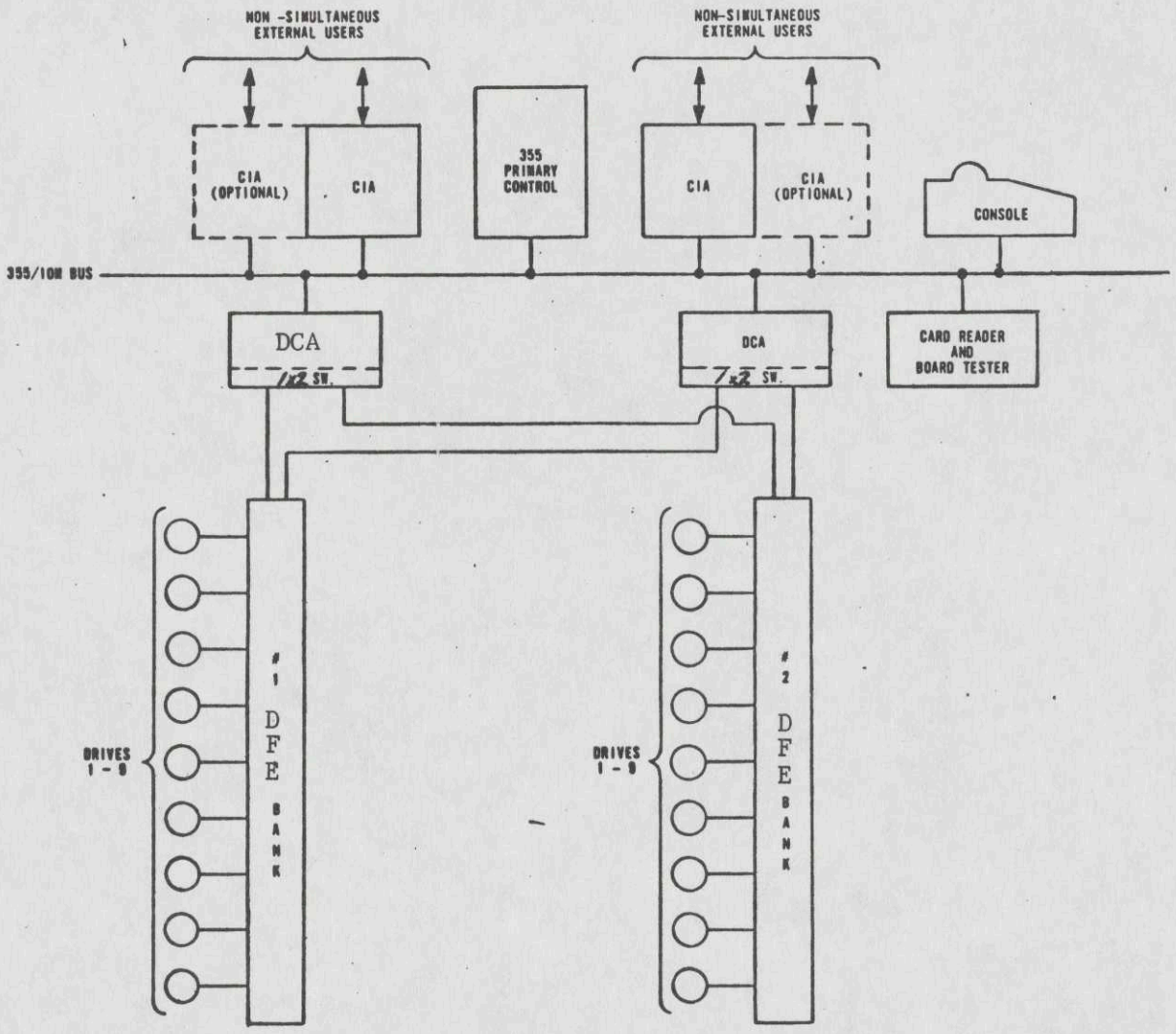
1.1 ELEMENTS OF THE SUBSYSTEM (continued)

f) The DFE shall perform those functions which are of direct concern to the drive specified for this subsystem. In addition, the DFE shall provide interfaces to the DCA and the devices. The Drives (Devices) to be connected to this subsystem are the IBM 2312 and 2313, or the HIS DSU180 or HIS DSU170B. IBM and HIS drives shall not be intermixed on a DFE. If the HIS and IBM drive interfaces are different, only simple board replacement in the DSU170B or the DFE shall be acceptable as a means to make IBM and HIS drives plug compatible.

g) The DCA and 355 Primary Controller shall write and read data on a discpack in a format compatible with the IBM 2314 removable disk subsystem.

The following diagram showing the maximum dual channel, single controller subsystem is included as an illustration of the connections of the subsystem elements. For a discussion of subsystem configurations refer to 43A177861.

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)



MAXIMUM DUAL CHANNEL SUBSYSTEM CONFIGURATION

B

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)

1.2 REFERENCE DOCUMENTS

GE-355 EPS-1, 43A219608, Revision B
Software EPS-1, 43A177865
Controller EPS-1, 43A177863
MQX Board Tester EPS-1, 43A177854
IBM 2312/2313 Drives: IBM File #S360-19, Form #A26-1586-1
IBM System 360 Component Descriptions, 2314 Direct Access Storage Facility, 2844 Auxiliary Storage Control: File #S360-07, Form #A26-3599-3
U.L. 478
IBM Field Engineering Manual, Theory of Operation, Y26-3671-3, March 1969
DAE EPS-1, M50EF00036
CIA EPS-1, 43A177858
B DSS175/180 Subsystem EPS-1, 43A177861
DSU170B EPS-1, M50EB00775
B DSU180 EPS-1, 59A301601

2.0 FUNCTIONAL CAPABILITIES

A requirement upon the DSS175/180 subsystem is that of IBM format compatibility. This format is characterized by variable field lengths, and the optional use of key fields as well as data fields. Also, the format includes the use of a Track Descriptor Record (Record 0) in addition to the Home Address identification of each track. The format is versatile, exhibits very useful user options. It is somewhat wasteful of storage space, and the use of fully variable key and data fields from sector to sector is probably operationally inefficient.

The discussion of functional capabilities must begin with the description of this format (paragraph 2.1). Paragraph 2.2 discusses the implementation of this format in GE 400/600 systems.

B The DSS175/180 subsystem hardware includes the capability of fully implementing the IBM format. The DCA is capable of formatting, reading, and writing variable data fields as well as key fields. DCA data processing is accomplished on a field basis, with software supplied data control words identifying the fields and their requirements. Thus, the format on the data track is the responsibility of the controller software.

Operational requirement of GE 400/600 systems are met by the implementation of fixed sector lengths with no key fields. The resulting format is compatible with IBM, but only on a subset basis.

2.1.1 Track Layout (continued)

d) The Count field of a sector is fixed in length.

e) The Key field of a sector (if present) can vary in length from 1 byte to 255 bytes.

[B] f) The Data field of a sector can vary from 0 byte to 7294 bytes.

g) The length of the Data field can be set to zero. If so, an End of File status condition is indicated by the IBM 2314 controller. A Key field may be present with a length ≠ 0.

h) "Gaps" between fields, within a sector, are fixed in length. "Gaps" between sectors are variable and a function of the length [B] of the key field plus the length of the Data field.

i) Lengths of the fields of a sector are measured in bytes (8 bit multiples), as opposed to lengths being measured in words (36 bit multiples), or characters (6 bit multiples).

j) A single data sector (including record zero) can be formatted, or a whole track can be formatted. If a single sector is formatted, the balance of the track is written with "ones" until the index mark is detected.

k) A "sync byte" (the last byte in every gap area) identifies the type of field following it.

l) The last four bytes of every field are identified as:

Burst CK	Burst CK	ID Byte	Bit CNT

where:

Burst CK = Cyclic code bytes for error detection.

These bytes are calculated from the preceding data in the field, as described in the IBM Field Engineering Theory of Operation manual (Y26-3671-3) page 1-13.

2.1.1 Track Layout (continued)

B

ID Byte = This byte identifies the DFE and device which wrote the field on the track. The format of this byte is identified in paragraph 3.2.11.2.

Bit CNT = Bit count check byte. This byte records, modulo 8, the number of one-bits written in the field in ones complement form. Functionally, this byte is included as another code checking byte. Failure to compare the bit CNT is the same as a cyclic check compare failure.

These last four bytes are not part of the data of a field and are not usually transmitted beyond the DCA.

THE ABOVE DESCRIPTION OF THE LAST FOUR BYTES PERTAINS TO IBM 2314 MODEL A1 SUBSYSTEMS. IN EARLIER, MODEL 1, SUBSYSTEMS THE ID BYTE AND BIT CNT BYTE ARE NOT INCLUDED --- A FIELD ENDS WITH THE TWO BURST CHECK BYTES. THE DCA WRITES ALL OF THE FOUR BYTES DESCRIBED ABOVE IN THE MANNER OF MODEL A1. See paragraph 2.2.

2.1.2 Field Structure

The fields discussed above exhibit the following structure:

2.3.3 Access Times (Refer to the DSU170B EPS, M50EB00775)

a) Latency Time:

The discpack rotates at 2400 rpm ± 2%. Therefore, the maximum rotational delay is 25 milliseconds ± 2% and the average rotational delay is 12.5 milliseconds.

b) Track Access Time:

The following access times are measured from "seek start" to "seek complete" and therefore, do not include any data transfer time.

- Maximum Track Seek Time (Between track 000 and 202):

  135 milliseconds (170B);60 milliseconds (180)

- Minimum Track Seek Time (Between Adjacent Tracks):

  25 milliseconds (170B); 10 milliseconds (180)

- Average Random Track Seek Time:

  75 milliseconds. (170B); 35 milliseconds (180)

2.4 SUMMARY OF FUNCTIONS OF THE 355 (CONTROL SOFTWARE)

From the DCA/DFE/Device point of view the 355 Control Software shall perform the following functions:

1) Interpret macro type instructions, received from the 600 system, into sequences of micro (type) commands for the DCA/DFE/Device combination.

   Ex: Macro type: Seek, Read, Write, Request status, etc.

   Ex: Micro type: Load External, Store External, Select Channel, Connect.

2) Provide sufficient data buffering in 355 memory to eliminate the possibility of a transfer timing error between the 600 system and 355/CIA.

   If the control software finds that the total buffer space available is filled and cannot keep up with a given data transfer, it will provide the ability to take a latency and resume the data transfer.

2.4 SUMMARY OF FUNCTIONS OF THE 355 (Control Software) (continued)

2) (continued)

Therefore, the Control Software shall not initiate a data transfer sequence to the DCA unless it has buffered (or has buffer space available for) sufficient data for at least one full sector.

3) Data transfers at the 600 level shall not be limited to a length equal to the sector length, but shall only be limited by end of cylinder, encountering alternate and defective tracks, and similar physical constraints.

The Control Software shall initiate data transfer sequences to the DCA equal in length to the sector length. Therefore, if a data transfer from the 600 system exceeds the sector length, the 355 shall be responsible to initiate multiple data transfer sequences to the DCA until the data transfer is complete. The multiple command sequences (of the 355) shall be transparent to the 600.

4) The Control Software shall perform a status mapping function to convert status information received from the DCA/DFE/DRIVE into the Common Peripheral Status format.

5) The Control Software shall provide a switching matrix function for multiple DCA's (CIA's) connected to the IOM bus.

6) Simultaneous data transfers to/from devices are possible only with multiple DCA's (on any one 355 Primary Controller).

The 355 shall <u>not</u> be required to accommodate simultaneous data transfers on more than two (2) DCA's and more than two (2) CIA's; for a total of 4 transfers taking place simultaneously.

If additional CIA's are connected to the 355, the 355 shall treat the excess as switched channels.

2.4 SUMMARY OF FUNCTIONS OF THE 355 (Control Software) (continued)

[B] 7) The 355 shall initiate micro sequences to Reserve/Release drives based on the macro type instructions received from the 600 system.
[B] Note that the DFE 2x1 switch (see paragraph 1.1) shall physically Reserve/Release drives, and the 2x1 switch shall remember the drives "reserve" status for later interrogation by the 355 control software.

[B] 8) The Control Software shall process interrupts, and perform status checks of the DCA. The Control Software shall relate status to device (based on information received from the DCA). In addition, the Control Software shall be responsible to return status to the 600 system consistent with the Common Peripheral Interface priority structure for status.

[B] 9) The Control Software shall convert the continuous binary seek address, received from the 600, into the Cylinder-Head-Sector format required by the DCA.

2.5 SUMMARY OF FUNCTIONS OF THE DCA

1) Provide an interface compatible with the 355/IOM Bus. The data interface shall be 36 bits.

2) Provide sufficient data buffering to minimize transfer timing errors for a configuration consisting of two CIA's and two DCA's which are transferring data simultaneously.

3) The DCA shall respond to the following 355 commands in a manner to be defined in later paragraphs:

Load External

Store External

Connect (Sequence). See paragraph 2.5.1

B 4) The DCA shall communicate with the DFE (and ultimately the drives) across the DFE interface described in paragraph 4.

5) The DCA shall control the physical formatting of gaps and sectors on the disc pack (drive) in a format compatible with the IBM 2314 Model A1 subsystem.

2.5 SUMMARY OF FUNCTIONS OF THE DCA (continued)

6) The DCA shall contain logic necessary to remember and act upon Key length information and Data length information. Information for this logic may originate from data read from a disc pack, or from the 355 during a Format operation.

[B] 7) The DCA shall convert the bit serial data received from the DFE into the 36 bit format required by the 355/IOM Bus. The DCA shall convert the 36 bit data of the 355/IOM bus into the bit serial stream of [B] "clock" and "data" bits required by the DFE (serialization/deserialization).

[B] 8) Provide miscellaneous control logic for the DFE.

9) Provide the "fill" characters and control logic required to write gap areas between sectors and between fields within a sector.

10) Provide Count Field (header) verification for data sectors (cylinder, head, record, track indicator bits, Key length, and Data length).

11) Provide check character generation logic (Write) and comparison checking (Read).

12) Provide a memory address register for transferring data to/from the 355 memory.

13) Provide maintenance (T&D) "wrap around" functions.

14) Provide address mark detection and generation logic.

15) Provide field identification (Sync byte detection).

16) Provide gap timing counters.

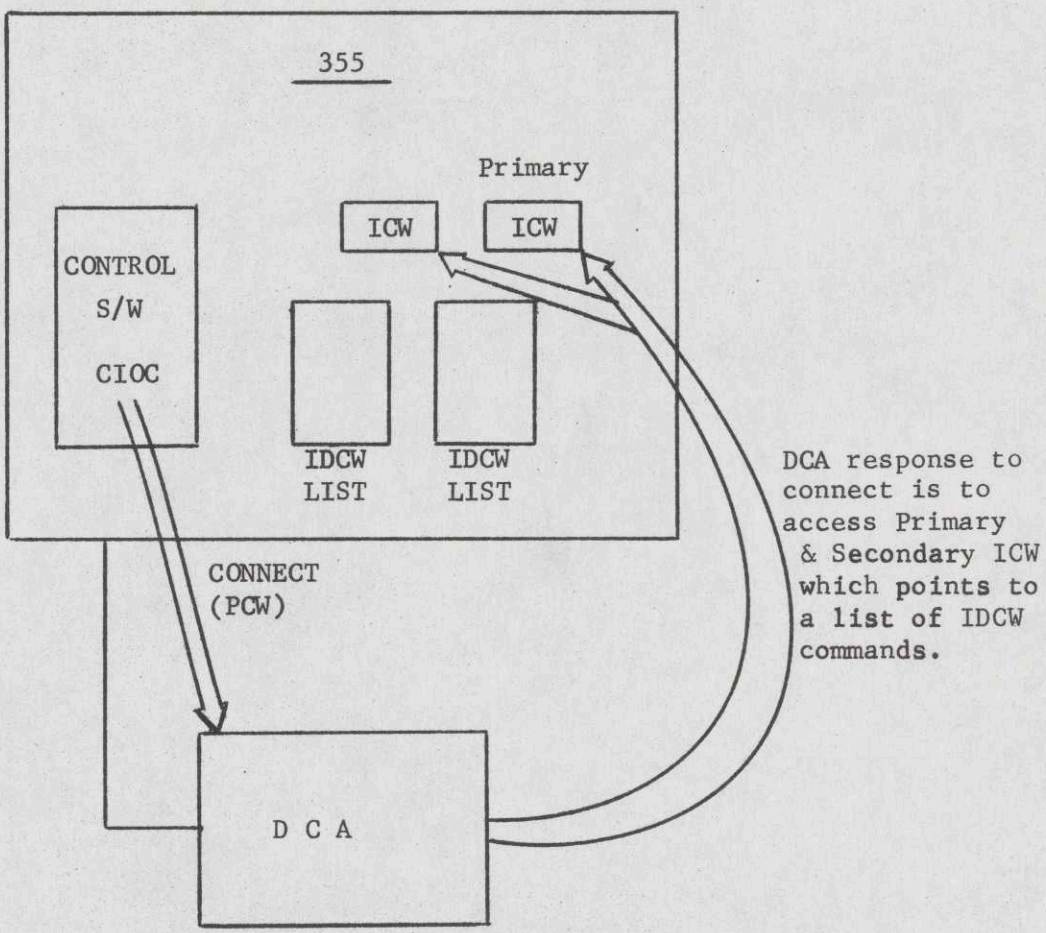
17) Detect whether sectors on a discpack have been formatted by an IBM 2314 Model 1 subsystem.

2.5.1 DCA Data Transfer Techniques

In order to provide continuous sector-to-sector data transfers, the control software will not generally handle each sector data transfer separately, with a new "connect" for each. Instead, the software/DCA communication is accomplished by means of a "list" of data transfer commands (IDCW's) prepared by control software, and executed by the DCA.

2.5.1 DCA Data Transfer Techniques (continued)

The process is outlined briefly below and discussed in detail in Section 3 of the EPS.



2.5.1 DCA Data Transfer Techniques (continued)

[B] The data transfer sequence begins by the issuance of a CONNECT to the DCA which causes it to access an ICW (Indirect Control Word) which points to the list of IDCW's. The IDCW is sent to the DCA by the 355/IOM.

The DCA depends on the following 355 and IOM functions for a data transfer operation:

- The Connect/Peripheral Control Word (PCW) function initiates all data transfer operations.
- The Indirect Control Word (ICW) function utilizes a list of field oriented DCA commands.
- The Instruction Data Control Word (IDCW) function provides the DCA with the location of data in 355/Memory and specifies the operation to be performed.

Once a data transfer operation has been initiated (by a Connect/PCW), the operation is sustained from field to field by allowing the DCA to access the ICW upon the successful completion of each field IDCW. The DCA shall continue to fetch IDCW's [B] until the DCA is commanded to stop (by an IDCW), or ICW Tally Run Out occurs or some fault has occurred.

Data transfer capabilities are further enhanced by the ability of the control software to switch the DCA to a secondary ICW (which points to a separate list of IDCW's) by setting a switch bit wihtin an IDCW in the list.

[B] 2.6 SUMMARY OF FUNCTIONS OF THE DFE

The Device File Electronics shall include the following functions, [B] (refer to paragraph 4.0 for further details on the DFE Interface).

1) Provide the Data Recovery logic necessary to translate the analog signals of the drives into serial streams of digital data bits and clock bits, for further processing by the DCA.

2) Provide the logic necessary to accept serial streams of clock and data bits to be written on the drives.

3) Provide a 2x1 crossbar switching function for data and control signals to/from each drive.

B 2.6 SUMMARY OF FUNCTIONS OF THE DFE (continued)

4) Provide and control both AC and DC power to the drives.

5) Provide physical drive status information to the DCA for eventual transmission to the 355.

6) Provide the device Reserve/Release function.

7) Provide a 5 megacycle clock.

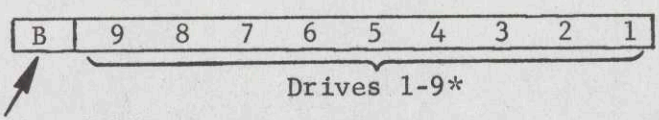
B 8) Provide lines for DFE identification.

2.7 DEVICE ADDRESSING

Channel Number is a 355 Control Software function necessary to select a channel adapter for I/O operations on the 355/IOM Bus. The DCA shall contain a wired "patch" corresponding to the channel number.

B The DFE Bank Number sent to the DCA can only have an address of zero or one even though from 1 to 4 DFE Banks can be present within the subsystem. However, only two DFE's are physically possible on one DCA. The DFE Bank shall have physical addresses within the range 0 thru seven (binary). 355 Control Software shall have the capability to map the 600 system Device Code into the correct DFE bank. Once set, DFE Banks are not expected to change, but any DFE (Bank) address can be connected to any DCA. B

The Device Code sent to the DCA shall be converted to the following form by 355 Control Software:



B DFE Bank 0 = 0 bit
DFE Bank 1 = 1 bit

* NOTE: A bit position designates a logical drive number. Only one drive bit can be set at any one time.

2.8 DCA BUFFER REQUIREMENTS

2.8.1 DCA/355/IOM Bus Interface Buffer

The DCA shall be required to have buffer storage for a minimum of 6 characters (36 bits) of data for this interface.

These Buffer requirements are based on the following conditions:

- DCA's shall always have the highest priority for data transfers on the 355/IOM/Bus.
- No more than two DCA's shall ever be connected to the 355/IOM Bus.
- No more than two DCA's and two CIA's are permitted to transfer data simultaneously on the 355/IOM Bus.
- Data transfers occur on a Field basis only.
- Data shall be transferred between the DCA and 355 memory on a "direct" by 36 bit basis.
- 355/IOM Bus service delays for a data transfer shall never exceed 13.8 microseconds for any reason.

[B] 2.8.2 DFE/DCA Interface Buffer

[B] During a read operation, the DCA shall be required to convert the bit serial data received from the DFE into 36 bit parallel data for transmission to the 355.

During a write operation, the DCA shall be required to convert 36 bit parallel data received from the 355 into bit serial data for [B] transmission to the DFE.

2.9 DATA INTEGRITY

2.9.1 DCA/355 IOM Interface

The 355/IOM does not contain the logic necessary to transmit the memory parity bit to the DCA, nor does the 355/IOM contain the logic necessary to check parity generated by the DCA. Refer to paragraph 3.1.3.3 for description of DCA parity checking function.

2.9.2 DCA/DFE Interface

Information is transferred between the DCA and the DFE in a bit-serial manner. "Burst check" and "Bit count" check bytes are generated by the DCA and written with the data. On subsequent read operations, the DCA regenerates the check bytes based on the data read, and compares them to the check bytes read from the disk.

The check byte algorithm, designed into the DCA for write operations, shall be compatible with the IBM 2314 Model A1 subsystem, and shall not cause an error condition to be detected by the IBM 2314 subsystem. The check byte algorithm, designed into the DCA for read operations, shall be compatible with the IBM 2314 Model 1 and Model A1 subsystems.

All information fields written on the discpack shall contain check bytes (see paragraph 2.1.1).

2.9.3 Status

Conceptually, status provided by the DCA can be separated into two logical groups:

- Device oriented conditions.
- DCA oriented conditions.

a) Control Software shall be provided with the ability to receive both status groups. Accesses for device oriented status shall require a sequence of 355 LDEX and STEX commands. Control software shall interrogate device oriented status under the following conditions only:

   - The DCA is in a static state (not busy). Therefore, 355 Control Software shall be required to remember whether the DCA is "busy" or not.

2.9.3 Status (continued)

a) (continued)

. A control software sequence is being executed which does not require a status return within a critical time period.

b) Upon the termination of a data transfer type operation, the DCA automatically stores information from both status groups at a fixed ("patched") location in 355 memory.

2.9.3.1 Device Status Group

The following conditions are reported as device status:

. Device Unsafe **

. Device Off-Line **

. End of Cylinder **

. Write Current Sense (error)

. Alternate Channel desire Control **

B

. Device Busy Positioning

. Pack Change

. Seek Incomplete

. Device Reserved to the Alternate Channel

For detailed information concerning these status conditions, refer to paragraph 3.2.7.
** NOTE: These status bits are also supplied during a DCA status service.

2.9.3.2 DCA Status Group

The following conditions are reported as DCA status:

. Device/DCA exception condition detected.

. Record Number did not compare*

2.9.3.2 DCA Status Group (continued)

- Count Field did not compare*.
- Data length or Key length < Data length or Key length in 355 Memory*.
- Connect/LDEX/STEX detected by the DCA while "busy".
- Check character error (count field).
- Check character error (key or data fields).
- ICW address.
- Transfer timing error (DCA/355 IOM).
- TRO caused terminate.
- Two consecutive index marks detected during a data transfer command.
- Write current sense error.
- [B] Data transfer operation in progress at index mark.
- Sync Byte failure.
- Invalid IDCW sequence.
- Compare error on Key or Data field.
- End of File Record (Data length = 0).
- 204_{10} (CC) detected - discpack was generated on an IBM 2314 Model 1.
- [B] Parity error during list service (IDCW).
- Control Software sync bit.
- SSI Bit Caused interrupt.

For detailed information concerning these status conditions, refer to paragraph 3.2.8.

* NOTE: These status conditions are possible with the Compare ID (CNC) command only.

2.10 OTHER FEATURES

2.10.1 Channel Number Patch

The channel number patch consists of a six-bit field which is switched into the IOM bus when the DCA requests service from the IOM. This field must be capable of being any six-bit code by "patching." This same physical "patch" will be used for both encode and decode in order to reduce the possibility of configuration problems. That is, the IOM will present the same six-bit code when it initiates a sequence to the DCA that the DCA would present when it initiates a sequence.

2.10.2 Program Interrupt Level Patches

The DCA will use two interrupt levels, each of which shall be "patchable", allowing the DCA to use 2 of 8 of the highest priority interrupt levels. The 2^3 bit shall be a constant "0."

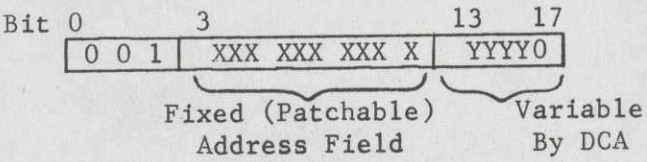
The two interrupt levels shall indicate the following events have occurred:

- A data transfer command has terminated.
- A "gated Attention" condition has occurred (such as seek complete) provided that the DCA is not busy with a data transfer command.

2.10.3 Fixed Memory Address Patch

Each DCA shall require a reserved area of 32 (18 bit) words in 355 memory for its own operational use. (Refer to paragraph 3.3, Memory Map, for further details.) The starting address shall be designated by an address "patch" physically located in the DCA.

When the DCA executes an operation that requires access to the reserved area, it will access 36 bits at a time using the following address format:



3.1.3 355/CIOC/PCW/ICW/IDCW (General) (continued)

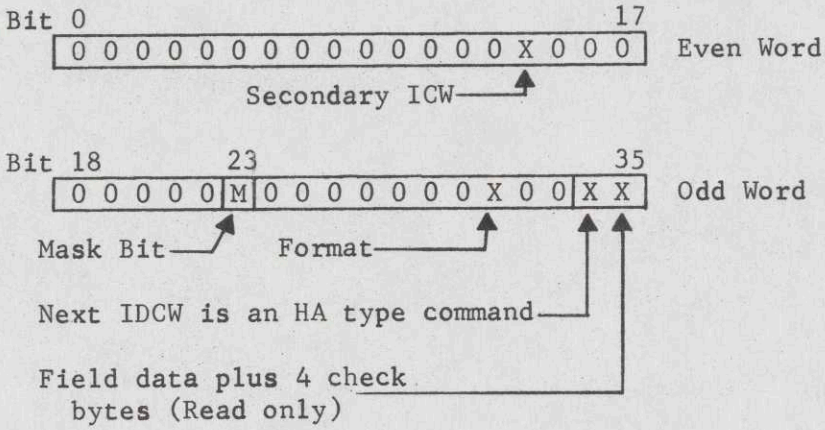
h) (continued)

An error was detected. The list of IDCW's shall be terminated prematurely. Error status shall be stored in 355/Memory.

Tally Run Out (TRO) was detected by the 355/IOM when it processed the ICW. Error status shall be stored in 355/Memory.

3.1.3.1 Peripheral Control Word Format (PCW):

Information contained in the 36 bit PCW shall conform to the following format:



The DCA shall not alter the contents of the PCW in 355 Memory. Refer to the 355 EPS-1, 43A219608, Revision B, for further details on the CIOC (Connect) instruction and the Peripheral Control Word (PCW).

a) Bit 0 thru 13, bit 15 thru 22, bit 24 thru bit 30, bit 32 and 33; The DCA shall ignore these bits.

Bit 14=1; The DCA shall go to secondary ICW list.

b) Bit 23 = 1; The DCA shall be forced into the masked state. The DCA shall not initiate any further action. See paragraph 3.1.3.4 for further details on the Masked state.

c) Bit 23 = 0; This bit is always zero during normal operation. See paragraph 3.1.3.4 for further details on the Masked state.

Bit 31 = 1; This bit will put the DCA into Format mode when operation is to start with HA.

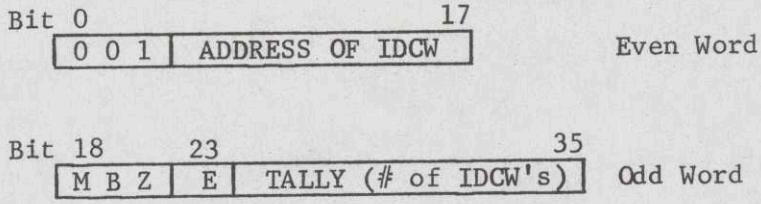
3.1.3.1 Peripheral Control Word Format (PCW) (continued):

d) Bit 34 = 1; The next command in the List of IDCW's (i.e., the first command in the List) is a Home Address (HA) type command. The DCA shall wait for index mark before attempting to write or read, and shall expect a "Count" type field consisting of 5 bytes of data plus 4 "check" bytes.

e) Bit 35 = 1; All Read type IDCW's in the list shall transfer 4 extra bytes to 355 memory. These 4 extra bytes consist of the 2 check bytes, the I.C. byte, and the Bit Count byte appended to each Field.

3.1.3.2 Indirect Control Word Format (ICW):

Information contained in the 36 bit ICW shall conform to the following format:



The contents of the ICW are altered by the IOM each time the ICW is accessed by the DCA. Refer to the GE-355 EPS-1, 43A219608, Rev. B (paragraph 2.3.4.2) for a detailed description of the ICW.

a) Location of ICW's in 355 Memory:

The DCA is capable of accessing either of two ICW's located in 355 memory. The PRIMARY ICW shall be located in locations A + 16 and A + 17. The ALTERNATE ICW shall be located in locations A + 18 and A + 19. (Refer to paragraph 3.3, Memory Map.)

b) ICW Address Switching:

In response to a CONNECT/PCW sequence, the DCA shall access the PRIMARY ICW if bit 14 = 0. B

3.1.3.2 Indirect Control Word Format (ICW): (continued)

b) ICW Address Switching: (continued)

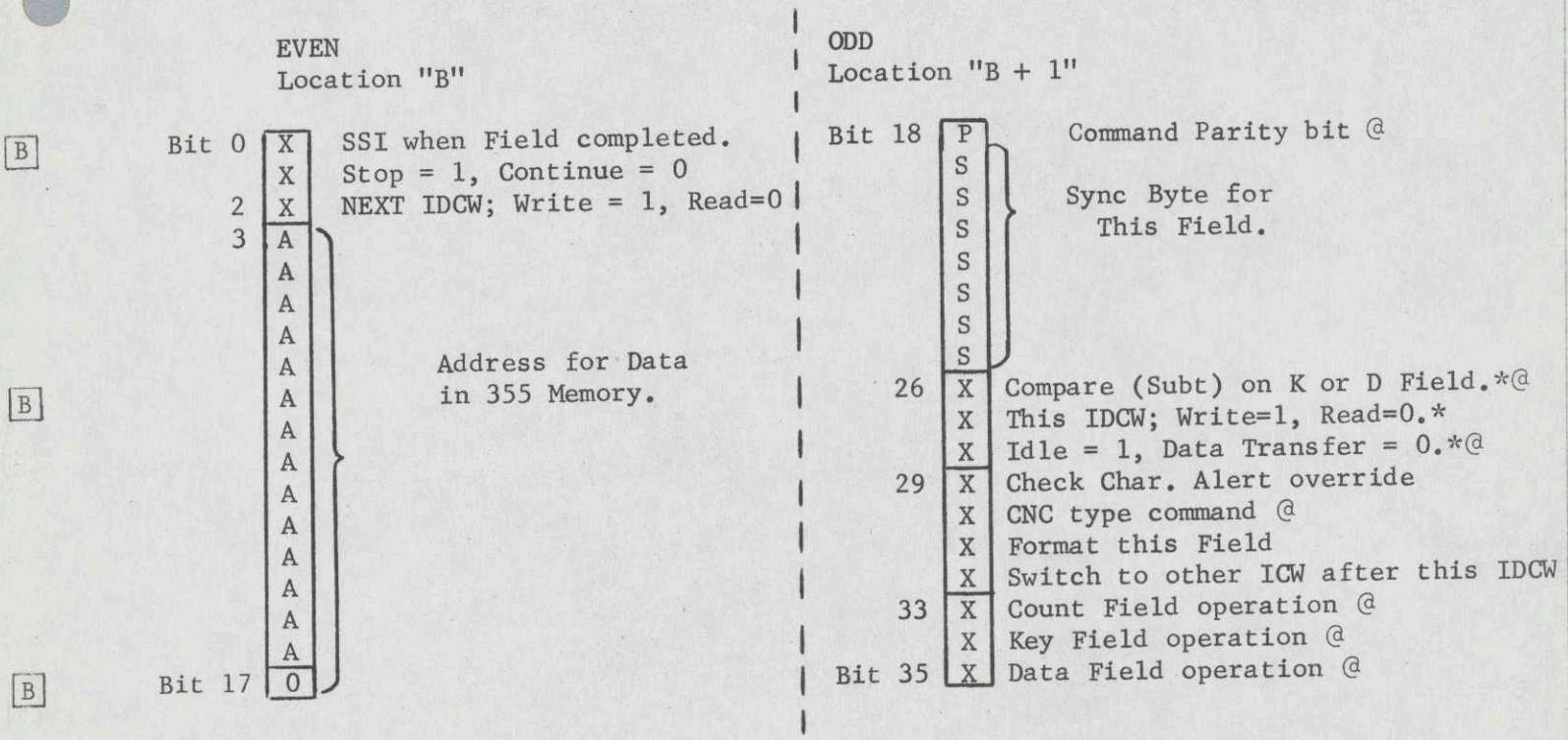
The DCA shall be capable of alternating between the PRIMARY ICW and the ALTERNATE ICW. Each IDCW contains an ICW switching bit which commands the DCA to change ICW's. The DCA shall continue to access the new ICW until another ICW switching bit is encountered within a later IDCW in the list.

c) ICW Status Indication:

Status, stored in 355/Memory as the result of an SSI, shall contain a unique bit designating which ICW was accessed for the IDCW just completed.

3.1.3.3 Instruction Data Control Word (IDCW):

Information contained in the 36 bit IDCW shall conform to the following format:



* See NOTE on following page.
@ See NOTE on following page.

3.1.3.3 Instruction Data Control Word (IDCW): (continued)

[B] @ NOTE: These bits must form ODD parity.

* NOTE: Valid Code combinations for these 3 bits are:

001 = Read from disc, no data transfer.
000 = Read from disc, data transfer.
010 = Write on disc, data transfer.
100 = Compare Data in Key or Data field.
011 = Write on disc, no data transfer.

[B] The undefined codes: 101,110 and 111 will be interpreted as 001,010 and 011 respectively.

The DCA shall not alter the contents of the IDCW in 355 Memory. Each IDCW shall specify an operation to be performed on a single field. Therefore, more than one IDCW shall be required to process a single sector, or multiple sectors.

With the bit structure described in this paragraph, it is possible to build an extensive and extremely versatile set of command codes. Of all the commands possible, only a subset is potentially useful. These commands are described in paragraph 3.4.3.2. However, the DCA shall not test the validity of any op-code, and undefined commands (op-codes) [B] shall have undefined results. The DCA will perform a parity check on the bits specified above.

a) Bit 0; Store Status and Interrupt Bit (SSI):

. Bit 0 = 1; SSI when this field (IDCW) has been completed.

After processing this field (IDCW), the DCA shall execute an SSI. Status shall be stored at fixed locations A and A + 1 (See paragraph 3.3.1 for status and paragraph 3.3, Memory Map). Termination of the IDCW list is not implied by the SSI bit unless the Stop bit is set also (Bit 1 = 1), or an error is detected. Conversely, if an error is detected, an SSI shall be executed by the DCA whether or not Bit 0 = 1.

The SSI sequence, executed by the DCA, shall be derived from the following IOM functions:

Double Precision data Word (36 bits).
SCM - Store Channel in Memory.
SXC - Set Interrupt Cell Unconditionally.

Refer to the GE-355 EPS-1, 43A219608, Rev. B., paragraph 4.0, for further requirements and detailed information.

3.1.3.3 Instruction Data Control Word (IDCW): (continued)

a) (continued)

. Bit 0 = 0; An SSI shall not occur unless an error is detected for the Field (IDCW).

b) Bit 1; Stop/Continue Bit:

. Bit 1 = 1; Stop:

After processing this field (this IDCW), the DCA shall terminate the data transfer operation. An SSI shall be executed by the DCA.

. Bit 1 = 0; Continue:

After processing this field (this IDCW), the DCA shall fetch the next IDCW and continue unless an error has been detected. If bit 0 is set (1), the DCA shall execute an SSI before the next IDCW in the list is fetched.

c) Bit 2; Next IDCW Specifies a Read or Write:

Timing constraints impose the requirement that the DCA initiate head switching (Read to Write, Write to Read) at the earliest opportunity. Head switching (if any) shall take place in the "all ones" switching area of the gap immediately following the Field specified by the IDCW. Head switching shall begin before the next IDCW is requested from the 355/IOM. Control Software shall recognize that successive IDCW's are related by this (bit) function. Refer to paragraph 3.2.8.4, invalid IDCW sequence status for further details.

. Bit 2 = 1; Next IDCW specifies a Write Operation:

Upon completion of the field specified by the IDCW, the DCA shall initiate a write operation to the selected device. If the DCA is already in the write mode, no head switching shall take place. The next IDCW must specify a Write Command.

B

3.1.3.3 Instruction Data Control Word (IDCW): (continued)

c) (continued)

. Bit 2 = 0; Next IDCW specifies a Read Operation:

Upon completion of the field specified by the IDCW, the DCA shall initiate a read operation to the selected device. If the DCA is already in the read mode, no head switching shall take place.

The next IDCW must specify any one of the following commands; Read, Compare Next Count Field (CNC), Idle, or Compare (data in Key or Data Fields).

d) Bits 3 thru 17; Data Address:

These bits specify the even starting location in 355/Memory for data transfer operations.

The DCA shall save this address, but bit 17 shall be ignored. The DCA shall increment the data address by two after each 36 bit memory access. Key length and data length control the length of the data transfer; Refer to paragraph 3.2.9 and 3.2.10.

e) Bit 18; This is the odd parity bit for command bits 26, 28, 30, 33, 34 & 35.

f) Bits 19 thru 25; Sync Byte for this Field:

These 7 bits contain the bit configuration of the Sync byte (1-7) preceding the field to be read by the IDCW. Refer to paragraph 2.1.2 for the bit configurations necessary for IBM compatible sync bytes. Write and Format commands ignore these 7 bits. Bit 25 shall be the "least significant" bit.

g) Bits 26 thru 28; Valid/Invalid bit Combinations:

Together, these three bits specify the basic operation to be performed by the DCA.

The following bit combinations shall be valid:

. 001 specifies that the DCA shall read a field, but data shall not be transferred to 355/Memory. The data address contained in the IDCW shall be ignored by the DCA.

3.1.3.3 Instruction Data Control Word (IDCW): (continued)

B g) (continued)

- 000 specifies that the DCA shall read a field. Read commands shall transfer data to 355/Memory starting at the location designated by the IDCW.

  However, the Compare Next Count Field (CNC) Command (bit 30 set) is an exception and shall cause the DCA to fetch data from 355/Memory starting at the location designated by the IDCW.

- 010 specifies that the DCA shall Write, or Format, a field. Data shall be transferred from 355/Memory starting at the location designated by the IDCW.

- 011 and Bit 31 together specify that the DCA shall Write (Format) a field, but the DCA shall require 36 bits of information from 355/Memory specifying Gap Length and Field Length. The DCA shall write zeros in the field. Information shall be transferred from the 355/Memory location designated by the IDCW.

- 100 specifies that the DCA shall perform a compare operation between data read from the disc and data in 355/Memory. This comparison operation shall be valid for Key Fields and Data Fields only. The DCA shall implement the compare operation by utilizing the 355/IOM subtract command. In brief, data read from the disc is subtracted (on a 36 bit basis) from data stored in 355/Memory and the result is stored in 355/Memory. Therefore, data in 355/Memory shall be destroyed.

  The data comparison shall start at the location designated by the IDCW.

- 101, 110, 111 specify invalid operations. The DCA shall not check for invalid operations. Therefore, the results of these invalid bit combinations shall be unpredictable.

3.1.3.3 Instruction Data Control Word (IDCW): (continued)

h) Bit 29; Check Character Alert Override:

If bit 29 is set (1), and a check character alert or sync failure is detected, the DCA shall not terminate, but shall request the next IDCW and continue. If the IDCW had the SSI bit set (bit 0 = 1) appropriate status shall be stored in 355/Memory. If the SSI bit was not set, the error status shall not be reset by the next IDCW.

i) Bit 30; Compare Next Count Field (CNC):

If bit 30 is set (1), the IDCW specifies that the DCA shall compare Count or Home Address Field data read from the disk against data stored in 355/Memory. The comparison shall start at the location designated by the IDCW. In performing the comparison, data stored in 355/Memory shall not be altered.

With one exception, the DCA shall automatically assume a field length of 9 bytes (72 data bits). If bit 34 of the PCW is set (1) and the IDCW is the first one requested by the DCA, the DCA shall automatically assume a field length of 5 bytes (40 data bits), implying a Home Address (HA) field.

j) Bit 31; Format This Field:

If bit 31 is set (1), the IDCW specifies that a Format operation shall be performed. The DCA shall request 36 bits of information from 355/Memory defining field length and gap length. The DCA shall remain in the Format mode until index mark is detected. Refer to paragraph 3.4.2.4, Format Operations for further details.

k) Bit 32; Switch ICW's:

The DCA shall provide the ability to alternate between the Primary ICW and the Alternate ICW. If bit 32 is set (1), the DCA shall not switch ICW's until the command specified by the IDCW has been completed. Refer to paragraph 3.1.3.2, ICW, for additional information.

3.1.3.3 Instruction Data Control Word (IDCW): (continued)

B 1) Bit 33, 34, 35; Field Designator Bits:

These three bit positions shall be used to identify the type of field to be processed by the DCA. These bits are mutually exclusive; i.e., only one bit of the three can be set (1) in any IDCW. The DCA shall not provide checking logic to determine if more than one bit is set.

. Bit 33 = 1; Count Field Designator Bit:

The DCA shall perform any additional functions peculiar to Count Field processing.

. Bit 34 = 1; Key Field Designator Bit:

The DCA shall perform any additional functions peculiar to Key Field processing.

. Bit 35 = 1; Data Field Designator Bit:

The DCA shall perform any additional functions peculiar to Data Field processing.

3.1.3.4 DCA Masked State:

a) The selected DCA shall be forced into the masked state by either an IOM fault, or by a one in bit position 23 of the PCW, or an LDEX (00) Initialize command, or a subsystem initialize pulse.

b) If the Masked bit is set by the PCW, any additional information contained in the PCW shall effectively be ignored. Note that List processing cannot take place and an interrupt to the 355 shall not occur.

c) Once the Mask Condition is set, the DCA shall be inhibited from initiating any further communication to the 355/IOM. However, the 355 shall be capable of initiating communications to the DCA. That is; the DCA shall accept, and process CONNECT (with mask bit reset), LDEX, and STEX, commands provided the DCA is not in the "Busy" state.

3.2 DCA REGISTER FUNCTIONS

a) Subsequent paragraphs, as a matter of convenience, use the term "register" to describe "storage Like" functions and discrete functional elements. However, DCA hardware shall be designed to provide the functions only, and the term "register" shall not be construed as restricting design to a specific implementation technique.

b) DCA - Register Features:

Unless otherwise noted, all "registers" shall have the following characteristics:

- The register shall have a unique address, and shall be accessable by Control Software.
- When loading a register, data shall be right-adjusted in the data/function field of the LDEX instruction. All unused bits shall be set to zero by Control Software.
- When "reading" a register, a LDEX/STEX sequence shall be required to transfer the contents of the register into 355 memory.
- Data read by the LDEX/STEX sequence shall be right-adjusted in the 18 bit memory word. Unused (non-applicable) bits shall be undefined and may, or may not, be zero.

3.2.1 Tag Register (4 bits)

B There are 4 time shared "Tag" lines common to all devices connected to a given DFE. Both the Tag register and the File Bus register (para.3.2.2) are required to send information to a device. The Tag register transmits the following information over the tag lines to a "selected" device:

- Cylinder address data is present on the File Bus.
- Head Address data is present on the File Bus.
- Difference address data is present on the File Bus.
- Control Information is present on the File Bus.

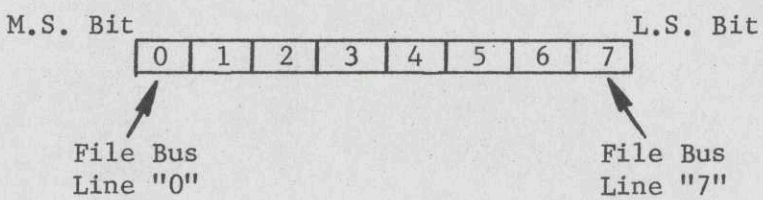
3.2.2 File Bus Register (8 bits)

[B] There are 8 time shared "address/control" Bus lines common to all devices connected to a given DFE. The File Bus register transmits the following information over these lines to a "selected" device:

- Cylinder Address
- Head Address
- Difference Address
- Control Information for the Device

The File Bus Register Format:

The File Bus register shall be organized as follows:



a) Refer to paragraph 3.2.1, Table of Tag and File Bus functions. With a few exceptions, all of the control and data bits contained in the table are set by Control Software. The exceptions are as follows:

- The Write Gate Control Function
- The Erase Gate Control Function
- The Select Head Control Function
- The Read Gate Control Function is normally set by the DCA. Control Software sets this bit when resetting certain Gated Attention conditions only. (See para. 3.2.6.)

3.2.2.1 File Bus Functions: (continued)

ADDRESS AND CONTROL BUS	CONTROL SIGNAL	WHO SETS THE BIT
Bit 5	Head Select; when this line is true, it enables the head for either reading or writing and erasing. The particular head selected is determined by the contents of the head address register.	DCA
Bit 6	Return to Zero; when this line is true, it initiates positioning motion to cylinder zero.	355
Bit 7	Head Advance; when this line is true, it increments the head address register so that the next head in order can be selected. This function can be used to select heads sequentially on a cylinder for multiple track read read or write operations.	355

b) Set Cylinder Tag (line 1);

[B] Refer to paragraph 4.2.4.3 for DFE interface details.

When this line is true, it indicates to the Drive Unit that the lines of the Address and Control Bus now contain positioning information. The positioning information is the Controller's desired cylinder address in binary. Control Software loads the file bus register with the Cylinder number.

c) Set Head Tag (Line 2):

[B] Refer to paragraph 4.2.4.4 for DFE interface details and bit assignments.

When this line is true, it indicates to the Drive Unit that the lines of the Address and Control Bus now contain head select information, and the direction of travel required. Control Software loads the following information and functions into the File Bus Register:

- Head Address
- Direction of Movement
- Reset File Unsafe

3.2.2.1 File Bus Functions: (continued)

d) Set Difference Tag (Line 3):

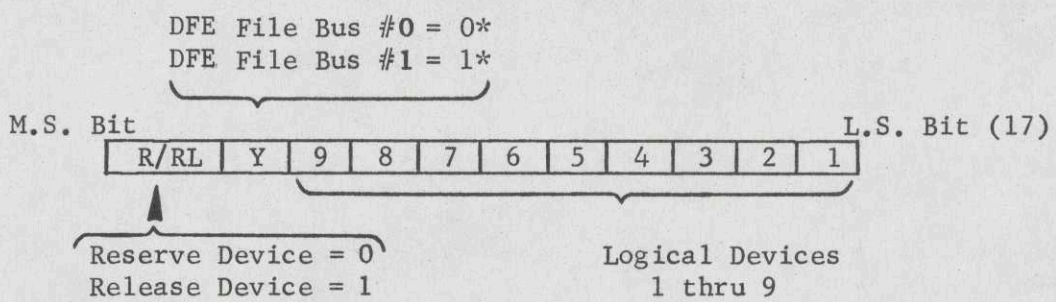
B Refer to paragraph 4.2.4.2 for DFE interface details and bit assignments.

When this line is true it indicates to the Drive Unit that the lines of the Address and Control Bus now contain positioning information. This information consists of a binary number representing the ones complement of the difference between the Drive Unit's current cylinder position and the cylinder address (position) desired by the Controller. Control Software calculates the difference and loads it into the File Bus register.

3.2.3 Device (Module) Select Register (11 bits)

B This register contains the address of the device to be "selected" and the DCA oriented address* of the DFE to be accessed. Control Software shall convert the device address into the register format illustrated.

B



B *NOTE: Only two DFE's can be connected to each DCA. Therefore, Control Software must correlate the DFE "Bank" number with the DCA oriented DFE address. (See para. 2.7)

B

a) When Control Software loads this register, the following events shall occur:

. The Device is "selected".

. The "Selected Device" signal is returned to the "Echo" register.

3.2.3 Device (Module) Select Register (11 bits) (continued)

a) (continued)

- Status for the selected device is returned to the "Device Status" register.
- The current cylinder address (stored in the device by a previous seek operation) is loaded into the "Cylinder Address Bus" register by the device (Refer to para. 3.2.5) provided a "File Unsafe" condition is not present in the device.
- [B] R/RL Bit = 0; the device is reserved to the DFE File Bus (and DCA) designated by Control Software, provided the device was not previously reserved to the alternate channel.
- R/RL Bit = 1; the device is released to the "other" channel immediately.
- If the selected device has been reserved by the "other" channel, access is blocked by the 2 x 1 switch at the device. The Device Status register shall have a bit set indicating "Device Reserved to alternate channel".
- The Device remains selected through all subsequent operations until the contents of this register are changed with another LDEX instruction.
- If the register is set to zero, no devices are selected.

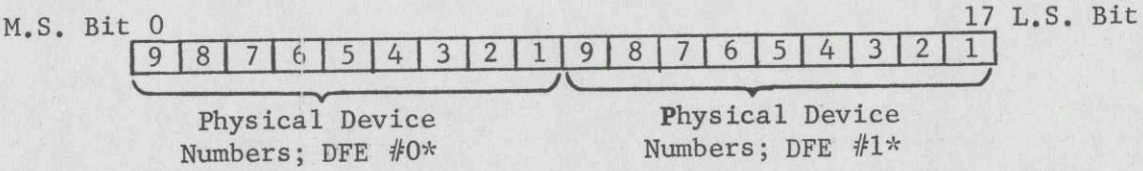
b) Device contains a File Unsafe Condition:

The CAR lines shall load the Cylinder Address register (para. 3.2.5) with additional details defining the cause of the File Unsafe condition. (Refer to paragraph 4.2.5.1.1)

3.2.4 Echo/Selected Device Register (18 bits)

B Nine unique lines are returned from each DFE which identify the physical device selected. The act of loading the Device Select register, (para. 3.2.3) with a logical device number, causes a "selected device" signal to be returned to the "Echo" register. However, the "selected device" line designates a physical device. Therefore, the same device can occupy one bit position in the "Device Select" register, and another bit position in the "Echo" register; both being correct.

B a) Nine lines are returned from each DFE (to the DCA) to physically identify each of nine devices. With two DFE's per DCA, a total of 18 lines are returned to the DCA. The "Echo" register shall be organized as follows:



B

B * NOTE: The DFE # is a DCA oriented number; that is, only two DFE's can be connected to each DCA.

b) Normally, Control Software will not load the "Echo" register but only access it with a LDEX/STEX sequence. However, T&D fault isolation procedures require the ability to load this register with an LDEX instruction sequence directed to each half of the 18 bit register.

c) Control Software shall access this register with a LDEX/STEX sequence. 18 bits of data shall be stored in 355 Memory organized as shown in paragraph (a).

d) Control Software shall determine which of the 9 bit groups (within the 18 bits) are to be checked for error.

e) Control Software shall analyze the data from the Echo register, and determine whether the following conditions exist:

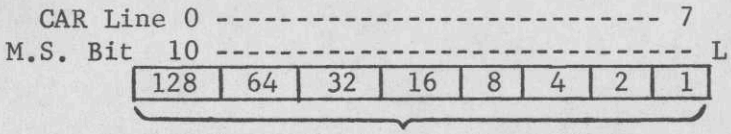
- One, and only one, bit is set; the correct response.
- No bits are set; an error.
- More than one bit is set; an error.

3.2.5 Cylinder Address Bus Register (8 bits)

a) Cylinder Address Bus (CAR) - The 8 lines are time shared between all the devices connected to a DFE. As a result of a "Device Select" (para. 3.2.3), the contents of the Cylinder Address register located in the device, are gated onto the CAR bus, switched through the DCA 1x2 matrix, and loaded into the "Cylinder Address Bus" register of the DCA.

b) The contents of this register shall reflect the last known cylinder position of the device's actuator, provided a File Unsafe condition is not present. Control Software shall use this information to calculate the difference address required for a new seek (see para. 3.4.27, "Seek Operation"for further details). A recalibrate (restore) operation sets a "latch" in the device which inhibits the outputs of the device's Cylinder Address register. The signals on the CAR lines are expected to reflect cylinder zero. If not, Control Software shall be required to interpret the situation.

c) The "Cylinder Address Bus" register shall be organized as follows:



Refer to paragraph 4.2.5.1, Cylinder Address Lines.

d) Normally, Control Software will not load the DCA's Cylinder Address Bus register, but only access it with a LDEX/STEX sequence. However, T&D fault isolation procedures require the ability to load this register from the 355.

e) If the selected device returns a File Unsafe condition, the Cylinder address register shall contain device status which further defines the cause of the file unsafe condition. Refer to Paragraph 4.2.5.1.1 for further details.

3.2.6 Gated Attention Register (18 bits)

B A "Gated Attention" condition originates at the device. Nine unique Gated Attention lines are returned from each DFE for a total of 18 lines to each DCA. Each line designates a logical device, thereby providing the ability to identify the origin of a Gated Attention condition.

A Gated Attention condition can occur at any time, and indicates one or more of the following conditions have occurred.

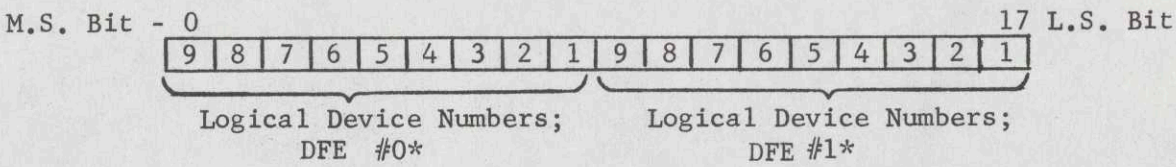
. Seek Complete or Restore (Re-Calibrate) complete;

. Pack Change, or Power turned on at the device, or I.D. plug change;

. Seek Incomplete (actuator failure);

. Device Released. The conditions causing this type of Gated Attention are described in para. 4.2.5.4.

The 18 bit register shall be organized as follows:



B

B * NOTE: The DFE # is a DCA oriented number; that is, only two DFE's can be connected to each DCA.

a) Each logical device sets a unique bit to the 1 state to indicate that a Gated Attention condition occurred. The device number (position) implied by this register is identical to that of the Device (module) Select register.

b) Due to the asynchronous nature of the Gated Attention signal, it is possible for simultaneous Gated Attention conditions to occur.

c) A "Gated Attention" condition does not require an immediate response from Control Software. Therefore, it is anticipated that the register shall accumulate a number of Gated Attention conditions from different devices before Control Software processes the information contained in this register.

3.2.6 Gated Attention Register (18 bits) (continued)

d) "Gated Attention" conditions remain set until Control Software elects to clear the conditions.

e) A "Gated Attention" interrupt shall be sent to Control Software only if the DCA is not busy with a data transfer type command.

3.2.6.1 Processing the Gated Attention Register

355 Control Software shall access this register with a LDEX/STEX sequence. All 18 bits shall be stored in 355 memory at one time.

The most significant 9 bits shall be valid for DFE #0, and the least significant 9 bits for DFE #1. Means shall be provided to load this register from the 355. In order to process a Gated Attention condition, Control Software shall be required to execute the following for each device indicated by the Gated Attention register:

- Select the device (paragraph 3.2.3).
- Access the "Echo" register and check for the proper response (paragraph 3.2.4).
- Access the Device Status register. Analyze the status bits to determine the cause of the Gated Attention (paragraph 3.2.7).
- Clear the Gated Attention condition based on the cause of the condition.

3.2.6.1 Processing the Gated Attention Register (continued)

a) Seek Complete and Restore (Recalibrate) Complete:

In order to clear this type of Gated Attention, Control Software shall execute the following functions:

- Select the Device (para. 3.2.3) which originated the interrupt.
- Load the File Bus register (para. 3.2.2) with bit 1 set to a 1 (Read Gate).
- Load the Tag register (para. 3.2.1) with bit "0" set to a 1 (Control).

b) Pack Change, Device Power Turned On, I.D. Plug Replaced:

Same as paragraph (a).

c) Seek Incomplete:

In order to clear this type of Gated Attention condition, a Restore (recalibrate) command sequence must be issued to the device. Note that another Gated Attention will occur, when the Restore operation is completed.

d) Alternate Channel Release:

A device (module) Select (para. 3.2.3) is sufficient to clear this type of Gated Attention condition.

3.2.7 Device Status Register (10 bits)

A Device (Module) Select must precede interrogation of this register in order for the status conditions to be oriented to the device of interest.

Control Software shall access the Device Status register with a LDEX/STEX sequence. However, T&D fault isolation procedures require the ability to force bit patterns into this register from the 355.

The effective length of this register, when accessed by Control Software shall be 9 bits. B

3.2.7 Device Status Register (10 bits) (continued)

Device Status register information shall be organized as follows:

DEVICE STATUS

0	0	Undefined when accessed by a LDEX/STEX sequence
	0	
	0	
	0	
	0	
	0	
	0	
	0	
8	X	Device reserved to alternate channel
	X	Seek Incomplete
	X	Pack Change
	X	Device Busy Positioning
	X	Alternate Channel desires Control
14	X	Write Current Sense (Error)
	X	End of Cylinder
	X	Device Off-Line
17	X	Device Unsafe

Status conditions represented are as follows:

Bits 0 - 6; Not Used.

Bit 7; Not Used, set to zero.

B Bit 8 = 1; Device Reserved to the Alternate DFE (channel). This condition indicates the device is not available to the DFE selecting the device. When set, all other bits are in an undefined state.

Bit 9 = 1; Seek Incomplete. The actuator mechanism has failed to detent (stop on a track). This is a Gated Attention condition.

3.2.7 Device Status Register (continued)

Bit 10 = 1; Pack Change, (Logical) address plug change, or device power switched on. A discpack is mounted in the device and power has been switched on (again). This is a gated attention condition.

Bit 11 = 1; Device Busy Positioning. The actuator is still in motion. This bit becomes a zero when the device actuator completes a Seek or Restore operation. This is a gated attention condition.

Bit 13 = 1; Alternate Channel Desires Control. Each device is connected to a 2x1 matrix. Possibly different DCA's are connected to each side of the matrix. If one DCA has control of the device, and the "other" DCA attempts to access the same device, then this status bit shall notify the controlling DCA that the device should be released at the earliest opportunity.

Bit 14 = 1; Write Current Sense Error. This status further defines a Drive Unsafe condition. When set, this bit indicates that write current has been sensed by the device. If Control Software detects this bit during a Seek or Restore sequence, Control Software shall terminate the sequence and not access the device again until the failure condition has been corrected.

Bit 15 = 1; End of Cylinder. The head select register, in the device, has counted from 19 to 20 during a multi-track operation.

Bit 16 = 1; Device Off-Line. This bit indicates that the heads are not extended and are not ready to read or write.

Bit 17 = 1; Device Unsafe. No further read, write, erase, seek, or head select operations can be performed on the device. Conditions which cause the file unsafe condition are described in paragraph 4.2.5.2.

3.2.7.1 Device Status Detected by the Control Software

The following device status conditions shall be detected by Control Software.

a) Echo register error (refer to para. 3.2.4).

b) Device Released. Refer to the description of bit 13 in para. 3.2.7.

When the controlling DCA (channel) releases the device, a Gated Attention signal is sent to the DCA which failed to gain control of the device earlier. After selecting the device, Control Software shall access the device status register and expect to find bits 8, 9, 10 and 11 reset to zero. Control Software shall be required to differentiate between Seek Complete (bit 11 = 0) and Device Released.

B 3.2.8 DCA Status Function

B The DCA shall provide the ability to detect different status conditions pertinent to data transfer type operations. Refer to para. 3.3.1 for Status Format.
Status conditions are stored in 355 Memory as the result of an SSI sequence executed by the DCA. Status shall be stored in memory only after a data transfer operation (IDCW) has been completed. Refer to the flow chart of para. 3.1.3.5 for further information on the conditions required for an SSI sequence.

Except where noted, the DCA shall not reset status unless either one of the following events occur:

- An SSI cycle has been successfully completed by the DCA.
- The DCA receives an initialize signal from the IOM.
- The DCA receives a "clear" command (LDEX-Reset).
- The DCA receives a CONNECT while in the masked state.

For a concise table of status conditions, refer to para. 3.4.4 and 3.3.1.

3.2.8.1 Software Sync Bit (Indicator):

Each time an SSI sequence is executed by the DCA, the DCA shall set this status bit to a one (1).

3.2.8.4 Invalid IDCW Sequence: (continued)

c) The previous IDCW specified a "Read Next Field" function, but the IDCW received by the DCA specifies a Write, or Format, operation. The IDCW shall be aborted by the DCA.

d) The previous IDCW specified a "Write Next Field" function, but the IDCW received by the DCA specifies a Read type operation (CNC, Compare K or D, Read, Idle). The IDCW shall be aborted by the DCA.

3.2.8.5* Sync Byte Failure:

This bit shall be set (1) if the sync byte preceding a Key or Data Field does not compare equal to the sync byte contained in the IDCW, and the IDCW specifies a read type operation (Compare K or D, Read, Idle). Commands (IDCW's) specifying Count Field, Write, or Format operations cannot cause this status condition to be set. If detected, the DCA shall process the field regardless of the error (including data transfers to memory).

B 3.2.8.6* Data on Index Mark:

This status bit shall be set (1), if the DCA detects an index mark while writing, or reading, a field on the disc. The Write or
B Read operation shall terminate immediately.

3.2.8.7* Write Current Sense Error:

B This status bit shall be set (1) if write current is not detected during a Write, or Format, command (IDCW). Upon detection of this error, the IDCW shall be aborted immediately.

3.2.8.8* Two Consecutive Index Marks Detected:

While executing a data transfer type command, the DCA detected two consecutive index marks, from the selected device, before the operation was completed. However, Format operations which Write the gap until the index mark is detected, shall not cause this bit to be set. Upon detection of this error, the IDCW shall be aborted immediately.

* See paragraph 3.2.8.18

3.2.8.18 Device/DCA Exception Condition:

Paragraphs marked with an * describe status conditions which cause this status bit to be set (1) also. This status bit provides Control Software with the means to check for pertinent status quickly, when software timing is critical.

With one exception, status conditions which set this bit cause the IDCW list processing sequence to end.

- Exception - If a check character alert or sync failure is detected and the "check character alert override" bit is set (1) in the IDCW.

3.2.8.19 204_{10} (CC) Detected:

This status bit shall be set (1) if a read type operation has been attempted on a discpack written by an IBM 2314 Model 1 subsystem. This status bit shall function as an indicator bit only, and shall not cause an SSI of itself, nor shall it cause the termination of a list of IDCW's. This status is not lost to Control Software because an SSI is required to reset the status condition (Refer to para. 3.2.8) under normal operations.

3.2.8.20 SSI Bit Caused the Interrupt:

This status bit does not indicate an error. The bit provides Control Software with a means to differentiate between an SSI sequence which signals the end of "List Processing" and an SSI which does not.

This bit shall be set (1) under the following conditions:

- Bit 0 of the IDCW was set (SSI specified),
- And bit 1 of the IDCW was not set (Stop not specified),
- And no error conditions occurred which cause "List Processing" to stop.

3.2.8.21 Command Parity Error:

This bit is set if the command bits and the parity bit in the IDCW do not form odd parity. The DCA will stop the data transfer operation immediately and report status.

3.2.9 Key Length Counter (8 bits)

This binary Counter is loaded with the Key Length byte contained in the count field of a sector. In brief, the DCA uses this counter to determine the number of data bytes in a Key field for checking purposes, and to control the length of a data transfer. The counter shall provide the ability to count from 0 to 255 bytes (in binary).

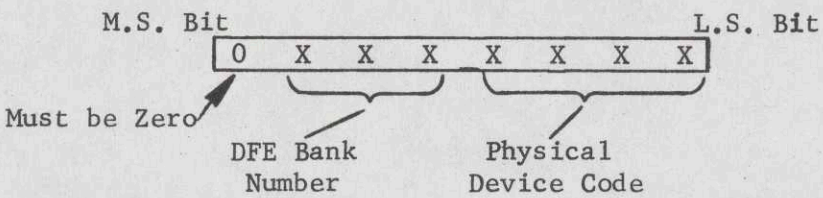
3.2.10 Data Length Counter (16 bits)

This binary counter is loaded with the two data length bytes contained in the Count field of a sector of from Memory for Format commands. All 16 bits shall be theoretically valid for the subsystem.

The contents of this counter shall not be accessible by a LDEX/STEX sequence.

In brief, the DCA uses this counter to determine the number of data bytes in a data field, for checking purposes, and to control the length of a data transfer. Note that the maximum number of data bytes physically possible on a track is limited to 7,403 bytes by the IBM format.

3.2.11.2 Indicator Byte Function (8 bits): (continued)



[B]

[B] . The DFE Bank Number shall be the binary number set by the address switches located in the DFE.

. The Physical Device Code shall be a binary number derived from the contents of the "Echo" register (para. 3.2.4).

a) Format Type Detection Function:

If the "indicator byte" contains a value of 204_{10} (octal 314), then the DCA shall set a status bit in the DCA status register but a data transfer operation shall not terminate.

Furthermore, the "Bit Count" checking logic shall be disabled.

If the "Indicator Byte" contains any other value than 204_{10}, then the "Bit Count" checking logic shall be enabled.

3.2.11.3 Bit Count Checking Function:

Briefly, the Bit Count Byte contains a number related to the number of data bits recorded in the field to which it is appended. Write Operations; The DCA shall generate the Bit Count byte to be written after each field on the disc. Read Operations; the DCA shall regenerate the Bit Count Byte, based on information read from the field, and compare against the Bit Count Byte originally written on the disc.

3.2.12.1 Non-Modulo 36 Data Transfers: (continued)

b) Read Operations

In a similar manner, the DCA shall "left-adjust" data transmitted to 355 memory. The memory map described by the example of paragraph (a) applies equally to a read operation. In this case, the DCA shall supply (fill in) the irrelevant "X" bits. Control Software must read the Count Field of a sector and extract Key length and Data length before it can determine the extent of valid data.

3.2.13 Serialization/Deserialization Register (36 bits)

a) Read; This register converts bit serial data received from the DFE into 36 parallel bits for transfer to the 355. [B]

b) Write; This register converts data, received as 36 parallel bits from the 355, into bit serial data for transfer to the DFE [B]

c) The operation of this register is under the control of the DCA.

d) T&D checking procedures for this register shall be defined by the EPS-2.

3.2.14 Data Buffer Register (36 bits)

This register functions as a data buffer between the Serialization/ Deserialization register and 355 memory. Data transfers across the 355/IOM bus shall be 36 bits, in the "direct" mode. T&D checking procedures for this register shall be defined by the EPS-2.

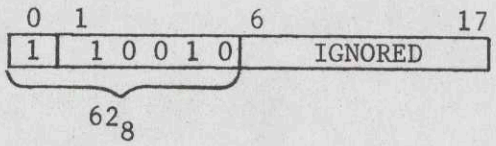
3.2.15 Set T&D Mode Function

A unique command function is provided to cause the DCA to enter a T&D mode of operation. T&D mode shall effectively block communication from the DCA to the DFE, inhibit Gated Attention interrupts from the DFE & enable testing functions directed to the Serialization/Deserialization Register. [B]

A 355/LDEX instruction is utilized to perform this function. The 18 bit memory word sent to the DCA shall be organized as follows:

3.2.15 Set T&D Mode Functions (continued)

a) Set T&D Mode:



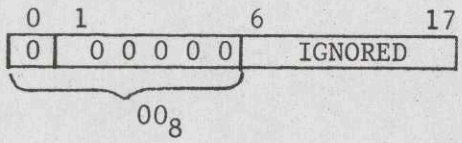
b) The DCA shall accept all commands (LDEX, STEX, CIOC) while in T&D Mode.

3.2.16 Reset the DCA Function

A Unique command function is provided to reset the DCA and send a "clear" signal to the DFE(s).

The 355/LDEX instruction provides the vehicle for implementing this function.

The 18 bit memory word, sent to the DCA, shall be organized as follows:

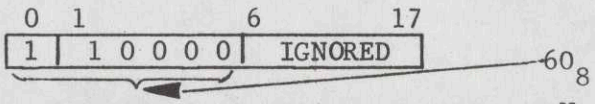


Upon receipt of this command, the DCA shall revert to the initialized (and masked) state.

3.2.17 Simulated Clock Function

A unique command function is provided to cause the Serialization/ Deserialization register to shift once. The function effectively substitutes for the DCA shift clock normally used.

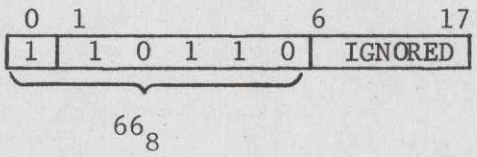
This function is not operable unless the DCA is in T&D mode (see para. 3.2.15). A 355/LDEX instruction is utilized to perform this function. The 18 bit memory word, sent to the DCA, shall be organized as follows:



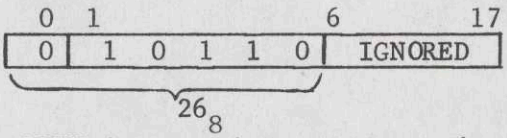
3.2.18 Force Check Character Alert Function (Non-T&D Mode):

A unique command function shall be provided to verify that the check character alert logic is capable of detecting an error during a normal read operation. A 355/LDEX instruction shall be utilized to initiate (or reset) this function. The 18 bit memory word, sent to the DCA, shall be of the following format:

a) To enable the Function:



b) To Reset the Function:



c) The LDEX instruction must precede a Connect Command and the resultant data transfer (read only) operation. During the check character checking sequence of the DCA, the DCA shall transfer the Byte Count into the Cyclic Check register logic; thereby causing a Check Character Alert.

d) Caution: This function shall be enabled when the DCA is in NORMAL mode only.

B 3.2.18.1 Octal 22 & 26, T&D Mode Only:

If T&D mode is set (par. 3.2.16), octal 22 and 26 command codes shall define additional T&D functions. These functions shall be described further in the EPS II.

3.2.20 Address of Hardware Register Functions

The 355 memory word associated with the LDEX instruction contains a 5 bit register address field. (See para. 3.1.1) In addition, a 6th bit determines whether the register shall be loaded or accessed. The following register addresses shall be used:

Register	Load	Unload
MODULE SELECT	41	01
FILE BUS	43	02
TAG	42	02
MEMORY ADDRESS REGISTER	---	03
GAP COUNTER	--	04
SHIFT REGISTER (para. 3.2.13)	--	20
GATED ATTENTION	--	34
SELECTED MODULE	--	35
CYLINDER ADDRESS	--	36
[B] KEY LENGTH COUNTER		36·($\overline{\text{SEL 1+2}}$)*
DEVICE STATUS	--	37

In addition, the following special T&D commands:

COMMAND	Load or Set	Unload, Reset
LDEX Register (T&D)	71	31 Enable to other registers.
LDEX Check Alert	$\overline{\text{T\&D}}$ - 66 (set)	$\overline{\text{T\&D}}$ - 26 (reset)
LDEX Clock	60	--
LDEX T&D Mode	62	22 (reset)
LDEX Reset	00	--
LDEX Status Service (Test SSI function)	T&D - 66	--
LDEX Shift Register Load	T&D - 26	--

[B] *Module Select Register "Reset".

3.3.1 Device/DCA Status (A, A+1)

The DCA executes a "double precision" store status and interrupt (SSI) operation to these locations.

Device Status and DCA Status information is discussed in detail in paragraphs 3.2.7 and 3.2.8.

The following table specifies the format for the 36 bits of termination status:

DCA Status Table:

NOTE: An "X" denotes that the state of the bit is undefined; i.e., a device or DFE address. An "exception condition" causes a bit to be set to a "1". The normal state is zero.

SSI STATUS TABLE

	Location A		Location A+1	
Physical binary address of selected device (from "Echo R.).	2^3 X	0	S/W Sync bit	1 18
	2^2 X		End of File Record	*
	2^1 X		Comparison KorD field error	*
	2^0 X		Invalid IDCW sequence	*
Physical binary address of selected DFE.	2^2 X		Sync Byte failure	*
	2^1 X		Write (Field) on index	*
	2^0 X		Write Current sense error	*
	0	7	2 consecutive index marks detected	*
	0		TRO Terminate (error)	*
	0		Transfer Timing Error	*
	0		ICW address(Primary=0,Second.=1)	28
SSI bit caused interrupt		11	Check Char.Error (K or D Field)	*
Command Parity Error			Check Char. Error (Count Field)	*
Alt.Chann.Desires Con.			Conn/LDEX/STEX received while busy	*
204_{10} (CC) Detected →			DL or KL<KL or DL in memory	
End of Cylinder →	*		Compare Count Field error ⊕	*
Device Off-Line →	*		Record # no compare ⊕	*
Device Unsafe →	*	17	Device/DCA Exception Condition	35

NOTE: ⊕ Mutually exclusive status Conditions.

NOTE: * Status Conditions marked with an * cause bit 35 (Device/DCA exception Condition) to be set.

3.4.2.2 Compare Operations (Key and Data Fields only):

Compare/D and Compare/K commands perform a comparison between data read from the disk and data in 355 memory. An entire field is always compared provided an error is not detected.

The DCA uses the IOM "SDM" (Subtract Channel data from Memory) command. Therefore, successful comparison alters the Data in 355 memory (to zero). If the comparison fails, the DCA shall continue to the end of the field and check the Check Characters before terminating (the list) with an SSI sequence. A unique status bit designates this type of compare failure.

3.4.2.3 Write Operations (Excluding Format):

After receipt of the IDCW, the DCA shall request data for writing the preamble (paragraph 3.3.4) from the fixed (patched) locations in memory. Subsequently, the DCA shall request data from memory beginning at the location specified by the address field of the IDCW. The Key Length and Data Length, read from the Count field by a previous IDCW and stored in the DCA, Control the length of the Data Transfer from memory. The DCA shall generate and append the 4 check bytes (paragraph 2.1.1 subparagraph "1"), to the field.

If the Read/Write Next bit of the IDCW specifies Write Next, the DCA shall continue writing (ones) in the gap area immediately following the field. If the next IDCW does not specify a Write operation the DCA shall SSI and terminate with an error.

If the Read/Write Next bit of the IDCW specifies a Read Next, the DCA shall switch to the Read Mode in the gap area immediately following the field. If the next IDCW does not specify a Read type operation (CNC, Compare K or D, Idle, Read), the DCA shall SSI and terminate with an error.

A check character alert cannot occur as the result of writing a field.

3.4.2.4 Format Operations:

Data for format commands originates at the location specified in the IDCW. The first 36 bits transferred shall contain Gap Length and Field Length in the following format:

3.4.26 Format/K/Write (Format) Next Field

a) Refer to paragraph 3.4.2.4 (Format Operations).

b) Refer to paragraph 3.4.20.b, c (Field, Gap Length, and Zero Data).

c) Refer to paragraph 3.4.18.c (Write/Format Next).

d) Refer to paragraph 3.4.4 (Status/Command Table).

3.4.27 Seek Operation

No time constraint exists; therefore, the sequence consists of LDEX's and STEX's, and performs the following functions:

[B] . The DFE Bank and Device selected and reserved, if possible.

[B] . Device Status is checked; if reserved by the "other" DFE Device bus, the sequence ends here.

. The previous (old) cylinder position is requested by the 355 (cylinder address register contents).

. Control Software calculates the difference between the old (previous) position and the forthcoming position.

. The difference between the old cylinder position and the forthcoming position is sent to the device.

. Control Software sends Forward or Reverse to the device.

. Control Software sends the new seek address (cylinder, head) to the Device.

. Control Software sends a "start actuator motion" command.

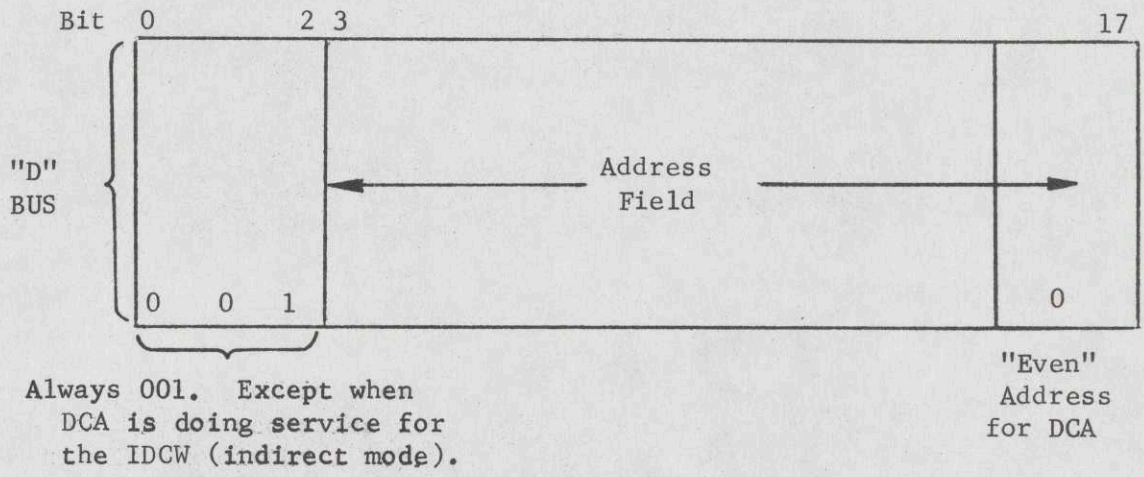
. The Control Software may elect to proceed in any of the following ways:

a) Select another device (de-select this device).

b) Keep the Device selected (a data transfer operation is next).

c) Release the device.

4.1.1.1 General DCA/IOM Command Format (continued)

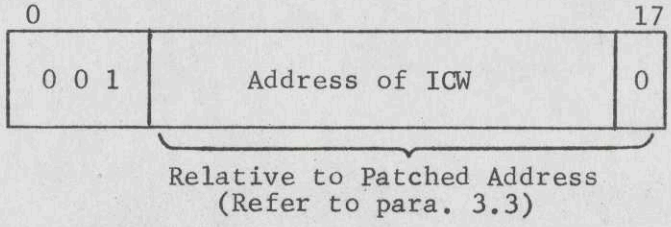


B

4.1.1.2 DCA Commands to IOM (ICW):

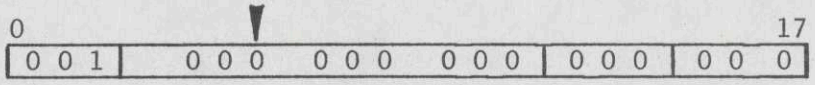
The following command structure is used by the DCA to access the ICW in memory and subsequently receive the IDCW.

"D" Bus (Address of ICW):

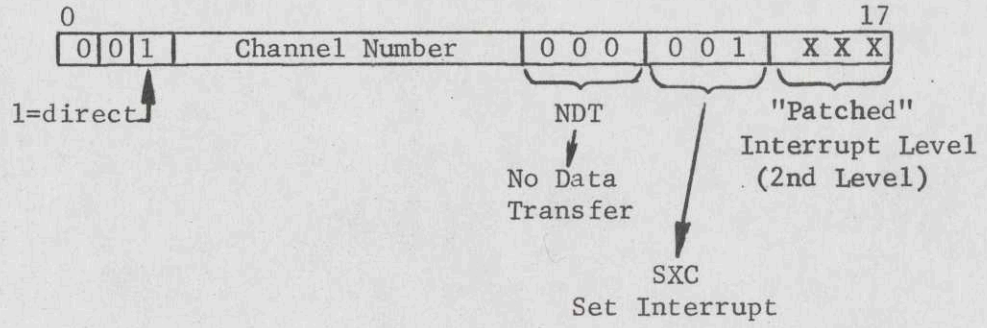


4.1.1.6 Gated Attention Interrupt (2nd Level):

"D" Bus: (Dummy Address)



"C" Bus:



[B] 4.2 DCA MODULE TO DFE 180

4.2.1 Interface Cables

[B] The DCA shall be connected to the DFE 180 via two data/signal cables per DFE Bus. Each DCA shall have electrical interfaces to two DFE Busses. Primary AC power will be distributed from the facility power distribution network and will not be available from the 355 cabinet.

4.2.2 Signal/Data Cable

[B] The signal/data cable will provide the necessary connection between the DCA and the DFE 180. These lines will consist of:

a) IBM device interface lines per the IBM 2312/2313 Disc Storage Drive System Reference Library Manual.

[B] b) Unique lines associated with the operation of the DFE 180.

c) Table 4.2.2 gives the Signal/Data lines with pin assignment to be used for the transmit and receive cables.

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
DEVICE CHANNEL ADAPTER (DCA)

DCA Pin Numbers	RECEIVE CABLE	DAE
33	Cylinder Address Bit 0	
34	Cylinder Address Bit 1	
35	Cylinder Address Bit 2	
36	Cylinder Address Bit 3	
37	Cylinder Address Bit 4	
38	Cylinder Address Bit 5	
39	Cylinder Address Bit 6	
40	Cylinder Address Bit 7	
2	Selected Device 1	
3	Selected Device 2	
4	Selected Device 3	
5	Selected Device 4	
6	Selected Device 5	
7	Selected Device 6	
8	Selected Device 7	
9	Selected Device 8	
10	Selected Device 9	
12	Gated Attention 1	
13	Gated Attention 2	
14	Gated Attention 3	
15	Gated Attention 4	
16	Gated Attention 5	
17	Gated Attention 6	
18	Gated Attention 7	
19	Gated Attention 8	
20	Gated Attention 9	
22	Device Busy	
31	RAC (1) Reserved to Alternate Channel	
24	Index Mark	
25	Write Current Sense	
26	Device Unsafe	
27	Seek Incomplete	
28	On-Line	
23	Pack Change	
29	End of Cylinder	
48	Stripped Clock	
50	Stripped Data	
46	5 MH Clock	
45	Operational In	
30	Alternate Channel Desires Control	
42	DFE Identification 2^0	
43	DFE Identification 2^1	
44	DFE Identification 2^2	

B
B

TABLE 4.2.2 (continued)

4.2.2 Signal/Data Cable (continued)

d) The cable to be used is 43B111147P3 with 50 twisted pairs. The length of the signal/data cable shall be a maximum of 50 ft.

e) The cable will be assembled per drawing 43D219358. The 355 cable connectors will be 43D140801P1. The DFE 180 cable connectors will be 43D140801P3. [B]

4.2.3 Signal/Data Line Characteristics

The signals will have a minimum pulse width of 100 nanoseconds. Logic level state in the inactive or static state will be in its high level or Logic 1 state. A maximum of 9 load gates may be used on the receiving end. Wiring between the connector box and the circuit board shall be twisted pair and not exceed a maximum of 6 feet. The transmitter circuit to be used will be 43B216548. The Receiver circuit will be 43D216547 or equivalent. The ground wire of the twisted pair shall be grounded at both ends except for operational in, operational out and DFE 180 ID lines which complete the circuit back to the transmitting end.

4.2.4 Output Signal/Data Lines

[B] The interface lines from the DCA to the DFE 180include 8 file bus lines, 4 tag lines, 9 module select lines, a device release line, a write data line, a clear line, read/write control lines, and an operational out line. Tag lines shall be used to indicate the type of information present on the file bus lines. The leading edge of the tag line must be delayed a minimum of 100 nanoseconds from the change of state of data on the bus. Data on the bus lines must not change state in the presence of a signal on a tag line and must remain unchanged for 100 nanoseconds following the termination of the tag pulse.

4.2.4.1 File Bus Lines (8):

These 8 time shared lines are used to transmit information as indicated by the tag lines from the DCA to the Device. These lines are also referred to as the "Address and Control Bus" lines. See Section 3.2.2.

4.2.4.5 Set Control Tag Line (1): (continued)

File Bus	Function	Control Tag Pulse Duration
Bit 7	Head Advance (when this line is true, it increments the head address register so that the next head in order can be selected. This function can be used to select heads sequentially on a cylinder for multiple track reading/writing). The minimum time between controller initiated head advance to head select signals shall be no less than 1.6 microseconds.)	Standard

4.2.4.6 Module Select Lines (9):

Nine (9) module select lines (one for each logical device) are controlled by the DCA to select and reserve the device that it wishes to communicate with. Once a selection has been made, the device will be reserved to the selecting channel until the DSC 170/355 controller (See paragraph 3.2.3) issues a release to the same logical device. The controller may also issue a clear (See paragraph 4.2.4.8). The term "module" is used to indicate the variable identy of the device determined by the ID Plug. (Logical Device.)

4.2.4.7 Release (1):

B This line is sent to the DFE 180 to release a reserved device and to reset the Reserved Alternate Channel (RAC) indication. The release line is module selected. The release line must not fall for at least 50 nanoseconds following the termination of the module select.

4.2.4.8 Clear (1)

B The clear line is used by the DCA to return that portion of the DFE 180 associated with that specific DCA to the reset state.

4.2.4.9 Write Data Line (1)

B This line is used to transfer data from the DCA to the DFE 180. It will contain both the data and data clocks to be recorded on the selected drive unit's media. The width of the pulses shall be 100 nanoseconds $\pm$ 10 nanoseconds.

4.2.4.10 Write Control (1):

[B] When this line is true, the DFE 180 shall accept clock and Data from the DCA.

4.2.4.11 Read Control (1):

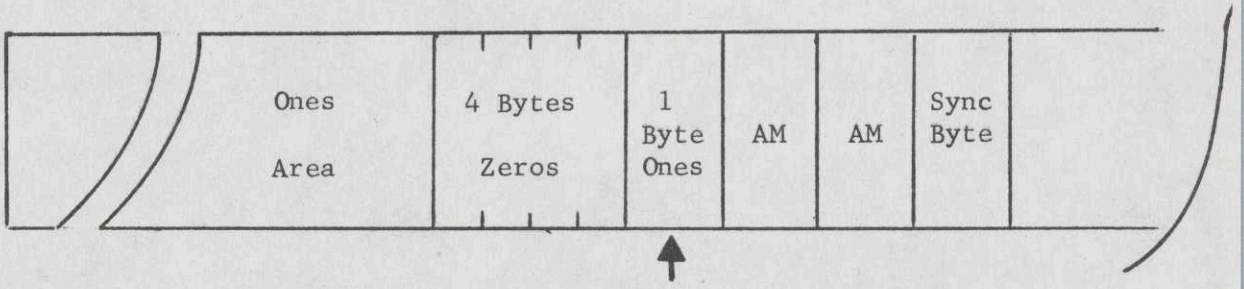
[B] When this line is true, the DFE 180 shall return read data and read clocks to the DCA.

4.2.4.12 Operational Out (1)

[B] An isolated contact at the DCA completes a circuit in the DFE 180. If the DCA contact should open, breaking the circuit, the DFE 180 is then informed that the DCA is no longer operational. The DFE will at such times reinitialize all control f/f and reset all reserve and RAC indications previously set by that channel.

4.2.4.13 Resolution Inhibit (1):

[B] A minimum of two bit times prior to the probable receipt of an address mark byte from the device, the DCA will enable the Resolution Inhibit line. This indication will inhibit the DFE from interchanging information on the clock and data lines to the DCA.



Gap area shown with arrow indicating when Resolution Inhibit goes true (Minimum of 2 bit times prior to possible AM). Normally, RI, will not go false until the end of the data transfer.

4.2.5 Input Signal/Data Lines

The input lines consist of 8 cylinder address lines, one Read Data line, one Read Clock line, one 5 MHz clock, 9 Module, and 9 Gated Attention, and 14 DFE 180/Device status lines. The following is a description of these lines. [B]

4.2.5.1 Cylinder Address Lines (8):

The cylinder address lines indicate to the DCA the cylinder address of the selected drive unit, under normal operation. The bit assignments are as follows:

Cylinder Address Lines	Cylinder Address
Bit 0	CAR 128
Bit 1	CAR 64
Bit 2	CAR 32
Bit 3	CAR 16
Bit 4	CAR 8
Bit 5	CAR 4
Bit 6	CAR 2
Bit 7	CAR 1

4.2.5.1.1 When a file unsafe condition occurs, the unsafe conditions will be automatically returned on the CAR lines:

Cylinder Address Lines	Cylinder Address
Bit 7	Multiple head select.
Bit 6	Read gate and write gate or erase gate.
Bit 5	Erase current and not erase gate.
Bit 4	Write gate and not seek ready.
Bit 3	Erase gate and not seek ready.
Bit 2	DC write current and not write gate.
Bit 1	Write gate and not AC write transitions.
Bit 0	Write gate and not erase current.

The file UNSAFE latches will be reset with a MOD Select and SET HEAD tag and File Bus 1 (select lock reset) and Index Mark.

4.2.5.2 Device Unsafe (1):

This line indicates to the DCA that the device selected has one or more of several faults. The following conditions in a device shall cause an UNSAFE signal.

1) Multiple Head Select
2) Write Gate and Not Seek Ready
3) Erase Gate and not Seek Ready
4) DC write Current and not Write Gate
5) Erase Current and not Erase Gate
6) Write Gate and not Erase Current
7) Write Gate and no AC Write Current Transitions
8) Read Gate and either Write Gate or Erase Gate
9) Loss of +5, +3, -3, -36, or +36V DC
10) Loss primary AC power

The first eight conditions are returned on the CAR lines and can be Reset. See paragraph 4.2.5.1 and 4.2.4.4.

4.2.5.3 Selected Device (9):

These lines are returned to the DCA to indicate that one of 9 drive units has been selected. These lines are physically oriented, one per switch/device. They do not indicate logical device numbers. The term "device" is used to indicate a single DSU 180 Physical Device unit. This same DSU 180 is sometimes referred to as the "Drive Unit". B

4.2.5.4 Gated Attention (9):

These lines indicate that a drive module has had one of the following take place:

1) Pack change, coming on line, ID Plug change

2) Seek completed, or restore (seek ready)

3) 600 ms has passed since the seek command was given but no detent was detected (seek incomplete)

4.2.5.4 Gated Attention (9): (continued)

Gated Attention lines can also indicate that a device is now available to the DCA because the following has occurred at the DFE 180. [B]

If a module is reserved or selected by DCA "A" and DCA "B" attempts to select the same module, a Reserved to Alternate channel indication is sent to DCA "B". Then, when DCA "A" released the module, a gated attention is sent by the DFE 180 to DCA "B". [B]

If neither DCA has a module reserved or selected and a gated attention comes from the module, it is issued to both DCA's. If a DCA has a module reserved or selected and a gated attention comes from the module, it is sent only to the DCA which had reserved or selected the module.

NOTE: The Gated Attention line is not module selected. The Gated Attention line is logically oriented as determined by the ID plug.

4.2.5.5 Pack Change (1):

This line indicates to the DCA that a pack change (power on sequence or top cover opened) has taken place and/or the ID plug has been changed. This line is module selected. Each channel will receive an independent indication of pack change and will be responsible for resetting its own pack change indication. The device Pack Change indication will be reset by Set Control Tag and File Bus Bit 1 set (Read Gate). The independent channel indications will be reset by MOD Select and Read Control from the channel.

4.2.5.6 Seek Incomplete(1):

When this line is true, it indicates that the device was unable to complete a Seek operation. A Return to Zero command (Restore) sent to the unit indicating a Seek Error will clear the Seek Error condition, return the heads to cylinder zero and cause a Gated Attention to be sent to the DCA.

4.2.5.7 Device Busy (1):

This line indicates to the DCA that the access mechanism in the selected device is in the seeking process.

4.2.5.8 Index (1):

This line indicates to the DCA that the physical beginning of a track in the selected device is now under the read/write head.

4.2.5.9 Write Current Sense (1):

This line indicates that the selected device is drawing AC write current.

4.2.5.10 On Line (1):

This line indicates that the selected device is available.

4.2.5.11 End of Cylinder (1):

This line becomes true when the head address register goes from 19 to 20 as it is incremented in a multitrack operation requiring the use of sequential head addresses.

4.2.5.12 Alternate Channel Desires Control (1):

This line becomes true on a channel when a device is reserved to that channel and the other channel attempts to select the reserved device. It shall remain true as long as the select line on the reserving channel is true, and the other channel is in the reserved to Alternate Channel state.

4.2.5.13 Reserved to Alternate Channel (1):

This line is returned true when a channel attempts to select a device which is reserved to the alternate channel. It shall remain true as long as the other channel reserves the device and the select line on the requesting channel remains true.

4.2.5.14 5MHz Clock (1):

B This line is used to send the signal from the 5 MHz oscillator in the DFE 180 to the DCA. The 5 MHz write pulse frequency shall be 5.0 MHz $\pm$ 0.05%. The width of the Write pulses shall be 100 ns $\pm$ 10 ns.

4.2.5.15 Stripped Clock (1):

This line is to contain only the clocks from the device with the data stripped out. This clock shall be 2.50 MHz $\pm$ 4.1% with a width of 100 ns $\pm$ 20 ns.

4.2.5.16 Stripped Data (1):

This line is to contain only the data from the device with the clocks stripped out. These data pulses will have a maximum (all 1's) rate of 2.50 MHz $\pm$ 4.1%. Data pulses shall have a pulse width of 100 ns $\pm$ 20 ns.

4.2.5.17 Operational In (1):

[B] An isolated contact at the DFE 180 completes a circuit in the DCA. If the contact should open, the DCA is informed that the DFE is no longer operational.

[B] 4.2.5.18 DFE 180 Identification Lines (3):

[B] The Physical DFE number is coded in binary on these three lines from the DFE 180.