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655 System Controller

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NOTE:

The engineering expressions "GE-655" and "655" are used throughout this document. They are equivalent to the contemporary expressions "6000 Line" and "6000".

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1.0 GENERAL DESCRIPTION

1.1 SCOPE

This specification defines the functional and operational requirements for the 6000 Line System Controller. In general, these requirements shall be equivalent in function, and compatible with, 600 Line needs as well; but shall not be limited to only those functions and capabilities defined for 600 Line Systems.

The capability to interface with G-635 system modules (Processor, IOC, Core Storage System) shall be provided; and will be accomplished by the use of port board options in the System Controller.

Capabilities required to function with H-6000B Systems shall be provided also.

The main body of this EPS-1 specifies 6000 Line requirements. Wherever the needs of 600 Line and H-6000B Systems are known to differ from (or conflict with) each other or standard 6000 Line needs, the function or capability shall be specified separately (as an exception) in Appendix B (600 Line needs) or Appendix C (H-6000B needs).

The capability to function with 600 Line Systems and H-6000B Systems does not imply a single model H-6000 System Controller. It need not be convertable (via customer "options") from one application to another. Rather, two basic versions (or models) are permitted by this EPS-1:

- An H-6000/H-6000B version.
- An H-6000/600 Line version.

1.2 APPLICABLE DOCUMENTS

The following documents of the issue in effect on the issue date of this specification, except as otherwise noted and controlled on an individual basis form a part of this specification to the extent specified herein.

1.2.1 Specifications

43A219600	EPS-1	GE-655 System
43A219601	EPS-1	GE-655 Processor
43A219603	EPS-1	6000/655 Core Storage Unit
43A219604	EPS-1	GE-655 Input/Output Multiplexer (IOM)
43A219614	EPS-1	GE-355 Intercomputer Channel
43A219617	EPS-1	GE-655 Maintainability Design
43A140648	PPS	GE-635 Memory Module
43A143120	PDS	GE-625/635 Memory Controller
43A174410		Interface Specification, 635 Memory Controller
M50EB00621	EPS	GE-615, 625/635, 635B Processors
M50EB00163	EPS	GE-635 Input/Output Controller (IOC-C)
43A177851	EPS-1	General Design Requirements for GE-655 and GE-355 Systems

1.2.2 Standards

Information Systems Group Standard No. 1.2.01, Information Processing Terminology.

IFIP-ICC Vocabulary of Information Processing, North Holland.

MIL STD 781B, Reliability Test, Exponential Distribution.

2.0 FUNCTIONAL CAPABILITIES

The H-6000 System Controller serves as the overall system coordinating control unit. It provides intra-system communcation between high speed core storage and the active modules (processors, input/output modules, inter-computer adapter, etc.).

The System Controller has neither program execution nor arithmetic capability, but acts as a passive system component. It serves the active system modules which call upon the System Controller to save or retrieve information, or to communicate with other system components.

Systems with more than one system controller provide additional effective information rate, since each system controller operates independently and its functions can be overlapped with those of other system controllers.

In addition to the capabilities specified in this section, the System Controller shall implement the capabilities to provide the customer software and hardware interfaces specified in Sections 3 and 4, and Appendix B and C.

2.1 STORE UNITS

The 6000 Line System Controller is a separate module, and provides connection to the following categories of storage units:

Category 1; 1 or 2 655/6000 core store units, or

Category 2; 1 or 2 6000 Line Semiconductor store units.

However, category 1 and 2 Store Units can be mixed on the same System Controller provided, the interface signals and timing are the same for the two Store Units (except for the "refresh" signals). When two store units are used, the 655 System Controller provides for interlacing of addresses and overlapping of cycles in the two units. Two store units with 500 nanosecond cycle times and on 10-foot cables permit accesses to alternate stores at intervals of 270 nanoseconds at the system controller ports.

2.2 SYSTEM PORTS

All ports for connection to 6000 Line active modules are optional. The maximum total number of ports is eight. The eight ports have "wired-in" positional priority in the order of their number (0...7); the lowest number has the highest priority. Thus simultaneous requests are serviced in a predetermined manner that is established by the order in which the active system modules are connected to the system controller. This priority can be modified by the Cyclic Priority switches on the Configuration Panel (Anti-Hog Switches).

2.3 PROGRAM INTERRUPT CELLS

The H-6000 System Controller provides 32 program interrupt cells. Program interrupt cells are set by active modules, such as I/O modules, to cause processor modules to be informed of some event.

2.4 PROGRAM INTERRUPT MASK REGISTERS

Four program interrupt mask registers are provided in the 655 System Controller. These mask registers can be assigned to any of the eight ports, and enable or inhibit the indication of program interrupts to the active module connected to the port. The assignment is made by configuration switches. Each mask register provides one bit corresponding to each of the program interrupt cells in the system controller. The assignment of a mask register to a system port designates it as a control port. Thus XIP (interrupt present) signals can exist simultaneously on multiple ports.

2.5 DATA PATH WIDTH

The data path width in the 6000 Line system is 72 bits plus two data parity bits. Transmission is via bi-directional buses. All accesses to storage are 72 bits wide with 72 bit transmission in parallel. 72 bits correspond to two instructions, two data words, or one double-precision fixed or floating point number. 36 bits may be accessed using single precision commands.

2.6 ELAPSED TIME CLOCK (ETC)

An elapsed time clock is provided in each system controller, read by the processor RSCR instruction and selected by its address field. The address field of the RSCR instruction may specify any of the processor ports, and hence the system controller, to be read. However, the operating system will normally only refer to the clock associated with the control store (zero address). Thus, the zero address could be the default condition provided by GMAP. The operating system therefore has available a common clock in multiprocessor systems.

Standard ETC

The System Controller shall contain a 52 bit elapsed time clock which has a 1 MHZ source oscillator frequency. The ETC increments every one microsecond and "rollover" is 142 years. The most significant 36 bits of the clock (bits 20 thru 55) shall be settable from the maintenance panel, with the design including the necessary safeguards to prevent accidental setting. The least significant bit shall be data bit 71 while the most significant bit shall be data bit 20 (See para. 3.4.13.5)

The clock shall be readable via the Processor Read System Controller Registers (RSCR) instruction with an address field of 4X octal, (para. 3.4.13).

Non-Standard ETC

Early System Controllers contain a 36 bit ETC which has a 1 MHZ source oscillator and a "rollover" every 19 hours. This ETC is not settable. The least significant bit is data bit "71" and the most significant bit is data bit "36". Bits 0-35 are forced to zero. Identical procedures are used to read this ETC and the aforementioned standard ETC.

Both Types Acceptable:

Both types of ETC are acceptable to this EPS-1. The standard 52 bit ETC shall be implemented at the earliest opportunity consistent with engineering and manufacturing schedules. System Controllers with the earlier 36 bit ETC, shall not be retrofitted except in one area; the original 512KHZ oscillator shall be changed to a 1MHZ oscillator.

2.7 OPTIONS

The following options shall be provided on the 655 System Controller. The major unit includes 32 program interrupt cells, no system ports and no store ports.

2.7.1 Store Sizes

Store sizes of 32K, 64K, 128K and 256K (36 bit) words may be attached to either store port. Sizes may be mixed (but not cycle times) on the two store ports of one system controller but the total on one system controller may not exceed 256K. (K = 1024 words.) When address interlacing by the system controller is selected (configuration switches), the store units must be of equal size.

2.7.2 Store Port Options:

655/6000 Store Units may be interfaced with the H-6000 System Controller using the following store port card options. Inter-module cable lengths are specified in the System EPS-1, 43A219600.

Option

#1 One 655/655 Store Port - consists of one pluggable 12" x 12" circuit board. (1st port)

#2 Same as #1 (2nd port)

A maximum of two store ports may be specified.

2.7.3 System Port Options:

H-6000 system active modules can interface with the 655 System controller using the system port card options listed below. Inter-module cable lengths are specified in the System EPS-1, 43A219600.
Options:

#5 655/655 System Port - consists of one pluggable 12" x 12" circuit board. (1st port)

#6 Same as #5 (2nd port)

#7 Same as #5 (3rd port)

#8 Same as #5 (4th port)

#9 Same as #5 (5th port)

#10 Same as #5 (6th port)

#11 Same as #5 (7th port)

#12 Same as #5 (8th port)

A maximum total of eight system ports may be specified.

2.7.4 635 Core Store Parity

Deleted from this section. Refer to Appendix B, paragraph B.2.7.4.

2.8 ADDRESSING

The number of bits used from the address lines depends on the size of the larger storage unit (or either storage unit for equal sizes). Bits representing powers of two larger than this size are ignored (except for parity). For example, if the larger storage unit is 64K, bit 0 is ignored; for two 32K units, bit 0 and 1 are ignored, etc.

3.0 SOFTWARE AND CUSTOMER INTERFACE REQUIREMENTS

The communication between the System Controller and the software is through the program interrupt cells, the illegal action codes, the connect, and commands to the system controller. Otherwise, the System Controller module is passive with no arithmetic or program execution capability.

The customer interfaces with the system controller are as follows:

- Notification of faults through his software.
- Program initiated commands which cause system controller actions.
- Configuration control of the system.
- Initialization of the system hardware.
- Use of maintenance aids.

3.1 CONFIGURATION CONTROL

[E] The configuration of the System Controller is determined by the settings of the following switches.

1. Mode, Store A and B
2. Size, Store A and B
3. Lower Store
4. Address Offset
5. Interlace
6. Execute Interrupt Mask Assignment (A, B, C and D)
7. Port Enable
8. Cycle Port Priority

The System Controller Configuration Panel shall contain these switches.

The settings of the switches shall be visible without opening the cabinet doors; this may be accomplished with remote indicators. Thus, the operator shall be able to determine the system configuration from one position without having to walk around cabinets or open doors.

— The functions of these switches are described in the following sections.

3.1.1 Mode Switches, Store A and B

There are two Mode switches, one for each of the two core store ports. The function of each of the three positions is as follows:

- o ON LINE — Normal operating position.
- o MAINT — Not accessible to ports but can be accessed by the System Controller test logic.
- o OFF LINE — Not accessible to System Controller. This position effectively removes the store from the system.

3.1.2 Size Switches, Store A and B

a) There are two size switches, one for each of the two core store ports. The roles of the two switches depend on the setting of the Lower Store switch. Reversing the setting of the Lower Store switch reverses the role of the size switches.

The roles are as follows:

- o The size switch associated with the lower store establishes the boundary for selection between store ports (see Section 3.2).
- o Both size switches outputs are combined to establish the boundary for the non-existent address illegal action (see Section 3.2).

b) The four positions of the Address Boundary switches are 32K, 64K, 128K and 256K where K = 1024 words.

c) If stores A and B are not equal in size, the larger store must be assigned the lower address range.

d) Multiple System Controller configurations with only one Store Unit on each SCU are permitted; but if Store Unit sizes are unequal, the larger store must be assigned the lower address range.

3.1.3 Lower Store Switch

The Lower Store Switch selects the store port to which the lower addresses (may or may not include system zero address) are routed.

Note that in configurations containing multiple System Controllers, each with only one Store Unit, both store ports require the "Lower Store" switch to be set.

3.1.6 Execute Interrupt Mask Assignment Switches (A, B, C, D) (continued)

Assignment of a mask register to a system port designates that port as a control port. Thus, interrupt present signals will be directed to all ports with mask registers assigned.

3.1.7 Port Mask Switches

These are three position switches.

There are eight switches, one for each of the eight system ports. The three positions are ON, program control, and OFF. In the ON (or OFF) position, the port will communicate (or not communicate) with an active module regardless of the associated mask bit. In the program control position, the port communication is turned on or off by the associated bit in the program controlled Port Mask register.

3.1.8 Cycle Port Priority Switches

In a multiprocessor system, the Cycle Port Priority Switches are used to group like modules (such as processors) to assure equal access to storage on the same system controller. The switches provided are as follows:

Cycle Port Priority Switch	Ports Linked
1	0 and 1
2	1 and 2
3	2 and 3
4	3 and 4
5	4 and 5
6	5 and 6
7	6 and 7

Thus, turning adjacent switches ON causes system ports to be linked so as to form groups. System ports within a group have equal access to storage. The maximum number of ports within one grouping of cyclic priority is five. The operation within a group is such that no system port may have two consecutive accesses to storage after another port has requested access.* In the case of continuous access requests from all ports within a group, access is granted in cyclic order starting with the highest priority (lowest numbered) system port.

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*Note: Unless a Read/Lock-SP command has been received; refer to para. 3.4.15 for conditions which might allow successive accesses by one port to occur.

3.1.8 Cycle Port Priority Switches (continued)

Between groups, access requests by the higher priority group must all be satisfied before any access requests by a lower priority group are acknowledged.

If requests from a higher priority group are received while a lower priority group is being serviced, the lower priority group service stops, and the higher priority group requests are serviced. The system controller stores the information necessary to return to the lower priority group after the higher priority group is serviced.

3.2 STORE PORT SELECTION

The following sections describe the logic for store port selection including address interlacing and non-existent address detection. The configuration switches which control these functions in the system controller are as follows:

- Address Boundary Switches (Section 3.1.2)
- Lower Address Store Switch (Section 3.1.3)
- Interlace OFF/ON (Section 3.1.5)

3.2.1 Configurations with Address Interlacing

Note: See also paragraph 2.7.1.

In an all 655 system, address interlacing may be between store units and/or system controllers. Interlacing may be obtained from either the 655 System Controllers alone, the 655 active modules alone, or both the 655 System Controllers and active modules.

The 655 System Controller interlaces on bit 16 while the 655 active modules interlace on bit 15.

3.2.2 Interlace Equation and Address Map

The interlacing method of the 655 System Controller alone is described as follows. When two storage systems are connected to a controller, they can be operated either phased or non-phased, as selected by the configuration panel INTERLACE switch. The bit compare algorithm (same as the G -645) is used in the system controller. When interlacing is ON, bit 16 of the address

3.2.2 Interlace Equation and Address Map (Continued)

The map of logical addresses in physical address space is as follows. M = store module size. Store A has the lower addresses (less than M).

Physical Address	Store A	Store B
0/1	0/1	M+0/1
2/3	M+2/3	2/3
4/5	4/5	M+4/5
⋮	⋮	⋮
M-4/3	M-4/3	2M-4/3
M-2/1	2M-2/1	M-2/1

3.2.3 Non-Existent Address Detection

The non-existent address illegal action in the system controller is based on the settings of the two Address Boundary switches. The Boolean equation for the non-existent address indication is as follows:

$$NEA = (Z_{32A}Z_{64B} + Z_{32B}Z_{64A})\, A_1A_2 + (Z_{32A}Z_{128B} + Z_{32B}Z_{128A})(A_0A_2 + A_0A_1) + (Z_{64A}Z_{128B} + Z_{128A}Z_{64B})\, A_0A_1$$

The symbols are defined in the previous section (3.2.2).

The NEA (non-existent address) detection in the system controller complements the NEA function in the active modules. It essentially covers the "holes" in address space between the sum of the Address Boundary switch settings and the next higher power of two sizes.

3.3 INITIALIZATION AND BOOT LOAD

3.3.1 635 Initialization

Deleted from this section. Refer to Appendix B, paragraph B.3.3.1.

3.3.2 H-6000 Initialization and Boot Load

The initialization and "boot load" logic for an "all 6000" system is specified and controlled by the 655 System EPS-1. The following description is included for information purposes.

The system controller will initialize itself when power turns on, but will not send out initialize signals through the system ports. However, the system ports of operating active modules, connected to a system controller during power-on or off, should be disabled to protect against transients.

The initialized state of the H-6000 System Controller is as follows:

a) Ready to execute a command.

b) Port Mask Bits (see also para 3.1.7):

1) Early Model System Controllers:

All Port Mask access enable bits set to zero (port disabled) if the Port Mask (Enable) switch is in the OFF or "Program Control" position. In the ON position, the port is forced to the enabled condition (one).

2) Later model System Controllers:

All Port Mask access enable bits set to one (port enabled) if the Port Mask (Enable) switch is in the ON or "Program Control" position. In the OFF position, the port is forced to the disabled condition (zero). Early model System Controllers shall not be retrofitted to conform to this paragraph.

c) All Execute (program) Interrupt cells are set to zeros.

d) All Execute (program) Interrupt Mask enable bits are set to ones (interrupts enabled).

Upon receipt of the Initialize Request signal from any enabled system port, the H-6000 System Controller will initialize itself and send the Initialize signal out all system ports not disabled by the Port Enable switch OFF.

The system controller will not send out the initialize signal when the Initialize button on the system controller maintenance panel is pushed.

3.4 SYSTEM CONTROLLER COMMANDS

The commands to the system controller through the system ports result from active modules fetching and storing information from/to the store units. Active modules may also signal each other through the system controller (for example, connects and program interrupts). The commands are encoded on the command lines by the active module and presented to the system port along with addresses, data, control pulses as appropriate.

The commands are described in the following sections. The following symbols and terms used in the command descriptions are defined as follows:

Y = the absolute effective address received by the system controller through a system port.

C(Y) = contents of the storage location specified by Y.

Basic data lines transmit bits 0 to 35.

Extended data lines transmit bits 36 to 71.

3.4.1 Read/Restore, Single Precision (RRS,SP) 00000

The C(Y) are sent to the requesting system port on the basic data lines. The C(Y) in storage are not altered. The word is selected using bit 0-17 of the address Y.

3.4.2 Read/Restore, Double Precision (RRS,DP) 00010

The C(Y pair) are sent to the requesting system port on the basic and extended data lines. The C(Y pair) in storage are not altered. The Y pair is selected by bits 0-16 of the address Y. Bit 17 of the address is not used.

3.4.3 Clear/Write, Single Precision (CWR,SP) 01000

The C(Y) are replaced by the data on the basic data lines from the requesting system port. The character positions to be written are specified by the zone lines. All one's specifies the entire word. Characters are specified by the codes shown in Section 4.1.1.2. Bits 0-17 of the address Y specify the word in storage to be altered.

TABLE 3-1

H-6000 AND G-635 SYSTEM CONTROLLER COMMANDS

OCTAL CODE	COMMAND LINES A	B	C	D	E/P	Note (1)	CMD FROM 6000 ACTIVE PORT	$CMD TO H6000 STORE	CMD FROM 600 ACTIVE PORT
00	0	0	0	0	0	0	RRS,SP	$RRS	RRS,SP
02	0	0	0	0	1	0	(Not used)	-	RRS,SP
04	0	0	0	1	0	0	RRS,DP	$RRS	RRS,DP
06	0	0	0	1	1	0	(Not used)	-	RRS,DP
10	0	0	1	0	0	0	RCL,SP	$RCL	(Not used)
12	0	0	1	0	1	0	RMSK,SP	$RRS (3)	RMSK
16	0	0	1	1	1	0	RMSK,DP	$RRS (3)	(Not used)
20	0	1	0	0	0	0	CWR,SP	$CW1	CWR,SP
22	0	1	0	0	1	0	(Not used)	-	CWR,SP
24	0	1	0	1	0	0	CWR,DP	$CW2	CWR,DP
26	0	1	0	1	1	0	(Not used)	-	CWR,DP
32	0	1	1	0	1	0	SMSK,SP	$RRS (3)	SMSK
36	0	1	1	1	1	0	SMSK,DP	$RRS (3)	(Not used)
40	1	0	0	0	0	0	RDLK,SP (2)	$RRS	RAR
42	1	0	0	0	1	0	(Not used)	-	RAR
54	1	0	1	1	0	0	RGR	$RRS (3)	(Not used)
56	1	0	1	1	1	0	SGR	$RRS (3)	(Not used)
60	1	1	0	0	0	0	WULK,SP (2)	$CW1	(Not used)
62	1	1	0	0	1	0	CON	$RRS (3)	CON
66	1	1	0	1	1	0	XEC	$RRS (3)	XEC
72	1	1	1	0	1	0	SXC	$RRS (3)	SXC

Notes: Octal command codes 14, 30, 34, 64, 70, 74, 76 are not used by either the 655 or 635 System Controllers.

CMD = command, SP = Single Precision, DP = Double Precision

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(1) This command bit has no line and is not transmittable. It is always zero and is included as a conceptual compatibility aid with 655 and 635 active modules.

(2) Not available with, or applicable to, early 6000 Line active Port Options.

(3) Sent to Storage Unit for timing purposes only. Functional for RGR and SGR only if these commands directed to Storage Unit.

3.4.4 Clear/Write, Double Precision (CWR,DP) 01010

The C(Y pair) are replaced by the data on the basic and extended data lines from the requesting system port. Bits 0-16 of the address Y (Bit 17 is not used) specify the word pair in storage to be altered.

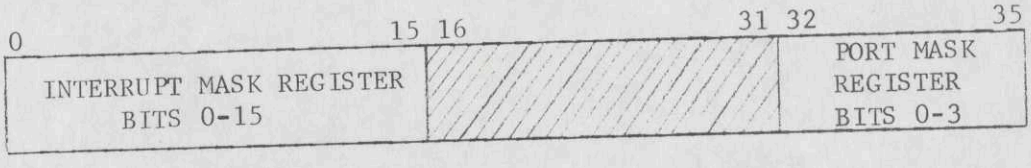
3.4.5 Read/Clear, Single Precision (RCL,SP) 00100

The C(Y) are sent to the requesting system port on the basic data lines, and the C(Y) are restored as zeros. Bits 0-17 of the address Y specify the word in storage to be accessed and altered.

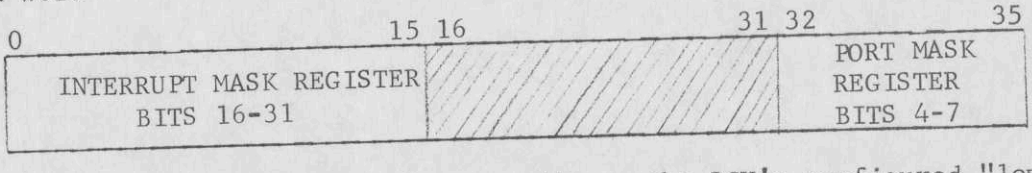
3.4.6 Read Interrupt and Port Mask Register, Single Precision (RMSK,SP) 00101

These registers are physically located within the System Controller. The contents of the Program Interrupt Mask Register assigned to the port and the Port Mask Register are read in the following format:*

Even Word



Odd Word



The address field (ZAC lines) must address the SCU's configured "lower" Storage Unit. The address LSB (bit 17=0 for even, bit 17=1 for odd) selects the even or odd enable word. The basic data lines are used to transfer the information.

There is only one Port Mask Register per system controller. It forms part of each Program Interrupt Mask Register for both loading and reading. The bits in the Port Mask Register may be overridden by the Port Mask Switches, hence the Port Mask bits returned by this command do not necessarily represent the actual state of the system port.

3.4.7 Read Interrupt and Port Mask Registers, Double Precision (RMSK,DP) 00111

This command is the same as the RMSK,SP command except that all mask bits are transferred using both the basic and extended data lines.*

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*Note: A port, which does not have an interrupt mask register assigned to it and which attempts an RMSK-SP or DP, will receive zeros in the data field.

3.4.8 Set Interrupt and Port Mask Registers, Single Precision (SMSK,SP) 01101

This command is the inverse of the RMSK,SP command. The bits of half of the Interrupt and Port Mask Registers are set per the format shown for the RMSK, SP command. The address field (ZAC lines) must address the System Controller's configured "lower" Storage Unit.

A program interrupt mask register must be assigned by the configuration panel switches to the system port attempting the SMSK command or a Not Control illegal action will be signaled.

3.4.9 Set Interrupt and Port Mask Registers, Double Precision (SMSK,DP) 01111

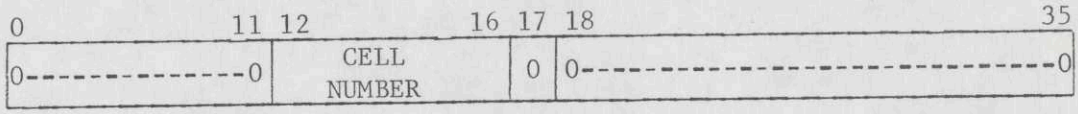
This command is the same as the SMSK,SP command except that both halves of the mask registers are set.

3.4.10 Read Program Interrupt Cells (XEC) 11011

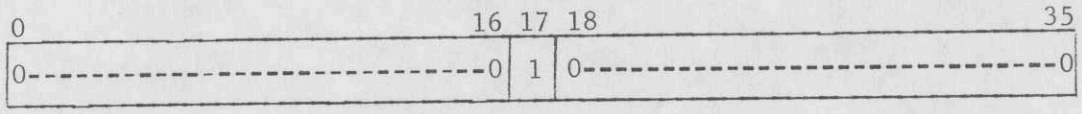
The XEC command is a single precision operation.

The XEC command is used by active modules to Read/Execute a System Controller "program (execute) interrupt cell" (i.e., bit). See also para. 3.4.11, SXC.

Each program (execute) interrupt cell (each bit position) has a hard-wired cell number (address code) associated with it. The System Controller responds to the XEC command by presenting to the active module a coded cell number associated with the highest priority program (Execute) Interrupt Cell that is set and unmasked for the port initiating the XEC command. The information is transferred on the basic data lines in the following format:



If no cells are set (and/or unmasked), the following code is returned:



3.4.10 Read Program Interrupt Cells (XEC) 11011 (continued)

The following table specifies the cell number (address code) associated with each Program (execute) interrupt cell (bit) position:

CELL (BIT) POSITION (DECIMAL)	ENCODED OCTAL CELL #, BITS 12-16	CELL (BIT) POSITION (DECIMAL)	ENCODED OCTAL CELL #, BITS 12-16
/0 Highest priority	/00	16	20
1	01	17	21
2	02	18	22
3	03	19	23
4	04	20	24
5	05	21	25
6	06	22	26
7	07	23	27
8	10	24	27
9	11	25	31
10	12	26	32
11	13	27	33
12	14	28	34
13	15	29	35
14	16	30	36
15	17	31	/37 Lowest Priori

The highest priority program (execute) interrupt cell (bit), reflected by the cell number sent to the active module, is reset by execution of the XEC command. Note that the encoded cell number is not stored by the System Controller.

The system port through which this command is attempted, must have a Program Interrupt Mask Register assigned or a Not Control illegal action will result.

The address field (ZAC lines) must address the System Controller's configured "lower" Storage Unit.

3.4.11 Set Program Interrupt Cell (SXC) 11101

The SXC command is a single precision operation.

The SXC command allows active modules to set (write) designated "one bits" into a 32 cell (i.e., 32 bit) "Program (execute) Interrupt" storage register, but only 16 bits at a time.

The "Program Interrupt cell(s)", corresponding to the "1" bits on the basic data lines, are set to 1. All other cells are unaffected. The correspondence, between the register's cells and the data bit positions of the basic data lines, is shown as follows:

0	15 16	34 35
INTERRUPT CELLS 0-15 OR 16-31	0----------0	U/L

U/L = Upper/Lower Select Bit.
Bit 35 = 0; Cells 0-15 are selected for alteration.
Bit 35 = 1; Cells 16-31 are selected for alteration.

These cells and their contents are physically located within the System Controller.

The address field (ZAC lines) must address the System Controller's configured "lower" Storage Unit.

Refer to paragraph 3.4.10 (XEC Command) for further information.

3.4.12 Connect (CON) 11001

A "CON" is a single precision operation. A Connect ($CON) pulse is sent to the port selected by bits 33, 34, and 35 of the C(Y). The C(Y) are not sent to the selected port. The C(Y) in storage are not altered. The word is selected using bits 0-17 of the address Y.

The Data Available ($DA) pulse is used to notify the requesting system port of the command completion. Any illegal action is signaled to the requesting system port and results in the $CON pulse being inhibited.

3.4.13 Read General Register (RGR) 10110; "RSCR" in Processor EPS-1

This command provides, to the active module, access to the registers in the 655 System Controller. The octal digits X (see below) of the effective address select the system controller and store unit to be accessed. The octal digits Y (see below) are "don't care" digits. The selected system controller does not transmit the contents of a storage location. Rather the contents of the system controller register specified by address bits 9 through 14 are transmitted to the active module via the requesting system port. This command causes a double precision transfer, hence both the basic and extended data lines are used. The address codes of the registers are as follows:

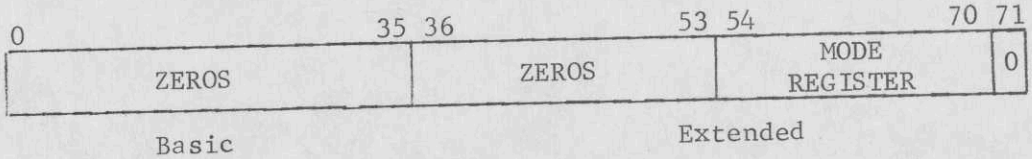
OCTAL ADDRESS	MNEMONIC	REGISTER
XYYY0X	MR	System Controller Mode Register*
XYYY1X	CFG	Configuration Switches*
XYY02X	MSK0	Interrupt Mask Register, Port 0*
XYY12X	MSK1	Interrupt Mask Register, Port 1*
XYY22X	MSK2	Interrupt Mask Register, Port 2*
XYY32X	MSK3	Interrupt Mask Register, Port 3*
XYY42X	MSK4	Interrupt Mask Register, Port 4*
XYY52X	MSK5	Interrupt Mask Register, Port 5*
XYY62X	MSK6	Interrupt Mask Register, Port 6*
XYY72X	MSK7	Interrupt Mask Register, Port 7*
XYYY3X	IC	Interrupt Cells*
XYYY4X	ETC	Elapsed Time Clock*
XYYY5X	ETC	Elapsed Time Clock*
XYYY6X	SU	Store Unit Mode Register
XYYY7X	SU	Store Unit Mode Register

---

*Note: The address field also must address the System Controller's configured "lower" Storage Unit.

3.4.13.1 Mode Register (RGR-MR)

The command RGR-MR will return, on bits 54 to 70 of the data lines, the current state of the margin logic. This may be the contents of the Mode Register, or the settings of the PARITY/MARGIN CONTROL switches on the maintenance panel, depending on the setting of the PROG-MANUAL switch and the Test-Normal Switch. The format is:



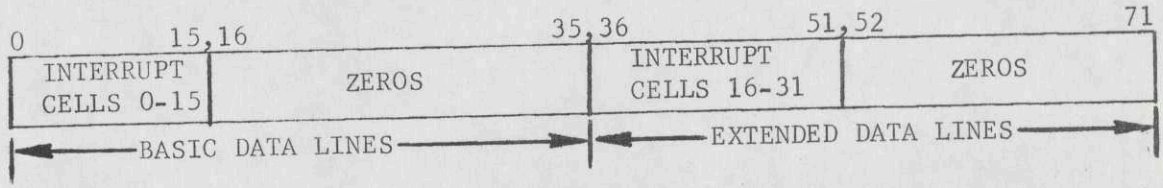
DATA BIT	FUNCTION
0-35	All Zeros
PU	Odd Parity Bit
36-53	All Zeros
54	$TS Margin MSB
55	$TS Margin LSB
56	$CMD Margin MSB
57	$CMD Margin LSB
58	$ANSWER Margin MSB
59	$ANSWER Margin LSB
60	$DA Margin MSB
61	$DA Margin LSB
62	$EOC Margin MSB
63	$EOC Margin LSB
64	+5 Volt Margin MSB
65	+5 Volt Margin LSB
66	Parity Override
67	Parity Disable
68	Disable Store IA
69	ZAC Parity Error
70	If "1", SCU will accept an SGR Command (see paragraph 3.4.14 and 3.6.4.2).
71	Zero
PL	Odd Parity Bit

CODE FOR MARGIN FUNCTIONS

MSC	LSB	FOR STROBES ($)	FOR VOLTAGE
0	0	Normal Timing	Normal
0	1	Slow Timing	-5%
1	0	Inhibit Strobe	Normal
1	1	Fast Timing	+5%

3.4.13.4 Interrupt Cells (RGR-IC)

The RGR-IC command causes the contents of the interrupt cells to be presented on the data lines in the following format:



The RGR-IC command does not alter the contents of the interrupt cells.

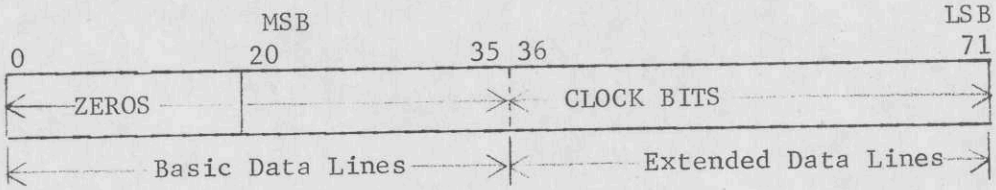
3.4.13.5 Elapsed Time Clock (RGR-ETC)

ETC operation is specified in paragraph 2.6.

The RGR-ETC command causes the contents of the Elapsed Time Clock register to be read and presented on the data lines (0-71).

- Standard Clock Format (52 bit clock):

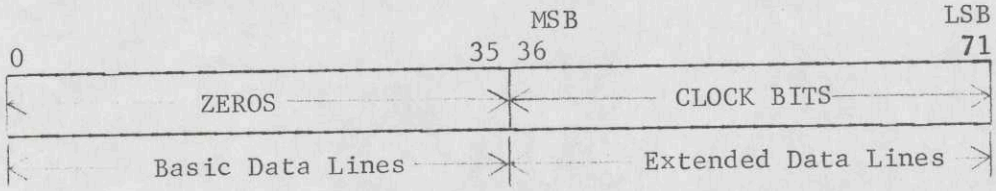
  Note: Applies to later model System Controllers only.



  Bit 71 is the least significant bit (LSB). The ETC is incremented by one at one microsecond intervals. Maximum ETC capacity is approximately 142 years before "rollover", if bits 20 thru 55 are set to zero. Active System modules shall not be notified when "rollover" occurs.

- Non-Standard Clock Format (36 bit clock):

  Note: Applies to early model System Controllers only.



  Bit 71 is the least significant bit (LSB). The ETC is incremented by one at one microsecond intervals. Maximum ETC capacity is approximately 19 hours before "rollover". This ETC is not settable. Active System modules shall not be notified when "rollover" occurs.

3.4.13.6 Storage Unit Maintenance Register (RGR-CU)

The RGR-CU command will return, on the extended data lines, the current state of the maintenance register from the storage unit. Refer to the EPS-1's for 655/6000 Storage Units for format.

3.4.14 Set General Registers (SGR); "SSCR" in Processor EPS-1

The SGR commands are the inverse of the RGR commands except that the Configuration Switches and the Elapsed Time Clock are not settable. In addition, the active module must have an Interrupt Enable Register assigned to its port, or a NOT CONTROL illegal action will result. Acceptable variations of SGR are: Mode Register, Interrupt Enable Registers, Interrupt Cells and store unit mode register. Any attempt to set the configuration switches or the Elapsed Time Clock will result in an Illegal Command IA code. (Ref. Figure 3.4.14).

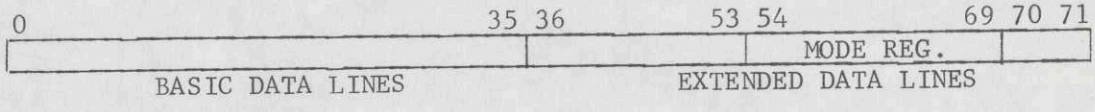
These three address assignments (XYYY1X, XYYY4X, XYYY5X) are not used and shall not be assigned to other functions. The address codes of the registers are the same as the codes used for the Read General Registers command. See Section 3.4.13.

3.4.14.1 Mode Register (SGR-MR)

The Mode Register is intended to be utilized by the T&D Programmer to margin strobes and voltages, as well as exercising the fault and parity logic within the SCU. To prevent possible erroneous use of the Mode Register, it is required that the SCU Maintenance Panel be in TEST and the PARITY/MARGIN CONTROL PROG-MAN switch be in the PROG position before the Mode Register is effective. If setting of the Mode Register is attempted when the SCU Maintenance Panel is in NORMAL, an ILLEGAL COMMAND IA code will be returned to the user.

Margin conditions specified by bits 54-69 of paragraph 3.4.13.1 (RGR-MR) can be set with the SGR-MR command.

MODE REGISTER FORMAT



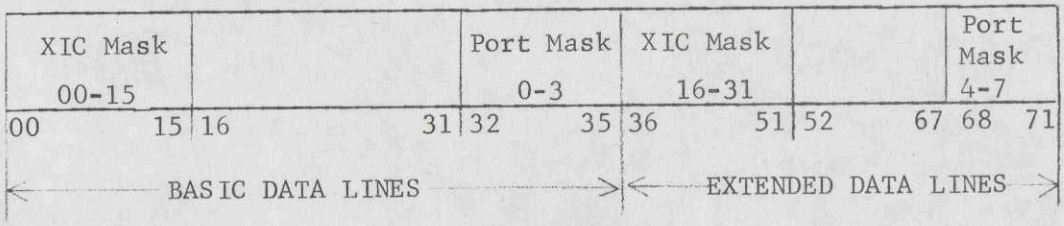
	OCTAL ADDRESS	DESIGNATED REGISTER	READABLE	SETTABLE
*	XXXX0X	MODE REGISTER	YES	YES
*	XXXX1X	CONFIGURATION SWITCHES	YES	NO
*	XXX02X	EXECUTE INTERRUPT MASK REG. PORT 0	YES	YES
*	XXX12X	EXECUTE INTERRUPT MASK REG. PORT 1	YES	YES
*	XXX22X	EXECUTE INTERRUPT MASK REG. PORT 2	YES	YES
*	XXX32X	EXECUTE INTERRUPT MASK REG. PORT 3	YES	YES
*	XXX42X	EXECUTE INTERRUPT MASK REG. PORT 4	YES	YES
*	XXX52X	EXECUTE INTERRUPT MASK REG. PORT 5	YES	YES
*	XXX62X	EXECUTE INTERRUPT MASK REG. PORT 6	YES	YES
*	XXX72X	EXECUTE INTERRUPT MASK REG. PORT 7	YES	YES
*	XXXX3X	INTERRUPT CELLS	YES	YES
*	XXXX4X	ELAPSED TIME CLOCK	YES	NO
*	XXXX5X	ELAPSED TIME CLOCK	YES	NO
	XXXX6X	STORE UNIT MODE REGISTER	YES	YES
	XXXX7X	STORE UNIT MODE REGISTER	YES	YES
	X = DON'T CARE			

Figure 3.4.14 Address Field for SGR/RGR

*Note: The address field also must address the System Controller's configured "lower" Storage Unit.

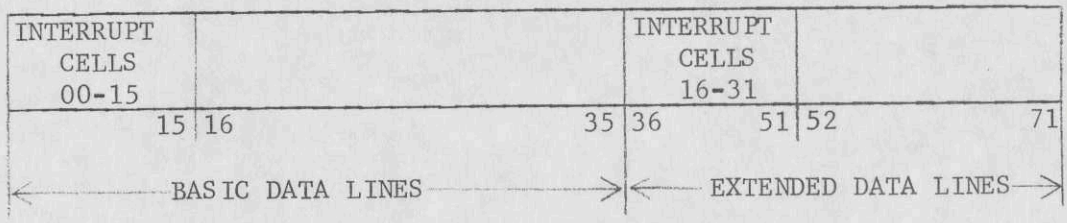
3.4.14.2 Set Interrupt Mask Register, Port "M" (SGR-MSKn)

The SGR-MSKn is the only means available to the user to set another port MASK. If the port designated by SGR address bits 9, 10, 11 does not have a mask assigned, that portion of the data will be dropped and no IA will be returned. The format is as follows:



3.4.14.3 Set Interrupt Cells (SGR-IC)

The SGR-IC command causes the data received to be stored into the Execute Cells as per the following format:



3.4.14.4 Set Storage Unit Maintenance Register (SGR-CU)

The SGR-CU will set the maintenance register within a Storage Unit based on information contained on the extended data lines (bits 36-71). Refer to the EPS-1's for 655/6000 Storage Units for format.

3.4.15 Lock/Unlock Function and Commands

The Read/Lock SP (40_8) and the Write/Unlock SP (60_8) commands, in conjunction with a "Key line" (para. 4.1.1.17), provide 6000 Line* active modules with the capability to perform a read cycle and a write cycle without an interfering cycle gaining access in between.

The intent of the "lock" capability is to provide a 600 Line "RAR like" function for System Software gating functions. Proper utilization of the "lock" function requires System Software to develop and implement unique control procedures.

3.4.15.1 Read/Lock, Single Precision (RDLK, SP)* 10000

a) The C(Y) are sent to the requesting active system port on the basic data lines. The C(Y) in storage are not altered. The word is selected using bits 0-17 of the address Y.

The precise time that access is granted to the Store Unit is a function of the "Key Line" and the Lock/Unlock state of the store unit at the time the RDLK command is received (see para 3.4.15.3).

b) 6000 Line active ports:

Upon decode of the RDLK command, the System Controller shall set a "Lock Flag" to remember the "Lock" request. Subsequent actions are specified in para 3.4.15.3.

---

*Note: Not available with, or applicable to, early 6000 Line active module Port Options.

3.4.15.2 Write/Unlock, Single Precision, (WULK, SP)* 11000

a) The C(Y) are replaced by the data on the basic data lines from the requesting system port. The entire word shall be written (36 bits of data). All the zone lines must be in the true state (ones). The word shall be selected using bits 0-17 of the address Y.

The "Unlock" capability is a function of the state of the "Key line".

b) 6000 Line Active Ports:

If the WULK command is received with the key line enabled;

- and the "lock" function is set, the "lock" function will be reset and the command executed.
- and the "lock" function is not set, the port shall remain "unlocked" and the command executed with no IA reported for this cause.

If the WULK command is received with the key line disabled;

- and the "lock" function is set, the lock function shall not be reset and the command executed with no IA reported for this cause.
- and the "lock" function is not set, the port shall remain "unlocked" and the command executed with no IA reported for this cause.

---

*Note: Not available with or applicable to, early 6000 Line active module Port Options.

3.4.15.3 Lock/Unlock Operation:

a) Description:

Two commands, Read/Lock SP (40_8) and Write/Unlock SP (60_8), plus a "key" line interact with one another to "Lock" and "Unlock" a storage unit. Lock Control circuitry will be set each time a Read/Lock command is received by the System Controller. When set, this lock flag will cause the System Controller to postpone all "other active module" requests that do not have their "Key" line enabled. The Lock circuitry will be reset when a Write/Unlock command is received with the "Key" line enabled, or when a time out period has been exceeded. The limits on the lock time out period shall be $19 < t < 27$ microseconds. An IA shall not be reported for a Lock Timer "run-out". It is assumed that the active module implementation of the Lock/Unlock commands will be such that an unlock command (60_8) must immediately follow a "Lock" (40_8) command.

b) Access Permissions and Priorities:

- A "Lock" initiated by a given active port prohibits another active port from accessing main store only if that other active port has its "Key" line disabled. Conversely, if the other active port has its "Key" line enabled, an intervening Store Unit access could occur during a Read/Lock and Write/Unlock sequence.

- A "Lock" is not recognized as such until the initiating active port is granted access by the normal active port priority logic (para 3.1.8).

- If two active ports transmit "Lock" commands simultaneously, they will be recognized in the order determined by the normal active port priority logic.

- If "Lock" Commands are "stacked up" for several active ports, they will be recognized in the order determined by the normal active port priority logic.

- Once a "lock" has been granted to an active port by the System Controller, both Storage Units are "locked" to that active port until a Lock Timer "run-out" occurs, or until a WULK command (with the key line enabled) is received.

3.5 ILLEGAL ACTION

Any illegal action detected by either the Store Units or the System Controller is encoded on the Illegal Action lines and transmitted to the system port through which the access request was attempted.

The H-6000 System Controller illegal action codes in Table 3-2 provide more extensive diagnostic information, due to extensive parity transmission and illegal command detection. Further, an ABORT function converts any cycle into an RRS type cycle in order to protect good data. Illegal actions detected by the Store Units are encoded (different codes) on illegal action lines and presented to the System Controller. The System Controller re-encodes the store unit illegal action and/or any illegal action detected by the System Controller for transmission through the system port. The store unit illegal actions are shown in Table 3-3.

When more than one illegal action occurs simultaneously, only the code of the event with the highest priority is transmitted. The priorities are shown in the tables.

3.5.1 System Controller Illegal Actions

The System Controller will present the Illegal Action lines to the system port that initiated the command approximately 100 nanoseconds following the Data Availabile Pulse ($DA). Encoded on the Illegal Action lines will be the status of the command that was last completed. Table 3-2 specifies the valid System Controller Illegal Action codes and the following paragraphs represent a brief description of each.

3.5.1.1 No Illegal Action 0000

An IA code of 0000 is issued by the System Controller when the initiated command is completed without detection of an error.

3.5.1.2 Non-Existent Address 0010

An IA code of 0010 indicates the port initiating the command sequence has attempted to access a storage location which violates the address range assigned by the Address Boundary switches on the System Controller Configuration Panel. See Section 3.2.3 for a description of the non-existent address conditions.

PRIORITY	OCTAL CODE	ILLEGAL ACTION LINES IA0	IA1	IA2	IA3	655	625/635
14	0	0	0	0	0	None	None
--	1	0	0	0	1	(Not used by system controller)	(Not used)
5	2	0	0	1	0	Non-existent address	Non-existent address
1	3	0	0	1	1	Fault on condition	(Not used)
--	4	0	1	0	0	(Not used)	Not master mode
12	5	0	1	0	1	Data parity, store to SC	(Not used)
11	6	0	1	1	0	Data parity in store	Store parity
10	7	0	1	1	1	Data parity store to SC and in store	(Not used)
4	10	1	0	0	0	Not control port	Not controlproc., Masked Port, Illegal Cmd.
13	11	1	0	0	1	Port masked	(Not used)
3	12	1	0	1	0	Illegal command	(Not used)
7	13	1	0	1	1	Store not ready	(Not used)
2	14	1	1	0	0	ZAC parity active module to SC	(Not used)
6	15	1	1	0	1	Data parity, active module to SC	(Not used)
8	16	1	1	1	0	ZAC parity, SC to store unit	(Not used)
9	17	1	1	1	1	Data parity, SC to store unit	(Not used)

E

Line IA3 is not in the 625/635.

SYSTEM CONTROLLER ILLEGAL ACTIONS

TABLE 3-2

3.5.1.8 Port Masked 1001

An Illegal Action code of 1001 indicates the System Controller has detected an active module attempting to issue a connect to a port that is masked. A port may be masked (disabled) via the "Port Mask" switches on the System Controller configuration panel or via program control of the Port Mask Register if the "Port Mask" switch is in the center (Program Control) position.

3.5.1.9 Illegal Command 1010

An Illegal Action code of 1010 indicates that the System Controller has detected a command that is invalid. There are 32 possible combinations; 16* are valid and 16* are invalid. In addition, an Illegal Command will be declared if the address field (ZAC lines), associated with any "register type" command (see section 3.4), do not address the System Controller's configured "lower" Storage Unit. When an Illegal Command occurs, the System Controller will abort the cycle and the Illegal Action Code 1010 is sent to the requesting system port.

3.5.1.10 Store Unit Not Ready 1011

An Illegal Action code of 1011 indicates a user has attempted to access an assigned Store Unit and one of the following conditions exists:

- o The Store Unit has had a power failure.
- o The Store Unit has had a temperature failure.
- o The Store Unit time out period has elapsed without receiving a command strobe.
- o The Store Unit has not responded with an $ANS or an $EOC. (e.g., Store Unit in Maintenance or Off-line.)

3.5.1.11 ZAC Parity Error, Active Module to S.C. 1100

An Illegal Action of 1100 indicates the System Controller detected a parity error on the ZAC information received from an active module issuing a System Controller Command. Write type commands will be aborted by the System Controller when a user ZAC Parity error is encountered. The ZAC information is passed on to the Store Unit unaltered, thus the store unit will also detect a user ZAC parity error if it exists. The Illegal Action priority in the System Controller will cause the ZAC parity error detected by the System Controller to be reported to the requesting system port.

3.5.1.12 Data Parity Error, Active Module to S.C. 1101

An Illegal Action code of 1101 indicates the System Controller detected a parity error on the data lines received from a requesting active module. Write type commands will be aborted by the System Controller when a Data Parity Error is encountered.

---

*Note: Early System Controllers have only 14 valid commands; see Table 3-1.

3.5.2.12 Parity Error - ZAC and Write Upper/Lower 1111

An Illegal Action code of 1111 indicates a ZAC parity error (IA code 1100) and a Data Parity Error - Write Upper (IA code 0110) both occurred. The Store Unit will abort the cycle.

3.6 MAINTAINABILITY AIDS

The maintainability aids provided in the System Controller are of the following general types:

- o Maintenance Panel
- o Self Test Provisions
- o Stop or Fault on Condition
- o Program Access and Control of T&D Aids

(Additional features may be specified in the GE-655 Maintainability Design EPS-1.)

3.6.1 Maintenance Panel

The Maintenance Panel shall have at least the following capabilities plus any additional features required by the specific hardware design.

- o Display all System Controller registers.
- o Display most control flip/flops and control points.
- o Initialize the System Controller and Store Units.
- o Control self-test of the System Controller and Store Units.
- o Allow oscilloscope trigger of self-test.
- o Controls for Stop or Fault on Condition.
- o Operation mode control, either manual or program, for the following marginal checking tests:
  - (1) Fast/slow/normal timing selection
  - (2) High/low/normal voltage
- o Parity disable switch - inhibits SCU detected parity errors (store detected parity errors will still be reported)
- o Manual lamp test
- o Switches needed to set the Elapsed Time Clock (see paragraph 2.6).

[E] The Maintenance Panel controls are all enabled or disabled by a single Test/Normal switch.

3.6.4.1 Fault Register in the 655 Processor

The Fault Register in the 655 Processor is used to differentiate ambiguous error conditions. Included in the register fields are the state of each of the Illegal Action lines from each System Controller connected to a processor system port.

Every error detected by the processor which results in a fault trap has a separate and unique bit or code set in the fault register, such that more than one fault indication may be in the register at the same time. The action of setting a new fault code (for a different code) does destroy the previous fault indications.

The bit format is shown in the 655 Processor EPS-1. See Section 1.2, Application Documents.

3.6.4.2 Program Controlled Tests via the SGR/RGR Commands

The following tests will be initiated and controlled via the SGR/RGR commands:

- o Set fast/slow/normal timing margins
- o Set high/low/normal voltage margins
- o Force the store unit to store data with incorrect parity on CWR-DP commands.
- o Disable parity checking in the system controller
- o Inhibit the indication of illegal actions by the store unit.
- o Force incorrect ZAC parity.

Bit 70 of the Data Lines (See para. 3.4.13.1):

Bit 70 provides a means for T&D to determine (via an RGR command) whether the Mode Register (margins) can be set in the System Controller. Bit 70 is a "one" (set) under the following conditions:

- o The SCU Normal/Test switch is in the "Test" position; and the Program/Manual switch is in the "Program" position. or
- o The System Control Center (SCAM functions) places the SCU in the "Test" state; and the Normal/Test switch is in the "Normal" position.

4.0 HARDWARE INTERFACES

The 655 System Controller has two types of interfaces to other system hardware modules:

- o System ports interface with active modules such as processors, IOM, etc.
- o Store ports interface with magnetic core store units.

The ports are provided as options (Section 2.2) for interfacing the System Controller with 655 modules. [E]

The following section describes the interface requirements between these port options and the appropriate module.

4.1 655 SYSTEM PORTS

4.1.1 System Port Interface Signals

The system port interface consists of 122 signal lines to/from the active module as shown in Figure 4-1. All communication between the active module and the System Controller takes place over these lines. The next sections describe these lines and the basic timing relationships.

The signal lines are listed below. The designation "true" indicates the interface receives/sends a high-level (+5 volts) when the signal is enabled. The designation "false" indicates the interface receives/sends a low level (0 volts) when the signal is enabled.

Basic Data Lines (36 data lines, bidirectional and 2 parity lines, unidirectional) (true)

Extended Data Lines (36 data lines, bidirectional and 2 parity lines, unidirectional) (true)

Zone Line (8 lines unidirectional from active module) (true)

Address Lines (18 undirectional from active module) (true)

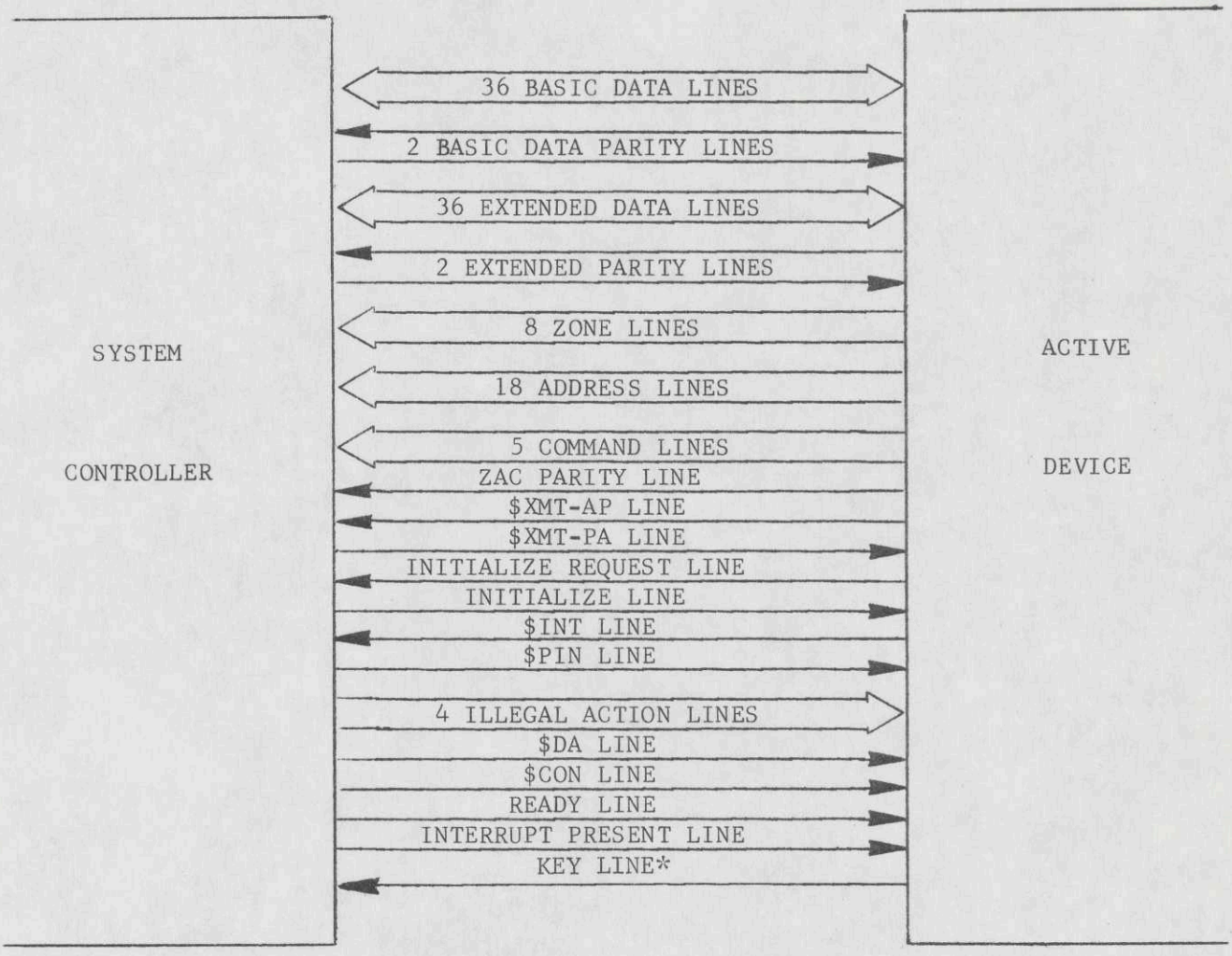
Command Lines (5 lines unidirectional from active module) (true)

ZAC Parity (1 line unidirectional from active module) (true)

Transmit Strobe ($XMT-AP) Line (1 line unidirectional from active module) (true)

Initialize Request Line (1 line unidirectional from active module) (false)

Access Request Strobe ($INT) Line (1 line unidirectional from active module) (false)



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SYSTEM PORT INTERFACE

FIGURE 4-1

E *NOTE: Not available with, or applicable to, early 6000 Line active Port Options.

4.1.1 System Port Interface Signals (Continued)

Acknowledge Strobe ($PIN) Line (1 line unidirectional from SC) (false)

Illegal Action Lines (4 lines unidirectional from SC) (true)

Data Available Strobe ($DA) Line (1 line unidirection from SC) (false)

Connect Strobe ($CON) Line (1 line unidirectional from SC) (false)

Transmit Strobe ($XMT-PA) Line (1 line unidirectional from SC) (false)

Initialize (1 line unidirectional from SC) (false)

Ready (RDY) (1 line unidirectional from SC) (false)

Interrupt Present (XIP) Line (1 line unidirectional from SC) (false)

Note: SC = System Controller

The operation of these lines is described in the following sections.

[E] Timing parameters are specified in Figure 4-4.

4.1.1.1 Basic Data and Extended Data

The 38 basic data lines (36 data lines and 2 unidirectional parity lines) plus the 38 extended data lines (36 data lines and 2 unidirectional parity lines) make up a 74 line bi-directional data path for transfer of data with parity to/from the System Controller. The sense of parity is odd with bit 72 as the basic data parity bit and bit 73 as the extended data parity bit. Bit 0 is the most significant bit, and bit 71 is the least significant bit.

All single precision operations will utilize the basic data lines. During single precision operations, the extended data lines and extended parity line are ignored.

4.1.1.2 Zone Lines

The (8) unidirectional Zone lines are used to specify which six or nine bit characters are to be operated on during a single precision store operation (clear write). The Store Unit will ignore the Zone lines for all commands except single precision stores.

[E] NOTE: See Figure 4-4 for timing.

4.1.1.2 Zone Lines (Continued)

E The following table shows the zone assignments.

DATA BITS AFFECTED	CHARACTER	SIZE	ZONE	LINE
00-05	6	9	Z0	Zone Zero
06-08	6		Z1U	Zone One Upper
09-11		9	Z1L	Zone One Lower
12-17	6		Z2	Zone Two
18-23	6	9	Z3	Zone Three
24-26	6		Z4U	Zone Four Upper
27-29		9	Z4L	Zone Four Lower
30-35	6		Z5	Zone Five

4.1.1.3 Address Lines

The 18 unidirectional address lines are used to specify the location in which a store module access is to occur or in the case of internal System Controller cycles the address of an internal register. Address line (0) is the most significant address bit and line (17) is the least significant address bit.

4.1.1.4 Command Lines

The (5) unidirectional command lines are used to specify the command to be executed when the access request ($INT) pulse from the active module is acknowledged. Illegal combinations of command lines will be trapped and the active module notified via the Illegal Action lines.

4.1.1.5 ZAC Parity

The active module will generate odd parity for the combined Zone, Address and Command (ZAC) lines and furnish this parity to the system port.

E

4.1.1.6 Transmit Strobe ($XMT-AP)

The transmit strobe ($XMT-AP) is utilized by the active module to control the strobing of data into the System Controller port board receive register.

E
E NOTE: See Figure 4-4 for timing.

4.1.1.7 Initialize Request

The system port will accept the Initialize Request signal from the active module (usually originated at the IOM or System Console). This signal will be accepted by the System Controller and distributed through other system ports via the Initialize Line.

4.1.1.8 Access Request Strobe ($INT)

The access request strobe ($INT) is used by the active module to initiate a System Controller command. Timing references to the $INT in this EPS-1 are to be the initial transition of the pulse.

4.1.1.9 Acknowledge Strobe ($PIN)

The acknowledge strobe ($PIN) notifies the active module that the requested cycle is in progress. The minimum time period (at the system port) from $INT to $PIN is a function of whether the System Controller is currently busy servicing another port, the priority of the port requesting access, the store speed, etc.
(See paragraph 4.1.2.)

4.1.1.10 Illegal Action Lines

The system port provides 4 unidirectional lines to the active module coded to provide Illegal Action information. These 4 lines will be valid following the transfer of the data. Parity is not generated on the Illegal Action lines.

4.1.1.11 Data Available Strobe ($DA)

The data available strobe ($DA) is the pulse issued by the System Controller indicating that the requested data will be valid in the active module port board a short time later. The active module will receive a $DA pulse for all System Controller cycles (store or read) with $DA preceding the Illegal Action lines. For store type cycles $DA is effectively an End of Cycle Pulse since there is no data sent to the requesting active module.

4.1.1.12 Connect Strobe ($CON)

The connect strobe ($CON) is a pulse from the System Controller to alert the active module of intermodule communication. $CON is a result of a connect command to the System Controller and will be generated as a function of the $DA pulse of the connect command. The System Controller will send $CON to the designated system port provided the port is enabled. $CON to a not enabled port will result in an illegal action to the system port originating the connect command.

NOTE: See Figure 4-4 for timing.

4.1.1.13 Program Interrupt Present (XIP)

The program interrupt present (XIP) is a level from the System Controller to an active module designated as a Control Module indicating a Program Interrupt cell requires service. The 655 System Controller can designate up to four system ports as control ports via the Program Interrupt Mask Register Assignment Switches on the System Controller Configuration Panel. (See Figure 4-4 for timing.)

4.1.1.14 Transmit Strobe ($XMT-PA)

The transmit strobe ($XMT-PA) is the signal used by the System Controller to strobe data into the active module port board data receive register. The System Controller will generate the ($XMT-PA) to control the strobing of data to be placed in the active module receive register. (See Figure 4-4 for timing.)

4.1.1.15 Initialize (INZ) Line

The Initialize (INZ) signal is a level from the System Controller to cause all on-line active modules to go to the initialized state. The initialize signal will occur asynchronous of all system timing.

4.1.1.16 Ready (RDY) Line

The Ready (RDY) line indicates the System Controller is available for access. Active modules must not attempt to access the System Controller when the READY line is in the disabled state.

4.1.1.17 Key Line*:

The Keyline is a necessary part of the "Lock" capability specified in paragraph 3.4.15. The enabled state corresponds to a "zero." The disabled state corresponds to a "one". The key line shall change state at the same time as the ZAC lines from the Active unit.

*NOTE: Not available with, or applicable to, early 6000 Line Active Port Options.

4.1.2 655 System Port Timing

The timing values at the System Controller Port Interface (SCI) shall be set to take advantage of the 10 foot minimum length cable delay (approximately 40 ns) and the turnaround logic delay within the active modules. The system controller shall utilize address bits 0, 1, 2 and 16 (0=most significant bit) for address look ahead. In order for the address look ahead function to be realized before the occurrence of the $INT pulse, it shall be necessary for the address bits to be valid at the SCI 10 ns prior to the initiation of $INT. The remaining lines (Zone, Address, Command and Data) shall be stable at the SCI within 50 ns following the initiation of the $INT pulse.

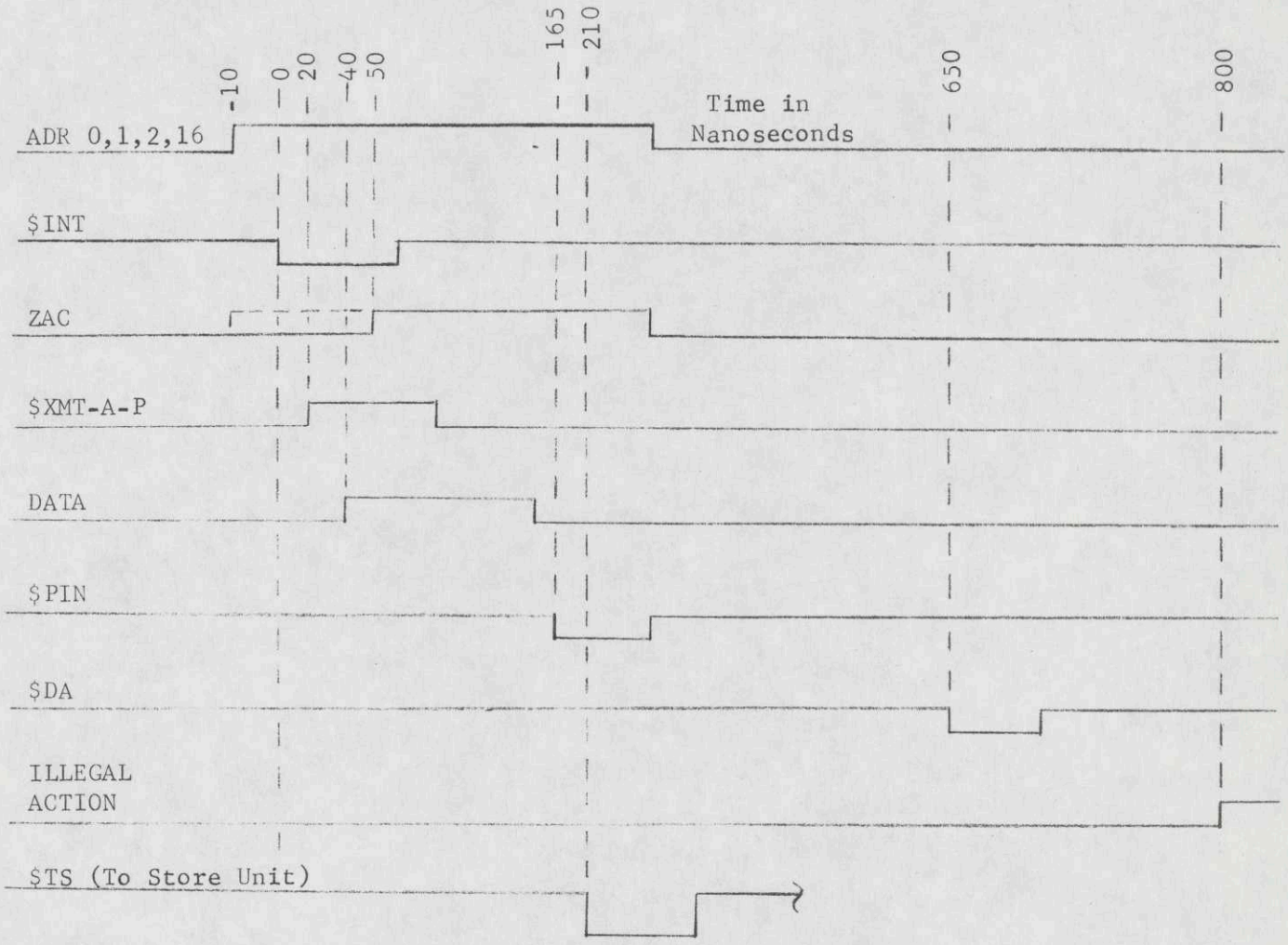
The System Controller shall take advantage of cable delay and internal active module turnaround time. That is, the system controller shall issue the $PIN pulse even though it is still using the ZAC and data lines, thus permitting an active module to prepare for the next cycle and have the ZAC and data lines as well as the $INT pulse at the SCI as soon as the system controller becomes available to start another cycle. Consequently, the ZAC lines (including address look-ahead lines) must remain stable at the SCI for a minimum of 100 ns following the initiation of the $PIN pulse at that interface.

In order to achieve the specified minimum Gibson mix rate (655 Processor EPS-1) the following maximum times must not be exceeded at the System Controller ports (junction panel) with 0.5 usec store units and 10 feet cable lengths from the System Controller to the Store Units.

- o $INT to $PIN 165 manoseconds maximum (no interfering requests)
- o $PIN to $DA* 505 nanoseconds maximum
- o $INT to $DA* 670 nanoseconds maximum (no interfering requests)

Figures 4-2 and 4-3 summarize the timing of the system port interface signals, with 655 (0.5 usec) Store Units on the store port. The times are not a specification but are illustrative.

*NOTE: Dependent on store unit cycle time.



Notes (1) Times are for a 6000 Line (0.5 μsec) store unit.

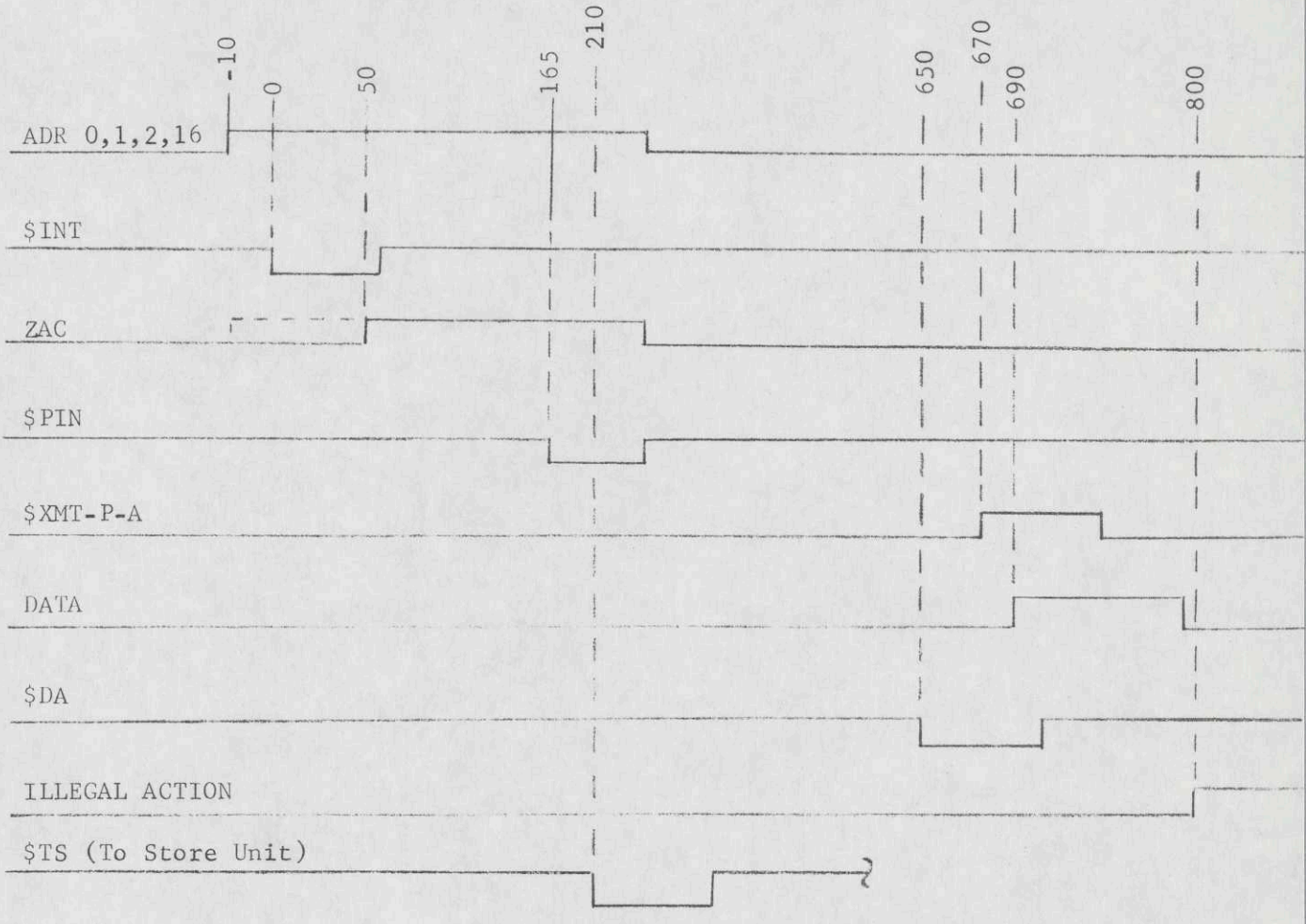
(2) This chart represents a clear write type store from a cold start (no overlap).

(3) The times are not a specification but are illustrative. Not to scale.

Figure 4-2

H-6000 System Controller Timing

Store Type Operation



NOTES: (1) Times are for a 6000 Line (0.5 μsec) store unit.

(2) This chart represents a read-restore type store cycle from a cold start (no overlap).

(3) The times are not a specification but are illustrative. Not to scale.

Figure 4-3

H-6000 System Controller Timing

Read Type Operation

6070/6080 SYSTEMS
H-6000 SYSTEM CONTROLLER/ACTIVE PORT INTERFACE SIGNALS

SIGNAL	WIDTH		OCCURRENCE	
	AVERAGE	TOLERANCE	AVERAGE	TOLERANCE
$INT	60	± 20	0	± 0 By definition Reference point.
ZAC (addr. 0,1,2, & 16)	275	From ($INT-50)nsec to ($PIN+120)nsec on successive cycles.	-20	+10 / -40 Must be stable at ($INT-10)nsec and remain stable until ($PIN+100)nsec.
ZAC (cmds, zones, addr)	275	From ($INT-50)nsec to ($PIN+120)nsec on successive cycles.	-20	+70 / -40 Must be stable at ($INT+50)nsec and remain stable until ($PIN+100)nsec.
$PIN (read cycles)	100	± 30	+165 (no interfering cycles).	± 10
$PIN (write cycles)	100	± 30	+215 (no interfering cycles).	± 20
DATA-AP	90	± 20	+ 30	+20 / -50
XMT-AP	60	± 10	+ 20	+10 / -30 Trailing edge of XMT-AP must precede trailing edge of Data by minimum of 30 nsec.
$DA (note 2)	60	± 20	+650 (no interfering cycles).	±20 $DA shall precede DATA-PA by 50 +10 / -30 nsec.
XMT-PA (note 2)	60	± 20	+670	±20 (± 10 nsec with respect to $DA).
DATA-PA (note 2)	100	± 20	+690	±20 Trailing edge of XMT-PA must precede trailing edge of DATA by minimum of 40 nsec.
IA Lines	700 (successive cycles to same Store Unit)	± 40	+800	±20

FIGURE 4.4 (Cont. Next Page)

SIGNAL	WIDTH		OCCURRENCE	
	AVERAGE	TOLERANCE	AVERAGE	TOLERANCE
$CON	60	± 20	$DA+100 nsec., (no interfering cycles).	± 20
XIP	True until answered or masked.	Not Applicable	$INT+400 nsec., (no interfering cycles).	± 30
ZAC (parity bit)	275	From ($INT-50)nsec to ($PIN+120)nsec on successive cycles.	-20	+70 / -40 Must be stable at ($INT+50)nsec and remain stable until (PIN+100)nsec.
DATA-AP (parity bit)	300(On successive cycles).	± 20	+20	+20 / -50
DATA-PA (parity bit) (note 2)	700	± 20	+690	±20 (same as DATA-PA)

NOTES:

(1) This Table is a rigid specification for signals received and transmitted by (and at) the System Controller active interface (System Controller's port board free edge connector).

(2) Actual "time of occurrence" is dependent on Storage Unit interactive cycle time as well as System Controller design tolerances; the Table assumes 530 nsecs. interactive cycle time (500 nsec. Store Unit), and 10 foot cables between the System Controller and Storage Units.

FIGURE 4.4

4.2 655 STORE PORTS

The same functional interface lines are required as for the system ports with the following deletions and additions. The following system port lines are deleted from the store port interface:

- o $XMT-AP/$XMT-PA lines
- o Access Request Strobe ($INT)
- o Request Acknowledged Strobe ($PIN)
- o Data Available Strobe ($DA)
- o Connect Strobe ($CON)
- o Ready (RDY)
- o Program Interrupt Present (XIP)
- [E] o Initialize Line (INZ)

The following additional lines are required in the store port interface:

- o Start Strobe
- o Power On/Off
- o Temperature Line (TMP)
- o Answer Line (ANS)
- o End of Cycle Line (EOC)
- o Override Parity Line
- o Transmit Pulses ($XMIT-AP and $XMIT-PA)
- o Refresh Request Line (MOS-Storage Unit)
- o Command Strobe Lines
- [E] o Initialize Line (INZ)

For further details of the interface and timing information, see the GE-655 Core Store Unit EPS-1 (Section 1.2, Applicable Documents) and [D] Appendix A.

The function of each of the additional lines is described in the following sections.

4.2.1 Start Strobe

The Start Strobe starts the storage unit timing, and alerts the storage unit to accept address, zone, and command information.

4.2.2 Power On/Off

A "0" logic level is sent from the core storage unit when the power supply has completed its power-on sequence. Whenever the power supply is operating within its specified margins the (PWR*) line shall be a "0" logic level. When the power supply is shut down or in the power-on sequence for (PWR*) line shall be a "1" logic level or floating.

4.2.3 Temperature Line

A "0" logic level is sent from the core storage unit when the temperature of the stack is within its operating margins. When the temperature has exceeded these margins, the line shall be a "1" logic level or floating.

4.2.4 Answer Line

The Answer pulse shall acknowledge to the System Controller that a cycle has been initiated.

4.2.5 End of Cycle Line

The End of Cycle pulse indicates to the System Controller that the core storage cycle requested is complete.

4.2.6 Override Parity Line

The override parity line signal from the System Controller allows core storage operation with even parity without an abort occurring. An illegal action will occur however.

4.2.7 Transmit Strobe Lines ($XMT-AP and $XMT-PA)

The $XMT Pulse Lines (two) are used to strobe data into the receive registers. A $XMT-AP strobes data into the receive register of the core store. The $XMT-PA strobes data into the receive register of the System Controller.

4.2.8 Command Strobe Lines

The four command strobes are negative pulses of standard pulse width sent to the storage unit to specify the type of cycle to be executed. They are $RRS, $CW1, $CW2, and $RCL. See also Table 3-1.

E

4.2.9 Initialize (INZ) Line

4.2.9.1 Core Storage Units

Refer to paragraph 4.1.1.15.

4.2.9.2 Semiconductor (MOS) Storage Units

This line serves two purposes with MOS Storage Units:

a) Provides the initialize signal as specified by para. 4.1.1.15.

b) Provides the Refresh Response signal as specified by paragraph 4.2.10.2.

4.2.10 Refresh Function*

The System Controller will contain the necessary logic to respond to an asynchronous refresh request signal from a semiconductor (MOS) type store unit. The request will be assigned highest priority. The response will take the form of granting the store unit a cycle time to complete the refresh function. The logic shall be designed in a manner which allows the same store port board to be connected to either a core storage unit or a MOS Storage Unit without change.

4.2.10.1 Refresh Request Line

The Refresh Request signal from the MOS Storage Unit will be a 60 $\pm$ 20 nanosecond negative pulse sent to the System Controller when a "refresh cycle" is required. The true (4.5 volt) level shall be defined as the normal (quiescent) line state.

*NOTE: Not available with, or applicable to, early 6000 line store ports.

4.2.10.2 Initialize/Refresh Response (INZ) Line

a) The initialize function provided by this line is specified in paragraph 4.1.1.15.

b) Refresh Response

As the result of a Refresh Request, the SCU shall transmit a Refresh Response signal (over the INZ line) to indicate to the Storage Unit that the Refresh Cycle can be executed. The System Controller shall assume that the Storage Unit Refresh Cycle shall take no longer than any other memory cycle. The Refresh Response signal shall be a negative pulse of approximately 400 nanoseconds duration. The true (4.5 volt) level is defined as the normal (quiescent) line state.

4.3 635 SYSTEM PORT INTERFACE

Deleted from this section. Refer to appendix B, paragraph B.4.3.

4.4 635 STORE PORT INTERFACE

Deleted from this section. Refer to appendix B, paragraph B.4.4.

	6030/6040/6050/6060	6070/6080	Comments
Interactive Cycle Time (leading edge of $TS to next $TS).	1200 ± 40 nanoseconds. See Note (1).	530 ± 30 nanoseconds. See Note (1).	Timing measured at the Store Port Board free edge connector in the System Controller.
Interactive Access Time (leading edge of $TS to "leading edge of data" sent from Storage Unit). See Note (3).	300 nanoseconds Min. 1035 nanoseconds Max.	300 nanoseconds Min. 380 nanoseconds Max.	Same as above.
Leading edge of $ANS	870 ± 10 nanoseconds, after the leading edge of $TS. See Notes (1), (2).	235 ± 10 nanoseconds after the leading edge of $TS. See Note (2).	Same as above.

Note (1) Assumes successive cycles.

Note (2) When two Storage Units are connected to the same System Controller, the "leading edge of "$ANS" from one Storage Unit shall not differ by more than 20 nanoseconds from the other Storage Unit.

Note (3) The "leading edge of data" specifies the leading edge of the latest (last) data bit sent to the System Controller.

TABLE A.1

Cont. on Page B1

APPENDIX B

600 Line Interface Requirements, Options and Differences.

B.1.0 General Description

B.1.1 Scope

The H-6000 System Controller shall provide the capability to interface with specific G-600 line active and passive system modules. System Controller "options" shall be provided for this purpose.

Most, but not all, H-6000 System Controller features/functions are compatible with 600 Line requirements. This appendix specifies those areas known to impose requirements unique and different from H-6000 Line needs. In all cases, the overriding and controlling objective is to provide the capability to interface with specified G-600 Line Systems and System Modules without requiring G-600 hardware or software changes.

Therefore, the intent of this appendix is to supplement the main body of this specification, for the purpose of more clearly specifying 600 Line optional connections.

B.1.2 Paragraph Number Convention:

For easier cross referencing, paragraph numbers marked *** directly supplement the content of identical paragraph numbers in the main body of this specification. As a result, appendix "B" paragraph numbers are not in continuous (consecutive) order.

B.2.0 Functional Capabilities

The objective is to provide the optional capability to interface with G-635 Processors and/or IOC's and/or Storage Units, but under specific conditions.

B.2.1 Store Units
***

The 6000 Line System Controller is a separate module and provides connection to 1 or 2 G-635 Core Store Units (1.0 usec cycle time). The System Controller shall not interface with G-615/G-625 Store Units (2.0 usec or slower cycle times).

G-635 Store Units and 6000 Line Store Units shall not be mixed on the same System Controller.

B.2.2 System Ports:
***

A maximum of two G-635 active ports shall be provided for connection to G-635 active modules. The remaining active ports shall be used for connection to 6000 Line active modules.

B.2.2 (cont.)

Number of G-635 active ports	Number of 6000 line active ports
1	7 (max.)
2	6 (max.)

The ports have "wired in" positional priority in the order of their numbers (0-7 max.), the lowest number has the highest priority.

Note that the "cyclic priority" switches provide the same function as the G-635 "anti-hog" switches.

B.2.4 Program Interrupt Mask Registers
***

Note that the equivalent G-635 "System Controller" only has one mask register, instead of four. This difference shall be transparent to G-635 System hardware and software.

B.2.5 Data Path Width:
***

The G-635 system uses two undirectional 36 bit data paths, instead of one 72 bit bi-directional data path. Note that the G-635 System can access 72 bits at a time, but the transmission is actually in two 36 bit bursts. The result is a longer cycle for 72 bit transfers. This difference shall be transparent to G-635 System hardware.

B.2.7.2 Store Port Option:
***

In addition to the H-6000 store port options specified, the following G-635 Store Options shall be provided.

- Option:

  #3 One 655/635 Store Port - consists of two pluggable circuit boards and internal cables (1st part).

  #4 Same as #3 (2nd port).

- A maximum of two store ports may be specified. However, 635 store options and 655 store options shall not be intermixed on the same System Controller.

B.2.7.3 System Port Option
***

In addition to the H-6000 active port options specified, the following G-635 active port options shall be provided.

o Option

#13-1 655/635 System Port - consists of three pluggable 12" x 12" circuit boards (1st port).

#14-Same as #13 (2nd port).

o A maximum of two 655/635 system ports may be specified. H-6000 and G-635 system port options may be mixed on the same system controller subject to the following restrictions:

635 and H-6000 processors shall not be intermixed.

IOM and IOC modules shall not be intermixed.

B.2.7.4 G-635 Core Store Parity

Options #3 and #4 of paragraph B.2.7.2 require that the G-635 core store unit transmit the "data upper" and "data lower" parity bits to the H-6000 system controller.

B.3.1 Configuration and Control
***

The configuration of the system controller, as determined by the switch functions described in paragraphs 3.1 thru 3.1.8, shall be different from the G-635 (except as noted).

B.3.1.8 Cycle Port Priority Switches
***

These switches are identical in function to the "Anti-Hog" switches of the G-635 "System Controller".

B.3.2.1 Configurations with Address Interlacing
***

With G-635 active modules connected to the H-6000 System Controller, the only interlacing available shall be between the core store units connected to the System Controllers.

B.3.3.1 G-635 Initialization

The H-6000 System Controller shall be capable of operation in a 635 environment. Therefore, a compatible capability to initialize and boot load in a G-635 system shall be provided. Further, this capability shall be transparent to G-635 system hardware and software.

B.3.3.1 (cont.)

Note that in the 635 system, boot loading is transparent to the system controller. However, the system controller is the distribution center for the initialize signals to the active modules.

The system controller will initialize itself when power turns on, but will not send out initialize signals through the system ports. However, the system ports of operating active modules, connected to a system controller during power-on or off, should be disabled to protect against transients.

The initialized state of the H-6000 System Controller is not compatible with the G-635 and is as follows:

a) Ready to execute a command

b) All port mask access enable bits set to one (port enabled) if the Port mask enable switch is in the ON or "Program Control" position. In the OFF position, the port is forced to the disabled condition (zeros).

c) All Execute (program) Interrupt cells are set to zeros

d) All Execute (program) Interrupt mask enable bits are set to ones (interrupts enabled).

Upon receipt of the Initialize Request signal from any enabled system port, the System Controller will initialize itself and send the Initialize signal out all system ports not disabled by the Port Enable switch OFF.

The system controller will not send out the initialize signal when the Initialize button on the system controller maintenance panel is pushed.

B.3.4 System Controller Commands
***

Note that some of the H-6000 commands are the same as G-635 commands. For the sake of clarity, additions and differences are shown and specified in Table 3-1 located in the main body of this specification.

The Protect Line (P) used to indicate Master/Slave mode in the G-635 has become a fifth command line in the H-6000 System Controller. Master/Slave mode are processor functions only, and are transparent to the H-6000 System Controller.

The G-635 port option shall provide the capability to accept and execute G-635 commands in a manner transparent to the G-635 system.

B.3.4.10 Read Program Interrupt Cells (XEC)
***

The format is the same as that of the G-635, except for the case of no cells set.

B.3.4.12 Connect (CON)

The G-635 "System Controller" sent the C(Y) to the selected port. The 6000 line system controller G-635 Option shall not provide this capability. Note that G-635 Systems do not utilize this capability. In all other ways, the "connect" command shall function in a manner identical to that specified for G-635 systems.

B.3.4.15.2 (b)
*** Write/Unlock; Effect on 600 Line Active Ports

Upon receipt of this command, the System Controller shall abort the operation and report an IA of "Not Control."

B.3.5 G-635 Illegal Action
***

For the sake of clarity, G-635 Illegal Action codes are shown and specified in Table 3-2 located in the main body of this specification. The System Controller G-635 port option shall provide the appropriate IA decodes in a manner transparent to G-635 hardware and software.

B.4.1.1.2 Zone Lines
***

Note that the 6000 Line zone line bit assignments and functions are identical with those of the G-635.

B.4.3 635 System Port Interface Summary

The 655 System Controller with the 655/635 system port option (see Section B.2.2) will interface with 635 active modules (processor, IOC, etc.). The 635 interface lines are provided. The characteristics of the 655/635 system port are summarized as follows:

- The 655/635 system port will perform voltage level conversion on 36 data lines and 31 ZAC lines.
- The port will generate parity on the incoming 635 Data and ZAC information.
- The 635 RAR cycle will be translated to a Read Restore cycle followed by a Clear Write cycle. Since it is possible for another port to obtain access to the same system controller between these two cycles, a 635 RAR cannot be used for gating purposes when connected to a 655 system controller.

B.4.3 (cont.)

- The 655 parity error Illegal Action codes will be lumped into the single 635 parity error Illegal Action, (i.e., 655 ZAC Data Core Parity errors will be reported to the 635 active module as a single store parity error).

- The 655/635 system port will develop the Not Master illegal action code for use by the 635 active module. The 655 does not have Not Master illegal action.

- The 655 System Controller will be pre-wired on the backpanels for a maximum of two 655/635 system ports.

B.4.4 635 Store Port - Interface Summary

The interface requirements between the 655 System Controller with the 655/635 Store Port option and an external 635 core store unit (AM8030 plus 0 or 1 AMM600) is defined in 43A164410, Core Memory Purchase Specification with one exception. The 635 core store unit shall be modified to provide two data parity lines (upper and lower) to the 655 System Controller. See Figure B.4-4.

B.4.4 635 Store Port - Interface Summary (cont.)

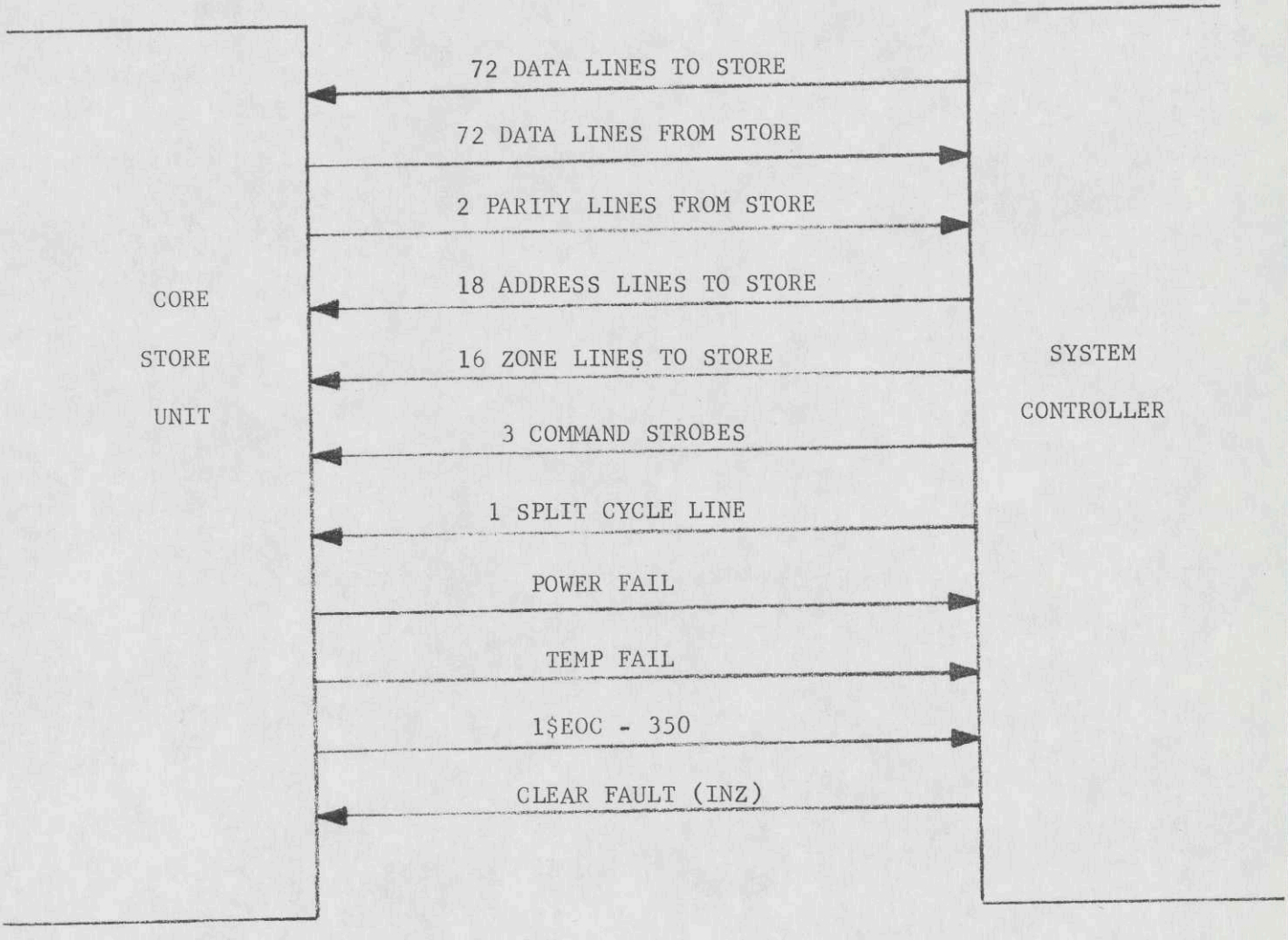


FIGURE B.4-4

STORE PORT INTERFACE

B.3.1.6 Execute Interrupt Mask Assignment Switches (A, B, C, D)
***

Note that the H-6000 System Controller has four program interrupt mask registers, whereas the G-635 System controller has only one mask register (hence only one control port).

B.3.1.7 Port Mask Switches:
***

These three position switches function the same as those in the G-625/635.

B.3.4.15.1(b) Read/Lock; Effect on 600 Line Active Ports:

***

The 600 Line RAR Command and the 6000 Line RDLK/SP both have the same command code. 600 Line Active Ports shall process this command as specified in paragraph B.4.3 (as a RRS followed by a CW1).

APPENDIX C

H-6000 B System Interface Requirements, Options, and Differences.

C.1.0 General Description

CAUTION: At this time (revision E), H-6000B requirements have not been established in approved documents. Appendix "C" cannot be considered a specification until approved System EPS-1's exist.

C.1.1 Scope

The H-6000 System Controller shall provide the capability to function in an H-6000B System. System Controller options shall be provided for this purpose, wherever unique features are required.

Most, but not all, H-6000 System Controller features/functions are compatible with 6000B requirements. This appendix specifies those areas known to impose requirements unique and different from H-6000 needs. In all cases, the overriding and controlling objective is to provide the capability to interface with specified 6000B Systems.

Therefore, the intent of this appendix is to supplement the main body of this specification for the purpose of more clearly specifying H-6000B optional connections.

C.1.2 Paragraph Number Convention:

For easier cross referencing, paragraph numbers marked *** directly supplement the content of identical paragraph numbers in the main body of this specification. As a result, Appendix "C" paragraph numbers are not in continuous (consecutive) order.

C.2.0 G-635 Port Options:

A System Controller within an H-6000B system shall not be required to interface to G-635 Active Modules or Storage Units. Therefore, the G-635 requirements of Appendix "B" are deleted for those System Controllers destined for 6000B Systems (see also paragraph 1.1).

C.2.6 Elapsed Time Clock
***

6000B Systems require System Controllers with a 52 bit/1 MHZ ETC.

C.3.3.2 H-6000 Initialization and Boot Load:
***

Initialization and Boot Load shall conform to that specified in paragraph 3.3.2. The Port Mask bits shall be set/reset as specified in paragraph 3.3.2 (b) (1).

C.3.4.13.5 Elapsed Time Clock (RGR-ETC)
***

6000B Systems require the 52 bit ETC. The RGR-ETC command response specified for the 52 bit clock conforms to this requirement.

C.3.4.15 Lock/Unlock Function
***

The 6000B System requires System Controllers with this capability.

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D E

TITLE: ENGINEERING PRODUCT SPECIFICATION, PART 1
GE-655 SYSTEM CONTROLLER

Prepared by: K. A. Edwards 8 April 1969
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