Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

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DSC181/DSC190 Controller

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1. GENERAL DESCRIPTION

This document specifies the controller requirements for the DSC181 and DSC190 Removable Media Disk Storage Controller. The basic elements of the controller are:

- MPC - Microprogrammed Peripheral Controller
- LA - Link Adapter
- CA - Controller Adapter
- Microprogram - Personalized control store firmware

1.1 INTRODUCTION

This Engineering Product Specification, Part 1, will describe in detail the interface presented to the external user's systems (EUS) by the DSC181/190 controller.

The controller comprises several pieces of hardware, however, the majority of this specification will treat it as a single box, since the external interface presented by the controller is the primary concern.

The controller is intended to satisfy a variety of needs. A subsystem may be configured in many different ways to meet data availability and throughput requirements. Refer to the DSS181/190 Subsystem EPS-1, 43A239851 for subsystem characteristics and capability.

Because the subsystem uses a microprogrammed control unit as part of the controller, the versatility and especially the adaptability to new requirements are significantly increased.

A major feature of the subsystem is the capability of using multiple sector lengths (of 288 or 1440 bytes or one sector per track) and other formats including sector lengths of the IBM format. The specific format implemented is a firmware option of the controller. This EPS-1 defines the initial format of the basic subsystem and includes the capabilities which are offered as options.

This EPS-1 covers the ultimate controller requirements for the DSS181 and DSS190. Not all of the features will be implemented initially on the DSS181. Refer to DSS181/190 Subsystem EPS-1, Section 1.8 for implementation phasing.

1.2 APPLICABLE DOCUMENTS

EPS-1 -	GECOS File System	43A233715
CPB 1518C	GE-600 Line Comprehensive Operating Supervisor(GECOS-III)	
EPS-1 -	Microprogrammed Peripheral Controller (MPC)	43A177875
EPS-1 -	PSI Link Adapter (LA)	43A177879
Purchase Specification -	DCT170 Disk Pack	M50EB00747
EPS-1 -	General Design Requirements Specification for GE-655 and GE-355	43A177851
EPS-1 -	DATANET-355	43A219609
EPS-1 -	GE-655 IOM Input/Output Multiplexer	43A219604
EPS-1 -	DSS181/DSS190 Subsystem	43A239851
EPS-1 -	Peripheral Subsystem Interface (PSI)	43A177874
EPS-1 -	Mass Storage Device Level Interface (DLI) BL0026, FSP-IF-300	
EPS-1 -	655 IOM Peripheral Subsystem Interface Adapter	43A177880
MPC	Microprogramming Reference Manual	MPC-1
EPS-1 -	DSC175/180 Controller	43A177863
EPS-1 -	DSU181 Disk Storage Unit	59A301822

AREA OBJECTIVES for NPL Microprogrammed Peripheral Controller (MPC) Document BL0021 Rev. 0 Draft 1

NPL Disk Subsystem Functional Specification NPL-FSP-MS-000, Order Number BL0004

Purchase Specification DSU190	59A301821
Common MPC Maintainability Specification	43A237500

NDM400 Mass Storage Device BL0034

NPL Peripheral Subsystem Interface Functional Specification FSP-IF-100. Order Number BL0000

NPL Mass Storage Subsystem Area Objectives, Number AOB-MS-000, Order Number BL003

EPS-1 DATANET 355/Mass Storage Link 43A232270

EPS-1 355 Computer Peripheral Subsystem Interface Channel (PSIC) 43A999997

1.3 DEFINITIONS

The following definitions are provided to be consistent with related documents.

EUS External User System. EUS refers to any 355 or 6000 line computer system with its associated peripheral subsystem interface (PSI).

PSI Peripheral Subsystem Interface. Refer to the PSI EPS-1, 43A177874.

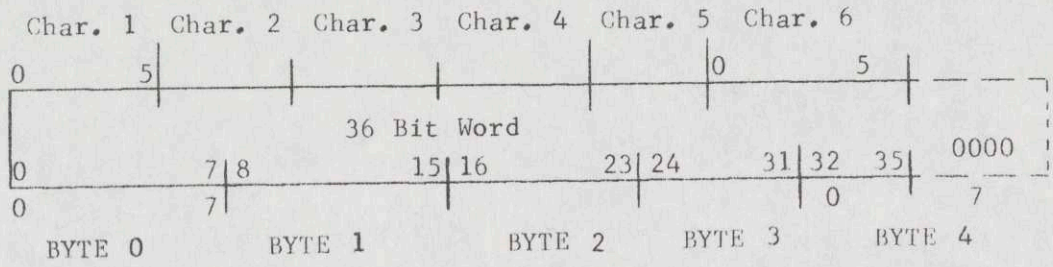
CHARACTER Six bits of information (as opposed to eight or nine bits)

WORD Six characters, 36 bits, referring to 6000 system word size (2 words contain 9 bytes)

BYTE Eight bits of information

DATA Data formats are described as either 6000 words (36 bits) or bytes (8 bits). Odd MOD words are described as four and 1/2 bytes with the addition of four zeros to match the byte PSI interface. The relationship of bits, characters, bytes and words is shown below.

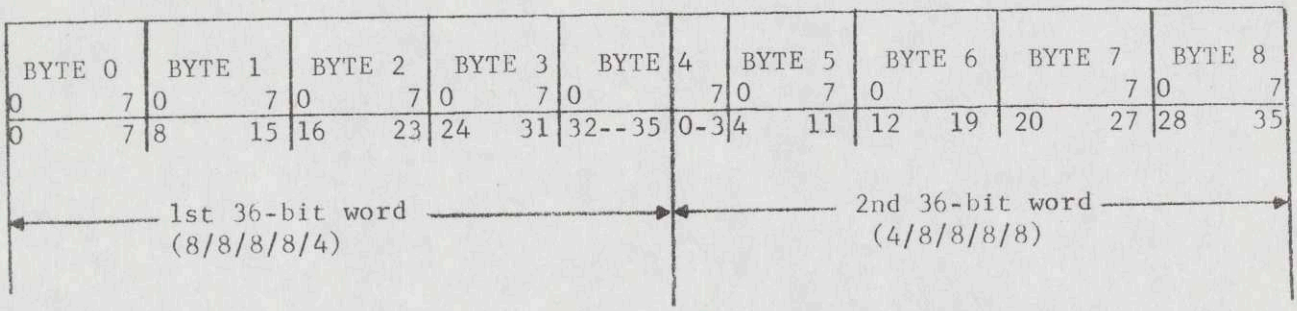
6 Bit Character



8 Bit Byte

Binary Data Transfer

The bytes are mapped into a pair of 36-bit words as shown below:



These are nine bytes per 72 bit word pair. The first 36-bit word is referred to as the 8/8/8/8/4 word, the second 36-bit word as the 4/8/8/8/8 word.

The bytes are transferred across the interface in the order Byte 0, Byte 1 . . . . . , Byte 8.

ASCII Data Transfer

The bytes are arranged in a 36-bit word as shown below:

0	BYTE 0	0	BYTE 1	0	BYTE 2	0	BYTE 3
	0 7		0 7		0 7		0 7
0	1 8	9	10 17	18	19 26	27	28 35

Bits 0, 9, 18 and 27 of the 36-bit word do not appear on the PSI. They are not sent to the MPC during a write, and forced to 0 for storage in memory during a read.

LA Link Adapter

CA Controller Adapter

ITR Isolation Test Routines

MPC Microprogrammed Peripheral Controller

DSC Disk Storage Controller

IOM Input/Output Multiplexer

DLI Device Level Interface

IAI Internal Adapter Interface

DSU Disk Storage Unit

SECTOR Physical description of data between gaps. Random addressable.

RECORD Data specified by one command, that is, part of sector or several sectors.

DEVICES Disk Storage Unit

DSS Disk Storage Subsystem

64 WORD SECTOR 288 bytes, 384 characters

320 WORD SECTOR 1440 bytes, 1920 characters

CONTROLLER MPC, LA, CA

COMMAND Operational instructions from EUS (read, write, etc.)

CHANNEL EUS connection path to the subsystem

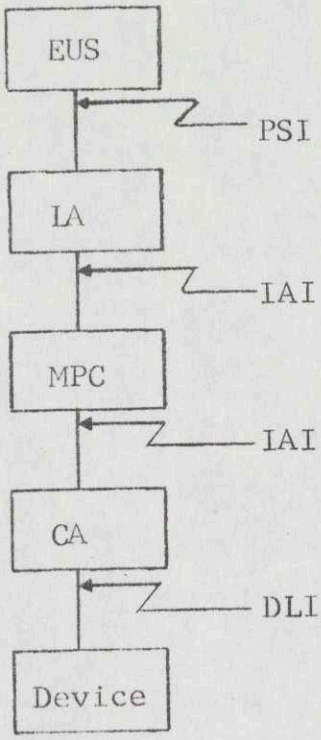
LOGICAL CHANNEL IOM multiplexed connection path for a transaction, that is, a channel program (IDCW, DCW's)

RPS Rotational Position Sensing

EDAC Error Detection and Correction

LOS Level of Simultaneity

TOLTS Total On-Line Testing System



External User System

Peripheral Subsystem Interface

Link Adapter

Internal Adapter Interface

Microprogrammed Peripheral Controller

Internal Adapter Interface

Controller Adapter

Device Level Interface

Device

2. FUNCTIONAL DESCRIPTION

The DSC181/190 controller provides the control for performing data formatting, positioner control, data path switching, file protection, head switching and associated functions required to reliably read and write data. Access to the controller by the 6000 system or DATANET 355 is via the Peripheral Subsystem Interface (PSI). Access to the drives is via the Device Level Interface (DLI). Interface connections to the system and device is shown in Figure 2.

Refer to the DSS181/DSS190 Subsystem EPS-1, 43A239851 for subsystem functionality.

2.1 SUMMARY OF CONTROLLER FUNCTIONS (See Section 1.3 for Abbreviation Explanations)

- Provide a variety of hardware configurations for single channel and dual cross-barred channel operations.
- Provide dual simultaneous transfer from two devices.
- Issue the necessary DSU181 commands to write the headers, sector gaps and data areas required to format the M4180 disk packs in fixed sector lengths of 288, 1440 bytes or one sector per track.
- Perform conversion of the continuous binary addresses received from the EUS to the non-continuous cylinder-head-sector addresses of the subsystem devices.
- Perform file protection by limiting the data sectors available to the processing system following each instruction. The sectors available-per-seek-instruction shall be specified by the processing system and can vary from 1 to 4096 (an entire cylinder or multiple cylinders).

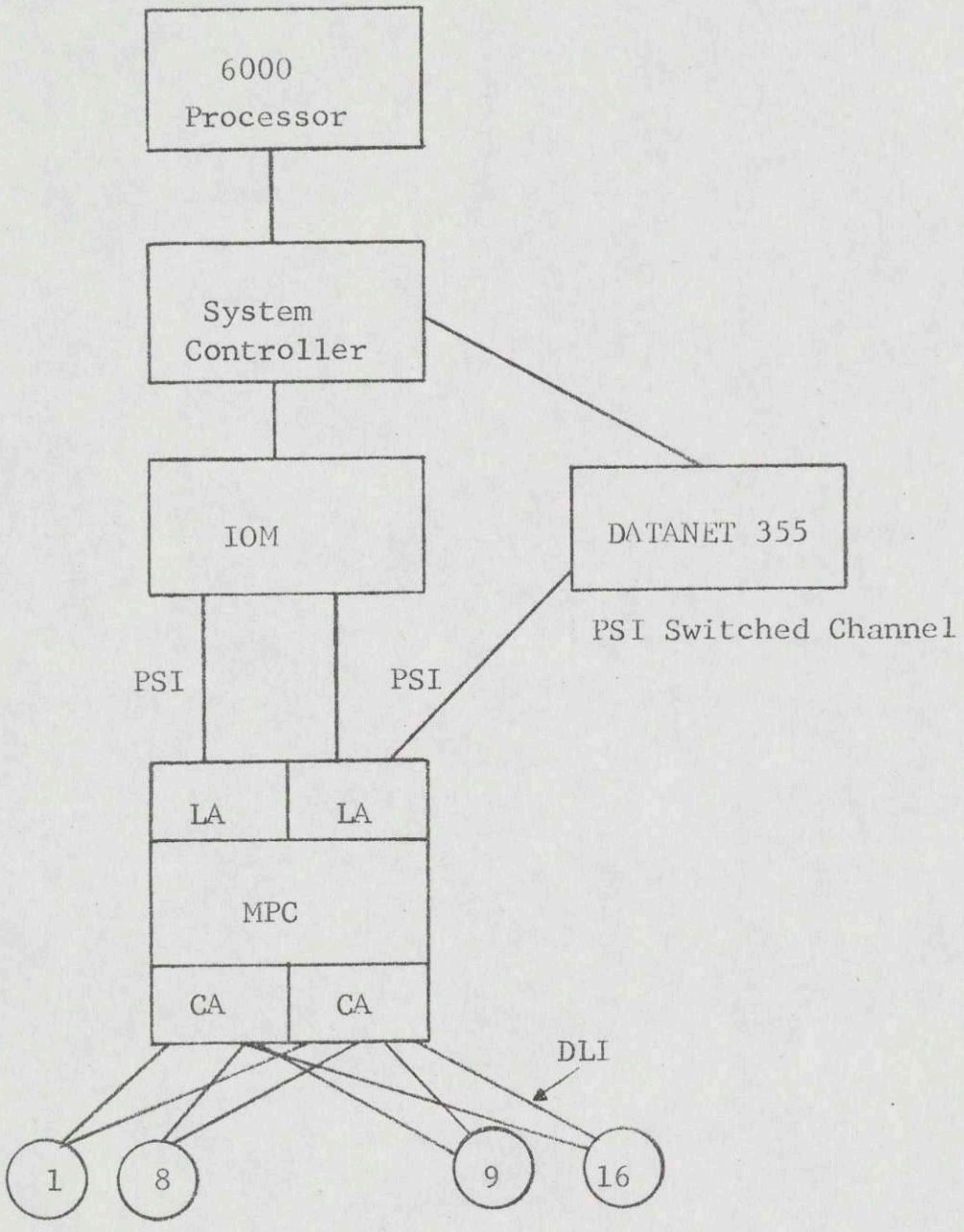


Figure 2. 6000 System with Dual Channel and Mass Store Link

- Issue the necessary DSU190 commands to write the headers, sector gaps and data areas as required to format the DSU190 disk packs in fixed sector length of 288, 1440 bytes or one sector per track.

- Perform status formatting necessary to reflect subsystem status to the EUS.

- Read and write multiple sequential data sectors as specified by the EUS processing system.

- Provide the means for the EUS to load the controller with new parameters to reconfigure the operating interface of the subsystem or a single device.

- Provide an interface to the Isolation Test routines resident in the controller for test and diagnostics aid in locating malfunctions. The interface for command and response communication between the controller firmware and the Isolation Test routines is defined in EPS-1, 43A237500.

- Provide maximum possible protection against accidental alteration of command execution routines which may be stored in the controller memory.

- For on-line maintenance purposes provide on command the detailed status information as generated by the subsystem, and retained either in core or hardware registers.

- Provide the ability to accept one additional command for each device after a given seek has been issued. See Section 5.6.4 for a discussion on command stacking. Proper use of this feature can increase throughput but improper use will decrease subsystem throughput.

- The communication interface between the controller and the EUS is defined to be the Peripheral Subsystem Interface (PSI).

- Storage of the address and control information associated with the last seek will be provided at the device level for all devices in the subsystem.

2.2 RECORD LAYOUT DSC181

Each device has a total of 203 cylinders. There are 203 tracks on each disk surface, and 20 heads per cylinder, for a total of 4060 tracks maximum. By convention, tracks on each disk surface are numbered from zero to 202, with 202 being the innermost track.

Cylinders are also numbered from zero to 202. Space allocation on the disk pack shall conform to the following:

- Cylinder 0 through 201 (4040 tracks); User Data, Systems Labels, Catalogs, Alternate Tracks, etc.
- Cylinder 202 (20 tracks); Must be reserved for T&D use only.
- The track format is in fixed sector lengths of 288, 1440 bytes and one sector per track.

2.3 RECORD LAYOUT DSS190

Each device has a total of 411 cylinders. There are 411 tracks on each disk surface, and 19 heads per cylinder for a total of 7809 tracks maximum. By convention, tracks on each disk surface are numbered from zero to 410, with 410 being the innermost track.

- Cylinders are also numbered from zero to 410. Space allocation on the disk pack shall conform to the following:
- Cylinder 0-409; User Data, Catalogs, Alternate Tracks, etc.
- Cylinder 410 (19 tracks); Must be reserved for T&D use only.

- The track format is in fixed sector lengths of 288, 1440 bytes and one sector per track.

2.4 STORAGE FORMATS

The DSS181 subsystem hardware includes the capability of fully implementing the IBM 2314A1 format. The CA is capable of formatting, reading and writing data fields as well as key fields. Data processing is accomplished on a field basis, with firmware supplied control identifying the fields and their contents. Thus the format of the track is the responsibility of the controller firmware.

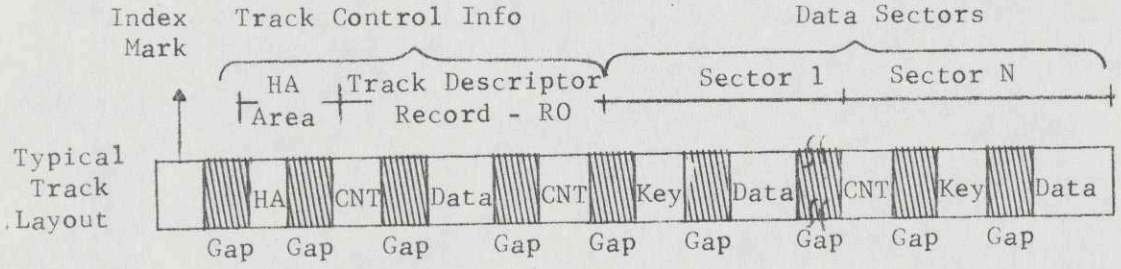
Initial operational requirement of the EUS is met by the implementation of fixed sector lengths with no key fields.

The above EUS requirements are met in the design of the controller microprogram and will not be constraints upon the hardware design. If the EUS requirements should change to different sector lengths, and/or the use of key fields, only the controller firmware would require change.

2.4.1 Basic Format (IBM 2314A1, reference only)

Track Layout:

A typical track layout is pictured below:



The track layout is characterized by the following summary:

a. Each track contains "Home Address" field, one per track.

b. Each track has one unique "Record Zero" sector. This sector may contain either count and data field, or count, key and data field. Normally, this sector is not used for User Data Storage. For the DSS181, the key field is not present and the data field is eight bytes long.

c. User Data Sectors may contain either count and data field, or count key and data field.

d. The count field of a sector is fixed in length (9 bytes).

e. The key field of the sector (if present) can vary in length from 1 byte to 255 bytes.

f. The data field of a sector can vary from 1 byte to 7294 bytes.

g. The length of the data field can be set to zero. If so, an End-of-File status condition is indicated when the field is read.

h. "Gaps" between fields, within a sector, are fixed in length. "Gaps" between sectors are variable and a function of the length of the key and data field.

i. Lengths of the fields of a sector are measured in bytes (8 bit multiples), as opposed to lengths being measured in words (36 bit multiples) or character (6 bit multiples).

j. A "sync byte" (the first byte in every field) identifies the type of field.

k. The last four bytes of every field are identified as:

Burst CK	Burst CK	ID Byte	Bit CNT

where:

Burst CK - Cyclic code bytes for error detection.

The CA computes the two cyclic check bytes. The first check byte is the exclusive OR of all the even numbered bytes written in the sector. The second check byte is the exclusive OR of all the odd numbered bytes written in the sector.

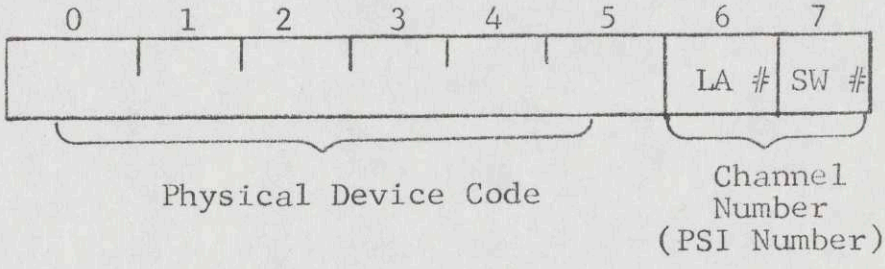
For a write operation, the two cyclic code bytes are added to the end of the field and written on the track.

On a read operation, the exclusive OR process is repeated until the cyclic code bytes at the end of the record are operated upon. If no error has occurred, the result is all 0's in the cyclic code check registers. The cyclic code check bytes are called burst bytes. The cyclic code check used has the following checking properties.

1. Detects all errors in which an odd number of bits are wrong.

2. Detects single bursts of error that are 16 bits or less in length.

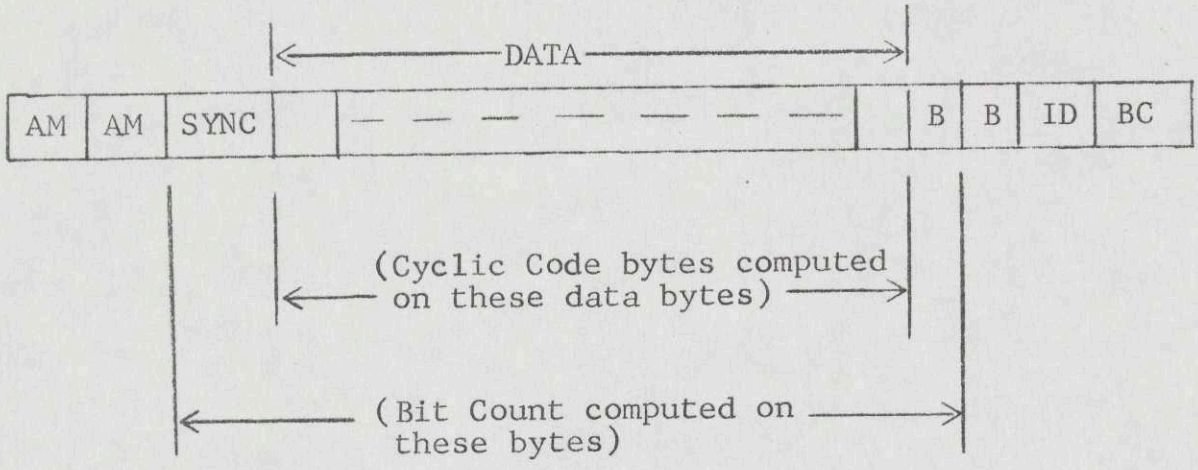
ID Byte = This byte identifies the physical device number and channel number of the device used when this byte was written on the track.



Bit CNT = Bit count check byte. This byte records, modulo 256, the number of one-bits written in the field in one's complement form. Functionally, this byte is included as another code checking byte. Failure to compare the bit CNT is the same as a cyclic check compare failure.

These last four bytes are not part of the data of a field and are not normally transmitted beyond the controller.

The above description of the last four bytes pertains to IBM 2314 Model A1 Subsystems. In earlier, Model 1, subsystems the ID byte and bit count byte are not included -- A field ends with the two burst check bytes. The four bytes described above will be written on the device in the manner of Model A1.

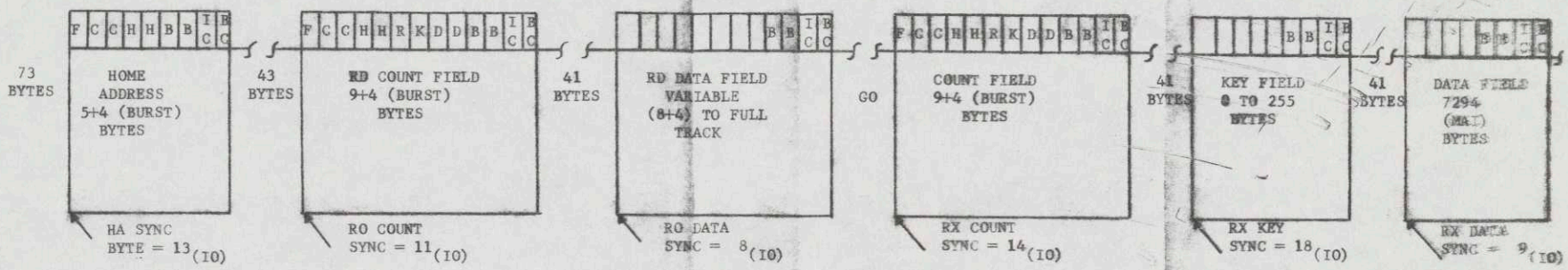


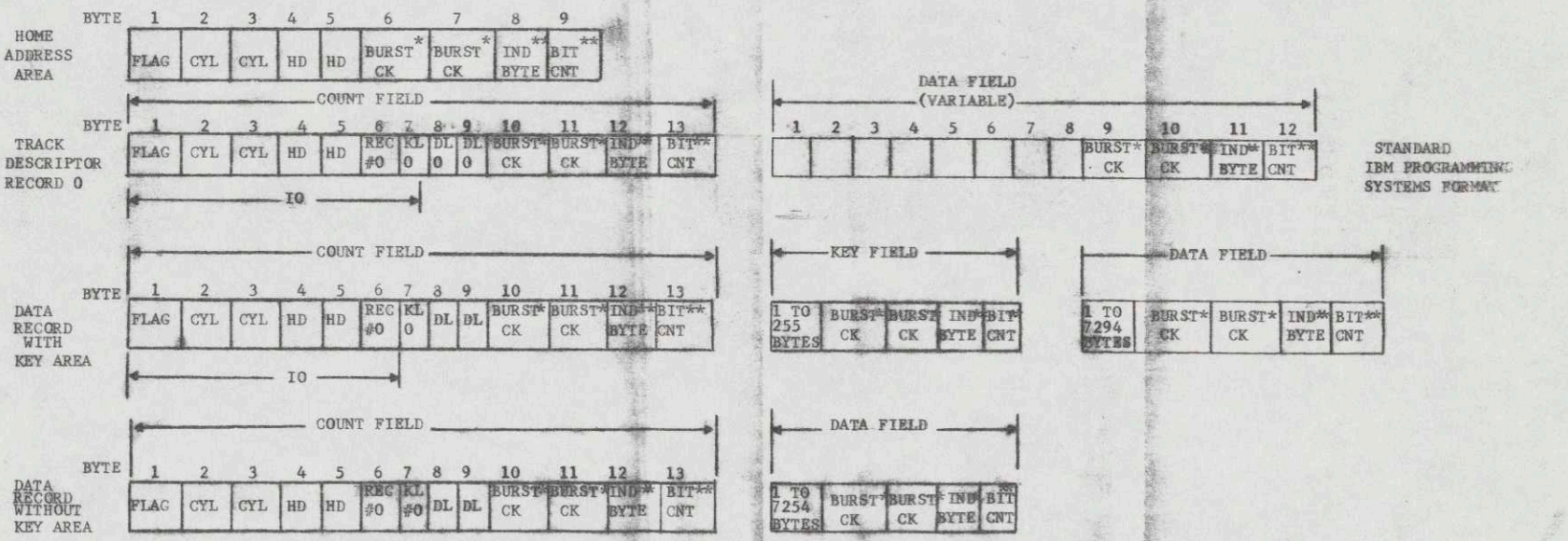
Field Structure

The fields discussed above exhibit the following structure.

In the above structure:

F = Flag Byte
CC = Cylinder Number in Binary
H = Head Number in Binary
R = Track Record Number in Binary
K = Key Field Length in Binary
DD = Data Field Length in Binary
GO = 43 Bytes if RO Data Length is 8
GO = 43 + .043 (DL) if RO Data Length > 8 Bytes
GN = 43 + .043 (KL + DL)
BB = Cyclic Burst Byte
IC = Indicator Byte
BC = Bit Count Byte

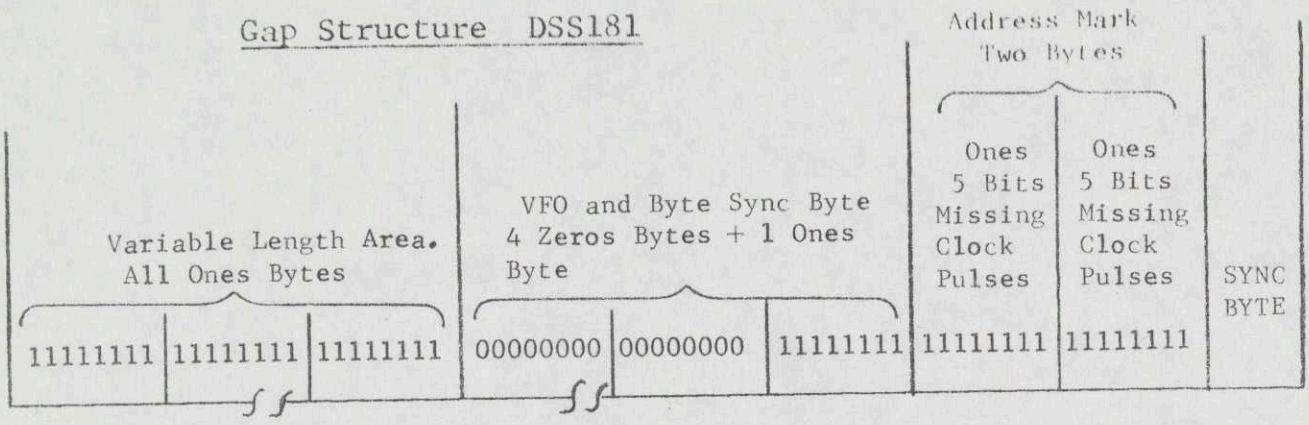




*CYCLIC CODE CHECK

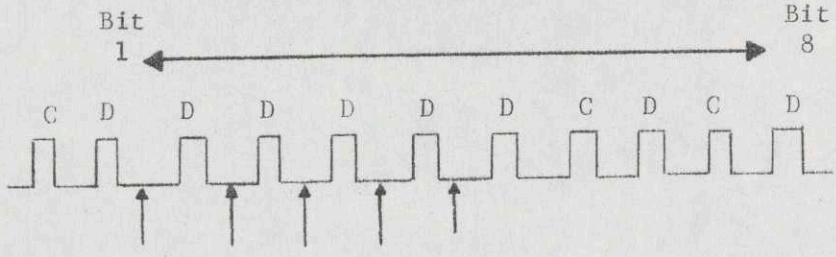
**INDICATOR AND BIT COUNT BYTE CONSTITUTE BIT COUNT APPENDAGE (BCA)

Gap Structure DSS181



Total gap length is 41 bytes between fields; 43 bytes between HA and RO count field; and 43 + .043 (DL + KL) between sectors. KL and DL are the lengths (in bytes) of the key and data fields of the preceding sector. Control firmware is responsible for calculation of the factor $\frac{K_L + DL}{23+65/256}$ during format operations. If KL = 0 and DL = 288 bytes, for example, then the gap length is 55 bytes.

The Address Mark is a special configuration of clock/data bits which indicate to the CA or device the beginning of a field.



Address Mark Byte. The arrows indicate missing clock bits.

C = Clock Bit D = Data Bit.

The Address Marks are the only areas on the track in which data bits are not separated by clock bits. This special condition, then, could not occur erroneously within a field. The CA or device hardware is charged with the responsibility of writing the AM at the beginning of each field, and detecting the AM at the beginning of each field on read operations.

2.4.2 Basic Subsystem 64 and 320 Word Format

The following paragraphs describe functions in terms of the CA and microprogram subsystem.

1. The subsystem shall be able to read and write disk packs in the general format described in paragraph 2.4.1, but for a fixed data length of 288 bytes, 1440 bytes and one sector per track.

2. The subsystem shall be able to read disk packs generated by the IBM 2314 Model 1 and Model A1 subsystems.

3. The subsystem shall be able to write sectors in the format of the IBM 2314 Model A1 subsystem only.

4. The subsystem will format an entire track of either 288 bytes, 1440 bytes or 7200 bytes, sectors upon receipt of a "Format Track" command from the EUS. The track shall conform to the IBM format and shall contain the following areas:

   One Home Address Area (HA)

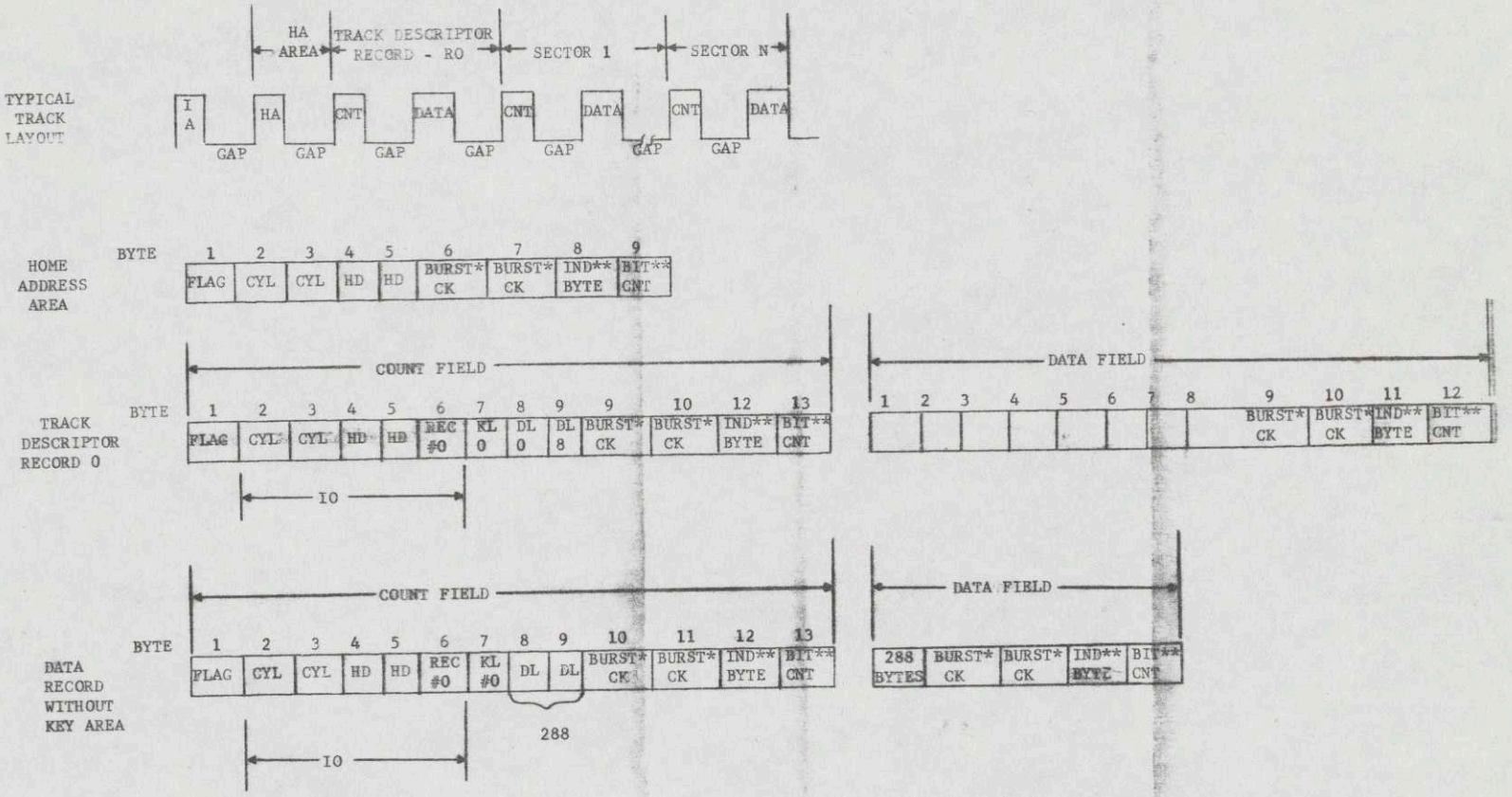
   One Record Zero Sector (R0 count field plus a data field DL of 8 bytes; no key field)

   Eighteen Data Sectors (each with a count field plus a data field DL of 288 bytes; no key field), or

   Four Data Sectors of 1440 bytes, or

   One Data Sector per track (DSS181 - 7200 bytes and DSS190 - 12960 bytes)

Basic DSS181 Format

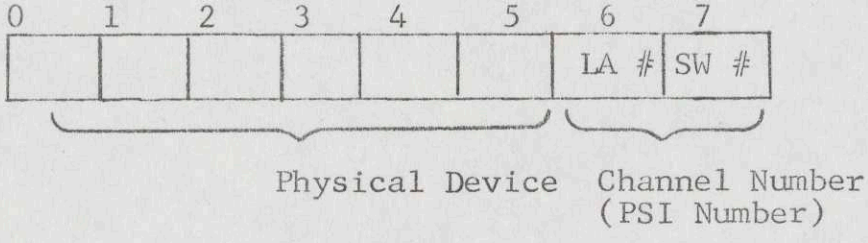


*CYCLIC CODE CHECK
**INDICATOR AND BIT COUNT BYTE CONSTITUTE BIT COUNT APPENDATE (BCA)

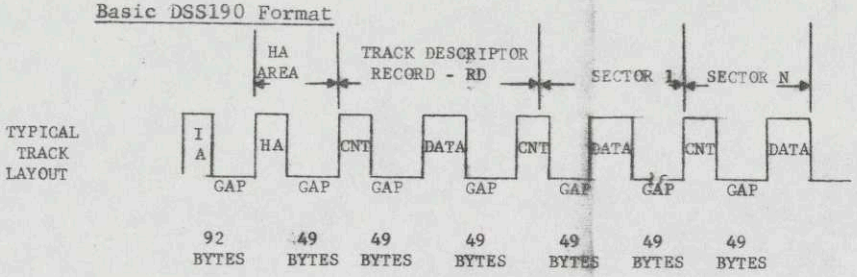
2.4.3 Basic Data Format

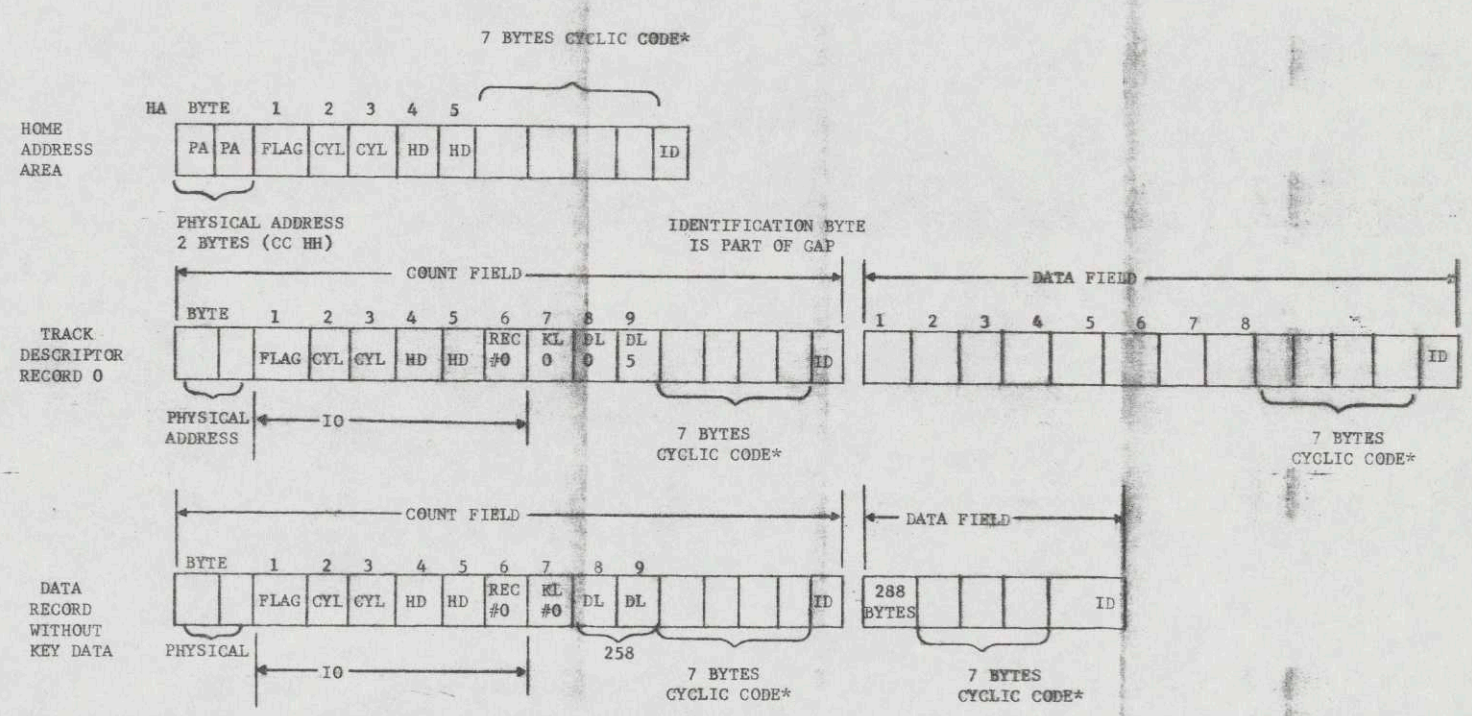
In the above structure:

I = Index Mark
HA = Home Address
CNT = Count Field
FLAG = Flag Byte
CYL = Cylinder Number in Binary
HD = Head Number in Binary
REO# = (Record) Sector + Number in Binary
KL = Key Field Length
DL = Data Length in Binary
ID = Identification Byte
Cyclic Code = 7 byte EDAC Code
PA = Physical Address
ID Byte = This byte identifies the physical device number and channel numbers of the device used when this byte was written on the track.



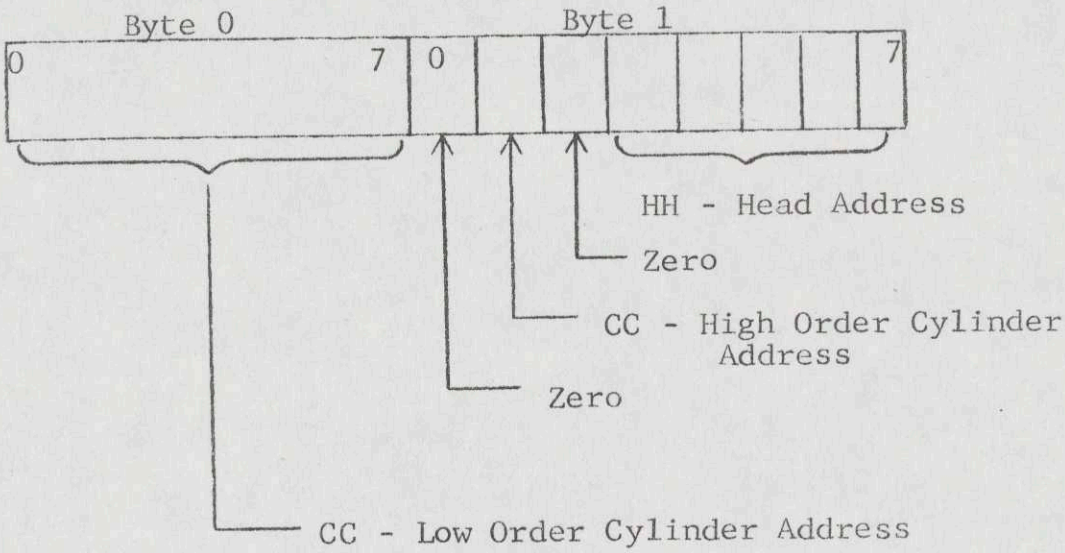
Basic DSS190 Format



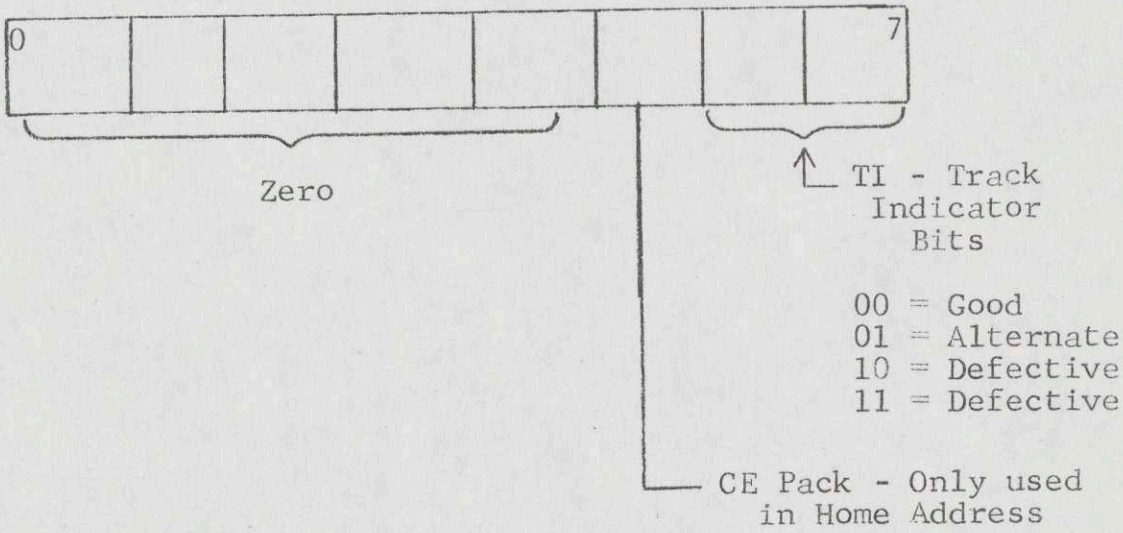


*Refer to Section 5.8.4 for the cyclic code to be used, EDAC Error Detection And Correction.

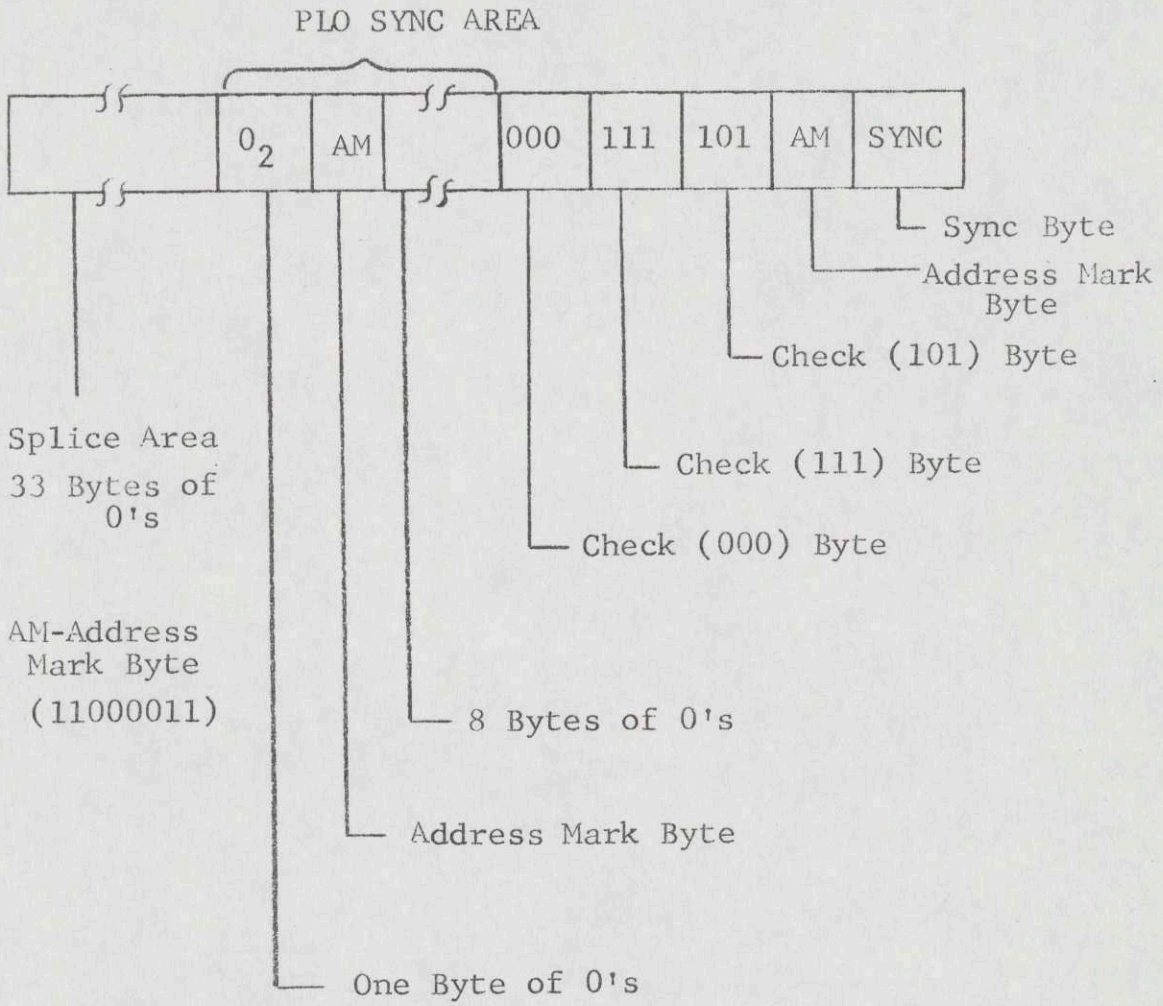
Physical Address



Flag Byte



GAP Format DSS190:



3. COMMAND DESCRIPTION

The controller will provide the following command set for use by the External User Systems. The last column indicates those commands which will be rejected with invalid device code based on the incorrect use of the device code.

Table of commands valid for device/controller

COMMANDS	BIT CODE	OCTAL CODE	LEGAL DEVICE CODE
Seek	011 100	34	D
Special Seek (T&D)	011 110	36	D
Preseek	011 111	37	D
Restore	100 010	42	D
Read	010 101	25	D
Read ASCII	010 011	23	D
Write	011 001	31	D
Write ASCII	011 010	32	D
Write and Compare	011 011	33	D
Read Nonstandard Size	000 100	04	D
Read Track Header	010 111	27	D
Format Track	001 111	17	D
Request Status	000 000	00	E
Reset Status	100 000	40	E
Read Control Register	010 110	26	E
Write Control Register	001 110	16	D
Read Status Register	010 010	22	E
Read EDAC Register	010 001	21	D
Release	111 110	76	D
Reserve Device	111 111	77	D
Set Standby	111 010	72	D
Bootload CS	001 000	10	C
ITR Boot	001 001	11	C
Execute Device Command (DLI)	011 000	30	D

Special Controller Commands - see Section 3.21

D = Device Only
E = Either
C = Controller Only

COMMAND (BIT) STRUCTURE

High \ Low	000	001	010	011	100	101	110	111
000	Req. Status				Read Non-Standard Sector Size			
001	Boot C.S.	ITR BOOT					WCR Write Control Register	Format
010		Read EDAC RER	RSR	Read ASCII		Read	RCR	Read Header
011	Execute Device	Write	Write ASCII	Write & Compare	Seek		Special Seek	Pre-Seek
100	Reset Status		Re-store					
101								
110								
111			Set Standby				Release	Reserve Device

SPECIAL CONTROLLER COMMAND
(BIT)STRUCTURE

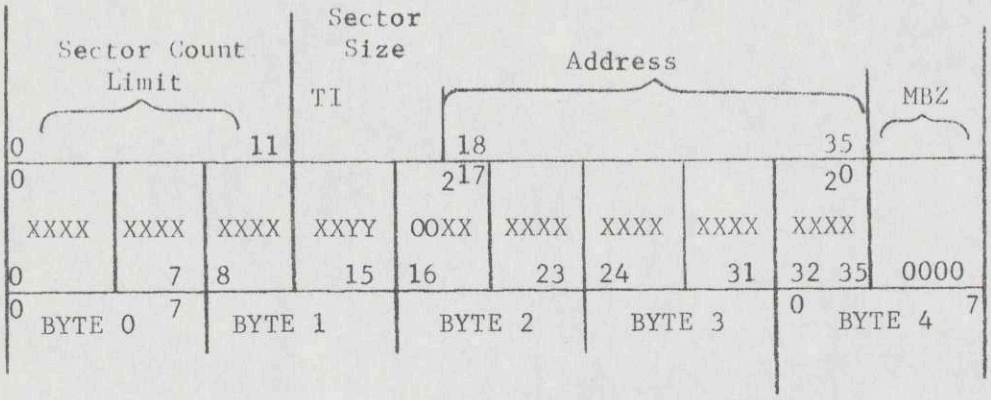
(Refer Section 3.21)

High \ Low	000	001	010	011	100	101	110	111
000	Suspend Controller		Read Controller Main ASCII		Read Lock Byte		Initiate Read Data	
001	Write Control Store		Write Controller Main ASCII		Write Lock Byte		Initiate Write Data	
010	Release Controller		Read Controller Main Binary					
011	Execute Control Store		Write Controller Main Binary		Conditional Write Lock Byte			
100								
101								
110								
111								

3.1 SEEK

During the I/O command sequence, when this instruction is received, the controller will check the IDCW. If an error condition is detected, the controller will terminate the instruction and report appropriate status. The seek command will perform an implicit reservation of the addressed device to the logical channel until the data transfer command that follows the seek is terminated, if there is no data transfer command following the seek, over the same logical channel the controller will release the device after positioning is complete. If the device code is valid the controller firmware will issue a request to the EUS for five seek address byres, (6 characters). If exactly five address bytes with last four bits equal zero are successfully received (no transfer timing or transmission parity alert), the controller firmware will save the sector count limit and convert the binary address to the cylinder, head, and sector format. Provided the address is valid, the controller will select the device and attempt to reserve the device to the issuing channel. If successful, it will then interrogate the device status. If an exception condition exists, the instruction will be terminated with an Attention or Device Busy status. If the device is ready, the controller will issue the required commands to the CA to perform the specified seek. The controller will at this time, terminate the instruction and report one of the status conditions to the EUS.

The five control bytes shall serve to define the specific seek operation to be accomplished as follows when fixed sector binary addressing is used.



Bits 0-11: These bits shall define the binary sector count with the file protection option. Least significant bit is 2^0 in bit position 11. Zero is a maximum count of 4096.

Bits 12-13: These two bits shall be the track indicator bits. (See Section 3.11 format track command.)

Bits 14-15: These bits shall be the sector size indicators:

YY= 00 64 Word, 288 bytes or one record per track

YY= 01 320 Word, 1440 bytes or one record per track

YY= 10 64 Word Seek Algorithm, one sector per track (must be used to format a one sector track on a pack where the rest of the sectors are of the 64 word format)

YY= 11 320 Word Seek Algorithm, one sector per track (must be used to format a one sector track on a pack where the rest of the sectors are of the 320 word format)

When addressing one sector per track with either YY = 10 or YY = 11 the binary address must decode to sector zero (first data sector). If the binary address does not decode to sector zero and the track is formatted with one sector per track (7200 or 12960 bytes) then MPC Data Alert sector size error will be returned.

Bits 18-35: These bits shall define the specific binary sector address to be located on the addressed device. Least significant bit is 2^0 (2^3 bit in byte 5), bit position 35.

Data Alert, Invalid Seek Address status shall result if other than five bytes are received or the last four bits of byte 5 are not zeros, during the instruction execution.

If a seek (or preseek) instruction decodes to any sector on track 202 for the DSS181 (or track 410 for the DSS190), the T&D tracks, it will be rejected with "Data Alert, Invalid Seek Address" status.

Seek instructions or special seek instructions following a restore that are received while the file is positioning will be accepted and will be executed after the file has completed the positioning operation.

The controller will terminate the Channel Busy state with appropriate termination status as shown in Table 4.

Off-Line Execution: Upon completion of the seek instruction command sequence (indicated by the reflection of Channel Ready status to the EUS upon termination of the busy state), the controller will have initiated the seek operation. The device to which the seek instruction is addressed will remain reserved to the logical channel that issued the seek until data transfer is complete or positioning is complete if no data transfer command follows. The device will be released by a release instruction or upon execution of a subsequent data transfer instruction. (Refer to Section 3.19, Device Reserve.) In multiple device subsystems, all devices may be in simultaneous off-line positioning operations. The controller will store the control information and address for each seek operation, so that it will not be necessary for the EUS to reissue a seek instruction prior to a data transfer command in the same channel program.

3.2 SPECIAL SEEK

Special seek is provided for Test and Diagnostic use; however, there are no restrictions within the controller on the use of this instruction by other EUS activities. It is identical in use to the seek instruction (see Section 3.1) except that the continuous binary address must reference a sector or cylinder 202 for DSS181; (410 for DSS190), the T&D cylinder.

Thus, if this instruction is addressed to a sector on any cylinder other than the T&D cylinder, it will be rejected with "Data Alert, Invalid Seek Address."

Upon termination of the Special Seek instruction, appropriate termination status and substatus will be reflected to the EUS: (Refer to Table 4.)

3.3 PRESEEK

The Preseek instruction will be executed as though the EUS had issued a Seek instruction except the preseek may not be followed by a data transfer command. In nearly all other respects, it will be treated the same as the Seek instruction. Except, a "Seek Incomplete" condition in the device will cause the controller to automatically restore the device but no retries will be attempted. The controller will not issue a special interrupt to the EUS channel. (See Section 5.6 for considerations on the reporting of special interrupts to the EUS.)

The other difference in the preseek instruction is that it must be issued only to devices which are not reserved to the given EUS channel. If a preseek instruction is issued to a device which is already reserved to the given channel, the controller will reject the instruction with "Instruction Rejected, Invalid Instruction Sequence."

Since preseek may not be followed by a data transfer command, the EUS must issue a Seek or Special Seek instruction prior to any device data transfer instructions. It is possible that, before the given channel issues the seek, an alternate channel connected to the device may issue an instruction that reserves the device to the alternate channel. If this should happen, the original (CA channel and thus the EUS) channel will not be notified that the preseek operation is nullified.

Upon termination of the preseek instruction, appropriate termination status and substatus will be reflected to the EUS: (Refer to Table 4.)

3.4 RESTORE

When track reference is lost due to machine error or a seek incomplete occurs, recalibrate must be issued to the device to return the access mechanism of the selected device to cylinder zero to re-establish the seek reference point. The controller will automatically recalibrate the device when there has been a seek incomplete.

Instruction Execution During Busy State:

Provided that the instruction was accepted (indicated by the reflection of Channel Busy Status to the EUS), the controller will attempt to reserve the device and initiate the specified restore operation.

If the restore instruction is received when the device is busy positioning, but not reserved to an alternate channel, it will be accepted and the channel will remain busy until the physical restore operation can be initiated. At this time, the instruction will be terminated with the appropriate status and the device released.

Off-Line Execution:

The Restore instruction results in the resetting of a seek incomplete and the recalibration of the access mechanism to cylinder zero.

The Restore must be followed by a Seek or Special Seek instruction before any data transfer to or from the device can occur. The Seek may be sent immediately upon receiving the channel ready status from the Restore termination. Refer to Table 4 for status returns supplied at command termination.

3.5 READ

Instruction Execution During Busy State:

Upon acceptance of the Read instruction and completion of the I/O command sequence, the controller will check to insure that the device code is valid, and the device has been reserved to the logical channel by a previous seek. The controller will then set up for the read operation.

If the device has completed the positioning operation from the previous seek instruction, the controller will initiate the data transfer. If the device has not completed the positioning of the previous seek instruction, the controller will stack the command and wait for an interrupt from the device. Upon receiving the interrupt, the controller will interrogate the device to determine that the device actuator is on cylinder. If the device is on cylinder with no errors, the controller will initiate a search for the addressed sector, and when it is found will initiate the data transfer.

Data will be read from the file, and transmitted to the EUS. The data transfer from the device will continue until one of the following occurs:

- An error condition is detected
- Sector count limit has been reached
- Terminate out signal is received from the EUS

If, at any time during the execution of a read instruction, a Terminate-Out signal is received from the EUS, data transfer to the EUS shall

terminate immediately. However, the controller will read and check the entire sector, thus the terminate status will be that for the last sector or partial sector transmitted.

Refer to Table 4 for status returns supplied at command termination.

3.5.1 Read ASCII

The execution of this command will be similar to the Read command with the exception that the controller will send a service code to the PSIA indicating ASCII mode and the PSIA will place four 8-bit bytes in each word. (Refer PSIA EPS-1). Refer to Table 4 for status returns supplied at command termination.

3.6 WRITE

Execution of this instruction is similar to the Read instruction, except that data is transferred from the EUS to the subsystem.

Instruction Execution During Busy State:

Upon acceptance of the Write instruction (reflection of Channel Busy status), and completion of the I/O command sequence, the controller will check that the device code is valid and that the device was previously reserved by a seek command through the same logical channel.

If the previous seek operation is not complete, the controller will wait for an interrupt from the device. Upon receiving the interrupt, the controller will interrogate the device to verify that the device is on cylinder. If the device is on cylinder and no error conditions exist, the controller will initiate data transfer from the EUS.

The data transfer to the device will continue until one of the following occurs:

- An error condition is detected.
- The sector count limit has been reached.
- Terminate-Out signal is received from the EUS.

A terminate out signal will terminate the data transfer at the EUS interface. The controller will continue to transfer data to the device until all the data received from the EUS prior to the TMO is recorded. When a partial sector is received from the EUS as a result of a Terminate Out signal, the remainder of the data sector shall be filled with zeros.

Refer to Table 4 for status returns supplied at command termination.

3.6.1 Write ASCII

The execution of this command will be the same as the write command with the exception that the controller will send a service code to the PSIA indicating ASCII mode and the PSIA will take four 8-bit bytes from each word (refer PSIA EPS-1). Refer to Table 4 for status returns supplied at command termination.

3.7 WRITE AND COMPARE

The execution of the write portion of this command shall be identical to the Write instruction. After the writing takes place at the addressed device, the controller will verify the write by moving the list pointer in the IOM back to the IDCW and re-transferring the data records (as in normal retry) to the controller from the EUS and reading the just written data records from the disk, and comparing the data received.

If at any time during the execution of the compare portion of the Write and Compare command a Terminate Out signal is received from the EUS data transfer from the EUS shall terminate.

The compare operation will be performed on complete sectors. If the data received from the EUS is not a multiple of a complete sector, the controller will zero fill and compare the data for the remainder of the sector. If the controller detects an error when reading the required sectors from the device, this status will be reflected regardless of the result of the compare operation. (Refer to Table 4 for status.)

3.8 READ NONSTANDARD SIZE SECTOR*

The Read Nonstandard command will be used to obtain all the fields on a track including count, key and data fields. The format of count fields, data fields, gaps, sync bytes, address marks and error detection codes must be the same as either the DSS181 or DSS190.

Instruction Execution During Busy State:

If the instruction is acceptable, the subsystem shall revert to the Channel Busy status.

Using the cylinder and head address from the preceding seek command, the controller will read the entire track starting at index mark and transmit all the information bytes to the EUS. (Note that this includes Home Address and Record Zero as well as all count, key and data records, but does not include gaps, sync bytes, address marks and error detection codes.) Data will be transferred to the EUS starting with the flag byte of the Home Address, as continuous data bytes until termination.

*Not Available on initial DSS181

The Read Nonstandard size sector command shall read only one track each time the command is issued.

The operation will continue until one of the following conditions is met:

- An error condition is detected.
- The sector count limit has been reached.
- A Terminate Out signal is received.

If an error condition is detected during a Read Nonstandard command the controller will terminate the instruction, send a terminate interrupt to the EUS and reflect appropriate status. If at any time during the transfer of the data, a Terminate Out signal is received from the EUS, data transfer shall terminate immediately. However, the subsystem will continue to read the remainder of the field. Thus, the status will be reflected for the last field read.

The controller will bypass the checking of the TI bits on the track. This eliminates the End-of-File status returns.

If the requested track cannot be read, the controller will not send any data to the EUS and will terminate the EUS channel with Data Alert, Header Verification Error. Refer to Table 4 for status returns supplied at command termination.

3.9 READ TRACK HEADER

When the subsystem initiates the Read Track Header instruction, the contents of the home address, and record zero count and data fields are transmitted to the EUS.

Instruction Execution During Busy State:

Upon acceptance (reflection of Channel Busy) of the Read Track Header instruction, the controller will verify the device code, and provided that a seek has been issued to the device through the same logical channel, the controller will execute the instruction.

The EUS sector number (as determined from the previous seek command) is used only to position the controller on the required track, as though the previous seek were to home address of the desired track. Head switching shall not occur on a Read Track Header instruction.

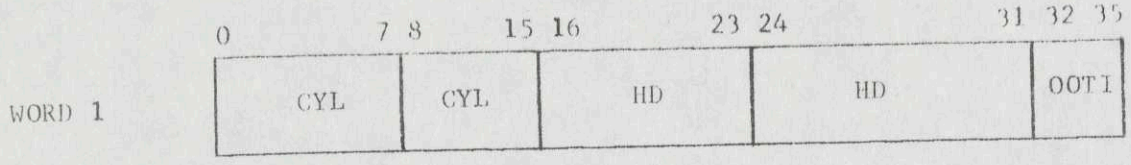
The byte oriented data maintained in the HA and R0 count and data field, will be read into the controller, before transmission of the data to the EUS is begun as a single block of data. The three fields will be sent to the EUS in the same five word format as that used for the Format Track instruction, except for one, bit 33 (Z bit) and the check character in word three bits (18-23). The "Z" bit position will always be returned as zero. The check character will not be computed and the controller will return zeros in the check character byte of word three bits (18-23). The format of the data sent to the EUS is shown below.

The amount of data transferred to the EUS will be 22 bytes, or less if the controller receives a Terminate-Out signal prior to the 22 bytes being transferred. Note that there is no conversion of the R0 data before it is sent to the EUS. The cylinder and head data in word one and two indicates the particular track on which the operation is being performed. If the CCHH in the home address does not agree with the CCHH computed from the Seek Address, the data will be sent to the EUS and the operation will be terminated with "Data Alert, Header Verification Error."

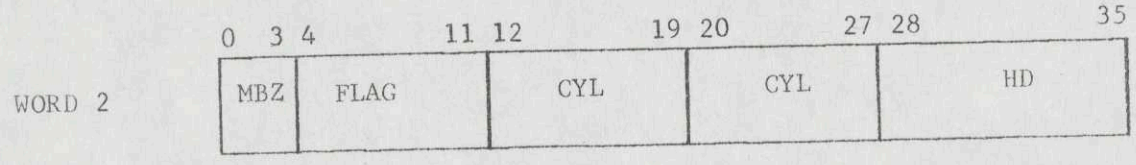
In the event an error condition is detected during a Read Track Header operation, the controller will terminate the instruction, send a terminate to the EUS, and reflect appropriate status.

If at any time during the execution of a Read Track Header instruction, a terminate out signal is received from the EUS, data transfer will terminate immediately. However, the subsystem will have read and checked the entire header so that appropriate status will be reflected. Refer to Table 4 for status returns supplied at command termination.

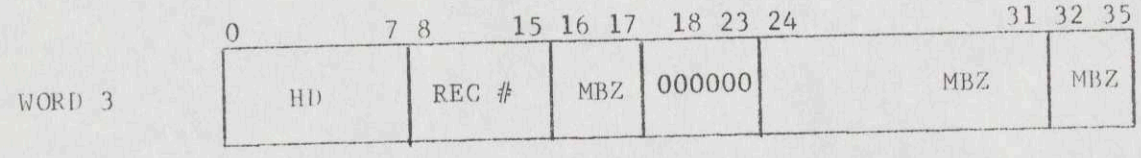
HA Home Address



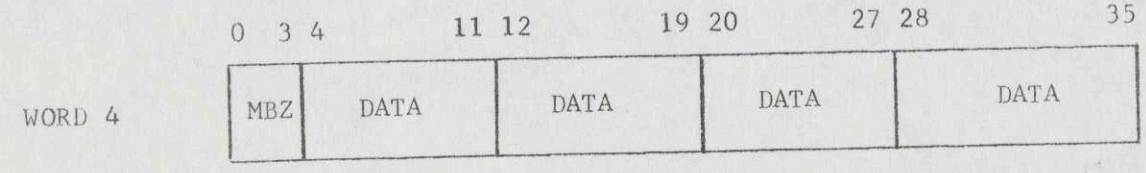
R0 COUNT FIELD



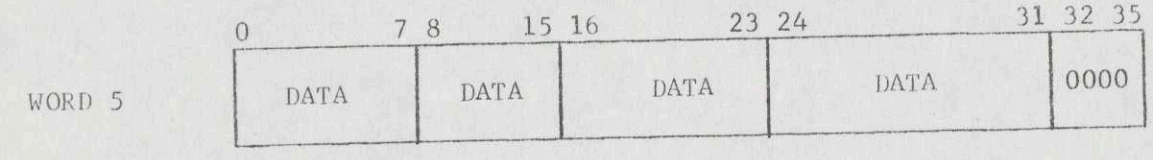
R0 COUNT FIELD



R0 DATA FIELD



R0 DATA FIELD



3.10 FORMAT TRACK

The Format Track instruction provides the means to format a complete track as a good, defective or alternate track. This instruction results in all headers, address marks, gaps and data fields being recorded on a given track, beginning at the Index Mark. (See Section 2.4.1 and 2.4.3 for a description of the track format.) The specific track is defined by the last Seek (or Special Seek) instruction sent to the device. The Seek instruction must immediately precede the Format instruction in the same DCW list, within the same channel program. Otherwise, the Format instruction will be rejected with "Instruction Rejected, Invalid Instruction Sequence."

Certain data provided by the EUS in the Seek and Format instruction data fields will be recorded on the track.

Except for Record Zero, the controller will write zeros in the data fields of all sectors on the track. The TI (Track Indicator) bits from the preceding Seek instruction will be written in the flag byte for the Home Address and the count fields of all records on the track, except Record Zero.

The TI bits will have the following meanings:

00 - Primary Track-Good

01 - Alternate Track-Good

10 - Defective Track - Alternate Assigned

11 - Defective Track - No Alternate Assigned

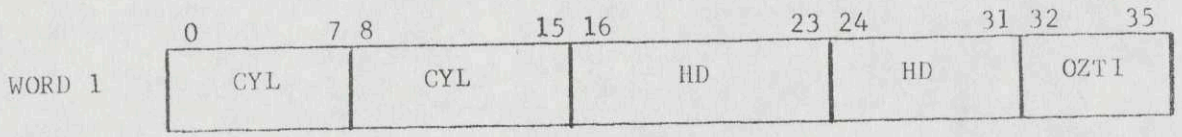
Instruction Execution During the Busy State:

The controller will first determine if the instruction itself can be processed by verifying the device status is good and that the Format instruction to the device was immediately preceded by a Seek instruction (or Special Seek, if the T&D cylinder is to be used). If the operation cannot be continued, the controller will terminate with the appropriate status.

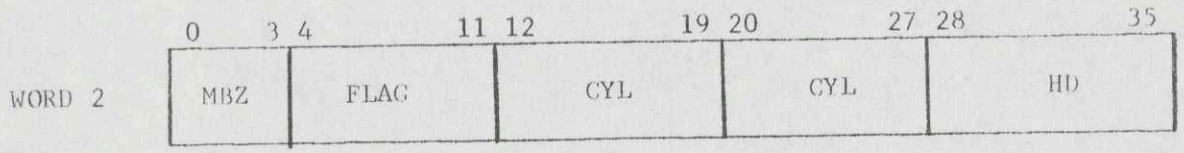
If the operation can be continued, the controller will always request five, 36-bit words (22 1/2 bytes) of data. If exactly 22 1/2 bytes are not received, the controller will terminate the instruction with "Instruction Rejected, Invalid Instruction Sequence."

The format of the data will be as follows:

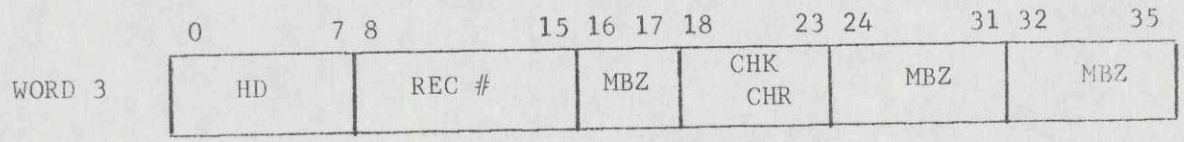
SEEK VERIFICATION DATA



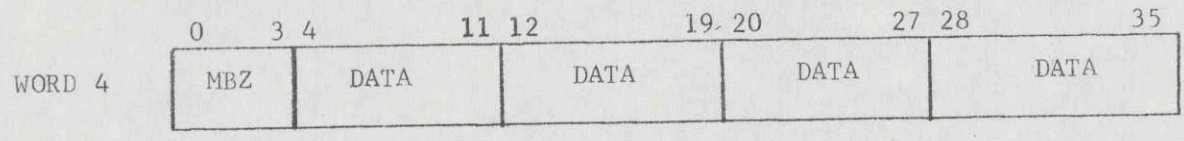
RO COUNT FIELD



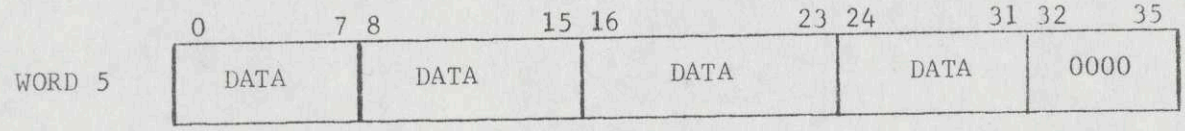
RO DATA FIELD



RO DATA FIELD



RO DATA FIELD



The first word received by the controller contains seek address verification data. The second and third words contain R0 count field information. The controller makes use of the seek address verification data information as follows:

1. It compares the cylinder, head and TI to that previously generated within the controller from the seek address. If they are not the same, the controller will terminate with "Data Alert, Invalid Seek Address." The TI bits supplied by the seek command are the new TI bits to be formatted. Any TI bits previously written on the track will be ignored.

2. The bit indicated as "Z" is to be used as a header bypass switch. If Z = 1, then the controller first must read the HA on the track and compare it to the cylinder and head information given in the command. Also, the controller shall read the first count field (Not R_0) and compare the data length with the sector size specified in the seek data. NOTE: This Z bit is not written on the track in the format operation since it has meaning only with regard to the controller function prior to formatting. When Z = 1, an additional revolution is required to format the track.

   If Z = 0, the controller shall wait for the Index Mark and format the track with no prior checks on information previously written(if any).

   NOTE: To insure data integrity, header bypass (Z - 0) should be used only on packs which have not been formatted previously.

The controller will always use the R0 Count Field information that is supplied by the EUS. Thus, when good tracks, as well as defective and alternate tracks, are to be formatted, the controller will write the six bytes of information received from the EUS (FLAG, CYL, CYL, HD, HD and Record Number) directly into R0 count field as received.

Words four and five contain the information to be written into the R0 data field. Note that for this controller, Record Zero has no key field and a data field of eight bytes. Thus, word four and word five will be written into bytes 1-8 of the R0 data field.

Word three, bits 18-23 will be used as a check character verification on all five words of data received from the EUS. If the check character is zero, the controller will bypass the verification operation. If the check character is nonzero, the controller will generate a 6-bit Exclusive Or check character from the five words (excluding the Check Character Position). If the check character from the EUS and the controller generated check character agree, the format operation will be continued. A mismatch will cause the operation to be terminated with "Data Alert, Invalid Seek Address." Note that this format for Record 0 is compatible with the Record 0 format that is used by IBM programming systems as defined in the "Component Descriptions, 2314 Direct Access Storage Facility." Also, the controller will alternate the high order bit in the flag byte for each count field starting with a "one" bit in the first data record.

A	0	0	0	0	0	T	I

COUNT FIELD FLAG BYTE

The flag byte in the Home Address will always use a high order bit of "zero." The alternating flag byte bit is included to provide pack format compatibility with the IBM 2314 controller.

The sector size to be formatted will be the size specified by the seek data:

YY = 00, 288 bytes
YY = 01, 1440 bytes
YY = 10, 12960 bytes (DSS190) - 7200 bytes (DSS181)
YY = 11, 12960 bytes (DSS190) - 7200 bytes (DSS181)

If an error condition is detected during the writing of a header, the writing of data will continue to the end of the header. The remainder of the track will not be formatted and data error status will be reported at terminate. Refer to Table 4 for status returns supplied at command termination.

3.11 REQUEST STATUS

When the controller receives a Request Status instruction, it will perform a table look-up operation based on the logical channel number to obtain controller held status for the last activity on the logical channel. If there is no controller held status then device held summary status, such as Attention and Device busy will be obtained from the device.

If an error was detected in the command sequence, the controller will supply the status for the detected error. Refer to Table 4.

The status table entry for the controller (device 0) will always be set to Channel Ready, No Substatus. Thus, a Request Status instruction addressed to the controller will cause the following status returns to be sent to the EUS.

Channel Ready	No Substatus
Instruction Rejected	* Parity Alert on IDCW
	* Invalid Op Code

*Detected errors during command sequence.

3.12 RESET STATUS

This instruction results in the resetting of any existing data alert MPC data alert and end-of-file status held in the controller for the given logical channel. The "Invalid Instruction Sequence" sub-status will also be reset.

The Reset Status instruction causes a hardware pull from the same tables in the controller as the Request Status. The controller will reset those status and determine if there also exists a MPC device attention, Attention or Device Busy status in the device, if so, the Reset Status will be returned with that status according to the major status priorities (see Section 4). If not, the appropriate "Channel Ready" status will be returned. Refer to Table 4.

A Reset Status instruction addressed to the controller (device 0) will have one of the following status returns:

Major Status	Substatus
Channel Ready	No Substatus
Instruction Rejected	* Parity Alert on IDCW
	* Invalid Op Code

3.13 WRITE CONTROL REGISTER

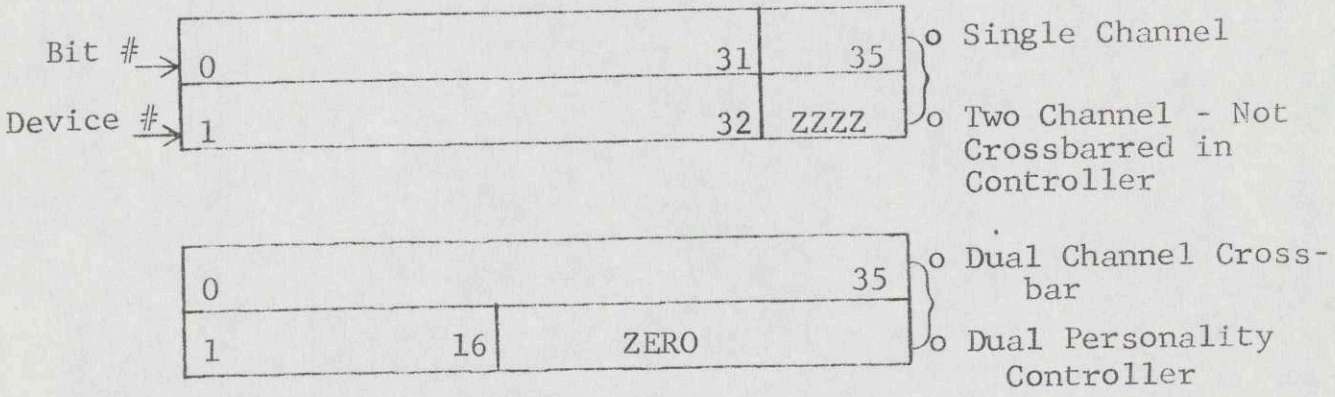
The write control register is provided to allow clearing the statistics tallies or presetting some value in the tallies. The operation of this command addressed to device is the same as the read control register except data is sent to the controller to be put in the tally registers. A write control register addressed to device zero is invalid. Refer to Table 4 for status returns supplied at command termination.

3.14 READ CONTROL REGISTER

The RCR instruction is provided to supply device seek complete/incomplete information or device operation statistics, depending on the device address associated with the command.

The RCR instruction can be addressed to any legal device. If the RCR is addressed to the controller (device zero), two 36-bit words will be transferred to the EUS. Two conditions for 32 devices.

For the DSS181 the format for each word shall be as follows:



Z - Must be Zero

Word 1 - Seek complete flag for each device, by device number.
Seek Complete = 1

Word 2 - Device available flag for each device, by device number.
Device Available = 0
Unavailable = 1

- Seek incomplete
- Standby
- Off-Line
- Device Busy Positioning

The combination of corresponding bits in Word #1 and Word #2 gives the following information.

#1	#2	
0	0	Device is available - No information about Seek Complete.
1	0	Device is available and there has been a Seek Complete.
0	1	Device is not available - Temporarily still busy positioning.
1	1	Device is not available

- Seek Incomplete
- Standby
- Off-Line
- Attention

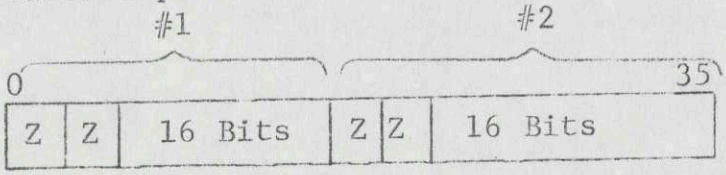
If a bit is set in Word 1 and corresponding bit in Word 2 = 0, the bit will be reset when a data transfer or new seek instruction is issued to the respective device. If a bit is set in Word 2 and the corresponding bit in Word 1 = 0 the bit will be reset when the positioning operation is complete.

If both bits are set they will be reset when the condition is cleared in the device. (That is the device is ready.)

If the RCR is addressed to a valid device other than the controller (device zero), the statistical counters for the addressed device will be transferred to the EUS.

The following sequence of 20 tally (16 bit) words will be returned for the requested device.

Ten (36 bit) words will be returned to the EUS, two tallies per word as shown below:



3.14.1 Basic Counters DSC181 and DSC190

1. Number of Movement Seeks - This counter contains the number of actuator movements of the device.

2. Write Type Data Transfer Command - Number of sectors. This counter contains the total number of sectors transferred from the EUS and written on the device.

3. Read Type Data Transfer Commands - Number of sectors. This counter contains the total number of sectors transferred from the device to the EUS.

4. Number of Data Transfer Commands - This counter contains the total number of data transfer commands issued to the device, that is, read or write.

5. Number of Seek Incompletes - This counter contains the number of seek incomplete status and controller received from the device.

6. Number of Sync Failures/Double Index/No Compare on Count Field - The sync byte on the disk pack did not agree with what it should be.

7. Number of Transfer Timing Errors DLI (CA) - This condition is caused by the controller being unable to keep up with data transfer to or from the device.

8. Number of Data Check Character Alerts - Error in the data field.

9. Number of Count Check Character Alerts - Error in the count field.

10. Number of DLI Parity Errors

3.14.2 Additional Counters for DSC190

11. Number of Alternate Tracks Processed - The track indicators on the pack indicated defective track alternate assigned and the controller went to the alternate track and continued the data transfer.

12. Number of EDAC Correctable Errors -

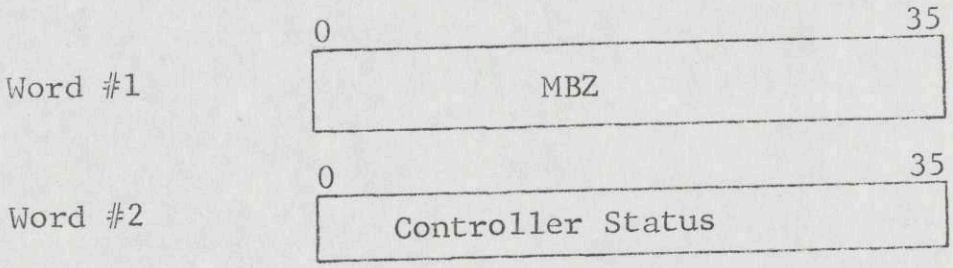
13. Number of EDAC Uncorrectable Errors -

14. Number of Retries before EDAC Correction - NOTE: DSS181 will use only the first five words (10 counters) and will return zeros for the other 10 counters.

These tallies are maintained in Read/Write Memory and may be preset or cleared to zero by using the write control register command. Refer to Table 4 for status returned on termination.

3.15 READ STATUS REGISTER

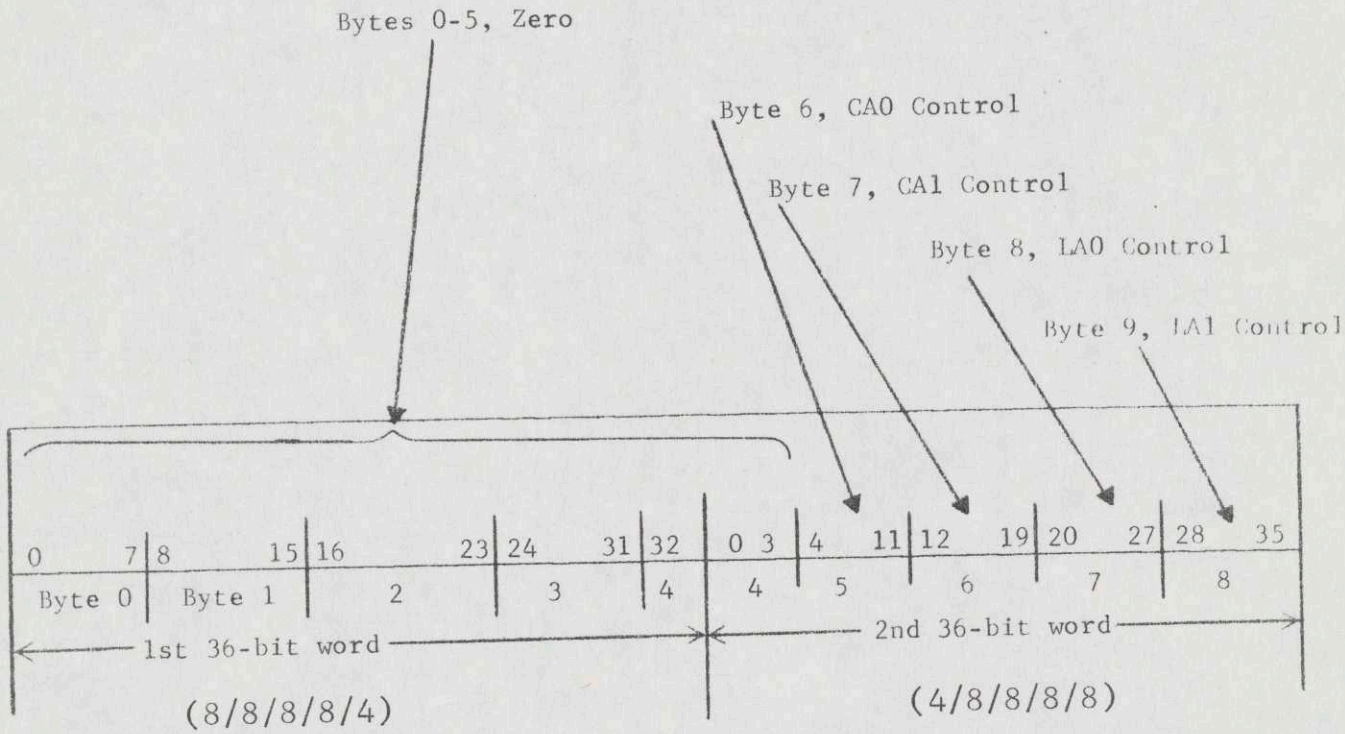
The RSR instruction is provided to supply two types of information to the EUS. The RSR command when addressed to the controller will transfer two 36-bit words to the EUS. The second word is the controller status. The first word will be returned as zero in order to be consistent with the DSS180 Read Status Register format. The format of these words will be as follows:



Word #1 - Must be zero

Word #2 - Will contain the current controller status.

Unless an error occurs in the process of data transmission, the controller will terminate with channel ready, regardless of the error being reported. Refer to Table 4.



Byte 6 and 7 - CA0, CA1

0 - Busy Flag
1 - Polling Pending
2 - Command Pending
3 - Low Priority Q Sampled
4 -
5 -
6 - Device # Error
7 - CA Error

Byte 8 and 9 - LA0, LA1

0 - Busy Flag
1 -
2 -
3 -
4 - Specials Pending (Disk)
5 - Specials Pending (Tape)
6 -
7 -

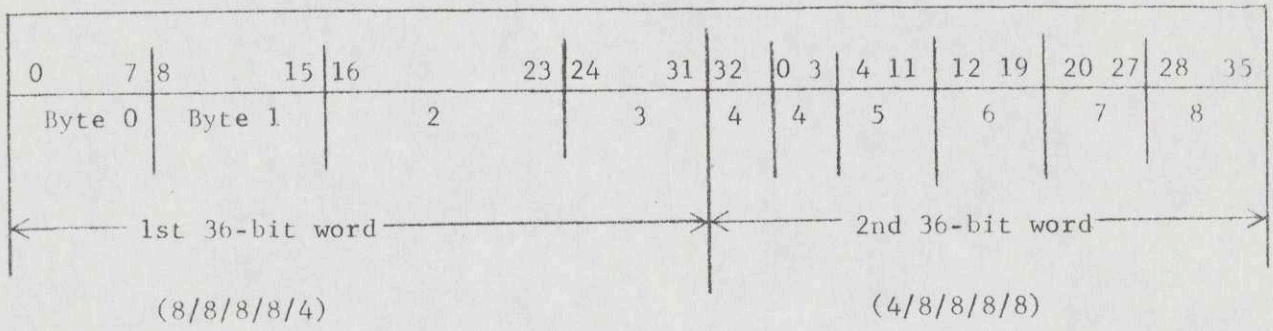
The RSR command addressed to a device will return two words of detailed status from the device in the following format:

Byte 0
Device Serial Number

Byte 1
Device Type

Byte 2
Addressed Device Summary Status

Byte 3-8
Addressed Device Detail Status



RSR Byte 0 Device Serial Number	0	
	1	
	2	Binary Number 1-32
	3	
	4	00000001
	5	
	6	00100000
	7	

		181	190
RSR Byte 1 Device Type	0	0	0
	1	1	1
	2	1	0
	3	0	1
	4	0	0
	5	0	1
	6	0	0
	7	0	0

Summary Status (DSU181 and DSU190)

	Bit Position	Status
RSR Byte 2 Summary Status (Std-All Dev)	0	Device Reserved
	1	Device Seized
	2	Device in Standby
	3	Positioner Busy
	4	DL1 Fault
	5	Device Protected
	6	Device Fault
	7	Device in Diagonal Mode

RSR	DS1 (DSU181)	
Byte 3	0	Command Parity Error
Detailed	1	No or Multiple Command Decode
Status	2	Invalid Command
Byte 1	3	Invalid Command Sequence
	4	State Violation
	5	Protection Violation
(STD-All Dev.)	6	Must be Zero (Not Applicable to DSU181)
	7	Data Parity Error

DSB1 - Detailed Status Byte 1 (DSU190)

Bit 0 - Command Parity Error

The command decoded by the MSD contained a parity error.

Bit 1 - No Command Decoded/Multiple Commands Decoded.

RSR Byte 3 Detailed Status Byte 1

The MSD detected a command strobe (DCS) but was unable to decode a command on the command lines, or more than one command was decoded by the MDS during a single DCS interval.

Bit 2 - Invalid Command

The command decoded by the MSD is not a valid command.

Bit 3 - Invalid Command Sequence

The command decoded by the MSD was not received in a valid sequence (order only, this does not reflect improper timing).

Bit 4 - State Violation

The command decoded by the MSD was received in violation of the operating state of the MSD.

Bit 5 - Protection Violated

A Write Command was decoded by the MSD when the device was "write protected."

Bit 6 - Transfer Timing Error

The MSD has detected a timing error during data transfer which resulted in incorrect data being recorded on the disk (in the case of a write operation) or incorrect data being transferred to the CA (in the case of a read operation).

Bit 7 - Data Parity Error

The MSD detected a parity error on the data lines.

	Bit Position	Status
RSR	DS2	(DSU181)
Byte 4	0	Must be Zero (Not applicable to DSU181)
Detailed	1	Must be Zero (Not applicable to DSU181)
Status	2	Must be Zero (Not applicable to DSU181)
Byte 2	3	Must be Zero (Not applicable to DSU181)
	4	Must be Zero (Not applicable to DSU181)
(Std-All Dev)	5	Spindle Speed Loss
	6	Must be Zero (Not applicable to DSU181)
	7	Must be Zero (Not applicable to DSU181)

DSB2 - Detailed Status Byte 2 (DSU190)

This byte contains those errors relative to MSD logic faults.

Bit 0 - Loss of Write Current

The MSD has detected the loss of Write Current during a write operation.

RSR Byte 4 Detailed Status Byte 2

Bit 1 - Write Current without Write command.

The MSD has detected the presence of Write Current without the presence of a Write command.

Bit 2 - Loss of AC Write Current

The MSD has detected the absence of repetitively switched current in the write head during a Write operation.

Bit 3 - No or Multiple Head Selection

None, or more than one head has been selected by the MSD.

Bit 4 - Unassigned (MBZ)

Bit 5 - Spindle Speed Loss

The MSD has detected a drop in spindle speed below 70 percent of full RPM.

Bit 6 - Overtemperature

The MSD had detected a rise in temperature of the power supply above the acceptable limit for proper operation.

Bit 7 - Loss of Voltage

The MSD has detected a drop in dc voltage below the acceptable level for proper operation.

RSR	DS3	(DSU181)
Byte 5	0	Seek Incomplete
Detailed	1	Must be Zero (Not applicable to DSU181)
Status	2	Must be Zero (Not applicable to DSU181)
Byte 3	3	Must be Zero (Not applicable to DSU181)
	4	Must be Zero (Not applicable to DSU181)
	5	Must be Zero (Not assigned by NPL DLI Spec.)
(STD-MHD only)	6	Must be Zero (Not assigned by NPL DLI Spec.)
	7	Must be Zero (Not assigned by NPL DLI Spec.)

DSB3 - Detailed Status Byte 3 (DSU190)

This byte contains those errors relative to electromechanical failures.

Bit 0 - Seek Incomplete

The MSD has failed to complete a seek operation within a specified time.

RSR Byte 5 Detailed Status Byte 3

Bit 1 - Positioner Overtravel

The positioner carriage of the MSD has traveled beyond the limits allowed for safe Read/Write operations.

Bit 2 - Unassigned (MBZ)

Bit 3 - Unassigned (MBZ)

Bit 4 - RPS Error

The MSD has detected an error in its rotational position sensing (RPS) circuitry and subsequent positioning information may be in error. Possibility of error is detected at index.

Bit 5 - Positioner Offset

The positioner has been offset from its nominal on-track position by means of the OPO or OPI commands.

Bit 6 - Read Clock Offset

The Read Clock phasing has been offset by the ARC or RRC commands.

Bit 7 - Fine Servo

The Positioner has arrived within 1/2 track of its destination and is automatically servo track following.

	Bit Position	Status
RSR	DS4	(DSU181)
Byte 6 Detailed Status Byte 4 Fault(Unsafe) (Dev. Specific)	0	Erase Current Unsafe
	1	DC Write Unsafe
	2	AC Write Unsafe
	3	Heads Unsafe
	4	Erase Gate and Busy
	5	Write Gate and Busy
	6	Write Gate and No Erase Current
	7	Voltage Unsafe

DSB4 - Detailed Status Byte 4 (DSU190)

RSR Bit 0 - Unassigned (MBZ)

Byte 6 Bit 1 - Unassigned (MBZ)

Bit 2 - Unassigned (MBZ)

Bit 3 - Brush Cycle Incomplete

Status The disk cleaning action has not been completed.

Byte 4 Bit 4 - Unassigned (MBZ)

Fault (Unsafe) Bit 5 - Unassigned (MBZ)

Bit 6 - Forward Set

The Positioner Drive Forward flip-flop is set for forward movement.

Bit 7 - Reverse Set

The Positioner Drive Reverse flip-flop is set for reverse movement.

RSR Byte 7 Detailed Status Byte 5 (Indicators) (Dev. Specific)	DS5	(DSU181)
	0	Brush at Stop
	1	Pack On
	2	Lid On
	3	Index Block In
	4	Attention Latch
	5	Heads Flying
	6	Zero Speed
	7	On-Line

DSB5 - Detailed Status Byte 5

RSR Byte 7 Detailed Status Byte 5 Indicators

Bit 0 - Unassigned (MBZ)

Bit 1 - Unassigned (MBZ)

Bit 2 - Unassigned (MBZ)

Bit 3 - Unassigned (MBZ)

Bit 4 - Heads Retracted

The Positioner is in the fully retracted position.

Bit 5 - Unassigned (MBZ)

Bit 6 - Unassigned (MBZ)

Bit 7 - Write and Read

Both Write and Read gates are on at the same time.

	Bit Position	Status
RSR	DS6	(DSU181)
Byte 8	0	Positioner Overtemperature
Device	1	Positioner Over-Velocity
Detail	2	Positioner Out of Limits
Status	3	Positioner Voltage Out of Limits
Byte 6	4	Must be Zero (Not applicable to DSU181)
	5	Must be Zero (Not applicable to DSU181)
	6	Must be Zero (Not applicable to DSU181)
	7	Must be Zero (Not applicable to DSU181)

DSB6 - Unassigned (MBZ)for (DSU190)
Therefore DSB7 will be read instead of DSB6 for RSR Byte 9 in the DSS190

DSB7 - Detailed Status Byte 7 (DSU190)

RSR
Byte 8
Device
Detail
Status
Byte 7

Bit 0 - Unassigned (MBZ)

Bit 1 - DC Voltage High

The dc voltage is higher than specified (above the high tolerance) which may shorten component life or affect normal operation.

Bit 2 - Unassigned (MBZ)

Bit 3 - Overtemperature (Logic)

The temperature in the logic card area has reached a level where reliability will be degraded.

Bit 4 - Read Amplitude Low

The Read Amplitude monitor has detected a read signal amplitude below the specified lower limit, which may cause read errors.

Bit 5 - Unassigned (MBZ)

Bit 6 - Unassigned (MBZ)

Bit 7 - Air Pressure High

The air pressure monitor has detected a rise in air pressure due to dirty filters or other blockage which may jeopardize the dust free integrity of the disk pack area.

3.16 READ EDAC REGISTER

The Read EDAC Register (RER) command addressed to the device may be used by the system software to retrieve the error correction data, displacement and sector number in error.

The two words will be returned in the format as follows:

To be defined later

This command is illegal for DSS181.

Refer to Table 4 for status returns

3.17 RELEASE

This command is used to release a device which has been reserved to this logical channel. The controller shall receive a device code which determines the device to be released.

Instruction execution During the Busy State:

If the device code is valid, the controller shall issue a release to that device. A release instruction addressed to a device that is not reserved will be accepted and treated as a legitimate instruction.

If an unrecoverable error condition is detected, the controller will send a terminate to the EUS and reflect appropriate status. If the designated device had been reserved by another channel, the Release shall terminate with a Device Busy - Alternate Channel in control status. If the Release is directed to a device which is still positioning, the release will be executed even though the seek is not complete and will terminate with a status of Channel Ready or appropriate error status. The Release command will reset the Diagnostic Mode before releasing the device if the device is in Diagnostic Mode. Refer to Table 4 for status supplied at termination.

3.18 DEVICE RESERVE

This command is used to explicitly reserve a device to a logical channel. The controller shall receive a device code which determines the device to be reserved.

Instruction Execution During the Busy State:

If the device code is valid, the controller shall issue a seize to that device. A reserve command addressed to a device that is reserved to the same EUS channel will be accepted and treated as a legitimate instruction.

If the designated device had been reserved by another channel, the reserve shall terminate with a Device Busy...Alternate Channel in control status. If the reserve is directed to a device which is still positioning, the reserve will be executed even though the preseek is not complete and will terminate with a status of channel ready or appropriate error status.

Refer to Table 4 for status returns supplied at command termination.

3.19 SET STANDBY

This command is used to cause a device to go into a standby state. The controller shall receive a device code which determines the device to be put in standby. In standby the device will be in a state which will allow the operator to change packs.

Instruction Execution During the Busy State:

If the device code is valid, the controller shall issue the set standby state to that device. A set standby instruction addressed to a device that is in standby will be accepted and treated as a legitimate instruction.

If the designated device had been reserved by another channel, the set standby shall terminate with a Device Busy - Alternate Channel in control status. If the set standby is directed to a device which is still positioning, the set standby will be executed even though the seek is not complete and will terminate with a status of channel ready or appropriate error status.

Refer to Table 4 for status returns supplied at command termination.

3.20 SPECIAL CONTROLLER COMMANDS

The "Special Controller Commands" are a group of commands dedicated to controller-type functions related to MPC controllers.

The group of commands are identified by a unique code in the "Channel Instruction Field" for the IDCW.

IDCW Format

The IDCW format for these commands is identical to the standard format as defined in Section 5.5.1. With the exception of the following special considerations, normal IDCW checking will be done on these Special Command IDCW's.

Within the IDCW format the following special considerations are to be observed.

Channel Instruction Field (Bits 24-29):

A configuration of "10XXXX" in this field identifies the IDCW as a "Special Controller Command" IDCW.

The MPC controller will interrogate this field of the IDCW, and upon finding the above configuration, interpret the "Device Instruction" field (bits 0-5) and "Device Address" fields (bits 6-11) as defined below:

Device Address Field (Bits 6-11):

For all Special Controller commands this field of the IDCW must be zero.

Device Instruction Field (Bits 0-5):

The allowable codes in this field are the following:

011010 - Write Controller Main Memory (BIN)
001010 - Write Controller Main Memory, ASCII
011100 - Conditional Write Lock Byte
001100 - Write Lock Byte
001000 - Write Control Store
010010 - Read Controller Main Memory (BIN)
000010 - Read Controller Main Memory (ASCII)
000100 - Read Lock Byte
011000 - Execute Control Store Microprogram
001110 - Initiate Write Data Transfer
000110 - Initiate Read Data Transfer

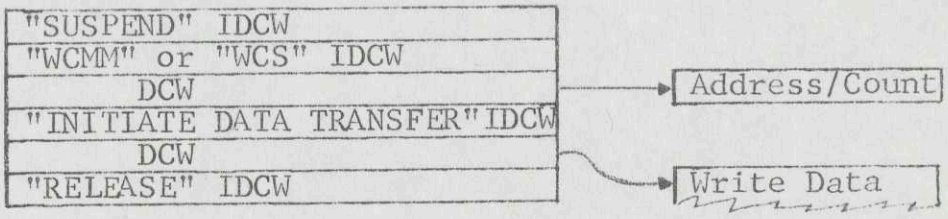
000000 - Suspend Controller
010000 - Release Controller

Channel Program Setup in External System

The following description is intended to define the sequences of IDCW's that the MPC controller will expect to see for the various Special Controller commands.

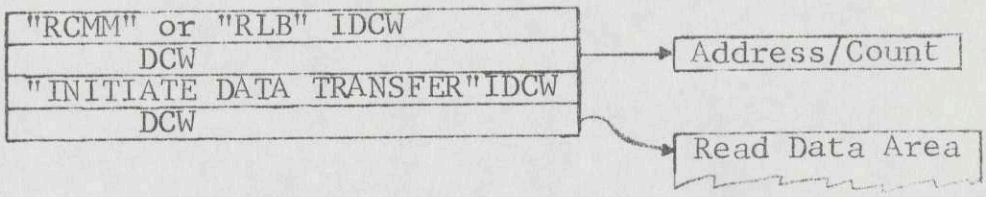
Write Controller Main Memory(WCMM) IDCW
Write Control Store (WCS) IDCW (ASCII or Binary)

For the execution of either of these IDCW's the following Channel Program setup will be required:

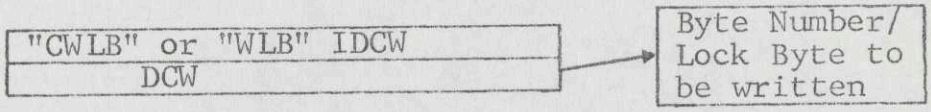


The "Suspend" IDCW can be omitted if the controller is already in the "Suspend" mode as the result of a previous IDCW. The "Release" IDCW can be omitted if it is desired to leave the controller in the "suspended" mode.

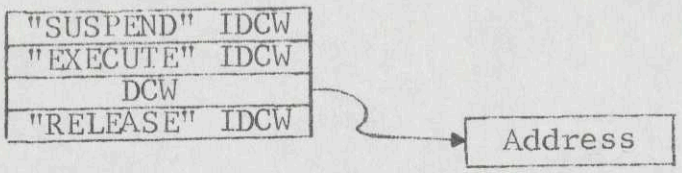
- Read Controller Main Memory (RCMM) IDCW (ASCII or Binary)
- Read Lock Byte (RLB) IDCW



- Conditional Write Lock Byte (CWLB) IDCW
- Write Lock Byte (WLB) IDCW



- Execute Control Store Microprogram (ECSM) IDCW



The "Suspend" IDCW can be omitted if the controller is already in the "Suspend" mode as the result of a previous IDCW. The "Release" IDCW can be omitted if it is desired to leave the controller in the "Suspended" mode.

Special Consideration

Special controller IDCW's cannot be mixed with normal command IDCW's in the same Channel Program.

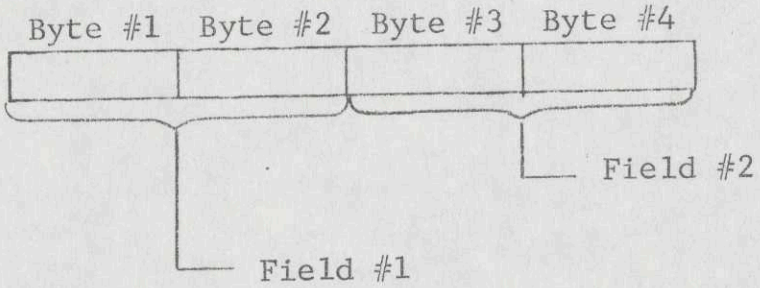
Special Command Descriptions

001010 - Write Controller Main Memory, ASCII
011010 - Write Controller Main Memory, Binary

These commands are used to write data from the external system into the MPC controller main memory.

Upon receiving this IDCW, the MPC controller will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and then receive four bytes of command data.

The controller will interpret this command data as follows:



Field #1 defines a 16-bit word address in the MPC controller main memory at which location the write operation is to start. There is no check made on the legality of this address.

Field #2 defines a 16-bit word count defining the maximum number of MPC controller words to be written by the execution of the command. (All zeros is a valid count.)

In all cases, controller "words" refer to the two-byte words.

Following the completion of the error-free reception of the command data the MPC controller will issue a "Move Pointer and Initiate Command Transfer" service code to the external system, and receive the next IDCW. This IDCW must be the "Initiate Write Data Transfer" IDCW. Upon the completion of the reception of this IDCW, the controller will issue either an "Initiate Data Transfer, Write ASCII" or "Initiate Data Transfer Write Binary" service code to the external system, and then proceed to receive the data to be written into MPC controller main memory.

The write operation will proceed until either the word count received in the command data is expired, or until the external system terminates the operation.

Special Considerations:

1. The command data which follows the "Write Controller Main Memory" IDCW must be formatted in external system memory in the "binary" mode.

2. The data to be written into controller main memory (sent after "Initiate Data Transfer IDCW) must be formatted in external system memory in the mode defined by the "Write Controller Main Memory" op code (either ASCII or Binary).

3. The controller must be in the "Suspend" state (suspend command preceded the write command), or the command will be rejected.

001000 - Write Control Store

The execution of this command is identical to the execution of the "Write Controller Main Memory, Binary" command, except that the write operation is into control store in the MPC controller, and a sum check accompanies the data to be written.

The "sum check" is sent as the last word (two-byte word) of the write data, and is not written into control store. The "sum check" will represent the twos-complement of the final summation represented by the addition of all MPC controller words (two-byte words) sent, with end-around carry (i.e., as each two-byte word is added to the sum check accumulation, carry out of the high-order byte of the two-byte accumulation is added back into the sum check accumulation). The sum check word is included in total word count specified for the command execution. Failure of the transmitted sum check to agree with the controller computed sum check will cause a failure status to be reflected by the MPC controller.

The controller must be in the "Suspend" state at the time the write command is received (suspend command preceded the write command), or the command will be rejected. (See status table which follows later.)

000010 - Read Controller Main Memory, ASCII
010010 - Read Controller Main Memory, Binary

The execution of these commands is identical to the definition and execution of the "Write Controller Main Memory" command with the following exceptions:

a. The operation is a "read" from Main Memory instead of a "write."

b. The second IDCW received from the external system must be an "Initiate Read Data Transfer" IDCW instead of an "Initiate Write Data Transfer" IDCW.

c. This command execution does not require the controller to be in the "Suspend" mode.

011100 - Conditional Write Lock Byte
001100 - Write Lock Byte
000100 - Read Lock Byte

These three commands provide a software "lock" capability in MPC controllers which are to be shared between two external user systems.

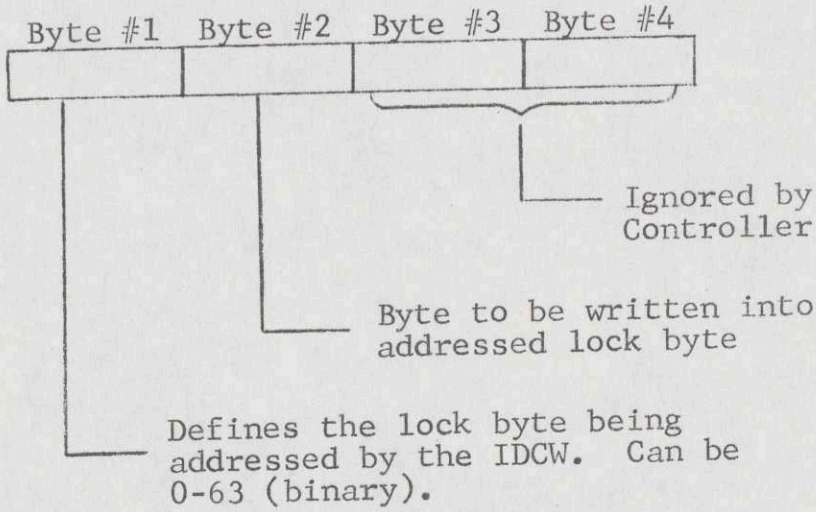
The controller does not have to be in the "Suspend" mode for these commands.

The execution of these commands is defined as follows:

Conditional Write Lock Byte

Upon receiving this IDCW, the MPC controller will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and then receive four bytes of command data.

The controller will interpret this command data as follows:



Upon completion of the reception of the command data, the controller will access the addressed lock byte. If the byte is nonzero, the controller will leave it unmodified and reflect this condition by means of termination status. This will terminate the execution of the channel program.

If the addressed lock byte is zero, the contents of Byte #2 of the command data are written into the addressed lock byte. The controller then executes whatever operation is indicated by the "Continue/ Marker" bits (bits 22,23) of the "Initiate Data Transfer" IDCW. This may be status and termination procedure, or continue to the next IDCW.

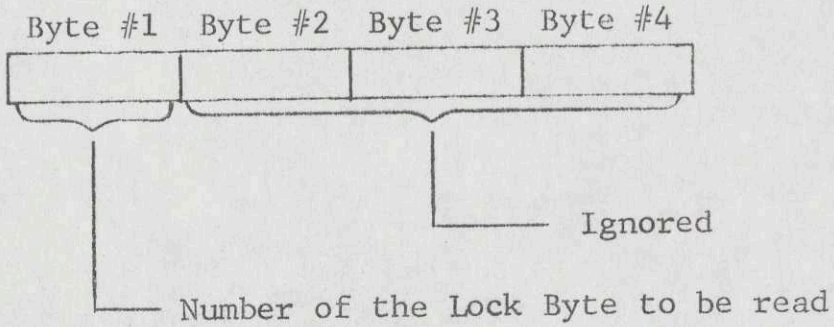
Write Lock Byte

This command is identical to the "Conditional Write Lock Byte" command, except that the controller does not first test the addressed lock byte. The write operation is executed unconditionally.

Read Lock Byte

This command is used to read the contents of any one of the 64 lock bytes contained in MPC main memory.

Upon receiving the "Read Lock Byte" IDCW, the MPC will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and then receive four bytes of command data. This data will be interpreted as follows:



Upon receiving the command data, the controller will issue a "Move Pointer and Initiate Command Transfer" service code to the external system, and then receive the next IDCW. This IDCW must be the "Initiate Read Data Transfer" IDCW.

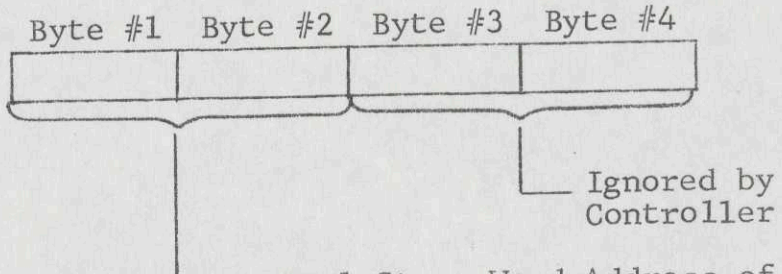
Upon completion of the reception of this second IDCW, the controller will issue an "Initiate Data Transfer, Read ASCII" service code to the external system, and send one byte of information. This byte will represent the contents of the addressed lock byte.

It should be noted that the contents of the lock byte will be stored in 6000 memory in the ASCII mode (i.e., placed in the high-order 9-bit field of the 6000 word).

011000 - Execute Control Store Microprogram

Upon receiving this IDCW, the MPC controller will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and proceed to receive four bytes of command data.

The controller will interpret this command data as follows:



Upon reception of the command data the controller will branch internally to the addressed microprogram. The return address will be saved in controller register "HUXAR" when this branch is made. Upon completion of its execution, the microprogram must return via a branch on the contents of AUXAR. Upon the return from the microprogram, the controller will take the appropriate action as defined by the "Continue/Marker" bits (22,23) of the "Initiate Data Transfer" IDCW.

The controller must be in the "suspend" state at the time the "Execute" command is received (suspend command preceded the execute command), or the execute IDCW will be rejected.

000000 - Suspend Controller

This command allows a controller to be "seized" by one external system in a situation where the controller is physically connected to more than one system via two or more PSI interfaces.

The command will cause the controller to take the following actions:

- Ignore all "Channel Program Waiting" lines from all PSI interfaces, and wait until all current I/O operations in progress at the time the Suspend command was received are completed. (This implies that any channel program has been initiated will be completed.)

- Issue a "Special Status Storage" and Special Interrupt to all connected PSI interfaces including the PSI interface over which the Suspend command was received.

The format of the four-byte status storage will be as follows:

Byte 1: 000_8

Byte 2: 000_8

Byte 3: 001_8

Byte 4: 000_8

The "Special Status Storage" and "Interrupt" will be sent to logical channel #0 in all cases, irrespective of the LC number over which the suspend command was received.

- Execute the action defined by the "Continue/ Marker" field of the "Suspend IDCW" (bits 22, 23) which will be one of the following:

  a. Make a status entry and generate a terminate interrupt.

  b. Make a status entry, generate a marker interrupt and access the next IDCW (continue bit on in suspend IDCW).

  c. Make no status entry, but immediately access and execute the next IDCW.

- Ignore all "Channel Program Waiting" lines from any other PSI interface other than the one over which the suspend was received. The PSI interface initiating suspend will be serviced normally, with the following exception:

  Subsequent IDCW's received by the controller over the PSI interface which issued the "suspend" command or the IDCW will be rejected with appropriate status (see status table which follows later).

  The "suspend" command must be the first IDCW or the channel program in which it is sent.

010000 - Release Controller

This command is used to reset the "suspend" condition set up by a "suspend" command. The controller will issue a "Special Status Storage" and special interrupt to logical channel #0 of all connected PSI interfaces. The "Special Status Storage" will consist of all zeros, except for byte 3, which will be a 002_8.

The controller will then execute a status entry and terminate interrupt.

STATUS RESPONSES FOR THE "SPECIAL CONTROLLER COMMAND" IDCW'S

Status (Major/Sub)	Commands Status Reflected To	Reason
Ready (0000)	All	Everything OK
MPC Command Reject (1101)		
01 - Illegal Procedure	Write Controller Main Memory Write Control Store Execute Control Store Microprogram	Controller Not in "Suspend" Mode
	Initiate Read/Write Data Transfer	IDCW Not Preceded by Spec Command IDCW
02 - Illegal Logical Chan Number	All (including non-Special IDCW's)	Illegal Logical Channel Number
03 - Illegal Log. Chan. Number to "Suspended" Controller	All	Controller suspended, and IDCW addressed to logical channel other than one over which the Suspend command was issued
04 - Continue Bit (not set)	Read/Write Controller Main Memory Write Control Store Read Lock Byte	A two - IDCW command has been received but the "Continue" bit (bit 22) of the first IDCW was not set.
MPC Data Alert (1011)		
01 - Transmission Parity	All	Parity error on data transmission.
02 - Inconsistent Command		
	All Lock Byte Commands	Illegal Lock Byte Number specified
03 - Sum Check Error	Write Control Store	Sum Check Error
04 - Byte Locked Out	Conditional Write Lock Byte	Referenced Lock Byte is nonzero (lock) and cannot be written.
Command Reject (0101)		
01 - Invalid Op Code	All	
02 - Invalid Device Code	All	
04 - Parity Error on IDCW/LC#	All	

The "Release" command must be the last IDCW of the channel program in which it is sent. This command will terminate the channel program irregardless of the state of the "continue" bit of the "release" IDCW.

3.21 BOOTLOAD CONTROL STORE

Control Store Personality Overlay:

This command is used for loading the Controller Personality into the Controller Control Store. The overlay operation is begun at control store location 512, and continues until terminated by the external system.

A "sum-check" word (two-bytes wide) will follow and be included as a part of the overlay data. This sum check word will represent the twos-complement of the result of the binary addition of all two-byte overlay words received, with end-around carry.

If the Control Store Personality Overlay command is executed error-free, the controller will reflect "Ready Major Status" followed by a termination interrupt. Upon completion of a successful overlay, the controller is set to the "normal" operating mode by the "WAIT" microprogram, which then branches to location 512, which is the first microinstruction of the personality overlay.

Any error detected during the reception and execution of the Control Store Personality Overlay command will be reflected by the controller reverting to the "halt" state, which will in turn cause the Operational-In line to the IOM to drop.

The Control Store overlay data must be formatted in the "ASCII" mode in the 6000 Memory (one-byte right-justified in each 9-bit segment of the 6000 word).

3.22 ITR BOOT

Control Store Test Overlay;

This command will result in the transfer from the external system of a maximum of 512 two-byte words (1024 bytes) which are written into Control Store, starting at location 512.

A "sum-check" word (two-bytes wide) will follow and be included as a part of the overlay data. This sum check word will represent the twos-complement of the result of the binary addition of all two-byte overlay words received, with end-around carry.

The external system can terminate the load operation early. Otherwise, the controller will terminate the load after receiving 512 two-byte words plus the sum-check word.

The Control Store overlay data must be formatted in the "ASCII" mode in the 6000 Memory (one byte right-justified in each 9-bit segment of the 6000 word).

The "Control Store Test Overlay" command is intended for executing ITR overlays (overlay of test micro-programs). As such, the execution of the command itself is considered to be a part of the overall ITR test execution. Therefore, if any error is detected during the execution of the overlay operation itself, the controller will halt, with appropriate fault symptoms displayed on the Controller Maintenance Panel. (This will result in the dropping of the Operational-In line to the IOM.)

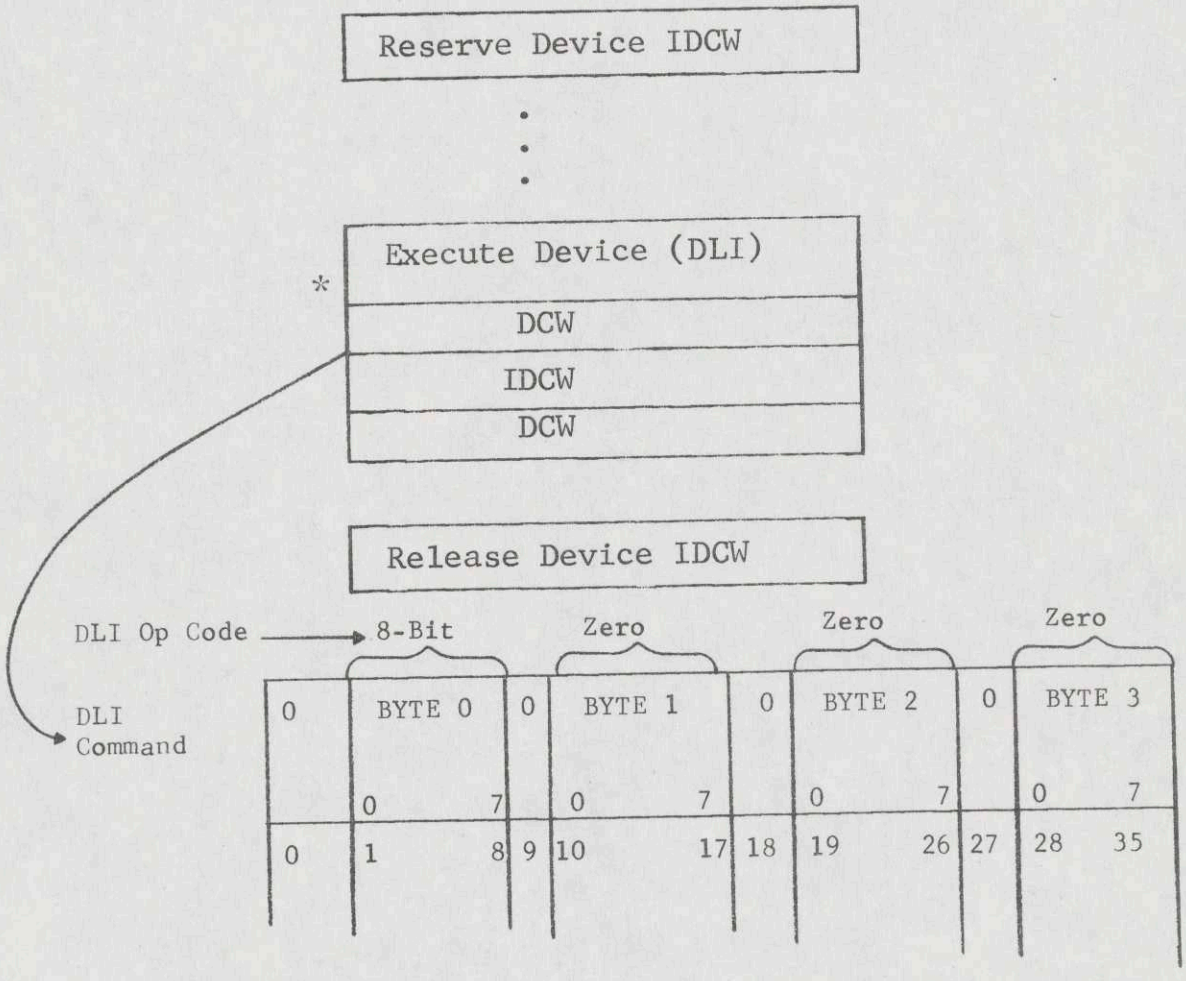
If the overlay operation is executed without error, the response to the system will be major status of "Ready" (0000), and "all-zeros" substatus, followed by a Terminate Interrupt.

Following successful completion of the test overlay, including Terminate Interrupt, the controller will drop the Operational-In line to the IOM, and commence execution of the overlay just received. The test overlay will be entered at Control Store address 514. The execution of the ITR overlay may result in the halting of the Controller (fault detected), in which case the Operational-In line to the IOM will remain down.

If the ITR overlay execution completes without a fault detection, the controller will raise the Operational-In line to the IOM, and will generate a Special Status storage followed by a Special Interrupt to the external system. The format of the Special Status storage will be as defined previously in this memo. At this point the controller will be idling in the "WAIT" routine, waiting for the next command from the external system.

3.23 Execute Device DLI Command Mode Control (30_8)

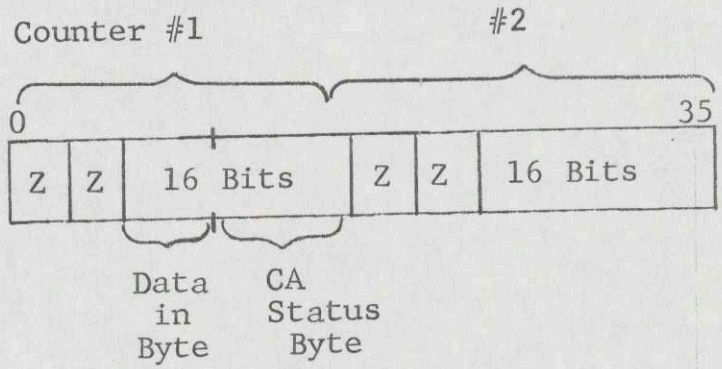
This command provides a mechanism for transferring DLI commands directly from the external user system to the addressed device. Prior to issuing this command, the EUS must have issued a Reserve Device command to the desired device. If the device is not reserved with the Execute Device (DLI) command is received by the controller, the command shall be rejected with MPC command reject - illegal procedure status. The correct channel program format is illustrated below:



*Only one DLI command for each Execute Device (DLI) command.

In response to a correct Execute Device (DLI) IDCW the controller will place the PSIA in the ASCII mode, and begin requesting the information bytes. The first byte will contain the DLI command which the controller places directly on the control lines to the addressed device. The other bytes are ignored by the controller.

If this DLI command requests information from the device, the requested byte and CA status is placed in the controller main memory in counter number one (number of movement seeks) of the error statistics for the addressed device. CA status is always placed in the second byte for both input and output.



The EUS may then retrieve this byte of device status by issuing the Read Control Register command to the same device as addressed by the Execute Device (DLI) command.

Termination status for this command is always "Ready," the only other status will be instruction rejected or MPC command reject.

DLI Commands

000000
000001
01 000010 SFU-Seek Forward Upper
01 000011 SFL-Seek Forward Lower
01 000100 SRU-Seek Reverse-Upper
01 000101 SRL-Seek Reverse-Lower
01 000110 COU-Cylinder Out-Upper
01 000111 COL-Cylinder Out-Lower
01 001000 HOU-Head Adr. Out-Upper
01 001001 HOL-Head Adr. Out-Lower
001010
001011
001100
001101
001110
11 001111 WRT-Write

01 010000 SZE-Seize Device
01 010001 RLS-Release Device
01 010010 RCB-Recalibrate
01 010011 SSM-Set Standby
01 010100 SLM-Set Local
01 010101 RDM-Reset Diagnostic Mode
01 010110 ENM-Enable Meter
01 010111 DSM-Disable Meter
01 011000 SPO-Shift Position Out
01 011001 SPZ-Shift Position In
01 011010 ARC-Advance Read Clock
01 011011 RRC-Retard
01 011100 HDS-Head Select
01 011101 HDD-Head Deselect
01 011110 SDM-Set Diagnostic Mode
01 011111 SDE-Set Diagnostic Escape

00100000 HIU-Head Adr. In-Upper
00100001 HIL-Head Adr. In-Lower
00100010 CIU-Cylinder In-Upper
00100011 CIL-Cylinder In-Lower
00100100 API-Angular Position In
10100101 RDX-Read
00100110 DNR-Service Number In
00100111 DTR-Service Type In
00101000 SSR-Summary Status In
00101001 DS1-Detail Status-Byte 1
00101010 DS2-Detail Status-Byte 2
00101011 DS3-Detail Status-Byte 3
00101100 DS4-Detail Status-Byte 4
00101101 DS5-Detail Status-Byte 5
00101110 DS6-Detail Status-Byte 6
00101111 DS7-Detail Status-Byte 7

01110000
110001
110010
110011
110100
110101
110110
110111
111000
111001
111010
111011
111100
111101
111110
00111111 DS8-Detail Status-Byte 8

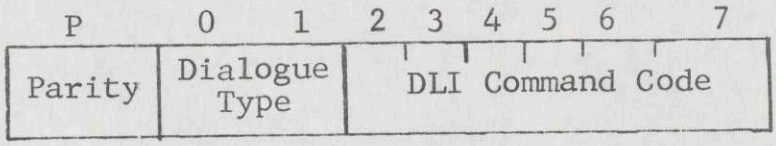
CA Awareness of the "Type" of DLI Dialogue

The DLI dialogues can be divided into four types:

Input	(00)
Output and Control	(01)
Data Transfer-READ	(10)
Data Transfer-WRITE	(11)

Rather than decoding the DLI command codes to determine the type of the DLI dialogue, a two-bit code will be supplied by firmware for such a purpose.

These two bits are an extension to the DLI command register as follows:



When using the Execute Device command (DLI) all eight bits must be supplied in the op code byte. Because the DLI command codes sent to the devices must carry good parity, the parity bit on this register reflects odd parity for bits 2-7 only.

When this register is loaded, the CA looks at bits 0-1, and if only one of the two bits is on, then the parity bit received from the MPC is reversed before loading the register. On reading, parity is regenerated.

4. STATUS

Table 4 lists the possible status returns to the various instruction terminations. The major statuses and substatuses are described in detail in the paragraphs below:

4.1 CHANNEL READY (0000)

No Substatus (000000)

This status indicates that the controller/device is on line and ready and no detectable error conditions exist. When received at termination of a seek type instruction, this substatus indicates that the on-line portion has been successfully completed. The controller is free to receive another instruction for that channel. When automatic retry is performed by the controller, the binary number coded in the substatus is the number of times the retry was performed.

Automatic Retry was performed	(00X001)
Once	(00X010)
Twice	
Three Times	(00X011)
Device in T&D Mode	(0010XX)

4.2 DEVICE BUSY (0001)

The device busy status in response to an instruction, indicates that the addressed storage unit is operating but temporarily not available.

Alternate Channel in Control (100000)

This substatus is sent to the EUS which is attempting to gain control of the device or to a release, reserve. set standby, set local instruction directed to a device reserved by a different channel (dual channel operation).

Device Positioning (000000)

This substatus indicates that the addressed device was busy positioning. This status will be returned only for Request Status and Reset Status.

4.3 ATTENTION (0010)

The Attention status indicates that a condition has occurred which may require manual intervention.

Write Inhibit (0000X1)

This substatus is sent to the EUS as the result of a write type instruction being issued to a file that is write inhibited.

Seek Incomplete (00001X)

This substatus results when the access mechanism of the addressed device has failed to position after a determined period of time. The controller has attempted to correct the condition three times with restore and seek sequences. Unless there is a permanent hardware failure, this attention condition may be corrected by issuing additional Restore instructions to the addressed device from the EUS. (The restore must be followed by a Seek before device data transfer can occur.)

Device Off-Line (100000)

This substatus is sent to the EUS to indicate that the addressed device is off-line power off, or not connected to the subsystem. OPI is down from the device.

Device Inoperable (001000)

This substatus indicates that the device is on-line but is operating in a fault condition and must be investigated. The fault status indicates the detection of an illegal combination of conditions within the device.

Device in Standby (010000)

This substatus indicates that the device is in a standby state, that is, the spindle motor has been turned off and heads retracted.

4.4 DATA ALERT (0011)

The Data Alert status indicates that an error was detected during execution of the last instruction on that I/O channel. Any new instruction, except Request Status, will reset the Data Alert status.

Transfer Timing Alert (000001)

A Transfer Timing Alert during data transfer will occur when data is lost because some hardware stage of the data transfer logic cannot keep up the transfer rate.

Transmission Parity Alert (000010)

This condition is defined as occurring when a parity error is detected by the MPC during the transmission of data bytes from the EUS or to or from the device.

Invalid Seek Address (000100)

A Special Seek was issued to a user cylinder, or a normal seek was issued to the T&D cylinder. The seek address exceeds the limit of one device. If the format track verification data does not match the seek address. If less than five bytes or more than five bytes are transferred as seek data.

This status will be returned also when the check character test on the format instruction has a compare mismatch.

Header Verification Failure (0X1000)

This status is returned to the EUS when the subsystem is unable to locate the desired sector on the addressed track, or when a cylic check alert is detected when the controller reads the count field of a particular sector. Also, if a cyclic check error occurs as a result of reading Home Address (HA), this substatus shall be returned.

Check Character Alert (X1X000)

This substatus indicates that the field cyclic check character generated in the CA did not compare with the one recorded on the media. This status will be set for all check character failures, whether they occur on a count or data field or the home address. If the cyclic check occurs on the data field, the status returned will be (010000). For write and compare operations, the status will be (110000) if the compare operation failed in addition to the cyclic check error on the data field.

Since the controller checks the count field for each sector in all sector read and write operations (excluding format), it is possible to get a cyclic check condition on the count field. When this happens, the controller will return a status of (011000), which is a combination of header verification failure and check character alert.

Compare Alert (1X0000)

This substatus resulting from a write and compare instruction indicates that the data recorded on the media does not compare to data received from the EUS.

4.5 END OF FILE (0100)

End of file status indicates that the data transfer for the last instruction tried to exceed some defined boundary. This boundary may be a physical limit (end of cylinder), last block of an alternate track or a program-imposed limit (sector count limit). An EOF shall be indicated any time the track indicators change or upon entering or leaving a track formatted as alternate.

End-of-File - Good Track Detected (000000)

This status will be returned by the controller if the sector address in the count field is correct but the controller detected a Good Track Indicator when it was expecting an Alternate or Defective Track. This status will occur only when the EUS has issued a seek to a track with "good" track indicators when it was expecting something else.

Last Consecutive Block (0000X1)

This condition shall occur when the last consecutive block of the addressed actuator position has been reached and the operation presently being executed has not been completed, or when the controller detects an overflow from an alternate track.

Sector Count Limit (00001X)

This condition indicates that the total number of data sectors specified in the sector count limit were accessed but the processing system has not issued a Terminate Out Signal.

Defective Track Detected, Alternate Assigned (000100)

This condition shall occur when a read or write type instruction is attempted on a defective track or when overflow is detected to a defective track. The track indicators on the defective track are binary 10.

Defective Track Detected, No Alternate Assigned (001000)

This status is similar to the other Defective Track status except that the track indicators are binary 11. This indicates that no alternate has been assigned to the defective track.

Alternate Track Detected (010000)

This status will be returned if the sector address in the count field is correct but the controller detected an alternate track when a good or defective track was expected.

4.6 INSTRUCTION REJECTED (0101)

The Instruction Rejected status indicates that the instruction just received is not acceptable to the subsystem and was not initiated. The status is reset when any new instruction is received.

Invalid Operation Code (000001)

This substatus indicates that an operation code invalid for this subsystem was received from the EUS.

Invalid Device Code (000010)

This substatus indicates that an invalid device code for this subsystem was received from the EUS. Further, no device with the given address is connected to the subsystem. If the device is connected but does not have power on, the status will be Attention Device Off-Line or a controller only command (special controller, bootload, ITR boot) was received with a nonzero device code.

Parity Alert on IDCW (000100)

This substatus indicates that a parity error was detected by the LA on the IDCW.

Invalid Instruction Sequence (001000)

This condition shall occur when the subsystem receives a Data Transfer instruction without a prior valid seek on the same logical channel. Restore and Preseek are not valid seeks for data transfer.

4.7 CHANNEL BUSY (1000)

The channel busy status is reflected by the channel and indicates that the controller is in the process of executing an instruction from the EUS where the channel must be dedicated to the operation.

4.8 MPC STATUS EXTENSIONS

The following new major status categories are established, for use by MPC controllers:

MPC Device Attention	1010
MPC Device Data Alert	1011
MPC Command Reject	1101

These three new categories are to be considered extensions of the currently existing Attention, Data Alert and Command Reject major status classifications, and each will be used to reflect the same basic type of status as its previously defined counterpart.

Substatus under these new major status classifications will be encoded as one of 64 possible 6-bit codes (as opposed to bit encloding).

Substatus codes 00_8 - 07_8 under MPC Device Attention, MPC Device Data Alert and MPC Command Reject are reserved for status returns which are generated independent from the device personality of the controller.

MPC Device Attention (1010)

- Configuration Error (000001)
- Device Number Error (000011)
- Multiple Devices (000010)
- CA Unexpected Interrupt (after initialize) or CA OPI down (001011)

Configuration Switch Error

This error condition will occur if the personality firmware loaded into a controller does not agree with the configuration switches on the MPC operator panel.

Multiple Devices

This substatus indicates that the controller has detected at least two devices with the same identification number.

Device Number Error

At least one device has an identification number which is outside the range of legal device numbers for the subsystem.

CA Unexpected Interrupt

The configured switch error will probably be returned as termination status for the first command issued to the controller after the personality firmware has been loaded. The Multiple Devices substatus and Device Number Error substatus will most likely be returned as termination status for the first command issued to the controller following the loading of the personality firmware. However, either may occur at any point in time. Also, both may occur in which case the Device Number Error will take priority.

MPC Device Data Alert (1011)

Transmission Parity 000001

Parity error on data transmission.

Inconsistent Command 000010

All lock byte commands if illegal lock byte number is specified.

Sum Check Error 000011

Sum check error on data written to the controller.

Byte Locked Out 000100

Conditional write lock byte is referenced to a lock byte which is nonzero (locked).

Error Correction Required 001001

EDAC Error Uncorrectable 001010

Sector Size Error 010001

Nonstandard Sector Size 010010

MPC Command Reject (1101)

Illegal Procedure 000001

Write controller main memory and write control store when the controller is not in "Suspend" mode.

Execute control store microprogram and initiate read/write data transfer IDCW not preceded by special controller command IDCW.

Illegal Logical Chan Number 000010

Illegal logical channel number on all types of IDCW's.

Illegal Logical Chan Number to "Suspended" Controller 000011

When the controller is suspended and an IDCW is addressed to a logical channel other than the one over which the Suspend command is issued.

Continue Bit Not Set 000100

The first IDCW of a two-IDCW command does not have the continue bit set. (Special controller commands.)

4.9 CHANNEL ABORT - CONTROLLER ERROR INTERRUPT

The controller will detect internal hardware errors, such as parity errors on internal registers, parity errors on main memory (read/write) data, parity errors on microinstructions accessed from control store, etc.

The detection of any one of these internal hardware errors will result in the automatic execution of an error interrupt, which forces the controller to branch to a fixed control store location, and establishes an "error interrupt in progress" state of the machine.

The microprogram which is automatically entered as a result of the error interrupt will first test the state of Configuration Switch #14 of the Maintenance Panel. If the switch is set, an immediate branch will be made to the Integrated Test Routine (ITR) module, located in the first 512 locations of control store. (The exact entry point to be determined during implementation.) Setting of switch 14 therefore implies that the MPC controller will be put in the ITR mode upon the occurrence of an error interrupt.

If switch 14 is not set, the error interrupt microprogram will take the following actions:

a. Safestore in a fixed main memory area (to be defined) the current contents of all pertinent hardware registers.

b. Terminate all existing activity in progress, including device movement. This must be evaluated and implemented on a device type basis. The execution of an active channel program (DCW list) will be aborted.

c. Reset the error interrupt level, and return the controller to normal operation (that is, waiting for command from central system).

The occurrence of the error interrupt will force the "operational-in" line of the PSI interface to the external system to revert to the "nonoperational" state. This line will stay in the "nonoperational" state until the "error interrupt in progress" state is reset by the microprogram.

Detection of Error Interrupt Sequence by External User System

The external indication that the controller has taken an error interrupt is the dropping of the "operational-in" line of the PSI interface to the external system. This line will be down for the duration of time the controller is in the "error interrupt in progress" state, which is a function of how many microinstructions must be executed by the error interrupt microroutine. As an order of magnitude, it can be assumed the "operational-in" line will be down for approximately 15 microseconds. Repeated error detections will result in repeated error interrupts, and the PSI adapter in the IOM will detect the PSI "operational-in" line dropping if a channel program (DCW list) is currently being executed for any one of the eight logical channels of the PSI. The adapter will generate a status storage, and mask the logical channel.

The error interrupt occurrence will go undetected by the external system, however, if no logical channel of the PSI interface is active or initiated, during the time the "operational-in" line to the EUS is down.

As described above, execution of an error interrupt sequence will result in the safestoring of pertinent registers in main memory. This safestore area can be accessed by the external system for diagnostic purposes as required, using the "Read Controller Main Memory" special controller command.

4.10 MAJOR/SUBSTATUS STATUS PRIORITIES

The priority of major status returns will be as follows:

Instruction Rejected (Highest)	(0101)
MPC Command Reject	(1101)
Data Alert	(0011)
MPC Device Data Alert	(1011)
End-of-File	(0100)
Attention	(0010)
MPC Device Attention	(1010)
Device Busy	(0001)
Channel Ready (Lowest)	(0000)

The following table defines the codes and priorities for substatus within major status. Substatus is listed in order from the highest to the lowest priority.

INSTRUCTION REJECTED	0101
IDCW Parity Alert	000100
Invalid Op Code	000001
Invalid Device Code	000010
Invalid Instruction Sequence	001000
MPC COMMAND REJECT	1101
Illegal Procedure	000001
Illegal Logical Channel Number	000010
Illegal, Suspended	000011
Continue Bit Not Set	000100

DATA ALERT	0011
Transmission Parity Alert	000010
Transfer Timing Alert	000001
Invalid Seek Address	000100
Header Verification Failure	0X1000
Cyclic Checkword Alert	X1X000
Compare Alert	1X0000
MPC DEVICE DATA ALERT	1011
Transmission Parity	000001
Inconsistent Command	000010
Sum Check Error	000011
Byte Locked Out	000100
Nonstandard Sector Size	010010
Sector Size Error	010001
EDAC Error Uncorrectable	001010
Error Correction Required	001001
END-OF-FILE	0100
Last Consecutive Block	0000X1
Block Count Limit	00001X
Defective Track (Alt. Track Assigned)	000100
Defective Track (No Alt. Assigned)	001000
Alternate Track Detected	010000
Good Track Detected	000000
ATTENTION	0010
Device Inoperable (Fault)	001000
Device Off-Line	100000
Seek Incomplete	000010
Write Inhibit	000001
Device Standby	010000

MPC DEVICE ATTENTION	1010
Configuration Error	000001
Device Number Error	000011
Multiple Device	000010
CA Error	001011
DEVICE BUSY	0001
Alternate Channel in Control	100000
Device Positioning	000000
CHANNEL READY	0000
No Substatus	000000
Retry was Performed	000001
Retry Twice	000010
Retry Three Times	000011
Device in T&D Mode	0010XX

Table 4

	INSTRUCTION REJECTED	IDCW Parity Alert	Invalid Op Code	Invalid Device Code	Invalid Instruction Sequence	DATA ALERT	Transmission Parity Alert	Transfer Timing Alert	Invalid Seek Address	Header Verification Failure	Cyclic Checkword Alert	Compare Alert	END-OF-FILE	Last Consecutive Block	Sector Count Limit	Defective Track	Defective Track	Alternate Track	Good Track Detected	ATTENTION	Device Inoperable	Device Off-Line	Seek Incomplete	Write Inhibit	Device in Standby
SEEK	x		x	x			x		x												x	x	x		x
SPECIAL SEEK	x		x	x			x		x												x	x	x		
PRESEEK	x		x	x	x		x		x												x	x	x		x
RESTORE	x		x	x																	x	x	x		x
READ	x		x	x	x		x	x		x	x			x	x	x	x	x	x		x	x			x
READ ASCII	x		x	x	x		x	x		x	x			x	x	x	x	x	x		x	x	x		x
WRITE	x		x	x	x		x	x		x	x			x	x	x	x	x	x		x	x	x	x	x
WRITE ASCII	x		x	x	x		x	x		x	x			x	x	x	x	x	x		x	x	x	x	x
WRITE & COMPARE	x		x	x	x		x	x		x	x	x		x	x	x	x	x	x		x	x	x		x
READ NONSTANDARD	x		x	x	x		x	x		x	x										x	x	x		x
READ TRACK HEADER	x		x	x	x		x	x		x	x										x	x	x		x
FORMAT TRACK	x		x	x	x		x	x	x	x	x										x	x	x	x	x
REQUEST STATUS	x		x	x			x	x	x	x	x	x		x		x	x	x	x		x	x	x	x	x
RESET STATUS	x		x	x																	x	x	x	x	x
WCR WRITE CONTROL REG.	x		x	x			x														x	x			
RCR READ CONTROL REG.	x		x	x			x																		
RSR READ STATUS REG.	x		x	x			x														x	x			x
RER READ STATUS REG.	x		x	x			x																		
RELEASE DEVICE	x		x	x																	x	x			x
RESERVE DEVICE	x		x	x																	x	x			x
SET STANDBY	x		x	x																	x	x			x
SPECIAL CONTROLLER CMDS	x		x	x																					
BOOTLOAD C.S.																									
ITR BOOT																									
EXECUTE DEVICE	x		x	x																					

Table 4

	DEVICE BUSY	Alternate Channel in Control	Device Positioning	CHANNEL READY	No Substatus	Retry Was Performed	Retry Twice	Retry Three Times	T&D Mode	MPC COMMAND REJECT	Illegal Procedure	Illegal Logical Chan. Number	Illegal Chan. No. to Suspend	Continue Bit Not Set	MPC DEVICE DATA ALERT	Transmission Parity	Inconsistent Command	Sumcheck Error	Byte Locked Out	Error Correction Required	EDAC Error Uncorrectable	Sector Size Error	Nonstandard Sector Size
SEEK	x			x		x	x	x				x											
SPECIAL SEEK	x			x		x	x	x				x											
PRESEEK	x			x		x	x	x				x											
RESTORE	x			x								x											
READ	x			x		x	x	x				x								x	x	x	x
READ ASCII	x			x		x	x	x				x								x	x		
WRITE	x			x		x	x	x				x											
WRITE ASCII	x			x		x	x	x				x											
WRITE & COMPARE	x			x		x	x	x				x											
READ NONSTANDARD	x			x		x	x	x															
READ TRACK HEADER	x			x		x	x	x				x								x	x		
FORMAT TRACK	x			x								x										x	x
REQUEST STATUS	x	x		x								x								x	x	x	x
RESET STATUS	x	x		x								x											
WCR WRITE CONTROL REG.				x								x											
RCR READ CONTROL REG.				x								x											
RSR READ STATUS REG.	x			x								x											
RER READ EDAC REG.				x								x											
RELEASE DEVICE	x			x								x											
RESERVE DEVICE	x			x								x											
SET STANDBY	x			x								x											
SPECIAL CONTROLLER CMDS				x						x		x	x	x		x	x	x	x				
BOOTLOAD C.S.				x								x											
ITR BOOT				x								x											
EXECUTE DEVICE				x																			

Table 4

	MPC DEVICE ATTENTION	Configuration Error	Device Number Error	Multiple Devices	CA Unexpected Interrupt		
SEEK			x	x	x		
SPECIAL SEEK			x	x	x		
PRESEEK			x	x	x		
RESTORE			x	x	x		
READ							
READ ASCII							
WRITE							
WRITE ASCII							
WRITE & COMPARE							
READ NONSTANDARD							
READ TRACK HEADER							
FORMAT TRACK							
REQUEST STATUS		x	x	x	x		
RESET STATUS		x	x	x	x		
WCR WRITE CONTROL REG.							
RCR READ CONTROL REG.							
RSR READ STATUS REG.							
RER READ EDAC							
RELEASE			x	x	x		
RESERVE DEVICE			x	x	x		
SET STANDBY			x	x	x		
SPECIAL CONTROLLER CMDS							
BOOTLOAD C.S.							
ITR BOOT							
EXECUTE DEVICE							

5. SOFTWARE VISIBILITY

5.1 COMMAND AND STATUS

5.1.1 Commands

The subsystem commands of the DSS175/180 will be implemented as a modified subset in the DSS181 and DSS190. The subsystem shall read and write multiple sequential data sectors, multiple tracks and multiple cylinders as specified by the EUS.

5.1.2 Status

The controller shall perform the status formatting necessary to reflect subsystem status to the EUS in the form of major status and substatus as defined for the DSS175/180. Additional device and controller status will be returned by the Read Status Register, and Read Control Register commands. The first word of status will be mapped by the MPC, so that the IOM status table will have major and minor status and will look to a user like the status of our current product offerings (167, 170, 180). Additional words of status will be placed in status tables in the controller that may be accessed with Read Status Register command, (Section 3.16) by the operating system.

New major status categories have been added for use by MPC controllers. These new major status are extensions of the present major status. Substatus under these major status will be encoded as one of 64 possible 6-bit codes (as opposed to bit coding). Reference Section 4.

The new major status will be used for reflecting status which cannot be mapped under existing major status categories, due to lack of substatus bits. Where more than one condition exists at any one time, a priority of substatus will be set up and only one condition indicated by substatus under the new major status at any one time.

5.1.3 Instruction Set Consideration

The following items apply to the entire instruction set and must be recognized by the EUS in its use of the subsystem.

- Each instruction which causes any data to be read from or written on a device (rather than controller store) must be preceded by a seek instruction to that device from the same logical channel and the control information associated with that seek can be used for only one data transfer instruction.

- The controller has the ability to recover from certain temporary errors within the subsystem. See Section 5.8 for a discussion of this feature.

5.1.4 EUS Controller Command Sequence

The controller will provide the command sequence interface as defined in the PSI EPS-I, 43A177874.

- All non-valid instruction codes will be rejected with Instruction Reject, Invalid Op Code.

- A Request Status or Reset Status instruction will return the last controller status stored by the controller or summary device status for the given device number. Note that this also includes "Instruction Reject, Invalid Device Code," for addresses where no device is configured on the subsystem.

- Boot Controller initiate status should be "Channel Busy, No Substatus."

- Initiate status for all operation codes (valid instruction codes) should be "Channel Busy, No Substatus." Thus, the channel will reflect "Channel Busy" until a terminate is received from the controller or the instruction is aborted by the EUS (hardware).

5.2 ADDRESSING

5.2.1 Device Addressing

Devices are connected radial and will be numbered 1-32 with physical device number. There will be no (ID plug) logical address plugs.

In DSS181/190 all devices will be addressable from the External User System (EUS). There will be no "S" device code plug denoting a device that cannot be reached except through special controller logic. It is important that all devices be accessible from the EUS in order to utilize the power of TOLTS in on-line testing and diagnosis of devices.

Device Identification

The physical device number and binary device identification number will be set by maintenance personnel at installation time. The numbers will be set from 1 through N (maximum 32) where N is the total number of devices.

For dual personality the devices will be numbered from 1 through N (maximum 16) on each CA.

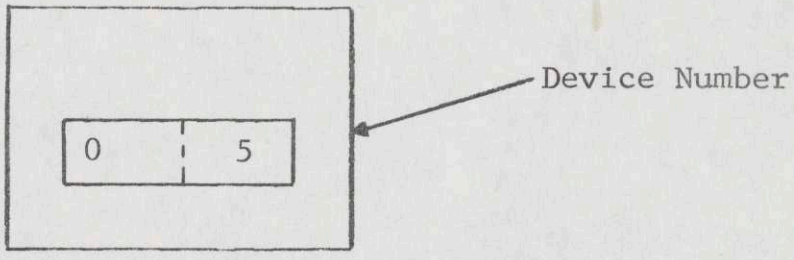
The DSU181 contains means to identify itself by "Type Number." This will be wired into the device in a semi-permanent fashion.

Six-Bit Binary Device Code

Six bits are provided by the EUS for specifying a device code. The six bit device code is the binary code of the two-digit decimal number (1-32) displayed on the device.

The controller will convert the six bit binary field device code into CA number and CA port number. A CA may have from 1 to 16 devices all addressable on-line. Device code 000000 is reserved for the controller.

The device code will be represented on the device as a two digit decimal number based on the binary device code.



Console Output Message

When outputting a device identification to the console typewriter, the software will have to convert the six bit binary device code into a two digit decimal number.

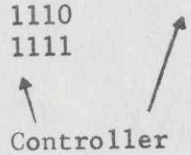
The physical device number visible on the device, binary device code and device identification number are the same and never change. The device number and port number need not be the same. The device identification number and port number (CA + device code) relationship is maintained in the controller. This relationship will be set up at initialization by the controller establishing which physical device is on which CA port. The relationship will be established on a device basis any time there is a power on indication from a device. The controller shall check the device identification number against the established relationship before any operation is performed. If the device identification number is different than previously established for the addressed CA port the controller shall terminate the command with "Device Attention," Device Off-Line.

CA Number	Port No. Internal CA and Device Code	Binary Device ID Number	6-Bit Binary Device Code	Physical Device Number 2-Digit Decimal
	Controller		000000	
0	00 0000	000001	000001	01
0	00 0001		000010	02
0	00 0010		000011	03
0	00 0011		000100	04
0	00 0100		000101	05
0	00 0101		000110	06
0	00 0110		000111	07
0	00 0111		001000	08
0	00 1000		001001	09
0	00 1001		001010	10
0	00 1010		001011	11
0	00 1011		001100	12
0	00 1100		001101	13
0	00 1101		001110	14
0	00 1110		001111	15
0	00 1111	010000	010000	16
1	01 0000	010001	010001	17
1	01 0001		010010	18
1	01 0010		010011	19
1	01 0011		010100	20
1	01 0100		010101	21
1	01 0101		010110	22
1	01 0110		010111	23
1	01 0111		011000	24
1	01 1000	011001	011001	25
1	01 1001	011010	011010	26
1	01 1010		011011	27
1	01 1011		011100	28
1	01 1100		011101	29
1	01 1101		011110	30
1	01 1110		011111	31
1	01 1111	100000	100000	32

Controller Table

Figure Device Code

CA Number	Port No. Internal CA and Device Code	Binary Device ID Number	6-Bit Binary Device Code	Physical Device Number 2-Digit Decimal
	Controller		000000	
0	00 0000	000001	000001	01
0	00 0001	000011	000011	03
0	00 0010	000101	000101	05
0	00 0011	000111	000111	07
0	00 0100	001001	001001	09
0	00 0101	001011	001011	11
0	00 0110	001101	001101	13
0	00 0111	001111	001111	15
0	00 1000	010001	010001	17
0	00 1001			
0	00 1010			
0	00 1011			
0	00 1100			
0	00 1101			
0	00 1110			
0	00 1111			
1	01 0000	000010	000010	02
1	01 0001	000100	000100	04
1	01 0010	000110	000110	06
1	01 0011	001000	001000	08
1	01 0100			
1	01 0101			
1	01 0110			
1	01 0111			
1	01 1000			
1	01 1001			
1	01 1010			
1	01 1011			
1	01 1100			
1	01 1101			
1	01 1110			
1	01 1111			



Controller Table

5.2.2 File Addressing

Initially standard GECOS software will use 64 word sectors on the DSS181. Disk packs may be formatted with either 64 word or 320 word sectors (1440 bytes). The controller will perform conversion of the continuous binary addresses received from the EUS to the noncontinuous cylinder-head sector addresses of the subsystem devices. Bit YY (Section 3.3.1) of the seek address will be set to indicate the addressing algorithm to be used by the controller. Direst "head," "cylinder," and "sector," addressing by the EUS will be used for all nonstandard sector sizes other than (64 or 320 words), including one sector per track. One sector per track may be addressed by either YY = 10 or YY = 11 but must decode to sector zero.

5.2.3 Multitrack Operation

For data transfers within a cylinder, the controller will automatically select the next sequential head on the access mechanism. This selection can be done without losing a disk revolution.

Data transfers to the EUS shall not be limited to a length equal to the sector length, but shall only be limited by the DCW tally, sector (block) count limit, defective tracks, (with no alternate assigned) unrecoverable error conditions, physical end of file, end of cylinder, and a seek address greater than that of the last addressable sector on cylinder 201 or 409.

5.2.4 Sector Size Options

Three sector sizes will be provided, basic 64 word for compatibility with existing disk systems, standard 320 word sector size and one sector per track. Sector sizes of 64 and 320 words will not be mixed on a given disk pack. 64 and 320 word sector packs may be mixed on a subsystem. One sector per track format may be mixed on either the 64 or 320 word formatted packs.

An error condition of MPC data alert status will be returned if the addressing specified does not match the sector size of the track.

The MPC data alert status will also be returned if sector size changes from one sector to another when reading multiple sectors or multiple tracks.

5.3 STARTUP

5.3.1 Channel Assignment and Configuration Control

Channel assignment and configuration control shall be accomplished by setting tables in the controller read/write memory. Basic configuration data will be entered on switches on the MPC maintenance panel and loaded into the tables during initialization. Under failure conditions of some module in the subsystem, these configuration tables will be changed in order to keep the data available and allow the subsystem to operate with only a reduction in throughput.

Configuration data for special configuration may be loaded into the configuration tables at start-up time after the controller has been booted. Loading configuration data from the EUS will be accomplished by using the special controller commands (refer to Section 3.22).

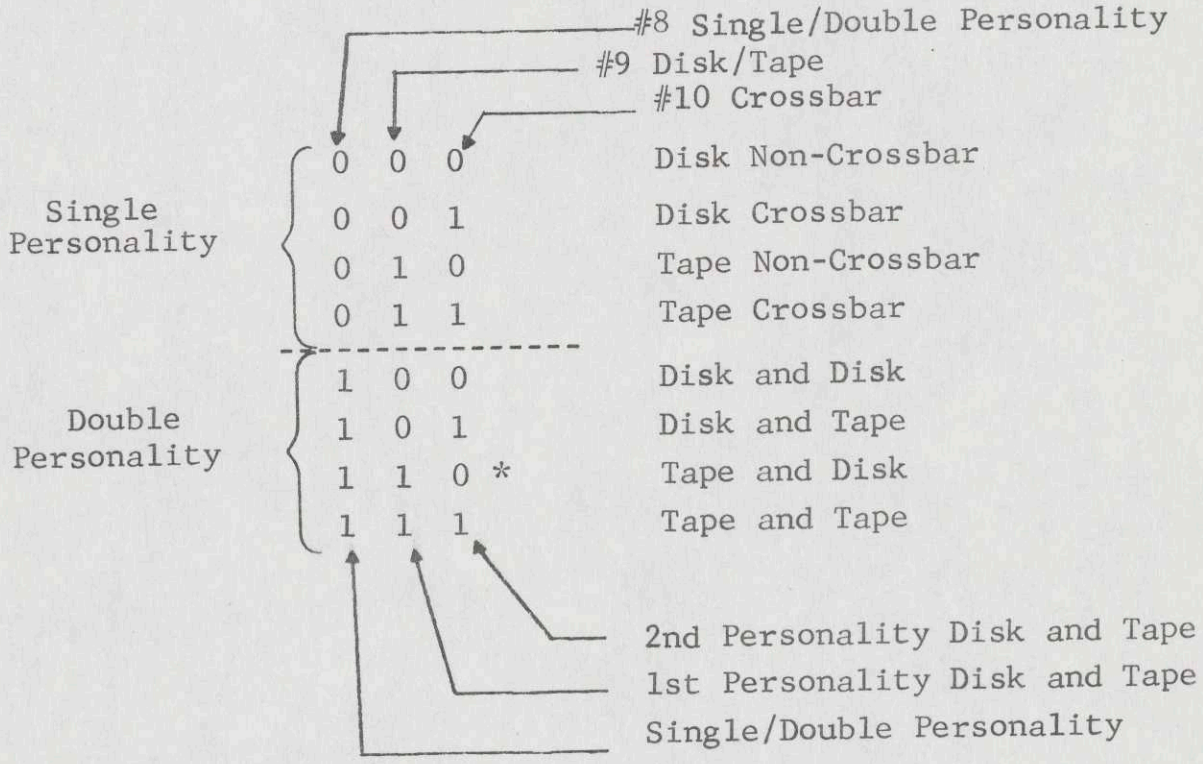
MPC Configuration Switch Allocation

The allocation of the configuration switches of the MPC maintenance panel is as follows:

Switch:
- 0 - ITR BLT Bypass
- 1 - ITR Loop Control
- 2 - LA to be used for booting:
  - 1 = LA on IAI Port 3
  - 0 = LA on IAI Port 2
- 3 - Number of LA's in Subsystem:
  - 1 = One LA (Port 2)
  - 0 = Two LA's (Ports 3 and 2)
- 4 - Inhibit Interval Timer Runout Detection
- 5, 6, 7 - Boot Device Identification
- 8, 9, 10 - Controller Configuration Definition
- 11, 12 - Not Allocated
- 13 - Main Memory Size: 0 = 1K Words, 1 = 4K Words
- 14 - Error Interrupt Safestore Bypass Control
- 15 - Used for Control Store Load (prototype, test only)

Note: Following "dc" initialization of a MPC controller, only PSI 0 of the LA defined by Switch 2 will be monitored for subsequent command from the central processor. Therefore only this PSI interface can be used for system-to-controller communication until the controller "personality" has been branched to as the result of a control store personality overlay command or a reset status command.

Controller configuration switches numbers 8, 9, 10 are defined as follows:



*Illegal Configuration

Configuration Switches

5.3.2 Subsystem Initialization

Initialization of controllers which have no personality firmware at startup and which will receive a personality overlay from the central system.

For configurations where startup has been loaded prior to MPC initialize time, the PSIA patch will be removed and MPC initialize will be provided from software by an initialize PCW. This allows software and/or T&D to set up the special interrupt channel (IOM channel #6) prior to MPC initialize and thereby have the capability to monitor the initialize and firmware overlay functions.

Initialization procedure:

1. The 6000 system is initialized from the system control center. No initialize is sent to the MPC as the PSIA patch is removed.

2. Startup (or T&D) is loaded through a CPI channel.

3. Software (startup or T&D) will set up mailboxes for the special interrupt channel (IOM channel #6).

4. Software will initialize the PSIA and the MPC by issuing the following two PCW's to logical channel #0 of the PSIA:

   - PCW to mask all logical channels within the PSIA and to initialize the MPC (bits 22-26 of the PCW = 37_8).

   - PCW to unmask logical channel #0 (bits 22-26 of the PCW = 00_8).

   The second PCW will be a "Normal" (non-T&D) PCW, and should be set up with associated control words pointing to an IDCW containing a Request Status command for device 0.

   The two PCW's can be in the same list.

   Unless software delays the time between PCW's the second PCW will be sent to the PSIA at a time when the MPC is not present (being initialized or is off-line executing the Basic Logic Test ITR test microprogram). This will result in a

Terminate Interrupt with power-off status being generated by the PSIA to software.

5. The MPC will initialize during which time Operational-In to the PSIA will drop.

6. The MPC will execute the Basic Logic Test Isolation Test Routine.

7. Upon completion of the BLT execution, the MPC will bring up the Operational-In line to the PSIA, and will generate a Special Interrupt, which indicates that the MPC is present and is ready to accept either extended ITR control store overlays, or the MPC personality control store overlay.

5.3.3 Controller Initialize Functions

Channel Initialize

The Channel Initialize function is a logical reset of one channel of the MPC controller, and occurs when the "Operational Out" line of the PSI interface to the controller reverts from the "Operational" to the "Nonoperational" state. (This is an indication that the external system has "gone away" due to either a power-off condition or an external system initialization condition.)

The occurrence of a "Channel Initialize" will cause the MPC controller to reset all activity associated with the physical PSI channel, including any allocation of devices, table entries, etc. Activity associated with any other physical PSI channel is not affected.

Controller Initialize

The occurrence of a "controller initialization" causes the entire MPC controller to be "dc reset." This type of reset is caused by any one of the following:

a. Actuation of the "Initialize" switch on the MPC operator panel.

b. An initialize signal from the MPC power supply during any MPC power-up sequence.

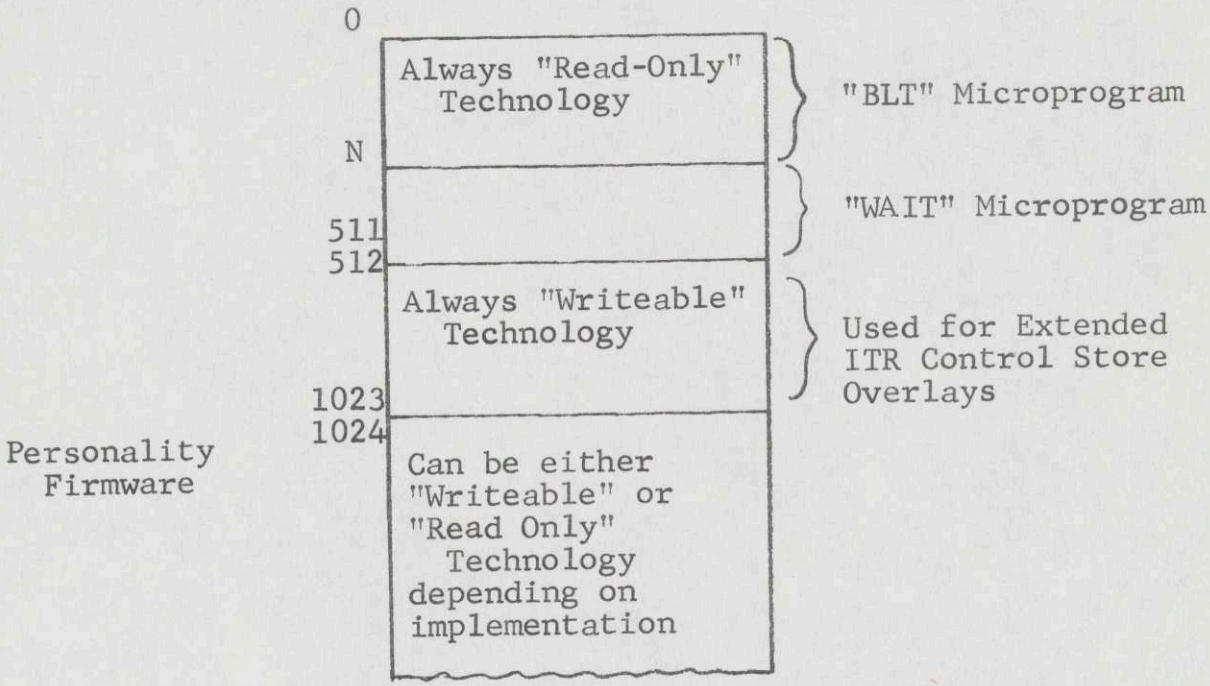
c. A remote initialize signal generated via the "SCAM" module (caused by actuation of the Initialize switch on the SCAM console).

d. A signal on the "Reset-Out" line of the PSI interface to the MPC (this signal is recognized by the MPC controller only if the "Operational-Out" line to the MPC controller is in the "operational" state).

Initialization by means of methos (a) or (b) results in the MPC controller being dc initialized and left in the halt mode, and requires actuation of the Start switch on the MPC operator panel or subsequent initialization by means of (c) or (d) to begin micro-instruction execution.

Upon actuation of the MPC Start switch, or immediately upon the fall of the initialization signal in the case of (c) or (d) above, microinstruction execution begins in the MPC controller starting at control store location 0, which is the starting location of the basic logic test (BLT) Isolation Test Routine microprogram.

The related Control Store memory map is shown as follows:



5.3.4 Control Store Bootload

Following dc initialization, the MPC controller begins microinstruction execution, starting at control store location 0 (except for initialization via methos (a) and (b) described above).

The BLT microprogram will be executed. This microprogram verifies that the basic logic of the MPC processor and link adapters is operational. If a hardware malfunction is detected during this test the BLT microprogram will cause the MPC to halt, with fault dictionary symptoms displayed on the MPC maintenance panel. (Configuration switch on the MPC maintenance panel can be set to cause the BLT microprogram to bypass the logic verification, and go directly to the WAIT microprogram.)

From the time dc initialization occurs until the completion of the execution of the BLT routine, the "Operational-In" line from the MPC controller to the IOM will be reset. This condition will cause any Channel Program initiated by System Software to the controller during this time to be terminated by the IOM with appropriate rejection status.

Upon completion of the execution of the BLT microprogram, the controller will time out for a minimum period of 2 milliseconds. (This is done to allow time for the System Software to "mask" logical channel 0, so the forthcoming Special Interrupt can be received from the controller.)

Following this timeout the controller will raise the Operational-In line to the IOM, and will generate a Special Status Storage and Special Interrupt to logical channel 0. The format of the Special Status Storage, as stored by the IOM in 6000 memory, will be as follows:

1 0 0	IOM Ch. No.	000 000 000	000 000 100	0XX XXX XXX
0	8	9 17	18 26	27 35

Note: If the Special Status Storage or Special Interrupt cannot be executed because the logical channel in the IOM PSI-Adapter is masked, the MPC controller will halt, and Operational-In line to the IOM will drop.

After issuing the Special Interrupt the MPC controller will start execution of the WAIT microprogram. This microprogram will monitor the PSI interface specified by switch 2 of the MPC configuration switches (on the MPC Maintenance Panel), and will detect the initiation of a channel program on this interface. (All other connected PSI interfaces will be ignored at this time.)

Note: Switch 2 set defines the WAIT routine will monitor PSI interface 0 of the LA connected to MPC Internal Port 3. Switch 2 not set defines PSI 0 of the LA connected to the MPC Internal Port 2.

The "WAIT" microprogram will recognize and act upon the following commands from the external user system.

a. Control Store Test Overlay: Op Code = 11_8
Device Code = 00_8

b. Control Store Personality Overlay: Op Code = 10_8
Device Code = 00_8

c. Reset Status Command: Op Code = 40_8
Device Code = 00_8

The reception of any command other than these commands will result in the MPC controller reverting to the halt state, and the Operational-In line to the IOM will drop. (This will result in a "power-off" status to the initiating 6000 system software.)

Control Store Test Overlay and Control Store Personality Overlay: Refer to Section 3.22 and 3.23.

Reset Status Command:

This is the standard Reset Status command as defined.

By using this command, 6000 System Software can interrogate an MPC controller after initializing the controller, to determine if the controller personality is resident to the controller. Upon receiving this command the WAIT routine will branch to the location in control store where the personality firmware should be resident. If personality firmware is present, it will respond to the Reset Status command normally. If personality firmware is not present, an error response (or no response) will result.

Although the WAIT routine can recognize the Reset Status command, the more normal sequence will be for the 6000 System Software to check a controller for "Personality Present" with a Reset Status command before initializing the controller.

Boot Procedure to be used by 6000 Startup Software

1. Check if controller requires rebooting.

   This step is optional.

   If startup software desires to check if the controller personality is loaded and operational, it can issue any legitimate command to the controller. If the controller responds normally, startup software can assume the controller is operational and does not require rebooting.

2. Initialize MPC Controller

   Startup software causes the controller to be "dc" initialized by issuing the "Reset and Mask LC's" PCW to the IOM PSI-Adapter. (PCW bits 21, 22, 23 = 111.)

   This PCW will cause an initialize signal to be sent to the MPC controller over the Reset-Out line of the PSI interface. In addition, all logical channels of the IOM PSI-Adapter will be masked.

3. Unmask Logical Channel 0

   Startup software unmasks logical channel 0 of the IOM PAI-Adapter by issuing any normal PCW to the PSI-Adapter.

   The purpose of this PCW is to insure that logical channel 0 of the IOM PSI-Adapter is unmasked, allowing the subsequent Special Status Storage and interrupt from the controller (signalling the "ready for boot" state) to be received. If logical channel 0 is not unmasked, the controller will detect an error sequence when it attempts to send the Special Status Storage, and will halt.

   The unmask PCW should be executed immediately following the reset PCW.* The MPC controller will delay for a minimum of 2 milliseconds following the completion of the initialize operation before issuing the Special Status Storage and Interrupt, to insure that Startup Software has adequate time to issue the unmask PCW. "Power-off" status will be the normal response to this PCW.

*Note that the Reset and Unmask PCW's can be queued together in the connect channel list, and issued via a single connect.

4. Issue the Control Store Personality Overlay Command

Upon reception of the Special Status Storage and Interrupt over logical channel 0, startup software will initiate the control store personality overlay command.

Execution of this command will result in the controller personality being loaded into the MPC control store. Upon successful completion of this command, the controller will issue a "Ready" status storage followed by a Termination Interrupt, and will then branch to the loaded personality and commenct normal controller operation.

If any error is detected during the overlay command execution, the MPC will revert to the halt state. This will result in "power-off" status to startup software indicating a retry must be initiated, starting with step 2 above.

Special Considerations

Illegal Commands:

Both the "Control Store Test Overlay" and the "Control Store Personality Overlay" command are considered illegal by the normal controller "personality"firmware. This implies that a controller must be "dc initialized" (reset-out line of the PSI) before the controller personality can be reloaded, or before ITR overlay procedures can be executed.

Restrictions on PSI Channel used following MPC Controller Initialize:

Following "dc" initialization of the MPC controller (via Reset-Out line) the controller will respond to command initiated only over the PSI interface specified by Configuration Switch 2 of the MPC maintenance panel. Therefore, 6000 software systems must be aware of the PSI channel defined by this switch setting and use that channel for all command initiations from the time the controller is "dc" initialized until the controller personality overlay is completed, and the normal controller personality is operational.

5.4 DEVICE RESERVE ALLOCATION AND ACCESS CONTROL RELEASE

There are two types of device reservation, implicit and explicit. Implicit reservation of a device to a logical channel is accomplished by selecting a device with a seek or restore command. The preseek command does not reserve the device. The device will remain reserved to the logical channel unit the data transfer command which follows the seek is terminated. When an error is detected during data transfer to or from a device, the device will be released automatically when the command is terminated. When EDAC is used and an error is indicated at terminate the device will remain reserved to the logical channel until a read EDAC register command is executed.

5.4.1 Explicit Device Reserve

This command is not required to enable access to a device. A channel program may be executed by an unseized, available device, but when the Explicit Device Reserve command is issued, that device can then only be accessed via the path (logical channel) that issued the Explicit Device Reserve command issued over the same path (logical channel). The only access that is available to a reserved device from other paths is to obtain summary status from that device.

5.4.2 Switched Channel Control

Either PSI channel of a switched pair LA may access any device on that channel by supplying the proper device number for the desired device. For switched channel configurations, access to any device will be given to the first requesting channel. In the crossbarred subsystem, the controller will attempt to access the device through either CA. If the CA is already in use, the requesting channel will be held busy until the alternate channel goes non-busy. The controller will then service the new request. (See also Section 5.4.5, independent systems sharing the same data base.)

5.4.3 Allocation of Devices

All devices that are on-line are addressable by the EUS. Nonallocated devices are very important in the operation of the subsystem in order to meet data availability requirements. Allocation of devices will be done by the operating system.

5.4.4 Devices Reserved from Allocation

The device allocation capabilities of GECOS and the on-line testing capabilities of TOLTS, allow the use of a versatile spare device philosophy. The allocation of devices to users, and the reserving of some devices for testing, or as spares, can be determined by customer needs -- based upon subsystem reliability predictions and operating statistics.

In most operating environments the important advantage of high data availability will lead to the reserving of one spare device. In such cases any one of the device numbers can be chosen as spare by the software not allocating that device number to production. In the event of a device failure, the data on the failed device can be brought quickly back into operation by deallocating the failed device and changing packs with the device designated as spare and then allocating it to production.

In order to achieve high data availability requires utilization of the spare device and requires the operating system to be able to exchange packs within or between job activities if a device fails and be able to continue the activity after the exchange has been made. The ability to exchange packs between a device that has failed and the device that was designated as spare (not allocated) applies to all types of files including removable files, perm files and perm files which contain operating system modules.

The ability to exchange packs has the following restrictions as presently implemented:

- The operator must initiate the function to exchange packs.
- The system must be able to retrieve all the necessary functions before an exchange can be attempted.
- At the time the exchange is requested, a unused device must be available within t of drives assigned to the particular cha By unused is meant a device which is co and has been either released (not allo or defined as removable and has not y allocated.

- Devices declared as shared with the Data Communications Subsystem via the Mass Store Link cannot be exchanged until the Mass Store Link has been notified, the device released from its allocation, and the new one assigned. This is a time consuming cycle which requires special interfaces. These interfaces must be established before this feature will be included.

If the exchange function cannot be accomplished, the operator must govern system activity. The following actions can be initiated depending upon system disposition:

1. Jobs using the device to be exchanged can be aborted until the device can be exchanged.

2. Device required to be exchanged contains the exchange modules (ST1). In this case, system performance will be extremely poor. The system can be aborted with a restart in mind and with a subsequent warm boot of the system performed. During the warm boot a new configuration card can be inserted via the card reader denoting the new device.

3. If a spare is not available the operator may release a device, it there is a device available to be released, so it can be used to perform the exchange function.

5.4.5 Shared Access

Shared access is a requirement of this subsystem.

It will be the responsibility of the EUS operating system (GECOS) to maintain the file space reservation and check this reservation status before executing a command from an alternate channel. File space may be a portion of a physical device or may bridge several devices. The EUS may use the lock byte capability provided in the controller to perform this function.

It will be the responsibility of the external user computer system to use the Reserve and Release commands if reservation is required at the device level.

The controller will provide Data Path Management (DPM) when shared or multiple access is required by the System/Systems.

5.4.5.1 Data Path Management for Shared Access by One EUS and Data Communications

For configurations (Figures 5.4.5.1a, 5.4.5.1b) where access to the data base is controlled by a single operating system.

The method that shall be used for data path management will be a combination of device pulling, firmware and software conventions.

The interface dialogue and signal discipline discussed in this section conform to the standard (DLI) Device Level Interface and is consistent with NPL.

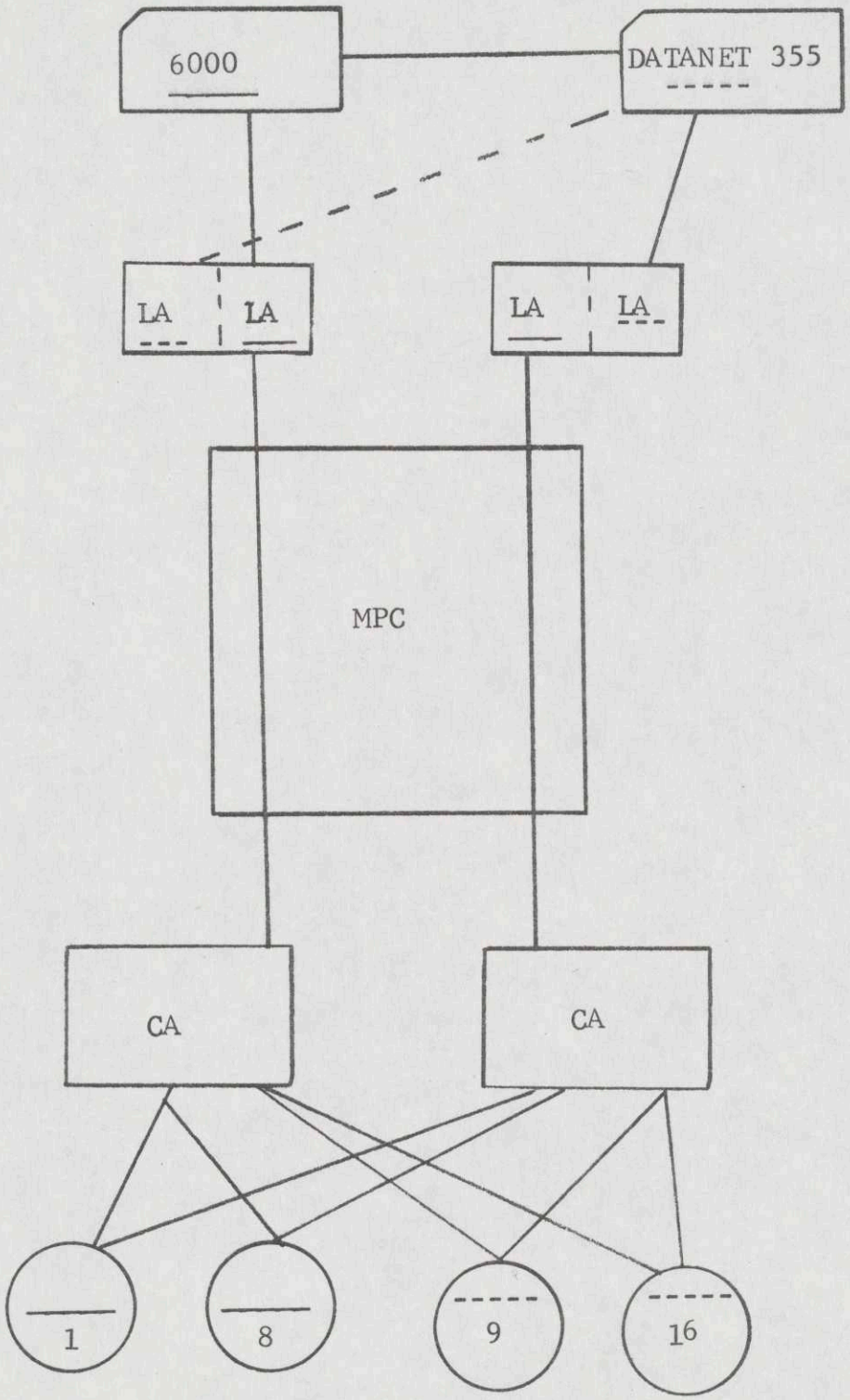


Figure 5.4.5.1a - Dual Channel Crossbar 2 x 16

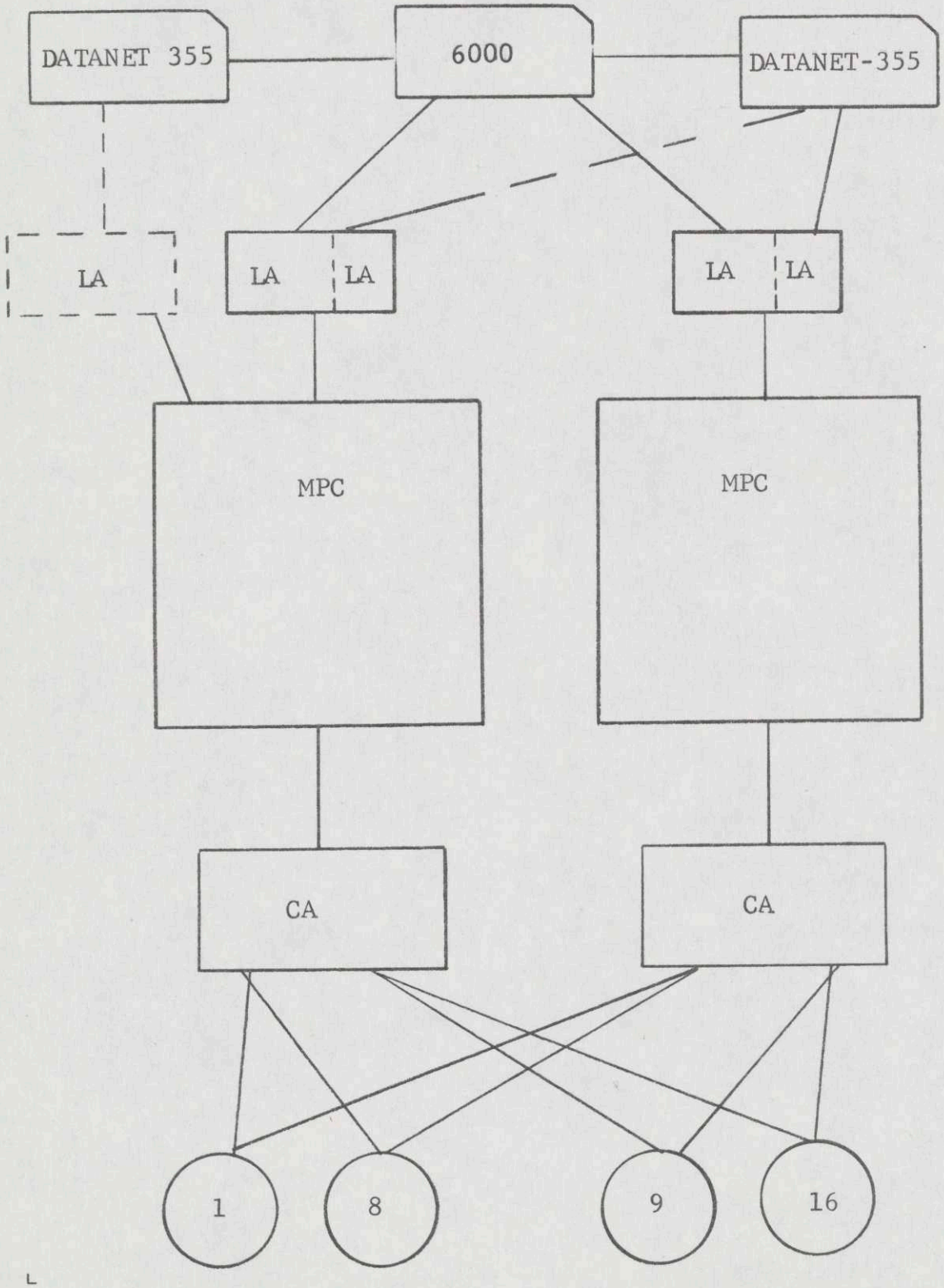


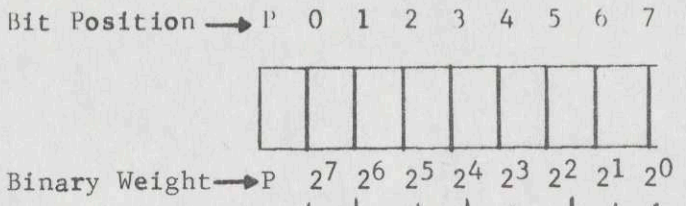
Figure 5.4.5.1b. Dual Channel Crossbar

The controller will use the summary status information as presently defined in the NPL DLI specification (refer Figure 5.4.5.1c) to handle Seek Completes, Pack Change and Alternate Channel in Control.

The controller will use the Block Multiplexing function (logical channels) to perform seek overlap and latency reduction for those commands queued in the controller.

The operating system may use the RCR command if desired. However, outstanding activities will be initiated when there is a logical channel available, even though no Seek Completes are indicated.

- For two controller (crossbarred) subsystems; each physical channel will have at least four logical channels.
- In two controller subsystems where each controller has two channels, the subsystem will look to the EUS, like 2(2X8)'s, that is two crossbarred subsystems.
- The operating system will issue all outstanding preseeks first. Preseeks will be executed first from the controller; that is, all outstanding before a data transfer is initiated.
- In single controller subsystems, the controller will service all outstanding DEN's before an RCR is executed. Therefore DATA in the device tables will be current when an RCR is received.
- When (2) controllers are configured in the subsystem, each controller will POLL the devices on the available CA/CA's approximately every second. Polling will establish the state of the device standby, busy, reserved and ready.



Bit 0 - Device reserved - The MSD is seized through the other port and is unavailable for functional operation through this port.

Bit 1 - Device seized - The MSD is seized through this port and is available for functional operation through this port.

Bit 2 - Device in Standby - The MSD is a Standby mode but can still accept all commands except those involving data transfer or head movement. Refer to the individual device specification for the definition of "standby."

Bit 3 - Positioner Busy - The MSD is executing a positioning command and the heads are in motion. This line is raised (where applicable) for seek, positioner offset, recalibrate, load and unload operations.

Bit 4 - DLI fault - The MSD has detected a fault condition of a type where the probability is low that the cause of the fault is located in the MSD. Diagnostic and recovery procedures should be directed equally at CA, interface, and MSD functions. Refer to Figures 4-3, 4-4 and 4-5 for the specific conditions that set this bit.

Bit 5 - Device protected - The MSD is write protected and will not execute any write commands.

Bit 6 - Device fault - The MSD has detected a fault condition of the type where the probability is high that the cause of the fault is located in the MSD. Diagnostic and recovery procedures should be directed primarily at the MSD.

Bit 7 - Device in diagnostic mode - The MSD is in the diagnostic mode.

Figure 5.4.5.1c. Summary Status Byte

Knowing the previous state of the device will allow the interpretation of pack change when DEN occurs because the device goes from Standby to Ready.

Knowing the previous state of the device will allow the interpretation of Seek Complete when DEN occurs because the device goes from Busy to Ready, if the CA is not busy.

Summary Status

The Summary Status Register in the device contains one byte of generalized information on the condition of the device, as shown in Figure 5.4.5.1c.

Whenever further definition of device conditions is required, detailed status must be requested.

Certain summary status changes initiate sense line signals (DEN's) to the CA: Figure 5.4.5.1d shows these indications.

The Summary Status Request command results in the transfer of the summary status byte from the device to the CA via the data lines. The Summary Status Request command may be issued to an unseized device.

Seek Complete

- Seek complete will be reported in word number 1 of the Read Control Register command (RCR).
- Seek incomplete will be reported in word number 2 as device unavailable and seek complete in word number 1.

  The controller will automatically retry seek incompletes by issuing a recalibrate (restore) and reissuing the seek. If the device still has seek incomplete after three retries, then the controller will issue one more recalibrate and report seek complete and device unavailable in the RCR words.

BIT	0		1		2		3		4		5		6		7	
	DEVICE RESERVED		DEVICE SEIZED		DEVICE IN STANDBY		POSITIONER BUSY		DLI FAULT		DEVICE PROTECT		DEVICE FAULT		DIAGNOSTIC MODE	
CHANGE IN STATE	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓	↑	↓
INDICATION TO ACTIVE PORT	X	X	—	—	—	DEN	—	DEN NOTE 1	FLT NOTE 2	—	—	—	FLT	—	—	—
INDICATION TO RESTRICTED PORT	—	DEN	X	X	—	—	—	—	FLT NOTE 2	—	—	—	FLT	—	—	—
INDICATION IF NO PORT SEIZED	X	X	X	X	—	DEN (BOTH) PORTS	—	DEN (BOTH) PORTS	FLT NOTE 3	—	—	—	FLT BOTH PORTS	—	X	X

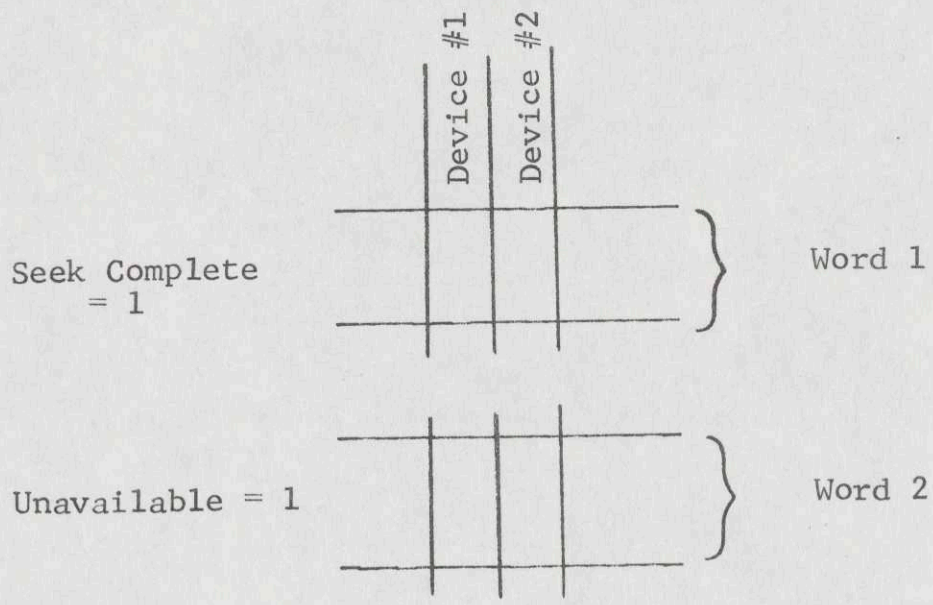
NOTE 1: The DEN indications produced by the falling edge of SS bit 3 (Positioner Busy becoming unbusy) shall also be produced in response to redundant positioning commands (e.g., seek with cylinder difference at zero, recalibrate when positioner is already at cylinder 000).

NOTE 2: Only for those DLI faults associated with this port.

NOTE 3: Only to port associated with the DLI fault.

Figure 5.4.5.1d. Sense Line Indicators for Changes in Summary Status Byte

- Device Busy positioning will be reported in word number 2; word number 1 will be reset.
- The controller will reset the Seek Complete in the device tables when a new activity is executed or when busy is received from the device as a result of polling.



- Seek Incomplete
- Standby
- Off-Line
- Device Busy

	#1	#2	
Positioning	0	0	Device is available - No information about Seek Complete.
• Attention	1	0	Device is available and there has been a Seek Complete.
	0	1	Device is not available - Temporarily still busy positioning.

1 1 Device is not available

- Seek Incomplete
- Standby
- Off-Line
- Attention

Pack Change

- Pack Change will be reported as a Special Interrupt.
- Pack Change is sent to all PSI channels any time Summary Status indicates the device is not in standby and was previously in standby.
- Pack Change

  1. Device failure - Exchange pack between failed device and spare device.

     - GECOS must change physical to logical device relationship table.
     - GECOS or operator must notify Mass Store Link (355) that pack has been moved and the device should be deallocated, before the device comes back on line.
     - Operator may request to GECOS that the pack be moved. GECOS sets device in standby, device seized by controller. Therefore, channel which issued the standby device will get DEN.

2. Device returned to on-line state

   - The controller knows device was in standby and is now ready.
   - The other channels will receive pack change, SPI based on polling.
   - The controller sends SPI to all PSI channels, including Mass Store Link.
   - When a failed device comes back on line for T&D, the device will be explicitly reserved to TOLTS.

Alternate Channel in Control

- Device reserved to alternate channel will not be returned, except as an error condition.

  Normally the device will be reserved (siezed) at the 2 x 1 switch only until completion of the activities, Positioning, Read/Write.

Explicit Reserve

An Explicit Reserve command from the EUS will not normally be used, permanently reserving a device until a Release is issued. Alternate Channel in control will be returned only after Time Out has occurred.

This allows the controller to hold any activities for a given device until the activity has been completed. If an error condition leaves the device reserved, the controller will time out and terminate the command and return reserved to alternate channel status.

The reserve command will not be used as a vehicle for controlling shared access. However, the reserve command may be used where hardware data paths and controllers are shared (for availability), but the devices are used independently. Examples of this application are message switching or test and diagnostic where a device needs to be reserved to a logical channel for a series of activities.

A device will not be reserved to a channel at the device for any period longer than the transaction takes. Seek, read, write.

Devices will be reserved to the channel which issued the seek only during positioning time. If a read/write or other data transfer is not stacked behind the seek in the same channel program, then the device can be accessed by the other controller and the arm moved. The controller which issued the seek will keep a record of the seek to device and use this information to reject the read or write command if the read or write is not preceded by a seek on the same logical channel.

When a device is used in shared access, there will not be any alternate channel in control except as an error condition in which the device is reserved to a channel due to a fault and cannot release the device. The MPC will time out reserve to alternate channel.

5.5 CHANNEL PROGRAMS

5.5.1 Instruction Data Control Word (IDCW) Format

The IDCW is used to place instructions for peripheral devices at appropriate places in a DCW list accessed only by list services. Any distinction in interpretation of the fields is given in the description of that field. The whole IDCW plus 4 zeros (5 bytes) is sent to the controller.

0 5	6 11	12 17	18 20	21	22	23	24 29	30 35	39
DEVICE INSTRUCTION	DEVICE ADDRESS	IGNORE	111	MASK	CONT	MARK	CHANNEL INSTRUCTION	CHAR OR RECORD TALLY	0000

The interpretation of these fields is as follows:

Device Instruction (Op Code)(Bits 0-5) -- This instruction is transmitted directly to the controller during the instruction sequence.

Device Address (Device Code)(Bits 6-11) -- This code is also transmitted to the controller during the instruction sequence. The first IDCW in a Channel Program will establish the device code and subsequent IDCW device codes will be ignored. This will make it impossible for a program to switch devices within a channel program (DCW list).

Bits 12-17 -- These bits are unused and unchecked.

Bits 18-20 -- Must be "111" -- If not, MPC controller reflects "channel status" of "011" in termination status message. (Channel status sent in bits 2, 3, 4 of byte 3 of MPC generated status message. See Section 5.2.)

Bit 21 -- Ignored.

Bit 22, 23 -- Continue/Marker Bits -- These two bits define the action to be taken by the MPC controller upon completion of the I/O operation:

Cont	Mark	
0	X*	The controller stores terminate status and causes a terminate interrupt at the end of this IDCW execution. This IDCW is the last IDCW in list.
1	0	This is not last IDCW in list. Upon completion of execution of this IDCW with Ready and no faults detected, the controller will issue a "Move Pointer" service code and obtain a new IDCW.
1	1	Upon completion of the execution of the IDCW, with ready status and no faults detected, the controller will store marker status and cause a marker interrupt, and then issue a "Move Pointer" service code to obtain a new IDCW.

Bits 24-29 -- Channel Instruction -- This field must contain one of the following codes:

00_8 -- Unit record transfer.

02_8 -- Peripheral action (nondata transfer; e.g., request status, release, restore).

*If continue bit equal zero then the mark bit is ignored.

06_8 -- Multirecord instruction. Illegal for disk controller.

10_8 -- Single character record (e.g., write file mark). Single character contained in bits 30-35 of IDCW. Illegal for disk controller.

$2X_8$ -- Command Extension Modifiers.

$4X_8$ -- Special controller commands (refer to Section 3.2.2).

In order to provide this capability, the "Channel Instruction" field of the IDCW (bits 24-29) will be provided with a new code in addition to those currently defined:

Bits	24	25	26	27	28	29	Octal	Definition
	0	0	0	0	0	0	0	Currently defined as "Unit Record Transfer"
	0	0	0	0	1	0	02	Currently defined as "Peripheral Action"
	0	0	0	1	1	0	06	Currently defined as "Multirecord Instruction"
	0	0	1	0	0	0	10	Currently defined as "Single Character Record"
	0	1	X	X	X	X	2X	New Definition, "Command Extension"
	1	0	X	X	X	X	4X	Special Controller Commands

The controller will examine the "Channel Instruction" field of the IDCW. If the high-order two bits of the field are encoded "01" it will then interpret the four low-order bits as follows:

Command Extension Modifiers:

IDCW Bits 24-29

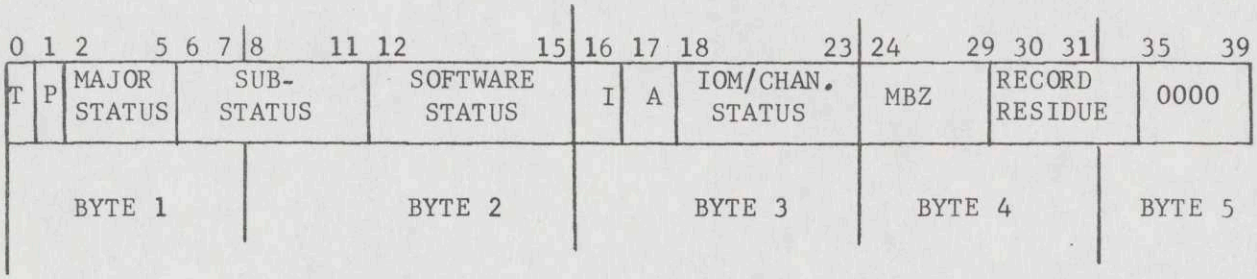
00 0001	21_8	Inhibit automatic retry
01 0010	22_8	Inhibit alternate track logic and end of cycle logic. • Read
01 0011	23_8	Special permission execution. • Read override RPS queue • Write override RPS queue
01 0100	24_8	EDAC Override DSS190, Check Character Override DSS181 • Write without EDAC and write the 7 bytes of error code as data from the EUS. • Read and transfer (EDAC) error code to EUS as data. • Read and transfer check character (CK), ID byte (ID), bit count (CNT), to EUS as data.
01 0101	25_8	Read and perform error correction on the data before transferring data to the EUS. (288 bytes record only.)
10 0000	40_8	Special Controller Command • Interpret the operation code as defined in Section 3.21.

The controller must check that this field is one of the above codes. In the event an illegal/undefined code is detected, the controller will reflect a "Channel Status" of "010" in the termination status message.

Bits 30-35 -- Record Tally or Character -- This field contains the character for a single character record (channel instruction field - 10), or the number of times the device instruction is to be re-issued by the controller (channel instruction field - 02 or 06). No specific checking required on this field.

5.5.2 Status Formats

The controller must recognize user faults reported to it by IOM central, and store this together with peripheral subsystem status, as shown in the description of the MPC status word as follows:



The status word format generated by the controller is compatible with the IOC-C format. The content of the IOM/channel status field is encoded differently. The fields have the following definitions:

Entry Present Bit (0) - Store as a one by the controller; software presently resets this bit to zero in EUS memory to indicate that the status has been examined.

Power Bit (1) - Is set to zero by the controller. Is set to one by the PSIA if the controller does not have its power on, or if there is no controller attached.

Major Status (2-5) - The major status from the controller. Zero when the power bit is one (and stored by PSIA).

Substatus (6-11) - The substatus from the controller. Zero when the power bit is one (PSIA action).

Software Status (12-15) - Stored as zero by the controller; is presently used by GECOS to indicate software detected errors to the slave program after the hardware has stored the status word.

Initiation Interrupt (16) - A one if the controller did not transfer data as a result of this instruction; i.e., this status occurred during an instruction sequence.

Abort Bit (17) - Stored as zero by controller. It is set to one by software if this transaction caused the program to be aborted.

IOM/Channel Status (18-23) - The IOM status field is divided into two independent 3-bit segments; bits 18-20 represent channel detected User Faults and bits 21-23 represent IOM central detected User Faults reported to the channel. These fields are formatted by the PSIA and sent to the controller for inclusion in the controller status word.

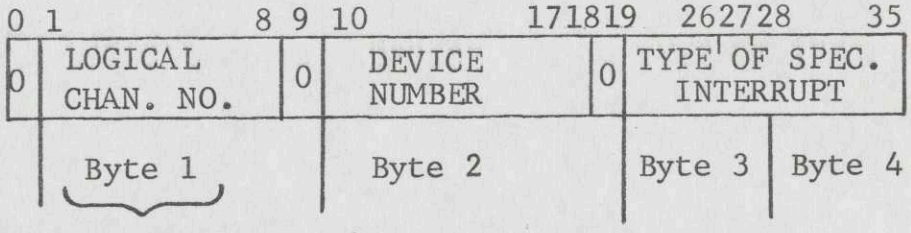
MBZ (25-29) - Unused at present; must be zero (MBZ).

Record Count Residue (30-35) - Residue record count for a peripheral action or multiple record instruction; these are defined as illegal in Section 5.5.1 and therefore stored as zero in all cases.

5.5.3 Special Interrupt Status

The IOM special interrupt channel 6 will be used by the controller to store special interrupt status.

SPI Status Word, Four Bytes stored in ASCII made by PSIA.



PSIA will insert the IOM channel number

Device Number "0" indicates the Special Status Storage concerns the MPC controller, as opposed to a particular physical device.

The following special status entries have been reserved for use by the controller (Device Number 0):

$(000)_8(000)_8(001)_8(000)_8$ - Issued by controller upon acceptance of Suspend command.

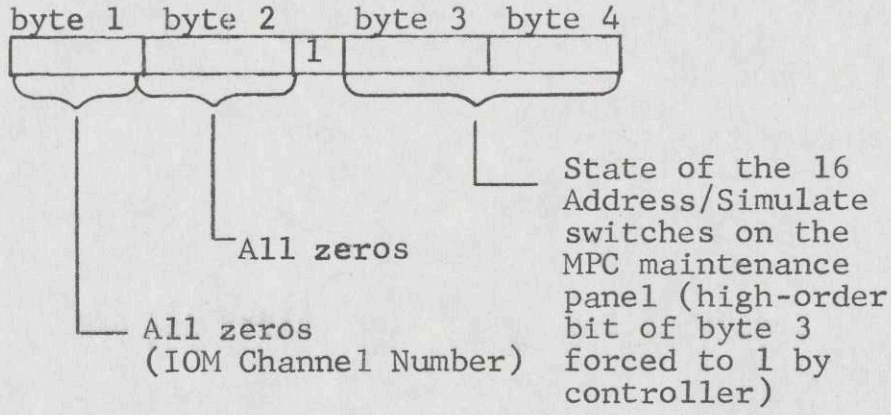
$(000)_8(000)_8(002)_8(000)_8$ - Issued by controller upon acceptance/execution of a Release command (terminates "suspend" state)

$(000)_8(000)_8(004)_8(000)_8$ - Initialize or ITR Boot Special Interrupt.

Generation of Special Status Storage via Operator Interrupt Switch

A "Special Status Storage" can be caused to occur from the MPC operator panel by actuation of the Operator Interrupt switch.

The format of this Special Status Storage will be as follows:



The Special Status Storage will be followed by generation of a Special Interrupt.

The Special Status Storage/Special Interrupt will be sent to all connected physical PSI interfaces over the logical channel that has the device reserved, or through logical channel zero if the device is not reserved on the physical channel.

Special Interrupt Type Codes:

Pack Change, Power On - 000 001

Device Released - 000 010

5.6 SPECIAL INTERRUPT PROCESSING

5.6.1 Device Event Notification

Device Event Notification (DEN) is a device related condition which may cause a Special Interrupt to be sent to the EUS. There are four categories of Event Notification to be considered:

- A Seek/Release/Preseek operation has been completed (busy to ready).
- A device reserved to one CA has been released (reserved or neutral).
- Power-on has occurred. Spindle on heads loaded (standby or ready).

If a device is connected to only one controller adapter, the MPC will receive only one event notification condition; however, if a device is connected to two CA's (dual port access) of one MPC, certain event notifications for the device will be reported over both CA's. When a device is reserved to a given CA, event notification will be reported to the MPC over both CA's.

5.6.2 Special Interrupts

The Special Interrupt is the means by which the controller reports Device Event conditions to the EUS. To minimize EUS overhead, the controller will selectively report Special Interrupts in the following manner:

a. Special Interrupts for Power-on (pack change), will be reported to all physical LA channels.

b. Device released to requesting channel causes a special interrupt to be sent only to the requesting physical EUS channel(s).

5.6.3 EUS Use of Multiple Seeks

The multidevice character of the subsystem and its relatively long access time (time required for seeks plus latency time), suggest the use of preseeks and multiple seeks to optimize subsystem performance. Such procedures imply that data services are not necessarily taken in the order in which the requests for service enter the queue within the controller.

To increase subsystem throughput, the EUS should position the device arm on the required cylinder prior to issuing the data transfer instruction. Thus, if there are multiple device I/O requests queued for the subsystem, the EUS should issue all possible seek operations prior to issuing the first data transfer. To determine which seek operations have been completed the EUS should interrogate the subsystem by the use of the Read Control Register instruction.

In response to this instruction, the subsystem reports, in part, seeks completed information for all devices. The data transfer commands can then be directed to those devices which have completed their seek operations.

Following each data transfer, new seeks may be issued (for new requests in the queue) and the Read Control Register instruction again is used to determine other seeks completed. In this manner, data transfer is overlapped with seeks on other devices with the corresponding optimization of throughput.

5.6.4 Command Stacking

A command stacking facility will be provided in the controller for use by the EUS. This feature enables the EUS to stack (per device) one additional reserving seek operation "on top of" a nonreserving seek type operation (preseek). Also, a device data transfer command, i.e., Read, Write, etc., may be stacked on top of a previous reserving seek (only) instruction. The Seek/Read/Write pair must be in the same channel program set up from one channel.

The reader should refer to Section 5.6.3, "EUS use of Multiple Seeks" for recommendations on the use of subsystem by the EUS for optimum performance.

When seek type commands are being stacked, only one command will be stacked on top of the command currently in (off-line) execution. Additional seek type instructions for the given device will be taken in sequence by the controller. Note that the Restore instruction may be stacked but the channel will remain busy until the Restore is initiated.

When the controller processes a stacked seek type request, it will initiate the positioning operation and unless the IDCW is chained, it will then terminate with appropriate status.

Data transfer instructions may be stacked on a reserving seek, immediately preceding. (Refer to Section 5.6.3.) In this case, the logical PSIA channel and device will remain busy until the arm has been positioned and the data transfer has been completed. Error recovery will cause the current IDCW to be re-executed.

All EUS command sequences, regardless of the stacking feature, are subject to the Instruction Reject, Invalid Instruction Sequence verification. For all valid combinations of Seek and Data Transfer instructions that are successfully executed, the status will be reported with the termination of the last instruction.

5.6.5 Block Multiplexing (BM) DSS190

Block Multiplexing on the PSI I/O channel of the IOM provides a facility for the subsystem to disconnect from a logical channel after an operation has been started such as a Seek/Data Transfer sequence and to reconnect the logical channel when the device is ready to begin a data transfer.

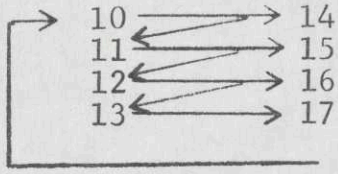
Standard configuration will be four logical channels per physical PSI with eight maximum. The logical channel numbers assigned to a physical channel are in numerical sequence. The logical channel number and device number relationship will be established when a connect is made and the channel program is set up.

The subsystem will accept and store up to one command sequence per logical channel or up to eight command sequences per physical channel. This capability when used with rotational position sensing allows the subsystem to service a greater number of I/O requests.

Standard single physical channel (four logical) will look to the EUS like a four-way crossbar. Standard dual simultaneous physical channels (four logical per PSI) will look like an eight-way crossbar.

Since the logical channel numbers are in sequence the EUS should set up an alternating channel table as shown below:

Assume logical channel number 10, 11, 12, 13 assigned to physical #1 and 14, 15, 16, 17 assigned to physical #2.



The controller will do latency reduction and change the logical channel number so that the correct DCW can be accessed in the IOM when data transfer starts. Each Seek Read/Write pair will be a different logical channel number. The lowest logical channel number will have the highest priority from the physical channel to the controller. A Command Extension Modifier can be set in the IDCW to notify the controller to take a particular command first and bypass latency reduction.

5.7 DISK PACK PROCESSING

5.7.1 Stranger Pack Processing (2314 or 3330 Formats with Nonstandard Sector Lengths)

The controller will be expected only to format "Stranger Packs" to the standard formats. There will be no facilities over the EUS interface for writing non-standard formats other than 64, 320 word or full track sectors. Reading nonstandard formats will be handled by a special command (read nonstandard sector size).

The accidental mounting and reading of a nonstandard format pack will not cause a failure of the controller. When it is determined that a pack is nonstandard, the controller will report MPC data alert "nonstandard sector size" status to the EUS. Nonstandard format pack will be identified as having a sector length other than 288 bytes, 1440 bytes or one sector per track.

Read Nonstandard Sector Size

This command will read an entire track starting with Home Address and will transmit counts, keys and data areas to the EUS. This command must be preceded by a seek with cylinder (CL), head (HH), but must be to sector zero. Only one track will be read, i.e., no head switching.

5.7.2 Formatting and Verification

Disk Pack Formatting and Verification

A software program will be provided for the customer to use in formatting and verifying disk packs. Verification, as used in this paragraph, means recording a selected worst case data pattern in each sector on the disk pack, reading, and verifying the data pattern(s). This program shall include recognition of defective tracks, assigning alternate tracks, if appropriate, and providing a record of these actions that is available to GECOS and accessible to the operator. This program shall accept as an input, vendor certification (defective track) data so that known defective tracks can be recognized.

Header Verification, Format Protect (Header Bypass)

The Header Bypass switch affects only the Format Track instruction. With the switch in the "OFF" position, the track address is verified before the track is formatted. To facilitate formatting a blank track, or a track that cannot be verified due to error conditions, the Bypass switch is placed in the "ON" position and the formatting is accomplished without track address verification. This switch is a software switch and is part of the format track command.

5.7.3 Defective Track Handling

The subsystem shall provide through use of the format track command, the ability to flag tracks on the disk packs magnetic surface, in four ways, as follows:

00 Good Primary

01 Good Alternate

10 Defective with Alternate Assigned

11 Defective with No Alternate Assigned

Defective track data obtained from disk pack certification procedures, will be an input to the Format Utility Routine. These marginal tracks may be recorded as defective, with no alternate assigned (11) and deleted from usage. or flagged defective with alternate assigned (10) and have an alternate track assigned.

5.7.4 Alternate Track Processing*

Once a track is formatted defective, (flagged in each sector header) and an alternate track address is recorded in the RO data field, attempts to write or read on the defective track shall result in the controller automatically seeking to the alternate address and performing the required data transfer operation. Following the completion of the data transfer on the alternate track, the controller shall return the actuator to the cylinder from where the defective track existed and continue the data transfer on the next rack. The EUS shall not be notified that this sequence of events occurred.

Should the controller detect a track with both track indicator bits set, the operation would be terminated with End-of-File, defective track detected, no alternate assigned status. Also, if the alternate address contained in the defective track were not a legal address, or Seek Incomplete or Header Verification error occurred when trying to access the alternate track the controller would respond with End-of-File defective track detected, no alternate assigned.

The execution of alternate track processing is under control of the IDCW and may be inhibited by command extension modifier (22). Refer to Section 5.5.1.

5.7.5 Cylinder End-of-File Processing*

When an end-of-cylinder condition is encountered, the controller shall automatically reposition the arm and continue with the data transfer on the next cylinder. If an error occurs in positioning to the next cylinder or it is the last user cylinder, the controller will terminate and return EOF last consecutive sector.

The execution of cylinder end-of-file processing is under control of the IDCW and may be inhibited by command extension modifier (22). Refer to Section 5.5.1.

*Not available on Initial DSS181

5.8 ERROR DETECTION AND RECOVERY

5.8.1 Controller Error Processing

Operations that detect certain device errors or recording surface errors may be temporary. The controller will automatically attempt to correct these errors three times before it reports the error to the EUS.

Automatic retry will be accomplished by moving the List Pointer in the IOM back to the last IDCW and retransferring the data records. (Refer to PSIA EPS-1, 43A177880).

If the error is corrected, the controller will continue as though no error had occurred. Thus, the error will be transparent to the EUS except for a longer than normal instruction execution time. The command will terminate with Ready Major status and substatus of 1, 2 or 3 indicating the number of retries performed. If the operation is still unsuccessful, the controller will complete the operation as necessary with the appropriate status reported to the EUS.

Those errors which are subject to three automatic recovery attempts by the controller are as follows:

1. Seek Incomplete as a result of any seek type instruction. Recovery will be attempted for Special Seek, Seek, Preseek.

2. Data alert header verification error as a result of sync failure, double index, or compare next count error. No repositioning will be attempted by the controller.

3. Transfer timing errors.

4. Check Character Alert on any read type instruction. This includes both count fields and data fields for all records.

5. Parity errors across the PSI (detected by the LA), or DLI.

6. EDAC (DSS190) error detected will be retried nine times before correction is indicated (3 normal, 3 head offset and 3 clock offset).

There will be a count of these errors maintained for each device. These counts will be available to the EUS through the Read Control Register command.

There is a possibility that imbedded DCW's (i.e., DCW's included in the data being read from the disk) can have an error in the address which will cause data to be sent to the wrong address in memory. Automatic retry by the controller should not be used for records which have imbedded DCW's since the retry if successful will put the data in the correct location but will not correct the locations where data was sent on the first transmission.

The execution of automatic retry is under control of the IDCW and may be inhibited by the command extension modifier (21). Refer to Section 5.5.1.

Automatic retry will be performed on each error type for each command listed below:

1. Seek Errors

   Seek
   Special Seek

2. Header Verification Errors

   Read
   Read ASCII
   Write
   Write ASCII
   Read Track Header
   Write and Compare

3. Transfer Timing Errors

   Read
   Read ASCII
   Write
   Write ASCII
   Write and Compare

4. a. Check Character Alert Data

      Read
      Read ASCII

   b. Check Character Alert Count Field

      Read
      Read ASCII

Write
Write ASCII
Read Track Header
Write and Compare

5. a. Parity Errors

Read
Write
Read ASCII
Write ASCII
Read Track Header
Write and Compare
Special Controller Commands

b. Invalid Seek Address

Seek
Preseek
Special Seek
Format Track

The basic MPC has built-in logic to detect internal hardware errors, such as parity errors on internal registers, parity errors on Main Memory (read/write) data, parity errors on microinstructions accessed from Control Store, etc.

The detection of any one of these internal hardware errors will result in the automatic execution of an error interrupt, which forces the MPC to branch to a fixed control store location, and establishes an "error interrupt in progress" state of the machine.

The microprogram which is automatically entered as a result of the error interrupt will first test the state of Configuration Switch #14 of the maintenance panel. If the switch is set, an immediate branch will be made to the Integrated Test Routine (ITR) module, located in the first 512 locations of control store. (The exact entry point to be determined during implementation.) Setting of Switch 14 therefore implies that the MPC controller will be put in the ITR mode upon the occurrence of an error interrupt.

If switch 14 is not set, the error interrupt microprogram will take the following actions:

a. Safestore in a fixed main memory area (to be defined) the current contents of all pertinent hardware registers.

b. Terminate all existing activity in progress, including device movement. This must be evaluated and implemented on a device type basis. The execution of an active channel program (DCW list) will be aborted.

c. Reset the error interrupt level, and return the controller to normal operation (i.e., waiting for command from central system).

The occurrence of the error interrupt will force the "Operation-In" line of the PSI interface to the EUS to revert to the "nonoperational" state. This line will stay in the "nonoperational" state until the "error interrupt in progress" state is reset by the MPC microprogram.

Detection of Error Interrupt Sequence by the EUS

The external indication that an MPC controller has taken an error interrupt is the dropping of the "Operational-In" line of the PSI interface to the EUS. This line will be down for the duration of time the MPC controller is in the "error interrupt in progress" state, which is a function of how many microinstructions must be executed by the error interrupt microroutine. As an order of magnitude, it can be assumed the "Operation-In" line will be down for approximately 15 microseconds. Repeated error detections will result in repeated error interrupts, and subsequent fluctuation of the "Operational-In" line.

The PSI Adapter in the IOM will detect the PSI "Operation-In" line dropping if a channel program (DCW list) is currently being executed for any one of the eight logical channels of the PSI. The adapter will generate a status storage, and mask the logical channel.

The MPC error interrupt occurrence will go undetected by the EUS however, if no logical channel of the PSI interface is active or initiated, during the time the "Operation-In" line to the IOM is down.

As described above, execution of an error interrupt sequence will result in the safestoring of pertinent registers in MPC main memory. This safestore area can be accessed by the EUS for diagnostic purposes as required, using the "Read Controller Main Memory" Special Controller command. (Refer to Section 3.3.21.)

5.8.2 Sector Limit Protect

The controller will perform file protection by limiting the data sectors available to the processing system following each Seek instruction. The sectors available per-seek-instruction shall be specified by the processing system and can very from 1 to N.

The desired sector count shall be sent to the controller during the execution of a Seek instruction. A sector count of zero shall be interpreted as the maximum number of sectors (4096) available.

5.8.3 Command and Address Integrity (Sum Check)

Check Character for EUS-Controller Communications

An additional check will be provided on certain types of data transmitted from EUS to the controller. Specifically, the data for format type operations, and all data transmitted to the controller with the special controller instruction should have a sum check type of check character in the last word transmitted. The data received shall be checked against the transmitted check character by the controller and the results compared. Only if the comparison is good, will the controller continue with the operation.

5.8.4 Error Detection and Correction Process DSS190

A 56 bit cyclic redundant check will be appended to count, key, and data fields. The generator polynomial is

$$P(X) = X^{56} + X^{55} + X^{49} + X^{45} + X^{41} + X^{39} + X^{38} + X^{37} + X^{36} + X^{31} + X^{22} + X^{19} + X^{17} + X^{16} + X^{15} + X^{14} + X^{12} + X^{11} + X^{9} + X^{5} + X + 1$$

This code has single error-burst correction capability with extremely high probability of detection for longer error bursts.

The encoding process utilizes a single 56-bit linear feedback shift register. Information is serially input to this register. At the completion of the information input the register contents serve as the check bits. Gating of the check bits out of the register necessitates feedback enable/inhibit control.

The decoding, that is, checking and error identification utilizes a high-speed decoding technique introduced by R. T. Chien. ("Burst-Correcting Codes with High-Speed Decoding", IEEE Transactions on Information Theory, pp. 109-113, January, 1969.) This technique deals with the factors of P(X) and the computational capabilities of the system.

$P(X) = P_0(X)\ P_1(X)\ P_2(X)\ P_3(X)$, where,

$P_0(X) = X^{22} + 1$; Order = 22,

$P_1(X) = X^{11} + X^{7} + X^{6} + X + 1$; Order = 89,

$P_2(X) = X^{12} + X^{11} + X^{10} + X^{9} + X^{8} + X^{7} + X^{6} + X^{5} + X^{4} + X^{3} + X^{2} + X + 1$; Order = 13,

$P_3(X) = X^{11} + X^{9} + X^{7} + X^{6} + X^{5} + X + 1$; Order = 23,

During a read operation data is serially input to the four linear feedback shift registers simultaneously. These registers are constructed according to polynomials $P_0(X)$, $P_1(X)$, $P_2(X)$ and $P_3(X)$. Utilization of the same 56 flip-flops use as a generator necessitates additional feedback control.

Upon completion of a field being read, including the 56 check bits the four check registers will contain $S_0(X)$, $S_1(X)$, $S_2(X)$, and $S_3(X)$; this is known as the syndrome. The following table shows the meanings of the $S_i(X)$ combinations:

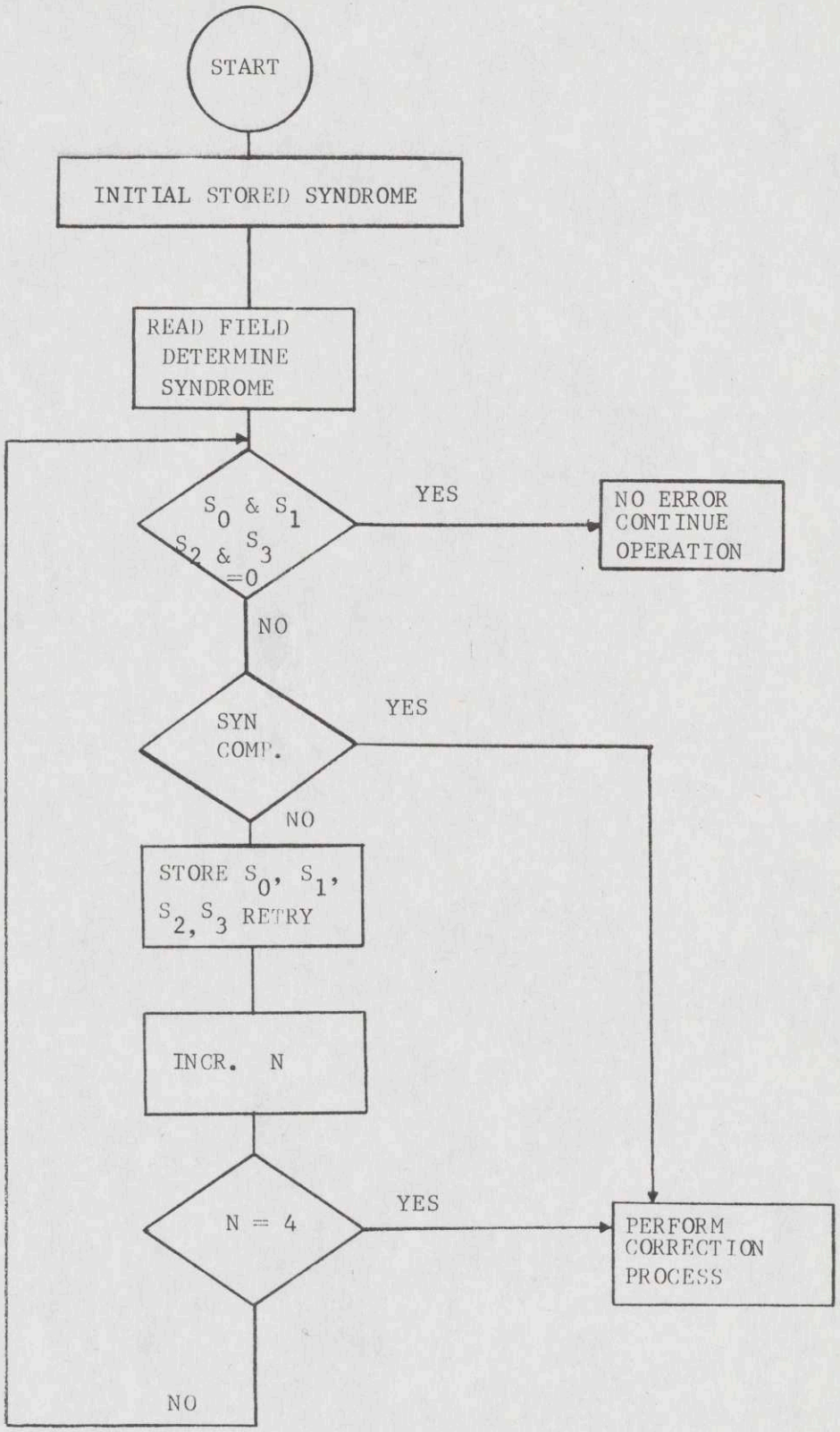
$S_0(X)$	$S_1(X)$	$S_2(X)$	$S_3(X)$	Comment
0	0	0	0	No error or non-detected error
0	≠0	-	-	Noncorrectable error
0	-	≠0	-	
0	-	-	≠0	
-	0	≠0	-	
-	0	-	≠0	
≠0	0	-	-	
≠0	-	0	-	
-	≠0	0	-	
-	-	0	≠0	
≠0	-	-	0	
-	≠0	-	0	
-	-	≠0	0	
≠0	≠0	≠0	≠0	Possible correctable error

Upon receipt of detected erroneous data the syndrome $S_0(X)$, $S_1(X)$, $S_2(X)$, $S_3(X)$ shall be saved. A retry shall be attempted and if an error is again detected comparison of the present syndromes with the saved syndromes will take place. If the two sets of syndromes compare a permanent error may be assumed and a correction attempt shall be made. If the syndrome miscompare, the syndrome of the first retry will be to attempt an error-free read. If the second retry is also detected as erroneous the process of syndrome comparison will repeat. If after four retries the errors persist and yield different syndromes a correction will be attempted. This retry procedure is flowcharted below.

The error identification process will be initiated by the MPC/CA. An 11-bit error pattern and r_0, r_1, r_2, r_3 will be transferred to the system for computation of error displacement and correction of appropriate data bits.

The details of displacement are shown below. It should be noted that the natural code length is 585, 442 bits. This must be incorporated in the calculations if displacement is measured from the MSB of information.

Initialization to zero of EDAC registers prior to encoding and decoding is required.


START
INITIAL STORED SYNDROME
READ FIELD DETERMINE SYNDROME
S_0 & S_1 S_2 & S_3 =0
YES
NO ERROR CONTINUE OPERATION
NO
SYN COMP.
YES
NO
STORE S_0, S_1, S_2, S_3 RETRY
INCR. N
N = 4
YES
PERFORM CORRECTION PROCESS
NO

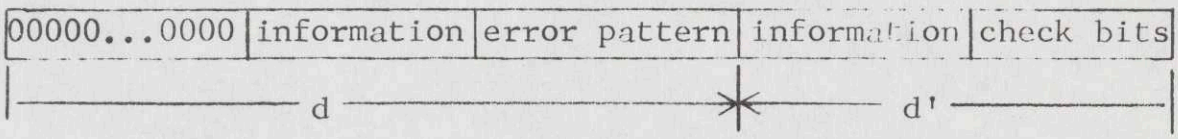
Error Identification

r_0 = number of shifts P_0 must undergo to transform s_0 to a correctable error pattern. (r_0 max = e_0)

r_1 = number of shifts P_1 must undergo to transform s_1 to a bit-to-bit comparison with the least significant segment of P_0. (r_1 max = e_1)

r_2 = number of shifts P_2 must undergo to transform s_2 to a bit-to-bit comparison with the least significant segment of P_0.

r_3 = number of shifts P_3 must undergo to transform s_3 to a bit-to-bit comparison with the least significant segment of P_0. (r_3 max = e_3)



$$d = [452387\ r_0 + 72358\ r_1 + 315238\ r_2 + 330902\ r_3] \bmod 585442$$

$$d' = [452387(e_0-r_0) + 72358(e_1-r_1) + 315238(e_2-r_2) + 330902(e_3-r_3)] \bmod 585442$$

General displacement equation:

$$d = A_0\ LCM(e_1,e_2,e_3)\ r_0 + A_1\ LCM(e_0,e_2,e_3)\ r_1 + A_2\ LCM(e_0,e_1,e_3)\ r_2 + A_3\ LCM(e_0,e_1,e_2)\ r_3$$

where,

$$A_0\ LCM(e_1,e_2,e_3)r_0 + A_1\ LCM(e_0,e_2,e_3)\ r_1 + A_2\ LCM(e_0e_1,e_3) + A_3\ LCM(e_0,e_1,e_2) = 1 \bmod 585442$$

with $e_0 = 22$, $e_1 = 89$, $e_2 = 13$, $e_3 = 23$

$$A_0(26611) + A_1(6578) + A_2(45034) + A_3(25454) = 1 \bmod 585442$$

yielding a minimum positive set: $A_0 = 17$, $A_1 = 11$, $A_2 = 7$, $A_3 = 13$.

5.8.5 Statistics Gathering

The controller will accumulate tallies of operating activity and error statistics to facilitate the diagnosis of subsystem problems before they become subsystem failures. Refer to Section 3.15 for a list of tallies maintained by the controller.

The EUS shall be able to access the statistical tables with a Read Control Register command, Section 3.15, and additionally will undoubtedly find it necessary to accumulate statistics of its own in order to evaluate subsystem performance.

5.8.5.1 Errors Logged on a Controller Basis

There are eleven counters which are maintained in the controller main memory. The contents of these counters are available to the external user system by proper usage of the Read Controller Main Memory command. Also, the EUS may load these counters with any count by using the Write Controller Main Memory command. The location of these counters will be specified during the design implementation.

5.8.5.2 PSI Parity Error Counter

This one-byte counter records the number of activities containing an error while transferring information across the PSI from PSIA to LA. An activity includes either an IDCW transfer or a record transfer. There are four of these counters, one for each possible PSI.

5.8.5.3 OPI/PSI Counter

This one-byte counter records the number of times that the OPI line on the PSI is dropped as the result of unsuccessful communication of the LA with the PSIA. The failure may be in the LA (where it appears as a PSI - related fault), in the PSI cable, or in the IOM/PSIA.

There are four of these counters - one for each possible PSI.

5.8.5.4 OPI/IAI Counter

This one-byte counter records the number of times that the OPI line is dropped due to either IAI faults detected by the LA, or LA faults which appear as IAI faults.

There are two of these counters in the controller - one for each possible LA.

5.8.5.5 Error Interrupt Counter

This one-byte counter records the number of times that the MPC executed an error interrupt.

This is a single counter for the controller.

6. RELIABILITY AND MAINTAINABILITY

(Refer to the DSS181/DSS190 Subsystem EPS-1 (43A239851) Section 6 for Reliability and Maintainability information.)

7. GENERAL DESIGN REQUIREMENTS

(Refer to the DSS181/DSS190 Subsystem EPS-1 (43A239851) Section 7 for General Design Requirements.)

DSC181/DSC190 CONTROLLER
EPS 1

SIGN-OFF SHEET

PREPARED BY: E W Herron 6/9/71
E.W. Herron Date
Advanced Subsystem Design

Reviewed by: Ted Strout 6-18 71
F.D. Strout, Manager Date
Advanced Subsystem Design

Reviewed by: Gordon K. Williams 6/22/71
G.R. Williams, Manager Date
Systems Design Engineering

Reviewed by: T J Beatson 6/22/71
T.J. Beatson, Manager Date
Systems Software Design

Reviewed by: L I Wilkinson 12/2-/71
L.I. Wilkinson, Manager Date
Systems Engineering

Reviewed by: J.R. Guilford Nov. 18, 1971
J.R. Guilford, Manager Date
I/O Design Engineering

Reviewed by: R L Mynatt 10/29/71
R.L. Mynatt, Manager Date
645/MPC Design Engineering

Reviewed by: R L Ruth 11/19/71
R.L. Ruth, Manager Date
Computer Design Engineering

Reviewed by: C A Conover 6/22/71
C.A. Conover, Manager Date
Advanced Systems Engineering

Approved by: C W Dix 11/19/71
C.W. Dix Date
Director of Engineering

Reviewed by: G B Krekeler
G.B. Krekeler, Manager Date
Language & Data Mgmt. Sys.

Reviewed by: R F Marshall 6/23/71
R.F. Marshall, Manager Date
Memory & Circuit Engrg

Exchange freight route classification
Reviewed by: R F Stevens 11/16/71
R.F. Stevens, Manager Date
Operating Systems Engineering

Reviewed by: P F Straka 6/23/71
P.F. Straka, Manager Date
Systems Engrg Maintainability

Reviewed by:
P.G. Smee, Manager Date
Product Engineering

Reviewed by: J D Hann 6/23/71
J.D. Hann, Program Director
Series 6000

Reviewed by: Concurrence received via phone, E W Herron 11/16/71
G.W. Muller, Manager Date
Disc Engineering

Reviewed by:

Approved by: D K Lundberg 6/25/71
D.K. Lundberg, Associate Date
Director-Product Marketing

Becomes CPS required for Feature Development

CE 301-1 (10-70)

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

C68-90

TITLE:

Engineering Product Specification - 1
DSC181/DSC190 Controller

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REVISION RECORD

REVISION LETTER	DATE	PAGES AFFECTED	APPROVALS	AUTHORITY
A	Issued DEC 10 1971			

TABLE OF CONTENTS

1. GENERAL DESCRIPTION

This document specifies the controller requirements for the DSC181 and DSC190 Removable Media Disk Storage Controller. The basic elements of the controller are:

- MPC - Microprogrammed Peripheral Controller
- LA - Link Adapter
- CA - Controller Adapter
- Microprogram - Personalized control store firmware

1.1 INTRODUCTION

This Engineering Product Specification, Part 1, will describe in detail the interface presented to the external user's systems (EUS) by the DSC181/190 controller.

The controller comprises several pieces of hardware, however, the majority of this specification will treat it as a single box, since the external interface presented by the controller is the primary concern.

The controller is intended to satisfy a variety of needs. A subsystem may be configured in many different ways to meet data availability and throughput requirements. Refer to the DSS181/190 Subsystem EPS-1, 43A239851 for subsystem characteristics and capability.

Because the subsystem uses a microprogrammed control unit as part of the controller, the versatility and especially the adaptability to new requirements are significantly increased.

A major feature of the subsystem is the capability of using multiple sector lengths (of 288 or 1440 bytes or one sector per track) and other formats including sector lengths of the IBM format. The specific format implemented is a firmware option of the controller. This EPS-1 defines the initial format of the basic subsystem and includes the capabilities which are offered as options.

This EPS-1 covers the ultimate controller requirements for the DSS181 and DSS190. Not all of the features will be implemented initially on the DSS181. Refer to DSS181/190 Subsystem EPS-1, Section 1.8 for implementation phasing.

1.2 APPLICABLE DOCUMENTS

EPS-1	- GECOS File System	43A233715
CPB 1518C	GE-600 Line Comprehensive Operating Supervisor(GECOS-III)	
EPS-1	- Microprogrammed Peripheral Controller (MPC)	43A177875
EPS-1	- PSI Link Adapter (LA)	43A177879
Purchase Specification	- DCT170 Disk Pack	M50EB00747
EPS-1	- General Design Requirements Specification for GE-655 and GE-355	43A177851
EPS-1	- DATANET-355	43A219609
EPS-1	- GE-655 IOM Input/Output Multiplexer	43A219604
EPS-1	- DSS181/DSS190 Subsystem	43A239851
EPS-1	- Peripheral Subsystem Interface (PSI)	43A177874
EPS-1	- Mass Storage Device Level Interface (DLI) BL0026, FSP-IF-300	
EPS-1	- 655 IOM Peripheral Subsystem Interface Adapter	43A177880
MPC	Microprogramming Reference Manual	MPC-1
EPS-1	- DSC175/180 Controller	43A177863
EPS-1	- DSU181 Disk Storage Unit	59A301822

AREA OBJECTIVES for NPL Microprogrammed Peripheral Controller (MPC) Document BL0021 Rev. 0 Draft 1

NPL Disk Subsystem Functional Specification NPL-FSP-MS-000, Order Number BL0004

Purchase Specification DSU190	59A301821
Common MPC Maintainability Specification	43A237500

NDM400 Mass Storage Device BL0034

NPL Peripheral Subsystem Interface Functional Specification FSP-IF-100. Order Number BL0000

NPL Mass Storage Subsystem Area Objectives, Number AOB-MS-000, Order Number BL003

EPS-1 DATANET 355/Mass Storage Link 43A232270

EPS-1 355 Computer Peripheral Subsystem Interface Channel (PSIC) 43A999997

1.3 DEFINITIONS

The following definitions are provided to be consistent with related documents.

EUS External User System. EUS refers to any 355 or 6000 line computer system with its associated peripheral subsystem interface (PSI).

PSI Peripheral Subsystem Interface. Refer to the PSI EPS-1, 43A177874.

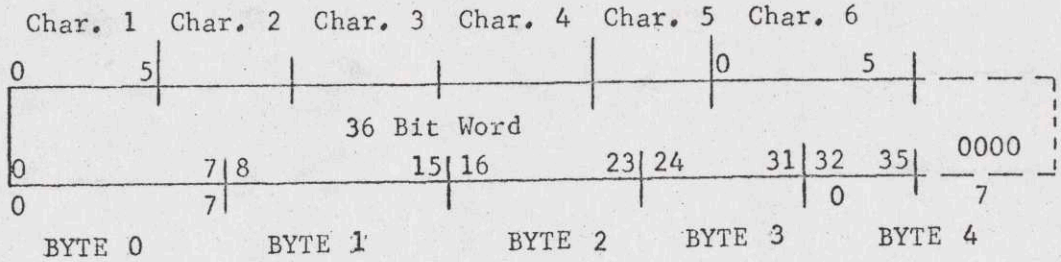
CHARACTER Six bits of information (as opposed to eight or nine bits)

WORD Six characters, 36 bits, referring to 6000 system word size (2 words contain 9 bytes)

BYTE Eight bits of information

DATA Data formats are described as either 6000 words (36 bits) or bytes (8 bits). Odd MOD words are described as four and 1/2 bytes with the addition of four zeros to match the byte PSI interface. The relationship of bits, characters, bytes and words is shown below.

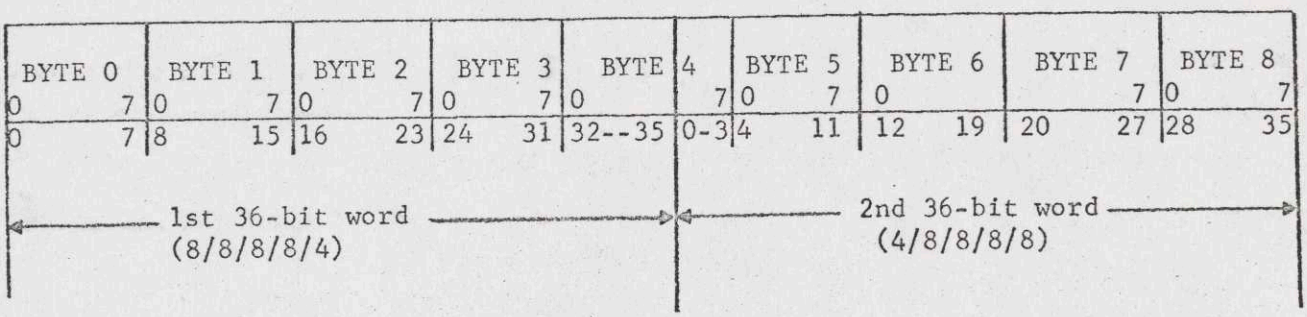
6 Bit Character



8 Bit Byte

Binary Data Transfer

The bytes are mapped into a pair of 36-bit words as shown below:



These are nine bytes per 72 bit word pair. The first 36-bit word is referred to as the 8/8/8/8/4 word, the second 36-bit word as the 4/8/8/8/8 word.

The bytes are transferred across the interface in the order Byte 0, Byte 1 . . . . . , Byte 8.

ASCII Data Transfer

The bytes are arranged in a 36-bit word as shown below:

0	BYTE 0		0	BYTE 1		0	BYTE 2		0	BYTE 3	
	0	7		0	7		0	7		0	7
0	1	8	9	10	17	18	19	26	27	28	35

Bits 0, 9, 18 and 27 of the 36-bit word do not appear on the PSI. They are not sent to the MPC during a write, and forced to 0 for storage in memory during a read.

LA Link Adapter

CA Controller Adapter

ITR Isolation Test Routines

MPC Microprogrammed Peripheral Controller

DSC Disk Storage Controller

IOM Input/Output Multiplexer

DLI Device Level Interface

IAI Internal Adapter Interface

DSU Disk Storage Unit

SECTOR Physical description of data between gaps. Random addressable.

RECORD Data specified by one command, that is, part of sector or several sectors.

DEVICES Disk Storage Unit

DSS Disk Storage Subsystem

64 WORD SECTOR 288 bytes, 384 characters

320 WORD SECTOR 1440 bytes, 1920 characters

CONTROLLER MPC, LA, CA

COMMAND Operational instructions from EUS (read, write, etc.)

CHANNEL EUS connection path to the subsystem

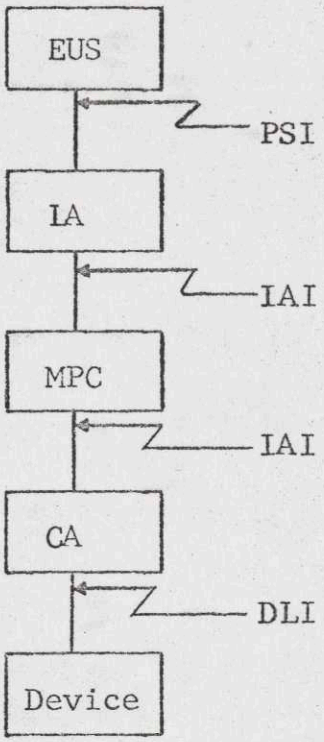
LOGICAL CHANNEL IOM multiplexed connection path for a transaction, that is, a channel program (IDCW, DCW's)

RPS Rotational Position Sensing

EDAC Error Detection and Correction

LOS Level of Simultaneity

TOLTS Total On-Line Testing System



External User System

Peripheral Subsystem Interface

Link Adapter

Internal Adapter Interface

Microprogrammed Peripheral Controller

Internal Adapter Interface

Controller Adapter

Device Level Interface

Device

2. FUNCTIONAL DESCRIPTION

The DSC181/190 controller provides the control for performing data formatting, positioner control, data path switching, file protection, head switching and associated functions required to reliably read and write data. Access to the controller by the 6000 system or DATANET 355 is via the Peripheral Subsystem Interface (PSI). Access to the drives is via the Device Level Interface (DLI). Interface connections to the system and device is shown in Figure 2.

Refer to the DSS181/DSS190 Subsystem EPS-1, 43A239851 for subsystem functionality.

2.1 SUMMARY OF CONTROLLER FUNCTIONS (See Section 1.3 for Abbreviation Explanations)

- Provide a variety of hardware configurations for single channel and dual cross-barred channel operations.
- Provide dual simultaneous transfer from two devices.
- Issue the necessary DSU181 commands to write the headers, sector gaps and data areas required to format the M4180 disk packs in fixed sector lengths of 288, 1440 bytes or one sector per track.
- Perform conversion of the continuous binary addresses received from the EUS to the non-continuous cylinder-head-sector addresses of the subsystem devices.
- Perform file protection by limiting the data sectors available to the processing system following each instruction. The sectors available-per-seek-instruction shall be specified by the processing system and can vary from 1 to 4096 (an entire cylinder or multiple cylinders).

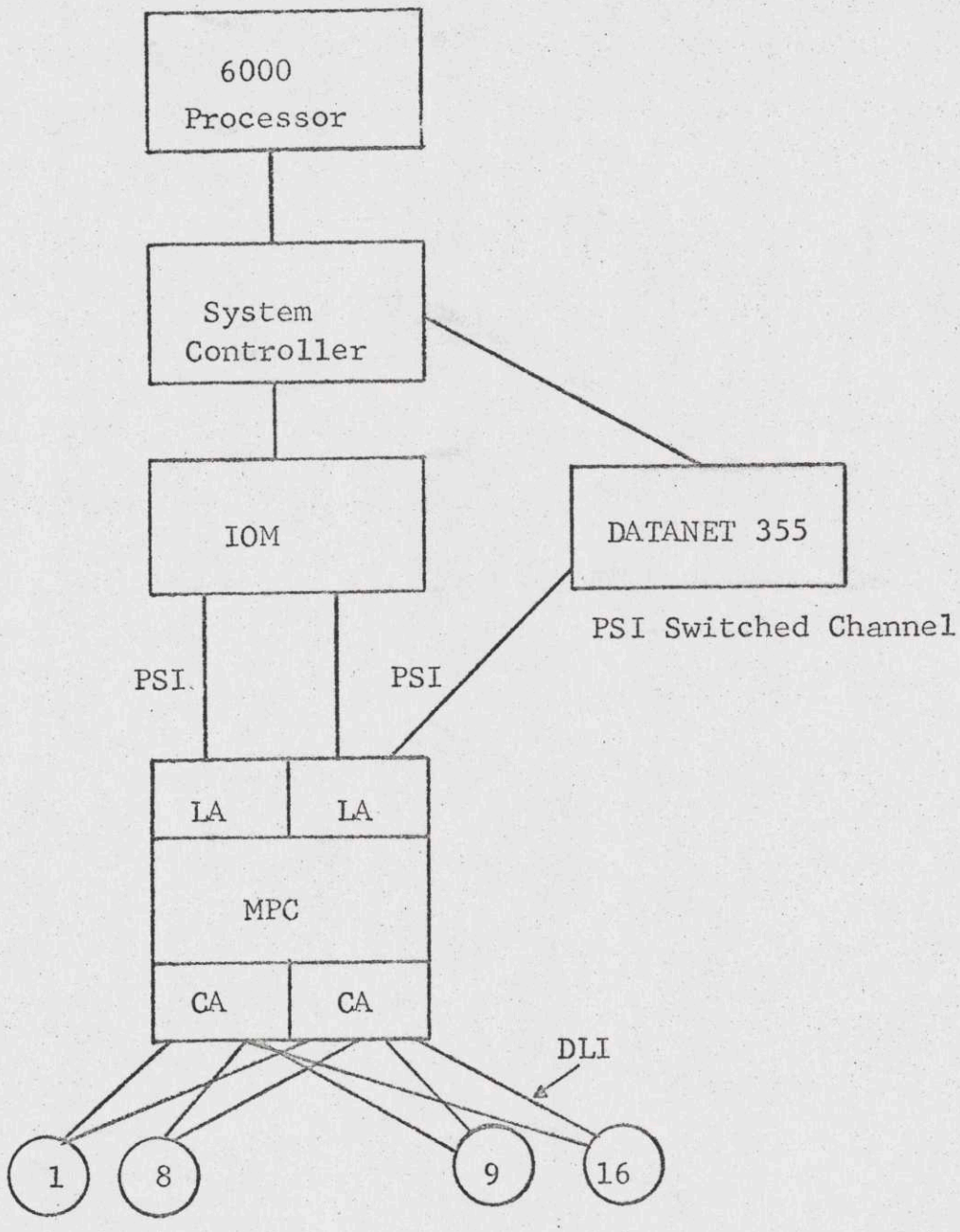


Figure 2. 6000 System with Dual Channel and Mass Store Link

- Issue the necessary DSU190 commands to write the headers, sector gaps and data areas as required to format the DSU190 disk packs in fixed sector length of 288, 1440 bytes or one sector per track.

- Perform status formatting necessary to reflect subsystem status to the EUS.

- Read and write multiple sequential data sectors as specified by the EUS processing system.

- Provide the means for the EUS to load the controller with new parameters to reconfigure the operating interface of the subsystem or a single device.

- Provide an interface to the Isolation Test routines resident in the controller for test and diagnostics aid in locating malfunctions. The interface for command and response communication between the controller firmware and the Isolation Test routines is defined in EPS-1, 43A237500.

- Provide maximum possible protection against accidental alteration of command execution routines which may be stored in the controller memory.

- For on-line maintenance purposes provide on command the detailed status information as generated by the subsystem, and retained either in core or hardware registers.

- Provide the ability to accept one additional command for each device after a given seek has been issued. See Section 5.6.4 for a discussion on command stacking. Proper use of this feature can increase throughput but improper use will decrease subsystem throughput.

- The communication interface between the controller and the EUS is defined to be the Peripheral Subsystem Interface (PSI).

- Storage of the address and control information associated with the last seek will be provided at the device level for all devices in the subsystem.

2.2 RECORD LAYOUT DSC181

Each device has a total of 203 cylinders. There are 203 tracks on each disk surface, and 20 heads per cylinder, for a total of 4060 tracks maximum. By convention, tracks on each disk surface are numbered from zero to 202, with 202 being the innermost track.

Cylinders are also numbered from zero to 202. Space allocation on the disk pack shall conform to the following:

- Cylinder 0 through 201 (4040 tracks); User Data, Systems Labels, Catalogs, Alternate Tracks, etc.
- Cylinder 202 (20 tracks); Must be reserved for T&D use only.
- The track format is in fixed sector lengths of 288, 1440 bytes and one sector per track.

2.3 RECORD LAYOUT DSS190

Each device has a total of 411 cylinders. There are 411 tracks on each disk surface, and 19 heads per cylinder for a total of 7809 tracks maximum. By convention, tracks on each disk surface are numbered from zero to 410, with 410 being the innermost track.

- Cylinders are also numbered from zero to 410. Space allocation on the disk pack shall conform to the following:
- Cylinder 0-409; User Data, Catalogs, Alternate Tracks, etc.
- Cylinder 410 (19 tracks); Must be reserved for T&D use only.

- The track format is in fixed sector lengths of 288, 1440 bytes and one sector per track.

2.4 STORAGE FORMATS

The DSS181 subsystem hardware includes the capability of fully implementing the IBM 2314A1 format. The CA is capable of formatting, reading and writing data fields as well as key fields. Data processing is accomplished on a field basis, with firmware supplied control identifying the fields and their contents. Thus the format of the track is the responsibility of the controller firmware.

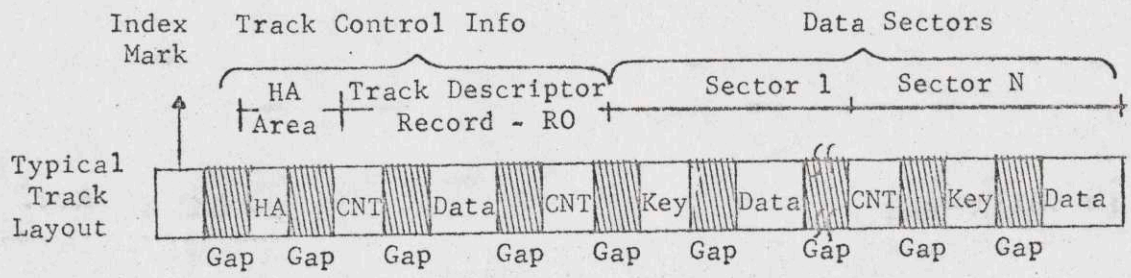
Initial operational requirement of the EUS is met by the implementation of fixed sector lengths with no key fields.

The above EUS requirements are met in the design of the controller microprogram and will not be constraints upon the hardware design. If the EUS requirements should change to different sector lengths, and/or the use of key fields, only the controller firmware would require change.

2.4.1 Basic Format (IBM 2314A1, reference only)

Track Layout:

A typical track layout is pictured below:



The track layout is characterized by the following summary:

a. Each track contains "Home Address" field, one per track.

b. Each track has one unique "Record Zero" sector. This sector may contain either count and data field, or count, key and data field. Normally, this sector is not used for User Data Storage. For the DSS181, the key field is not present and the data field is eight bytes long.

c. User Data Sectors may contain either count and data field, or count key and data field.

d. The count field of a sector is fixed in length (9 bytes).

e. The key field of the sector (if present) can vary in length from 1 byte to 255 bytes.

f. The data field of a sector can vary from 1 byte to 7294 bytes.

g. The length of the data field can be set to zero. If so, an End-of-File status condition is indicated when the field is read.

h. "Gaps" between fields, within a sector, are fixed in length. "Gaps" between sectors are variable and a function of the length of the key and data field.

i. Lengths of the fields of a sector are measured in bytes (8 bit multiples), as opposed to lengths being measured in words (36 bit multiples) or character (6 bit multiples).

j. A "sync byte" (the first byte in every field) identifies the type of field.

k. The last four bytes of every field are identified as:

Burst CK	Burst CK	ID Byte	Bit CNT

where:

Burst CK - Cyclic code bytes for error detection. The CA computes the two cyclic check bytes. The first check byte is the exclusive OR of all the even numbered bytes written in the sector. The second check byte is the exclusive OR of all the odd numbered bytes written in the sector.

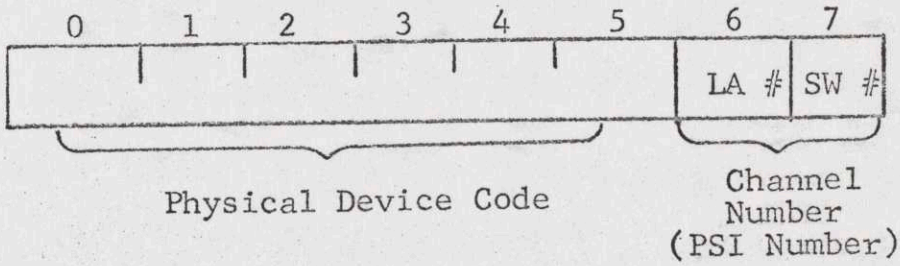
For a write operation, the two cyclic code bytes are added to the end of the field and written on the track.

On a read operation, the exclusive OR process is repeated until the cyclic code bytes at the end of the record are operated upon. If no error has occurred, the result is all 0's in the cyclic code check registers. The cyclic code check bytes are called burst bytes. The cyclic code check used has the following checking properties.

1. Detects all errors in which an odd number of bits are wrong.

2. Detects single bursts of error that are 16 bits or less in length.

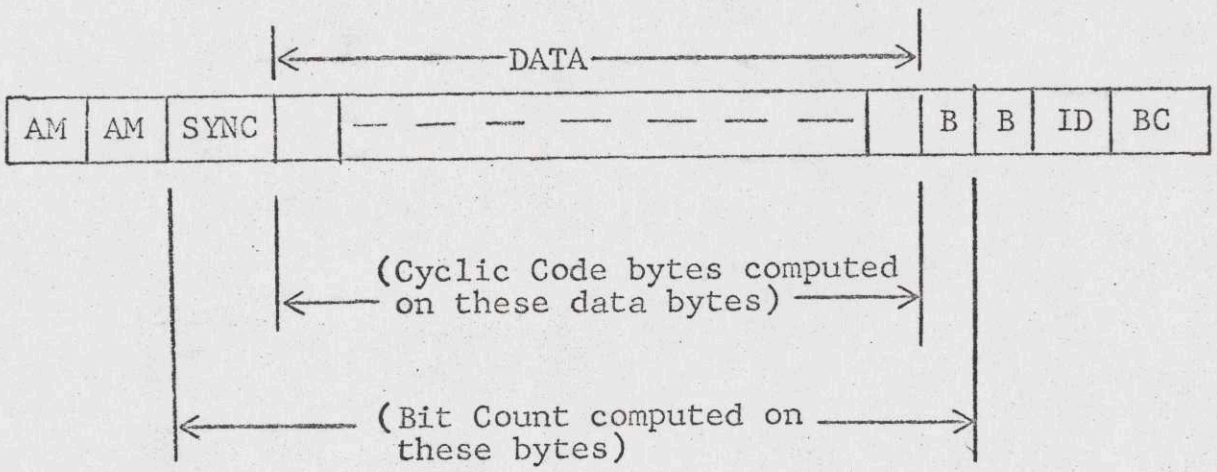
ID Byte = This byte identifies the physical device number and channel number of the device used when this byte was written on the track.



Bit CNT = Bit count check byte. This byte records, modulo 256, the number of one-bits written in the field in one's complement form. Functionally, this byte is included as another code checking byte. Failure to compare the bit CNT is the same as a cyclic check compare failure.

These last four bytes are not part of the data of a field and are not normally transmitted beyond the controller.

The above description of the last four bytes pertains to IBM 2314 Model A1 Subsystems. In earlier, Model 1, subsystems the ID byte and bit count byte are not included -- A field ends with the two burst check bytes. The four bytes described above will be written on the device in the manner of Model A1.



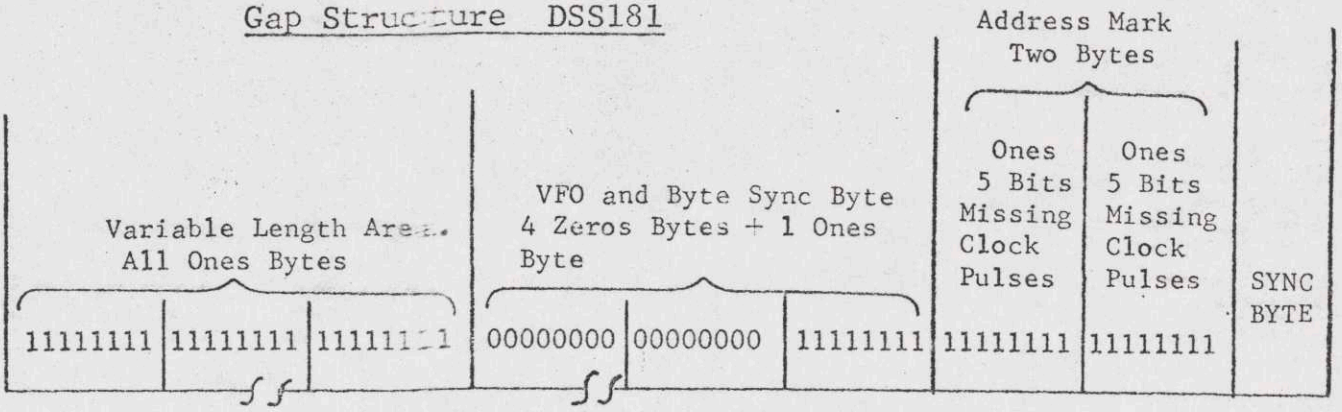
Field Structure

The fields discussed above exhibit the following structure.

In the above structure:

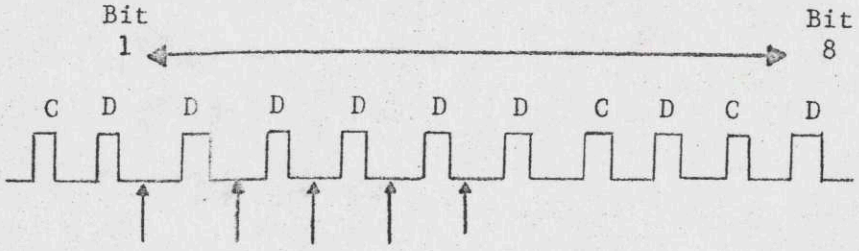
F = Flag Byte
CC = Cylinder Number in Binary
H = Head Number in Binary
R = Track Record Number in Binary
K = Key Field Length in Binary
DD = Data Field Length in Binary
GO = 43 Bytes if RO Data Length is 8
GO = 43 + .043 (DL) if RO Data Length > 8 Bytes
GN = 43 + .043 (KL + DL)
BB = Cyclic Burst Byte
IC = Indicator Byte
BC = Bit Count Byte

Gap Structure DSS181



Total gap length is 41 bytes between fields; 43 bytes between HA and RO count field; and 43 + .043 (DL + KL) between sectors. KL and DL are the lengths (in bytes) of the key and data fields of the preceding sector. Control firmware is responsible for calculation of the factor $\frac{K_L + DL}{23+65/256}$ during format operations. If KL = 0 and DL = 288 bytes, for example, then the gap length is 55 bytes.

The Address Mark is a special configuration of clock/data bits which indicate to the CA or device the beginning of a field.



Address Mark Byte. The arrows indicate missing clock bits.

C = Clock Bit D = Data Bit.

The Address Marks are the only areas on the track in which data bits are not separated by clock bits. This special condition, then, could not occur erroneously within a field. The CA or device hardware is charged with the responsibility of writing the AM at the beginning of each field, and detecting the AM at the beginning of each field on read operations.

2.4.2 Basic Subsystem 64 and 320 Word Format

The following paragraphs describe functions in terms of the CA and microprogram subsystem.

1. The subsystem shall be able to read and write disk packs in the general format described in paragraph 2.4.1, but for a fixed data length of 288 bytes, 1440 bytes and one sector per track.

2. The subsystem shall be able to read disk packs generated by the IBM 2314 Model 1 and Model A1 subsystems.

3. The subsystem shall be able to write sectors in the format of the IBM 2314 Model A1 subsystem only.

4. The subsystem will format an entire track of either 288 bytes, 1440 bytes or 7200 bytes, sectors upon receipt of a "Format Track" command from the EUS. The track shall conform to the IBM format and shall contain the following areas:

   One Home Address Area (HA)

   One Record Zero Sector (R0 count field plus a data field DL of 8 bytes; no key field)

   Eighteen Data Sectors (each with a count field plus a data field DL of 288 bytes; no key field), or

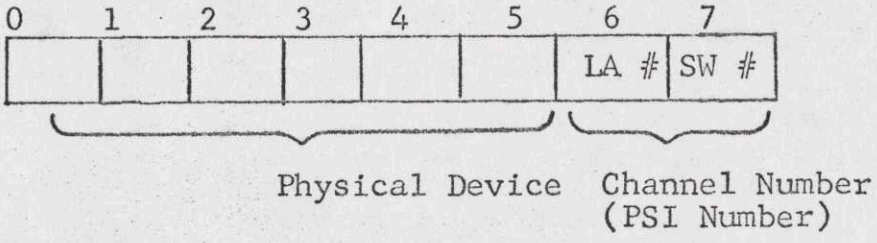
   Four Data Sectors of 1440 bytes, or

   One Data Sector per track (DSS181 - 7200 bytes and DSS190 - 12960 bytes)

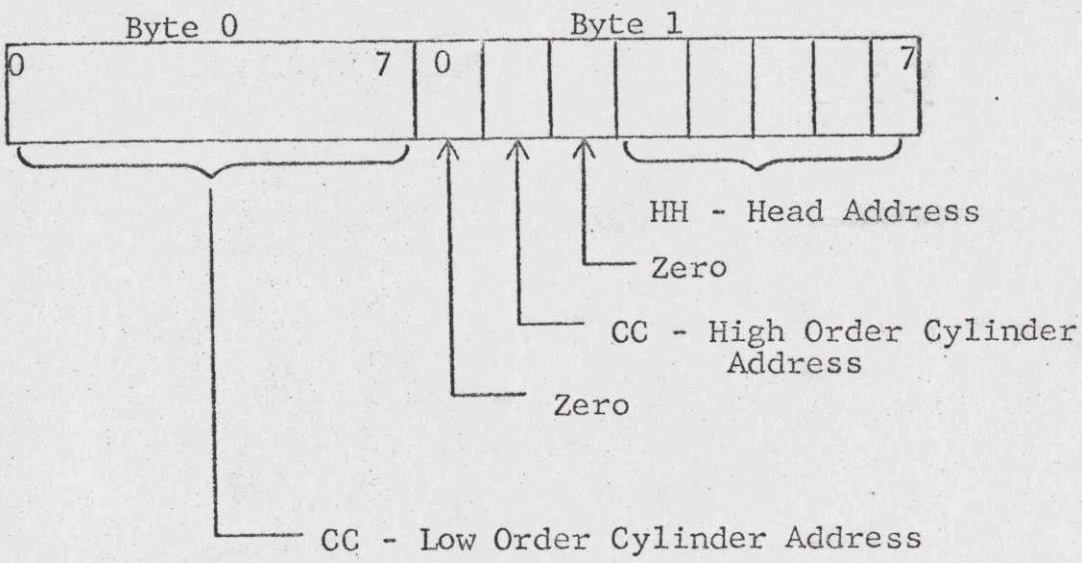
2.4.3 Basic Data Format

In the above structure:

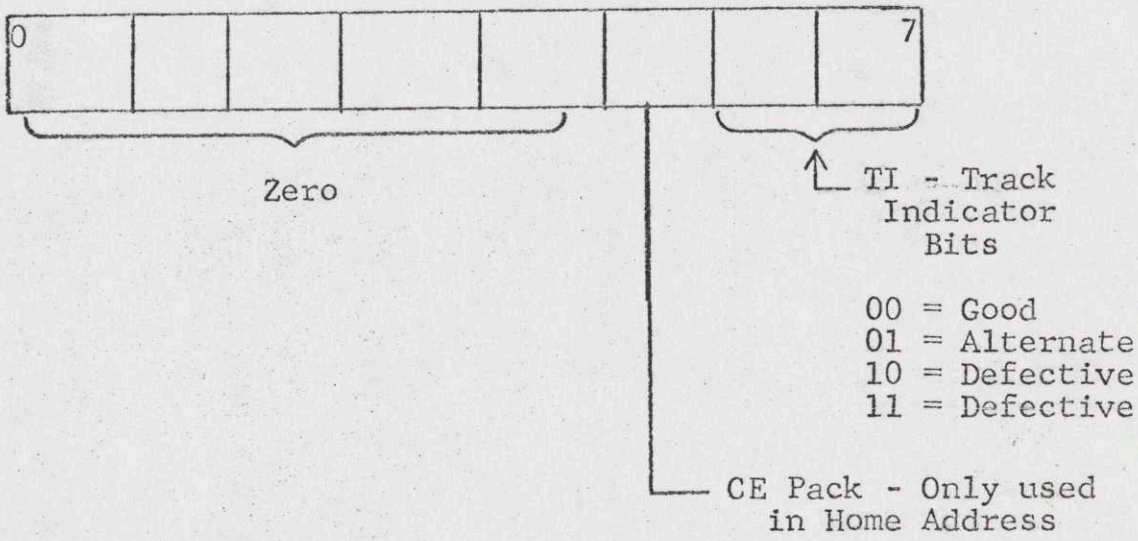
I = Index Mark
HA = Home Address
CNT = Count Field
FLAG = Flag Byte
CYL = Cylinder Number in Binary
HD = Head Number in Binary
REO# = (Record) Sector + Number in Binary
KL = Key Field Length
DL = Data Length in Binary
ID = Identification Byte
Cyclic Code = 7 byte EDAC Code
PA = Physical Address
ID Byte = This byte identifies the physical device number and channel numbers of the device used when this byte was written on the track.



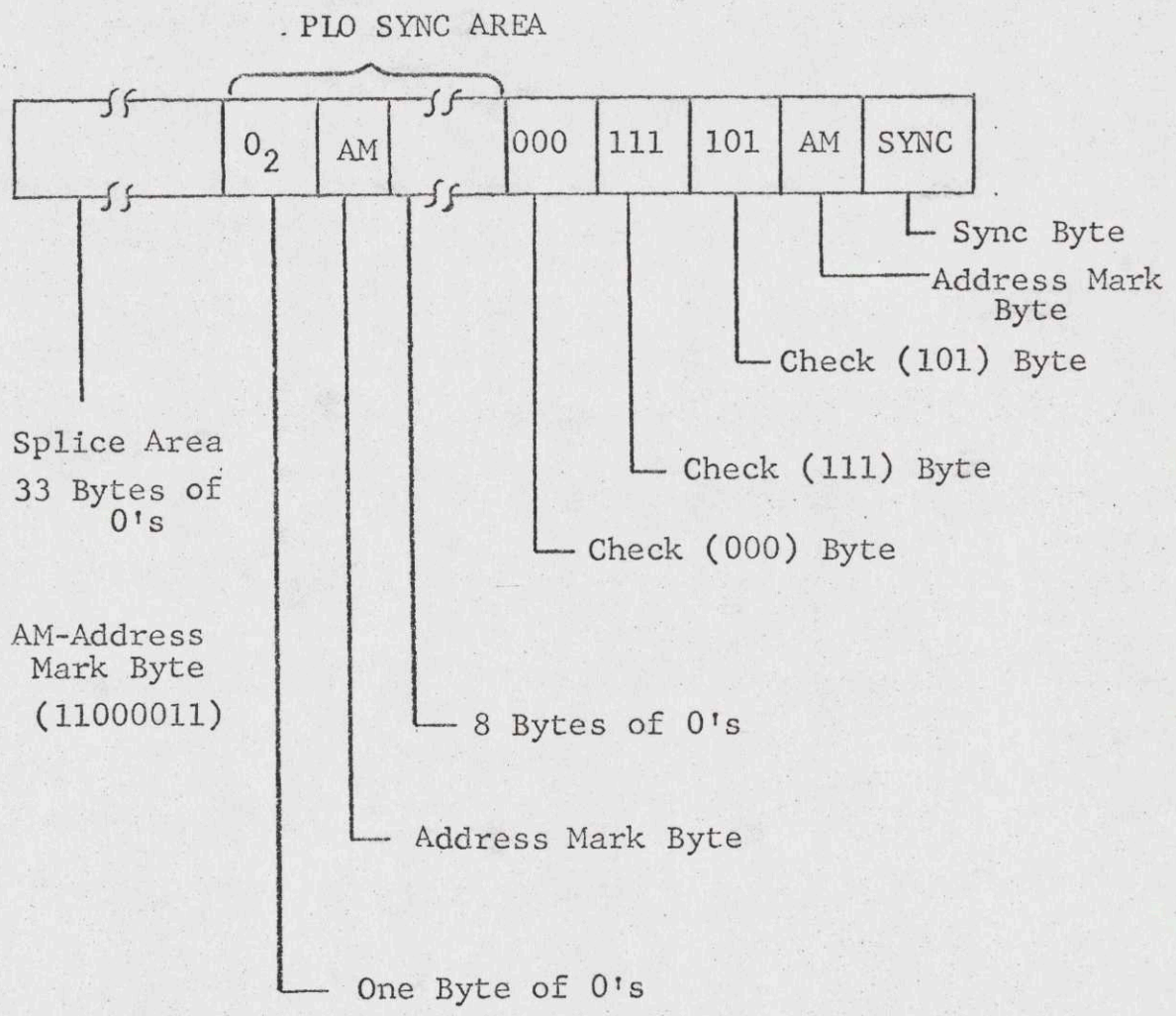
Physical Address



Flag Byte



GAP Format DSS190:



3. COMMAND DESCRIPTION

The controller will provide the following command set for use by the External User Systems. The last column indicates those commands which will be rejected with invalid device code based on the incorrect use of the device code.

Table of commands valid for device/controller

COMMANDS	BIT CODE	OCTAL CODE	LEGAL DEVICE CODE
Seek	011 100	34	D
Special Seek (T&D)	011 110	36	D
Preseek	011 111	37	D
Restore	100 010	42	D
Read	010 101	25	D
Read ASCII	010 011	23	D
Write	011 001	31	D
Write ASCII	011 010	32	D
Write and Compare	011 011	33	D
Read Nonstandard Size	000 100	04	D
Read Track Header	010 111	27	D
Format Track	001 111	17	D
Request Status	000 000	00	E
Reset Status	100 000	40	E
Read Control Register	010 110	26	E
Write Control Register	001 110	16	D
Read Status Register	010 010	22	E
Read EDAC Register	010 001	21	D
Release	111 110	76	D
Reserve Device	111 111	77	D
Set Standby	111 010	72	D
Bootload CS	001 000	10	C
ITR Boot	001 001	11	C
Execute Device Command (DLI)	011 000	30	D

Special Controller Commands - see Section 3.21

D = Device Only
E = Either
C = Controller Only

COMMAND (BIT) STRUCTURE

High \ Low	000	001	010	011	100	101	110	111
000	Req. Status				Read Non-Standard Sector Size			
001	Boot C.S.	ITR BOOT					WCR Write Control Register	Format
010		Read EDAC RER	RSR	Read ASCII		Read	RCR	Read Header
011	Execute Device	Write	Write ASCII	Write & Compare	Seek		Special Seek	Pre-Seek
100	Reset Status		Re-store					
101								
110								
111			Set Standby				Release	Reserve Device

SPECIAL CONTROLLER COMMAND
(BIT)STRUCTURE

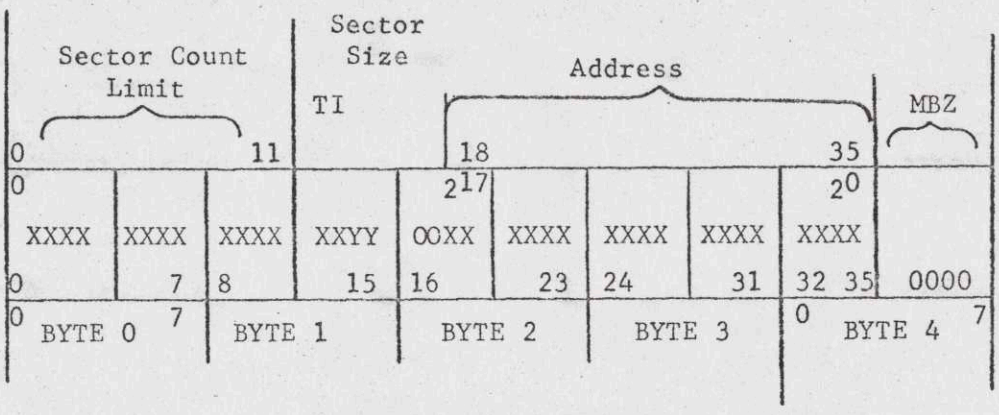
(Refer Section 3.21)

High \ Low	000	001	010	011	100	101	110	111
000	Suspend Controller		Read Controller Main ASCII		Read Lock Byte		Initiate Read Data	
001	Write Control Store		Write Controller Main ASCII		Write Lock Byte		Initiate Write Data	
010	Release Controller		Read Controller Main Binary					
011	Execute Control Store		Write Controller Main Binary		Conditional Write Lock Byte			
100								
101								
110								
111								

3.1 SEEK

During the I/O command sequence, when this instruction is received, the controller will check the IDCW. If an error condition is detected, the controller will terminate the instruction and report appropriate status. The seek command will perform an implicit reservation of the addressed device to the logical channel until the data transfer command that follows the seek is terminated, if there is no data transfer command following the seek, over the same logical channel the controller will release the device after positioning is complete. If the device code is valid the controller firmware will issue a request to the EUS for five seek address byres, (6 characters). If exactly five address bytes with last four bits equal zero are successfully received (no transfer timing or transmission parity alert), the controller firmware will save the sector count limit and convert the binary address to the cylinder, head, and sector format. Provided the address is valid, the controller will select the device and attempt to reserve the device to the issuing channel. If successful, it will then interrogate the device status. If an exception condition exists, the instruction will be terminated with an Attention or Device Busy status. If the device is ready, the controller will issue the required commands to the CA to perform the specified seek. The controller will at this time, terminate the instruction and report one of the status conditions to the EUS.

The five control bytes shall serve to define the specific seek operation to be accomplished as follows when fixed sector binary addressing is used.



Bits 0-11: These bits shall define the binary sector count with the file protection option. Least significant bit is 2^0 in bit position 11. Zero is a maximum count of 4096.

Bits 12-13: These two bits shall be the track indicator bits. (See Section 3.11 format track command.)

Bits 14-15: These bits shall be the sector size indicators:

YY= 00 64 Word, 288 bytes or one record per track

YY= 01 320 Word, 1440 bytes or one record per track

YY= 10 64 Word Seek Algorithm, one sector per track (must be used to format a one sector track on a pack where the rest of the sectors are of the 64 word format)

YY= 11 320 Word Seek Algorithm, one sector per track (must be used to format a one sector track on a pack where the rest of the sectors are of the 320 word format)

When addressing one sector per track with either YY = 10 or YY = 11 the binary address must decode to sector zero (first data sector). If the binary address does not decode to sector zero and the track is formatted with one sector per track (7200 or 12960 bytes) then MPC Data Alert sector size error will be returned.

Bits 18-35: These bits shall define the specific binary sector address to be located on the addressed device. Least significant bit is 2^0 (2^3 bit in byte 5), bit position 35.

Data Alert, Invalid Seek Address status shall result if other than five bytes are received or the last four bits of byte 5 are not zeros, during the instruction execution.

If a seek (or preseek) instruction decodes to any sector on track 202 for the DSS181 (or track 410 for the DSS190), the T&D tracks, it will be rejected with "Data Alert, Invalid Seek Address" status.

Seek instructions or special seek instructions following a restore that are received while the file is positioning will be accepted and will be executed after the file has completed the positioning operation.

The controller will terminate the Channel Busy state with appropriate termination status as shown in Table 4.

Off-Line Execution: Upon completion of the seek instruction command sequence (indicated by the reflection of Channel Ready status to the EUS upon termination of the busy state), the controller will have initiated the seek operation. The device to which the seek instruction is addressed will remain reserved to the logical channel that issued the seek until data transfer is complete or positioning is complete if no data transfer command follows. The device will be released by a release instruction or upon execution of a subsequent data transfer instruction. (Refer to Section 3.19, Device Reserve.) In multiple device subsystems, all devices may be in simultaneous off-line positioning operations. The controller will store the control information and address for each seek operation, so that it will not be necessary for the EUS to reissue a seek instruction prior to a data transfer command in the same channel program.

3.2 SPECIAL SEEK

Special seek is provided for Test and Diagnostic use; however, there are no restrictions within the controller on the use of this instruction by other EUS activities. It is identical in use to the seek instruction (see Section 3.1) except that the continuous binary address must reference a sector or cylinder 202 for DSS181; (410 for DSS190), the T&D cylinder.

Thus, if this instruction is addressed to a sector on any cylinder other than the T&D cylinder, it will be rejected with "Data Alert, Invalid Seek Address."

Upon termination of the Special Seek instruction, appropriate termination status and substatus will be reflected to the EUS: (Refer to Table 4.)

3.3 PRESEEK

The Preseek instruction will be executed as though the EUS had issued a Seek instruction except the preseek may not be followed by a data transfer command. In nearly all other respects, it will be treated the same as the Seek instruction. Except, a "Seek Incomplete" condition in the device will cause the controller to automatically restore the device but no retries will be attempted. The controller will not issue a special interrupt to the EUS channel. (See Section 5.6 for considerations on the reporting of special interrupts to the EUS.)

The other difference in the preseek instruction is that it must be issued only to devices which are not reserved to the given EUS channel. If a preseek instruction is issued to a device which is already reserved to the given channel, the controller will reject the instruction with "Instruction Rejected, Invalid Instruction Sequence."

Since preseek may not be followed by a data transfer command, the EUS must issue a Seek or Special Seek instruction prior to any device data transfer instructions. It is possible that, before the given channel issues the seek, an alternate channel connected to the device may issue an instruction that reserves the device to the alternate channel. If this should happen, the original (CA channel and thus the EUS) channel will not be notified that the preseek operation is nullified.

Upon termination of the preseek instruction, appropriate termination status and substatus will be reflected to the EUS: (Refer to Table 4.)

3.4 RESTORE

When track reference is lost due to machine error or a seek incomplete occurs, recalibrate must be issued to the device to return the access mechanism of the selected device to cylinder zero to re-establish the seek reference point. The controller will automatically recalibrate the device when there has been a seek incomplete.

Instruction Execution During Busy State:

Provided that the instruction was accepted (indicated by the reflection of Channel Busy Status to the EUS), the controller will attempt to reserve the device and initiate the specified restore operation.

If the restore instruction is received when the device is busy positioning, but not reserved to an alternate channel, it will be accepted and the channel will remain busy until the physical restore operation can be initiated. At this time, the instruction will be terminated with the appropriate status and the device released.

Off-Line Execution:

The Restore instruction results in the resetting of a seek incomplete and the recalibration of the access mechanism to cylinder zero.

The Restore must be followed by a Seek or Special Seek instruction before any data transfer to or from the device can occur. The Seek may be sent immediately upon receiving the channel ready status from the Restore termination. Refer to Table 4 for status returns supplied at command termination.

3.5 READ

Instruction Execution During Busy State:

Upon acceptance of the Read instruction and completion of the I/O command sequence, the controller will check to insure that the device code is valid, and the device has been reserved to the logical channel by a previous seek. The controller will then set up for the read operation.

If the device has completed the positioning operation from the previous seek instruction, the controller will initiate the data transfer. If the device has not completed the positioning of the previous seek instruction, the controller will stack the command and wait for an interrupt from the device. Upon receiving the interrupt, the controller will interrogate the device to determine that the device actuator is on cylinder. If the device is on cylinder with no errors, the controller will initiate a search for the addressed sector, and when it is found will initiate the data transfer.

Data will be read from the file, and transmitted to the EUS. The data transfer from the device will continue until one of the following occurs:

- An error condition is detected
- Sector count limit has been reached
- Terminate out signal is received from the EUS

If, at any time during the execution of a read instruction, a Terminate-Out signal is received from the EUS, data transfer to the EUS shall

terminate immediately. However, the controller will read and check the entire sector, thus the terminate status will be that for the last sector or partial sector transmitted.

Refer to Table 4 for status returns supplied at command termination.

3.5.1 Read ASCII

The execution of this command will be similar to the Read command with the exception that the controller will send a service code to the PSIA indicating ASCII mode and the PSIA will place four 8-bit bytes in each word. (Refer PSIA EPS-1). Refer to Table 4 for status returns supplied at command termination.

3.6 WRITE

Execution of this instruction is similar to the Read instruction, except that data is transferred from the EUS to the subsystem.

Instruction Execution During Busy State:

Upon acceptance of the Write instruction (reflection of Channel Busy status), and completion of the I/O command sequence, the controller will check that the device code is valid and that the device was previously reserved by a seek command through the same logical channel.

If the previous seek operation is not complete, the controller will wait for an interrupt from the device. Upon receiving the interrupt, the controller will interrogate the device to verify that the device is on cylinder. If the device is on cylinder and no error conditions exist, the controller will initiate data transfer from the EUS.

The data transfer to the device will continue until one of the following occurs:

- An error condition is detected.
- The sector count limit has been reached.
- Terminate-Out signal is received from the EUS.

A terminate out signal will terminate the data transfer at the EUS interface. The controller will continue to transfer data to the device until all the data received from the EUS prior to the TMO is recorded. When a partial sector is received from the EUS as a result of a Terminate Out signal, the remainder of the data sector shall be filled with zeros.

Refer to Table 4 for status returns supplied at command termination.

3.6.1 Write ASCII

The execution of this command will be the same as the write command with the exception that the controller will send a service code to the PSIA indicating ASCII mode and the PSIA will take four 8-bit bytes from each word (refer PSIA EPS-1). Refer to Table 4 for status returns supplied at command termination.

3.7 WRITE AND COMPARE

The execution of the write portion of this command shall be identical to the Write instruction. After the writing takes place at the addressed device, the controller will verify the write by moving the list pointer in the IOM back to the IDCW and re-transferring the data records (as in normal retry) to the controller from the EUS and reading the just written data records from the disk, and comparing the data received.

If at any time during the execution of the compare portion of the Write and Compare command a Terminate Out signal is received from the EUS data transfer from the EUS shall terminate.

The compare operation will be performed on complete sectors. If the data received from the EUS is not a multiple of a complete sector, the controller will zero fill and compare the data for the remainder of the sector. If the controller detects an error when reading the required sectors from the device, this status will be reflected regardless of the result of the compare operation. (Refer to Table 4 for status.)

3.8 READ NONSTANDARD SIZE SECTOR*

The Read Nonstandard command will be used to obtain all the fields on a track including count, key and data fields. The format of count fields, data fields, gaps, sync bytes, address marks and error detection codes must be the same as either the DSS181 or DSS190.

Instruction Execution During Busy State:

If the instruction is acceptable, the subsystem shall revert to the Channel Busy status.

Using the cylinder and head address from the preceding seek command, the controller will read the entire track starting at index mark and transmit all the information bytes to the EUS. (Note that this includes Home Address and Record Zero as well as all count, key and data records, but does not include gaps, sync bytes, address marks and error detection codes.) Data will be transferred to the EUS starting with the flag byte of the Home Address, as continuous data bytes until termination.

*Not Available on initial DSS181

The Read Nonstandard size sector command shall read only one track each time the command is issued.

The operation will continue until one of the following conditions is met:

- An error condition is detected.
- The sector count limit has been reached.
- A Terminate Out signal is received.

If an error condition is detected during a Read Nonstandard command the controller will terminate the instruction, send a terminate interrupt to the EUS and reflect appropriate status. If at any time during the transfer of the data, a Terminate Out signal is received from the EUS, data transfer shall terminate immediately. However, the subsystem will continue to read the remainder of the field. Thus, the status will be reflected for the last field read.

The controller will bypass the checking of the TI bits on the track. This eliminates the End-of-File status returns.

If the requested track cannot be read, the controller will not send any data to the EUS and will terminate the EUS channel with Data Alert, Header Verification Error. Refer to Table 4 for status returns supplied at command termination.

3.9 READ TRACK HEADER

When the subsystem initiates the Read Track Header instruction, the contents of the home address, and record zero count and data fields are transmitted to the EUS.

Instruction Execution During Busy State:

Upon acceptance (reflection of Channel Busy) of the Read Track Header instruction, the controller will verify the device code, and provided that a seek has been issued to the device through the same logical channel, the controller will execute the instruction.

The EUS sector number (as determined from the previous seek command) is used only to position the controller on the required track, as though the previous seek were to home address of the desired track. Head switching shall not occur on a Read Track Header instruction.

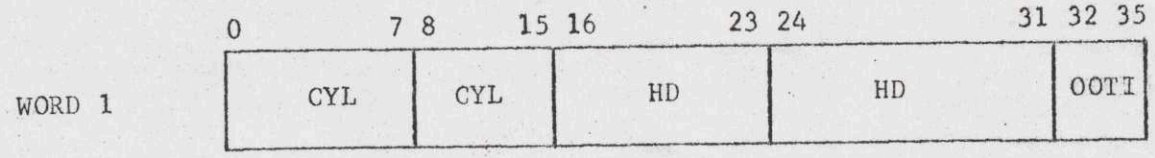
The byte oriented data maintained in the HA and R0 count and data field, will be read into the controller, before transmission of the data to the EUS is begun as a single block of data. The three fields will be sent to the EUS in the same five word format as that used for the Format Track instruction, except for one, bit 33 (Z bit) and the check character in word three bits (18-23). The "Z" bit position will always be returned as zero. The check character will not be computed and the controller will return zeros in the check character byte of word three bits (18-23). The format of the data sent to the EUS is shown below.

The amount of data transferred to the EUS will be 22 bytes, or less if the controller receives a Terminate-Out signal prior to the 22 bytes being transferred. Note that there is no conversion of the R0 data before it is sent to the EUS. The cylinder and head data in word one and two indicates the particular track on which the operation is being performed. If the CCHH in the home address does not agree with the CCHH computed from the Seek Address, the data will be sent to the EUS and the operation will be terminated with "Data Alert, Header Verification Error."

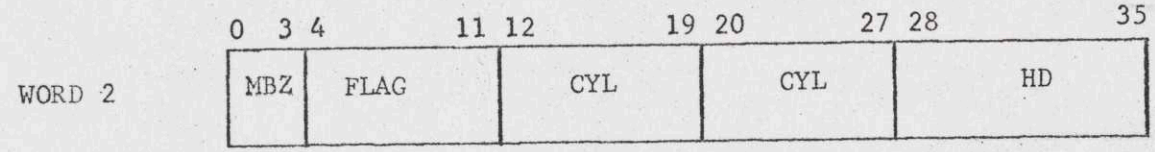
In the event an error condition is detected during a Read Track Header operation, the controller will terminate the instruction, send a terminate to the EUS, and reflect appropriate status.

If at any time during the execution of a Read Track Header instruction, a terminate out signal is received from the EUS, data transfer will terminate immediately. However, the subsystem will have read and checked the entire header so that appropriate status will be reflected. Refer to Table 4 for status returns supplied at command termination.

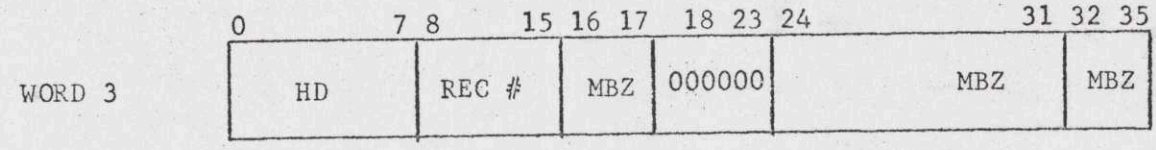
HA Home Address



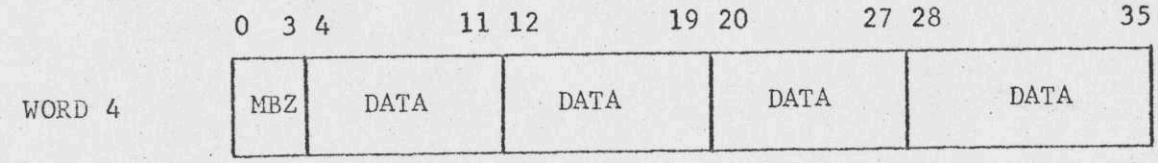
R0 COUNT FIELD



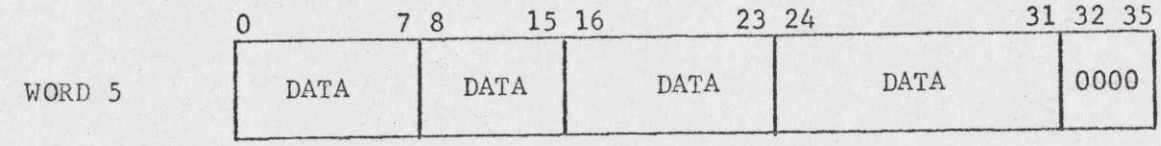
R0 COUNT FIELD



R0 DATA FIELD



R0 DATA FIELD



3.10 FORMAT TRACK

The Format Track instruction provides the means to format a complete track as a good, defective or alternate track. This instruction results in all headers, address marks, gaps and data fields being recorded on a given track, beginning at the Index Mark. (See Section 2.4.1 and 2.4.3 for a description of the track format.) The specific track is defined by the last Seek (or Special Seek) instruction sent to the device. The Seek instruction must immediately precede the Format instruction in the same DCW list, within the same channel program. Otherwise, the Format instruction will be rejected with "Instruction Rejected, Invalid Instruction Sequence."

Certain data provided by the EUS in the Seek and Format instruction data fields will be recorded on the track.

Except for Record Zero, the controller will write zeros in the data fields of all sectors on the track. The TI (Track Indicator) bits from the preceding Seek instruction will be written in the flag byte for the Home Address and the count fields of all records on the track, except Record Zero.

The TI bits will have the following meanings:

- 00 - Primary Track-Good
- 01 - Alternate Track-Good
- 10 - Defective Track - Alternate Assigned
- 11 - Defective Track - No Alternate Assigned

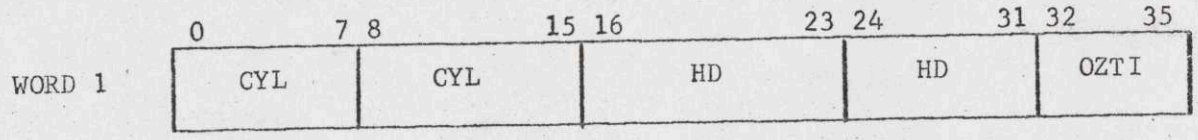
Instruction Execution During the Busy State:

The controller will first determine if the instruction itself can be processed by verifying the device status is good and that the Format instruction to the device was immediately preceded by a Seek instruction (or Special Seek, if the T&D cylinder is to be used). If the operation cannot be continued, the controller will terminate with the appropriate status.

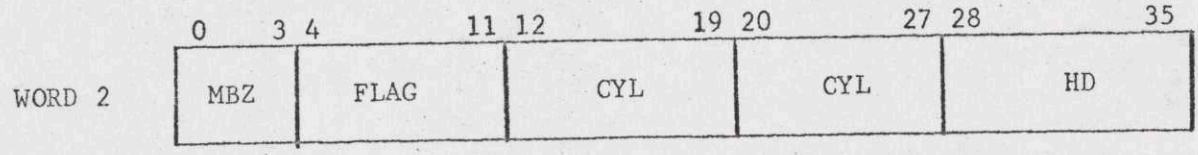
If the operation can be continued, the controller will always request five, 36-bit words (22 1/2 bytes) of data. If exactly 22 1/2 bytes are not received, the controller will terminate the instruction with "Instruction Rejected, Invalid Instruction Sequence."

The format of the data will be as follows:

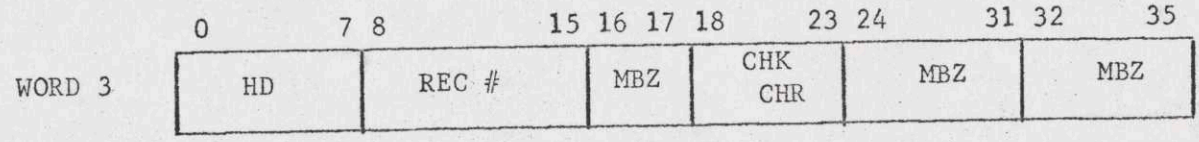
SEEK VERIFICATION DATA



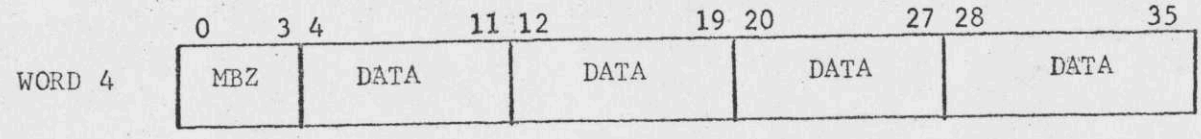
RO COUNT FIELD



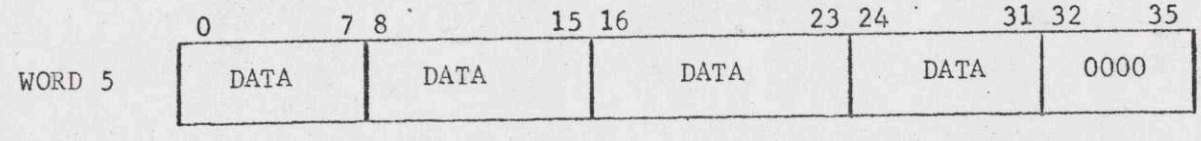
RO DATA FIELD



RO DATA FIELD



RO DATA FIELD



The first word received by the controller contains seek address verification data. The second and third words contain R0 count field information. The controller makes use of the seek address verification data information as follows:

1. It compares the cylinder, head and TI to that previously generated within the controller from the seek address. If they are not the same, the controller will terminate with "Data Alert, Invalid Seek Address." The TI bits supplied by the seek command are the new TI bits to be formatted. Any TI bits previously written on the track will be ignored.

2. The bit indicated as "Z" is to be used as a header bypass switch. If Z = 1, then the controller first must read the HA on the track and compare it to the cylinder and head information given in the command. Also, the controller shall read the first count field (Not R_0) and compare the data length with the sector size specified in the seek data. NOTE: This Z bit is not written on the track in the format operation since it has meaning only with regard to the controller function prior to formatting. When Z = 1, an additional revolution is required to format the track.

   If Z = 0, the controller shall wait for the Index Mark and format the track with no prior checks on information previously written(if any).

   NOTE: To insure data integrity, header bypass (Z - 0) should be used only on packs which have not been formatted previously.

The controller will always use the R0 Count Field information that is supplied by the EUS. Thus, when good tracks, as well as defective and alternate tracks, are to be formatted, the controller will write the six bytes of information received from the EUS (FLAG, CYL, CYL, HD, HD and Record Number) directly into R0 count field as received.

Words four and five contain the information to be written into the R0 data field. Note that for this controller, Record Zero has no key field and a data field of eight bytes. Thus, word four and word five will be written into bytes 1-8 of the R0 data field.

Word three, bits 18-23 will be used as a check character verification on all five words of data received from the EUS. If the check character is zero, the controller will bypass the verification operation. If the check character is nonzero, the controller will generate a 6-bit Exclusive Or check character from the five words (excluding the Check Character Position). If the check character from the EUS and the controller generated check character agree, the format operation will be continued. A mismatch will cause the operation to be terminated with "Data Alert, Invalid Seek Address." Note that this format for Record 0 is compatible with the Record 0 format that is used by IBM programming systems as defined in the "Component Descriptions, 2314 Direct Access Storage Facility." Also, the controller will alternate the high order bit in the flag byte for each count field starting with a "one" bit in the first data record.

A	0	0	0	0	0	T	I

COUNT FIELD FLAG BYTE

The flag byte in the Home Address will always use a high order bit of "zero." The alternating flag byte bit is included to provide pack format compatibility with the IBM 2314 controller.

The sector size to be formatted will be the size specified by the seek data:

YY = 00, 288 bytes
YY = 01, 1440 bytes
YY = 10, 12960 bytes (DSS190) - 7200 bytes (DSS181)
YY = 11, 12960 bytes (DSS190) - 7200 bytes (DSS181)

If an error condition is detected during the writing of a header, the writing of data will continue to the end of the header. The remainder of the track will not be formatted and data error status will be reported at terminate. Refer to Table 4 for status returns supplied at command termination.

3.11 REQUEST STATUS

When the controller receives a Request Status instruction, it will perform a table look-up operation based on the logical channel number to obtain controller held status for the last activity on the logical channel. If there is no controller held status then device held summary status, such as Attention and Device busy will be obtained from the device.

If an error was detected in the command sequence, the controller will supply the status for the detected error. Refer to Table 4.

The status table entry for the controller (device 0) will always be set to Channel Ready, No Substatus. Thus, a Request Status instruction addressed to the controller will cause the following status returns to be sent to the EUS.

Channel Ready	No Substatus
Instruction Rejected	* Parity Alert on IDCW
	* Invalid Op Code

*Detected errors during command sequence.

3.12 RESET STATUS

This instruction results in the resetting of any existing data alert MPC data alert and end-of-file status held in the controller for the given logical channel. The "Invalid Instruction Sequence" sub-status will also be reset.

The Reset Status instruction causes a hardware pull from the same tables in the controller as the Request Status. The controller will reset those status and determine if there also exists a MPC device attention, Attention or Device Busy status in the device, if so, the Reset Status will be returned with that status according to the major status priorities (see Section 4). If not, the appropriate "Channel Ready" status will be returned. Refer to Table 4.

A Reset Status instruction addressed to the controller (device 0) will have one of the following status returns:

Major Status	Substatus
Channel Ready	No Substatus
Instruction Rejected	* Parity Alert on IDCW
	* Invalid Op Code

3.13 WRITE CONTROL REGISTER

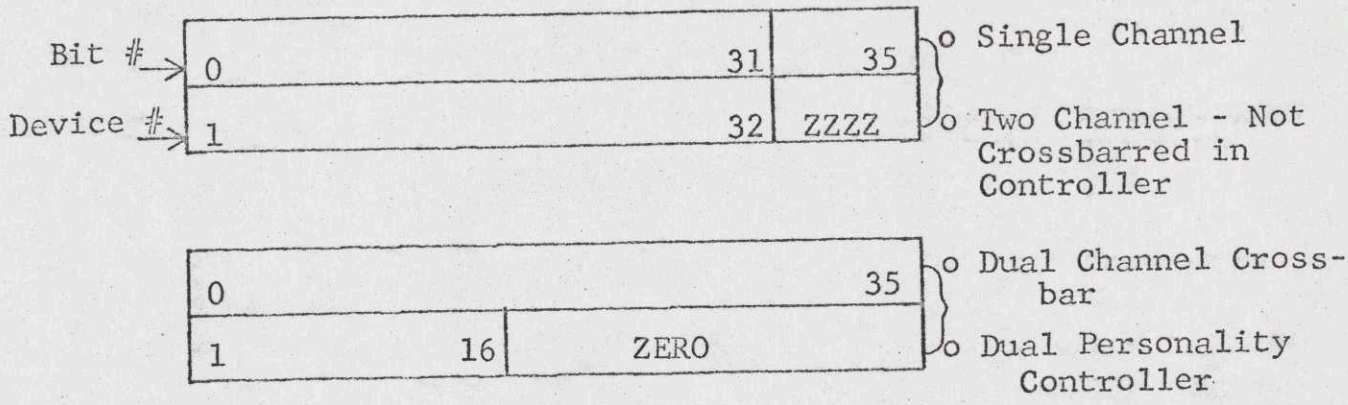
The write control register is provided to allow clearing the statistics tallies or presetting some value in the tallies. The operation of this command addressed to device is the same as the read control register except data is sent to the controller to be put in the tally registers. A write control register addressed to device zero is invalid. Refer to Table 4 for status returns supplied at command termination.

3.14 READ CONTROL REGISTER

The RCR instruction is provided to supply device seek complete/incomplete information or device operation statistics, depending on the device address associated with the command.

The RCR instruction can be addressed to any legal device. If the RCR is addressed to the controller (device zero), two 36-bit words will be transferred to the EUS. Two conditions for 32 devices.

For the DSS181 the format for each word shall be as follows:



Z - Must be Zero

Word 1 - Seek complete flag for each device, by device number.
Seek Complete = 1

Word 2 - Device available flag for each device, by device number.
Device Available = 0
Unavailable = 1

- Seek incomplete
- Standby
- Off-Line
- Device Busy Positioning

The combination of corresponding bits in Word #1 and Word #2 gives the following information.

#1	#2	
0	0	Device is available - No information about Seek Complete.
1	0	Device is available and there has been a Seek Complete.
0	1	Device is not available - Temporarily still busy positioning.
1	1	Device is not available

- Seek Incomplete
- Standby
- Off-Line
- Attention

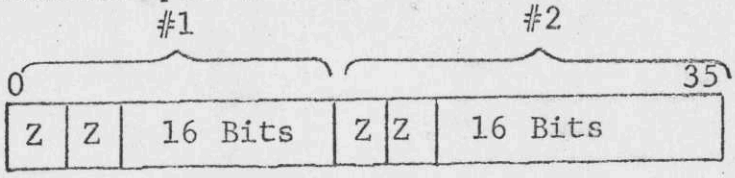
If a bit is set in Word 1 and corresponding bit in Word 2 = 0, the bit will be reset when a data transfer or new seek instruction is issued to the respective device. If a bit is set in Word 2 and the corresponding bit in Word 1 = 0 the bit will be reset when the positioning operation is complete.

If both bits are set they will be reset when the condition is cleared in the device. (That is the device is ready.)

If the RCR is addressed to a valid device other than the controller (device zero), the statistical counters for the addressed device will be transferred to the EUS.

The following sequence of 20 tally (16 bit) words will be returned for the requested device.

Ten (36 bit) words will be returned to the EUS, two tallies per word as shown below:



3.14.1 Basic Counters DSC181 and DSC190

1. Number of Movement Seeks - This counter contains the number of actuator movements of the device.

2. Write Type Data Transfer Command - Number of sectors. This counter contains the total number of sectors transferred from the EUS and written on the device.

3. Read Type Data Transfer Commands - Number of sectors. This counter contains the total number of sectors transferred from the device to the EUS.

4. Number of Data Transfer Commands - This counter contains the total number of data transfer commands issued to the device, that is, read or write.

5. Number of Seek Incompletes - This counter contains the number of seek incomplete status and controller received from the device.

6. Number of Sync Failures/Double Index/No Compare on Count Field - The sync byte on the disk pack did not agree with what it should be.

7. Number of Transfer Timing Errors DLI (CA) - This condition is caused by the controller being unable to keep up with data transfer to or from the device.

8. Number of Data Check Character Alerts - Error in the data field.

9. Number of Count Check Character Alerts - Error in the count field.

10. Number of DLI Parity Errors

3.14.2 Additional Counters for DSC190

11. Number of Alternate Tracks Processed - The track indicators on the pack indicated defective track alternate assigned and the controller went to the alternate track and continued the data transfer.

12. Number of EDAC Correctable Errors -

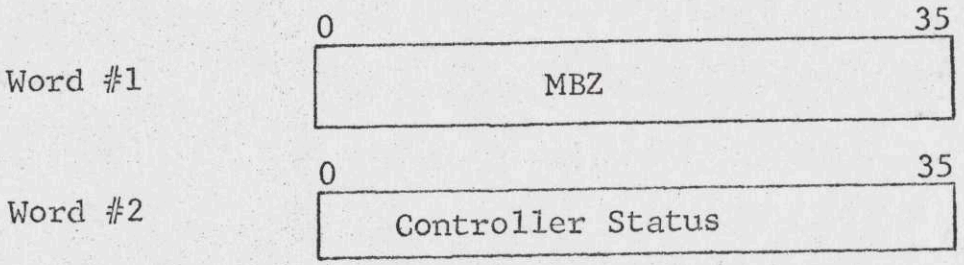
13. Number of EDAC Uncorrectable Errors -

14. Number of Retries before EDAC Correction - NOTE: DSS181 will use only the first five words (10 counters) and will return zeros for the other 10 counters.

These tallies are maintained in Read/Write Memory and may be preset or cleared to zero by using the write control register command. Refer to Table 4 for status returned on termination.

3.15 READ STATUS REGISTER

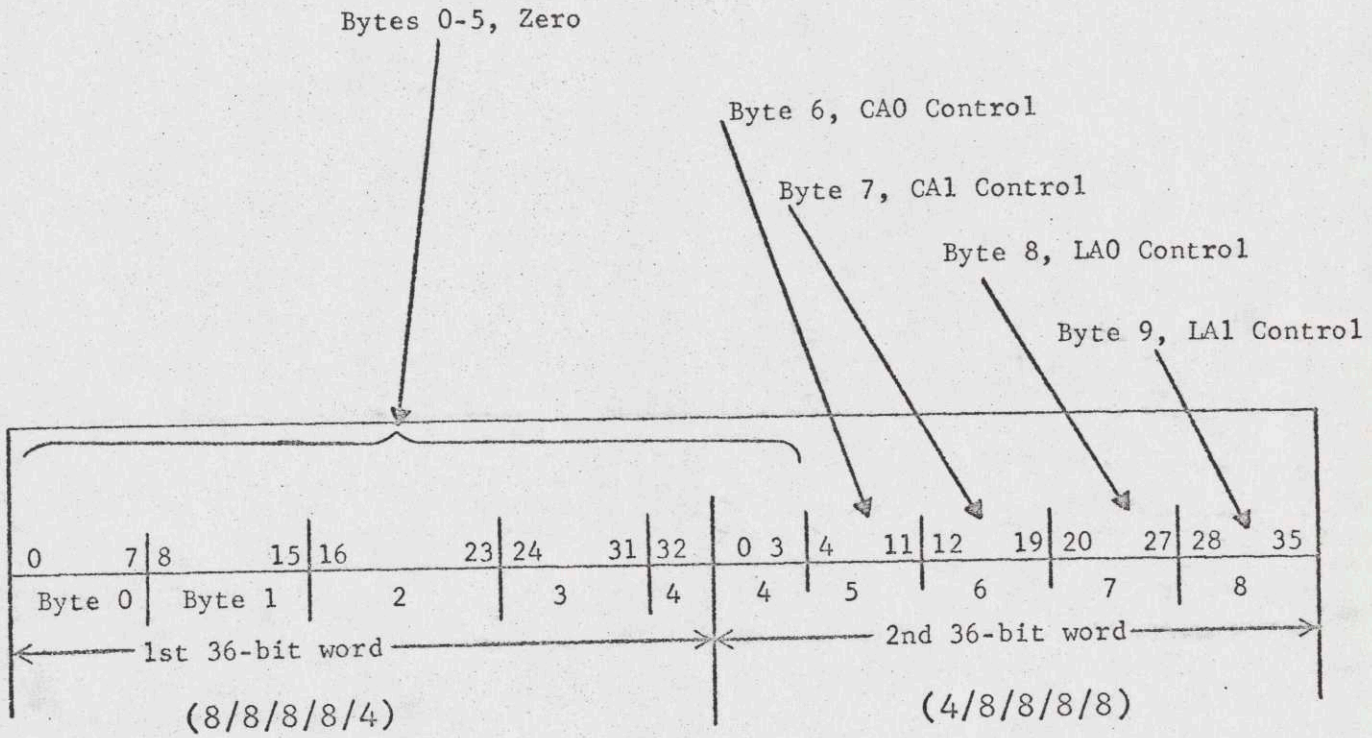
The RSR instruction is provided to supply two types of information to the EUS. The RSR command when addressed to the controller will transfer two 36-bit words to the EUS. The second word is the controller status. The first word will be returned as zero in order to be consistent with the DSS180 Read Status Register format. The format of these words will be as follows:



Word #1 - Must be zero

Word #2 - Will contain the current controller status.

Unless an error occurs in the process of data transmission, the controller will terminate with channel ready, regardless of the error being reported. Refer to Table 4.



Byte 6 and 7 - CA0, CA1

0 - Busy Flag
1 - Polling Pending
2 - Command Pending
3 - Low Priority Q Sampled
4 -
5 -
6 - Device # Error
7 - CA Error

Byte 8 and 9 - LA0, LA1

0 - Busy Flag
1 -
2 -
3 -
4 - Specials Pending (Disk)
5 - Specials Pending (Tape)
6 -
7 -

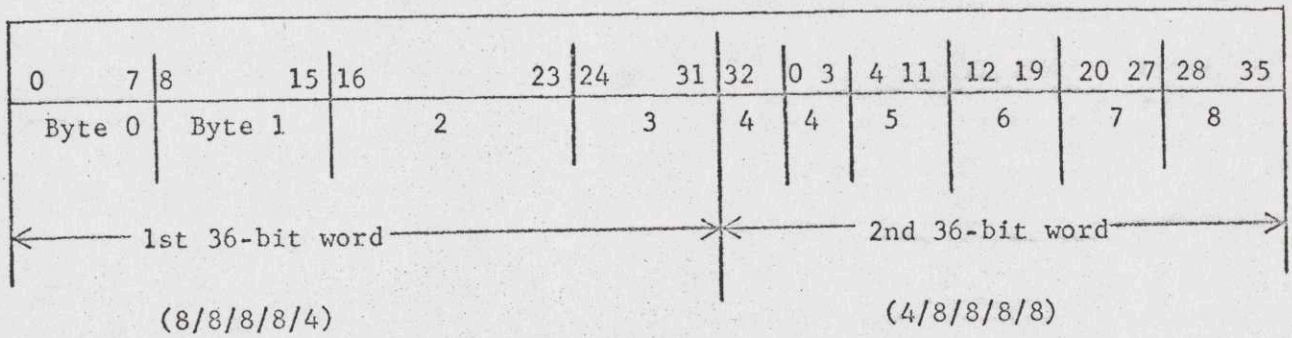
The RSR command addressed to a device will return two words of detailed status from the device in the following format:

Byte 0
Device Serial Number

Byte 1
Device Type

Byte 2
Addressed Device Summary Status

Byte 3-8
Addressed Device Detail Status



RSR Byte 0 Device Serial Number	0	
	1	
	2	Binary Number 1-32
	3	
	4	
	5	00000001
	6	00100000
	7	

		181	190
RSR Byte 1 Device Type	0	0	0
	1	1	1
	2	1	0
	3	0	1
	4	0	0
	5	0	1
	6	0	0
	7	0	0

Summary Status (DSU181 and DSU190)

	Bit Position	Status
RSR Byte 2 Summary Status (Std-All Dev)	0	Device Reserved
	1	Device Seized
	2	Device in Standby
	3	Positioner Busy
	4	DL1 Fault
	5	Device Protected
	6	Device Fault
	7	Device in Diagonal Mode

RSR Byte 3 Detailed Status Byte 1	DS1 (DSU181)	
	0	Command Parity Error
	1	No or Multiple Command Decode
	2	Invalid Command
	3	Invalid Command Sequence
	4	State Violation
	5	Protection Violation
(STD-All Dev.)	6	Must be Zero (Not Applicable to DSU181)
	7	Data Parity Error

DSB1 - Detailed Status Byte 1 (DSU190)

Bit 0 - Command Parity Error

The command decoded by the MSD contained a parity error.

Bit 1 - No Command Decoded/Multiple Commands Decoded.

RSR Byte 3 Detailed Status Byte 1

The MSD detected a command strobe (DCS) but was unable to decode a command on the command lines, or more than one command was decoded by the MDS during a single DCS interval.

Bit 2 - Invalid Command

The command decoded by the MSD is not a valid command.

Bit 3 - Invalid Command Sequence

The command decoded by the MSD was not received in a valid sequence (order only, this does not reflect improper timing).

Bit 4 - State Violation

The command decoded by the MSD was received in violation of the operating state of the MSD.

Bit 5 - Protection Violated

A Write Command was decoded by the MSD when the device was "write protected."

Bit 6 - Transfer Timing Error

The MSD has detected a timing error during data transfer which resulted in incorrect data being recorded on the disk (in the case of a write operation) or incorrect data being transferred to the CA (in the case of a read operation).

Bit 7 - Data Parity Error

The MSD detected a parity error on the data lines.

	Bit Position	Status
RSR	DS2	(DSU181)
Byte 4	0	Must be Zero (Not applicable to DSU181)
Detailed	1	Must be Zero (Not applicable to DSU181)
Status	2	Must be Zero (Not applicable to DSU181)
Byte 2	3	Must be Zero (Not applicable to DSU181)
	4	Must be Zero (Not applicable to DSU181)
(Std-All Dev)	5	Spindle Speed Loss
	6	Must be Zero (Not applicable to DSU181)
	7	Must be Zero (Not applicable to DSU181)

DSB2 - Detailed Status Byte 2 (DSU190)

This byte contains those errors relative to MSD logic faults.

Bit 0 - Loss of Write Current

The MSD has detected the loss of Write Current during a write operation.

RSR Byte 4 Detailed Status Byte 2

Bit 1 - Write Current without Write command.

The MSD has detected the presence of Write Current without the presence of a Write command.

Bit 2 - Loss of AC Write Current

The MSD has detected the absence of repetitively switched current in the write head during a Write operation.

Bit 3 - No or Multiple Head Selection

None, or more than one head has been selected by the MSD.

Bit 4 - Unassigned (MBZ)

Bit 5 - Spindle Speed Loss

The MSD has detected a drop in spindle speed below 70 percent of full RPM.

Bit 6 - Overtemperature

The MSD had detected a rise in temperature of the power supply above the acceptable limit for proper operation.

Bit 7 - Loss of Voltage

The MSD has detected a drop in dc voltage below the acceptable level for proper operation.

RSR	DS3	(DSU181)
Byte 5	0	Seek Incomplete
Detailed	1	Must be Zero (Not applicable to DSU181)
Status	2	Must be Zero (Not applicable to DSU181)
Byte 3	3	Must be Zero (Not applicable to DSU181)
	4	Must be Zero (Not applicable to DSU181)
	5	Must be Zero (Not assigned by NPL DLI Spec.)
(STD-MHD only)	6	Must be Zero (Not assigned by NPL DLI Spec.)
	7	Must be Zero (Not assigned by NPL DLI Spec.)

DSB3 - Detailed Status Byte 3 (DSU190)

This byte contains those errors relative to electromechanical failures.

Bit 0 - Seek Incomplete

The MSD has failed to complete a seek operation within a specified time.

RSR Byte 5 Detailed Status Byte 3

Bit 1 - Positioner Overtravel

The positioner carriage of the MSD has traveled beyond the limits allowed for safe Read/Write operations.

Bit 2 - Unassigned (MBZ)

Bit 3 - Unassigned (MBZ)

Bit 4 - RPS Error

The MSD has detected an error in its rotational position sensing (RPS) circuitry and subsequent positioning information may be in error. Possibility of error is detected at index.

Bit 5 - Positioner Offset

The positioner has been offset from its nominal on-track position by means of the OPO or OPI commands.

Bit 6 - Read Clock Offset

The Read Clock phasing has been offset by the ARC or RRC commands.

Bit 7 - Fine Servo

The Positioner has arrived within 1/2 track of its destination and is automatically servo track following.

	Bit Position	Status
RSR	DS4	(DSU181)
Byte 6	0	Erase Current Unsafe
Detailed	1	DC Write Unsafe
Status	2	AC Write Unsafe
Byte 4	3	Heads Unsafe
Fault(Unsafe)	4	Erase Gate and Busy
	5	Write Gate and Busy
(Dev. Specific)	6	Write Gate and No Erase Current
	7	Voltage Unsafe

DSB4 - Detailed Status Byte 4 (DSU190)

RSR Bit 0 - Unassigned (MBZ)

Byte 6 Bit 1 - Unassigned (MBZ)

Bit 2 - Unassigned (MBZ)

Bit 3 - Brush Cycle Incomplete

Status The disk cleaning action has not been completed.

Byte 4 Bit 4 - Unassigned (MBZ)

Fault (Unsafe) Bit 5 - Unassigned (MBZ)

Bit 6 - Forward Set

The Positioner Drive Forward flip-flop is set for forward movement.

Bit 7 - Reverse Set

The Positioner Drive Reverse flip-flop is set for reverse movement.

RSR Byte 7 Detailed Status Byte 5 (Indicators) (Dev. Specific)	DS5	(DSU181)
	0	Brush at Stop
	1	Pack On
	2	Lid On
	3	Index Block In
	4	Attention Latch
	5	Heads Flying
	6	Zero Speed
	7	On-Line

RSR Byte 7 Detailed Status Byte 5 Indicators

DSB5 - Detailed Status Byte 5

Bit 0 - Unassigned (MBZ)

Bit 1 - Unassigned (MBZ)

Bit 2 - Unassigned (MBZ)

Bit 3 - Unassigned (MBZ)

Bit 4 - Heads Retracted

The Positioner is in the fully retracted position.

Bit 5 - Unassigned (MBZ)

Bit 6 - Unassigned (MBZ)

Bit 7 - Write and Read

Both Write and Read gates are on at the same time.

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	Bit Position	Status
RSR Byte 8 Device Detail Status Byte 6	DS6	(DSU181)
	0	Positioner Overtemperature
	1	Positioner Over-Velocity
	2	Positioner Out of Limits
	3	Positioner Voltage Out of Limits
	4	Must be Zero (Not applicable to DSU181)
	5	Must be Zero (Not applicable to DSU181)
	6	Must be Zero (Not applicable to DSU181)
	7	Must be Zero (Not applicable to DSU181)

DSB6 - Unassigned (MBZ)for (DSU190) Therefore DSB7 will be read instead of DSB6 for RSR Byte 9 in the DSS190

DSB7 - Detailed Status Byte 7 (DSU190)

RSR Byte 8 Device Detail Status Byte 7

Bit 0 - Unassigned (MBZ)

Bit 1 - DC Voltage High

The dc voltage is higher than specified (above the high tolerance) which may shorten component life or affect normal operation.

Bit 2 - Unassigned (MBZ)

Bit 3 - Overtemperature (Logic)

The temperature in the logic card area has reached a level where reliability will be degraded.

Bit 4 - Read Amplitude Low

The Read Amplitude monitor has detected a read signal amplitude below the specified lower limit, which may cause read errors.

Bit 5 - Unassigned (MBZ)

Bit 6 - Unassigned (MBZ)

Bit 7 - Air Pressure High

The air pressure monitor has detected a rise in air pressure due to dirty filters or other blockage which may jeopardize the dust free integrity of the disk pack area.

3.16 READ EDAC REGISTER

The Read EDAC Register (RER) command addressed to the device may be used by the system software to retrieve the error correction data, displacement and sector number in error.

The two words will be returned in the format as follows:

To be defined later

This command is illegal for DSS181.

Refer to Table 4 for status returns

3.17 RELEASE

This command is used to release a device which has been reserved to this logical channel. The controller shall receive a device code which determines the device to be released.

Instruction execution During the Busy State:

If the device code is valid, the controller shall issue a release to that device. A release instruction addressed to a device that is not reserved will be accepted and treated as a legitimate instruction.

If an unrecoverable error condition is detected, the controller will send a terminate to the EUS and reflect appropriate status. If the designated device had been reserved by another channel, the Release shall terminate with a Device Busy - Alternate Channel in control status. If the Release is directed to a device which is still positioning, the release will be executed even though the seek is not complete and will terminate with a status of Channel Ready or appropriate error status. The Release command will reset the Diagnostic Mode before releasing the device if the device is in Diagnostic Mode. Refer to Table 4 for status supplied at termination.

3.18 DEVICE RESERVE

This command is used to explicitly reserve a device to a logical channel. The controller shall receive a device code which determines the device to be reserved.

Instruction Execution During the Busy State:

If the device code is valid, the controller shall issue a seize to that device. A reserve command addressed to a device that is reserved to the same EUS channel will be accepted and treated as a legitimate instruction.

If the designated device had been reserved by another channel, the reserve shall terminate with a Device Busy...Alternate Channel in control status. If the reserve is directed to a device which is still positioning, the reserve will be executed even though the preseek is not complete and will terminate with a status of channel ready or appropriate error status.

Refer to Table 4 for status returns supplied at command termination.

3.19 SET STANDBY

This command is used to cause a device to go into a standby state. The controller shall receive a device code which determines the device to be put in standby. In standby the device will be in a state which will allow the operator to change packs.

Instruction Execution During the Busy State:

If the device code is valid, the controller shall issue the set standby state to that device. A set standby instruction addressed to a device that is in standby will be accepted and treated as a legitimate instruction.

If the designated device had been reserved by another channel, the set standby shall terminate with a Device Busy - Alternate Channel in control status. If the set standby is directed to a device which is still positioning, the set standby will be executed even though the seek is not complete and will terminate with a status of channel ready or appropriate error status.

Refer to Table 4 for status returns supplied at command termination.

3.20 SPECIAL CONTROLLER COMMANDS

The "Special Controller Commands" are a group of commands dedicated to controller-type functions related to MPC controllers.

The group of commands are identified by a unique code in the "Channel Instruction Field" for the IDCW.

IDCW Format

The IDCW format for these commands is identical to the standard format as defined in Section 5.5.1. With the exception of the following special considerations, normal IDCW checking will be done on these Special Command IDCW's.

Within the IDCW format the following special considerations are to be observed.

Channel Instruction Field (Bits 24-29):

A configuration of "10XXXX" in this field identifies the IDCW as a "Special Controller Command" IDCW.

The MPC controller will interrogate this field of the IDCW, and upon finding the above configuration, interpret the "Device Instruction" field (bits 0-5) and "Device Address" fields (bits 6-11) as defined below:

Device Address Field (Bits 6-11):

For all Special Controller commands this field of the IDCW must be zero.

Device Instruction Field (Bits 0-5):

The allowable codes in this field are the following:

011010 - Write Controller Main Memory (BIN)
001010 - Write Controller Main Memory, ASCII
011100 - Conditional Write Lock Byte
001100 - Write Lock Byte
001000 - Write Control Store
010010 - Read Controller Main Memory (BIN)
000010 - Read Controller Main Memory (ASCII)
000100 - Read Lock Byte
011000 - Execute Control Store Microprogram
001110 - Initiate Write Data Transfer
000110 - Initiate Read Data Transfer

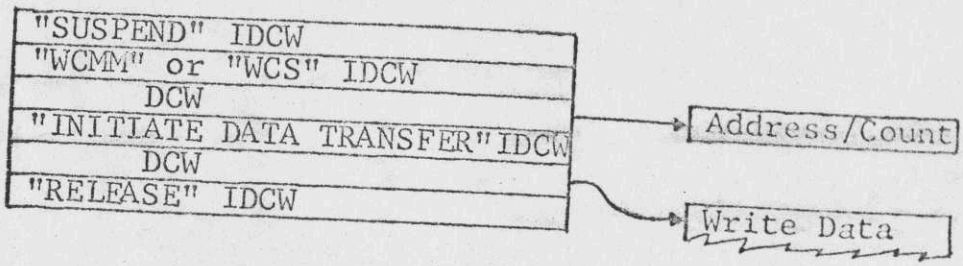
000000 - Suspend Controller
010000 - Release Controller

Channel Program Setup in External System

The following description is intended to define the sequences of IDCW's that the MPC controller will expect to see for the various Special Controller commands.

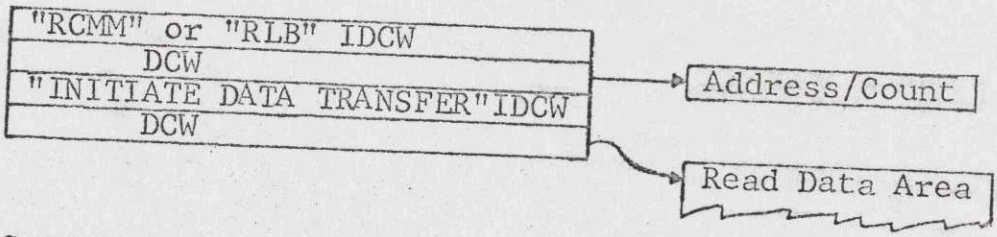
Write Controller Main Memory(WCMM) IDCW
Write Control Store (WCS) IDCW (ASCII or Binary)

For the execution of either of these IDCW's the following Channel Program setup will be required:

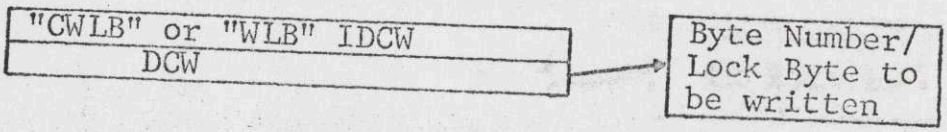


The "Suspend" IDCW can be omitted if the controller is already in the "Suspend" mode as the result of a previous IDCW. The "Release" IDCW can be omitted if it is desired to leave the controller in the "suspended" mode.

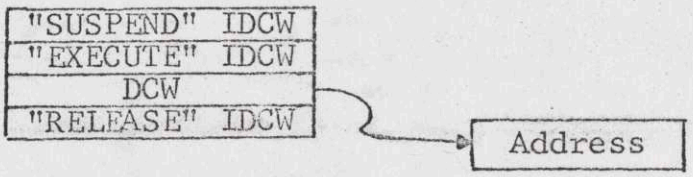
- Read Controller Main Memory (RCMM) IDCW (ASCII or Binary)
- Read Lock Byte (RLB) IDCW



- Conditional Write Lock Byte (CWLB) IDCW
- Write Lock Byte (WLB) IDCW



- Execute Control Store Microprogram (ECSM) IDCW



The "Suspend" IDCW can be omitted if the controller is already in the "Suspend" mode as the result of a previous IDCW. The "Release" IDCW can be omitted if it is desired to leave the controller in the "Suspended" mode.

Special Consideration

Special controller IDCW's cannot be mixed with normal command IDCW's in the same Channel Program.

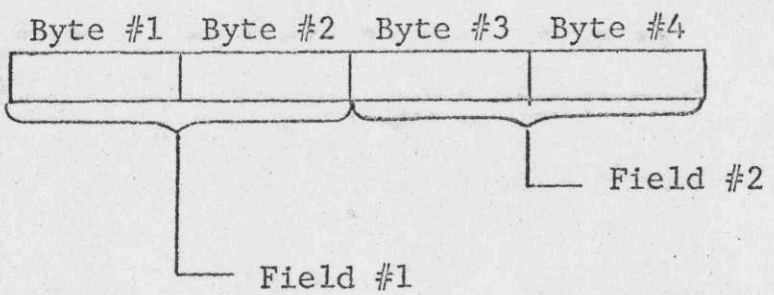
Special Command Descriptions

001010 - Write Controller Main Memory, ASCII
011010 - Write Controller Main Memory, Binary

These commands are used to write data from the external system into the MPC controller main memory.

Upon receiving this IDCW, the MPC controller will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and then receive four bytes of command data.

The controller will interpret this command data as follows:



Field #1 defines a 16-bit word address in the MPC controller main memory at which location the write operation is to start. There is no check made on the legality of this address.

Field #2 defines a 16-bit word count defining the maximum number of MPC controller words to be written by the execution of the command. (All zeros is a valid count.)

In all cases, controller "words" refer to the two-byte words.

Following the completion of the error-free reception of the command data the MPC controller will issue a "Move Pointer and Initiate Command Transfer" service code to the external system, and receive the next IDCW. This IDCW must be the "Initiate Write Data Transfer" IDCW. Upon the completion of the reception of this IDCW, the controller will issue either an "Initiate Data Transfer, Write ASCII" or "Initiate Data Transfer Write Binary" service code to the external system, and then proceed to receive the data to be written into MPC controller main memory.

The write operation will proceed until either the word count received in the command data is expired, or until the external system terminates the operation.

Special Considerations:

1. The command data which follows the "Write Controller Main Memory" IDCW must be formatted in external system memory in the "binary" mode.

2. The data to be written into controller main memory (sent after "Initiate Data Transfer IDCW) must be formatted in external system memory in the mode defined by the "Write Controller Main Memory" op code (either ASCII or Binary).

3. The controller must be in the "Suspend" state (suspend command preceded the write command), or the command will be rejected.

001000 - Write Control Store

The execution of this command is identical to the execution of the "Write Controller Main Memory, Binary" command, except that the write operation is into control store in the MPC controller, and a sum check accompanies the data to be written.

The "sum check" is sent as the last word (two-byte word) of the write data, and is not written into control store. The "sum check" will represent the twos-complement of the final summation represented by the addition of all MPC controller words (two-byte words) sent, with end-around carry (i.e., as each two-byte word is added to the sum check accumulation, carry out of the high-order byte of the two-byte accumulation is added back into the sum check accumulation). The sum check word is included in total word count specified for the command execution. Failure of the transmitted sum check to agree with the controller computed sum check will cause a failure status to be reflected by the MPC controller.

The controller must be in the "Suspend" state at the time the write command is received (suspend command preceded the write command), or the command will be rejected. (See status table which follows later.)

000010 - Read Controller Main Memory, ASCII
010010 - Read Controller Main Memory, Binary

The execution of these commands is identical to the definition and execution of the "Write Controller Main Memory" command with the following exceptions:

a. The operation is a "read" from Main Memory instead of a "write."

b. The second IDCW received from the external system must be an "Initiate Read Data Transfer" IDCW instead of an "Initiate Write Data Transfer" IDCW.

c. This command execution does not require the controller to be in the "Suspend" mode.

011100 - Conditional Write Lock Byte
001100 - Write Lock Byte
000100 - Read Lock Byte

These three commands provide a software "lock" capability in MPC controllers which are to be shared between two external user systems.

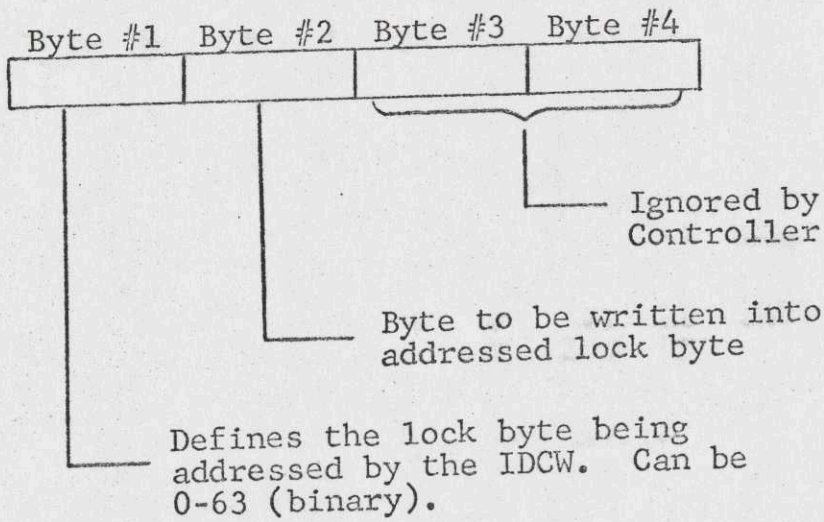
The controller does not have to be in the "Suspend" mode for these commands.

The execution of these commands is defined as follows:

Conditional Write Lock Byte

Upon receiving this IDCW, the MPC controller will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and then receive four bytes of command data.

The controller will interpret this command data as follows:



Upon completion of the reception of the command data, the controller will access the addressed lock byte. If the byte is nonzero, the controller will leave it unmodified and reflect this condition by means of termination status. This will terminate the execution of the channel program.

If the addressed lock byte is zero, the contents of Byte #2 of the command data are written into the addressed lock byte. The controller then executes whatever operation is indicated by the "Continue/ Marker" bits (bits 22,23) of the "Initiate Data Transfer" IDCW. This may be status and termination procedure, or continue to the next IDCW.

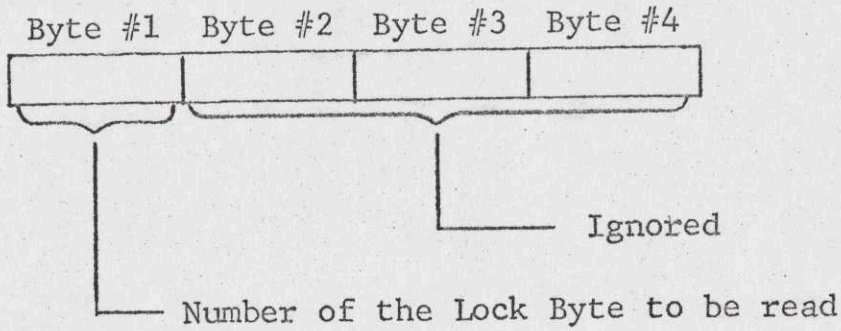
Write Lock Byte

This command is identical to the "Conditional Write Lock Byte" command, except that the controller does not first test the addressed lock byte. The write operation is executed unconditionally.

Read Lock Byte

This command is used to read the contents of any one of the 64 lock bytes contained in MPC main memory.

Upon receiving the "Read Lock Byte" IDCW, the MPC will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and then receive four bytes of command data. This data will be interpreted as follows:



Upon receiving the command data, the controller will issue a "Move Pointer and Initiate Command Transfer" service code to the external system, and then receive the next IDCW. This IDCW must be the "Initiate Read Data Transfer" IDCW.

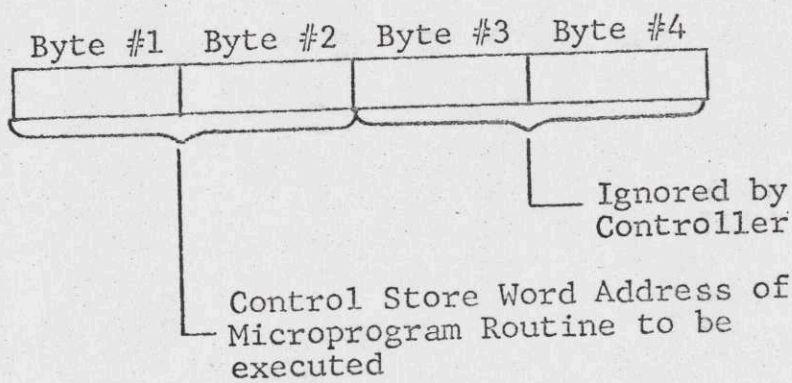
Upon completion of the reception of this second IDCW, the controller will issue an "Initiate Data Transfer, Read ASCII" service code to the external system, and send one byte of information. This byte will represent the contents of the addressed lock byte.

It should be noted that the contents of the lock byte will be stored in 6000 memory in the ASCII mode (i.e., placed in the high-order 9-bit field of the 6000 word).

011000 - Execute Control Store Microprogram

Upon receiving this IDCW, the MPC controller will issue an "Initiate Data Transfer, Write Binary" service code to the external system, and proceed to receive four bytes of command data.

The controller will interpret this command data as follows:



Upon reception of the command data the controller will branch internally to the addressed micro-program. The return address will be saved in controller register "HUXAR" when this branch is made. Upon completion of its execution, the microprogram must return via a branch on the contents of AUXAR. Upon the return from the microprogram, the controller will take the appropriate action as defined by the "Continue/Marker" bits (22,23) of the "Initiate Data Transfer" IDCW.

The controller must be in the "suspend" state at the time the "Execute" command is received (suspend command preceded the execute command), or the execute IDCW will be rejected.

000000 - Suspend Controller

This command allows a controller to be "seized" by one external system in a situation where the controller is physically connected to more than one system via two or more PSI interfaces.

The command will cause the controller to take the following actions:

- Ignore all "Channel Program Waiting" lines from all PSI interfaces, and wait until all current I/O operations in progress at the time the Suspend command was received are completed. (This implies that any channel program has been initiated will be completed.)

- Issue a "Special Status Storage" and Special Interrupt to all connected PSI interfaces including the PSI interface over which the Suspend command was received.

The format of the four-byte status storage will be as follows:

Byte 1: 000_8

Byte 2: 000_8

Byte 3: 001_8

Byte 4: 000_8

The "Special Status Storage" and "Interrupt" will be sent to logical channel #0 in all cases, irrespective of the LC number over which the suspend command was received.

- Execute the action defined by the "Continue/ Marker" field of the "Suspend IDCW" (bits 22, 23) which will be one of the following:

  a. Make a status entry and generate a terminate interrupt.

  b. Make a status entry, generate a marker interrupt and access the next IDCW (continue bit on in suspend IDCW).

  c. Make no status entry, but immediately access and execute the next IDCW.

- Ignore all "Channel Program Waiting" lines from any other PSI interface other than the one over which the suspend was received. The PSI interface initiating suspend will be serviced normally, with the following exception:

  Subsequent IDCW's received by the controller over the PSI interface which issued the "suspend" command or the IDCW will be rejected with appropriate status (see status table which follows later).

  The "suspend" command must be the first IDCW or the channel program in which it is sent.

010000 - Release Controller

This command is used to reset the "suspend" condition set up by a "suspend" command. The controller will issue a "Special Status Storage" and special interrupt to logical channel #0 of all connected PSI interfaces. The "Special Status Storage" will consist of all zeros, except for byte 3, which will be a 002_8.

The controller will then execute a status entry and terminate interrupt.

The "Release" command must be the last IDCW of the channel program in which it is sent. This command will terminate the channel program irregardless of the state of the "continue" bit of the "release" IDCW.

3.21 BOOTLOAD CONTROL STORE

Control Store Personality Overlay:

This command is used for loading the Controller Personality into the Controller Control Store. The overlay operation is begun at control store location 512, and continues until terminated by the external system.

A "sum-check" word (two-bytes wide) will follow and be included as a part of the overlay data. This sum check word will represent the twos-complement of the result of the binary addition of all two-byte overlay words received, with end-around carry.

If the Control Store Personality Overlay command is executed error-free, the controller will reflect "Ready Major Status" followed by a termination interrupt. Upon completion of a successful overlay, the controller is set to the "normal" operating mode by the "WAIT" microprogram, which then branches to location 512, which is the first microinstruction of the personality overlay.

Any error detected during the reception and execution of the Control Store Personality Overlay command will be reflected by the controller reverting to the "halt" state, which will in turn cause the Operational-In line to the IOM to drop.

The Control Store overlay data must be formatted in the "ASCII" mode in the 6000 Memory (one-byte right-justified in each 9-bit segment of the 6000 word).

3.22 ITR BOOT

Control Store Test Overlay;

This command will result in the transfer from the external system of a maximum of 512 two-byte words (1024 bytes) which are written into Control Store, starting at location 512.

A "sum-check" word (two-bytes wide) will follow and be included as a part of the overlay data. This sum check word will represent the twos-complement of the result of the binary addition of all two-byte overlay words received, with end-around carry.

The external system can terminate the load operation early. Otherwise, the controller will terminate the load after receiving 512 two-byte words plus the sum-check word.

The Control Store overlay data must be formatted in the "ASCII" mode in the 6000 Memory (one byte right-justified in each 9-bit segment of the 6000 word).

The "Control Store Test Overlay" command is intended for executing ITR overlays (overlay of test micro-programs). As such, the execution of the command itself is considered to be a part of the overall ITR test execution. Therefore, if any error is detected during the execution of the overlay operation itself, the controller will halt, with appropriate fault symptoms displayed on the Controller Maintenance Panel. (This will result in the dropping of the Operational-In line to the IOM.)

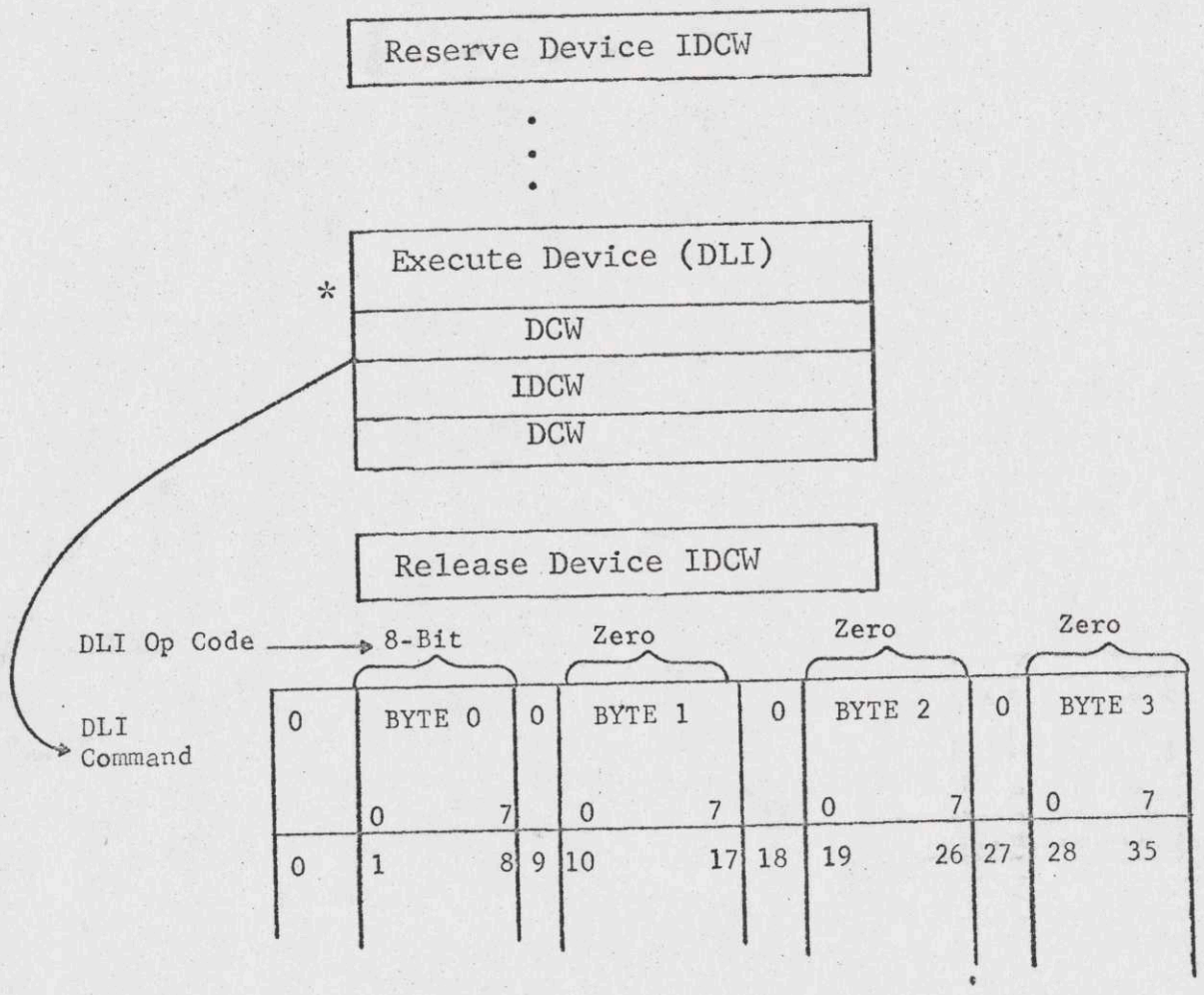
If the overlay operation is executed without error, the response to the system will be major status of "Ready" (0000), and "all-zeros" substatus, followed by a Terminate Interrupt.

Following successful completion of the test overlay, including Terminate Interrupt, the controller will drop the Operational-In line to the IOM, and commence execution of the overlay just received. The test overlay will be entered at Control Store address 514. The execution of the ITR overlay may result in the halting of the Controller (fault detected), in which case the Operational-In line to the IOM will remain down.

If the ITR overlay execution completes without a fault detection, the controller will raise the Operational-In line to the IOM, and will generate a Special Status storage followed by a Special Interrupt to the external system. The format of the Special Status storage will be as defined previously in this memo. At this point the controller will be idling in the "WAIT" routine, waiting for the next command from the external system.

3.23 Execute Device DLI Command Mode Control (30_8)

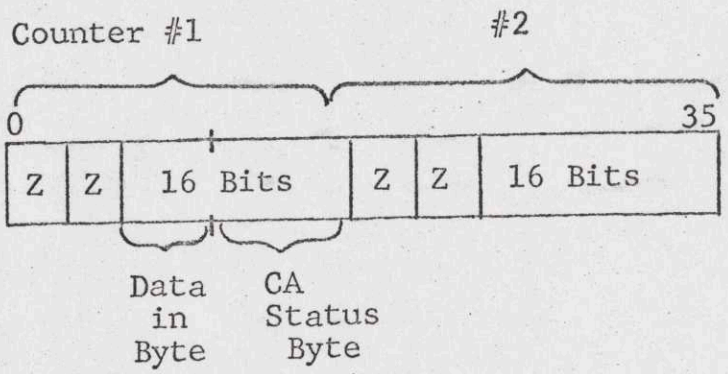
This command provides a mechanism for transferring DLI commands directly from the external user system to the addressed device. Prior to issuing this command, the EUS must have issued a Reserve Device command to the desired device. If the device is not reserved with the Execute Device (DLI) command is received by the controller, the command shall be rejected with MPC command reject - illegal procedure status. The correct channel program format is illustrated below:



*Only one DLI command for each Execute Device (DLI) command.

In response to a correct Execute Device (DLI) IDCW the controller will place the PSIA in the ASCII mode, and begin requesting the information bytes. The first byte will contain the DLI command which the controller places directly on the control lines to the addressed device. The other bytes are ignored by the controller.

If this DLI command requests information from the device, the requested byte and CA status is placed in the controller main memory in counter number one (number of movement seeks) of the error statistics for the addressed device. CA status is always placed in the second byte for both input and output.



The EUS may then retrieve this byte of device status by issuing the Read Control Register command to the same device as addressed by the Execute Device (DLI) command.

Termination status for this command is always "Ready," the only other status will be instruction rejected or MPC command reject.

DLI Commands

	000000	
	000001	
01	000010	SFU-Seek Forward Upper
01	000011	SFL-Seek Forward Lower
01	000100	SRU-Seek Reverse-Upper
01	000101	SRL-Seek Reverse-Lower
01	000110	COU-Cylinder Out-Upper
01	000111	COL-Cylinder Out-Lower
01	001000	HOU-Head Adr. Out-Upper
01	001001	HOL-Head Adr. Out-Lower
	001010	
	001011	
	001100	
	001101	
	001110	
11	001111	WRT-Write

01	010000	SZE-Seize Device
01	010001	RLS-Release Device
01	010010	RCB-Recalibrate
01	010011	SSM-Set Standby
01	010100	SLM-Set Local
01	010101	RDM-Reset Diagnostic Mode
01	010110	ENM-Enable Meter
01	010111	DSM-Disable Meter
01	011000	SPO-Shift Position Out
01	011001	SPZ-Shift Position In
01	011010	ARC-Advance Read Clock
01	011011	RRC-Retard
01	011100	HDS-Head Select
01	011101	HDD-Head Deselect
01	011110	SDM-Set Diagnostic Mode
01	011111	SDE-Set Diagnostic Escape

00100000	HIU-Head Adr. In-Upper
00100001	HIL-Head Adr. In-Lower
00100010	CIU-Cylinder In-Upper
00100011	CIL-Cylinder In-Lower
00100100	API-Angular Position In
10100101	RDX-Read
00100110	DNR-Service Number In
00100111	DTR-Service Type In
00101000	SSR-Summary Status In
00101001	DS1-Detail Status-Byte 1
00101010	DS2-Detail Status-Byte 2
00101011	DS3-Detail Status-Byte 3
00101100	DS4-Detail Status-Byte 4
00101101	DS5-Detail Status-Byte 5
00101110	DS6-Detail Status-Byte 6
00101111	DS7-Detail Status-Byte 7

01110000	
110001	
110010	
110011	
110100	
110101	
110110	
110111	
111000	
111001	
111010	
111011	
111100	
111101	
111110	
00111111	DS8-Detail Status-Byte 8

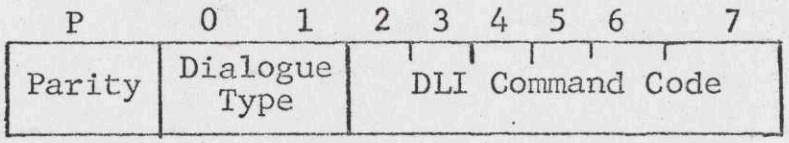
CA Awareness of the "Type" of DLI Dialogue

The DLI dialogues can be divided into four types:

Input	(00)
Output and Control	(01)
Data Transfer-READ	(10)
Data Transfer-WRITE	(11)

Rather than decoding the DLI command codes to determine the type of the DLI dialogue, a two-bit code will be supplied by firmware for such a purpose.

These two bits are an extension to the DLI command register as follows:



When using the Execute Device command (DLI) all eight bits must be supplied in the op code byte. Because the DLI command codes sent to the devices must carry good parity, the parity bit on this register reflects odd parity for bits 2-7 only.

When this register is loaded, the CA looks at bits 0-1, and if only one of the two bits is on, then the parity bit received from the MPC is reversed before loading the register. On reading, parity is regenerated.

4. STATUS

Table 4 lists the possible status returns to the various instruction terminations. The major statuses and substatuses are described in detail in the paragraphs below:

4.1 CHANNEL READY (0000)

No Substatus (000000)

This status indicates that the controller/device is on line and ready and no detectable error conditions exist. When received at termination of a seek type instruction, this substatus indicates that the on-line portion has been successfully completed. The controller is free to receive another instruction for that channel. When automatic retry is performed by the controller, the binary number coded in the substatus is the number of times the retry was performed.

Automatic Retry was performed	(00X001)
Once	(00X010)
Twice	(00X011)
Three Times	(0010XX)
Device in T&D Mode	

4.2 DEVICE BUSY (0001)

The device busy status in response to an instruction, indicates that the addressed storage unit is operating but temporarily not available.

Alternate Channel in Control (100000)

This substatus is sent to the EUS which is attempting to gain control of the device or to a release, reserve. set standby, set local instruction directed to a device reserved by a different channel (dual channel operation).

Device Positioning (000000)

This substatus indicates that the addressed device was busy positioning. This status will be returned only for Request Status and Reset Status.

4.3 ATTENTION (0010)

The Attention status indicates that a condition has occurred which may require manual intervention.

Write Inhibit (0000X1)

This substatus is sent to the EUS as the result of a write type instruction being issued to a file that is write inhibited.

Seek Incomplete (00001X)

This substatus results when the access mechanism of the addressed device has failed to position after a determined period of time. The controller has attempted to correct the condition three times with restore and seek sequences. Unless there is a permanent hardware failure, this attention condition may be corrected by issuing additional Restore instructions to the addressed device from the EUS. (The restore must be followed by a Seek before device data transfer can occur.)

Device Off-Line (100000)

This substatus is sent to the EUS to indicate that the addressed device is off-line power off, or not connected to the subsystem. OPI is down from the device.

Device Inoperable (001000)

This substatus indicates that the device is on-line but is operating in a fault condition and must be investigated. The fault status indicates the detection of an illegal combination of conditions within the device.

Device in Standby (010000)

This substatus indicates that the device is in a standby state, that is, the spindle motor has been turned off and heads retracted.

4.4 DATA ALERT (0011)

The Data Alert status indicates that an error was detected during execution of the last instruction on that I/O channel. Any new instruction, except Request Status, will reset the Data Alert status.

Transfer Timing Alert (000001)

A Transfer Timing Alert during data transfer will occur when data is lost because some hardware stage of the data transfer logic cannot keep up the transfer rate.

Transmission Parity Alert (000010)

This condition is defined as occurring when a parity error is detected by the MPC during the transmission of data bytes from the EUS or to or from the device.

Invalid Seek Address (000100)

A Special Seek was issued to a user cylinder, or a normal seek was issued to the T&D cylinder. The seek address exceeds the limit of one device. If the format track verification data does not match the seek address. If less than five bytes or more than five bytes are transferred as seek data.

This status will be returned also when the check character test on the format instruction has a compare mismatch.

Header Verification Failure (0X1000)

This status is returned to the EUS when the subsystem is unable to locate the desired sector on the addressed track, or when a cylic check alert is detected when the controller reads the count field of a particular sector. Also, if a cyclic check error occurs as a result of reading Home Address (HA), this substatus shall be returned.

Check Character Alert (X1X000)

This substatus indicates that the field cyclic check character generated in the CA did not compare with the one recorded on the media. This status will be set for all check character failures, whether they occur on a count or data field or the home address. If the cyclic check occurs on the data field, the status returned will be (010000). For write and compare operations, the status will be (110000) if the compare operation failed in addition to the cyclic check error on the data field.

Since the controller checks the count field for each sector in all sector read and write operations (excluding format), it is possible to get a cyclic check condition on the count field. When this happens, the controller will return a status of (011000), which is a combination of header verification failure and check character alert.

Compare Alert (1X0000)

This substatus resulting from a write and compare instruction indicates that the data recorded on the media does not compare to data received from the EUS.

4.5 END OF FILE (0100)

End of file status indicates that the data transfer for the last instruction tried to exceed some defined boundary. This boundary may be a physical limit (end of cylinder), last block of an alternate track or a program-imposed limit (sector count limit). An EOF shall be indicated any time the track indicators change or upon entering or leaving a track formatted as alternate.

End-of-File - Good Track Detected (000000)

This status will be returned by the controller if the sector address in the count field is correct but the controller detected a Good Track Indicator when it was expecting an Alternate or Defective Track. This status will occur only when the EUS has issued a seek to a track with "good" track indicators when it was expecting something else.

Last Consecutive Block (0000X1)

This condition shall occur when the last consecutive block of the addressed actuator position has been reached and the operation presently being executed has not been completed, or when the controller detects an overflow from an alternate track.

Sector Count Limit (00001X)

This condition indicates that the total number of data sectors specified in the sector count limit were accessed but the processing system has not issued a Terminate Out Signal.

Defective Track Detected, Alternate Assigned (000100)

This condition shall occur when a read or write type instruction is attempted on a defective track or when overflow is detected to a defective track. The track indicators on the defective track are binary 10.

Defective Track Detected, No Alternate Assigned (001000)

This status is similar to the other Defective Track status except that the track indicators are binary 11. This indicates that no alternate has been assigned to the defective track.

Alternate Track Detected (010000)

This status will be returned if the sector address in the count field is correct but the controller detected an alternate track when a good or defective track was expected.

4.6 INSTRUCTION REJECTED (0101)

The Instruction Rejected status indicates that the instruction just received is not acceptable to the subsystem and was not initiated. The status is reset when any new instruction is received.

Invalid Operation Code (000001)

This substatus indicates that an operation code invalid for this subsystem was received from the EUS.

Invalid Device Code (000010)

This substatus indicates that an invalid device code for this subsystem was received from the EUS. Further, no device with the given address is connected to the subsystem. If the device is connected but does not have power on, the status will be Attention Device Off-Line or a controller only command (special controller, bootload, ITR boot) was received with a nonzero device code.

Parity Alert on IDCW (000100)

This substatus indicates that a parity error was detected by the LA on the IDCW.

Invalid Instruction Sequence (001000)

This condition shall occur when the subsystem receives a Data Transfer instruction without a prior valid seek on the same logical channel. Restore and Preseek are not valid seeks for data transfer.

4.7 CHANNEL BUSY (1000)

The channel busy status is reflected by the channel and indicates that the controller is in the process of executing an instruction from the EUS where the channel must be dedicated to the operation.

4.8 MPC STATUS EXTENSIONS

The following new major status categories are established, for use by MPC controllers:

MPC Device Attention	1010
MPC Device Data Alert	1011
MPC Command Reject	1101

These three new categories are to be considered extensions of the currently existing Attention, Data Alert and Command Reject major status classifications, and each will be used to reflect the same basic type of status as its previously defined counterpart.

Substatus under these new major status classifications will be encoded as one of 64 possible 6-bit codes (as opposed to bit encloding).

Substatus codes 00_8 - 07_8 under MPC Device Attention, MPC Device Data Alert and MPC Command Reject are reserved for status returns which are generated independent from the device personality of the controller.

MPC Device Attention (1010)

- Configuration Error (000001)
- Device Number Error (000011)
- Multiple Devices (000010)
- CA Unexpected Interrupt (after initialize) or CA OPI down (001011)

Configuration Switch Error

This error condition will occur if the personality firmware loaded into a controller does not agree with the configuration switches on the MPC operator panel.

Multiple Devices

This substatus indicates that the controller has detected at least two devices with the same identification number.

Device Number Error

At least one device has an identification number which is outside the range of legal device numbers for the subsystem.

CA Unexpected Interrupt

The configured switch error will probably be returned as termination status for the first command issued to the controller after the personality firmware has been loaded. The Multiple Devices substatus and Device Number Error substatus will most likely be returned as termination status for the first command issued to the controller following the loading of the personality firmware. However, either may occur at any point in time. Also, both may occur in which case the Device Number Error will take priority.

MPC Device Data Alert (1011)

Transmission Parity	000001

Parity error on data transmission.

Inconsistent Command	000010

All lock byte commands if illegal lock byte number is specified.

Sum Check Error	000011

Sum check error on data written to the controller.

Byte Locked Out	000100

Conditional write lock byte is referenced to a lock byte which is nonzero (locked).

Error Correction Required	001001
EDAC Error Uncorrectable	001010
Sector Size Error	010001
Nonstandard Sector Size	010010

MPC Command Reject (1101)

Illegal Procedure	000001

Write controller main memory and write control store when the controller is not in "Suspend" mode.

Execute control store microprogram and initiate read/write data transfer IDCW not preceded by special controller command IDCW.

Illegal Logical Chan Number 000010

Illegal logical channel number on all types of IDCW's.

Illegal Logical Chan Number to "Suspended" Controller 000011

When the controller is suspended and an IDCW is addressed to a logical channel other than the one over which the Suspend command is issued.

Continue Bit Not Set 000100

The first IDCW of a two-IDCW command does not have the continue bit set. (Special controller commands.)

4.9 CHANNEL ABORT - CONTROLLER ERROR INTERRUPT

The controller will detect internal hardware errors, such as parity errors on internal registers, parity errors on main memory (read/write) data, parity errors on microinstructions accessed from control store, etc.

The detection of any one of these internal hardware errors will result in the automatic execution of an error interrupt, which forces the controller to branch to a fixed control store location, and establishes an "error interrupt in progress" state of the machine.

The microprogram which is automatically entered as a result of the error interrupt will first test the state of Configuration Switch #14 of the Maintenance Panel. If the switch is set, an immediate branch will be made to the Integrated Test Routine (ITR) module, located in the first 512 locations of control store. (The exact entry point to be determined during implementation.) Setting of switch 14 therefore implies that the MPC controller will be put in the ITR mode upon the occurrence of an error interrupt.

If switch 14 is not set, the error interrupt microprogram will take the following actions:

a. Safestore in a fixed main memory area (to be defined) the current contents of all pertinent hardware registers.

b. Terminate all existing activity in progress, including device movement. This must be evaluated and implemented on a device type basis. The execution of an active channel program (DCW list) will be aborted.

c. Reset the error interrupt level, and return the controller to normal operation (that is, waiting for command from central system).

The occurrence of the error interrupt will force the "operational-in" line of the PSI interface to the external system to revert to the "nonoperational" state. This line will stay in the "nonoperational" state until the "error interrupt in progress" state is reset by the microprogram.

Detection of Error Interrupt Sequence by External User System

The external indication that the controller has taken an error interrupt is the dropping of the "operational-in" line of the PSI interface to the external system. This line will be down for the duration of time the controller is in the "error interrupt in progress" state, which is a function of how many microinstructions must be executed by the error interrupt microroutine. As an order of magnitude, it can be assumed the "operational-in" line will be down for approximately 15 microseconds. Repeated error detections will result in repeated error interrupts, and the PSI adapter in the IOM will detect the PSI "operational-in" line dropping if a channel program (DCW list) is currently being executed for any one of the eight logical channels of the PSI. The adapter will generate a status storage, and mask the logical channel.

The error interrupt occurrence will go undetected by the external system, however, if no logical channel of the PSI interface is active or initiated, during the time the "operational-in" line to the EUS is down.

As described above, execution of an error interrupt sequence will result in the safestoring of pertinent registers in main memory. This safestore area can be accessed by the external system for diagnostic purposes as required, using the "Read Controller Main Memory" special controller command.

4.10 MAJOR/SUBSTATUS STATUS PRIORITIES

The priority of major status returns will be as follows:

Instruction Rejected (Highest)	(0101)
MPC Command Reject	(1101)
Data Alert	(0011)
MPC Device Data Alert	(1011)
End-of-File	(0100)
Attention	(0010)
MPC Device Attention	(1010)
Device Busy	(0001)
Channel Ready (Lowest)	(0000)

The following table defines the codes and priorities for substatus within major status. Substatus is listed in order from the highest to the lowest priority.

INSTRUCTION REJECTED	0101
IDCW Parity Alert	000100
Invalid Op Code	000001
Invalid Device Code	000010
Invalid Instruction Sequence	001000
MPC COMMAND REJECT	1101
Illegal Procedure	000001
Illegal Logical Channel Number	000010
Illegal, Suspended	000011
Continue Bit Not Set	000100

DATA ALERT	0011
Transmission Parity Alert	000010
Transfer Timing Alert	000001
Invalid Seek Address	000100
Header Verification Failure	0X1000
Cyclic Checkword Alert	X1X000
Compare Alert	1X0000
MPC DEVICE DATA ALERT	1011
Transmission Parity	000001
Inconsistent Command	000010
Sum Check Error	000011
Byte Locked Out	000100
Nonstandard Sector Size	010010
Sector Size Error	010001
EDAC Error Uncorrectable	001010
Error Correction Required	001001
END-OF-FILE	0100
Last Consecutive Block	0000X1
Block Count Limit	00001X
Defective Track (Alt. Track Assigned)	000100
Defective Track (No Alt. Assigned)	001000
Alternate Track Detected	010000
Good Track Detected	000000
ATTENTION	0010
Device Inoperable (Fault)	001000
Device Off-Line	100000
Seek Incomplete	000010
Write Inhibit	000001
Device Standby	010000

MPC DEVICE ATTENTION	1010
Configuration Error	000001
Device Number Error	000011
Multiple Device	000010
CA Error	001011
DEVICE BUSY	0001
Alternate Channel in Control	100000
Device Positioning	000000
CHANNEL READY	0000
No Substatus	000000
Retry was Performed	000001
Retry Twice	000010
Retry Three Times	000011
Device in T&D Mode	0010XX

Table 4

	INSTRUCTION REJECTED	IDCW Parity Alert	Invalid Op Code	Invalid Device Code	Invalid Instruction Sequence	DATA ALERT	Transmission Parity Alert	Transfer Timing Alert	Invalid Seek Address	Header Verification Failure	Cyclic Checkword Alert	Compare Alert	END-OF-FILE	Last Consecutive Block	Sector Count Limit	Defective Track	Defective Track	Alternate Track	Good Track Detected	ATTENTION	Device Inoperable	Device Off-Line	Seek Incomplete	Write Inhibit	Device in Standby
SEEK	x	x	x	x		x			x											x	x	x			x
SPECIAL SEEK	x	x	x	x		x			x											x	x	x			
PRESEEK	x	x	x	x	x	x			x											x	x	x			x
RESTORE	x	x	x	x																x	x	x			x
READ	x	x	x	x	x	x	x			x	x		x	x	x	x	x	x	x	x	x				x
READ ASCII	x	x	x	x	x	x	x			x	x		x	x	x	x	x	x	x	x	x	x			x
WRITE	x	x	x	x	x	x	x			x	x		x	x	x	x	x	x	x	x	x	x	x		x
WRITE ASCII	x	x	x	x	x	x	x			x	x		x	x	x	x	x	x	x	x	x	x	x		x
WRITE & COMPARE	x	x	x	x	x	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x			x
READ NONSTANDARD	x	x	x	x	x	x	x			x	x									x	x	x			x
READ TRACK HEADER	x	x	x	x	x	x	x			x	x									x	x	x			x
FORMAT TRACK	x	x	x	x	x	x	x		x	x	x									x	x	x	x		x
REQUEST STATUS	x	x	x	x		x	x		x	x	x	x	x		x	x	x	x	x	x	x	x	x		x
RESET STATUS	x	x	x	x																x	x	x	x		x
WCR WRITE CONTROL REG.	x	x	x	x		x														x	x				
RCR READ CONTROL REG.	x	x	x	x		x																			
RSR READ STATUS REG.	x	x	x	x		x														x	x				x
RER READ STATUS REG.	x	x	x	x		x																			
RELEASE DEVICE	x	x	x	x																x	x				x
RESERVE DEVICE	x	x	x	x																x	x				x
SET STANDBY	x	x	x	x																x	x				x
SPECIAL CONTROLLER CMDS	x	x	x																						
BOOTLOAD C.S.																									
ITR BOOT																									
EXECUTE DEVICE	x	x	x																						

Table 4

	DEVICE BUSY / Alternate Channel in Control	Device Positioning	CHANNEL READY / No Substatus	Retry Was Performed	Retry Twice	Retry Three Times	T&D Mode	MPC COMMAND REJECT / Illegal Procedure	Illegal Logical Chan. Number	Illegal Chan. No. to Suspend	Continue Bit Not Set	MPC DEVICE DATA ALERT / Transmission Parity	Inconsistent Command	Sumcheck Error	Byte Locked Out	Error Correction Required	READ Error Uncorre table	Sector Size Error	Nonstandard Sector Size
SEEK	x		x	x	x	x			x										
SPECIAL SEEK	x		x	x	x	x			x										
PRESEEK	x		x	x	x	x			x										
RESTORE	x		x						x										
READ	x		x	x	x	x			x							x	x	x	x
READ ASCII	x		x	x	x	x			x							x	x		
WRITE	x		x	x	x	x			x										
WRITE ASCII	x		x	x	x	x			x										
WRITE & COMPARE	x		x	x	x	x			x										
READ NONSTANDARD	x		x	x	x	x													
READ TRACK HEADER	x		x	x	x	x			x							x	x		
FORMAT TRACK	x		x						x									x	x
REQUEST STATUS	x	x	x						x							x	x	x	x
RESET STATUS	x	x	x						x										
WCR WRITE CONTROL REG.			x						x										
RCR READ CONTROL REG.			x						x										
RSR READ STATUS REG.	x		x						x										
RER READ EDAC REG.			x						x										
RELEASE DEVICE	x		x						x										
RESERVE DEVICE	x		x						x										
SET STANDBY	x		x						x										
SPECIAL CONTROLLER CMDS			x					x	x	x	x	x	x	x	x				
BOOTLOAD C.S.			x						x										
ITR BOOT			x						x										
EXECUTE DEVICE			x																

Table 4

	MPC DEVICE ATTENTION	Configuration Error	Device Number Error	Multiple Devices	CA Unexpected Interrupt	
SEEK			x	x	x	
SPECIAL SEEK			x	x	x	
PRESEEK			x	x	x	
RESTORE			x	x	x	
READ						
READ ASCII						
WRITE						
WRITE ASCII						
WRITE & COMPARE						
READ NONSTANDARD						
READ TRACK HEADER						
FORMAT TRACK						
REQUEST STATUS		x	x	x	x	
RESET STATUS		x	x	x	x	
WCR WRITE CONTROL REG.						
RCR READ CONTROL REG.						
RSR READ STATUS REG.						
RER READ EDAC						
RELEASE			x	x	x	
RESERVE DEVICE			x	x	x	
SET STANDBY			x	x	x	
SPECIAL CONTROLLER CMDS						
BOOTLOAD C.S.						
ITR BOOT						
EXECUTE DEVICE						

5. SOFTWARE VISIBILITY

5.1 COMMAND AND STATUS

5.1.1 Commands

The subsystem commands of the DSS175/180 will be implemented as a modified subset in the DSS181 and DSS190. The subsystem shall read and write multiple sequential data sectors, multiple tracks and multiple cylinders as specified by the EUS.

5.1.2 Status

The controller shall perform the status formatting necessary to reflect subsystem status to the EUS in the form of major status and substatus as defined for the DSS175/180. Additional device and controller status will be returned by the Read Status Register, and Read Control Register commands. The first word of status will be mapped by the MPC, so that the IOM status table will have major and minor status and will look to a user like the status of our current product offerings (167, 170, 180). Additional words of status will be placed in status tables in the controller that may be accessed with Read Status Register command, (Section 3.16) by the operating system.

New major status categories have been added for use by MPC controllers. These new major status are extensions of the present major status. Substatus under these major status will be encoded as one of 64 possible 6-bit codes (as opposed to bit coding). Reference Section 4.

The new major status will be used for reflecting status which cannot be mapped under existing major status categories, due to lack of substatus bits. Where more than one condition exists at any one time, a priority of substatus will be set up and only one condition indicated by substatus under the new major status at any one time.

5.1.3 Instruction Set Consideration

The following items apply to the entire instruction set and must be recognized by the EUS in its use of the subsystem.

- Each instruction which causes any data to be read from or written on a device (rather than controller store) must be preceded by a seek instruction to that device from the same logical channel and the control information associated with that seek can be used for only one data transfer instruction.

- The controller has the ability to recover from certain temporary errors within the subsystem. See Section 5.8 for a discussion of this feature.

5.1.4 EUS Controller Command Sequence

The controller will provide the command sequence interface as defined in the PSI EPS-I, 43A177874.

- All non-valid instruction codes will be rejected with Instruction Reject, Invalid Op Code.

- A Request Status or Reset Status instruction will return the last controller status stored by the controller or summary device status for the given device number. Note that this also includes "Instruction Reject, Invalid Device Code," for addresses where no device is configured on the subsystem.

- Boot Controller initiate status should be "Channel Busy, No Substatus."

- Initiate status for all operation codes (valid instruction codes) should be "Channel Busy, No Substatus." Thus, the channel will reflect "Channel Busy" until a terminate is received from the controller or the instruction is aborted by the EUS (hardware).

5.2 ADDRESSING

5.2.1 Device Addressing

Devices are connected radial and will be numbered 1-32 with physical device number. There will be no (ID plug) logical address plugs.

In DSS181/190 all devices will be addressable from the External User System (EUS). There will be no "S" device code plug denoting a device that cannot be reached except through special controller logic. It is important that all devices be accessible from the EUS in order to utilize the power of TOLTS in on-line testing and diagnosis of devices.

Device Identification

The physical device number and binary device identification number will be set by maintenance personnel at installation time. The numbers will be set from 1 through N (maximum 32) where N is the total number of devices.

For dual personality the devices will be numbered from 1 through N (maximum 16) on each CA.

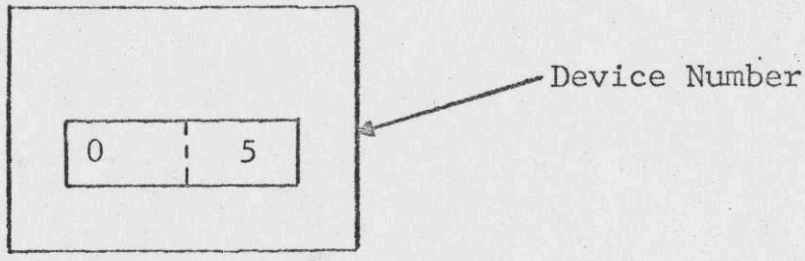
The DSU181 contains means to identify itself by "Type Number." This will be wired into the device in a semi-permanent fashion.

Six-Bit Binary Device Code

Six bits are provided by the EUS for specifying a device code. The six bit device code is the binary code of the two-digit decimal number (1-32) displayed on the device.

The controller will convert the six bit binary field device code into CA number and CA port number. A CA may have from 1 to 16 devices all addressable on-line. Device code 000000 is reserved for the controller.

The device code will be represented on the device as a two digit decimal number based on the binary device code.



Console Output Message

When outputting a device identification to the console typewriter, the software will have to convert the six bit binary device code into a two digit decimal number.

The physical device number visible on the device, binary device code and device identification number are the same and never change. The device number and port number need not be the same. The device identification number and port number (CA + device code) relationship is maintained in the controller. This relationship will be set up at initialization by the controller establishing which physical device is on which CA port. The relationship will be established on a device basis any time there is a power on indication from a device. The controller shall check the device identification number against the established relationship before any operation is performed. If the device identification number is different than previously established for the addressed CA port the controller shall terminate the command with "Device Attention," Device Off-Line.

CA Number	Port No. Internal CA and Device Code	Binary Device ID Number	6-Bit Binary Device Code	Physical Device Number 2-Digit Decimal
	Controller		000000	
0	00 0000	000001	000001	01
0	00 0001		000010	02
0	00 0010		000011	03
0	00 0011		000100	04
0	00 0100		000101	05
0	00 0101		000110	06
0	00 0110		000111	07
0	00 0111		001000	08
0	00 1000		001001	09
0	00 1001		001010	10
0	00 1010		001011	11
0	00 1011		001100	12
0	00 1100		001101	13
0	00 1101		001110	14
0	00 1110		001111	15
0	00 1111	010000	010000	16
1	01 0000	010001	010001	17
1	01 0001		010010	18
1	01 0010		010011	19
1	01 0011		010100	20
1	01 0100		010101	21
1	01 0101		010110	22
1	01 0110		010111	23
1	01 0111		011000	24
1	01 1000	011001	011001	25
1	01 1001	011010	011010	26
1	01 1010		011011	27
1	01 1011		011100	28
1	01 1100		011101	29
1	01 1101		011110	30
1	01 1110		011111	31
1	01 1111	100000	100000	32

Controller Table

Figure Device Code

CA Number	Port No. Internal CA and Device Code	Binary Device ID Number	6-Bit Binary Device Code	Physical Device Number 2-Digit Decimal
	Controller		000000	
0	00 0000	000001	000001	01
0	00 0001	000011	000011	03
0	00 0010	000101	000101	05
0	00 0011	000111	000111	07
0	00 0100	001001	001001	09
0	00 0101	001011	001011	11
0	00 0110	001101	001101	13
0	00 0111	001111	001111	15
0	00 1000	010001	010001	17
0	00 1001			
0	00 1010			
0	00 1011			
0	00 1100			
0	00 1101			
0	00 1110			
0	00 1111			
1	01 0000	000010	000010	02
1	01 0001	000100	000100	04
1	01 0010	000110	000110	06
1	01 0011	001000	001000	08
1	01 0100			
1	01 0101			
1	01 0110			
1	01 0111			
1	01 1000			
1	01 1001			
1	01 1010			
1	01 1011			
1	01 1100			
1	01 1101			
1	01 1110			
1	01 1111			

Controller Table

5.2.2 File Addressing

Initially standard GECOS software will use 64 word sectors on the DSS181. Disk packs may be formatted with either 64 word or 320 word sectors (1440 bytes). The controller will perform conversion of the continuous binary addresses received from the EUS to the noncontinuous cylinder-head sector addresses of the subsystem devices. Bit YY (Section 3.3.1) of the seek address will be set to indicate the addressing algorithm to be used by the controller. Direst "head," "cylinder," and "sector," addressing by the EUS will be used for all nonstandard sector sizes other than (64 or 320 words), including one sector per track. One sector per track may be addressed by either YY = 10 or YY = 11 but must decode to sector zero.

5.2.3 Multitrack Operation

For data transfers within a cylinder, the controller will automatically select the next sequential head on the access mechanism. This selection can be done without losing a disk revolution.

Data transfers to the EUS shall not be limited to a length equal to the sector length, but shall only be limited by the DCW tally, sector (block) count limit, defective tracks, (with no alternate assigned) unrecoverable error conditions, physical end of file, end of cylinder, and a seek address greater than that of the last addressable sector on cylinder 201 or 409.

5.2.4 Sector Size Options

Three sector sizes will be provided, basic 64 word for compatibility with existing disk systems, standard 320 word sector size and one sector per track. Sector sizes of 64 and 320 words will not be mixed on a given disk pack. 64 and 320 word sector packs may be mixed on a subsystem. One sector per track format may be mixed on either the 64 or 320 word formatted packs.

An error condition of MPC data alert status will be returned if the addressing specified does not match the sector size of the track.

The MPC data alert status will also be returned if sector size changes from one sector to another when reading multiple sectors or multiple tracks.

5.3 STARTUP

5.3.1 Channel Assignment and Configuration Control

Channel assignment and configuration control shall be accomplished by setting tables in the controller read/write memory. Basic configuration data will be entered on switches on the MPC maintenance panel and loaded into the tables during initialization. Under failure conditions of some module in the subsystem, these configuration tables will be changed in order to keep the data available and allow the subsystem to operate with only a reduction in throughput.

Configuration data for special configuration may be loaded into the configuration tables at start-up time after the controller has been booted. Loading configuration data from the EUS will be accomplished by using the special controller commands (refer to Section 3.22).

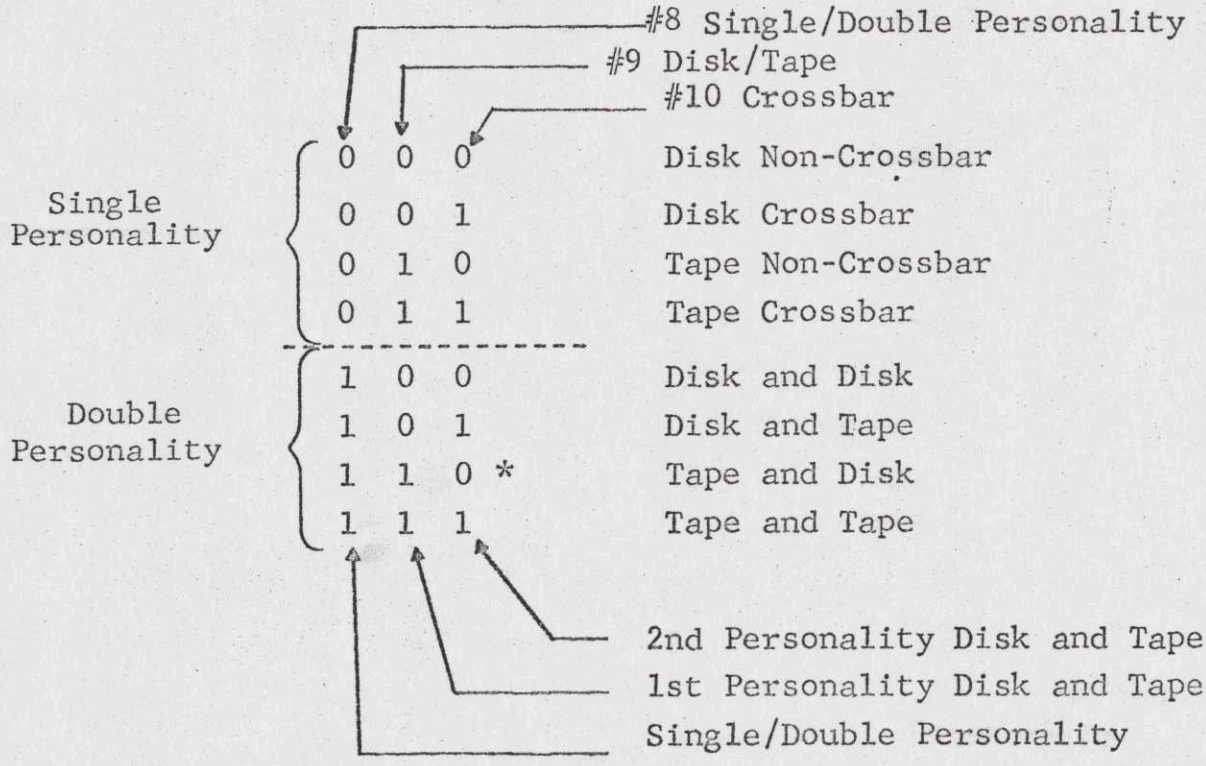
MPC Configuration Switch Allocation

The allocation of the configuration switches of the MPC maintenance panel is as follows:

Switch:
- 0 - ITR BLT Bypass
- 1 - ITR Loop Control
- 2 - LA to be used for booting:
  - 1 = LA on IAI Port 3
  - 0 = LA on IAI Port 2
- 3 - Number of LA's in Subsystem:
  - 1 = One LA (Port 2)
  - 0 = Two LA's (Ports 3 and 2)
- 4 - Inhibit Interval Timer Runout Detection
- 5, 6, 7 - Boot Device Identification
- 8, 9, 10 - Controller Configuration Definition
- 11, 12 - Not Allocated
- 13 - Main Memory Size: 0 = 1K Words, 1 = 4K Words
- 14 - Error Interrupt Safestore Bypass Control
- 15 - Used for Control Store Load (prototype, test only)

Note: Following "dc" initialization of a MPC controller, only PSI 0 of the LA defined by Switch 2 will be monitored for subsequent command from the central processor. Therefore only this PSI interface can be used for system-to-controller communication until the controller "personality" has been branched to as the result of a control store personality overlay command or a reset status command.

Controller configuration switches numbers 8, 9, 10 are defined as follows:



*Illegal Configuration

Configuration Switches

5.3.2 Subsystem Initialization

Initialization of controllers which have no personality firmware at startup and which will receive a personality overlay from the central system.

For configurations where startup has been loaded prior to MPC initialize time, the PSIA patch will be removed and MPC initialize will be provided from software by an initialize PCW. This allows software and/or T&D to set up the special interrupt channel (IOM channel #6) prior to MPC initialize and thereby have the capability to monitor the initialize and firmware overlay functions.

Initialization procedure:

1. The 6000 system is initialized from the system control center. No initialize is sent to the MPC as the PSIA patch is removed.

2. Startup (or T&D) is loaded through a CPI channel.

3. Software (startup or T&D) will set up mailboxes for the special interrupt channel (IOM channel #6).

4. Software will initialize the PSIA and the MPC by issuing the following two PCW's to logical channel #0 of the PSIA:

   - PCW to mask all logical channels within the PSIA and to initialize the MPC (bits 22-26 of the PCW = 37_8).

   - PCW to unmask logical channel #0 (bits 22-26 of the PCW = 00_8).

   The second PCW will be a "Normal" (non-T&D) PCW, and should be set up with associated control words pointing to an IDCW containing a Request Status command for device 0.

   The two PCW's can be in the same list.

   Unless software delays the time between PCW's the second PCW will be sent to the PSIA at a time when the MPC is not present (being initialized or is off-line executing the Basic Logic Test ITR test microprogram). This will result in a

Terminate Interrupt with power-off status being generated by the PSIA to software.

5. The MPC will initialize during which time Operational-In to the PSIA will drop.

6. The MPC will execute the Basic Logic Test Isolation Test Routine.

7. Upon completion of the BLT execution, the MPC will bring up the Operational-In line to the PSIA, and will generate a Special Interrupt, which indicates that the MPC is present and is ready to accept either extended ITR control store overlays, or the MPC personality control store overlay.

5.3.3 Controller Initialize Functions

Channel Initialize

The Channel Initialize function is a logical reset of one channel of the MPC controller, and occurs when the "Operational Out" line of the PSI interface to the controller reverts from the "Operational" to the "Nonoperational" state. (This is an indication that the external system has "gone away" due to either a power-off condition or an external system initialization condition.)

The occurrence of a "Channel Initialize" will cause the MPC controller to reset all activity associated with the physical PSI channel, including any allocation of devices, table entries, etc. Activity associated with any other physical PSI channel is not affected.

Controller Initialize

The occurrence of a "controller initialization" causes the entire MPC controller to be "dc reset." This type of reset is caused by any one of the following:

a. Actuation of the "Initialize" switch on the MPC operator panel.

b. An initialize signal from the MPC power supply during any MPC power-up sequence.

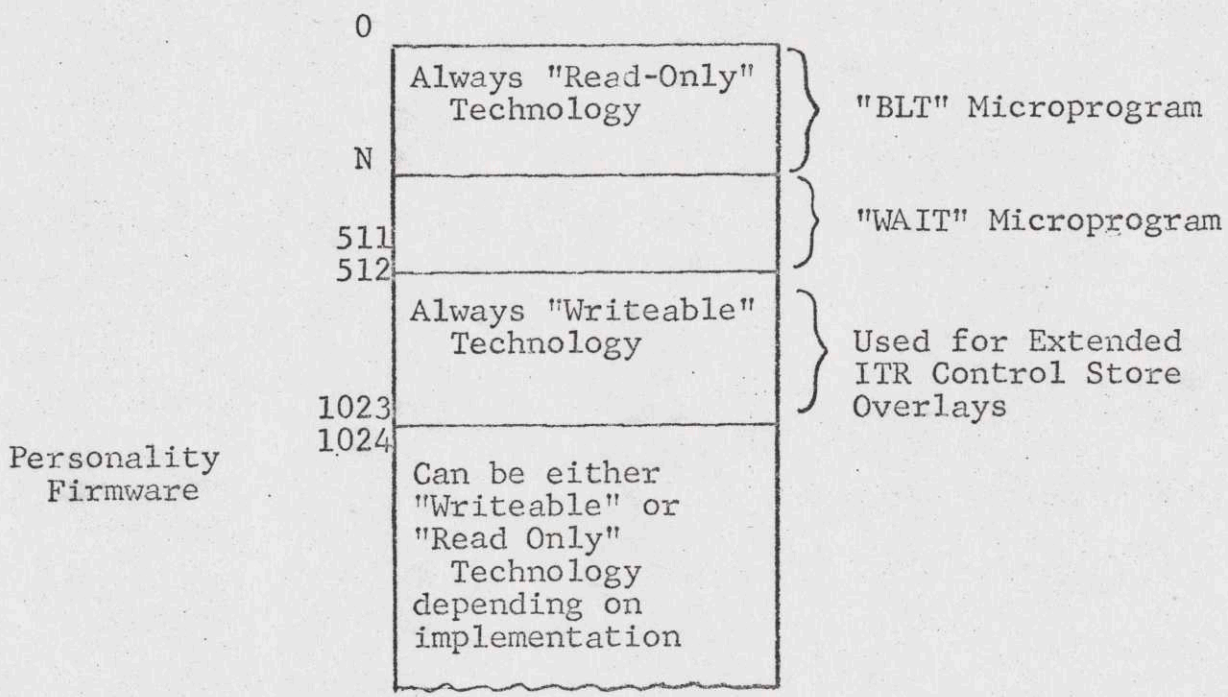
c. A remote initialize signal generated via the "SCAM" module (caused by actuation of the Initialize switch on the SCAM console).

d. A signal on the "Reset-Out" line of the PSI interface to the MPC (this signal is recognized by the MPC controller only if the "Operational-Out" line to the MPC controller is in the "operational" state).

Initialization by means of methos (a) or (b) results in the MPC controller being dc initialized and left in the halt mode, and requires actuation of the Start switch on the MPC operator panel or subsequent initialization by means of (c) or (d) to begin micro-instruction execution.

Upon actuation of the MPC Start switch, or immediately upon the fall of the initialization signal in the case of (c) or (d) above, microinstruction execution begins in the MPC controller starting at control store location 0, which is the starting location of the basic logic test (BLT) Isolation Test Routine microprogram.

The related Control Store memory map is shown as follows:



5.3.4 Control Store Bootload

Following dc initialization, the MPC controller begins microinstruction execution, starting at control store location 0 (except for initialization via methos (a) and (b) described above).

The BLT microprogram will be executed. This microprogram verifies that the basic logic of the MPC processor and link adapters is operational. If a hardware malfunction is detected during this test the BLT microprogram will cause the MPC to halt, with fault dictionary symptoms displayed on the MPC maintenance panel. (Configuration switch on the MPC maintenance panel can be set to cause the BLT microprogram to bypass the logic verification, and go directly to the WAIT microprogram.)

From the time dc initialization occurs until the completion of the execution of the BLT routine, the "Operational-In" line from the MPC controller to the IOM will be reset. This condition will cause any Channel Program initiated by System Software to the controller during this time to be terminated by the IOM with appropriate rejection status.

Upon completion of the execution of the BLT microprogram, the controller will time out for a minimum period of 2 milliseconds. (This is done to allow time for the System Software to "mask" logical channel 0, so the forthcoming Special Interrupt can be received from the controller.)

Following this timeout the controller will raise the Operational-In line to the IOM, and will generate a Special Status Storage and Special Interrupt to logical channel 0. The format of the Special Status Storage, as stored by the IOM in 6000 memory, will be as follows:

1 0 0	IOM Ch. No.	000 000 000	000 000 100	0XX XXX XXX
0	8	9 17	18 26	27 35

Note: If the Special Status Storage or Special Interrupt cannot be executed because the logical channel in the IOM PSI-Adapter is masked, the MPC controller will halt, and Operational-In line to the IOM will drop.

After issuing the Special Interrupt the MPC controller will start execution of the WAIT microprogram. This microprogram will monitor the PSI interface specified by switch 2 of the MPC configuration switches (on the MPC Maintenance Panel), and will detect the initiation of a channel program on this interface. (All other connected PSI interfaces will be ignored at this time.)

Note: Switch 2 set defines the WAIT routine will monitor PSI interface 0 of the LA connected to MPC Internal Port 3. Switch 2 not set defines PSI 0 of the LA connected to the MPC Internal Port 2.

The "WAIT" microprogram will recognize and act upon the following commands from the external user system.

a. Control Store Test Overlay: Op Code = 11_8
Device Code = 00_8

b. Control Store Personality Overlay: Op Code = 10_8
Device Code = 00_8

c. Reset Status Command: Op Code = 40_8
Device Code = 00_8

The reception of any command other than these commands will result in the MPC controller reverting to the halt state, and the Operational-In line to the IOM will drop. (This will result in a "power-off" status to the initiating 6000 system software.)

Control Store Test Overlay and Control Store Personality Overlay: Refer to Section 3.22 and 3.23.

Reset Status Command:

This is the standard Reset Status command as defined.

By using this command, 6000 System Software can interrogate an MPC controller after initializing the controller, to determine if the controller personality is resident to the controller. Upon receiving this command the WAIT routine will branch to the location in control store where the personality firmware should be resident. If personality firmware is present, it will respond to the Reset Status command normally. If personality firmware is not present, an error response (or no response) will result.

Although the WAIT routine can recognize the Reset Status command, the more normal sequence will be for the 6000 System Software to check a controller for "Personality Present" with a Reset Status command before initializing the controller.

Boot Procedure to be used by 6000 Startup Software

1. Check if controller requires rebooting.

   This step is optional.

   If startup software desires to check if the controller personality is loaded and operational, it can issue any legitimate command to the controller. If the controller responds normally, startup software can assume the controller is operational and does not require rebooting.

2. Initialize MPC Controller

   Startup software causes the controller to be "dc" initialized by issuing the "Reset and Mask LC's" PCW to the IOM PSI-Adapter. (PCW bits 21, 22, 23 = 111.)

   This PCW will cause an initialize signal to be sent to the MPC controller over the Reset-Out line of the PSI interface. In addition, all logical channels of the IOM PSI-Adapter will be masked.

3. Unmask Logical Channel 0

   Startup software unmasks logical channel 0 of the IOM PAI-Adapter by issuing any normal PCW to the PSI-Adapter.

   The purpose of this PCW is to insure that logical channel 0 of the IOM PSI-Adapter is unmasked, allowing the subsequent Special Status Storage and interrupt from the controller (signalling the "ready for boot" state) to be received. If logical channel 0 is not unmasked, the controller will detect an error sequence when it attempts to send the Special Status Storage, and will halt.

   The unmask PCW should be executed immediately following the reset PCW.* The MPC controller will delay for a minimum of 2 milliseconds following the completion of the initialize operation before issuing the Special Status Storage and Interrupt, to insure that Startup Software has adequate time to issue the unmask PCW. "Power-off" status will be the normal response to this PCW.

*Note that the Reset and Unmask PCW's can be queued together in the connect channel list, and issued via a single connect.

4. Issue the Control Store Personality Overlay Command

Upon reception of the Special Status Storage and Interrupt over logical channel 0, startup software will initiate the control store personality overlay command.

Execution of this command will result in the controller personality being loaded into the MPC control store. Upon successful completion of this command, the controller will issue a "Ready" status storage followed by a Termination Interrupt, and will then branch to the loaded personality and commenct normal controller operation.

If any error is detected during the overlay command execution, the MPC will revert to the halt state. This will result in "power-off" status to startup software indicating a retry must be initiated, starting with step 2 above.

Special Considerations

Illegal Commands:

Both the "Control Store Test Overlay" and the "Control Store Personality Overlay" command are considered illegal by the normal controller "personality"firmware. This implies that a controller must be "dc initialized" (reset-out line of the PSI) before the controller personality can be reloaded, or before ITR overlay procedures can be executed.

Restrictions on PSI Channel used following MPC Controller Initialize:

Following "dc" initialization of the MPC controller (via Reset-Out line) the controller will respond to command initiated only over the PSI interface specified by Configuration Switch 2 of the MPC maintenance panel. Therefore, 6000 software systems must be aware of the PSI channel defined by this switch setting and use that channel for all command initiations from the time the controller is "dc" initialized until the controller personality overlay is completed, and the normal controller personality is operational.

5.4 DEVICE RESERVE ALLOCATION AND ACCESS CONTROL RELEASE

There are two types of device reservation, implicit and explicit. Implicit reservation of a device to a logical channel is accomplished by selecting a device with a seek or restore command. The preseek command does not reserve the device. The device will remain reserved to the logical channel unit the data transfer command which follows the seek is terminated. When an error is detected during data transfer to or from a device, the device will be released automatically when the command is terminated. When EDAC is used and an error is indicated at terminate the device will remain reserved to the logical channel until a read EDAC register command is executed.

5.4.1 Explicit Device Reserve

This command is not required to enable access to a device. A channel program may be executed by an unseized, available device, but when the Explicit Device Reserve command is issued, that device can then only be accessed via the path (logical channel) that issued the Explicit Device Reserve command issued over the same path (logical channel). The only access that is available to a reserved device from other paths is to obtain summary status from that device.

5.4.2 Switched Channel Control

Either PSI channel of a switched pair LA may access any device on that channel by supplying the proper device number for the desired device. For switched channel configurations, access to any device will be given to the first requesting channel. In the crossbarred subsystem, the controller will attempt to access the device through either CA. If the CA is already in use, the requesting channel will be held busy until the alternate channel goes non-busy. The controller will then service the new request. (See also Section 5.4.5, independent systems sharing the same data base.)

5.4.3 Allocation of Devices

All devices that are on-line are addressable by the EUS. Nonallocated devices are very important in the operation of the subsystem in order to meet data availability requirements. Allocation of devices will be done by the operating system.

5.4.4 Devices Reserved from Allocation

The device allocation capabilities of GECOS and the on-line testing capabilities of TOLTS, allow the use of a versatile spare device philosophy. The allocation of devices to users, and the reserving of some devices for testing, or as spares, can be determined by customer needs -- based upon subsystem reliability predictions and operating statistics.

In most operating environments the important advantage of high data availability will lead to the reserving of one spare device. In such cases any one of the device numbers can be chosen as spare by the software not allocating that device number to production. In the event of a device failure, the data on the failed device can be brought quickly back into operation by deallocating the failed device and changing packs with the device designated as spare and then allocating it to production.

In order to achieve high data availability requires utilization of the spare device and requires the operating system to be able to exchange packs within or between job activities if a device fails and be able to continue the activity after the exchange has been made. The ability to exchange packs between a device that has failed and the device that was designated as spare (not allocated) applies to all types of files including removable files, perm files and perm files which contain operating system modules.

The ability to exchange packs has the following restrictions as presently implemented:

- The operator must initiate the function to exchange packs.
- The system must be able to retrieve all the necessary functions before an exchange can be attempted.
- At the time the exchange is requested, an unused device must be available within the set of drives assigned to the particular channel. By unused is meant a device which is configured and has been either released (not allocatable) or defined as removable and has not yet been allocated.

- Devices declared as shared with the Data Communications Subsystem via the Mass Store Link cannot be exchanged until the Mass Store Link has been notified, the device released from its allocation, and the new one assigned. This is a time consuming cycle which requires special interfaces. These interfaces must be established before this feature will be included.

If the exchange function cannot be accomplished, the operator must govern system activity. The following actions can be initiated depending upon system disposition:

1. Jobs using the device to be exchanged can be aborted until the device can be exchanged.

2. Device required to be exchanged contains the exchange modules (ST1). In this case, system performance will be extremely poor. The system can be aborted with a restart in mind and with a subsequent warm boot of the system performed. During the warm boot a new configuration card can be inserted via the card reader denoting the new device.

3. If a spare is not available the operator may release a device, it there is a device available to be released, so it can be used to perform the exchange function.

5.4.5 Shared Access

Shared access is a requirement of this subsystem.

It will be the responsibility of the EUS operating system (GECOS) to maintain the file space reservation and check this reservation status before executing a command from an alternate channel. File space may be a portion of a physical device or may bridge several devices. The EUS may use the lock byte capability provided in the controller to perform this function.

It will be the responsibility of the external user computer system to use the Reserve and Release commands if reservation is required at the device level.

The controller will provide Data Path Management (DPM) when shared or multiple access is required by the System/Systems.

5.4.5.1 Data Path Management for Shared Access by One EUS and Data Communications

For configurations (Figures 5.4.5.1a, 5.4.5.1b) where access to the data base is controlled by a single operating system.

The method that shall be used for data path management will be a combination of device pulling, firmware and software conventions.

The interface dialogue and signal discipline discussed in this section conform to the standard (DLI) Device Level Interface and is consistent with NPL.

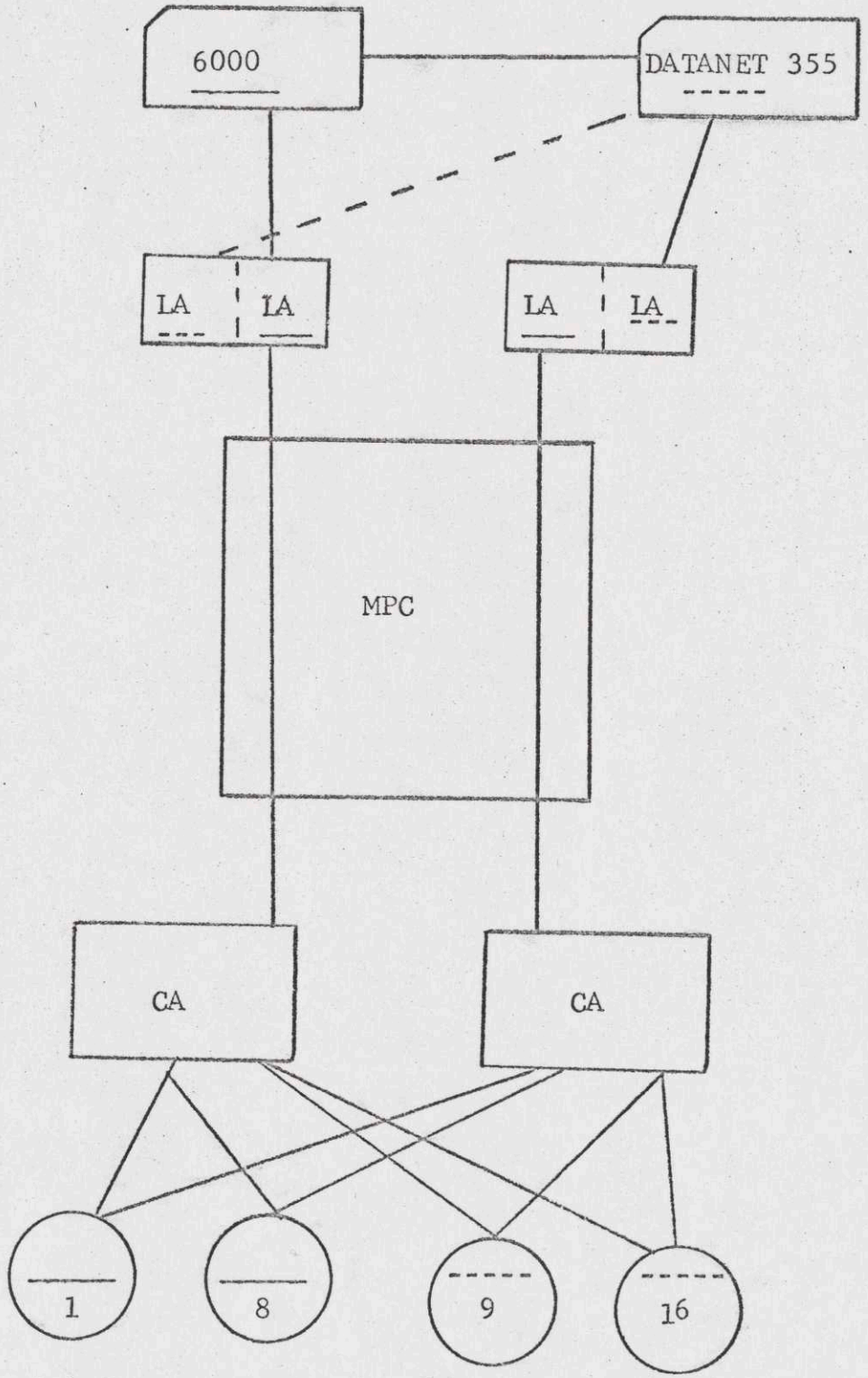


Figure 5.4.5.1a - Dual Channel Crossbar 2 x 16

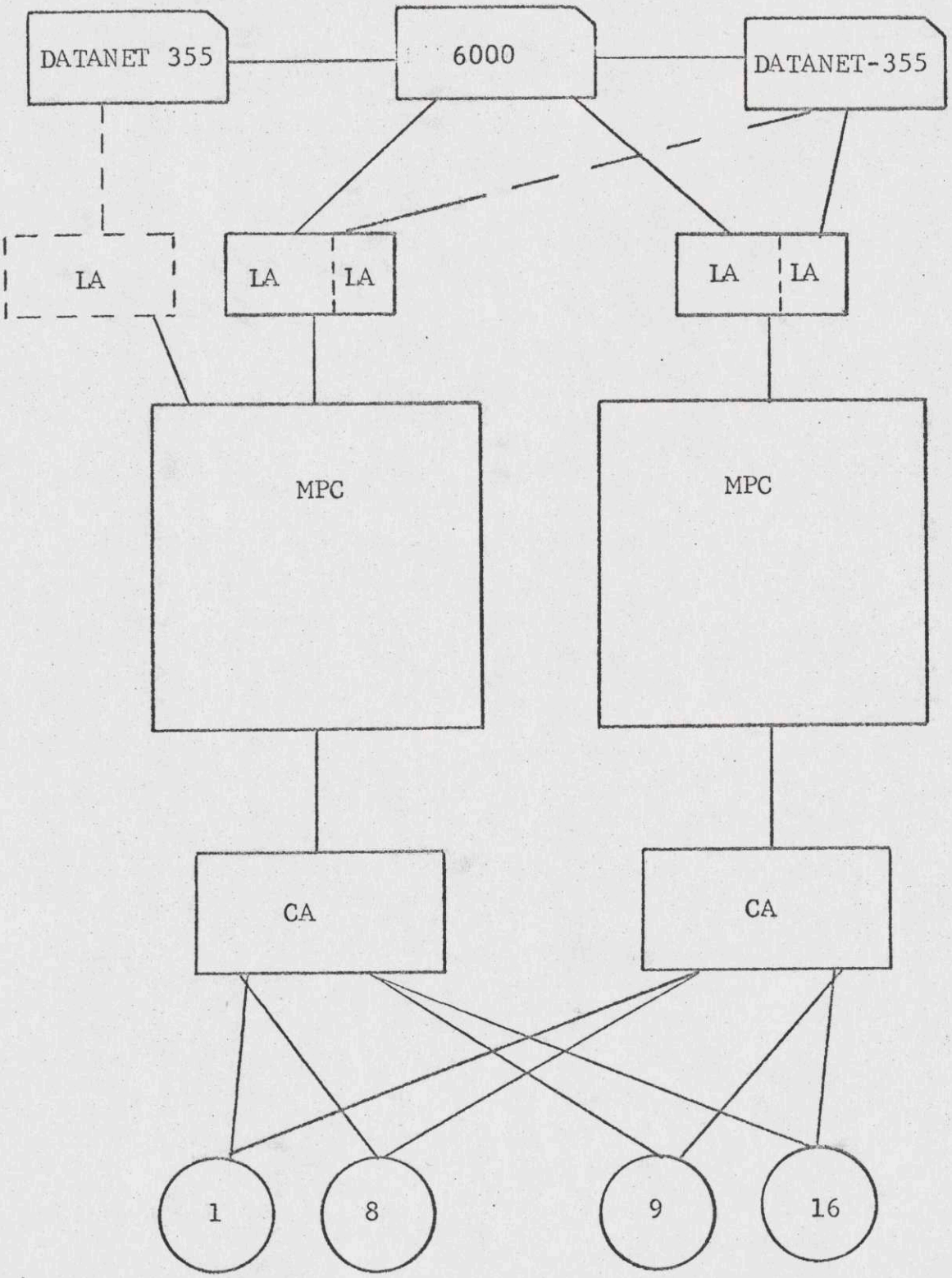


Figure 5.4.5.1b. Dual Channel Crossbar

The controller will use the summary status information as presently defined in the NPL DLI specification (refer Figure 5.4.5.1c) to handle Seek Completes, Pack Change and Alternate Channel in Control.

The controller will use the Block Multiplexing function (logical channels) to perform seek overlap and latency reduction for those commands queued in the controller.

The operating system may use the RCR command if desired. However, outstanding activities will be initiated when there is a logical channel available, even though no Seek Completes are indicated.

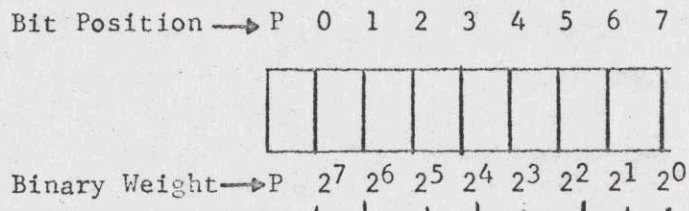
- For two controller (crossbarred) subsystems; each physical channel will have at least four logical channels.

- In two controller subsystems where each controller has two channels, the subsystem will look to the EUS, like 2(2X8)'s, that is two crossbarred subsystems.

- The operating system will issue all outstanding preseeks first. Preseeks will be executed first from the controller; that is, all outstanding before a data transfer is initiated.

- In single controller subsystems, the controller will service all outstanding DEN's before an RCR is executed. Therefore DATA in the device tables will be current when an RCR is received.

- When (2) controllers are configured in the subsystem, each controller will POLL the devices on the available CA/CA's approximately every second. Polling will establish the state of the device standby, busy, reserved and ready.



Bit 0 - Device reserved - The MSD is seized through the other port and is unavailable for functional operation through this port.

Bit 1 - Device seized - The MSD is seized through this port and is available for functional operation through this port.

Bit 2 - Device in Standby - The MSD is a Standby mode but can still accept all commands except those involving data transfer or head movement. Refer to the individual device specification for the definition of "standby."

Bit 3 - Positioner Busy - The MSD is executing a positioning command and the heads are in motion. This line is raised (where applicable) for seek, positioner offset, recalibrate, load and unload operations.

Bit 4 - DLI fault - The MSD has detected a fault condition of a type where the probability is low that the cause of the fault is located in the MSD. Diagnostic and recovery procedures should be directed equally at CA, interface, and MSD functions. Refer to Figures 4-3, 4-4 and 4-5 for the specific conditions that set this bit.

Bit 5 - Device protected - The MSD is write protected and will not execute any write commands.

Bit 6 - Device fault - The MSD has detected a fault condition of the type where the probability is high that the cause of the fault is located in the MSD. Diagnostic and recovery procedures should be directed primarily at the MSD.

Bit 7 - Device in diagnostic mode - The MSD is in the diagnostic mode.

Figure 5.4.5.1c. Summary Status Byte

Knowing the previous state of the device will allow the interpretation of pack change when DEN occurs because the device goes from Standby to Ready.

Knowing the previous state of the device will allow the interpretation of Seek Complete when DEN occurs because the device goes from Busy to Ready, if the CA is not busy.

Summary Status

The Summary Status Register in the device contains one byte of generalized information on the condition of the device, as shown in Figure 5.4.5.1c.

Whenever further definition of device conditions is required, detailed status must be requested.

Certain summary status changes initiate sense line signals (DEN's) to the CA: Figure 5.4.5.1d shows these indications.

The Summary Status Request command results in the transfer of the summary status byte from the device to the CA via the data lines. The Summary Status Request command may be issued to an unseized device.

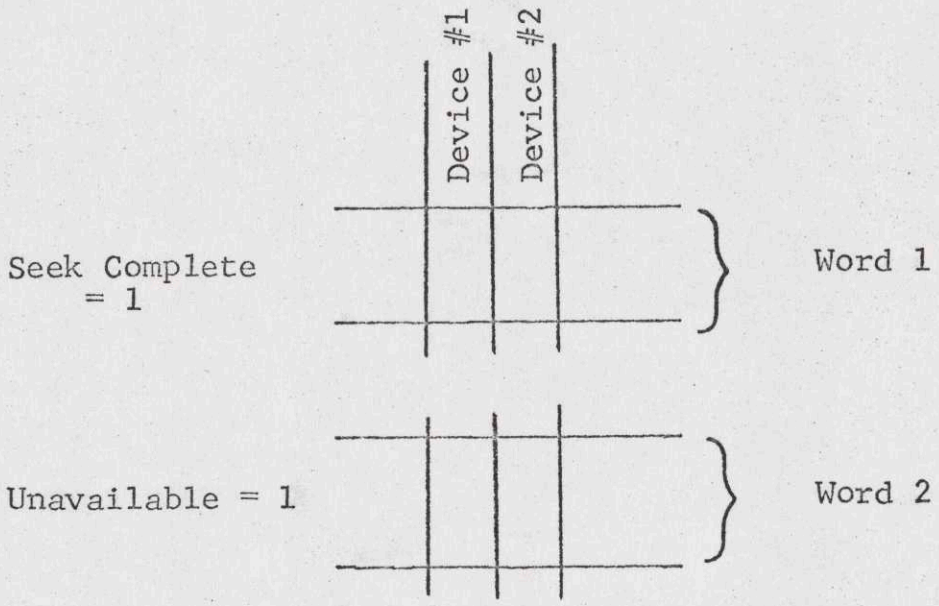
Seek Complete

- Seek complete will be reported in word number 1 of the Read Control Register command (RCR).

- Seek incomplete will be reported in word number 2 as device unavailable and seek complete in word number 1.

  The controller will automatically retry seek incompletes by issuing a recalibrate (restore) and reissuing the seek. If the device still has seek incomplete after three retries, then the controller will issue one more recalibrate and report seek complete and device unavailable in the RCR words.

- Device Busy positioning will be reported in word number 2; word number 1 will be reset.
- The controller will reset the Seek Complete in the device tables when a new activity is executed or when busy is received from the device as a result of polling.



- Seek Incomplete
- Standby
- Off-Line
- Device Busy

	#1	#2	
Positioning	0	0	Device is available - No information about Seek Complete.
Attention	1	0	Device is available and there has been a Seek Complete.
	0	1	Device is not available - Temporarily still busy positioning.

1 1 Device is not available

- Seek Incomplete
- Standby
- Off-Line
- Attention

Pack Change

- Pack Change will be reported as a Special Interrupt.
- Pack Change is sent to all PSI channels any time Summary Status indicates the device is not in standby and was previously in standby.
- Pack Change

  1. Device failure - Exchange pack between failed device and spare device.

     - GECOS must change physical to logical device relationship table.
     - GECOS or operator must notify Mass Store Link (355) that pack has been moved and the device should be deallocated, before the device comes back on line.
     - Operator may request to GECOS that the pack be moved. GECOS sets device in standby, device seized by controller. Therefore, channel which issued the standby device will get DEN.

2. Device returned to on-line state

   - The controller knows device was in standby and is now ready.
   - The other channels will receive pack change, SPI based on polling.
   - The controller sends SPI to all PSI channels, including Mass Store Link.
   - When a failed device comes back on line for T&D, the device will be explicitly reserved to TOLTS.

Alternate Channel in Control

- Device reserved to alternate channel will not be returned, except as an error condition.

  Normally the device will be reserved (siezed) at the 2 x 1 switch only until completion of the activities, Positioning, Read/Write.

Explicit Reserve

An Explicit Reserve command from the EUS will not normally be used, permanently reserving a device until a Release is issued. Alternate Channel in control will be returned only after Time Out has occurred.

This allows the controller to hold any activities for a given device until the activity has been completed. If an error condition leaves the device reserved, the controller will time out and terminate the command and return reserved to alternate channel status.

The reserve command will not be used as a vehicle for controlling shared access. However, the reserve command may be used where hardware data paths and controllers are shared (for availability), but the devices are used independently. Examples of this application are message switching or test and diagnostic where a device needs to be reserved to a logical channel for a series of activities.

A device will not be reserved to a channel at the device for any period longer than the transaction takes. Seek, read, write.

Devices will be reserved to the channel which issued the seek only during positioning time. If a read/write or other data transfer is not stacked behind the seek in the same channel program, then the device can be accessed by the other controller and the arm moved. The controller which issued the seek will keep a record of the seek to device and use this information to reject the read or write command if the read or write is not preceded by a seek on the same logical channel.

When a device is used in shared access, there will not be any alternate channel in control except as an error condition in which the device is reserved to a channel due to a fault and cannot release the device. The MPC will time out reserve to alternate channel.

5.5 CHANNEL PROGRAMS

5.5.1 Instruction Data Control Word (IDCW) Format

The IDCW is used to place instructions for peripheral devices at appropriate places in a DCW list accessed only by list services. Any distinction in interpretation of the fields is given in the description of that field. The whole IDCW (plus 4 zeros (5 bytes) is sent to the controller.

0 5	6 11	12 17	18 20	21	22	23	24 29	30 35	39
DEVICE INSTRUC-TION	DEVICE ADDRESS	IGNORE	111	MASK	CONT	MARK	CHANNEL INSTRUC-TION	CHAR OR RECORD TALLY	0000

The interpretation of these fields is as follows:

Device Instruction (Op Code)(Bits 0-5) -- This instruction is transmitted directly to the controller during the instruction sequence.

Device Address (Device Code)(Bits 6-11) -- This code is also transmitted to the controller during the instruction sequence. The first IDCW in a Channel Program will establish the device code and subsequent IDCW device codes will be ignored. This will make it impossible for a program to switch devices within a channel program (DCW list).

Bits 12-17 -- These bits are unused and unchecked.

Bits 18-20 -- Must be "111" -- If not, MPC controller reflects "channel status" of "011" in termination status message. (Channel status sent in bits 2, 3, 4 of byte 3 of MPC generated status message. See Section 5.2.)

Bit 21 -- Ignored.

Bit 22, 23 -- Continue/Marker Bits -- These two bits define the action to be taken by the MPC controller upon completion of the I/O operation:

Cont	Mark	
0	X*	The controller stores terminate status and causes a terminate interrupt at the end of this IDCW execution. This IDCW is the last IDCW in list.
1	0	This is not last IDCW in list. Upon completion of execution of this IDCW with Ready and no faults detected, the controller will issue a "Move Pointer" service code and obtain a new IDCW.
1	1	Upon completion of the execution of the IDCW, with ready status and no faults detected, the controller will store marker status and cause a marker interrupt, and then issue a "Move Pointer" service code to obtain a new IDCW.

Bits 24-29 -- Channel Instruction -- This field must contain one of the following codes:

00_8 -- Unit record transfer.

02_8 -- Peripheral action (nondata transfer; e.g., request status, release, restore).

*If continue bit equal zerc then the mark bit is ignored.

06_8 -- Multirecord instruction. Illegal for disk controller.

10_8 -- Single character record (e.g., write file mark). Single character contained in bits 30-35 of IDCW. Illegal for disk controller.

$2X_8$ -- Command Extension Modifiers.

$4X_8$ -- Special controller commands (refer to Section 3.2.2).

In order to provide this capability, the "Channel Instruction" field of the IDCW (bits 24-29) will be provided with a new code in addition to those currently defined:

Bits 24	25	26	27	28	29	Octal	Definition
0	0	0	0	0	0	0	Currently defined as "Unit Record Transfer"
0	0	0	0	1	0	02	Currently defined as "Peripheral Action"
0	0	0	1	1	0	06	Currently defined as "Multirecord Instruction"
0	0	1	0	0	0	10	Currently defined as "Single Character Record"
0	1	X	X	X	X	2X	New Definition, "Command Extension"
1	0	X	X	X	X	4X	Special Controller Commands

The controller will examine the "Channel Instruction" field of the IDCW. If the high-order two bits of the field are encoded "01" it will then interpret the four low-order bits as follows:

Command Extension Modifiers:

IDCW Bits 24-29

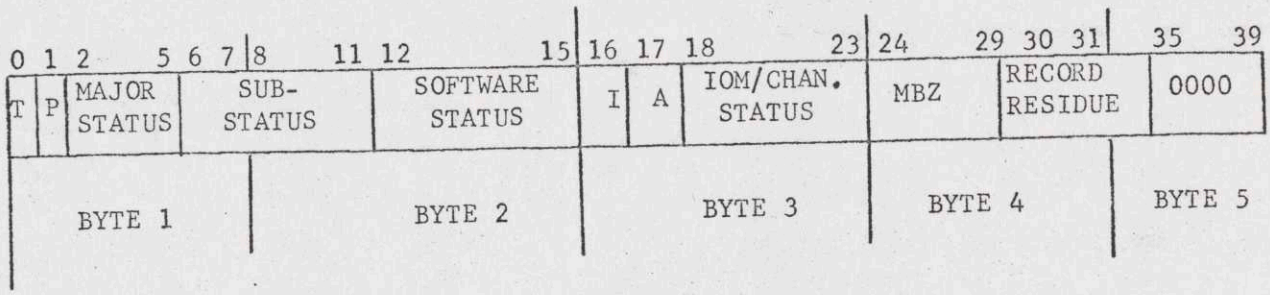
00 0001	21_8	Inhibit automatic retry
01 0010	22_8	Inhibit alternate track logic and end of cycle logic. • Read
01 0011	23_8	Special permission execution. • Read override RPS queue • Write override RPS queue
01 0100	24_8	EDAC Override DSS190, Check Character Override DSS181 • Write without EDAC and write the 7 bytes of error code as data from the EUS. • Read and transfer (EDAC) error code to EUS as data. • Read and transfer check character (CK), ID byte (ID), bit count (CNT), to EUS as data.
01 0101	25_8	Read and perform error correction on the data before transferring data to the EUS. (288 bytes record only.)
10 0000	40_8	Special Controller Command • Interpret the operation code as defined in Section 3.21.

The controller must check that this field is one of the above codes. In the event an illegal/undefined code is detected, the controller will reflect a "Channel Status" of "010" in the termination status message.

Bits 30-35 -- Record Tally or Character -- This field contains the character for a single character record (channel instruction field = 10), or the number of times the device instruction is to be re-issued by the controller (channel instruction field - 02 or 06). No specific checking required on this field.

5.5.2 Status Formats

The controller must recognize user faults reported to it by IOM central, and store this together with peripheral subsystem status, as shown in the description of the MPC status word as follows:



The status word format generated by the controller is compatible with the IOC-C format. The content of the IOM/channel status field is encoded differently. The fields have the following definitions:

Entry Present Bit (0) - Store as a one by the controller; software presently resets this bit to zero in EUS memory to indicate that the status has been examined.

Power Bit (1) - Is set to zero by the controller. Is set to one by the PSIA if the controller does not have its power on, or if there is no controller attached.

Major Status (2-5) - The major status from the controller. Zero when the power bit is one (and stored by PSIA).

Substatus (6-11) - The substatus from the controller. Zero when the power bit is one (PSIA action).

Software Status (12-15) - Stored as zero by the controller; is presently used by GECOS to indicate software detected errors to the slave program after the hardware has stored the status word.

Initiation Interrupt (16) - A one if the controller did not transfer data as a result of this instruction; i.e., this status occurred during an instruction sequence.

Abort Bit (17) - Stored as zero by controller. It is set to one by software if this transaction caused the program to be aborted.

IOM/Channel Status (18-23) - The IOM status field is divided into two independent 3-bit segments; bits 18-20 represent channel detected User Faults and bits 21-23 represent IOM central detected User Faults reported to the channel. These fields are formatted by the PSIA and sent to the controller for inclusion in the controller status word.

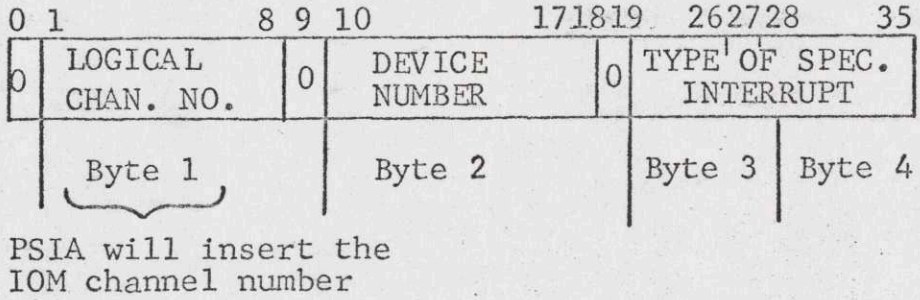
MBZ (25-29) - Unused at present; must be zero (MBZ).

Record Count Residue (30-35) - Residue record count for a peripheral action or multiple record instruction; these are defined as illegal in Section 5.5.1 and therefore stored as zero in all cases.

5.5.3 Special Interrupt Status

The IOM special interrupt channel 6 will be used by the controller to store special interrupt status.

SPI Status Word, Four Bytes stored in ASCII made by PSIA.



PSIA will insert the IOM channel number

Device Number "0" indicates the Special Status Storage concerns the MPC controller, as opposed to a particular physical device.

The following special status entries have been reserved for use by the controller (Device Number 0):

$(000)_8(000)_8(001)_8(000)_8$ - Issued by controller upon acceptance of Suspend command.

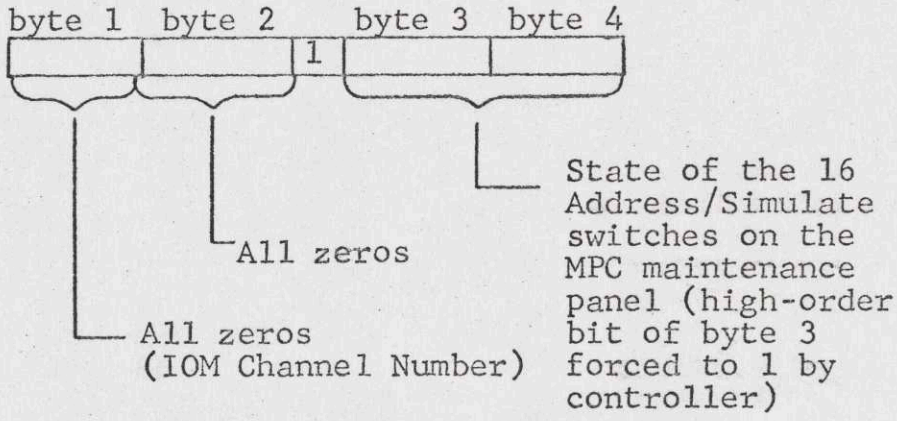
$(000)_8(000)_8(002)_8(000)_8$ - Issued by controller upon acceptance/execution of a Release command (terminates "suspend" state)

$(000)_8(000)_8(004)_8(000)_8$ - Initialize or ITR Boot Special Interrupt.

Generation of Special Status Storage via Operator Interrupt Switch

A "Special Status Storage" can be caused to occur from the MPC operator panel by actuation of the Operator Interrupt switch.

The format of this Special Status Storage will be as follows:



The Special Status Storage will be followed by generation of a Special Interrupt.

The Special Status Storage/Special Interrupt will be sent to all connected physical PSI interfaces over the logical channel that has the device reserved, or through logical channel zero if the device is not reserved on the physical channel.

Special Interrupt Type Codes:

Pack Change, Power On - 000 001

Device Released - 000 010

5.6 SPECIAL INTERRUPT PROCESSING

5.6.1 Device Event Notification

Device Event Notification (DEN) is a device related condition which may cause a Special Interrupt to be sent to the EUS. There are four categories of Event Notification to be considered:

- A Seek/Release/Preseek operation has been completed (busy to ready).
- A device reserved to one CA has been released (reserved or neutral).
- Power-on has occurred. Spindle on heads loaded (standby or ready).

If a device is connected to only one controller adapter, the MPC will receive only one event notification condition; however, if a device is connected to two CA's (dual port access) of one MPC, certain event notifications for the device will be reported over both CA's. When a device is reserved to a given CA, event notification will be reported to the MPC over both CA's.

5.6.2 Special Interrupts

The Special Interrupt is the means by which the controller reports Device Event conditions to the EUS. To minimize EUS overhead, the controller will selectively report Special Interrupts in the following manner:

a. Special Interrupts for Power-on (pack change), will be reported to all physical LA channels.

b. Device released to requesting channel causes a special interrupt to be sent only to the requesting physical EUS channel(s).

5.6.3 EUS Use of Multiple Seeks

The multidevice character of the subsystem and its relatively long access time (time required for seeks plus latency time), suggest the use of preseeks and multiple seeks to optimize subsystem performance. Such procedures imply that data services are not necessarily taken in the order in which the requests for service enter the queue within the controller.

To increase subsystem throughput, the EUS should position the device arm on the required cylinder prior to issuing the data transfer instruction. Thus, if there are multiple device I/O requests queued for the subsystem, the EUS should issue all possible seek operations prior to issuing the first data transfer. To determine which seek operations have been completed the EUS should interrogate the subsystem by the use of the Read Control Register instruction.

In response to this instruction, the subsystem reports, in part, seeks completed information for all devices. The data transfer commands can then be directed to those devices which have completed their seek operations.

Following each data transfer, new seeks may be issued (for new requests in the queue) and the Read Control Register instruction again is used to determine other seeks completed. In this manner, data transfer is overlapped with seeks on other devices with the corresponding optimization of throughput.

5.6.4 Command Stacking

A command stacking facility will be provided in the controller for use by the EUS. This feature enables the EUS to stack (per device) one additional reserving seek operation "on top of" a nonreserving seek type operation (preseek). Also, a device data transfer command, i.e., Read, Write, etc., may be stacked on top of a previous reserving seek (only) instruction. The Seek/Read/Write pair must be in the same channel program set up from one channel.

The reader should refer to Section 5.6.3, "EUS use of Multiple Seeks" for recommendations on the use of subsystem by the EUS for optimum performance.

When seek type commands are being stacked, only one command will be stacked on top of the command currently in (off-line) execution. Additional seek type instructions for the given device will be taken in sequence by the controller. Note that the Restore instruction may be stacked but the channel will remain busy until the Restore is initiated.

When the controller processes a stacked seek type request, it will initiate the positioning operation and unless the IDCW is chained, it will then terminate with appropriate status.

Data transfer instructions may be stacked on a reserving seek, immediately preceding. (Refer to Section 5.6.3.) In this case, the logical PSIA channel and device will remain busy until the arm has been positioned and the data transfer has been completed. Error recovery will cause the current IDCW to be re-executed.

All EUS command sequences, regardless of the stacking feature, are subject to the Instruction Reject, Invalid Instruction Sequence verification. For all valid combinations of Seek and Data Transfer instructions that are successfully executed, the status will be reported with the termination of the last instruction.

5.6.5 Block Multiplexing (BM) DSS190

Block Multiplexing on the PSI I/O channel of the IOM provides a facility for the subsystem to disconnect from a logical channel after an operation has been started such as a Seek/Data Transfer sequence and to reconnect the logical channel when the device is ready to begin a data transfer.

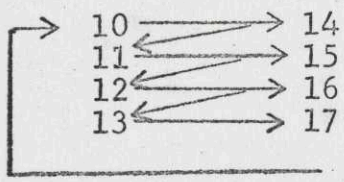
Standard configuration will be four logical channels per physical PSI with eight maximum. The logical channel numbers assigned to a physical channel are in numerical sequence. The logical channel number and device number relationship will be established when a connect is made and the channel program is set up.

The subsystem will accept and store up to one command sequence per logical channel or up to eight command sequences per physical channel. This capability when used with rotational position sensing allows the subsystem to service a greater number of I/O requests.

Standard single physical channel (four logical) will look to the EUS like a four-way crossbar. Standard dual simultaneous physical channels (four logical per PSI) will look like an eight-way crossbar.

Since the logical channel numbers are in sequence the EUS should set up an alternating channel table as shown below:

Assume logical channel number 10, 11, 12, 13 assigned to physical #1 and 14, 15, 16, 17 assigned to physical #2.



The controller will do latency reduction and change the logical channel number so that the correct DCW can be accessed in the IOM when data transfer starts. Each Seek Read/Write pair will be a different logical channel number. The lowest logical channel number will have the highest priority from the physical channel to the controller. A Command Extension Modifier can be set in the IDCW to notify the controller to take a particular command first and bypass latency reduction.

5.7 DISK PACK PROCESSING

5.7.1 Stranger Pack Processing (2314 or 3330 Formats with Nonstandard Sector Lengths)

The controller will be expected only to format "Stranger Packs" to the standard formats. There will be no facilities over the EUS interface for writing non-standard formats other than 64, 320 word or full track sectors. Reading nonstandard formats will be handled by a special command (read nonstandard sector size).

The accidental mounting and reading of a nonstandard format pack will not cause a failure of the controller. When it is determined that a pack is nonstandard, the controller will report MPC data alert "nonstandard sector size" status to the EUS. Nonstandard format pack will be identified as having a sector length other than 288 bytes, 1440 bytes or one sector per track.

Read Nonstandard Sector Size

This command will read an entire track starting with Home Address and will transmit counts, keys and data areas to the EUS. This command must be preceded by a seek with cylinder (CL), head (HH), but must be to sector zero. Only one track will be read, i.e., no head switching.

5.7.2 Formatting and Verification

Disk Pack Formatting and Verification

A software program will be provided for the customer to use in formatting and verifying disk packs. Verification, as used in this paragraph, means recording a selected worst case data pattern in each sector on the disk pack, reading, and verifying the data pattern(s). This program shall include recognition of defective tracks, assigning alternate tracks, if appropriate, and providing a record of these actions that is available to GECOS and accessible to the operator. This program shall accept as an input, vendor certification (defective track) data so that known defective tracks can be recognized.

Header Verification, Format Protect (Header Bypass)

The Header Bypass switch affects only the Format Track instruction. With the switch in the "OFF" position, the track address is verified before the track is formatted. To facilitate formatting a blank track, or a track that cannot be verified due to error conditions, the Bypass switch is placed in the "ON" position and the formatting is accomplished without track address verification. This switch is a software switch and is part of the format track command.

5.7.3 Defective Track Handling

The subsystem shall provide through use of the format track command, the ability to flag tracks on the disk packs magnetic surface, in four ways, as follows:

00 Good Primary

01 Good Alternate

10 Defective with Alternate Assigned

11 Defective with No Alternate Assigned

Defective track data obtained from disk pack certification procedures, will be an input to the Format Utility Routine. These marginal tracks may be recorded as defective, with no alternate assigned (11) and deleted from usage. or flagged defective with alternate assigned (10) and have an alternate track assigned.

5.7.4 Alternate Track Processing*

Once a track is formatted defective, (flagged in each sector header) and an alternate track address is recorded in the RO data field, attempts to write or read on the defective track shall result in the controller automatically seeking to the alternate address and performing the required data transfer operation. Following the completion of the data transfer on the alternate track, the controller shall return the actuator to the cylinder from where the defective track existed and continue the data transfer on the next rack. The EUS shall not be notified that this sequence of events occurred.

Should the controller detect a track with both track indicator bits set, the operation would be terminated with End-of-File, defective track detected, no alternate assigned status. Also, if the alternate address contained in the defective track were not a legal address, or Seek Incomplete or Header Verification error occurred when trying to access the alternate track the controller would respond with End-of-File defective track detected, no alternate assigned.

The execution of alternate track processing is under control of the IDCW and may be inhibited by command extension modifier (22). Refer to Section 5.5.1.

5.7.5 Cylinder End-of-File Processing*

When an end-of-cylinder condition is encountered, the controller shall automatically reposition the arm and continue with the data transfer on the next cylinder. If an error occurs in positioning to the next cylinder or it is the last user cylinder, the controller will terminate and return EOF last consecutive sector.

The execution of cylinder end-of-file processing is under control of the IDCW and may be inhibited by command extension modifier (22). Refer to Section 5.5.1.

*Not available on Initial DSS181

5.8 ERROR DETECTION AND RECOVERY

5.8.1 Controller Error Processing

Operations that detect certain device errors or recording surface errors may be temporary. The controller will automatically attempt to correct these errors three times before it reports the error to the EUS.

Automatic retry will be accomplished by moving the List Pointer in the IOM back to the last IDCW and retransferring the data records. (Refer to PSIA EPS-1, 43A177880).

If the error is corrected, the controller will continue as though no error had occurred. Thus, the error will be transparent to the EUS except for a longer than normal instruction execution time. The command will terminate with Ready Major status and substatus of 1, 2 or 3 indicating the number of retries performed. If the operation is still unsuccessful, the controller will complete the operation as necessary with the appropriate status reported to the EUS.

Those errors which are subject to three automatic recovery attempts by the controller are as follows:

1. Seek Incomplete as a result of any seek type instruction. Recovery will be attempted for Special Seek, Seek, Preseek.

2. Data alert header verification error as a result of sync failure, double index, or compare next count error. No repositioning will be attempted by the controller.

3. Transfer timing errors.

4. Check Character Alert on any read type instruction. This includes both count fields and data fields for all records.

5. Parity errors across the PSI (detected by the LA), or DLI.

6. EDAC (DSS190) error detected will be retried nine times before correction is indicated (3 normal, 3 head offset and 3 clock offset).

There will be a count of these errors maintained for each device. These counts will be available to the EUS through the Read Control Register command.

There is a possibility that imbedded DCW's (i.e., DCW's included in the data being read from the disk) can have an error in the address which will cause data to be sent to the wrong address in memory. Automatic retry by the controller should not be used for records which have imbedded DCW's since the retry if successful will put the data in the correct location but will not correct the locations where data was sent on the first transmission.

The execution of automatic retry is under control of the IDCW and may be inhibited by the command extension modifier (21). Refer to Section 5.5.1.

Automatic retry will be performed on each error type for each command listed below:

1. Seek Errors

   Seek
   Special Seek

2. Header Verification Errors

   Read
   Read ASCII
   Write
   Write ASCII
   Read Track Header
   Write and Compare

3. Transfer Timing Errors

   Read
   Read ASCII
   Write
   Write ASCII
   Write and Compare

4. a. Check Character Alert Data

      Read
      Read ASCII

   b. Check Character Alert Count Field

      Read
      Read ASCII

Write
Write ASCII
Read Track Header
Write and Compare

5. a. Parity Errors

Read
Write
Read ASCII
Write ASCII
Read Track Header
Write and Compare
Special Controller Commands

b. Invalid Seek Address

Seek
Preseek
Special Seek
Format Track

The basic MPC has built-in logic to detect internal hardware errors, such as parity errors on internal registers, parity errors on Main Memory (read/write) data, parity errors on microinstructions accessed from Control Store, etc.

The detection of any one of these internal hardware errors will result in the automatic execution of an error interrupt, which forces the MPC to branch to a fixed control store location, and establishes an "error interrupt in progress" state of the machine.

The microprogram which is automatically entered as a result of the error interrupt will first test the state of Configuration Switch #14 of the maintenance panel. If the switch is set, an immediate branch will be made to the Integrated Test Routine (ITR) module, located in the first 512 locations of control store. (The exact entry point to be determined during implementation.) Setting of Switch 14 therefore implies that the MPC controller will be put in the ITR mode upon the occurrence of an error interrupt.

If switch 14 is not set, the error interrupt microprogram will take the following actions:

a. Safestore in a fixed main memory area (to be defined) the current contents of all pertinent hardware registers.

b. Terminate all existing activity in progress, including device movement. This must be evaluated and implemented on a device type basis. The execution of an active channel program (DCW list) will be aborted.

c. Reset the error interrupt level, and return the controller to normal operation (i.e., waiting for command from central system).

The occurrence of the error interrupt will force the "Operation-In" line of the PSI interface to the EUS to revert to the "nonoperational" state. This line will stay in the "nonoperational" state until the "error interrupt in progress" state is reset by the MPC microprogram.

Detection of Error Interrupt Sequence by the EUS

The external indication that an MPC controller has taken an error interrupt is the dropping of the "Operational-In" line of the PSI interface to the EUS. This line will be down for the duration of time the MPC controller is in the "error interrupt in progress" state, which is a function of how many microinstructions must be executed by the error interrupt microroutine. As an order of magnitude, it can be assumed the "Operation-In" line will be down for approximately 15 microseconds. Repeated error detections will result in repeated error interrupts, and subsequent fluctuation of the "Operational-In" line.

The PSI Adapter in the IOM will detect the PSI "Operation-In" line dropping if a channel program (DCW list) is currently being executed for any one of the eight logical channels of the PSI. The adapter will generate a status storage, and mask the logical channel.

The MPC error interrupt occurrence will go undetected by the EUS however, if no logical channel of the PSI interface is active or initiated, during the time the "Operation-In" line to the IOM is down.

As described above, execution of an error interrupt sequence will result in the safestoring of pertinent registers in MPC main memory. This safestore area can be accessed by the EUS for diagnostic purposes as required, using the "Read Controller Main Memory" Special Controller command. (Refer to Section 3.3.21.)

5.8.2 Sector Limit Protect

The controller will perform file protection by limiting the data sectors available to the processing system following each Seek instruction. The sectors available per-seek-instruction shall be specified by the processing system and can very from 1 to N.

The desired sector count shall be sent to the controller during the execution of a Seek instruction. A sector count of zero shall be interpreted as the maximum number of sectors (4096) available.

5.8.3 Command and Address Integrity (Sum Check)

Check Character for EUS-Controller Communications

An additional check will be provided on certain types of data transmitted from EUS to the controller. Specifically, the data for format type operations, and all data transmitted to the controller with the special controller instruction should have a sum check type of check character in the last word transmitted. The data received shall be checked against the transmitted check character by the controller and the results compared. Only if the comparison is good, will the controller continue with the operation.

5.8.4 Error Detection and Correction Process DSS190

A 56 bit cyclic redundant check will be appended to count, key, and data fields. The generator polynomial is

$$P(X) = X^{56} + X^{55} + X^{49} + X^{45} + X^{41} + X^{39} + X^{38} + X^{37} + X^{36} + X^{31} + X^{22} + X^{19} + X^{17} + X^{16} + X^{15} + X^{14} + X^{12} + X^{11} + X^{9} + X^{5} + X + 1$$

This code has single error-burst correction capability with extremely high probability of detection for longer error bursts.

The encoding process utilizes a single 56-bit linear feedback shift register. Information is serially input to this register. At the completion of the information input the register contents serve as the check bits. Gating of the check bits out of the register necessitates feedback enable/inhibit control.

The decoding, that is, checking and error identification utilizes a high-speed decoding technique introduced by R. T. Chien. ("Burst-Correcting Codes with High-Speed Decoding", IEEE Transactions on Information Theory, pp. 109-113, January, 1969.) This technique deals with the factors of P(X) and the computational capabilities of the system.

$$P(X) = P_0(X)\ P_1(X)\ P_2(X)\ P_3(X), \text{ where,}$$

$$P_0(X) = X^{22} + 1; \quad \text{Order} = 22,$$

$$P_1(X) = X^{11} + X^{7} + X^{6} + X + 1; \quad \text{Order} = 89,$$

$$P_2(X) = X^{12} + X^{11} + X^{10} + X^{9} + X^{8} + X^{7} + X^{6} + X^{5} + X^{4} + X^{3} + X^{2} + X + 1; \quad \text{Order} = 13,$$

$$P_3(X) = X^{11} + X^{9} + X^{7} + X^{6} + X^{5} + X + 1; \quad \text{Order} = 23,$$

During a read operation data is serially input to the four linear feedback shift registers simultaneously. These registers are constructed according to polynomials $P_0(X)$, $P_1(X)$, $P_2(X)$ and $P_3(X)$. Utilization of the same 56 flip-flops use as a generator necessitates additional feedback control.

Upon completion of a field being read, including the 56 check bits the four check registers will contain $S_0(X)$, $S_1(X)$, $S_2(X)$, and $S_3(X)$; this is known as the syndrome. The following table shows the meanings of the $S_i(X)$ combinations:

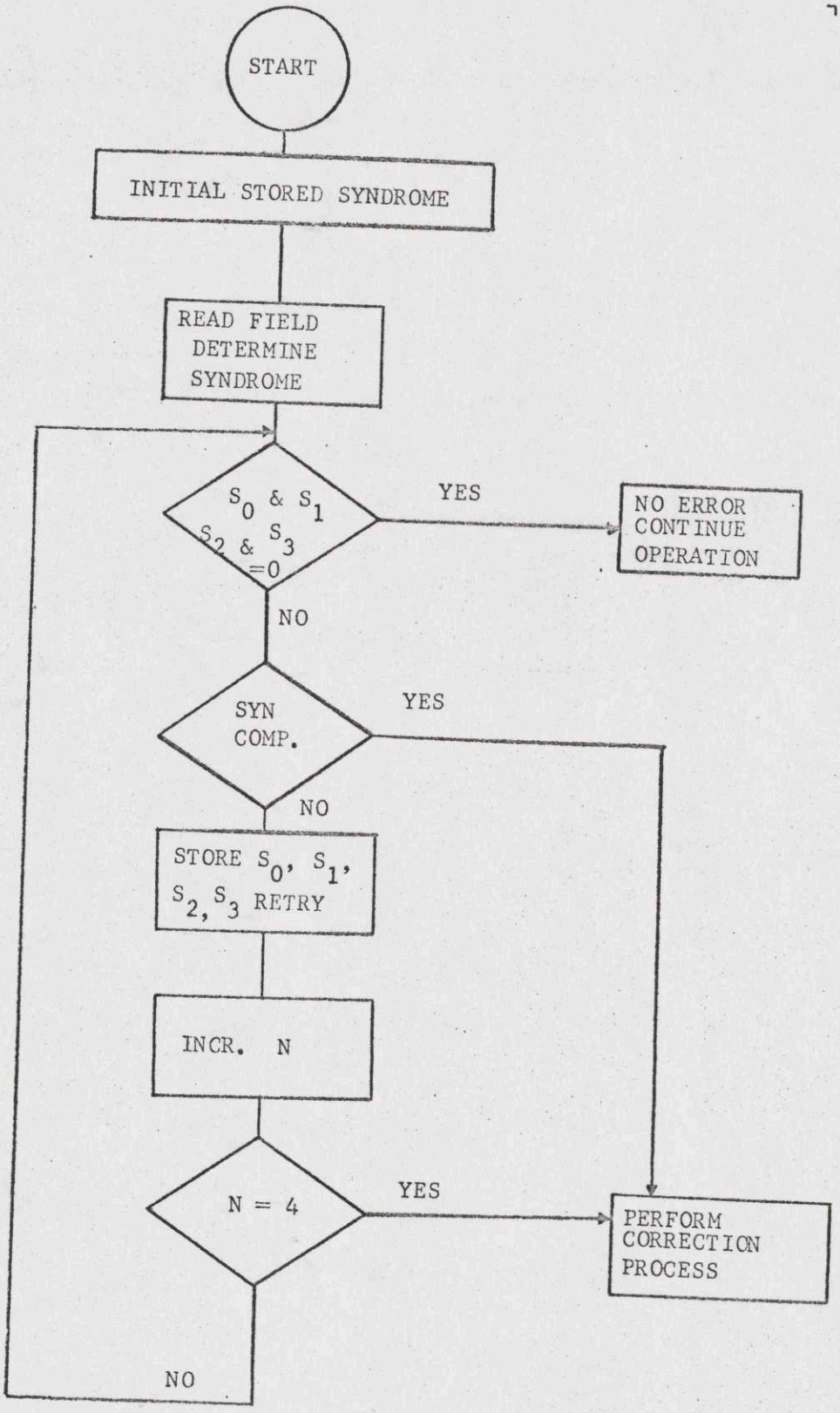
$S_0(X)$	$S_1(X)$	$S_2(X)$	$S_3(X)$	Comment
0	0	0	0	No error or non-detected error
0	≠0	-	-	Noncorrectable error
0	-	≠0	-	
0	-	-	≠0	
-	0	≠0	-	
-	0	-	≠0	
≠0	0	-	-	
≠0	-	0	-	
-	≠0	0	-	
-	-	0	≠0	
≠0	-	-	0	
-	≠0	-	0	
-	-	≠0	0	
≠0	≠0	≠0	≠0	Possible correctable error

Upon receipt of detected erroneous data the syndrome $S_0(X)$, $S_1(X)$, $S_2(X)$, $S_3(X)$ shall be saved. A retry shall be attempted and if an error is again detected comparison of the present syndromes with the saved syndromes will take place. If the two sets of syndromes compare a permanent error may be assumed and a correction attempt shall be made. If the syndrome miscompare, the syndrome of the first retry will be to attempt an error-free read. If the second retry is also detected as erroneous the process of syndrome comparison will repeat. If after four retries the errors persist and yield different syndromes a correction will be attempted. This retry procedure is flowcharted below.

The error identification process will be initiated by the MPC/CA. An 11-bit error pattern and r_0, r_1, r_2, r_3 will be transferred to the system for computation of error displacement and correction of appropriate data bits.

The details of displacement are shown below. It should be noted that the natural code length is 585, 442 bits. This must be incorporated in the calculations if displacement is measured from the MSB of information.

Initialization to zero of EDAC registers prior to encoding and decoding is required.


START
INITIAL STORED SYNDROME
READ FIELD DETERMINE SYNDROME
S_0 & S_1 S_2 & S_3 =0
YES
NO ERROR CONTINUE OPERATION
NO
SYN COMP.
YES
NO
STORE S_0, S_1, S_2, S_3 RETRY
INCR. N
N = 4
YES
PERFORM CORRECTION PROCESS
NO

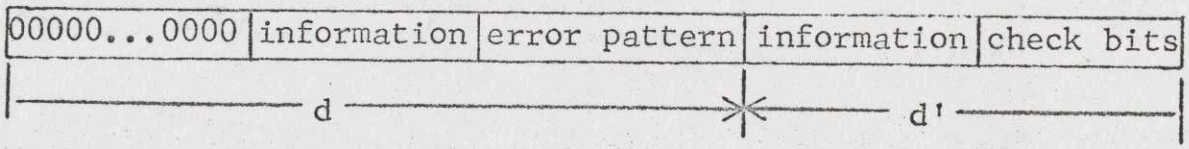
Error Identification

r_0 = number of shifts P_0 must undergo to transform s_0 to a correctable error pattern. (r_0 max = e_0)

r_1 = number of shifts P_1 must undergo to transform s_1 to a bit-to-bit comparison with the least significant segment of P_0. (r_1 max = e_1)

r_2 = number of shifts P_2 must undergo to transform s_2 to a bit-to-bit comparison with the least significant segment of P_0.

r_3 = number of shifts P_3 must undergo to transform s_3 to a bit-to-bit comparison with the least significant segment of P_0. (r_3 max = e_3)



$$d = [452387\ r_0 + 72358\ r_1 + 315238\ r_2 + 330902\ r_3] \bmod 585442$$

$$d' = [452387(e_0-r_0) + 72358(e_1-r_1) + 315238(e_2-r_2) + 330902\ (e_3-r_3)] \bmod 585442$$

General displacement equation:

$$d = A_0\ LCM(e_1,e_2,e_3)\ r_0 + A_1\ LCM(e_0,e_2,e_3)\ r_1 + A_2\ LCM(e_0,e_1,e_3)\ r_2 + A_3\ LCM(e_0,e_1,e_2)\ r_3$$

where,

$$A_0\ LCM(e_1,e_2,e_3)r_0 + A_1\ LCM(e_0,e_2,e_3)\ r_1 + A_2\ LCM(e_0e_1,e_3) + A_3\ LCM(e_0,e_1,e_2) = 1 \bmod 585442$$

with $e_0 = 22$, $e_1 = 89$, $e_2 = 13$, $e_3 = 23$

$$A_0(26611) + A_1(6578) + A_2(45034) + A_3(25454) = 1 \bmod 585442$$

yielding a minimum positive set: $A_0 = 17$, $A_1 = 11$, $A_2 = 7$, $A_3 = 13$.

5.8.5 Statistics Gathering

The controller will accumulate tallies of operating activity and error statistics to facilitate the diagnosis of subsystem problems before they become subsystem failures. Refer to Section 3.15 for a list of tallies maintained by the controller.

The EUS shall be able to access the statistical tables with a Read Control Register command, Section 3.15, and additionally will undoubtedly find it necessary to accumulate statistics of its own in order to evaluate subsystem performance.

5.8.5.1 Errors Logged on a Controller Basis

There are eleven counters which are maintained in the controller main memory. The contents of these counters are available to the external user system by proper usage of the Read Controller Main Memory command. Also, the EUS may load these counters with any count by using the Write Controller Main Memory command. The location of these counters will be specified during the design implementation.

5,8.5.2 PSI Parity Error Counter

This one-byte counter records the number of activities containing an error while transferring information across the PSI from PSIA to LA. An activity includes either an IDCW transfer or a record transfer. There are four of these counters, one for each possible PSI.

5.8.5.3 OPI/PSI Counter

This one-byte counter records the number of times that the OPI line on the PSI is dropped as the result of unsuccessful communication of the LA with the PSIA. The failure may be in the LA (where it appears as a PSI - related fault), in the PSI cable, or in the IOM/PSIA.

There are four of these counters - one for each possible PSI.

5.8.5.4 OPI/IAI Counter

This one-byte counter records the number of times that the OPI line is dropped due to either IAI faults detected by the LA, or LA faults which appear as IAI faults.

There are two of these counters in the controller - one for each possible LA.

5.8.5.5 Error Interrupt Counter

This one-byte counter records the number of times that the MPC executed an error interrupt.

This is a single counter for the controller.

6. RELIABILITY AND MAINTAINABILITY

(Refer to the DSS181/DSS190 Subsystem EPS-1 (43A239851) Section 6 for Reliability and Maintainability information.)

7. GENERAL DESIGN REQUIREMENTS

(Refer to the DSS181/DSS190 Subsystem EPS-1 (43A239851) Section 7 for General Design Requirements.)

DSC181/DSC190 CONTROLLER
EPS-1

SIGN-OFF SHEET

PREPARED BY: E. W. Herron 6/18/71
E.W. Herron Date
Advanced Subsystem Design

Reviewed by: Fred Strout 6-18-71 (9-20-71 F.D.S.)
F.D. Strout, Manager Date
Advanced Subsystem Design

Reviewed by: Gordon R. Williams 6/22/71
G.R. Williams, Manager Date
Systems Design Engineering

Reviewed by: T. J. Beatson 6/22/71
T.J. Beatson, Manager Date
Systems Software Design

Reviewed by: L. I. Wilkinson 10/25/71
L.I. Wilkinson, Manager Date
Systems Engineering

Reviewed by: J. R. Guilford Nov. 18, 1971
J.R. Guilford, Manager Date
I/O Design Engineering

Reviewed by: R. L. Mynatt 10/29/71
R.L. Mynatt, Manager Date
645/MPC Design Engineering

Reviewed by: R. L. Ruth 11/19/71
R.L. Ruth, Manager Date
Computer Design Engineering

Reviewed by: C. A. Conover 6/22/71
C.A. Conover, Manager Date
Advanced Systems Engineering

Reviewed by: C. W. Dix 11/14/71
C.W. Dix Date
Director of Engineering
I have one reported Disc Engineering constraint
CWD

Reviewed by: B. B. Krekeler 6/25/71
G.B. Krekeler, Manager Date
Language & Data Mgmt. Sys.

Reviewed by: E. F. Marshall 6/23/71
R.F. Marshall, Manager Date
Memory & Circuit Engrg

Exchange freight mode classification
Reviewed by: R. F. Stevens 71/11/16
R.F. Stevens, Manager Date
Operating Systems Engineering

Reviewed by: P. F. Straka 6/23/71
P.F. Straka, Manager Date
Systems Engrg Maintainability

Reviewed by: P. G. Smee 6/23/71
P.G. Smee, Manager Date
Product Engineering

Reviewed by: J. D. Hann 6/25/71
J.D. Hann, Program Director Date
Series 6000

Reviewed by: Concurrence received by phone, E. W. Herron 11/16/71
G.W. Muller, Manager Date
Disc Engineering

Reviewed by:

Approved by: D. K. Lundberg 6/25/71
D.K. Lundberg, Associate Date
Director-Product Marketing