PRELIMINARY

Honeywell

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INFORMATION
SYSTEMS INC.

TITLE: 645F/6100 SCU EPS I
DRAFT

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REVISION RECORD

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645F/6100 SCU EPS-I (DRAFT)

NOTE: Until such time that the requirements for the 645F System Controller can be incorporated into the existing System Controller EPS-I, the unique requirements for the 645F System Controller will be initially distributed as Appendix A to 6000 SCU EPS-I, 43A219602.

Where conflicts exist between the present EPS-I and Appendix A, this Appendix shall apply.

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A.1.0 GENERAL DESCRIPTION

A.1.1 Scope

This appendix shall apply as a performance requirement of the system controller when upgraded to operate with the 645 Follow-On or 6100 Subsystem.

A.1.2 Description

The System Controller will have the following features which are in addition to or different from the present 6000 System Controller:

- The System Controller shall contain a 52 bit elapsed time clock which has a source oscillator frequency of 1 microsecond and turn over of 142 years. The most significant 36 bits of the clock shall be settable from the maintenance panel with the design including the necessary safeguards to prevent accidental setting. The least significant bit shall be data bit 71 while the most significant bit shall be data bit 20 (See Fig. A1).

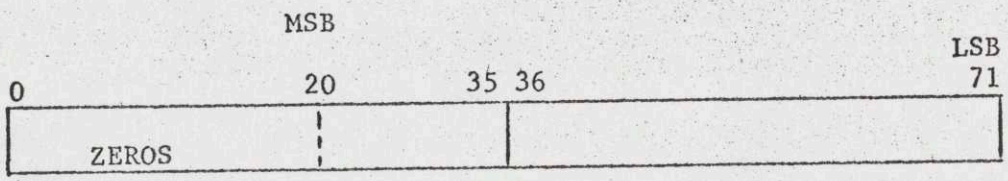

Fig. A1 Clock Data Field

The clock shall be readable via the Read System Controller Registers (RSCR) instruction with an address field of 40 octal. (Ref. Section 2.6 of this EPS-I).

- Lock Function - The System Controller will have a control flag designated "Lock". Two new command codes 40_8 Lock (Read Single Precision) and 60_8 Unlock (Write Single Precision) will be

added to the legal command field. The Lock Control Flip-Flop will be set each time a command code at 40_8 is received by the System Controller. When set, this flag will cause the System Controller to postpone all active module requests that do not have their "Key" line enabled. The Lock Flip-Flop will be reset when a command code of 60_8 (unlock) is received with the key line enabled, or the time out period has been exceeded. The time out period shall be about 20 micro seconds. It is assumed that the active module implementation of the Lock/Unlock commands will be such that an unlock command (60_8) must always immediately follow a "Lock" (40_8) command. The Lock/Unlock commands when used in conjunction with the key line provide the active modules with the ability to perform a read cycle and a write cycle without an interferring cycle gaining access in between. (Ref. Sections 3.1 and 3.4 of this EPS-I).

Must be sure CPU will always Unlock eventually occurs

- The System Controller initialize logic will initialize the Port Mask Register to the "one" (ports enabled) state. The configuration panel Port Enable Switches will override the Port Mask Register when in the ON or OFF position. The register will control when the Port Enable switches are in the Program Control Position. (Reference Section 3.3 of this EPS-I).

- Refresh Function - The System Controller will contain the necessary logic to respond to an asynchronous refresh request signal from a MOS type store unit. The response will take the form of granting the store unit a cycle time to complete the refresh function.