Honeywell

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INFORMATION
SYSTEMS INC.

TITLE: No. 43A239854

ENGINEERING PRODUCT SPECIFICATION, PART 1
6000B INPUT/OUTPUT MULTIPLEXER (IOM) CENTRAL

REVISION RECORD

REVISION LETTER	DATE	PAGES AFFECTED	APPROVALS	AUTHORITY

1.0 GENERAL DESCRIPTION

The IOM Central controls access to storage for the various channels of the IOM by providing appropriate services to the channels, one at a time.

The IOM has eight generic types of channels:

- Data Channel
- Connect Channel
- Fault Channel
- Wraparound Channel
- Bootload Channel
- Snapshot Channel
- Scratchpad Access Channel
- Special Status Channel

Each channel has assigned to it four (4) 36 bit mailbox words. The use of these words vary with the type of channel. The words are listed below in the order that they appear in a memory map (lowest address first) and the definitions appear later in the text.

List Point Word (LPW)
List Pointer Word Extension
Status Control Word (SCW)
Working Storage for Data Control Word (DCW)

The data channels are "payload" channels; they are responsible for information transfer with all external peripheral devices and adapters. The other seven types of channels are "overhead" channels; they perform specialized internal functions necessary for successful operation of the IOM.

The IOM Central includes a scratchpad storage to hold various channel control words. The scratchpad is a high speed store accessible to the IOM Central and the scratchpad access channel. It is used to reduce the time required for performing various services to channels, by storing control words for from 16 to 32 payload channels. The LPW, LPW extension and DCW (see paragraph 3.2) for each channel will normally be stored in scratchpad memory, unless scratchpad is not provided for a particular group of channels (see paragraph 2.2.2).

Following the introduction to the various functions, a description of a typical operation is included at the beginning of Section 3.0.

1.3 SCOPE OF THIS DOCUMENT

This document defines the functional and operational characteristics of the IOM Central and its overhead channels. This document does not define the various payload channels beyond the characteristics of their common interface to the IOM Central. For information about the payload channels refer to the Engineering Product Specifications for these channels.

1.4 APPLICABLE DOCUMENTS

EPS-1, 6000B System (43A239924)

EPS-1, 6000 System Controller (43A219602)

EPS-1, IOM Common Peripheral Channel (43A219605)

EPS-1, 6000B IOM Direct Channel (43A239853)

EPS-1, IOM Peripheral Subsystem Interface Adapter (43A177880)

EPS-1, Console Channel Adapter (43A232500)

General Design Requirements for 655/355 (43A177851)

655 Maintainability Design (43A219617)

1.5 DEFINITIONS

1.5.1 Tally Runout (TRO)

In this document, a tally runout is a fault, defined as an exhausted LPW tally field (the contents of LPW bits 24 - 35 equal to zero), and LPW bits 21 and 22 set to 0, 1, respectively, at the time the LPW is taken from its mailbox in core or in scratchpad.

1.5.2 Pre-Tally Runout (PTRO)

A pre-tally runout is defined as a tally in either a DCW or an LPW which will be reduced to zero by the current channel service (DCW during data service, LPW during list service).

1.5.3 List Pointer Word (LPW)

A word containing an address "pointing" to a list of control words, either DCW's or PCW's. NOTE: Only an LPW for a Connect Channel may point to a PCW.

1.5.4 Data Control Word (DCW)

A word containing an address indicating the first or current word of data in a list of data. IDCW, TDCW, IOTP, IONTP, and IOTD are variations of DCW's.

1.5.5 Peripheral Control Word (PCW)

A word containing the number of the channel to be connecting and, for CPI, an instruction or operation to be performed by a peripheral subsystem.

1.5.6 Status Control Word (SCW)

A word containing an address indicating the first or current empty position in a list of status words used by a particular channel.

2.0 FUNCTIONAL CAPABILITIES

2.1 BASIC CHARACTERISTICS

2.1.1 General

The 6000B IOM will have the following characteristics:

- The ability to operate in a GCOS III mode with no Operating System or Slave software programming interface difference over the 6000 IOM design.
- The capability of operating in an Extended GCOS, MULTICS, or VMM mode where addressable memory space to 2^{24} locations is possible.
- The ability to change MODE by a manually operated configuration switch.
- The capability of interfacing up to eight (8) 6000B or 6000 System Controllers. There shall be one three position switch for each pair of ports. The following pairs of ports may be interlaced:

  Ports A and B
  Ports C and D
  Ports E and F
  Ports G and H

  The interlace mode may either be two (address bit 22) or four (address bit 21) word blocks.
- Provision for control word scratchpad storage for at least 24 payload channels.
- The ability to indicate with a configuration switch per port, that either all or half of the address range assigned to a memory port is available.
- The ability to support word or 9 bit character channels.

2.2 CONFIGURATIONS

2.2.1 Basic IOM Central

The basic IOM Central has one connect channel, one system fault channel, one wraparound channel, one snapshot channel, one bootload channel, one scratchpad access channel, and one special status channel. No payload channels or system controller ports are included. Space is provided for 36 payload channel boards, one of which is used for the wraparound channel.

2.2.2 Options

- From one to eight Ports to connect to 6000B or 6000 System Controllers may be added.
- Provisions for adding space for 19 additional payload channel boards to the basic IOM.
- Payload Channels: The following payload channels may be used with the IOM:

  6000B IOM Common Peripheral Channel (2 board spaces per channel required)

  6000B IOM Peripheral Subsystem Interface Adapter (3 spaces per channel required)

  6000B IOM Direct Channel (1 board space per channel required)

  6000B IOM Console Channel Adapter (3 board spaces required for each two channels)
- Scratchpad: Scratchpads may be supplied for storage of control words. Scratchpads are added in groups of 16 channels. A maximum of 32 payload channels may be handled by the scratchpads.

  When scratchpad modules are used, the channels whose control words are stored in the scratchpad will be determined on the basis of channel number, as follows:

  The first optional scratchpad module is used for storage of control words for channels numbered 010_8-027_8.

  The second optional scratchpad module is used for storage of control words for channels numbered 030_8-047_8.

2.4 CONCURRENT OPERATION

The time required for the IOM Central to perform an indirect data service (and consequently for other types of service) is intended to be substantially less than the time required for the requesting channel to accumulate or disperse the data. As a result, the IOM Central will be time shared by a number of channels operating concurrently. The IOM Central provides appropriate services to the channels, one at a time. Such concurrent operation of channels will be successful only if the fraction of available service time used by each channel, summed over all concurrently operating channels is less than one, and if there is a sufficient amount of buffering in each concurrently operating channel.

2.5 DATA FORMATS

An indirect data channel may work with byte sizes of 9, 36 or 72 bits. The IOM Central is capable of packing successive 9 bit bytes received from an indirect data channel into successive 9 bit byte positions, left to right, in a 36-bit word. It also may unpack 9 bit bytes from successive byte positions in a 36-bit word, left to right, for transmission to an indirect data channel. The Common Peripheral Channel will perform its own packing and unpacking.

Evolving system configurations and peripheral data transfer rates emphasize the need to fully utilize the available 6000B system controller interface, not only to maximize IOM thruput but to minimize I/O interference with storage access by system processors. The use of a 72 bit interface can result in a thruput increase when operating with a channel capable of buffering the 72-bit data width. The IOM Central design will incorporate the 72-bit data transfer capability.

Thus for indirect data channels the data in core store can be formatted as

- one 9-bit character per access
- one 36-bit word per access
- two 36-bit words per access

The formatting chosen for programming purposes must be consistent with the character size used by the indirect data channel. The 3-bit codes shown in the following formats identify the various character positions within a word. Each type of indirect data channel determines which of the three formats can be used. A 36-bit channel will access one 36-bit word per access, and a 72-bit channel may access either one or two 36-bit words per access, depending upon the address and tally requirements.

3.0 SOFTWARE AND CUSTOMER INTERFACE REQUIREMENTS (continued)

When the channel has determined that its peripheral is receptive to the instruction, the channel will request the IOM to perform a list service, using the LPW in channel 020 core mailbox to obtain a DCW. The DCW is checked for several conditions, including absolutizing the address when specified, and placed in either* the core or scratchpad mailbox for channel 020. This particular DCW should be either an IOTP or an IOTD (I/O Transfer and Proceed or I/O Transfer and Disconnect). The LPW is updated and placed in both core and scratchpad mailboxes for channel 020. The channel now requests a data service of IOM, specifying an indirect data load. The IOM uses the DCW from the scratchpad mailbox for channel 020 to obtain the first word or word pair from the data area in core specified by the DCW. The address and tally fields are updated and checked, and the DCW returned to the mailbox in core* or in scratchpad. The channel sends a release to the peripheral when its output buffers are full.

The peripheral will subsequently request the data to be sent over its interface data lines. By a succession of Data and List Service requests, the channel will continue to supply data until one of the following types of events occur: (1) An abnormal status condition such as a parity error; (2) The peripheral has reached a termination condition; (3) All DCW's in the list including the final IOTD are exhausted.

Anything which causes the end of operation with the peripheral, with the exception of a system fault, will cause the channel to request the IOM to do a status service. Using the Status Control Word for channel 020, the IOM will store status in the status queue indicated by the SCW, update the SCW and restore it to the core mailbox.

Following the status service, the channel will request the IOM to do a multiplex interrupt service. Using a combination of configuration switches and interrupt level indication in the service request, the IOM will retrieve one of 32 interrupt multiplex words, set a bit to indicate which channel is causing the interrupt and restore the word, then finally set the corresponding interrupt cell in the system controller. This will inform the software that the sequence of operations is concluded.

3.1 SOFTWARE INTERFACE

The IOM is responsible for moving information between core storage and various peripheral devices as controlled by demand from the peripheral control units associated with the peripheral devices. These operations do not occur continuously, but are initiated by connects, controlled by control words, and their completions are indicated by program interrupts.

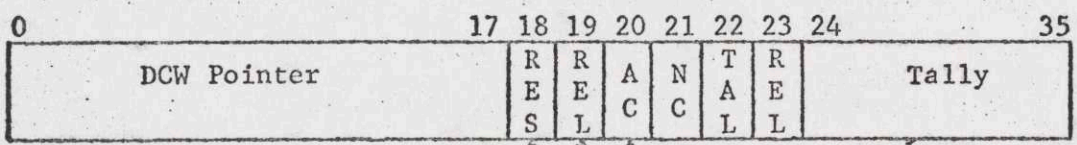
*To the scratchpad if the scratchpad (option) is in; otherwise to core.

3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

After the operation of a channel has been initiated, the IOM Central hardware must place into the LPW extension (in core and in scratchpad when available) the absolute address of each Instruction DCW which it encounters while servicing the list. (These are described in paragraph 3.2.3.)

The LPW and LPW extension have the formats shown below:

GCOS, Extended GCOS or VMM LPW

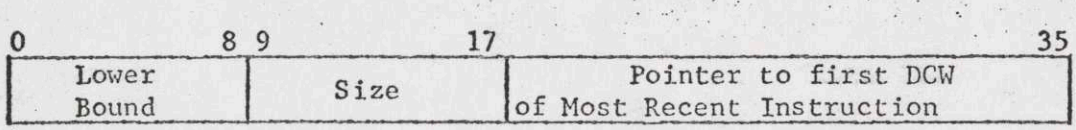


Restrict IDCW's

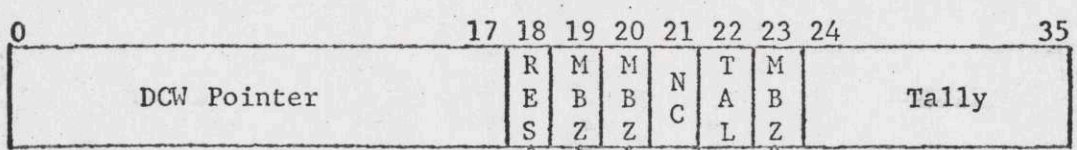
IOM-controlled Image of Rel Bit

Appending Control - If 1, Append Address Extension to DCW Pointer
If 0, Append Zeros to DCW Pointer
MBZ for all overhead channels (not checked)
MBZ for GCOS mode

GCOS, Extended GCOS or VMM LPWX



MULTICS LPW

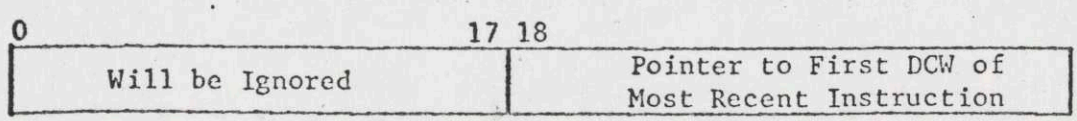


Restrict IDCW's

(Checked)

(Not checked)

MULTICS LPWX



3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

The various fields are defined as follows:

DCW (or PCW) Pointer (LPW 0-17) - Provides the least significant 18 bits of a 24 bit address of the DCW or PCW list. In MULTICS Mode, or for the address of a PCW in any mode, the most significant six address bits will be zero. In Extended GCOS or VMM Mode, the most significant six address bits of the DCW depend on the state of LPW 20 (see below). Updating of this field is controlled by the NC (no change), TAL (Tally Control) and tally fields as shown in Table 3.2.1. When updating is called for, the IOM Central increments this field by one (two if the channel is the connect channel) during each list service.

Restricted Bit (LPW 18) - Provides the software with a way to restrict the use of Instruction DCW's by users without having to scan all DCW lists. If this bit is one and an Instruction DCW is encountered by the IOM Central, it will abort the I/O transaction and indicate a User Fault: Instruction DCW in Restricted Mode to the channel. If bit 18 is a zero, the list is unrestricted and Instruction DCW's will be allowed. (Bit 18 of the LPW for the connect channel must be set to zero by the software to preserve future compatibility and will be ignored by the IOM Central.) When the IOM Central encounters a Transfer DCW (TDCW) during a list service, it will at that time logically OR TDCW bit 34 into LPW bit 18 to provide the software with a way to switch immediately from unrestricted to restricted operation dynamically. Any subsequent encounter with an IDCW (Instruction DCW) will cause a user fault for that channel if the LPW bit 18 has been set to 1 by the TDCW. There will be no way to switch dynamically from restricted to unrestricted operation. Only replacing the LPW and issuing a CIOC for the restricted channel will restore the unrestricted operation. In addition, only unrestricted users in Extended GCOS or VMM modes may have TDCW 33 = 1 (i.e., change LPW 20). Note: An exception occurs during a Reverse List Service where LPW Bit 18 is unconditionally reset.
REL (LPW 19) - Reserved mode for storage of REL flag (bit 23) condition at the time an IDCW was fetched, or whenever a first-list service was performed.

AC (LPW 20) - Is defined as the Appending Control bit. In the Extended GCOS or VMM Mode this bit defines when a DCW list address should be appended with zeros (LPW 20 = 0), or should be appended with the current address extension (LPW 20 = 1). This bit may be changed from a zero to a one via a transfer type DCW, and will be reset to zero during a Reverse List Service. MBZ in MULTICS. A system fault will be reported if LPW 20 = 1 in GCOS Mode.

3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

NC - No Change (LPW 21) - Provides the software with a way to control the updating of the LPW (both address and tally fields) as shown in Table 3.2.1. When set to a one, bit 21 inhibits the updating of the address and tally fields of the LPW. It forces a PTRO to be indicated for a Connect Channel service regardless of the state of LPW bit 22.

TAL - Tally Indication Control (LPW 22) - Provides the software with a way to control the recognition of PTRO (Pre-Tally Run-Out) condition by all channels as shown in Table 3.2.1. When set to a one, bit 22 allows the recognition of PTRO and TRO; when zero, these conditions are not indicated, and a tally of zero will not cause a fault indication. This bit is overridden by LPW bit 21, NC.

REL (LPW 23) - Provides the software with a way to control the interpretation of DCW addresses for indirect channels by the IOM as absolute or relative. Depending on whether this bit is zero or one, each DCW address is treated as absolute or relative, respectively. The IOM Central converts relative addresses to absolute and checks them for boundary errors (see description of lower bound and size fields of LPW). Bit 23 of the LPW for the connect channel will be ignored by the IOM Central. When the IOM Central encounters a TDCW during a list service it will logically OR TDCW bit 35 into LPW bit 23 to provide software with a way to switch immediately from absolute to relative operation dynamically. On a reverse list service bit 19 of the LPW will replace bit 23. There will be no way to switch from relative to absolute operation except by a new LPW and connect (CIOC). For direct channels which use list service to obtain a DCW, no conversion of addresses in the DCW is possible; the program must provide absolute addresses, and LPW bit 23 should be zero for future compatibility. In MULTICS mode, LPW 23 = 1 will cause a system fault: Relative Error, MULTICS mode.

Tally (LPW 24-35) - Defines the number of PCW's or DCW's remaining in the list. Updating of this field by the IOM Central is controlled by the NC, TAL, and the value of the tally, as shown in Table 3.2.1. When updating is called for, the IOM Central decrements this field by one during each list service. Upon detecting a TRO condition for a channel as defined in Table 3.2.1, the IOM Central will indicate a User Fault: LPW TRO to the channel. (A System Fault: LPW TRO will be indicated if the list service is for the connect channel.) The tally is decremented when a transfer DCW is encountered and is decremented again when the next DCW is pulled after the transfer has occurred.

The payload channel never gets a PTRO indication. It must determine when to stop requesting list service on the basis of information in DCW or on the basis of some external influence.

3.2.1 List Pointer Words (LPW and LPW Extension) (continued)

Lower Bound (LPW Ext. 0-8 and Size (LPW Ext. 9-17) - Provide the software with a way of effectively setting up a base address register for each data channel. During a list service, if the REL bit (LPW 23) is one, the IOM Central checks the address and tally of the new DCW for possible boundary errors and, provided there is no boundary error, converts the relative address to an absolute address which is then placed in the DCW mailbox (or scratchpad). No checking or conversion is performed by the IOM Central if the REL bit is zero. In MULTICS mode these fields are ignored as the REL bit is always zero.

Pointer to First DCW of Most Recent Instruction (LPW Ext. 18-35) - Will be updated by the IOM Central during the first list service after a PCW, and during any list service which encounters an Instruction DCW. Each time that this field is updated, the IOM Central will copy the DCW pointer field of the LPW (or the transfer DCW, if one is encountered) into this field of the LPW extension in core, and in scratchpad when available. Thus, if the most recent instruction was a PCW, this field will point to the first data DCW; if the most recent instruction was an Instruction DCW, this field will point to the Instruction DCW. It is possible for the software to determine how many instructions were executed by the IOM before an abnormal termination, by examining this field of the LPW extension in the core mailbox after termination. This field will be used as the DCW Pointer (LPW 0-17) on a reverse list service.

3.2.2 Peripheral Control Words (PCW)

The PCW is used by the Connect Channel to initiate the operation of a channel, or to mask (turn off) the operation of a channel that was previously initiated. The software can issue one or more PCW's with a single CIOC instruction by arranging the PCW's in a list and setting up an LPW for the Connect Channel to define the location and length of the list.

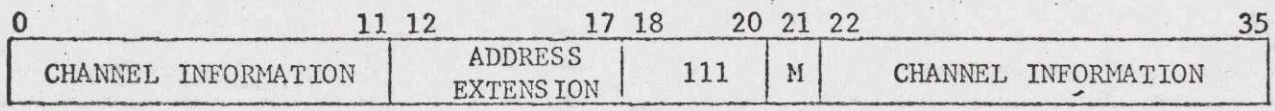
A non-PCW word encountered during a list service by the connect channel will cause a system fault. The PCW list should not contain more than one PCW for any one channel, unless the EPS-1 for that channel explicitly permits such operation.

Each PCW fills two words of core and must occupy a y-pair, that is, a pair of words obtained by a double-precision core access. A list of PCW's must occupy sequential y-pairs.

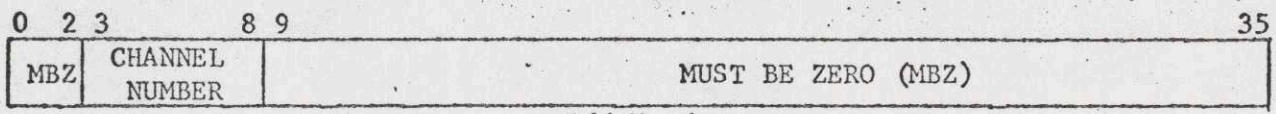
3.2.2 Peripheral Control Words (PCW) (continued)

The PCW for all payload channels has the format shown below. The PCW for the snapshot channel is shown in paragraph 3.8; the PCW for the wraparound channel is in 3.9.1; and the PCW for the scratchpad access channel in 3.11.

The software must be aware of the channel type and peripheral subsystem characteristics before writing more than one PCW for the same channel in the PCW list. In order to issue more than one command to the common peripheral channel for instance, subsequent commands must appear in the DCW list as IDCW's.



Even Word



Odd Word

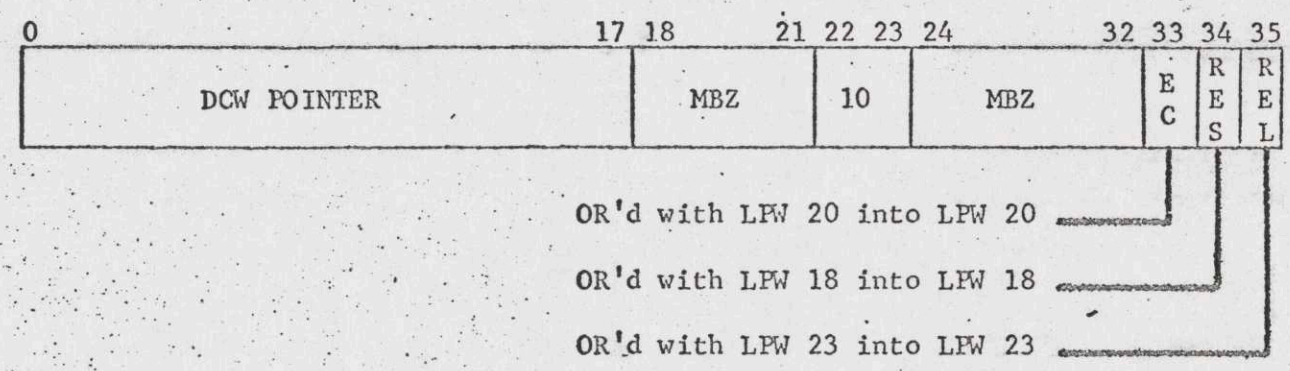
All 36 bits of the even word of the PCW are sent to the channel whose channel number is specified in the Odd Word of the PCW. Bits 18-20 of the Even Word must be 111_2 or 7_8 to identify the word as a PCW.

Bits 12-17 contain the address extension which is maintained by the channel for subsequent use by the IOM in generating a 24-bit address for list or data services for the extended address modes.

A channel will change from the normal condition to a masked condition as a result of a System Initialize, a system fault flag from the IOM Central, or as a result of a PCW with bit 21 = 1. This masked condition is a state in which a channel will not request service in spite of a need for such service that may be generated in the channel. A channel will change from the masked condition to normal as a result of a PCW with bit 21 = 0.

3.2.3.2 Transfer DCW

The TDCW provides the software and the user with the ability to change control bits and to link one DCW list to another DCW list. The format of the TDCW is shown below. Bits 18-21 and 24-32 are not checked by IOM Central.



DCW Pointer (0 - 17) - Specifies bits 6 -23 of the address (absolute or relative, depending on the REL bit in the LPW) of the next DCW. The IOM Central absolutizes the address, if necessary, and places bits 6 - 23 of the absolute address in the DCW Pointer Field of the LPW, so that subsequent DCW's will be obtained from the new list. The most significant six bits (address extension) of the next DCW address are implied to be zero if MULTICS Mode or if Extended GCOS or VMM Mode and LPW 20 = 0. In Extended GCOS or VMM Mode and LPW 20 = 1, the address extension will be the present address extension held by the channel.

Bits 18 - 21 - Must be zero.

Bits 22 - 23 - Must be coded 10_2 to identify the DCW as a TDCW.

Bits 24 - 32 - Must be zero.

Bit 33 - In Extended GCOS or VMM, bit 33 may be used to conditionally change LPW 20 from a zero to a one. That is, if TDCW 33 = 1 and if bit 18 of the present LPW is zero (unrestricted), LPW 20 will be set to a one. This will allow (system) software to control when the address extension bits from the PCW or IDCW will be used for accessing the users DCW list. Transfer DCW 33 = 1 and LPW 18 = 1 (restricted) is a user fault in Extended GCOS or VMM. TDCW 33 MBZ for GCOS and MULTICS (not checked). In GCOS, if TDCW 33 = 1, LPW 20 will be set to a one and cause a system fault.

3.2.3.3 I/O Transfer and Disconnect (IOTD)
I/O Transfer and Proceed (IOTP)
I/O Non-Transfer and Proceed (IONTP) (continued)

Mod 64 Bit (21) - Data DCW 21 was defined on the 655 IOM to be used, if a sub-word (character) channel were defined, to specify the manner of DCW tally update. That is, tally updating would be done once per word or once per character. For the 6100 IOM, tally will be on a word basis if a 9-bit character channel is ever defined.

In Extended GCOS or VMM, data DCW 21 = 0 will cause the data address DCW 0 - 17 (absolutized if called for by LPW 23) to be appended with the 6-bit address extension from the PCW for each data transfer; DCW 21 = 1 is a system fault in Extended GCOS or GCOS mode.

In VMM Mode, DCW 21 = 1 and LPW 23 = 0 (absolute) will result in the formation of a 24 bit modulo 64 address from DCW (0 - 17). DCW 21 = 1 and LPW 23 = 1 (relative) is a system fault in VMM.

In the MULTICS Mode, data DCW 21 = 0 will cause the absolute data address DCW 0 - 17 to be appended with 6 leading zeros for each data transfer; DCW 21 = 1 will initially cause the data address DCW 0 - 17 to be left justified 6 bits to form a 24 bit modulo 64 address to be used for data transfer. Subsequent data transfers will use the initial contents of DCW (0-5), stored in the channel, as the address extension.

Type (22 - 23) must be coded to identify the type of DCW.

00 IOTD	I/O Transfer and Disconnect. The current device instruction is ended (terminated) when the channel detects the tally run-out condition of the tally.
01 IOTP	I/O Transfer and Proceed. The current device instruction proceeds to a new DCW when the channel detects the tally run-out condition of the tally.
10	See Section 3.2.3.2 on Transfer DCW (TDCW).
11 IONTP	Same as IOTP except that no core accesses are made. If data is being read from a peripheral device, the block of data is discarded. If data is being written to a peripheral device, the IOM Central generates a block of zeros.

3.2.4 Status Control Word (SCW) (continued)

Circular queue addresses will be incremented after each entry until an entry is made in the queue tail. After the queue tail entry is made, the address will rotate back to the head of the queue.

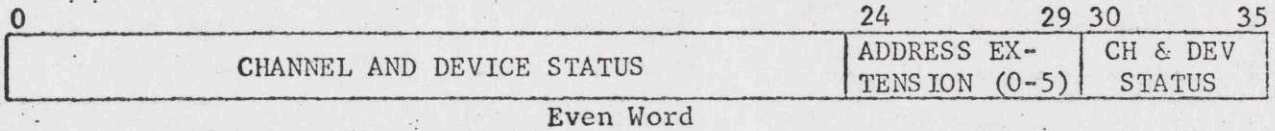
The tally of the SCW will be decremented for each status entry in either list or queue mode, but the suppression of address changes will not occur when the tally has been decremented to zero if circular status is called for.

Bits 20 - 23 are not used, and must be set to zero by the software. These bits are not examined by IOM Central.

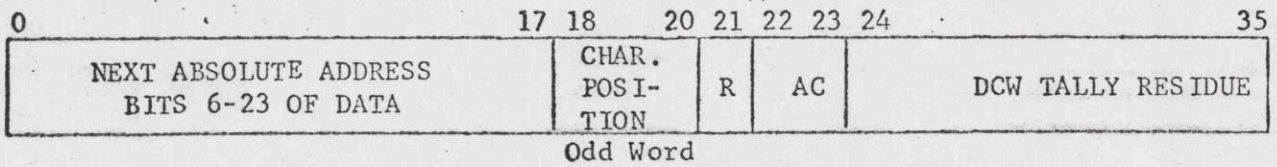
Tally (24 - 35) defines the number of unoccupied y-pairs (72-bits) in the status queue. The IOM Central will decrement the tally by one each time that status is stored in the queue, except when the tally is zero (before updating). As a result, if tally = N, the status queue actually consists of N + 1 y-pairs. The (N + 1)th y-pair corresponds to a tally of zero, and is therefore subject to being overlaid by subsequent status. SCW TRO is not a fault condition. In the circular queue mode the tally will continue to be decremented when it reaches zero.

3.2.5 Channel and Device Status Words

When the IOM Central performs a status service for a channel, it will store two words into the y-pair defined by the SCW for the channel. These two words will have the following format.



Even Word



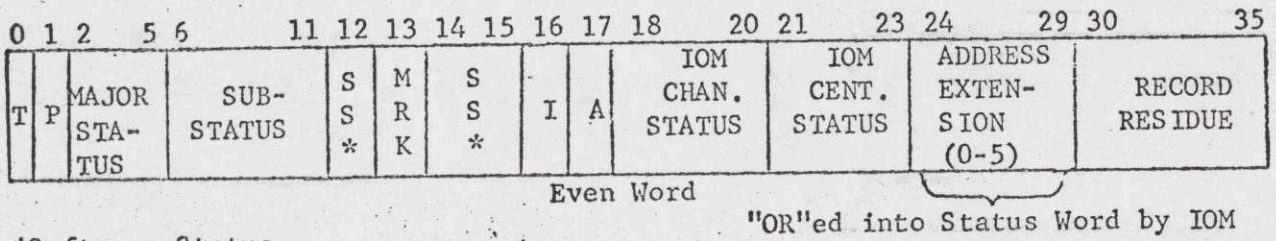
Odd Word

3.2.5 Channel and Device Status Words (continued)

EVEN WORD:

Channel and Device Status (0 - 35) will be generated by the channel and sent to the IOM Central during the status service. The IOM Central will obtain the address extension bits from the channel's Transaction Command (for status service), and will "OR" them into bits 24-29 of the status word supplied by the channel; therefore, the channel must insure that bits 24-29 of the even status word are zero. The IOM Central will store the channel and device status word in the even word of the y-pair defined by the Status Control Word.

The Common Peripheral Channel Status is shown for illustrative purposes only and reference should be made to the EPS-1 for the Common Peripheral Channel for explanation of the fields shown.



*Software Status

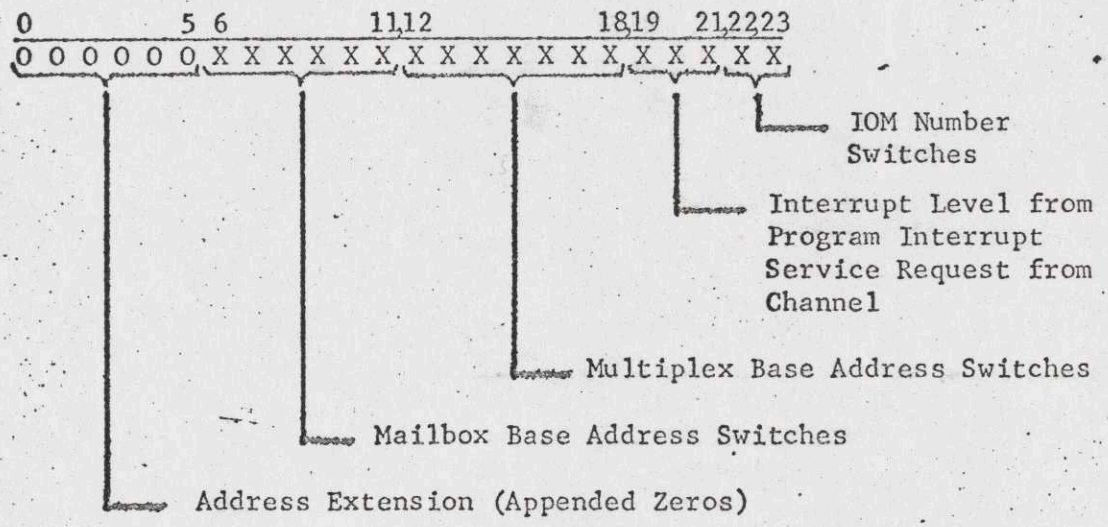
ODD WORD:

The IOM Central will obtain the DCW for the channel (from the core mailbox or from the scratchpad, as appropriate) and store this DCW residue in the odd word of the y-pair defined by the SCW. The information in the DCW residue (as a result of updating by the IOM Central during data services) must meet the following requirements so that it can be properly interpreted by software.

3.2.7 Interrupt Multiplex Word (IMW)

The IOM has the ability to set any of the 32 program interrupt cells located in the system controller containing the base address of the IOM. It should be noted however that for any given IOM identity switch setting, the IOM can set only 8 of these program interrupt cells. The use of this interrupt provision is restricted by system assignment of program interrupt cells. The IOM uses the 32 interrupt cells in conjunction with the 32 core locations in the IOM mailbox area to establish a channel's identity. There is a one-to-one correspondence in address between the program interrupt cells and the IMW words.

The IOM Central pulls the IMW from the core location having the address determined as follows:



One IMW is provided for each program interrupt cell which can be set by the IOM Central. The particular one of the 32 words in the IMW area, and the interrupt cell in the System Controller, are determined by two factors:

a) The IOM number, as set by the IOM number switches on the maintenance panel, will determine the two least significant bits of the IMW address. This provides one word for each of four possible IOM's at each of eight interrupt levels. The switches are further described in paragraph 3.5.2.

b) The interrupt level as determined by the logic in each channel. The channel will wire, patch, or logically manipulate bit positions 13-15 of the data presented with a program interrupt service request, providing as many as eight possible interrupt levels for each channel from the total of 32 levels. Note that this interrupt level becomes bits 19-21 of the IMW address once the IOM has appended an address extension of zeros.

3.3 BOUNDARY CHECKING

3.3.1 Notation

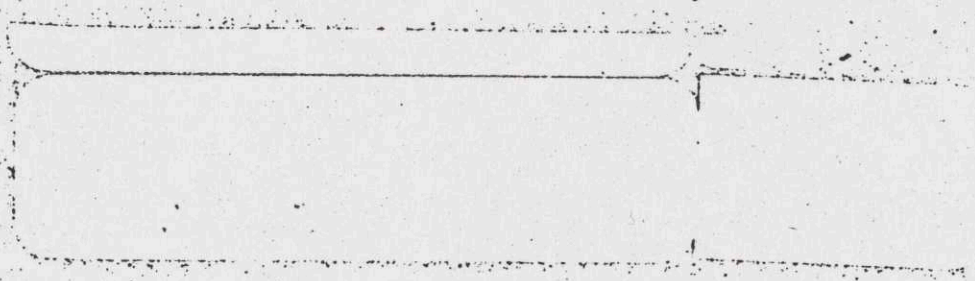
The following notation will be used to define boundary checking and address conversion:

A = initial DCW address (relative)

S = the number of 512-word blocks addressable by the program; (size) - S is relative to the Lower Bound; i.e., the number of 512 word blocks "starts" at the Lower Bound.

T = initial DCW tally = DCW (24-35)

Note: If T = 0000_8 it must be treated as 10000_8 by the IOM Central in the boundary check.



LB = Lower Bound = LPW Ext. (0-8) = Upper 9 bits of 18 bit address

3.3.2 Check Performed

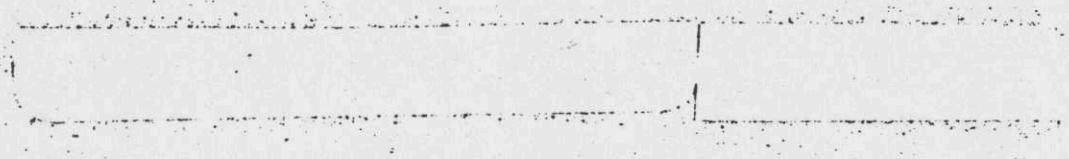
1) A User Fault:Boundary Error will be indicated if

$$S + LB - 2^9 > 0$$

2) A User Fault:Boundary Error will be indicated if:

for IOTD, IOTP, IONTP;

$$S \times 2^9 - A - T < 0 \text{ or for TDCW } S \times 2^9 - A \leq 0$$



Note: Unlike the 6000 IOM which interpreted size = 0 as a User Fault, the 6000B IOM will interpret size = 0 as the specifier for 256K (512 consecutive blocks of 512 words each). The only valid lower bound for size 0 is an LB of zero.

3.3.3 Address Result

If a User Fault does not occur, then the lower 18 bits of the absolute address will be:

$$\sum_{N=6}^{14} \left[(\text{LPW Ext. (N)} + \text{DCW (N)}) \times 2^{17-N}\right] + \sum_{N=15}^{23} \left[\text{DCW(N)} \times 2^{17-N}\right]$$

3.4 CHANNEL NUMBERING

The channel number is a 9-bit binary number, usually expressed as a 3-digit octal number, which identifies a specific channel for both the hardware and the software. Each channel has provision for defining its channel number by a patch arrangement in the channel. Only the 6 low-order bits of the channel number are to be implemented. The high order 3 bits must be zero for upward compatibility.

Channel numbers are used for the following purposes in the IOM:

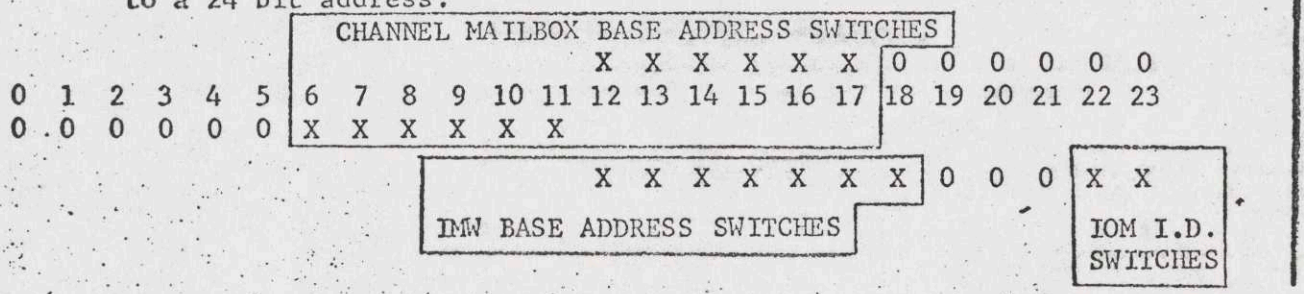
- A channel recognizes that a PCW is intended for it on the basis of channel number;
- The IOM Central uses the channel number supplied by the channel to determine the location of control word mailboxes in core store or in scratchpad;
- The IOM Central places the channel number in the system fault word when a system fault is detected and indicated, so that the software will know which channel was affected.

Channel numbers 010_8 - 077_8 may be assigned to payload channels, and channel numbers 000_8 - 007_8 are reserved for assignment to overhead channels:

Channel No.	Overhead Channel Assigned
0	Illegal use - not assigned
1	Fault Channel
2	Connect Channel
3	Snapshot Channel
4	Wraparound Channel
5	Bootload Channel
6	Special Status Channel
7	Scratchpad Access Channel

3.5 MAILBOXES AND STORE MAP

Communication between software and the IOM depends on an understanding of where control words, such as the LPW, SCW, and IMW, are located in storage. To facilitate this, two related base addresses are defined by switches on the IOM configuration panel. These switches are indicated by X in the diagram below which illustrates the relationship between the sets of switches. The paragraphs which follow describe the use of the switches relative to a 24 bit address.



3.6 SYSTEM FAULT CHANNEL

The system fault channel controls the indication to the software of system faults that are detected by theIOM.

Once it has been activated by the detection of a system fault, the system fault channel obtains an indirect data service from the IOM Central. During this indirect data service the system fault word is transferred from the fault channel to core under control of the DCW for the system fault channel. The system fault channel operates in the indirect-36 mode. The system fault channel is the top priority channel, and will be wired as number 001_8.

Immediately after the data service has been completed, without relinquishing control, the system fault channel obtains a program interrupt service using level one (without storing status), does a list service if necessary and then de-activates itself, waiting for another possible system fault.

The software determined tally of the fault channel DCW should be sufficient to allow for several faults occurring in succession. When this number is exceeded and the tally reaches zero a pre-tally runout indicator will cause the fault channel to request a list service. The software determined LPW obtained during this service should point to a DCW which will overlay the original fault channel DCW and should have the same initial address and tally. Thus the fixed size queue (n words) will cycle and have, at most, the last n fault words.

The LPW extension and SCW mailboxes for the system fault channel are not used by the IOM.

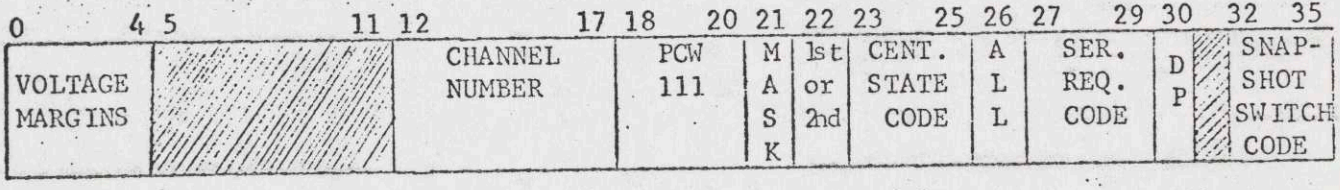
3.8 SNAPSHOT CHANNEL

The snapshot channel provides the test and diagnostic software with a way of sampling control lines and signals in the IOM Central at times specified by the software. The snapshot channel is activated by a PCW addressed to it.

The PCW defines the state of the IOM Central at which the snapshot is to occur. This includes such factors as the channel number of the channel being serviced, and the type of service, as well as the control state of the IOM Central. When the snapshot conditions are met, the specified information is switched into the snapshot register and then stored in core as data, under control of the DCW for the snapshot channel. Sampling continues until a PTRO condition is indicated by the IOM Central. When the PTRO is indicated, the snapshot channel obtains a program interrupt service using level one (without storing status) and then de-activates itself waiting for another PCW.

The Snapshot Channel is wired as channel number 3. The LPW, LPW extension and SCW in the mailbox area for the Snapshot Channel are not used.

The even word of the PCW for the Snapshot Channel has the following format:



Explanation of PCW fields: (See note below)

0-4	Voltage Margin Control
5-11,31	These bits must be zero.
12-17	Channel number of channel that is to be in operation when the information is strobed into the Snapshot Register.
18-20	These bits are 111 for a PCW.
21	This bit will mask the snapshot channel if set to "1".
22	If this bit is "0", the Snapshot Register will be strobed the first time the central is in the state requested. If the bit is a "1", the strobe will occur the second time the central is in the requested state.

3.8 SNAPSHOT CHANNEL (continued)

32-35 (continued)

Code 32-35	Area of IOM Referenced
0000	Data bus from stores (DR bus 00-35)
0001	Data bus from stores (DR bus 36-71)
0010	Control word reg. 00-35 (C reg. 00-35)
0011	Control word Incrementer/Decrementer (C_{ADD} 00-17, C_{DEC} 24/35)
0100	Control word reg. 36-71 (C reg. 36-71)
0101	Data from stores register switch (H Sw. 00-35)
0110	I/O bus input from channels (S Bus 00-35)
0111	Service request register (T reg. 00-35)
1000	Data Register, from I/O bus from channels (D reg. 00-35)
1001	Data bus to store (DT bus 00-35)
1010	Data bus to store (DT bus 36-71)
1011	Zone, address, and command (ZAC)
1100	Channel number register and misc. control signals to be defined in EPS-2
1101	Not used
1110	Not used
1111	Not used

3.9 WRAPAROUND CHANNEL (WAC)

The wraparound channel provides the test and diagnostic software with a way of causing the IOM Central to perform specific types of service on behalf of a specific channel, designated by the T&D software. The wraparound channel is activated by receipt of a PCW addressed to it, and assumes the identity of the channel number contained in the PCW.

By appropriate coding of the PCW the following operations can be caused to happen:

- Load data into the data register of the wraparound channel.
- Perform list service (or first list service) in lieu of a specified channel.
- Perform status service in lieu of a specified channel.
- Perform program interrupt service using specified program interrupt cell and multiplex bit number.
- Perform indirect data load or store in lieu of a specified channel.
- Perform direct load or store using specified storage location.
- Perform direct read clear using specified storage location.
- Load specified status into status register of the wraparound channel.
- Cause a system fault, or a user fault.

After performing the action specified by the PCW, the wraparound channel de-activates itself, waiting for another PCW. There is no automatic storage of status and no automatic program interrupt associated with the operation of the wraparound channel.

At the end of each service by the Wraparound Channel, I/O bus control and flag lines are loaded into the wraparound status register. A PCW specifying a status service for the wraparound channel will return this information to core, using the SCW for the channel specified in the PCW, probably the SCW for the WAC channel.

The wraparound channel will be wired as channel number 004_8.

The mailbox area is not used automatically; the SCW should be used when accessing the status information stored in the WAC hardware.

The Wraparound Channel utilizes four word formats:

1) Peripheral Control Word (36 bits)
2) Data Word, Single Precision (36 bits + parity)
3) Data Word, Double Precision (72 bits + 2 parity)
4) Status Word (36 bits)

3.9.1 Peripheral Control Word (PCW)

The even word of the PCW for the Wraparound Channel has the following format (the odd word addresses channel 004_8):

0 12	17	18 20	21 23	24	25	26	27 29	30 35
ADDRESS/MULTIPLEX INTERRUPT SERV. ADDR. EXT.		111	SERVICE REQUEST CODE	MOD	*	AEC	ACTION CODE	TEST CHANNEL NUMBER

* Byte Size

The PCW fields are described as follows:

0-17 Contains bits 6-23 of the absolute store address for direct data service or Mailbox address when Indirect data service uses an indirect Mailbox. Bits 12-17 will be used as address bits 0-5 if bit 26 equals a "1". This field also can contain the Program Interrupt Cell for a Multiplex Program Interrupt Service in bits 13-15.

18-20 Always 111 for a PCW.

21-23 Service Request Code which determines the type of service of an action PCW. These codes are defined as follows:

000	Invalid
001	List Service
010	Status Service
011	Interrupt Service
100	Indirect Data Load Service
101	Indirect Data Store Service
110	Direct Data Load Service
111	Direct Data Store Service

24 Mod bit - when equal to 1 indicates the first list service, or read clear for direct data load single precision.

25 Byte size - determines the byte size during an indirect data service.

0 = 9 bit byte

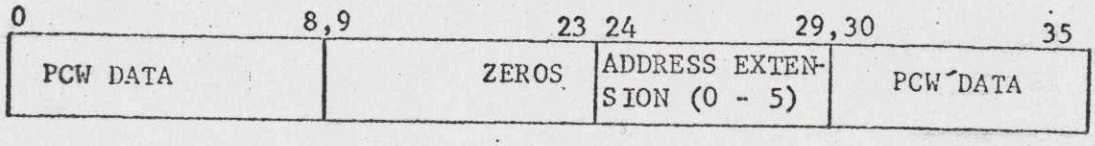
1 = 36 bit byte

26 Address Extension Control - determines if address extension bits 12-17 will be outputted with transaction command.

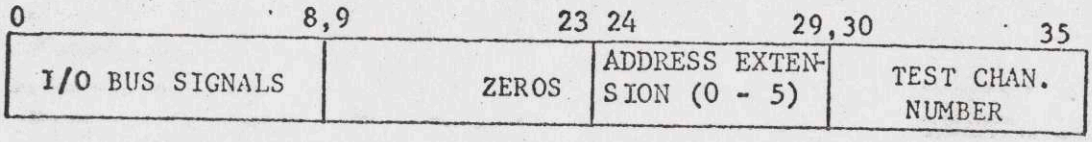
3.9.3 Status Word

The Wraparound Channel Status Register is loaded from the input data lines when the Wraparound Channel receives a data PCW specifying the Status Register. The Status Register is also loaded with the I/O Bus Control points and flags at the end of each service that the Wraparound Channel performs as a result of an action PCW. The bus will also be loaded if the Wraparound Channel receives a PCW with an action code of 11.

The Status Word is stored in core when a Status Service is specified in an action PCW. The format of the Status Word in the Wraparound Channel is then one of the following:



or



In the second case, the fields are designated as follows:

Bit 0 = SCN
1 = DTA
2 = DBL
3 = TLO
4 = TL1
5 = SYS
6 = US0
7 = US1
8 = US2

30-35 = Test channel number which was received with the last action PCW (with the exception of the Status Service Request).

Note: Bit 9 through 23 are not implemented and will always be returned to core as zeros for a status return.

Bits 24 - 29 are "OR'ed" in by the IOM Central from the address extension bits in the transaction command.

3.11 SCRATCHPAD ACCESS CHANNEL

The scratchpad access channel provides the test and diagnostic software with a way of loading or storing the contents of the channel mailboxes. By appropriate coding of the PCW the scratchpad mailboxes of a specified channel can be loaded or stored from specified locations in core. The channel will access the scratchpad when it is physically present; if a channel has no scratchpad, the mailbox in core for that channel will be accessed.

The scratchpad access channel will be wired as channel number 07. The LPW, LPW extension, and SCW mailboxes for the scratchpad access channel will not be used by the IOM Central. Only the DCW for channel 07_8 will be used.

The scratchpad access channel will do an indirect data service under control of its DCW, reading from scratchpad and storing into core, or vice-versa. Upon completion of the transfer, an appropriate multiplex interrupt to level one is executed.

Software should not issue successive connects to the scratchpad access channel until the interrupt is received from the previous connect; otherwise the action called for by the connect may not be performed.

Format for the PCW using the Scratchpad Access Channel is as follows:

Even Word:

0 – 17	18 – 20	21 – 23	24	25	26	27 – 29	30 – 35
ADDRESS	111	SERV. REQ. CODE	0	1	0	000	000111

Odd Word:

0 – 8	9 – 35
000000100	MBZ

It may be seen by examination of the PCW that the Scratchpad Access Channel is operated by means of the Wraparound Channel. The PCW is addressed to the Wraparound Channel, which does a service in lieu of the Scratchpad Access Channel using the DCW for channel 07_8.

3.11 SCRATCHPAD ACCESS CHANNEL (Continued)

24 Mod bit must be zero to allow accessing of scratchpad when available.

25 Byte size should be 1 to access the full 36 bit word.
26 Address extension control - should be zero.
27 - 29 Action code is 000.

30 - 35 Specify the channel number of the scratchpad access channel 007_8.

Odd Word:

Bits 0 - 8 Address the PCW to the Wraparound Channel, 004_8.

9 - 35 These bits are unused and must be zero for future compatibility.

3.12 MAINTENANCE PANEL AND CONFIGURATION SWITCHES

In order to provide for both static and dynamic test capability of the IOM Central, maintenance functions and Maintenance Panel controls are being incorporated to allow simulation of the listed inputs to the Central:

(a) System Store Data
(b) System Store Strobe Responses
(c) Channel Transactions or Service Requests
(d) Channel Data

3.12.1 Fault Location Aids

In addition to the above, which are basically for free-standing test and checkout without attachment to or from any other system component, several maintenance and test aids will be available for dynamic fault location and isolation. Capabilities of these aids are listed below. Note that their primary purpose is to facilitate field maintenance; however, their use in debug and test will provide needed help in initial equipment bring-up.

(a) Single step store cycle
(b) Single step for IOM major cycle
(c) Halt on store address match
(d) Halt on fault (fault channel number match)
(e) Halt on IOM control state match
(f) Halt on channel number match
(g) Halt on channel request code match

3.12.4 Configuration Switches

The IOM maintenance panel configuration switches are listed in the following table. The functions they perform (when not obvious) are defined elsewhere in this specification.

Function	Quantity/Type*
IOM Base Address	12/A
Multiplex Base Address	7/A
IOM Number	2/A
Operating System	1/C
Bootload:	
- Tape/card select	1/A
- Tape channel number	6/A
- Card channel number	6/A
- Bootload	1/B
- System initialize	1/B
- Bootload Port	3/A
Port Configuration (Per Port)	
- Address Assignment	3/A
- Interlace	1/D
- Port Enable	1/A
- System Initialize Enable	1/A
- Half Size	1/A
Alarm Disable	1/A
Test/Normal	1/A

*A = 2 position toggle switch
B = Momentary Contact Pushbutton Switch
C = Four-Position Rotary Switch
D = 3 Position Toggle Switch

4.0 HARDWARE INTERFACE REQUIREMENTS

4.1 STORAGE INTERFACES

4.1.1 System Controller

The IOM Central will interface with from zero to eight 6000B or 6000 system controller ports for performing the following types of cycles:

- Read Restore, Single Precision (RRS,SP)
- Read Restore, Double Precision (RRS,DP)
- Read, Clear Single Precision (RCL,SP)
- Clear Write, Single Precision (CWR,SP)
- Clear Write, Double Precision (CWR,DP)
- Set Execute Interrupt Cell (SXC)

In addition, the IOM will respond to a $CON occurring during a system controller connect cycle. The IOM will generate and check parity on this interface. (See paragraph 4.2.6)

4.1.2 Scratchpad Storage

Each module of the optional scratchpad storage will provide at least48 36-bit words of storage with a complete cycle time of less than 500 nanoseconds. The interface to the scratchpad can be tailored to the requirements of the IOM Central, although full advantage should be taken of the fact that the scratchpad store actually substitutes for a portion of core store so that similar control functions should be provided.

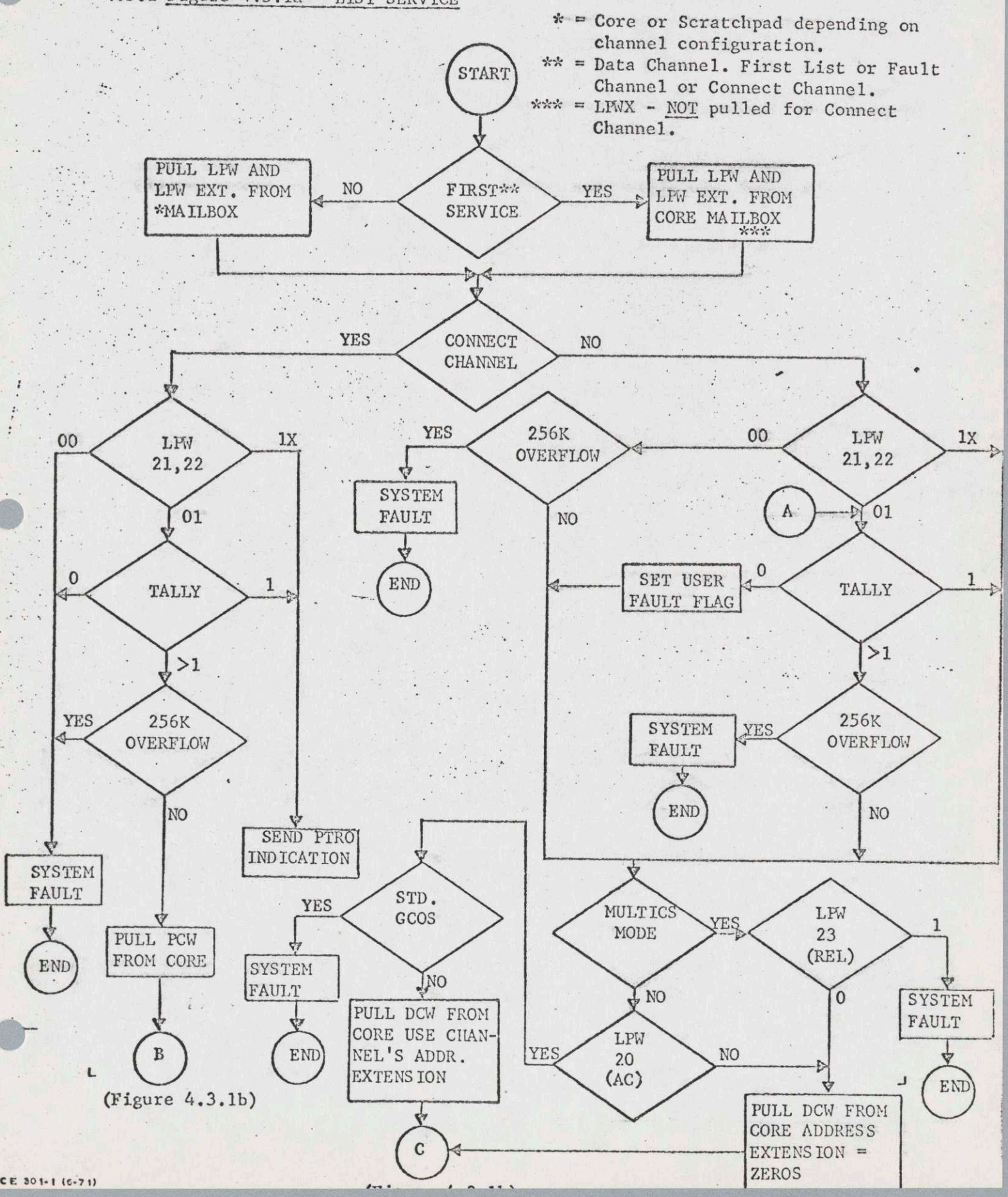
4.2 PRIORITY

The I/O bus priority system is based on a channel's physical location on the bus - the closer to the physical top of the bus, the higher the priority. In addition to the priorities for I/O bus resident boards, the IOM Central overhead channels are also involved in the total priority system. The priority within each I/O bus is fixed. Priority among the I/O buses and the overhead channels is also wired and fixed as follows:

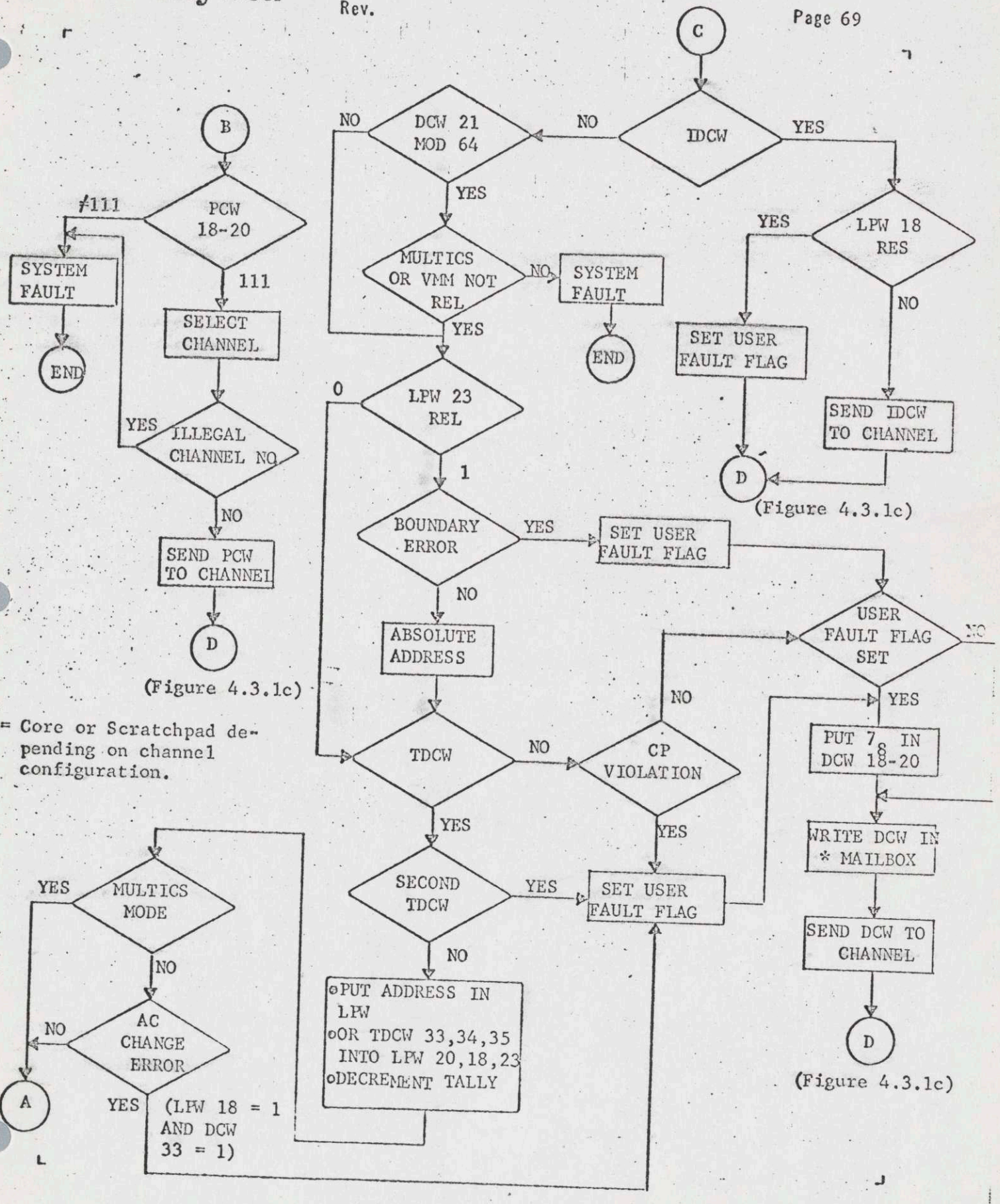
a) Fault Channel (highest priority)
b) Snapshot Channel (second highest priority)
c) I/O Bus #1 (Up to 17 Device Channels or 8 Common Peripheral Channels)
d) I/O Bus #2 (Up to 19 Device Channels or 9 Common Peripheral Channels)
e) I/O Bus #3 (Up to 19 Device channels or 9 Common Peripheral Channels)
f) Maintenance Panel
g) Connect Channel (Lowest Priority)

(A "Device Channel" may be either a High Speed or a Medium Speed Device Channel, or a similar type of channel).

4.3.1 Figure 4.3.1a - LIST SERVICE



(Figure 4.3.1b)



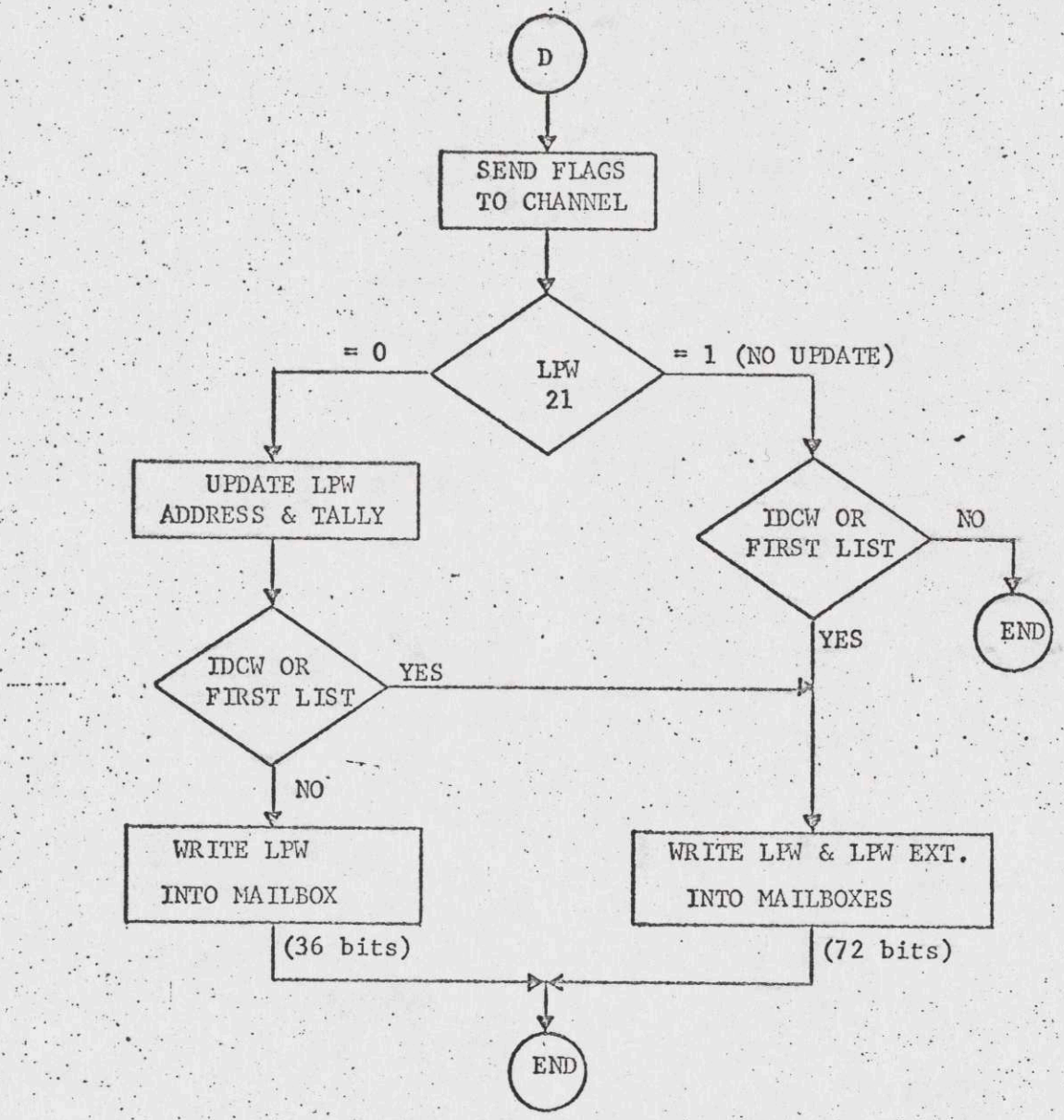
(Figure 4.3.1c)

(Figure 4.3.1c)

* = Core or Scratchpad depending on channel configuration.

(Figure 4.3.1c)

4.3.1 Figure 4.3.1c - LIST SERVICE



4.3.2 Backup List Service

In response to a "backup list service" request from a channel, the IOM Central shall regenerate a list pointer word (LPW) and a list pointer word extension (LPWE) for that channel and shall continue operation on the channel by using the regenerated LPW and LPWE. The format of the regenerated LPW shall be:

REGENERATED LPW		SOURCE
bits 0 - 17	=	LPWE bits 18 - 35 (the pointer to the last IDCW)
bit 18, 20	=	0
bits 19, 21, 22	=	LPW bits 19, 21, 22
bit 23	=	LPW bit 19*
bits 24 -35	=	LPW bits 24 - 35

The format of the regenerated LPWE shall be identical to the format of the current LPWE.

The result of executing the regenerated LPW and LPWE shall be a DCW fetch from the last location to contain an IDCW. Mode shall be non-restricted. Addressing shall be relative or absolute in accordance with the contents of LPW bit 19 (equal to REL flag condition at the time an IDCW was encountered). Tally shall be equal to the LPW tally present at the time of the "backup list service" request. Tally control (bits 21 and 22) shall be the same as the current LPW. Lower Bound and Size constraints for relative addressing shall be the same as the current LPWE.

The DCW pulled following reconstruction of the LPW must be an IDCW. If not, a fault shall be reported by the channel (not by the Central).

The end result of responding to a "backup list service" request shall be a retry (i.e., repeat) of the last command and data transfer sequence entered into for this channel by backing up in the control word list to the last command executed and then retracing the list from that point.

4.3.3 Indirect Data Service

Figure 4.3.3 is a flow diagram of indirect data service. When an indirect data service is performed for a channel, the IOM Central pulls the channel's DCW from the core mailbox, or from the scratchpad.

*The IOM shall load bit 19 with LPW bit 23 each time an IDCW is fetched or whenever a first-list service is performed. (Gecos mode only)

4.3.3 Indirect Data Service (cont.)

The DCW address defines the location of the data unless the DCW type is IONTP. If the channel is performing a peripheral read (core write) operation, and the DCW is IONTP, there is no storage cycle for data transfer (the data is discarded). If the channel is performing a peripheral write (core read) operation and the DCW type is ONTP, the IOM Central generates a data character or word equal to zero and transfers it to the channel.

The IOM Central updates as appropriate the DCW address, tally and character position, and then writes the DCW back into the mailbox (core or scratchpad).

4.3.4 Direct Data Service

The direct data service consists of one core storage cycle (Read Restore or Clear Write, Double or Single Precision) using an absolute 24-bit address supplied by the channel. This service is used by "peripherals" capable of providing addresses from an external source, such as the 355 Intercomputer Channel.

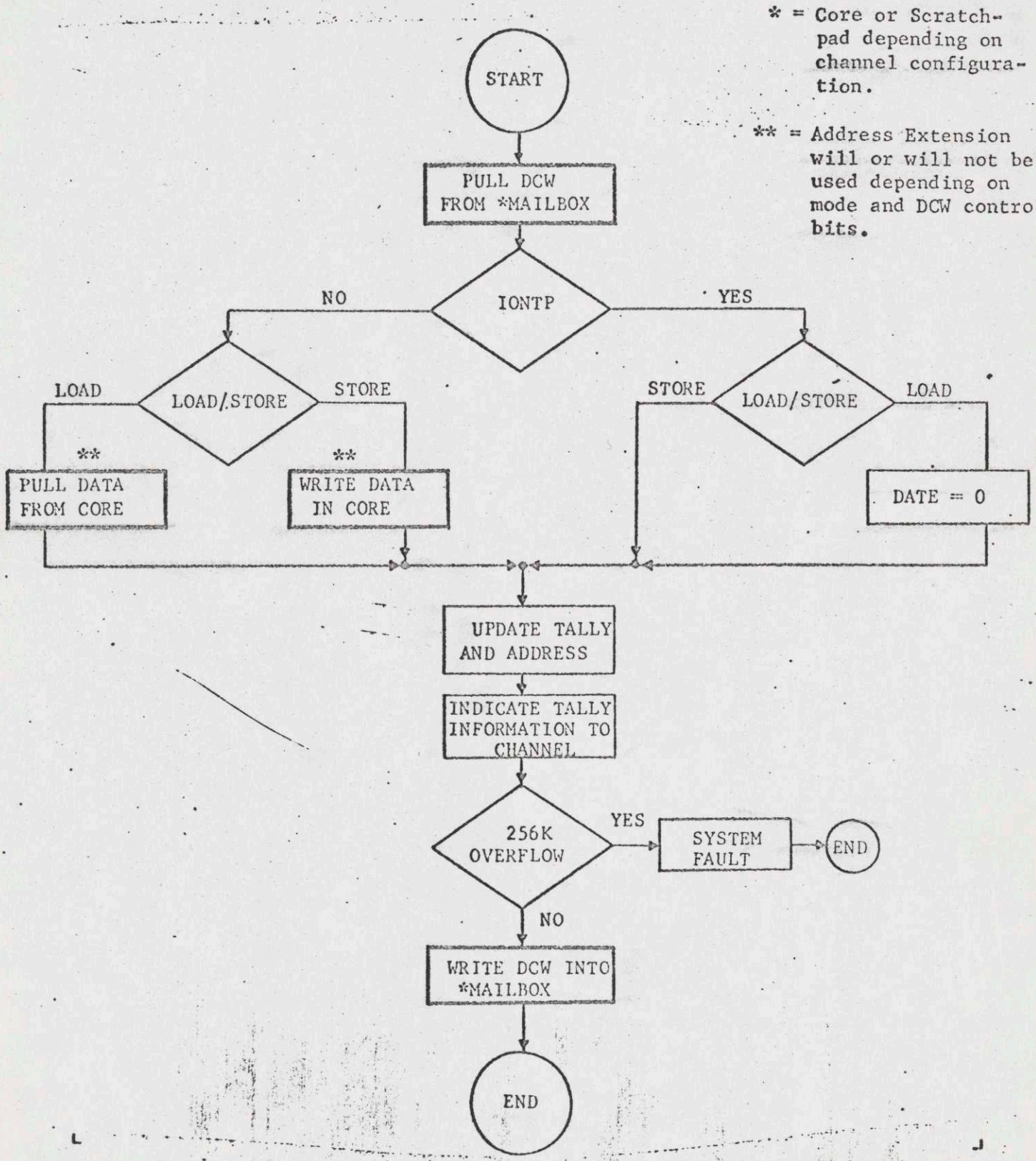
4.3.5 Status Service

Figure 4.3.5a is a flow diagram of status service. When a status service is performed for a channel, the IOM Central pulls the channel's SCW from the core mailbox.

The SCW address defines the y-pair where status is to be stored. The status consists of one word of channel and peripheral status obtained from the channel, and one word of DCW residue which the IOM Central obtains from the DCW mailbox (in core or scratchpad). Before transferring these two words to core the IOM Central inserts character position residue and read bit from the channel into bits 18-21 of the DCW residue and inserts the channel's address extension bits into bits 24-29 of the channel status word.

If the tally in the SCW is zero and the SCW does not indicate a circular queue the IOM Central does not update the SCW address and tally. This provides a means for causing all status from a particular channel to be stored in the same y-pair in core. If the SCW tally is not zero, the IOM Central updates the SCW by adding two to the address and by subtracting one from the tally. The SCW is then returned to the SCW mailbox in core store. For an SCW which indicates a circular queue the IOM Central updates the SCW by adding two to the address and by subtracting one from the tally until the end of the queue is reached. The SCW then updates the address back to the top of the queue.

4.3.2 Figure 4.3.3a - INDIRECT DATA SERVICE



4.5 FAULTS (cont.)

- User Faults - A user fault is an abnormal condition that can be caused by a user program operating in the slave mode in the processor.

- System Faults - A system fault is an abnormal condition that cannot be caused by a user program operating in slave mode, and therefore is assumed to have been caused by a software error or a hardware malfunction.

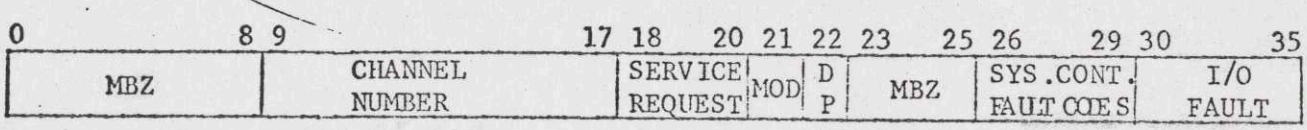
User faults can be detected by the IOM Central or by a channel. If a user fault is detected by the IOM Central, the fault is indicated to the channel, and the channel is responsible for reporting the user fault as status in its regular status queue. A user fault condition does not cause the channel to be masked by the hardware, although the software may take this action in response to the indication of a user fault, if it chooses to.

System faults are detected by the IOM Central and indicated by the system fault channel. The data channel being serviced when the system fault was detected is automatically masked by the hardware in an attempt to protect the system from a recurrence of the fault.

Because of their nature of timing relationship, certain hardware malfunctions also must be reported as user faults.

4.5.1 System Faults

The IOM system fault word format is shown below:



4.6.2 PCW List Address - Any Mode

(0-5) 6 Zeroes appended for address extension

(0 - - 17) Contents of Connect channel LPW 0-17

(0-5) (6 - - 23) 2^{24} Address

4.6.3 DCW List Addresses

(0-5) 6 Zeroes if Extended GCOS or VMM Mode "and" LPW

20 = 0 "or" if MULTICS Mode or Standard GCOS

"or"

(12-17) PCW or IDCW 12-17 if Extended GCOS or VMM mode "and"

LPW 20 = 1

(0 - - 17) Contents of payload channel LPW 0-17

(0 - 5) (6- - 23) 2^{24} Address

4.6.4 Data Addresses

a) Extended GCOS

.DCW 21 = 0

(12-17) Extension from PCW or IDCW 12-17

(0-17) Absolutized contents of DCW 0-17

(0-5) (6-23) 2^{24} Address

.DCW 21 = 1 is a system fault

b) MULTICS

.DCW 21 = 0

(0-5) 6 Zeroes of address extension

(0-17) contents of data DCW 0-17

(0-5) (6-23) 2^{24} Address

APPENDIX A

IOM CENTRAL BUS INTERFACE

A.1 SCOPE

This Appendix describes the performance requirements for the IOM Central/Channel Interface.

A.2 IOM CENTRAL BUS INTERFACE

The IOM Central/Channel interface is implemented as a common, time-shared bus. All signals on the bus are in complement form. The I/O bus is organized as follows:

- The 37-bit (36 information plus parity) "D" bus carries service requests, address extension and data from the channel to the central.
- The 37-bit (36 information plus parity) "U" bus carries data, address extension and control words from the central to all channels.
- The 11-bit "C" bus provides control flags and strobes from the Central to all channels. It also carries the common Channel Requests for Service (CRS) line from the channels to the central.
- The 6-bit "P" bus carries the five serial priority lines from channel to channel, plus Group Activity Inhibit (GAI).
- The 6-bit "N" bus provides the channel number which accompanies a peripheral control word.

A.2.1 D BUS: INPUT DATA BUS

When a channel requests service it must specify the type of service by placing certain information on the data input bus. The formats required for the specific services are given below:

Program Interrupt Service (PI)

0 — 12	13 — 15	16,17,18	20,21 — 26,27	29,30 — 32,33	35
NOT USED	PROG. INTER. LEVEL	MBZ	ADDR. ext. (0-2)	CHANNEL NUMBER	SERVICE REQUEST CODE	NOT USED	ADDR EXT (3-5)

A.2.1 D BUS: INPUT DATA BUS (cont.)

- Character Position & "READ" Field - The character position residue is to be ORed into the character position field of the DCW residue status word (the odd word of status pair); the "READ" bit is placed in bit 21 of the DCW residue status word. The generation of these bits is the responsibility of the channel, and they are only valid during a status service.

- Address extension (0-2) and (3-5) - These two fields specify the 6-bit address extension to be used by the central in forming 24 bit addresses.

- Direct Data Address Field for a service request of DLD or DST, the address field together with the address extension fields specify an absolute address to be used on the direct load or direct store cycle. This field is ignored for a service request of ILD or IST.

- Mod Field - This 1-bit field is valid only for a service request of LST and DLD.

  A "1" in the Mod field for LST indicates that this is a "first list service" and that the central must obtain the LPW and LPW extension from core rather than from the scratchpad. A "1" in the Mod field for DLD indicates that the service requested is a Direct Read C

- DP Double Precision Field - A one-bit in this field indicates that the service requested is to be double precision. Valid only with ILD, IST, DLD, or DST.

- Character (Byte) Size Field - A one-bit field generated by the channel which describes the character size (CS) used in an indirect DATA Service. The CS bits are coded as follows:

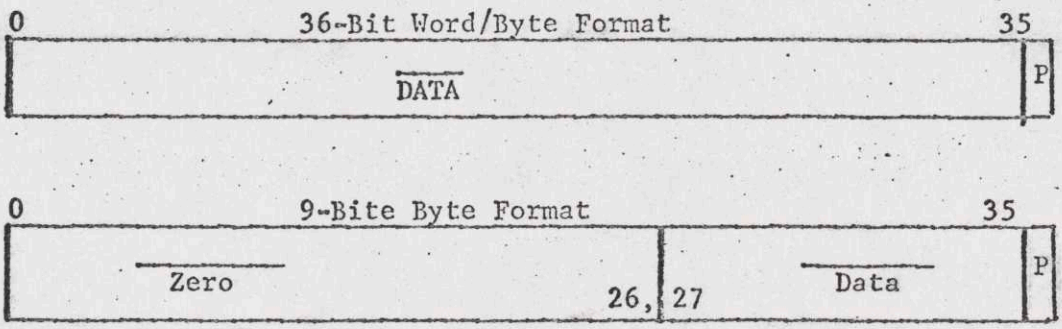
  This bit equal to "0" indicates a CS of 9 bits or equal to "1" indicates a CS of 36 bits.

  NOTE: The CS bits must be provided during a list service as well as during DATA services. Data transfers of 72 bits are accomplished by a double precision transfer of two 36-bit words.

A.2.1 D BUS: INPUT DATA BUS (cont.)

Data Formats

There are two possible data formats on the "D" bus. The data formats on the "D" bus are as follows:



A.2.2 U BUS: OUTPUT DATA BUS

Information from the central to the channel appears on the U bus in one of three separate formats:

(1) PCW information - The PCW obtained as a result of a connect operation is sent to the channel on the U bus. The information is not reformatted by the channel, but is placed on the U-bus exactly as it was obtained from the store.

(2) DCW information - A DCW obtained during a list service is placed on the U bus so that the channel may extract address extension character position and action code information.

(3) Data - Data intended for a channel is placed on the U bus, right justified (i.e., a 9-bit character will be placed on U 27-35).

A.2.3 C BUS: CONTROL BUS

The 11-bit C bus is defined as follows:

- Channel Initialize - Upon receipt of this signal all channels are required to go to a masked condition. CIN will appear as a negative level for more than 1 microsecond.
- Scan, Double and Data - These signals govern the interaction between the channels and the central
- Channel Request for Service - A channel initiates service by placing this line to the "0" state (see paragraph 4.3).

A.2.3 C BUS: CONTROL BUS (cont.)

- TLO, TL1 - (Tally Indicators) - These two bits indicate the contents of the tally field for three general conditions:

  a) Indirect Data Service: DCW tally after updating.

  b) List Service, except Connect Channel: DCW tally as it will be placed in the mailbox.

  c) List Service, Connect Channel: These flags are not applicable during service to the connect channel.

  The bits are coded as follows:

TLO	TL1	Tally Value
0	0	Zero or greater than three
0	1	One
1	0	Two
1	1	Three

- System Fault - The central will place a "0" on this line to indicate that it has detected a System Fault. A channel is required to go into a masked state upon receiving a System Fault indication.

- User Fault - These three lines are encoded to provide the channel with User Fault information whenever the central has detected a User Fault (see paragraph 4.4.2).

US0	US1	US2	Fault
0	0	0	No User Fault
0	0	1	LPW Tally runout (not connect channel)
0	1	0	2 TDCW's in succession
0	1	1	Boundary Error
1	0	0	Address control change in restricted mode
1	0	1	IDCW in restricted mode
1	1	0	Character Size discrepancy
1	1	1	Parity error on Data bus

A.2.4 N BUS: CHANNEL NUMBER BUS

This 6-bit bus indicates the channel which is to respond to a Peripheral Control Word (PCW). The channel number will be provided only in conjunction with a connect service (i.e., it will not be "wrapped back around" to a channel during data, list, status, etc.)

Prepared by: _____

L. K. Hooker Date
Systems Design Engineering

Approved by: _____

C. W. Dix, Director Date
Engineering

_____

W. W. Castor, Director Date
Large Systems Product Marketing

_____

W. M. Gaines Date
Program Director
Large Systems Program Management

Reviewed By

_____

C. T. Clingen, Manager Date
CISL

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C. A. Conover, Manager Date
Advanced Systems Engineering

_____

R. L. Ruth, Manager Date
Computer Design Engineering

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R. F. Stevens, Manager Date
Operating Systems Engineering

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P. F. Straka, Manager Date
Systems Maintainability Eng.

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L. I. Wilkinson, Manager Date
Systems Engineering

_____

T. J. Beatson, Manager Date
System Software Design

_____

S. F. Gangi, Manager Date
600 I/O System Software

_____

J. R. Guilford, Manager Date
I/O Design Engineering

_____

G. R. Williams, Manager Date
Systems Design Engineering