HONEYWELL EDP

HARDWARE BULLETIN

SERIES 200

TYPE 281-2B COMMUNICATION CONTROL AND TYPE 285-2B COMMUNICATION ADAPTER

SUBJECT: Equipment Specifications - the Type 281-2B Single-Channel Communication Control and the Type 285-2B Communication Adapter

SPECIAL INSTRUCTIONS: This bulletin supersedes the bulletin entitled Model 281-2B and Model 285-2B Single-Channel Bit-Stream Synchronous Communication Control Units, File No. 412.0007.1100.00.00. References used are as follows: the bulletin entitled Types 286-1, -2 and -3 Multi-Channel Communication Controls, Including Features 086 and 087, Order No. 160, the Honeywell Series 200, Models 200/1200/2200 Programmers' Reference Manual, Order No. 139; the Honeywell Series 200, Model 120 Programmers' Reference Manual, Order No. 141.

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THE TYPE 281-2B SINGLE-CHANNEL COMMUNICATION CONTROL AND THE TYPE 825-2B COMMUNICATION ADAPTER

I. GENERAL DESCRIPTION

The Honeywell Type 281-2B Communication Control and Type 285-2B Communication Adapter provide the interconnection of a Series 200 central processor with a remote terminal on either switched, voice-grade telephone lines or leased point-to-point voice-grade private lines. Both the Types 281-2B and 285-2B are connected to the line by means of the Bell DATA-PHONE Datasets 201A or 201B. The same model dataset is required at each end of the given transmission line. The communication control or adapter is directly compatible with all Series 200 central processors except the Type 121; compatibility with the Type 121 central processor requires the presence of either Feature 1015 or Feature 1016 (see the Model 120 Programmers' Reference Manual, pages 1-15 and 1-16).

Figure 1, page 2, illustrates typical applications of the Types 281-2B and 285-2B. The Type 281-2B connects one voice-grade telephone line to a Series 200 central processor. The Type 285-2B is used in conjunction with a Type 286 Multi-Channel Communication Control to connect one voice-grade telephone line to a Series 200 central processor when a maximum of 63 lines are to be connected.

The line is characterized by bit-stream synchronous transmission of data in two-way, non-simultaneous, half-duplex mode. The synchronizing clock is supplied in the dataset. The transmission code may be Honeywell, ASCII (American Standard Code for Information Interchange), or others whose transmission line character length is eight bits (see Sections IV and VII).

When the Bell DATA-PHONE Dataset 201A is present, the Types 281-2B and 285-2B transmit at the rate of 250 characters (or 2000 bits) per second; when the Bell Dataset 201B is present, they transmit at the rate of 300 characters (or 2400 bits) per second.

The remote terminals (Figure 1) consist of a Series 200 central processor equipped with a Type 281-2B Communication Control, or a Series 200 central processor equipped with a Type 286 Multi-Channel Communication Control and a Type 285-2B Communication Adapter Unit.

Other computers and high-speed devices utilizing Bell Dataset 201A or 201B, and conforming to the code and format restrictions discussed in Section IV, may also be used.

One standard Series 200 logic drawer contains one Type 281-2B Communication Control or eight Type 285-2B Communication Adapters.

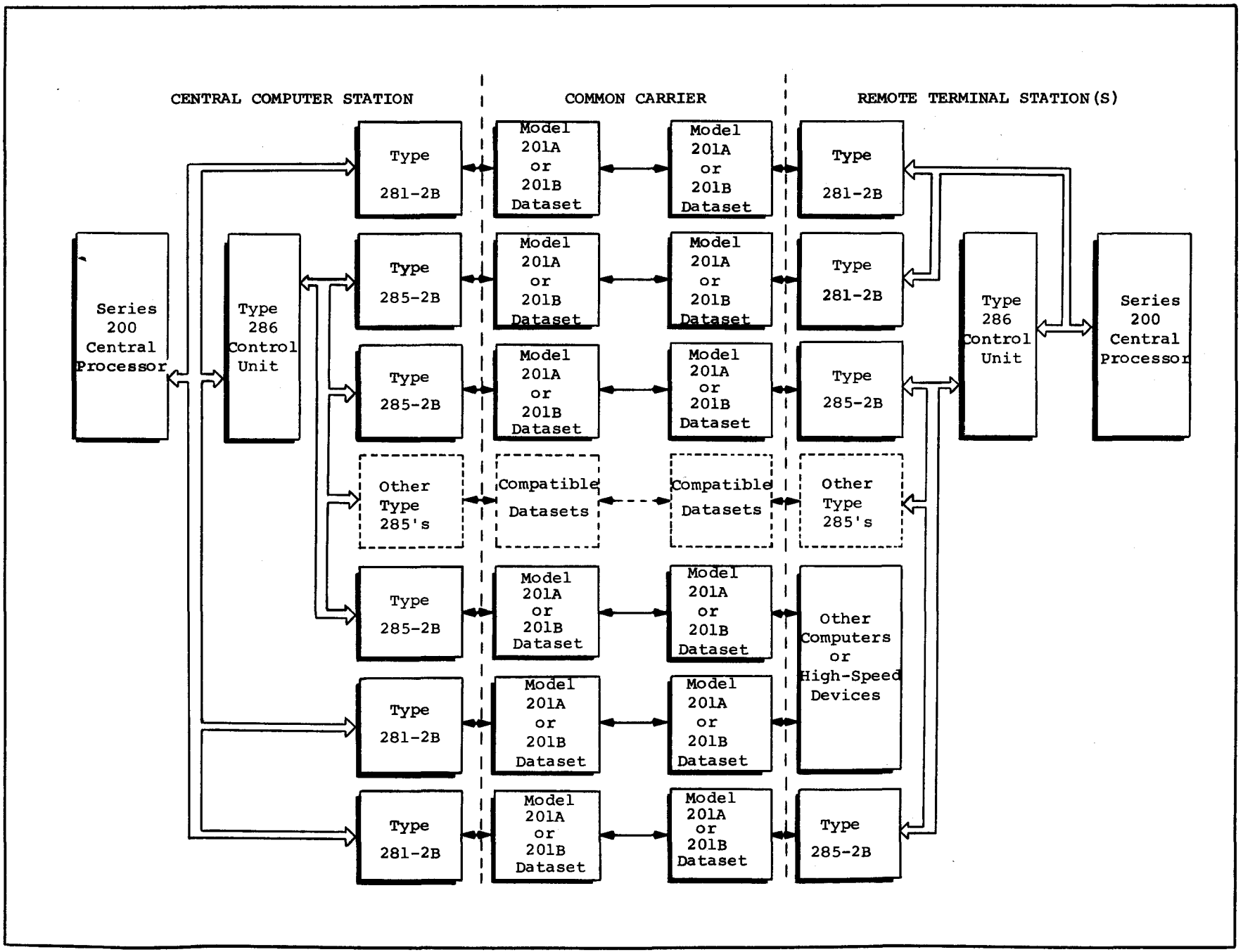


Figure 1. Typical Applications for Types 281-2B and 285-2B

II. INTERFACE

A. Type 281-2B Interface with Series 200 Central Processor

Standard peripheral interface logic for non-simultaneous input and output connects the Type 281-2B to the standard Series 200 peripheral bus.

B. Type 285-2B Interface with Type 286

Section IV of the Honeywell bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls describes this interface circuit.

III. DATASET/CONTROL INTERFACE

A. Common-Carrier Line Termination

The common-carrier line termination is a Bell Dataset 201A or 201B. The maximum permissible cable length is 50 feet.

B. Signals

The signal and control leads on the 201A and 201B meet the Electronic Industries Association specifications as outlined in Documents Number RS232 and RS232A. The datasets convert the voltage-level signals of the Types 281-2B and 285-2B to audio-frequency signals for transmission on the line.

IV. CODE CHARACTERISTICS AND FORMAT

A. Codes

The Types 281-2B and 285-2B are designed to handle transmission codes of eight - or fewer - bits per character. Line signals, however, are transmitted or received in an eight-bit-per-character format. For Series 200 central processors, this line format entails using two six-bit main memory locations to store each eight-bit line character. Bits 1 through 6 are placed in the rightmost (n+1) memory location and bits 7 and 8 are placed in the leftmost (n) location.

If parity checking and generation are provided, the eighth bit of each character is the parity bit; it is supplied and checked by the control unit.

1. Type 281-2B Control Character Recognition

The Type 281-2B Communication Control is provided with selectable character-recognition ability to aid system efficiency and to provide flexibility in operating with different transmission codes and formats. The Type 281-2B is thus able to recognize a maximum of six characters and - on recognition - to take various control actions (see Section VI,B) without central processor intervention. The characters and control actions may be selected by jumper cards according to system requirements.

The Honeywell and ASCII (see Tables I and II, pages 5 and 6, respectively) are the two most notable codes. Control characters for both of these codes are the standard ASCII control characters. Several of the control characters are recognized by the Type 281-2B and they initiate various actions in the communication control, as described in Section VI,B,1.

2. Type 285-2B Control Character Recognition

The Type 285-2B Communication Adapter, utilized with the Type 286 Multi-Channel Communication Control, has provision for recognizing only synchronization characters. All other character recognition must be accomplished by means of central processor programming. Control characters are selected and recognized by program to meet system requirements (see Section VII).

B. Message Format

The general line format is as follows:

Synchronization Character	Start-of-Message Character	Data Characters	End-of-Message Character	LRC Character

The major line format requirement is that each message be preceded by at least two synchronization characters; actually, provision of four synchronization characters is recommended. End-of-message character recognition is also necessary in systems where variable-length messages are used. A longitudinal redundancy check (LRC) character (see Section VI,E,2) may follow an end-of-message (EOM) character. A typical message sequence for the Type 281-2B is demonstrated in Table III, page 7.

Table I. Honeywell 6-Bit Code

High-Speed Printer	Octal Code	Binary Code	High-Speed Printer	Octal Code	Binary Code
0	00	000000	-	40	100000
1	01	000001	J	41	100001
2	02	000010	K	42	100010
3	03	000011	L	43	100011
4	04	000100	M	44	100100
5	05	000101	N	45	100101
6	06	000110	O	46	100110
7	07	000111	P	47	100111
8	10	001000	Q	50	101000
9	11	001001	R	51	101001
'	12	001010	#	52	101010
=	13	001011	$	53	101011
:	14	001100	*	54	101100
Space	15	001101	"	55	101101
>	16	001110	≠	56	101110
&	17	001111	!	57	101111
+	20	010000	<	60	110000
A	21	010001	/	61	110001
B	22	010010	S	62	110010
C	23	010011	T	63	110011
D	24	010100	U	64	110100
E	25	010101	V	65	110101
F	26	010110	W	66	110110
G	27	010111	X	67	110111
H	30	011000	Y	70	111000
I	31	011001	Z	71	111001
;	32	011010	@	72	111010
.	33	011011	,	73	111011
)	34	011100	(	74	111100
%	35	011101	C_R	75	111101
■	36	011110	□	76	111110
?	37	011111	¢	77	111111

NOTE

Bit 7 must be a one. Bit 8 is the parity bit.

Table II. American Standard Code for Information Interchange

b_7 b_6 b_5 →	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
Bits b_4 b_3 b_2 b_1 ↓	Column →	0	1	2	3	4	5	6	7
Row ↓									
0 0 0 0	0	NUL	DLE	SP	0	\	P	@	p
0 0 0 1	1	SOH	DC1	!	1	A	Q	a	q
0 0 1 0	2	STX	DC2	"	2	B	R	b	r
0 0 1 1	3	ETX	DC3	#	3	C	S	c	s
0 1 0 0	4	EOT	DC4	$	4	D	T	d	t
0 1 0 1	5	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	6	ACK	SYN	&	6	F	V	f	v
0 1 1 1	7	BEL	ETB	'	7	G	W	g	w
1 0 0 0	8	BS	CAN	(	8	H	X	h	x
1 0 0 1	9	HT	EM	)	9	I	Y	i	y
1 0 1 0	10	LF	SS	*	:	J	Z	j	z
1 0 1 1	11	VT	ESC	+	;	K	[	k	{
1 1 0 0	12	FF	FS	,	<	L	~	l	|
1 1 0 1	13	CR	GS	-	=	M	]	m	}
1 1 1 0	14	SO	RS	.	>	N	^	n	~
1 1 1 1	15	SI	US	/	?	O	_	o	DEL

CONTROL CHARACTERS

NULL Null/Idle
SOH Start of Heading (CC)
STX Start of Text (CC)
ETX End of Text (CC)
EOT End of Transmission (CC)
ENQ Enquiry (CC)
ACK Acknowledge (CC)
BELL Audible or attention signal
BS Backspace (FE)
HT Horizontal Tabulation (punch card skip) (FE)
LF Line Feed
VT Vertical Tabulation (FE)
FF Form Feed (FE)
CR Carriage Return (FE)
SO Shift Out
SI Shift In

DLE Data Link Escape (CC)
DC1, DC2, DC3 } Device Controls
DC4 Device Control (stop)
NACK Negative Acknowledge (CC)
SYNC Synchronous Idle (CC)
ETB End of Transmission Block (CC)
CNCL Cancel

EM End of Medium
ESC Escape
FS File Separator (IS)
GS Group Separator (IS)
RS Record Separator (IS)
US Unit Separator (IS)
DEL Delete

NOTE

(CC) Communication control
(FE) Format effecter
(IS) Information separator

Table III. Type 281-2B Typical Message Transmission Sequence (Honeywell Code, No Hardware LRC Option, and Parity Present)

CHARACTER	CENTRAL PROCESSOR	CONTROL UNIT
SYNC CHARACTERS	000000 010110	P0010110
	000000 010110	P0010110
	000000 010110	P0010110
	000000 010110	P0010110
DATA CHARACTERS	000001 010111	P1010111
	000001 110111	P1110111
	000001 111010	P1111010
	000001 010101	P1010101
ETX	000000 000011	00000011
	LRC Character	LRC Character
		Release of RWC Interrupt Function Set

P = Parity

V. RECOMMENDED OPERATIONAL PROCEDURES

A. Attended Operation

The basic steps occurring during manual operation are as follows:

1. The communication programs are loaded into memory and the peripheral devices are readied.

2. An operator at either station calls the other by means of the dataset handset. The operators agree verbally on procedures.

3. The communication programs are activated.

4. The operators press the dataset DATA buttons.

NOTE

If the handset is cradled in a switched-circuit service system, a "time-out" and line release occur when no activity is detected on the line within 30 seconds. No line release occurs if the handset is not cradled; in this case, an attempted line release changes the dataset from DATA to TALK. Attempted line release has no effect on non-switched circuit private-leased lines.

5. The transmitter sends out a control block inquiring whether the receiver is ready or not ready to accept data. The block is retransmitted at programmed time intervals until an appropriate "acknowledge" control block is accepted from the receiver.

6. The transmitter sends out data blocks; an "answer back" is generally required for each data block sent.

7. When the last block is acknowledged correctly, an end-of-transmission (EOT) control block is sent by the transmitter.

8. The receiver acknowledges receipt of the EOT control block by returning its own EOT block.

9. Because transmission is now complete, the operators are alerted and any of these actions may be executed -

   a. The operators may converse with each other (handset off cradle, dataset in talk mode);

   b. The operators may release the line manually (handset in cradle, dataset in talk mode);

c. "Time-out" may release the line (handset in cradle, dataset in data mode);

d. Program action may release the line, as described in Section VI,A,4,d (handset in cradle, dataset in data mode).

B. Advanced Operational Procedures for the Type 281-2B

A more advanced operational procedure - available to the Type 281-2B Communication Control - than that described in the foregoing Section V,A, employs both datasets in the unattended answering mode and computers having the interrupt capability. In this procedure, once step 1 in Section V,A, has been completed, no operator intervention is required at the receiving station (see Section VI,A,4,d).

VI. PROGRAMMING REFERENCE DATA FOR THE TYPE 281-2B

A. General Considerations

1. Variable-Length Block Data Transfer

The Type 281-2B transfers data in blocks of characters. These blocks may vary in length. The upper limit of their size is determined by the computer's main memory capacity and the data storage facilities available in the terminal equipment.

A block may be broken into smaller blocks (sub-blocks) and these sub-blocks may be chained together in transfer so that data flow is continuous. The initial transfer in each block must reference a sub-block of at least two characters in length. Character-by-character transfer can occur after the initial transfer of this two-character sub-block.

2. Codes

The Type 281-2B is able to transmit and receive codes whose character length is eight bits or less. Line-signal character length is eight bits in all cases.

3. Bell Datasets 201A and 201B

The Type 281-2B Communication Control can be used with either Bell Dataset 201A or 201B. As described in the fourth paragraph of Section I, the transmission rates for the Datasets 201A and 201B are 2000 and 2400 bits per second, respectively.

4. System Requirements

a. Interrupt Capability

The interrupt capability (Models 200/1200/2200 Programmers' Reference Manual, Appendix D) is standard on all Series 200 central processors except the Type 201; here, Feature 012 -

Program Interrupt - provides this capability (Models 200/1200/2200 Programmers' Reference Manual, page 1-16).

The Type 281-2B Communication Control can be used in conjunction with the Type 201 central processor even though Feature 012 is not present. However, central processor operations are somewhat restricted if the optional Feature 012 is not present.

b. Feature 087, Longitudinal Redundancy Check (LRC)

If longitudinal-redundancy-check character computation and checking is to be accomplished by hardware, Feature 087 should be present.

When Feature 087 is present, the user must specify:

1. Whether the eighth bit is the parity of the LRC character;

2. Whether the eighth bit is the half-add sum of the parity bits in the characters sent or received before the LRC characters;

3. Whether the eighth bit is a constant one or zero;

4. Whether the LRC character should be the half-add sum or the complement of the half-add sum of the characters preceding it.

c. Parity Generation/Checking Capability

The user may select even-parity check/generation, odd-parity check/generation, or no parity check.

NOTE

Parity is normally checked and generated in the 8-bit of each character. It is therefore necessary for the customer to specify how the 8-bit of any LRC character is to be handled. This must be specified if the hardware LRC option is present or if a programmed LRC character is to be developed.

d. Unattended Operation Capability

When this capability is present (see Section V,B), the dataset answers incoming calls without operator intervention. The central processor is interrupted when synchronization is established, and a Peripheral Control and Branch (PCB) instruction enables unattended phone "hang-up" upon completion of transmission.

e. Type 213-3 Interval Timer and Type 213-4 Time-of-Day Clock

These product-line peripheral units are used in conjunction with communication equipment.

B. Control Characters

1. ASCII and Honeywell Codes

Standard ASCII control characters (see Table II, page 6) are used in transmission of ASCII and Honeywell codes. These ASCII characters are distinguished by a zero located in the seventh bit position. When the Honeywell code is used, the program provides the data characters with a one in the seventh bit position. Thus, Honeywell data characters are distinguished from control characters.

The following three ASCII control characters are recognized.

a. Synchronization Character (SYNC) P0010110

At least two consecutive synchronization characters must be recognized before synchronization is achieved. To ensure proper synchronization, at least four SYNC characters should be transmitted before each block.

The SYNC characters are generated by program - they are designated as octal 26's with a zero in the seventh bit position. These characters - when received by the Type 281-2B Communication Control - are filtered (see Section VI,B,2,a and b) and not transferred to the central processor.

b. Termination Characters

There are two termination characters: end-of-text (ETX), P0000011 and end-of-transmission block (ETB), P0010111.

Termination control characters ETX and ETB facilitate automatic termination of data transfer instructions. Such automatic termination is necessary when character blocks of variable lengths are sent. Termination procedures are similar to those occurring when a record mark is sensed in memory (see Section VI,D).

2. Other Codes

The Type 281-2B is capable of recognizing and responding to six control characters. Any of these may be selected to initiate various actions necessary to the operation of a particular communication system. Upon character recognition, the following actions may be taken:

a. Filter

The character recognized is not transferred to the central processor.

b. Achieve Synchronization

The character (SYNC) recognized is used to achieve synchronization. For any system, only one character may be so specified. Usually this character is also selected to actuate step a., Filter, so that it will not be transferred to the central processor.

c. Interrupt

The recognized character causes Interrupt to be set in the communication control.

d. Terminate

Character recognition causes the beginning of termination procedures (see Section VI,D).

e. Inhibit Recognition

The recognized character causes the character-recognized circuit to be inhibited on the next character.

f. Inhibit Parity

Character recognition causes the inhibition of parity generation and checking on the next character.

g. RWC Release

Character recognition causes the release of the read/write channel.

h. Inhibit LRC Current

Character recognition is not included in LRC computation.

i. Inhibit LRC Next

Character recognition prohibits inclusion of the next character in the LRC computation.

j. Check/Deliver LRC Next

Character recognition notifies the communication control that the next character to be received or sent is the LRC character. The communication control takes appropriate action.

NOTE

The above actions may also be effected by using the PCB instructions "Unassigned PCB" shown in Table V, page 23.

C. Transmit/Receive

Table IV, below, shows the general conditions required to set or reset the communication control interrupt.

Table IV. Communication Control Interrupt

Interrupt Condition	Condition
Set	When a record mark is sensed while a "Transmit" PDT instruction is active.
Set	When a record mark is sensed while a "Receive" PDT instruction is active.
Set	When a termination control character is received on the line while a "Receive" PDT instruction is active.
Set	When an inactivity error occurs. NOTE The above actions also cause RWC release.
Set	When a user-selected character is recognized. This can occur only after synchronization has been achieved (see Section VI,B,2).
Set	When synchronization has been achieved.
Reset	When a "Reset Interrupt Condition" PCB instruction (C3 = 75) is issued.
Reset	When a PDT ("Receive" or "Transmit") instruction is issued.
Reset	When a "Reset Interrupt/Allow Condition" PCB instruction (C3 = 70) is issued.
Reset	When the INITIALIZE button is depressed on the central processor control panel.

1. Transmit

A "Transmit" PDT instruction may not be issued until the "Output Request" PCB instruction is satisfied. When a PDT instruction is issued, the unit becomes "busy" and the "Output Request" PCB instruction is no longer satisfied.

NOTE

If reception has just been terminated, the "Output Request" PCB instruction will not be satisfied for two character-times.

The "Transmit" PDT instruction transfers six-bit frames from memory to the communication control. Two six-bit frames are used by the communication control to form one eight-bit line character. Thus, the control discards the leftmost four bits of each frame-pair sent from the central processor.

If the communication control provides parity, the eighth-bit position of the line character contains the parity bit and the corresponding bit coming from the central processor is discarded. If the communication control does not provide parity, or if it inhibits parity, the eighth bit is supplied by the central processor.

The first frame-pairs sent by the central processor must be SYNC characters; data characters follow. Any ASCII control characters other than those discussed in Section VI,B,1, are treated by the control as data characters.

Procedures for terminating transmission begin when a record mark is sensed by the control. Termination procedures are discussed in Section VI,D.

NOTE

If required by the given communication system, termination may also occur when a control character is sensed.

2. Receive

The first recognized group of two SYNC characters arriving in succession over the line sets the Interrupt condition in the communication control.

NOTE

If required, the control Interrupt condition may be set by a selected start-of-text (STX) character, with no interrupt occurring when synchronization is achieved.

The "Input Request" PCB instruction is recognized at this time. After the "Input Request" PCB instruction is satisfied, a "Receive" PDT is issued without a demand and no data is received for two character-times, the read/write channel is released and no inactivity error occurs (see Section VI,E,3,b).

Upon receiving a PDT instruction to receive, the communication control receives from the line and transfers data characters to the central processor. For every eight-bit line character received, the communication control sends two six-bit frames to the central processor. One six-bit frame is transferred at a time.

The leftmost four bits of the frame-pair are sent to the central processor as zeros. Thus, if parity is provided, the parity bit is transferred to the central processor.

The first frame-pairs received by the communication control are synchronization (SYNC) characters. These are filtered out by the communication control; they do not reach the central processor. Data characters follow the SYNC characters. The ASCII code control characters - other than those discussed in Section VI,B,1 - are treated by the communication control as data characters.

Procedures for terminating transmission begin when either a record mark or one of the termination characters is sensed by the control. Termination procedures are discussed in Section VI,D.

D. Termination Procedures

1. Record Marks

Record marks are sensed in memory when a character is transferred to the central processor or from it.

a. Reception

When a record mark is sensed in memory, the read/write channel is released, the Interrupt condition is set and the "Input Request" PCB instruction is satisfied. The communication control continues to receive information from the line for two character times, then terminates reception. Termination of reception involves stopping the control clock,

loss of synchronization, turning off the "Input Request" PCB instruction, and turning on the "Output Request" PCB instruction.

If a PDT instruction is issued and the read/write channel regained within N character-times after the interrupt occurs, or after the "Input Request" PCB instruction is satisfied, then termination as described in the preceding paragraph does not occur. Instead, reception continues as before with no loss of data. This is called "chaining" a PDT instruction.

The number of character-times (N) is dependent upon the number of characters (M) transferred by the PDT instruction before the interrupt occurred, or before the "Input Request" PCB instruction was satisfied. If M=1, then N=1; if M>1, then N=2.

b. Transmission

When a record mark is sensed in memory, the read/write channel is released, the Interrupt condition is set, and the "Output Request" PCB instruction is satisfied. The communication control continues to transmit characters from its two registers onto the line for two character-times; then it terminates transmission by stopping the control clock.

If a "Transmit" PDT instruction is issued and the read/write channel is regained within (N) character-times, then chaining of the "Transmit" PDT instruction is possible.

The number of character-times (N) is dependent upon the number of characters (M) transferred by the PDT instruction before the interrupt occurred, or before the "Output Request" PCB instruction was satisfied. If M=1, then N=1; if M>1, then N=2.

2. Position of Record Marks in Memory

a. Reception

During character reception, a record mark is placed in the rightmost memory position of the last frame-pair to be received. Thus, if the last frame-pair received is placed in memory positions 41 and 42, the record mark is placed in position 42.

b. Transmission

During character transmission, a record mark is placed in the next memory position after the last character to be transmitted. Thus, if the last frame-pair of a block transmitted is located in memory positions 40 and 41, the record mark is placed in position 42.

3. Termination Control Characters

After the character recognition mechanism has sensed the reception of a termination control character and that character has been transferred to the central processor, the communication control terminates activity as it would if a record mark were sensed.

NOTE

An LRC character may be present after the termination character, as discussed in Section VI,E,2.

E. Error Checking

1. Parity Error

If the parity checking ability of the communication control is utilized, a parity bit is generated both on transmitting and receiving each character. These bits are compared after each character is received (with the possible exception of the LRC character) and a Parity Error condition is set if they are not equal. The Parity Error condition is tested and reset by a PCB instruction. The Parity Error condition is also reset when a "Transmit" PDT instruction is issued. The condition must be tested within one character time of receipt of the characters being checked.

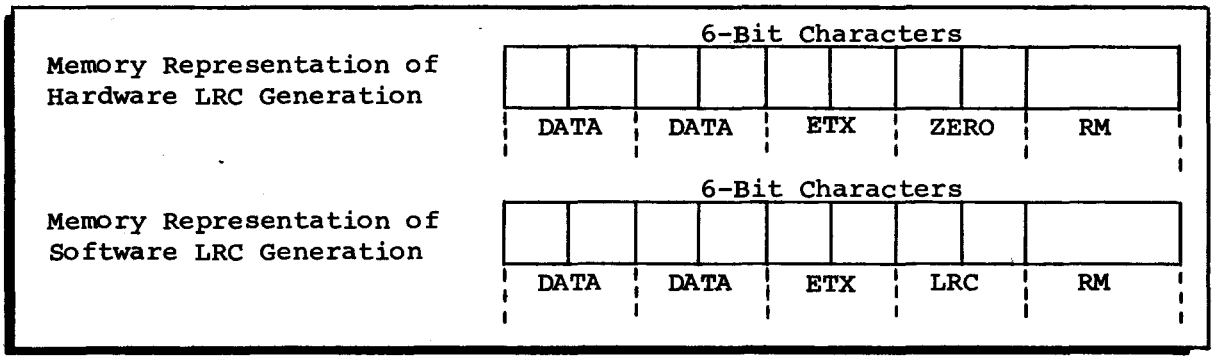
2. Longitudinal Redundancy Check

Upon recognition of a terminal control character, the read/write channel is released and the Interrupt condition is set in the control. In addition, the communication control inhibits character recognition and - if necessary - parity checking or generation on the next LRC character.

a. Transmission

If Feature 087 - the hardware LRC option - is present, an all-zero character (two six-bit frames) is transferred to the communication control after the termination control character. The communication control transmits the LRC character it has developed to the dataset in place of the zero character it received from the central processor.

If Feature 087 is not present, a program-developed LRC character is transferred to the communication control after the termination control character. The communication control forwards this LRC character to the dataset.



b. Reception

If LRC checking is used, a separate PDT instruction is usually issued to receive the LRC character from the line. The "Receive" PDT instruction is issued after the termination control character is received and transferred to the central processor. Receipt of the termination control character is indicated by an interrupt and the normal termination indications described in Section VI,D,1.

This separate PDT instruction to receive the LRC character is unnecessary if fixed-length blocks are transmitted and no control-recognized termination character is used. In this last case, a record mark terminates reception of the whole block, including the LRC character.

If Feature 087 is present, testing of the "Parity/LRC Error" PCB instruction indicates whether an LRC error has occurred. This PCB instruction must be issued within one character-time of receiving the LRC character.

If LRC checking is accomplished by software, then a program-developed LRC character is compared with the received LRC character to determine if an error has occurred.

Usually all characters except SYNC and - if needed - NULL are included in LRC calculations. However, adjustments can be made here to meet system requirements.

3. Device Error

The Device Error condition is tested by a PCB instruction. This condition is set when one of the following errors occur:

a. Timing Error

A timing error occurs if - on receiving data - a PDT instruction has not been issued in sufficient time to take the data from the communication control. A test for this error should be made within two character-times of receiving the last character of a block.

This error is always set two character-times after reception of a complete block of data.

b. Inactivity Error

If a PDT instruction is active but there is no line activity during two character-times, the read/write channel is released, the Interrupt condition in the communication control is set and the Device Error condition is set.

The Device Error condition is reset by one of the following conditions:

1. The INITIALIZE button on the central processor is activated;

2. The "Device Error" PCB instruction is tested;

3. A "Transmit" PDT instruction is issued;

4. Synchronization is achieved.

F. Noise, Synchronization, and Continuous Character Transmission

1. Noise and Synchronization

The Bell Dataset is equipped with an automatic gain control (AGC) amplifier. In the absence of a carrier on the line, the gain of this amplifier is very high. Any noise coming over the line in the absence of a carrier is therefore greatly amplified and may - by chance - have the configuration of a SYNC character.

To minimize the possibility of false synchronization on noise, the communication control achieves synchronization and begins reception only when it has recognized two successive SYNC characters. In normal noise situations, this is sufficient to prevent false synchronization.

2. Continuous Character Transfer

The communication control has the capability of transmitting a character continuously upon direction from the central processor. Once the central processor has issued this direction, no further central processor action is required until a halt of such character transmission is desired. The transmitted character is selected by the central processor under program control. Upon receiving it, the communication control is capable of filtering this character. In this case, the character or characters filtered are fixed and determined by jumper cards in the communication control.

The procedure for generating a continuous character is as follows:

a. Issue the "Continuous Transmission" PCB instruction.

b. Transmit a single-line character using the "Transmit" PDT instruction. The character referenced by the PDT instruction is continuously transmitted.

c. Issue the "Stop Continuous Transmission" PCB instruction. Transmission of the character referenced in b., above, will stop.

   If it is desired to transmit data immediately after continuous character transmission has been halted with no break in line transmission, a "Transmit" PDT instruction must be issued within one character-time of issuing the "Stop Continuous Transmission" PCB instruction.

   This can also be achieved if a "Transmit" PDT instruction is issued before the "Stop Continuous Transmission" PCB instruction. In this case, the read/write channel is held and, when the "Stop Continuous Transmission" PCB instruction is issued, the characters referenced by the PDT instruction are transmitted.

   The continuous character transmission capability can be used to reduce the possibility of false synchronization further by maintaining a signal on the line at all times. It is also useful when dealing with certain formats where long periods of idle-character transmission are necessary.

G. Line Release

Whenever there is no activity (no transmission occurring) on the line, a "time-out" clock starts in the communication control. If no data transfer occurs within 30 seconds, the communication line is released and the Device Error condition is set. A PCB instruction is also available to release the line. It is possible (by jumper card arrangement) to have both the 30 second time-out line release and the PCB line release or the PCB line release alone.

There are no time-out and line release activities in those systems operating on private lines.

H. Instructions

1. "Typical Instructions Using Interrupt Capability" (Honeywell Series 200/1200/2200 Programmers' Reference Manual, pages 1-3 and D-1 through D-5)

Instruction	Function
a. Load Control Register (LRC)	Loads the registers that are affected in the interrupt loop.
b. Store Control Register (SCR)	Stores the registers that are affected in the interrupt loop.
c. Peripheral Control and Branch (PCB)	Checks for errors and busy conditions, resets Interrupt and Allow conditions, and determines which trunk caused an interrupt.
d. Peripheral Data Transfer (PDT)	Instruction used to transmit and receive data.
e. Resume Normal Mode (RNM)	Used to return to the normal sequence of instructions from the Interrupt loop.

2. Typical Instructions Without Interrupt Capability

The PCB and PDT instructions in c and d of Section VI,H,1, above, also apply here.

Continuous testing of the communication control with "Input" or "Output" PCB instructions tells the central processor when to issue a "Receive" or "Transmit" PDT instruction. When a PDT instruction is issued, the communication control becomes busy.

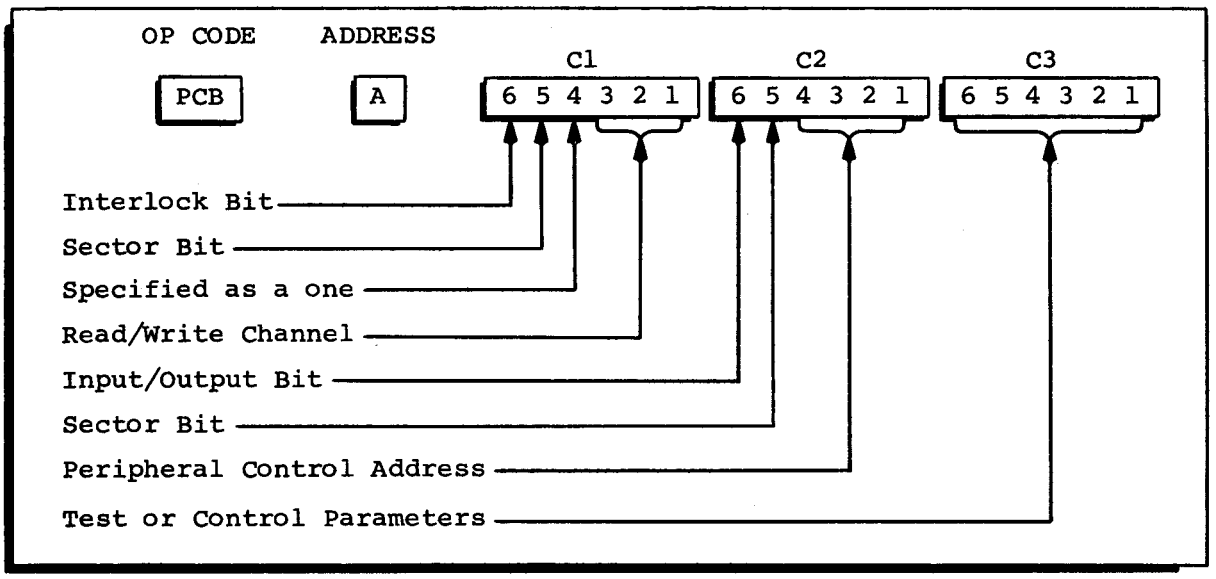
The communication control becomes busy when -

a. A PDT instruction is being implemented, and

b. The dataset is not operative (conditions to be defined).

3. PCB Instruction Format

The following PCB instruction format is for all Series 200 central processors.



A Address - Memory location to which the program will branch (in a branching PCB instruction) if the condition tested for by the PCB instruction is true or if an action cannot be effected.

Interlock Bit - If this bit is a one, high-speed transfer is specified.

Sector Bit - Selects sector 1 (zero) or sector 2 (one). The sector bit in control character C1 must agree with the sector bit in C2.

Read/Write Channel (RWC) - Selects the RWC between main memory and a peripheral communication control. The low-order three bits of C1 contain the number of the read/write channel to be tested for availability and must be set to zero if no RWC is to be tested.

Sector 1	Sector 2
RWC1 = 001001	RWC4 = 011001
RWC2 = 001010	RWC5 = 011010
RWC3 = 001011	RWC6 = 011011
RWC1'= 001101	RWC4'= 011101

Input/Output Bit - Zero = Transmit data from memory to communication control.

One = Receive data from communication control.

Sector Bit - Selects input/output sector 1 (zero) or sector 2 (one). The sector bit in C1 must agree with the sector bit in C2.

Peripheral Control Unit (PCU) - Logical address of the communication control.

Test or Control Parameters - See Table V, pages 23 and 24 for coding of C3 characters.

Table V. PCB C3 Character Coding (Type 281-2B Only)

INSTRUCTION	DESCRIPTION	VARIANT (C3-octal)
	BRANCHING	
Device Busy	Is the communication control busy? If yes, branch to A address. If no, program continues in sequence. (See Section VI,H,1).	10
Parity Error LRC Error	Is the Parity/LRC Error condition set? If yes, branch to A address. If no, program continues in sequence.	40
Device Error	Is the Error condition set? If yes, branch to A address. If no, program continues in sequence.	50
Interrupt	Did unit specified in C2 control character interrupt? If yes, branch to A address. If no, program continues in sequence.	75
Input Request	Should a "Receive" PDT instruction be issued? If yes, branch to A address. If no, program continues in sequence.	61
Output Request	Is the unit capable of accepting a Transmit instruction? If yes, branch to A address. If no, program continues in sequence.	60
Unassigned PCB	To provide additional flexibility for operation with special systems, two unassigned PCB instructions are provided. These PCB instructions can be used to effect any of the control actions listed in Section VI,B. They must be specified by the user and are implemented by a jumper card.	

(continued)

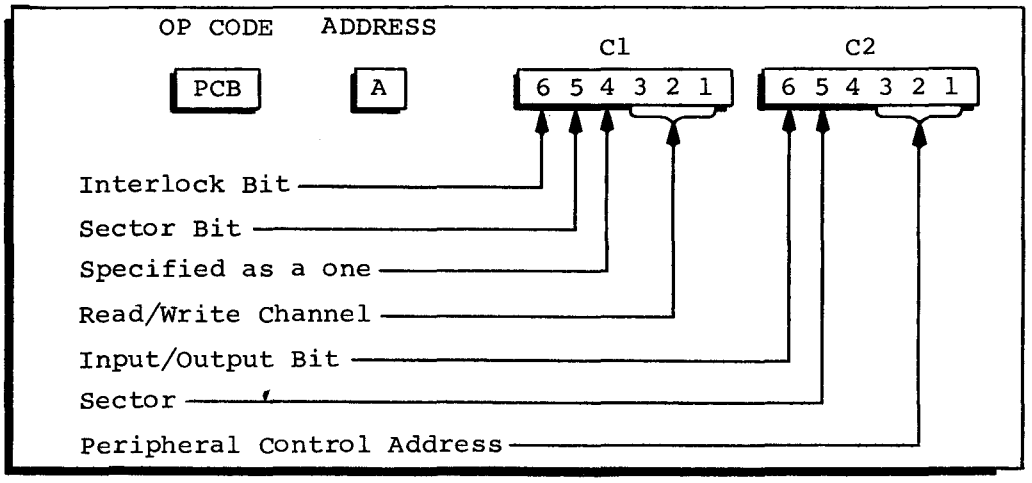
Table V. PCB C3 Character Coding (Type 281-2B Only) (Cont.)

INSTRUCTION	DESCRIPTION	VARIANT (C3-octal)
	NON-BRANCHING	
Set Allow function*	Allow condition in communication control is set.	71
Reset Allow function; Reset Interrupt function*	Allow and Interrupt conditions in communication control are reset.	70
Reset Interrupt function	Interrupt condition is communication control is reset.	74
Hang Up	Hang up the dataset.	27
Continuous Transmission	Continuously transmit the next character sent by a "Transmit" PDT instruction.	21
Stop Continuous Transmission	Halt continuous character transmission.	20

* Both the Allow condition and Interrupt condition in the communication control must be set in order for the central processor to be interrupted.

4. PDT Instruction Format

The following PDT instruction format is for all Series 200 central processors.



A Address - Contains the address of the main memory location to or from which data is transferred in Type 281-2B programming.

Interlock Bit - If this bit is a one, high-speed transfer is implemented.

Sector Bit - Selects sector 1 (zero) or sector 2 (one). The sector bit in C1 must agree with the sector bit in C2.

Read/Write Channel (RWC) - Selects the RWC between main memory and a peripheral communication control.

Sector 1	Sector 2
RWC1 = 001001	RWC4 = 011001
RWC2 = 001010	RWC5 = 011010
RWC3 = 001011	RWC6 = 011011
RWC1'= 001101	RWC4'= 011101

Input/Output Bit - Zero = Transmit data from memory to communication control.

One = Receive data from communication control.

Sector Bit - Selects sector 1 (zero) or sector 2 (one). The sector bit in C1 must agree with the sector bit in C2.

Peripheral Control Unit (PCU) - Logical address of the communication control.

VII. PROGRAMMING REFERENCE DATA FOR THE TYPE 285-2B

A. General Considerations

1. Data Handling Ability

The Type 285-2B Communication Adapter transfers single data bits from the line to the associated buffer in the Type 286 Multi-Channel Communication Control, or from the associated buffer in the Type 286 to the Type 285-2B.

2. Code

The Type 285-2B is capable of receiving or transmitting any code whose character length is eight bits. Each line character is stored in the Series 200 central processor memory in two consecutive locations (see the bulletin Types 286-1, -2 and -3 Multi-Channel Communication Controls). Two codes of particular interest are the Honeywell Code and the ASCII Code, shown in Tables I and II, respectively, on pages 5 and 6.

3. Datasets

The Type 285-2B may be operated with either Bell DATA-PHONE Dataset 201A at 2000 bits per second or Bell DATA-PHONE Dataset 201B at 2400 bits per second.

4. Character Recognition

With the Type 286, the Type 285-2B has the ability to recognize idle characters, thereby obtaining synchronization. The Type 285-2B Communication Adapter Unit acts as a single-bit buffer for the Type 286 Multi-Channel Communication Control.

All other character recognition must be accomplished by program in the central processor.

5. Optional Features

All optional features available to the Types 285-2B/286 are described in the bulletin Types 286-1, -2 and -3 Multi-Channel Communication Controls.

B. Control Characters

Control characters are selected to meet system requirements. Except in the case of the synchronization character, they are recognized by program.

Standard ASCII control characters are used with transmission of ASCII and Honeywell Codes (see Tables I and II). These control characters have a zero in the seventh-bit position of the Honeywell data characters and can be distinguished by the program from the control characters.

C. Programming Requirements

Since the Type 285-2B acts primarly as a single-bit buffer between the dataset and the Type 286, programming requirements are specified in the bulletin Types 286-1, -2 and -3 Multi-Channel Communication Controls.

APPENDIX A

RECOMMENDED MESSAGE FORMATS AND MODE OF OPERATION

A number of message formats, control character sequences, and error control procedures are suggested for users of the Type 281-2B Communication Control and the Type 285-2B Communication Adapter. These suggestions are intended not to restrict the flexibility of the communication equipment but to comply with recommendations contained in the American Standards Association X.3 Task Group paper X3.3.4/63, Error Control Procedures for Data Communications, dated October 1, 1965, and to advance a method of transmission error control that is gaining wide acceptance in the communication industry. The inclusion of a transmission message numbering sequence is suggested to alleviate the possibility of gross error (loss of complete blocks of data) and to keep the allowable number of control sequences to a minimum.

A. Error Control

The following recommendations are offered to standardize the use of character and block parity.

1. Character Parity

Odd character parity should be generated on transmission and checked on reception, whether this is accomplished by the hardware or by programming.

2. Block Parity (Longitudinal Redundancy Check)

Bits 1 through 7 of the LRC character should contain the half-add sums of the corresponding bit positions of all characters following, but not including, the preceding STX character up to and including the ETX character, regardless of whether the LRC character is generated and checked by hardware or by software. Bit 8 should contain an odd-parity check on the LRC character.

B. Hardware Character Recognition

The suggested standards for the use of synchronization, start-of-text, and end-of-text characters are as follows.

1. Synchronization

Synchronization is achieved by the use of ASCII SYNC characters, as described in Section VI,B. Four such characters should precede each message on the Type 281-2B; they are neither included in the computation of the LRC character nor delivered to main memory. Their use with the Type 286 is described in the bulletin Type 286-1, -2, and -3 Multi-Channel Communication Controls.

2. Start-of-Text Character

The start of text is signalled by an ASCII STX character which immediately follows the synchronization characters. The STX character is followed by the message sequence number of a data block or by the control character(s) of a control block, as described below. Recognition of this character causes the generation of an interrupt by the receiving unit. Following the occurrence of an STX character, an ETX character must appear before the next STX character.

3. End-of-Text Character

An ASCII ETX character is used to terminate each data block and each control block; this character always precedes the LRC character. Parity checking should extend one character beyond the ETX character in order to include the LRC character. Recognition of ETX causes the receiving unit to release the read/write channel and generate an interrupt. Following the occurrence of an ETX character, an STX character must appear before the next ETX character.

C. Disconnect

The disconnect feature is required on switched-service networks but not on private-line systems. This feature is activated by a "Special Strobe" PDT instruction on the Type 286, by a special PCB instruction or a 30-second, no activity "time-out" on the Type 281-2B.

D. Data Message Format

The recommended format for a data message is as follows:

SYNC	
SYNC	
SYNC	ASCII
SYNC	
STX	
Sequence Number	
Data Characters	
ETX	ASCII
LRC	

1. Message Sequence Number

The STX character in each data block should be immediately followed by a one-character message sequence number, the value of which changes from one block to the next. The simplest method of sequencing is to use only two sequence numbers which appear alternately. The use of a full set of 64 sequence numbers is recommended for better control of message sequencing. Since the transmitter, in response to a NACK signal, retransmits the last data block (or EOT or TEL control block), the receiver must store the sequence number of the previously received data block in order to reject a duplicate message.

E. Control Message Format

The recommended format for a control message is as follows:

SYNC
SYNC
SYNC
SYNC
STX
Control Character(s)
ETX
LRC

The control character(s) can be any of the following (maximum of two characters).

1. Acknowledge (ACK) - This single ASCII character, sent by the receiver to signify positive response, directs the transmitter to transmit the next data or control block.

2. Negative Acknowledge (NACK) - This single ASCII character, sent by the receiver to signify negative response, directs the transmitter to retransmit the last data or control (except ENQ) block.

3. End of Transmission (EOT) - This single ASCII character is sent by the transmitter to signify the end of transmission. The transmitter must wait for the acknowledgement before disconnecting. The receiver must issue a positive response (ACK) to an EOT character before disconnecting.

4. Enquiry (ENQ) - This single ASCII character is generated by the transmitter to request a response from the receiver. It can be used as an error response to a control message to request a repeat of the last reply-back or control message. If the receiver responds to an ENQ message with a NACK, the transmitter retransmits the previous data or control block. (It is the responsibility of the receiver to store the sequence number of the last block received or the nature of the last control block received in order to avoid duplication.)

5. Telephone Request (TEL) - This two-character ASCII sequence, DLE BELL, can be issued by either terminal and requires a reply by the other terminal. A receiver responds to a TEL message with an ACK message; a transmitter responds with another TEL message. This message signifies that alternate voice communication is desired. It is issued in place of a data message by the transmitter and in place of an acknowledge (ACK) or negative acknowledge (NACK) message by the receiver.

6. Wait Before Transmit (WBT) - This two-character ASCII sequence, DLE RS,, is issued by the receiver in place of ACK or NACK to direct the transmitter to delay its transmission. It should be issued repetitively (to avoid a "time-out" disconnect) until the receiver is ready to accept a normal data message, at which time the pending message should be sent.

F. Transmitter Control Messages

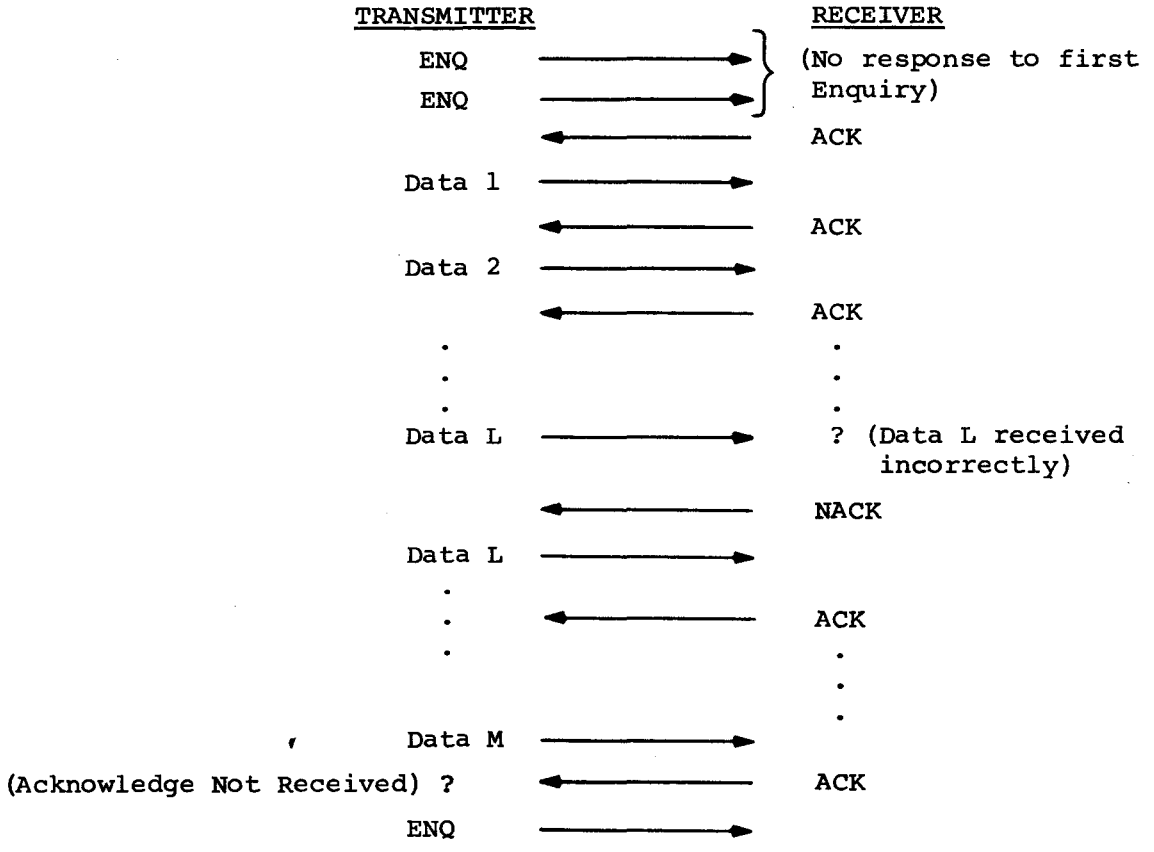
The transmitter always expects a reply when it sends a control message. If no reply is received within n seconds (where n must be less than 30), the transmitter should send an ENQ message. If the transmitter sends three successive ENQ messages with either no reply or garbled replies, it should either attempt an alternate message, such as the telephone request, or else disconnect. If the transmitter receives three consecutive NACK messages, it should send a telephone request to discuss alternate action. Alternatively, the transmitter can automatically disconnect and either wait to be re-called or else redial, as appropriate.

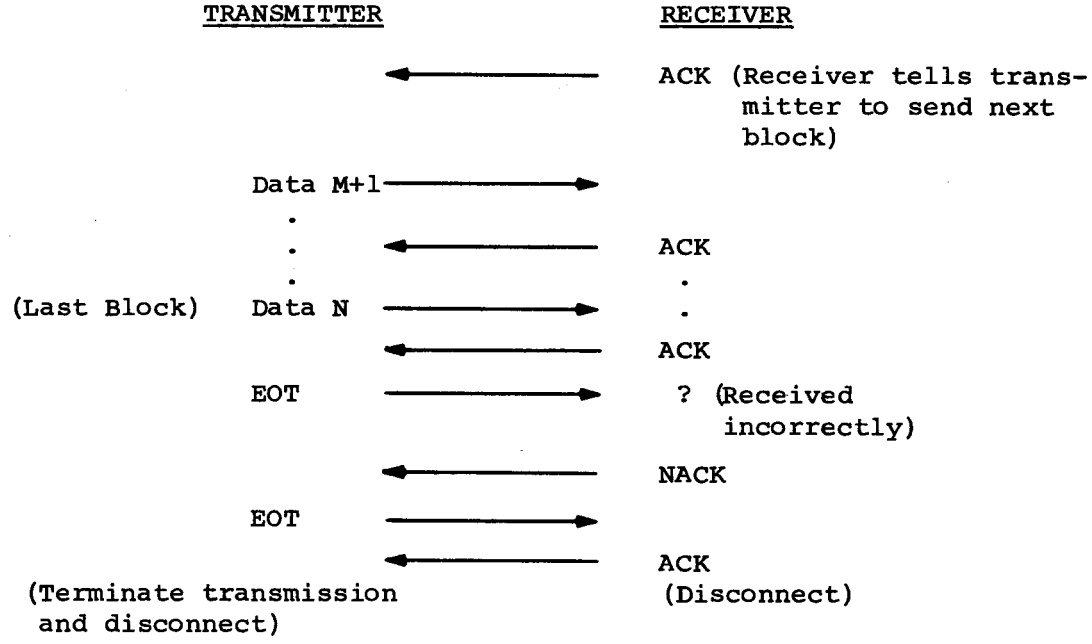
In the examples that follow, ACK, NACK, WBT, TEL, EOT, and ENQ represent control messages; Data 1, Data 2, ...Data N represent data messages.

1. Start-Up Procedure

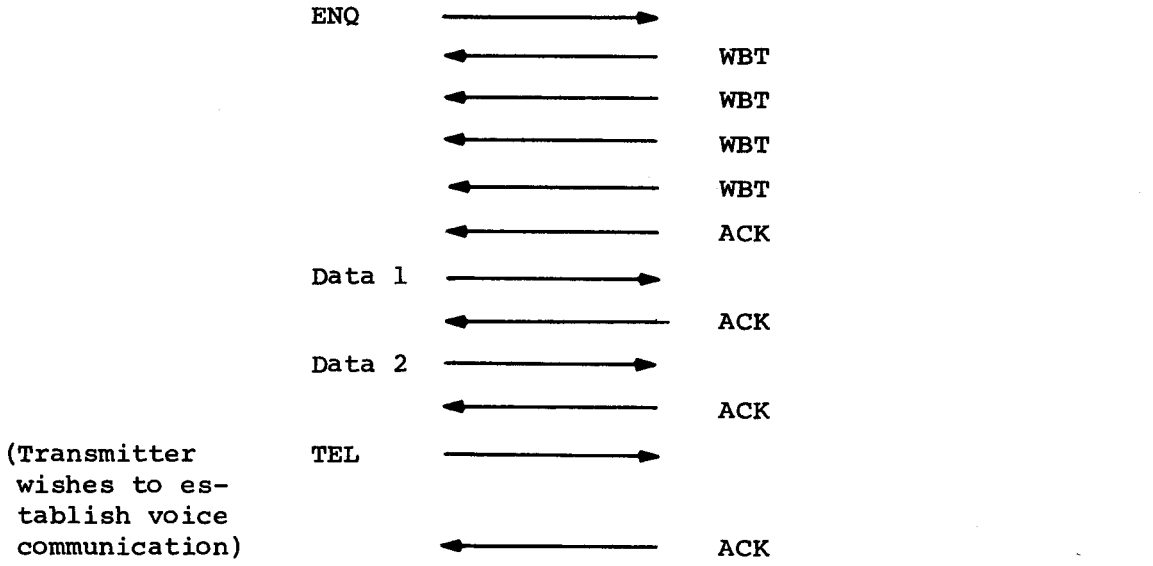
To start transmission, the transmitter sends ENQ messages at n-second intervals until it receives a reply of ACK or WBT. When an ACK message is received, the transmitter sends its first data message.

2. Example 1

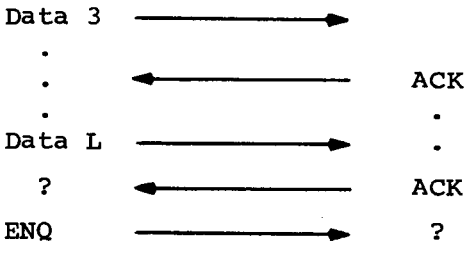


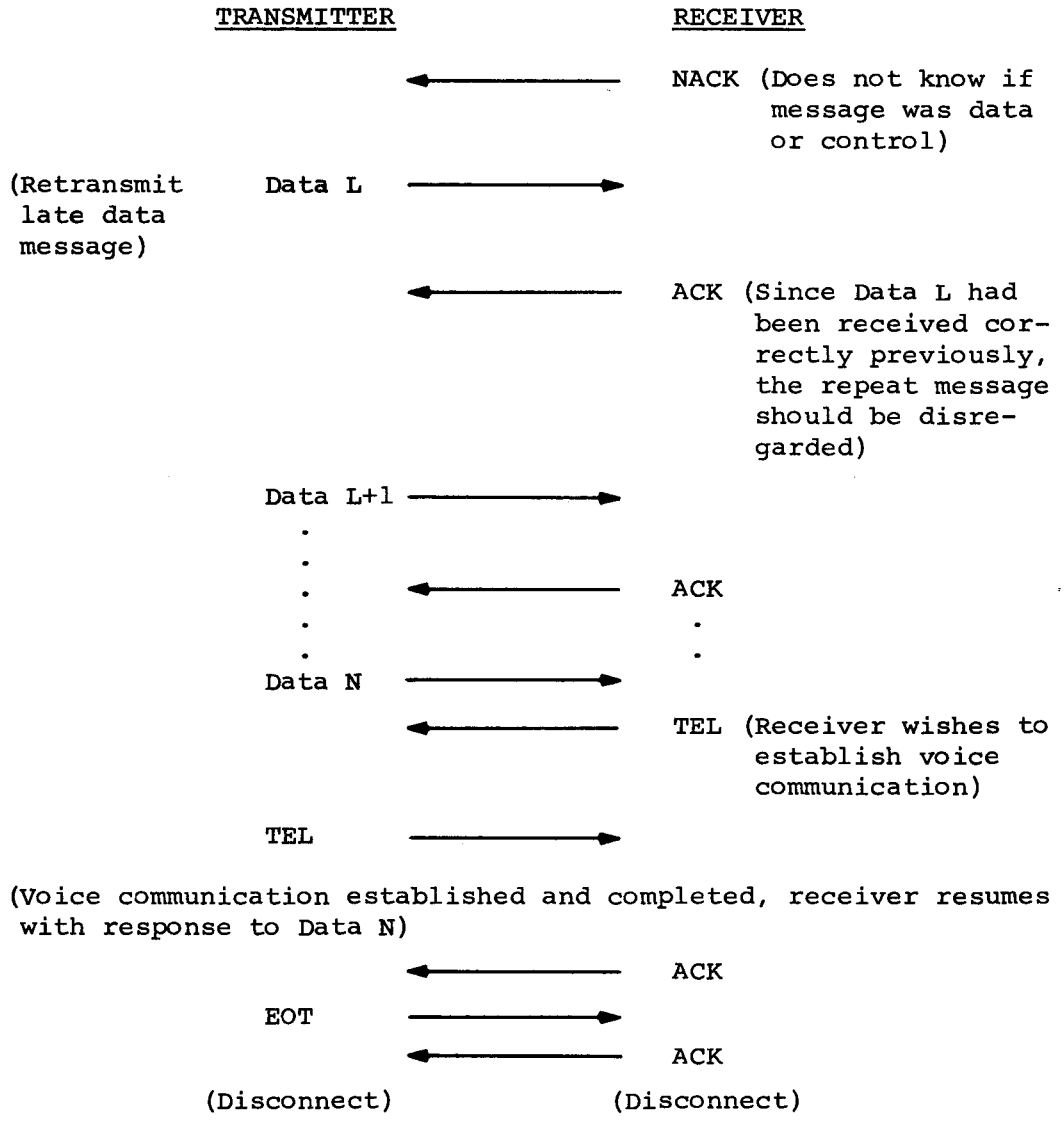


3. Example 2



(Voice communication established and completed, transmitter continues)




TRANSMITTER
RECEIVER
NACK (Does not know if message was data or control)
(Retransmit late data message)
Data L
ACK (Since Data L had been received correctly previously, the repeat message should be disregarded)
Data L+1
ACK
Data N
TEL (Receiver wishes to establish voice communication)
TEL
(Voice communication established and completed, receiver resumes with response to Data N)
ACK
EOT
ACK
(Disconnect)
(Disconnect)

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: SERIES 200 TYPE 281-2B COMMUNICATION CONTROL AND TYPE 285-2B COMMUNICATION ADAPTER HARDWARE BULLETIN

DATED: MAY, 1966

FILE NO: 112.0005.1100.0-063

ERRORS NOTED:

Fold

Cut Along Line

SUGGESTIONS FOR IMPROVEMENT:

Fold

FROM: NAME _____ DATE _____

COMPANY _____

TITLE _____

ADDRESS _____

_____

FIRST CLASS
PERMIT NO. 39531
WELLESLEY HILLS
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BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

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HONEYWELL
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Cut Along Line

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