HONEYWELL EDP

HARDWARE BULLETIN

SERIES 200

TYPE 281-2A COMMUNICATION CONTROL AND TYPE 285-2A COMMUNICATION ADAPTER

SUBJECT: Equipment specifications for the Type 281-2A Communication Control and the Type 285-2A Communication Adapter.

SPECIAL INSTRUCTIONS: References used in this publication include the Series 200 Hardware Bulletins Type 281-2D Communication Control and Type 285-2D Communication Adapter, Order Number 079, and Type 286-1, -2, and -3 Multi-Channel Communication Controls, Order Number 160; also the Honeywell Series 200 Programmers' Reference Manual (Model 120), Order Number 141.

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FOREWORD

The Type 281-2A Communication Control and the Type 285-2A Communication Adapter provide the interconnection of a Series 200 central processor with Honeywell and IBM remote terminals by way of Bell DATA-PHONE Datasets 202C1 on switched voice-grade telephone lines or by way of Bell DATA-PHONE Datasets 202D1 on leased point-to-point voice-grade private line service. The communication control and communication adapter operate with either a two-wire or four-wire system.

The Type 281-2A and Type 285-2A are compatible with all Series 200 central processors; however, their operation in conjunction with the Type 121 requires the presence of a Series 200 control unit adapter (either Feature 1015 or Feature 1016, as described in the Programmers' Reference Manual (Model 120), Order Number 141.

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SECTION I

INTRODUCTION

GENERAL DESCRIPTION

As illustrated in Figure 1-1, the Type 281-2A Communication Control is used to connect one voice-grade telephone line to the Series 200 central processor. The Type 285-2A Communication Adapter is used in conjunction with a Type 286 Multi-Channel Communication Control to connect one voice-grade telephone line when a maximum of 63 communication lines may be connected to a central processor. The Honeywell remote terminal is a Series 200 central processor equipped with a Type 281-2A or a Type 285-2A. The IBM remote terminals utilized with the Types 281-2A and 285-2A are the IBM 7701 Magnetic Tape Terminal, and the IBM 1013 Card Reader/Punch and other compatible IBM synchronous transmitter/receiver units.

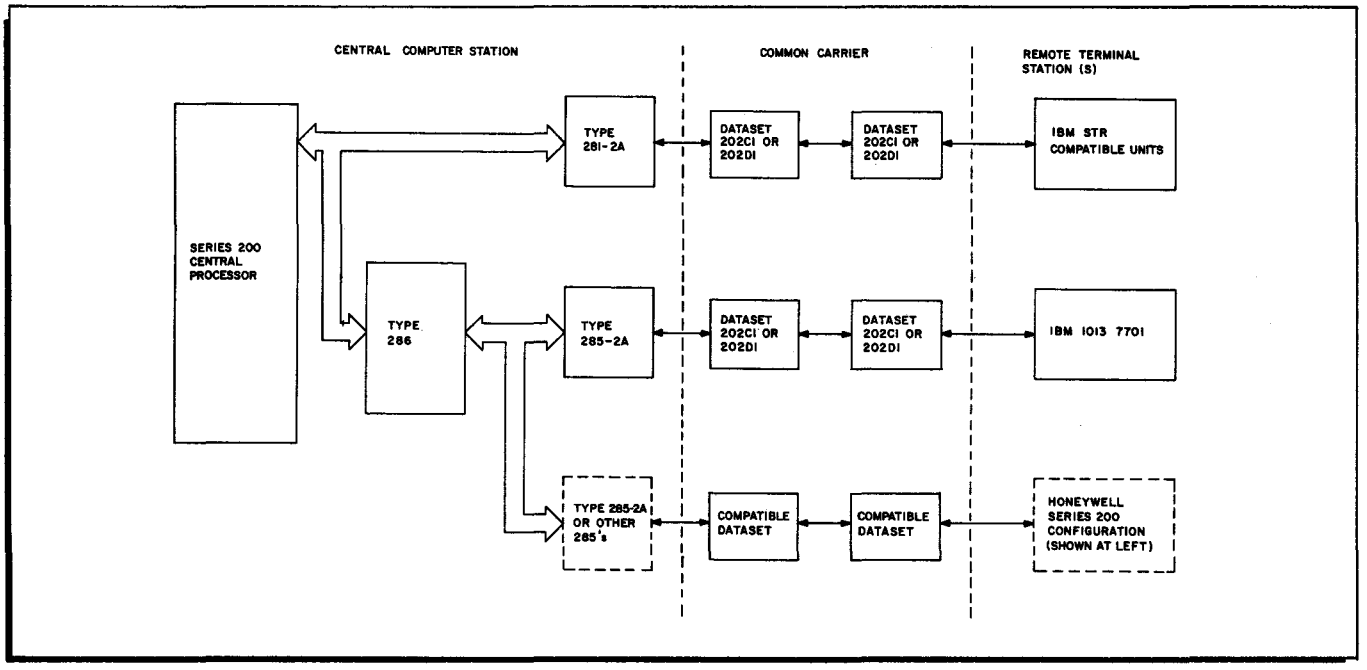


Figure 1-1. Typical Application for Types 281-2A and 285-2A

The communication line is characterized by bit-stream synchronous transmission of IBM four-of-eight code (see Table 2-1) in half-duplex (two-way, non-simultaneous) mode. An initial "hand-shaking" procedure — the exchange of a predetermined configuration of characters — establishes synchronization (see "Line Format and Control," Section III), which is maintained by a clock in the Types 281/285-2A.

The maximum line speed in the switched, voice-grade systems using the Bell DATA-PHONE Datasets 202C is 150 characters, or 1200 bits, per second; in those leased-line private services using the Bell DATA-PHONE Dataset 202D, it is 225 characters, or 1800 bits, per second.

INTERFACE WITH THE SERIES 200 PERIPHERAL BUS AND WITH THE TYPE 286

The standard Series 200 logic drawer contains one Type 281-2A Communication Control or two Type 285-2A Communication Adapters.

Type 281-2A Interface with the Series 200 Central Processor

Standard peripheral interface logic for non-simultaneous input and output connects the communication control to the standard Series 200 peripheral line.

Type 285-2A Interface with the Type 286

Section IV of the Honeywell Hardware Bulletin Type 286-1, -2, and -3 Multi-Channel Communication Controls describes this interface circuit.

INTERFACE WITH DATASET

Common-Carrier Line Termination

The common-carrier line terminates in a Bell DATA-PHONE Dataset 202C or 202D connected to the Type 281-2A. The maximum permissible cable length is 50 feet.

Signals

The signal and control leads on the Bell DATA-PHONE Datasets 202C and 202D meet Electronic Industries Association standards. The datasets convert the voltage-level signals of the communication devices into audio-frequency signals for transmission on the line.

SECTION II

GENERAL PROGRAMMING REFERENCE DATA

DATA HANDLING ABILITY

The Type 281-2A Communication Control transfers single line characters to the central processor and receives line characters from the central processor; the communication control also transfers single data bits to the communication line and receives bits from the line.

The Type 285-2A Communication Adapter transfers single data bits from the communication line to the associated buffer in the Type 286 Multi-Channel Communication Control, or it transfers bits from the Type 286 associated buffer to the line.

CODE

The Types 281-2A and 285-2A are capable of receiving or transmitting any code whose character length is eight bits. Each line character is stored in two consecutive locations in the Series 200 central processor's main memory. In the application discussed here, these communication controls and adapters are implemented to work with the eight-level IBM four-of-eight code shown in Table 2-1.

Table 2-1. Character Codes

SYMBOL	4-of-8 TRANSMISSION CODE			SERIES 200 MEMORY LOCATION	
	1 2 4	8 R O	X N	A	A + 1
SPACE	2 4	8 O		00	56
0	2	8 R	N	02	32
1	1	O	X N	03	41
2	2	O	X N	03	42
3	1 2	R	N	02	23
4	4	O	X N	03	44
5	1 4	R	N	02	25
6	2 4	R	N	02	26
7	1 2 4	R		00	27
8		8 O	X N	03	50
9	1	8 R	N	02	31
A	1	R O	X	01	61
B	2	R O	X	01	62
C	1 2	O	X	01	43

Table 2-1 (cont). Character Codes

SYMBOL	4-of-8 TRANSMISSION CODE								SERIES 200 MEMORY LOCATION	
	1	2	4	8	R	O	X	N	A	A + 1
D			4		R	O	X		01	64
E	1		4			O	X		01	45
F		2	4			O	X		01	46
G	1	2	4					N	02	07
H				8	R	O	X		01	70
I	1			8		O	X		01	51
J	1				R		X	N	03	21
K		2			R		X	N	03	22
L	1	2					X	N	03	03
M			4		R		X	N	03	24
N	1		4				X	N	03	05
O		2	4				X	N	03	06
P	1	2	4				X		01	07
Q				8	R		X	N	03	30
R	1			8			X	N	03	11
S		2			R	O		N	02	62
T	1	2				O		N	02	43
U			4		R	O		N	02	64
V	1		4			O		N	02	45
W		2	4			O		N	02	46
X	1	2	4			O			00	47
Y				8	R	O		N	02	70
Z	1			8		O		N	02	51
/	1				R	O		N	02	61
# =	1	2		8	R				00	33
.	1	2		8				N	02	13
$	1	2		8			X		01	13
,	1	2		8		O			00	53
@ '			4	8	R			N	02	34
⌑)			4	8		O	X		01	54
*			4	8			X	N	03	14
% (			4	8		O		N	02	54
& +		2	4	8				N	02	16
-		2	4	8			X		01	16

Table 2-1 (cont). Character Codes

SYMBOL	4-of-8 TRANSMISSION CODE			SERIES 200 MEMORY LOCATION	
	1 2 4	8 R O	X N	A	A + 1
?	2	8 O	X	01	52
!	2	8	X N	03	12
RM ≠	2	8 O	N	02	52
GM ≢	1 4	8	N	02	15
MC Δ	1 4	8	X	01	15
SM ╫	1 4	8 O		00	55
WS Y (end file)	2	8 R	X	01	32
TM √	1 4	8 R		00	35
>	2 4	8 R		00	36
<	2 4	R O		00	66
;	4	8 R O		00	74
\	2	8 R O		00	72
: (NOTE 2)	1 2 4	8		00	17
[	2 4	R	X	01	26
] (TEL)	4	8 R	X	01	34
BLANK		R O	X N	03	60
IDLE	1	8 R O		00	71
TRANSMIT LEADER	1 4	R O		00	65
CONTROL LEADER	1 4	R	X	01	25
SOR-1/ACK-1	1 2	R	X	00	63
SOR-2/ACK-2	1 2	R O		01	23
ERROR/INQUIRY	1	8 R	X	01	31

NOTE 1

NOTE 1 - These codes are valid only if the IBM terminal is operating in the binary mode.

NOTE 2 - This character (colon) is transmitted as the substitute character.

CHARACTER RECOGNITION

Both the communication control and the adapter are capable of recognizing Idle characters (line bits 18RO), thereby obtaining synchronization. In addition, the Type 281-2A is able to recognize and take action on several control characters.

CONTROL CHARACTERS

The characters used for line control are listed in Table 2-2, and control character functions are described in Table 2-3.

Table 2-2. Control Characters

Name	4-of-8 TRANSMISSION CODE			SERIES 200 MEMORY LOCATION	
	1 2 4	8 R O	X N	A	A + 1
IDLE	1	8 R O		00	71
TRANSMIT LEADER (TL)	1 4	R O		00	65
CONTROL LEADER (CL)	1 4	R	X	01	25
SOR2 - ACK2	1 2	R O		00	63
SOR1 - ACK1	1 2	R	X	01	23
INQUIRY - ERROR	1	8 R	X	01	31
TEL	4	8 R	X	01	34
EOT	2	8 R	X	01	32

Table 2-3. Description of Control Characters

SIGNAL	LEADER FIRST CHARACTER 1 2 4 8 R O X N	TRAILER SECOND CHARACTER 1 2 4 8 R O X N	FUNCTION & REMARKS
IDLE	IDLE 1 8 R O	(Not a two-character sequence)	Generated whenever no other characters are being sent by IBM. Used to establish and maintain synchronization.
*END OF IDLE (EOI) **	CL 1 4 R X	IDLE 1 8 R O	For change of direction of transmission during idle periods.
*TEL **	CL 1 4 R X	TEL 4 8 R X	Indication to other terminal to switch to alternate communications mode.
*EOT **	CL 1 4 R X	EOT 2 8 R X	Indication to other terminal that transmission is completed.
TEST PATTERN	CL 1 4 R X	(Repeated indefinitely)	
Control Signals Transmitted Only by Machine Sending Data			
*INQUIRY (INQ) **	TL 1 4 R O	INQ 1 8 R X	Calls for a reply from the receiving terminal (ACK1, ACK2, ERR).

Table 2-3 (cont). Description of Control Characters

SIGNAL	LEADER FIRST CHARACTER 1 2 4 8 R O X N	TRAILER SECOND CHARACTER 1 2 4 8 R O X N	FUNCTION & REMARKS
Control Signals Transmitted Only by Machine Sending Data			
Start of Record 1	TL 1 4 R O	SOR1 1 2 R X	Conditions both sending and receiving machines for transmission of data SOR1 used for the first and all following odd-numbered transmittal records.
Start of Record 2	TL 1 4 R O	SOR2 1 2 R O	SOR2 used for second and all even-numbered records.
*END OF TRANSMITTAL RECORD (EOTR)	TL 1 4 R O	(Longitudinal-parity-check character)	Ends both transmit and receive data conditions and calls for a reply from the receive machine.
Control Signals Transmitted Only by Machine Receiving Data			
*Acknowledge 1	1 CL 1 4 R X	ACK1 1 2 R X	Acknowledge for the correct reception of a record preceded by SOR1.
*Acknowledge 2	CL 1 4 R X	ACK2 1 2 R O	Acknowledge for the correct reception of a record preceded by SOR2.
*ERROR (ERR)	CL 1 4 R X	ERR 1 8 R X	Calls for a repeat transmission of the last transmitted record.
* Signal causes a change in direction of the transmission. ** Reception in receive data condition is treated as a transmission error.			

MESSAGE FORMAT

The message format required on the communication line is shown in Table 2-4.

Table 2-4. Normal Sequence on Half-Duplex Control Signals

TRANSMITTING STATION	RECEIVING STATION
Send: IDLE (1.3 seconds) CL IDLE } End of IDLE	Send: IDLE (1.3 seconds) CL IDLE } End of IDLE

Table 2-4 (cont). Normal Sequence on Half-Duplex Control Signals

TRANSMITTING STATION	RECEIVING STATION
Transmitter Ready	
Send: IDLE (1.3 seconds) TL, INQ } INQUIRY	
	Send: 4 IDLES CL, ACK-2 } Reply Good
Send: 4 IDLES TL, SOR-1 } Start of Record DATA TL, LRC } End of Record	
	Send: 4 IDLES CL, ACK-1 } Reply Good
Send: 4 IDLES TL, SOR-2 } Start of Record DATA TL, LRC } End of Record	
	Send: 4 IDLES CL, ACK-2 } Reply Good
Send: 4 IDLES TL, SOR-1 } Start of Record DATA TL, LRC } End of Record	
	Send: 4 IDLES CL, ERR } Reply Bad
Send: 4 IDLES TL, SOR-1 } Start of Record DATA TL, LRC } End of Record	
	Send: 4 IDLES CL, ACK-1 } Reply Good
. . .	. . .

Table 2-4 (cont). Normal Sequence on Half-Duplex Control Signals

TRANSMITTING STATION	RECEIVING STATION
Transmitter Ready	
Send: 4 IDLES CL EOT } End of Transmission	
	Send: 4 IDLES CL EOT } End of Transmission
Program alerts operator that transmission is completed.	
NOTE: Except for idle and inquiry messages, the IBM terminal does not necessarily precede its messages with idle characters. Honeywell controls and adapters will, however, send idle characters.	

TURN-AROUND DELAY

The maximum "turn-around" delay for each directional reversal of transmission on a two-wire system is 220 milliseconds.

SECTION III
OPERATIONAL PROCEDURES

LINE FORMAT AND CONTROL

An operator at either installation calls the other, using the dataset handset. The operators agree on procedures, then switch the datasets to DATA; the computer program is notified to begin transmitting Idle messages to obtain synchronization. The Idle message is:

Idle character during 1.3 seconds,
A control leader,
One idle character } End of Idle.

The latter two characters signify end of idle to the other terminal. The computer now "listens" for three seconds; if an idle message is not received from the other terminal, it repeats its idle message.

The transmitting terminal, after it receives and recognizes an end-of-idle signal, sends idle characters for 1.3 seconds, then follows it with the inquiry signal. If the receiving terminal is ready, it responds with an acknowledge signal (ACK-2). The inquiry signal is composed of a transmit leader character followed by an inquiry character. The acknowledge signal is a control leader followed by an ACK-2 character which denotes the receipt of an even number of records (zero, in this case). Having received ACK-2, the transmitting terminal sends a start-of-record signal, composed of a transmit leader and a start-of-record -1 character. The -1 indicates that this is an odd-numbered record — in this case, the first odd-numbered record. The transmitting terminal now accepts the first character of the record (in the four-of-eight code) for transmission on the line.

When the first character is sent, the transmitting terminal accepts the next and continues the same process of sending through the entire record. At the record's end, the transmitter sends the end-of-transmittal-record (EOTR) signal, composed of a transmit leader, then the longitudinal redundancy check (LRC) character. If no errors exist, the receiving terminal returns Acknowledge — a control leader and ACK-1 character. This allows the transmitting terminal to begin sending the next record. Transmission of records continues until all of the records are transmitted or the receiving terminal senses the end of the recording medium.

If a previous record has been in error, the error signal — a control leader and the ERR character — is returned to the transmitter and the previous record is retransmitted. Following IBM procedures, the transmitter must make three attempts to send a single record before

alternate action is taken. When all records are transmitted, an end-of-transmission (EOT) signal, composed of a control leader and the EOT character, is sent. The receiving terminal returns an identical signal, thus alerting both operators. If all records cannot be sent, the operators are alerted to take alternate action.

TELEPHONE REQUEST

This signal, indicating a request to change to the alternate telecommunication mode, may be sent by either terminal. The receiving terminal, to request the alternate mode, responds to the end-of-record signal with an end-of-idle signal. The transmitting terminal sends an inquiry signal and the receiver responds with "TEL." Both operators then depress TALK on their handsets and converse. After conversing, both operators depress the DATA keys on their handsets, notifying the program to continue. The terminals re-establish synchronization. The transmitting terminal sends an inquiry signal and the receiver returns the appropriate acknowledgment for the last message received before the "TEL" request was made.

The computer — acting as transmitter — requests alternate mode, ignores the acknowledgment, and sends a "TEL" signal instead of the next data message. The receiver echoes the request signal and both datasets are switched to TALK, as described above. When the conversation is finished, synchronization is re-established; then the transmitter sends an inquiry signal. Upon sensing this signal, the receiver again sends the acknowledgment which was ignored before the "TEL" request was made.

INTERMEDIATE CHECK CHARACTERS

The IBM transmission terminals (viz., the 7702 and 1013) have two transmission modes, a binary mode recognizing a 64-character set of IBM codes, and a binary-coded-decimal (BCD) mode in which 56 combinations of the 64-character set are legal codes. In the binary-coded-decimal mode, a message from the IBM transmission terminal may contain more than one longitudinal-redundancy-check (LRC) character. Each intermediate longitudinal-redundancy-check character is preceded by a record mark or group mark character, since the longitudinal redundancy check may not be a legal four-of-eight code character. The LRC character is computed only on the preceding block.

SUBSTITUTE CHARACTER

The IBM 7702 terminal — when operating in the binary-coded-decimal mode — can substitute a special character for characters which are in error when read from tape. Substitution is achieved as follows:

1. The IBM unit is reading tape and transmitting the record. When the first erroneous character is detected, the substitute character is sent in its place and the message is then terminated by a control leader and an idle character. The remainder of the message is not sent.

2. The program, interpreting this message as erroneous because of the end-of-idle signal, sends the error signal.

3. The IBM terminal retransmits the identical message two more times, if required, since re-reading of the tape record may be successful.

4. If, after three attempts, the record cannot be read completely, the IBM unit generates and sends a message containing only one data character — the substitute character.

5. After this message has been acknowledged, the IBM unit retransmits the original message in its entirety.

The substitute character is sent to replace all erroneous characters.

SECTION IV
DATA AND FORMAT CHECKS

CHARACTER CHECK

The receiving program should check the legality of each four-of-eight code character. In the Type 281-2A, this check is provided by hardware. Each character — except the LRC character — must contain four 1 bits and four 0 bits.

LONGITUDINAL REDUNDANCY CHECK

The transmitting terminal generates a half-add sum for each of the eight bit positions of the data character. This check character guarantees even parity in each data-character bit position throughout the record or message. When operation is in the binary-coded-decimal mode in conjunction with an IBM 1013 terminal, record and group mark characters are treated as data characters and included in the LRC computation. The receiving terminal generates a check character over the bits of incoming messages in a manner similar to this check over the bits being transmitted.

ODD AND EVEN MESSAGES

Each message transmitted is designated as odd- or even-numbered. The receiver responds with the acknowledge signal ACK-1 for odd-numbered messages and ACK-2 for even-numbered messages. This feature helps prevent loss and duplication of messages if data characters become modified to seem like control characters and vice versa, or if control characters are lost.

LOSS OF SYNCHRONIZATION

Transmission procedure is such that there is always a signal on the communication line within any three-second period. If, for any reason, no activity occurs on the line during a three-second period, the communication controls lose synchronization. When the Type 285-2A Communication Adapter Unit is being used, a "Receive Clear" PDT instruction is executed to enable re-establishment of synchronization at a later time. During initial synchronization, a "Receive Clear" PDT instruction need not be issued to the Type 286 Multi-Channel Communication Control, nor need the Type 285-2A be reset before idle characters are transmitted. When the Type 281-2A Communication Control is being used, a "Sync Stop" PCB instruction is executed to enable re-establishment of synchronization at a later time. This PCB instruction is also used to establish initial synchronization with the Type 281-2A Communication Control.

Loss of synchronization is indicated by the reception of characters which are predominantly illegal — that is, not four-of-eight code characters — over a period of time sufficient to exclude the possibility of a noise burst on the line. Such a time period is in the order of several hundred milliseconds.

In the case of the Type 285-2A, the "Receive Clear" and "Special Strobe" PDT instructions are performed when loss of synchronization is detected. These instructions enable the inception of resynchronization procedures. The end-of-transmittal record is not sensed and no reply is made. The transmitting terminal waits three seconds, then sends an idle message to re-establish synchronization.

In the case of the Type 281-2A operation, the "Sync Stop" PCB instruction is performed when loss of synchronization is detected. This instruction enables the inception of resynchronization procedures. No reply is given once loss of synchronization is detected. The transmitter waits three seconds, then sends an idle message to re-establish synchronization.

If either the Type 281-2A or the Type 285-2A ceases to transmit, the IBM terminal clock is stopped and synchronization is lost. Then the resynchronization procedure occurs. After resynchronization is achieved, the transmitter sends the inquiry signal and the program retransmits its last control signal.

SECTION V
PROGRAMMING FOR THE TYPE 281-2A

VARIABLE-LENGTH BLOCK DATA TRANSFER

The Type 281-2A transfers data in blocks consisting of one or more characters. Computer main memory capacity and available data storage facilities in the terminal equipment determine the maximum number of characters in a block.

SYSTEM REQUIREMENTS

Interrupt Capability

The interrupt capability is standard on all Series 200 central processors except the Model 201; here it is present only with the inclusion of optional Feature 012. The Type 281-2A Communication Control may be used with the Model 201 whether or not this capability is present; however, central processor operations are somewhat restricted if the interrupt capability is not present.

Feature 087 — Longitudinal Redundancy Check (LRC)

The Type 281-2A must include the optional Feature 087 if a hardware check of LRC character computation is required.

Type 213-3 Interval Timer and Type 213-4 Time-of-Day Clock

These product-line peripheral units are used in conjunction with the communication equipment.

TRANSMISSION

Data characters may be transmitted individually or in blocks. All messages sent must conform to the line format and synchronization procedures discussed in Sections III, IV, and V, and illustrated in Table 2-4. All characters sent — except the LRC character — must be in IBM four-of-eight code.

Procedures for terminating transmission begin when the communication control senses a record mark in memory. The record mark is established by program. A "Transmit" PDT instruction is not issued until the "Output Request" PCB instruction is satisfied. When the "Transmit" PDT instruction is issued, the communication control becomes "busy," and the "Output Request" PCB instruction is no longer recognized.

NOTE: The "Output Request" PCB instruction is not satisfied for two character-times after termination of reception. The PDT instruction causes six-bit frames to be transferred from memory to the communication control. Two six-bit frames are used by the communication control to form one eight-bit line character. The leftmost four bits of each frame-pair sent from the central processor are discarded by the communication control.

When single characters are being transmitted (see Note below), a PDT instruction is issued for each character. Each PDT instruction except the first is used in response to an interrupt and an "Output Request" PCB instruction. The interrupt occurs and the "Output Request" PCB instruction is satisfied each time a character with a record mark in the next higher memory location is transferred to the communication control. A PDT instruction is issued for the next character to be sent; it holds the read/write channel active for approximately one character-time before the actual transfer occurs. After the transfer is made, the interrupt function is again set and the "Output Request" PCB instruction is again satified. Transfer of successive characters continues under program control until the complete block has been sent.

NOTE: The first PDT instruction in such a transfer series addresses a field of at least two line characters.

If data is to be transmitted in blocks, one PDT instruction suffices for an entire block. The PDT instruction terminates when a record mark is sensed in memory.

NOTE: If synchronization is lost during transfer, the "Sync Stop" PCB instruction is issued before resynchronization procedures are begun. This instruction is also issued prior to the establishment of initial synchronization. This is true whether the terminal is receiving or is transmitting.

RECEPTION

Either a transmit leader or a control leader is the first character of every two-character control signal. The communication control recognizes these leaders on reception. Upon recognition, these actions are initiated:

1. The Interrupt condition is set in the communication control;
2. The "Input Request" PCB instruction is satisfied; and
3. The leader character is transfered to the central processor, the read/write channel is released and termination procedures are initiated if a "Receive" PDT instruction is active at the time of leader recognition.

In addition to leaders, the communication control also recognizes idle, group mark, and record mark characters. The communication control uses idle characters to establish synchronization, but does not transfer them to the central processor unless they form part of an end-of-idle signal. Transmission of idle characters does not cause an interrupt. Group mark and

record mark characters are recognized only during binary-coded-decimal mode operation; in this mode the communication control acts on group mark and record mark characters as if it had received a leader character.

Reception proceeds as follows:

1. When the initial interrupt occurs and the first "Input Request" PCB instruction is satisfied, the central processor recognizes a transmit leader or control leader received from the line.
2. In response to these indications, a "Receive" PDT instruction is issued within one character-time, addressing a four-character central processor field.
3. Upon issuing the PDT instruction, the communication control becomes busy and the "Input Request" PCB instruction is no longer satisfied.

After the PDT instruction is issued, characters are transferred to the central processor. For every eight-bit line character received by the communication control, two six-bit frames are sent to the central processor, one six-bit frame at a time. The leftmost four bits of the frame-pair are sent to the central processor as zeros.

Because the first "Receive" PDT instruction addressed a four-character central processor field, two line characters are received and transferred to the central processor before a record mark is sensed in memory. When the record mark is sensed, the read/write channel is released, the interrupt condition is set in the communication control, the communication control is no longer busy, and the "Input Request" PCB instruction is again satisfied. The two characters now received form a control signal. Responding, the program examines the received signal, determines its location in the message sequence, and initiates the appropriate action. Some of the program-initiated actions are as follows:

1. If the terminal — as a receiver — recognizes a start-of-record control signal, the central processor issues a "Receive" PDT instruction within one character time to accept the subsequent data characters.
2. If the terminal — as a transmitter — recognizes the correct acknowledgment signal, the program transmits the next data block.
3. If the terminal — as a receiver — recognizes an inquiry control signal indicating that initial synchronization has been achieved, the program replies with an ACK-2 signal.

   NOTE: When the central processor is the receiving terminal during synchronization or resynchronization procedures, the "Clock Correct" PCB instruction is issued upon reception of the first idle message.

Data reception begins in the receiving terminal after a start-of-record signal is recognized. As stated in 1., above, a "Receive" PDT instruction is issued within one character-time after

this signal's reception. The "Receive" PDT instruction may accept one or more line characters. Characters are transferred to the central processor until a record mark is sensed in memory or a transmit or control leader is received from the line.

If data characters are received one at a time, an interrupt occurs and the "Input Request" PCB instruction is satisfied after each line character is transferred from the communication control to the central processor. The interrupt and subsequent PDT instruction are caused by the presence of a record mark in memory. Now, unless the end of the block is reached, a "Receive" PDT instruction is issued for the next character. This PDT instruction holds the read/write channel active while the character is being received from the communication line and assembled in the communication control. After such assembly, the character is transferred to the central processor. A record mark is again sensed in memory, causing the read/write channel to be released and termination procedures to follow. A new PDT instruction may then be issued for the next character.

NOTE: The first PDT instruction for the control signal must address a two-line-character field.

If data is received in blocks, data transfer terminates when a record mark is sensed in memory or when a transmit or control leader is received. After the leader character is transferred to the central processor, the read/write channel is released and termination procedures follow. If termination is caused be reception of a transmit leader, another "Receive" PDT instruction is needed for reception of the subsequent LRC or idle character.

TERMINATION PROCEDURES

A record mark is sensed in memory when a character is transferred to the central processor or from it. The following termination procedures are used during transmission and reception.

Transmission

When a record mark is sensed in memory during character transmission, the read/write channel is released, the Interrupt condition is set, the "Output Request" PCB instruction is satisfied, and the communication control is no longer busy. The communication control completes transmission of the character in its shift register. If a "Transmit" PDT instruction is issued and the read/write channel is regained in one character-time, transmission continues without loss of data. This is the process of "chaining" PDT instructions. During transmission, there is no termination on character recognition.

Reception

If — during reception — a record mark is sensed in memory, the read/write channel is

released, the Interrupt conditon is set, and the "Input Request" PCB instruction is satisfied. The communication control is no longer busy. The same process occurs after a transmit leader, control leader, group mark (in the BCD mode) or record mark (in the BCD mode) character has been received in the communication control and transferred to the central processor. The communication control continues to receive information from the line for two character-times. If a "Receive" PDT instruction is issued and the read/write channel is regained within one character time, reception and transfer to the central processor contine without loss of data; thus, "Receive" PDT instructions are "chained." If no "Receive" PDT instruction is issued, the "Output Request" PCB instruction is not satisfied for two character-times after the record mark is sensed.

Record Mark Position

During reception, the record mark is placed in the rightmost memory position of the last frame-pair to be received. During transmission, the record mark is placed in the next memory position after the last frame transmitted.

BINARY-CODED-DECIMAL MODE OPERATION

The Type 281-2A Communication Control implements a binary-coded-decimal mode of operation which enables it to transfer binary-coded-decimal data from IBM terminal devices. When INITIALIZE is pressed on the central processor control panel, or when synchronization is established, the communication control automatically enters binary mode operation. A "BCD Mode" PCB instruction is available to change the communication control into the binary-coded-decimal mode of operation. This PCB instruction is issued each time synchronization or resynchronization occurs and communication control operation in the binary-coded-decimal mode is desired.

Intermediate LRC Characters

During operation in the binary-coded-decimal mode, longitudinal-redundancy-check characters may occur in the middle of a data message. These characters are immediately preceded by a record mark or group mark character.

During reception in the binary-coded-decimal mode of operation, the communication control recognizes the record mark and group mark characters. The communication control takes the same action as if the second transmit leader of a message (i.e., a part of EOTR) has been received. Another PDT instruction is chained to receive the LRC character and the data following it. Communication control recognition of a record mark or group mark character during transmission does not affect the central processor. Termination of transmission, as in the case of binary mode operation, occurs only when a record mark is sensed in main memory.

Substitute Character

In the binary-coded-decimal mode of operation, illegal characters may be read from the tape, changing the transmission format. Initially, the substitute character is sent instead of the illegal character and the message is terminated with an end-of-idle signal. The operational sequence which follows is described in Section IV.

If a control leader is recognized by the communication control during reception, termination occurs as previously described in this section (see "Termination Procedures"). After interruption of the central processor, another PDT instruction is issued to receive the subsequent idle character. The program — having determined whether a data message has ended with an end-of-transmittal-record (EOTR) character or an idle signal — takes appropriate action.

Error Checking

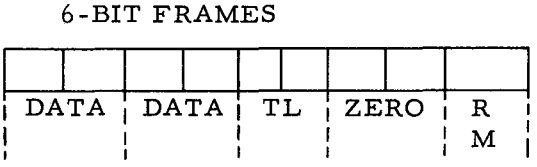
FOUR-OF-EIGHT CODE CHECK

The communication control checks each received character, ensuring that it contains four ones and four zeros. Any illegal character sets an Error condition. This condition is tested and reset by a PCB instruction issued within one character-time of LRC character reception. No four-of-eight code check is performed on LRC characters.

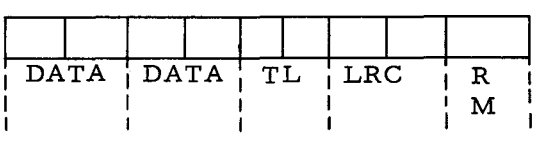
LRC GENERATION/CHECKING

In transmission, if Feature 087 — the hardware LRC option — is present, an all-zero character (two six-bit frames) is transferred to the communication control after the second transmit leader character. The communication control transmits its generated LRC character to the line instead of the central processor's zero character. If the option is not present, a program-developed LRC character is transferred to the communication control after the second transmit leader character. The communication control transmits this LRC character to the line. Memory representation of this character is illustrated below.

Hardware LRC Generation



Software LRC Generation



In reception, a separate PDT instruction is needed for LRC character reception. This "Receive" PDT instruction is issued after the second transmit leader is received and transferred to the central processor. When Feature 087 is present, a test of the LRC/four-of-eight "Error" PCB instruction within one character-time of LRC character reception indicates whether an LRC error has occurred. If LRC error checking is accomplished by software, a program-developed LRC character is compared with the received LRC character for detection of possible error.

Longitudinal-redundancy-check characters occurring in binary-coded-decimal mode operation after record mark or group mark characters are treated in the same manner as the LRC character that is a part of the end-of-transmittal-record signal.

TIMING ERROR

When receiving data, a timing error occurs if a PDT instruction is not issued in sufficient time to take data from the communication control. The error may be tested by a "Device Error" PCB instruction immediately after issuance of a "Receive" PDT instruction, or within two character-times after reception of a block of data.

NON-ACTIVITY ERROR

If a "Receive" PDT instruction is active and no activity occurs on the line within two character-times, the Device Error condition is set and the read/write channel is released. Upon release of the read/write channel, the Interrupt condition is set.

NOTE: The Device Error condition is reset by one of four conditions:

1. The control panel INITIALIZE button is pressed;
2. The "Device Error" PCB instruction is issued;
3. A "Transmit" PDT instruction is issued; or
4. Synchronization is accomplished.

Continuous Character Transmission

The communication control, when so directed by the central processor, is capable of continuously transmitting the same character without further central processor intervention until an end of the transmission is desired. The character transmitted is selected by the central processor under program control. This communication control capability permits it to send idle messages and to establish and maintain synchronization on the line. The following procedures establish continuous character transmission:

1. Issue the "Continuous Transmission" PCB instruction.
2. Transmit a single line character using the "Transmit" PDT instruction.
3. Issue the "Stop Continuous Transmission" PCB instruction, halting transmission of the single character.

If a new "Transmit" PDT instruction is issued within one character-time of the "Stop Continuous Transmission" PCB instruction, the designated new character or characters are sent without interruption of line transmission. A new "Transmit" PDT instruction may also be issued before the "Stop Continuous Transmission" PCB instruction. When this is done, the read/write channel is held until the PCB instruction is issued.

Peripheral Control and Branch (PCB) Instruction

FORMAT

The format for the Type 281-2A Communication Control PCB instruction is shown in Figure 5-1. A description of the informtion contained in each control character is listed below the figure. The PCB instruction initiates control and testing of the Type 281-2A.

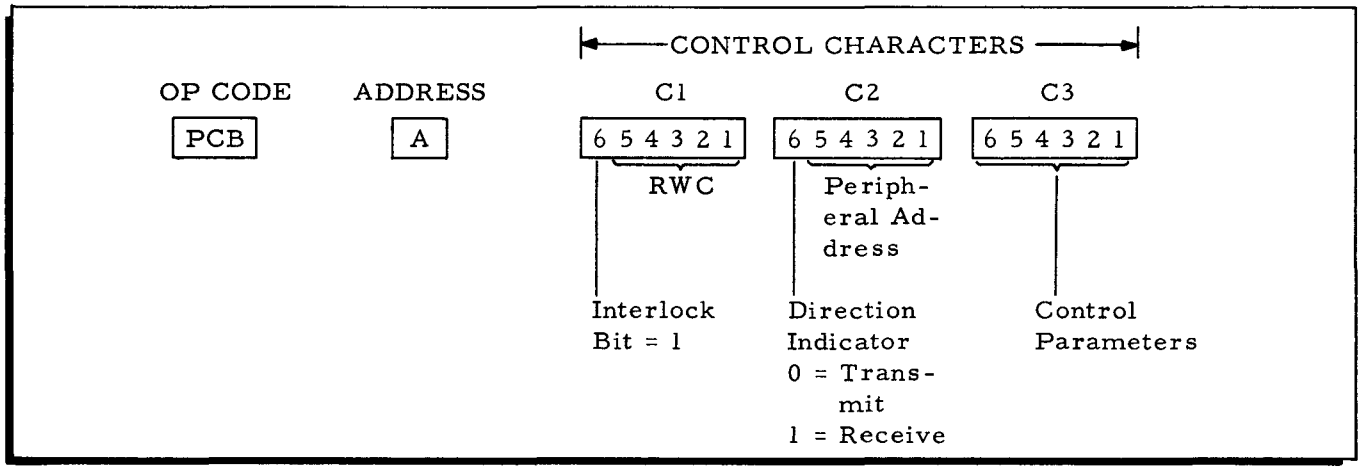


Figure 5-1. Type 281-2A PCB Instruction Format

A Address — Memory location to which the program branches (in a branching PCB) if the condition tested for by the PCB is true.

Interlock Bit — If the interlock bit is a "1", memory access is not granted to RWC1'.

Read/Write Channel (RWC) — Selects the RWC between main memory and the peripheral device. C1 contains the number of the RWC being tested for availability and must be set to zero if no RWC is to be tested (see the appropriate Programmers' Reference Manual).

Peripheral Address — Logical address of the communication control on the peripheral bus.

Control Parameters (C3) — The C3 character of the PCB specifies questions and control for the Type 281-2A.

CONTROL AND TEST FUNCTIONS

The control and test operations, together with their associated octal codes, are listed in Tables 5-1 and 5-2.

Table 5-1. Branching PCB Instructions

INSTRUCTION	DESCRIPTION	C3 (OCTAL)
1. Unit Busy*	Is the communication control Busy?	10
2. Interrupt	Did the unit on trunk specified in C2 interrupt?	75
3. Input Request	Should a PDT instruction to receive be issued?	61
4. Output Request	Is the unit capable of accepting a PDT instruction to transmit?	60
5. Four-of-eight Code Error LRC Error	Has an illegal character(s) been received?	40
6. Device Error	Is the Device Error condition set?	50

*The control unit indicates "busy" when:

a. A PDT instruction is being implemented.

b. The dataset is not operative —

(1) The dataset is in the TALK mode,

(2) No connection has been made with local telephone exchange.

If the answer to the above question is "yes" the program branches to the A Address.

If the answer to the question is "no" the program continues in sequence.

Table 5-2. Non-Branching PCB Instructions

INSTRUCTION	DESCRIPTION	C3 (OCTAL)
1. Set Allow Condition	Allow condition in communication control unit is set.	71
2. Reset Allow and Reset Interrupt Conditions	Allow condition and Interrupt condition are reset.	70
3. Reset Interrupt* Condition	Interrupt condition in communication control unit is reset.	74
4. BCD Mode	Set communication control unit to operate in BCD mode.	23
5. Sync Stop	Stop clock in communication control unit as a preliminary action to re-establishing synchronization.	25
6. Clock Correct	Set clock correction for a receiver terminal.	27

Table 5-2 (cont). Non-Branching PCB Instructions

INSTRUCTION	DESCRIPTION	C3 (OCTAL)
7. Continuous transmission	Continuously transmit the next character sent by a "Transmit" PDT instruction.	21
8. Stop Continuous Transmission	Halt continuous character transmission.	20

*The interrupt condition in the Type 281-2A is set when:

a. The RWC is released. The RWC is released when:

(1) A record mark is sensed while a "Transmit" PDT instruction is active;

(2) A record mark is sensed while a "Receive" PDT instruction is active;

(3) A transmit leader, control leader, group mark character (BCD mode) or record mark character (BCD mode) is received while a "Receive" PDT instruction is active;

(4) A non-activity error has occurred.

b. A transmit leader, control leader, group mark character (BCD mode) or record mark character (BCD mode) is received from the line.

The interrupt condition in the Type 281-2A can be reset by:

a. Issuing a "Reset Interrupt" PCB instruction (C3 = 74);

b. Issuing a "Reset Interrupt/Allow" PCB instruction (C3 = 70);

c. Issuing a PDT instruction ("Receive" or "Transmit");

d. Pressing the INITIALIZE button on the central processor control panel.

Peripheral Data Transfer (PDT) Instruction

FORMAT

The format for all PDT instructions for the Type 281-2A Communication Control is shown in Figure 5-2. The PDT instructions are addressed to the communication control by the C2 control character.

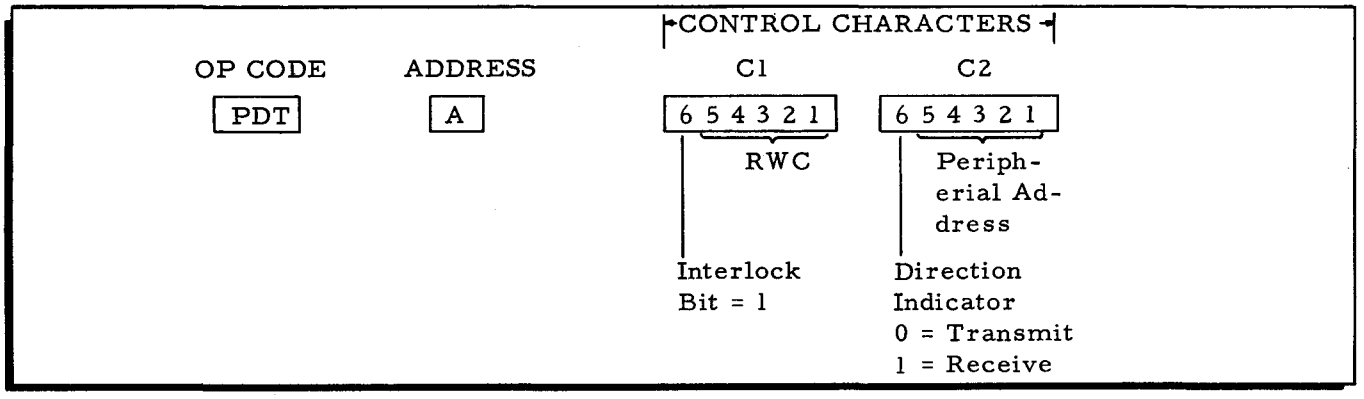


Figure 5-2. PDT Instruction Format

A Address — Contains the address of the main memory location to or from which data is transferred in Type 281 programming. For Types 285/286 programming, see the Honeywell Hardware Bulletin Types 286-1, -2, and -3 Multi-Channel Communication Controls.

Interlock Bit — If the interlock bit is a "1", memory access is not granted to RWC1'.

Read/Write Channel — Selects the RWC between main memory and peripheral devices (see the appropriate Programmers' Reference Manual).

Direction Indicator — Direction of data transfer:

1 = Move data from the Type 281-2A to memory.
0 = Move data from memory to the Type 281-2A.

Peripheral Address — Logical address of control unit on the peripheral bus.

The character or characters referenced by the new "Transmit" PDT instruction are sent without interrupting line transmission.

SECTION VI
PROGRAMMING FOR THE TYPE 286 AND 285-2A

TYPE 286 PROGRAMMING

Programming requirements for the Type 286 are described in the Honeywell Hardware Bulletin entitled Type 286-1, -2, and -3 Multi-Channel Communication Controls.

"SPECIAL STROBE" PDT INSTRUCTION

When executed, this PDT instruction activates a strobe line to the Type 285-2A Communication Adapter Unit by way of the Type 286. The strobe is interpreted according to the state of the Type 285-2A, transmit or receive.

Type 285-2A in the Transmit State

The "Special Strobe" PDT instruction, executed while the Type 285-2A is in the transmit state and after synchronization is achieved, allows any phase correction derived from the receiving terminal clock to be applied to the transmitter's clock when it, in turn, enters the receive mode. Such correction is required only when the Type 285-2A is in the data receiving terminal. The "Special Strobe" PDT instruction can not be executed simultaneously with the "Start of Sending" PDT instruction, although it can be executed simultaneously with the "End of Sending" PDT instruction.

Type 285-2A in the Receive State

Resetting of Type 285-2A synchronization is accomplished by the Type 286 only after a line inactivity period greater than 1.3 seconds. If — because of receiving illegal four-of-eight code characters — the Type 285-2A loses synchronization, the "Special Strobe" PDT instruction may be used to reset the communication adapter unit. The "Special Strobe" PDT instruction is executed in addition to the "Receive Clear" PDT instruction. The latter PDT instruction resets synchronization in the Type 286.

TIMING CONSIDERATION

The program must empty the Type 286 data buffer register within one character-time (6.4 milliseconds) following the interrupt.

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: SERIES 200 TYPE 281-2A COMMUNICATION CONTROL AND TYPE 285-2A COMMUNICATION ADAPTER HARDWARE BULLETIN

DATED: JUNE, 1966

FILE NO: 112.0005.113.0-416

ERRORS NOTED:

Fold

SUGGESTIONS FOR IMPROVEMENT:

Fold

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COMPANY _____

TITLE _____

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