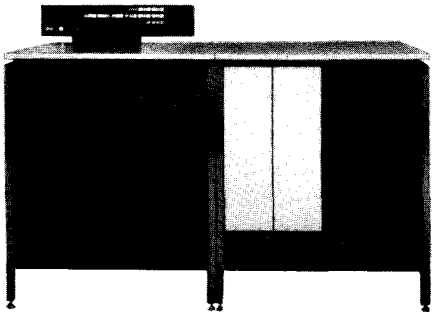
HONEYWELL

HARDWARE BULLETIN

SERIES 200



201 CENTRAL PROCESSOR

In the Honeywell Series 200 Data Processing System, the Type 201 Central Processor is a computing and control center of the Model 200. It is subdivided into five major units: the arithmetic unit, the main memory, the control memory, the control unit, and the input/output traffic control. Under the direction of an internally stored program, the central processor monitors and coordinates the various activities of the entire system.

The arithmetic unit performs such operations as comparisons and binary and decimal addition and subtraction.

The control memory is a magnetic core storage unit consisting of 16 individually addressable control registers. During a program run, the control registers are used to store the main memory addresses that direct the retrieval and execution of all instructions.

Using information stored in control memory, the control unit selects, interprets, and executes the instructions in the internally stored program. Besides the standard instructions, the Type 201 repertoire includes an editing instruction (Feature 013) and a set of advanced programming instructions (Feature 011) — all in variable-length, two-address format (see accompanying table).

The input/output traffic control directs the time sharing of the main memory among the central processor and as many as four simultaneously operating peripheral devices. The traffic control makes it possible, for example, to read cards, punch cards, print, read or write magnetic tape, and compute — all at the same time. Typically, the central processor is free to perform other operations during 80 to 99.9 percent of processing intervals shared with peripheral operations.

The basic 2,048-character, magnetic core main memory may be expanded by adding one memory module of 2,048 characters and one or more modules of 4,096 characters each, up to a total of 32,768 characters. In systems equipped with the advanced programming instructions, the first 24 memory locations are designated as six index registers. There are no reserved input/output areas in main memory; the programmer has complete freedom in specifying both the sizes and the locations of input/output areas.

The program interrupt facility (Feature 012) signals the existence of a particular condition in a peripheral control. A program interrupt may occur whenever a peripheral device has completed an input/output operation — for example, when a tape read or write operation is completed or after the receipt of a character from a remote station by a communication control. Peripheral interrupts can be inhibited or allowed by the program as necessary.

An outstanding design feature of the Series 200 permits execution of stored programs in conjunction with a technique known as "item mark trapping." This facility provides for automatic changes in program sequence without executing programmed instructions to initiate such changes. Sequence changes are initiated by sensing the presence of an item mark in the op code position of the instruction, a method which enhances compatibility between systems having different features installed.

An integral part of the central processor is the operator's control panel. By using various switches, the operator can start and stop the machine and can load and interrogate main and control memory locations. The control panel is equipped with four "sense" switches which can be used in conjunction with programmed instructions to control the path of program execution.

A significant structural feature of the Series 200 is the use of integrated system modules. Each peripheral control and central processor logic unit is housed in a separate drawer which tilts out of the central processor housing for easy access.

(Continued on reverse side)

Specifications remain subject to change in order to allow the introduction of design improvements.

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Honeywell
ELECTRONIC DATA PROCESSING

SPECIFICATIONS

PROCESSING UNIT: Six-bit character.

DATA FORMAT: Variable-length data fields of from one to virtually the maximum number of characters in the main memory.

INSTRUCTION FORMAT: Variable-length, two-address instructions. Typical format consists of op code, two addresses, and a variant character.

MAIN MEMORY SIZE: Basic memory, 2,048 characters. Additional memory available, consisting of one 2,048-character module and up to seven 4,096-character modules.

INTERNAL OPERATIONS: Decimal and binary arithmetic, logic, program control, peripheral control, and editing.

PERIPHERAL ADDRESS ASSIGNMENTS: Sixteen. Peripheral controls which are capable of both reading and writing require two address assignments.

READ/WRITE CHANNELS: Three read/write channels are standard; an auxiliary channel is optional.

MAIN MEMORY CYCLE TIME: 2 microseconds.

CONTROL MEMORY ACCESS TIME: 270 nanoseconds.

CHECKING: Parity bit generated for each character as it is stored in memory. Character parity checked on readout.

ADDRESSING MODES: Two-character address specifies any of 4,096 memory locations; three-character address specifies any of 32,768 memory locations.

TYPICAL OPERATING SPEEDS: See accompanying table.

SPECIAL FEATURES: Silicon semiconductor circuitry, six index registers, up to four simultaneous input/output operations concurrent with computing, program interrupt, indirect addressing.

INSTRUCTION REPERTOIRE TYPE 201

The execution times listed in this table are based on realistic situations involving three-character addressing mode. The data fields referenced by both the A and B addresses are five characters long. Times for **indexed** operations assume that all address fields are indexed. In actual practice, higher speeds will be attained because in many cases abbreviated instruction formats can be used, thus shortening execution times.

NAME OF OPERATION	STANDARD FORMAT	EXECUTION TIME (MICROSECONDS) ADDRESSES NOT INDEXED	ADDRESSES INDEXED
Arithmetic Instructions			
Decimal Add[1]	A/A,B	48.0	60.0
Decimal Subtract[1]	S/A,B	48.0	60.0
Binary Add	BA/A,B	46.0	58.0
Binary Subtract	BS/A,B	46.0	58.0
Zero and Add	ZA/A,B	36.0	48.0
Zero and Subtract	ZS/A,B	36.0	48.0
Logical Instructions			
Half Add	HA/A,B	46.0	58.0
Extract	EXT/A,B	46.0	58.0
Compare	C/A,B	38.0	50.0
Substitute	SST/A,B,V	24.0	36.0
Branch	B/A	12.0	18.0
Branch on Condition Test	BCT/A,V	14.0	20.0
Branch on Character Condition	BCC/A,B,V	24.0	36.0
Branch if Character Equal	BCE/A,B,V	24.0	36.0
General Control Instructions			
Set Word Mark	SW/A,B	20.0	32.0
Set Item Mark	SI/A,B	20.0	32.0
Clear Word Mark	CW/A,B	20.0	32.0
Clear Item Mark	CI/A,B	20.0	32.0
Halt	H/A	12.0	18.0
No Operation	NOP	6.0	—
Store Control Registers	SCR/A,V	20.0	26.0
Load Control Registers	LCR/A,V	20.0	26.0
Change Addressing Mode	CAM/V	8.0	—
Change Sequencing Mode	CSM/A,B,V	22.0	34.0
Interrupt Control Instruction			
Resume Normal Mode	RNM/A,B	20.0	32.0
Data Move Instructions			
Move Characters to Word Mark	MCW/A,B	36.0	48.0
Load Characters to A-Field Word Mark	LCA/A,B	36.0	48.0
Move and Translate	MAT/A,B,V_1,V_2	50.0	62.0
Extended Move	EXM/A,B,V	38.0	50.0
Editing Instruction			
Move Characters and Edit[2]	MCE/A,B	86.0	98.0
Input/Output Instructions			
Peripheral Data Transfer	PDT/A,C_1,C_2	14.0	20.0
Peripheral Control and Branch[3]	PCB/A,C_1,C_2	14.0	20.0

[1]Times indicate no recomplement cycle required; if required add 20 microseconds.

[2]Based on five characters scanned in both second and third passes.

[3]If a branch occurs, add 2 microseconds.