SECTION II

MEMORY SYSTEMS

PREFACE

This section presents the Theory of Operation, Assembly Drawing, Parts list, and Schematic for each of the Hewlett-Packard memory products. The memory products are divided into two types of memory systems: Standard Performance Memory Systems and High Performance Memory Systems. Each of the systems is available either with or without fault control memory controllers. Table 1 and Table 2 list the components associated with each of the memory systems. An Installation and Service Manual for each of the memory systems is available and should be used in conjunction with the material provided in this Engineering and Reference Document. The titles and part numbers of the manuals are:

Standard Performance Memory Systems Installation And Service Manual, part no. 5955-4310.

High Performance Memory Systems Installation And Service Manual, part no. 5955-4311.

Table 1. Standard Performance Memory System Products

PRODUCT NO.	DESCRIPTION	PART NO.
2102B	Standard Performance Memory Controller	02102-60001
2102C	Standard Performance Fault Control Memory Controller	02102-60003
12994A	8K byte (4K word) Memory Module	5060-8369
12998A	16K byte (8K word) Memory Module	5060-8359
13187A	32K byte (16K word) Memory Module	5060-1332
13187B	32K byte (16K word) Memory Module	13187-60001
12746A *	64K byte (32K word) Memory Module	12746-60001
12747A	128K byte (64K word) Memory Module	12747-60001
12779A	256K byte (128K word) Standard Performance Check Bit Array	12779-60001
12780A	512K byte (256K word) Standard Performance Check Bit Array	12780-60001

(HP 1000 M/E/F ERD)

Table 2. High Performance Memory System Products

PRODUCT NO.	DESCRIPTION	PART NO.
2102E	High Performance Memory Controller	02102-60002
2102H	High Performance Fault Control Memory Controller	02102-60004
12741A	32K byte (16K word) High Performance Memory Module	12741-60001
12746H **	64K byte (32K word) High Performance Memory Module	12746-60002
12747H	128K byte (64K word) High Performance Memory Module	12747-60002
12779H	256K byte (128K word) High Performance Check Bit Array	12779-60002
12780H	512K byte (256K word) High Performance Check Bit Array	12780-60002

* The 12746A is a half-loaded (64K byte) 12747A (128K byte) Memory Array Board. These boards are used with the Standard Perfomance 2102B or 2102C Memory Controllers, and are identical in operation.

** The 12746H is a half-loaded (64K byte) 12747H (128K byte) Memory Array Board. These boards are used with the High Performance 2102E or 2102H Memory Controllers, and are identical in operation.

(HP 1000 M/E/F ERD)

MEMORY
CONTROLLERS

HP 2102A
MOS MEMORY SYSTEM

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

CONTENTS

CONTENTS (continued)

TABLES

1. INTRODUCTION

This document provides theory of operation for the 2102A MOS Memory System used in the 21MX Computer Series and is divided into two sections; general theory of operation and detailed theory of operation. The general theory gives an overview of memory system operations. The detailed theory describes significant events occurring during memory system operations and the functional components which produce them.

2. GENERAL THEORY OF OPERATION

The general theory of operation consists of a description of the memory system and a brief description of each of the three memory cycles.

3. Description

The memory system consists physically of one memory controller PCA and one or more memory PCA's. The system functions in three cycles: read, write and refresh. Each type of cycle requires two input/output (I/O) "T" periods (650 nanoseconds).

The read cycle reads out a 16-bit data word from the memory address supplied to it by the CPU and supplies it to the S-bus. The write cycle writes a 16-bit data word into the memory address supplied to it by the CPU. In write mode the controller derives a parity bit from the data word supplied to it and stores the parity bit, with the 16-bit data word, in memory. When the data is retrieved in read mode, the controller again derives the parity of the 16-bit word and checks it against the parity bit supplied from memory. If they disagree, the CPU is notified with an error signal.

The memory is composed of semiconductor integrated circuits (IC's) which require refreshing at least every 2 milliseconds. This is done with a refresh cycle which occurs, automatically, approximately every 32 microseconds. Each refresh cycle refreshes 1/64th of the memory so that the total memory is refreshed, according to requirement, every 2 milliseconds.

The refresh cycle is performed, normally, in I/O "T" periods 2 and 3 but, when it occurs while memory is under DCPC control, it is performed in periods 4 and 5. This leaves periods 2 and 3 for the DCPC read cycle.

The refresh cycle is performed automatically, without external stimulation. When a refresh cycle is started, the CPU is notified so that read and write cycles are inhibited until the refresh cycle is complete.

4. Read Cycle

The read cycle is initiated when the $\overline{\text{Read}}$ signal from the CPU becomes active. The memory address, from the CPU, is supplied to the M-register (on the controller) and memory. It is stored in the M-register to be

continually supplied to memory until the data is read out from the stored memory address. The 16-bit data word is read out from memory and stored in the T-register and the parity bit is supplied to the parity circuits. The parity circuits check parity and, after the result of the check is ready, the S-bus gates are opened to enable passage of the memory data word to the S-bus. Also the parity error status is generated to the CPU. Then the controller and memory circuits are restored to the ready-for-new-cycle state.

5. Write Cycle

A write cycle begins with data supplied to memory and to the T-register and parity circuits on the memory controller. The T-register stores the data and a parity bit is derived from it by the parity circuits. The address into which the data is to be written is supplied to memory and the M-register and the $\overline{\text{Write}}$ signal to the memory controller is activated by the CPU. Then the memory controller enables writing into memory and the M-register stores the address and becomes the address source for memory. The controller opens the memory gates to pass the data from the T-register to memory and the data is written into the selected address of memory.

6. Refresh Cycle

A refresh cycle is initiated automatically by an oscillator on the controller PCA. When a refresh cycle starts, reading or writing is disabled by the controller and the CPU is notified that a refresh cycle is in process. A 0-to-63 counter on the controller PCA selects a different row of memory elements to be refreshed by each refresh cycle. Essentially, in a refresh cycle, the controller only indicates the row of memory elements to be refreshed. Refreshing of the memory elements is performed within the memory IC.

7. DETAILED THEORY OF OPERATION

The detailed theory of operation consists of a description of how a word of memory is addressed, a description of memory signals, identification of the functional units on the memory controller and memory PCA's, a description of the initial conditions before a read or write cycle starts, and a detailed description of a read cycle, a write cycle, and a refresh cycle.

8. Memory Addressing

Memory for a 21MX computer is contained on one or more PCA's. Each PCA contains either one or two rows of memory IC's. There are 17 IC's in a row, one IC for each bit of the 17-bit memory word. A one-row PCA is referred to as a 4K PCA. The two-row PCA is referred to as an 8K PCA. The 4K and 8K descriptions refer to the approximate number of 17-bit memory words the PCA is capable of storing.

> *Note: The word "row" is used, in this discussion, to refer to two different items:*
>
> > *a. A group of 17 memory IC's arranged in a row on a PCA.*
> >
> > *b. A row of 64 memory elements within an IC.*

Each IC contains a 64-row by 64-column matrix of memory elements for a total of 4,096 (approximately 4K) memory elements within each IC. A row of 17 such IC's is capable of storing 4,096 17-bit memory words, with each bit of the memory word stored in a separate IC dedicated to that bit. The bits are stored in identical elements in the IC's; that is, the same column and row are addressed on each IC to form the 17-bit word.

A 20-bit address word is used to select a 17-bit word stored in memory. To select a memory word, four items must be identified; the PCA, the row of IC's on the PCA (row 1 or 2), the row of elements within each IC, and the column of elements within each IC. These items and the bits of the memory address used to identify them are listed below.

MEMORY ADDRESS BITS	ITEM IDENTIFIED
13 through 19	PCA
12	Row (1 or 2) of IC's on the PCA
6 through 11	Column of elements within each IC
0 through 5	Row of elements within each IC

Bits 6 through 11, which identify the column of memory elements, form a 6-bit binary word. The same is true of bits 0 throgh 5 which identify the row of memory elements. The column and row words are supplied to each IC and are decoded within each IC to select the single designated memory element.

For purposes of refreshing memory, only the 64 rows on each IC are addressed; (it isn't necessary to address each individual memory element for refreshing).

9.   Signal Description

Table 1 lists all control and status signals used in the memory and provides a brief description of their function.

Table 1. Memory System Signals

SIGNAL	FUNCTION
$\overline{\text{Read}}$	Initiates a memory read cycle.
$\overline{\text{Write}}$	Initiates a memory write cycle.
$\overline{\text{MPV}}$	Indicates a memory protect violation to the controller. In a DCPC operation, it has no effect. In a normal read operation, an all "1"s word is supplied to the S-bus. In a normal write mode, no write cycle occurs.
$\overline{\text{DMAEN}}$	Indicates that a DCPC read or write cycle is going to occur. The DCPC is free to read and write in the protected area of memory.

Table 1. Memory System Signals (continued)

SIGNAL	FUNCTION
$\overline{\text{DMAREAD}}$	Delays a refresh cycle which might be ready to begin until time periods T4 and T5. (The refresh cycle normally occurs during T2 and T3.) This leaves T2 and T3 for the DCPC read cycle.
$\overline{\text{P4NF}}$ and $\overline{\text{P5NF}}$	The last two of six time periods occurring in a T period. $\overline{\text{P4NF}}$, together with $\overline{\text{TST}}$, enables read in of data into the T-register in a write cycle. The $\overline{\text{P5NF}}$ which occurs in time period T6 (or T3, if a DCPC read cycle is beginning), enables the refresh cycle to begin, if one is due.
TA, TB, and TC	These signals are a binary word which, when decoded, indicate the current T period.
PON	Indicates that the power supply is receiving ac line power and is operating properly. When PON becomes inactive, reading and writing is inhibited and refresh cycles occur every 32 micro-seconds, independent of conditions external to the memory system.
$\overline{\text{TEN}}$	Opens the S-bus gates to pass data from the T-register to the S-bus after the $\overline{\text{Read}}$ signal has become inactive in a read cycle.
$\overline{\text{TST}}$	Together with the $\overline{\text{P4NF}}$ signal, enables the T-register to store the data from the S-bus in a write operation.
R/W RR	Either this signal or R/W WR is jumpered, on the memory PCAs, to select read mode or write mode for the memory IC's. The IC, when enabled by active $\overline{\text{CLK}}$ and $\overline{\text{CS}}$ signals, will read when the jumpered signal is high and write when it is low.
R/W WR	Either this signal or R/W RR is jumpered, on the memory PCA, to select read mode or write mode for the memory IC's. The IC, when enabled by active $\overline{\text{CLK}}$ and $\overline{\text{CS}}$ signals, will read when the jumpered signal is high and write when it is low.
$\overline{\text{CS}}$ and $\overline{\text{CLK}}$	Both signals are required to enable the memory IC's to read or write. Reading or writing is selected by the R/W RR or R/W RW signal.
$\overline{\text{MREF}}$	Informs memory that a refresh cycle is in progress. Used, on the memory PCA, together with the $\overline{\text{CLK}}$ signal, to activate the CLOCK input to the memory IC's during a refresh cycle.
A0 thru A5	These six bits of the memory address word are used, by the refresh circuits, to select the row of memory elements to be refreshed. The bits are in the form of a binary code which is decoded, in the IC, to identify the row of memory elements.
MSRDY	Indicates, to the CPU, that the memory system is available for another memory cycle.
$\overline{\text{REFRESH}}$	Indicates, to the CPU, that a refresh cycle is about to begin. Read and write cycles are inhibited during a refresh cycle.
$\overline{\text{PE}}$	Indicates, to the CPU, that the data word read from memory, during the current cycle, contains a parity error.
$\overline{\text{METDIS}}$	Signal generated by DMS for read protection.

10. Functional Unit Identification

In the following discussion, it is necessary to refer to the functional units of the memory system, such as flip-flops, multiplexers, and registers by name. Since the functional units aren't identified by name on the logic diagrams, they are listed in tables 2 and 3, along with their reference designations, to enable use of the logic diagrams in following the discussion.

Table 2. Identification of Memory Controller Functional Units

NAME	REFERENCE DESIGNATION
Read flip-flop (FF)	U92B
Write FF	U92A
R/W Delay FF	U83A
MSRDY FF	U74B and U76B
Clock FF	U74A and U84C
Delay Line	U95
M-register Control FF	U51A and U51B
M-register input gates	U11, U12, U13, and U24
M-register	U21, U22, and U23
T-register Control FF	U65B
T-register	U32, U35, U41, and U45
S-bus gates	U33, U36, U43, and U46
Memory gates	U31 and U34
Parity circuits	U42 and U45
T-register multiplexer	U54
Refresh oscillator	U91A and U91B
Strobe A FF	U87C and U87D
Strobe B FF	U87A and U87B
Refresh decoder	U77
Refresh FF	U83B
Refresh Delay FF	U84A and U84B
Refresh Transmit FF	U74C and U76C
Row select counter	U81A, U81B, and U71
Refresh drivers	U61
Power Sense FF	U65A

Table 3. Identification of Memory PCA Functional Units

NAME	REFERENCE DESIGNATION
PCA select circuits	XW1, U61A thru U61D, and U81A thru U81D
Control circuits	U121, U171B, U171C, U131A, and U131B
Bus drivers/receivers	U12, U62, U82, U122, and U152

11. Pre-Cycle Conditions

When no cycle is in progress, the following conditions exist in the memory system:

a. The M-register input gates are open so that any memory address supplied by the CPU passes through the gates to the M-register and to memory.

b. The M-register is ready to accept any address supplied but will not store it until early in a read or write cycle.

c. The memory IC's are disabled for both reading and writing.

d. The memory address, for a read or write cycle is supplied to the M-register and memory either before or approximately at the time the $\overline{\text{Read}}$ or $\overline{\text{Write}}$ signal from the CPU becomes active.

e. The T-register is not receptive to data from either memory or the S-bus.

f. The S-bus gates are disabled for passage of data from the T-register, or memory, to the S-bus and for passage of data from the S-bus to the T-register and memory.

g. The memory gates are disabled for passage of data from the T-register to memory.

h. The MSRDY signal to the CPU is active (high) indicating the memory system is ready for a cycle.

12. Read Cycle

Information concerning events occurring in a read cycle are presented briefly, in table form, in table 4 and in narrative form in the paragraphs following the table.

Table 4. Read Cycle Events

CAUSE	EVENT
$\overline{\text{Read}}$ signal, from CPU, active (low).	The Read FF (U92B) is set.
Read FF set.	The R/W Delay FF (U83A) is set, the MSRDY FF is reset, and the MSRDY signal, which has been active, becomes inactive.
Read FF set and no refresh cycle.	The CS signal to memory IC's becomes active (low).
R/W Delay FF set and PON signal from power supply active (high) .	1. The delay line (U95) is pulsed and begins, generating pulses at fixed delay intervals. 2. The Clock FF (U74A and U84C) is set (pin U74-12 high).
Clock FF set.	1. The $\overline{\text{CLK}}$ signal to memory is active (low). 2. The $\overline{\text{ICLK}}$ signal is active (low). 3. The ICLK signal is active (high).
Memory address available to memory PCA's, $\overline{\text{CS}}$ and $\overline{\text{CLK}}$ signals active, R/W WR signal high, and the signal jumpered on the memory PCA's to select read or write mode (either the R/W WR or R/W RR signal) high.	The memory supplies the data from the selected address to the T-register and the S-bus gates. However, the S-bus gates are not yet enabled to pass data to the S-bus.
$\overline{25}$ pulse from delay line (pin U85-1)	The M-register stores the address present at its input and applies it steadily to memory.
$\overline{75}$ pulse from delay line (pin U85-2).	The R/W Delay FF is reset ending the input pulse to the delay line.
$\overline{75}$ pulse from delay line (pin U85-3)	The M-register control FF (U51A and U51B) is reset. This closes the M-register input gates, isolating the M-register and memory from the address supplied by the CPU. However, the address is stored in the M-register, which supplies it to memory.
$\overline{275}$ pulse from delay line (pin U85-7).	The MSRDY FF is set and the MSRDY signal to the CPU becomes active (high). It remains high until the next cycle.
Read FF set, Clock FF set (ICLK signal active), and end of next P5 CPU time period occurs.	The T-Register Control FF (U65B) is set. (This FF is active in the reset condition.)
T-Register Control FF reset (active).	1. The B inputs are selected on the T-register and the T-register multiplexer (U54). 2. The T-register, with its B inputs selected, accepts the 16-bit memory data word from memory. 3. The T-register multiplexer supplies the parity bit (bit 16) from memory to the parity circuits through Nand gate U55A. 4. Starting at this time, the parity circuits compare the parity which they derive from the data in the T-register with the parity bit supplied by memory and prepare an indication (the $\overline{\text{PE}}$ signal) of agreement or error. (The $\overline{\text{PE}}$ signal is supplied to the CPU later in the cycle.)

Table 4. Read Cycle Events (continued)

CAUSE	EVENT
$\overline{350}$ pulse from delay line (pin U85-6)	1. The T-Register Control FF is set (made inactive). This selects the A inputs on the T-register and T-register multiplexer and causes the T-register to store the 16-bit data word from memory and supply it steadily to the parity circuits and S-bus gates.
	2. With its A inputs selected, the T-register multiplexer stores the parity bit (bit 16) from memory and supplies it steadily to the parity circuits.
	3. The Clock FF is reset. This deactivates the $\overline{ICLK}$ and ICLK signals and the $\overline{CLK}$ signal to memory. With the $\overline{CLK}$ signal inactive, the memory IC's stop supplying data to the T-register and S-bus gates. However, the data is now stored in the T-register.
	4. The M-register Control FF is set. This stops the M-register from supplying the address stored in it to memory and opens it to accept any new address supplied from the M-register input gates. (These events result from a low output from gate U52B.) However, the M-register input gates won't open to pass new address information to the M-register until the $\overline{350}$ pulse becomes inactive (approximately 125 nanoseconds after it begins).
$\overline{400}$ pulse from delay line (pin U85-8).	The Read FF is reset. This enables the S-bus gates ($\overline{ENWDATA}$ signal through T-register multiplexer) to pass new data from the S-bus to the T-register and memory (but neither are in a condition to receive data).
$\overline{TEN}$ signal from CPU becomes active (low) and $\overline{Read}$ signal from CPU is inactive (high).	The S-bus gates are enabled for transmission of data from the T-register to the CPU by gate U56B.
$\overline{450}$ pulse from delay line (pin U85-4), $\overline{TEN}$ signal from CPU active, and $\overline{Read}$ signal inactive.	The $\overline{PE}$ signal is enabled by the Parity Strobe signal, at gate U52A, to indicate to the CPU whether or not a parity error exists in the data being transmitted to the CPU.
$\overline{TEN}$ signal becomes inactive.	The S-bus gates are disabled for transmitting data from the T-register to the S-bus.
$\overline{350}$ pulse becomes inactive (high).	The M-register input gates are opened to pass any address supplied by the CPU to memory and the M-register.

A read cycle is initiated when the $\overline{Read}$ signal from the CPU becomes active (low), setting the Read FF. This closes the S-bus gates to isolate memory and the T-register from any signals on the S-bus. The transition of the Read FF output, from reset to set, activates (low level) the $\overline{CS}$ signal to memory and sets the R/W Delay FF. This resets the MSRDY FF, deactivating (low) the MSRDY signal to the CPU to inform it that a memory cycle is in process. Also, the delay line is pulsed to start its sequence of delayed output signals.

The Clock FF is set, by the set condition of the R/W Delay FF, to activate the $\overline{CLK}$ signal to the memory IC's. The reset condition of the Write FF makes the R/W WR signal to the memory PCA's high. This and

the active $\overline{\text{CLK}}$ signal enable the bus driver/receivers, on the memory PCA selected by the memory address to pass data from the memory IC's on the selected PCA to the B inputs of the T-register and the S-bus gates. (By this time, the memory address is supplied to memory and the M-register, from the CPU through the open M-register input gates.) The active $\overline{\text{CLK}}$ and $\overline{\text{CS}}$ signals from the controller enable the memory IC's on the selected PCA to read or write. Reading, rather than writing, is selected by the high condition of either the R/W WR or R/W RR signal from the controller. (One of these signals is jumpered on the memory PCA's to select read or write for the memory IC's. Both signals are high at this time.) With all three read conditions met, the data is read out of the IC's at the selected memory address and supplied to the S-bus gates and the B inputs of the T-register. However, the S-bus gates are not yet enabled to pass the data word to the S-bus.

The delay line, which was pulsed when the R/W Delay FF was set, activates the $\overline{25}$ pulse 25 nanoseconds after being pulsed. This causes the M-register to store the address supplied to it, through the M-register input gates, from the CPU. With the address stored, it supplies it steadily to all memory PCA's.

When the $\overline{75}$ delay line signal (pin U85-2) becomes active, 75 nanoseconds after the delay line is pulsed, the R/W Delay FF is reset, ending the input pulse to the delay line. This pulse continues passing through the delay line, activating the delay line signals with its leading edge and deactivating them with its trailing edge.

When the $\overline{75}$ signal from the delay line becomes active (low), the M-register control FF is reset, closing the M-register input gates. From this point on, the memory is no longer dependent on the CPU M-register.

The $\overline{275}$ delay line signal (pin U85-7) sets the MSRDY FF to activate the MSRDY signal to the CPU. This notifies the CPU that the memory system is ready for a new memory cycle.

The end of the first P5 time period occurring after the Clock FF is set resets the T-register control FF. (The T-register control FF is active when reset.) This selects the B inputs to the T-register and T-register multiplexer. With its B inputs selected, the T-register passes the data from memory to the S-bus gates and the parity circuits. The parity circuits derive the parity of the 16-bit data word and compare it to the parity bit supplied to them from memory through the T-register multiplexer. The result of this comparison is supplied to the CPU, as the $\overline{\text{PE}}$ signal, later in the cycle.

When the $\overline{350}$ delay line signal becomes active (low), the T-Register Control FF is set (made inactive), selecting the A inputs to the T-register and T-register multiplexer. With its A inputs selected, the T-register stores the 16-bit data word and applies it steadily to the S-bus gates and the parity circuits (the memory gates are closed, isolating memory from the contents of the T-register). The T-register multiplexer stores the parity bit supplied it from memory and applies it steadily to the parity circuits through gate U55A.

Activation of the $\overline{350}$ signal also resets the clock FF. This deactivates the CLK signal to the memory IC's ending readout. However, the data word is now stored in the T-register.

The M-Register Control FF is set again by the active 350 signal but the M-register input gates remain closed until the $\overline{350}$ signal becomes inactive, later in the cycle.

The Read FF is reset when the $\overline{400}$ delay line signal (pin U85-8) becomes active. This activates the $\overline{\text{ENWDATA}}$ signal which passes through the T-register multiplexer to enable passage of data through the S-bus gates to memory and the T-register. However, the T-register is disabled from receiving data and although data can be supplied direct to the memory IC's, it cannot be read into them.

When the $\overline{\text{TEN}}$ signal from the CPU becomes active (low), providing the Read FF is reset, transmission of the data word from the T-register, through the S-bus gates, to the S-bus is enabled. From this time until the $\overline{\text{TEN}}$ signal is deactivated the data is transmitted to the CPU.

When the $\overline{450}$ delay line signal becomes active, the $\overline{\text{Parity Error}}$ ($\overline{\text{PE}}$) signal is enabled to communicate to the CPU whether or not a parity error was found in the data word being supplied to the CPU.

The M-register input gates are opened when the $\overline{350}$ delay line signal becomes inactive (high). Then any address supplied to the controller passes through to memory and the M-register. This completes the cycle and leaves the memory system ready for the next cycle.

13.   Write Cycle

A synopsis of write cycle events is supplied in table 5. The paragraphs following the table supply a more complete description of events in narrative form.

Table 5. Write Cycle Events

CAUSE	EVENT
READ and WRITE FF's both clear.	$\overline{\text{ENWDATA}}$ will be active (low) enabling S-bus data into the B inputs of the T-register multiplexer and to the memory.
$\overline{\text{TST}}$ and $\overline{\text{P4NF}}$ signals from CPU both active (low)	Selects the B input of the T-register multiplexer, sending the S-bus data to the parity generators and the A inputs of the T-register multiplexer.
$\overline{\text{TST}}$ active (low) and $\overline{\text{P4NF}}$ inactive (high)	Selects the A inputs of the T-register, latching the S-bus date. This stores the S-bus data in the T-register.
$\overline{\text{Write}}$ signal from CPU active (low) and the address supplied to memory is not located in a protected area of memory or, if it is, this cycle is under the control of the dual-channel port controller.	The Write FF is set.
Write FF set.	1. Transmission of data from the S-bus to the T-register and memory is inhibited ($\overline{\text{ENWDATA}}$ goes high) (gate U62C). 2. The memory gates are opened to enable passage of data from the T-register to memory. 3. Transmission of the parity bit to memory is enabled (gate U53A). 4. The R/W Delay FF is set, resetting the MSRDY FF. This de-activates the MSRDY signal to the CPU. 5. The $\overline{\text{CS}}$ signal to the memory IC's is activated (gate U73A). 6. The R/W RR and R/W signals to memory became low (gates U72A and B). 7. The low condition of the R/W RR signal disables the bus drivers on the memory PCA, inhibiting transmission of data from memory to the T-register, parity circuits, and S-bus gates (gate U171C on memory PCA). Also, writing into the memory IC's is selected and reading out of them is disabled.

Table 5. Write Cycle Events (continued)

CAUSE	EVENT
R/W Delay FF set and PON signal from power supply is active (high)	1. The Clock FF is set (U83A and U84D). 2. The delay line is pulsed, initiating its sequence of pulses delayed by fixed time intervals (gate U94A).
Clock FF set.	1. The $\overline{CLK}$ signal to all memory PCA's becomes active (low). 2. The PCA and row decoding logic enables the CLK signal (high) to only the selected row of memory IC's. 3. With the $\overline{CS}$ and CLK signals active, the selected memory ICs are enabled for reading or writing. Writing is selected by the low condition of the R/W RR or R/W WR signal (whichever is jumpered on the memory PCA, to pin 12 of the memory ICs). The address is already supplied to the memory PCA's through the M-register input gates on the controller PCA. Whatever is in the T-register will be written into memory.
$\overline{25}$ pulse, from delay line, active (low) (pin U85-1)	The M-register stores the address supplied to it through the M-register input gates and supplies it steadily to the memory.
$\overline{75}$ pulse, from delay line, active (low) (pin U85-2)	1. The R/W Delay FF is reset ending the input pulse to the delay line. 2. The MSRDY FF is enabled for reset by the next $\overline{275}$ pulse from the delay line.
$\overline{75}$ pulse, from delay line, active (low) (pin U85-3)	1. The M-Register Control FF is reset. This closes the M-register input gates so that the address is no longer supplied from the CPU to the M-register (gate U62B). However, the address is already stored in the M-register.
$\overline{275}$ pulse, from delay line, active (low) (pin U85-7).	The MSRDY FF is set, activating the MSRDY signal to the CPU. This indicates to the CPU the memory is ready for another cycle.
$\overline{350}$ pulse, from delay line, active (low) (pin U85-6)	1. The M-Register Control FF is set. 2. The M-register stops supplying the address to memory and becomes receptive to any new address supplied to it through the M-register input gates. However, the M-register input gates aren't open yet and won't be until all the memory and controller circuits are returned to the idle state (when the $\overline{350}$ pulse ends) (gate U62B). 3. The Clock FF is reset. This stops the memory from writing.
$\overline{400}$ pulse, from delay line, becomes active (low) (pin U85-8)	1. The Write FF is reset. 2. The S-bus gates open for passage of data from the S-bus to the memory and the T-register ($\overline{ENWDATA}$ signal low at pin U54-12). 3. The memory gates close, inhibiting passage of data from the T-register to memory (gate U62C). Also, the parity bit is blocked from passing to the memory at gate U53A.

Table 5. Write Cycle Events (continued)

CAUSE	EVENT
(cont) $\overline{400}$ pulse	4. The R/W WR signal to the memory PCA's becomes high. Also, the R/W RR signal becomes high provided no refresh cycle is starting.
$\overline{350}$ pulse becomes inactive.	The M-register input gates open to pass any new address to memory and the M-register. This completes the write cycle.

The write cycle begins when the CPU activates $\overline{TST}$. At CPU time period P4, the S-bus data is allowed to pass through the T-register multiplexer to the A inputs of the T-register multiplexer and to the parity circuits. At the end of P4, the T-register stores the S-bus data.

The address into which data is to be written, is present at the memory IC's as soon as the CPU supplies it to the M-register input gates. These gates are always open (except during refresh cycles) to enable address information to be supplied to memory and the M-register between cycles.

The $\overline{Write}$ signal from the CPU sets the Write FF if the address is not in the protected area of memory (MPV not active (high)) or if this write cycle is requested by the dual-channel port controller (DCPC can access any address in memory). If the address is in the protected area of memory and this is not a DCPC write cycle, the Write FF will not be set (gate U66B) and no memory cycle will occur.

Shortly after the Write FF is set, the MSRDY signal to the CPU is deactivated and writing into memory is enabled by signals from the controller (R/W and $\overline{CS}$).

The M-register then stores the address supplied to it through the M-register input gates and applies the address steadily to the memory.

The S-bus gates close and the memory gates open to supply the contents of the T-register and the parity bit to the memory through the bus driver/receivers on the memory PCA's. (These bus driver/receivers are always enabled to receive data).

The clock FF is set, activating the $\overline{CLK}$ signal to the memory PCA's. The module and row decoding on the memory PCA's will enable the CLK signal to only one row of memory IC's. Writing begins as soon as the CLK signal reaches the memory ICs. These conditions remain stable for enough time to ensure reliable writing of the data and parity bit into the proper address in memory.

After enough time has elapsed for read-in of the data into memory, the MSRDY signal to the CPU becomes active to notify the CPU that the memory system is ready for another cycle. This signal then remains active until shortly after the next cycle is started. After another time period, the M-register stops supplying the address to memory and becomes receptive to a new address. However, the M-register input gates don't open to allow passage of a new address from the CPU to the memory and M-register until after the controller and memory circuits are recovered from the present cycle.

At approximately the time the M-register stops supplying the address to the memory, writing into memory is inhibited by deactivation of several required signals from the controller. Then the Write FF is reset and the S-bus gates are enabled to pass data from the S-bus to the memory and T-register again. They remain

in this condition until the next cycle. The M-register input gates are opened later to enable any address supplied by the CPU, for the next cycle, to be applied to memory and the M-register. This completes the write cycle.

14. Refresh Cycle

Events occurring during a refresh cycle are described briefly in table 6.

Table 6. Refresh Cycle Events

CAUSE	EVENT
PON active (high) and Pulse (negative) output from refresh oscillator (gate U91-pin 7) and Strobe A FF reset (gate U87-pin 8 high).	Strobe B FF is set (gate U87-pin 3 low), activating the strobe B input to the refresh decoder to enable its Q_B output (pin 9).
Occurrence of CPU time period P5 of the next T4 time period following enabling of refresh decoder Q_B output (gate U77-pin 9).	1. Strobe A FF set (gate U87-pin 11 high). 2. Refresh FF released from clamped reset condition. 3. $\overline{REFRESH}$ signal to CPU becomes active (low). 4. Strobe A input to the refresh decoder becomes low, enabling the Q_A (pin 7) output of the refresh decoder. 5. Strobe B FF is reset (gate U87-pin 8 low) making the Strobe B input to the refresh decoder high and disabling the Q_B output (pin 9) of the refresh decoder. (The Strobe B FF remains reset until the next refresh cycle — approximately 32 microseconds later).
$\overline{DMAREAD}$ signal not active and occurrence of next T6 time period.	Refresh decoder Q_A output (gate U77-pin 7) becomes high.
$\overline{DMAREAD}$ signal not active, occurrence of time period P5 of T6 and refresh decoder Q_A output high. (When the $\overline{DMAREAD}$ signal is inactive, the refresh cycle is performed during time period T2 and T3).	1. MSRDY FF set, deactivating the MSRDY signal to the CPU. 2. Refresh Transmit FF set, activating (low) the $\overline{MREF}$ signal to the memory, disabling the M-register input gates, disabling M-register IC U21, resetting (outputs low) M-register IC's U22 and U23, activating the R/W RR signal to memory, disabling the $\overline{CS}$ signal to memory and enabling the refresh address driver.
$\overline{DMAREAD}$ signal active, and occurrence of next time period T3.	Refresh decoder Q_A output (gate U77-pin 7) becomes high.
$\overline{DMAREAD}$ signal active, and occurrence of P5 of T3 and refresh decoder Q_A output high. (When the $\overline{DMAREAD}$ signal is active, the refresh cycle is performed during time period T4 and T5.)	1. MSRDY FF set, deactivating the MSRDY signal to the CPU. 2. Refresh Transmit FF set, activating (low) the MREF signal to the memory, disabling the M-register input gates, disabling M-register IC U21, resetting (outputs low) M-register IC's U22 and U23, activating the R/W RR signal to memory, disabling the $\overline{CS}$ signal to memory and enabling the refresh address driver.

Table 6. Refresh Cycle Events (continued)

CAUSE	EVENT
Refresh decoder Q_A output high (DMAREAD active and T3 or $\overline{DMAREAD}$ not active and T6) and occurrence of the end of time period P5.	Refresh FF is set, resetting the Strobe A FF (gate U87-pin 8 high), disabling the Q_A output of the refresh decoder, and deactivating the $\overline{REFRESH}$ signal to the CPU.
Strobe A FF is reset.	Refresh FF is reset and clamped reset. (The Strobe A FF is not set again until the next refresh cycle — approximately 32 microseconds later).
PON signal from power supply is active (high) and refresh FF set.	Refresh Delay FF set (gate U84-pin 3 high)
PON signal from power supply inactive (low and occurrence of a pulse (positive) from the refresh oscillator (gate U91-pin 6).	Refresh Delay FF set (gate U84-pin 3 high).
Refresh Delay FF set.	1. Delay line pulsed, initiating its sequence of output signals at fixed time intervals from the time it was pulsed. 2. Clock FF set, activating (low) the $\overline{CLK}$ signal to memory. The selected row of memory addresses are refreshed from this time until the Clock FF is reset later in the cycle.
Clock FF set.	The PON signal, from the power supply, is disabled from affecting operation of the memory controller until the memory IC's are disabled by deactivation of the $\overline{CLK}$ signal (when the Clock FF is reset).
$\overline{25}$ signal from delay line	(The effect of the $\overline{25}$ signal on the M-register has already been performed by the active $\overline{IREF}$ signal which became active when the Refresh Transmit FF was set.)
$\overline{75}$ signal from delay line (pin U85-2)	1. Refresh Delay FF reset, ending the input pulse to the delay line. 2. M-register Control FF, which was set by the $\overline{350}$ signal in the last cycle, is reset.
$\overline{275}$ signal from delay line (pin U85-7)	MSRDY FF is reset, activating the MSRDY signal to the CPU. This informs the CPU the memory system is ready to receive an instruction for another cycle.
$\overline{350}$ signal from delay line	1. Clock FF is reset, deactivating the $\overline{CLK}$ signal to memory. This ends refreshing of the selected row of memory addresses by disabling the memory IC's. 2. The row select counter is stepped one increment to select the next sequential row of memory addresses to be refreshed during the next refresh cycle. 3. M-Register Control FF is set. However, the M-register remains disabled until the $\overline{IREF}$ signal becomes inactive (when the $\overline{450}$ signal occurs). Also, the M-register input gates are not enabled until the $\overline{350}$ signal becomes inactive (when the cycle ends).

Table 6. Refresh Cycle Events (continued)

CAUSE	EVENT
$\overline{400}$ signal from delay line (pin U85-8).	(No effect on the refresh cycle.)
$\overline{450}$ signal from delay line (pin U85-4)	Refresh Transmit FF reset with the following effects:
	a. $\overline{MREF}$ signal to memory deactivated.
	b. Refresh drivers disabled.
	c. M-register enabled to receive an address. (However the M-register input gates are not yet enabled to supply one. They won't be enabled until the 350 pulse becomes inactive.
	d. R/W RR signal to memory deactivated and $\overline{CS}$ signal released from the inhibited condition (but not activated).
Deactivation of the $\overline{350}$ delay line signal.	M-register input gates are enabled. This allows an address from the CPU to be supplied to the M-register which is now enabled to receive one. This ends the refresh cycle.

15.   Functional Component Description

The following paragraphs describe the function of each functional unit on the memory controller PCA and a memory PCA. Refer to tables 2 and 3 for a cross-reference between the reference designations used to identify these functional units on the logic diagram and the names with which they are identified in this discussion. Refer to logic diagram 5060-8360 for logic details of the memory controller and to diagrams 5060-8369 (4K memory) and 5060-8359 (8K memory) for logic details of the memory PCA's.

16.   Memory Controller PCA Functional Components

The following paragraphs describe the function of the functional units on the memory controller PCA.

17.   READ FLIP-FLOP. The Read FF stores the occurrence of an active $\overline{Read}$ signal, from the CPU, to initiate a read cycle. The output of the Read FF, as it is set, sets the R/W Delay FF which pulses the delay line. It is also supplied to the T-Register Control FF (U65B), the T-register multiplexer (U54), and the memory gates (U31 and U34). At the memory gates, it closes the gates to inhibit data from being supplied from the T-register to memory. It also results in activating (reseting) the T-Register Control FF (U65B) at the end of the next P5 period. With the T-Register Control FF output active (low) the B inputs to the T-register and the T-register multiplexer are selected. As a result, the T-register accepts data from memory, enabling Nand gate U55 to pass the parity bit from memory to the parity circuits for checking, and inhibiting the S-bus from passing data from the T-register to the S-bus. (Transmission of data from the T-register to the S-bus occurs later in the read cycle.)

The Read FF is reset approximately 400 nanoseconds after the delay line is pulsed. The reset condition of the flip-flop, along with an active $\overline{TEN}$ signal from the CPU, enables passage of read data from the T-register, through the S-bus gates, to the S-bus to complete a read cycle. Also, along with the active $\overline{TST}$ signal from the CPU, during a write cycle, the reset condition of the Read FF enables the S-bus gates to

pass data from the S-bus to the memory and the R-register. Later in a write cycle, the reset condition of the Read FF is required to enable passage of data from the T-register, through the memory gates, to the memory.

18.   WRITE FLIP-FLOP. The Write FF stores the occurrence of an active Write signal to initiate a write cycle. When the flip-flop is set by the Write signal, the R/W Delay FF is set, pulsing the delay line. This produces the sequence of events listed in the delay line discussion. When set, the Write FF, along with the off state of the Read FF, enables passage of data from the T-register to memory in write mode. The set condition of the flip-flop also enables passage of the parity bit from the parity circuits to the memory IC's.

The Write FF is reset approximately 400 nanoseconds after the delay line is pulsed. When not in write mode, the reset condition of the Write FF, along with a no-refresh cycle condition sets the R/W RR and R/W WR signals to the memory PCA's in the high condition to enable reading data from the memory IC's. Also, the reset state of the Write FF, along with the reset state of the Read FF, enables the S-bus gates to pass data from the S-bus to the T-register. (When the $\overline{TST}$ signal from the CPU becomes active, the T-register stores this data for transmission to the memory.)

19.   R/W DELAY FLIP-FLOP. The R/W Delay FF (U83A) pulses the delay line when set by the set condition of either the Read FF or Write FF. It is reset approximately 75 nanoseconds after the delay line is pulsed. The set condition of the R/W Delay FF sets the MSRDY FF to deactivate the MSRDY signal to the CPU. This informs the CPU that the memory system is not available for a memory cycle.

20.   MSRDY FF. The MSRDY FF (U74B and U76B), when set, deactivates the MSRDY signal to the CPU to indicate the memory system is unprepared to accept a request for a read or write operation. It is set at the beginning of a refresh, read, or write cycle. It is reset by the $\overline{275}$ pulse from the delay line (pin U85-7) which occurs 275 nanoseconds after a read, write, or refresh cycle begins. Thus, the MSRDY signal to the CPU is inactive (low) for approximately 275 nanoseconds beginning when a read, write, or refresh cycle begins.

21.   CLOCK FLIP-FLOP. The Clock FF (74A and U84C), when set by the Ref Delay FF at the beginning of a refresh cycle, activates the ICLK signal to the T-Register Control FF and the CLK signal to all memory IC's. The CLK signal must be active (high) for each memory IC to enable it to be read out of, written into, or refreshed. It also activates the $\overline{ICLK}$ signal to the Power Sense FF (U65A) and to the Row Select Counter (U81A, U81B, and U71).

The Clock FF is reset by the $\overline{350}$ pulse from the delay line 350 nanoseconds after the start of the current cycle (whether it is a read, write, or refresh cycle). This deactivates the $\overline{CLK}$, ICLK, and $\overline{ICLK}$ signals. If the cycle is a refresh cycle, the rising (trailing) edge of the $\overline{ICLK}$ signal steps the Row Select Counter to the next sequential row of memory bits on each memory IC in preparation for the next refresh cycle. This signal is gated through the Refresh Drivers (U61), which are enabled only during a refresh cycle to ensure that the counter is not stepped by read or write cycles.

22.   DELAY LINE. The delay line (U95) is used in read, write, and refresh cycles to generate seven signals, at fixed time intervals, starting from the time it receives an input signal. In all three types of cycles, it receives its input signal at the start of the cycle. The seven output signals perform the same functions in each cycle. Thus, once pulsed, the delay line programs a fixed sequence of events. The pulse which passes through the delay line is approximately 90 nanoseconds long. Each output pulse is also approximately 90 nanoseconds long and is active in the high state. The delay line buffer, U85, inverts the delay line signals so that, as output from U85, the signals are active in the low state.

The events resulting from each of the output pulses are as follows:

OUTPUT PULSE	U85 PIN NO.	EFFECT
$\overline{25}$	1	When active (low) locks the M-register (U21, U22, and U23) so no information can be written into it and makes the stored contents available as output (readout) to the memory.
$\overline{75}$	2	Resets the Ref Delay FF and R/W Delay FF. Since these are the flip-flops which supply the activating pulses to the delay line, the input pulse ends when they are reset approximately 90 nanoseconds after it was begun (the pulse length is increased by delays other than the one produced by the delay line).
$\overline{75}$	3	When active, resets the M-Register Control FF (U51A and U51B). This disables the M-Register Input Gates (U11, U12, U13, and U24) so that the M-Register is isolated from the external input source. Also, with the M-Register Control FF reset, the M-Register is locked to input although it remains enabled for reading. The M- Register Control FF remains set until the 350 pulse becomes active.
$\overline{275}$	7	When activated, resets the MSRDY FF, activating the MSRDY signal to the CPU.
$\overline{350}$	6	Resets the Clock FF, deactivating the ICLK and $\overline{\text{ICLK}}$ signals and the CLK signal to the memory IC's. This ends the period of memory IC read, write, or refresh activity.

The rising edge of the $\overline{\text{ICLK}}$ signal steps the Row Select Counter to select the next row of memory bits to be refreshed by the next refresh cycle. (This occurs only if the present cycle is a refresh cycle.)

The $\overline{350}$ pulse also sets the M-Register Control FF to unlock the M-Register to prepare it to accept a new address. (However, a new address must pass through the M-register Input Gates which are not enabled until the $\overline{350}$ pulse becomes inactive approximately 90 to 100 nanoseconds after it becomes active. Therefore, writing into the M-register is not enabled until approximately 425 nanoseconds after the start of a cycle.)

The T-Register Control FF is set by the active $\overline{350}$ pulse. It is held locked in the set condition as long as the $\overline{350}$ pulse remains active (approximately 90 to 100 nanoseconds).

When the $\overline{\text{ICLK}}$ signal becomes inactive, the next P5NF signal from the CPU clocks the Power Sense FF. If line power is not present when the P5NF signal becomes active, the Power Sense FF is reset, all reading and writing is inhibited,

OUTPUT PULSE	U85 PIN NO.	EFFECT
$\overline{350}$ (cont)		and refresh cycles are initiated directly by the refresh oscillator, independent of CPU timing and signals.
$\overline{400}$	5	Resets the Read FF and Write FF and locks both in the reset condition, inhibiting starting of any read or write operation, while it is active. Therefore, no read or write cycle can be initiated until approximately 525 nanoseconds after the start of the last cycle (whether read, write or refresh).
$\overline{450}$	4	Resets the Refresh Transmit FF to cut off the refresh signal to the memory IC's.
		Enables the $\overline{PE}$ signal output to the S-bus. However, this signal is only transmitted when the $\overline{TEN}$ signal from the CPU is active (low).

23.　**M-REGISTER CONTROL FLIP-FLOP.** The M-Register Control FF exerts an inhibiting control over the M-register input gates and determines whether the M-register is in a condition to store an address or read out a stored address. The M-register input gates are enabled to pass a signal from the CPU to the M-register by the set condition of the M-Register Control FF, provided a no-refresh cycle condition exists and the $\overline{350}$ delay line signal is not active. The M-register is enabled to store an address by the set condition of the $\overline{25}$ delay line signal, and a no-refresh cycle condition. When the M-Register Control FF is reset or the $\overline{25}$ delay line signal is active (low), provided a refresh cycle is not in progress, the M-register is enabled to supply the address stored in it to memory.

24.　**M-REGISTER INPUT GATES.** M-register input gates U11, U12, U13, and U24, when enabled by the M-register control circuits, open to pass the address on the S-bus to the M-register. The gates are enabled by the high level of the output from U62B-6 which occurs near the end of a read, write, or refresh cycle approximately 500 nanoseconds after the delay line is pulsed. They remain enabled until the beginning of a refresh cycle ($\overline{IREF}$ signal active) or until the $\overline{75}$ delay line signal becomes active approximately 100 nanoseconds after the $\overline{READ}$ or $\overline{WRITE}$ signal becomes active.

The M-register input gates pass two different sets of memory address bits, depending on whether or not the Memory Expansion Module (MEM) is installed. If only basic memory is used, the $\overline{\text{Memory Expansion Bus Enable}}$ ($\overline{MEBEN}$) signal is held inactive (high) and memory bits 0 through 14 (MB 0 through MB 14) are passed to the M-register with memory extend bits 10 through 19 (MEB 10 through MEB 19) disabled. (Memory bit MB 15 is not used and is clamped in the low condition, as supplied to the memory PCA's.) If the MEM is installed, gate IC U12 is disabled, cutting off memory bits MB 10 through MB 14 from the M-register and memory PCA's, and enabling memory extend bits MEB 10 through MEB 19.

25.　**M-REGISTER.** The M-register (U21, U22, and U23) stores the memory address to be acted upon in read or write mode. The address is received from the S-bus and is supplied to the memory PCA's in both read and write mode. The address is supplied to the M-register when the M-register input gates (U11, U12, U13, and U24), which isolate the register from the S-bus, are open. These gates are open during the time between the end of the $\overline{350}$ delay line pulse from the last cycle (approximately 500 nanoseconds after the delay line was pulsed in the last cycle) and the time the $\overline{75}$ pulse becomes active when the next cycle is initiated.

The M-register is receptive to the address supplied to it, in both read and write cycles, in the time between the end of the last cycle (approximately 500 nanoseconds after the delay line was pulsed) and the time the $\overline{25}$ delay line signal occurs in the present read or write cycle. The address present at the M-register input when the $\overline{25}$ pulse becomes active (low) is the one which will be stored in the register.

The contents of the M-register are supplied to the bus linking the M-register, the M-register input gates, and the memory PCA's at all times except when the M-register is accepting input and during a refresh cycle.

M-register IC U21, stores the refresh memory bits, 0 through 5 and is never cleared. IC's U22 and U23, which handle memory bits 6 through 19 are cleared (all outputs low) by a refresh cycle and remain cleared throughout the cycle.

26. **T-REGISTER CONTROL FLIP-FLOP.** The T-Register Control FF (U65B), when active (in the reset condition, with its output (low), causes the T-register to accept new data from the memory PCA's. This data is supplied to the S-bus during a read cycle after the Read signal from the CPU becomes inactive (high) and the $\overline{\text{Transmit Enable}}$ ($\overline{\text{TEN}}$) signal from the CPU is active (low). It also causes the T-register multiplexer to select its B inputs. (The $\overline{\text{TST}}$ signal, from the CPU, performs, in a write cycle, a function exactly equivalent to the T-Register Control FF function; that is, it causes the T-register and the T-register multiplexer to select their B inputs.)

The T-Register Control FF is active (reset) only during read mode. It is active for about 75 nanoseconds, from the occurrence trailing (rising) edge of the P5 signal (while the Clock FF is set) until the 350 pulse from the delay line becomes active.

27. **T-REGISTER.** The T-register stores data in process of transfer between memory and the S-bus (in read mode) or between the S-bus and memory (in write mode). It is controlled by the T-Register Control FF in read mode and by the $\overline{\text{TST}}$ signal, from the CPU, in write mode. (The DCPC is allowed to read from, and write into, the protected zone of memory, through action of gates U66B and U66D.)

The T-register accepts data in a write cycle during time period P4 while the $\overline{\text{TST}}$ signal from the CPU is active (low). (The data comes from the S-bus.) It accepts data during a read cycle during a time period starting with the trailing (rising) edge of P5 while the Clock FF is set (ICLK signal becomes active) and ending approximately 75 nanoseconds later (the $\overline{350}$ delay line output becomes active). (The data comes from memory.)

When the Select A/B signal is high, the T-register accepts the inputs from either the S-bus gates (U33, U36, U43, and U46) or memory which are applied to its B inputs. It applies them as outputs to the parity circuits, memory gates (U31 and U34), and the S-bus gates. When the Select A/B signal is high, the T-register can be considered to be in the accept input mode.

The low condition of the Select A/B signal puts the T-register in the store mode (with its A inputs selected). In the store mode, the inputs which were applied to the B inputs when the Select A/B signal was high are stored in the register and applied to the parity circuits, memory gates, and S-bus gates.

Although the T-register is made up of IC's designed to be multiplexers, the latching effect normally associated with flip-flops is achieved by connecting the T-register outputs back to its A inputs. This latching effect

results from the fact that, due to the construction of the internal circuits of the IC, the A inputs are selected and supplied as outputs before the B inputs are unselected. After the short overlap period in which both the A and B inputs are selected, the B inputs are unselected but, because of the overlap period, they are already locked into the A input-register output loop. With the B inputs stored in the loop, they remain there until the B inputs are again selected; then the stored data is replaced with new data.

28.   S-BUS GATES. The S-bus gates (U33, U36, U43, and U46) isolate the T-register from the S-bus. These gates are bidirectional; when enabled for receiving by the T-register multiplexer (pin U54-12 low), they open to pass the contents of the S-bus to the T-register. The gates enable receiving and the T-register stores the data from the S-bus during a write cycle at the occurrence of the first P4 period while the $\overline{\text{TST}}$ signal from the CPU is active (low).

When enabled for transmitting by low $\overline{\text{TEN}}$ and high $\overline{\text{READ}}$ signals from the CPU, they pass the T-register contents to the S-bus. This condition occurs during a read cycle.

29.   MEMORY GATES. The memory gates isolate memory from the T-register. (The T-register is isolated from memory by gates on the memory PCA's.) They are unidirectional gates which, when enabled by the T-register multiplexer (pin U54-12) and the $\overline{\text{RFF}}$ signal, pass the data stored in the T-register to the memory PCA's. Both enabling signals must be simultaneously high. This condition occurs in write mode after the Write FF is set.

30.   T-REGISTER MULTIPLEXER. The T-register multiplexer enables and disables reception of input data from the S-bus, supplies the parity bit from memory to the parity circuits for parity checking during a read cycle and stores the parity bit for continued application to the parity circuits during a read cycle after its outputs are disconnected from its B inputs by deactivation of the T-Register Control FF.

Like the T-register, the A or B inputs of the T-register multiplexer are selected to be output by the Select A/B signal which is derived from the $\overline{\text{Temporary Store}}$ ($\overline{\text{TST}}$) and $\overline{\text{P4NF}}$ signals in write mode and from the T-Register Control FF in read mode. When the A/B signal is high, the B inputs are supplied as outputs; when it is low, the A inputs are supplied as outputs.

In write mode the B inputs are selected during P4 time when the $\overline{\text{TST}}$ signal is active (low). At this time, the low condition of the Read FF signal on pin 13 is supplied to the S-bus gates to enable reception, by the T-register, of input data from the S-bus. The parity bit, which is generated by the parity circuits from the data in the T-register, is supplied to N and gate U55A but, since the Read FF signal on pin 3 is low, U55A blocks transmission of the parity bit back to the parity circuits (this circuit is for use in read mode and is, therefore, disabled in write mode).

In read mode, the Read FF signal at gate U54-pin 13 is supplied to the S-bus gates to isolate the T-register from S-bus inputs during the read operation. Also, the Read FF signal at gate U54-pin 3 and the parity bit from memory are supplied to Nand gate U55A. The active Read FF signal enables the gate to supply the

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parity bit to the parity circuits for parity checking. After the Select A/B signal becomes inactive (when the T-Register Control FF is set when the 350 delay line pulse occurs) the Read FF signal and parity bit are stored in the multiplexer until the Select A/B signal again becomes active. This is necessary to meet parity circuit requirements.

31.   PARITY CIRCUITS. The parity circuits (U42, U45, and U52A) generate a parity bit (bit 16), in write mode, and supply it to memory along with the 16 data bits. In read mode, they check the parity bit and generate a $\overline{\text{Parity Error}}$ ($\overline{\text{PE}}$) signal to the CPU if the parity they read from the 16 data bits does not agree with the parity bit (bit 16) supplied from memory.

In a read cycle, the parity bit (MDS16) is supplied from memory, through the T-register multiplexer B inputs and Nand gate U55A, to the parity circuits. If a disagreement exists between the parity bit and the parity of bits 0 through 15 stored in the T-register, the $\overline{\text{PE}}$ signal becomes active near the end of the cycle when the Parity Strobe ($\overline{450}$ pulse) from the delay line becomes active.

The T-register multiplexer outputs are disconnected from the B inputs at approximately the time the delay line 350 pulse occurs (the T-Register Control FF is deactivated). This disconnects Nand gate U55A from the Read FF signal and parity bit before the parity status has been communicated to the CPU through the $\overline{\text{PE}}$ signal. To continue supplying the parity bit to the parity circuits until the $\overline{450}$ pulse occurs, the Read FF signal and the parity bit are stored in the T-register multiplexer the same way it is done in the T-register, by connecting the appropriate multiplexer outputs (pins 4 and 7) to the A inputs.

Although the parity bit generated by the parity circuits in write mode passes through the T-register multiplexer, it is blocked at Nand gate U55A by the inactive (low) Read FF signal and does not reach the parity circuits.

Even or odd parity is selectable by connecting, or leaving unconnected, the PAR terminals E1 and E2. If the terminals are connected, even parity is selected. To select odd parity, the terminals are left open.

32.   REFRESH OSCILLATOR. The refresh oscillator (U91A and U91B) is a free-running oscillator which generates a negative pulse (from pin U91-7) and a positive pulse from pin U91-6 to initiate a refresh cycle approximately once every 32 microseconds. This is approximately one refresh cycle for every 20 I/O cycles (an I/O cycle is composed of time periods T2 through T6).

33.   STROBE B FLIP-FLOP. The strobe B flip-flop (U87A and U87B), when set by a pulse from the refresh oscillator, enables the Q_B output of multiplexer U77. This allows the strobe A flip-flop (U87C and U87D) to be set during the next T4 time period. The strobe B flip-flop remains set only until the strobe A flip-flop is set. Setting the strobe A flip-flop produces a negative signal from pin U87-8 which resets the strobe B flip-flop and disables the Q_B output of the multiplexer.

Once reset, the strobe B flip-flop remains so (Q_B output of the multiplexer disabled) until the next refresh oscillator pulse initiates a new refresh cycle.

34. STROBE A FLIP-FLOP. The Strobe A FF (U87C and U87D) is set (pin U87-11 high) when the signal $\overline{P5NF}$ becomes active (low) in the first T4 period following a refresh oscillator pulse. When set, it enables the Q_A output of the Refresh Multiplexer and releases Refresh FF U83 from its fixed reset condition. Also, it resets the Strobe B FF, disabling the Q_B output of the Refresh multiplexer and activates the $\overline{REFRESH}$ signal to the CPU to inform it that a refresh cycle is starting. It remains set until the Refresh FF is set. This occurs at the end of the first T6 period following the Refresh oscillator pulse if the dual channel port controller (DCPC) is not active ($\overline{DMA\ READ}$ signal active). If the $\overline{DMA\ READ}$ signal is active, the Refresh FF is set and the Strobe A FF is reset at the end of the first T3 period following the Refresh oscillator pulse to leave the T2 and T3 periods for DMA activity.

Once reset the Strobe A FF remains reset (pin U87-11 low) until the next Refresh oscillator pulse initiates another refresh cycle. The reset condition of the Strobe A FF disables the Q_A output of the Refresh multiplexer, holds the $\overline{REFRESH}$ signal in the inactive condition, and fixes the Refresh FF in the reset condition.

35. REFRESH DECODER. The refresh decoder (U77) synchronizes refresh operations with I/O timing. This is done by using the TA and TB signals (as a binary count of 0 to 4) to select one of the four inputs, in each of the two input sets (set A and set B) to be supplied as output. Only two inputs of the A input set are used and the B input set uses only one input. The unused inputs are disabled.

The Q_B output, when enabled by the Strobe B FF, enables setting of the Strobe A FF. With the Strobe A FF set, the Q_A multiplexer output is enabled. The Q_A output initiates the refresh cycle by setting the Refresh FF and allowing the next P5NF period to set the Refresh Transmit FF and the MSRDY FF.

The B input, $\overline{TC}$, is selected when TA and TB are both active. Thus, the Q_B output becomes active (high), provided it is enabled by the Strobe B FF, during I/O time period T4 ($TA \cdot TB \cdot \overline{TC}$). With the Q_B output high during T4, occurrence of the P5NF signal sets the Strobe A FF to enable setting of the Refresh FF.

The two A inputs are used to select the T period in which a refresh cycle is to be initiated. The normal start time is when the P5NF signal becomes active during period T6. However, if a DMA (DCPC) read operation is in progress, the start time is delayed until the P5NF signal becomes active during T3. This leaves periods T2 and T3 free for the DCPC read operation.

The $\overline{DMA\ READ}$ signal input is selected by the TA and TB select signals during period T6. If it is active (high) and the A output has been enabled by the Strobe A FF, a normal refresh cycle is initiated when the P5NF signal becomes active during T3. If the DMA READ signal at pin U77-4 is active (high), indicating the DCPC is reading out of memory, it is selected during period T3. Then, providing the A output has been enabled by the Strobe A FF, the delayed refresh cycle is started at T3 and P5NF time.

36. REFRESH FLIP-FLOP. When the Refresh FF (U83) is set, while power is available (PON signal active), it resets the Strobe A FF to disable the multiplexer Q_A output and deactivate the $\overline{REFRESH}$ signal to the CPU. It also sets the Ref Delay FF which initiates the sequence of delay line outputs and sets the Clock FF. The Refresh FF is set by the falling edge of the P5NF signal when the multiplexer Q_A output is active. This occurs at the end of the T6 period, for a normal refresh cycle or at the end of the T3 period for a refresh cycle delayed by DCPC read activity.

37.   **REFRESH TRANSMIT FF.** The Refresh Transmit FF (U74C and U76C) is set at the beginning of the P5 period during the T3 period in which the multiplexer Q_A output becomes active (for a normal refresh cycle). For a refresh cycle delayed by a DCPC read operation, it is set when P5NF begins in the T3 period in which the multiplexer Q_A output becomes active.

When set, the Refresh Transmit FF enables transmission of the Refresh Address for the memory row selected for refreshing from the Memory Row Select Counter, thorough the refresh transmit gates (U61) to all memory IC's. It also activates the IREF, $\overline{\text{IREF}}$, and $\overline{\text{MREF}}$ signals. The $\overline{\text{MREF}}$ signal is sent to the memory to indicate a refresh cycle is beginning. The Refresh Transmit FF is reset by a pulse from the delay line 450 nanoseconds after it is set.

38.   **REFRESH DELAY FF.** The Refresh Delay FF (U84A and U84B), when set by the active output of gate U82-pin 8, initiates the delay line sequence and sets the Clock FF. It is reset by the 75 pulse from the delay line (pin U85-2) 75 nanoseconds after it pulses the delay line (75 nanoseconds after the refresh cycle is initiated).

39.   **ROW SELECT COUNTER.** The row select counter (U81A, U81B, and U71) is a six-stage binary counter which supplies a 0-to-63 count of the 64 rows of memory bits to be refreshed on each refresh cycle. (Only one row of memory bits is refreshed in each refresh cycle.) Near the end of the 63rd refresh cycle, the counter is returned to the 0 count and the 0-to-63 cycle is repeated.

The counter is stepped to the next higher count by the positive-going edge of the $\overline{\text{ICLK}}$ signal from the Clock FF. This occurs near the end of the refresh cycle when the Clock FF is reset by the 350 signal from the delay line (pin U85-6). The 350 signal is activated 350 nanoseconds after the start of the refresh cycle. Gating the $\overline{\text{ICLK}}$ signal, which steps the counter, through the Refresh Drivers (U61), which are only enabled during a refresh cycle, ensures that the counter is not stepped during a read or write cycle.

40.   **POWER SENSE FLIP-FLOP.** The Power Sense FF (U65A) senses the presence of line power to the computer through the PON signal. It is clocked once every T-period by the P5NF signal provided the memory is not presently in the first 350 nanoseconds of a memory cycle. (During the first 350 nanoseconds of a memory cycle, the $\overline{\text{ICLK}}$ signal is active, inhibiting the Power Sense FF clock.) If line power fails, it inhibits reading and writing and makes refresh cycles independent of CPU signals and timing.

If line power fails and the PON signal becomes inactive, the next P5NF signal (provided the clock signal is not inhibiting) resets the Power Sense FF. This inhibits read and write cycles by stopping the R/W Delay FF from pulsing the Delay Line and setting the Clock FF. It also makes refresh cycles independent of CPU signals and timing by starting a refresh cycle (by setting the Ref Delay FF) and causing refresh cycles to be initiated directly by the Refresh Oscillator gate U91-pin 6 (through pins 1 and 13 of U82A).

If a read, write or refresh cycle is in progress when line power fails, the clock-inhibiting effect of the $\overline{\text{ICLK}}$ signal enables it to be completed before normal operation is interrupted.

41.   Memory PCA Functional Components.

The following paragraphs describe the operation of each functional unit on a memory PCA. These are the PCA select circuits, the control circuits, the memory IC's, and the bus drivers/receivers.

42.   PCA SELECT CIRCUITS. The PCA select circuits decode memory address bits 13 through 19 to determine if the PCA on which they are located is the PCA selected for the read or write operation to be performed. The PCA select circuits are composed mainly of miniature switch assembly XW1 and exclusive Nor gates U61A through U61D and U81A through U81D.

Bits 13 through 19 of the memory address form the PCA select word. One exclusive Nor gate and one switch are assigned to each bit of the PCA select word. (Bit 12 can be included in the PCA select word by connecting strapping terminals CC.) The identity of each memory PCA is established by setting switches B through H (also switch A if bit 12 is to be included in the PCA select word) to a unique combination of switch settings.

The outputs of all exclusive Nor gates are tied to a common signal line which supplies the signal to the control circuits which indicates the local PCA is selected. For this signal to be active (high) the outputs of all contributing gates must be high. This occurs only when each bit of the PCA select word matches the input to the exclusive Nor gate from the associated switch. Thus, the signal from the exclusive Nor gates which enables the control circuits is only active when the PCA select word matches the PCA identity.

43.   CONTROL CIRCUITS. The control circuits (U171B, U171C, U131A, and U131B) enable readout from the memory IC's to the T-register, in a read cycle, and supply one of two enabling signals to the memory IC's under conditions determined from the input signals to the control circuits. The enabling signal to the memory IC's is the clock signal, supplied to pin 17 on the IC. It, together with the CS signal from the controller, is required to enable read, write, or refresh operations in the IC's.

The input signals to the control circuits are the $\overline{\text{CLK}}$, $\overline{\text{MREF}}$, R/W RR, R/W WR, bit 12 of the memory address word stored in the M-register, and the PCA select signal from the PCA select circuits. The three outputs from the control circuits are two clock signals, one to memory IC row 0 and one to row 1, and the Transmit Enable signal to the bus drivers/receivers. All three signals must be enabled by the PCA select signal which indicates this PCA contains the memory address in the M-register.

The Transmit Enable signal is active (high) when the PCA select signal, $\overline{\text{CLK}}$ signal, and R/W WR signals are active. This occurs during a read cycle or if a protected area of memory has been addressed, in either a read or write cycle, while not operating under DCPC control.

The control circuits supply a clock signal to either the row 0 or row 1 IC's (on an 8K memory PCA) when the $\overline{\text{CLK}}$ signal from the controller is active and the $\overline{\text{MREF}}$ signal from the CPU is not active. Bit 12 of the memory address is used to select the IC row. If bit 12 is low, row 0 is selected to receive a clock signal; if bit 12 is high, row 1 receives the clock signal. On a 4K memory PCA, which has only one row (row 0), the clock signal to the IC's is active when bit 12 is low.

The clock signal is supplied to the IC's during all three cycles; read, write, and refresh. If the $\overline{\text{MREF}}$ signal is active (low), as would be the case during a refresh period, both row 0 and row 1 will receive a CLK signal.

44.   MEMORY INTEGRATED CIRCUITS. The memory IC's store the 16 bits of data from the T-register and the parity bit from the controller parity circuits. The row and column in the IC which identifies the individual all into which a "1" or "0" is to be written is specified by bits 0 through 5 (row) and 6 through 11 (column) of the memory address word from the M-register, as previously described. Reading or writing must be enabled by an active (high) clock signal at pin 17 and an active (low) $\overline{CS}$ signal at pin 5 (SELECT). Reading out the data ("1" or "0") from the selected address is done when the signal at pin 12 (READ/WRITE) is high (provided the clock and $\overline{CS}$ signals are active). When the signal at pin 12 is low and the clock and $\overline{CS}$ signals are active, a "1" or "0" from the T-register can be written into the selected memory cell.

The signal at pin 12 is connected to either the R/W RR or R/W WR signal from the controller, depending on whether terminals AA or BB are connected at strapping option W2 on the memory PCA. If terminals AA are connected, pin 12 is connected to the R/W RR signal and reading out from the memory IC is enabled and writing is inhibited during a refresh cycle. (Actually, no data from the memory IC's reach the T-register during a refresh cycle because the bus drivers/receivers are not transmit-enabled during a refresh cycle.) If terminals BB are connected, the R/W WR signal is connected to pin 12 on the memory IC and writing into the memory IC is enabled and reading out of it is inhibited during a refresh cycle. No data will be written because the $\overline{CS}$ signal is not active during a refresh cycle.

During a read operation, the data bit is read out through pin 7 and supplied to the T-register through the bus drivers/receivers. In a write operation, the data bit from the T-register (or parity circuits) is supplied through the bus drivers/receivers to pin 6 of the memory IC.

45.   BUS DRIVERS/RECEIVERS. The bus drivers/receivers isolate the T-register, on the memory controller PCA, from the memory IC's. They are constantly enabled for receiving but must be enabled, by the control circuits, to transmit data to the T-register. (Although the bus drivers/receivers never inhibit data from the T-register from being supplied to the memory IC's, the memory gates on the controller PCA allow the T-register to transmit data to the memory IC's only under certain conditions during a write cycle. Also, the memory IC's themselves must be enabled, by the control circuits on the memory PCA, to accept data.)

Transmission of memory data to the T-register, through the bus drivers/receivers, is enabled by the control circuits when the PCA is selected by the memory address word and a read cycle is in progress or if an attempt is being made, while not in DCPC mode, to read out of a protected area of memory which is located on this PCA ($\overline{CLK}$ signal active (low), R/W WR signal high, and this PCA selected). (Reading out of a protected area is enabled during a DCPC read operation.)

46.   MEMORY PROTECT VIOLATIONS

The action taken by the memory system when a protected area of memory is addressed depends on several factors: whether the current cycle is a read or write cycle and whether the cycle is a normal CPU-requested cycle or one initiated by the DCPC. In any case, when a memory protect violation occurs, the memory makes no direct attempt to inform the CPU of the violation. That will be done by the memory protect PCA.

47.   Normal Read Cycle

When a memory protect violation occurs in a normal read cycle, the cycle is completed normally except that the data is blocked at the T-register and an all "1"s word is supplied to the S-bus.

48.   DCPC Read or Write Cycle

A DCPC-initiated read or write cycle is completed normally. (The DCPC is allowed to access the protected area of memory.)

49.   Normal Write Cycle

If a protected area of memory is addressed for a normal write cycle, the cycle is not started; because the Write FF will not be set by the Write signal from the CPU. The $\overline{\text{DMAEN}}$ and $\overline{\text{MPV}}$ signals supplied to the memory controller are combined in Nand gate U66B to produce a low level signal to the J input of the Write FF. Then, when the $\overline{\text{Write}}$ signal from the CPU clocks the flip-flop, the flip-flop remains in the reset condition. Since the write cycle must be started by setting the Write FF, the write cycle does not begin.
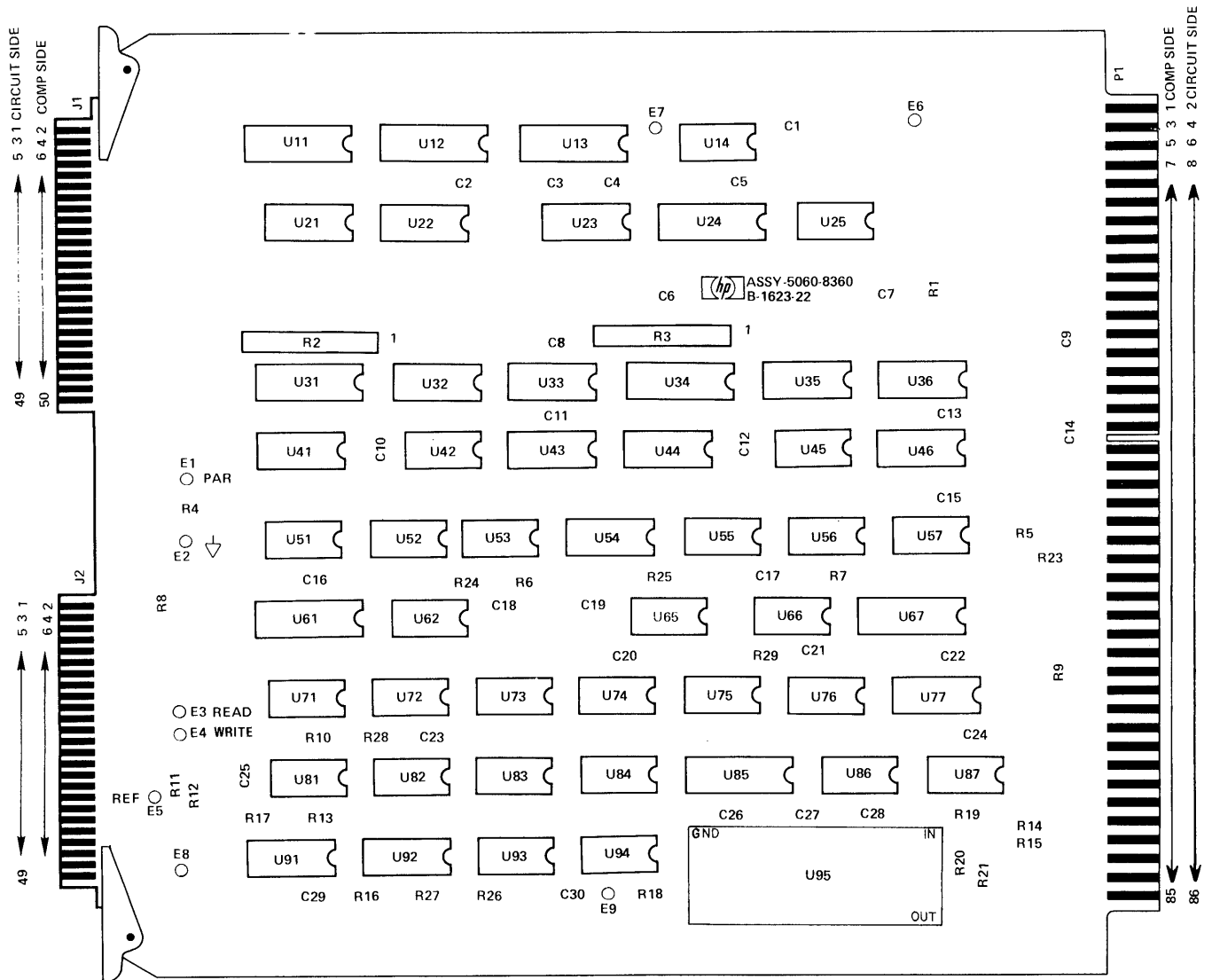
Memory Controller Assy
5060-8360

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
1 3	C2,4,6,10,16,22, 26	CAP 0.1UF		0150-0121			7
1 3 5	C1,3,5,7,8,11, 12,13,15,17-21, 23-25,27,28,30	CAP .01UF		0160-2055			20
	C29	CAP 820PF 5%		0160-3539			1
	C9,14	CAP 3.3UF 20%		0180-0210			2
	E1-9	STUD SOLDER TERM		0360-0294			9
	R19	RES 100 5% .25		0683-1015			1
1	R8,10,26-28	RES 1000 5% .25		0683-1025			5
1	R1,21,23,25	RES 10K 5% .25		0683-1035			4
	R15	RES 330 5% .25		0683-3315			1
1 3	R6,11,12,14 24	RES 470 5% .25		0683-4715			5
1	R7,9,13,18,29	RES 4700 5% .25		0683-4725			5
	R20	RES 100 5% .5		0686-1015			1
	R17	RES 20K 5%.125		0698-4285			1
	R5	RES 7.5K 1%.125		0757-0440			1
	R16	RES 90.9K 1%.125		0757-0464			1
	U66	SOCKET 14 DIP LO		1200-0483			1
		PIN GRV .062X.25		1480-0116			2
	U95	DELAY LINE		1810-0064			1
	R2,3	RES NET 8X500		1810-0132			2
	U87	IC		1820-0054			1
1	U65,81	IC		1820-0077			2

IIA -32

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
	U71	IC		1820-0099			1
	U77	IC		1820-0620			1
	U53	IC		1820-0621			1
	U92	IC		1820-0629			1
13	U25,51,55,66,76, 84,86,93	IC		1820-0681			8
1	U14,57,75	IC		1820-0683			3
	U52,74	IC		1820-0685			2
	U62	IC		1820-0686			1
1	U72,73,94	IC		1820-0690			3
	U83	IC		1820-0693			1
	U91	IC		1820-0730			1
1	U11-13,61	IC		1820-0755			4
1	U24,31,34	IC		1820-0756			3
	U67,85	IC		1820-0760			2
1	U32,35,41,44,54	IC		1820-1077			5
1	U33,36,43,46	IC		1820-1081			4
	U21-23	IC		1820-1113			3
	U42,45	IC		1820-1140			2
	U56,82	IC		1820-1158			2
	R4	RES VAR 50K		2100-3054			1
		EXTRACTOR-PC		5040-6006			1
		EXTRACTOR-PC		5040-6075			1
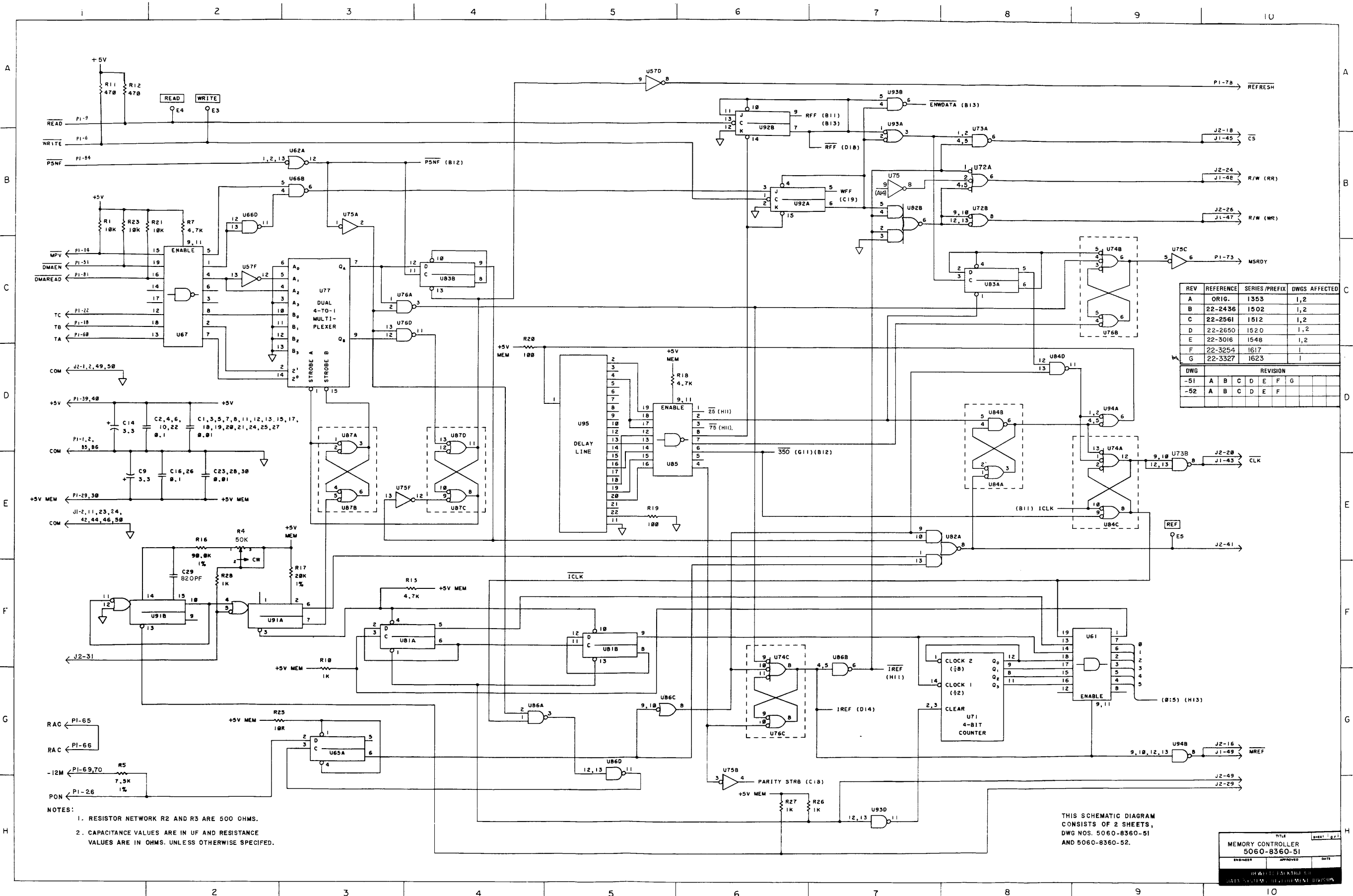
MEMORY CONTROLLER
5060-8360-51

THIS SCHEMATIC DIAGRAM
CONSISTS OF 2 SHEETS,
DWG NOS. 5060-8360-51
AND 5060-8360-52.

NOTES:
1. RESISTOR NETWORK R2 AND R3 ARE 500 OHMS.
2. CAPACITANCE VALUES ARE IN UF AND RESISTANCE
   VALUES ARE IN OHMS, UNLESS OTHERWISE SPECIFED.

Memory Controller
5060-8360-52

HP 2102B
MOS MEMORY SYSTEM

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

CONTENTS

TABLES

1. INTRODUCTION

This document provides theory of operation for the 2102B MOS Memory System used in the 21MX Computer Series and is divided into two sections; general theory of operation and detailed theory of operation. The general theory gives an overview of memory system operations. The detailed theory describes significant events occurring during memory system operations and the functional components that produce them.

NOTE

To operate the 2102B Memory Controller in a 21MX M- or K-Series Computer the controller must be date coded 1728 or above.

2. GENERAL THEORY OF OPERATION

The general theory of operation consists of a description of the memory system and a brief description of each of the three memory cycles.

3. Description

The memory system consists physically of one Memory Controller PCA, part 02102-60001, and one or more of several types of Memory PCA's which can be intermixed on the same controller. The Memory PCA's that are described as part of the 2102B Memory System are:

13187B   32K Bytes (16K Words) Memory Module, part no. 13187-60001

12747A   128K Bytes (64K Words) Memory Module, part no. 12747-60001

NOTE: K= 1024

Other memory modules that may be used as part of the 2102B Memory System are described in the 2102A Theory of Operation.

The memory arrays are organized around 4K (13187B) or 16k (12747A) N channel MOS/RAM IC chips. The word size is 17-bits (2 bytes plus parity bit). The system functions in three cycles: read, write, and refresh. Each type of cycle requires two input/output (I/O) "T" periods in an M-Series and one to three "T" periods in an E-Series Computer.

The read cycle reads out a 16-bit data word from the memory address sent to it by the CPU and transfers it to the S-bus. The write cycle writes a 16-bit data word into the memory address sent to it by the CPU. In the write mode the controller derives a parity bit from the data word and stores the parity bit with the data word in memory. When the data is is retrieved in read mode, the controller again derives the parity of the 16-bit data word and checks it against the parity bit supplied from memory. If they disagree, the CPU IS notified with an error signal.

The memory is composed of semiconductor integrated circuits (IC's) which require refreshing at least every 2 milliseconds. This is done with a refresh cycle that occurrs, automatically, approximately every 16 microseconds. Each refresh cycle refreshes 1/128th of the memory so that the total memory is refreshed, as required , every 2 milliseconds.

The refresh is performed normally in I/O Timing periods T2 and T3 but, when memory is under DCPC control it is performed in periods T4 and T5. This leaves periods T2 and T3 for the DCPC (DMA) read cycle.

The refresh cycle is performed automatically, without external stimulation. When a refresh cycle is started, the CPU is notified so that read and write cycles are inhibited until the refresh cycle is complete.

4. Read Cycle

The read cycle is initiated when the $\overline{\text{READ}}$ signal from the CPU becomes active. The memory address, from the CPU, is supplied to the M-register (on the controller) and memory. It is stored in the M-register to be continually supplied to memory until the data is read out from the stored memory address. The 16-bit word is read out from memory and stored in the T-register and the parity bit is supplied to the parity circuits. The parity circuits check parity, after the result of the check is ready, the parity error status is sent to the CPU. The S-bus gates are opened to enable transfer of the memory data word to the S-bus. Then the controller and memory circuits are restored to the ready-for-new-cycle state.

5. Write Cycle

A write cycle begins with data supplied to memory, to the T-register, and parity circuits on the controller. The T-register stores the data and a parity bit is derived from it by the parity circuits. The address into which the data is to be written is supplied to memory and the M-register. The $\overline{\text{WRITE}}$ signal to the memory controller is activated by the CPU. Then the memory controller enables writing into memory and the M-register stores the address and becomes the address source for memory. The controller opens the memory gates to pass the data from the T-register to memory and the data is written into the selected address of memory.

6. Refresh Cycle

A refresh cycle is initated automatically by an oscillator on the controller PCA. When a refresh starts, reading or writing is disabled by the controller and the CPU is notified that a refresh cycle is in process. A 0-to-127 counter on the controller PCA selects a different row of memory elements within the IC to be refreshed by each refresh cycle (4K RAMS use the counter as a 0-to-63 counter). Essentially, in a refresh cycle the controller only indicates the row of memory elements to be refreshed. Refreshing of the memory elements is performed within the memory IC.

7. DETAILED THEORY OF OPERATION

The detailed theory of operation consists of a description of how a word of memory is addressed, a description of memory signals, identification of the functional units on the memory controller and memory PCA's, a description of initial conditions before a read or write cycle starts, and a tabular summary of a read, write, and refresh cycle.

8. Memory Addressing

The 2102B memory is contained on one or more PCA's. Each PCA contains four rows of memory IC's. There are 17 IC's in a row, one for each bit of the 16-bit data word plus the parity bit. A board may be loaded with 4K or 16K RAM IC's. The 13187B is loaded with four rows of 4k IC's and is referred to as a 16K board. The 12747A is loaded with four rows of 16K IC's and is referred to as a 64K board. The 16K and 64K designations refer to the approximate number of 17-bit memory words the PCA is capable of storing.

NOTE

The word "row" is used, in this discussion, to refer to two different items:

a. A group of IC's arranged in a row on a PCA.
b. A row of memory elements within an IC.

Each 4K IC contains a 64-row by 64-column matrix of memory elements for a total of 4096 (commonly referred to as 4K) memory elements within each IC. A row of 17 such IC's is capable of storing 4096 17-bit memory words, with each bit of the memory word stored in a seperate IC dedicated to that bit.
The bits are stored in identical elements in the IC; that is, the same column and row are addressed on each IC to form the 17-bit word. The 16K IC operates in the same manner except that it has a 128-row by 128-column matrix of memory elements for a total of 16,384.

The basic memory addressing consists of a 15-bit address word. The Memory Expansion Module (MEM), which is part of the DMS option, expands the 15-bit memory address word to a 20-bit memory address word. This provides an addressing capability for one million words of memory. We will use the 20-bit address word for this discussion.

A 20-bit address word is used to select a 17-bit data word stored in memory. To select a memory word, four items must be identified; the PCA, the row of IC's on the PCA, the row of elements within each IC, and the column of elements within each IC . The memory address bits used to identify these items are listed in table 1 for 4k IC's and table 2 for 16K IC's.

Table 1. Memory Addressing 4K RAM IC's

MEMORY ADDRESS BITS	ITEM IDENTIFIED
14 through 19	PCA
12,13	ROW (1 through 4) of IC's on the PCA
6 through 11	COLUMN of elements within each IC
0 through 5	ROW of elements within each IC

Table 2. Memory Addressing 16K RAM IC's

MEMORY ADDRESS BITS	ITEM IDENTIFIED
16 through 19	PCA
14,15	ROW (1 through 4) of IC's on the PCA
7 through 13	COLUMN of elements within each IC
0 through 6	ROW of elements within each IC

Bits 6 through 11 for the 4K IC and bits 7 through 13 for the 16K IC, form a binary word that identifies the column of memory elements. The same is true for the bits that identify the row of elements. The column and row words are supplied to each IC and are decoded within each IC to select the single designated memory element.

For the purpose of refreshing, only the 64 (4K IC) or the 128 (16K IC) rows on each IC are addressed. It is not necessasry to address each individual memory element for refreshing.

9.   Signal Description

Table 3 lists the control and status signals used in the memory and contains a brief description of their function.

Table 3. Memory System Signals

SIGNAL	FUNCTION
$\overline{READ}$	Initiates a memory read cycle.
$\overline{WRITE}$	Initiates a memory write cycle.
$\overline{MPV}$	Indicates a memory protect write violation to the controller. In a DCPC operation, it has no effect. In a normal write mode, no write cycle occurs.

Table 3. Memory System Signals (continued)

SIGNAL	FUNCTION
$\overline{\text{DMAEN}}$	Indicates that a DCPC memory cycle is going to occur. DCPC activity disables memory protection logic. The DCPC is free to read or write in the protected area of memory.
$\overline{\text{DMAREAD}}$	Delays a refresh cycle which might be ready to begin until time periods T4 and T5. (The refresh cycle normally occurs during T2 and T3.) This leaves T2 and T3 for the DCPC read cycle.
$\overline{\text{P4NF}}$-$\overline{\text{P5NF}}$	The last two clock periods occurring in a T period. P4NF, together with TST enables read storing of data into the T-register during a write cycle. The $\overline{\text{P5NF}}$ which occurs in time period T6 (or T3, if a DCPC read cycle is beginning) enables the refresh cycle to begin if one is due.
TA,TB & TC	These signals, when decoded, indicate the current time period. These signals are active in the following "T" periods. TA= T3:T5; TB= T4:T6; TC= T5:T6.
PON	Indicates that the power supply is receiving ac line power and is operating properly. When PON becomes inactive, reading and writing is inhibited and refresh cycles occur every 16 microseconds, independent of conditions external to the memory system.
$\overline{\text{TEN}}$	Opens the S-bus gates to pass data from the T-register to the S-bus after the $\overline{\text{READ}}$ signal has become inactive in a read cycle.
$\overline{\text{TST}}$	Together with the $\overline{\text{P4NF}}$ signal, enables the T-register to store the data from the S-bus in a write operation.
$\overline{\text{MEBEN}}$	Enables the M-register to accept the 20 bit expanded memory address. The basic address bits MB10:MB14 are blocked at U37 of the M-register.
$\overline{\text{METDIS}}$	Indicates a read is being attempted in a protected area of memory. The S-bus read gates are disabled, the S-bus presents an all "1's" word to the CPU. METDIS is suppressed for a DCPC read cycle.
R/$\overline{\text{W}}$ RR	This signal when active, is used to activate the write logic on the memory PCA's.
$\overline{\text{CLK}}$	This signal is required to enable the memory IC's to read or write. Reading or writing is selected by the R/W RR signal.

Table 3. Memory System Signals (continued)
_____

SIGNAL   FUNCTION
_____

$\overline{MREF}$ Informs memory that a refresh cycle is in progress.
                         Used, on the memory PCA, together with the $\overline{CLK}$ signal,
                         to activate the $\overline{RAS}$ input to the memory IC's during a
                         refresh cycle.

RFA0 thru   These seven bits of the address word are used, by the
RFA6   refresh circuits, to select the row of memory elements
                         to be refreshed. The bits are in the form of a binary
                         code which is decoded in the IC to identify the row
                         of memory elements. With 4K RAM IC's only six bits are
                         required, so bit RFA6 is ignored as an address.

MSRDY   Indicates, to the CPU, that the memory system is
(M-or K-   available for another memory cycle.
Series)

$\overline{MBUSY}$ Indicates, to the CPU, that the memory system is busy.
(E-Series)   When the signal is no longer active (goes high) the
                         memory system is available for another memory cycle.

$\overline{REFRESH}$ Indicates, to the CPU, that a refresh cycle is about to
                         begin. Read and write cycles are inhibited during a
                         refresh cycle.

$\overline{PE}$ Indicates to the CPU that the data word read from
                         memory, during the current cycle, contains a parity
                         error.

$\overline{CS}$ and R/$\overline{W}$(WR) activated by the controller but they are not
used with the Memory PCA's discussed in this text.
_____

10. Functional Unit Identification

In the following discussion, it is necessary to refer to the functional
units of the memory system, such as flip-flops, multiplexers, and
registers by name. Since the functional units may not be identified
by name on the logic diagrams, they are listed in tables 3 and 4,
along with their reference designations and the logic diagram
coordinate location, to enable use of the logic diagram in following
the discussion.

Table 4. Memory Controller Functional Units

NAME and COORDINATE		REFERENCE DESIGNATIONS
Read flip-flop (FF)	D1	U 57B
Write FF	E1	U 57A
R/W Delay FF	D2	U 53B
MSRDY FF	C2	U 23C and U 23D (not used on E-Series)
MBUSY Gate	C2	U 32 (not used on M-Series)
Clock FF	F3	U 63D and U 83C
Delay Line	D4	U 42
Delay Line Buffer	E4	U 52
Delay Multiplexer	F5	U 62
Address Drivers	E12-14	U 14,35, and 37
M-register	C12-14	U 17,27,45,and 47
T-register Control FF	C15	U 53A
T-register	D16-20	U 75,85,95,and 105
T-register Multiplexer	D15	U 44
S-bus Gates	B16-20	U 77,87,97,and 107
Data Drivers	E17,19	U 84 and 104
Parity Circuits	C17,19	U 74 and 94
Refresh Oscillator	E6,7	U 61A and 61B
Refresh Sync FF	E8	U 71C and 71D
Refresh Pending FF	D7	U 71A and 71B
Refresh Decoder	D7	U 81
Refresh FF	E8	U 102
Refresh Delay FF	C3	U 23A and 23B
Refresh Cycle FF	F8	U 83B and 101D
Refresh Address Counter	F6	U 24
Refresh Drivers	F7	U 25
Power Sense FF	B9	U 102B

Table 5 Memory PCA Functional Units

NAME and COORDINATE		REFERENCE DESIGNATION
Board Select Circuits	H2	U 101 and 111
Bus Drivers/Receivers	A3-9	U 12,32,42,52, and 62
Control Receivers	F1	U 142
Address Multiplexer	F4-I4	U 53,83, and 103 (Element, Row and Column, Select)
IC Row Select Decoder	J4	U 72 and 82
IC Row Select Drivers	J6	U 73
Timing Line	H6	U 132

11. Pre-Cycle Conditions

When no cycle is in progress the following conditions exist in the memory system:

a. The M-register is open so that any address supplied by the CPU passes thru the M-register and the address drivers to the memory modules.

b. The M-register is ready to accept any address supplied to it but
will not store the address until early in a read or write cycle.

c. The memory IC's are disabled for both reading and writing.

d. The memory address, for a read or write cycle is supplied to the
M-Register and memory either before or approximately at the time
the READ or WRITE signal from the CPU becomes active.

e. The T-register is not receptive to data from memory or the S-bus.

f. The S-bus gates are disabled for passage of data from the
T-register, or memory, to the S-bus and for passage of data from
the S-bus to the T-register and memory.

g. The T-register data drivers are disabled for passage of data from
the T-register to memory.

h. The MSRDY signal (M- or K-Series only) to the CPU is active (high)
indicating the memory system is ready for a cycle.

i. The MBUSY signal (E-Series only) to the CPU is inactive (high)
indicating the memory is ready for a cycle.

12. Functional Component Description

The following paragraphs describe each functional unit on the memory
controller PCA and the memory PCA. Refer to tables 4 and 5 for a
cross reference between the reference designations used to identify
these functional unit on the logic diagram and the names with which
they are identified in this discussion. Refer to logic diagram
02102-60001 for logic details of the memory controller and to diagram
5950-3749 for logic details of the memory PCA's. Simplified timing
diagrams are located at the end of this text.

13. Memory Controller PCA Functional Components

The following paragraphs describe the function of the functional units
on the memory controller PCA.

14. READ FLIP-FLOP. The Read FF stores the occurrence of an active
READ signal from the CPU to initiate a read cycle. The output of the
read FF activates the MBUSY signal to an E-Series CPU, sets the R/W
Delay FF which pulses the delay line. The Read FF output is also sent
to the T-register Control FF (U53A). The Read FF output combined with
ICLK, activates the T-register Control FF on the leading (negative
going) edge of the 300 delay line signal. With the T-register Control
FF active (U53 pin 5 low) the B inputs to the T-register and the
T-register multiplexer are selected. As a result, the T-register
accepts data from memory and Nand gate U55D is permitted to pass the
parity bit from memory to the parity circuits.

If the read cycle is using DMS in an E-Series Computer (E·MEM), The
Read FF is reset approximately 425 nanoseconds after the delay line is
pulsed. Under all other conditions the Read FF is reset approximately
375 nanoseconds after the delay line is pulsed. The reset condition of
the Read FF deactivates the MBUSY signal to the CPU.

15. WRITE FLIP-FLOP. The Write FF stores the occurrence of an active WRITE signal to initiate a write cycle. When the FF is set, The MBUSY signal is activated and sent to an E-Series CPU, sets the R/W Delay FF which pulses the delay line. This produces the sequence of events listed in the delay line discussion. When set the Write FF enables the passage of data from the T-register to memory and also enables the parity bit from the parity circuits to pass to the memory IC's.

The Write FF is reset approximately 425 nanoseconds after the delay line is pulsed. The reset condition of the Write FF, along with a no-refresh cycle condition sets R/W̄ RR signal to the memory PCA's in the inactive (high) condition to enable reading data from the memory IC's. Also, the reset state of the Write FF and the active TST signal from the CPU enables the S-bus gates to pass data from the S-bus to the T-register. The T-register stores this data for transmission to the memory.

16. R/W DELAY FLIP-FLOP. The R/W Delay FF (U53B) pulses the delay line when triggered by the set condition of either the Read FF or the Write FF. It is reset approximately 75 nanoseconds after the delay line is pulsed. The set condition sets the MSRDY FF to deactivate the MSRDY signal to an M-series CPU. This informs the CPU that the memory system is not available. Also, a PULSE signal is sent to the M-register to inhibit the M-register from accepting any new address and inhibits the S-bus write gates from accepting new data from the CPU.

17. MSRDY or MBUSY SIGNAL. The MSRDY FF (U23C&D), when set deactivates the MSRDY signal to an M-Series CPU to indicate the memory system is unprepared to accept a request for a read or write operation. It is set at the beginning of a refresh, read, or write cycle. It is reset approximately 300 nanoseconds after the delay line has been pulsed. The MBUSY performs a similar function in an E-Series CPU except that it is active low and output via OR gate U32. The MBUSY signal is active (low) during the periods that the Read or Write FF is set or when the IREF (internal refresh) signal is low. The MBUSY active signal indicates to an E-Series CPU that the memory system is unprepared to accept a read or write command.

18. CLOCK FLIP-FLOP. The Clock FF (U63D and U83C), when set (U83-8 high), activates ICLK to gate U34. The trailing (negative going) edge steps the RFA (refresh address) counter (U24) during a refresh cycle. ICLK is used with RFF to reset the T-register Control FF U53 when clocked by the 300 pulse from the delay line. ICLK to the M-register gate and the Power Sense FF (U102). The CLK signal to the memory modules. The CLK signal must be active for each memory IC to be read out of, written into, or refreshed.

The Clock FF is set and reset by signals from the Delay Multiplexer (U62). For an E-Series DMS read cycle the clock is set by 50 and reset by 425. For all other memory cycles, the Clock FF is set by the R/W Delay FF or the Refresh Delay FF (U23A and B) and reset by 375. Resetting the Clock FF deactivates ICLK, ICLK, and CLK. If the cycle is a refresh cycle, the trailing (negative going) edge of ICLK gated

with IREF (U34A) increments the RFA counter in preparation for the next refresh cycle. ICLK is used to reset the Power Sense FF, after completing the current cycle, in the event of a power failure.

19.   DELAY LINE. The Delay Line (U42) is used in every memory cycle and generates nine signals at fixed intervals with respect to its input pulse. The delay line outputs are buffered and inverted in the Delay Line Buffer (U52). The buffered signals are active in the low state. The signal names 50, 75, 300 etc, refer to the buffered delay line outputs occurring at 50, 75 and 300 nanoseconds after the delay line input signal. The pulse that passes through the delay line is approximately 90 nanoseconds wide.

The events resulting from each of the output pulses are as follows:

OUTPUT PULSE	U33 or U52 PIN NO.	EFFECT
$\overline{50}$	U52-18	When active low sets the Clock FF for an E-Series DMS read cycle.
$\overline{75}$	U33-8	Resets the R/W Delay FF and Refresh Delay FF (U23 A and B), terminates the delay line input signal producing a pulse approximately 90 ns wide in the delay line.
$\overline{300}$	U52-16	When activated, resets the MSRDY FF and clocks the T-register Control FF.
$\overline{325}$	14	If the memory cycle is a write or refresh cycle $\overline{325}$ terminates the CLK at U93B to the memory modules.
$\overline{375}$	12	While $\overline{375}$ is active and $\overline{425}$ is not active, a reset pulse approximately 50 ns wide clears the Read FF and restores the MBUSY to its inactive state. This same reset pulse becomes a CLKCLR pulse to hold the M-register latch closed. This pulse is selected for all memory cycles except an E-Series DMS read.
$\overline{400}$	9	When selected by the Delay Multiplexer (all cycles except an E-Series DMS read) sets the T-register Control FF causing the T-register to store data returned by the memory module during a read cycle. For a write cycle this pulse has no effect on the T-register Control FF for it is already set. This pulse also clears the Clock FF. Refer to paragraph 13 for description of the Clock FF.

$\overline{425}$ 7   For an E-Series DMS read cycle the $\overline{425}$ active and $\overline{475}$ not active perform the same function described in $\overline{375}$ (U62 pin 2). For all other read cycles $\overline{425}$ terminates the activity started at $\overline{375}$ and generates a parity strobe (U62 pin 6). Resets the Write FF or the Refresh Cycle FF in a write or refresh cycle.

$\overline{450}$ 5   During an E-Series DMS read, $\overline{450}$ will perform the same read functions described in $\overline{400}$.

$\overline{475}$ 3   During an E-Series DMS read, $\overline{475}$ will perform the same read functions described in $\overline{425}$.

20. DELAY LINE MULTIPLEXER. The Delay Line Multiplexer (U62) select input (pin 1) is used to select the A or B input lines (with the gate pin 15 tied low). The A inputs are selected when pin 1 is low and B when pin 1 is high. The select line is controlled by OR gate U83 output pin 12.

When using any M-Series computer or an E-Series computer without DMS (Dynamic Mapping System) the jumper at U83 pin 13 is installed in the W2 position forcing the select line high and selecting the B inputs for all read cycles. An E-Series computer with DMS will have the jumper installed in W3 forcing pin 13 high. When the signals at pins 1 and 2 are inactive the output of U83 will be low causing the select line to select the A inputs of the multiplexer. This will be during a read cycle; when a write or refresh cycle is in progress the signal at either pin 1 or pin 2 becomes active, again selecting the B inputs.

21. M-REGISTER. The M-register (U17,U27,U45, and U47) stores the memory address to be acted upon in a read or write mode. The address is received from the M-bus and is supplied to the memory PCA's in both read and write mode. The M-register is open during the time between the end of the delay line pulse from the last cycle (approximately 500 nanoseconds after the delay line was pulsed in the last cycle) and the time the $\overline{PULSE}$ signal becomes active when the next cycle is initiated. The M-register is receptive to the address supplied to it in both read and write cycles. The address present at the M-register input when the $\overline{PULSE}$ signal becomes active (low) is the one that will be stored in the register.

The contents of the M-register are supplied to the bus linking the register and the memory PCA's at all times except during a refresh cycle.

When operating without DMS, the signal $\overline{MEBEN}$ (memory expansion bus enable) is inactive (high). This prevents the random information on the MEB lines from being supplied to the memory PCA's. With DMS installed the active $\overline{MEBEN}$ signal allows the expanded memory address bits to be supplied to the memory PCA's while inhibiting the original page address bits MB10:MB14 at U27.

22. ADDRESS DRIVERS. The Address Drivers (U35,U37, and U14) are used to buffer the M-register. In addition U35 is switched off during a refresh cycle to isolate U45 of the M-register from the memory IC's, while the refresh row address is being sent to memory by the Refresh Address Driver (U25).

23. T-REGISTER CONTROL FLIP-FLOP. The T-register Control Flip flop (U53A) in the reset (Q low) condition selects the B inputs of the T-register and the T-register Multiplexer. This allows the T-register to accept data from the memory PCA's during a read cycle. The read data is supplied to the S-bus after the READ signal from the CPU becomes inactive (high) and the TEN (transmit enable) signal from the CPU is active (low). The TST (T store) signal from the CPU in a write cycle causes the T-register and T-register Multiplexer to select their B inputs.

The T-register Control FF is active (reset) only during read mode. It is active from the leading (falling) edge of the 300 signal (while the Clock FF is set) until the CLOSE-T signal as the 400 or 450 pulse from the delay line becomes active.

24. T-REGISTER. The T-register (U75,U85,U95, and U105) stores data in process of transfer between memory and the S-bus in a read cycle and between the S-bus and memory in a write cycle. It is controlled by the T-register Control FF in read mode and by the TST signal from the CPU in write mode.

The T-register accepts data in a write cycle during P4 while the TST signal from the CPU is active (low) and the data is on the S-bus. Data is accepted from memory during a read cycle starting with the leading edge of 300 (with RFF and ICLK present on the Control FF) and ending with CLOSE-T (400 or 450 delay line output becomes active).

When the select A/B signal is high, the T-register accepts the data at its B inputs from either the S-bus gates or memory. The outputs are applied to the Parity Generator/Checker,Data Drivers, and the S-bus Gates. When The select A/B signal is high the T-register can be considered to be in the accept input mode.

The low condition of the select A/B signal selects the A inputs and puts the register in the store mode. The inputs which were applied to the B inputs when the select A/B signal was high are now stored in the register and are still applied to the same external circuits.

Although the T-register is made up of IC's designed to be multiplexers, the latching effect normally associated with flip-flops is achieved by connecting the outputs back to its A inputs. This latching effect results from the fact that in the internal circuits of the IC, the A inputs are selected and supplied as outputs before the B inputs are deselected. After the short overlap period in which both the A and B inputs are selected, the B inputs are deselected. Because of the overlap the B inputs are locked into the A output loop. The inputs remain stored there until the B inputs are again selected; then the stored data is replaced with new data.

25. S-BUS GATES. The S-bus gates (U77,U87,U97, and U107) isolate the T-register from the S-bus. When U87 and U107 are enabled for receiving by the $\overline{TST}$ signal and the controller signals from U54 through AND gate U65B, the S-bus gates open to pass the contents of the S-bus to the T-register. The T-register stores the data during a write cycle at the occurrence of the P4 period while the $\overline{TST}$ signal from the CPU is active (low).

When U77 and U97 are enabled for transmitting by active (low) $\overline{TEN}$ and inactive (high) $\overline{METDIS}$ signals from the backplane, the gates pass the contents of the T-register to the S-bus. This condition occurs during a read cycle. $\overline{METDIS}$ is active only when an attempt is made to read a protected memory address in a normal read cycle.

26. DATA DRIVERS. The Data Drivers (U84 and U104) isolate the T-register from memory. They are enabled only during a write cycle by the $\overline{WFF}$ and WFF signals from the Write FF and pass the data stored in the T-register to the memory bus drivers and receivers.

27. T-REGISTER MULTIPLEXER. The T-register multiplexer (U44) supplies the parity bit from memory to the Parity Generator/Checker (U74 and U94) for parity checking during a read cycle and stores the parity bit for continued application to the parity circuits during a read cycle after its outputs are disconnected from its B inputs by deactivation of the T-register Control FF.

Like the T-register, the A or B inputs of the multiplexer are selected to be output by the select A/B signal derived from $\overline{TST}$ and $\overline{P4NF}$ signals in the write mode and from the T-register Control FF in the read mode. When the A/B signal is high, the B inputs are selected as outputs; when it is low, the A inputs are selected as outputs.

In write mode although the parity bit is supplied to the multplexer at pin 10 it is blocked from being returned to the parity circuits by a low DREAD signal at pin 13 of U55D.

28. PARITY GENERATOR/CHECKER CIRCUITS. The parity circuits (U74,U94, and U64) generate a parity bit (MDS16) in write mode, and supply it to memory along with the 16 data bits. In read mode, they check the parity bit and generate a $\overline{PE}$ (parity error) signal to the CPU if the parity generated from the 16 data bits does not agree with the parity bit supplied from memory.

In a read cycle, the parity bit (MDS16) is supplied from memory, through the T-register multiplexer B inputs and NAND gate U55D, to the parity circuits. If a disagreement exists between the parity bit and the parity of bits 0 through 15 stored in the T-register, The $\overline{PE}$ signal becomes active near the end of the cycle when the parity strobe (at 425 or 475) from the delay line becomes active at U54A setting the Parity Error FF. The TEN signal from the CPU is inverted in U67, this signal PAREN is used to gate the Parity Error FF output to the CPU at U66. The PAREN signal activates U66D when the word read out of memory is being transfered to the S-bus. The active $\overline{PE}$ signal informs the CPU that the word being sent contains a parity error.

The T-register Multiplexer outputs are disconnected from the B inputs by the CLOSE-T (at $\overline{400}$ or $\overline{450}$) signal . The parity bit and the DREAD signals are latched into the multiplexer with the A inputs supplying the outputs of the multiplexer and the parity circuits.

Although the parity bit generated by the parity circuits in the write mode passes through the T-register multiplexer, it is blocked at NAND gate U55D by the inactive (low) DREAD signal and does not reach the parity circuits.

29. REFRESH OSCILLATOR. The refresh oscillator U61A and U61B is a free-running osciillator, that generates a negative pulse at U61-9 and a positive pulse at U61-10 to initiate a refresh cycle approximately every 16 microseconds. This is approximatey one refresh cycle for every 10 I/O cycles, (an I/O cycle is composed of time periods T2 through T6). The normal refresh cycle is started by the negative output of the oscillator at pin 9 setting the Refresh Sync FF. In the event of a power failure the positive output (pin 10) of the oscillator is used with the inactive outputs of the Power Sense FF to refresh the memory IC's independent of the CPU.

30. REFRESH SYNC FF. The Refresh Sync flip-flop U71A and U71B, when set by a pulse from the refresh oscillator, enables the B output of Multiplexer U81 at pin 9. This allows the Refresh Pending flip-flop U71C and U71D to be set during the next T4 time period. The Refresh Sync FF remains set only until the Refresh Pending FF is set. Setting the Refresh Pending FF (U71C and U71D) produces a negative signal at U71-8 which resets the Refresh Sync FF and disables the B output of the multiplexer (U81).

Once reset, the Refresh Sync FF remains so until the next refresh oscillator pulse initiates a new refresh cycle.

31. REFRESH PENDING FF. The Refresh Pending flip-flop U71C and U71D is set when the $\overline{P5NF}$ becomes active (low) in the first T4 period following a Refresh Oscillator pulse. When set, it enables the A output of the Refresh Multiplexer U81-7. It also resets the Refresh Sync FF, disabling the B output of the multiplexer and activates the $\overline{REFRESH}$ signal to the CPU to inform it that a refresh cycle is starting. It remains set until the Refresh Start FF is set. This occurs at the end of the first T6 period following the Refresh Oscillator pulse if the Dual Channel Port Controller (DCPC) signal $\overline{DMAREAD}$ is not active. If the $\overline{DMAREAD}$ signal is active, the Refresh Start FF is set and the Refresh Pending FF is reset at the end of the next T3 period, leaving time periods T2 and T3 for DMA (DCPC) activity.

Once reset the Refresh Pending FF remains reset (U71-11 low) until the refresh oscillator initiates the next refresh cycle. The refresh pending reset disables the A output of the refresh multplexer, holds the $\overline{REFRESH}$ signal in the inactive condition, and returns the Refresh Start FF to the reset condition.

32. REFRESH SYNC DECODER. The Refresh Sync Decoder (U81) is a dual
4-line to 1-line data selector multiplexer used to synchronize refresh
operations with I/O timing. This is done by using the TA and TB
signals as a binary count of 0 to 4 to select one of the four inputs
in each of the two input sets (set A and set B) to be supplied as
output. Only two inputs of the A input set (pins 4 and 5) are used and
the B input set uses only one (pin 10) input. The unused inputs are
grounded. The A output is pin 7 and the B output is pin 9.

When enabled by the Refresh Sync FF, the B output enables setting of
the Refresh Pending FF at the next $\overline{P5NF}$. The Refresh Pending FF low
output at pin 8 enables the decoder A output. The A output at the next
$\overline{P5NF}$ of T6 or T3 initates a refresh cycle by setting the Refresh Start
FF (U102) and the Refresh Cycle FF (U80A and U101D).

The B input, TC, is selected when TA and TB are both active. Thus, the
B output becomes active (high), provided that it is enabled by the
Refresh Sync FF, during the I/O time period T4 [(TA)(TB)($\overline{TC}$)]. With
the B output high during T4, occurrence of $\overline{P5NF}$ sets the Refresh
Pending FF.

The Two A inputs are used to select the T period in which a refresh
cycle is to be iniated. The normal start time is when the P5NF signal
becomes active during period T6. However, if a DMA (DCPC) read cycle
is in progress, the start time is delayed until the $\overline{P5NF}$ signal
becomes active during T3. This leaves periods T2 and T3 free for the
DCPC operation.

The $\overline{DMAREAD}$ signal is selected by the TA and TB select signals during
period T6 (pin 5 of the decoder) for a normal cycle and period T3 (pin
4 of the decoder) for a DCPC read operation. When the signal DMAREAD
is inactive (high) it is applied high to the decoder at pin 5 and if
the A output has been enabled by the Refresh Pending FF, A normal
refresh cycle is initiated when the $\overline{P5NF}$ signal becomes active at T6.
If the $\overline{DMAREAD}$ signal is active (low) it is applied high to the
decoder at pin 4, now with the A output enabled a DCPC (DMA) refresh
cycle will be initiated when the $\overline{P5NF}$ signal becomes active at the end
of T3.

33. REFRESH START FF. The Refresh Start flip-flop (U102), set by the
Refresh Sync Decoder and the $\overline{P5NF}$, resets the Refresh Pending FF
disabling the decoder (U81) A output and disables the REFRESH signal
to the CPU. With PONFF active at U92A the Refresh Delay FF is set
(U23A and U23B) and the Parity Error FF (U32) is disabled. The Refresh
Delay FF initiates the delay line sequence, sets the Clock FF and
MSRDY FF. The Refresh Start FF is set by the Refresh Sync Decoder A
output, at the end of time period T6 for a normal refresh cycle, or at
the end of the T3 period for a refresh cycle when memory is under DCPC
read (DMAREAD) control.

34.   REFRESH CYCLE FF. The Refresh Cycle FF (U83B and U101D) is set by the same decoder output and P5NF signal as the Refresh Start FF. When set, it initiates the MREF, IREF, and IREF signals. The MREF signal is sent to memory to indicate that a refresh cycle is beginning. The IREF and ICLK signals are used to step the Refresh Address Counter (U24). The IREF and IREF signals are used to gate the Refresh Address Driver (U25) on, gate the M-register Address Driver (U35) off, and to inhibit several read and write signals. IREF also activates the MBUSY signal to an E-Series CPU. The Refresh Cycle FF is reset by the 425 pulse from the delay line.

35.   REFRESH DELAY FF. The Refresh Delay FF (U23A and U23B), when set by the active output of the start FF and gate U92A-6 initiates the delay line sequence, sets the Clock FF (U83 and U63), and set the MSRDY FF to inform an M-Series CPU that memory is busy. The Refresh Delay FF is reset by the 75 pulse from the delay line.

36.   REFRESH ADDRESS COUNTER. The Refresh Address Counter (U24) is a seven stage binary counter which supplies a 0-to-127 row address of memory bits to be refreshed. Only one row of memory bits is refreshed in each refresh cycle. Near the end of the 128th cycle the counter is returned to zero and the count cycle is restarted. The 4K memory IC'S use only the first 64 counts and ignore RFA6. The full 128 row addresses are required for the 64K memory IC's.

The counter is stepped to the next higher count by the negative going edge of the ICLK signal from the Clock FF. This occurs near the end of the refresh cycle when the Clock FF is reset by a signal from the Delay Line Multiplexer. Gating the ICLK signal with the IREF signal ensures that the counter is stepped only during a refresh cycle and not during a read or write cycle. Also,the IREF and IREF signals enable the Refresh Address Driver only during the refresh cycle.

37.   POWER SENSE FF. The Power Sense FF (U102B) senses the presence of line power to the computer through the PON signal from the CPU. It is clocked every memory cycle by the trailing edge of the ICLK signal. This allows the current cycle to be completed in the event that line power fails. If line power fails, reading and writing are inhibited and refresh cycles become independent of CPU signals and timing.

When line power fails the PON signal becomes inactive, the next trailing edge of the ICLK signal resets the Power Sense FF. This inhibits read and write cycles by disabling the MSRDY or the MBUSY signals to the CPU at U64. It also makes the refresh cycles independent of the CPU signals by causing the refresh cycle to be started directly by the Refresh Oscillator output at pin 10.

38. Memory PCA Functional Components.

The following paragraphs describe the operation of the functional units on a memory PCA. These are MDS-bus drivers/receivers, board and row select circuits, the memory IC's, and the address control and multiplexer circuits.

39. MDS BUS DRIVERS/RECEIVERS. The 17-bit Memory Data Signal Bus (MDS00 through MDS16) is driven (read cycle) and received (write cycle) by line driver/receivers U12, U62, U52, U42, and U32. The receivers are always enabled and write data is available to the data-in pins of the memory IC's whenever transmitted from the controller PCA but the memory IC's must be enabled before the data is stored. The MDS-bus drivers are enabled for a read cycle by an active (low) DRIVEMDS. The DRIVEMDS signal (U161) becomes active 30 nanoseconds after the clock ($\overline{CLK}$) is active, if it is not a refresh cycle ($\overline{MREF}$ high), not a write cycle (R/$\overline{W}$ RR high), and the board is selected (BDSELECT high).

The DRIVEMDS signal also enables the parity bit (bit 16) to be sent to the MDSBUS through U142.

40. BOARD SELECT CIRCUITS. The board select circuits (U101 and U111), exclusive-NOR gates compare the high order address with a jumper plug configurable board address (refer to your Memory Module Installation Manual for memory module assignments and jumper configurations). Memory address bits 16 through 19 for 16K RAM IC's or 14 through 19 for 4K RAM IC's form the board select word. The identity (module assignment) of each memory board is established by installing jumpers in XW1 A through F. Jumpers A, B, and C of XW2 are only installed for 4K RAMS and must be out for 16K RAMS.

The outputs of the EXNOR gates are tied to a common signal line which supplies the signal (BDSELECT) to the control circuits to indicate that the board has been selected. This signal is active (high) only when each bit of the board select word matches the input to the gate from the associated jumper. When the board select word matches the board identity the BDSELECT signal becomes active, selecting the B inputs of the Row Select Multiplexer (U72) and enabling the MDS-bus drivers during a read cycle (U161).

Gates U111C and D and their associated jumpers are used for partial loading of memory IC's.

41. ROW SELECT CIRCUITS. The Row Select Decoder (U82) decodes two address bits, 12 and 13 (XW3 E and G jumpers in) for 4K RAMS or 14 and 15 (XW3 D and F jumpers in) for 16K RAMS, to provide a one of four selection of the four rows of memory IC's. The active low signal ($\overline{RS0}$, $\overline{RS1}$, $\overline{RS2}$, or $\overline{RS3}$) forces the corresponding output of the Row Select Multiplexer (U72) high when the B inputs are selected (BDSELECT high).

The high GATE output enables the appropriate $\overline{RAS}$ driver (U73) when the CLOCK signal is present in a read or write cycle. The active $\overline{RAS}$ (Row Address Strobe) output of the driver is applied to pin 4 of all 17 memory IC's in the selected row. These IC's are now enabled to accept the row address bits. The $\overline{RAS}$ signal remains active for the duration of CLOCK.

If a refresh cycle is to be performed, the memory controller will issue $\overline{MREF}$ (low), activating BMREF (high), disabling the Row Select Multiplexer (U72-15). This forces the GATE0 through GATE4 lines high. Thus when the CLOCK signal becomes active, all rows of all installed memory PCA's will receive a $\overline{RAS}$ signal, regardless of Board Select or Row Select Decoder outputs. The refresh signals $\overline{IREF}$ and IREF disable the low-order M-register address Driver (U35), preventing the M-register from supplying the low-order address to the memory PCA. The low-order address will be furnished by the Refresh Address Driver (U24). The $\overline{CAS}$ (column Address strobe) signal is not required for a refresh cycle and refreshing of the memory elements is performed within the memory IC's.

42. ROW/COLUMN ADDRESS CIRCUITS. Drivers U53, U83, and U103 are used in conjunction with their control circuits to multiplex the memory row and column address from the CPU to the memory IC's.

The Address Flip Control gates U131A through D are used to generate the gating signals for the drivers of the Address multiplexer. The idle state for the $\overline{GATELO}$ signal (when no cycle is in progress) is low. The active $\overline{GATELO}$ enables driver U53 of the Address Multiplexer, resulting in the low order (row) address bits (A0:A6) being presented to the memory IC's as soon as the address is available from the M-bus. The address was available before the CLOCK became active. The ground at pin 17 of U83 ensures that the CAS line is held inactive. Bit A6 is used by the 4K RAMs as $\overline{CS}$ (chip select). Also the active $\overline{GATELO}$ signal applied to U131B and C ensures that GATEHI4K and GATEHI16K are inactive therefore U83 and U103 are disabled. When any cycle is initiated, the CLOCK signal becoming active fires the appropriately enabled $\overline{RAS}$ Driver and the Timing Line U132. With the row address strobe ($\overline{RAS}$) applied to the selected row of memory IC's (except for a refresh cycle when all rows are activated) the row address is stored in the memory IC's. The address continues to be supplied until $\overline{GATELO}$ becomes inactive.

The T30 output of the Timing Line is applied to U31A and U31D (30 nanoseconds after CLOCK). RAM Select jumper XW1-G is in for the RAMs used with the 13187B or the 12747A boards, and holds FASTCYC low (inactive) inhibiting SWITCH30. When the T90 output of the Timing Line becomes active it and the T30 signal at U131D switch the output, SWITCH90, low and U163C output $\overline{GATELO}$, high. The inactive $\overline{GATELO}$ signal disables U53, removing the row address bits and $\overline{CAS}$ inhibit signal from the memory IC's.

The inactive $\overline{GATELO}$ signal to U131B and C allows either of these gates to be enabled. The RAM Select jumper XW1-H is out for 4K RAMs and in for 16K RAMs. The signal 4KRAM is active (high) for a 4K RAM board. The active 4KRAM and inactive $\overline{GATELO}$ signals cause U131C output to become active (low). The U131C output GATEHI4K activates U83 to pass the high order column address bits 6 through 11 to the memory IC's. If

this is a read or write cycle $\overline{BMREF}$ will be inactive high and is used to enable $\overline{CS}$. When ALLOWCAS becomes active at pin 17, the memory IC's will store the column address. If this is a refresh cycle $\overline{BMREF}$ will be active (low) and $\overline{CS}$ will be inactive inhibiting the memory IC from accepting the column address.

The signal 4KRAM is inactive (low) for a 16K RAM board. This will lock out U131C and U83 will not be selected. Gate U131B will be enabled by the inverted 4KRAM signal from U162C when $\overline{GATELO}$ becomes inactive. The output of U131C, $\overline{GATEHI16K}$, becomes active (low), enables U103, and presents the 16K RAM high order column address bits (A7:A13) to the memory IC's. Generation of ALLOWCAS is delayed, for the 13187B and 12747A boards, to allow the column address to fully stabilize. Any active output of U161B, U163A or U163B will force ALLOWCAS high (active).

For the 13187B board FASTCYC is inactive inhibiting U161B. The inactive FASTCYC and inactive 16KRAM signal at U162B produce an inactive 4KSLOW signal to U163B. CLOCK is active for all cycles, and when T120 becomes active the output of U163B (4KCAS) goes low forcing ALLOWCAS high. U83 is enabled at this time and ALLOWCAS at pin 1 is inverted and applied to the memory IC's as $\overline{CAS}$ (column Address Strobe). If this is a read or write cycle ($\overline{BMREF}$ inactive) the column address will be stored in the selected row of memory IC's.

For the 12747A board, if a read or write cycle is in progress the active 16KCAS output of U163A is generated by CLOCK (active), $\overline{BMREF}$ (inactive), and T120 active. The low (16KCAS) output of U163A forces ALLOWCAS high. U103 is enabled at this time and ALLOWCAS at pin 17 is inverted and applied to the memory IC's as $\overline{CAS}$ (Column Address Strobe). The column address will be stored in the selected row of memory IC's. During a refresh cycle $\overline{BMREF}$ would be active inhibiting U163A. Therefore, 16KCAS would be high, ALLOWCAS would remain inactive, and the memory IC's would not be enabled to accept a column address.

43. Memory Array Summary.

To summarize the events that have occurred: the board has been selected (BDSELECT high), the row has been selected (one of four $\overline{RAS}$ lines low), the IC row address is stored, the column address is stored, it is established that this is not a refresh cycle ($\overline{BMREF}$ low), the $\overline{CS}$ signal is active for 4K IC's, and the active $\overline{RAS}$ then $\overline{CAS}$ (low) are applied to the IC's. This state will remain until the active $\overline{CLK}$ (low) from the controller becomes inactive.

The selected row of memory IC's on the selected board is now ready to complete a read or write cycle. For a write cycle, the R/$\overline{W}$ RR (low) signal from the controller (which has been present from the beginning of the cycle) causes $\overline{WRITE}$ (U142-3) to be applied to pin 3 of all arrays. With the stable address and the other memory conditions as discussed above, data bits and the parity bit that have been available on the MDSBUS and the receivers are accepted at pin 2 and stored at the specified address.

For a read cycle the data is read out of the selected IC's when the address is gated in. The bus drivers have been activated by the inactive $\overline{MREF}$ (high) signal, the inactive R/$\overline{W}$ RR (high) signal, and the T30 signal from the timing line activating the $\overline{DRIVEMDS}$ signal.

If a refresh cycle to be performed, $\overline{MREF}$ is active (low) from the controller setting BMREF high. BMREF inhibits $\overline{DRIVEMDS}$ and forces GATE0 through GATE3 signals high to the $\overline{RAS}$ drivers. BMREF is inverted by gate U162 and and applied to the 4K IC's as an inactive $\overline{CS}$ (chip select) signal and inhibits the generation of the ALLOWCAS signal for 16K IC's. When the active CLOCK signal is ANDed with the GATE0: GATE3 signals (overriding the BDSELECT and Row Address Decoder outputs) all rows on all boards are selected. The refresh address from the controller is sent to the IC's. The inactive $\overline{WRITE}$ signal inhibits the Data In (pin 2) lines and refreshing is accomplished internally.

44. Memory Protect Violations.

The action taken by the memory system when a protected area of memory is addressed depends on several factors: whether the current cycle is a read or write cycle and whether the cycle is a normal CPU requested cycle or one initiated by the DCPC. In any case, when a memory protect violation occurs, the memory makes no direct attempt to inform the CPU of the violation. This is be done by the memory protect PCA.

45. DMS READ CYCLE.
When a memory protect violation occurs in a DMS read cycle, the cycle is completed normally except that the data is blocked at the S-bus gates. The S-bus goes high and appears as an all "1"s word on the S-bus. This occurs because the T-register output is blocked at the S-bus gates by the active (low) $\overline{METDIS}$ signal from the memory protect PCA. The parity circuits are disabled by this same signal through U67D to the Parity Error FF output gate U66D and the $\overline{PE}$ signal remains inactive.

45. DCPC READ OR WRITE CYCLE.
A DCPC read or write cycle is completed normally. The DCPC is allowed access to the protected area of memory.

47. NORMAL WRITE CYCLE.
If a protected area of memory is addressed for a normal write cycle, the cycle is not started because the Write FF will not be set by the $\overline{WRITE}$ signal from the CPU. With $\overline{DMAEN}$ inactive (hign) and $\overline{MPV}$ active (low) the output of U65D will produce a low level signal to the J input of the Write FF. Then, when the $\overline{WRITE}$ signal from the CPU clocks the flip-flop, it remains in the reset condition. Since the write cycle must be started by setting the Write FF, the write cycle does not begin. Note when the $\overline{DMAEN}$ (DCPC write) is active (low) it overrides the $\overline{MPV}$ signal holding the output of U65D hign allowing the write cycle to be performed.

48. Read Cycle

Information concerning events occurring in a read cycle are presented
in table 6.

Table 6. Read Cycle Events

CAUSE	EVENT
$\overline{READ}$ signal, from the CPU active (low)	The Read FF (U57B) is set.
Read FF set	a. The R/W Delay FF (U53B) is set, the MSRDY FF is reset, and the MSRDY signal, which has been active, becomes inactive (M-Series).
	b. The $\overline{MBUSY}$ signal which has been inactive, becomes active (E-Series).
	c. RFF output applied to T-register Control FF gate U55A.
R/W Delay FF set and PONFF signal from power supply active (high).	a. Delay line (U42) is pulsed and outputs pulses at fixed delay intervals.
	b. Clock FF is set for all cycles except an E-Series DMS read.
	c. Power Sense FF set, PONFF output gates $\overline{MBUSY}$ or MSRDY signal to CPU.
	d. $\overline{PULSE}$ signal disables input to the M-register, the address available at the input is stored and steadily applied to the memory PCA's.
Clock FF set.	a. The $\overline{CLK}$ signal to memory is active (low).
	b. The $\overline{ICLK}$ signal is active (low).
	c. The ICLK signal is active (high).
Memory address available to memory PCA's, $\overline{CLK}$ signal active, R/$\overline{W}$ RR signal inactive (high)	The memory supplies the data from the selected address to the T-reg. and the S-bus gates. However, the S-bus gates are not yet enabled to pass data to the S-bus.

Table 6. Read Cycle Events (continued)

CAUSE	EVENT
	NOTE
	Delay Mux (U62) A-input lines are selected and gated for an E-Series DMS read cycle. The B-input lines are selected and gated for all other cycles.
$\overline{50}$ pulse from delay line (U52-18)	Clock FF is set for an E-Series DMS read. (See Clock FF set.)
$\overline{75}$ pulse from delay line (U33-8)	Resets the R/W Delay FF, terminating the delay line input signal and producing a pulse approximately 90 nanoseconds wide in the delay line. $\overline{PULSE}$ signal becomes inactive, $\overline{ICLK}$ keeps the M-register inputs disabled.
$\overline{300}$ pulse from delay line (U52-16)	Sets the MSRDY FF and clocks the T-register Control FF.
Read FF set, Clock FF set (ICLK signal active), and the leading edge of the $\overline{300}$ pulse occurs.	T-register Control FF is reset (U53A).(This FF is active in the reset condition.)
T-register Control FF reset (active)	a. The B inputs are selected on the T-register and T-register MUX (U44). b. The T-register accepts the 16-bit data word from memory. c. The MUX supplies the parity bit (bit 16) from memory to the parity circuits through NAND gate U55D. d. The parity circuits compare the bit which they derive from the data in the T-register with the parity bit supplied by memory and prepare a signal ($\overline{PE}$) parity error. The $\overline{PE}$ signal is supplied to the CPU later in the cycle.
$\overline{375}$ pulse from delay line (U52-12).	a. Read FF is reset. $\overline{CLKCLR}$ ($\overline{375}$ to 425) signal continues to inhibit the M-register from accepting a new address. This pulse is selected for every read cycle except an E-Series DMS read.

Table 6. Read Cycle Events (continued)

CAUSE	EVENT
	b. At the end of the $\overline{\text{CLKCLR}}$ ($\overline{425}$) the M-register opens to accept any new address on the M-bus.
$\overline{400}$ pulse from delay line (U52-9).	When selected by the Delay Mux: a. Sets the T-register control FF causing the T-register to store data word from memory and supply it to the parity circuits and S-bus gates.
	b. The T-register Mux stores the parity bit (MDS16) from memory and supplies it to the parity circuits.
	c. the clock ff is reset. this de-activates the $\overline{\text{ICLK}}$ and ICLK signals and the $\overline{\text{CLK}}$ signal to memory, and the memory IC's stop supplying data to the T-register. However, the data is now stored in the T-register.
$\overline{425}$ pulse from delay line (U52-7).	The activities described for the $\overline{375}$ pulse now occur for an E-Series DMS read. This signal is one of two Parity Strobes selected by the Delay latches the data read from the memory module into the T-register as described for the $\overline{400}$ pulse.
	b. This pulse is used for all other read cycles by the Delay Mux at U62-6 to gate the parity error status through U54A to the Parity Error FF to indicate to the CPU whether or not a parity error exists in the data being transmitted to the CPU.
$\overline{\text{TEN}}$ signal from CPU becomes active (low) and $\overline{\text{READ}}$ signal from CPU is inactive (high). NOTE: This will occur for an E-series DMS read following the $\overline{475}$ pulse from the delay line.	The S-bus gates are enabled for transmission of data from the T-register to the CPU by gate 65A.
$\overline{450}$ pulse from delay line (U52-5).	During an E-Series DMS read the Delay Mux will select the $\overline{450}$ pulse to perform the activities described for $\overline{400}$ pulse.
$\overline{\text{TEN}}$ signal becomes inactive.	S-bus gates are disabled for transmission of data from the T-register to the S-bus.

Table 6. Read Cycle Events (continued)

CAUSE	EVENT
$\overline{475}$ pulse from delay line (U52-3).	Selected by the Delay Mux during an E-Series DMS read to strobe the the parity logic as described for the $\overline{425}$ pulse.

49. Write Cycle

Information concerning events occurring in a write cycle are presented in table 7.

Table 7. Write Cycle Events

CAUSE	EVENT
A CPU instruction places data on the S-bus and activates $\overline{TST}$ and $\overline{P4NF}$ signals (low).	a. $\overline{TST}$ is low at U65B pin 5, and pin 4 is low (R/W Delay FF reset). The low output enables the S-bus write gates to pass data to the T-register. b. The U65B output ANDed with P4NF selects the B inputs to the T-register Mux and the T-register sending the data to the parity generators and the A inputs of the T-register. c. The input to the Mux at pin 13 is forcing a one to the parity generator while the other 16 bits are used for parity generation.
$\overline{P4NF}$ inactive (high)	Selects the A inputs of the T-register, latching the S-bus data. This stores the S-bus data in the T-register.
$\overline{MPV}$ active $\overline{DMAEN}$ inactive.	The address supplied to memory is located in a protected area of memory and the cycle is not under control of the DCPC. The Write FF will not be set and the write cycle will be inhibited.
$\overline{DMAEN}$ active.	Write cycle is under control of DCPC, the write FF will be set and the write cycle will proceed.

Table 7. Write Cycle Events (continued)

CAUSE	EVENT
Write FF Set.	a. Activates the $\overline{\text{MBUSY}}$ signal to notify an E-Series CPU that memory is busy.
	b. Sets the R/W Delay FF.
	c. Activates the R/$\overline{\text{W}}$(RR) (low) signal to the memory PCA's, to activate the write logic and inhibit the read logic.
	d. Selects the B inputs to the Delay Multiplexer (U62).
	e. Enables the T-register Data Drivers (U84 and U104) and the parity bit gate (U66C).
	f. $\overline{\text{CS}}$ and R/$\overline{\text{W}}$(WR) (U93A and U103A) are activated but are not used with the memory PCA's discussed in this text.
R/W Delay FF set. PONFF output from Power Sense FF active (high).	a. The clock FF (U63D and U83C) is set through AND gate U72D and Delay Multiplexer U62.
	b. The Delay Line (U42) is pulsed and outputs pulses at fixed delay intervals.
	c. The MSRDY FF is reset notifying an M-Series CPU that memory is busy.
	d. The signal $\overline{\text{PULSE}}$ shuts off the input to the M-register. The address that has been supplied from the M-bus is now stored in the M-register and continuously supplied to memory.
Clock FF set.	a. $\overline{\text{CLK}}$ signal to all memory PCA's becomes active (low).
	b. $\overline{\text{ICLK}}$ signal is active (low). Will continue to hold M-register gates off after $\overline{\text{PULSE}}$ is reset. applied to Power Sense FF trailing edge will be used as a clock later in the cycle.
$\overline{75}$ pulse from delay line, active (low) (U33-8).	R/W Delay FF is reset ending the input pulse to the delay line.

Table 7. Write Cycle Events (continued)

CAUSE	EVENT
$\overline{300}$ pulse from delay line, (U52-16).	The MSRDY FF is set. Indicates to the CPU that memory is ready for another cycle.
$\overline{325}$ pulse from delay line, (U82-4).	ANDed with WFF at U92, deactivates $\overline{CLK}$ to memory. This stops memory from writing.
$\overline{375}$ pulse from delay line, (U52-12).	While the $\overline{375}$ pulse is present and and $\overline{425}$ is not present at the Delay Multiplexer (U62-3) a 50 nanosecond pulse is used as the $\overline{CLKCLR}$ signal to hold the M-register input gates closed and the T-register latched while the memory system logic is being reset.
$\overline{400}$ pulse from delay line, (U52-9).	Resets the Clock FF.
$\overline{425}$ pulse from delay line, (52-7).	a. Terminates the $\overline{CLKCLR}$ pulse. This allows the M-register to accept any new address from the M-bus. U54-12 becoming high will also allow the S-bus write gates and the T-register B inputs to be enabled with the TST and the $\overline{P4NF}$ signals of a new write cycle. b. While the $\overline{425}$ pulse is present and $\overline{475}$ is not present at U72A a 50-ns clear pulse is applied to the Write FF, The FF is reset and cannot be set until the pulse is terminated. The T-register data drivers are disabled, $\overline{MBUSY}$ becomes inactive to notify an E-Series CPU that memory is ready for another cycle. The R/$\overline{W}$(RR) becomes positive to the memory PCA's.
$\overline{475}$ pulse from delay line	Terminates the CLR pulse to the Write FF, allowing another write cycle to begin.

50. Refresh Cycle.

Events occurring during a refresh cycle are described in table 8.

Table 8. Refresh Cycle Events

CAUSE	EVENT
Refresh Oscillator output low at U61-9.	Sets Refresh Sync FF (U71A and B), this enables the B output of Refresh Sync Decoder (81-9).
Occurrence of $\overline{P5NF}$ of the next T4 time period after Refresh Sync Decoder B output enabled.	Sets Refresh Pending FF (U71C and D).
Refresh Pending FF Set.	a. Resets Refresh Sync FF.
	b. Enables the A output of the Refresh Sync Decoder. The time of the output signal will be controlled by the status of the $\overline{DMAREAD}$ signal.
	c. $\overline{REFRESH}$ signal to CPU becomes active (low). This signal will allow a read or write cycle that is in progress to be completed. However it will inhibit a read or write cycle from starting.
$\overline{DMAREAD}$ inactive next T6 time period occurs.	Refresh decoder output (U87-7) A output becomes high.
$\overline{P5NF}$ of T6 becomes active.	A output gated through U101B sets the Refresh Start FF (U102) and the Refresh Cycle FF (U83B and U101D).
NOTE: With $\overline{DMAREAD}$ active the same events occur at the end of T3 instead of the end of T6. The normal refresh cycle is performed during time periods T2 and T3. When memory is under control of DCPC ($\overline{DMAREAD}$ active) the read cycle is performed during time periods T2 and T3 and the refresh cycle is moved to periods T4 and T5.	
Refresh Start FF set.	a. Resets the Refresh Pending FF disabling the A output of the Sync Decoder and deactivates the $\overline{REFRESH}$ signal to the CPU.
	b. Gated with the active PONFF signal through U92 to set the Refresh Delay FF (U23A and B) and to ensure that the Parity Error FF (U32a and B) is reset disabling the $\overline{PE}$ signal to the CPU.

Table 8. Refresh Cycle Events (continued)

CAUSE	EVENT
Refresh Cycle FF set and Refresh Delay FF set.	a. The Refresh Cycle FF activates the $\overline{MREF}$ signal to the Memory PCA's and $\overline{IREF}$ and IREF (internal refresh) for use on the controller. The M-register Address Driver (U35) is disabled and the row address to be refreshed is supplied by the Refresh Address Counter and Driver (U24 and U25). $\overline{MBUSY}$ becomes active to the CPU. b. The Refresh Delay FF pulses the delay line, activates the $\overline{PULSE}$ signal to the M-register, sets the MSRDY FF, and sets the Clock FF. Setting the Clock FF activates $\overline{CLK}$, $\overline{ICLK}$, and ICLK. The selected row of memory addresses is refreshed from this time until the Clock FF is reset later in the cycle.
$\overline{75}$ pulse from delay line.	Refresh Delay FF reset, ending input to delay line.
$\overline{300}$ pulse from delay line.	MSRDY FF reset, informs an M-Series Cpu that memory is ready for another cycle.
$\overline{325}$ pulse from delay line.	$\overline{325}$ gated with IREF (U92B) disables the active $\overline{CLK}$ signal to memory. This ends refreshing of the selected row of memory addresses.
$\overline{375}$ pulse from delay line.	Activates the $\overline{CLKCLR}$ signal which will keep the M-register disabled after the Clock FF is reset.
$\overline{400}$ pulse from delay line.	Resets the Clock FF. The Row Address counter is stepped one increment to to select the next sequential row of memory addresses to be refreshed during the next refresh cycle.
$\overline{425}$ pulse from delay line.	a. Deactivates the $\overline{CLKCLR}$ pulse, The M-register enabled to receive an address. b. Refresh FF reset, all logic reset to start a new cycle. $\overline{MBUSY}$ signal becomes inactive, notifies an E-Series CPU that memory is ready for a new cycle.

E-SERIES

	175	175	175	NOTE 1			
	T6	T2	T3	T4	T5	T6	

READ

TEN

MBUSY ←————375————→ 50*

*ADDITIONAL TIME
E-SERIES DMS READ

P				TAB		
PNM				SI		
INC		NOP	NOP	PASS		
READ						

READ SIGNALS

WRITE

TST

MBUSY ←————425————→

S3	S1				
M	TAB				
	PASS	NOP	NOP		
	WRITE				

WRITE SIGNALS
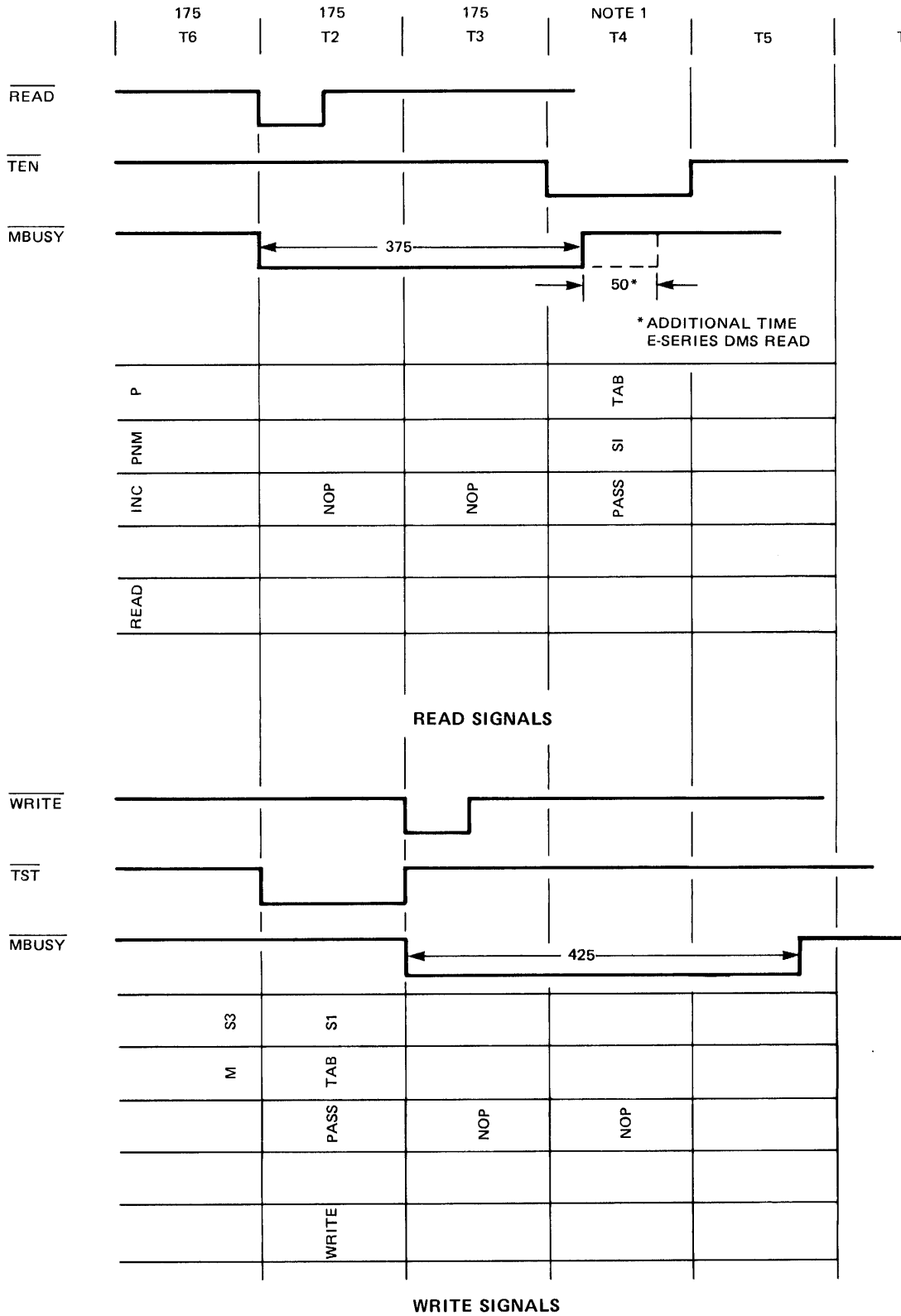
NOTE: FOR THE READ CASE, THE LENGTH OF THIS T-PERIOD WILL BE
THE MEMORY CYCLE TIME (DEPENDENT ON MEMORY TYPE)
MINUS 350ns. FOR THE WRITE CASE THE T-PERIOD WILL BE 175ns.
ALL ITEMS REPRESENTED IN NANOSECONDS

7700-129

M-SERIES
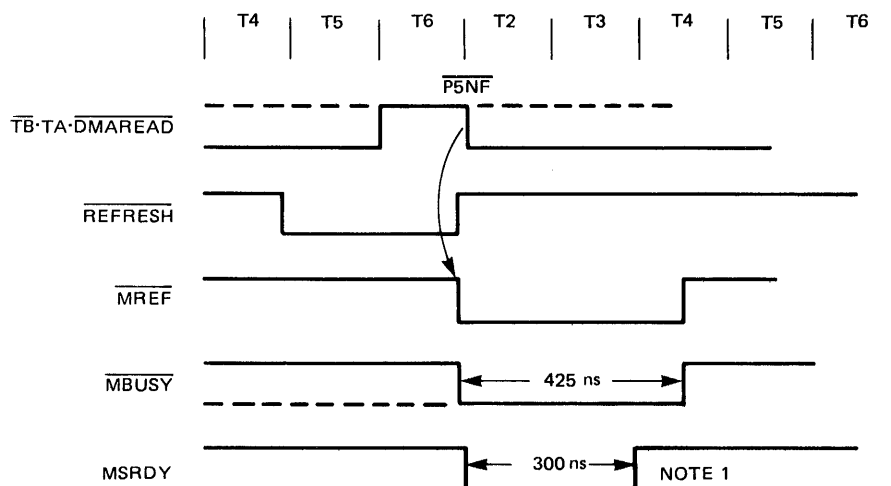
325 T6	325 T2	325 T3	325 T4	325 T5	325 T6

READ ‾‾‾‾ ← 108 →

TEN ‾‾‾‾

MSRDY ← 300 →

SI		TAB			
M		S2			
PASS	NOP	PASS			
READ					

READ SIGNALS

WRITE ‾‾‾‾ → 108 ←

TST ‾‾‾‾

MSRDY ← 300 →

	S1				
	TAB				
	PASS	NOP	NOP		
	WRITE				

WRITE SIGNALS

NOTE: ALL ITEMS REPRESENTED IN NANOSECONDS

NOTE 1:   MSRDY SIGNAL IS FOR M-SERIES COMPUTER ONLY.
NOTE 2:   MBUSY SIGNAL IS FOR E-SERIES COMPUTER ONLY.

7700-131

NORMAL MEMORY REFRESH
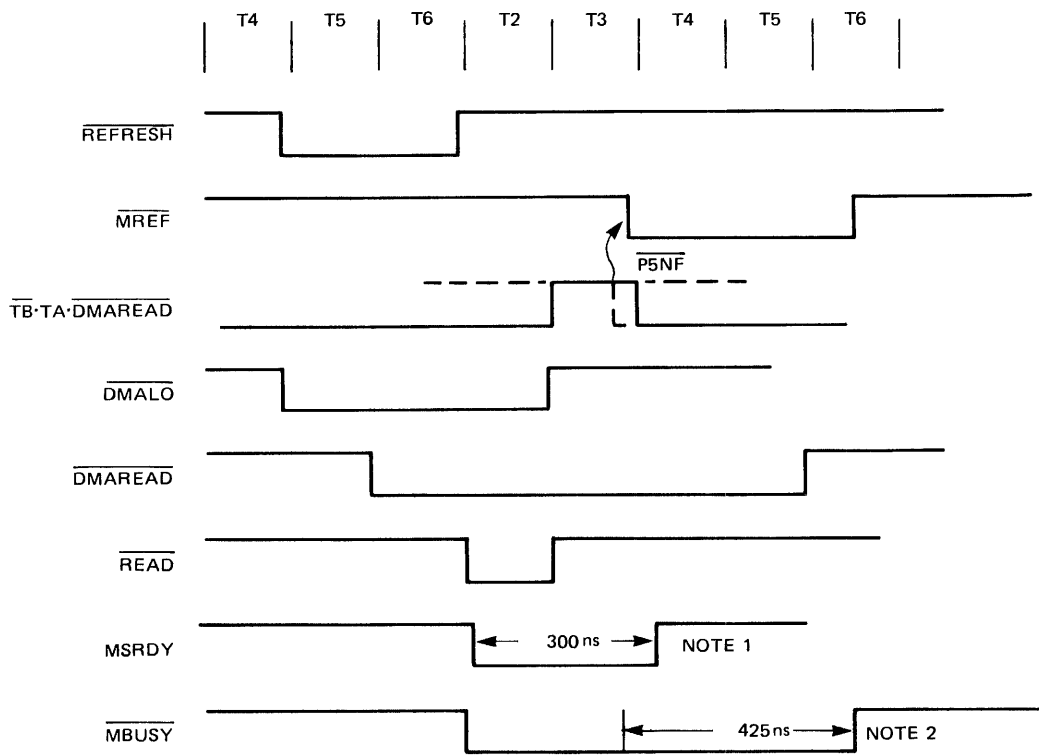
MEMORY REFRESH DURING DCPC OUTPUT (DMAREAD) TRANSFERS
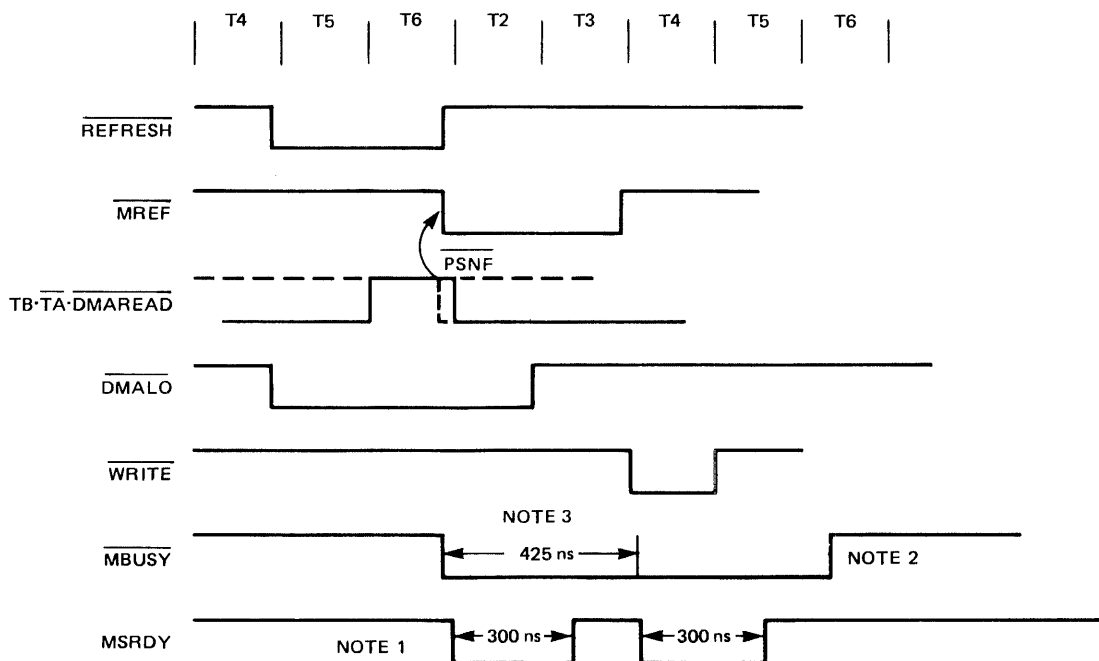
NOTE 1: MSRDY SIGNAL IS FOR M-SERIES COMPUTER ONLY.
NOTE 2: MBUSY SIGNAL IS FOR E-SERIES COMPUTER ONLY.
NOTE 3: MBUSY REMAINS DUE TO REFRESH CYCLE START.

MEMORY REFRESH DURING DCPC INPUT TRANSFERS
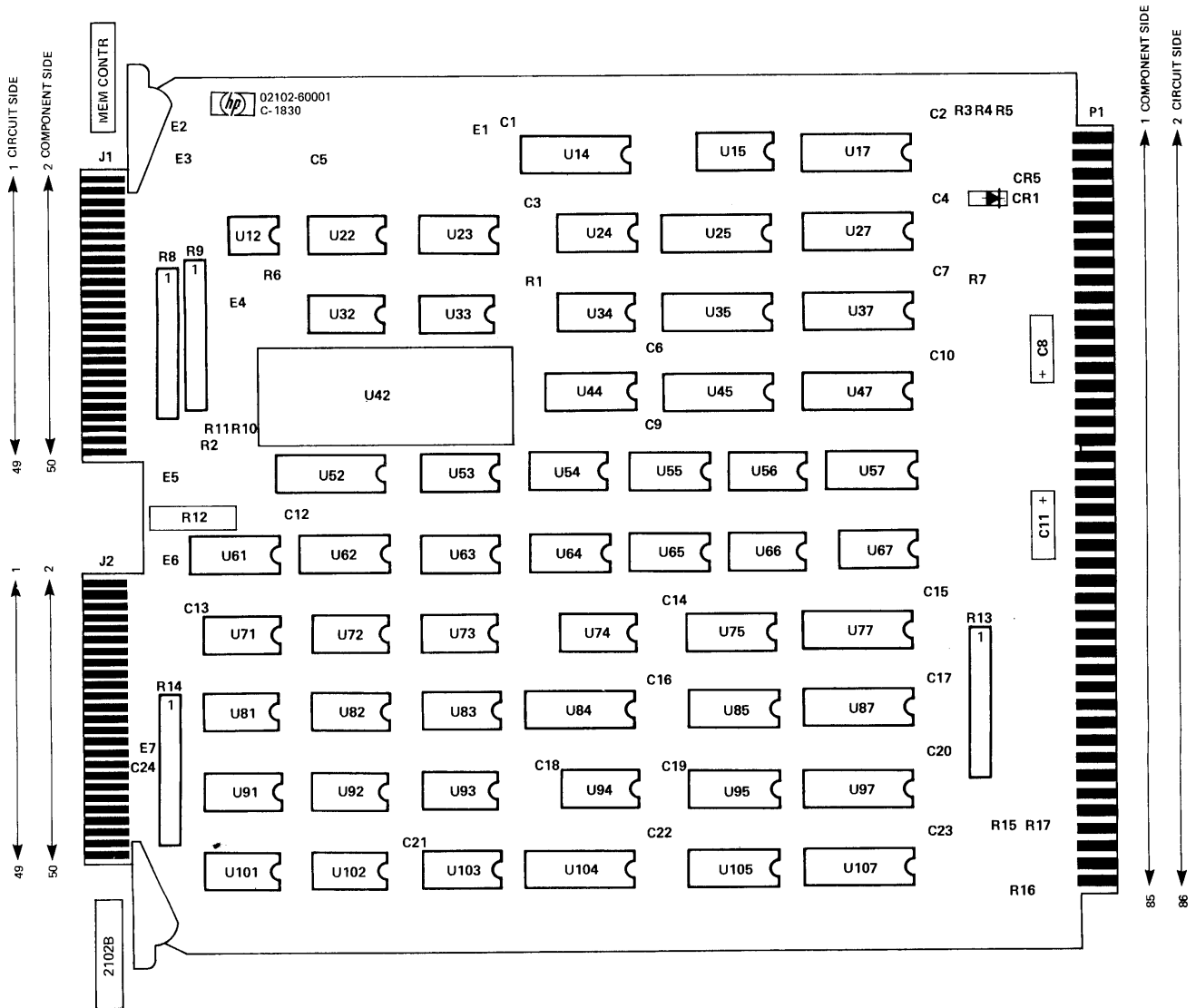
7700-132

2102B Standard Performance Memory Assembly
02102-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01 03	C1-4,6,7,9,10,15-17 20,22,23	CAP 0.1UF		0150-0121		U	14
01	C5,13,14,18,19,21	CAP .01UF		0160-2055		U	6
00	C12	CAP 820PF 5%		0160-3539		U	1
01	C25	CAPACITOR-FIXED		0160-5107		U	1
01	C24	CAP 20UF -10+75%		0180-0049		U	1
00	C8,11	CAP 15UF 10%		0180-1746		U	2
		TERM-STUD SGL		0360-1682		U	7
00	R1	RES 100 5% .25		0683-1015		U	1
01	R15,16	RES 330 5% .25		0683-3315		U	2
01	R3,4,7	RES 470 5% .25		0683-4715		D	3
00	R2,5	RES 4700 5% .25		0683-4725		U	2
03	R18	RES 47K 5% .25		0683-4735		U	1
00	R6	RES 100 5% .5		0686-1015		U	1
00	R17	RES 2.87K 1%.125		0698-3151		U	1
01	R11	RES 42.2K 1%.125		0698-3450		U	1
00	R10	RES 20K 5%.125		0698-4285		U	1
		SOCKET 8 DIP LU		1200-0455		U	1

ITEM NO	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
00	W1,3	JMPR PLUG .3"C-C		1258-0124		U	2
		PIN GRV .062X.25		1480-0116		U	2
00	U42	DELAY LINE		1810-0064		U	1
00	R8,9	NTWK RES 9X500		1810-0274		U	2
01	R13,14	NTWK RES 9X4.7K		1810-0279		U	2
00	U57	IC SN74S112N		1820-0629		U	1
01	U23,55,63,72,101	IC SN74S00N		1820-0681		U	5
01	U22,67,82	IC SN74S04N		1820-0683		U	3
01	U32,83	IC SN74S10N		1820-0685		U	2
00	U54	IC SN74S11N		1820-0686		U	1
01	U73,93,103	IC SN74S40N		1820-0690		U	3
01	U53,102	IC SN74S74N		1820-0693		U	2
00	U61	IC U7896L0259X		1820-0730		U	1
01	U44,62,75,85,95,105	IC SN74S157N		1820-1077		U	6
01	U64,92	IC SN74S51N		1820-1158		U	2
01	U71	IC SN74LS00N		1820-1197		U	1
00	U81	IC SN74LS153N		1820-1244		U	1
00	U56	IC SN74S132N		1820-1307		U	1
		IC SN74S08N		1820-1367		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	U15,34			1820-1367			
01	U33,91,13	IC SN74LS14N		1820-1416		U	3
00	U65	IC SN74S32N		1820-1449		U	1
00	U66	IC SN74S38N		1820-1451		U	1
00	U24	IC SN74393 N		1820-1464		U	1
01 03	U14,25,35,37,84,87, 104,107	IC SN74S241N		1820-1624		U	8
01	U52,77,97	IC SN74S240N		1820-1633		U	3
01	U74,94	IC SN74S280N		1820-1638		U	2
01	U17,27,45,47	IC SN74S373N		1820-1676		U	4
00	CR1,2	DIODE 1N5817		1901-1080		D	2
00	R12	RES 50K POT		2100-3054		U	1
		LABEL-USA		7120-6830		L	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
		BOARD-ETCHED		02102-80001		W	1

2102 B MEMORY CONTROLLER

TITLE: 2102 B

NEXT ASSEMBLY

PART NUMBER: -02102-60001

HEWLETT PACKARD

D-02102-60001-51

2102B MEMORY CONTROLLER

HEWLETT PACKARD

IIB -43/-44

HP 2102C
FAULT CONTROL
MEMORY CONTROLLER

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and F-Series Computers Engineering and Reference Documentation and is not available separately.

PREFACE

INTRODUCTION

This document provides Theory of Operation for the Fault Control Memory
Controller HP 2102C. The controller operates in conjunction with the
HP 12779A, HP 12780A Check Bit Arrays, and the standard performance
memory array modules. The associated schematics are located in this
section under the sub-headings MEMORY ARRAY MODULES and MEMORY CHECK
BIT ARRAYS. Brief descriptions of the ECC code and error detection
display are contained in Appendix A.

GENERAL

The ECC controller (2102C) is compatible with the 21MX-M and 21MX-E computers,
8K, 16K and 64K array boards, memory expansion (MEM), DMA, and memory protect
features. The controller detects single, double, and some triple errors, and
corrects all single errors. Refresh control is also provided.

Data is encoded in the array boards as a 22-bit distance-4 "Hamming plus parity bit"
code. This is a seperable code, consisting of 16 bits of data, 5 check bits
corresponding to Hamming code check bits for a distance-3 code, and an overall
parity bit (over all 22 bits) to provide a distance-4 code.

Four jumpers on the controller board allow selection of 1) even/odd overall
parity bit (for testing purposes), 2) MXE/not MXE CPU selection, 3) stop/
don't stop on single-bit errors , 4) MEM installed/not installed.

Error correction is performed on a read-thru basis only, i.e., corrected data is
not written back to the arrays. Double and triple errors (single errors also if
jumper set) force a "Parity Error" indication to the CPU.

ADDRESS PATH

The MB and MEB buses are received into three 74S241 buffers, four 74S00, and
two 74S04 gates. If MEM is not present or not active, MEBEN- will be high,
BMEBEN+ low. Thus when the controller is asserting ENABMBRCVR-, MB0+ through MB13+
will be buffered through the S241's onto A0+ through A13+ (the array board's
address bus).

A14+ and A15+ will be generated by section two of a 74S241 because of HIMBORD+
being active, HIMBMEB- being inactive. Since BMEBEN+ is low, GMEB16- through
GMEB19- will be high, forcing A16+ through A19+ to be low. Thus A0+ through
A14+ copy MB0+ through MB14+, while a A15+ through A19+ are low, producing
the desired 32K address space.

If MEM is present and active, BMEBEN- will be low, BMEBEN+ high, begetting HIMBMEB+
high, and HIMBORD+, HIMBMEB- low. This will cause MB0+ through MB9+ to be

buffered onto AØ+ through A9+ as before (if ENABMBRCVR- is active), while MEB1Ø+ through MEB15+ are gated to A1Ø+ through A15+. Since BMEBEN+ is high, MEB16+ through MEB19+ are gated onto A16+ through A19+, producing a one-megaword address space.

Note that the controller idles with ENABMBRCVR- active, so that the address for a read/write operation is set up quickly on the A-Bus through capacitive drivers (S24Ø & S241's) as soon as possible. Also, during idle times, LATCHMB+ is high and ENABMBLATCHLO- is high, allowing the A-Bus to be transferred to the MB-register (three 74S373 latches) but not read out. During a read or write operation, LATCHMB+ is dropped along with ENABMBLATCHLO-, latching the A-Bus and holding it stable by enabling the outputs of the MB-register. LATCHMB+ disables ENABMBRCVR- so that changes in the MB-Bus due to noise on the SBUS will not drive the A-Bus, overriding the MB-register.

During refresh, ENABMBRCVR- is high, causing A7+ through A19+ to be arbitrary (since the MB-bus is not defined during refresh) while AØ+ through A6+ are driven not by the S373 (SH2,D6), but by the 74S24Ø at E9 (REF-active). Thus the refresh row counter drives the refresh address onto the A-bus. The counter is incremented for the next refresh cycle at the end of the current refresh cycle (REF+ going low).

READ-DATA PATH

The CPU/array card's data buses (SBUS/MDSBUS respectively) require that the following hold true;
1) SBUS --→ MDS BUS (WRITE) no inversion
2) MDSBUS --→ SBUS (READ) inversion

For read operations, the automatic inversion takes place at the "DATA CORRECTION" XOR gates (SH1,A9→E9) since the other input of these gates is normally high. During a read cycle, LOADRTREG+ is high, gating the check-bits MDS16+ through CMDS2Ø+ to a set of five 93S48 parity generators, along with the data-bits MDSØ+ through MDS15+. The odd parity outputs will all be low if no errors have occured. Four 74S138 decoders perform a 5-line to 32-line decode of these outputs without the need for additional decoding circuitry due to the availability of the even parity outputs and active high and low enable inputs on the 74S138's. From coding

theory, it is easy to show that sixteen of the decoder outputs (all of which
are active low) correspond to errors in the data bits, five to errors in the
five Hamming code checkbits (MDS16+ to CMDS2Ø+), one to "NO-ERROR" (P16P2ØOK-),
and the remaining ten outputs to errors in ten data bit positions which in
this machine do not physically exist. If a decoder output corresponding to
one of these positions activates, a triple (or greater) error has occured.
This will activate ECCHALT+, halting the CPU at the end of the cycle by forcing
PE- low. P16P2ØOK- is used by the controller also in determining double errors,
in conjunction with the parity bit P21 (stored in the check-bits boards in
the CMDS21+position). If an ordinary single error occurs in the check-bits,
the P-ERROR register (SH1,J6) will latch the syndrome. During diagnostics
the "single error stop" jumper is removed, a standard memory diagnostic run
(which tests only for failing data-bit chips), then, a six -LED display informs
the user of the syndrome and thus the failing data or check bit position (refer
to HP 2102C Fault Control Memory Controller Installation and Service Manual,
part no. 02102-90011 for display interpretation).

Single errors in the data-bit positions are corrected by inverting the erroneous
bit in the XOR gates. This will be effected by the appropriate decoder output
being low. The "single error stop" jumper defeats correction to allow diagnostics
to read the erroneous data.

The controller will open and drop LOADRTREG+ at the appropriate times to latch
read data. Corrected or unchanged data passes from the invert gates to two octal
74S241 buffers. The CPU may read the T-register during the cycle or in later
T-periods by issuing TEN-. MEM must have METDIS- inactive (implying no read
protect violation) at this time in order for the T-register contents to be dumped
onto the S-bus. Also at this time, the parity error latch will be enabled onto
the PE- line, halting (or interrupting) the CPU if a "Stop-Type" error occurred
in the corresponding read cycle.

During refresh, the T-register remains unchanged and the parity error F/F
is not strobed.

The overall parity bit is checked by one additional parity generator (SH1,G6),
plus two XOR gates, to signal an overall parity error (P21OK- high).

WRITE-DATA PATH

Write data from the CPU is presented on the S-bus to two octal 74S373 latches
which form the T-register for write cycles. The CPU loads the register by
issuing TST- and P4NF- prior to the WRITE- command signal. Data falls
through the latches onto the MDS-BUS through two 74S241 buffers. Since TSTRCVD+
is high, the sense of the even and odd parity outputs for the check-bit
checkers is reversed. MDS-BUS data parity is formed for each check-bit and
buffered onto the CMDS-BUS through a 74S240 octal driver (SH1,F2). Also,
the overall parity bit P21GEN+ is generated using a 93S48.
This parity bit is buffered onto CMDS21+ and will be stored in the check-bits
boards.

IDLE CONDITIONS

When the ECC controller is not performing a read, write, or refresh cycle, the
idle state of the controller is as follows:

READFF+	low
WRITEFF+	low
TSTRCVD+	low or high
PWRON+	HI (+5 ACTIVE), LOW (+5 DOWN)
PERROR+	low
ALLOWIN+	high
MBUSY+	low
LOADRTREG+	low
CLOCKSTP-	high
REFOPSTART-	high
REFPREP+	low
REFWARN-	high
REF+	low

ALL DELAY TAPS (T100+ --→ T475+) low

If power is on (PWRON+ HIGH), then OSC+ may be high or low, but if power is
off (PWRON+ LOW), then the controller is "idle" only when OSC+ is HIGH.

READ CYCLE CONTROL (POWER ON)
The CPU initiates a read cycle by issuing READ- to the controller. If this
is an MEM read (MEM jumper out), the clock to the array boards must be delayed
until the address bus stabalizes (requiring a 5Ø nsec delay from READ-↓ to
CLK-↓). An MEM read will activate DELREAD+ (SH3,C3), which generates DELREADSTART-.

A non-MEM read will set the READFF+ flop, due to READOK+ being high when READ -
goes low. DELREADSTART- also sets the READFF+ flop for MEM read cycles. In
either case, READFF- going low or DELREADSTART- going low will beget IOINPROG+
high. IOINPROG+ high activates CLK- low (starting the read cycle in the
appropriate array card), and thereby activates HITIT+, firing the main timing
line (SH3,C9). IOINPROG+ also generates LATCHMB+ low and ENABMBLATCHLO- low,
latching the A-BUS contents and holding the A-BUS by enabling the MB- register
outputs. In parallel with the above operations, BREAD+ going high will
activate RDBUSY-(SH3,D6), setting the MBUSY+ flop to inform the CPU that the
memory system is busy. BREAD+ also clears the TSTRCVD+ flop (SH3,E3),
enabling the internal data bus elements such that read-data may pass from the
MDS-BUS to the S-BUS.

About 1ØØ nsec after CLK- goes low, the T1ØØ+ timing line tap will go
high, setting the LOADRTREG+ flop, setting "MEMORY SOON READY" to an MX-CPU
(setting MBUSY- high).

As T2ØØ+ goes high (2ØØ nsec after CLK-↓) the ALLOWIN+ flop is cleared,
terminating the input signal to the delay line. Thus the delay line contains
a 2ØØ nsec long pulse.

At T39∅+ time, the LOADRTREG+ flop is cleared, thereby latching read data (SH2,F8). As T39∅+ goes high, the CLOCKSTP- flop is cleared. This asserts CLOCKSTP-, forcing CLK- to go high. MDS-BUS data remains valid for only 6 nsec after CLK- goes high, thus LOADTREG+ must go low before CLK- goes high. This is assured because CLOCKSTP- and LOADRTREG+ are on the same chip.

At T42∅+ time, SETMREADY- will be generated if MXE+ is high (SH3,A6). SETMREADY- low resets the MBUSY+ flop, indicating to the CPU that the cycle is complete and that read-data will be stable on the S-BUS in no more than 55 nsec.

At T475+ time the PERROR+ flop is clocked with the results of the error detection logic. If an error has occured which is supposed to halt the CPU, ECCHALT+ will be high. This will be the case whenever a triple error occurs, or when the following conditions exist:

P16P2∅0K-	P210K-	SINGSTP+	ECCHALT+ACTIVE?
LO	LO	LO	NO, NO ERROR
LO	HI	LO	NO, P22 BAD, SINGLE ERROR
HI	LO	LO	YES, DOUBLE ERROR
HI	LO	HI	NO, DOUBLE ERROR
HI	HI	LO	NO, SINGLE ERROR
HI	HI	HI	YES, SINGLE ERROR

Also at T475+ time, LASTTHING- will activate (SH3,G9), clearing the READFF+ flop and terminating the cycle. READFF- going high brings IOINPROG+ low, setting the ALLOWIN+ flop, preparing it for the next cycle. ALLOWIN- low sets the CLOCKSTP- flop. The controller should now be in the "IDLE" state.

WRITE CYCLE CONTROL (POWER ON)
The CPU initiates a write cycle by issuing WRITE- to the controller. If MPV- is inactive or if DMAEN- is active then ALLOWWRITE- will be low, allowing the write cycle to proceed if a TST- has previously been received. Normally, TST- will activate, along with a P4NF-, in the T-period prior to WRITE-. This would activate TSTP4+ and TSTP4-, setting the TSTRCVD+ flop. This flop

enables R/W̄ (RR)+ to go low, enabling the array boards for a write operation.
Issuence of WRITE- without a prior TST- sometimes occurs due to the CPU
storing into the A and B registers. In this case, the write to memory is
inhibited. The TSTRCVD+ flop is reset by the occurance of a read operation.

Assuming that TSTRCVD- is active, WRITEOK+ will be high, allowing WRITE- to
clock the WRITEFF+ flop. (No delay is required for MEM-WRITES).

WRITEFF- going low will generate IOINPROG+ high, starting the same chain of
events that occured in the read cycle previously described.

The LOADRTREG+ and PERROR+ flops will not be set due to READFF+ and WRITEFF- being
low, respectively. Termination of the write cycle by LASTTHING- going low
is identical to the termination of a read cycle.

REFRESH CYCLE CONTROL (POWER ON)
A 555 timer, connected as an astable, functions as a free-running refresh
oscillator. Every 15 μsec. the OSC+ signal goes high, causing GOSC- to clear
the REFWARN- flop. This enables a strobe input of a 74LS153 multiplexor
(SH3,H3), so that at the next T3-period (TA+ high, TB+ low, and TC+ low) the
NOTTC+ signal will be selected. This will generate REFWARNTIME+, which is then
sampled with BP4NF+ to assert RWARNT-, setting the REFREP+ flop (SH3,H8).
This forces REFRESH- to be issued to the CPU, warning it of an impending
refresh cycle and resetting the REFWARN- flop. An ordinary read or write
cycle may be starting at the next T-period, making it necessary to warn
the CPU two T-periods ahead of the actual refresh cycle.

If DMA is active (DMAREAD- low), the multiplexor will elect to start the
refresh cycle at the next T4-period (TA+ high, TB+ low) otherwise, (with
DMAREAD- high) the multiplexor selects T2 as the start of the refresh cycle.
In either case, the signal REFTIME+ will go high for the T-period preceeding
the above mentioned T-periods. REFTIME+ is then sampled by the trailing edge
of P5NF- at the end of the T-period preceeding the T-period in which the
refresh cycle will start. P4NF- of that T-period has already caused SETR1-
and SETREF- to go low, setting the REF+ flop. REF+ high will assert MREF- to
the array boards, allowing the row selects to be enabled. Also, REF+ will
disable the low-order MB-register outputs by bringing ENABMBLATCHLO- high.

At the same time the refresh counter buffers will be enabled by REF- low. The result is that the low-order address bits will contain the value of the refresh counter, while the high-order address bits will be arbitrary (MB-BUS undefined). Since TSTANDNOTREF+ is low, R/$\overline{W}$ (RR)+ will be high. The state of the controller is thus prepared for refresh.

As P5NF- deactivates, SAMPLERT+ goes high, sampling the DOREF+ signal and setting the REFOPSTART- flop. REFOPSTART- low sets the WRITEFF+ flop, starting the refresh cycle and resetting REFPREP+.

From this point on, the events that took place in a write cycle will be the events that take place in the refresh cycle. Exceptions are:

1. When ALLOWIN+ goes low (at T2ØØ+ time), the REFOPSTART- flop is reset, allowing the WRITEFF+ flop to be reset at the end of the cycle.
2. When the cycle ends (LASTTHING- going low), the transistion of WRITEFF- from low to high resets the REF+ flop.
3. R/$\overline{W}$ (RR)+ is held high (READ mode).

POWER OFF AND POWER ON CONDITIONS

During POWER-FAIL and POWER-UP times the PON+ signal will be low, while +5M will be stable. This condition allows the controller to power down unnecessary logic (powered by +5), while at the same time performing refresh cycles, as needed, to retain memory contents. Since many signals will be floating during these periods it is necessary to lock-out spurious CPU "signals" due to noise, etc. The PWRON+ flop accomplishes these functions.

The sense of PON+ is sampled by the controller at the end of every refresh cycle by the low to high transistion of REF-. Since the refresh cycle was started by the low to high transistion of GOSC-, and since the duty cycle of the refresh oscillator is approximately 30%, it is obvious that PWRON+ will change only when GOSC- is high (GOSC + low). The importantce of this condition will be seen later.

All signals to the array boards are controlled by powered logic which is activated directly or indirectly from the READFF+/WRITEFF+ flops, hence CPU signals will not affect the refresh cycles in any way. Should power be restored, the PWRON+ flop will change sense at the end of a refresh cycle, insuring that no array board signals will "jitter" due to PWRON+ activating in the middle of a cycle.

To initiate a power-off refresh cycle, the controller will, at some time, receive a high to low transition on OSC+, forcing REFONLYPWROFF- to go low, setting the REF+ flop. Activity on signals SAMPRT-, SETR1-, and RWARNT- is inhibited by PWRON+ being low. The setting of REF+ causes the MB-register output controls and the refresh counter buffers to activate in the usual manner (see Refresh Cycle Control). Since PWRON- is high, DOREF+ will be high. The falling edge of OSC+ will cause REFONLYPWROFF- to go high, activating SAMPLERT+, forcing the REFOPSTART- flop to be set (because DOREF+ is high).

REFOPSTART- going low triggers the same events described under refresh cycle control. Note that at the end of each refresh cycle, should PWRON+ go high, the state of OSC+ is still guaranteed to be high, avoiding the possibility of double-triggering the refresh cycle flops.

Substantial power is saved in the controller by powering down the data paths and much of the address and control logic. Due to the performance required by the controller, however, substantial +5M power is still used for the Schottky control logic.

POWER-UP (INITIALIZATION)
When power is first turned on, the controller will require at least one refresh cycle after PON+ goes high to sense PON+ (setting PWRON+). Since the CPU will try to start cycles in a shorter interval, the controller holds off the CPU by forcing MBUSY- low to the CPU whenever PWRON- is high and PON+ has come up. This allows proper power-up in the controller without ignoring CPU cycle requests. Since no "reset" signal is available from the CPU, it is necessary to initialize the controller at power-up time to it's "idle condition" described earlier in a "round-about" manner. To see how reset is accomplished, the following flow table is presented:

```
┌─────────────────────────────────────────────┐
│ START                                         │
│ All flops and logic powered by +5M            │
│ arbitrary, +5 down, +5M up, PON+ low,         │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ PWRON+ flop reset by +5 being down            │
│ (FIVEDN- LOW)                                 │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ OSC+ goes low  at some time, PWRON- is        │
│ high, therefore REFONLYPWROFF- goes low.      │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ LASTTHING- goes low, REF+ is set high,        │
│ DOREF+ high, REFPREP+ low.                    │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ LASTTHING- going low forces READFF-  and      │
│ WRITEFF-  to go high, forcing IOINPROG+       │
│ low, forcing ALLOWIN+ high, ALLOWIN- low,     │
│ (forcing HITIT+ low), setting CLOCKSTP-       │
│ high.  Stay here for  5 µsec (→ delay line    │
│ settles).                                     │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ OSC+ goes high, REFONLYPWROFF- goes high,     │
│ setting REFOPSTART- low (since DOREF+ is      │
│ high), setting WRITEFF- low.                  │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ Refresh cycle starts as usual, T39∅+ initializes│
│ LOADRTREG+, WRITEFF- resets PERROR+.          │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ State of controller determined, cycle         │
│ terminates in usual manner. MBUSY+ reset.     │
└─────────────────────────────────────────────┘
                        ↓
┌─────────────────────────────────────────────┐
│ TSTRCVD+ flop initialized by first read or    │
│ write cycle from the CPU.  PWRON+ is          │
│  initialized by PON+.                         │
└─────────────────────────────────────────────┘
```

APPENDIX A

ERROR CORRECTION AND DETECTION

The ECC option is a 22-bit, distance four code, which is physically a 21-bit
hamming code (16 data bits, 5 check bits) plus an overall (even) parity bit.
Under jumper selection, the following protocols may be chosen:

JUMPER "IN"

Corrects single-bit errors; issues a "Parity Error" to the
CPU if a double (or greater) bit error occurs.

JUMPER "OUT"

Issues a "Parity Error" to the CPU if single bit errors
occur.

"IN" is the normal operating position, however "OUT" is required for periodic
maintenance, and is desirable also for extremely fault-secure applications
programming. All hard and soft failures of up to two bits within a word are
detected, including single and double cell and chip failures. Up to ~5%
(best case) of the array rams may fail without degrading the CPU or halting.
Many multiple (3 or more) faults are also detected.

ECC CODE

This particular hamming code has been chosen to minimize parity generator
fan-in, so that the utmost in speed of code generation and correction may be
attained. Numbering the data bits as 0 through 15 in the usual way, the six
check bits are as follows:

$$P20 = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_8$$

$$P19 = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12}$$

$$P18 = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{13} \oplus D_{14}$$

$$P17 = D_0 \oplus D_2 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15}$$

$$P16 = D_0 \oplus D_3 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$$

$$P21 = D_4 \oplus D_8 \oplus D_{11} \oplus D_{14} \oplus D_{15} \qquad \text{NOTE: } \oplus = \text{"EXCLUSIVE OR"}$$

In this code, P16 through P20 may be generated and checked via single
9-input parity generators. P21 is the overall parity bit, and requires
only a 5-input parity generator to form. If each data bit is included
an even number of times in the check equations P16 through P20, the parity
of the data bits plus P16 through P20 would be even. Therefore if P21
is the even parity of those data bits which are included an even number of
times, the parity of D0 through D15 plus P16 through P21 must be even.
Thus for code generation, P21 may be quickly formed. For checking operations,
a 22-bit parity check must be generated or else single-bit errors would
sometimes be decoded as double-bit errors.

ECC STORAGE
The data bits are stored in the normal way in the 8K or 16K array boards,
while P16 is stored in the array boards in the location formerly occupied
by the ordinary parity bit. The P17 through P21 check bits of up to 256K
words of data are condensed onto a single check-bit board. Hence a 256K ECC
memory system would consist of an ECC controller board, 16 16K array boards
(or 32 8K array boards), and one 256K x 5 bit check bits board. Thus a check
bit board must be included for each 256K words of main memory, assuming 16K
rams for the check bits array.

SYNDROME LATCH

A six-bit register latches the error detection logic's syndrome
and displays the result in six LEDS mounted on the board. The
latch is tested (as well as the LEDs) by bringing CLRPERR- low on
J2. This lights all six LEDS. The detection logic clocks the latch
whenever a "Parity Error" signal is sent to the CPU. Thus an
error in a word that is fetched, for example, as the first word
in a multiple-fetch instruction will be held in the latch. The
64 possible syndromes and their meanings are interpreted by first
reading the yellow LEDS, from left to right, looking at them from J1,
component side up. This yields the "yellow digit", an octal number.
Similarly, the "red digit" is obtained from the red LEDS.

YELLOW DIGIT	RED DIGIT	ERROR DETECTED
X	1	Double (or greater) error
X	3	Double (or greater) error
X	5	Double (or greater) error
7	7	No errors, all bits good
0	0	Bit 0
1	0	Triple or greater
2	0	Triple or greater
3	0	Bit 1
4	0	Triple or greater
5	0	Bit 2
6	0	Bit 3
7	0	Bit 4
0	2	Triple or greater
1	2	Bit 5
2	2	Bit 6
3	2	Triple or greater
4	2	Bit 7
5	2	Triple or greater
6	2	Bit 8
7	2	Bit 20
0	4	Triple or greater
1	4	Bit 9
2	4	Bit 10
3	4	Bit 11
4	4	Bit 12
5	4	Triple or greater
6	4	Triple or greater
7	4	Bit 19
0	6	Bit 13
1	6	Bit 14
2	6	Triple or greater
3	6	Bit 18
4	6	Bit 15
5	6	Bit 17
6	6	Bit 16
7	6	Bit 21

YELLOW DIGIT	RED DIGIT	ERROR DETECTED
0	7	Double (or greater) error
1	7	Double (or greater) error
2	7	Double (or greater) error
3	7	Double (or greater) error
4	7	Double (or greater) error
5	7	Double (or greater) error
6	7	Double (or greater) error

2102C Standard Performance Fault Control Memory Assembly
02102-60003

IIC -22

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
00	C30	CAP 1000PF 5%		0160-0938		U	1
01 03	C3,5,8,9,12,13,15,17 21-23,27,29,32-35	CAP .01UF		0160-2055		U	17
01 03	C1,2,6,10,11,14,16 18-20,24-26,31	CAP 1.0UF 20%		0160-4892		U	14
00	C4	CAP 22UF 10%		0180-0228		D	1
00	C7,28	CAP 68UF 20%		0180-1835		D	2
00	E1-8	TERM-STUD SGL		0360-1682		U	8
00	R9	RES 330 5% .25		0683-3315		U	1
00	R6-8	RES 470 5% .25		0683-4715		D	3
01	R4	RES 2.87K 1%.125		0698-3151		U	1
00	R15	RES 4.22K 1%.125		0698-3154		U	1
01	R3	RES 46.4K 1%.125		0698-3162		U	1
00	R14	RES 12.1K 1%.125		0757-0444		D	1
		SOCKET PC SINGLE		1251-1556		U	8
		JMPR PLUG .3"C-C		1258-0124		U	4
		PIN GRV .062X.25		1480-0116		U	2
01	R1,2,11	NTWK RES 9X330		1810-0272		U	3
01	R10,12,13	NTWK RES 9X470		1810-0273		U	3

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
00	R5	NTWK RES 9X4.7K		1810-0279		U	1
00	U72	IC DIGITAL D		1813-0086		U	1
01	U111	IC DIGITAL		1813-0108		U	1
00	U102	IC SN74S112N		1820-0629		U	1
01	U16,24,63,105	IC SN74S00N		1820-0681		U	4
01	U46,115,134	IC SN74S04N		1820-0683		U	3
01	U73,132,136	IC SN74S10N		1820-0685		U	3
01	U14,23,92,103,133	IC SN74S74N		1820-0693		U	5
01	U54,55,65,75,85	IC SN74S86N		1820-0694		U	5
00	U82	IC SN74S174N		1820-1076		U	1
00	U95	IC SN74LS74N		1820-1112		U	1
00	U94	IC SN74S133N		1820-1130		U	1
00	U125	IC SN74LS02N		1820-1144		U	1
00	U112	IC SN74S51N		1820-1158		U	1
01	U124	IC SN74LS04N		1820-1199		U	1
01	U44,64,74,84	IC SN74S138N		1820-1240		U	4
00	U104	IC SN74LS153N		1820-1244		U	1
01	U26,36,113,126	IC SN74S02N		1820-1322		U	4
		IC SN74S08N		1820-1367		U	1

ITEM NO.	REFERENCE DESIGNATOR FIRST SIX	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
0 0	U123			1820-1367			
01	U122	IC SN74LS14N		1820-1416		U	1
0 0	U114	IC SN74S32N		1820-1449		U	1
01	U83,93	IC SN74S37N		1820-1450		U	2
0 0	U13	IC SN74S38N		1820-1451		U	1
0 0	U11	IC SN74393 N		1820-1464		U	1
01 03	U25,31,51,56,76,86, 96	IC SN74S241N		1820-1624		U	7
01	U15,21,91	IC SN74S240N		1820-1633		U	3
01 03	U12,22,32,35,41,61 66,101	IC SN74S373N		1820-1676		U	8
01 03	U33,34,42,43,52,53, 62	IC AM93S48PC		1820-1968		U	7
01	U121	IC NE555V		1826-0355		U	1
01	CR7	DIODE 1N5817		1901-1080		D	1
01	CR4,5,6,8	DIODE-LIGHT EMIT		1990-0486		U	4
01	CR1,2,3	LED-VISIBLE		1990-0487		U	3
		EXTRACTOR-PC GRY		5040-6006		W	2
		BOARD-ETCHED		5090-0593		W	1

ECC MEMORY CONTROLLER

ECC MEMORY CONTROLLER

HEWLETT PACKARD

NEXT ASSEMBLY: 2102C

PART NUMBER: 02102-60003

D-02102-60003-52

ECC MEMORY CONTROLLER

HEWLETT PACKARD

NEXT ASSEMBLY 2102C

PART NUMBER 02102-60003

D-02102-60003-53

HP 2102E
HIGH SPEED
MEMORY CONTROLLER

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and
F-Series Computers Engineering and Reference
Documentation and is not available separately.

PREFACE

INTRODUCTION

This document provides a Theory of Operation for the High Speed Memory
Controller HP 2102E. The controller operates in conjunction with the
HP 12741A High Speed Memory Array PCA and is compatabile with memory
expansion (MEM), memory protect, dual channel part controller (DCPC).

The schematic for the 12741A is located in this section under the sub-
heading MEMORY ARRAY MODULES.

GENERAL

The HP 21MX-E High Speed Controller (2102E) is compatible with the 12741A
16-pin array card, Memory Expansion (MEM), DCPC, and Memory Protect features.
The controller, in conjunction with the 16-pin Mostek 4027P-2 4K RAM, constitutes
a high speed memory system for the HP 21MX-E series computers. Provision is
made for simple parity and refresh control. Substantial built-in test
equipment (BITE) is provided for ease of manufacturing and testability.

ADDRESS PATH

The MB and MEB buses are received from the backplane into three 74S241 buffers,
four 74S00 gates, and two 74S04 inverters (SH1, I3, J3, G4, H4, I4, J4).

If MEM is active, MEBEN- will be low, forcing BMEBEN- low, BMEBEN+ high.
The controller will idle with ENABMBRCVR- low, LATCHMB+ high, and ENABMBLATCHLO-
high. This will assert HIMBORD+ low, HIMBMEB+ high, and HIMBMEB- low, enabling
the 74S241's and 74S00's such that the memory address bus (A0+ through A19+)
will contain the value of MB0+ through MB9+ and MEB10+ through MEB19+
respectively. MB10+ through MB14+ will not be gated onto the A-BUS.

If MEM is not active, MEBEN- will be high, BMEBEN- high, and BMEBEN+ low.
In this case the contents of MB0+ through MB14+ are gated onto A0+ through
A14+ because HIMBMEB+ is low, HIMBMEB- high. Since BMEBEN+ is low, A15+
through A19+ will be low (zero), producing the desired 32K address space.

In either case, the desired address is formed on the A-BUS prior to any read
or write operation and is received into three 74S373 register chips (SH1, G5, H5, I5)
which form the MB register. When a read or write cycle actually starts, the
A-BUS contents are latched into this register. As the latch is closed,
the outputs are enabled onto the A-BUS by LATCHMB+ and ENABMBLATCHLO- going low.
After the register's outputs are stable, the MB and MEB receivers are disabled
(by ENABMBRCVR- going high) so that noise on the S-BUS will not "jiggle"
the A-BUS during the cycle. The register drives the A-BUS until the cycle
terminates, at which time the controller returns to it's idle state (ENABMBRCVR-
low, LATCHMB+ and ENABMBLATCHLO- high).

During refresh cycles, ENABMBRCVR- is forced high (SH2, E5, by REF- being low) so that the refresh address counter (SH1, H7) can be buffered onto the A-BUS by a 74S240 buffer. Thus A0+ through A6+ will contain the refresh row address while A7+ through A19+ will "float" and be indeterminite. The termination of a refresh cycle will cause REF+ to go low, incrementing the refresh counter and disabling the refresh address buffer due to REF- going high.

A connection is made to J2-44 (CC-) to allow test equipment to clear the refresh counter, allowing the test program to start the controller in a known state.

READ-DATA PATH
The CPU/array card data buses require that the following hold true;

1)   S-BUS → MDS-BUS (WRITE) no inversion
2)   MDS-BUS → S-BUS (READ) inversion

This inversion is necessary due to the fact that the array cards store true data but read-out inverted data on the MDS-BUS.

For read operations, the data inversion takes place through the T-register S-BUS drivers; a pair of 74S240 buffers (SH1, E10, F10).

The data from the array card addressed during the read operation appears on the MDS-BUS at the controller and passes immediately into the read T-register (SH1, B2, C2, D2), where the data is latched as soon as possible in order to allow the clock to the array cards to be turned off as soon as possible (this allows precharge time for the RAM's to occur in parallel with the "turn-around" time of the CPU before the next cycle starts). The parity bit (MDS16+) is also latched at this time in a 74S74 flop (SH1, D7). Data passes from the read T-register onto the 16-bit internal data bus due to TSTRCVD+ being low, enabling the read T-register outputs. Two 74S240 buffers then drive the data onto the CPU's S-BUS whenever the CPU decides to read the T-register. The occurance of TEN- low will cause the 74S240's to be enabled only if METDIS- is high (SH2, F1, F2). This corresponds to the abscence of a read-protect violation.

The data contained on the internal data bus passes into the 74S280 parity
generator/checkers, along with the latched parity bit (MDS16FF+) to form a
partial parity check across two 9-bit fields. A jumper plug provides for
selection of either even or odd parity generation and checking. The partial
checks are then exclusive or'ed by a 74S51 AOI gate to form the total parity
check (SH1, C6, PERROR-). If a parity error has occurred, PERROR- will be
low, otherwise it is high. The controller will strobe PERROR- when it is stable
(see READ CYCLE CONTROL).

Any attempt to read non-existent memory will result in the MDS-BUS not being
actively driven by any array card, hence the MDS-BUS will be "pulled-up"
by two 330-Ω R-packs so that all 17 bits will be high. This causes the S-BUS
to eventually be driven to all zeros by the 74S240's (due to the inversion),
resulting in an all-zero   read. Since there are 17 bits high, no parity
error occurs if "odd" parity has been selected, which is the normal operating
condition.

During refresh, the T-register remains unchanged since the LOADRTREG+
signal will not change.

WRITE-DATA PATH

Prior to a write operation, the CPU issues a TST- in conjunction with P4NF-,
indicating the desire to store S-BUS data in the T-register. When this occurs,
TSTP4+ will go high (SH2, F1) and TSTP4- low, enabling two 74S373 latches to
read the contents of the S-BUS (SH1, B10, C10, D10). These latches constitute
the write T-register and it should be noted that this register is distinct
from the read T-register. Due to this separation, any attempt to read the
T-register after a T-store will not necessarily recover the data just stored,
i.e., the T-register must not be used by the microcode as a "scratchpad".
Similar restrictions apply to writing data just read without an intervening
T-store.

The occurance of TSTP4- going low will set the TSTRCVD+ flop, begetting TSTRCVD+
high and TSTRCVD- low. This will set up the internal data bus such that the
write T-register drives it and the read T-register is disabled. The 74S280

parity generators then form the parity bit on the PERROR- line, which is then buffered by a 74S38 (SH1, D6) onto the MDS16+ line. The parity generators are assured of "seeing" only data bits and odd/even select due to the MDS16FF+ flop being held set by TSTRCVD- being low (SH1, D7).

IDLE CONDITIONS

When the controller is not performing a read, write, or refresh cycle, the idle state of the controller is as follows:

SAMPPON+, DELPON+ high (+5V up), low (+5V down)

MDS16FF+	indeterminate
PWRON+	high (+5V up), low (+5V down)
READFF+	low
WRITEFF+	low
READEDGE+	low
TSTRCVD+	indeterminate
ALLOWIN+	high
CLOCKSTP-	high
PERRORFF+	low
LOADRTREG+	low
REFWARN-	high
REFOPSTART-	high
RPREP+	low
REF+	low
MBUSY+	low

ALL DELAY LINE TAPS (T55+ → T23∅ + &DELREAD+) low

If the +5V supply is on then OSC+ may be either high or low but if the +5V supply is off, then OSC+ must be high for the controller to be in the defined "idle" state.

READ CYCLE CONTROL

The CPU initiates a read cycle by issuing READ- to the controller. If MEM is not installed, READOK+ will be high (SH2, B3). This enables the READFF+ flop to be clocked by READ- and be set. READFF- goes low, forcing IOINPROG+ high (SH2, B5). Since CLOCKSTP- is high CLK- will go low, initiating the read cycle at the array cards. If MEM is installed the READOK+

line will be low, inhibiting the set of READFF+. Instead, READ- will
activate BREAD+ (SH2, C1), firing a 5Ø nsec delay line. The delay of CLK-
in this case (MEM active) is necessary to allow the MEM mapping hardware to
generate the extended address bits so that the array cards may perform a
board select function. After the delay, DELREAD+ will go high, generating
DELREADSTART- (SH2, C3), which begets IOINPROG+ high. CLK- will then go low
as before. DELREADSTART- will also set the READFF+ flop.

The READEDGE+ flop forces the controller to accept only falling edges of READ-
as valid commands. Under DCPC, READ- may be active for longer than a memory
cycle, hence SETMBUSY- and DELREADSTART- are inhibited from "double-triggering"
on READ- being held at a logic low level by the READEDGE+ flop (SH2, C4).

In either case, BREAD+ will reset the TSTRCVD+ flop (SH2, F3) since a write
operation is no longer allowable (until the next T-store is received).
The presence of READEDGE+ will also force SETMBUSY- low (SH2, E4), setting the
MBUSY+ flop, activating MBUSY- low to the CPU (SH2, C1Ø). MBUSY- low indicates
to the CPU that the memory is busy and will not accept further read or write
cycle requests. When MBUSY- goes high later in the cycle, it will signify
that a T-store, read, or write cycle request may be accepted, and that in
case the cycle was a read cycle, that the read-data is stable on the S-BUS.

When IOINPROG+ goes high, LATCHMB+ goes low, as does ENABMBLATCHLO-, since
REF- is high (SH2, B6). This action causes the MB register (SH1) to latch
the set-up address and to drive the latched contents of the register onto
the A-BUS. The MB and MEB receivers will be disabled now by ENABMBRCVR-
going high, due to LATCHMB+ going low.

As CLK- falls, ALLOWIN- being low will enable HITIT+ to go high, firing the
main timing line (SH2, C7). Note that both the main timing line and the MEM
delay line are tri-state lines whose outputs are enabled by ENABLINES- being
low. During testing, the ENL+ signal is grounded at J2-47 (SH2, C1) to allow
the various timing pulses to be inserted on the associated tap nets; all of

which come out to the J2 connector. This feature allows the controller to
be single-stepped at manual or machine speeds.

Fifty-five nanoseconds after HITIT+ goes high, the T55+ tap goes high (SH2,C7)
resetting the ALLOWIN+ flop and thereby terminating the input signal   HITIT+.
Thus the timing line will contain a pulse whose duration is a minimum of
$\sim$58 nsec. and a maximum of $\sim$72 nsec.(neglecting pulse shortening of the falling
edge, which is not truly negligible). T55+ going high will also activate
OPENTREG- low (SH2, E8) and, since READFF+ is high, sets the LOADRTREG+ flop.
This enables the read T-register to pass the MDS-BUS read data which will
appear there in about another 100 nsec. Note that because WRITEFF+ is low
during a read cycle, the R/$\overline{W}$ (RR)+ line will be high, allowing the array
cards to initiate a read cycle (SH2, D7).

At "T150+ time" (150 nsec. after HITIT+ went high), the T150+ line will go
high, forcing T150- to go low, resetting the MBUSY+ flop (SH2, C10). This
causes MBUSY- to go high, signalling the "end" of the read cycle to the CPU
and informing it that read-data will be stable on the S-BUS in no more than
55 nsec., assuming that TEN- is low and METDIS- is high. At T185+ time, T185+
resets the LOADRTREG+ flop , latching the MDS-BUS read-data in
the read T-register (SH2, E9). The rise of LOADRTREG- will sample MDS16+
into the MDS16FF+ flop (SH1, D7). T185+ will also reset the CLOCKSTP-
flop, forcing CLOCKSTP- low, forcing CLK- high (SH2, C7, B6). The rise of
CLK- starts the precharge of the addressed arrays and at the same time disables
the MDS-BUS drivers on the addressed array card. Due to the data becoming
disabled and the need for data hold time at the read T-registers inputs, the
CLK- must not be allowed to go high too soon before LOADRTREG+ goes low.
To help insure that this happens correctly the CLOCKSTP- and LOADRTREG+
flops are integrated onto the same chip and are assumed to be matched in
propogation delays to within $\pm$2 nsec from CLOCK to Q going low. T150- also resets
the READEDGE+ flop ,disabling DCPC READ- commands from double-triggering MBUSY-
and READFF+.

At T230+ time, the PERRORFF+ flop is clocked, sampling the results of the
parity checkers (SH2, D9). If an error has occured, PERRORFF+ will go high and
activate PE- to the CPU (if TEN- is low and METDIS- is high (SH2, D10)) at P5 time.
The PERRORFF+ flop is reset and initialized by any cycle (INHIBITPE- low). T230+
also generates LASTTHING- low, resetting the READFF+ flop (SH2, C9, B4).

The resetting of the READFF+ flop causes READFF- to go high and IOINPROG+ low (SH2, B4, B5). This forces LATCHMB+ and ENABMBLATCHLO- high (their idle state) and sets the ALLOWIN+ flop. ALLOWIN- going low sets the CLOCKSTP- flop high (it's idle state).

LATCHMB+ going high activates ENABMBRCVR- low, re-enabling the MB and MEB receivers for the next read or write cycle.

WRITE CYCLE CONTROL

The CPU initiates a write cycle be issuing WRITE- to the controller. In order for the controller to accept the request, the CPU must have previously issued a T-store (TST- and P4NF-). Normally the CPU will only violate this protocol when it writes data into the A or B registers, in which case locations zero and one of the memory should be protected from the write operation. Additionally, the write operation will not be accepted if the memory protect feature has detected a violation (MPV- low) and DMA is not active (DMAEN- high). Assuming all of the proper conditions are satisfied, TSTRVCD- and ALLOWWRITE- will be low, activating WRITEOK+ high (SH2, D3). Since the CPU will have loaded the M-register prior to the write operation, an MEM delay is not necessary and the WRITE- signal will directly clock the WRITEFF+ flop and set it (SH2, D4). WRITEFF- going low activates IOINPROG+ high, generating the same sequence of events that occured in a read cycle when IOINPROG+ went high (some exceptions will be noted below). WRITEFF+ going high will also generate SETMBUSY- low, setting MBUSY- low (SH2, E4). Additionally, REF+ and TSTRCVD- will be low, begetting TSTANDNOTREF+ high, allowing R/$\overline{W}$ (RR)+ to go low (SH2, D6, D7). This enables the array cards to start a write cycle when CLK- goes low (in response to IOINPROG+ going high).

The generation of CLK- , HITIT+, etc. occur as in the read cycle except that at T55+ time the LOADRTREG+ flop is not disturbed, (since READFF+ is low), and at T185+ time the LOADRTREG+ flop is, again, not disturbed(since it was already reset). The subsequent generation of LASTTHING- low resets the WRITEFF+ flop, dropping IOINPROG+, and triggering the same "reset" operations as described under read cycle control. The PERRORFF+ flop is not disturbed, due to INHIBITPE- being low.

REFRESH CYCLE CONTROL (POWER ON)

An NE555 timer, connected as an astable, functions as a free-running precision refresh oscillator. Every 3$\emptyset$ μsec., the OSC+ signal goes high, causing GOSC+ to go high and clear the REFWARN- flop (SH2, J2, J3). Note that the oscillator may be single stepped, for testing purposes, by grounding HLT- (J2-29) and pulsing SINGLEREF- (J2-31) low. REFWARN- going low enables a section of a multiplexor whose function is to decode the T-periods of the CPU clock. When TA+ and TB+ are high and TC+ is low (NOTTC+ high) the CPU will be in a T3-period. This brings REFWARNTIME+ high, which is then sampled with BP5NF+ to generate RWARNT-, clocking the RPREP+ flop at the P5 to P1 transistion (SH2, H5, H6, H7). REFPREP+ high forces REFRESH- to be issued, signaling the CPU that a refresh cycle is going to occur in another two T-periods. This acts as a warning only, the CPU may still squeeze in one more read or write cycle. REFPREP- low enables the second section of the multiplexor and resets REFWARN-.

If DMA is active, the multiplexor will elect to start the refresh cycle at the next T4-period (TA+ high, TB+ low), otherwise, with DMAREAD- high, the multiplexor will start the refresh cycle at the next T2-period. In either case, the REFTIME+ signal will go high in the T-period preceeding the afore-mentioned T-periods. The REFTIME+ signal is then sampled by BP4NF+ to generate SETR1- (SH2, I5), which activates SETREF-, setting the REF+ flop. REF+ is responsible for holding MREF- active during the refresh cycle (SH2, G1$\emptyset$) and the holding R/$\overline{W}$(RR)+ in the read mode (high) (SH2, D6). MREF- informs the array cards that all rows must be selected, regardless of the state of board select or row select decoders on the cards. REF- low enables the refresh counter buffer and disables the MB and MEB receivers along with the MB register. At the trailing edge of P5 during the selected T-period, the signal SAMPRT- goes high, raising SAMPLERT+ to clock the DOREF+ signal into the REFOPSTART- flop (SH2, G5, G6, G7). REFOPSTART- going low sets the WRITEFF+ flop, starting the refresh cycle as described under write cycle control (SH2, D4). Write cycle events will occur but the state of R/$\overline{W}$(RR)+ is held high so that no write into the arrays will actually occur. REFOPSTART- low also resets the RPREP+ flop.

During the refresh cycle, ALLOWIN+ will go low, resetting the REFOPSTART- flop (SH2,G7)

At the end of the cycle the reset of the WRITEFF+ flop (by LASTTHING-) causes
WRITEFF- to go high, resetting the REF+ flop and terminating the refresh
cycle. The fall of REF+ increments the refresh counter, while the rise of
REF- samples the state of the PON+ line into the PWRON+ flop (SH2, E2).
The controller then returns to its idle condition.

POWER OFF AND POWER ON CONDITIONS
During power-fail and power-up times the PON+ signal will be low while +5M
is up. This condition allows the controller to power-down unnecessary logic
(powered by +5V), while at the same time performing refresh cycles, as needed,
to retain memory contents. Since many signals will be floating (undriven)
during these periods it is necessary to lock-out spurious CPU "signals"
due to noise, etc.   The PWRON+ flop (SH2, E2) accomplishes these functions.

The sense of PON+ is sampled by the controller at the end of every refresh
cycle by the low to high transistion of REF-. Since the refresh cycle was
initiated by the low to high transistion of OSC+, and since the duty cycle
of OSC+ is about 30%, it is clear that PWRON+ will only change state while
OSC+ is still high. The importance of this condition will be seen later.

All signals from the CPU or internal signals which are powered by +5V
are gated against PWRON+ or PWRON- so that "jitter" on these signals will not occur,
accidently starting a read, write, or refresh cycle, nor will any flops be put
into a non-idle state. Since PWRON+ can only change state at the end of a
refresh cycle (when the controller is in an idle state), the signals gated
with PWRON+ and PWRON- will not jitter during the middle of a cycle.

To start a power-off refresh cycle, the controller will, at some time, receive
a high to low transition of OSC+, generating a low to high transistion on
GOSC-, activating REFONLYPWROFF- (SH2, J3, J4, J5). REFONLYPWROFF- going
low sets the REF+ flop. Activity on signals SAMPRT-, RWARNT-, and SETRI-
is inhibited by PWRON+ being low. The setting of REF+ causes the MB
register outputs and the refresh counter buffers to activate in the usual
manner (see REFRESH CYCLE CONTROL). Since PWRON- is high, DOREF+ is high,
allowing the falling edge of GOSC- to sample DOREF+ into the REFOPSTART-
flop (through the use of SAMPLERT+ going high) (SH2, G5, G6, G7).

Note that REFONLYPWROFF- being low generates LASTTHING- (SH2, C9). The function of this event will be described under POWER-UP (INITIALIZATION).

REFOPSTART- going low triggers the usual events described under REFRESH CYCLE CONTROL. At the end of each refresh cycle, should PON+ (and thus PWRON+) go high, the state of OSC+ is <u>still</u> guaranteed to be high, avoiding the possibility of double-triggering the refresh cycle flops (due to GOSC- being low).

POWER-UP (INITIALIZATION)

Since no "reset" signal is available from the CPU, it is necessary to initialize the controller to its idle condition (described earlier) in a round-about manner. This is accomplished through the use of PON+, and the events triggered by power-off refresh.

When power is first turned on, +5M is guaranteed to be up for at least one refresh period while PON+ is low. Also, +5M down will draw FIVEDN- low so that PWRON+ will start out low (SH2, E2). Since the controller will require at least one refresh period (32 μsec) after PON+ goes high to set PWRON+ (and thereby be receptive to read and write cycle requests), the PON+ signal is used to force REFRESH- to the CPU to "hold-off" cycle requests until the sense of PON+ has been checked. While PON+ is low, and while +5V is valid, the CPU will issue TC+ as the I/O T-period counter advances. This allows NOTTC+ to clock PON+ through two flip flops to keep DELPON+ low and thus REFRESH- high. when PON+ goes high, REFRESH- will go low at least one I/O cycle later, insuring that the auto-restart state machine in the CPU will not advance without the microprogram advancing. This would happen due to a freeze in the CPU from a READ in microprogram location zero. REFRESH- is guaranteed to activate within two I/O cycles after PON+ goes high, insuring that CPU reads and writes will be held off by a freeze until the PWRON+ flop is updated by a power-off-refresh cycle. When PWRON- finally does go low, DELPON+ is reset, deactivating REFRESH-.

The following flow table illustrates how the controller initializes after only one power-off refresh cycle:

```
                        ( START )
                            |
                            v
+-----------------------------------------------------------+
| All flops and logic powered by +5M in an arbitrary state, |
| +5M up, PON+ low, +5V arbitrary.                          |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| PWRON+ flop reset by FIVEDN- low (+5M down).              |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| OSC+ goes low at some time, PWRON- is high, therefore     |
| REFONLYPWROFF- goes low.                                  |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| REFONLYPWROFF+ high forces LASTTHING- low, resetting      |
| READFF+ and WRITEFF- flops.  REFONLYPWROFF- low sets      |
| REF+ flop.                                                |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| READFF-, WRITEFF-, and DELREADSTART- (due to PWRON+ low)  |
| all high force IOINPROG+ low, setting ALLOWIN+ flop.      |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| ALLOWIN- low sets CLOCKSTP- flop, IOINPROG+ low forces    |
| CLK- high, forcing HITIT+ low, allowing delay taps to     |
| settle to "all low".                                      |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| After ~10 µsec, OSC+ goes high, REFONLYPWROFF- goes       |
| high, setting REFOPSTART- low (if it wasn't already low   |
| at power up time).  REFOPSTART- low sets the WRITEFF+     |
| flop, starting the refresh cycle in the usual "power-off" |
| manner. RPREP+ is set low.                                |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
|  T150+ and T185+ high clear the LOADRTREG+, MBUSY+, and   |
| READEDGE+ flops.  WRITEFF+ high clears the PERRORFF+ flop.|
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| State of controller now determined, refresh cycle         |
| terminates in the usual manner, bringing the controller   |
| into its idle condition, except TSTRCVD+ flop is not      |
| deterministic, which is a don't care condition for        |
| power-up purposes.  NOTTC+ initializes SAMPPON+, DELPON+. |
+-----------------------------------------------------------+
                            |
                            v
+-----------------------------------------------------------+
| After PON+ goes high, controller goes to the PWRON+ state |
| (when REF- goes high) with REFWARN- active (low).  The    |
| controller is now ready for cycle requests.              |
+-----------------------------------------------------------+
```

2102E High Performance Memory Assembly
02102-60002

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
00	C20	CAP 1000PF 5%		0160-0938		U	1
01 02	C5,8,10,12,13,14,16, 18,19,22,24,26	CAP .01UF		0160-2055		U	12
01	C27	CAP 22UF 10%		0180-0228		D	1
00	C1,23	CAP 68UF 20%		0180-1835		D	2
01	E1-8	TERM-STUD SGL		0360-1682		U	8
01	R5	RES 47K 5% .25		0683-4735		U	1
01	R7	RES 464 1%.125		0698-0082		D	1
01	R3	RES 2.87K 1%.125		0698-3151		U	1
01	R9	RES 4.22K 1%.125		0698-3154		U	1
01	R11	RES 4.64K 1%.125		0698-3155		D	1
01	R10	RES 12.1K 1%.125		0757-0444		D	1
		SOCKET PC SINGLE		1251-1556		U	4
00	W1,2	JMPR PLUG .3"C-C		1258-0124		U	2
		PIN GRV .062X.25		1480-0116		U	2
00	P1,2	NTWK RES 9X330		1810-0272		U	2
00	R4,8	NTWK RES 9X470		1810-0273		U	2
00	R6	NTWK RES 9X4.7K		1810-0279		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
0 0	U81	IC DIGITAL D		1813-0086		U	1
0 1	U91	PC022-5591		1813-0106		U	1
0 1	U52,63	IC SN74S112N		1820-0629		U	2
0 1	U16,64,73,82	IC SN74S00N		1820-0681		U	4
0 1	U46,84,85	IC SN74S04N		1820-0683		U	3
0 1	U54,62	IC SN74S10N		1820-0685		U	2
0 1	U24,51,53,71,72,74	IC SN74S74N		1820-0693		U	6
0 0	U35	IC SN74LS74N		1820-1112		U	1
0 0	U23	IC SN74S51N		1820-1158		U	1
0 1	U45	IC SN74LS04N		1820-1199		U	1
0 0	U55	IC SN74LS153N		1820-1244		U	1
0 1	U25,65,75,93	IC SN74S02N		1820-1322		U	4
0 0	U44	IC SN74S08N		1820-1367		U	1
0 1	U92	IC SN74LS14N		1820-1416		U	1
0 0	U34	IC SN74S32N		1820-1449		U	1
0 0	U83	IC SN74S37N		1820-1450		U	1
0 0	U61	IC SN74S38N		1820-1451		U	1
0 0	U43	IC SN74393 N		1820-1464		U	1
		ICSN74S241N		1820-1624		U	5

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	U11,31,56,86,96			1820-1624			
01	U15,26,42,66	IC SN74S240N		1820-1633	U		4
00	U13,33	IC SN74S280N		1820-1638	U		2
01 03	U12,21,22,32,36,41 76	IC SN74S373N		1820-1676	U		7
00	U95	IC NE555V		1826-0355	U		1
01	CR1	DIODE 1N5817		1901-1080	D		1
		EXTRACTOR-PC GRY		5040-6006	W		1
		EXTRACTOR-PC WHT		5040-6075	W		1
		BOARD-ETCHED		02102-80002	W		1

HP 2102H
HIGH SPEED FAULT CONTROL
MEMORY CONTROLLER

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and
F-Series Computers Engineering and Reference
Documentation and is not available separately.

```
+----------------------------------------------------------+-----------------+
|                                                          |                 |
|    HIGH SPEED FAULT CONTROL MEMORY CONTROLLER            |   SECTION    I  |
|                                                          |                 |
+----------------------------------------------------------+-----------------+
```

1. INTRODUCTION

This document provides the theory of operation for the High Speed Fault
Control (HSFC) Memory System used in the HP 1000 E-or F-Series Computer and is
divided into two sections: general theory of operation and detailed theory of
operation. The general theory gives an overview of memory system operations,
while the detailed theory describes significant events occuring during memory
operations and the functional components that produce them. References to the
M-Series Computer in this discussion are for information relative to
configuration only. The high speed memory products offer no practical
advantage in the M-Series, therefore they are only supported on E-/F-Series
Computers. Brief descriptions of the ECC code and error detection display are
contained in Appendix A.

2. GENERAL THEORY OF OPERATION

The general theory of operation consists of a description of the memory system
and a brief description of each of the three memory cycles.

3. DESCRIPTION

The High Speed Fault Control (HSFC) Memory Option is compatible with HP 1000-E
and F-Series computers, high speed 16K word and 64K word memory array boards,
memory expansion (MEM), DMA (DCPC), and memory protect features. The HSFC
system consists of a 2102H Memory Controller, part number 02102-60004, one or
more 12779H or 12780H Fault Control Array boards (also known as check bit
boards) part numbers 12779-60002 and 12780-60002, and one or more high
performance memory array boards. The controller is able to detect all single
and double bit errors, as well as some triple bit errors; all single bit
errors are corrected when fault control is enabled. Refresh control is also
provided.

Memory data is encoded as a 22-bit distance-4 "Hamming plus parity bit" code.
This is a separable code consisting of 16 data bits, 5 check bits
corresponding to Hamming code check bits for a distance-3 code, and a parity
bit (over all 22 bits) to provide a distance-4 code. The 16 data bits and one
of the check bits are stored on the normal memory array boards (usually used
for 16 data bits plus one overall parity bit), while the remaining four check
bits and the overall parity bit are stored on the check bit array boards. The
check bit boards must be configured to exactly match the amount of memory on
the memory array boards so that diagnostics will not generate parity errors

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where there is no memory. Configuration, installation, and troubleshooting information is contained in the High Speed Memory System Installation and Service Manual, part no. 5955-4311.

Four jumpers on the controllers allow configuration/testing: 1) "Test" generates odd (in) or even (out) overall parity and is used for testing the parity generators (e.g. Memory protect/parity error diagnostic); 2) "MX" (not used with 2102H controllers) determines use with M-series (in) or E-/F-Series (out) CPU's; 3) "CORRECT" selects whether a parity error is generated on single bit errors (out) or double bit errors (in), the latter being the case when all single bit errors are corrected; 4) "MX + MEM-" generates a delay for DMS reads (out) or no delay (in). The check bit boards are hardware configurable for standard speed (250ns) RAMs (W3, W5 in for 12779A/12780A) or high speed (150ns) RAMs (W4, W6 in for 12779H/12780H). XW1 and XW2 provide jumper selectable address configuration for both starting address and amount of addressable memory (up to 256K words for 12780H, 128K words for 12779H).

The read cycle reads out a 22-bit data word from the memory address sent to it by the CPU and transfers the 16 data bits to the S-bus. The write cycle writes a 16-bit data word with 6 check bits into the memory address sent to it by the CPU. In the write mode the controller derives the check bits from the data word and stores the check bits and the data word in memory. When the data is retrieved in the read mode, the controller again derives the check bits for the 16-bit data word and compares them with the check bits supplied from memory. With the "CORRECT" jumper in, single bit errors are corrected. Correction is performed on a read-through basis only, i.e. corrected data is not written back to the arrays. Double and triple bit errors cause a parity error indication to be sent to the CPU. If the "CORRECT" jumper is out, errors are not corrected, and a parity error indication is sent to the CPU for single bit errors.

The memory is composed of semiconductor Random Access Memorys (RAMs) which require refreshing every two milliseconds. This refresh cycle automatically occurs approximately every 16 microseconds. Each refresh cycle refreshes 1/128th of the memory so that the total memory is refreshed, as required, every two milliseconds.

The refresh is performed normally in I/O Timing periods T2 and T3, but when memory is under DCPC control for a read, it is performed in periods T4 and T5. This leaves periods T2 and T3 for the DCPC (DMA) read cycle. When a refresh cycle is started, the CPU is notified so that read and write cycles are inhibited until the refresh cycle is complete.

4. Read Cycle

The read cycle is initiated when the READ- signal from the CPU becomes active. The memory address from the CPU is buffered by the M-register (on the controller) and supplied to memory. The address is stored in the M-register and is continually supplied to memory until the data is read out from the stored memory address. The 16-bit data word is read from memory and stored in

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the Read T-register, and the check bits are supplied to the parity circuits. After the result of the parity check is valid, the parity error status is sent to the CPU. The S-bus drivers are opened to enable transfer of the memory data word to the S-bus. Finally, the controller and memory circuits are restored to the idle state.

5. Write Cycle

In a write cycle, the data to be written to memory and the address into which it should be written are both valid before WRITE- is issued by the CPU. The address is buffered by the M-register on the controller and passed on to memory; the data is latched in the Write T-register and supplied to the syndrome generators and to memory. Following the WRITE- signal from the CPU, the address is latched in the controller MB-register and the data bits and check bits are written into the selected memory address. At the completion of the write cycle, the controller and memory circuits are restored to the idle state.

6. Refresh Cycle

A refresh cycle is initated automatically by an oscillator on the controller. Before refresh starts, the CPU is notified that a refresh cycle will occur so that it will not begin a memory cycle. A 0-to-127 counter on the controller selects a different row of memory elements within the RAM IC's to be refreshed by each refresh cycle (4K RAMs use the counter as a 0-to-63 counter.) In a refresh cycle, all RAMs are refreshed at the same time; the row addresses are used only internal to the RAM integrated circuits.

7. DETAILED THEORY OF OPERATION

The detailed theory of operation consists of a description of how a word of memory is addresed, a description of memory signals, identification of the functional units on the memory controller, a description of initial conditions before a read or write cycle starts, and a summary of a read, write, and refresh cycle.

8. HP 1000 Memory Addressing

The HP 1000 main memory is contained on one or more PCA's. Each PCA contains four rows of RAMs (memory IC's). There are 17 RAMs in a row, one for each bit of the 16-bit data word plus the parity bit. A board may be loaded with 4K or 16K RAM IC's. The 12741A and 13187B are loaded with four rows of 4K RAMs and are referred to as 16K boards. The 12747H and 12747A are loaded with four rows of 16K RAMs and are referred to as 64K boards. The 16K and 64K designations refer to the amount of addressable memory (i.e., 16-bit data words) available on the PCA; 1K is defined as 1024.

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NOTE

In this discussion, the word "row" is used to
refer to two different items:

a. A group of IC's arranged in a row on a PCA.
b. A row of memory elements within an IC.

Each 4K RAM contains a 64-row by 64-column matrix of memory elements for a
total of 4096 (4 times 1024 equals 4096 equals 4K) memory elements within the
RAM. A row of 17 such RAMs is capable of storing 4096 17-bit memory words,
with each bit of the memory word stored in a separate RAM dedicated to that
bit. Each bit of a data word is stored in an identical element in each RAM;
that is, the same column and row are addressed on each RAM to form the 17-bit
word. The 16K RAM operates in the same manner except that it has a 128-row by
128-column matrix of memory elements for a total of 16,384.

The basic memory addressing consists of a 15-bit address word. The Memory
Expansion Module (MEM), which is part of the Dynamic Mapping System (DMS)
option, expands the 15-bit memory address word to a 20-bit memory address
word. This provides an addressing capability for one million words of memory.

The 20-bit address word is used to select a 17-bit data word stored in main
memory. To select a memory word, four items must be identified; the PCA, the
row of IC's on the PCA, the row of elements within each IC, and the column of
elements within each IC. The memory address bits used to identify these items
are listed in Table 1 for 4K IC's and Table 2 for 16K IC's.

Bits 6 through 11 for the 4K RAM and bits 7 through 13 for the 16K RAM form a
binary word that identifies the column of memory elements. The same is true
for the bits that identify the row of elements. The column and row words are
supplied to each RAM and are decoded within each RAM to select the single
designated memory element.

For the purpose of refreshing, only the 64 (4K RAM) or the 128 (16K RAM) rows
on each RAM are addressed. It is not necessary to address each individual
memory element for refreshing.

Table 1. Memory Addressing 4K RAM IC's

MEMORY ADDRESS BITS	ITEM IDENTIFIED
14 through 19	Memory PCA
12, 13	ROW (0 through 3) of RAMs on the PCA
6 through 11	COLUMN of elements within each RAM
0 through 5	ROW of elements within each RAM

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Table 2. Memory Addressing 16K RAM IC's

MEMORY ADDRESS BITS	ITEM IDENTIFIED
16 through 19	Memory PCA
14, 15	ROW (0 through 3) of RAMs on the PCA
7 through 13	COLUMN of elements within each RAM
0 through 6	ROW of elements within each RAM

9. Signal Description

Table 3 lists the control and status signals used in the memory system and contains a brief description of their function.

Table 3. Memory System Signals

SIGNAL	FUNCTION
READ- (From CPU or DCPC to controller)	Initiates a memory read cycle
WRITE- (From CPU or DCPC to controller)	Initiates a memory write cycle.
MPV- (From MP to controller)	Indicates a memory protect write violation to the controller. In a DCPC operation, it has no effect. In a normal write mode, no write cycle occurs.
DMAEN- (From DCPC to controller)	Indicates that a DCPC memory cycle is going to occur. DCPC activity disables memory protection logic. The DCPC is free to read or write in the protected area of memory.
DMAREAD- (From DCPC to controller)	Delays a refresh cycle which might be ready to begin until time periods T4 and T5. (The refresh cycle normally occurs during T2 and T3.) This leaves T2 and T3 for the DCPC read cycle.
P4NF-,P5NF- (From CPU to controller)	The last two clock periods occurring in a T period. P4NF- together with TST- enables storing of data into the T-register during a write cycle. The P5NF- which occurs in time period T6 (or T3 if a DCPC read cycle is beginning) enables the refresh cycle to begin if one is due.

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Table 3. Memory System Signals (Continued)

SIGNAL	FUNCTION
TA+,TB+,TC+ (from CPU to controller)	These signals, when decoded, indicate the cur- rent I/O time period. These signals are active in the following "T" periods: TA =T3 thru T5; TB =T4 thru T6; TC =T5 thru T6.
PON+ (From power supply to controller)	Indicates that the power supply is receiving ac line power and is operating properly. When PON becomes inactive, reading and writing is inhib- ited and refresh cycles occur every 16 micro- seconds (if the system has battery backup), in- dependent of conditions external to the memory system.
POPIO+ (From CPU to controller)	An initializing signal generated by the CPU (if it is in the halt state) during T5 when PON+ is low or when Preset is pressed on the front pan- el. Used to initialize the syndrome latch and the single bit error detection latch.
TEN- (From CPU or DCPC to controller)	Allows the S-bus drivers to pass data from the Read T-register to the S-bus after the READ- signal has become inactive in a read cycle.
TST- (From CPU or DCPC to controller)	Together with the P4NF- signal, enables the Write T-register to latch the data from the S-bus for a write operation.
MEBEN- (From MEM to controller)	Enables the expanded address from MEM to be passed to the memory arrays and to be latched by the MB-register. If MEBEN- is high, all ad- dress bits 0 to 14 are taken from the MB bus with bits 15 - 19 held at logic 0. If MEBEN- is low, address bits 0 to 9 are taken from the MB-bus, and address bits 10 to 19 are taken from the MEB-bus (from MEM).
METDIS- (From MEM to controller)	Indicates a read is being attempted in a pro- tected area of memory. The S-bus drivers are disabled, so the S-bus presents an all "1's" word to the CPU. METDIS- is suppressed for a DCPC read cycle.
R/W-(RR)+ (From controller to memory array)	This signal, when active low, is used to acti- vate the write logic on the memory PCA's. This signal is held high for a read cycle.

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Table 3. Memory System Signals (Continued)

SIGNAL	FUNCTION
CLK- (From controller to memory arrays)	This signal initiates a memory cycle on the memory array boards. Reading or writing is selected by the R/W(RR)+ signal, while a refresh cycle is indicated by MREF- low.
MREF- (From controller to memory arrays)	Informs memory that a refresh cycle is to occur. Used on the memory PCA with the CLK- signal to initate a RAS-only-refresh for the RAMs.
MBUSY- (From controller to CPU)	Indicates to the CPU that the memory system is busy. When the signal is no longer active (goes high) the memory system is available for another memory cycle.
REFRESH- (from controller to CPU)	Indicates to the CPU that a refresh cycle will begin in two T periods. Read and write cycles are inhibited during a refresh cycle.
PE- (From controller to CPU)	Indicates to the CPU that the data word read from memory during the current cycle contains a parity error. For the HSFC memory system, this may be interpreted as a single or double bit error depending on the "CORRECT" jumper configuration.
MB0 thru MB14+ (From CPU or DCPC to controller)	This is the memory address bus. Used in CPU and DCPC read and write cycles.
MEB10+ thru MEB19+ (From MEM to controller)	This is the extended memory address bus. The upper 10 address bits are taken from this bus when MEM is enabled (MEBEN- low).
A0+ thru A19+ (From controller to memory arrays)	This is the address bus to the memory arrays. The use of the 20 bit address was discussed in in paragraph 8. In a refresh cycle, the contents of the refresh counter are enabled onto A0+ thru A6+.
MDS0+ thru MDS16+ (Bidirectional - controller and memory arrays)	This is the memory data bus on which data (and one parity or check bit) passes to and from the memory arrays on read and write cycles.

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Table 3. Memory System Signals (Continued)

+---+
SIGNAL   FUNCTION
CMDS17+ thru CMDS21+   This is the memory data bus on which check bit
(Bidirectional -   data passes to and from the check bit arrays
controller and   in a fault control system.
check bit arrays)
S-Bus   This is the main bus for data transfer within
(Bidirectional -   the CPU and for CPU/external memory transfers.
CPU and controller)
NOTE: CS- and R/W-(WR)+ are activated by the controller but they are
not used with the Memory PCA's discussed in this text.
+---+

10. FUNCTIONAL UNIT DESCRIPTION

The HSFC memory system is broken up into three basic elements: the memory
controller (2102H), the check bit array boards (12779H and 12780H), and the
memory arrays. The proper schematics should be consulted in conjunction with
the theory of operation for each of these. They are:

                2102H   D-02102-60004-51,52,53
                12779H/12780H   D-5955-4303-51
                12741A   D-5950-3749-51
                12746H/12747H   D-5955-4304-51

All functional components and signal names are well marked on the schematics
and will be referred to in the following discussions.

11. IDLE (Pre-Cycle) CONDITIONS:

When no cycle is in progress, the following conditions exist in the memory
system:

a. The MB/MEB Receivers and Mux are enabled so that any address supplied by
    the CPU (addresses are valid before READ-, WRITE- become active) is driven
    on the A-bus to the memory arrays.

b. The MB-register is enabled to receive the memory address. The register
    will be latched and its outputs enabled early in the read or write cycle.

c. The Read T-register and Write T-register are not enabled to latch MDS-bus
    or S-bus data.

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d. The S-bus drivers and CMDS-bus drivers have their outputs tri-stated (not enabled).

e. The READFF+ and WRITEFF+ outputs are low.

f. MBUSY- is high indicating memory is available for a cycle.

g. PERROR+ is low.

h. PWRON+ is high if +5v is active, low if +5v is inactive.

i. All REFRESH related signals are inactive, i.e. CPU Refresh Warning FF and Refresh Cycle FF are low, REFRESH- (to CPU) and MREF- (to memory arrays) are high.

j. All delay line taps are low.

k. The Syndrome Latch/Display and Single Bit Error FF/LED retain their respective last-clocked states.

l. CLK- to the memory arrays and check bit arrays is high, so the RAMs are inactive (disabled).

12. ADDRESS PATH

The address on the MB-bus from the CPU and the MEB-bus from MEM are received into three 74S241 buffers (sh2,E1), four 74S00, and two 74S04 gates. If MEM is not present or not active, MEBEN- will be high, BMEBEN+ low. Thus when the controller is asserting ENABMBRCVR-, MB0+ through MB13+ will be buffered through the S241's onto A0+ through A13+ (the array boards' address bus).

A14+ and A15+ will be generated by section two of a 74S241 because of HIMBORD+ being active, HIMBMEB- being inactive. Since BMBEN+ is low, GMEB16- through GMEB19- will be high, forcing A16+ through A19+ to be low. Thus A0+ through A14+ copy MB0+ through MB14+, while a A15+ through A19+ are low, producing the desired 32K address space.

If MEM is present and active, BMEBEN- will be low, BMEBEN+ high, forcing HIMBMEB+ high, and HIMBORD+, HIMBMEB- low. This will cause MB0+ through MB9+ to be buffered onto A0+ through A9+ as before (if ENABMBRCVR- is active), while MEB10+ through MEB15+ are gated to A10+ through A15+. Since BMEBEN+ is high, MEB16+ through MEB19+ are gated onto A16+ through A19+, producing a one million word address space.

Note that the controller idles with ENABMBRCVR- active, so the address for a read/write operation is set up quickly on the A-bus through the capacitive drivers (S240's and S241's) as soon as possible. Also, during idle times, LATCHMB+ is high and ENABMBLATCHLO- is high, allowing the contents of the A-bus to be transferred to the MB-register (three 74S373 latches) but not read out. During a read or write operation, LATCHMB+ is dropped along with

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ENABMBLATCHLO-, latching the A-bus and holding it stable by enabling the outputs of the MB-register. LATCHMB+ disables ENABMBRCVR- causing the outputs of the MB/MEB receivers to be tri-stated so that changes on the MB-bus due to noise on the S-bus will not drive the A-bus and cause glitches on the A-bus.

During refresh, ENABMBRCVR- is high, causing A7+ through A19+ to be arbitrary (since the MB-bus is not defined during refresh) while A0+ through A6+ are driven not by the S373 (SH2,D6), but by the 74S240 at E9 (REF- active). Thus the refresh counter buffer drives the refresh address onto the A-bus. The counter is incremented for the next refresh cycle at the end of the current refresh cycle (REF+ going low).

13. READ-DATA PATH

The CPU data bus (S-bus) to memory array data bus (MDS-bus) path must have the following relationship:

1) S-bus to MDS-bus (WRITE)   Data normal
2) MDS-bus to S-bus (READ)   Data inverted

This inversion is necessary because of the fact that the memory array cards store true data but read out inverted data on the MDS-bus. For read operations, the inversion takes place automatically at the "DATA CORRECTION" XOR (exclusive or) gates (SH1,A9 thru E9) since the other input of these gates is normally high. During the first part of a read cycle when LOADRTREG+ is high, the check-bits MDS16+ through CMDS20+ and the data-bits MDS0+ through MDS15+ are gated to a set of five 93S48 parity generators. The odd parity outputs will all be low if no errors have occurred. Four 74S138 decoders perform a 5-line to 32-line decode of these outputs without the need for additional decoding circuitry because of the availability of the even parity outputs and active high and low enable inputs on the 74S138's.

From coding theory, it is easy to show that sixteen of the decoder outputs (all of which are active low) correspond to errors in the data bits, five to errors in the five Hamming code check bits (MDS16+ to CMDS20+), one to "NO-ERROR" (P16P200K-), and the remaining ten outputs to errors in ten data bit positions which in this machine do not physically exist. If a decoder output corresponding to one of these positions is active, a triple (or greater) error has occurred. Any triple (or greater) error which is detected will activate ECCHALT+, which is clocked into the parity error FF and forces PE- low, halting the computer at the end of the cycle. This same result can occur if a double-bit error is detected with the "CORRECT" jumper in or if a single-bit error is detected with the "CORRECT" jumper out. P16P200K is also used by the controller in conjunction with the parity bit P21 (CMDS21+) to detect double-bit errors. The double-bit error is detected if the data word has correct overall parity (P210K-low) and the syndrome decodes to an error (i.e. one or more of the P160K- thru P200K- signals is high).

The first time a single-bit error occurs (P210K- high), the Single Bit Error FF is latched (the LED goes out) and remains so until PRESET on the CPU front

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panel is pressed. Presetting the CPU causes a train of POPIO pulses which will initialize both this flip-flop and the Syndrome Latch/Display so that all LEDs are on; this provides a test for the LEDs.

The syndrome is latched if a parity error occurrence is clocked into the Parity Error FF. With the "CORRECT" jumper in, the display can be decoded only to indicate double bit or triple/greater bit errors; with the "CORRECT" jumper out, the display will indicate the single bit in error. This latter mode can be useful in finding bad bits if standard memory diagnostics are run.

If the "CORRECT" jumper is in, single errors in the data bit positions are corrected by passing the erroneous bit thru the XOR gates (i.e. the normal inversion is omitted for a faulty bit); this is a result of the appropriate decoder output being low. If the "CORRECT" jumper is out, correction is defeated to allow diagnostics to read the erroneous data.

The T-register Control FF will activate and deactivate LOADRTREG+ at the appropriate times to latch read data from the arrays. Corrected or unchanged data passes from the invert gates to two octal 74S241 buffers. The CPU reads the T-register during the cycle or in later T-periods by issuing TEN-. MEM must have METDIS- inactive (implying no read protect violation) when TEN- is low in order for the T-register contents to be dumped onto the S-bus. Also at this time, the parity error latch will be enabled onto the PE- line. During refresh the T-register remains unchanged and the Parity Error FF is not strobed.

The overall parity bit is checked by one additional parity generator (SH1, G6), plus two XOR gates, to signal an overall parity error (P210K- high).

14. WRITE-DATA PATH

Write data from the CPU S-bus is presented to two octal 74S373 latches on the controller which form the Write T-register. Prior to the WRITE- signal the data is latched by the concurrence of TST- and P4NF-. Also at this time, the Read T-register outputs are disabled (thus pulling up the check bit inputs to the Parity Generator/Checker), and the write data is driven onto the MDS bus to the memory arrays thru two 74S241 buffers. Because of the check bit input pullups, the 93S48's generate odd parity over the data bit inputs; these bits are inverted by the 74S240 CMDS driver to provide the desired even parity over each grouping of data bits. A separate 93S48 is used to generate overall odd parity which is also inverted to provide overall even parity. Check bit CMDS 16+ is stored on the regular memory array PCA, while check bit CMDS17+ thru CMDS20+ and overall parity bit CMDS21+ are stored on the check bit array PCA.

15. READ CYCLE CONTROL (POWER ON)

The CPU initiates a read cycle by issuing READ- (low) to the controller. If this is a MEM read in a E-/F-Series CPU (MX + MEM- jumper out), the clock to the array boards must be delayed until the address bus stabilizes (requiring a

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50ns delay from READ-↓ to CLK-↓). This is accomplished by delaying the setting of the Read FF until DELREADSTART- (SH3,C3) presets it 50ns after the READ- edge clocks the flip-flop (with the J input held low because the jumper is out).

A non-MEM read will set the Read FF, since READOK+ is high when READ- goes low. Note that for both types of reads, the setting of the READ FF depends on the Power Sense FF indicating that power is on. This is because only refresh cycles (to prevent harmful or spurious reads or writes) should occur if the main +5 volt supply is inactive. In either case, READFF- going low or DELREADSTART- going low will set IOINPROG+ high. IOINPROG+ high activates CLK- low (starting the read cycle in the appropriate array card), and also activates HITIT+, firing the main timing line (SH3,C9). IOINPROG+ high also sets LATCHMB+ low and ENABMBLATCHLO- low, disabing the MB/MEB Receiver outputs but latching the A-bus contents and holding the A-bus by enabling the MB-register outputs. In parallel with the above operations BREAD+ going high will activate RDBUSY-(SH3,D6), and set the MBUSY FF to inform the CPU that the memory system is busy (MBUSY- low). BREAD+ also clears the Write Validate FF (SH3,E3), enabling the internal data bus elements such that read data may pass from the MDS-bus to the S-bus.

About 100ns after CLK- goes low, the T100+ timing line tap will go high, setting the T-register Load Control FF (LOADRTREG+ high), and setting SETMREADY- active in an M-Series CPU (MBUSY- high). This latter action occurs only if the "MX" jumper is in, indicating that the controller is in an M-Series CPU.

As T150+ goes high (150ns after CLK-↓) the Pulse Generator FF (U103) is cleared terminating the input signal (HITIT+) to the delay line. Thus the delay line contains approximately a 150ns long pulse. ALLOWIN+ going low also ends various set and reset pulses, and sets up new event qualifiers while disqualifying previous events.

At T200+ time, the T-register Load Control FF is cleared (LOADRTREG+ low), thereby latching read data into the Read T-register (SH2,F8). As T200+ goes high, CLOCKSTP- becomes active forcing CLK- to go high, which ends the active memory cycle on the array cards. It is possible for MDS-bus data to remain valid for only 6ns after CLK- goes high, thus LOADTREG+ must go low before CLK- goes high. This is assured because CLOCKSTP- and LOADTREG+ are on the same chip.

At T215+ time, SETMREADY- will be generated if the controller is in an E- or F-Series CPU, i.e. if MXE+ is high (SH3, A6). SETMREADY- low resets the MBUSY+ flop, indicating to the CPU that the cycle is complete and that read data will be stable (valid) on the S-bus in 55ns maximum if TEN- is low

At T290+ time the Parity Error FF (SH3,G8) and the Single Bit Error FF (SH3,G9) are clocked with the results of the error detection logic. If an error has occurred which is supposed to halt the CPU, ECCHALT+ will be high. This will be the case whenever a triple error (or greater) occurs, or when the following conditions exist:

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P16P200K-	P210K-	SINGSTP+	ECCHALT+	ERROR CONDITION
LO	LO	LO	LO	NO ERROR
LO	HI	LO	LO	P21 BAD, SINGLE ERROR
HI	LO	LO	HI	DOUBLE ERROR
HI	LO	HI	LO	DOUBLR ERROR
HI	HI	LO	LO	SINGLE ERROR
HI	HI	HI	HI	SINGLE ERROR

Also at T290+ time, LASTTHING- will activate (SH3,G9), clearing the Read FF and terminating the cycle. READFF- going high brings IOINPROG+ low, setting ALLOWIN+ active, preparing it for the next cycle. ALLOWIN- low sets CLOCKSTP- (this terminates CLK-) and terminates LASTTHING-. The controller should now be in the "IDLE" state.

16. WRITE CYCLE CONTROL (POWER ON)

The CPU initiates a write cycle by issuing WRITE- low to the controller. If MPV- is inactive (no attempted write into a memory protected area) or if DMAEN- is active (OK for DMA) then ALLOWWRITE- will be low, allowing the write cycle to proceed if a TST- has previously been received and power is on (as discussed for Read Cycle). Normally, TST- will activate (along with a P4NF-) in the T-period prior to WRITE- going low, to store data into the Write T-register. This would also activate TSTP4+ and TSTP4-, setting the Write Validate FF (TSTRCVD + and - active). This flip-flop enables R/W(RR)+ to go low (after the Write FF is clocked), enabling the array boards for a write operation. Issuance of WRITE- without a prior TST- can occur if the CPU stores into the A or B registers. In this case, the write to memory is inhibited (the A and B registers, although addressed as memory locations 0 and 1, are physically different from these memory locations.) The Write Validate FF is reset by the occurence of a read operation. As discussed earlier, TSTRCVD+ and - enable the write data path to the MDS-bus and disable the read data path from the MDS-bus.

Assuming that TSTRCVD+ is active, WRITEOK+ will be high, allowing WRITE- to clock the Write FF. No delay is required for MEM-Writes since the address is set up in the previous microcycle (worst case) giving a 175ns setup time.

WRITEFF- going low will generate IOINPROG+ high, starting the same chain of events that occurred in the read cycle previously described.

The T-reg Load Control FF, Parity Error FF, and Single Bit Error FF will not be set since READFF+ and WRITEFF- are low. Termination of the write cycle by LASTTHING- going low is identical to the termination of a read cycle.

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17. REFRESH CYCLE CONTROL (POWER ON)

U121 (SH3,J1), connected as an astable multivibrator, functions as a free-running refresh oscillator. Every 15 microseconds, the OSC+ signal goes high, causing GOSC- to clear the REFWARN FF(SH3,J4). This enables a strobe input of a 74LS153 multiplexor (SH3,H3), so that at the next T4 period (TA+ high, TB+ high, and TC+ low) REFWARNTIME+ will go high; the signal it then sampled with BP5NF+ to assert RWARNT- (if PWRON+ is high), setting the CPU Refresh Warning FF (SH3,H8). This causes REFRESH- to be issued to the CPU (warning it of an impending refresh cycle) enables the Refresh Time Decoder (SH3,H3) to choose the actual refresh time, and resets the REFWARN FF. It is possible for a read or write cycle to start at the next T-period (READ- or WRITE- low at beginning of T5), making it necessary to warn the CPU two T-periods before the actual refresh cycle begins on the memory array cards (so a memory cycle and refresh cycle won't happen coincidentally).

If a DMA read is occurring (DMAREAD- low starting at T6 to indicate read during T2 and T3), the refresh cycle will start at the next T4 period; otherwise (with DMAREAD- high) the refresh cycle will start at T2. The signal REFTIME+ will go high during T6 or T2 (DMAREAD- high and low respectively). At P4 of the proper T-period, the Refresh Cycle FF (SH3,I8) is set by SETREF- and issues MREF- to the memory arrays to indicate that a refresh cycle is to be performed. REF- low brings ENABMBLATCHLD- high (disabling the low order MB-register outputs) and drives the 7-bit refresh address onto the A-bus by enabling the Refresh Counter Buffer (SH2,E9).

As a result, the low-order address bits will contain the value of the Refresh Counter, while the high-order address bits will be arbitrary (MB-bus undefined). Since TSTANDNOTREF+ (SH3,E6) is low, R/W-(RR)+ will be high so that inadvertant writing into the RAMs does not occur. The state of the controller is thus prepared for refresh.

At the P5NF- rising edge, SAMPLERT+ goes high, sampling the DOREF+ signal and causing the REFOPSTART- to go low (SH3,G8). REFOPSTART- low sets the Write FF, starting the refresh cycle, resets the CPU Refresh Warning FF, and disables the Refresh Time Decode Multiplexor.

From this point on, the events that take place in a refresh cycle are the same as the events that take place in a write cycle except for:

1. When ALLOWIN+ goes low at T150+ (SH3,C7), the REFOPSTART FF (U133) is reset. This allows the Write FF to be reset at the end of the cycle since the set input to the Write FF is brought high.

2. When the cycle ends (LASTTHING- going low), the transistion of WRITEFF- from low to high resets the Refresh Cycle FF. This ends MREF- to the arrays, disables the Refresh Counter Buffer, increments the Refresh Address Counter, and clocks the Power Sense FF.

3. R/W(RR)+ is held high (Read mode).

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18. POWER OFF AND POWER ON CONDITIONS

During Power-Fail and Power-Up times the PON+ signal will be low. +5M will be stable before PON+ goes high at Power-Up; it will also be stable if the dc power is off and the CPU has battery backup. +5M is valid for a minimum of 50 microseconds after PON+ goes low in a power fail condition without battery backup. Separating +5M (battery backed up) and +5V (not backed up) allows memory contents to be retained under battery backup by performing refresh cycles but not having to power logic not needed for refresh. Since many signals will be floating during these periods it is necessary to lock-out spurious CPU "signals" due to noise, etc. The Power Sense FF accomplishes this lockout function.

The sense of PON+ is sampled by the controller at the end of every refresh cycle by the low to high transistion of REF-. Since the refresh cycle was started by the low to high transistion of GOSC-, and since the duty cycle of the refresh oscillator is approximately 30% (high for 50 microseconds), it is obvious that PWRON+ will change only when GOSC- is high (GOSC+ low). The importance of this condition will be seen later.

All signals to the array boards are controlled by powered logic which is activated directly or indirectly from the Read FF or Write FF, hence CPU signals will not affect the refresh cycle in any way since both flip-flops have inputs qualified by PWRON+/-. Should power be restored, the Power Sense FF will change state at the end of a refresh cycle, insuring that no array board signals will "jitter" due to PWRON+ activating in the middle of a refresh cycle.

A power-off refresh cycle is initiated by a high to low transition on OCS+, forcing REFONLYPWROFF- to go low (since PWRON- is high), setting the Refresh Cycle FF. Activity on signals SAMPRT-, SETR1-, and RWARNT- is inhibited by PWRON+ being low. The setting of REF+ causes the MB-register output controls and the Refresh Counter Buffers to activate in the usual manner (see Refresh Cycle Control). Since PWRON- is high, DOREF+ will be high; when the rising edge of OSC+ causes REFONLYPWROFF- to go high, SAMPLERT+ goes high and sets the REFOPSTART FF (because DOREF+ is high).

REFOPSTART- going low triggers the same events described under refresh cycle control. Note that at the end of each refresh cycle, should PWRON+ go high, the state of OCS+ is still guaranteed to be high, avoiding the possibility of double-triggering the refresh cycle flip-flops.

Substantial power is saved in the controller by powering down the data paths and much of the address and control logic. Due to the performance required by the controller, however, substantial +5M power is still used for the Schottky control logic.

19. POWER-UP (INITIALIZATION)

When power is first turned on, the controller will require at least one

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refresh cycle after PON+ goes high to sense PON+ (setting PWRON+). Since the CPU will try to start cycles in a shorter interval, the controller holds off the CPU by forcing MBUSY- low to the CPU whenever PWRON- is high and PON+ has come up (SH3,D6). This allows proper power-up sequence in the controller without ignoring CPU cycle requests. Since no "reset" signal is available from the CPU, it is necessary to initialize the controller at power-up time to its "idle condition" described earlier. To see how reset is accomplished the following flow table is presented:

```
----------------------------------------------------------
| START!!                                                 |
| All FFs and logic powered by +5M arbitrary,            |
| +5 down, +5M up, PON+ low.                             |
----------------------------------------------------------
                           |
----------------------------------------------------------
| Power Sense FF reset by +5 being down (SH3,D3)          |
| (FIVEDN- LOW), MBUSY- low                               |
----------------------------------------------------------
                           |
----------------------------------------------------------
| OCS+ goes low at some time, PWRON- is high,             |
| therefore REFONLYPWROFF- goes low.                      |
----------------------------------------------------------
                           |
----------------------------------------------------------
| LASTTHING- goes low (SH3,D9), REF+ is set high |
| (REFRESH CYCLE FF), DOREF+ high.                        |
----------------------------------------------------------
                           |
----------------------------------------------------------
| LASTTHING- going low forces READFF- and                 |
| WRITEFF- to go high, forcing IOINPROG+ low,            |
| forcing ALLOWIN+ high, ALLOWIN- low, (forcing          |
| HITIT+ low), setting CLOCKSTP- high.  Stay here|
| for approximately 5 microseconds until OCS+            |
| goes high, thus delay line taps will settle.           |
----------------------------------------------------------
                           |
----------------------------------------------------------
| OSC+ goes high, REFONLYPWROFF- goes high,              |
| setting REFOPSTART- low (since DOREF+ is high),|
| setting WRITEFF- low.                                   |
----------------------------------------------------------
                           |
----------------------------------------------------------
| Refresh cycle starts as usual, T200+ initial-           |
| izes T-reg Load Control FF, WRITEFF+ generates |
| INHIBITPE- and resets Parity Error FF.                 |
----------------------------------------------------------
                           |
```

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```
                                   |
     -------------------------------------------------------
     | State of controller determined, cycle termin-       |
     | ates in usual manner.  MBUSY FF reset, MBUSY-        |
     | goes high.                                           |
     -------------------------------------------------------
                                   |
     -------------------------------------------------------
     | Write Validate FF set by TST- in a write cycle      |
     | and reset by BREAD+ in a read cycle.  PWRON+        |
     | is initalized by PON+ (Power Sense FF clocked        |
     | by now existant refresh cycle FF pulses).            |
     -------------------------------------------------------
```
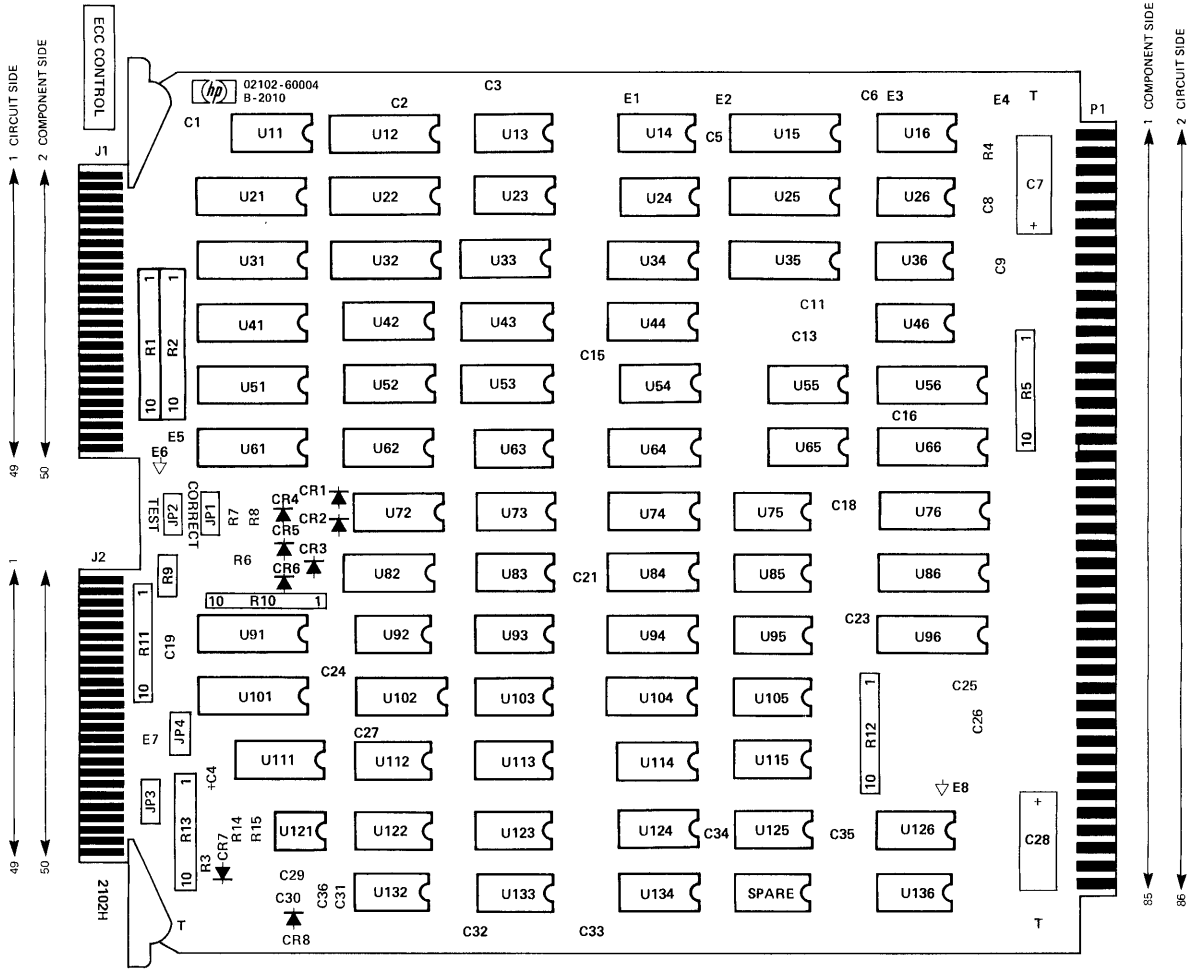
(HP 1000 M/E/F ERD)

ECC CONTROL

02102-60004
B-2010

1 CIRCUIT SIDE
2 COMPONENT SIDE

J1

49 50

J2

1

49 50

2102H

CORRECT
TEST

1 COMPONENT SIDE
2 CIRCUIT SIDE

P1

85 86

C1 C2 C3 E1 E2 C6 E3 E4 T

U11 U12 U13 U14 C5 U15 U16 R4
U21 U22 U23 U24 U25 U26 C8 C7 +
U31 U32 U33 U34 U35 U36 C9
U41 U42 U43 U44 C11 C13 U46
C15
U51 U52 U53 U54 U55 U56 R5
C16
E5 U61 U62 U63 U64 U65 U66
E6
R1 R2
10 10
R7 R8 CR4 CR1 U72 U73 U74 U75 C18 U76
JP2 CR5 CR2
R6 CR6 CR3
10 R10 1 U82 U83 C21 U84 U85 U86
R9
C19 U91 U92 U93 U94 U95 C23 U96
R11
10
C24 U101 U102 U103 U104 U105 C25
JP4 C27 R12 C26
E7 U111 U112 U113 U114 U115
JP3 +C4
R13 U121 U122 U123 U124 C34 U125 C35 U126
R3 CR7 R14 R15
10 C29
C30 C36 C31 U132 U133 U134 SPARE U136
CR8 C32 C33
+
C28
T T

2102H High Performance Fault Control Memory Assembly
02102-60004

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	C30	CAP 1000PF 5%		0160-0938		U	1
01 03	C3,5,8,9,12,13,15,17 C21-23,27,29,32-35	CAP .01UF		0160-2055		U	17
01 03	C1,2,6,10,11,14,16 C18-20,24-26,31	CAP 1.0UF 20%		0160-4892		D	14
01	C4	CAP 22UF 10%		0180-0228		D	1
01	C7,28	CAP 68UF 20%		0180-1835		D	2
01	E1-8	TERM-STUD SGL		0360-1682		U	8
01	R9	RES 330 5% .25		0683-3315		U	1
01	R6-8	RES 470 5% .25		0683-4715		D	3
01	R4	RES 2.87K 1%.125		0698-3151		D	1
01	R15	RES 4.22K 1%.125		0698-3154		D	1
01	R3	RES 46.4K 1%.125		0698-3162		D	1
01	R14	RES 12.1K 1%.125		0757-0444		D	1
		SOCKET PC SINGLE		1251-1556		U	8
		JMPR PLUG .3"C-C		1258-0124		U	4
		PIN GRV .062X.25		1480-0116		U	2
01	R1,2,11	NTWK RES 9X330		1810-0272		U	3
01	R10,12,13	NTWK RES 9X470		1810-0273		U	3

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	R5	NTWK RES 9X4.7K		1810-0279		U	1
01	U72	IC DIGITAL D		1813-0086		U	1
01	U111	IC DIGITAL		1813-0122		U	1
01	U102	IC SN74S112N		1820-0629		U	1
01	U16,24,63,105	IC SN74S00N		1820-0681		U	4
01	U46,115,134	IC SN74S04N		1820-0683		U	3
01	U73,132,136	IC SN74S10N		1820-0685		U	3
01	U14,23,92,103,133	IC SN74S74N		1820-0693		U	5
01	U54,55,65,75,85	IC SN74S86N		1820-0694		U	5
01	U82	IC SN74S174N		1820-1076		U	1
01	U95	IC SN74LS74N		1820-1112		U	1
01	U94	IC SN74S133N		1820-1130		U	1
01	U125	IC SN74LS02N		1820-1144		U	1
01	U112	IC SN74S51N		1820-1158		U	1
01	U124	IC SN74LS04N		1820-1199		U	1
01	U44,64,74,84	IC SN74S138N		1820-1240		U	4
01	U104	IC SN74LS153N		1820-1244		U	1
01	U26,36,113,126	IC SN74S02N		1820-1322		U	4
01		IC SN74S08N		1820-1367		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	U123			1820-1367			
01	U122	IC SN74LS14N		1820-1416		U	1
01	U114	IC SN74S32N		1820-1449		U	1
01	U83,93	IC SN74S37N		1820-1450		U	2
01	U13	IC SN74S38N		1820-1451		U	1
01	U11	IC SN74393 N		1820-1464		U	1
01 03	U25,31,51,56,76,86 U96	ICSN74S241N		1820-1624		U	7
01	U15,21,91	IC SN74S240N		1820-1633		U	3
01 03	U12,22,32,35,41,61 U66,101	IC SN74S373N		1820-1676		U	8
01 03	U33,34,42,43,52,53, U62	IC AM93S48PC		1820-1968		U	7
01	U121	IC NE555V		1826-0355		U	1
01	CR7	DIODE 1N5817		1901-1080		D	1
01	CR4,5,6,8	DIODE-LIGHT EMIT		1990-0486		U	4
01	CR1,2,3	LED-VISIBLE		1990-0487		U	3
		EXTRACTOR-PC GRY		5040-6006		W	2

High Speed FC Mem Controller schematic — HEWLETT PACKARD, TITLE: HIGH SPEED FC MEM CONTROLLER, NEXT ASSEMBLY: 2102H, PART NUMBER: D-02102-60004-51, SHEET 1 OF 1

HIGH SPEED FC MEM CONTROLLER

2102H

HEWLETT PACKARD

NEXT ASSEMBLY 2102H

PART NUMBER 02102-60004

D-02102-60004-53

ERROR CORRECTION AND DETECTION

The ECC option is a 22-bit, distance four code, which is physically a 21-bit hamming code (16 data bits, 5 check bits) plus an overall (even) parity bit. Under jumper selection, the following protocols may be chosen:

JUMPER "IN"

Corrects single-bit errors; issues a "Parity Error" to the CPU if a double (or greater) bit error occurs.

JUMPER "OUT"

Issues a "Parity Error" to the CPU if single bit errors occur.

"IN" is the normal operating position, however "OUT" is required for periodic maintenance, and is desirable also for extremely fault-secure applications programming. All hard and soft failures of up to two bits within a word are detected, including single and double cell and chip failures. Up to ᨆ5% (best case) of the array rams may fail without degrading the CPU or halting. Many multiple (3 or more) faults are also detected.

ECC CODE

This particular hamming code has been chosen to minimize parity generator fan-in, so that the utmost in speed of code generation and correction may be attained. Numbering the data bits as 0 through 15 in the usual way, the six check bits are as follows:

$$P20 = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_8$$

$$P19 = D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12}$$

$$P18 = D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{13} \oplus D_{14}$$

$$P17 = D_0 \oplus D_2 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15}$$

$$P16 = D_0 \oplus D_3 \oplus D_6 \oplus D_7 \oplus D_8 \oplus D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$$

$$P21 = D_4 \oplus D_8 \oplus D_{11} \oplus D_{14} \oplus D_{15} \qquad \text{NOTE: } \oplus = \text{"EXCLUSIVE OR"}$$

In this code, P16 through P20 may be generated and checked via single
9-input parity generators. P21 is the overall parity bit, and <u>requires</u>
only a 5-input parity generator to form. If each data bit is included
an even number of times in the check equations P16 through P20, the parity
of the data bits plus P16 through P20 would be even. Therefore if P21
is the even parity of those data bits which <u>are</u> included an even number of
times, the parity of D0 through D15 plus P16 through P21 must be even.
Thus for code generation, P21 may be quickly formed. For checking operations,
a 22-bit parity check must be generated or else single-bit errors would
sometimes be decoded as double-bit errors.

ECC STORAGE

The data bits are stored in the normal way in the 8K or 16K array boards,
while P16 is stored in the array boards in the location formerly occupied
by the ordinary parity bit. The P17 through P21 check bits of up to 256K
words of data are condensed onto a single check-bit board. Hence a 256K ECC
memory system would consist of an ECC controller board, 16 16K array boards
(or 32 8K array boards), and one 256K x 5 bit check bits board. Thus a check
bit board must be included for <u>each</u> 256K words of main memory, assuming 16K
rams for the check bits array.

SYNDROME LATCH

A six-bit register latches the error detection logic's syndrome
and displays the result in six LEDS mounted on the board. The
latch is tested (as well as the LEDs) by bringing CLRPERR- low on
J2. This lights all six LEDS. The detection logic clocks the latch
whenever a "Parity Error" signal is sent to the CPU. Thus an
error in a word that is fetched, for example, as the first word
in a multiple-fetch instruction will be <u>held</u> in the latch. The
64 possible syndromes and their meanings are interpreted by first
reading the yellow LEDS, from left to right, looking at them from J1,
component side up. This yields the "yellow digit", an octal number.
Similarly, the "red digit" is obtained from the red LEDS.

YELLOW DIGIT	RED DIGIT	ERROR DETECTED
X	1	Double (or greater) error
X	3	Double (or greater) error
X	5	Double (or greater) error
7	7	No errors, all bits good
0	0	Bit 0
1	0	Triple or greater
2	0	Triple or greater
3	0	Bit 1
4	0	Triple or greater
5	0	Bit 2
6	0	Bit 3
7	0	Bit 4
0	2	Triple or greater
1	2	Bit 5
2	2	Bit 6
3	2	Triple or greater
4	2	Bit 7
5	2	Triple or greater
6	2	Bit 8
7	2	Bit 20
0	4	Triple or greater
1	4	Bit 9
2	4	Bit 10
3	4	Bit 11
4	4	Bit 12
5	4	Triple or greater
6	4	Triple or greater
7	4	Bit 19
0	6	Bit 13
1	6	Bit 14
2	6	Triple or greater
3	6	Bit 18
4	6	Bit 15
5	6	Bit 17
6	6	Bit 16
7	6	Bit 21

YELLOW DIGIT	RED DIGIT	ERROR DETECTED
0	7	Double (or greater) error
1	7	Double (or greater) error
2	7	Double (or greater) error
3	7	Double (or greater) error
4	7	Double (or greater) error
5	7	Double (or greater) error
6	7	Double (or greater) error

MEMORY ARRAY
MODULES

1 CIRCUIT SIDE
2 COMPONENT SIDE

1 CIRCUIT SIDE
2 COMP SIDE

E1

C3 C4 C5 C52 C6 C53 C7

C2

U12

C8

U31

C1

U51

C13 C14

U61 U62

W3

U81 U82

R25 R17 R5 R6 C22

XWI

C27 R7

R8

U121 U122

C32 C33 C58

U131 U132

C36 R10 R11

C37

U152

R24 CR2 R4

U171 U172

E4 E2 E3

E5

C10

C57

C18

C23

C28

C30

C38

C40

C42 C43

C44

U25 C9

C11 U36 C12

C56 U45 + C48

C15 U56

C16 U65 C17

C19 U76 + C49

C20 U85 C21

C24 U96 C50 +

C25 U105 C26

C29 U116

C30 C31

C34 U136 CR1 C51 +

U145 C35 CR3 R15

C39 U156 R14 R13 C47

C40 U165 C41

C45 C54 C46

U16

C45 C54 C46 R13 C47

1 2

49 50

49 50

1 2

85 86

12994A 8KB Memory Module Assembly
5060-8369

IIF -1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER.
1 3	C3,5-8,13,32, 43-47,52-54,55	CAP 1.0UF 20%		0160-0127			16
1 3 5	C1,2,4,9-12,14-31 33-35,38-42,56-60 56-60	CAP .01UF		0160-2055			38
1	C36,37	CAP 820PF 5%		0160-3539			2
1	C48-51	CAP 68UF 20%		0180-1835			4
	E1-6	STUD SOLDER TERM		0360-0294			6
1	R10,11,17	RES 1000 5% .25		0683-1025			3
1	R5,6,24	RES 10K 5% .25		0683-1035			3
	R4	RES 270 5% .25		0683-2715			1
	R14	RES 560 5% .25		0683-5615			1
	R7,8	RES 17.8 1% .5		0698-3389			2
	R15	RES 383 1% .50		0698-3404			1
	XW1	SOCKET 16 DIP LO		1200-0482			1
	A-H	JMPR PLUG .3"C-C		1258-0124			8
		PIN GRV .062X.25		1480-0116			2
	R25	RES NET 7X1K		1810-0030			3
	U172	IC		1820-0683			1
	U171	IC		1820-0686			1
1	U61,81	IC		1820-1073			2
1 3	U12,62,82,122, 152	IC		1820-1081			5
	U131	IC		1820-1158			1
	U132	IC		1820-1288			1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
1	U31,51,121	IC		1820-1477			3
	CR3	DIODE SIL		1901-0040			1
	CR2	DIODE		1901-1080			1
	CR1	DIODE BD		1902-3104			1
	W2,3	WIRE JUMPERS		8159-0005			2
		EXTRACTOR-PC		5040-6006			1
		EXTRACTOR-PC		5040-6075			1
		4K RAM 22PIN HR		5080-9785			17

BITS (0:16)

CLOCK DRIVERS

ROW 0

BUS DRIVERS RECEIVERS

+5V MEM

U172E CLK

U172D U171B

R9 1K

U172C MREF

U171C

U131B C36 820PF

+12V MEM

R11 1K U132 R8 17.8

ENABLE

CLK J1-43
MREF J1-49
R/W WR J1-47
R/W RR J1-48
A12 J1-5

U121

+5V MEM

U172A A12

A12

U131A C37 820PF

R5 10K

R7 17.8 (C) (AB) ROW 0 ARRAYS

R6 10K

R10 1K

R17 1K +5V U81A W3

R25A U81D

+5V R25B U61A

R25C U61D

R25D U61B

R25E U81B

R25F U81C

R25G U61C

A13 J1-7
A14 J1-9
A15 J1-11
A16 J1-13
A17 J1-15
A18 J1-19
A19 J1-21

REFRESH ADDRESSES

A0 J1-4
A1 J1-6
A2 J1-8
A3 J1-10
A4 J1-12
A5 J1-14

A6 J1-16
A7 J1-18
A8 J1-20
A9 J1-22
A10 J1-1
A11 J1-3

XW1

+5V MEM R4 270

+5V MEM R3 1K

ENABLE

U51

+5V MEM

R1G R1F R1E R16G R1D

(F) (A9) ROW 0 ARRAYS

R16F R16E R16D

+5V MEM

+12V MEM P1-43,44

VDD MEM

C50 68UF

C3,5-7, 32,44-47 1UF

-12V MEM P1-69,70

R15 383 CR1 R14 560 C51 68UF C43,52 53,54 1UF -3V MEM

+5V P1-39,40

C49 68UF C8 1UF C1,14 22,33,42 0.01UF +5V

+5V MEM P1-29,30

C48 68UF C13 1UF C2,4,9-12,15-21, 23-31,34,35,38-41 0.01UF +5V MEM

CS J1-45

+5V R2 1K

ENABLE

U31

R1C R16B R16A R16G

R12 R1C R1B R1A

+5V MEM

(E) (AB) ROW 0 ARRAYS

RACLO P1-65
RACLO P1-66

VDD TURN ON

+12V MEM

J1-2,11,23,24, 42,44,46,50
COM TP2
COM P1-1,2,85,86 TP3

CR2

R24 10K

VDD TO PIN 18 ALL ARRAYS (C8)

NOTES:
1. UNLESS OTHERWISE SPECIFIED, ALL RESISTANCE VALUES ARE IN OHMS AND ARE 1/4W, 5% CARB COMP.
2. RESISTOR NETWORKS R1,R16 AND R25 ARE 1K.

MEMORY MODULE	JUMPER POSITIONS (XW1)								W3
	A	B	C	D	E	F	G	H	
0-4K	IN	IN	IN	IN	IN	IN	IN	IN	IN
8K-12K	IN	OUT	IN	IN	IN	IN	IN	IN	IN

TYPICAL (B6) (F5) (C5)
OF ROW 1 (C) (F) (D)
ARRAYS

CLOCK SELECT READ/ WRITE (I/O)

U16 Dout

(A4) (A)

-3V MEM
+5V MEM VDD (G4)

U12 J1-26 MDS0
J1-28 MDS1
J1-30 MDS2
J1-32 MDS3

REC TRANS ENABLE ENABLE

D IN U25 Dout
D IN U36 Dout
D IN U45 Dout
D IN U56 Dout
D IN U65 Dout
D IN U76 Dout
D IN U85 Dout
D IN U96 Dout
D IN U105 Dout
D IN U116 Dout
D IN U125 Dout
D IN U136 Dout
D IN U145 Dout
D IN U156 Dout
D IN U165 Dout
D IN U176 Dout

U62 J1-34 MDS4
J1-36 MDS5
J1-38 MDS6
J1-40 MDS7

REC TRANS ENABLE ENABLE

U82 J1-25 MDS8
J1-27 MDS9
J1-29 MDS10

REC TRANS ENABLE ENABLE

U122 J1-31 MDS11
J1-33 MDS12
J1-35 MDS13

REC TRANS ENABLE ENABLE

U152 J1-37 MDS14
J1-39 MDS15
J1-41 MDS16

REC TRANS ENABLE ENABLE

MEMORY ARRAYS (RAMS)

REV	REFERENCE	SERIES/PREFIX
A	ORIG.	1353
B	22-2220	1422
C	ERRATA	NO CHANGE
D	22-2363	1422
E	22-2561	1512
F	22-2684	1523
G	22-3083	1540

4K MEMORY MODULE
5060-8369-51

HEWLETT-PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

IIF -5/-6
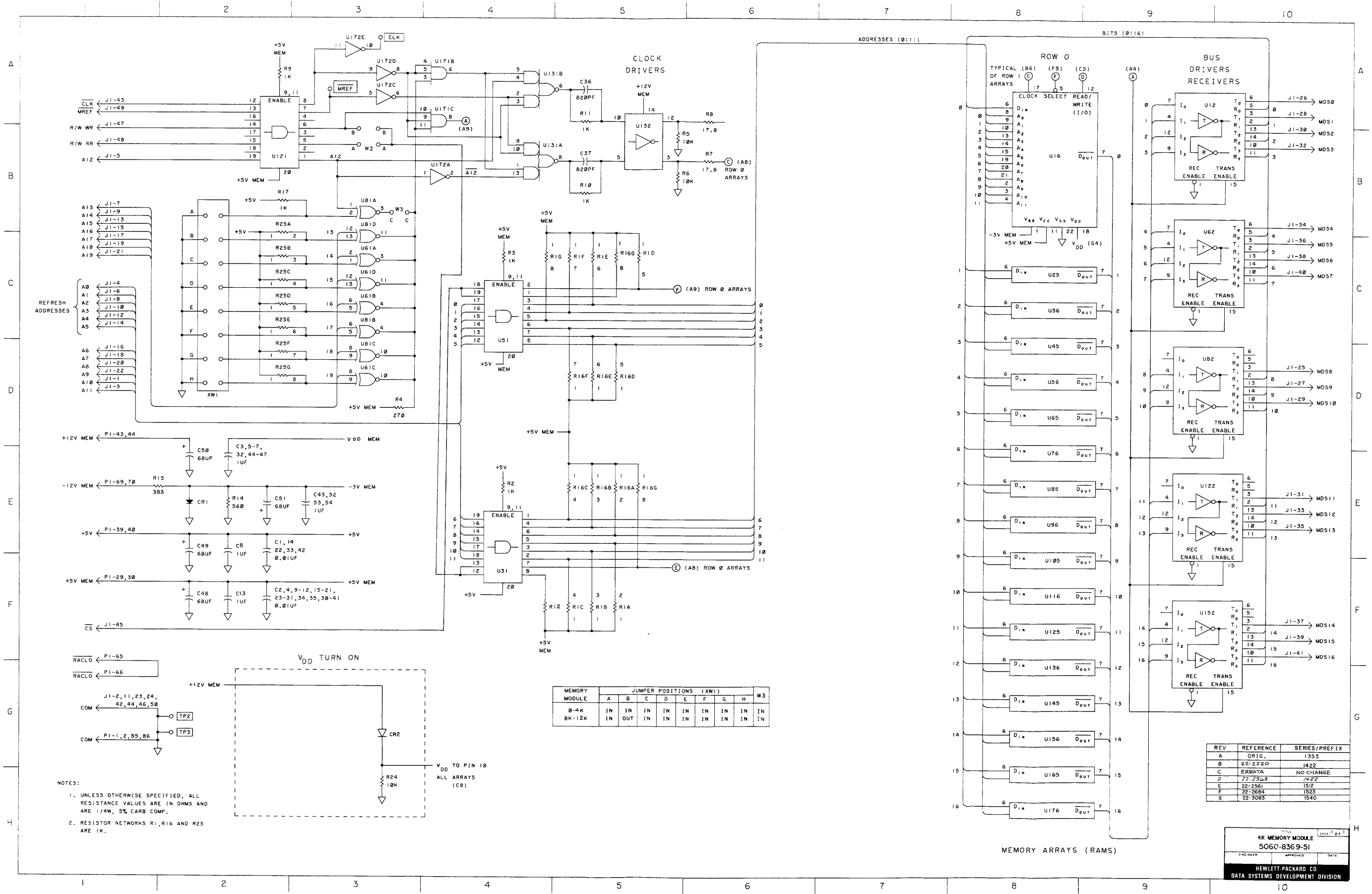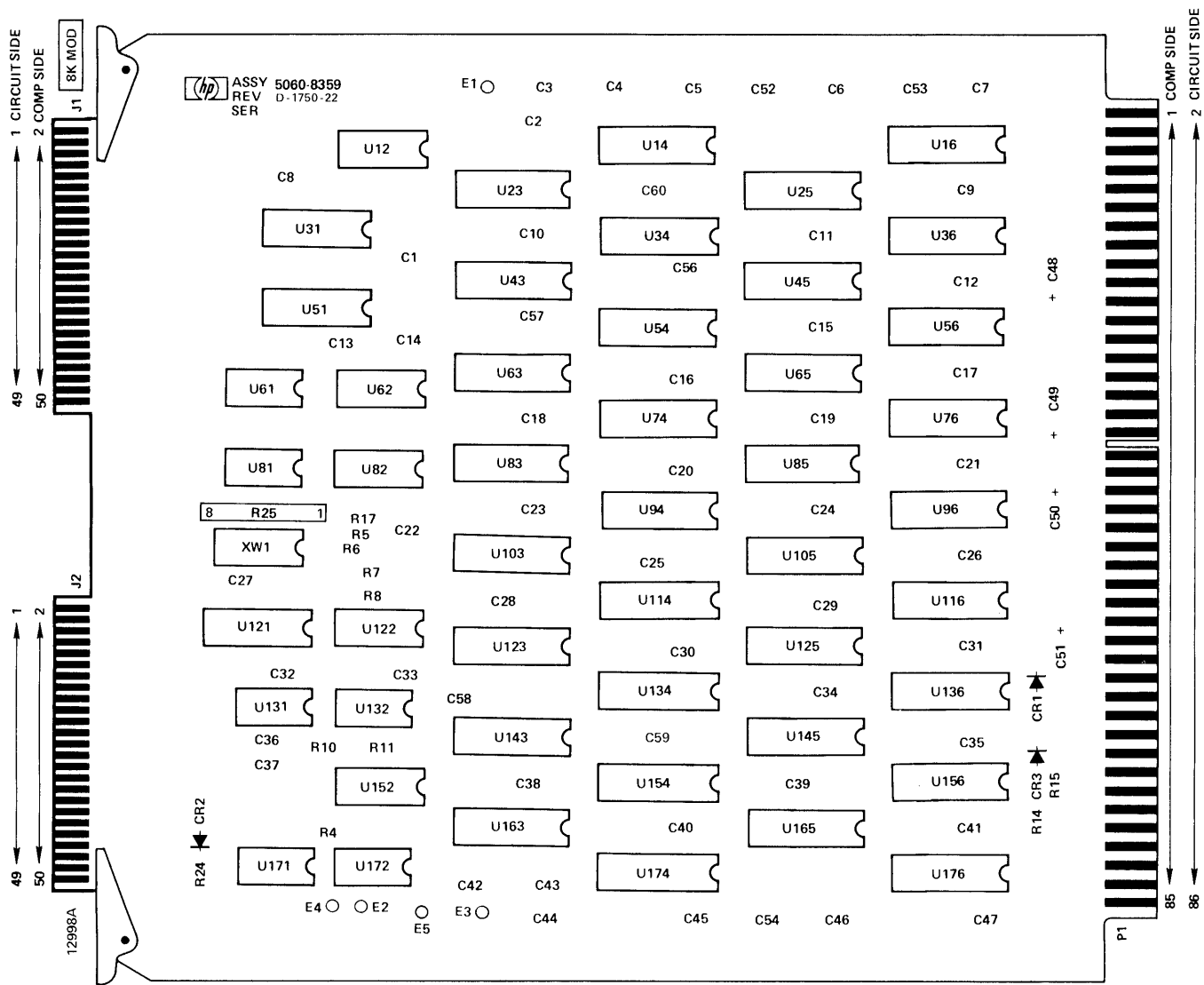
12998A 16KB Memory Module Assembly
5060-8359

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
13	C3,5-8,13,32 43-47,52-54,55	CAP 1.0UF 20%		0160-0127			16
13	C1,2,4,9-12,14-31 33-35,38-42,56-60	CAP .01UF		0160-2055			38
	C36,37	CAP 820PF 5%		0160-3539			2
	C48-51	CAP 68UF 20%		0180-1835			4
	E1-6	STUD SOLDER TERM		0360-0294			6
1	R10,11,17	RES 1000 5% .25		0683-1025			3
1	R5,6,24	RES 10K 5% .25		0683-1035			3
	R4	RES 270 5% .25		0683-2715			1
	R14	RES 560 5% .25		0683-5615			1
	R7,8	RES 17.8 1% .5		0698-3389			2
	R15	RES 383 1% .50		0698-3404			1
	XW1	SOCKET 16 DIP LO		1200-0482			1
	A-H	JMPR PLUG .3"C-C		1258-0124			8
		PIN GRV .062X.25		1480-0116			2
	R25	RES NET 7X1K		1810-0030			1
	U172	IC		1820-0683			1
	U171	IC		1820-0686			1
	U61,81	IC		1820-1073			2
13	U12,62,82,122, 152	IC		1820-1081			5
	U131	IC		1820-1158			1
	U132	IC		1820-1288			1
1	U31,51,121	IC 8T95B		1820-1477			3

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
	CR3	DIODE SIL		1901-0040			1
	CR2	DIODE		1901-1080			1
	CR1	DIODE BC		1902-3104			1
	W2	WIRE JUMPERS		8159-0005			1
		EXTRACTOR-PC		5040-6006			1
		EXTRACTOR-PC		5040-6075			1
1 3 5 7 9 11 13	U14,16,23,25,34,36, 43,45,54,56,63,65, 74,76,83,85,94,96, 103,105,114,116,123 125,134,136,143,145 154,156,163,165,174 176	4K RAM 22PIN HR		5080-9785			34

8K MEMORY MODULE
5060-8359-51

HEWLETT PACKARD CO
DATA SYSTEMS DEVELOPMENT DIVISION

IIF -11/-12

ASSY 5061-1332
REV B-2011

1 CIRCUIT SIDE
2 COMPONENT SIDE

J1

49
50

1
2

49
50

J2

C23

C24

1 COMPONENT SIDE
2 CIRCUIT SIDE

P1

85
86

E1   C3
U11 U12 XW1   R5 U13   R7 C2 R8 U14 U15   C4
          R4   R6   R9
E2 U10   C5   C6
      C1 R1   R10
      E3 R2   R11
          R3
   U16 U17   E4   C9   U18 U19 U20 U21 C13 C14
                   CR1 CR2 C7   R12 R13 R14 R15 R16   R17 R18 R19
                   C8   C10   C15
   C16 U22 U23 U24 C17 C11 U25 C19 U26 R33 R34 R35 R36 U27 C22
   R20 R21 R22 R23 C18   R29   R31 R32   C20   C21
             R24 R26 C12 R30
             R25 R27 R28

U28 U29 U30 U31 U32 U33 U34 U35 U36 U37 U38 U39 U40 U41 U42 U43 U44

U45 U46 U47 U48 U49 U50 U51 U52 U53 U54 U55 U56 U57 U58 U59 U60 U61

CR3

U62 U63 U64 U65 U66 U67 U68 U69 U70 U71 U72 U73 U74 U75 U76 U77 U78

U79 U80 U81 U82 U83 U84 U85 U86 U87 U88 U89 U90 U91 U92 U93 U94 U95

C25 C26   C28   C29   C30   C32
                               C31   CR4
E5   E6   C27   R37

13187A 32KB Memory Module Assembly
5061-1332

IIF -13

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
11 03 05 07 09	C14,16-21,23,25,26 28-30,32,33,35,37, 39,41,43,45,46,48, 50,52,54,56,57,59, 61,63,65,67,69	CAP 1.0UF 20%		0160-0127		U	34
01	C1,7-12,15	CAP .01UF		0160-2055		U	8
01	C2-4,13	CAP 620PF 5%		0160-3536		U	4
00	C31	CAP 56UF 6VDC		0180-0548		U	1
01	C5,6,22,24	CAP 68UF 20%		0180-1835		U	4
00	E1-6	STUD SOLDER TERM		0360-0294		U	6
00	R37	RES 464 1% .50		0698-0090		U	1
00	R1	RES 261 1%.125		0698-3132		U	1
01	R12,18,19,33	RES 19.6 1%.125		0698-3429		U	4
01	R16,20-32,34-36	RES 1.78K 1%.125		0757-0278		U	17
01	R3,9,14,17	RES 1K 1%.125		0757-0280		U	4
00	R39	RES 750 1%.125		0757-0420		U	1
01	R2-7,10,11,13,15	RES 10K 1%.125		0757-0442		U	10
		SOCKET 14 DIP LO		1200-0483		U	1
		IMPR PLUG .3"C-C		1258-0124		U	7
		PIN GRV .062X.25		1480-0116		U	2
		IC SN74S00N		1820-0681		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	U18,19	PART NO CONT		1820-0681			
01	U20,21	IC SN74S10N		1820-0685		U	2
01	U11,12	IC N82S42A		1820-1073		U	2
01	U14,15	IC MM40026CL		1820-1288		U	2
00	U13	IC P2550A		1820-1338		U	1
01	U17,23,25,27	IC PT96P		1820-1476		U	4
01	U10,16,22,24,26	IC PT95B		1820-1477		U	5
01	CR1,2	DIODE SILICON		1901-0539		U	2
00	CR3	DIODE 1N5817		1901-1080		U	1
01	CR4	DIODE-ZNR 4.99V		1902-3092		U	1
		EXTRACTOR-PC		5040-6006		W	1
		EXTRACTOR-PC		5040-6075		W	1
		BOARD-ETCHED		5080-9776		W	1
01	U28-95	4K RAM-18PIN CER		5080-9781		3	68

MEMORY MODULE
TI TMS 4050
TITLE
13187A
NEXT ASSEMBLY

HEWLETT PACKARD

PART NUMBER
C-5061-1332-51

IIF-17/-18
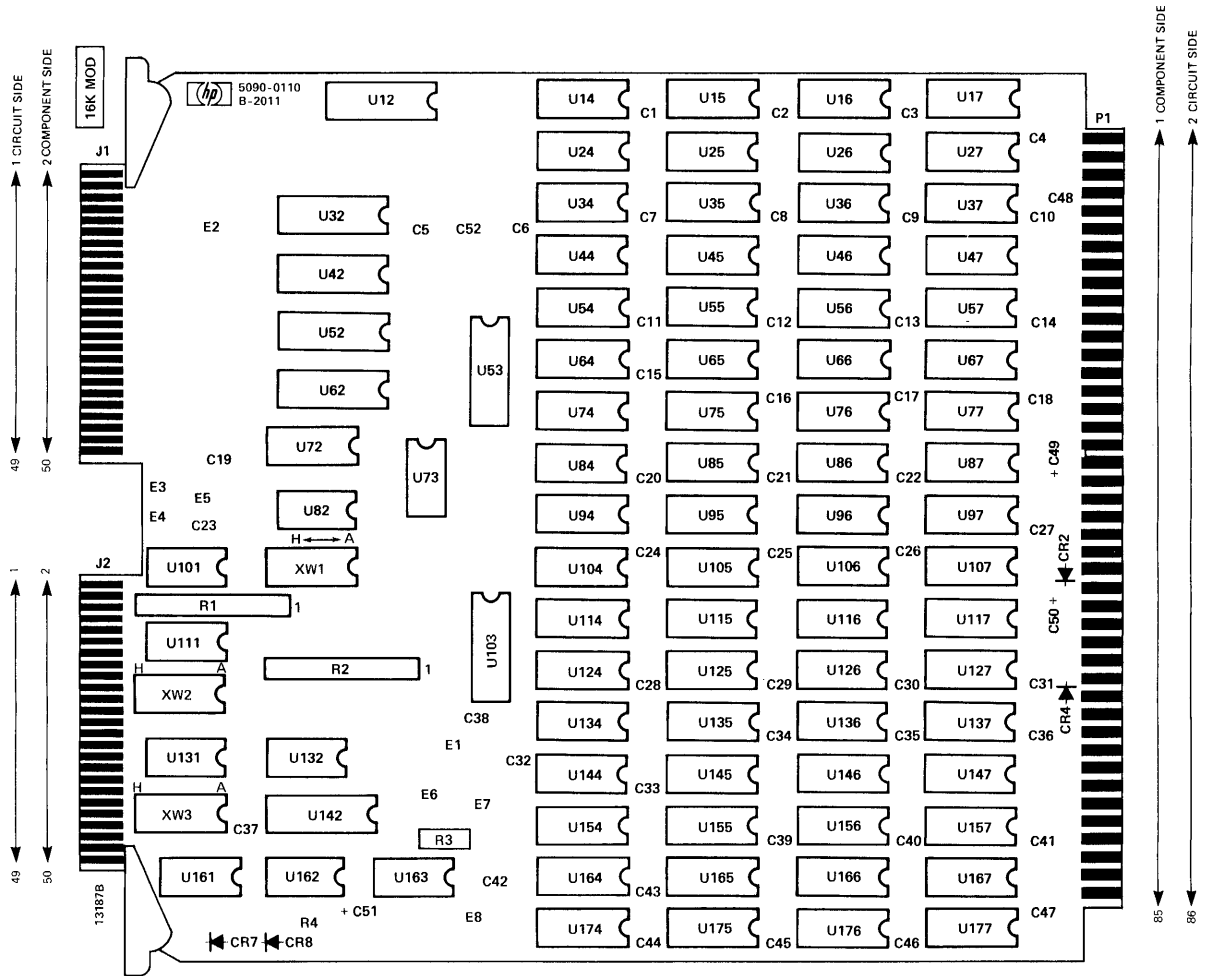
13187B 32KB Memory Module Assembly
13187-60001

ITEM NO	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	C1-47,52	CAP 1.0UF 20%		0160-4892		U	48
00	C50	CAP 22UF 10%		0180-0228		D	1
01	C48,49	CAP 56UF 6VDC		0180-0548		U	2
00	C51	CAP 68UF 20%		0180-1835		D	1
01	F1-8	TERM-STUD SGL		0360-1682		U	8
00	R4	RES 464 1% .50		0698-0090		U	1
00	R3	RES 237 1%.125		0698-3442		U	1
00	XW1	SOCKET 16 DIP LO		1200-0482		U	1
00	W1-7	JMPR PLUG .3"C-C		1258-0124		U	7
		PIN GRV .062X.25		1480-0116		U	2
00	R1,2	NTWK RES 9X4.7K		1810-0279		U	2
01	U132	IC DIGITAL		1813-0176		U	1
00	U131	IC SN74S00N		1820-0681		U	1
01	U161,163	IC SN74S10N		1820-0685		U	2
00	U72	IC SN74S158N		1820-1015		U	1
01	U101,111	IC N82S42A		1820-1073		U	2
00	U162	IC SN74S02N		1820-1322		U	1
		IC 82S50A		1820-1338		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
00	U82			1820-1338			
00	U73	IC SN74S37N		1820-1450		U	1
01	U42,53,62,83,142	IC SN74S240N		1820-1633		U	5
01	U12,32,52	IC SN74LS241N		1820-1918		U	3
00	CR8	DIODE 1N2071		1901-0029		D	1
00	CR2,4	DIODE 1N5817		1901-1080		D	2
00	CR7	DIO-ZNR 5.62V 2%		1902-3105		D	1
		LABEL-WARNING		7120-6492		U	1
00	W8-13	WIRE JUMPERS		8159-0005		D	6
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
01 03 05 07 09 11 13	U14-17,24-27,34-37, 44-47,54-57,64-67, 74-77,84-87,94-97, 104-107,114-117, 124-127,134-137, 144-147,154-157, 164-167,174-177	STRESD 1818-0334		5090-0109		3	68
		BOARD-ETCHED		5090-0110		1	1
		PS SEQUENCER		ET13480		1	0

16-PIN, 4K RAM MEMORY MODULE
SCHEMATIC DIAGRAM
HEWLETT-PACKARD
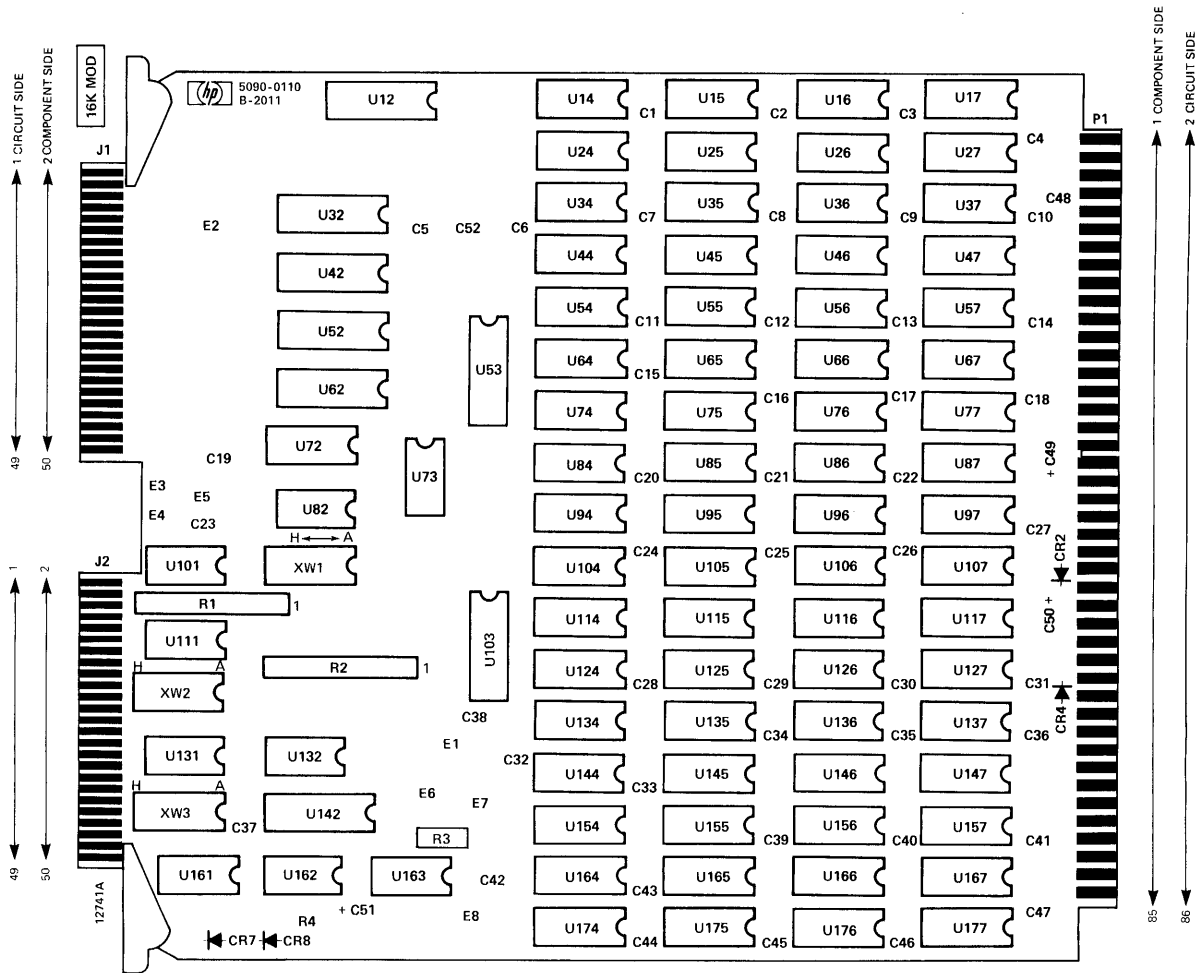
12741A 32KB High Performance Assembly
12741-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	C1-47,52	CAP 1.0UF 20%		0160-4892		U	48
00	C50	CAP 22UF 10%		0180-0228		D	1
01	C48,49	CAP 56UF 6VDC		0180-0548		U	2
00	C51	CAP 68UF 20%		0180-1835		D	1
00	E1-8	TERM-STUD SGL		0360-1682		U	8
00	R4	RES 464 1% .50		0698-0090		U	1
00	R3	RES 237 1%.125		0698-3442		U	1
00	XW1	SOCKET 16 DIP LU		1200-0482		U	1
00	W1-6	JMPR PLUG .3"C-C		1258-0124		U	6
		PIN GRV .062X.25		1480-0116		U	2
00	P1,2	NTWK RES 9X4.7K		1810-0279		U	2
01	U132	IC DIGITAL		1813-0176		U	1
00	U131	IC SN74S00N		1820-0681		U	1
01	U161,163	IC SN74S10N		1820-0685		U	2
00	U72	IC SN74S158N		1820-1015		U	1
01	U101,111	IC N82S42A		1820-1073		U	2
00	U162	IC SN74S02N		1820-1322		U	1
		IC 82S50A		1820-1338		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
00	U82			1820-1338			
00	U73	IC SN74S37N		1820-1450		U	1
01	U42,53,62,83,142	IC SN74S240N		1820-1633		U	5
01	U12,32,52	IC SN74LS241N		1820-1918		U	3
01	CR8	DIODE 1N2071		1901-0029		D	1
00	CR2,4	DIODE 1N5817		1901-1080		D	2
00	CR7	DIO-ZNR 5.62V 2%		1902-3105		D	1
		LABEL-WARNING		7120-6492		U	1
00	W7-12	WIRE JUMPERS		8159-0005		D	6
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
01 03 05 07 08 09 11 13	U14-17,24-27,34-37, 44-47,54-57,64-67, 74-77,84-87,94-97, 104-107,114-117, 124-127 134-137,144-147, 154-157,164-167, 174-177	4K RAM-16PIN CER		5090-0108		3	68
		BOARD-ETCHED		5090-0110		1	1
		PS SEQUENCER		ET13480		1	0

16-PIN, 16K RAM MEMORY MODULE SCHEMATIC

HEWLETT PACKARD
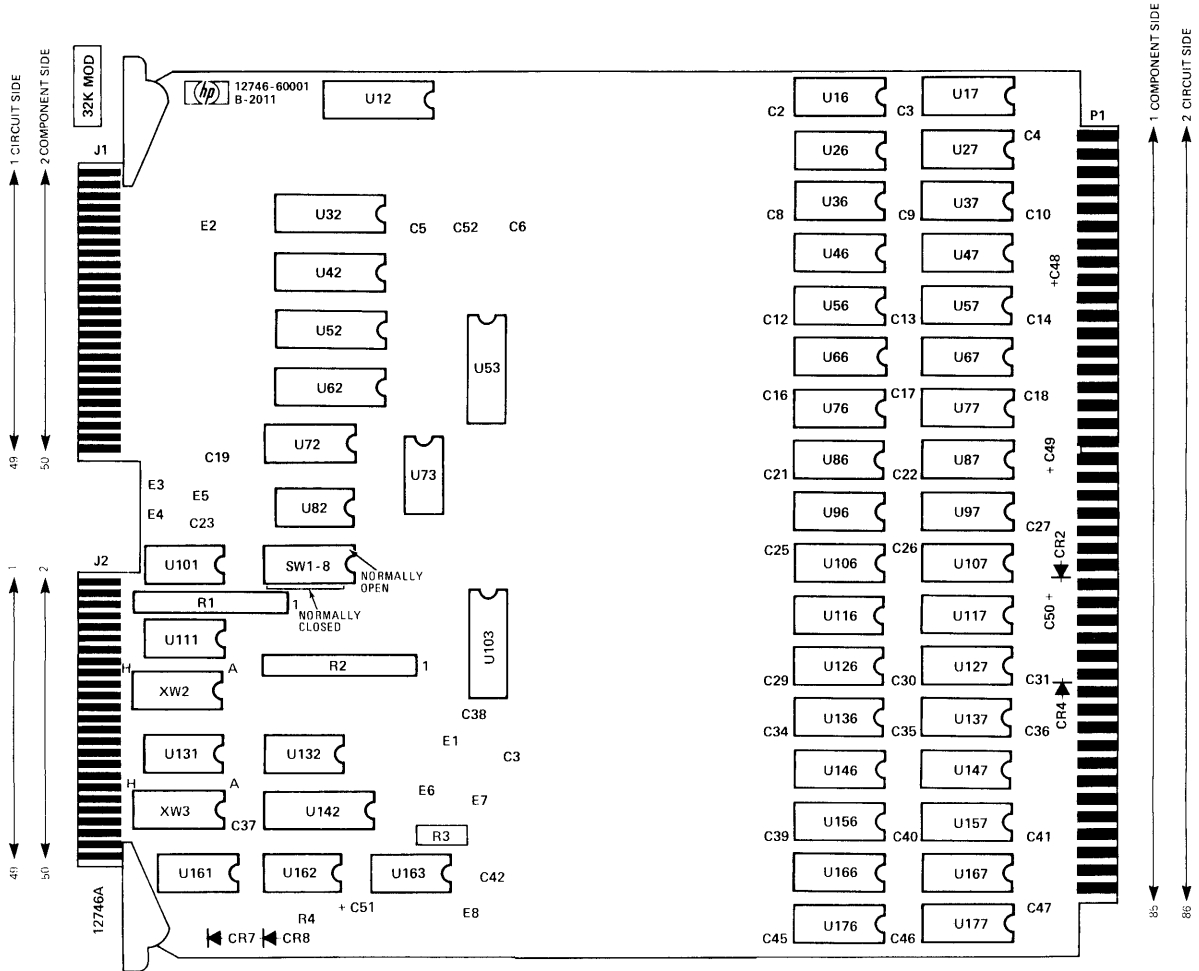
12746A Memory Module Assembly
12746-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01 03 05	C2-6,8-10,12-14 16-19,21-23,25-27, 29-32,34-42,45-47,52	CAP 1.0UF 20%		0160-4892		U	38
00	C51	CAP 68UF 20%		0180-1835		D	1
01	E1-8	TERM-STUD SGL		0360-1682		U	8
00	R4	RES 464 1% .50		0698-0090		U	1
		PIN GRV .062X.25		1480-0116		U	2
00	R1,2	NTWK RES 9X4.7K		1810-0279		U	2
01	U132	IC DIGITAL		1813-0176		U	1
00	U131	IC SN74S00N		1820-0681		U	1
01	U161,163	IC SN74S10N		1820-0685		U	2
00	U72	IC SN74S158N		1820-1015		U	1
01	U101,111	IC N82S42A		1820-1073		U	2
00	U162	IC SN74S02N		1820-1322		U	1
00	U82	IC 82S50A		1820-1338		U	1
00	U73	IC SN74S37N		1820-1450		U	1
01	U42,53,62,103,142	IC SN74S240N		1820-1633		U	5
01	U12,32,52	IC SN74LS241N		1820-1918		U	3
		SW DIP 8 ROCKER		3101-2243		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
		LABEL-WARNING		7120-6492		U	1
01	W8-11	WIRE JUMPERS		8159-0005		D	4
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
		BOARD-ETCHED		5090-0110		1	1
01 03 05 07 09 11 13	U16,17,26,27,36,37, 46,47,56,57,66,67, 76,77,86,87,96,97, 106,107,116,117,126 127,136,137,146,147 156,157,166,167,176 177	STRESD 1818-0340		5180-0601		3	34
		ASSY-COMP SEQ		12746-64001		A	1
		PS SEQUENCER		ET13480		1	0

IIF -33
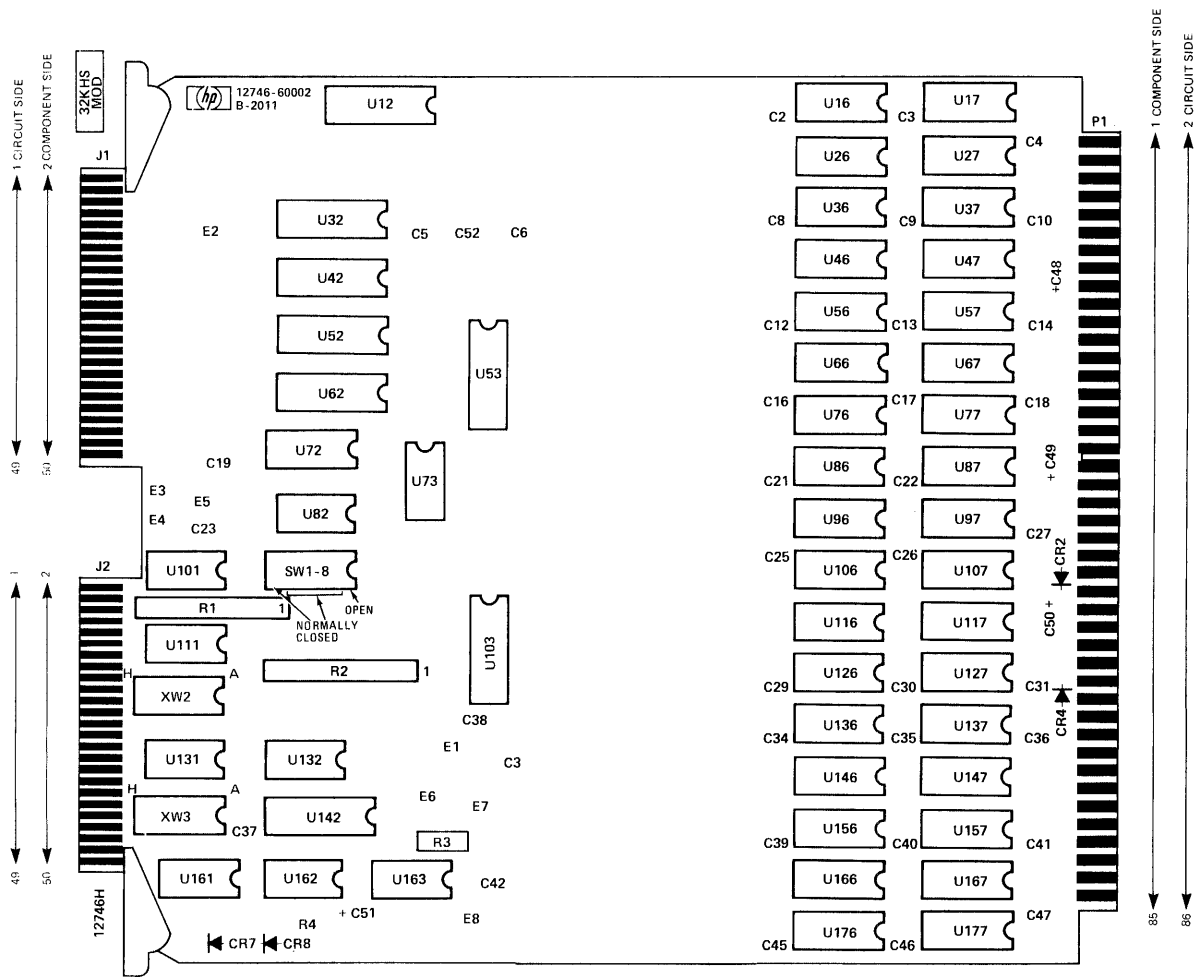
12746H Memory Module Assembly
12746-60002

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01 03 05	C2-6,8-10,12-14,16-19 21-23,25-27,29-32, 34-42,45-47,52	CAP 1.0UF 20%		0160-4892		U	38
01	C51	CAP 68UF 20%		0180-1835		D	1
01	F1-8	TERM-STUD SGL		0360-1682		U	8
01	R4	RES 464 1% .50		0698-0090		U	1
		PIN GRV .062X.25		1480-0116		U	2
01	P1,2	NTWK RES 9X4.7K		1810-0279		U	2
01	U132	IC DIGITAL		1813-0176		U	1
01	U131	IC SN74S00N		1820-0681		U	1
01	U161,163	IC SN74S10N		1820-0685		U	2
01	U72	IC SN74S158N		1820-1015		U	1
01	U101,111	IC N82S42A		1820-1073		U	2
01	U162	IC SN74S02N		1820-1322		U	1
01	U82	IC 82S50A		1820-1338		U	1
01	U73	IC SN74S37N		1820-1450		U	1
01	U42,53,62,103,142	IC SN74S240N		1820-1633		U	5
01	U12,32,52	IC SN74LS241N		1820-1918		U	3
		SW DIP 8 ROCKER		3101-2243		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
		LABEL-WARNING		7120-6492		U	1
0 1	W7-10	WIRE JUMPERS		8159-0005		D	4
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
		BOARD-ETCHED		5090-0110		1	1
0 1 0 3 0 5 0 7 0 9 1 1 1 3	U16,17,26,27,36,37 U46,47,56,57,66,67 U76,77,86,87,96,97 U106,107,116,117,126 U127,136,137,146,147 U156,157,166,167,176 U177	STRESD 1818-0509		5180-0601		3	34
		ASSY-COMP SEQ		12746-64002		A	1
		PS SEQUENCER		ET13480		1	0
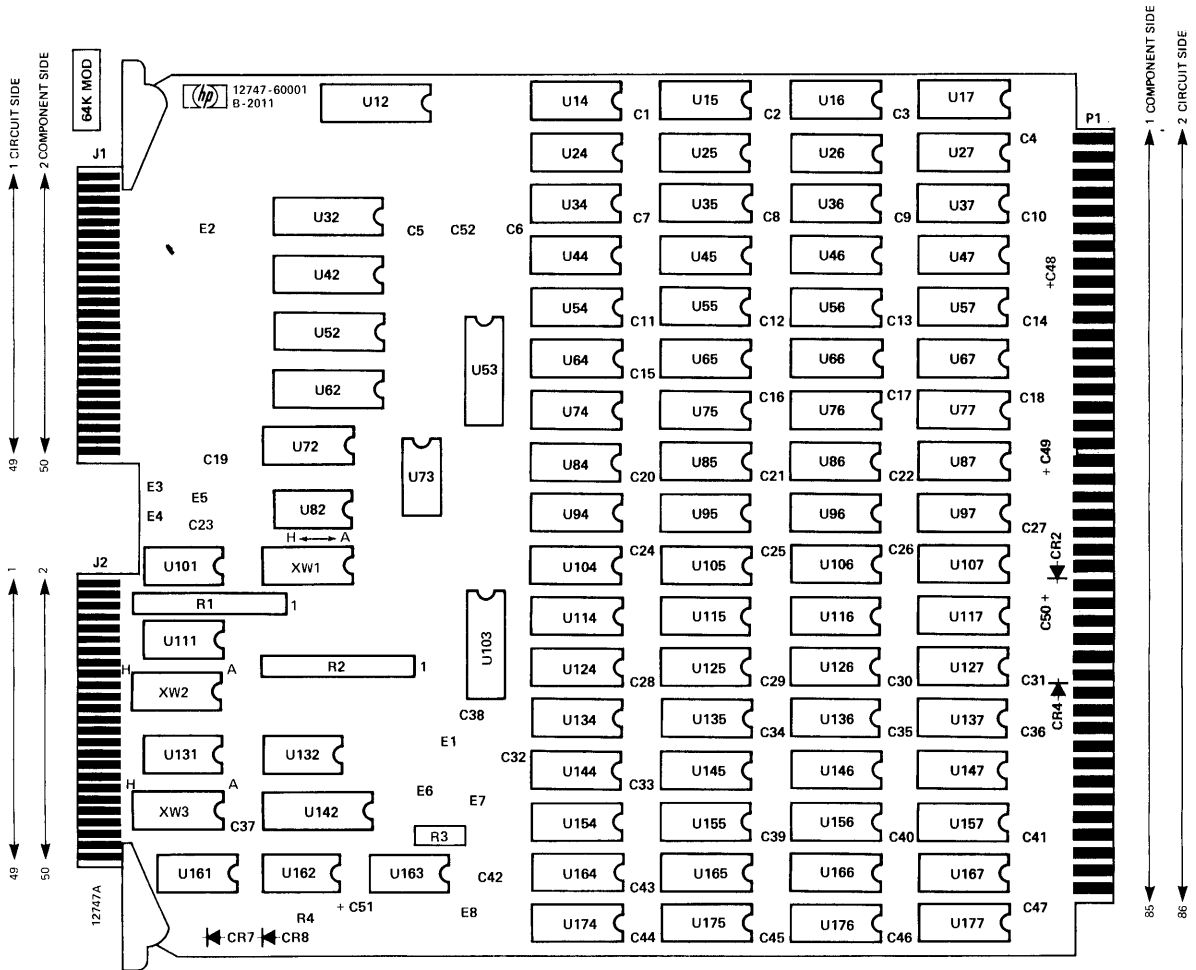
12747A Memory Module Assembly
12747-60001

ITEM NO	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	C1-47,52	CAP 1.0UF 20%		0160-4892		U	48
00	C51	CAP 68UF 20%		0180-1835		D	1
01	F1-8	TERM-STUD SGL		0360-1682		U	8
00	R4	RES 464 1% .50		0698-0090		U	1
		PIN GRV .062X.25		1480-0116		U	2
00	R1,2	NTWK RES 9X4.7K		1810-0279		U	2
01	U132	IC DIGITAL		1813-0176		U	1
00	U131	IC SN74S00N		1820-0681		U	1
01	U161,163	IC SN74S10N		1820-0685		U	2
00	U72	IC SN74S158N		1820-1015		U	1
01	U101	IC N82S42A		1820-1073		U	1
00	U162	IC SN74S02N		1820-1322		U	1
00	U62	IC 82S50A		1820-1338		U	1
00	U73	IC SN74S37N		1820-1450		U	1
01	U42,53,62,103,142	IC SN74S240N		1820-1633		U	5
01	U12,32,52	IC SN74LS241N		1820-1918		U	3
		SW DIP 8 ROCKER		3101-2243		U	1
		LABEL-WARNING		7120-6492		U	1

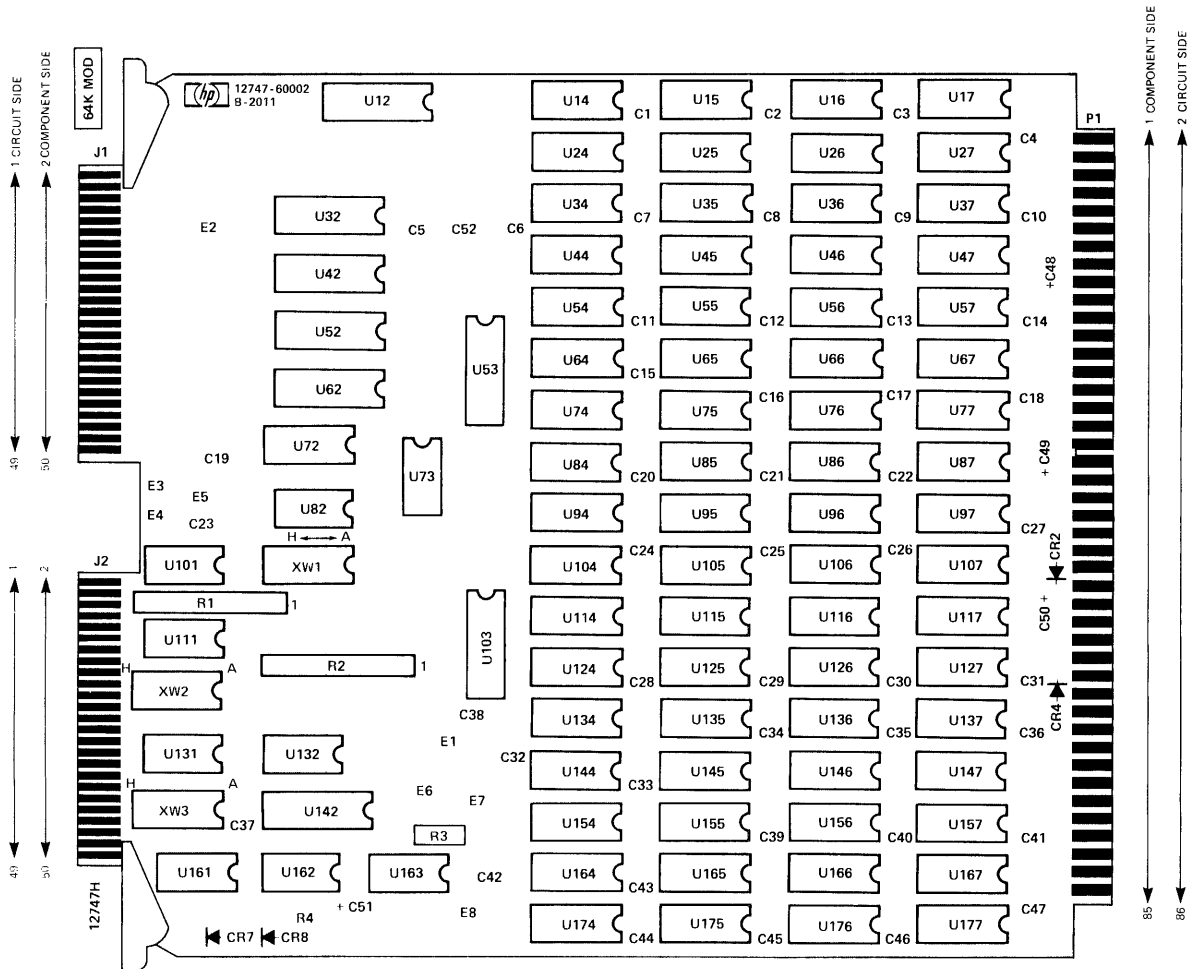| ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	W9,10	WIRE JUMPERS		8159-0005		D	2
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		N	1
		EXTRACTOR-PC WHT		5040-6075		N	1
		BOARD-ETCHED		5090-0110		1	1
01 03 05 07 09 11 13	U14-17,24-27,34-37, 44-47,54-57,64-67, 74-77,84-87,94-97, 104-107,114-117, 124-127,134-137, 144-147,154-157, 164-167,174-177,	STRESD 1818-0340		5081-2705		3	68
		ASSY-COMP SEQ		12747-64001		A	1
		PS SEQUENCER		ET13480		1	0

12747H Memory Module Assembly
12747-60002

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	C1-47,52	CAP 1.0UF 20%		0160-4892		U	48
01	C51	CAP 68UF 20%		0180-1835		D	1
01	F1-8	TERM-STUD SGL		0360-1682		U	8
01	P4	RFS 464 1% .50		0698-0090		U	1
		PIN GRV .062X.25		1480-0116		U	2
01	R1,2	NTWK RES 9X4.7K		1810-0279		U	2
01	U132	IC DIGITAL		1813-0176		U	1
01	U131	IC SN74S00N		1820-0681		U	1
01	U161,163	IC SN74S10N		1820-0685		U	2
01	U72	IC SN74S158N		1820-1015		U	1
01	U101	IC N82S42A		1820-1073		U	1
01	U162	IC SN74S02N		1820-1322		U	1
01	U82	IC 82S50A		1820-1338		U	1
01	U73	IC SN74S37N		1820-1450		U	1
01	U42,53,62,103,142	IC SN74S240N		1820-1633		U	5
01	U12,32,52	IC SN74LS241N		1820-1918		U	3
		SW DIP 4ROCKER		3101-2063		U	1
		LABEL-WARNING		7120-6492		U	1

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01	W5-7	WIRE JUMPERS		8159-0005		D	3
		BAG-ASTAT		9222-0746		C	1
		FXTRACTOR-PC GRY		5040-6006		W	1
		FXTRACTOR-PC WHT		5040-6075		W	1
		BOARD-ETCHED		5090-0110		1	1
01	U14-17	STRESD 1818-0509 ,24-27,34-37		5081-2705		3	68
03	44-47	,54-57,64-67					
05	74-77	,84-87,94-97					
07	U104-1	07,114-117,					
09	U124-1	27,134-137,					
11	U144-1	47,154-157,					
13	U164-1	67,174-177,					
		ASSY-COMP SEG		12747-64002		A	1
		PS SEQUENCER		ET13480		1	0

MEMORY CHECK
BIT ARRAYS

HP 12779A/12780A AND 12779H/12780H
FAULT CONTROL MEMORY
CHECK BIT ARRAY BOARDS

THEORY OF OPERATION

NOTE

This document is part of the HP 1000 M, E, and
F-Series Computers Engineering and Reference
Documentation and is not available separately.

THEORY OF OPERATION

Data Paths

The five-bits (CMDS17 through CMDS20) along with the existing parity
bit (MDS16), comprise the data correcting bits to correct the data bus.
The parity bit stored in the check bit board position CMDS21 is used in
conjunction with the other parity bits in determining double bit errors.
These check bits are received by a 74S04 (U162) so that write data may
be set up at the data-in pins of the RAMs. The RAMs used on the module
are non-inverting, the MDS-BUS transceivers (U161) provide an inverting
data path from write to read operation. The MDS-BUS drivers are driven
by a 8T95 and are enabled only when there is NOT a refresh, ($\overline{\text{MREF}}$ is
high) when there is a read cycle (R/$\overline{\text{W}}$-(RR) is high), when the clock is
active ($\overline{\text{CLK}}$ is low), and when the board is selected (DRMDS - is low).

Board Select

Two exclusive nor gate ICs (U71 and U142) compare the high-order
address bits with a jumper plug configurable board address. Jumpers
XW1 A through D provide a binary module selection of the board address.

Jumpers XW1-E, XW1-F, XW2-C and CW2-D provide for module sizes as per
the chart below:

	WX1-E	XW1-F	XW2-C	XW2-D
128KW	out	in	out	out
64KW	in	in	out	out
32KW	in	in	in	out
16KW	in	in	in	in

Row selection. Row Selection is provided by two 3205 one of eight decoders and four 74S158 inverting multiplexers (U91, U92, U101, U102, U121, U122). The one of eight decoders provide row selection (one of sixteen 16K RAM rows) from the higher order address lines while the multiplexers provide a convenient method of refreshing all the RAMs.

Address Drivers. Two inverting octal three-state gates (U12 and U32-74S240's) provide three functions. First, they offer a high input impedance for the address lines so many module and standard arrays can be bussed together. Secondly, they provide a method to multiplex the row address and column address lines to the RAMs. Lastly they provide low impedance address driving capabilities to the RAMs. In addition, the $\overline{\text{CAS}}$ driver is multiplexed with the column address lines thus providing a precise timing relation between $\overline{\text{CAS}}$ and the RAM column addresses.

When no memory cycle is in progress, the check bit module(s) idles with the row addresses A0 through A6 active and CAS inactive (HIGH). During this time, $\overline{\text{CLK}}$ is HIGH, CLK+ is low and all delay line timing taps (t30,t90 and t120 of U41) are inactive (low).

Memory Timing. Memory timing is provided by a tapped delay line and a memory clock pulse. Any memory cycle is in initiated by a HIGH to LOW transition of $\overline{\text{CLK}}$. This raises CLK+, firing the appropriately enabled $\overline{\text{RAS}}$ driver(s) and the delay line (U41). At t90 (90ns after CLK+) GATE LO- (U62-1) goes HIGH which disables the low-order row addresses and forces GATE HI 16K (U52-3) to go LOW which enables the high-order column addresses A7 through A13. $\overline{\text{CAS}}$ goes low about 30ns later when allow cast is enabled by t120 (delay line tap).

Refresh. If a refresh cycle is to be performed, the controller will issue $\overline{\text{MREF}}$ LOW. BD MREF goes HIGH and when the controller issues the clock ($\overline{\text{CLK}}$ low), all rows will receive a $\overline{\text{RAS}}$ signal, regardless of board select or row select decoders. A refresh signal is issued every 15 usec assuring that all row addresses on all array modules are refreshed every 2 ms.

ERROR CORRECTION AND DETECTION

The ECC option is a 22-bit, distance four code, which is physically a
22-bit hamming code (16 data bits, 5 check bits) plus an overall (even)
parity bit. The error correction code is described in the HP 2102C
Fault Control Memory Theory of Operation.

HP 12779H/12780H CHECK BIT ARRAY BOARDS

The high speed fault control (HSFC) array board(s) (check bit array boards) are used in conjunction with the 2102H HSFC controller and regular high speed memory array boards. The check bit board is used to store the parity check bits generated by the controller. Five check bits and an overall parity bit are generated; one check bit (P16) is stored in the parity position (bit 16) on a regular array board, while the remaining four check bits (P16-P20) and the overall parity bit (P21) are stored on the checkbit board. The check bit boards use same address and control lines (on J1) which the standard array boards use; a separate data path is provided on J2 for the checkbit boards, and the standard data path is not received on the boards. The RAMs used on the check bit array boards are 16K, 150 nsec RAMs (HP burned in part number 5090-0114). The 12779H is half-loaded with RAMs and can accomodate a maximum address space of 128K words; the 12780H is fully-loaded and has a maximum address space of 256K words. The board blank can also be used for 12779A/12780A modules; jumpers W3, W4, W5, W6 provide selection between the standard speed and high speed modules as follows:

```
               |W3 | W4 | W5 | W6
12779A/12780A  |IN | OUT| IN | OUT
-----------------------------------------
12779H/12780H  |OUT| IN | OUT| IN
```

2.0 THEORY OF OPERATION

2.1 Data Paths

The five-bits CMDS17 through CMDS21 (along with P16 sotred in the existing parity bit) comprise the data correcting bits to correct the data bus. These check bits are received by a 74S04 (U162) so that write data may be quickly set up at the data-in pins of the RAMs. The RAMs used on the module are non-inverting, so the 8T95 CMDS-BUS transceivers (U161) provide an inverting data path from write to read operation, the need for which was previously discussed. The CMDS-BUS drivers are enabled (DR MDS- LOW) only when there is NOT a refresh (MREF is high), when there is a read cycle (R/W is high, when the clock is active (CLK is low), and when the board is selected (BD SEL+ is HIGH).

2.2 Board Select

The 82S42 exclusive-nor-gates (U71 and U142) compare the high-order address bits (A14 thru A19) with a jumper plug configurable board address. Jumpers XW1 A through D provide a binary module selection of the board address.

Jumpers XW1-E, XW1-F, XW2-C and XW2-D provide for module sizes as per the chart below:

(HP 1000 M/E/F-SERIES ERD)

	WX1-E	XW1-F	XW2-C	XW2-D
128KW	out	in	out	out
64KW	in	in	out	out
32KW	in	in	in	out
16KW	in	in	in	in

Jumpers XW2-A and XW2-B allow placement of a 16KW or 32KW block within a 64KW segment of memory.

2.3 Row Selection

Row selection is provided by two 3205 one of eight decoders and four 74S158 inverting multiplexers (U91,U92,U101,U102,U121,U122). The one of eight decoders provide row selection (one of sixteen 16K RAM rows) from the higher order address lines while the multiplexers provide a convenient method of refreshing all the RAMs.

2.4 Address Drivers

Two inverting octal three-state gates (U12 and U32-74S240's) provide three functions. First, they offer a high input impedance for the address lines so many module and standard arrays can be bussed together. Secondly, they provide a method to multiplex the row address and column address lines to the RAMs. Lastly they provide low impedance address driving capabilities to the RAMs. In addition, the CAS driver is multiplexed with the column address lines thus providing a precise timing relation between CAS and the RAM column addresses. Four 74S37's (U111,U112,U131,U132) provide the drive capability necessary to drive the RAS signals to the memory arrays.

2.5 Idle Conditions

When no memory cycle is in progress, the check bit module(s) idles with the row addresses A0 through A6 active and CAS inactive (HIGH). During this time, CLK is HIGH, CLK+ is low and all delay line timing taps (t30,t90 and t120 or U41) are inactive (low).

2.6 Memory Timing (READ or WRITE cycle)

Memory timing is provided by a tapped delay line and a memory clock pulse. Any memory cycle is initiated by a HIGH to LOW transition of CLK. This raises CLK+, firing the appropriately enabled RAS driver(s) and the delay line (U41).

Since W4 and W6 are installed for the 12779H/12780H, T30+ is the only timng tap of interest from the delay line. At T30+ (30ns delay from CLK+ high) GATELO- is driven high and soon after GATE 16K- is driven low. This sequence disables low order address drivers and enables the high order address drives and CAS- onto the rray address bus. T30+ also generates allow CAS+ (since

(HP 1000 M/E/F-SERIES ERD)

this is not a refresh cycle) so that CAS- is also driven to the arrays. A read or write cycle will occur according to the state of the input R/W line. The cycle ends when CLK from the controller goes high. This diasbles the RAS drivers, and 30 nsec later when T30+ goes low CAS to the arrays goes high, the high order address drivers are disabled, and the low order address drivers are disabled, and the low order address drivers are enabled (GATELO- low). The board is now in the "IDLE" state.

2.7 Refresh

If a refresh cycle is to be performed, the controller will issue MREF LOW. BD MREF goes HIGH, generating logic one's at all multiplexor outputs, so when the controller issues the clock (CLK low), all rows will receive a RAS signal regardless of board select or row select decoders. A refresh signal is issued every 15 sec assuring that all row addresses on all array modules are refreshed every 2 ms.

(HP 1000 M/E/F-SERIES ERD)
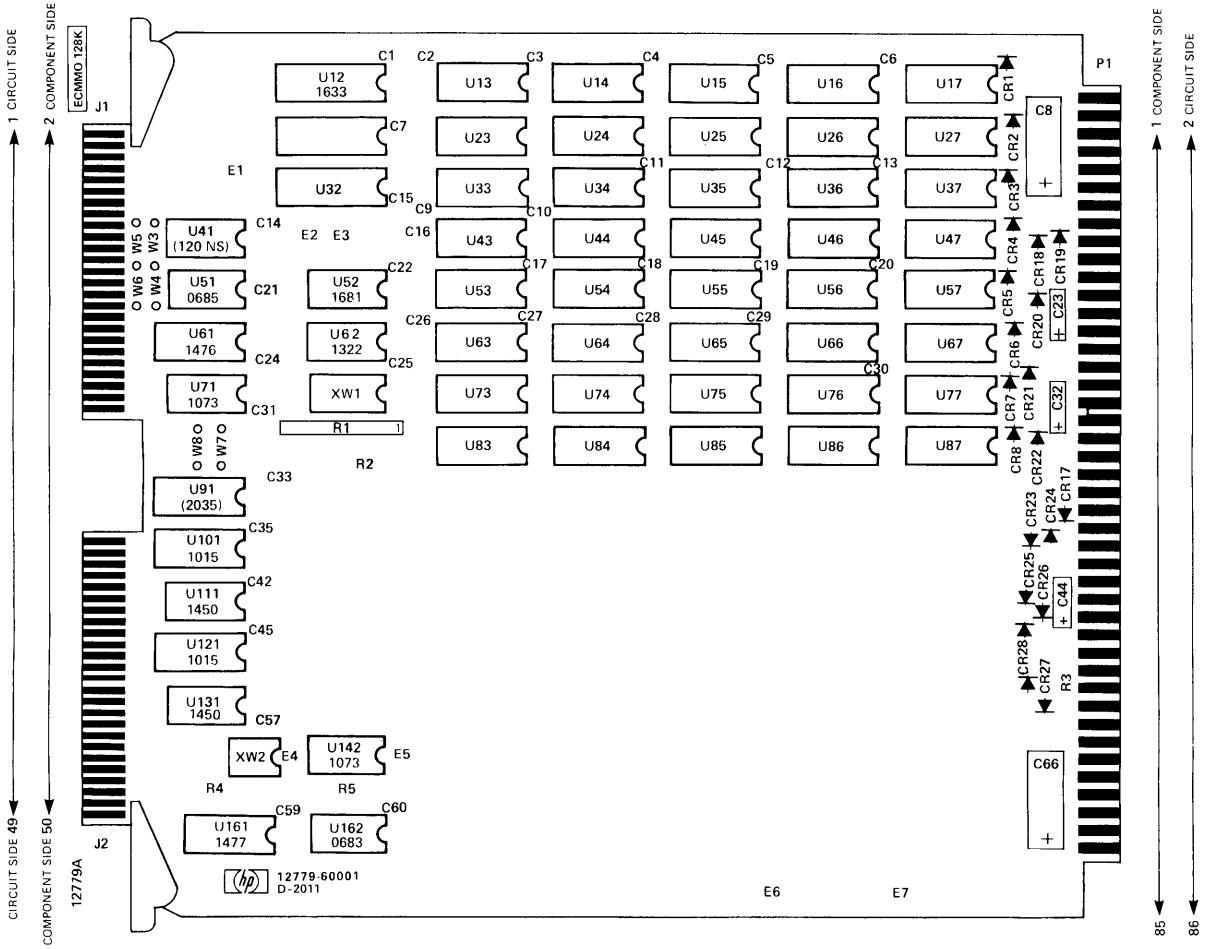
12779A 256KB Check Bit Array Assembly
12779-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01 03 05	C9-14,21,22,24,25,31 33,35,42,45,52,59, 60	CAP .01UF		0160-2055		U	18
01	C1-7,15-20,26-30	CAP 1.0UF 20%		0160-4892		U	18
00	C8,66	CAP 68UF 20%		0180-1835		U	2
01	C23,32,44	CAP-TA 3.30F		0180-2690		U	3
00	E1-7	TERM-STUD SGL		0360-1682		U	7
00	R3	RES 464 1% .50		0698-0090		U	1
00	R4,5	RES 4.64K 1%.125		0698-3155		U	2
00	R2	RES 237 1%.125		0698-3442		U	1
		PIN GRV .062X.25		1480-0116		U	2
00	R1	NTWK RES 9X4.7K		1810-0279		U	1
01	U41	IC DIGITAL		1813-0176		U	1
00	U52	IC SN74S00N		1820-0681		U	1
00	U162	IC SN74S04N		1820-0683		U	1
00	U51	IC SN74S10N		1820-0685		U	1
01	U101,121	IC SN74S158N		1820-1015		U	2
01	U71,142	IC N82S42A		1820-1073		U	2
		IC SN74S02N		1820-1322		U	1

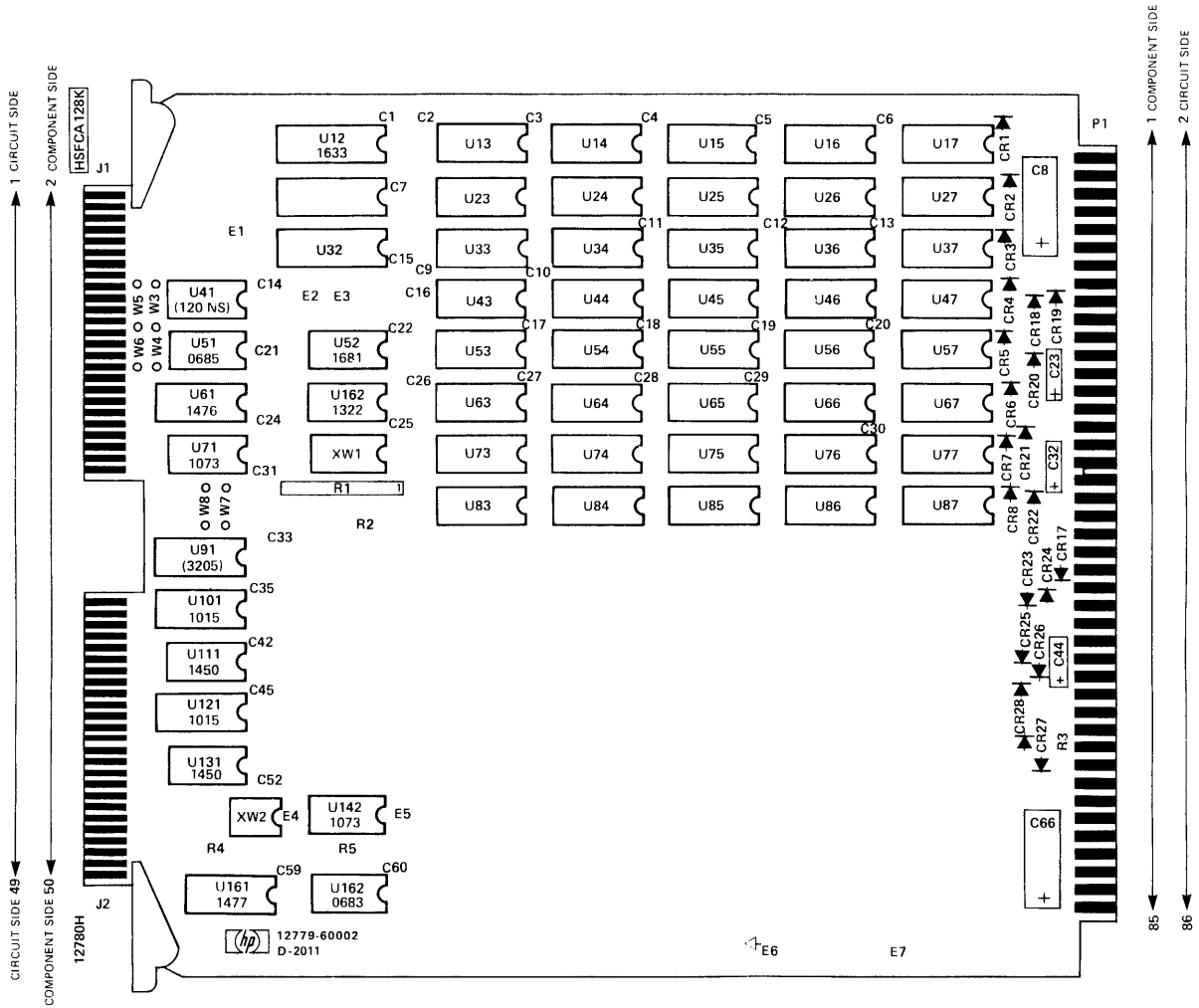| ITEM NO	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
00U62				1820-1322			
01	U111,131	IC SN74S37N		1820-1450		U	2
00U61		IC 8T96B		1820-1476		U	1
00U161		IC 8T95B		1820-1477		U	1
01	U12,32	IC SN74S240N		1820-1633		U	2
00U91		I.C. BINARY DCDR		1820-2035		U	1
01CR28		DIODE 1N2071		1901-0029		D	1
01	CR1-8,17-26	DIODE 1N5817		1901-1080		D	18
00CR27		DIO-ZNR 5.62V 2%		1902-3105		D	1
		SW DIP 7ROCKER		3101-1974		U	1
		SW DIP 4ROCKER		3101-2063		U	1
		LABEL-WARNING		7120-6492		U	1
01	W3,5,7	WIRE JUMPERS		8159-0005		U	3
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
01 03 05	U13-17,23-27,33-37, 43-47,53-57,63-67, 73-77,83-87	STRESD 1818-0340		5180-0601		3	40
		BD ETCHED		5090-0560		1	1
		PS SEQUENCER		ET13480		1	0

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12779H 256KB Check Bit Array Assembly
12779-60002

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01 03 05	C9-14, 21,22,24,25,31 C33,35,42,45,52,59, C60	CAP .01UF		0160-2055		U	18
01	C1-7,15-20,26-30,	CAP 1.0UF 20%		0160-4892		U	18
01	C8,C6	CAP 68UF 20%		0180-1835		D	2
01	C23,32,44	CAP-TA 3.30F		0180-2690		U	3
01	E1-7	TERM-STUD SGL		0360-1682		U	7
01	R3	RES 464 1% .50		0698-0090		U	1
01	R4,5	RES 4.64K 1%.125		0698-3155		U	2
01	R2	RES 237 1%.125		0698-3442		U	1
		PIN GRV .062X.25		1480-0116		U	2
01	R1	NTWK RES 9X4.7K		1810-0279		U	1
01	U41	IC DIGITAL		1813-0176		U	1
01	U52	IC SN74S00N		1820-0681		U	1
01	U162	IC SN74S04N		1820-0683		U	1
01	U51	IC SN74S10N		1820-0685		U	1
01	U101,121	IC SN74S158N		1820-1015		U	2
		IC N82S42A		1820-1073		U	2
		IC SN74S02N		1820-1322		U	1

12779H 256KB Check Bit Array Parts List (12779-60002) Sht. 2 of 2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	U02			1820-1322			
01	U111,131	IC SN74S37N		1820-1450		U	2
01	U61	IC 8T96B		1820-1476		U	1
01	U161	IC 8T95B		1820-1477		U	1
01	U12,32	IC SN74S240N		1820-1633		U	2
01	U91	I.C. BINARY DCDR		1820-2035		U	1
01	CR22	DIODE 1N2071		1901-0029		D	1
01	CR1-8,17-26	DIODE 1N5817		1901-1080		D	18
01	CR27	DIO-ZNR 5.62V 2%		1902-3105		D	1
		SW DIP 7ROCKER		3101-1974		U	1
		SW DIP 4ROCKER		3101-2063		U	1
		LABEL-WARNING		7120-6492		U	1
01	W4,6,7	WIRE JUMPERS		8159-0005		D	3
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
		BD ETCHED		5090-0560		1	1
01 03 05	U13-17,23-27,33-37, U43-47,53-57,63-67, U73-77,83-87,	STRESD 1818-0509		5081-2705		3	40
		PS SEQUENCER		ET13480		1	0

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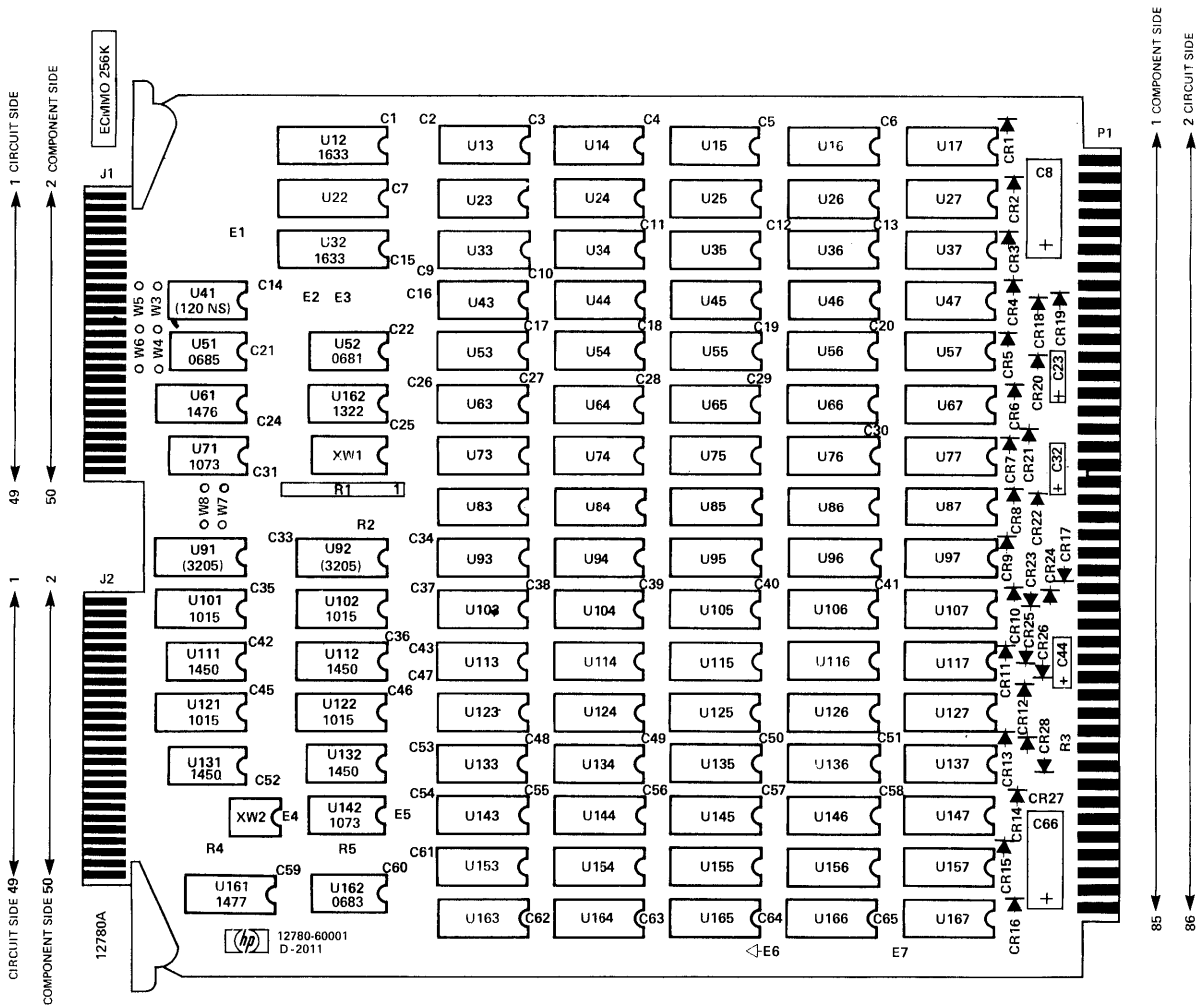
12780A 512KB Check Bit Array Assembly
12780-60001

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01 03 05	C4-10,21,22,24,25,31 33-36,42,43,45,46, 52-60	CAP .01UF		0160-2055		U	28
01 03	C1-7,15-25,26-30, 37-41,47-51,61-65	CAP 1.0UF 20%		0160-4892		U	33
00	C8,66	CAP 68UF 20%		0180-1835		D	2
01	C23,32,44	CAP-TA 3.30F		0180-2690		U	3
00	E1-7	TERM-STUD SGL		0360-1682		U	7
00	R3	RES 464 1% .50		0698-0090		U	1
00	R4,5	RES 4.64K 1%.125		0698-3155		D	2
00	R2	RES 237 1%.125		0698-3442		U	1
		PIN GRV .062X.25		1480-0116		U	2
00	R1	NTWK RES 9X4.7K		1810-0279		U	1
01	U41	IC DIGITAL		1813-0176		U	1
00	U52	IC SN74S00N		1820-0681		U	1
00	U162	IC SN74S04N		1820-0683		U	1
00	U51	IC SN74S10N		1820-0685		U	1
01	U101,102,121,122	IC SN74S158N		1820-1015		U	4
01	U71,142	IC N82S42A		1820-1073		U	2

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ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
00	U62	IC SN74S02N		1820-1322		U	1
01	U111,112,131,132	IC SN74S37N		1820-1450		U	4
00	U61	IC 8T96B		1820-1476		U	1
00	U161	IC 8T95B		1820-1477		U	1
01	U12,32	IC SN74S240N		1820-1633		U	2
01	U91,92	I.C. BINARY DCDR		1820-2035		U	2
00	CR28	DIODE 1N2071		1901-0029		D	1
01	CR1-26	DIODE 1N5817		1901-1080		D	26
00	CR27	DIO-ZNR 5.62V 2%		1902-3105		D	1
		SW DIP 7ROCKER		3101-1974		U	1
		SW DIP 4ROCKER		3101-2063		U	1
		LABEL-WARNING		7120-6492		U	1
01	W3,5,8	WIRE JUMPERS		8159-0005		U	3
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
01 03 05 07 09 11 13	U13-17,23-27,33-37, 43-47,53-57,63-67, 73-77,83-87,93-97, 103-107,113-117, 123-127,133-137, 143-147,153-157, 163-167	STRESD 1818-0340		5180-0601		3	80
		BD ETCHED		5090-0560		1	1
		PS SEQUENCER		ET13480		1	0

12780H 512KB Check Bit Array Assembly
12780-60002

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ITEM NO	REFERENCE DESIGNATOR FIRST SIX	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	L O C	QUANTITY PER
01 03 05	C9-14,21,22,24,25,31 C33-36,42,43,45,46, C52-60	CAP .01UF		0160-2055		U	2R
01 03	C1-7,15-20,26-30, C37-41,47-51,61-65	CAP 1.0UF 20%		0160-4892		U	33
01	C8,66	CAP 68UF 20%		0180-1835		D	2
01	C23,32,44	CAP-TA 3.30F		0180-2690		U	3
01	F1-7	TERM-STUD SGL		0360-1682		U	7
01	R3	RES 464 1% .50		0698-0090		U	1
01	R4,5	RES 4.64K 1%.125		0698-3155		D	2
01	R2	RES 237 1%.125		0698-3442		U	1
		PIN GRV .062X.25		1480-0116		U	2
01	P1	NTWK RES 9X4.7K		1810-0279		U	1
01	U41	IC DIGITAL		1813-0176		U	1
01	U52	IC SN74S00N		1820-0681		U	1
01	U162	IC SN74S04N		1820-0683		U	1
01	U51	IC SN74S10N		1820-0685		U	1
01	U101,102,121,122,	IC SN74S158N		1820-1015		U	4
01	U71,142	IC N82S42A		1820-1073		U	2

ITEM NO.	REFERENCE DESIGNATOR (FIRST SIX)	PART DESCRIPTION	PARENT OPTION	PART NUMBER	COMP. OPTION	LOC	QUANTITY PER
01	U62	IC SN74S02N		1820-1322		U	1
01	U111,112,131,132	IC SN74S37N		1820-1450		U	4
01	U61	IC 8T96B		1820-1476		U	1
01	U161	IC 8T95B		1820-1477		U	1
01	U12,32	IC SN74S240N		1820-1633		U	2
01	U91,92	I.C. BINARY DCDR		1820-2035		U	2
01	CR2B	DIODE 1N2071		1901-0029		D	1
01	CR1-26	DIODE 1N5817		1901-1080		D	26
01	CR27	DIO-ZNR 5.62V 2%		1902-3105		D	1
		SW DIP 7ROCKER		3101-1974		U	1
		SW DIP 4ROCKER		3101-2063		U	1
		LABEL-WARNING		7120-6492		U	1
01	W4,6,8	WIRE JUMPERS		8159-0005		D	3
		BAG-ASTAT		9222-0746		C	1
		EXTRACTOR-PC GRY		5040-6006		W	1
		EXTRACTOR-PC WHT		5040-6075		W	1
		BD ETCHED		5090-0560		1	1
01 03 05 07 09 11 13	U13-17,23-27,33-37, U43-47,53-57,63-67, U73-77,83-87,93-97, U103-107,113-117 U123-127,133-137 U143-147,153-157 U163-167,	STRESD 1818-0509		5081-2705		3	80
		PS SEQUENCER		ET13480		1	0