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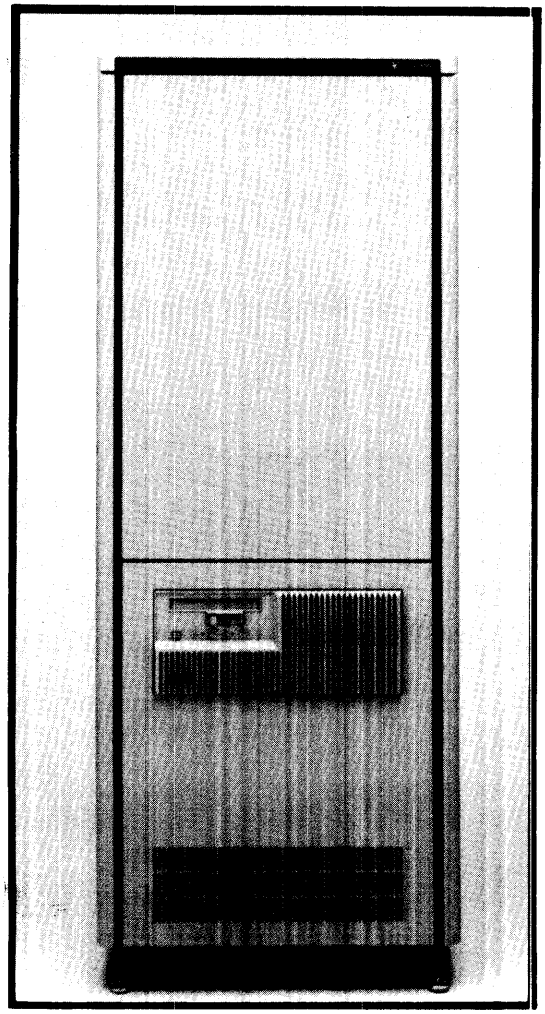
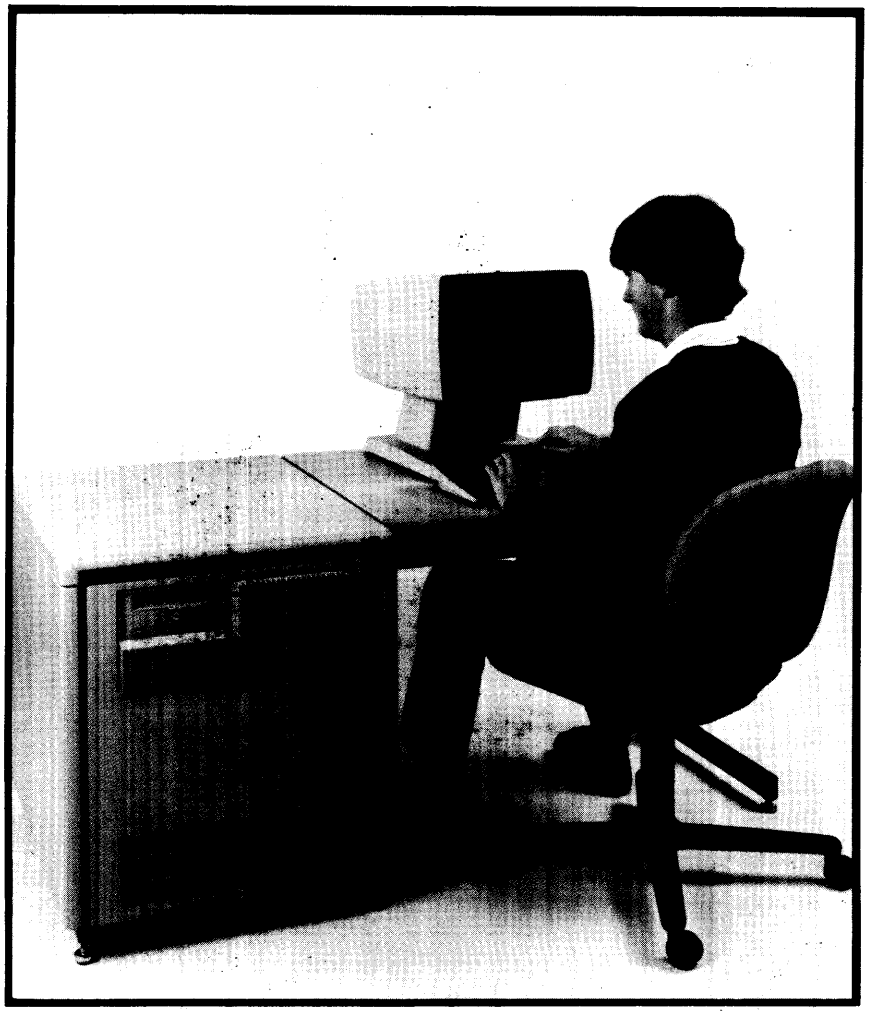
HP 1000 A900 Computer

Engineering and Reference Documentation

HP 1000 A-Series





HEWLETT PACKARD

HP 1000 A900 Computer

Engineering and Reference Documentation

Data Systems Division
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Printing History

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition	May 1984	
Update 1	Jan 1985	
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Update 2	Apr 1986	

NOTICE

Many of the schematic diagrams and parts lists in this document contain the generic number (manufacturer's number) of the IC packs. These are for your convenience when referring to pack diagrams and general operating conditions in semiconductor manufacturer's catalogs. The generic number, however, should not be used to order replacement parts from Hewlett-Packard. Many parts used in Hewlett-Packard equipment are purchased with special specifications and tolerances, or may undergo special testing and treatment (such as burn-in). Replacement parts therefore must be ordered using the Hewlett-Packard part number to ensure that the replacement part will restore the equipment to its proper operating conditions.

Preface

The detailed information provided in this document pertains to the card comprising the computer processor of the HP 1000 A900, a computer system which is available in the following:

* The HP 2139A in a rack-mountable 20-slot cabinet with power supply.

* The Micro-29 Computer System

* The HP Model 29 Computer System

The Input/Output (I/O) interfaces are not described since the information on them is provided in other manuals. The other manuals available covering this computer are the following:

Title	Part Number
HP 1000 A900 Computer Reference Manual	02139-90001
HP 1000 A900 Installation and Service Manual	02139-90002
HP 92049A RTE Microprogramming Manual	92049-90001
HP Micro/1000 System Computer Installation and Service Manual	02430-90001

The first chapter of this document provides an overview of the HP 1000 A900 processor by describing the functions and physical arrangements of the major blocks of the circuitry. Subsequent chapters provide information for each card including an overall block diagram, its description, followed by the theory of operation.

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Chapter 1
HP 1000 A900 Computer

1.1 Introduction

The HP 1000 A900 computer, subsequently referred to as the A900, offers a number of significant technical features:

* Three times the performance levels of the A600 and A700 and thus the highest speed operation in the HP 1000 A-Series computer family.

* Execution of superset of the A600 and A700 instructions.

* A microinstruction word of 48-bits, easily microcoded by using a paraphraser type of microassembler.

* A significantly improved micromachine.

* A fast cache memory.

* Standard Schottky TTL logic, FAST TTL logic, PLA's, EDC chips, and three SOS LSI chips providing efficient, fast floating-point operations.

* Compatibility with the A/L-Series I/O system which uses a DMA select code in its operation.

The A900 consists of five printed circuit cards. The five cards perform all processing of data, control of the main memory system, 768k bytes (3 Mb optional) of main memory and interfacing to the I/O subsystem. An optional control store card allows user microprogramming.

1.2 System Environment

The system environment of the A900 processor is shown in Figure 1-1. The backplane carries the logic signals, clock signals, and dc power. The computer cards and I/O cards plug into the backplane. The frontplane provides internal bus signal interconnections between the memory controller card and memory array cards. Additionally a different frontplane connects the optional control store to the sequencer card.

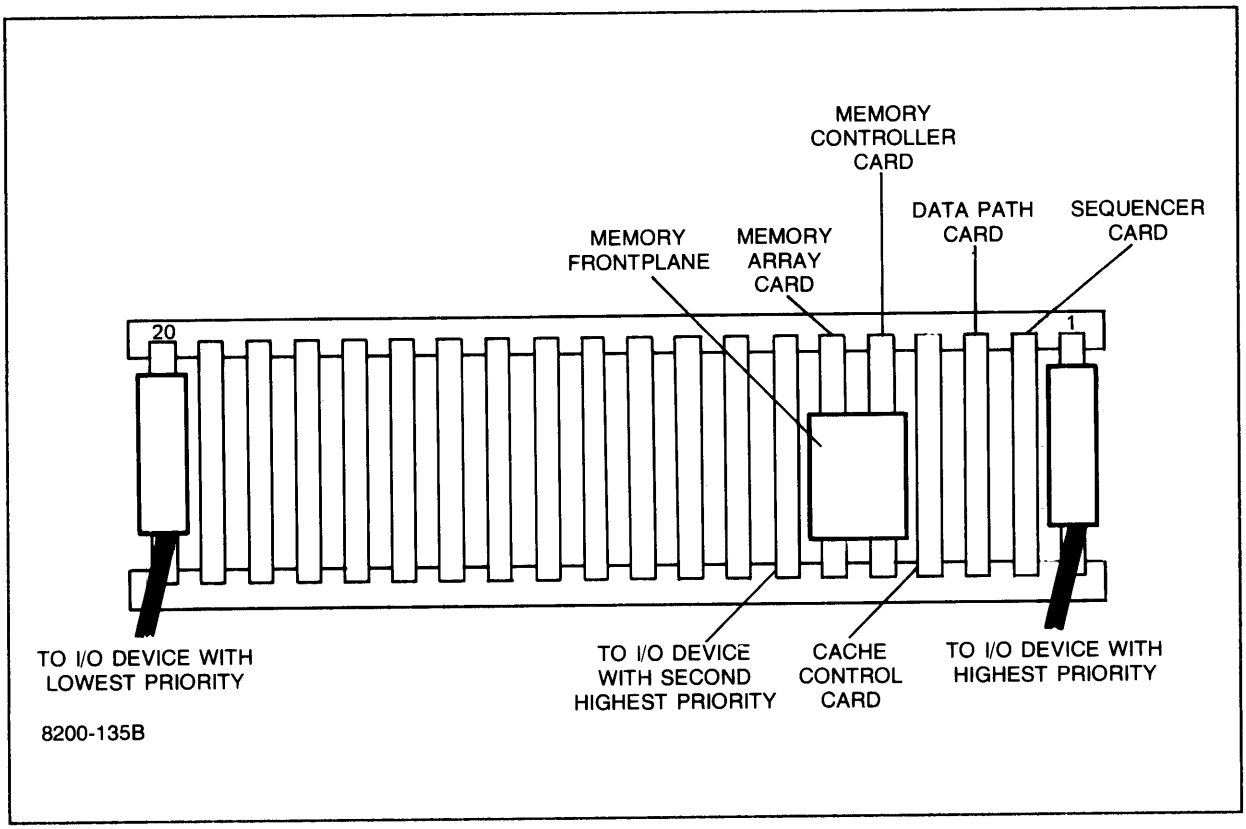

Figure 1-1. Processor Cards in a Typical System Environment

The control store card must be in slot one followed by the sequencer card, the data path card, the cache control card, the memory controller card, and the memory array cards, in this order. The I/O cards are below the memory array cards in descending interrupt and DMA priority. If the control store card is not used, an I/O card or a priority jumper card must be installed in the first slot. Any unused slots between two I/O cards must be filled with a priority jumper card in order to guarantee interrupt and DMA priority chains.

1.3 Description of Operation

The basic A900 processor consists of two processor cards called the sequencer and data path cards, a cache control card, a memory controller card, and a memory array card.

The A900 computer is designed for user microprogramming. Microprograms are stored in the processor's internal control store which is expandable using one HP 12205A Control Store card. This card combines writable control store and PROM control store.

In operation, the ALU and sequence logic of the processor on the sequencer and data path cards carries out the commands of the microinstructions of the microprograms stored in the control store on the sequencer card. These microprograms may be either the standard base set of the processor, or user microprograms. All HP 1000 Computer Series instructions are executed by microroutines of the base set. For microprogramming information refer to the HP 92049A Microprogramming Package Reference Manual, Part No. 92049-90001.

The cache memory controller contains the dynamic mapping system, virtual control panel (VCP) PROMs, boot memory RAMs, interface to the I/O system, and control logic for the cache memory. Hardwired address creation logic matches the processor to the cache memory speed. The memory controller card has the actual cache memory data store, the interrupt logic and the logic for implementing error detection and correction (EDC). Memory cards are available in 768k byte or 3M byte increments with error correction.

The CPU only uses the backplane for I/O instructions, leaving all of its bandwidth available for I/O. This is possible because all I/O operations occur on a standard A-Series backplane (identical to the HP 1000 L-Series backplane), and direct memory accesses (DMA) are merged with CPU requests in the cache (the only request source for main memory).

1.4 System Support Features

1.4.1 Virtual Control Panel

The Virtual Control Panel (VCP) is an interactive program stored in PROM on the cache control card. In a manner similar to a conventional computer control panel, the VCP enables an external device (such as a terminal) to control the CPU. Thus, the operator can access the various registers (A,B, etc.), examine or change memory, and control execution of a program.

In a typical application, the VCP could be an HP 262X (e.g., HP 2626A) or HP 264X (e.g., HP 2646A) terminal interfaced by an HP 12005A Asynchronous Serial Interface Card. When not used as the VCP, the VCP-assigned terminal can be employed in the same way as any other terminal connected to the system. When the A900 computer is operating as a node in a computer network via DS/1000-IV, the VCP can be an adjacent computer in the network.

1.4.2 Self-Test Capability

The A900 computer contains firmware microcode for self testing. Two self-test routines are stored in PROM on the sequencer and cache control cards. These routines are executed whenever computer power is turned on, providing a convenient confidence-check of the processor cards and memory cards. Execution of both routines can also be initiated by a switch on the sequencer card, and execution of the second routine can be initiated by operator command via the VCP.

Refer to the following manual for additional information regarding the self-test capability:

HP 1000 A900 Computer Installation and Service Manual, Part No. 02139-90002.

1.4.3 DC Power Requirements

Table 1-1 shows DC power requirements for the A900 computer cards.

Chapter 9 includes backplane information covering items such as connector pinouts, the card cage layout, and the card cage assembly drawing.

An optional battery backup card and battery pack can be added to sustain memory for 15 to 90 minutes for up to five memory cards minutes in the event of a complete power failure. Another power supply option provides two 25-kHz voltages that can be rectified at the load and used to power accessory plug-in cards for measurement and control applications.

NOTE

Power requirements for I/O interface cards are provided in the individual manuals covering these cards.

1.4.3.1 Cooling Requirements

The computer has no external cooling requirements. Internal fans should be used for adequate ventilation to maintain operation within the environmental limitations.

1.4.3.2 Environmental Specifications

Table 1-2 shows the computer's environmental specifications.

Table 1-1. Power Specifications

CARD	CURRENT		POWER
	+5V	+5M ADDRESSED	(RMS INPUT TO SUPPLY)
12201A Sequencer			45 W
12202A Data Path			42 W
12203A Cache Control			37 W
12204A Mem. Controller			33 W
12220A EC Array (768k-byte)	1.0 A* 0 A**	2.0 * 1.0 A**	12 W
12221A EC Array			
1 card	1.1 A	2.1 A	
2 cards	2.2 A	3.3 A	
3 cards	3.3 A	4.5 A	
4 cards	4.4 A	5.7 A	
5 cards	5.5 A	6.9 A	
6 cards	6.6 A	8.1 A	
7 cards	7.7 A	9.3 A	
8 cards	8.8 A	10.5 A	
12205A Control Store		3.7 A	
PCS Added		0.7 A	

* Addressed
** Unaddressed

Note:
The operating power specification is not cumulative when adding additional array cards since power consumption is proportional to access rate and only one card is accessed at any one time (only one card at a time is operating). When a card is being accessed, all other cards dissipate standby power.

1.5 Input Power Requirements

The AC power requirements below apply to the power supply input:

Line Voltage	86-138 Vac (115 Vac -25%/+20% standard) 178-276 Vac (230 Vac -23%/+20% option 15)
Line Frequency	47.5 to 66 Hz.
Maximum Power Required	800 Watts

The optional DC power requirements given below must be charged from an external source:

+External Battery Input:	15.0V maximum
-External Battery Input:	Ground

Table 1-2. Environmental Specifications

AMBIENT TEMPERATURE:	
Operating:	0 degrees to 55 degrees C (32 degrees to 131 degrees F) up to 3048 metres (10,000 ft) 0 degrees to 45 degrees C (32 degrees to 131 degrees F) up to 4572 metres (15,000 ft)
Non-operating:	-40 degrees to 75 degrees C (-40 degrees to 167 degrees F) -40 degrees to 60 degrees C (-40 degrees to 140 degrees F) with Battery Backup
RELATIVE HUMIDITY:	
5% to 95%, without condensation	
ALTITUDE:	
Operating:	to 4.6 km (15,000 ft)
Non-operating:	15.3 km (50,000 ft)
VIBRATION AND SHOCK:	
HP 1000 A900-Series products are type tested for normal shipping and shock and vibration. (Contact factory for review of any application that requires operating under continuous vibration.)	

MANUAL UPDATE

MANUAL IDENTIFICATION
Title: HP 1000 A900 Computer E & R Doc.
Part Number: 02139-90003
Edition Date: May, 1984

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Update Number: 2
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THIS UPDATE GOES WITH: First Edition (May, 1984) with Update 1
or: Reprint (January, 1985)

THE PURPOSE OF THIS MANUAL UPDATE
is to accumulate all the changes to the latest edition of the manual. Earlier updates to the latest edition which have not been incorporated are contained herein. This update package consists of all new and changed pages (backup pages are provided when necessary) plus this cover letter.

CHANGED PAGES
have the update number at the bottom of the page. Changes are marked with a vertical bar in the margin. When an update is incorporated in a subsequent reprinting of the manual, these bars are not removed. "New" pages are those with a page number not present in the latest edition of the manual.

TO UPDATE YOUR MANUAL
replace existing pages in the latest edition of the manual with corresponding pages from this update package. Remove all replaced pages. In addition, insert any new pages from this update.

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Chapter 2
Conventions and General Description

This section covers the following:

* Signal names and abbreviations used in this document.

* An overall block diagram of the processor.

* The I/O addressing and interrupt systems.

2.1 Signal Names

All signal names include a trailing plus "+" or minus "-" sign to indicate the assertion sense of the signal; i.e., high true "+" or low true "-". If the signal is applied on a bus, the assertion sense is that which the microprogrammer would see in the principle data paths. The signal names are unique throughout the processor so that signal names referenced in the theory of operation correspond to the same signal names on the schematic.

Preceding the sense sign, there may be a number or numbers in brackets, indicating the bit or bits of the signal or bus.

2.1.1 Signal Name Fields

Each signal name is divided into fields with period (.) separators.

2.1.1.1 Signal Category Field

The first field defines the signal as being in one of five categories:

1. Clock signals begin with "CK".

2. Signals limited to one card begin with a two character acronym (or mnemonic) that represents the card:

AR	Memory Array
CA	Cache Array
CS	Control Store
DP	Data Path
MC	Memory Controller
SQ.	Sequencer

3. Backplane signals that are standard in the A-Series/L-Series type system begin with "LBP".

4. Other backplane signals begin with "BP".

5. Frontplane signals begin with "FP".

Signals that fall into one of two categories may begin with either appropriate mnemonic.

2.1.1.2 Application Field

The second field (follows the first period) indicates how the signal is applied: For example:

STK	Subroutine Save Stack
MEM	Memory control signal
INCD	Increment register
RTN	Return
UIR	Microinstruction register signal
CAC1	CA card clock 1 signal
CAC2	CA card clock 2 signal

2.1.1.3 Function Field

The third field indicates the general function of the signal. Some of the more common general functions include:

ACK The signal is intended as an acknowledge indication from one functional unit to another.

ADDR The associated signal is a component of an address bus.

BUS The associated signal is a component of a bus.

CLK This signal is used as a clock input.

CLR This signal is used as a clear input to a counter, register, etc.

EN This signal is used to gate, or enable the output of some functional unit onto a (shared) bus.

LD This signal is used to enable the loading of a counter, register, etc.

REG The associated signal is a component of a continuously available register data path.

REQ This signal is intended as a request indication from one functional unit to another.

SET This signal is used to enable the setting of a counter, register, flip-flop, etc., to a known value other than logical zero.

WR This signal is used as a RAM write strobe.

2.1.1.4 Other Signal Name Conventions

In situations where multiple copies of a signal exist, they are distinguished by an A,B,C or D suffix. Signals which are simply delayed versions of others are distinguished by a leading "BUF", e.g., MC.BUF.ADDR7+.

Signals which constitute one element of a data path, such as a bus, are uniquely defined by a one or two digit suffix that is not separated by a period, e.g., SQ.XT.BUS7-.

2.2 Component Identification

The IC components of the A900 processor are given a part identification code which identifies their physical location on the card (or board). The first character is the letter "U" and the remaining characters are four digits that locate the IC on the component matrix within that card (an assembly diagram is provided for each card at the end of each card's section). The IC can be located on the schematic page by the mnemonic/number identification given in parentheses following each parts reference designator (U number); e.g., xxyy, identify the part as falling on the xx'th row and yy'th column).

Discrete components are identified by one or two letters (C - capacitor, R - resistor, etc.) to indicate the type of component followed by an appropriate sequence number (1, 2, 3, etc.).

2.3 Overall Block Diagram

Figure 2-1 illustrates the major sections of the computer which are contained on the five A900 cards described in this manual. In order of importance they are the following:

* Microprogram Sequencer Section
* Processor Data Path Section
* Memory Addressing Logic
* Cache Memory
* Memory Controller Section
* Input/Output Logic Section

Other sections not shown in the block diagram are memory array, memory maps, data store RAM, processor registers, and control store.

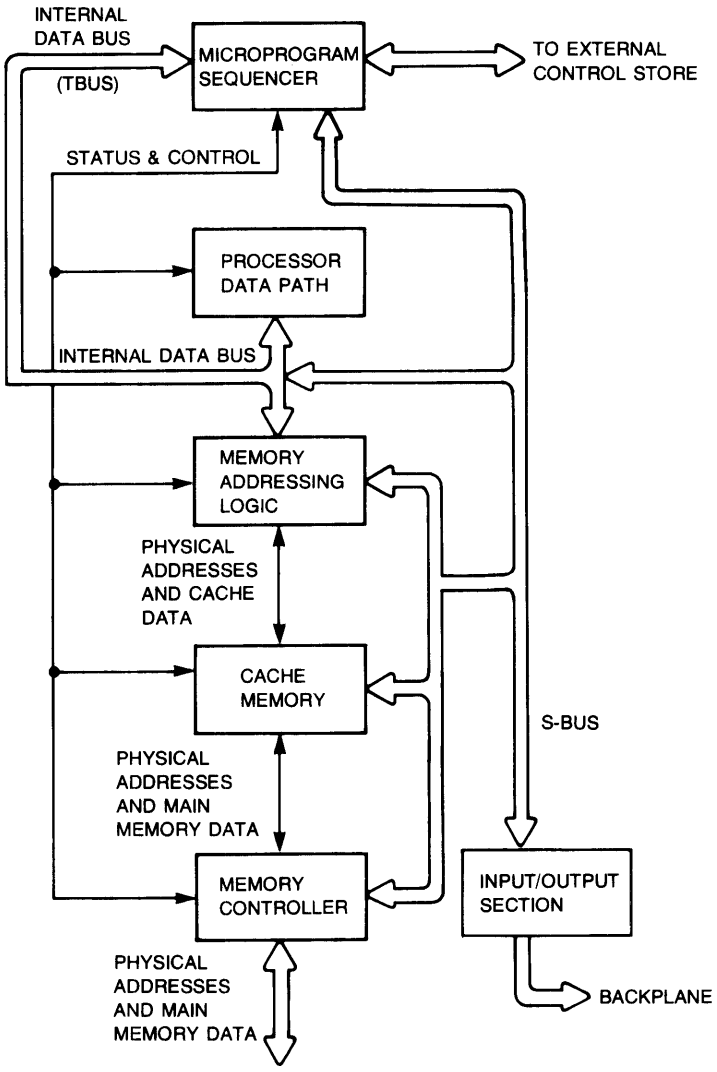

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Figure 2-1. Block Diagram of the A900 Processor

2.3.1 Summary of Processor Cards

The A900 is a microprogrammed computer and thus the processor can be called a micromachine which is contained on the computer cards as follows:

* The HP 12201A Sequencer card contains the microprogram sequencer for microcode execution. It also contains the PROMs of the control store that provides the instruction base set. Control signals for the micromachine come from this card.

* The HP 12202A Data Path card has the data-path logic circuitry which provides temporary data storage and all the internal manipulation of data. It provides the micromachine's arithmetic capability, including floating-point.

* The HP 12203A Cache Control card contains the I/O interface, memory address generation, and DMS maps. The cache arbitration logic determines whether the processor or main memory has access to the cache at any given time and whether requested memory locations are located in the cache.

* The HP 12204A Memory Controller card contains the memory control logic, error correction logic, and interrupt logic. The data RAMs for cache memory, boot memory, scratch memory, etc. are also contained on this card. (External control store is available on the optional HP 12205A card.)

* One or more of the following cards provide main memory with error correction: the HP 12220A 768 kbyte memory array, and the HP 12221A 3 Mbyte memory array.

The following paragraphs summarize the operating descriptions of the functional blocks, and the sections following provide complete operating descriptions and theory of operation for each of the cards.

2.3.2 Functional Blocks

As shown in the block diagram, the following functional blocks are the major divisions of the processor. Each of the functional divisions is contained on a card that is named for the primary function located on that card.

2.3.2.1 Microprogram Sequencer And Clock

The microprogram sequencer on the Sequencer (SQ) card controls all microcode flow and generates control signals used by all other blocks. In operation, it creates the address of the subsequent microinstruction to determine the microinstruction sequence for executing the current macroinstruction. For this process, the sequencer logic brings together status inputs from other blocks, the currently executing microinstruction, and information from data path circuits.

For the A900 Processor, each microinstruction is 48 bits wide. The total address space available for microcode is 32k words (addressed by 15 bits in microinstruction type-3 microwords). The basic processor includes 6k words of PROM control store, and the optional control store card is available for expansion using either PROM or RAM.

The clock circuitry resides on the sequencer card and provides multiple versions of clock signals with low skew to all parts of the system.

2.3.2.2 Processor Data Path

The Data Path (DP card) contains all circuitry for implementing microcode which does not involve memory or I/O. It includes the arithmetic circuitry with accumulators, an ALU, a barrel shifter for right or left bit shifting, floating-point chips, and primary and secondary register files with 16 registers each. There is also a number of status registers on this card, for example interrupt status, cache status, and sequencer self-test status.

To improve processor performance the data path has been pipelined. An explanation of pipelining is given in the microprogramming manual.

2.3.2.3 Cache Memory

The memory addressing logic block located on the Cache (CA) Control card generates the address used for access to the main memory. It chooses a logical address from one of the three CPU memory address registers (PC, M1, M2) or from the backplane for DMA accesses. All three of the CPU address registers can be loaded with an incremented version of the current address. One of the registers can also be loaded from the data path, or with data returning from the cache (for MRG and indirect resolution). Indirection and DMA accesses are handled transparently to the CPU.

The cache memory is split between the CA and Memory Controller (MC) cards. It provides the processor with much faster effective memory access than that obtainable with the main memory alone because of the shorter distances and faster RAMs used in the cache.

If the data is in the cache, a read or write occurs in one microcycle according to the "hit ratio". This is a function of the total size of cache, block size, set associativity and of the program being run. The cache size is 4k bytes with a two-word (four byte) block size, and a "set associativity" of one (sometimes called direct mapped). A hit ratio of about 88% is typically achieved for typical benchmark programs.

The effective access time to the CPU is a function of hit ratio and fault handling time; i.e., the time required to update the cache with the proper data when a "miss" occurs. Fault handling time for the A900 processor is four-microcycle time periods and thus the effective access time for the cache is 1.36 times the 130 ns microcycle time.

All DMA accesses are handled through the cache. For CPU accesses the block is allocated for both reads and writes. (in cache terminology: store-to, read allocate, and write allocate for both CPU and DMA)

For its address the cache memory takes a 15-bit logical address plus a 5-bit map-set select address and translates via a 1024-entry mapping RAM (32 map sets of 32 maps each) into a 24-bit physical address. It also checks for violations of read or write protected pages.

2.3.2.4 Memory Controller

The Memory Controller (MC) card controls all processor accesses to the main memory. It is responsible for main memory requests from the cache, memory array initialization and timing, refresh operations for the dynamic RAMs, and error detection/correction.

The main memory path width is 39 bits (32 data bits and seven check bits) generated (on writes to main memory) and checked (on reads from main memory) by using two LSI error correction chips. When an error is detected, the Parity Violation Register records both the physical address and the error syndrome bits. If the error has multiple bits and cannot be corrected, the error logging is disabled and an interrupt is generated.

2.3.2.5 Memory Array

A minimum A900 computer system includes one memory array card. To increase memory capacity, additional array cards may be added. The number of array cards that may reside in the system is limited to eight. Each additional array card that is added to the system reduces the backplane slots available for I/O cards. (I/O cards or array cards can be plugged into the same slot). The various memory array cards available use 64k, and 256k RAMs for a total of 768k bytes, and 3M bytes, respectively.

Data is stored in memory as two 16-bit words and seven check bits. 117 RAMs are on each array card, arranged in three banks. Data is transferred over the frontplane to the memory controller. All data transfers occur 39 bits at a time.

The data capacity of a memory system depends on the number of address lines available. Since there are 24 address lines, 32M bytes of memory can be addressed. The amount of memory in the system depends on the number of array cards present. There can be eight array cards in an A900 system, using the 20-slot box. If a full complement of HP 12221A 3M byte array cards is installed, 24M bytes of main memory are possible.

2.3.3 External Control Store

The optional Control Store (CS) card provides space for 4k words of 48-bit wide writable control store. On the same card, sockets permit the installation of 2k- to 8k-words of PROM control store according to the size of the available PROMs. This card is for users who wish to develop their own special purpose microcode. The CS is part of main control store and is loaded through the I/O system.

The CS card has a backplane interface through the I/O Master circuitry, which handles the DMA and decoding of I/O instructions necessary to load the writeable control store. It also interfaces through the frontplane with the Sequencer card. The CS appears to the processor as a memory. It receives microaddresses from the Sequencer and returns microinstructions to the Sequencer.

2.4 Interfaces

2.4.1 I/O Interface

The A900 processor, like other members of the A-Series, uses the same I/O System as the HP 1000 L-Series computer. Therefore, the signals and theory of operation that apply to this I/O system also apply to the A900 computer with a few exceptions. That is, there are important differences in the way that A900 implements the A-Series/L-Series I/O protocols. Primarily they stem from the fact that A900 does not use the A-Series/L-Series backplane for its CPU memory accesses. For detail information on the A-Series/L-Series backplane and the I/O master, refer to the HP 1000 A-Series/L-Series Computer I/O Interfacing Guide, Part No. 02103-90005.

2.4.2 Memory Interface

The memory interface functions that deal with DMA through the backplane are performed by the CA card in A900. All DMA is handled through the cache. In the event of a cache miss, DMA accesses cause a block of memory to be allocated in the cache for both read and write operations.

Because the CPU deals directly with the cache, memory requests through the backplane are not used. However, I/O instructions fetched by the processor will be broadcast across the backplane with RNI- asserted.

2.4.3 Processor Interface

The CA and MC cards of the processor perform the I/O interface functions. The CA card handles I/O handshaking and reset functions with help from the CPU. The MC card performs interrupt, slave-mode, and CCLK.

2.5 Interrupt System

A block diagram of the interrupt system is shown in Figure 2-2. The microinterrupt portion of the system, which appears at the left of the block diagram, is located on the SQ card. When a microinterrupt occurs, the cause is latched in the UINT register, BP.UINTP+ is asserted, and a branch to the UIV address is forced. This jump to the UIV address will also occur if BP.IND.INT- goes low or if BP.JTAB.INT- goes low during a JTAB line. Additional details can be found in Chapter 3 (Sequencer Card).

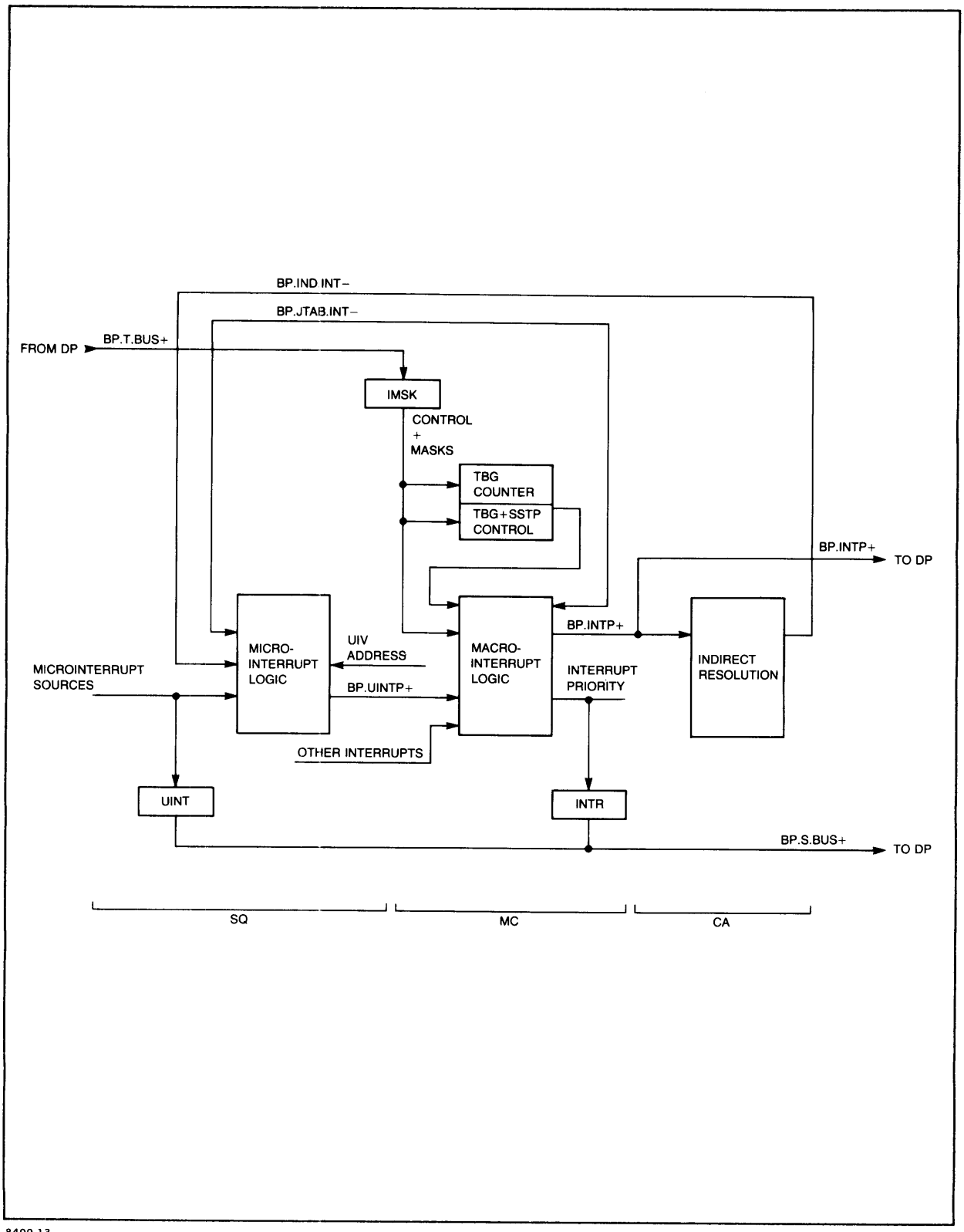
Most of the macrointerrupt portion of the system, which appears at the center of the block diagram, is located on the MC card. (The theory of operation for it is contained in Chapter 6.) The macrointerrupt logic looks at all the macrointerrupt conditions and their masks. If there is an unmasked interrupt pending, BP.INTP+ will be asserted "high". Notice that UINTP or SSTP are not included in the generation of INTP. The BP.JTAB.INT- signal is similar to INTP but it includes SSTP and the TDI mask condition indicated by MEM/JTDI. It is only valid during a JTAB line. If it is asserted "low" during a JTAB line it will cause a branch to the UIV address.

The logic also looks at all the interrupt conditions (including UINTP) and generates a value indicating the highest priority interrupt. This value is readable via the INTR register. The TBG centers around a counter which counts down BP.CCLK+ to produce 10 millisecond ticks. Additional logic controls the TBG and generates the SSTP interrupt. The IMSK register provides control and mask signals for all of this logic.

The remaining portion of the macrointerrupt system is found on the CA card. The indirect resolution logic counts the number of indirects which have occurred in resolving a DEF. If three or more have occurred and BP.INTP+ is "high", BP.IND.INT- will be asserted "low". This will cause a branch to the UIV address. More details about the indirect resolution logic can be found in Chapter 5 under Memory Address Creation, Indirect Addressing.

2.6 Self-Test

Self-Test resides in control store, and consists of about 1.5k words of microcode. It is a go/no-go test, with fault detection better than 92% and fault isolation to the card level of about 89%. In the case of expensive, field replaceable components, fault isolation is provided to the component level. Error codes are output through the nine LEDs on the sequencer card. For operation of the self-test refer to the HP 1000 A900 Computer Installation and Service Manual.



8400-13

Figure 2-2. Block Diagram of the Interrupt System

Technical Manual Update

02139-90003

Note that "*" indicates changed page.

UPDATE	DESCRIPTION
2	Replace or add the following pages with the pages supplied:

Title page*/ii*
5-3*/5-4
5-35/5-36*
5-37*/5-38*
5-39*/Blank
6-49*/6-50
9-9*/9-10

Replace the following drawings with the drawings provided:

12203-60004-51
thru
12203-60004-66

with

12203-60011-51
thru
12203-60011-66

Correction on dwg #D-02430-60004-51 in Section 9.

Chapter 3
Microprogram Sequencer

3.1 Introduction

This chapter describes the block diagram and the theory of operation of the sequencer (SQ) card. The latter part of this chapter describes clock generation since clock generation circuitry is contained on the sequencer card. To understand fully the operation of this microprogrammed computer, please refer to the HP 92049A RTE Microprogramming Package Reference Manual, Part No. 92049-90001.

3.2 Block Description

The sequencer circuitry is implemented mostly on the SQ card although the condition selection function is contained on the data path card. Figure 3-1 is a block diagram of the sequencer card shown in Figure 3-2.

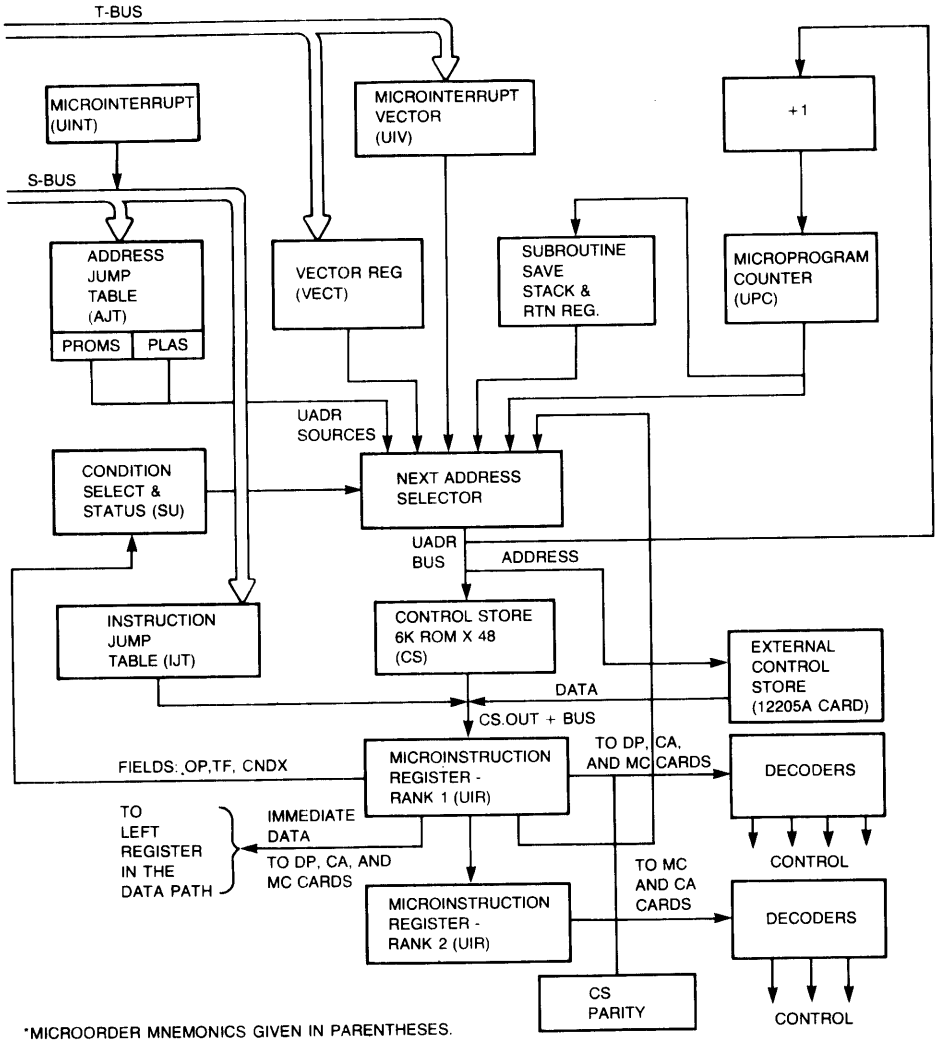
The card is divided into the following functional blocks:

Next Address Selector
Microprogram Counter
Microinstruction Register
Subroutine Save Stack
Vector Register
Instruction Jump Table
Entry Lookup Table and JTAB Line
Microinterrupt Vector Register
Control Store

Paragraphs under subheading 3.2 describe these blocks in general and paragraphs under subheading 3.3 describe their logical operations (theory of operation).

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

The terms "right" and "left" are used in some of the functional block names. These names are relative to their position on the block diagram and are used throughout the A900 processor and microprogram terminology.



8300-87A

Figure 3-1. Sequencer Card Functional Block Diagram

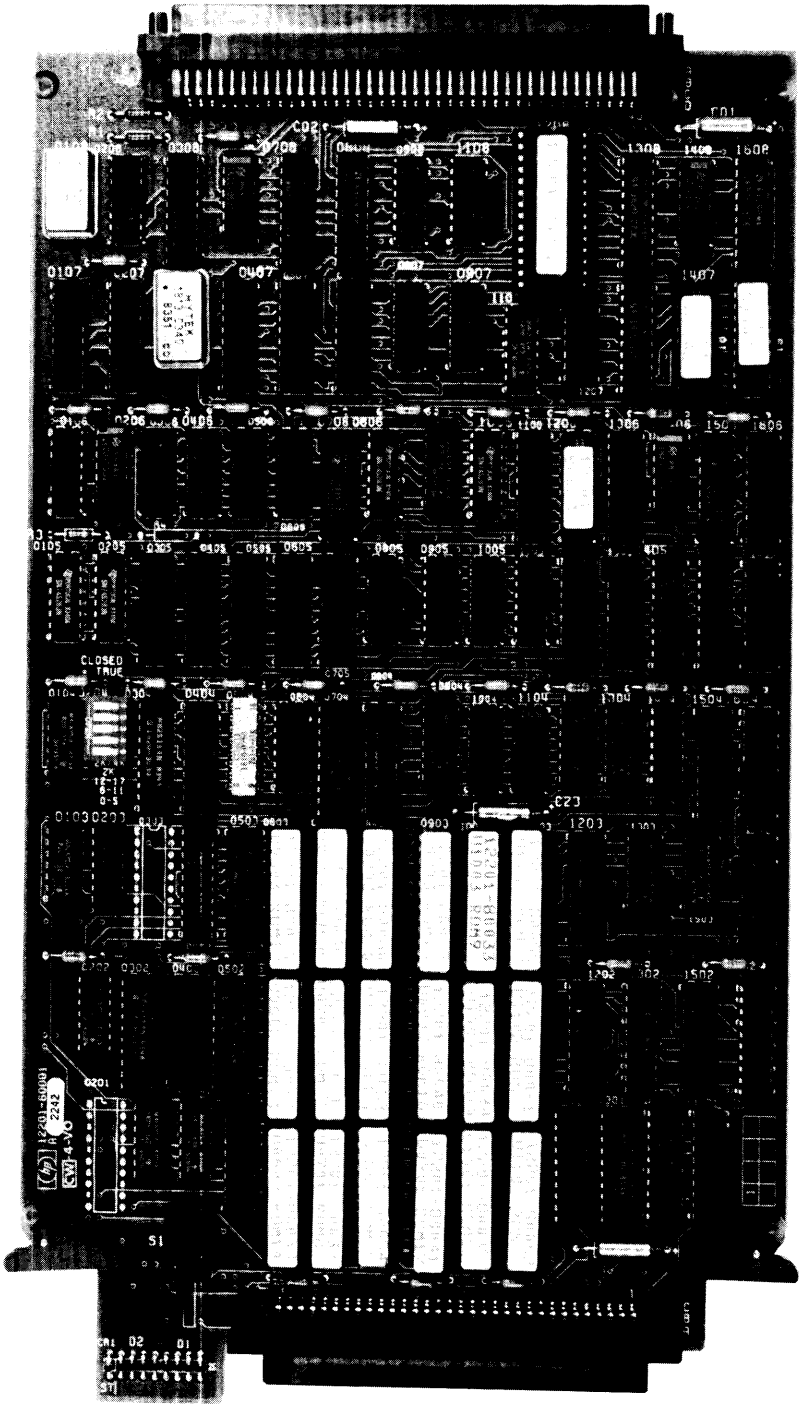


Figure 3-2. Sequencer Card (12201-60001)

3.2.1 Next Address Selector

This functional block generates the next microaddress. A "low true" version of this address appears on a 15-bit bus known as SQ.UADR- which has six tristate sources (the output of the Next Address Selector). Some are related to OP field functions and some to other functions. The related sources for the next address that are not OP field functions are the UIV (microinterrupt vector) and VECT (vector) registers and the two halves of the AJT (address jump table). These sources are described in more detail in later paragraphs.

Selection is controlled mostly by the OP field of the instruction in the UIR (microinstruction register). The Next Address Select functional block contains a stack RTN register, a UIR/RTN multiplexer, and a CNDX MET/UPC multiplexer for this purpose.

To execute sequential microinstructions the UPC (microprogram counter) is selected. The UIR is selected for microjumps and jump subroutines. If it is a long target all 15 address bits come from the UIR. For short targets, the lower 8 bits come from the UIR and the upper 7 bits come from the UPC. Therefore, short branches are restricted to the current 256 word page. A return from subroutine selects the address from the STACK. For conditional operations, if the condition is met then either a target address or the stack is selected. If not met the UPC is selected (condition-met signal comes from the condition-select and status register).

In operation, a 2:1 multiplexer selects between UIR and stack RTN based on whether a JMP/JSB or stack RTN type operation is occurring. The output of this MUX and UPC is fed into another 2:1 multiplexer with its select controlled by the CNDX.MET+ signal for conditional operations.

For unconditional operations the CNDX.MET+ signal is forced to the "met state" by the condition logic which in turn forces the MUX to select UIR/RTN. The output of this MUX is another SQ.UADR- source. It is the correct OP field address except for the following four cases. For the (1) IMM and (2) SP1C operations, the address always come from UPC. For the (3) JMPC and (4) JSBC operations, the upper 7 bits of the address come from UPC. Since the upper and lower bits of the address may come from different sources, the multiplexer and buffer have separate enables for their upper and lower bits.

The "low true SQ.UADR-" bus is buffered to form the "high true" SQ.UADR+ bus which is used by the on card control store. Another buffer generates the FP.UADR+ bus which is sent to the SQ card frontplane for use by external control store and diagnostic tools.

The condition-met-logic that generates the CNDX.MET+ signal is located on the data path card (refer to Chapter 4).

3.2.2 Control Store

The SQ card has three banks of CS (control store) which are addressed by the 15-bit SQ.UADR+ bus. Each bank contains six PROMs with 8 outputs each for a total of 48 bits. Initially, 2k x 8 PROMs are used for a total size of 6k words. However, two switches allow future expansion to 4k x 8 or 8k x 8 PROMS as they become available, thus allowing up to 24k on card control store.

The three banks of control store must be addressed contiguously and must start at address 00000. Three switches indicate which of the three banks are actually loaded with PROMS. All of the on-card PROMS must be of the same size.

The 48-bit FP.CS.OUT+ bus is driven by the output of the control store, by the IJT, or by external control store connected via the SQ card frontplane. The logic which controls the selection of the source understands up to two banks of external control store. If either external bank overlaps the on-card control store, the external bank will take precedence. This allows on-card PROMS to be "patched" with external PROM or WCS.

If the selection logic determines that none of the above sources should drive the bus, it enables a buffer which drives 16 of the 48 bits. The buffer forces OP/JSB, STOU/NOP, STOT/NOP, MEM/NOP, and SPO/NOP. A microinterrupt occurs when this NOCS condition is detected.

3.2.3 Microinstruction Register and Parity

At the end of each microcycle, the value on the FP.CS.OUT+ bus is clocked into the 48-bit UIR. The output of the register, known as BP.UIR.REG+, is used on the SQ card and sent to the DP, CA, and MC cards via the backplane. This register forms the first rank of the UIR. It controls functions which are occurring during the current microcycle.

Some of the first rank bits are clocked into a register at the end of the microcycle. The output of this register, known as BP.R2.UIR.REG+, is sent to the CA and MC cards via the backplane. This register forms the second rank of the UIR. It controls functions which will occur during the following microcycle.

On the SQ card, BP.UIR.REG+ is sent to a 48-bit parity tree which checks for odd parity. A microinterrupt occurs if an error is detected. Therefore, bit 47 of the microinstruction should always be adjusted to generate odd parity over the instruction.

3.2.4 Microprogram Counter

The UPC appears near the upper-right corner of the SQ Block Diagram. At the end of every microcycle it is loaded with an incremented version of SQ.UADR+. This increment is done using a 15-bit adder with one of its inputs forced to zero and its carry input asserted.

3.2.5 Subroutine Save Stack

The subroutine save stack is a 15-bit by 16 word RAM and control logic which includes a 4-bit stack pointer register. A single bus connects the RAM inputs, the RAM outputs, the stack input register, and the return register (RTN). The stack input register is loaded with an incremented version of SQ.UADR+, the same as UPC (both registers will always hold the same value).

The stack pointer register always points to the top of the stack in the RAM, and the RTN register always holds a copy of the value on the top of the stack. Normally, the RAM is addressed directly by the stack pointer. The top of stack value, which is read out of the RAM, is loaded into RTN at the end of each microcycle. (The value is already there, but loading it again provides a new copy.) This is the idle state for the stack.

During a JSB type operation, an incremented version of the stack pointer is used to address the RAM, and the value in the Stack Input register is written into the RAM and into the RTN register. Also, the stack pointer is updated with its incremented value. Updating performs a stack push and leaves the stack in its idle state. For an RTN type operation, the value in the RTN register is used by the address generation logic.

The RAM is addressed with a decremented version of the stack pointer, and at the end of the microcycle the RTN register is updated with the value read out of the RAM. The stack pointer is updated with its decremented value. Updating performs a stack pop and again leaves the stack in its idle state.

In order to allow detection of underflow and overflow, RAM location 0 is not used during normal operation. A push (JSB) from stack level 15 writes to location 0 and a pop (RTN) from stack level 0 transfers to the address held in location 0. However, both of these actions cause a microinterrupt to occur (see below). MEM/JTAB microorder will set the stack pointer to 0.

3.2.6 Instruction Jump Table

The instruction jump table looks at the upper nine bits of the macroinstruction on the BP.S.BUS+ and generates a 48-bit microinstruction word. During a line containing a MEM/JTAB, this microinstruction is enabled onto the FP.CS.OUT+ bus and is loaded into the UIR at the end of the microcycle. It, therefore, becomes the first line of emulation code for the current macroinstruction.

Eight bits of the microinstruction are hardwired to force TF/TRUE, CNDX/TRUE, and OP/SP1C or OP/RTNC (one op field bit is not hardwired). The remaining 40 bits are generated by five PLAs, each having 32 terms. This allows the required decoding to select the first emulation microinstruction.

3.2.7 Address Jump Table

The intent of the AJT is quite similar to that of the IJT. It must look at a macroinstruction on the BP.S.BUS+ and generate a 15-bit address which will be used in the following microcycle to generate the second emulation microinstruction for the current macroinstruction. However, due to the level of decoding needed, and to certain timing constraints, the AJT is more complex than the IJT.

Two types of decoding are used in the AJT. First, a PLA looks at all 16 macroinstruction bits. The PLA has 48 terms allowing the entire instruction set to be split into 48 groups; in this way the HP 1000 base-set instructions are categorized, including a useful vectoring of the I/O instructions. However, the PLA is not capable of handling the large number of instructions in the 101xxx/105xxx (octal) group.

To handle this second large group of instructions, PROMs are used to look at the lower nine bits of the macroinstruction. The PROMs make possible the complete decoding of this instruction group. Only the A/B bit (bit 11) cannot be distinguished. For most instructions this bit is efficiently handled using either the LREG/CAB or CNDX/IR11 microorders. Logic looks at the value on the BP.S.BUS+ and decides whether to use the PLA or the PROM. The PLA generates only seven bits of the address. When it is selected, the remaining bits are driven to produce even addresses in the range of 01000 to 01376 (octal). The PROM generates a full 15-bit address and can, therefore, point anywhere in control store. Note that both the PLA and the PROM must generate "low true" addresses.

The data on the BP.S.BUS+ arrives sufficiently late to require a special technique to load addresses into registers from the AJT as follows: A transparent latch is inserted between the BP.S.BUS+ and the AJT which enables the AJT outputs directly onto the SQ.UADR+ bus during some of the "dead time" at the beginning of the following microcycle. The latch is opened during any microcycle with an MEM/JTAB in the UIR. Therefore, the data starts propagating through the AJT as soon as it is available. At the end of the microcycle the latch closes, but the data continues to propagate to the AJT output which will becomes valid before it is needed in the following microcycle.

With the above scheme, the decision about which half of the AJT to use is still made in the JTAB microcycle. The enables for the PLA and PROM are both generated and clocked into a register at the end of the JTAB microcycle. The register outputs are used to enable the appropriate half of the AJT in the following microcycle. Neither half is enabled if an unmasked interrupt or single step is present in the JTAB microcycle.

Since the decoding done by the IJT line is less complete than that done by the AJT, the AJT serves one more function. The IJT "guesses" at a microinstruction a useful operation for the first emulation line of many macroinstructions. However, for some macroinstructions this line is actually harmful. For this reason, the AJT generates a signal (BP.NO.EXECUTE-) which can inhibit any stores or memory operations indicated by the IJT microinstruction. This signal is asserted by the AJT PLA and the AJT PROM for unrecognized instructions, and by the AJT PROM when the IJT guessed wrong for the actual instruction.

Note that if two consecutive microcycles contain MEM/JTAB, the AJT latch does not close between them and the AJT output never becomes valid. This can happen only for the JMP,D macroinstruction, which has only one line of emulation code and therefore never uses the AJT address. However, BP.NO.EXECUTE must still remain valid so that during the JMP,D instruction the OP address, described above under Next Address Selector section, is substituted for the AJT output.

3.2.8 Microinterrupt Vector Register

The UIV is a double-ranked register. Its first rank is an eight-bit register which is loaded from the lower bits of the TBUS in the microcycle after STOT/UIV is coded. This first register is also cleared when PON+ is low, indicating that power is not yet valid. The second rank is 16-bits wide, and is updated every microcycle. Its lower bits are copied from the first rank, and its upper bits are set to a fixed value. The second rank is used to drive the SQ.UADR- bus under a number of conditions which are described below. Neither of the ranks is inverting, so the value loaded into the first rank appears inverted when it reaches the "low true" SQ.UADR- bus. The upper bits of the second rank are set to allow UIV to produce "high true" addresses in the range from 00000 to 00377 (octal). When the first rank is reset when PON+ is low, the address produced is octal 00377.

When the lower 15 bits of UIV are being used as an address, the 16th bit drives the BP.NO.EXECUTE- signal. This bit is driven so that in the microcycle in which UIV is used as an address, the stores and memory operations indicated by the microinstruction in the UIR will be inhibited.

The UIV will be selected to drive the SQ.UADR- bus during the current microcycle if any of the following conditions are true.

1. The LBP.PON+ signal was low three microcycles ago.

2. A microinstruction with even parity was detected in the UIR during the previous microcycle.

3. A stack underflow or overflow occurred during the previous microcycle.

4. An address pointing to nonexistent control store was generated two microcycles ago.

5. The Time Base Generator was not serviced between two consecutive ticks.

6. The ZAP counter (see below) had a value of all ones in the previous microcycle.

7. The previous microinstruction included an MEM/JTAB and an unmasked interrupt or single step was pending.

8. The previous microinstruction included a memory operation which went three or more indirect cycles, and an unmasked interrupt was pending.

3.2.9 Vector Register

The VECT register is a 16-bit register which is loaded from the TBUS in the microcycle after an STOT/VECT is coded. Unless the AJT or UIV override it, the lower 15 bits of the register drive the SQ.UADR- bus in the microcycle after an SP2/JMPV is coded. The register is inverting so that so that "high true" data loaded into the register will correctly appear "low true" for the SQ.UADR- bus. When the VECT address is being used, its 16th bit is drives the BP.NO.EXECUTE- signal. Therefore, this upper bit should always be loaded with zero for nondiagnostic microcode.

3.2.10 Microinterrupt Register

The UINT register is an 8-bit register which is enabled to drive the BP.S.BUS+ during a microcycle which includes an RREG/UINT. The register's inputs are most of the signals which request a microinterrupt. The register normally is clocked at the end of each microcycle. However in the cycle after a microinterrupt is first requested, the UINTP+ signal goes high indicating that a microinterrupt is pending. This also freezes the UINT clock, causing it to hold the microinterrupt condition(s) which caused the freeze. UINT stays frozen until UINTP is cleared using the SP2/CLUI special. Note that any microinterrupts which occur while UINT is frozen will not show up in UINT even though the rest of the microinterrupt process will occur normally.

3.2.11 Self-Test Hardware

The SQ card is self tested using hardware on the card, which includes the sequencer self-test register (SQST) and the ZAP counter, and a microcode routine executed by the processor.

The Sequencer Self-Test Register (SQST) is a 16-bit register used to drive the BP.S.BUS during a microcycle which has an RREG/SQST microorder in the UIR. It is loaded from the 15-bit microaddress bits SQ.UADR+. The ZAP counter described below controls the clocking of the SQST register.

The ZAP counter is a four-bit up counter which is controlled by two microorder specials. A microcycle with SP2/ZPOF in the UIR stops the counter and loads it with octal 10 at the end of the microcycle. A microcycle with SP2/ZPON in the UIR causes the counter to start counting at the end of the following microcycle. It then increments at the end of each microcycle until an SP2/ZPOF occurs. When the counter reaches 17 (octal) it will request a microinterrupt. This causes the UIV register to be selected as the microaddress source during the following microcycle.

If a MEM/JTAB or MEM/JTDI occurs during the cycle when the counter reaches octal 17, the ZAP microinterrupt does not occur and the IJT, AJT and macrointerrupt related effects of the JTAB do not occur. While the top bit of the counter is set, the SQST register is clocked once every microcycle. While the top bit is clear, the SQST register is frozen. This allows the self-test to take snapshots of the SQST values. The top bit also affects the operation of the stack. If it is clear, and a JSBC is coded, the stack will do a push, whether or not the condition was met.

3.2.12 Clock Generation

The clock generation circuitry resides mainly on the SQ card. It is a state machine whose four outputs are the four principal clocks which are used by the system. The state machine runs from a crystal controlled oscillator, running at 30.00 MHz. It produces three clocks which are used within the processor. These are the CAC clock, the CPU clock, and the MEM clock. It also generates the backplane SCLK signal and the timebase clock CCLK. The time relationships of these signals are shown in Figure 3-3. They all have a free running period of 133 ns and duty cycle of 50 percent.

The clock signals from the state machine are as follows:

a. The CAC clock is used by the memory addressing logic, the cache memory, and I/O interface logic. The CAC clock is frozen by the memory controller when a memory data error is being corrected.

b. The CPU clock is applied to the microprogram sequencer and data path circuits. The CPU clock (like the CAC clock) is frozen by a memory data error. Also it is frozen when the cache memory cannot meet a request of the CPU; for example when the address counter cannot be incremented because of DMA interference or when it is not able to supply read data due to a cache fault.

c. The MEM clock runs continuously and is applied to the memory controller.

d. SCLK has a period of 267 ns with a 5/8ths duty cycle; i.e., it is asserted low for five out of every eight 33 ns periods. SCLK freezes only when CAC clock freezes; i.e., during memory data errors. Note that this freeze occurs even if DMA is not the source of the memory request. SCLK is aligned with the CAC clock, so that the rising SCLK occurs on a rising edge of the CAC clock.

The CCLK clock used by the timebase generator and the I/O backplane is generated by a crystal controlled oscillator on the MC card. It has a frequency of 14.7456 Mhz.

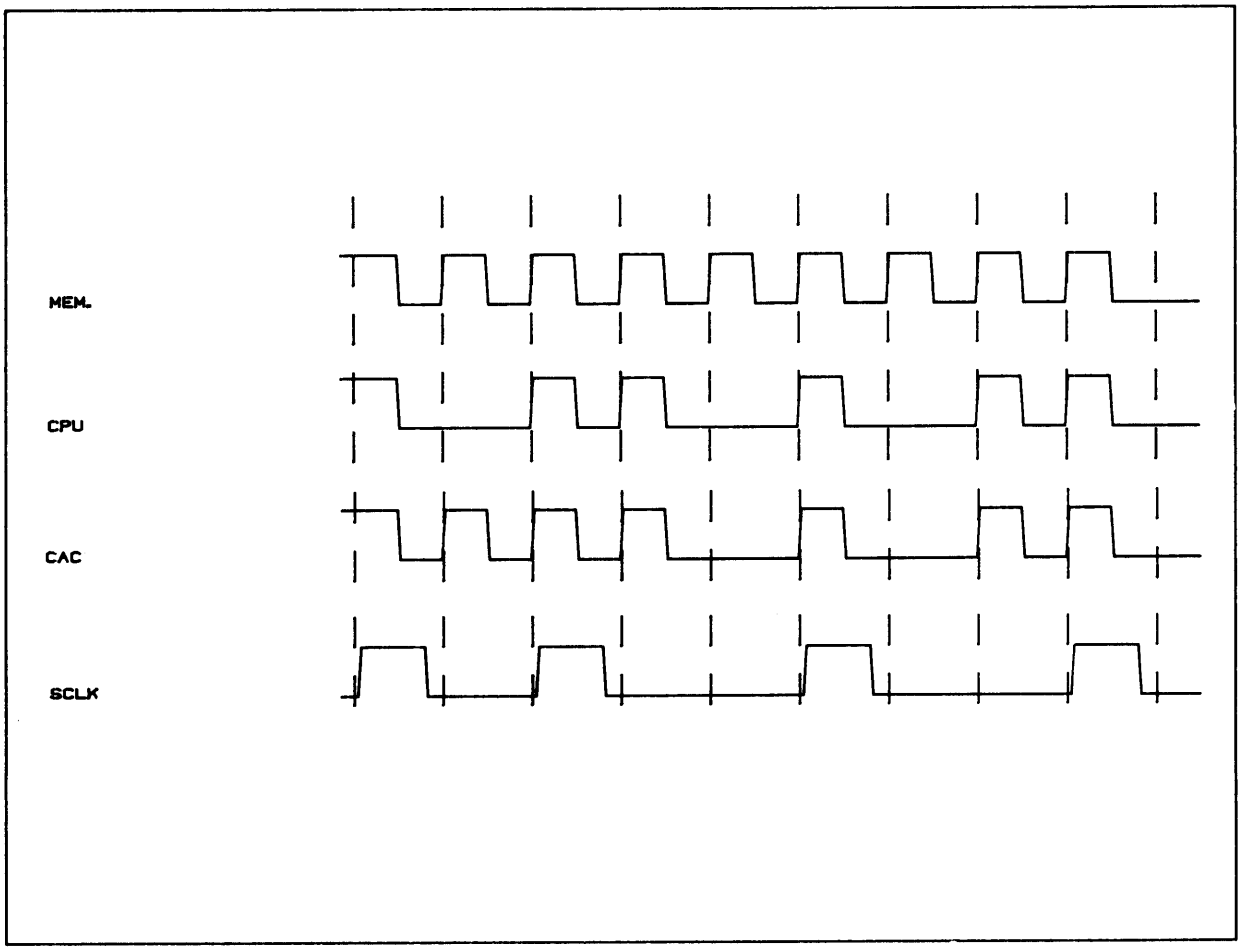


Figure 3-3. Relationships of the Major Clock Signals

3.3 Theory of Operation

The A900 Computer Sequencer card theory of operation is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 3-1 and the schematics at the end of this section of the manual. The schematic pages are referred to by a two letter card mnemonic followed by a page number; e.g., the schematics of the sequencer card are SQ1, SQ2, etc.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U0407 (SQ115C) refers to part U0407 on the sequencer card in row 4/column 7, which is shown on schematic page SQ11 at horizontal location 5 and vertical location C.

3.3.1 Next Address Selection (Op Field Related)

The address sources which are not OP field related, and the logic which controls their selection are described in later paragraphs.

The logic which generates the OP field related address is shown on sheet SQ1 and consists of the following multiplexers: At the top of the page is the 2:1 multiplexer which selects between the TARGET field (BP.UIR.REG[43:37]+ and BP.UIR.REG[7:0]+) and the RTN register (SQ.RTN.REG[14:0]+). This MUX is made from four chips, U1108 (SQ12B), U0908 (SQ14B), U0905 (SQ15B), and U1105 (SQ17B), and is always enabled.

Across the center of SQ1 is the 2:1 multiplexer which selects between the output of the upper multiplexer (SQ.TARGET.RTN[14:0]+) and the UPC register (SQ.UPC.REG[14:0]+) based on the CNDX.MET+ signal from the DP card. The UPC is selected when the CNDX.MET+ signal is "low".

The MUX that selects between the first MUX and the UPC is made from four chips U0907 (SQ12D), U0807 (SQ14D), U0805 (SQ15D), and U1005 (SQ17D). The inverted tristate outputs of this lower MUX can be enabled to drive a "low true" microaddress onto SQ.UADR[14:0]-. The lower and upper bits of the MUX can be enabled independently.

In the lower right part of the SQ1 is the inverting tristate buffer which can drive SQ.UPC.REG[14:0]+ onto SQ.UADR[14:0]-. This buffer consists of U0707 (SQ15E) and U0705 (SQ17E). The upper and lower bits have independent enables. Note that if either the lower MUX or the UPC buffer is selected to drive SQ.UADR[14:0]-, the BP.NO.EXECUTE- signal is forced "high" so that the current microinstruction executes normally.

In order to generate the proper microaddress, the OP field function through signal BP.UIR.REG[46:44]+ controls the select of the upper MUX and the output enables of the lower MUX and UPC buffer. In addition, this signal sometimes forces the CNDX.MET+ signal high (described under condition selection in the DP card section). These actions are summarized in the following table.

OP FUNCTION	UIR.REG [46:44]+	RTN or TARGET	CNDX.MET+ Forced Hi	SQ.UADR [14:8]-	SQ.UADR [7:0]-
JMPC	0 0 0	TARGET	No	UPC Buffer	Lower Mux
JMPL	0 0 1	TARGET	Yes	Lower Mux	Lower Mux
RTNC	0 1 0	RTN	No	Lower Mux	Lower Mux
RTNI	0 1 1	RTN	Yes	Lower Mux	Lower Mux
JSBC	1 0 0	TARGET	No	UPC Buffer	Lower Mux
JSBL	1 0 1	TARGET	Yes	Lower Mux	Lower Mux
SP1C	1 1 0	RTN	No	UPC Buffer	UPC Buffer
IMM	1 1 1	RTN	Yes	UPC Buffer	UPC Buffer

This table indicates that the select for the upper MUX can come directly from BP.UIR.REG45+ with the RTN register being selected when the UIR bit is high. The logic which controls the output enables is shown in the lower left corner of SQ1. It includes an inverting multiplexer U1205 (SQ13E) and a pair of inverters, U1404 (SQ12E).

This control logic looks at the three OP field bits and at SQ.R2.OP.ADR.EN- to determine the proper combination of output enables. SQ.R2.OP.ADR.EN- is a version of SQ.R1.OP.ADR.EN- which has been delayed one microcycle by the register located at U1605 (SQ105C).

A "high" SQ.R2.OP.ADR.EN- indicates that an address that is not a result of the OP field is being used during the current microcycle and, therefore, the lower MUX and UPC buffer should both be disabled. The "low true" output enables for the lower MUX are called SQ.HI.COND- and SQ.LO.COND-. The low true output enables for the UPC buffer are called SQ.HI.UNCOND- and SQ.LO.UNCOND-. The conditions which the control logic implements is tabulated below:

OP FUNCTION	UIR.REG+ [46:44]	SQ.R2.OP. ADR.EN-	SQ.HI. COND-	SQ.HI. UNCOND-	SQ.LO. COND-	SQ.LO. UNCOND-
JMPC	0 0 0	0	1	0	0	1
JMPL	0 0 1	0	0	1	0	1
RTNC	0 1 0	0	0	1	0	1
RTNI	0 1 1	0	0	1	0	1
JSBC	1 0 0	0	1	0	0	1
JSBL	1 0 1	0	0	1	0	1
SP1C	1 1 0	0	1	0	1	0
IMM	1 1 1	0	1	0	1	0
NonOP	X X X	1	1	1	1	1

The gate located at U0202 combines SQ.HI.UNCOND- with SQ.R2.AJT.JM.EN- to form the actual enable for the upper half of the UPC buffer. This half of the buffer is enabled when the OP field control logic drives SQ.HI.UNCOND- "low" or when the AJT control logic drives SQ.R2.AJT.JM.EN- "low" (refer to the paragraph on the address jump table).

The buffer which converts SQ.UADR[14:0]- to SQ.UADR[14:0]+ consists of U1501 (SQ32D) and U0404 (SQ34D). This buffer is always enabled. The spare bit is used to convert BP.NO.EXECUTE- to FP.NO.EXECUTE+ which is available on the SQ card frontplane to facilitate debug. Another buffer consisting of U0501 (SQ35D) and U0402 (SQ37D), converts SQ.UADR- to FP.UADR+. FP.UADR is available on the SQ card frontplane for use by external control store. The "low true" output enable on this buffer is driven by FP.BD.ON- which comes from external control store via the SQ card frontplane. Note that this signal must be grounded if the frontplane microaddress is being examined without external control store connected. Grounding can be accomplished by shorting two pins on the frontplane connector.

3.3.2 Control Store

The lower 24 bits of control store are shown on sheet SQ5 while the upper 24 bits are shown on sheet SQ6. The PROM banks are the following locations:

BANK 0
U0803 (SQ52D) U0802 (SQ52C) U0801 (SQ52B),
U1103 (SQ62D) U1102 (SQ62C) U1101 (SQ62B).

BANK 1
U0703 (SQ54D) U0702 (SQ54C) U0701 (SQ54B),
U1003 (SQ64D) U1002 (SQ64C) U1001 (SQ64B).

BANK 3
U0603 (SQ55D) U0602 (SQ55C) U0601 (SQ55B),
U0903 (SQ65D) U0902 (SQ65C) U0901 (SQ65B).

The first release PROMs are 27S291s, which are 2k x 8 parts in slim 24-pin packages. The card was designed so that it accepts pin compatible 4k x 8 and 8k x 8 PROMs as they become available. The outputs of each PROM are connected to the appropriate bits of FP.CS.OUT[47:0]+, and its first 11 address inputs are connected to SQ.UADR[10:0]+. Its "low true" chip select (pin 20) is connected to one of the SQ.BANK.EN[2:0]- lines depending upon its bank number. The remaining two PROM inputs are connected to SQ.PROM.A11+ and SQ.PROM.A12+. The function of these two signals varies with the size of the PROM being used according to the following table:

Signal	2k x 8	4k x 8	8k x 8
SQ.PROM.A12+	Chip Select	Chip Select	Address 12
SQ.PROM.A11+	Chip Select	Address 11	Address 11

3.3.2.1 PROM Enable Requirements

There are several requirements which must be met before a bank of PROMs is enabled. The logic which determines whether these conditions are met is shown on schematic sheet SQ9. The "on card" control store must not be enabled if the IJT has been enabled, or if either bank of external control store is being addressed. If external control store is being addressed either FP.XCS1- or FP.XCS2- go low. These signals come from the CS card via the frontplane. They are pulled high when no CS card is connected to the SQ card frontplane.

The IJT is enabled when SQ.IJT.EN- goes low. These three signals are NANDed by the gate located at U0906 (SQ92D) to produce SQ.PROM.EN- which goes high if the on-card PROMs are not enabled. This signal is used as the low true enable for a 2:4 decoder located at U1004 (SQ95C). When it is enabled, this decoder may pull one of the SQ.BANK.EN[2:0]- signals low, based on the values of SQ.BANK.SEL[1:0]-. These select signals are "low true" versions of the address bits which select between the three banks.

3.3.2.2 PROM Address Bits

The address bits selected depend on the size of the PROMs being used, so the bank select bits are generated by a 4:1 multiplexer located at U0604 (SQ94D). The select inputs of this MUX are connected to SQ.2K.0.4K.PROM- and SQ.2K.PROM- which are normally pulled "high". However, they can be pulled "low" by two switches (2k and 2k/4k) located in the DIP switch at U0204 (SQ92D). The address bits which are selected for various combinations of the two jumpers are shown in the following table:

PROM Size	2k x 8	4k x 8	8k x 8	Undefined
2k/4k Switch	in	in	out	out
2k Switch	in	out	out	in
SQ.2K.0.4K.PROM-	0	0	1	1
SQ.2K.PROM-	0	1	1	0
SQ.BANK.SEL1-	SQ.UADR12-	SQ.UADR13-	SQ.UADR14-	GND
SQ.BANK.SEL0-	SQ.UADR11-	SQ.UADR12-	SQ.UADR13-	GND

It is desirable that the on-card PROMs only show up at the bottom of the address space. That is, they should not have any images at the high end of the address space. For 8k x 8 PROMs images do not occur since the bank select bits are the top two address bits. For the 4k x 8 PROM there is one address bit remaining above the bank select bits. This leads to two copies of each PROM bank - a real one at the bottom of memory, and an image at the top of memory. Thus, the PROM can only be selected when the upper address bit is low.

For the 2k x 8 PROM there are two address bits above the bank select bits, which leads to four images - one real and three aliases. Consequently, the PROM is selected only when the top two address bits are both low. The extra chip selects of the 2k x 8 and 4k x 8 PROMs are driven by upper address bits to perform this function. However, when the SQ.PROM.A[12:11]+ bits are used as chip selects, they are be driven from different address bits than when they are used as address bits. These differences, which are a function of PROM size, are summarized below.

PROM Size	2k x 8	4k x 8	8k x 8
SQ.PROM.A12+			
Used as:	Chip Sel.	Chip Sel.	Address
Gets:	SQ.UADR14-	SQ.UADR14-	SQ.UADR12+
SQ.PROM.A11+			
Used as:	Chip Sel.	Address	Address
Gets:	SQ.UADR13-	SQ.UADR11+	SQ.UADR11+

The logic to generate SQ.PROM.A[12:11]+ consists of a pair of INVERT-OR-AND gates, U0104 (SQ96E). The gate which produces SQ.PROM.A12+ acts as an inverting 2:1 multiplexer which selects between the inverted versions of the appropriate address bits based on the state of the 2k/4k switch. Similarly, the gate which generates SQ.PROM.A11+ acts as a multiplexer which is controlled by the 2k switch. SQ.2K.O.4K.PROM+ and SQ.2K.PROM+ are generated from their "low true" versions by simply inverting paths through the PLA U0304 (SQ94E).

During a microcycle when the IJT is not enabled and an address is generated which does not fall in any bank of control store a NOCS (No Control Store) error occurs. Sixteen bits of FP.CS.OUT+ are forced during this cycle, and a microinterrupt is generated two lines later. U1602 (SQ73C) and U0403 (SQ73D)do the forcing. They are enabled by the SQ.R1.NOCS.ERR- signal going "low". The companion signal SQ.R1.NOCS.ERR+ is synchronized to the microcycle boundary by the register located at U1504 (SQ85E) to become SQ.R2.NOCS.ERR+ which is used by the microinterrupt logic. These two complementary signals are generated by the PLA located at U0304 (SQ94E).

The code for the PLA to generate the NOCS error signals is listed in Figure 3-4. PLA looks at SQ.PROM.EN- to determine if external control store or the IJT is active. It also looks at the 2k and 2k/4k jumpers and SQ.UADR[14:11]- to determine if the current address falls in the on-card control store.

Also the PLA gets an indication of which banks actually contain PROMS from SQ.BANK.IN[2:0]-. These lines are normally pulled high but they can be pulled low by three switches (BNK0, BNK1, BNK2) which are located in the DIP switch at U0204 (SQ92D). This PLA is also to invert the signals coming from the 2k and 2k/4k jumpers.

```
*
*
*                                S        S
*                                Q     S S Q
*                                .     Q Q .
*                                2     . . 2
*       S S S                    K     R R K
*       Q Q Q              S . S     1 1 . S
*       . . . S S S S      Q O Q     . . O Q
*       B B B Q Q Q Q      . . .     N N . .
*       A A A . . . .      P 4 2     O O 4 2
*       N N N U U U U      R K K     C C K K
*       K K K A A A A      O . .     S S . .
*       . . . D D D D      M P P     . . P P
*       I I I R R R R      . R R     E E R R
*       N N N 1 1 1 1      E O O     R R O O
*       2 1 0 4 3 2 1      N M M     R R M M
*       - - - - - - - - - - -        + - + +
*
*       0 0 0 0 0 0 0 1 1 0          1 1 1 1
*PIN:   7 6 5 4 3 2 1 3 1 9          9 8 7 6
*
 SENSE:                              L H H H
*                          B B B     B B B B
*ROW    6 5 4 3 2 1 0 3 1 0          9 8 7 6
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - - - - - L -          . . A .   Inverter
   1    - - - - - - - - - L          . . . A   Inverter
   2    - - - - - - - H - -          A A . .   IJT or External
   3    L - - H H L H L L L          A A . .   2K Bank 2
   4    - L - H H H L L L L          A A . .   2K Bank 1
   5    - - L H H H H L L L          A A . .   2K Bank 0
   6    L - - H L H - L L H          A A . .   4K Bank 2
   7    - L - H H L - L L H          A A . .   4K Bank 1
   8    - - L H H H - L L H          A A . .   4K Bank 0
   9    L - - L H - - L H H          A A . .   8K Bank 2
  10    - L - H L - - L H H          A A . .   8K Bank 1
  11    - - L H H - - L H H          A A . .   8K Bank 0
*
```

Figure 3-4. "No Control Store" Error Signals PLA (U0304) Code

3.3.3 Microinstruction Register and Parity

On the left-half of schematic SQ8 is the first rank of the UIR (micro-instruction register). This 48-bit register consists of six register chips, U0804 (SQ82D), U0503 (SQ82C), U1502 (SQ82B), U1203 (SQ84C), U1202 (SQ84D), and U1302 (SQ84B). The register is clocked every microcycle by the CPU clock (CK.CPU1.SQ+), the inputs are connected to FP.CS.OUT[47:0]+, and the continuously-enabled outputs drive BP.UIR.REG[47:0]+. Most of the bits of the register bus go to the backplane for use by the DP, CA, and MC boards.

The chip U1504 (SQ85E) is part of the second rank of the UIR. It is also continuously clocked and converts BP.UIR.REG[23:20]+ to BP.R2.UIR.REG[23:20]+. These signals are used on the SQ board and are also sent to the CA and MC boards via the backplane.

Parity checking of the 48-bits of BP.UIR.REG+ is accomplished as follows:

a. The control-store parity checking logic is shown at the right side of schematic SQ8. It is a two-level parity tree based on the type-74S280 nine-input parity generator. Two generators, U0401 (SQ85C) and U1503 (SQ85B), generate parity on the 16 NOCS bits ([46:44], [25:20], and [14:8]). For odd parity of NOCS the AOI gate at U0103 (SQ87A) combines the outputs of the two generators U0401 and U1503 to form the signal SQ.8.46.OD+ which goes "high". This signal is read as bit-7 of the UINT register.

b. Generators U0904 (SQ85D), U1204 (SQ87D), and U1303 (SQ87C) check parity on 27 more bits.

c. The generator at U1304 (SQ87B) checks the remaining five bits of the UIR as well as combining the output signals from the first layer of generators. This produces the signal SQ.CSPAR.ERR+ which is "high" when the parity is even and "low" when the parity is odd. Signal CSPAR.ERR+ is used by the microinterrupt logic.

3.3.4 Microprogram Counter

The incrementer used by the UPC and stack-input registers is shown across the top of schematic SQ3. It consists of four adders, U0806 (SQ32B), U1006 (SQ34B), U0205 (SQ35B), and U0105 (SQ37B). The carry input to the lower adder is driven "high", while the carry is rippled through the remaining stages. The "A" inputs are tied low, while the "B" input receives the microaddress from SQ.UADR[14:0]+. The incremented outputs drive SQ.INCD.UADR[14:0]+.

The 15-bit UPC consists of U0607 (SQ35C) and U0505 (SQ37C). The register is loaded with the incremented microaddress from SQ.INCD.UADR[14:0]+ at the end of each CPU clock. Its outputs drive SQ.UPC.REG[14:0]+ which is used by the OP field address selection logic. The spare 16th bit of the register is used as one of two levels of PON synchronization. It converts LBP.PON+ to SQ.R1.PON+.

3.3.5 Subroutine Save Stack

The stack is shown on schematic SQ4. The stack input register consists of U0407 (SQ42B) and U0405 (SQ44B). It is loaded from SQ.INCD.UADR[14:0]+ at the rise of each CPU clock. Its outputs are enabled to drive SQ.STK.DATA[14:0]+ whenever SQ.STK.PUSH- is "low".

The RTN register consists of U0708 (SQ45B) and U0605 (SQ47B). It is loaded from SQ.STK.DATA[14:0]+ at every rise of the CPU clock. Its outputs continually drive SQ.RTN.REG[14:0]+ which is used by the OP field address generation logic. The spare 16th bit of this register is used as the second stage of the PON synchronizer. It converts SQ.R1.PON+ to SQ.R2.PON+. The stack RAM consists of 16 by 4 high speed RAMS, U0506 (SQ42C), U0606 (SQ44C), U0406 (SQ45C), and U0306 (SQ47C).

The RAM address inputs are connected to SQ.STK.ADDR[3:0]+. The addressed location is driven onto SQ.STK.DATA[14:0]+ whenever CK.MEM.D20.SQ+ (SQ.STK.CS-) is "low" and CK.MEM.D50.STK- (SQ.STK.WE-) is "high" (CK.MEM.D10.STK.SQ+ (CS-) is "low" and CK.MEM.D50.STK.SQ- (WE-) is "high"). If the CS- and WE- signals are both "low", the data from SQ.STK.DATA[14:0]+ is written into the addressed location. The WE- signal is generated by a gate U0906 (SQ45D). It is a function of SQ.STK.PUSH+, a delayed version of the microcycle clock. The timing of the CS- and WE- signals is shown in Figure 3-5.

NOTE: Because delayed clocks never freeze if a push occurs while the CPU microcycle is frozen, the value being pushed will be written into the same location several times without harmful consequences.

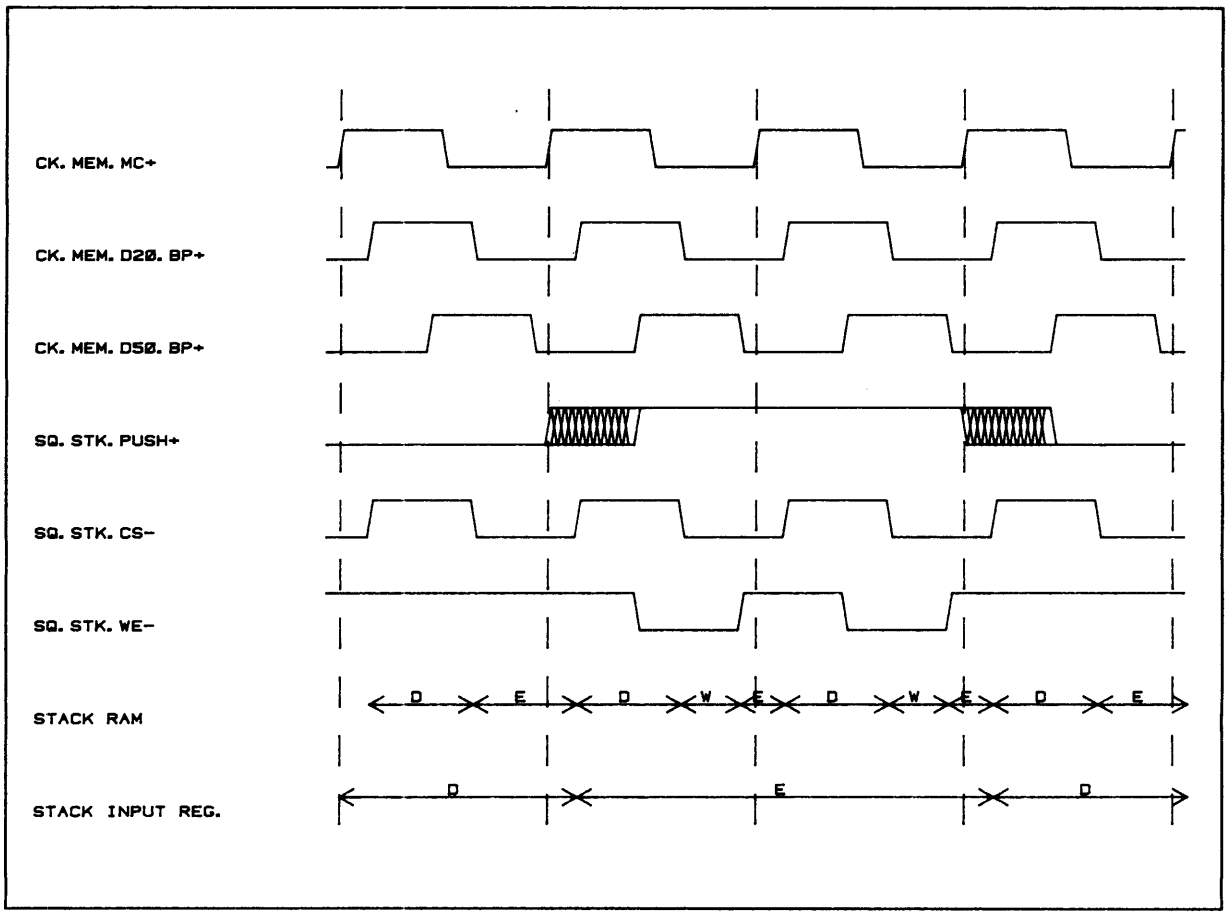


Figure 3-5. Subroutine Stack Timing

The stack is controlled by a simple state machine whose four state variables form the "stack pointer". The state machine consists of a 512 by 8 PROM U1206 (SQ43E) and U1106 (SQ45E).

The register holds the four-state variables called SQ.STK.PNTR[3:0]+, and is clocked at the rise of each CPU clock. The PROM produces SQ.STK.ADDR[3:0]+ which does the following:

1. Addresses the stack RAM and is the input to the state register.

2. Generates both senses of SQ.STK.PUSH that control the stack as described above.

3. Generates two signals relating to stack errors. SQ.STK.OVF+ goes "high" when a stack overflow occurs (JSB with Stack Pointer = 17 octal).

SQ.STK.UND.OVF+ goes "high" when an overflow occurs or when a stack underflow occurs (RTN with Stack Pointer = 0).

The inputs to the PROM include its four state variables SQ.STK.PNTR[3:0]+. In addition, the OP field bits BP.UIR.REG[46:45]+ indicate what type of stack operation should be performed. SQ.ZAP.1XXX+ is also an input. When it is "high", OP/JSBC will do an unconditional push. This feature is used only by self-test. BP.CNDX.MET+ is also sent to the PROM so that it can decide if conditional operations should be done. Finally, SQ.JTAB.MEM+ resets the stack pointer to zero when MEM/JTAB or MEM/JTDI occurs.

The function of the PROM is straight forward. Normally, SQ.STK.PNTR[3:0]+ is passed directly to SQ.STK.ADDR[3:0]+, and SQ.STK.PUSH is deasserted. During an operation requiring a pop, SQ.STK.ADDR[3:0]+ receives a decremented version of SQ.STK.PNTR[3:0]+. During an operation which requires a push, SQ.STK.PUSH is asserted and SQ.STK.ADDR[3:0]+ receives an incremented version of SQ.STK.PNTR[3:0]+.

3.3.6 Instruction Jump Table

The IJT is shown on the right half of schematic SQ7. It consists of five PLAs, U0704 (SQ75D), U0302 (SQ75C), U0502 (SQ75B), U1201 (SQ77D), and U1301 (SQ77C), and one U1401 buffer (SQ77A). The PLAs all receive BP.S.BUS[15:7]+ as inputs. The IJT drives FP.CS.OUT[47:0]+ when SQ.IJT.EN- is "low". This enable signal is generated by gates at U1404 (SQ108C), U0608 (SQ106D), and U1608 (SQ103B) which implement the following equation:

```
not(SQ.IJT.EN-) =  BP.UIR.REG13+ and
                   BP.UIR.REG14+ and
                   SQ.R2.PON+    and
                   SQ.ZAP.ONES-  and
                   SQ.R2.UIV.EN-
```

In other words the IJT is enabled if a JTAB or JTDI is present, power is up, the ZAP counter is not timing out, and a microinterrupt did not occur in the previous cycle.

The buffer drives FP.CS.OUT[45:38]+, and the rest of the bits are driven by the PLAs. The following table indicates which bits are driven by which PLA.

Type	Chip	Program	Drives FP.CS.OUT+
82S153	U0704	Fig. 3-6	[7:0]
82S153	U0302	Fig. 3-7	[15:8]
82S153	U0502	Fig. 3-8	[23:16]
82S153	U1201	Fig. 3-9	[31:24]
82S153	U1301	Fig. 3-10	[47:46] and [37:32]

The code listing for the Instruction Jump Table PLAs are shown in Figure 3-6, 3-7, 3-8, 3-9, and 3-10.

3.3.7 Next Address Selection (Not OP Field Related)

The OP field bits and BP.CNDX.MET+ affect the selection of the address in the same microcycle that the address is being used. All other address selection decisions are made one microcycle before the address is used. Thus, during the present microcycle, logic must choose whether UIV, VECT, the AJT, or the OP field address will be used in the following microcycle:.

The logic chooses UIV if:

a. A microinterrupt is pending.

b. A macrointerrupt or single step is pending during a JTAB line.

c. A macrointerrupt is pending after the address generation logic has resolved three levels of indirect.

The logic may choose the following:

a. The AJT during a JTAB line if no interrupt is pending.

b. The VECT during a line containing a SP2/JMPV.

c. The OP field address if none of the above conditions exist.

The logic which makes this choice is centered around the Next Address PLA U1405 (SQ103C).

The coding for the Next Address PLA is listed in Figure 3-11.

The PLA inputs include all the interrupt sources as follows:

1. SQ.R2.NOCS.ERR+ being "high" indicates that an access to non-existent control store occurred in the previous microcycle.

2. .CSPAR.ERR+ indicates a control store parity error during the present microcycle when it goes "high".

3. SQ.STK.UND.OVFL+ goes "high" to indicate that a stack underflow or overflow is occurring in the current microcycle.

4. SQ.ZAP.ONES+ goes "high" when the ZAP counter is at octal 17.

5. BP.MISSED.TICK- goes "low" when logic on the MC card determines that firmware has not serviced a TBG tick quickly enough. Since the MC board uses an unfreezable version of the microcycle clock, the falling edge of BP.MISSED.TICK- must cause the microinterrupt. The falling edge is used by delaying BP.MISSED.TICK- in register U1605 (SQ105C) to form the SQ.R2.MISSED.TICK- input to the. A microinterrupt is caused only when the delayed signal is "high" and the undelayed signal is "low" which occurs only at the falling edge of the signal. The signal is pulled "high" when the MC board is not plugged-in to prevent spurious interrupts.

6. BP.JTAB.INT- is driven "low" by logic on the MC board if an unmasked macrointerrupt or single step is pending during a JTAB line. It is ignored at all other times.

7. BP.IND.INT+ is driven "high" by logic in the CA board if an unmasked interrupt is pending and an indirect resolution has taken three or more cycles. It is pulled "high" when the CA board is not plugged in to prevent spurious interrupts from occurring.

8. SQ.JTAB.MEM+ is generated by the gate at U0608 (SQ103B) and goes "high" when power is up and a MEM/JTAB or MEM/JTDI occurs.

9. SQ.R2.UIV.EN- goes "low" if a microinterrupt occurs in the previous cycle.

10. SQ.JMPV.SP2- is generated by the PLA at U1606 (SQ103B) and goes "low" when an SP2/JMPV occurs.

11. SQ.R2.PON+ is the fully synchronized version of LBP.PON+.

```
*                                      F F F F F F F F
*                                      P P P P P P P P
*       B B B B B B B B S B            . . . . . . . .
*       P P P P P P P P Q P            C C C C C C C C
*       . . . . . . . . . .            S S S S S S S S
*       S S S S S S S S I S            . . . . . . . .
*       B B B B B B B B J B            0 0 0 0 0 0 0 0
*       U U U U U U U U T U            U U U U U U U U
*       S S S S S S S S . S            T T T T T T T T
*       1 1 1 1 1 0 0 0 E 1            0 0 0 0 0 0 0 0
*       4 3 2 1 0 9 8 7 N 5            7 6 5 4 3 2 1 0
*       + + + + + + + + - +            + + + + + + + +
*       0 0 0 0 0 0 0 0 1 0            1 1 1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 1 9            9 8 7 6 5 4 3 2
 SENSE:                                H H H H H H H H
*                       B B            B B B B B B B B
*ROW    7 6 5 4 3 2 1 0 1 0            9 8 7 6 5 4 3 2
*_ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
   0    L L H L - - - - - L            . . . . . . . .     AND,D
   1    L H L L - - - - - L            . . . . . . . .     XOR,D
   2    L H H L - - - - - L            . . . . . . . .     IOR,D
   3    L L H H - - - - - L            . . . . . . . .     JSB,D
   4    L L H H - - - - - H            . . . . . . . .     JSB,I
   5    L H L H - - - - - L            . . . . . A . .     JMP,D
   6    L H H H - - - - - L            . . . . . . . .     ISZ,D
   7    H L L - - - - - - L            . . . . . . . .     AD*,D
   8    H L H - - - - - - L            . . . . . . . .     CP*,D
   9    H H L - - - - - - L            . . . . . . . .     LD*,D
  10    H H H - - - - - - L            . . . . . . . .     ST*,D
  11    H H H - - - - - - H            . . . . . . . .     ST*,I
  12    H L - - - - - - - H            . . . . . . . .     AND,I XOR,I
  13    L H - - - - - - - H            . . . . . . . .     IOR,I JMP,I
  14    - H L - - - - - - H            . . . . . . . .     ISZ,I AD*,I
  15    L - H L - - - - - H            . . . . . . . .     CP*,I LD*,I
  16    L L L L L - - - - L            . . . . . A A .     SRGA
  17    L L L H L - - - - L            . . . . . A A .     SRGB
  18    L L L - H H L - - L            . . . . . A . A     ASGCM*
  19    L L L - H L H - - L            . . . . . A . A     ASGCL*
  20    L L L - H H H - - L            . . . . . A . A     ASGCC*
  21    L L L - H L L - - L            . . . . . A . A     ASG*
  22    L L L - H - - - - H            . A A . . . . .     IOG
  23    L L L - L L - H - H            . . . . . . . .     MPY,DLD
  24    L L L L L L H L - H            . . . . . . . .     DIV
  25    L L L H L L H L - H            . . . . . . . .     DST
  26    L L L - L L L L - H            . . . . . . . .     ASL,LSL,RRL
  27    L L L L L H L L - H            . . . . . . . .     ASR,LSR,RRR
  28    L L L - L H H H - H            . . . . . . . .     EIG,DMS,ECT.
  29    L L L - L H L H - H            . . . . . . . .     SIS,LIS,VMA,ECT.
  30    L L L - L H H L - H            . . . . . . . .     RESERVED
  31    L L L H L H L L - H            . . . . . . . .     DII,VIS,FLT PT,ECT.
 D2-D9  - - - - - - - - L -            ^ ^ ^ ^ ^ ^ ^ ^
```

Figure 3-6. Instruction Jump Table PLA (U0704) Coding

5d 75b

```
*                                       F F F F F F F F
*                                       P P P P P P P P
*         B B B B B B B B S B           . . . . . . . .
*         P P P P P P P P Q P           C C C C C C C C
*         . . . . . . . . . .           S S S S S S S S
*         S S S S S S S S I S           . . . . . . . .
*         B B B B B B B B J B           0 0 0 0 0 0 0 0
*         U U U U U U U U T U           U U U U U U U U
*         S S S S S S S S . S           T T T T T T T T
*         1 1 1 1 1 0 0 0 E 1           1 1 1 1 1 1 0 0
*         4 3 2 1 0 9 8 7 N 5           5 4 3 2 1 0 9 8
*         + + + + + + + + - +           + + + + + + + +
*         0 0 0 0 0 0 0 0 1 0           1 1 1 1 1 1 1 1
*PIN:     8 7 6 5 4 3 2 1 1 9           9 8 7 6 5 4 3 2
 SENSE:                                 H H H H H H H H
*                               B B     B B B B B B B B
*ROW      7 6 5 4 3 2 1 0 1 0           9 8 7 6 5 4 3 2
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0      L L H L - - - - - L           A . . A . . . .   AND,D
   1      L H L L - - - - - L           A . . A . . . .   XOR,D
   2      L H H L - - - - - L           A . . A . . . .   IOR,D
   3      L L H H - - - - - L           A . . A A . A .   JSB,D
   4      L L H H - - - - - H           A . . A . . . .   JSB,I
   5      L H L H - - - - - L           . A A A A A . A   JMP,D
   6      L H H H - - - - - L           A . A A A . A .   ISZ,D
   7      H L L - - - - - - L           A . . A . . . .   AD*,D
   8      H L H - - - - - - L           A . . . . . . .   CP*,D
   9      H H L - - - - - - L           . . . A . . . .   LD*,D
  10      H H H - - - - - - L           A . A A A . A .   ST*,D
  11      L H L H - - - - - H           A . A A A A . .   JMP,I
  12      H - - - - - - - - H           A . A A . . . .   AND,I XOR,I
  13      - H - L - - - - - H           A . A A . . . .   IOR,I ST*,I
  14      - H H - - - - - - H           A . A A . . . .   ISZ,I AD*,I
  15      - - H L - - - - - H           A . A A . . . .   CP*,I LD*,I
  16      L L L L L - - - - L           A . . A A . A .   SRGA
  17      L L L H L - - - - L           A . . A A . A .   SRGB
  18      L L L - H H L - - L           A . . A A . A .   ASGCM*
  19      L L L - H L H - - L           A . . A A . A .   ASGCL*
  20      L L L - H H H - - L           A . . A A . A .   ASGCC*
  21      L L L - H L L - - L           A . . A A . A .   ASG*
  22      L L L - H - - - - H           A . . A . . . A   IOG
  23      L L L - L L - H - H           A A . . . . . .   MPY,DLD
  24      L L L L L L H L - H           A A . . . . . .   DIV
  25      L L L H L L H L - H           A A . . . . . .   DST
  26      L L L - L L L L - H           A . . . A . A .   ASL,LSL,RRL
  27      L L L L L H L L - H           A . . . A . A .   ASR,LSR,RRR
  28      L L L - L H H H - H           . A . . . A A .   EIG,DMS,ECT.
  29      L L L - L H L H - H           . A . . . . . .   SIS,LIS,VMA,ECT.
  30      L L L - L H H L - H           . A . . . . . .   RESERVED
  31      L L L H L H L L - H           . A . . . . . .   DII,VIS,FLT PT,ECT.
 D2-D9    - - - - - - - - L -           ^ ^ ^ ^ ^ ^ ^ ^
```

Figure 3-7. Instruction Jump Table PLA (U0302) Coding

SQ 75 C

```
*                                  F F F F F F F F
*                                  P P P P P P P P
*      B B B B B B B B S B         . . . . . . . .
*      P P P P P P P P Q P         C C C C C C C C
*      . . . . . . . . . .         S S S S S S S S
*      S S S S S S S S I S         . . . . . . . .
*      B B B B B B B B J B         O O O O O O O O
*      U U U U U U U U T U         U U U U U U U U
*      S S S S S S S S . S         T T T T T T T T
*      1 1 1 1 1 0 0 0 E 1         2 2 2 2 1 1 1 1
*      4 3 2 1 0 9 8 7 N 5         3 2 1 0 9 8 7 6
*      + + + + + + + + - +         + + + + + + + +
*      0 0 0 0 0 0 0 0 1 0         1 1 1 1 1 1 1 1
*PIN:  8 7 6 5 4 3 2 1 1 9         9 8 7 6 5 4 3 2
 SENSE:                            H H H H H H H H
*                      B B         B B B B B B B B
*ROW   7 6 5 4 3 2 1 0 1 0         9 8 7 6 5 4 3 2
*_ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
   0   L L H L - - - - - L         . . . . A . . .     AND,D
   1   L H L L - - - - - L         . . . . . . . .     XOR,D
   2   L H H L - - - - - L         . . . . . A . .     IOR,D
   3   L L H H - - - - - L         . . . . A A A A     JSB,D
   4   L L H H - - - - - H         . . . . A A A A     JSB,I
   5   L H L H - - - - - L         . . . . A A . .     JMP,D
   6   L H H H - - - - - L         A A A . A . A .     ISZ,D
   7   H L L - - - - - - L         . . . . A . . A     AD*,D
   8   H L H - - - - - - L         . . . . . . . .     CP*,D
   9   H H L - - - - - - L         . . . . A A . .     LD*,D
  10   H H H - - - - - - L         A A A . A A A A     ST*,D
  11   H H H - - - - - - H         A A A . A A A A     ST*,I
  12   H L - - - - - - - H         . . . . A A A A     AND,I XOR,I
  13   L H - - - - - - - H         . . . . A A A A     IOR,I JMP,I
  14   - H L - - - - - - H         . . . . A A A A     ISZ,I AD*,I
  15   L - H L - - - - - H         . . . . A A A A     CP*,I LD*,I
  16   L L L L L - - - - L         . A . . A A . A     SRGA
  17   L L L H L - - - - L         . A . . A A . A     SRGB
  18   L L L - H H L - - L         . . . . . A A .     ASGCM*
  19   L L L - H L H - - L         . . . . A . . A     ASGCL*
  20   L L L - H H H - - L         . . . . . A A .     ASGCC*
  21   L L L - H L L - - L         . . . . A . . A     ASG*
  22   L L L - H - - - - H         . . . . A . . .     IOG
  23   L L L - L L - H - H         . . . . A A A A     MPY,DLD
  24   L L L L L L H L - H         . . . . A A A A     DIV
  25   L L L H L L H L - H         A A A . A A A A     DST
  26   L L L - L L L L - H         . . . . A A A .     ASL,LSL,RRL
  27   L L L L L H L L - H         . . . . . . . A     ASR,LSR,RRR
  28   L L L - L H H H - H         A . A . A . . A     EIG,DMS,ECT.
  29   L L L - L H L H - H         . . . . A A . .     SIS,LIS,VMA,ECT.
  30   L L L - L H H L - H         A . A . A A A A     RESERVED
  31   L L L H L H L L - H         . . . . A A . .     DII,VIS,FLT PT,ECT.
 D2-D9 - - - - - - - - L -         ^ ^ ^ ^ ^ ^ ^ ^
```

Figure 3-8. Instruction Jump Table PLA (U0502) Coding

5?75?

*											F	F	F	F	F	F	F	F	
*											P	P	P	P	P	P	P	P	
*		B	B	B	B	B	B	B	B	S	B	.	.	.	.	.	.	.	.	
*		P	P	P	P	P	P	P	P	Q	P	C	C	C	C	C	C	C	C	
*		.	.	.	.	.	.	.	.	.	.	S	S	S	S	S	S	S	S	
*		S	S	S	S	S	S	S	S	I	S	.	.	.	.	.	.	.	.	
*		B	B	B	B	B	B	B	B	J	B	O	O	O	O	O	O	O	O	
*		U	U	U	U	U	U	U	U	T	U	U	U	U	U	U	U	U	U	
*		S	S	S	S	S	S	S	S	.	S	T	T	T	T	T	T	T	T	
*		1	1	1	1	1	0	0	0	E	1	3	3	2	2	2	2	2	2	
*		4	3	2	1	0	9	8	7	N	5	1	0	9	8	7	6	5	4	
*		+	+	+	+	+	+	+	+	-	+	+	+	+	+	+	+	+	+	
*		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	
*PIN:		8	7	6	5	4	3	2	1	1	9	9	8	7	6	5	4	3	2	
SENSE:												H	H	H	H	H	H	H	H	
*										B	B	B	B	B	B	B	B	B	B	
*ROW		7	6	5	4	3	2	1	0	1	0	9	8	7	6	5	4	3	2	
*-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0		L	L	H	L	-	-	-	-	-	L	A	A	.	.	.	.	A	A	AND,D
1		L	H	L	L	-	-	-	-	-	L	A	A	.	.	.	.	A	A	XOR,D
2		L	H	H	L	-	-	-	-	-	L	A	A	.	.	.	.	A	A	IOR,D
3		L	L	H	H	-	-	-	-	-	L	A	.	.	.	.	.	.	.	JSB,D
4		L	L	H	H	-	-	-	-	-	H	.	.	A	.	.	.	.	.	JSB,I
5		L	H	L	H	-	-	-	-	-	L	A	A	.	.	.	.	.	A	JMP,D
6		L	H	H	H	-	-	-	-	-	L	A	A	.	.	.	.	.	.	ISZ,D
7		H	L	L	-	-	-	-	-	-	L	A	A	.	.	.	.	A	.	AD*,D
8		H	L	H	-	-	-	-	-	-	L	A	A	.	.	.	.	.	.	CP*,D
9		H	H	L	-	-	-	-	-	-	L	A	A	.	.	.	.	A	.	LD*,D
10		H	H	H	-	-	-	-	-	-	L	A	.	.	.	.	.	.	.	ST*,D
11		H	H	H	-	-	-	-	-	-	H	.	.	A	.	.	.	.	.	ST*,I
12		H	L	-	-	-	-	-	-	-	H	.	.	A	.	.	.	.	.	AND,I XOR,I
13		L	H	-	-	-	-	-	-	-	H	.	.	A	.	.	.	.	.	IOR,I JMP,I
14		-	H	L	-	-	-	-	-	-	H	.	.	A	.	.	.	.	.	ISZ,I AD*,I
15		L	-	H	L	-	-	-	-	-	H	.	.	A	.	.	.	.	.	CP*,I LD*,I
16		L	L	L	L	L	-	-	-	-	L	A	.	.	.	.	.	.	A	SRGA
17		L	L	L	H	L	-	-	-	-	L	A	.	.	.	.	A	.	A	SRGB
18		L	L	L	-	H	H	L	-	-	L	.	.	.	A	A	A	A	.	ASGCM*
19		L	L	L	-	H	L	H	-	-	L	.	.	.	A	A	A	A	.	ASGCL*
20		L	L	L	-	H	H	H	-	-	L	.	.	.	A	A	A	A	.	ASGCC*
21		L	L	L	-	H	L	L	-	-	L	.	.	.	A	A	A	A	.	ASG*
22		L	L	L	-	H	-	-	-	-	H	.	A	.	.	.	.	.	.	IOG
23		L	L	L	-	L	L	-	H	-	H	.	.	A	.	.	.	.	.	MPY,DLD
24		L	L	L	L	L	L	H	L	-	H	.	.	A	.	.	.	.	.	DIV
25		L	L	L	H	L	L	H	L	-	H	.	.	A	.	.	.	.	.	DST
26		L	L	L	-	L	L	L	L	-	H	A	.	.	.	.	.	A	.	ASL,LSL,RRL
27		L	L	L	L	L	H	L	L	-	H	.	A	.	.	.	.	.	A	ASR,LSR,RRR
28		L	L	L	-	L	H	H	H	-	H	.	.	A	.	.	.	.	A	EIG,DMS,ECT.
29		L	L	L	-	L	H	L	H	-	H	.	.	A	.	.	.	A	A	SIS,LIS,VMA,ECT.
30		L	L	L	-	L	H	H	L	-	H	.	.	A	.	.	.	A	A	RESERVED
31		L	L	L	H	L	H	L	L	-	H	.	.	A	.	.	.	A	A	DII,VIS,FLT PT,ECT.
D2-D9		-	-	-	-	-	-	-	-	L	-	^	^	^	^	^	^	^	^	

Figure 3-9. Instruction Jump Table PLA (U1201) Coding

SQ 77 B

*																			
*											F	F	F	F	F	F	F	F	
*											P	P	P	P	P	P	P	P	
*		B	B	B	B	B	B	B	B	S	B	.	.	.	.	.	.	.	.	
*		P	P	P	P	P	P	P	P	Q	P	C	C	C	C	C	C	C	C	
*		.	.	.	.	.	.	.	.	.	.	S	S	S	S	S	S	S	S	
*		S	S	S	S	S	S	S	S	I	S	.	.	.	.	.	.	.	.	
*		B	B	B	B	B	B	B	B	J	B	0	0	0	0	0	0	0	0	
*		U	U	U	U	U	U	U	U	T	U	U	U	U	U	U	U	U	U	
*		S	S	S	S	S	S	S	S	.	S	T	T	T	T	T	T	T	T	
*		1	1	1	1	1	0	0	0	E	1	4	4	3	3	3	3	3	3	
*		4	3	2	1	0	9	8	7	N	5	7	6	7	6	5	4	3	2	
*		+	+	+	+	+	+	+	+	-	+	+	+	+	+	+	+	+	+	
*		0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	1	
*PIN:		8	7	6	5	4	3	2	1	1	9	9	8	7	6	5	4	3	2	
SENSE:												H	H	H	H	H	H	H	H	
*										B	B	B	B	B	B	B	B	B	B	
*ROW		7	6	5	4	3	2	1	0	1	0	9	8	7	6	5	4	3	2	
*	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

0	L	L	H	L	-	-	-	-	-	L	.	A	.	.	.	.	.	.	AND,D	
1	L	H	L	L	-	-	-	-	-	L	A	A	.	.	.	.	.	.	XOR,D	
2	L	H	H	L	-	-	-	-	-	L	.	A	.	.	.	.	.	.	IOR,D	
3	L	L	H	H	-	-	-	-	-	L	.	A	.	.	.	.	.	.	JSB,D	
4	L	L	H	H	-	-	-	-	-	H	.	A	.	.	.	.	.	.	JSB,I	
5	L	H	L	H	-	-	-	-	-	L	A	A	A	A	.	.	.	.	JMP,D	
6	L	H	H	H	-	-	-	-	-	L	A	A	.	.	A	A	.	.	ISZ,D	
7	H	L	L	-	-	-	-	-	-	L	.	A	.	.	A	A	A	A	AD*,D	
8	H	L	H	-	-	-	-	-	-	L	.	A	.	.	A	A	A	A	CP*,D	
9	H	H	L	-	-	-	-	-	-	L	A	A	.	.	A	A	A	A	LD*,D	
10	H	H	H	-	-	-	-	-	-	L	.	A	.	.	A	A	A	A	ST*,D	
11	H	H	H	-	-	-	-	-	-	H	.	A	.	.	A	A	A	A	ST*,I	
12	H	L	-	-	-	-	-	-	-	H	A	A	.	.	.	.	.	.	AND,I XOR,I	
13	L	H	-	-	-	-	-	-	-	H	A	A	.	.	.	.	.	.	IOR,I JMP,I	
14	-	H	L	-	-	-	-	-	-	H	A	A	.	.	.	.	.	.	ISZ,I AD*,I	
15	L	-	H	L	-	-	-	-	-	H	A	A	.	.	.	.	.	.	CP*,I LD*,I	
16	L	L	L	L	L	-	-	-	-	L	A	A	.	.	.	.	.	.	SRGA	
17	L	L	L	H	L	-	-	-	-	L	A	A	.	.	.	.	.	A	SRGB	
18	L	L	L	-	H	H	L	-	-	L	A	A	.	.	A	A	A	A	ASGCM*	
19	L	L	L	-	H	L	H	-	-	L	A	A	A	.	.	A	A	A	ASGCL*	
20	L	L	L	-	H	H	H	-	-	L	A	A	A	.	.	A	A	A	ASGCC*	
21	L	L	L	-	H	L	L	-	-	L	A	A	.	.	A	A	A	A	ASG*	
22	L	L	L	-	H	-	-	-	-	H	.	A	A	A	.	.	.	.	IOG	
23	L	L	L	-	L	L	-	H	-	H	.	A	.	.	.	.	.	.	MPY,DLD	
24	L	L	L	L	L	L	H	L	-	H	.	A	.	.	.	.	.	.	DIV	
25	L	L	L	H	L	L	H	L	-	H	A	A	.	.	.	.	.	.	DST	
26	L	L	L	-	L	L	L	L	-	H	.	A	.	.	.	.	.	A	ASL,LSL,RRL	
27	L	L	L	L	L	H	L	L	-	H	A	A	.	.	A	A	.	.	ASR,LSR,RRR	
28	L	L	L	-	L	H	H	H	-	H	A	A	.	.	A	A	A	.	EIG,DMS,ECT.	
29	L	L	L	-	L	H	L	H	-	H	A	A	A	A	.	A	.	A	SIS,LIS,VMA,ECT.	
30	L	L	L	-	L	H	H	L	-	H	.	A	A	A	A	A	.	A	RESERVED	
31	L	L	L	H	L	H	L	L	-	H	A	A	.	.	.	.	.	.	DII,VIS,FLT PT,ECT.	
D2-D9	-	-	-	-	-	-	-	-	L	-	^	^	^	^	^	^	^	^		

Figure 3-10. Instruction Jump Table PLA (U1301) Coding

50 77 c

```
*
*                         S
*                         Q
*                         .           S
*       F       B S   S   R           Q   S
*       P       P Q   Q   2         S .   Q S
*       .       . . S . S .         S Q R S . Q
*       S B   S M S Q R Q M S       Q . 1 Q U .
*       Q P B Q I T . 2 . I Q       . R . . I T
*       . . P . S K C . R S . S     R 1 O R N B
*       J J . Z S . S N 2 S J Q     1 . P 1 T G
*       T T I A E U P O . E M .     . V . . P .
*       A A N P D N A C U D P R     U E A A . M
*       B B D . . D R S I . V 2     I C D J P I
*       . . . O T . . . V T . .     V T R T U S
*       M I I N I O E E . I S P     . . . . L S
*       E N N E C V R R E C P O     E E E E S E
*       M T T S K F R R N K 2 N     N N N N E D
*       + - - + - + + + - - - +     - - - - + +
*
*       0 0 0 0 0 0 0 0 1 1 1 0     1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 5 2 1 9     9 8 7 6 4 3
*
 SENSE:                             L L L L H H
*                       B B B B     B B B B B B
*ROW    7 6 5 4 3 2 1 0 5 2 1 0     9 8 7 6 4 3
*_ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _ _
   0    H L - L - - - - H - - H     A . . . . .   JTAB INTERRUPT
   1    - - L - - - - - H - - H     A . . . . .   INDIRECT INTERRUPT
   2    L - - H - - - - H - - H     A . . . A .   ZAP INTERRUPT
   3    - - - - L - - - H H - H     A . . . A A   TBG MISSED INTERRUPT
   4    - - - - - H - - H - - H     A . . . A .   STACK INTERRUPT
   5    - - - - - - H - - - - H     A . . . A .   CS PARITY INTERRUPT
   6    - - - - - - - H H - - H     A . . . A .   NO CS INTERRUPT
   7    - - - - - - - - - - - L     A . . . . .   POWER NOT STABLE
   8    H H H L H L L L H - - H     . . . A . .   AJT ENABLE
   9    H H H L - L L L H L - H     . . . A . .   AJT ENABLE
  10    L - H L H L L L H - L H     . A . . . .   VECT ENABLE
  11    L - H L - L L L H L L H     . A . . . .   VECT ENABLE
  12    L - H L H L L L H - H H     . . A . . .   OP ADDRESS ENABLE
  13    L - H L - L L L H L H H     . . A . . .   OP ADDRESS ENABLE
  14    H - H H H L L L H - H H     . . A . . .   OP ADDRESS ENABLE
  15    H - H H - L L L H L H H     . . A . . .   OP ADDRESS ENABLE
  16    - - - - - - L - L - - H     . . A . . .   OP ADDRESS ENABLE
```

Figure 3-11. Next Address PLA (U1405) Coding

52 103c

The PLA produces four signals which indicate which address to use in the following microcycle:

1. SQ.R1.UIV.EN- goes "low" if the UIV address should be used in the following microcycle.

2. SQ.R1.AJT.EN- goes "low" if the AJT address should be used in the following microcycle.

3. SQ.R1.VECT.EN- goes "low" if the VECT address should be used in the following microcycle.

4. SQ.R1.OP.ADR.EN- goes "low" if the OP field address should be used in the following microcycle.

The PLA produces two additional outputs:

1. SQ.TBG.MISSED+ goes "high" when a falling edge is detected in BP.MISSED.TICK-.

2. SQ.UINTP.PULSE+ goes "high" whenever one of the five "high true" microinterrupt signals goes "high".

Note that because the microinterrupt conditions occur for only one microcycle, this signal is usually a one microcycle long pulse.

There is a priority order in the selection of the address source. In general:

a. UIV is selected over AJT.

b. AJT is selected over VECT.

c. VECT is selected over the OP field address (refer to the exception below).

Because detecting a TBG.MISSED microinterrupt requires the ANDing of two inputs, any functions which include NOT(TBG.MISSED) must have twice as many terms as normal in order to perform an OR of the inverted TBG.MISSED inputs.

Also, if a JTAB and a ZAP occur at the same time, they cancel each other. In this case, UIV will be selected if a microinterrupt or indirect macrointerrupt is pending, and the OP address will be selected for all other cases (JMPV will not work). In addition, if a microinterrupt is in process (UIV is enabled this cycle), the OP address will always be selected in the following cycle unless a CS parity error occurs.

3.3.8 Address Jump Table

The Address Jump Table (AJT) consists of a PLA and two PROMs. The AJT latch consists of U1307 (SQ24C) and U1308 (SQ24B). Its inputs are connected to BP.S.BUS[14:0]+ and its outputs continually drive SQ.AJT.IN.BUS[14:0]+. The latch is normally closed, but the gate at U0301 (SQ21C) opens the latch during the second half (CPU clock low) of each microcycle that uses the IJT (SQ.IJT.EN- low). Opening the latch allows the data from the SBUS to reach the AJT.

The AJT PLA U1208 (SQ27C) looks at SQ.AJT.IN.BUS[15:0]+ and drives SQ.UADR[7:1]- and BP.NO.EXECUTE- when SQ.R2.AJT.16.EN- is "low". At the same time, a buffer U1604 (SQ27B) drives SQ.UADR[14:8]- and SQ.UADR0- to generate even addresses in the range from octal 01000 to 01376.

The two 512 by 8 PROMs are U1407 (SQ25C) and U1607 (SQ25B). They look at SQ.AJT.IN.BUS[8:0]+ and drive SQ.UADR[14:0]- and BP.NO.EXECUTE- whenever SQ.R2.AJT.09.EN- is "low". The following table indicates which bits are controlled by which PROM or PLA.

		AJT PROM / PLA		
Type		Loc.	Prog.	Drives
PLA	82S100	U1208	SPL01	SQ.UADR[7:1]- , BP.NO.EXECUTE-
PROM	7649A	U1407	SPR01	SQ.UADR[7:0]-
PROM	7649A	U1607	SPR02	SQ.UADR[14:8]-, BP.NO.EXECUTE-

The coding for the AJT PLA U1208 is listed in Figures 3-12.

```
*        SSSSSSSSSSSSSSSS
*        QQQQQQQQQQQQQQQQ
*        ................        B
*        AAAAAAAAAQAAAAAA        P
*        JJJJJJJJJJJJJJJJ        .
*        TTTTTTTTTTTTTTTT        N
*        ................        O
*        IIIIIIIIIIIIIIII        .
*        NNNNNNNNNNNNNNNN  SSSSSSSE
*        ................  QQQQQQQX
*        BBBBBBBBBBBBBBBB  .......E
*        UUUUUUUUUUUUUUUU  AAAAAAAC
*        SSSSSSSSSSSSSSSS  DDDDDDDU
*        1111110000000000  RRRRRRRT
*        5432109876543210  7654321E
*        ++++++++++++++++  --------
*        2222222200000000  11111111
*PIN:    0123456723456789  01235678
 SENSE:                    LLLLLLLH
*        IIIIIIIIIIIIIIII
*        1111110000000000  FFFFFFFF
*ROW     5432109876543210  76543210     COMMENT
*- - - - - - - - - - - - - - - - -  *  - - - - -
   0     LH--------------  ......AA  *  DIRECT
   1     L-H-------------  ......AA  *  DIRECT
   2     L--H------------  ......AA  *  DIRECT
   3     -LLHL-----------  .A.....A  *  AND
   4     -LHHL-----------  .A...A.A  *  IOR
   5     -LHLL-----------  .A..A..A  *  XOR
   6     -LLHH-----------  ..AAAA.A  *  JSB
   7     -LHHH-----------  .A.A.A.A  *  ISZ
   8     -HLL------------  .....A.A  *  AD*
   9     -HLH------------  .A.AAA.A  *  CP*
  10     -HHL------------  .A..AA.A  *  LD*
  11     -HHH------------  .A.AA.AA  *  ST*,D ST*,I
  12     -LHLH-----------  .AA..A.A  *  JMP,I
  13     LLLL-LLL--LLLL--  .A.AA..A  *  NOP
  14     LLLL-L------L---  .A.A...A  *  SRG NOSKIP
  15     LLLL-L------H---  .A.A..AA  *  SRG SKIP
  16     LLLL-H----LLL-LL  .AA.AA.A  *  ASG NO SKIP
  17     LLLL-H----------  .AA....A  *  ASG SKIP
  18     HLLLLLL-HLLLLLLL  .AAAA..A  *  | MPY JLA
  19     HLLLLLLH-LLLLLLL  .AAA.A.A  *  | DIV JLA
  20     HLLLHLL-HLLLLLLL  .AAAA.AA  *  | DLD JLB
  21     HLLLHLLH-LLLLLLL  .AAA.AAA  *  | DST JLB
  22     HLLLLLLLLLLH----  .AA..AAA  *  ASL
  23     HLLLLLLLLLLHLLLL  .AA.AAAA  *  ASLO
  24     HLLLLLHLLLLH----  ..AAA..A  *  ASR
```

Figure 3-12. Address Jump Table PLA (U1208) Coding (Sheet 1 of 2)

SQ 87c

```
*       SSSSSSSSSSSSSSS
*       QQQQQQQQQQQQQQQ
*       ...............         B
*       AAAAAAAAAQAAAAA         P
*       JJJJJJJJJJJJJJJ         .
*       TTTTTTTTTTTTTTT         N
*       ...............         O
*       IIIIIIIIIIIIIII         .
*       NNNNNNNNNNNNNNN   SSSSSSSE
*       ...............   QQQQQQQX
*       BBBBBBBBBBBBBBB   .......E
*       UUUUUUUUUUUUUUU   AAAAAAAC
*       SSSSSSSSSSSSSSS   DDDDDDDU
*       1111110000000000  RRRRRRRT
*       5432109876543210  7654321E
*       ++++++++++++++++  --------
*       2222222200000000  11111111
*PIN:   0123456723456789  01235678
 SENSE:                   LLLLLLLH
*       IIIIIIIIIIIIIII
*       1111110000000000  FFFFFFFF
*ROW    5432109876543210  76543210     COMMENT
*- - - - - - - - - - - - - - - -   *   - - - - -
  25    HLLLLLLLLLHL----  ....AA.A  *   LSL
  26    HLLLLLHLLLHL----  ....A..A  *   LSR
  27    HLLLLLLLLHLL----  ..AA.A.A  *   RRL
  28    HLLLLLHLLHLL----  ..AA...A  *   RRR
  29    HLLLLL-LL---LLLL  ......A.  *   SHIFT 0
  30    HLLL-H---HH-----  ..A...AA  *   IO BIT 7
  31    HLLL-H---H-H----  ..A...AA  *   IO BIT 7
  32    HLLL-H--H-H-----  ..A..A.A  *   IO BIT 8
  33    HLLL-H--H--H----  ..A..A.A  *   IO BIT 8
  34    HLLL-H-H--H-----  ..A.A..A  *   IO BIT 9
  35    HLLL-H-H---H----  ..A.A..A  *   IO BIT 9
  36    HLLL-H----LLL--H  ....A..A  *   IO BIT 0
  37    HLLL-H----LLL-H-  .....A.A  *   IO BIT 1
  38    HLLL-H----LLLH--  ......AA  *   IO BIT 2
  39    HLLL-H----LLH---  ..A....A  *   SELECT 10-17
  40    HLLL-H---LLLL---  AA.....A  *   IO BIT 7
  41    HLLL-H-HL-LLL---  A.A....A  *   MIA,LIA
  42    HLLL-H-LH-LLL---  A..A...A  *   SFC,SFS
  43    HLLL-HLLLHLLL---  AAAA...A  *   STF
  44    HLLL-HHLLHLLL---  A.AA...A  *   CLF
  45    HLLLHH-HHHLLL---  A......A  *   CLC
  46    HLLLLH-HHHLLL---  ...A...A  *   STC
  47    HLLL-H-LLL------  AAAAAAAA  *   HLT
```

Figure 3-12. Address Jump Table PLA (U1208) Coding (Sheet 2 of 2)

The actual decision about enabling the AJT is made in the microcycle before the enabling occurs. SQ.R1.AJT.EN- goes "low" to indicate that the AJT should be used in the following microcycle. The details of its generation are given under Next Address Selection, above. In general, it goes "low" if the following four conditions are met:

1. Power must be up.

2. The UIR at present contains a MEM/JTAB.

3. There are no unmasked interrupts pending.

4. There is no single step pending.

The AJT PROMs have two sides which are selected by generating SQ.RS.AJT.09.EN- to control their CE input as follows:

First, four gates, U1207 (SQ93C), U1207 (SQ93B), U0906 (SQ94B), and U0301 (SQ94B) look at BP.S.BUS[15:7]+ to generate SQ.AJT.PROM+. This signal goes "high" if the AJT PROM should be used in the next cycle, and goes "low" if the AJT PLA should be used.

Second, four gates, U0202 (SQ93A), U0301 (SQ93A), U0206 (SQ94A), and U0301 (SQ95A) look at BP.S.BUS[15:11]+ to generate SQ.S.JMP+. This signal goes "high" if the data on the SBUS looks like a JMP,D instruction.

The gated functions are:

```
SQ.AJT.PROM+ =    (BP.S.BUS15+) and
               not(BP.S.BUS14+) and
               not(BP.S.BUS13+) and
               not(BP.S.BUS12+) and
               not(BP.S.BUS10+) and
                  (BP.S.BUS9+ ) and
                ( (BP.S.BUS11+) or
                  (BP.S.BUS8+)  or
                  (BP.S.BUS7+)   )

SQ.S.JMP+    = not(BP.S.BUS15+) and
               not(BP.S.BUS14+) and
                  (BP.S.BUS13+) and
               not(BP.S.BUS12+) and
                  (BP.S.BUS11+)
```

Third, SQ.AJT.PROM+ and SQ.S.JMP+ select the 2:4 decoder U1004 (SQ96C) which produces SQ.R1.AJT.09.EN-, SQ.R1.AJT.16.EN-, and SQ.AJT.JM.EN-. SQ.R1.AJT.EN- enables the decoder:

a. All three of these outputs remain "high" while SQ.R1.AJT.EN- is "high".

b. When SQ.R1.AJT.EN- is "low", SQ.R1.AJT.09.EN- goes "low" when SQ.AJT.PROM+ is "high",

c. SQ.R1.AJT.16.EN- goes "low" when SQ.AJT.PROM+ and SQ.S.JMP+ are both "low".

d. SQ.R1.AJT.JM.EN- goes "low" if SQ.S.JMP+ is "high".

Fourth, two of the rank one decoder outputs are converted to SQ.R2.AJT.09.EN- and SQ.R2.AJT.16.EN- by the continually clocked register U1605 (SQ105C). These rank two versions are used to actually enable the appropriate half of the AJT.

A third rank one decoder output is converted to SQ.R2.AJT.JM.EN- by the continually clocking register U1504 (SQ85E). This rank two version is used to enable the upper half of the buffer which drives UADR from UPC. All this means that the PROM will be selected for SBUS values from 101200 to 101777 and from 105000 to 105777.

The UPC buffer will be selected for SBUS values from 024000 to 027777 (JMP,D). The PLA will be selected for all other values.

3.3.9 Microinterrupt Vector Register

The first rank of the UIV register consists of U1506 (SQ22E). This register is held clear when SQ.R2.PON+ is "low". It is loaded from BP.T.BUS[7:0]+, and always drives SQ.UIV.REG[7:0]+. The gate at U1406 (SQ21D) causes it to load at the end of a microcycle in which SQ.UIV.STOT- is "low".

The second rank of the UIV register consists of U1606 (SQ23E) and U1603 (SQ23D). These registers are clocked at the end of every microcycle. The lower register is loaded from SQ.UIV.REG[7:0]+ and drives SQ.UADR[7:0]- when SQ.R2.UIV.EN- is "low". The upper register drives SQ.UADR[14:8]- and BP.NO.EXECUTE- when SQ.R2.UIV.EN- is "low". The address bits are always loaded with all ones, and the remaining bit is loaded with zero.

SQ.R2.UIV.EN- is a version of SQ.R1.UIV.EN- which has been delayed one microcycle by the register U1605 (SQ105C). The generation of SQ.R1.UIV.EN- is described under Next Address Selection, above, but in general it goes "low" when one of the following four conditions is true.

1. A microinterrupt is pending.

2. A macrointerrupt or single step is pending during a JTAB line.

3. An indirect interrupt has been detected on the CA board.

4. Power is in the process of coming up.

3.3.10 Vector Register

The VECT register is composed of U1608 (SQ25E) and U0808 (SQ25D). It is loaded from BP.T.BUS[15:0]+ at the end of the microcycle when the gate at U1406 (SQ21E) determines that SQ.VECT.STOT- is "low". VECT drives SQ.UADR[14:0]- and BP.NO.EXECUTE- when SQ.R2.VECT.EN- is "low". This signal is a version of SQ.R1.VECT.EN- which has been delayed one microcycle by the register U1605 (SQ105C).

The generation of SQ.R1.VECT.EN- is described under Next Address Selection above, but in general it goes "low" if the following four conditions are all true:

1. There is an SP2/JMPV in the UIR.

2. There is not an MEM/JTAB or MEM/JTDI in the UIR.

3. There are no pending microinterrupts.

4. There is no pending indirect interrupt.

3.3.11 Microinterrupt Register

The UINT register consists of U1305 (SQ104E). This 8-bit register drives BP.S.BUS[7:0]+ when SQ.UINT.RREG- is "low". Its inputs are connected to microinterrupt related signals as listed in the following table:

UINT Bit	Signal	Comment
0	SQ.R2.NOCS.ERR+	NOCS previous cycle
1	SQ.CSPAR.ERR+	Control store parity
2	SQ.STK.UND.OVF+	Stack under/overflow
3	SQ.TBG.MISSED+	TBG timeout error
4	SQ.ZAP.ONES+	ZAP
5	SQ.STK.OVF+	Stack overflow
6	no connection	
7	SQ.8.46.OD+	Parity on NOCS driver

Normally, the register is clocked at the end of each microcycle. However, the clock can be controlled by PLA U1505 (SQ103B). The coding for the microinterrupt and ZAP counter PLA is listed in Figure 3-13.

```
*                                       S
*                                       Q
*       S   B B                         .   S
*       Q   P P B B B B S   U   Q S   S
*       .   . . P P P P Q   I   . Q   Q S
*       R   U U . . . . . S N   R . S . Q
*       2 B I I U U U U L Q T   1 R Q J .
*       . P R R I I I I E . P   . 1 . M L
*       Z . . . R R R R D R .   Z . Z P E
*       A U R R . . . . . 2 P   A U A V D
*       P I E E R R R R R . U   P I P . .
*       . N G G E E E E E P L   . N . S I
*       E T 4 4 G G G G G O S   E T L P N
*       N P 5 4 3 2 1 0 8 N E   N P D 2 8
*       + + + + + + + + + + +   + + - - +
*       0 0 0 0 0 0 0 0 1 1 0   1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 2 1 9   9 8 7 6 5
 SENSE:                         H H L L L
*                         B B B B B B B B B
*ROW    7 6 5 4 3 2 1 0 2 1 0   9 8 7 6 5
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  0     - - - - - - - - - L -   A . A . A   PON-
  1     - - H L H H H L - H -   . . . A .   JMPV
  2     - - H L H H L H - H -   . . A . .   ZPOF
  3     - - H L H H L L - H -   A . . . .   ZPON
  4     - - H L H L L H - H -   . . . . A   LDON
  5     H - L - - - - - - H -   A . . . .   ZAP.EN AND ZPOF-
  6     H - - H - - - - - H -   A . . . .   ZAP.EN AND ZPOF-
  7     H - - - L - - - - H -   A . . . .   ZAP.EN AND ZPOF-
  8     H - - - - L - - - H -   A . . . .   ZAP.EN AND ZPOF-
  9     H - - - - - H - - H -   A . . . .   ZAP.EN AND ZPOF-
 10     H - - - - - - L - H -   A . . . .   ZAP.EN AND ZPOF-
 11     - H L - - - - - - H -   . A . . .   UINTP AND CLUI-
 12     - H - H - - - - - H -   . A . . .   UINTP AND CLUI-
 13     - H - - L - - - - H -   . A . . .   UINTP AND CLUI-
 14     - H - - - H - - - H -   . A . . .   UINTP AND CLUI-
 15     - H - - - - L - - H -   . A . . .   UINTP AND CLUI-
 16     - H - - - - - L - H -   . A . . .   UINTP AND CLUI-
 17     - - L - - - - - L H -   . . . . A   LED8 AND LDOF-
 18     - - - H - - - - L H -   . . . . A   LED8 AND LDOF-
 19     - - - - L - - - L H -   . . . . A   LED8 AND LDOF-
 20     - - - - - H - - L H -   . . . . A   LED8 AND LDOF-
 21     - - - - - - L - L H -   . . . . A   LED8 AND LDOF-
 22     - - - - - - - H L H -   . . . . A   LED8 AND LDOF-
 23     - - L - - - - - - H H   . A . . .   UINTP PULSE AND JFSS-
 24     - - - H - - - - - H H   . A . . .   UINTP PULSE AND JFSS-
 25     - - - - L - - - - H H   . A . . .   UINTP PULSE AND JFSS-
 26     - - - - - H - - - H H   . A . . .   UINTP PULSE AND JFSS-
 27     - - - - - - H - - H H   . A . . .   UINTP PULSE AND JFSS-
 28     - - - - - - - H - H H   . A . . .   UINTP PULSE AND JFSS-
```

Figure 3-13. Microinterrupt and ZAP Counter PLA (U1505) Coding

When one or more of the microinterrupt signals go "high", the signal SQ.UINTP.PULSE+ also goes "high". When this happens, the PLA causes SQ.R1.UINTP+ to go "high". At the end of the microcycle, this signal is clocked into the register U1605 (SQ105C), causing BP.UINTP+ to go "high".

Signal BP.UINTP+ has several uses. First it is sent to the macrointerrupt logic on the MC board to indicate that a microinterrupt has occurred. Second, it is sent back to the PLA where it is used to force SQ.R1.UINTP+ "high", and thereby latch the fact that a microinterrupt has occurred, even though the signal which caused the interrupt may have since returned to its noninterrupting state. And third it causes the gate U1406 (SQ103E) to freeze the clock to the UINT register. This causes the register to take a snapshot of its inputs during the cycle when the microinterrupt occurred.

SQ.UINTP.PULSE+ is ignored by the PLA if it occurs at the same time as SP2/JFSS. This prevents the UINT register from freezing even though the rest of the microinterrupt process occurs (useful in self-test). The PLA resets SQ.R1.UNITP+ to the "low" state when an SP2/CLUI is found in the UIR. This in turn allows BP.UINTP+ to return "low" and thereby unfreeze the UINT register.

3.3.12 Self-Test and Miscellaneous

The SQST register consists of U1306 (SQ112E) and U0305 (SQ112D). The lower 15 bits of the register can be loaded from SQ.UADR[14:0]+. The ZAP counter can freeze the clocking of the register which normally occurs at the microcycle boundary. The register drives BP.S.BUS[15:0]+ when SQ.SQST.RREG- is "low".

The ZAP counter is U1107 (SQ107B) synchronous-up counter. It is clocked at the end of each microcycle and its enable and load signals are used to control its counting sequence.

The PLA U1505 (SQ103B) produces two signals related to the ZAP counter. The coding for this PLA is listed in Figure 3-13, above. SQ.R1.ZAP.EN+ goes "high" when a SP2/ZPON is present in the UIR. At the end of the microcycle, it is clocked into the register U1605 (SQ105C) to become SQ.R2.ZAP.EN+. This signal enables the counter to start counting. It is also fed back to the PLA to force SQ.R1.ZAP.EN+ "high". This latches the counter into the enabled state.

When an SP2/ZPOF occurs in the UIR, the PLA forces SQ.ZAP.LD- to go "low", causing the counter to be loaded with a value of octal 10 at the end of the microcycle. The PLA also forces SQ.R1.ZAP.EN+ "low", which in turn causes SQ.R2.ZAP.EN+ to go "low" during the following cycle. This disables the counter and resets the latching function that previously held SQ.R1.ZAP.EN+ high. Thus the counter holds the value of 10 (octal) until another SP2/ZPON occurs.

The counter's upper bit becomes SQ.ZAP.1XXX+ which is inverted by the gate at U1404 (SQ106D) to become SQ.ZAP.1XXX-. When SQ.ZAP.1XXX- is "high", the gate at U1406 (SQ107D) freezes the clock to the SQST register. This signal also has an effect on stack operation. The ripple-carry output of the counter (SQ.ZAP.ONES+) goes "high" when the counter is all "ones". This signal can cause a microinterrupt and can change the operation of the IJT and AJT if it occurs at the same time as a MEM/JTAB or MEM/JTDI.

The PLA U1505 also decodes five orders from the SP2 field. Four of them (CLUI, JFSS, ZPON, and ZPOF) are used only within the PLA as described above. The fifth (JMPV) is sent to an output to produce SQ.JMPV.SP2-. It should be noted that the SP2 field only exists when the OP field contains a SP1C or RTNC. Therefore it is necessary for the PLA to look at two OP field bits (BP.UIR.REG[45:44]+) as well as the SP2 field bits (BP.UIR.REG[3:0]+).

The 3:8 decoder U1104 (SQ116B) produces two enables used to select the register which drives the SBUS. These signals (called SQ.SQST.RREG- and SQ.UINT.RREG-) are generated based on five of the RREG field bits (BP.UIR.REG[30:26]+). Since the sixth RREG field bit (BP.UIR.REG31+) is not looked at, the enables occur for two different RREG field values. This is not a problem since the DP board will use the SBUS as an RREG source for only one of the two values. The decoder is disabled when BP.KIS.S.OFF- is "low". This signal is used by the CA board to force all registers off the SBUS during certain phases of cache operation. The signal is pulled "high" when the CA board is not plugged in.

The 3:8 decoder U1408 (SQ116B) produces four enables used to select the register which will be loaded from the TBUS. Three of the signals (SQ.UIV.STOT-, BP.LED.STOT-, SQ.VECT.STOT-) are used on the SQ board while the fourth (BP.ACCL.STOT-) is sent to the DP board. Since stores occur the cycle after they appear in the microinstruction, the second rank of the STOT field bits (BP.R2.UIR.REG[23:20]+) is used to control the decoder. The decoder is disabled when BP.STORE.EN- is "high". The DP board drives this signal "high" when it is necessary to disable stores.

The LED register consists of a U0706 (SQ112B). It is reset to zeroes when SQ.R2.PON+ is "low". It is loaded from BP.T.BUS[7:0]+ at the end of a microcycle in which SQ.LED.STOT- is low. Its outputs (SQ.LED.REG[7:0]+ drive the cathodes of eight LEDs whose anodes are all connected to +5V. This causes a LED to light when its corresponding register bit is set "low".

A pair of cross coupled open collector gates at U0203 (SQ113D) are used to debounce a RESET switch which can drive LBP.PON+ "low". When the switch is in its normal position, the PON signal can be driven by connecting to one of the switches' terminals.

3.3.13 Clock Generation

The four main processor clocks for A900 are all generated on the Sequencer card and are shown on schematic SQ12. The relationship of the clocks during normal operation and during freezes is shown in Figure 3-14.

The two gates at U0206 (SQ124A) normally pass the output of the main oscillator U0108 (SQ123A) to SQ.CLOCK.BASE+. When FP.EXT.CLK.EN- is pulled "low", an external clock (injected at FP.EXT.CLK-) is sent to SQ.CLOCK.BASE+ in place of the main oscillator. All of the clocks come out of one common register located at U0308 (SQ125B). This is to keep the relative clock skews to a minimum. This register is clocked by SQ.CLOCK.BASE+. There are four main clocks: MEM clock, CAC clock, CPU clock, and the backplane SCLK.

The MEM clock has several versions:

1. CK.MEM.MC+ goes directly to the chips located on the memory controller card (MC).

2. MEM.CLK (SQ.MEM.CLK+) from U0207 (SQ125C) is used to drive the delay line located at U0307 (SQ125A). There are three delayed versions of the MEM clock: CK.MEM.D20.BP+, CK.MEM.D30.BP+, and CK.MEM.D50.BP+. These are delayed 20, 30 and 50 ns, respectively, to use throughout the processor to shape write pulses for RAMs and to use in other places where non-standard edges are needed.

The CAC clock has two versions both of which go to the CA card:

1. CK.CAC1.CA+ 2. CK.CAC2.CA+

The CPU clock is generated in four versions. The first two are used only on the SQ card, and the other two go to the DP card:

1. CK.CPU1.SQ+ 2. CK.CPU2.SQ+,

3. CK.CPU3.DP+ 4. CK.CPU4.DP+

The fourth clock is CK.SCLK.SQ+ which is driven to the backplane by a pair of drivers, U0107 (SQ127C). The parallel connection is to improve rise and fall times on the heavily loaded (both capacitively and with resistor terminations) LBP.SCLK- line and to share the DC load heating effects.

3.3.13.1 Main Oscillator Clock

The main oscillator clock is divided into two by the one-stage ring counter consisting of a flip-flop in U0207 (SQ125D) and an inverter in U0107 (SQ127C). The clock produces the signal called SQ.LAST.30NS+ which is asserted for the last 33 ns of every 66 ns, (and for the last 33 ns of each 133 ns.) SQ.LAST.30NS+ is used as the select for the MUX located at U0208 (SQ123B).

For the SQ.LAST.30NS+ period (the last 33 ns of every 66 ns period), the clocks MEM, CAC and CPU, which are similar, get their next state from the "B" input of the MUX U0208. For the first 33 ns, the three clocks get their next state from the "A" input, which is driven with the present state of each clock, respectively. As a result, all three clocks do not change for two cycles.

For MEM clock, the first 33 ns is the high state. A copy of MEM clock is delayed another cycle using the same register that makes copies of all of the clock signals U0207 (SQ125D). The delayed MEM clock (SQ.DLY.MEM.CLK+) then forces the next state of all three clocks low by disabling the output of the 2:1 MUX located at U0208 (SQ123B). Thus, MEM clock always has a 50% duty cycle since it is forced high for the first 33 ns by SQ.PULLUP+. It remains high due to the feedback of itself, and then is low for two 33 ns periods due to the disabling of the next state MUX.

Note that the other two clock signals also have to be low for the last two 33 ns periods. Their first 33 ns is dependent upon BP.PE.FREEZE- for CAC clock, and both BP.PE.FREEZE- and BP.CPU.FREEZE- for CPU clock. Their second 33 ns is always the same as the first, due to the feedback path of the "B" inputs. Thus MEM, CAC, and CPU clocks are always aligned on their rising edges (microcycle boundary).

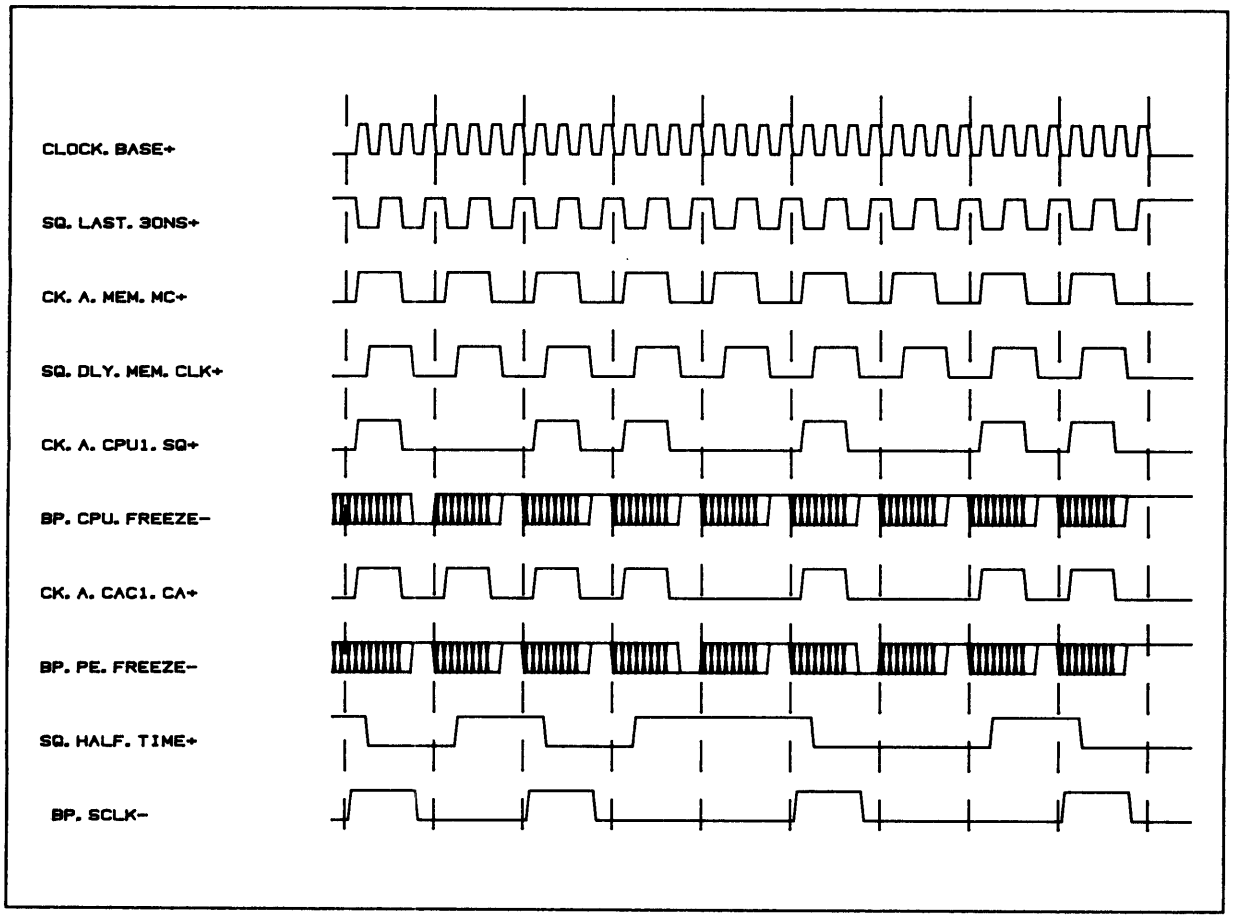


Figure 3-14. Clock Relationships

The clock conditions are:

a. MEM clock is always a 50% duty cycle,

b. CAC clock always rises with MEM clock unless BP.PE.FREEZE- is asserted (low) during the last 33 ns of a clock period,

c. CPU clock always rises with CAC and MEM clock unless either BP.PE.FREEZE- or BP.CPU.FREEZE- is asserted during the last 33ns of a clock period.

Note that if a clock freezes, it does so for an entire MEM clock period. Both BP.PE.FREEZE- and BP.CPU.FREEZE- are pulled up by resistors so that the SQ card can be operated without the CA and MC cards present.

SCLK is generated by the 8:1 MUX located at U0106 (SQ123D), with help from the AND-OR gate at U0103 (SQ124D). Figure 3-15 shows the state flow for SCLK.

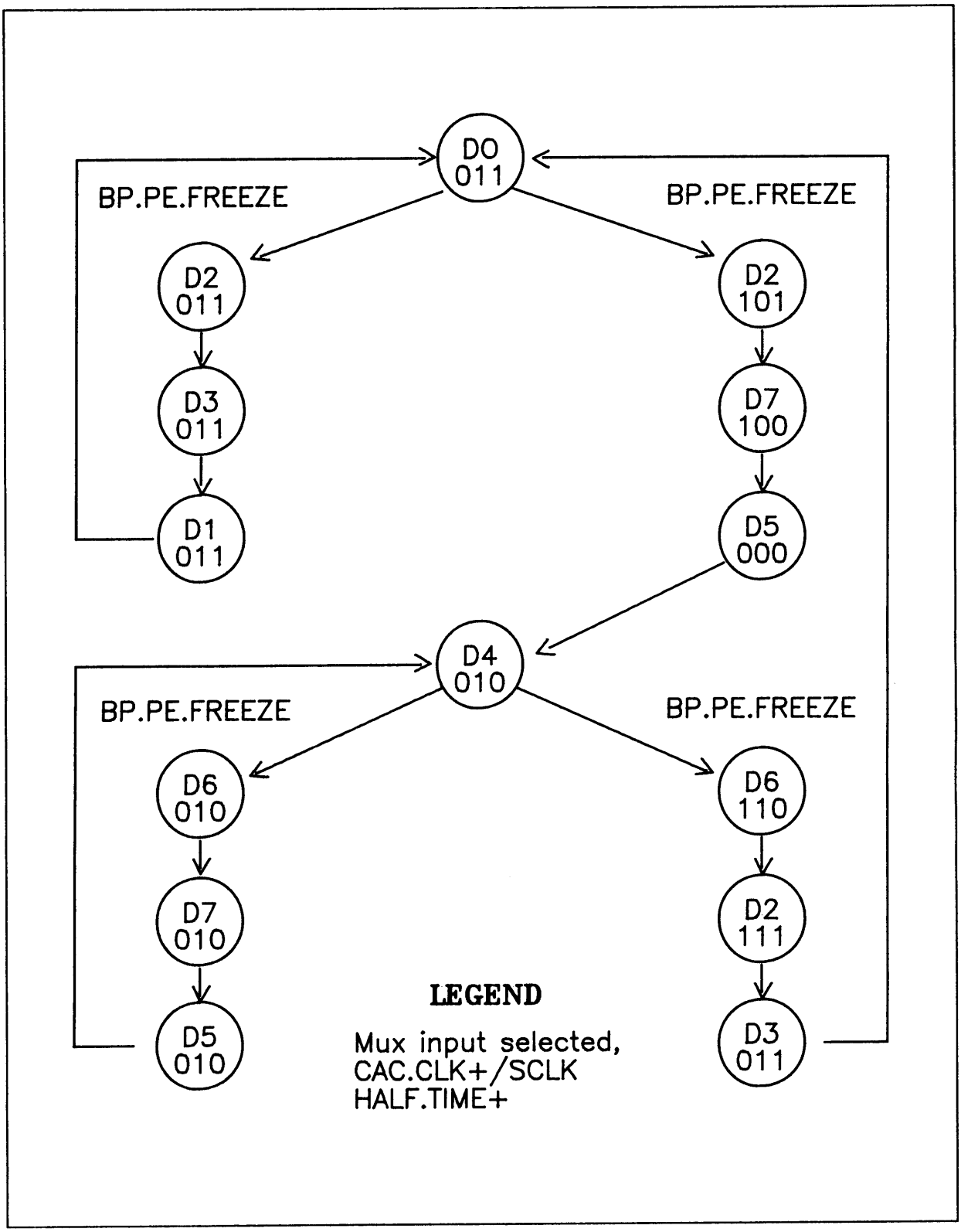


Figure 3-15. State Flow for SCLK

The signal SQ.HALF.TIME- is asserted 33 ns after CAC clock is active (coincident with SCLK). For this to happen, CAC clock assertions (rising edge of CK.CAC1.CA+) must have passed since the deassertion of SCLK (rising edge of LBP.SCLK-):

a. The first CAC clock assertion comes with the SCLK deassertion.

b. On the second CAC clock assertion, SCLK- is ready to rise with the next rising edge of CAC clock. At that time, SQ.MEM.CLK+ and SQ.DLY.MEM.CLK+ are both low and so input D0 of the 8:1 MUX is selected.

Thus the rising of SCLK- is dependent upon BP.PE.FREEZE- being high (as CAC clock):

a. Regardless of the SCLK state, the next input state is D2 following the present SCLK value.

b. If SCLK remains asserted, then the next input states are D3 followed by D1, both of which leave SCLK asserted.

c. The next input state is D0 which again checks whether BP.PE.FREEZE- is deasserted.

When BP.PE.FREEZE- is deasserted, SCLK becomes deasserted:

a. Input state D2 follows, regardless, and SCLK remains deasserted.

b. SQ.HALF.TIME+ deasserts also and so the next input state is D7, which follows SCLK.

c. Input state D5 follows which causes SCLK to be asserted.

d. In the next input state (D4) CAC clock might go high again. If it does not, then SCLK follows the path of D6, D7, D5 and back to D4 with SCLK remaining asserted and SQ.HALF.TIME+ remaining deasserted.

e. If CAC clock does go high, then SQ.HALF.TIME+ asserts one clock later and the path taken is D4, D6, D2, D3, and back to the starting point of D0, with SCLK always asserted.

The communication clock is generated by a 14.7456 oscillator on the memory controller card (refer to Chapter 6).

3.4 Parts Locations

The parts locations for the sequencer card are shown in Figure 3-16.

3.5 Replaceable Parts List

The replaceable parts list for the sequencer card are listed in Table 3-1. The names and addresses of the manufacturers of the parts are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

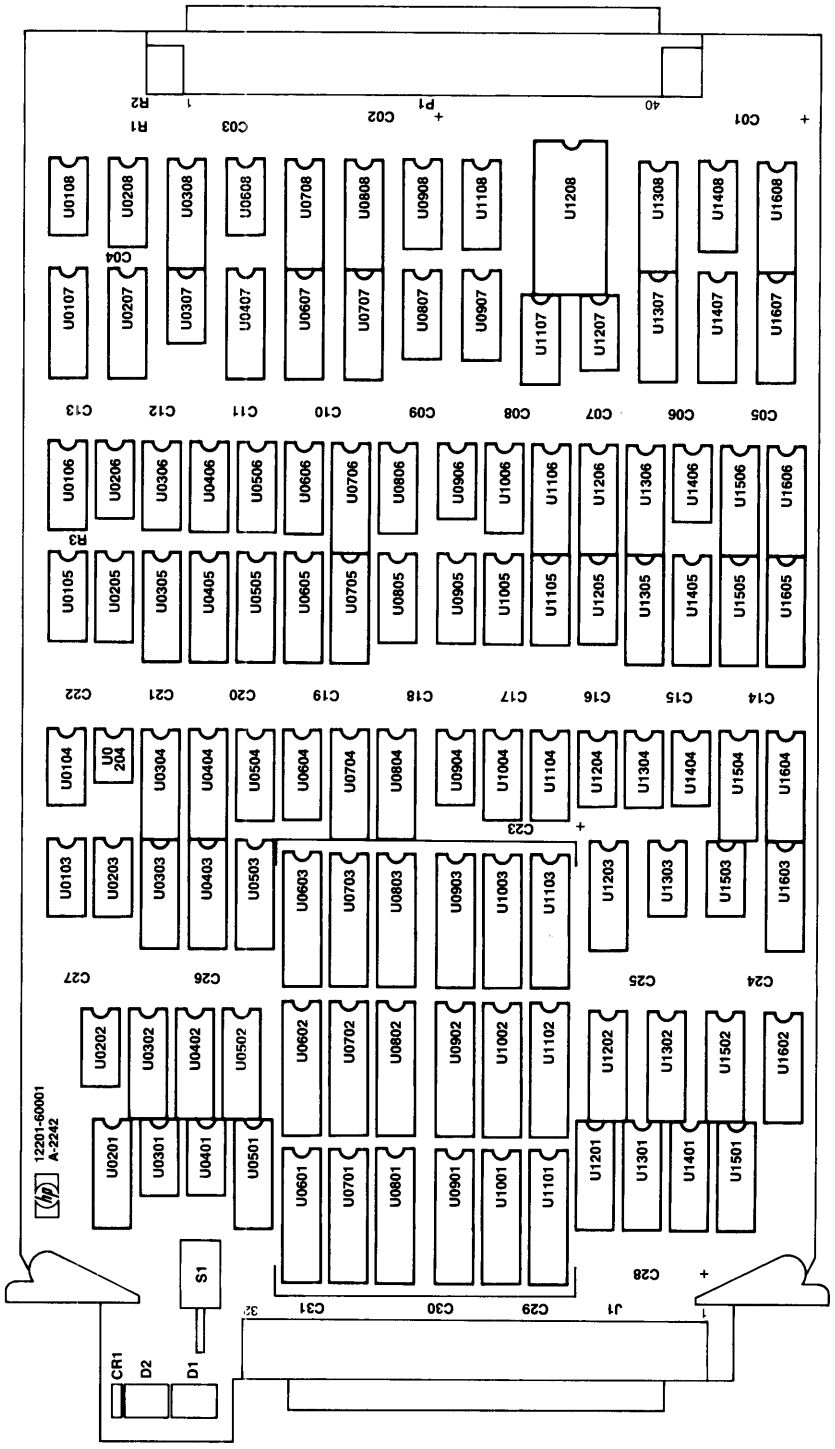


Figure 3-16. Sequencer Card Parts Locations

Table 3-1. Sequencer Card Replaceable Parts (Sheet 1 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12201-60001	1	1	PCA-SEQR/A900	28480	12201-60001
C1	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-4835	7	27	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C31	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1990-0685	7	1	LED-LAMP LUM-INT=200UCD	28480	HLMP-6620
DS1	1990-0652	8	2	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
DS2	1990-0652	8		LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
R1	0757-0280	3	2	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
S1	3101-1675	6	1	SWITCH-TGL SUBMIN DPST .5A 120VAC/DC PC	28480	3101-1675
U103	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U104	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U105	1820-1871	6	4	IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U106	1820-2936	6	1	IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U107	1820-2698	7	8	IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U108	1813-0237	1	1	XTAL-CLOCK-OSCILLATOR 30-MHZ 0.10% TTL	28480	1813-0237
U202	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U203	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U204	3101-2461	0	1	SWITCH-RKR DIP-RKR-ASSY 5-1A .1A 30VDC	28480	3101-2461
U205	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U206	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U207	1820-2701	3	22	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U208	1820-2654	5	5	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U301	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U302	1820-3026	7	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3026
U304	1820-3030	3	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3030
U305	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U306	1816-1495	1	4	IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U307	1813-0340	7	1	IC DLY-LN HYBRID MULTI-TAP	28480	1813-0340
U308	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U401	1820-1638	3	6	IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U402	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U403	1820-2795	5	3	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U404	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U405	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U406	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U407	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U501	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U502	1820-3027	8	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3027
U503	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U504	1810-0256	8	1	NETWORK-RES 16-DIP1.0K OHM X 15	01121	316A102
U505	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U506	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U604	1820-2769	3	1	IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC

Table 3-1. Sequencer Card Replaceable Parts (Sheet 2 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U606	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U607	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U608	1820-0606	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U704	1820-3025	6	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3025
U705	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U706	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U707	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U708	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U804	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U805	1820-2763	7	4	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F258PC
U806	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U807	1820-2763	7		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F258PC
U808	1820-2526	0	2	IC RGTR TTL S D-TYPE OCTL	34335	AM74S534PC
U904	1820-1638	3		IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U905	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U906	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U907	1820-2763	7		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F258PC
U908	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U1004	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U1005	1820-2763	7		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F258PC
U1006	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1104	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1105	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U1106	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1107	1820-1453	0	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U1108	1820-2654	5		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U1201	1820-3028	9	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3028
U1202	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1203	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1204	1820-1638	3		IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U1205	1820-1015	0	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U1206	12201-80023	9	1	IC-STACK CNTRL	28480	12201-80023
U1207	1820-1275	4	1	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U1208	12201-80002	4	1	IC AJT	28480	12201-80002
U1301	1820-3029	0	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3029
U1302	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1303	1820-1638	3		IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U1304	1820-1638	3		IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U1305	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1306	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1307	1820-2700	2	2	IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1308	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1401	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1404	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U1405	1820-3031	4	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3031
U1406	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1408	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1501	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U1502	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1503	1820-1638	3		IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U1504	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1505	1820-3032	5	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3032
U1506	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U1602	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1603	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1604	1820-2698	7		IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U1605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1606	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1608	1820-2526	0		IC RGTR TTL S D-TYPE OCTL	34335	AM74S534PC

2 2 2 2 dock 1200 - 0500

REVISIONS			
SYM	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	MAF/KO	10/27/82
B	REPLACE HAND-DRAWN VELLUM BY MA- CHINE GENERATED VERSION ON APERTURE CARD. NO CHANGE IN CONTENT.	JW/	1/17/84

D-12201-60001-51

SQ.RTN.REG+ 15
BP.UIR.REG+ 19

-2654 74F157 U1108 (-2654 74F157 U0908, U0905, U1105)

-2763 74F258 U0907 (-2763 74F258 U0807, U0805, U1005)

SQ.TARGT.RTN+

SQ.UPC.REG+ 15
U0504 1x1K +5
BP.CNDX.MET+ (37)
SQ.LO.COND- (298)
SQ.HI.COND- (279)
SQ.UADR- 15

-2698 74F240 U0707, U0705

-0683 74504 U1404
-1015 74S158 U1205
SQ.PULLUP+ (17)
SQ.UIR.REG46- (313)
SQ.UIR.REG 44- 2 (440)
SQ.LO.UNCOND- (299)
SQ.HI.UNCOND- (361)
-1367 74S08 U0202
SQ.HI.UN.OR.JM- (362)
BP.NO.EXECUTE- (36)
SQ.R2.OP.ADR.EN- (392)
SQ.R2.AIT.JM.EN- (390)

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5
INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ1

	SEQUENCER - A900 OP ADDRESS SELECT	
	12201A	12201-60001-51
		D-12201-60001-51

SQ1

REVISIONS			
ZONE	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	MAF/KO	10/27/82
B	CORRECTED NOS. ON 74F373/74F374	MAF/KO	2/23/83
C	PCO 22-6962; U1407 WAS 12201-80021; U1607 WAS 12201-80022	GD/KYO	6/29/83

12201-60001-52

SQ.AJT.IN.BUS+

PROM 12201-80043 7849A-5 U1607

PROM 12201-80042 7849A-5 U1407

PROM 12201-80002 82S100 U1208

-2700 74F373 U1308

-2700 74F373 U1307

-2698 74F240 U1604

-1322 74S04 U0301

-2701 74F374 U1603

-2526 74S534 U0808

-1449 74S32 U1406

-1730 74LS273 U1506

-2701 74F374 U1606

-2526 74S534 U1608

SPR02 #19

SPR01 #18

SPL01

UIV

VECT

+5V

109C SQ.IJT.EN- (23) 6
70D 90C CK.A.CPU1.SQ+ (21) 5
129B 30D 40B 80D

(243) CK.CPU1.AJT.SQ-

109C SQ.R2.AJT.09.EN- (301)
109C SQ.R2.AJT.16.EN- (204)

109E 119D 139B 70R 90C BP.S.BUS+ /16

129C 10E 30B 70B 110C SQ.PULLUP+ (17)

119B SQ.UIV.STOT- (450)
129B CK.A.CPU2.SQ+ (18) 6 (333)
40E 80B 100E
119B SQ.VECT.STOT- (451)

SQ.UIV.REG+

110B 136B BP.T.BUS+ /16

CK.CPU2.UIV.SQ+

CK.CPU2.VECT.SQ+ (245)

49A 100C SQ.R2.PON+ (112)
110C SQ.R2.UIV.EN- (158)
109C SQ.R2.VECT.EN- (303)

(36) BP.NO.EXECUTE- 19D 30E 134E

15/ SQ.UADR- 19D 30E 90C

NOTE:
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ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ2

	SEQUENCER-A900 AJT,UIV,VECT	HEWLETT PACKARD
	12201A NEXT ASSEMBLY	12201-60001-52 PART NUMBER
	SHEET OF	D-12201-60001-52

SQ2

D-12201-60001-53

A	AS ISSUED	MAF/KO	10/27/82
B	Correct pgs. on 74F374	MAF/KO	2/23/83

INC

-1871 745283 U0806 — SQ.INC.CARRY 1+ (363)
-1871 745283 U1006 — SQ.INC.CARRY 2+ (364)
-1871 745283 U0205 — SQ.INC.CARRY 3+ (365)
-1871 745283 U0105

129E 10E 20D 70B 110C — SQ.PULLUP+ (17)

15 SQ.UADR+ → 50A 60A 90E 110D

15 SQ.INCD.UADR+ → 40A

119C 135D — LBP.PON+ (101)

UPC

15 SQ.UPC.REG+ → 10D

(385) SQ.RI.PON+ → 40A

-2701 74F374 U0607
-2701 74F374 U0505

129B 20C 40B 80D — CK.A.CPU1.SQ+ (21)

(253) FP.NO.EXECUTE+ → 142C

15 FP.UADR+ → 141B

(187) FP.CK.CPU.SQ- → 142C

SQ.UADR+

-2698 74F240 U1501
-2698 74F240 U0404
-2698 74F240 U0501
-2698 74F240 U0402

19D 29D 90C — SQ.UADR- 15

19D 29D 134E — BP.NO.EXECUTE- (36)

143D — FP.BD.ON- (111)

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ3

	SEQUENCER-A900 INCREMENTER &UPC	HEWLETT PACKARD
	12201A	12201-60001
	SHEET OF	D-12201-60001-53

SQ3

	D-12201-80001-54		
A	As Issued	MAF/KO	12/27/82
B	Corrected nos. on 74F374 & Chgd Fab		
	PNs to Purch PNs per PRCR "A"	MAF/KO	2/23/83

RTN

STACK INPUT

39C SQ.RI.PON+ (385)

39B SQ.INCD.UADR+ 15

-2701 74F374 U0404 (U0407) — D8 D7 D6 D5 D4 D3 D2 D1 / Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 — CLK OE

-2701 74F374 U0405 — D8 D7 D6 D5 D4 D3 D2 D1 / Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 — CLK OE

-2701 74F374 U0706 — D8 D7 D6 D5 D4 D3 D2 D1 / Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 — CLK OE

-2701 74F374 U0605 — D8 D7 D6 D5 D4 D3 D2 D1 / Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 — CLK OE

(112) SQ.R2.PON+ → 20E 100C 110C

15 SQ.RTN.REG+ → 10A

129B 20C 30D CK.A.CPU1.SQ+ (21)

SQ.STK.DATA+

1816-1495 27S07 U0506 — A3 A2 A1 A0 / I4 I3 I2 I1 / O4 O3 O2 O1 — CS WE

1816-1495 27S07 U0606 — A3 A2 A1 A0 / I4 I3 I2 I1 / O4 O3 O2 O1 — CS WE

1816-1495 27S07 U0406 — A3 A2 A1 A0 / I4 I3 I2 I1 / O4 O3 O2 O1 — CS WE

1816-1495 27S07 U0306 — A3 A2 A1 A0 / I4 I3 I2 I1 / O4 O3 O2 O1 — CS WE

SQ.STK.ADDR+

(SQ.STK.WE-)
(SQ.STK.CS-)

129A 134D CK.A.MEM.D20.BP+ (307)

129A 134D CK.A.MEM.D50.BP+ (455)

CK.MEM.D50.STK- (153)
CK.A.MEM.D20.BP+ (307)

-0685 74S10 U0906

HRIS; HAII - 7649A-S

STACK CONTROL

12201-80023 7949R-5 U1206 — A8 A7 A6 A5 A4 A3 A2 A1 A0 / O8 O7 O6 O5 O4 O3 O2 O1 — CE

109C SQ.ITAB.MEM+ (202)
10D 135D BP.CNDX.MET+ (37)
109B SQ.ZAP.1XXX+ (330)
89A 10A 100B 110A 131B BP.UIR.REG+ 2

SPR03

14 (310) SQ.STK.UND.OVF+
13 (408) SQ.STK.OVF+
12 (308) SQ.STK.PUSH+
11 (308) SQ.STK.PUSH-

(310) SQ.STK.UND.OVF+ → 100E
(408) SQ.STK.OVF+ → 100D

-2701 74F374 U1106 — D8 D7 D6 D5 D4 D3 D2 D1 / Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 — CLK OE

SQ.STK .ADDR+

SQ.STK .PNTR+

129B 20D 80B 100E CK.A.CPU2.SQ+ (18)

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ4

	SEQUENCER - A900 STACK	HEWLETT PACKARD
	12201A	12201-60001
		D-12201-80001-54

SQ4

D-12201-60001-55

ITR	REVISIONS	APPROVED	DATE
A	AS ISSUED	MAF/KO	10/27/82
B	PCO 22-6962: U801,U802,U803 were 12201-80005/-80004/-80003; U701, U702,U703 were 12201-80011/-80010/ -80009; U601,U602,U603 were 12201-80017/-80016/-80015.	GD/KYO	6/29/83
C	PCO 22-6912:U801,U802,U803 were 12201-80026/-80044/-80024.	GD/KYO	9/8/83
D	PCO 22-7056: U801,U802,U803 were 12201-80047/-80046/-80045.	GD/DM	10-3-83
E	PCO 22-7103, U803 was 12201-80052.	GD/DM	12-8-83
F	PCO 22-7197 U0701,U0702,U0703 WERE 12201-80032/-80031/-80030.	GD/DM	2-24-84
G	REPLACE HAND-DRAWN VELLUM BY MACHINE GENERATED VERSION ON APERTURE CARD. NO CHANGE IN CONTENT.	JW/NL	4-17-84
H	PCO 22-7584: U801,U802,0803 were 12201-80054/-80053/-80060; U601, U608,U603 were 12201-80038/-80037/ -80036.	JW/	11-26-84

398 50A 90E 110D — SQ-UADR* 11

27S291 U0801 — SPRCS #2
27S291 U0701 — SPRCS #8
27S291 U0601 — SPRCS #14
27S291 U0802 — SPRCS #1
27S291 U0702 — SPRCS #7
27S291 U0608 — SPRCS #13
27S291 U0803 — SPRCS #0
27S291 U0703 — SPRCS #6
27S291 U0603 — SPRCS #12

24 FP.CS.OUT* — 68E 75D 80A 147B

99E 50E SQ.PROM.A12+ (16)
99E 50E SQ.PROM.A11 (15)
99C 50E SQ.BANK.EN0- (102)
99C 50E SQ.BANK.EN1- (103)
99C 50E SQ.BANK.EN2- (104)

NOTE:
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ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ5

TITLE: SEQUENCER - A900 LOW CONTROL STORE	HEWLETT PACKARD
SIZE: 12201A	PART NUMBER: 12201-60001
SHEET OF	D-12201-60001-55

Update 1

ITR	REVISIONS	APPROVED	DATE
A	AS ISSUED	MAF/KO	10/27/82
B	PCO 22-6962 U1101,U1102,U1103 WERE 12201-80008/-80007/-80006:U1001, U1002,U1003 WERE 12201-80014/-80013/ -80012;U0901,U0902,U0903 WERE 12201-80020/-80019/-80018.	GD/KYO	6-29-83
C	PCO 22-6912:U1101,U1102,U1103 WERE 12201-80029/-80028/-80027	GD/KYO	9/8/83
D	PCO 22-7058:U1101,U1102;U1103 WERE 12201-80050/-80049/-80048	GD/DM	10-3-83
E	PCO 22-7103;U1101,U1102 WERE 12201-80057/-80056	GD/DM	12-8-83
F	PCO 22-7197;U1001,U1002,U1003 WERE 12201-80035/-80034/-80033	GD/DM	2-24-84
G	REPLACE HAND-DRAWN VELLUM BY MACHINE GENERATED VERSION ON APERTURE CARD. NO CHANGE IN CONTENT.	JW/ NL	4-17-84
H	PCO 22-7584: U1101,U1102,U1103 were 12201-80062/-80061/-80055; U901, U902,U903 were 12201-80041/-80040/ -80039.	JW/	11-26-84

D-12201-60001-56

398 SOA 90E 110D — SQ.UADR+ 11

U1101 — SPRCS #5 — SQ.PROM.A12+ (16), SQ.PROM.A11 (15)

U1001 — SPRCS #11 — SQ.PROM.A12+ (16), SQ.PROM.A11 (15)

U0901 — SPRCS #17 — SQ.PROM.A12+ (16), SQ.PROM.A11 (15)

U1102 — SPRCS #4 — SQ.BANK.EN0- (102), SQ.BANK.EN1- (103), SQ.BANK.EN2- (104)

U1002 — SPRCS #10 — SQ.BANK.EN0- (102), SQ.BANK.EN1- (103), SQ.BANK.EN2- (104)

U0902 — SPRCS #16 — SQ.BANK.EN0- (102), SQ.BANK.EN1- (103), SQ.BANK.EN2- (104)

U1103 — SPRCS #3 — SQ.BANK.EN0- (102), SQ.BANK.EN1- (103), SQ.BANK.EN2- (104)

U1003 — SPRCS #9 — SQ.BANK.EN0- (102), SQ.BANK.EN1- (103), SQ.BANK.EN2- (104)

U0903 — SPRCS #15 — SQ.BANK.EN0- (102), SQ.BANK.EN1- (103), SQ.BANK.EN2- (104)

99E 50E — SQ.PROM.A12+ (16)
99E 50E — SQ.PROM.A11 (15)
99C 50E — SQ.BANK.EN0- (102)
99C 50E — SQ.BANK.EN1- (103)
99C 50E — SQ.BANK.EN2- (104)

24 FP.CS.OUT+ → 59E 79D 80A 147B

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ6

SEQUENCER - A900 HIGH CONTROL STORE	HEWLETT PACKARD
	12201-60001
	D-12201-60001-56

Update 1

SQ 6

	D-12201-60001-57		
A	As Issued	eaf/ko	10/27/82
B	Chgd Fab PN to Purch PN per PRCR "A"	eaf/ko	2/23/83

IJT

109E
119D 139B
20C 90C

BP.S.BUS+ /9

-3027
825153
U0502
SPL04
3-27

-2795
74F244
U1401

OP/SPIC, RTNC
TF/TRUE
CNDX/TRUE
SQ.GND.TMP+

NO CS FORCE

129C
10E 20D
30B 110C

SQ.PULLUP+ (17)

-2795
74F244
U1602

OP/JSBC
STOU/NOP
STOT/NOP
MEM/NOP
SPO/NOP

-2795
74F244
U0403

SQ.GND.TMP.+

-3026
825153
U0302
SPL03
3-26

-3025
825153
U0704
SPL02
3-25

-3029
825153
U1301
SPL06
3-29

-3028
825153
U1201
SPL05
3-28

99D SQ.R1.NOCS.ERR= (157)

109C
20C 90C

SQ.IJT.EN- (23)

SQ.IJT.EN- (23)

48/ FP.CS.OUT+

59E 69E
80A 147B

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ7

	SEQUENCER - A900 IJT NO CS DRIVER	HEWLETT PACKARD
		12201-60001
		D-12201-60001-57

SQ7

REVISIONS			
ZONE	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	mcf/ko	10/27/82
B	CORRECTED NOS. ON 74F374	mcf/ko	2/23/83

D-12201-60001-58

UIR (R1)

59E 69E
79D 147B
FP.CS.OUT+ /48

48/ BP.UIR.REG+ → 10A 40E 100B 110A 130B

(338) (344) (339) (345) → -1158 74S51 U0103 → (270) SQ.8.46.OD+ → 100D

1298 20D
40E 100E
CK.A.CPU2.SQ+ (18)

-2701 74F374 U1502 — D8..D1 → Q8..Q1 — CLK, OE — 11, 1
-2701 74F374 U1302 — D8..D1 → Q8..Q1 — CLK, OE — 11, 1
-1638 74S280 U1503 — A..I → EV, OD, NC — 3
-1638 74S280 U1304 — A..I → EV, OD, NC — 3

(47) (46) (45) (44) (74) (73) (72) (71) → (240) (239) (238) (237) (175) (174) (173) (172)
(97) (52) (51) (50) (95) (94) (93) (92) → (331) (30) (27) (67) (149) (148) (147) (146)
(38) (27) (67) (177) (176) (240) (239) (238) (257) → (338) SQ.20.46.EV+ / (339) SQ.20.46.OD+
(331) (175) (174) (173) (172) → (276) SQ.CSPAR.ERR+ → 100E

SQ.27.35.OD+ (340)
SQ.36.47.OD+ (343)

-2701 74F374 U0503
-2701 74F374 U1202
-1638 74S280 U0401
-1638 74S280 U1303

(70) (43) (42) (41) (40) (39) (54) (53) → (171) (136) (135) (170) (169) (168) (185) (184)
(90) (89) (88) (87) (86) (85) (84) (83) → (144) (143) (142) (183) (182) (181) (180) (179)
(136) (135) (170) (169) (168) (185) (184) → (344) SQ.8.14.EV+ / (345) SQ.8.14.OD+
(149) (148) (147) (146) (144) (143) (142) (183) (182)

-2701 74F374 U0804
-2701 74F374 U1203
-1638 74S280 U0904
-1638 74S280 U1204

(100) (99) (98) (91) (80) (75) (69) (68) → (152) (151) (150) (145) (109) (108) (134) (107)
(82) (81) (79) (78) (77) (76) (49) (48) → (178) (141) (140) (139) (138) (137) (177) (176)
(171) (152) (151) (150) (145) (109) (108) (134) (107) → (337) SQ.0.15.OD+
(181) (180) (179) (178) (141) (140) (139) (138) (137)

1298 20C
30D 40B
CK.A.CPU1.SQ+ (21)

UIR (R2)

-2701 74F374 U1504

4/ BP.R2.UIR.REG+ → 110C 134B

998 SQ.R1.AJT.JM.EN- (381) → (390) SQ.R2.AJT.JM.EN- → 10E
109A SQ.LED.IN8+ (368) → (297) SQ.LED.REG8+ → 100B 110B
99D SQ.R1.NOCS.ERR+ (382) → (302) SQ.R2.NOCS.ERR+ → 100E

(240) (239) (238) (237) → (167) (166) (165) (164)

NOTE:
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ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ8

	SEQUENCER - A900 UIR & PARITY	HEWLETT PACKARD
	NEXT ASSEMBLY	12201-60001
	SHEET OF	D-12201-60001-58

D-12201-60001-58			
REV	REVISION	APPROVED	DATE
A	AS ISSUED	maf/ko	10/27/82
B	CHGD FAB P/N TO PURCH P/N per PRCR "A"	maf/ko	2/23/83

-1322 74S02 U0301 — 13 SQ.S.JMP.A+

-0681 74S00 U0206 — 3 SQ.S.JMP.C- (420)

-1322 74S02 U0301 — 1 SQ.S.JMP+ (417)

-1367 74S08 U0202 — 3 SQ.S.JMP.B+

(418) (419) (28) (29) (30)

-0685 74S10 U0906 — SQ.S.10X.LOS+ (415); (31) (34); 8 SQ.S.10X- (414)

-1275 74S260 U1207 — (25) (28) (30) (35); 5

-1322 74S02 U0301 — 10 (354) SQ.AJT.PROM+

-1275 74S260 U1207 — (29) (33) (26); SQ.S.NO.RIGHT- (421)

SQ.AJT.PROM+ TRUE FOR:

S15					S0
1	000	101	XXX	XXX	XXX
1	000	X01	1XX	XXX	XXX
1	000	X01	X1X	XXX	XXX

-1072 74S139 U1004

(381) SQ.R1.AJT.JM.EN- → 80E
(378) SQ.R1.AJT.09.EN- → 100B
(379) SQ.R1.AJT.16.EN- → 100B
(102) SQ.BANK.EN0- → 50E 60E
(103) SQ.BANK.EN1- → 50E 60E
(104) SQ.BANK.EN2- → 50E 60E

109C SQ.R1.AJT.EN- (380)

109E 119D 139B 20C 70A — BP.S.BUS+ 9

19D 29D 30E — SQ.UADR- 4

+5 R16 1810-0256 2x10K U0504

109C 20C 70D 143D 143D — SQ.IJT.EN- (23); BP.S.BUS+ (190); SQ.UADR- (189)

-0685 74S10 U0906

-2769 74F153 U0604 — (22) (19) (20) (24); 1Y 7 (355) SQ.BANK.SEL0-; 2Y 9 (356) SQ.BANK.SEL1-

+5 R16 1810-0256 5x10K U0504

SQ.PROM.EN- (300)

3101-2461 U0204 — 2K/4K, 2K, BNK2, BNK1, BNK0

SQ.2K.0.4K.PROM- (154)
SQ.2K.PROM- (155)
SQ.BANK.IN2- (273)
SQ.BANK.IN1- (272)
SQ.BANK.IN0- (271)

-3030 82S153 U0304 — SPL07

(341) SQ.2K.0.4K.PROM+

-1158 74S51 U0104 — SQ.2K.PROM+ (342) (221)

(382) SQ.R1.NOCS.ERR+ → 80E
(157) SQ.R1.NOCS.ERR- → 70D
(16) SQ.PROM.A12+ → 50E 60E
(15) SQ.PROM.A11+ → 50E 60E

39B 50A 60A 110D — SQ.UADR+ 2

■ POWERED BY VCCM.

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ALL IC'S ARE 1820-XXXX.
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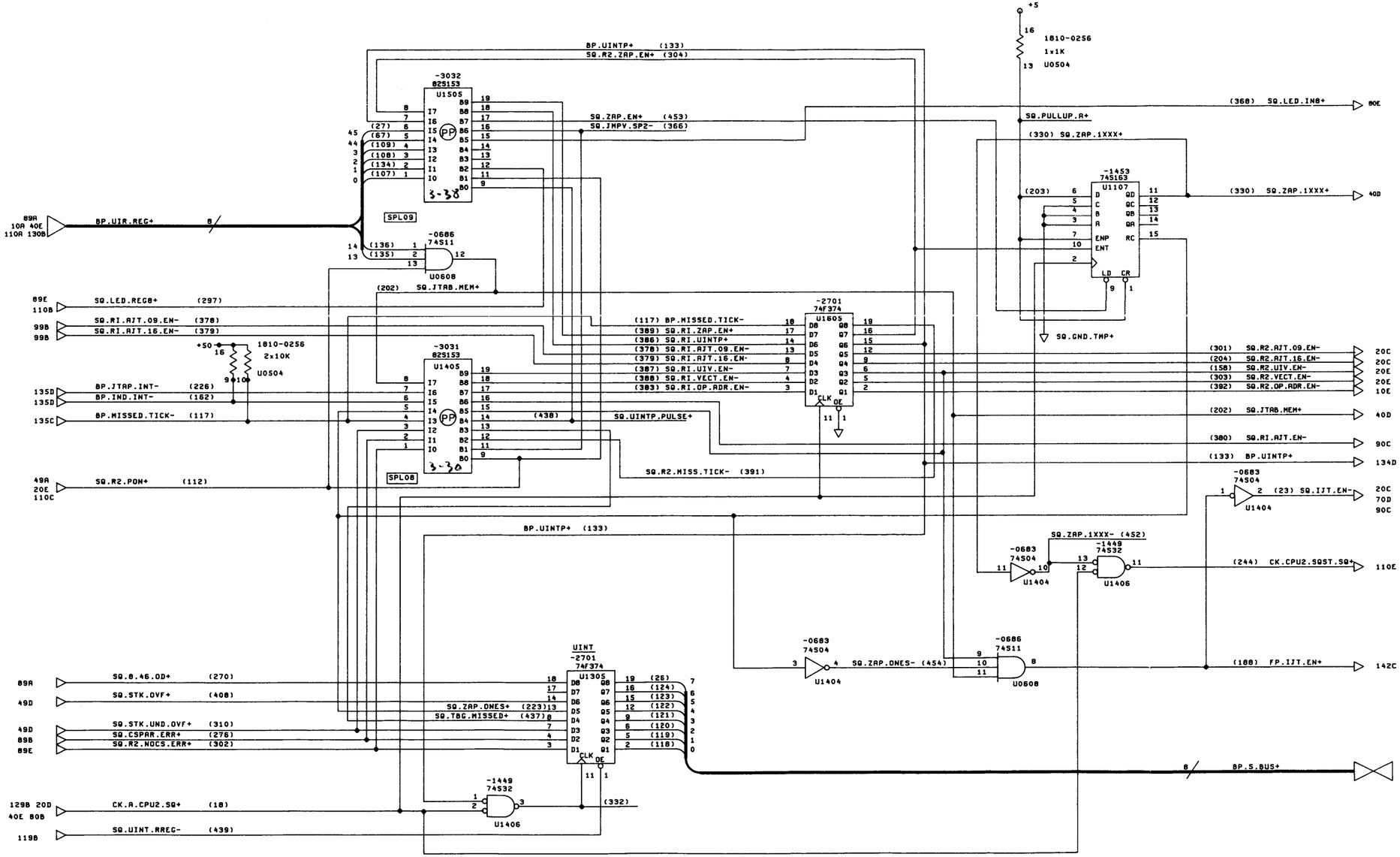
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ9

	SEQUENCER A900 CS & AJT CONTROL	HEWLETT PACKARD
		12201-60001
		D-12201-60001-59

SQ 9

	D-12201-60001-60		
REV	REVISIONS	REVISED	APPR
A	As Issued	ef/ko	10/23/82
B	Chgd. Fab.P/N to Purch.P/N per PRCR 'A'	ef/ko	2/23/83



SEQUENCER - A900
UINT, ZAP, & CONTROL

12201-60001

D-12201-60001-60

SQ10

	D-12201-60001-61		
A	As Issued	mef/ko	10/27/82
B	Corrected Nos. on 74F374 : chgd. G2A to G2B & G2B to G2A on 74S138	mef/ko	2/23/83

89A 10A
40E 110A
130B

BP.UIR.REG+ /5

+5
16 '1810-0256
1x1K
U0504
15

135C

BP.KIS.S.OFF- (163)

RREG

-1240
74S138
U1104

(137) 1 A
(138) 2 B
(139) 3 C
6 G1
(140) 5 G2B
(141) 4 G2A

Y7 7
Y6 9
Y5 10
Y4 11
Y3 12
Y2 13
Y1 14
Y0 15

(439) SQ.UINT.RREG- 100E

SQ.SQST.RREG- (306)

89E 100B

SQ.LED.REG8+ (297)

136B
20E

BP.T.BUS+ /8

LED

(LED9)

+5

SQ.LED.REG+

9 1 LED 10

1990-0685
CR1

-1730
74LS273
U0706

(132) 18 D8
(131) 17 D7
(130) 14 D6
(129) 13 D5
(127) 8 D4
(126) 7 D3
(106) 4 D2
(125) 3 D1

CR 11

Q8 19 (376)
Q7 16 (375)
Q6 15 (374)
Q5 12 (373)
Q4 9 (372)
Q3 6 (371)
Q2 5 (370)
Q1 2 (369)

(376) 8
(375) 7
(374) 6
(373) 5

4 LEDS 11 12 13 14

1990-0652
D2

(372) 4
(371) 3
(370) 2
(369) 1

4 LEDS 15 16 17 18

1990-0652
D1

-1240
74S138
U1408

(164) 20 A
(165) 21 B
(166) 22 C
(167) 23 G2B
6 G1
5 G2A
4

Y7 7
Y6 9
Y5 10
Y4 11
Y3 12
Y2 13
Y1 14
Y0 15

(238) BP.RCCL.STOT- 134E
(451) SQ.VECT.STOT- 20E
(227) BP.LED.STOT- 134E
(462) SQ.UIV.STOT- 20D

STOT

136D

CK.CPU4.LED.BP+ (248)

49A
20E 100C

SQ.R2.PON+ (112)

89E
134B
129C 10E 20D 30B 70B
135C

BP.R2.UIR.REG+ /4

SQ.PULLUP+ (17)

BP.R2.STORE.EN- (228)

RESET SWITCH

+5
1 R3
215 ohms
2

(159) SQ.SWCH.PON-

-1451
74S38
U0203

1 2 3

4 3
NORMALLY
1 2
S1
U0101
3101-1675

-1451
74S38
U0203

4 5 6

+5
16 1810-0256
U0504
14 1x10K

(101) LBP.PON+ 30B 135D

39B
50A
60A
90E

SQ.UADR+ 15/

SQST

-2701
74F374
U0305

(222) 18 D8
(221) 17 D7
(312) 13 D6
(311) 8 D5
(4) 7 D4
(12) 4 D3
(11) 4 D2
(11) 3 D1

CLK 11
OE 1

Q8 19 (31)
Q7 16 (25)
Q6 15 (28)
Q5 12 (30)
Q4 9 (29)
Q3 6 (35)
Q2 5 (34)
Q1 2 (33)

109D

CK.CPU2.SQST.SQ+ (244)

-2701
74F374
U1306

(10) 18 D8
(14) 17 D7
(9) 14 D6
(8) 13 D5
(7) 8 D4
(13) 7 D3
(6) 4 D2
(5) 3 D1

CLK 11
OE 1

Q8 19 (26)
Q7 16 (124)
Q6 15 (123)
Q5 12 (122)
Q4 9 (121)
Q3 6 (120)
Q2 5 (119)
Q1 2 (118)

16/ BP.S.BUS+ 109E 139B 20C 70A 90C

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 182J-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

SQ11

	SEQUENCER - A900 LED & DECODE	HEWLETT PACKARD
		12201-60001
		D-12201-60001-61

SQ 11

REVISIONS			
ZONE	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	mef/ko	10/27/82
B	CORRECTED NUMBERS ON 74F374	mef/ko	2/23/83

D-12201-60001-62

MAIN OSCILLATOR
1813-0237
HY4550 (DIPOSC)
30 MHZ
VCC=14
GND= 7
U0108
8 SQ.DOT+ (359)

-0681
74S00
U0206

SQ.SWBOTS-(413)

-0681
74S00
U0206
8 SQ.CLOCK BASE+

+5M
R1 1K
R2 1K

143D FP.EXT.CLK.EN- (336)
143D FP.EXT.CLK- (335)

1810-0256
+5
2X10K
U050A

135C BP.CPU.FREEZE- (181)
135C BP.PE.FREEZE- (105)

-0686
74S11
U0808
6 SQ.CPU.FRZ- (358)

-2654
74F157
U0208
(249) CK.A.MEM+
(185) CK.A.CAC+
(110) CK.A.CPU+

DELAY LINE
1813-0340
HY 5072
U0307
Vcc=14
GND= 7
IN
(455) CK.A.MEM.D50.BP+ 40D 134D
(334) CK.A.MEM.D30.BP+ 134D
(307) CK.A.MEM.D20.BP+ 40C 134D

-2701
74F374
U0308
(252) CK.A.SCLK.SQ+
(250) CK.A.MEM.MC+ 134D
(241) CK.A.CAC1.CA+ 134D
(242) CK.A.CAC2.CA+ 134D
(21) CK.A.CPU1.SQ+ 20C 30D 40B 80D
(18) CK.A.CPU2.SQ+ 20D 40E 80B 100E
(246) CK.A.CPU3.DP+ 134D
(247) CK.A.CPU4.DP+ 134D
(275)
SQ.GND.TMP+(1)

-2698
74F240
U0107
(191) LBP.SCLK- 134D
(17) SQ.PULLUP+ 10E 20D 30B 70B 110C
SQ.LAST.30NS- (367)

-2936
74F151
U0106
(251) CK.A.SCLK+

-2701
74F374
U0207
SQ.LAST.30NS+ (296)

-1158
74S51
U0103
SQ.PRE.HALF+(377)

(357) SQ.CPU.CLK+
(274) SQ.CAC.CLK+
(277) SQ.DLY.MEM.CLK+
(156) SQ.MEM.CLK+
SQ.SCLK+ (205)
SQ.HALF.TIME+ (360)
SQ.HALF.TIME- (278)
SQ.SCLK- (305)
SQ.LAST.30NS+ (296)

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

■ POWERED FROM +5M (VCCM)

SQ12

	SEQUENCER-A900 CLOCKS	HEWLETT PACKARD
	12201-60001	
	D-12201-60001-62	

		D-12201-60001-63	
A	AS ISSUED	aef/ko	10/27/82

BP.UIR.REG+ 89A 10A 40E 100B

46	(38)	P1-30C	BP.UIR.REG46+
45	(27)	P1-30B	
44	(67)	P1-30A	
43	(149)	P1-29D	
42	(148)	P1-29C	
41	(147)	P1-29B	
40	(146)	P1-29A	
39	(144)	P1-27D	
38	(143)	P1-27C	
37	(142)	P1-27B	
36	(183)	P1-27A	
35	(182)	P1-26D	
34	(181)	P1-26C	
33	(180)	P1-26B	
32	(179)	P1-26A	
31	(178)	P1-25D	
30	(141)	P1-25C	
29	(140)	P1-25B	
28	(139)	P1-25A	
27	(138)	P1-24D	
26	(137)	P1-24C	
25	(177)	P1-24B	
24	(176)	P1-23D	BP.UIR.REG24+
19	(175)	P1-22C	BP.UIR.REG19+
18	(174)	P1-22B	
17	(173)	P1-22A	
16	(172)	P1-21D	
15	(171)	P1-21C	
14	(136)	P1-21B	
13	(135)	P1-21A	
12	(170)	P1-19D	
11	(169)	P1-19C	
10	(168)	P1-19B	
9	(185)	P1-19A	
8	(184)	P1-18D	
7	(152)	P1-18C	
6	(151)	P1-18B	
5	(150)	P1-18A	
4	(145)	P1-17D	
3	(109)	P1-17C	
2	(108)	P1-17B	
1	(134)	P1-17A	
0	(107)	P1-16D	BP.UIR.REG0+

89E 110C BP.R2.UIR.REG+

23	(167)	P1-23C	BP.R2.UIR.REG23+
22	(166)	P1-23B	
21	(165)	P1-23A	
20	(164)	P1-22D	BP.R2.UIR.REG20+

BP.T.BUS15+

P1-16C	(234)	15	
P1-16B	(233)	14	
P1-15D	(232)	13	
P1-15C	(231)	12	
P1-15B	(229)	11	
P1-15A	(236)	10	
P1-14D	(235)	9	
P1-14C	(132)	8	
P1-14B	(131)	7	
P1-14A	(130)	6	
P1-13D	(127)	5	
P1-13C	(129)	4	
P1-13B	(128)	3	
P1-13A	(106)	2	
P1-11D	(126)	1	
P1-11C	(125)	0	B.P.T.BUS0+

20E 110B BP.T.BUS+

BR.S.BUS15+

P1-39B	(31)	15	
P1-38D	(25)	14	
P1-38C	(28)	13	
P1-38B	(30)	12	
P1-37D	(29)	11	
P1-37C	(35)	10	
P1-37B	(34)	9	
P1-37A	(33)	8	
P1-35D	(26)	7	
P1-35C	(124)	6	
P1-35B	(123)	5	
P1-35A	(122)	4	
P1-34D	(121)	3	
P1-34C	(120)	2	
P1-34B	(119)	1	
P1-34A	(118)	0	BR.S.BUS0+

109E 119D 20C 70A 90C BP.S.BUS+

MC1674
CA147E

P1-09C	BP.R2.STORE.EN-	(228)	110C U1408-4
P1-09D	BP.MISSED.TICK-	(117)	100C
P1-32D	BP.KIS.S.OFF-	(163)	110A
P1-10D	BP.CPU.FREEZE-	(161)	120B
P1-10C	BP.PE.FREEZE-	(105)	120B
P1-33A	BP.IND.INT-	(162)	100C
P1-40C	BP.JTAB.INT-	(226)	100C
P1-40B	BP.CNDX.MET+	(37)	10D 40D
P1-33B	LBP.PDN+	(101)	119C 30B
P1-08D	CK.A.CPU4.LED.BP+	(248)	110C

U308-6	129B	CK.A.CPU3.DP+ (246)	P1-06A
-5	129B	CK.A.CPU4.DP+ (247)	P1-06B
-16	129B	CK.A.CAC1.CA+ (241)	P1-10A
-15	129B	CK.A.CAC2.CA+ (242)	P1-10B
-19	129B	CK.A.MEM.MC+ (250)	P1-31D
307-4	129A 40C	CK.A.MEM.D20.BP+ (307)	P1-33C
-8	129A 40D	CK.A.MEM.D50.BP+ (455)	P1-33D
-10	129A	CK.A.MEM.D30.BP+ (334)	P1-31B
1605-15	109C	BP.UINTP+ (133)	P1-11B
705-12	19D 29D 30E	BP.NO.EXECUTE- (36)	P1-32C
1408-11	119B	BP.ACCL.STOT- (225)	P1-39C
-13	119B	BP.LED.STOT- (227)	P1-09B
107-12	129C	LBP.SCLK- (191)	P1-32B

CA111E

NOTE:
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ALL RESISTANCE IN OHMS.
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NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

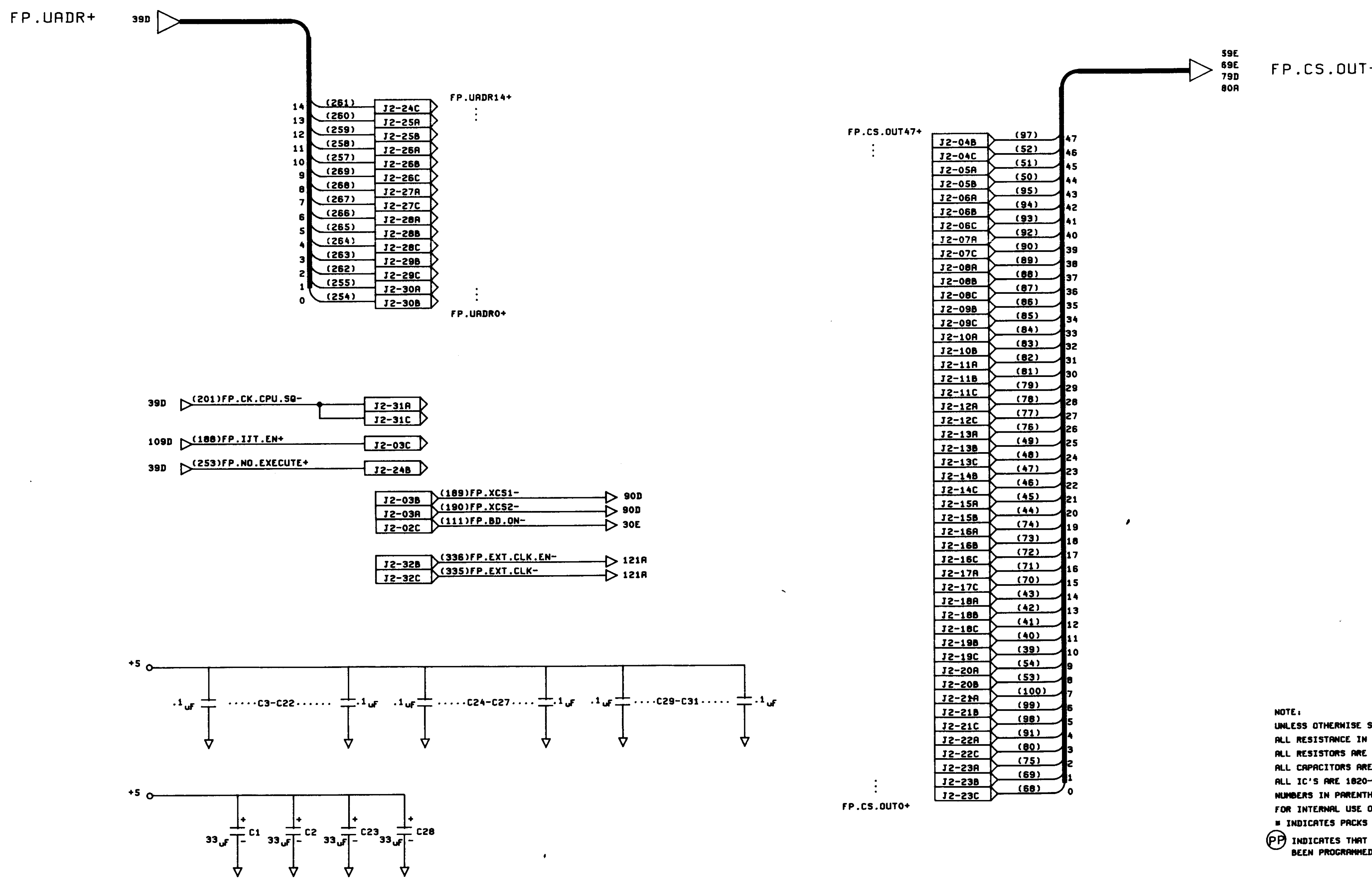
SQ13

	SEQUENCER - A900 BACKPLANE	HEWLETT PACKARD
	12201-60001	
	D-12201-60001-63	

SQ13

D-12201-60001-64

REV	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	maf/ko	10/27/82



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED

SQ14

SEQUENCER - A900
FRONTPLANE

HEWLETT PACKARD

12201-60001

D-12201-60001-64

S Q 14

Chapter 4
Data Path Section

4.1 Introduction

This chapter covers the block diagram description and theory of operation of the data path (DP) card. Also, to understand the operation of a microprogrammed computer, it is necessary to have some knowledge of its microprogramming aspects. For the A900 the HP 92049A RTE Microprogramming Package Reference Manual, Part No. 92049-90001, contains the required information.

The Microprogramming Reference Manual defines the mnemonics of microinstructions and microorders used in this manual.

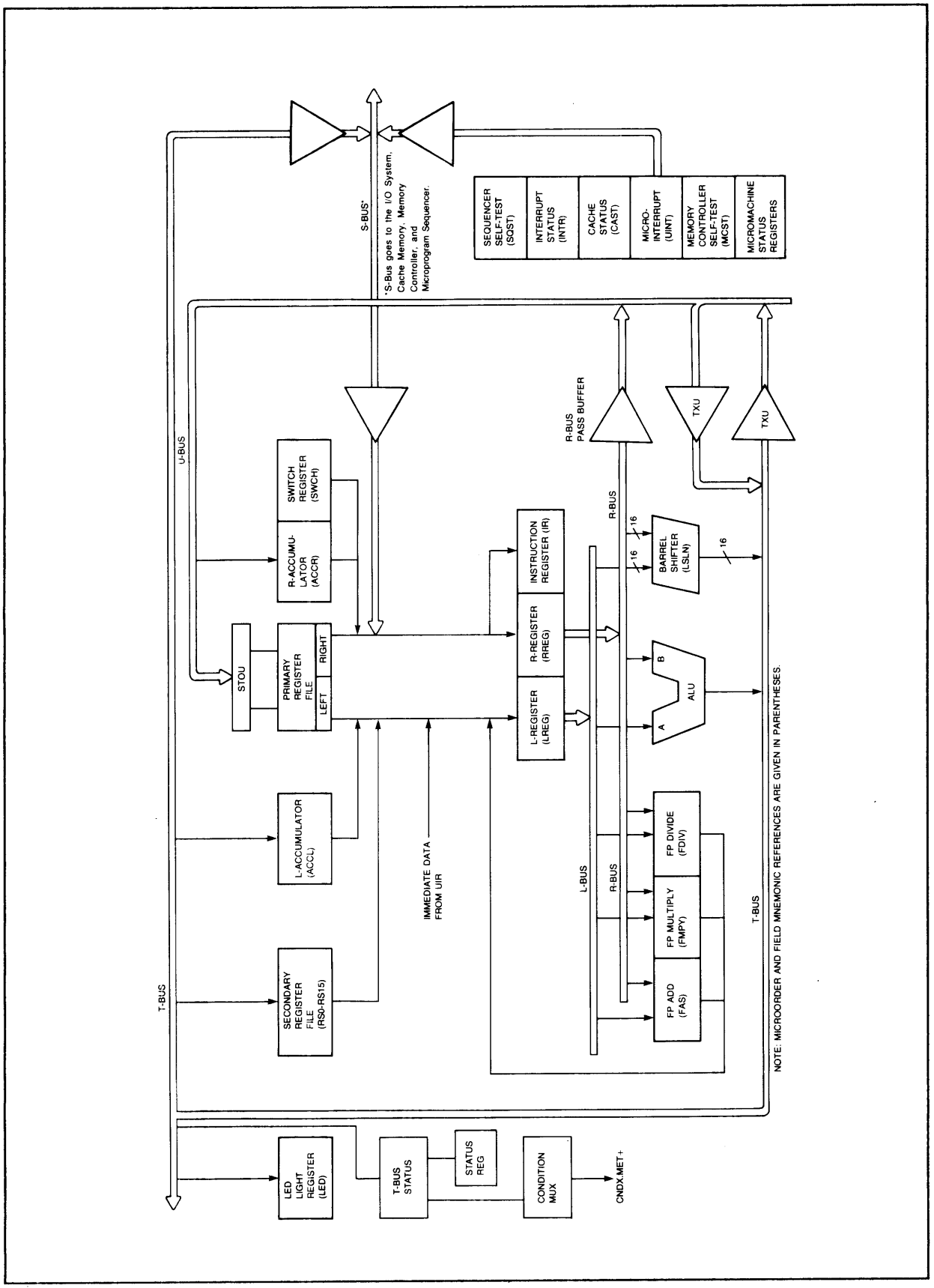
4.2 Block Description

The DP card contains mostly data path circuitry, although it also has the condition selection function which is used by the SQ card. Figure 4-1 is a block diagram of the data path card which is shown in Figure 4-2.

The card is divided into the following functional blocks:

Primary Register File
Secondary Register File
Left and Right Accumulators
Left and Right Registers
Instruction Register
ALU Functions
Floating-Point Functions
Barrel-Shifter
Flags
LED Light Register
Condition Decoders

The terms "right" and "left" are used in some of the functional block names. These names are relative to their position on the block diagram and are used throughout the A900 processor and microprogram terminology.



8300-90A

Figure 4-1. Data Path Card Functional Block Diagram

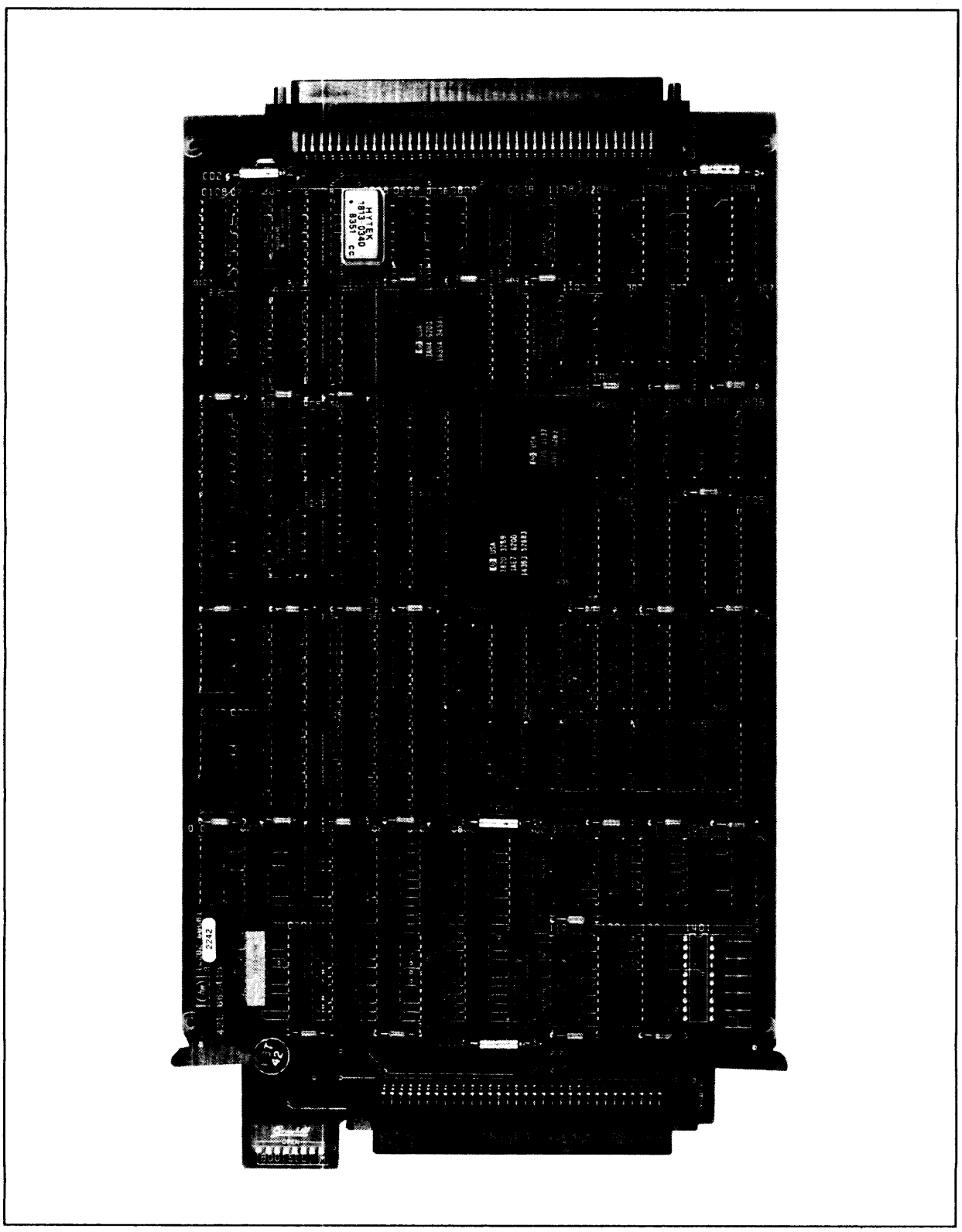


Figure 4-2. Data Path Card (12202-60001)

The paragraphs of 4.2 give a general description of these functional blocks. The paragraphs under 4.3 describe their logical operations (theory of operations).

Operation of the data path from the microprocessor point of view is provided in the HP 92049A Microprogramming Package Reference Manual. The data path is implemented entirely on the DP card.

4.2.1 Primary Register File

The primary register file is located near the top of the DP block diagram. It consists of a pair of single-ported files (RP Left and RP Right) each having 16 registers of 16 bits each. The microprogrammer can treat it as a single double-ported file.

The output of the left file can drive DP.L.IN.BUS+ which is the input to the Left-register (LREG). The output of the right file can drive DP.R.IN.BUS+ which is the input to the Right-register (RREG). The two read addresses indicated by the current microinstruction are supplied to the two files during the second half of the current microcycle. When the files are being read, their outputs are loaded into the LREG and RREG at the end of the microcycle. This allows two file registers to be read at one time.

At the end of the current microcycle the value on the UBUS is loaded into the STOU register. This is the value generated by the microinstruction in the previous cycle. If this value is to be written into the primary register file, the write address from the previous microcycle is used to address both register files during the first half of the following microcycle. A write pulse is generated at this time which writes the data from the STOU register into both files. Since both files are always written simultaneously with the same data at the same address, they always have identical contents (except when they power up and have not yet been written).

The function of the register addressing logic is quite simple. The right read address comes directly from the RREG field of the UIR (microinstruction register) located on the SQ card. The left read address comes from logic which either passes the LREG field of the UIR directly, or forces 0 or 1 for CAB, or forces 2 or 3 for CXY. Depending on the value of the STOU field of the UIR the write address comes from either the left or right read address which is then delayed for two microcycles. It is an exception when microorder TAB is in the STOT field. In this case the delayed write address is forced to either 0 or 1 if the TAB is A/B addressable. This case also forces a write pulse to occur at the appropriate time. Finally the addressing logic must supply the files with the write address during the first half of the microcycle, and with the read address during the second half.

4.2.2 Secondary Register File

The Secondary Register File (RS) is a single ported file with 16 registers of 16 bits each. It receives its address directly from the LREG field of the UIR. Its outputs are enabled to drive the input of the L-Register when RS0 to RS15 appear in the LREG field. If the file is enabled in this way, and a SP0/RSLR occurs in the UIR, the data from the TBUS is written into the file. In this case, the data coming out of the file is undefined.

4.2.3 Left and Right Accumulators

The Left and Right Accumulators (ACCL and ACCR) are both 16-bit transparent latches. ACCL is enabled to drive DP.L.IN.BUS+ whenever LREG/ACCL is present in the UIR (SQ card). The latch opens (becomes transparent) if there was an STOT/ACCL in the previous cycle, or if there is an SP0/ACCL in the current cycle. If the latch is open and enabled in the same cycle, TBUS data can reach the LREG input, which makes ACCL appear as though it were not pipelined.

ACCR is very similar. It drives DP.L.IN.BUS+ if there is an RREG/ACCR, and opens if there was an STOU/ACCR in the previous cycle, or if there is an SP0/ACCR in the present cycle. If it is enabled and open in the same cycle, UBUS data reaches the RREG input, which makes ACCR appear as though it were not pipelined.

4.2.4 Left and Right Registers

The Left and Right Registers (LREG and RREG) are located near the center of the DP Block Diagram. They are both 16-bit registers which are clocked at the end of each microcycle. LREG is loaded from DP.L.IN.BUS+ and continually drives DP.L.BUS+. The LREG input can be driven by the primary or secondary register file or ACCL as described above.

The LREG input has several other sources. A 16-bit buffer drives it with a constant from the IMMEDIATE field of the UIR (SQ card) when IMM or RTNI appears in the OP field. Another 16-bit buffer drives a constant of all ones or all zeros. Ones are driven if LREG/ONES is present or if LREG/SIGN is present and the MSB of LREG is currently high. Zeros are driven if LREG/ZERO is present or if LREG/SIGN is present and the MSB of LREG is currently low. Finally the FXXX register drives the input with the output of one of the floating point chips if FAS, FMPY, or FDIV appear in the LREG field.

RREG is loaded from DP.R.IN.BUS+ and continually drives DP.R.BUS+. The RREG input can be driven from the right side of the primary register file or from ACCR as described above. In addition, a 16-bit buffer drives a constant of all zeros when RREG/ZERO appears, or a constant of all ones when RREG/ONES appears. An eight-bit buffer drives the lower bits with the value of the switch register when RREG/SWCH appears. Finally, a 16-bit buffer drives DP.R.IN.BUS+ with the value on BP.S.BUS+ (the SBUS) when the RREG field specifies a source which is on another card.

4.2.5 Instruction Register

The Instruction Register (IR) is a 16-bit register which is loaded from DP.R.IN.BUS+ at the end of each microcycle which has an SP2/LDIR in the UIR. The value in IR affects the operation of the following microorders: LREG/CAB, LREG/CXY, TBUS/LSLN, TBUS/SRG, SP2/SRG1, SP2/ASG.

4.2.6 Arithmetic Logic Unit

The ALU is a standard 16-bit ALU using look ahead carry. Its inputs come from DP.L.BUS+ and DP.R.BUS+. Its output goes through a 16-bit tristate buffer which drives the result onto BP.T.BUS+ (the TBUS) if any of the following orders were present in the TBUS field of the UIR in the preceding microcycle: ADD0, ADD1, ADDC, LMR0, LMR1, LMRC, RML0, RML1,RMLC, AND, OR, XOR.

The ALU actually performs its operation in the cycle after the operation appears in the UIR. The carry-in for the ALU is determined in the cycle preceding the cycle in which it is used by the ALU. If the operation is arithmetic, the COUT and OVFL conditions are updated at the end of the cycle in which the ALU operation is actually performed.

4.2.7 Barrel-Shifter

The barrel-shifter consists of two shifters, one large (12-bit shifter) and the other small (3-bit shifter). The large shifter receives 32-bits of data from the LBUS and RBUS. It shifts this information left by 0, 4, 8, or 12 bits. The upper-20 bits (out of 32) of the large shifter's output are sent to the small shifter which shifts it left 0, 1, 2, or 3 bits. This produces a 16-bit value which drives the BP.T.BUS+.

The shifter is selected to drive the TBUS if any of the following microorders were present in the UIR during the preceding microcycle: TBUS/LBUS, TBUS/LSLN, TBUS/SRG, SP0/LSL. By selecting the proper combination of the two shifters any logical shift from 0 to 15 bits can be performed. To allow each stage of SRG shift to take only one pass through the data path, the upper bit of the shifter output can be forced to zero, or to the value of the E-Register, or to the value of the upper bit of LREG. Similarly, the lower bit of the shifter output can be forced to zero, or to the value of the E-Register.

4.2.8 Floating-Point Chips

Each floating-point chip's "D" output is connected to DP.D.BUS+ which is the input to the FXXX register. The appropriate chip is used as the source for FXXX when FAS, FMPY, or FDIV appears in the LREG field of the current UIR. As mentioned above in paragraph 4.2.4, the output of FXXX can be used as an input to LREG. At the same time that the enabled chip's "D" outputs are being loaded into LREG, the chip's error output (ERR) is clocked into a register to become the FERR condition during the following microcycle.

Each chip's "A" data inputs are connected to DP.L.BUS+, and its "B" data inputs are connected to DP.R.BUS+. Each chip's "F" control inputs are connected to the TBUS field of the UIR delayed by one microcycle. The chips' clear inputs are asserted low in any cycle in which SP1/FCLR appears in the UIR. Since the chips appear to be loaded, unloaded, and cleared synchronously, none of these inputs have any effect unless the chip is clocked at the appropriate time. If FAS, FMPY, or FDIV appears in the SP2 field of the UIR, the corresponding chip appears to receive a clock at the end of the current microcycle.

In actuality, the chips are clocked before the end of the cycle in order to avoid a hold time problem. The FXXX register is clocked at this same time in order to hold the output data until the end of the cycle. (FXXX does not add a cycle of pipeline delay.)

4.2.9 TBUS and UBUS

The TBUS (mnemonic used in microprogramming) is actually named BP.T.BUS+ on the schematic. It is the source for writing to the secondary register file or to ACCL. In addition it goes off the DP card via the backplane and is used as the source for writing most other registers which are writable by the micromachine. As mentioned above, the TBUS can be driven by the output of the ALU or shifter. There is also a 16-bit bidirectional buffer (TXU) which can drive the value from the UBUS onto the TBUS. This buffer is enabled to drive the TBUS if UBUS appeared in the TBUS field of the UIR during the previous microcycle.

The UBUS is actually named DP.U.BUS+. As mentioned above, it is the source for writing the primary register file and ACCR. It can be driven by the bidirectional buffer (TXU) which connects the TBUS and UBUS. This buffer drives the TBUS value onto the UBUS if there was a TBUS in the UBUS field of the UIR during the previous microcycle. If RBUS appeared in the UBUS field of the preceding microcycle, the RBUS buffer drives the value from the RBUS onto the UBUS. The upper bits of the RBUS buffer can be bypassed by the PG buffer.

If SP0/PG0 is used at the same time as UBUS/RBUS, the upper 6 bits of the UBUS are driven with "00" and the lower 10 bits with the value from the RBUS. Similarly, if SP0/PG30 is used at the same time as UBUS/RBUS, the upper 6 bits of the UBUS are driven with octal 36 and the lower 10 bits with the value from the RBUS.

4.2.10 TBUS Status

The TBUS status logic looks at the value on the TBUS and generates the following status conditions: T0, T15, TZ, TL8Z, TLTZ, TU6Z, TU8Z, TULZ, TON. It is also involved in the generation of the ASGN condition. All these conditions must be tested in the cycle after the value appears on the TBUS.

4.2.11 Flags

The F1 and F2 flags are for internal microcode use only, while the E-Register and the O-Register are macroaccessible registers. Notice that, unless otherwise noted, in the following descriptions microorders in the SP1 field associated with "F1, F2, or O" are conditional if there is an SP1C in the OP field:

a. F1 is set by SP1/STF1, cleared by SP1/CLF1, MEM/JTAB, or MEM/JTDI, SP1/CMF1, and tested using CNDX/F1.

b. F2 is set by SP1/STF2, cleared by SP1/CLF2, MEM/JTAB, or MEM/JTDI, complemented by SP1/CMF2, and tested using CNDX/F2.

c. Flag "O" is set by SP1/STO, cleared by SP1/CLO, and tested using CNDX/O. "O" is also be set if an arithmetic ALU operation generates an overflow during a microcycle with SP1/ENOE (not conditional) in the UIR.

Flag "E" cannot be directly tested, and none of its associated SP1 microorders are conditional. Flag "E" is set and cleared as follows:

a. Set by SP1/STE, and cleared by SP1/CLE.

b. Set, cleared or complemented at the end of a microcycle which contains an SP2/ASG based on the value of the appropriate IR bits.

c. Set if an ALU add operation generates a carry during a microcycle which has an SP1/ENOE. (Note: "E" is not cleared).

d. Set if an ALU subtract operation generates a borrow during a microcycle with an SP1/ENOE.

e. An exception is SP2/ASG occurring along with TBUS/RML1. In this case Flag "E" is set if no borrow is generated.

f. Set or cleared if the preceding line contained a TBUS/SRG and the IR contains an SRG instruction indicating a shift with "E" or a CLE.

The E-Register can be tested using the macroinstruction ASGN (Alter-Skip-Group No-Skip) condition. With an appropriate macroinstruction ASG (Alter-Skip-Group) instruction in the IR, this condition indicates the value which "E" had two microcycles before the condition appears in the UIR.

4.2.12 Condition Selection and Status

The condition selection circuitry and the status register are located on the DP card but the "condition met" signal goes on the SQ card. It is shown in the lower left corner of the DP Block Diagram. The condition multiplexer is made up of five 8:1 multiplexers. The first four select one condition out of a block of eight. The final multiplexer selects the high- or low-true output of one of the first four to produce the CNDX.MET+ signal. The six selects for the two layers of multiplexers come from the TF and CNDX fields of the current microinstruction. One of the bits of the OP field is used to disable the last multiplexer in order to force CNDX.MET+ "true" for certain OP field operations.

The 32 conditions come from a variety of sources throughout the machine. One of the conditions is tied permanently high (indicating TRUE), while another 23 come directly from continuously clocking registers, many of which are on the DP card. The final eight conditions come from the status register. This register is updated with a copy of eight of the other conditions at the end of a microcycle which has an SP0/SU in the UIR.

4.2.13 Instruction Set Emulation

Many of the data path features simplifying the emulation of the HP 1000 instruction set are described in the paragraphs below and the HP 92049A RTE Microprogramming Package Reference Manual. The conventions used to indicate the microinstruction field and microorder is field/microorder; e.g., STOT/TAB is microorder TAB in the STOT field).

a. STOT/TAB writes to the A- or B-Register in the primary register file if the memory address being stored to is 0 or 1 and A/B addressability is enabled. This feature requires interaction with the memory address creation hardware. A/B addressability is very fundamental to the HP 1000 instruction set.

b. LREG/CAB conditionally addresses the A- or B-Registers in the primary register file based on the value of bit 11 of the IR. This is an important feature since it allows one set of microcode to emulate both the "A" and "B" versions of the same macroinstruction.

c. LREG/CXY conditionally addresses the X- or Y-Registers in the primary register file based on the value of bit 3 of the IR. In this case one set of microcode can emulate both the "X" and "Y" versions of the same macroinstruction.

d. SP1/ENOE in a microinstruction causes E- and O-Registers to be updated based on the ALU operation occurring in the current cycle (refer to Flags in the paragraph 4.2.12).

e. TBUS/SRG and SP2/SRG1 in the same microinstruction causes the shifter to execute a 16-bit shift in the following cycle according to the first shift group of the SRG instruction in the IR. It includes updating "E" if a shift with "E" is indicated, or "E" is cleared if the SRG instruction in the IR includes a CLE (this will override the effect of the shift on "E".

f. TBUS/SRG in a microinstruction without SP2/SRG1 causes the shifter to execute a 16-bit shift in the following cycle according to the second shift group of the SRG instruction in the IR. It includes updating "E" if a shift with "E" is indicated. Both of the SRG shifts assume that the quantity to be shifted appears in both LREG and RREG.

g. SRG instruction emulation code results in two consecutive microinstruction cycles containing TBUS/SRG. The first cycle contains SP2/SRG1. The intermediate result is recycled via ACCL and ACCR to avoid a wasted cycle.

h. In the first cycle (contains SP2/ASG in the microinstruction), "E" is cleared and/or complemented based on the appropriate bits of the ASG instruction in the IR. In the second SRG cycle, carry-in to the ALU will be forced "true" if the ASG instruction in the IR includes an IN*. The operation of SP1/ENOE will also be slightly different in this microinstruction line (see above).

i. ASG instruction emulation code assumes that the four cases of PAS, CL*, CM*, and CC* will be vectored to separate lines of emulation code. All four cases (PAS, CL*, AND CC*) use RREG/ZERO as one source, store to CAB, and include SP2/ASG, resulting in the following:

   1. For CL* and CC* the LREG source is ZERO.

   2. For PAS and CM* the LREG source is CAB.

   3. For PAS and CL* the TBUS field contains ADD0.

   4. For CM* and CC* the TBUS field contains RML1.

   These four lines along with the action of the ASG special do all the data manipulation required by an ASG instruction and result in the ASG skip condition. The ASGN (Alter-Skip-Group No-Skip) condition should be tested two lines after ASG appears in the SP2 field. It examines the old value of "E", bits of LREG, TBUS status, and the ASG instruction in the IR to determine if the instruction should skip. It is true if no skip occurs.

4.3 Theory of Operation

The theory of operation for the A900 Computer data path card is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 4-1 and the schematics at the end of this section of the manual. The schematic pages are referred to by a two letter card acronym followed by a page number; e.g., the schematics of the data path card are DP1, DP2, etc.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U0907 (DP93D) refers to part U0907 on the data path card in row 9/column 7, which is shown on schematic page U9 at horizontal location 3 and vertical location D.

4.3.1 Primary Register File

The major parts of the Primary Register File is shown on schematic sheet DP1.

The STOU register is composed of U1605 (DP12B) and U1604 (DP12C). It is loaded from DP.U.BUS[15:0]+ at the end of each microcycle, and continually drives DP.STOU.REG[15:0]+. It is a dual-ported file with a right side and a left side, referring to right and left locations on the block diagram.

The right primary-register file (RREG) is composed of four 16 by 4 RAMs: U1607 (DP13B), U1507 (DP15B), U1606 (DP16B), and U1506 (DP17B). Its inputs come from DP.STOU[15:0]+ and it is addressed by DP.R.ADR[3:0]-.

Its outputs drive DP.R.IN.BUS[15:0]+ when DP.R.RP.CS- is low.

The left primary-register file (LREG) is composed of another four RAMs: U1407 (DP13D), U1307 (DP15D), U1406 (DP16D), and U1206 (DP17D). Its inputs also come from DP.STOU.REG[15:0]+. It is addressed by DP.L.ADR[3:0]- and its outputs drive DP.L.IN.BUS[15:0]+ when DP.L.RP.CS- is low.

4.3.1.1 Address Generation

The address generation logic for the primary files is shown on schematic sheet DP9. DP.R.ADR[3:0]- comes from a 2:1 multiplexer located at U1207 (DP97B). The select of this MUX is connected directly to the microcycle clock (CK.CPU3.DP+). During the first half of each microcycle, the MUX selects the write address which is present on DP.WR.TAB.ADR[3:0]+. During the second half, it selects the read address from BP.UIR.REG[29:26]+, the lower four bits of the ~~LREG~~ RREG field.

The 2:1 multiplexer located at U1107 (DP97C) generates DP.L.ADR[3:0]- in a similar manner. Its select comes from the same microcycle clock, and during the first half of the cycle it selects the write address from DP.WR.TAB.ADR[3:0]+. During the second half of the cycle it selects the read address from DP.LREG.ADR[3:0]+. These signals come from the LREG/ADDR PLA located at U1007 (DP93C). The program for the LREG Address Generation PLA is listed in Figure 4-3.

The PLA looks at all six bits of the LREG field (BP.UIR.REG[37:32]+), plus one bit of the OP field (BP.UIR.REG44+), plus two bits from the IR (DP.IR.REG3+ and DP.IR.REG11+). The OP field bit is used to differentiate between 4- or 5-bit and 6-bit LREG fields. For most LREG values, the lower four bits of the LREG field are simply passed to DP.LREG.ADR[3:0]+ directly. For LREG/CAB.CAB, LREG/ZERO.CAB, and LREG/ACCL.CAB the PAL produces an address of 0 or 1 based on the value of DP.IR.REG11+. For LREG/CXY.CXY and LREG/ACCL.CXY the address produced is a 2 or 3 based on the value of DP.IR.REG3+. Notice that the PLA does not distinguish between 4-bit and 5-bit LREG fields.

4.3.1.2 Write Address Signals

The write address for the primary file must be delayed by two microcycles. The 2:1 registered multiplexer located at U0908 (DP94B) selects between the left and right read addresses based on one bit of the STOU field (BP.UIR.REG24+). For STOU/NOP and STOU/LR, it selects DP.LREG.ADR[3:0]+. For STOU/ACCR and STOU/RR it selects BP.UIR.REG[29:26]+. At the end of the current microcycle, the selected value is loaded into the register to become DP.WR.ADR[3:1]+ and BP.B.DP.ADR+. A gate located at U0808 (DP95B) generates BP.AB.DP.WR+ which goes "high" when DP.WR.ADR[3:1]+ and DP.R2.RP.WR- all go "low". This signal is sent to the CA card to indicate that the data path is writing to the A- or B-Register. It is used in conjunction with BP.B.DP.ADR+ to update the TA and TB registers.(MC 150 0)

The CA card sends the data path a similar set of signals to indicate when the A- or B-Registers should be updated due to a TAB store to "A" or "B". The 2:1 registered multiplexer located at U1108 (DP95B) normally selects DP.WR.ADR[3:1]+ and BP.B.DP.ADR+. However, if the cache is storing to TA or TB, it asserts BP.AB.CA.WR- low. This causes the MUX to select a constant of "0" or "1", depending on the value of BP.B.CA.ADR+, which goes high if TB is written to.

The value selected by the MUX will be loaded into the MUX register at the end of each microcycle. This produces DP.WR.TAB.ADR[3:0]+ which is the rank-three version of the write address. It is the version used by the two read/write multiplexers.

To determine whether the primary file should be written, the RREG/STOU PLA U0907 (DP93D) looks at the STOU field (BP.UIR.REG[25:24]+) and DP.R1.STORE.EN-. The code for the RREG/STOU PLA is listed in Figure 4-4.

If DP.R1.STORE.EN- is "low" and STOU/LR or STOU/RR is present, the signal DP.R1.RP.WR- goes "low". The PLA also produces DP.R1.ACCR.STOU- which goes "low" when STOU/ACCR is present and DP.R1.STORE.EN- is "low".

```
*          B B B B B B B       D D D D
*          P P P P P P P   D   P P P P
*        D . . . . . . . D P   . . . .
*        P U U U U U U U P .   L L L L
*        . I I I I I I I . I   R R R R D
*        I R R R R R R R L R   E E E E P
*        R . . . . . . . . .   G G G G .
*        . R R R R R R R B R   . . . . L
*        R E E E E E E E U E   A A A A .
*        E G G G G G G G S G   D D D D B
*        G 4 3 3 3 3 3 3 1 1   R R R R I
*        3 4 7 6 5 4 3 2 5 1   3 2 1 0 T
*        + + + + + + + + + +   + + + + +
*        0 0 0 0 0 0 0 0 1 0   1 1 1 1 1
*PIN:    8 7 6 5 4 3 2 1 1 9   9 8 7 6 5
 SENSE:                       H H H H H
*                             B B B B B B
*ROW     7 6 5 4 3 2 1 0 1 0   9 8 7 6 5
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0     - - - - H H L H - -   . . . . A   ONES 4/5/6   --1101
   1     - - - - H L H H H -   . . . . A   SIGN 4/5/6   --1011
   2     - H - - H H H H - H   . . . A .   CAB  4/5     --1111
   3     - L L - H H H H - H   . . . A .   CAB       6   0-1111
   4     - L H L L H H H - H   . . . A .   CAB       6   100111
   5     L H - - H H H L - -   . . A . .   CXY  4/5     --1110
   6     H H - - H H H L - -   . . A A .   CXY  4/5     --1110
   7     L L L - H H H L - -   . . A . .   CXY       6   0-1110
   8     H L L - H H H L - -   . . A A .   CXY       6   0-1110
   9     - - - - - - - L H -   . . . A .   PASS 4/5/6   ----0-
  10     - - - - - H L - - -   . A . . .   PASS 4/5/6   ----0-
  11     - - - - H - L - - -   A . . . .   PASS 4/5/6   ----0-
  12     - - - - - L - H - -   . . . A .   PASS 4/5/6   ---0--
  13     - - - - - L H - - -   . . A . .   PASS 4/5/6   ---0--
  14     - - - - H L - - - -   A . . . .   PASS 4/5/6   ---0--
  15     - H - - L - - H - -   . . . A .   PASS 4/5     --0---
  16     - H - - L - H - - -   . . A . .   PASS 4/5     --0---
  17     - H - - L H - - - -   . A . . .   PASS 4/5     --0---
  18     - L L - L - - H - -   . . . A .   PASS       6   0-0---
  19     - L L - L - H - - -   . . A . .   PASS       6   0-0---
  20     - L L - L H - - - -   . A . . .   PASS       6   0-0---
  21     - L H L - - H L - -   . . A . .   PASS       6   10---0
  22     - L H L - H - L - -   . A . . .   PASS       6   10---0
  23     - L H L H - - L - -   A . . . .   PASS       6   10---0
  24     - L H L H - - H - -   . . . A .   PASS       6   101---
  25     - L H L H - H - - -   . . A . .   PASS       6   101---
  26     - L H L H H - - - -   . A . . .   PASS       6   101---
  27     - L H - H - - - - -   A . . . .   PASS       6   1-1---
  28     - L H H - - - H - -   . . . A .   PASS       6   11----
  29     - L H H - - H - - -   . . A . .   PASS       6   11----
  30     - L H H - H - - - -   . A . . .   PASS       6   11----
```

Figure 4-3. LREG Address Generation PLA (U1007) Code

```
*
*                                          D
*                                  D       P
*                                  P       .
*       D D D D D D D D C .         R D       D
*       P P P P P P P P K R   D 1 P   D D P
*       . . . . . . . . . 1   P . . D P P .
*       U U U U U U U U A .   . A S P . . A
*       I I I I I I I I . S   R C W . S R C
*       R R R R R R R R C T   1 C C R . . C
*       . . . . . . . . P O   . R H . B B R
*       R R R R R R R R U R   R . , R U I .
*       E E E E E E E E 3 E   P S R P S T R
*       G G G G G G G G . .   . T R . . . R
*       3 3 2 2 2 2 2 2 D E   W O E E E E E
*       1 0 9 8 7 6 5 4 P N   R U G N N N G
*       + + + + + + + + - -   - - - + - - -
*
*       0 0 0 0 0 0 0 0 1 0   1 1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 1 9   8 7 6 5 4 3 2
*
 SENSE:                       L L L H L L L
*                       B B   B B B B B B B
*ROW    7 6 5 4 3 2 1 0 1 0   8 7 6 5 4 3 2
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    L H - - - - - - L -   . . . . . . A  RREG/ACCR
   1    L L L H H - - - L -   . . . . . A .  RREG/ZERO,ONES
   2    L L - L - - - - L -   . . . . A . .  RREG/SQST - PVRH,PNTR - FA
   3    L L - H L - - - L -   . . . . A . .  RREG/INTR,MCST,MAPS,CAST
   4    L L H H H L - - L -   . . . . A . .  RREG/BPRM
   5    H H - - - - - - L -   . . . . A . .  RREG/TAB
   6    H L - - - - - - - -   . . . A . . .  RREG/Rx
   7    L L H H H H - - L -   . . A . . . .  RREG/SWCH
   8    - - - - - - L H - L   . A . . . . .  STOU/ACCR
   9    - - - - - - H - - L   A . . . . . .  STOU/LR,RR
*
*
```

Figure 4-4. RREG/STOU PLA (U0907) Code

4.3.1.3 Cache and Data Path Write

At the end of each microcycle DP.R1.RP.WR- is clocked into the register located at U0404 (DP123B) to become DP.R2.RP.WR-. This signal is used in the generation of BP.AB.DP.WR+ (refer to Write Address Signals, above).

It is also combined with BP.AB.CA.WR- by the gate located at U0204 (DP122A) to form DP.R2.RP.TAB.WR+. When this rank-two signal goes "high" it indicates that either the cache or data path has determined that the primary register file should be written during the first half of the following microcycle. At the end of the microcycle this signal is clocked into the register located at U0404 (DP123B) to form DP.R3.RP.TAB.WR+.

The gate at U1105 (DP11D) causes CK.CPU3.D20.RP- (DP.RP.WE-) to go "low" during an early portion of the microcycle if DP.R3.RP.TAB.WR+ is "high". This write pulse is sent to all of the RAMS of the primary register file. The chip select (CS) input of the RAM must also be "low" for the write to occur. To assure this, the CS input is brought "low" during the first half of each microcycle. It is also brought "low" during the second half of the microcycle if the register file is being used as an RREG (or LREG) source.

For the right side, the gate located at U0302 (DP11D) causes CK.CPU3.CR.DP- (DP.R.RP.CS-) to go "low" when either CK.CPU3.DP+ or DP.R.RP.EN+ is "high". For the left side, another gate located at U0302 (DP11D) causes CK.CPU3.CL.DP- (DP.L.RP.CS-) to go "low" when either CK.CPU3.DP+ or DP.L.RP.EN+ is "high". The timing of the write pulse and chip select is shown in Figure 4-5.

The figure shows the signals for the right side, but timing for the left side is analogous.

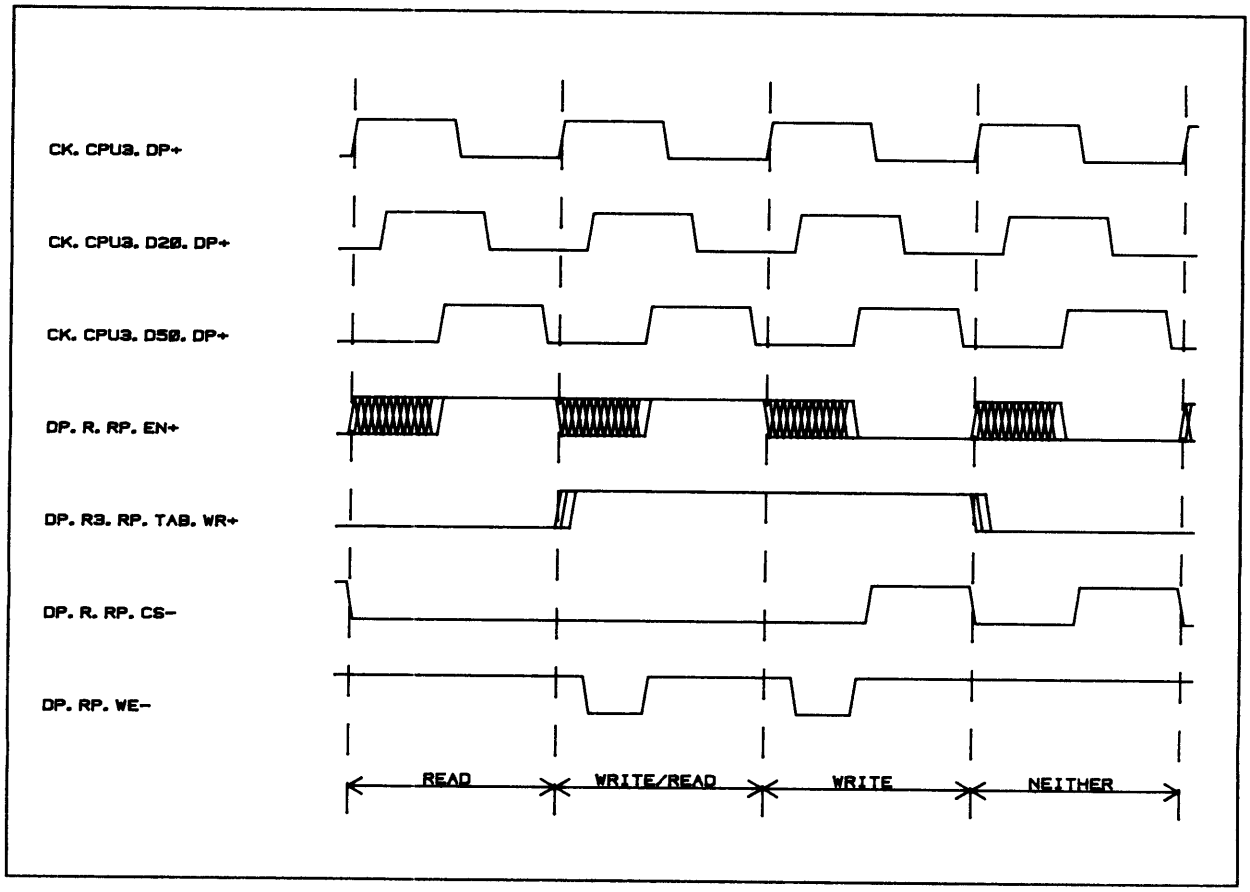


Figure 4-5. Timing of Write Pulse and Chip Select of Primary File

4.3.2 Secondary Register File

The Secondary Register File (RS) is shown on schematic sheet DP2. It consists of four 16 by 4 RAMs: U0708 (DP23B), U0608 (DP24B), U0706 (DP26B), and U0406 (DP27B). Its inputs come from BP.T.BUS[15:0]+ and it is addressed by the lower four bits of the LREG field (BP.UIR.REG[35:32]+). Its outputs are enabled to drive DP.L.IN.BUS[15:0]+ when CK.CPU4.CS.DP- (DP.RS.CE-) is "low". The file is written when CK.CPU3.D50.RS- (DP.RS.WE-) goes "low" at the same time that DP.RS.CE- is "low". DP.RS.WE- is generated by a gate located at U1105 (DP21B). This gate passes an inverted version of the delayed microcycle clock when DP.RSLR.SP0+ and BP.NO.EXECUTE- are both "high".

During the write, the files outputs are disabled. Therefore, the value loaded into the LREG in a cycle which contains an SP0/RSLR is undefined. DP.RS.CE- is generated by gate U0308 (DP21B). This gate passes the microcycle clock whenever DP.RS.EN- is "low". This assures that the register file is disabled during the first half of the microcycle. Figure 4-6 shows the timing of the write pulse and chip enable.

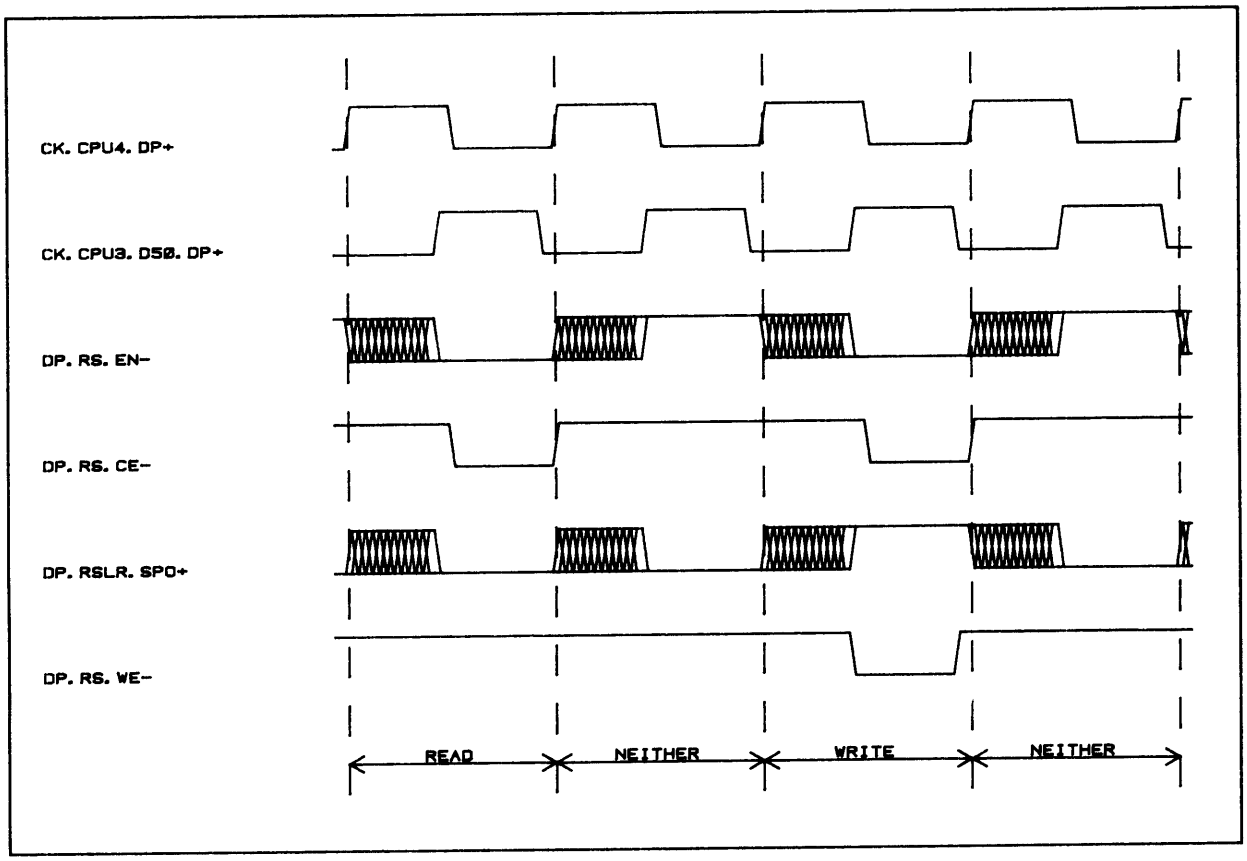


Figure 4-6. Secondary File Write Pulse and Chip Enable Timing

4.3.3 Left and Right Accumulators

The ACCL register is composed of a pair of transparent latches, U0606 (DP34D) and U0506 (DP34E). Its inputs come from DP.T.BUS+, and it drives DP.L.IN.BUS+ when DP.ACCL.LREG- is asserted "low". The latch opens (becomes transparent) when CK.CPU4.ACCL.DP- goes "high". This signal, which is generated by the IOA gate located at U1504 (DP117E), goes "high" during the second half of a microcycle in which either DP.ACCL.SP0- or BP.ACCL.STOT- is "low". The latter of these signals is generated on the SQ card (refer to Chapter 3).

The ACCR register is composed of a pair of transparent latches, U1505 (DP34A) and U1603 (DP34B). Its inputs come from DP.U.BUS[15:0]+, and it drives DP.R.IN.BUS[15:0]+ when DP.ACCR.RREG- is asserted "low". The latch opens (becomes transparent) when CK.CPU4.ACCR.DP- goes high. This signal which is generated by the IOA gate U1504 (DP117E), goes "high" during the second half of a microcycle in which either DP.ACCR.SP0- or DP.R2.ACCR.STOU- is "low". The latter of these signals is a version of DP.R1.ACCR.STOU- (see above) which has been delayed one microcycle by the register located at U0404 (DP123B).

4.3.4 Left and Right Registers (LREG and RREG)

The LREG and RREG registers and several of their sources are shown on schematic sheet DP3. LREG is composed of two registers, U1205 (DP38D) and U1305 (DP38E). At the end of each microcycle it is loaded from DP.L.IN.BUS[15:0]+, and it continually drives DP.L.BUS[15:0]+. The remaining LREG sources are the FXXX register, the IMM buffer, and the ZERO/ONES/SIGN buffer. The FXXX register is described in paragraph 4.3.8 (Floating Point Chips) below.

The IMM buffer is composed of U0206 (DP32D) and U0408 (DP32E). Its inputs come from the IMMEDIATE field of the UIR (BP.UIR.REG[43:36]+ and BP.UIR.REG[7:0]+). It drives DP.L.IN.BUS[15:0]+ when DP.IMM.EN- goes "low". The ZERO/ONES/SIGN buffer is composed of U0106 (DP36D) and U0407 (DP36E). All sixteen of its inputs are connected to DP.L.BIT+, and it drives DP.L.IN.BUS[15:0]+ when DP.L.BIT.EN- goes "low".

4.3.4.1 LREG Source

The LREG source is determined by the LREG-SEL PLA which is U0306 (DP93E). The code for this PLA is shown in Figure 4-7.

```
*
*
*       D D | D D D D D D | C                   D D D
*       P P | P P P P P P | K             D     P P P D
*       . . | . . . . . . | .   D         P D   . . . P
*       U U | U U U U U U | A   P     D . P A F F . .
*       I I | I I I I I I | .   . D P L . C D M F
*       R R | R R R R R R | C   L P . . F C I P A
*       . . | . . . . . . | P   . . I B X L V Y S
*       R R | R R R R R R | U   R R M I X . . . .
*       E E | E E E E E E | 3   P S M T X L L L L
*       G G | G G G G G G | .   . . . . . R R R R
*       4 4 | 3 3 3 3 3 3 | D   E E E E E E E E E
*       5 4 | 7 6 5 4 3 2 | P   N N N N N G G G G
*       + + | + + + + + + | +   - - - - - - - - -
*
*       0 0 | 0 0 0 0 0 0 | 0   1 1 1 1 1 1 1 1 1
*PIN:   8 7 | 6 5 4 3 2 1 | 9   9 8 7 6 5 4 3 2 1
*
 SENSE:                     |     H L L L L L L L L
*                           | B   B B B B B B B B B
*ROW    7 6 | 5 4 3 2 1 0 | 0   9 8 7 6 5 4 3 2 1
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - | - - - - L L | -   . . . . . . . . A   FAS
   1    - - | - - - - L H | -   . . . . . . . A .   FMPY
   2    - - | - - - - H - | -   . . . . . . A . .   FDIV
   3    L H | - H - - - - | L   . . . . . A . . .   ACCL      5
   4    - L | L H - - - - | L   . . . . . A . . .   ACCL      6
   5    L H | - L H L L - | L   . . . . A . . . .   FAS/FMPY  5
   6    - L | L L H L L - | L   . . . . A . . . .   FAS/FMPY  6
   7    L H | - L H L H L | L   . . . . A . . . .   FDIV      5
   8    - L | L L H L H L | L   . . . . A . . . .   FDIV      6
   9    L H | - L H L H H | L   . . . A . . . . .   SIGN      5
  10    - L | L L H L H H | L   . . . A . . . . .   SIGN      6
  11    L H | - L H H L - | L   . . . A . . . . .   ZERO,ONES 5
  12    - L | L L H H L - | L   . . . A . . . . .   ZERO,ONES 6
  13    - L | H L L - - - | L   . . . A . . . . .   ZERO      6
  14    H H | - - - - - - | L   . . A . . . . . .   OP/IMM   4
  15    - L | H H - - - - | -   . A . . . . . . .   RS0-RS15  6
  16    L H | - L L - - - | -   A . . . . . . . .   A-R7      5
  17    - L | L L L - - - | -   A . . . . . . . .   A-R7      6
  18    L H | - L H H H - | -   A . . . . . . . .   CXY,CAB   5
  19    - L | L L H H H - | -   A . . . . . . . .   CXY,CAB   6
20    - L H L H - - - - | A . . . . . . . .   R8-R15     6
 *
 *
```

Figure 4-7. LREG Select PLA (U0306) Code

Its inputs include the six bits of the LREG field (BP.UIR.REG[37:32]+) and two bits of the OP field (BP.UIR.REG[45:44]+). The OP field bits are used to distinguish between 4, 5, and 6 bit LREG fields, and to detect when an OP/IMM or OP/RTNI is present. Six of the outputs of the PLA are used to select one of the possible LREG sources to drive DP.L.IN.BUS[15:0]+. The three remaining outputs are used to select the source for the FXXX register which are described in paragraph 4.3.8. Table 4-1 specifies which source is selected for the various OP and LREG microorders.

The primary register file is always enabled during the first half of each microcycle to allow writes to occur. To prevent the other sources from contending for attention during this time, the microcycle clock (CK.CPU3.DP+) is the final input to the PLA. It disables all sources except the primary and secondary register files during the first half of the microcycle. As mentioned above the register file enables are controlled by individual gates for timing reasons. The DP.L.BIT+ signal used as the input to the ZERO/ONES/SIGN buffer is generated by the LREG ADDR PLA, U1007 (DP93C). It goes "high" for LREG/ONES. For LREG/SIGN it is a copy of DP.L.BUS15+. For all other LREG orders it remains "low". The code for the LREG-ADDR PLA is listed in Figure 4-7 (LREG Select) above.

4.3.4.2 RREG Sources

RREG is composed of two registers, U1306 (DP38B) and U0701 (DP38C). At the end of each microcycle it is loaded from DP.R.IN.BUS[15:0]+, and it continually drives DP.R.BUS[15:0]+. The remaining RREG sources are the SWCH buffer, the SBUS buffer, and the ZERO/ONES buffer. The SWCH buffer is U0301 (DP27D). Each of its eight inputs is normally pulled "high" by a resistor located at U0201 (DP25D). However, the eight switch-register switches in the DIP switch U0101 (DP25D) can pull any of the inputs "low".

The buffer drives DP.R.IN.BUS[7:0]+ when DP.SWCH.RREG- is "low". The SBUS buffer is composed of U1308 (DP32A) and U1208 (DP32B). Its inputs come from the SBUS (BP.S.BUS[15:0]+). It drives DP.R.IN.BUS[15:0]+ when DP.S.BUS.EN- goes "low". The ZERO/ONES buffer is composed of U1408 (DP36A) and U1608 (DP36B). All sixteen of its inputs are connected to the inverted lower bit of the RREG field (DP.UIR.REG26-), and it drives DP.R.IN.BUS[15:0]+ when DP.R.BIT.EN- goes "low".

The RREG source is determined by the RREG-STOU PLA which is located at U0907 (DP93D). The code for this is listed in Figure 4-4, above. Its inputs include the six bits of the RREG field (BP.UIR.REG[31:26]+). Five of the PLA outputs are used to select one of the possible RREG sources to drive DP.R.IN.BUS[15:0]+. Table 4-2 shows which source is selected for the various RREG microorders.

Table 4-1. Source Selection for OP and LREG Microorders

Microorder	Causes	To Go	Comment
OP/IMM	DP.IMM.EN-	Lo	Overrides others
OP/RTNI	DP.IMM.EN-	Lo	Overrides others
LREG/FAS	DP.FXXX.EN-	Lo	
	and DP.FAS.LREG-	Lo	FXXX source
LREG/FMPY	DP.FXXX.EN-	Lo	
	and DP.FMPY.LREG-	Lo	FXXX source
LREG/FDIV	DP.FXXX.EN-	Lo	
	and DP.FDIV.LREG-	Lo	FXXX source
LREG/ACCL	DP.ACCL.LREG-	Lo	
LREG/ZERO	DP.L.BIT.EN-	Lo	
LREG/ONES	DP.L.BIT.EN-	Lo	
LREG/SIGN	DP.L.BIT.EN-	Lo	
LREG/RS0 to LREG/RS15	DP.RS.EN-	Lo	
LREG/A	DP.L.RP.EN+	Hi	
LREG/B	DP.L.RP.EN+	Hi	
LREG/CAB	DP.L.RP.EN+	Hi	
LREG/CXY	DP.L.RP.EN+	Hi	
LREG/X	DP.L.RP.EN+	Hi	
LREG/Y	DP.L.RP.EN+	Hi	
LREG/R4 to LREG/R15	DP.L.RP.EN+	Hi	

Table 4-2. Source Selection for RREG Microorders

Microorder	Causes	To Go
RREG/SWCH	DP.SWCH.RREG-	Lo
RREG/ACCR	DP.ACCR.RREG-	Lo
RREG/ZERO	DP.R.BIT.EN-	Lo
RREG/ONES	DP.R.BIT.EN-	Lo
RREG/A	DP.R.RP.EN+	Hi
RREG/B	DP.R.RP.EN+	Hi
RREG/X	DP.R.RP.EN+	Hi
RREG/Y	DP.R.RP.EN+	Hi
RREG/R4 to RREG/R15	DP.R.RP.EN+	Hi
RREG/BPRM	DP.S.BUS.EN-	Lo
RREG/CAST	DP.S.BUS.EN-	Lo
RREG/FA	DP.S.BUS.EN-	Lo
RREG/INTR	DP.S.BUS.EN-	Lo
RREG/IOGO	DP.S.BUS.EN-	Lo
RREG/MADR	DP.S.BUS.EN-	Lo
RREG/MAPS	DP.S.BUS.EN-	Lo
RREG/MCST	DP.S.BUS.EN-	Lo
RREG/PNTR	DP.S.BUS.EN-	Lo
RREG/PVRH	DP.S.BUS.EN-	Lo
RREG/PVRL	DP.S.BUS.EN-	Lo
RREG/SQST	DP.S.BUS.EN-	Lo
RREG/TAB	DP.S.BUS.EN-	Lo
RREG/UINT	DP.S.BUS.EN-	Lo

The primary register file is always enabled during the first half of each microcycle to allow writes to occur. To prevent the other sources from contending for attention during this time, the microcycle clock (CK.CPU3.DP+) is also an input to the PLA. It disables all sources except the register file during the first half of the microcycle. The opcodes for RREG/ZERO and RREG/ONES have been chosen so that their inverted lower bit provides the proper input to the ZERO/ONES buffer.

4.3.5 Instruction Register

The IR is composed of U0403 (DP123E) and U1405 (DP124E). It constantly drives DP.IR.REG11+ and DP.IR.REG[9:0]+.

The gate located at U0308 (DP122E) generates a clock which loads it from DP.R.IN.BUS[15:0]+ at the end of each microcycle in which DP.LDIR.SP2- is "low".

4.3.6 Arithmetic Logic Unit

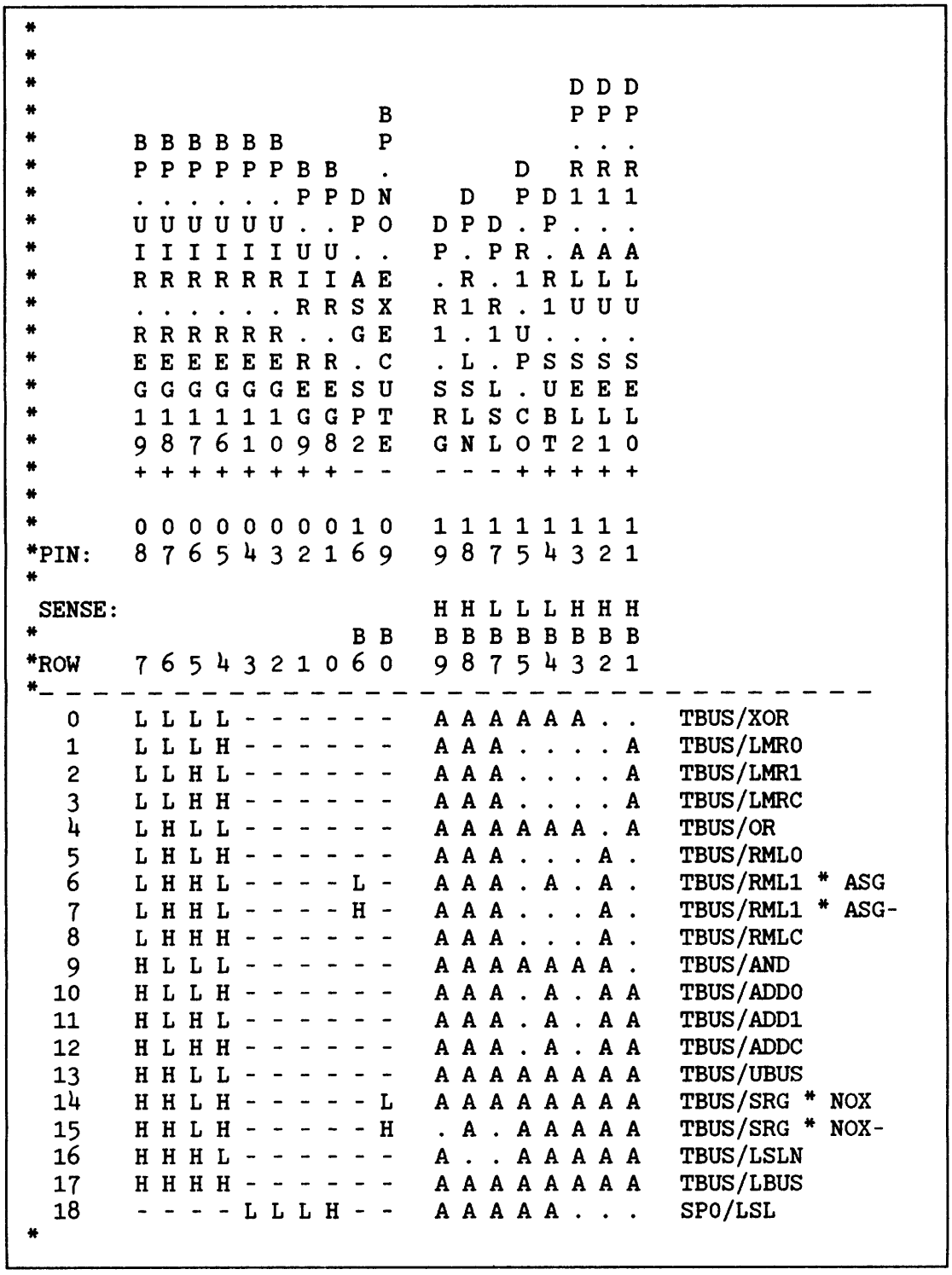
The ALU (Arithmetic Logic Unit) itself appears on schematic sheet DP5. It consists of four 74S381 ALU slices: U1304 (DP52B), U1204 (DP54B), U01004 (DP56B), and U0804 (DP57B). The A inputs come from DP.R.BUS[15:0]+, the B inputs come from DP.L.BUS[15:0]+, and the outputs drive DP.ALU.OUT[15:0]+.

U0904 (DP57D) and U1404 (DP57E) buffer the ALU output. They drive BP.T.BUS[15:0]+ when DP.R2.ALU.EN- is "low". U1104 (DP55D) does carry look-ahead across the four ALU slices. The look-ahead is done in a conventional manner with carry-in to the entire ALU (DP.R2.ALU.CIN0+) being sent to the least significant slice and to the look-ahead chip. The look-ahead chip also receives the generate and propagate outputs (DP.R2.ALU.G[2:0]- and DP.R2.ALU.P[2:0]-) from the lower three slices. It in turn generates the carry-in to the upper three slices (DP.R2.ALU.CIN[3:1]+).

4.3.6.1 ALU Functions

The function performed by the ALU is controlled by DP.R2.ALU.SEL[2:0]+. These rank-two signals are generated from DP.R1.ALU.SEL[2:0]+ by the register located at U0704 (DP103B) which delays them by one microcycle. The rank-one signals are generated by the ALU-SHIFT PLA U0803 (DP112C) along with two related signals. The code for this PLA is listed in Figure 4-8.

DP.R1.SUBT+ indicates that the current operation is one of the six subtracts. DP.R1.UP.CO+ indicates that the current operation is an add or subtract and that the COUT and OVFL conditions should therefore be updated. The TBUS field (BP.UIR.REG[19:16]+) provides the information necessary to generate these signals as shown in Table 4-3.



```
*
*
*                                                    D D D
*                                          B         P P P
*       B B B B B B        B               P         . . .
*       P P P P P P B B    .                   D     R R R
*       . . . . . . P P D N      D     P D 1 1 1
*       U U U U U U . . P O    D P D . P . . .
*       I I I I I I U U . .    P . P R . A A A
*       R R R R R R I I A E    . R . 1 R L L L
*       . . . . . . R R S X    R 1 R . 1 U U U
*       R R R R R R . . G E    1 . 1 U . . . .
*       E E E E E E R R . C    . L . P S S S S
*       G G G G G G E E S U    S S L . U E E E
*       1 1 1 1 1 1 G G P T    R L S C B L L L
*       9 8 7 6 1 0 9 8 2 E    G N L O T 2 1 0
*       + + + + + + + + - -    - - - + + + + +
*
*       0 0 0 0 0 0 0 0 1 0    1 1 1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 6 9    9 8 7 5 4 3 2 1
*
 SENSE:                        H H L L L H H H
*                          B B  B B B B B B B B
*ROW    7 6 5 4 3 2 1 0 6 0    9 8 7 5 4 3 2 1
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    L L L L - - - - - -    A A A A A A . .   TBUS/XOR
   1    L L L H - - - - - -    A A A . . . . A   TBUS/LMR0
   2    L L H L - - - - - -    A A A . . . . A   TBUS/LMR1
   3    L L H H - - - - - -    A A A . . . . A   TBUS/LMRC
   4    L H L L - - - - - -    A A A A A A . A   TBUS/OR
   5    L H L H - - - - - -    A A A . . . A .   TBUS/RML0
   6    L H H L - - - - L -    A A A . A . A .   TBUS/RML1 * ASG
   7    L H H L - - - - H -    A A A . . . A .   TBUS/RML1 * ASG-
   8    L H H H - - - - - -    A A A . . . A .   TBUS/RMLC
   9    H L L L - - - - - -    A A A A A A A .   TBUS/AND
  10    H L L H - - - - - -    A A A . A . A A   TBUS/ADD0
  11    H L H L - - - - - -    A A A . A . A A   TBUS/ADD1
  12    H L H H - - - - - -    A A A . A . A A   TBUS/ADDC
  13    H H L L - - - - - -    A A A A A A A A   TBUS/UBUS
  14    H H L H - - - - - L    A A A A A A A A   TBUS/SRG * NOX
  15    H H L H - - - - - H    . A . A A A A A   TBUS/SRG * NOX-
  16    H H H L - - - - - -    A . . A A A A A   TBUS/LSLN
  17    H H H H - - - - - -    A A A A A A A A   TBUS/LBUS
  18    - - - - L L L H - -    A A A A A . . .   SP0/LSL
*
```

Figure 4-8. ALU-SHIFT PLA (U0803) Code

Table 4-3. TBUS Field vs ALU Add, Subtract, And Select Signals

TBUS	UIR[19:16]+	ALU.SEL[2:0]+	SUBT+	UP.CO+
XOR	0000	100	0	0
LMR0	0001	001	1	1
LMR1	0010	001	1	1
LMRC	0011	001	1	1
OR	0100	101	0	0
RML0	0101	010	1	1
RML1	0110	010	1	1
RML1*ASG	0110	010	0	1
RMLC	0111	010	1	1
AND	1000	110	0	0
ADD0	1001	011	0	1
ADD1	1010	011	0	1
ADDC	1011	011	0	1
UBUS	1100	---	0	0
SRG	1101	---	0	0
LSLN	1110	---	0	0
LBUS	1111	---	0	0

Only the first 12 TBUS operations are actually performed in the ALU. For the remaining four operations, signals DP.R1.UP.CO+ and DP.R1.SUBT+ are both forced "low". This is also true if the SP0 field contains an LSL indicating that a shift should be performed. An SP2/ASG which appears at the same time as a TBUS/RML1 forces DP.R1.SUBT+ "low" rather than "high" as it normally would be. Notice that these two signals are actually generated "low true" and then inverted at the PLA's output. Both signals are delayed by the register located at U0703 (DP114C) to form DP.R2.UP.CO+ and DP.R2.SUBT+.

4.3.6.2 ALU Carry-In

As mentioned above the overall carry-in to the ALU is DP.R2.ALU.CIN0-. This is a version of DP.R1.ALU.CIN0- which has been delayed one microcycle by register U0704 (DP103B). This signal is generated by the E/CIN/COUT PLA U0604 (DP103C). The code for this PLA is listed in Figure 4-9. The CIN signal is being generated in the cycle before it will actually be used. Therefore it must look at the current TBUS field to determine what should be done. For operations that are not arithmetic, CIN is never asserted. For the arithmetic operations which specify carry or borrow, CIN is asserted appropriately. Since the ALU actually does "A minus B" as "A plus (not B) plus CIN", a borrow occurs when CIN is "low". Thus CIN must be asserted for ADD1, LMR0, and RML0.

```
*
*                                 D                 D
*          B                      P                 P
*          P     B B B B     .   D D               .
*          .     P P P P     R   P P D     D       R
*        D N D . . . .     2 . . P D P     1 D
*        P O P U U U U     . R R . P .     . P D
*        . . . I I I I     A 2 2 E . R     A . P
*        R E I R R R R D L . . N A 2     L R .
*        2 X R . . . . P U A A O S .     U 2 E
*        . E . R R R R . . L L E G U     . . .
*        S C R E E E E C C U U . . P     C C E
*        U U E G G G G O I . . S S .     I O N
*        B T G 1 1 1 1 U N P G P P C     N U O
*        T E 2 9 8 7 6 T 3 3 3 1 2 0     0 T E
*        + - + + + + + + - - - - + +     + + -
*
*        0 0 0 0 0 0 0 1 1 1 1 1 1 0     1 1 1
*PIN:    8 7 5 4 3 2 1 6 5 4 3 2 1 9     9 8 7
*
 SENSE:                                  H H L
*                           B B B B B B B   B B B
*ROW     7 6 4 3 2 1 0 6 5 4 3 2 1 0     9 8 7
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0     - - - H L H L - - - - - - -     A . .   ADD1
   1     - - - H L H H H - - - - - L     A . .   ADDC*UPCO-
   2     L - - H L H H - - - L - - H     A . .   ADDC*UPCO+*SUBT-
   3     L - - H L H H - H L - - - H     A . .   ADDC*UPCO+*SUBT-
   4     H - - H L H H - - H H - - H     A . .   ADDC*UPCO+*SUBT+
   5     H - - H L H H - L - H - - H     A . .   ADDC*UPCO+*SUBT+
   6     - - - L - L H - - - - - - -     A . .   LMR0,RML0
   7     - - - L - H H L - - - - - L     A . .   LMRC,RMLC*UPCO-
   8     L - - L - H H - - H H - - H     A . .   LMRC,RMLC*UPCO-*SUBT-
   9     L - - L - H H - L - H - - H     A . .   LMRC,RMLC*UPCO-*SUBT-
  10     H - - L - H H - - - L - - H     A . .   LMRC,RMLC*UPCO-*SUBT+
  11     H - - L - H H - H L - - - H     A . .   LMRC,RMLC*UPCO-*SUBT+
  12     - - H - - - - - - - - - L -     A . .   ASG
  13     - - - - - - - H - - - - - L     . A .   UPCO-
  14     L - - - - - - - - - - L - - H   . A .   UPCO+*SUBT-
  15     L - - - - - - - H L - - - H     . A .   UPCO+*SUBT-
  16     H - - - - - - - - - H H - - H   . A .   UPCO+*SUBT+
  17     H - - - - - - - L - H - - H     . A .   UPCO+*SUBT+
  18     L H - - - - - - - - - L L - H   . . A   UPCO+*SUBT-
  19     L H - - - - - - H L - L - H     . . A   UPCO+*SUBT-
  20     H H - - - - - - - - H H L - H   . . A   UPCO+*SUBT+
  21     H H - - - - - - L - H L - H     . . A   UPCO+*SUBT+
*
```

Figure 4-9. E/CIN/COUT PLA (U0604) Code

For three of the remaining arithmetic operations (ADDC, LMRC, and RMLC), CIN is based on the value of COUT in the cycle in which the ALU operation is actually occurring when DP.R2.UP.CO+ is "low":

a. When COUT is not being updated in the current cycle the value of COUT (DP.COUT+) can be used directly.

b. For ADDC, COUT is sent directly to CIN.

c. For LMRC and RMLC, its inverse is sent to CIN.

However, if DP.R2.UP.CO+ is "high", CNDX/COUT AND CNDXOVFL are both updated at the end current cycle. The value used to update COUT (described in the next paragraph) must also generate CIN:

a. Normally an add will follow an add or a subtract will follow a subtract so that the current carry-out can go directly to CIN.

b. If add follows subtract or subtract follows add, the sense of carry must be reversed.

4.3.6.3 ALU Carry-Out

The COUT condition (DP.COUT+) is held in the register which is located at U0704 (DP103B). It is updated at the end of each cycle with the value from DP.R2.COUT+ which is generated by the E/CIN/COUT PLA located at U0604 (DP103C). This is the same PLA used to generate CIN to the ALU. Its code is listed in Figure 4-9, above. COUT is updated based on the carry-out from the ALU. This value is not directly available, but must be generated from the CIN to the high-order ALU slice (DP.R2.ALU.CIN3+) and the GENERATE and PROPAGATE outputs from that slice (DP.R2.ALU.G3- and DP.R2.ALU.P3-) as follows:

```
        CARRY-OUT = GENERATE + (PROPAGATE * CIN)
                    or using Demorgan
not CARRY-OUT = (not GENERATE * not PROPAGATE) +
                (not GENERATE * not CIN)
```

The following COUT updates may occur in the current operation:

a. If the current operation is an add, DP.R2.SUBT+ will be "low" and COUT is updated with carry-out.

b. If the current operation is a subtract, DP.R2.SUBT+ will be "high" and COUT is updated with no carry-out.

c. If the current operation is not arithmetic, DP.R2.UP.CO+ will be "low", and COUT is updated with its current value.

4.3.6.4 Overflow Condition

The OVFL condition (DP.OVFL+) is also held in register U0704 (DP103B). It is updated at the end of each cycle with the value from DP.R2.OVFL+ which is generated by the O/OVFL PLA U0504 (DP105D). The code for this PLA is is listed in Figure 4-10.

```
*           D D
*         B P P
*         P . .                 D
*         . R R     D D         P
*       D N 2 2     P P D D . D   D
*       P O . .     . . P P A P   P
*       . . A A     R E . . L .   .
*       L E L L D   2 N S C U R   R D
*       . X U U P   . O T L . .   2 P
*       B E . . .   U E O O O B   . .
*       U C S S O D P . . . U U   O O
*       S U E E V P . S S S T S   V .
*       1 T L L F . C P P P 1 1   F I
*       5 E 1 0 L O O 1 1 1 5 5   L N
*       + - + + + + + - - - + +   + +
*
*       0 0 0 0 0 0 0 0 1 1 1 0   1 1
*PIN:   8 7 6 5 4 3 2 1 3 2 1 9   9 8
*
 SENSE:                           H H
*                         B B B B   B B
*ROW    7 6 5 4 3 2 1 0 3 2 1 0   9 8
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - H - L - - - - -   A .   UPCO-
   1    H - H H - - H - - - L H   A .   ADD
   2    L - H H - - H - - - H L   A .   ADD
   3    L - H L - - H - - - L H   A .   RML
   4    H - H L - - H - - - H L   A .   RML
   5    H - L H - - H - - - L L   A .   LMR
   6    L - L H - - H - - - H H   A .   LMR
   7    - L - - - H - - - - - -   . A   NOX
   8    - H - - - H - - - H - -   . A   CLO-
   9    - H - - - - - - L - - -   . A   STO+
  10    H H H H - - H L - - L H   . A   ADD
  11    L H H H - - H L - - H L   . A   ADD
  12    L H H L - - H L - - L H   . A   RML
  13    H H H L - - H L - - H L   . A   RML
  14    H H L H - - H L - - L L   . A   LMR
  15    L H L H - - H L - - H H   . A   LMR
*
```

Figure 4-10. O/OVFL PLA (U0504) Code

The PLA looks at the sign of both ALU inputs (DP.L.BUS15+ and DP.R.BUS15+) and the sign of the ALU output (DP.ALU.OUT15+) to determine if an overflow has occurred. For an add operation, an overflow occurs when the two inputs have the same sign and the output has the opposite sign. To determine when an overflow has occurred for a subtract operation, it is useful to break the operation (A minus B minus BORROW) into two separate components.

First complement B which yields "minus B minus 1" and then add in "A plus (not BORROW)". This gives "A minus B minus 1 plus (not BORROW)". It can be shown that these operation are the same. The first half of the operation (not B) cannot overflow. The second half is an add so the overflow rules from above apply. Thus, to determine overflow for a subtract, complement the sign of the input being subtracted. Then apply the overflow rules for addition:

When DP.R2.UP.CO+ is high the PLA uses this algorithm for updating OVFL. It uses the lower two bits of the ALU function select (DP.R2.ALU.SEL[1:0]+) to determine which input sign should be inverted if the operation is a subtract. When DP.R2.UP.CO+ is low OVFL is simply updated with its current value.

4.3.7 Barrel-Shifter

The barrel-shifter is made up of a large 12-bit shift section and a small 3-bit shift section. The 12-bit shifter is shown on schematic sheet DP6. It is composed of four shifter slices, U1102 (DP62C), U1503 (DP63C), U1203 (DP65C), and U1303 (DP66C), and multiplexers U1602 (DP62E), and U1302 (DP64E). The shifter slices take values from DP.L.BUS[15:0]+ and DP.R.BUS[15:4]+ and shift them left by 0, 4, 8, or 12 places to form the left (upper) 16 bits of the intermediate result known as DP.SH.MIDL[15:0]+.

Since the 12-bit shifter can shift up to three positions, it needs an additional three bits to work with. These right (lower) 3-bits of the intermediate result, known as DP.SH.MIDR[15:13]+, are produced from DP.R.BUS[15:1]+ by the two MUXs. The number of bits shifted is controlled by DP.SH.TX.SEL[3:2]+ as shown in Table 4-4.

Table 4-4. Number of Bits Shifted By 12-bit Shifter

DP.SH.TX. SEL[3:2]+	Shift	DP.SH.MIDL15+ Gets	DP.SH.MIDR13+ Gets
0 0	Pass	DP.L.BUS15+	DP.R.BUS13+
0 1	Left 4	DP.L.BUS11+	DP.R.BUS9+
1 0	Left 8	DP.L.BUS7+	DP.R.BUS5+
1 1	Left 12	DP.L.BUS3+	DP.R.BUS1+

The 3-bit shifter is shown on schematic sheet DP7. It is composed of four shifter slices, U1402 (DP72B), U1403 (DP74B), U1103 (DP75B), and DP1003 (DP77B), and of two 8:1 multiplexers, U0903 (DP72D) and U1202 (DP72E). The shifter slices and MUXs all have tristate outputs which are enabled when DP.R2.SH.EN- is "low". When they are enabled, the shifter slices drive BP.T.BUS[14:1]+ with the intermediate result from the large shifter (DP.SH.MIDL[14:0]+ and DP.SH.MIDR[15:14]+) shifted left by 0, 1, 2, or 3 places. The number of bits shifted is controlled by DP.SH.TX.SEL[1:0]+ as shown in Table 4-5

Table 4-5. Number of Bits Shifted By 3-Bit Shifter

DP.SH.TX. SEL[1:0]+	Function	BP.T.BUS14+ gets	BP.T.BUS1+ gets
0 0	Pass	DP.SH.MIDL14+	DP.SH.MIDL1+
0 1	Left 1	DP.SH.MIDL13+	DP.SH.MIDL0+
1 0	Left 2	DP.SH.MIDL12+	DP.SH.MIDR15+
1 1	Left 3	DP.SH.MIDL11+	DP.SH.MIDR14+

4.3.7.1 SRG Shift Sources

When it is enabled, the lower MUX drives BP.T.BUS0+. It can act as an extension of the main part of the 3-bit shifter and shift the intermediate result by 0 to 3 places. To implement SRG shifts it can also select the E-Register or a constant of "0" as sources. The signal which is selected is controlled by DP.SH.T0.SEL[2:0]+ as indicated in Table 4-6.

Table 4-6. SRG Source Selection by Lower MUX

DP.SH.T0. SEL[2:0]+	Function	BP.T.BUS0+ gets
0 0 0	Pass	DP.SH.MIDL0+
0 0 1	Left 1	DP.SH.MIDR15+
0 1 0	Left 2	DP.SH.MIDR14+
0 1 1	Left 3	DP.SH.MIDR13+
1 0 0	-	-
1 0 1	E	DP.E+
1 1 0	-	-
1 1 1	Zero	DP.GND+

When it is enabled, the upper MUX drives BP.T.BUS15+. It can act as an extension of the main part of the 3-bit shifter and shift the intermediate result by 0 to 3 places. To implement SRG shifts it can also select the E-Register, the sign of LREG, or a constant of 0 as sources. The signal selection is controlled by DP.SH.T15.SEL[2:0]+ as shown in Table 4-7.

Table 4-7. SRG Source Selection By Upper MUX

DP.SH.T15. SEL[2:0]+	Function	BP.T.BUS15+ gets
0 0 0	Pass	DP.SH.MIDL15+
0 0 1	Left 1	DP.SH.MIDL14+
0 1 0	Left 2	DP.SH.MIDL13+
0 1 1	Left 3	DP.SH.MIDL12+
1 0 0	L15	DP.L.BUS15+
1 0 1	E	DP.E+
1 1 0	-	-
1 1 1	Zero	DP.GND+

4.3.7.2 SRG Control

When the effect of the 12-bit shifter and 3-bit shifter are combined, a left shift of 0 to 15 places can be performed. All eight SRG shifts can also be performed by controlling the upper and lower output bits specially, and placing the value to be shifted on both LBUS and RBUS. The control values needed for each of these 24 shifts are shown in Table 4-8.

Table 4-8. Control Values for 24-Shifts Of Barrel-Shifter

Shift Type	DP.SH.T15. SEL[2:0]+	DP.SH.T0. SEL[2:0]+	DP.SH.TX. SEL[3:0]+	SRG1: 9876 SRG2: 4210
Pass	0 0 0	0 0 0	0 0 0 0	
Left 1	0 0 1	0 0 1	0 0 0 1	
Left 2	0 1 0	0 1 0	0 0 1 0	
Left 3	0 1 1	0 1 1	0 0 1 1	
Left 4	0 0 0	0 0 0	0 1 0 0	
Left 5	0 0 1	0 0 1	0 1 0 1	
Left 6	0 1 0	0 1 0	0 1 1 0	
Left 7	0 1 1	0 1 1	0 1 1 1	
Left 8	0 0 0	0 0 0	1 0 0 0	
Left 9	0 0 1	0 0 1	1 0 0 1	
Left 10	0 1 0	0 1 0	1 0 1 0	
Left 11	0 1 1	0 1 1	1 0 1 1	
Left 12	0 0 0	0 0 0	1 1 0 0	
Left 13	0 0 1	0 0 1	1 1 0 1	
Left 14	0 1 0	0 1 0	1 1 1 0	
Left 15	0 1 1	0 1 1	1 1 1 1	
SRG NOP	0 0 0	0 0 0	0 0 0 0	0---
SRG *LS	1 0 0	1 1 1	0 0 0 1	1000
SRG *RS	1 0 0	0 1 1	1 1 1 1	1001
SRG R*L	0 0 1	0 0 1	0 0 0 1	1010
SRG R*R	0 1 1	0 1 1	1 1 1 1	1011
SRG *LR	1 1 1	1 1 1	0 0 0 1	1100
SRG ER*	1 0 1	0 1 1	1 1 1 1	1101
SRG EL*	0 0 1	1 0 1	0 0 0 1	1110
SRG *LF	0 0 0	0 0 0	0 1 0 0	1111
SRG.SEL	7 6 5	4 3 0	1 2 1 0	

All of the control bits except DP.SH.T15.SEL2+ and DP.SH.T0.SEL2+ can be driven from LSL register U0702 (DP117B), or LSLN register U0602 (DP27B), or the SRG register U0603 (DP114B). The inverting LSL register is loaded from a delayed rank-one version of the TBUS field (DP.F1.UIR.REG[19:16]+) at the end of each microcycle. It is enabled in the cycle after an SP0/LSL or TBUS/LBUS occurs, and causes the shifter to shift left by the number of places indicated by the inverse of the value in the preceding TBUS field.

The LSLN register is loaded from the lower bits of IR (DP.IR.REG[3:0]+) at the end of each microcycle. It is enabled in the cycle after a TBUS/LSLN occurs and causes the shifter to shift left by the number of places indicated by the lower bits of IR in the preceding cycle.

During a cycle which includes a TBUS/SRG, the SRG-control PLA U0503 (DP113B) produces eight control signals known as DP.SRG.SEL[7:0]+. The code for this PLA is listed in Figure 4-11. Two of the signals (DP.SRG.SEL7+ and DP.SRG.SEL4+) are clocked into the register located at DP0703 (DP114C) at the end of each microcycle. This converts them to DP.SH.T15.SEL2+ and DP.SH.T0.SEL2+.

The SRG-control PLA guarantees that these two signals remain "low" unless the TBUS/SRG order appears. The remaining outputs are clocked into the SRG register at the end of each microcycle. The SRG register is enabled in the cycle after the TBUS/SRG order occurs and causes the shifter to perform the shift which was decided on by the SRG-control PLA in the preceding cycle.

The SRG-control PLA uses DP.R1.SRG- to determine that the SRG microorder has occurred. The DP.SRG1.SP2- signal is used to determine if the first (SRG1) or second (SRG2) shift of an SRG instruction is being executed. If DP.SRG1.SP2- is "low" (SRG1), the PLA uses DP.IR.REG[9:6]+ to determine DP.SRG.SEL[7:0]+. If DP.SRG1.SP2- is "low" (SRG2), the PLA uses DP.IR.REG4+ and DP.IR.REG[2:0]+ to determine DP.SRG.SEL[7:0]+.

Table 4-8 above indicates which SRG.SEL signal drives each of the shifter control lines. Notice that several of the control signals have identical values for all of the SRG shifts. This allows only eight SRG.SEL signals to control ten-shifter control lines.

The ALU-Shift PLA U0803 (DP112C) controls the enabled register of the three registers (LSL, LSLN, or SRG) to drive the shifter control signals. The code for the PLA is listed in Figure 4-8 above. The PLA looks at the SP0 field (BP.UIR.REG[11:8]+) and the TBUS field (BP.UIR.REG[19:16]+) to determine which type of shift should be used:

a. DP.R1.SRG- goes "low" if BP.NO.EXECUTE- is deasserted (high) and TBUS/SRG appears without SP0/LSL.

b. DP.R1.LSLN- goes "low" if TBUS/LSLN appears without SP0/LSL.

c. DP.R1.LSL- goes "low" in all other cases including TBUS/LBUS and SP0/LSL.

Notice that the first two signals are generated in their "low true" form while the third signal is generated "high true" and then inverted by the PLA output stage. These three signals are delayed by the register located at U0703 (DP114C) to form DP.R2.SRG-, DP.R2.LSLN-, and DP.R2.LSL- which are used to actually enable the SRG, LSLN, and LSL registers.

```
*
*
*
*                                  B   D D D D D D D D
*       D D D D D D D D            P   P P P P P P P P
*       P P P P P P P P D .            . . . . . . . .
*       . . . . . . . . P S            S S S S S S S S
*       I I I I I I I I . R            R R R R R R R R
*       R R R R R R R R R G            G G G G G G G G
*       . . . . . . . . 1 1            . . . . . . . .
*       R R R R R R R R . .            S S S S S S S S
*       E E E E E E E E S S            E E E E E E E E
*       G G G G G G G G R P            L L L L L L L L
*       9 8 7 6 4 2 1 0 G 2            7 6 5 4 3 2 1 0
*       + + + + + + + + - -            + + + + + + + +
*
*       0 0 0 0 0 0 0 0 1 0            1 1 1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 1 9            9 8 7 6 5 4 3 2
*
 SENSE:                                H H H H H H H H
*                                  B B   B B B B B B B B
*ROW    7 6 5 4 3 2 1 0 1 0            9 8 7 6 5 4 3 2
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    H L L L - - - - L L   A . . A A . . A   SRG1 *LS
   1    H L L H - - - - L L   A . . . A A A A   SRG1 *RS
   2    H L H L - - - - L L   . . A . . . . A   SRG1 R*L
   3    H L H H - - - - L L   . A A . A A A A   SRG1 R*R
   4    H H L L - - - - L L   A A A A A . . A   SRG1 *LR
   5    H H L H - - - - L L   A . A . A A A A   SRG1 ER*
   6    H H H L - - - - L L   . . A A . . . A   SRG1 EL*
   7    H H H H - - - - L L   . . . . . A . .   SRG1 *LF
   8    - - - - H L L L L H   A . . A A . . A   SRG2 *LS
   9    - - - - H L L H L H   A . . . A A A A   SRG2 *RS
  10    - - - - H L H L L H   . . A . . . . A   SRG2 R*L
  11    - - - - H L H H L H   . A A . A A A A   SRG2 R*R
  12    - - - - H H L L L H   A A A A A . . A   SRG2 *LR
  13    - - - - H H L H L H   A . A . A A A A   SRG2 ER*
  14    - - - - H H H L L H   . . A A . . . A   SRG2 EL*
  15    - - - - H H H H L H   . . . . . A . .   SRG2 *LF
*
*
```

Figure 4-11. SRG Control PLA U0503 Code

4.3.8 Floating-Point Chips

The three floating-point chips are shown on schematic sheet DP4:

a. The FAS function is implemented by the 1AE7 located at U0905 (DP42C).

b. The FMPY function is implemented by the 1AH4 located at U0807 (DP45C).

c. The FDIV function is implemented by the 1AH7 located at U1106 (DP47C).

These three chips are connected in a very similar manner. The FAS chip is described here, but the same description applies to the other two chips by substituting either FMPY or FDIV for FAS.

The A-inputs of the chip are connected to DP.L.BUS[15:0]+ and the B-inputs are connected to DP.R.BUS[15:0]+. The chip's D-outputs drive DP.D.BUS[15:0]+ when DP.FAS.LREG- is "low". At the same time its ERR output drives DP.FERR+. This signal is loaded into the register located at U0307 (DP82C) at the end of each microcycle to become CNDX/FERR.

The chip's four F-inputs control the operation it performs. They are driven by DP.R2.UIR.REG[19:16]+, a version of the TBUS field which has been delayed by the register located at U0605 (DP43E). The chip's "low true" clear input is driven by DP.FCLR.SP1-. This signal goes "low" during cycles that include SP1/FCLR. The clock for the chip is produced by a gate located at U0505 (DP45D). It clocks the chip during a microcycle in which DP.FAS.SP2- is "low" indicating that a SP2/FAS is present.

The chips are clocked before the end of the cycle to avoid a hold time problem with the data at their inputs. This is done using a delayed version of the microcycle clock which has a rising edge about 30 ns after the middle of the microcycle (CK.CPU3.D30.BF-). Note that the chips actually need a falling-edge clock so this clock is inverted by the gates at U0505 (DP45D).

Because the chips are clocked early, their outputs change before the end of the cycle. However, a register is placed between the chip outputs and LREG consisting of U0705 (DP49B) and U0806 (DP49C). This register is clocked at the same time as the chips so that it catches the current chip outputs and holds them until the end of the microcycle when they can be transferred to LREG. Note that the FERR condition is not delayed in this manner, but its value never changes during a cycle in which the chips are unloaded.

4.3.9 TBUS and UBUS

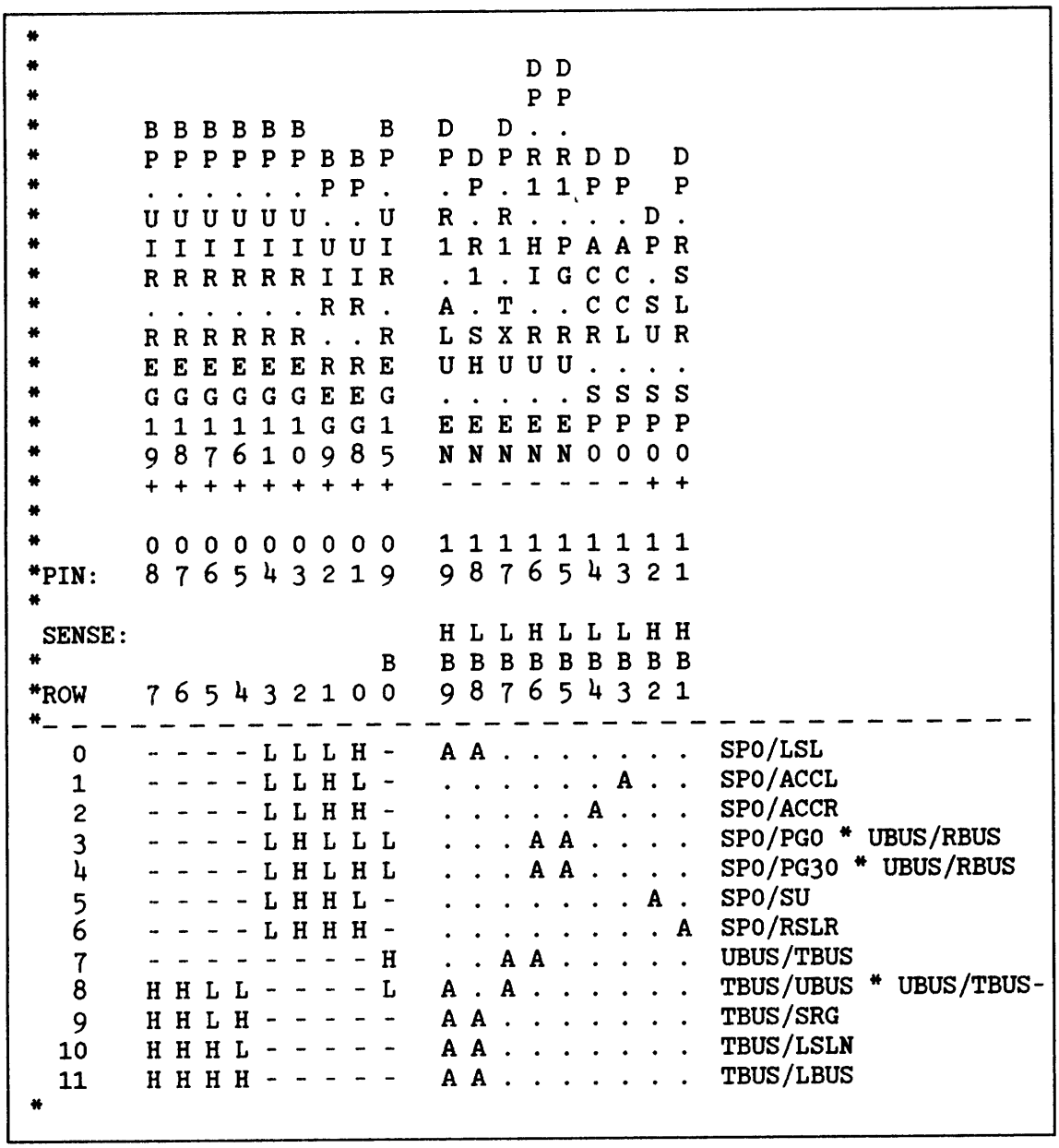
The TBUS can be driven by the ALU buffer or by the shifter. It can also be driven by the TXU buffer. This buffer consists of bidirectional buffers U0901 (DP75C) and U1101 (DP75D). When DP.R2.TXU.EN- is "low" the TXU buffer links the TBUS and UBUS. If DP.R2.UIR.REG15+ (the rank-2 version of the UBUS field) is "low", BP.T.BUS[15:0]+ is driven from DP.U.BUS[15:0]+. If DP.R2.UIR.REG15+ is "high", DP.U.BUS[15:0]+ will be driven from BP.T.BUS[15:0]+. The UBUS can also be driven by the RBUS buffer. This buffer is composed of DP1201 (DP64B) and U1301 (DP65B).

When DP.R2.UIR.REG15+ is low, DP.U.BUS[7:0]+ is driven from DP.R.BUS[7:0]+. When DP.R2.HI.RU.EN- is low, DP.U.BUS[15:8]+ is driven from DP.R.BUS[15:8]+. It is also possible to force the upper six bits of the UBUS to point to "page 0" or "page 30". This is done using the PG buffer U0801 (DP62B). When DP.R2.PG.RU.EN- is "low", DP.U.BUS[9:8]+ is driven from DP.R.BUS[9:8]+ and DP.U.BUS[15:10]+ is driven with a constant. If BP.R2.UIR.REG8+ is "low" the constant is 000000, and if it is "high" the constant will be 011110 binary.

The TBUS-UBUS PLA, located at U0802 (DP112E), controls the sources which drive the TBUS and UBUS. The code for this PLA is is listed in Figure 4-12. The PLA looks at the TBUS field (BP.UIR.REG[19:16]+), the UBUS field (BP.UIR.REG15+), and the SP0 field (BP.UIR.REG[11:8]+). It causes DP.R1.SH.EN- to go "low" when TBUS/LSL, TBUS/LBUS, TBUS/SRG, or SP0/LSL are present. DP.R1.TXU.EN- goes "low" when TBUS/UBUS is present. DP.R1.ALU.EN- goes "low" in all other cases. These three rank-one signals are converted to rank-two by register U0902 (DP114E). The rank-two versions (DP.R2.SH.EN-, DP.R2.TXU.EN-, and DP.R2.ALU.EN-) enable one of the three sources to drive the TBUS.

The DP.R1.TXU.EN- signal also goes "low" when UBUS/TBUS occurs. In this case the presence of UBUS/TBUS (BP.UIR.REG15+ "high") causes TXU to drive the UBUS instead of the TBUS. (Notice that if TBUS/UBUS and UBUS/TBUS both occur at the same time, the TBUS is driven by the ALU.)

The presence of UBUS/RBUS (BP.UIR.REG15+ low), indicates that the lower half of the RBUS buffer should be enabled. DP.R1.HI.RU.EN- goes "low" if UBUS/RBUS occurs unmodified. DP.R1.PG.RU.EN- goes "low" if UBUS/RBUS occurs along with SP0/PG0 or SP0/PG30. In this case, the lower bit of the SP0 field (BP.UIR.REG8+) indicates which constant value should be used. All of these rank-one signals are converted to their rank-two counterparts by the register located at U0902 (DP114E). The rank-two signals (DP.R2.UIR.REG8+, DP.R2.UIR.REG15+, DP.R2.R2.HI.RU.EN-, and DP.R2.PG.RU.EN-) are used to control the driving of the UBUS as described above.



```
*
*                                          D D
*                                          P P
*       B B B B B B     B   D   D . .
*       P P P P P P B B P   P D P R R D D   D
*       . . . . . . P P .   . P . 1 1 P P   P
*       U U U U U U . . U   R . R . . . . D .
*       I I I I I I U U I   1 R 1 H P A A P R
*       R R R R R R I I R   . 1 . I G C C . S
*       . . . . . . R R .   A . T . . C C S L
*       R R R R R R . . R   L S X R R R L U R
*       E E E E E E R R E   U H U U U . . . .
*       G G G G G G E E G   . . . . . S S S S
*       1 1 1 1 1 1 G G 1   E E E E E P P P P
*       9 8 7 6 1 0 9 8 5   N N N N N 0 0 0 0
*       + + + + + + + + +   - - - - - - - + +
*
*       0 0 0 0 0 0 0 0 0   1 1 1 1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 9   9 8 7 6 5 4 3 2 1
*
 SENSE:                     H L L H L L L H H
*                       B   B B B B B B B B B
*ROW    7 6 5 4 3 2 1 0 0   9 8 7 6 5 4 3 2 1
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - L L L H -   A A . . . . . . .  SP0/LSL
   1    - - - - L L H L -   . . . . . . A . .  SP0/ACCL
   2    - - - - L L H H -   . . . . . A . . .  SP0/ACCR
   3    - - - - L H L L L   . . . A A . . . .  SP0/PG0 * UBUS/RBUS
   4    - - - - L H L H L   . . . A A . . . .  SP0/PG30 * UBUS/RBUS
   5    - - - - L H H L -   . . . . . . . A .  SP0/SU
   6    - - - - L H H H -   . . . . . . . . A  SP0/RSLR
   7    - - - - - - - - H   . . A A . . . . .  UBUS/TBUS
   8    H H L L - - - - L   A . A . . . . . .  TBUS/UBUS * UBUS/TBUS-
   9    H H L H - - - - -   A A . . . . . . .  TBUS/SRG
  10    H H H L - - - - -   A A . . . . . . .  TBUS/LSLN
  11    H H H H - - - - -   A A . . . . . . .  TBUS/LBUS
*
```

Figure 4-12. TBUS-UBUS PLA (U0802) Code

4.3.10 TBUS Status

The TBUS Status logic is shown in the upper-left corner of schematic sheet DP8. It centers around two PLAs U0401 (DP82A) and U0402 (DP82B). Both PLAs are programmed identically as listed in Figure 4-13.

The upper PLA receives BP.T.BUS[15:8]+ and produces four outputs. DP.TU8.ON- goes "low" if all 8-bits are "high". If all 8-bits are "low" DP.TU8Z- goes "low" and DP.TU8Z+ goes "high". DP.TU6Z+ goes "high" if the upper 6-bits are all "low".

The lower PLA receives BP.T.BUS[9:0]+ and produces four outputs. DP.TL8.ON- goes "low" if the lower 8-bits are all "high". If the lower 8-bits are "low" DP.TL8Z- goes "low" and DP.TL8Z+ goes "high". DP.TLTZ+ goes "high" if all 10-bits are "low". Certain PLA outputs are used directly to generate the TU8Z, TU6Z, TLTZ, and TL8Z status conditions. Three gates U0204 (DP84A) and U0302 (DP84A) combine other PLA outputs to form the TON, TZ, and TULZ status conditions. All seven TBUS status conditions are clocked into the register U0202 (DP85B) for use by the condition circuitry in the following cycle.

The TBUS status outputs are buffered by U0202 (DP85A), stored in the status register U0208 (DP84C) and multiplexed in U0102, U0108, U0207 (DP87A/C/D) and U0107 (DP88D) to generate CNDX.MET+.

```
*
*
*       B B B B B B     B B
*       P P P P P P B B P P   D
*       . . . . . . P P . .   P
*       T T T T T T . . T T   . D D
*       . . . . . . T T . .   T P P
*       B B B B B B . . B B   L . . D D
*       U U U U U U B B U U   / T T P P
*       S S S S S S U U S S   U L L . .
*       7 6 5 4 3 2 S S 9 8   8 / / T T
*       / / / / / / 1 0 / /   . U U U L
*       1 1 1 1 1 1 / / - -   0 8 8 6 T
*       5 4 3 2 1 0 9 8 - -   N Z Z Z Z
*       + + + + + + + + + +   - - + + +
*
*       0 0 0 0 0 0 0 0 1 0   1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 1 9   8 7 6 5 4
*
 SENSE:                       L L H H H
*                         B B   B B B B B
*ROW    7 6 5 4 3 2 1 0 1 0   8 7 6 5 4
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    L L L L L L L L L L   . . . . A   10 ZERO
   1    L L L L L L - - - -   . . . A .    6 ZERO
   2    L L L L L L L L - -   . A A . .    8 ZERO
   3    H H H H H H H H - -   A . . . .    8 ONES
*
```

Figure 4-13. TBUS-Status PLAs (U0401, U0402) Code

4.3.11 Flags, "E" and "O"

4.3.11.1 Flag-STOR PLA

The F1 flag (DP.F1+) is stored in the register U0404 (DP123B). At the end of every microcycle it is loaded with the value of DP.F1.IN+ which is generated by the Flags-STOR PLA U0304 (DP123C). The PLA looks at the OP and SP1 fields as well as the BP.CNDX.MET+ and BP.JTAB.MEM- signals. The code for Flags-STOR PLA is listed in Figure 4-14.

The flag is always cleared if BP.JTAB.MEM- is "low" indicating that a MEM/JTAB of MEM/JTDI is present. The flag is also controlled by three specials in the SP1 field (CLF1, CMF1, and STF1). These specials are always executed if the OP field contains RTNC. If the OP field contains SP1C, the specials will only be executed if BP.CNDX.MET+ is "high". The PLA causes the flag to be set if a STF1 occurs or if the flag is clear and a CMF1 occurs. Notice that each of these situations requires two PLA terms to handle both the RTNC and SP1C cases.

If the flag is already "high", it is allowed to remain "high" if the SP1 field does not contain a CMF1 or CLF1. or if the OP field does not contain RTNC or SP1C, or if the OP field contains SP1C and BP.CNDX.MET+ is "low" indicating that the SP1 field should not be executed. This combination of conditions requires six terms in the PLA. The F2 flag (DP.F2+) is very similar. It is stored in the same register, and updated from DP.F2.IN+ which is generated by the same PLA. The internal function is different only in that it uses the CLF2, CMF2, and STF2 specials.

4.3.11.2 E(SRG-ASG) PLA

The E-Register (DP.E+), which is stored in the register located at U0408 (DP103B), is one of the most versatile (read: difficult to implement) on the DP card. It requires two PLAs to generate the next value for "E". The outputs of these two PLAs (DP.E.ASG.SRG- and DP.E.ENOE-) are "ORed" together by the gate located at U0707 to form DP.E.IN+ which is loaded into "E" at the end of each microcycle. The E(SRG-ASG) PLA U0708 (DP103E) generates DP.E.SRG.ASG-. The code for this PLA is listed in Figure 4-15.

```
*                                                                   D
*                                                 B                 P
*           B B B                                 P                 .
*         B P P P B B B B .       B               .       D D       R
*         P . . . P P P P N       P               .     D P P       1
*         . U U U . . . . O       .               .     P P .       .
*         C I I I U U U U .       J   D D . . .   S     S C T       S
*         N R R R I I I I E       T   P P S C T   T     T L O       T
*         D . . . R R R R X       A   . . T L O   O     O O R       O
*         X R R R . . . . E D D B   F F O O R   R     R R E       R
*         . E E E R R R R C P P .   2 1 . . E   E     E S S .       E
*         M G G G E E E E U . . M   . . S S .   .     . P P E       .
*         E 4 4 4 G G G G T F F E   I I P P E   E     E 1 1 N       E
*         T 6 5 4 7 6 5 4 E 2 1 M   N N 1 1 N   N     N - - -       N
*         + + + + + + + + - + + -   + + - - -   -     - - - -       -
*         0 0 0 0 0 0 0 0 1 1 1 0   1 1 1 1 1   1     1 1 1 1       1
*PIN:     8 7 6 5 4 3 2 1 3 2 1 9   9 8 7 6 5   4     3 2 1 0       0
 SENSE:                             H H L L L   L     L L L L       L
*                                   B B B B B   B     B B B B       B
*ROW      7 6 5 4 3 2 1 0 3 2 1 0   9 8 7 6 5   4     3 2 1 0       0
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    H H H L L H H H H - - -   . . . . A   A     A A A A       A   STOR*SP1C*MET
   1    - - - - - - - - L H - -   . . . . A   A     A A A A       A   STOR-
   2    - - - - - - - L - H - -   . . . . A   A     A A A A       A   STOR-
   3    - - - - - - L - - H - -   . . . . A   A     A A A A       A   STOR-
   4    - - - - - H - - - H - -   . . . . A   A     A A A A       A   STOR-
   5    - - - - H - - - - H - -   . . . . A   A     A A A A       A   SP1C-
   6    - - - L - - - - - H - -   . . . . A   A     A A A A       A   SP1C-
   7    - - L - - - - - - H - -   . . . . A   A     A A A A       A   SP1C-
   8    - - L H L H H L L - - - -   . . . A .   .     . . . .       .   CLO*RTNC
   9    H H H L H H L L - - - -   . . . A .   .     . . . .       .   CLO*SP1C*MET
  10    - - L H L H L L L - - - -   . . A . .   .     . . . .       .   STO*RTNC
  11    H H H L H L L L - - - -   . . A . .   .     . . . .       .   STO*SP1C*MET
  12    - - L H L H L L H - - - H   . A . . .   .     . . . .       .   STF1*RTNC
  13    H H H L H L L L H - - - H   . A . . .   .     . . . .       .   STF1*SP1C*MET
  14    - - L H L H L H H - - L H   . A . . .   .     . . . .       .   CMF1*RTNC
  15    H H H L H L H H - - L H   . A . . .   .     . . . .       .   CMF1*SP1C*MET
  16    - - - - - - - L - - - H H   . A . . .   .     . . . .       .   (CMF1+CLF1)-
  17    - - - - - - H - - - - H H   . A . . .   .     . . . .       .   (CMF1+CLF1)-
  18    - - - - - L - - - - - - H H   . A . . .   .     . . . .       .   (CMF1+CLF1)-
  19    - - - H - - - - - - - H H   . A . . .   .     . . . .       .   (SP1C+RTNC)-
  20    - - L - - - - - - - - H H   . A . . .   .     . . . .       .   (SP1C+RTNC)-
  21    L H - - - - - - - - - H H   . A . . .   .     . . . .       .   SP1C*MET-
  22    - L H L H H L H - - - H   A . . . .   .     . . . .       .   STF2*RTNC
  23    H H H L H H L H - - - H   A . . . .   .     . . . .       .   STF2*SP1C*MET
  24    - L H L H H H H - L - H   A . . . .   .     . . . .       .   CMF2*RTNC
  25    H H H L H H H H - L - H   A . . . .   .     . . . .       .   CMF2*SP1C*MET
  26    - - - - - - - L - - H - H   A . . . .   .     . . . .       .   (CMF2+CLF2)-
  27    - - - - - - L - - - H - H   A . . . .   .     . . . .       .   (CMF2+CLF2)-
  28    - - - - - L - - - - H - H   A . . . .   .     . . . .       .   (CMF2+CLF2)-
  29    - - - H - - - - - - H - H   A . . . .   .     . . . .       .   (SP1C+RTNC)-
  30    - - L - - - - - - - H - H   A . . . .   .     . . . .       .   (SP1C+RTNC)-
  31    L H - - - - - - - - H - H   A . . . .   .     . . . .       .   SP1C*MET-
```

Figure 4-14. Flags-STOR PLA (U0304) Code

```
*
*
*                                                  D
*        B                                         P
*        P                                         .    D
*        .                                         R    P
*        N D D D D D D D D D D    D                2    .
*        O P P P P P P P P P P    P  D  D  .       E
*        . . . . . . . . . . .    .  P  P  S       .
*        E I I I I I I I S C A    L  .  .  R       A
*        X R R R R R R R T L S    .  L  R  G       S
*        E . . . . . . . E E G    B  .  2  1       G
*        C R R R R R R R . . .    D  U  B  .  .     .
*        U E E E E E E E S S S    P  S  U  S  S     S
*        T G G G G G G G P P P    .  1  S  R  P     R
*        E 8 7 6 5 2 1 0 1 1 2    E  5  0  G  2     G
*        - + + + + + + + - - -    +  +  +  -  -     -
*
*        0 0 0 0 0 0 0 0 1 1 1    1  1  1  1  1  0     1
*PIN:    8 7 6 5 4 3 2 1 7 6 5    4  3  2  1  9        9
*
 SENSE:                                                L
*                          B  B  B  B  B  B  B  B       B
*ROW     7 6 5 4 3 2 1 0 7 6 5    4  3  2  1  0        9
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0     L - - - - - - - - - -    H  -  -  -  -        A    NOX+
   1     H - - - - - - - - - -    H  H  H  -  -  H  -  A    ASG-*SRG-*CLE-
   2     H - - - - - - - - L -    -  -  -  -  -  -  -  A    STE
   3     H - L L - - - - - - -    L  H  -  -  -  -  -  A    ASG PAE
   4     H - H L - - - - - - -    L  L  -  -  -  -  -  A    ASG CME
   5     H - H H - - - - - - -    L  -  -  -  -  -  -  A    ASG CCE
   6     H L - - L - - - - - -    H  -  -  L  L  A    SRG1 *LS,*RS,R*L,R*R
   7     H H L L L - - - - - -    H  -  -  L  L  A    SRG1 *LR
   8     H H L H L - - - - - -    -  H  L  L  A    SRG1 ER*
   9     H H H L L - - - - - -    -  H  -  L  L  A    SRG1 EL*
  10     H H H H L - - - - - -    H  -  -  L  L  A    SRG1 *LF
  11     H - - - - L - - - - -    H  -  -  L  H  A    SRG2 *LS,*RS,R*L,R*R
  12     H - - - - H L L - - -    H  -  -  L  H  A    SRG2 *LR
  13     H - - - - H L H - - -    -  H  L  H  A    SRG2 ER*
  14     H - - - - H H L - - -    -  H  -  L  H  A    SRG2 EL*
  15     H - - - - H H H - - -    H  -  -  L  H  A    SRG2 *LF
*
*
```

Figure 4-15. E(SRG-ASG) PLA (~~U0708~~ U303) Code

dp 1032

The E(SRG-ASG) PLA handles the SP1/STE and SP1/CLE functions as well as the updating implied by a TBUS/SRG or SP2/ASG microinstruction:

a. If BP.NO.EXECUTE- is "low", or if DP.CLE.SP1-, DP.ASG.SP2-, and DP.R2.SRG-are all "high", "E" will be updated with its current value.

b. If DP.CLE.SP1- is "low", "E" will be cleared unless some other condition is trying to set it.

c. If DP.STE.SP1- is "low", "E" will be set.

d. If DP.ASG.SP2- is "low", IR bits six and seven (DP.IR.REG[7:6]+) are used to determine if "E" should be held, cleared, set, or complemented.

e. If DP.R2.SRG- is "low" and DP.SRG1.SP2- is "low", DP.IR.REG[8:5]+ determine if "E" should be held, cleared, or updated from the upper or lower bit of LREG (DP.L.BUS15+ or DP.L.BUS0+).

f. If DP.R2.SRG- is "low" and DP.SRG.SP2- is "high", DP.IR.REG4+ and DP.IR.REG[2:0]+ determine if "E" should be held or updated from the upper or lower bit of LREG.

4.3.11.3 E/CIN/COUT PLA

The E/CIN/COUT PLA, which is located at U0604 (DP103C), generates DP.E.ENOE-. The code for this PLA is listed in Figure 4-9, above. This PLA can only affect the value of "E" if BP.NO.EXECUTE- and DP.R2.UP.CO+ are both "high" and DP.ENOE.SP1- is "low" (SP1/ENOE occurs in the line following an arithmetic TBUS field operation). When this is the case, "E" is set at the end of the cycle if the current operation will produce a carry or borrow out. Carry and borrow are determined in the same manner used to generate the COUT condition (refer to paragraph 4.3.6.3 above). This process can only set "E", never clear it.

The O-Register (DP.O+) is stored in register U0704 (DP103B). At the end of each microcycle it is updated with the value from DP.O.IN+, which is generated by the O-OVFL PLA U0504 (DP105E). The code for this PLA is listed in Figure 4-10 above.

The O-Register can be affected by microinstructions SP1/CLO, SP1/STO, and SP1/ENOE. The value of "O" can only be changed if BP.NO.EXECUTE- is "high". Unless one of the following conditions occur, "O" will be updated with its old value. If DP.CLO.SP1- is "low", "O" will be cleared. It DP.STO.SP1- is "low" "O" will be set. If DP.ENOE.SP1- is "low" and DP.R2.UP.CO+ is "high", the value being used to update the OVFL condition will be ORed into the value of "O". Thus "O" will be set if an overflow occurs and left unchanged otherwise. Overflow is detected in the same manner used to update the OVFL condition (refer to paragraph 4.3.6.4 above).

4.3.12 HP 1000 Instruction Set Emulation

Most of the special HP 1000 instruction set emulation features have been described in previous paragraphs.

However, the ASG-No-Skip (ASGN) condition needs additional explanation. The ASG-Skip PLA, U0203 (DP126D), does most of the work for generating this condition. The code for this PLA is listed in Figure 4-16. It looks at six bits from the IR in order to determine which conditions should be tested. These bits and their meanings are listed in Table 4-9.

Table 4-9. ASGN PLA Code

IR Bit	Name	Meaning
DP.IR.REG0+	RSS	Reverse Skip Sense
DP.IR.REG1+	SZ*	Skip if all Zero
DP.IR.REG3+	SL*	Skip if Lsb zero
DP.IR.REG4+	SS*	Skip if Sign zero
DP.IR.REG5+	SEZ	Skip if E Zero
DP.IR.REG9+	CM*/CC*	complement the data before testing

The PLA produces three outputs. DP.SKP.TZ+ goes "high" if SZ* occurs without RSS, indicating that a skip should occur if the TZ condition is true. DP.SKP.NOT.TZ+ goes "high" if SZ* occurs with RSS, indicating that a skip should occur if the TZ condition is false. DP.SKP.MOST.ASG+ goes "high" if any of the other conditions indicate that a skip should occur. These three signals, along with outputs from the two TBUS-Status PLAs (paragraph 4.3.10, above), are used by the AOI gate U0103 (DP84C) to produce the signal DP.ASGN+ which goes "high" if none of the ASG conditions indicate that a skip should occur. The function used to generate DP.ASGN+ is the following:

```
not (DP.ASGN+) =  (DP.SKP.MOST.ASG+) +
                  (DP.SKP.TZ+ * DP.TL8Z+ * DP.TU8Z+) +
                  (DP.SKP.NOT.TZ+ * DP.TL8Z-) +
                  (DP.SKP.NOT.TZ+ * DP.TU8Z-)
```

```
*
*
*                                          D
*                                          P
*                                        D .
*                                        P S
*                                        . K
*       D   D D D D D D                  S P
*       P D P P P P P P                D K .
*       . P . . . . . . D              P P M
*       L . I I I I I I P              . . O
*       . L R R R R R R .              S N S
*       B . . . . . . . O              K O T
*       U B R R R R R R L              P T .
*       S U E E E E E E D              . . A
*       1 S G G G G G G .              T T S
*       5 0 9 5 4 3 1 0 E              Z Z G
*       + + + + + + + + +              + + +
*
*       0 0 0 0 0 0 0 0 0              1 1 1
*PIN:   8 7 6 5 4 3 2 1 9              9 8 7
*
 SENSE:                                H H H
*                                      B B B
*ROW    7 6 5 4 3 2 1 0 0              9 8 7
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - L L L L H -              . . A   RSS
   1    - - - H - - - L L              . . A   SEZ
   2    - - - H - - - H H              . . A   SEZ RSS
   3    - L L - - H - L -              . . A   SL*
   4    - H H - - H - L -              . . A   SL* CM*(or CC*)
   5    L - L - H - - L -              . . A   SS*
   6    H - H - H - - L -              . . A   SS* CM*(or CC*)
   7    - H L - L H - H -              . . A   SL* RSS
   8    - L H - L H - H -              . . A   SL* RSS CM*(or CC*)
   9    H - L - H L - H -              . . A   SS* RSS
  10    L - H - H L - H -              . . A   SS* RSS CM*(or CC*)
  11    H H L - H H - H -              . . A   SL* SS* RSS
  12    L L H - H H - H -              . . A   SL* SS* RSS CM*(or CC*)
  13    - - - - - - H H -              . A .   SZ* RSS
  14    - - - - - - H L -              A . .   SZ*
*
*
```

Figure 4-16. ASG-Skip PLA (U0203) Code

DP.SKP.MOST.ASG+ indicates skips caused by conditions other than SZA and SZB. It is generated in a straight forward manner with the following exceptions:

a. The SEZ condition is based on DP.OLD.E+ that is a delayed version of DP.E+. The delay is one microcycle inserted by the register U0404 (DP123B). This is necessary since "E" must be tested before it is modified by the ASG instruction.

b. The SLA,SLB, SSA, and SSB skip conditions are based on bits of LREG (DP.L.BUS0+ and DP.L.BUS15+). However, since the complement required by a CM* or CC* operation is done in the ALU, the PLA must complement the LREG bits before they are tested if the CM*/CC* bit is set.

c. An RSS (Reverse Skip Sense) by itself indicates that a skip should always occur. However, an RSS with another condition indicates that a skip should occur if that condition is not met.

d. If SS* (SSA or SSB), SL* (SLA or SLB), and RSS occur together, a skip will occur only if (SS*, RSS) and (SL*, RSS) both indicate that a skip should occur. However, for most combinations of conditions, a skip will occur if conditions so indicate.

4.3.13 Special Decoding

The advent of the PLA allows a single chip to decode many fields and convert them to control signals. Examples of this are the TBUS field, SP0/LSL, and the SP1 specials which control F1 and F2. However, some specials must be decoded by more than one chip. The TBUS-UBUS PLA U0802 (DP112E) decodes the SU, RSLR, ACCL, and ACCR specials in the SP0 field to generate the following four "low true" signals: DP.SU.SP0-, DP.RSLR.SP0+, DP.ACCL.SP0-, and DP.ACCR.SP0-. The code for the TBUS-UBUS PLA is listed in Figure 4-12, above.

The decoder U0305 (DP123D) decodes the SP1 field (BP.UIR.REG[7:4]+). This decoder uses two OP field bits (BP.UIR.REG[45:44]+) to enable it only when RTNC or SP1C appear in the OP field. The FCLR, ENOE, STE, CLE, and NINC specials are decoded to produce five "low true" outputs (DP.FCLR.SP1-, DP.ENOE.SP1-, DP.STE.SP1-, DP.CLE.SP1-, and DP.NINC.SP1-).

Since the first four of these specials are unconditional, their outputs can be used directly. Since SP1/NINC is conditional when OP/SP1C occurs, DP.NINC.SP1- must be qualified by the AOI gate located at U0105 (DP128D). This gate produces BP.NINC.SP1- which goes "low" if DP.NINC.SP1- and DP.UIR.REG46+ are both "low" (OP/RTNC) or if DP.NINC.SP1- is "low" and BP.CNDX.MET+ is "high" (condition is met for OP/SP1C).

The Flags-STOR PLA U0304 (DP123C) decodes several more SP0 orders which are conditional when OP/SP1C occurs. The code for this PLA is listed in Figure 4-14, above. The STO and CLO microorders are decoded to produce DP.STO.SP1- and DP.CLO.SP1-. Notice that each special uses two PLA terms, one for the RTNC case and one for the SP1C case. This PLA also produces DP.R1.STORE.EN- which goes "high" if the STOU and STOT stores indicated by the current UIR has not been performed. It goes "high" (no store) if BP.NO.EXECUTE- is "low" or if OP/SP1C and SP1/STOR both occur when 2BP.CNDX.MET+ is "low" (condition not met). DP.R1.STORE.EN- is delayed by the register U0404 (DP123B) to form BP.R2.STORE.EN- which is used to stop the STOT stores.

The decoder U0405 (DP107C) decodes the SP2 field (BP.UIR.REG[3:0]+). It looks at two OP field bits (BP.UIR.REG[45:44]+) to assure that it is only enabled when OP/RTNC or OP/SP1C occur. It decodes the FAS, FMPY, FDIV, LDIR, ASG, SRG1, and SU specials to produce the corresponding "low" true outputs: DP.FAS.SP2-, DP.FMPY.SP2-, DP.FDIV.SP2-, DP.LDIR.SP2-, DP.ASG.SP2-, DP.SRG1.SP2-, and DP.SU.SP2-.

4.3.14 Timing and Clocks

Two copies of the CPU clock are used by the DP card (CK.CPU3.DP+ and CK.CPU4.DP+). Gated clocks are generated directly from these versions. In addition CK.CPU4.DP+ is buffered by U0507 (DP66D) to produce CK.CPU4.B1.DP+ and CK.CPU4.B2.DP+ which are used as ungated clocks. This chip also produces FP.CK.CPU.DP+ which is available on the frontplane for diagnostic purposes.

A delay line U0503 (DP66E) delays CK.CPU3.DP+ by 20, 30, 40, and 50 nanoseconds. The four delayed clocks are called CK.CPU3.Dnn.DP+ where nn is the delay in nanoseconds.

Because of clock skew problems, a UIR bit cannot be sent directly into a register which is clocked at the microcycle boundary. Usually this is not a problem since there is logic which adds delay between the UIR bit and the following register. However, for seven of the bits a register clocked in the middle of the microcycle is used to add this delay. U0601 (DP25E) is clocked 40 ns into the microcycle to convert BP.UIR.REGn+ to DP.F1.UIR.REGn+ for n = 8, [19:15], and 26.

4.4 Parts Locations

The parts locations for the data path card are shown in Figure 4-17.

4.5 Replaceable Parts List

The replaceable parts list for the data path card are listed in Table 4-10. The names and addresses of the manufacturers of the parts are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

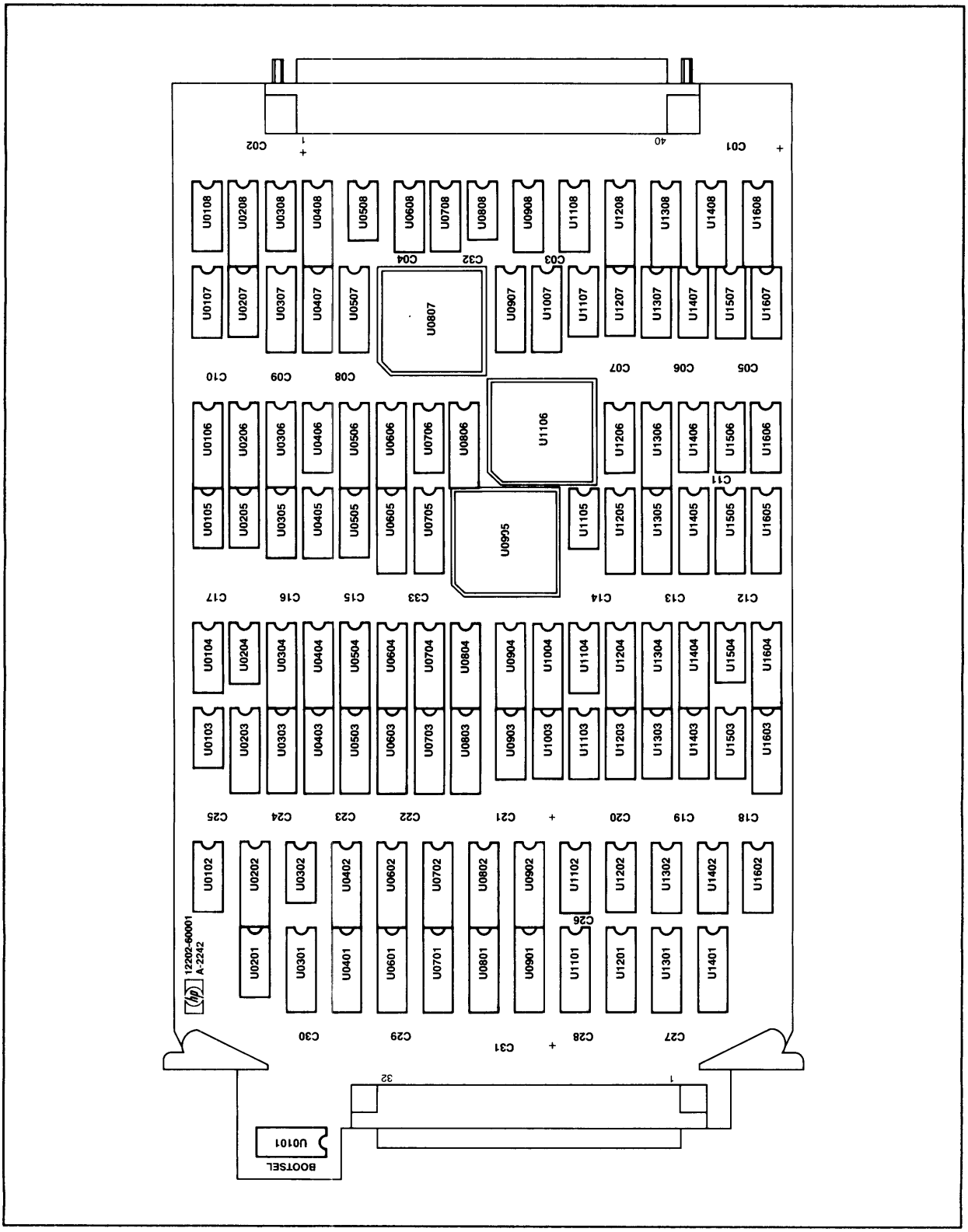


Figure 4-17. Data Path Card Parts Locations

Table 4-10. Data Path Card Replaceable Parts (Sheet 1 of 2)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12202-60001	2	1	PCA-DATA PATH	28480	12202-60001
C1	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-4835	7	29	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C31	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C32	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C33	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
U101	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U102	1820-2936	6	5	IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U103	1020-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U104	1820-2936	6		IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U105	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U106	1820-2795	5	15	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U107	1820-2936	6		IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U108	1820-2936	6		IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U201	1010-0256	8	1	NETWORK-RES 16-DIP1.0K OHM X 15	01121	316A102
U202	1820-2701	3	21	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U203	1020-3044	9	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3044
U204	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U205	1020-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U207	1820-2936	6		IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U208	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U301	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U302	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U303	1820-3037	0	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3037
U304	1820-3043	8	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3043
U305	1020-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U306	1820-3033	6	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3033
U307	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U308	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U401	1820-3036	9	2	IC PRGMBL-LGC TTL S PLA	28480	1820-3036
U402	1820-3036	9		IC PRGMBL-LGC TTL S PLA	28480	1820-3036
U403	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U404	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U405	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U406	1816-1495	1	12	IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U407	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U408	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U503	1820-3041	6	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3041
U504	1820-3039	2	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3039
U505	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U506	1820-2700	2	4	IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U507	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U508	1813-0340	7	1	IC DLY-LN HYBRID MULTI-TAP	28480	1813-0340
U601	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U602	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC

Table 4-10. Data Path Card Replaceable Parts (Sheet 2 of 2)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U603	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U604	1820-3038	1	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3038
U605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U606	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U608	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U701	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U702	1820-2526	0	1	IC RGTR TTL S D-TYPE OCTL	34335	AM74S534PC
U703	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U704	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U705	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U706	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U708	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U801	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U802	1820-3040	5	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3040
U803	1820-3042	7	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3042
U804	1820-1458	5	4	IC ARITH-LGC-UN TTL S 4-BIT	01295	SN74S381N
U806	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U808	1820-1275	4	1	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U901	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U902	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U903	1820-1302	8	2	IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S251N
U904	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U907	1820-3034	7	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3034
U908	1820-1981	9	2	IC RGTR TTL S QUAD 2-INP	34335	AM25S09PC
U1003	1820-2458	7	8	IC MISC TTL S 4-BIT	34335	AM25S10PC
U1004	1820-1458	5		IC ARITH-LGC-UN TTL S 4-BIT	01295	SN74S381N
U1007	1820-3035	8	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3035
U1101	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U1102	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1103	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1104	1820-1305	1	1	IC GEN TTL S LOOK-AHD-CRY	01295	SN74S182N
U1105	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U1107	1820-2763	7	2	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F258PC
U1108	1820-1981	9		IC RGTR TTL S QUAD 2-INP	34335	AM25S09PC
U1201	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1202	1820-1302	8		IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S251N
U1203	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1204	1820-1458	5		IC ARITH-LGC-UN TTL S 4-BIT	01295	SN74S381N
U1205	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1206	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1207	1820-2763	7		IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F258PC
U1208	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1301	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1302	1820-2769	3	2	IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1303	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1304	1820-1458	5		IC ARITH-LGC-UN TTL S 4-BIT	01295	SN74S381N
U1305	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1306	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1307	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1308	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1402	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1403	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1404	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1405	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1406	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1407	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1408	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1503	1820-2458	7		IC MISC TTL S 4-BIT	34335	AM25S10PC
U1504	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U1505	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1506	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1507	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1602	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1603	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1604	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1606	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1607	1816-1495	1		IC TTL S 64-BIT STAT RAM 35-NS 3-S	34335	AM27S07APC
U1608	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795

	B-12202-80001-51		
A	AS ISSUED	mcf/ko	10/25/82
B	DEL. P/N 5180-0195 & ADDED P/N 1816-1495 PER PRCR 'A'. CORRECTED NOS. ON 74F374	mcf/ko	2/23/83

STOU

RIGHT PRIMARY REGISTER FILE

LEFT PRIMARY REGISTER FILE

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

	DATA PATH - A900 PRIMARY REGISTER FILE	HEWLETT PACKARD
	12202A	12202-60001
	SHEET OF	D-12202-60001-51

DP1

			D-12202-60001-52
A	AS ISSUED	maf/ko	10/25/82
B	DEL. P/N 5180-0195 & ADDED 1818-1495 PER PRCR 'A'. CORRECTED NOS. ON 74F374.	maf/ko	2/23/83

SECONDARY REGISTER FILE

30C 80E 90A 100E 110C 120C 136B — BP.UIR.REG+ /4

59C 79B 30E 80A 131B 143B — BP.T.BUS+ /16

99E DP.RS.EN- (466) → -1449 74S32 U0308

1816-1495 27507 U0708 / U0808 / U0706 / U0406

119D DP.RSLR.SP0+ (266)
139C 100C 110D 120B 68C 10E BP.NO.EXECUTE- (46) / CR.CPU3.D50.DP+ (227) → -0688 74S20 U1105

(DP.RS.CE-) (DP.RS.WE-) CK.A.CPU4.CS.DP+ (131) CK.CPU3.D50.RS- (130)

16 / DP.L.IN.BUS+ → 19C 30C 49A

(231) CK.CPU4.LED.BP+ → 137D 146C

1810-0256 +5V U0201 3 x 1K

(198) DP.PULLUP+ → 80E 110E

(496) LBP.MCHOD- → 137D

(494) LBP.ICHOD- → 137D

1810-0256 RDIP +5V 8 x 1K

3101-2243 DIPSW U0101

U0201 DP.SMCH7+ (312) DP.SMCH6+ (311) DP.SMCH5+ (310) DP.SMCH4+ (309) DP.SMCH3+ (308) DP.SMCH2+ (307) DP.SMCH1+ (306) DP.SMCH0+ (305)

-2785 74F244 U0301

8 / DP.R.IN.BUS+ → 19A 30A 39C

139C BP.LED.STOT- (330)
139C 60E 110E 120E CK.A.CPU4.DP+ (9) → -1449 74S32 U0308

99D 146C DP.SMCH.RREG- (313)

-2701 74F374 U0601

30C 80E 90A 100E 110C 120C 136B BP.UIR.REG+ /7

68E CK.CPU3.D40.DP+ (357)

7 / DP.F1.UIR.REG+ → 30C 40E 110A

DP2

	DATA PATH - A900 SECONDARY REGISTER FILE AND SWITCHES	
	12202A	12202-60001
		D-12202-60001-52

DP2

			D-12202-60001-53
A	AS ISSUED	maf/ko	10/25/82
B	CORRECTED NOS. ON 74F373 & 74F374		
	PER PRCR 'A'	maf/ko	2/23/8

SBUS

ACCR

ZERO/ONES

RREG

IMM

ACCL

ZERO/ONES/SIGN

LREG

19A 29C 39C 120E 133C — DP.R.IN.BUS+ 16 / BP.S.BUS+ 16

99D DP.S.BUS.EN- (151)

-2795 74F244 U1308: (340) 8 1A4 1Y4 12 (109) 15; (339) 6 1A3 1Y3 14 (108) 14; (338) 4 1A2 1Y2 16 (107) 13; (337) 2 1A1 1Y1 18 (106) 12; (336) 17 2A4 2Y4 3 (105) 11; (335) 15 2A3 2Y3 5 (104) 10; (348) 13 2A2 2Y2 7 (111) 9; (347) 11 2A1 2Y1 9 (110) 8; 1G 2G; 1 19

-2795 74F244 U1208: (346) 8 1A4 1Y4 12 (94) 7; (345) 6 1A3 1Y3 14 (93) 6; (344) 4 1A2 1Y2 16 (92) 5; (343) 2 1A1 1Y1 18 (91) 4; (342) 17 2A4 2Y4 3 (90) 3; (341) 15 2A3 2Y3 5 (89) 2; (334) 13 2A2 2Y2 7 (88) 1; (333) 11 2A1 2Y1 9 (87) 0; 1G 2G; 1 19

-2700 74F373 U1505: (117) 18 D8 Q8 19 (109) 15; (116) 17 D7 Q7 16 (108) 14; (115) 14 D6 Q6 15 (107) 13; (114) 13 D5 Q5 12 (106) 12; (113) 8 D4 Q4 9 (105) 11; (112) 7 D3 Q3 6 (104) 10; (119) 4 D2 Q2 5 (111) 9; (118) 3 D1 Q1 2 (110) 8; G OE; 11 1

-2700 74F373 U1603: (159) 18 D8 Q8 19 (94) 7; (158) 17 D7 Q7 16 (93) 6; (157) 14 D6 Q6 15 (92) 5; (156) 13 D5 Q5 12 (91) 4; (155) 8 D4 Q4 9 (90) 3; (154) 7 D3 Q3 6 (89) 2; (153) 4 D2 Q2 5 (88) 1; (152) 3 D1 Q1 2 (87) 0; G OE; 11 1

-2795 74F244 U1408: 8 1A4 1Y4 12 (109) 15; 6 1A3 1Y3 14 (108) 14; 4 1A2 1Y2 16 (107) 13; 2 1A1 1Y1 18 (106) 12; 17 2A4 2Y4 3 (105) 11; 15 2A3 2Y3 5 (104) 10; 13 2A2 2Y2 7 (111) 9; 11 2A1 2Y1 9 (110) 8; 1G 2G; 1 19

-2795 74F244 U1608: 8 1A4 1Y4 12 (94) 7; 6 1A3 1Y3 14 (93) 6; 4 1A2 1Y2 16 (92) 5; 2 1A1 1Y1 18 (91) 4; 17 2A4 2Y4 3 (90) 3; 15 2A3 2Y3 5 (89) 2; 13 2A2 2Y2 7 (88) 1; 11 2A1 2Y1 9 (87) 0; 1G 2G; 1 19

-2701 74F374 U1306: (109) 18 D8 Q8 19 (7) 15; (108) 17 D7 Q7 16 (21) 14; (107) 14 D6 Q6 15 (20) 13; (106) 13 D5 Q5 12 (42) 12; (105) 8 D4 Q4 9 (19) 11; (104) 7 D3 Q3 6 (18) 10; (111) 4 D2 Q2 5 (10) 9; (110) 3 D1 Q1 2 (25) 8; CLK OE; 11 1

-2701 74F374 U0701: (94) 18 D8 Q8 19 (24) 7; (93) 17 D7 Q7 16 (23) 6; (92) 14 D6 Q6 15 (22) 5; (91) 13 D5 Q5 12 (45) 4; (90) 8 D4 Q4 9 (44) 3; (89) 7 D3 Q3 6 (43) 2; (88) 4 D2 Q2 5 (41) 1; (87) 3 D1 Q1 2 (17) 0; CLK OE; 11 1

16 DP.R.BUS+ → 40A 50A 60B 80D 100E 140C

16 DP.R.IN.BUS+ → 19A 29A 30A 120E

898 79C 10A 143C — DP.U.BUS+ 16

119E CK.CPU4.ACCR.DP- (228)

99D DP.ACCR.RREG- (233)

99D DP.R.BIT.EN- (149)

29E DP.P1.UIR.REG26+ (413) — 74S04 U0205 -0683 — DP.UIR.REG26- (4)

19C 29B 49A — DP.L.IN.BUS+ 16 / 20E 80E 90A 100E 110C 120C 136B — BP.UIR.REG+ 16

99D DP.IMM.EN- (134)

-2795 74F244 U0206: (222) 8 1A4 1Y4 12 (77) 15; (221) 6 1A3 1Y3 14 (76) 14; (220) 4 1A2 1Y2 16 (75) 13; (100) 2 1A1 1Y1 18 (74) 12; (99) 17 2A4 2Y4 3 (73) 11; (98) 15 2A3 2Y3 5 (72) 10; (166) 13 2A2 2Y2 7 (85) 9; (165) 11 2A1 2Y1 9 (84) 8; 1G 2G; 1 19

-2795 74F244 U0408: (170) 8 1A4 1Y4 12 (83) 7; (169) 6 1A3 1Y3 14 (82) 6; (168) 4 1A2 1Y2 16 (81) 5; (167) 2 1A1 1Y1 18 (80) 4; (219) 17 2A4 2Y4 3 (79) 3; (217) 15 2A3 2Y3 5 (78) 2; (213) 13 2A2 2Y2 7 (71) 1; (212) 11 2A1 2Y1 9 (70) 0; 1G 2G; 1 19

-2700 74F373 U0806: (12) 18 D8 Q8 19 (77) 15; (34) 17 D7 Q7 16 (76) 14; (33) 14 D6 Q6 15 (75) 13; (31) 13 D5 Q5 12 (74) 12; (30) 8 D4 Q4 9 (73) 11; (29) 7 D3 Q3 6 (72) 10; (14) 4 D2 Q2 5 (85) 9; (13) 3 D1 Q1 2 (84) 8; G OE; 11 1

-2700 74F373 U0506: (40) 18 D8 Q8 19 (83) 7; (39) 17 D7 Q7 16 (82) 6; (38) 14 D6 Q6 15 (81) 5; (37) 13 D5 Q5 12 (80) 4; (36) 8 D4 Q4 9 (79) 3; (35) 7 D3 Q3 6 (78) 2; (28) 4 D2 Q2 5 (71) 1; (11) 3 D1 Q1 2 (70) 0; G OE; 11 1

-2795 74F244 U0106: 8 1A4 1Y4 12 (77) 15; 6 1A3 1Y3 14 (76) 14; 4 1A2 1Y2 16 (75) 13; 2 1A1 1Y1 18 (74) 12; 17 2A4 2Y4 3 (73) 11; 15 2A3 2Y3 5 (72) 10; 13 2A2 2Y2 7 (85) 9; 11 2A1 2Y1 9 (84) 8; 1G 2G; 1 19

-2795 74F244 U0407: 8 1A4 1Y4 12 (83) 7; 6 1A3 1Y3 14 (82) 6; 4 1A2 1Y2 16 (81) 5; 2 1A1 1Y1 18 (80) 4; 17 2A4 2Y4 3 (79) 3; 15 2A3 2Y3 5 (78) 2; 13 2A2 2Y2 7 (71) 1; 11 2A1 2Y1 9 (70) 0; 1G 2G; 1 19

-2701 74F374 U1205: (77) 18 D8 Q8 19 (5) 15; (76) 17 D7 Q7 16 (60) 14; (75) 14 D6 Q6 15 (59) 13; (74) 13 D5 Q5 12 (58) 12; (73) 8 D4 Q4 9 (57) 11; (72) 7 D3 Q3 6 (56) 10; (85) 4 D2 Q2 5 (69) 9; (84) 3 D1 Q1 2 (68) 8; CLK OE; 11 1

-2701 74F374 U1305: (83) 18 D8 Q8 19 (67) 7; (82) 17 D7 Q7 16 (66) 6; (81) 14 D6 Q6 15 (65) 5; (80) 13 D5 Q5 12 (63) 4; (79) 8 D4 Q4 9 (62) 3; (78) 7 D3 Q3 6 (61) 2; (71) 4 D2 Q2 5 (55) 1; (70) 3 D1 Q1 2 (8) 0; CLK OE; 11 1

16 DP.L.BUS+ → 40A 50A 60C 70C 80D 90C 100E 120D 140B

59C 79B 20A 80A 131B 143B — BP.T.BUS+ 16

119E CK.CPU4.ACCL.DP- (288)

99E DP.ACCL.LREG+ (232)

99E DP.L.BIT.EN- (140)

99D DP.L.BIT+ (3)

10B 68D 80D — CK.A.CPU4.B1.DP+ (52)

40E 68D 80D 100B 110B — CK.A.CPU4.B2.DP+ (16)

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +SM
INDICATES THAT THIS PART HAS BEEN PROGRAMMED

DP3

	DATA PATH - A900 PIPELINE REGISTERS	
	12202A	12202-60001
		D-12202-60001-53

DP

	AS ISSUED	mcf/ko	10/25/82
	CORRECTED NOS. ON 74F374;CHGD 1RE7-6201 TO 1RE7-6200;CHGD 1RH4-6201 TO 1RH4-6200 PER PRCR 'A'	mcf/ko	2/23/83

D-12202-60001-54

FAS

FMPY

FDIV

39A 50A 60B 80D 100E 140C — DP.R.BUS+ /16

39C 50A 60C 70C 80D 90C 100E 120D 140B — DP.L.BUS+ /16

DP.R2.UIR.REG+

DP.D.BUS+

16/ DP.L.IN.BUS+ — 19C 29B 30C

1RE7-6200 U0905 — ADDCHILDA

1RH4-6200 U0807 — TOSDATA

1RH7-6202 U1106 — GAZINTA

VDD = 30
VCC = 18,19
GND = 1,20, 31,48

-2901 74F374 U0705

-2701 74F374 U0806

-2701 74F374 U0805

-1322 74S02 U0505

-0683 74S04 U0205

129D DP.FCLR.SP1- (193)

99E DP.FAS.LREG- (417)
99E DP.FMPY.LREG- (421)
99E DP.FDIV.LREG- (419)

109C DP.FAS.SP2- (418)
109C DP.FMPY.SP2- (422)
109C DP.FDIV.SP2- (420)

DP.R2.FAS.SP2- (456)
DP.R2.FMPY.SP2- (458)
DP.R2.FDIV.SP2- (457)

29E 110A DP.F1.UIR.REG+ /4

30E 68D 80D 100B 110B CK.A.CPU4.B2.DP+ (16)

68E CK.CPU3.D30.BF- (356)

99E DP.FXXX.EN- (242)

(129) CK.CPU3.D30.BF-

CK.FAS.DP-
CK.FMPY.DP-
CK.FDIV.DP- (360)

(361)
(359)

(194) DP.FERR+ — 80C

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

DP4

DATA PATH - A900
SOS LSI

HEWLETT PACKARD

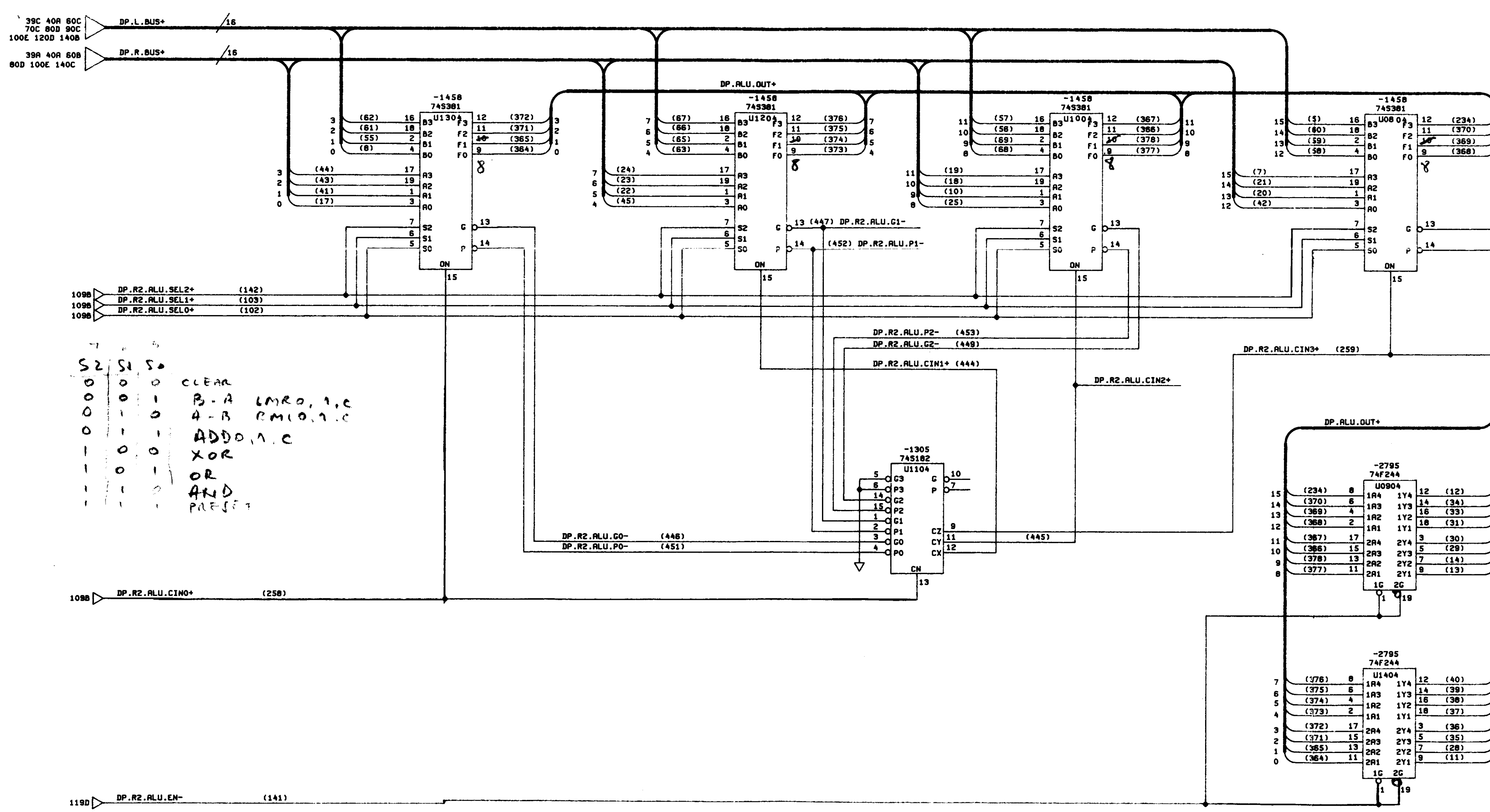
12202-60001

D-12202-60001-54

D-12202-60001-55

REV	REVISIONS	APPROVED	DATE
A	AS ISSUED	maf/ko	10/25/82

ALU



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

DP5

DATA PATH - A900
ALU

HEWLETT PACKARD
12202-60001
D-12202-60001-55

REVISIONS				
ZONE	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	maf/ko	10/25/82

D-12202-60001-56

PG

RBUS

BIG SHIFT

-2795 74F244 U0801

119E DP.R2.UIR.REG8+ (144)

119E DP.R2.PG.RU.EN- (261)

70E 119E DP.R2.UIR.REG15+ (143)

119E DP.R2.HI.RU.EN- (260)

-2795 74F244 U1201

-2795 74F244 U1301

16 DP.U.BUS+ → 10A 30C 79C 143C

38A 40A 50A 60D 100E 140C DP.R.BUS+ 16

-2458 25S10 U1102

-2458 25S10 U1503

-2458 25S10 U1203

-2458 25S10 U1303

39C 40A 50A 70C 80D 90C 100E 120D 140B DP.L.BUS+ 16

119B DP.SH.TX.SEL3+ (27)

119B DP.SH.TX.SEL2+ (26)

16 DP.SH.MID+ → 70A

-2789 74F153 U1602

-2789 74F153 U1302

-2795 74F244 U0507

(325) FP.CK.CPU.DP+ → 146B

(16) CK.A.CPU4.B2.DP+ → 30E 40E 80D 100B 110B

(52) CK.A.CPU4.B1.DP+ → 10B 30E 80D

1813-0340 HY5072 U0508

(227) CK.CPU3.D50.DP+ → 10E 20B

(357) CK.CPU3.D40.DP+ → 20E

(358) CK.CPU3.D30.DP+ → 40E

(355) CK.CPU3.D20.DP+ → 10D

139C 20D 110E 120E CK.A.CPU4.DP+ (9)

139C 10D 90B 120B CK.A.CPU3.DP+ (6)

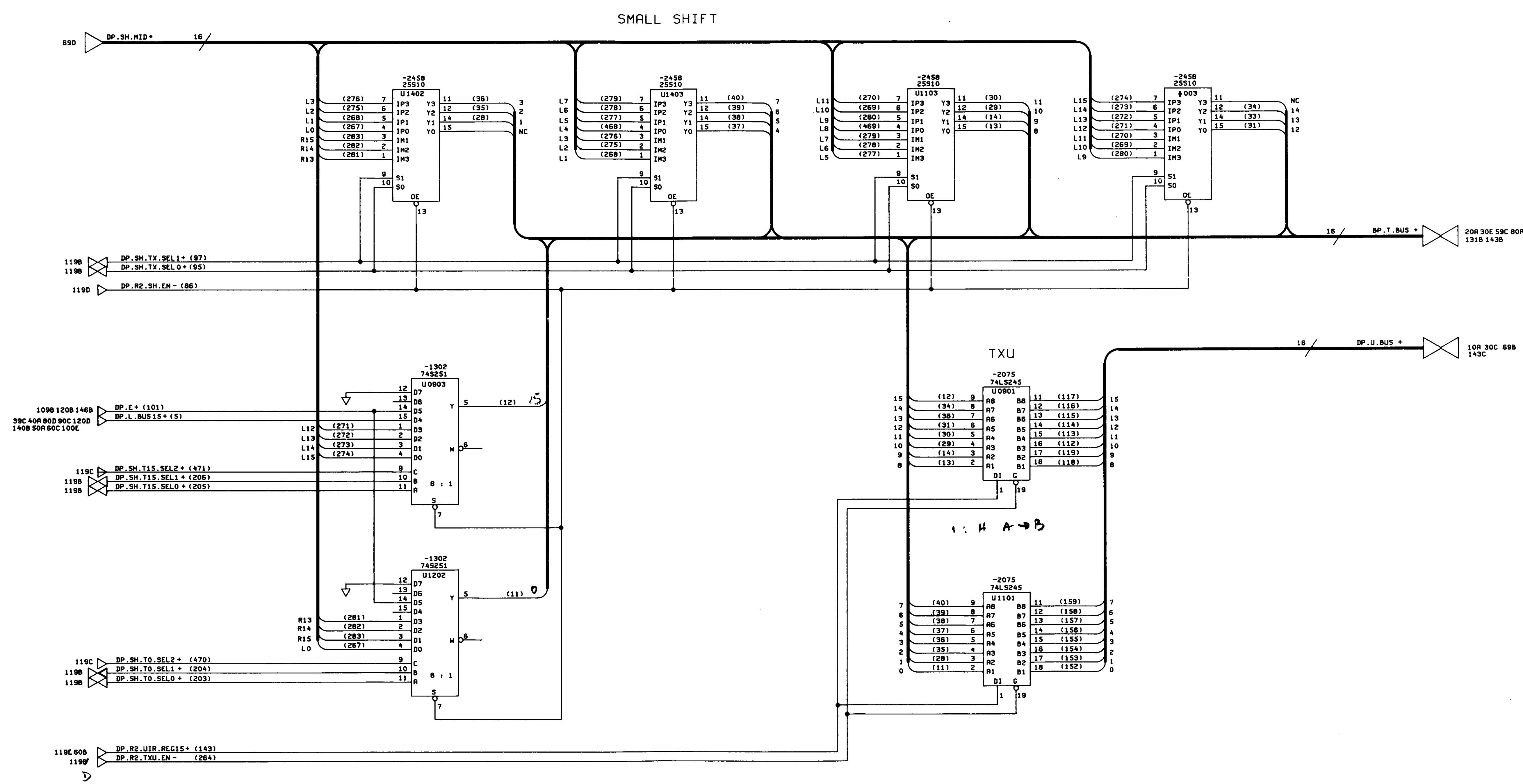
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

DP6

	DATA PATH - A900 BIG SHIFT & PASR	HEWLETT PACKARD
		12202-60001
		D-12202-60001-56

D- 12202-60001-57

SYM	REVISIONS	APPROVED	DATE
A	ISSUED	mf/k.o	10/25/82



DP7

DATA PATH-A900
SMALL SHIFT AND TXU

TITLE: 1220 (NEXT ASSEMBLY)

HEWLETT PACKARD

12202-60001 (PART NUMBER)

D - 12202-60001-57

A	AS ISSUED	mgf/ko	10/25/82
B	CHGD. FAB P/No TO PURCH. P/No. CORRECTED NOS. ON 74F374 PER PRCR 'A'	mgf/ko	2/23/83

D-12202-80001-58

TBUS STATUS

CONDITION MUX

STATUS REG

DP.CNDX+

DP.CNDX.0.15+ (406)

DP.CNDX.0.7- (401)

DP.CNDX.0.7+ (400)

DP.CNDX.8.15-

DP.CNDX.16.23+

DP.CNDX.16.23-

DP.CNDX.24.31+

DP.CNDX.24.31-

DP.TON+ (488)

DP.TZ+ (492)

DP.TULZ+ (487)

DP.RSGN+ (379)

DP.SKP.NOT.TZ+ (284)

DP.SKP.TZ+ (472)

DP.SKP.MOST.RSG+ (150)

DP.FERR+ (194)

LBP.IORQ- (495)

BP.INTP+ (328)

CK.A.CPU4.B1.DP+ (52)

CK.CPU4.STAT.DP+ (358)

CK.A.CPU4.B2.DP+ (16)

DP.L.BUS15+ (L15) (5)

DP.L.BUS0+ (L0) (8)

DP.R.BUS15+ (R15) (7)

DP.R.BUS0+ (R0) (17)

DP.F2+ (191)

DP.F1+ (190)

DP.COUT+ (173)

DP.OVFL+ (197)

DP.IR.REG11+ (243)

DP.O+ (196)

DP.PULLUP+ (TRUE) (198)

BP.T.BUS+ /16

BP.UIR.REG+ /7

BP.CNDX.MET+ (161) ▷ 120C 137D

DPL01

DPL01

DATA PATH - A900 STATUS	HEWLETT PACKARD
12202-80001	
D-12202-80001-58	

	D-12202-60001-59		
A	AS ISSUED	aaf/ko	10/25/82
B	CHGD. FAB. P/Ns TO PURCH. P/Ns per PRCR "A"	aaf/ko	2/23/83

WRITE ADDRESS DELAY

READ/WRITE

20A 20E 30C 40A 80E 100E 110A 120C 136B — BP.UIR.REG+ /16

DP.WR.ADR+

-1981 25S09 U0908

-1981 25S09 U1108

-2763 74F258 U1207

-2763 74F258 U1107

DP.WR. TAB.ADR+

4/ DP.R.ADR- → 10A

4/ DP.L.ADR- → 10C

139C BP.B.CA.ADR+ (328)
139C 10D 60E 120B CK.A.CPU3.DP+ (6)
139C 120A BP.AB.CA.WR- (209)

DP.LREG.ADR+

100E 110A 129E DP.IR.REG+ 2

LREG ADDR -3035 82S153 U1007 DPL04

-1275 74S260 U0808

39C 40A 100E 120D 50A 80D 100E 120D 60C 70C 140B
DP.R2.RP.WR- (262)
DP.L.BUS15+ (5)

RREG/STOU -3034 82S153 U0907 DPL03

LREG SEL -3033 82S153 U0306 DPL02

129C DP.R1.STORE.EN- (257)

(326) DP.RB.DP.WR+ → 137D
(210) DP.B.DP.ADR+ → 137D

(438) DP.R1.RP.WR- → 120B
(428) DP.R1.ACCR.STOU- → 120A
(313) DP.SMCH.RREG- → 20D 148C
(467) DP.R.RP.EN+ → 10D
(151) DP.S.BUS.EN- → 30B
(149) DP.R.BIT.EN- → 30C
(233) DP.ACCR.RREG- → 30C

(3) DP.L.BIT+ → 30E

(424) DP.L.RP.EN+ → 10D
(466) DP.RS.EN- → 20B
(134) DP.IMM.EN- → 30D
(140) DP.L.BIT.EN- → 30E
(242) DP.FXXX.EN- → 40E
(232) DP.ACCL.LREG- → 30E
(418) DP.FDIV.LREG- → 40D
(421) DP.FMPY.LREG- → 40D
(417) DP.FAS.LREG- → 40D

NOTE:
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ALL RESISTORS ARE 1/8W. 1%.
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NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

DP9

	DATA PATH - A900 RP, LREG, RREG CONTROL	HEWLETT PACKARD
		12202-60001
		D-12202-60001-59

REVISIONS			
ZONE	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	maf/ko	10/25/82
B	CORRECTED G2A TO G2B & G2B TO G2A ON 74S138. CORRECTED NOS. ON 74F374.		
	CHGD. FAB. P/No TO PURCH. P/No PER PRCR "A"	maf/ko	2/23/83

D-12202-80001-80

-2701
74F374
U0704

-0681
74S00
U0204

-0683
74S04
U0205

SP2
-1240
74S138
U0405

E.CIN.COUT
-3038
825153
U0604

E(SRG/ASG)
-3037
825153
U0303

O & OVFL
-3039
825153
U0504

DPL08 4-27

DPL05 4-42

DPL07 4-28

NOTE:
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ALL IC'S ARE 1820-XXXX.
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# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

DP10

	DATA PATH - A900 E, O, CONT, OVFL, SP2	HEWLETT PACKARD
	NEXT ASSEMBLY	12202-60001
	SHEET OF	D-12202-60001-60

DP10

	D-12202-60001-61		
A	AS ISSUED	maf/ko	10/25/82
B	CORRECTED NOS. on 74F374; CHGD.FAB P/Ns to PURCH. P/Ns per PRCR 'A'.	maf/ko	2/23/83

28E 40E — DP.F1.UIR.REG+ /6

129E 90C 100E — DP.IR.REG+ /9

SRG CONTROL -3041 825153 U0503 (PP) — DPL10 — 4-35

DP.SRG.SEL+

SRG -2701 74F374 U0603

LSLN -2701 74F374 U0602

LSL -2526 745534 U0702

NOTE:
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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

109C — DP.SRG1.SP2- (285) (BRG 1/2)

30E 40E 68D 80D 100B — CK.A.CPU4.B2.DP+ (16)

20A 20E 30C 80E 90A 100E 120C 136B — BP.UIR.REG+ /9

ALU/SHIFT -3042 825153 U0803 (PP) — DPL09 — 4-22

TBUS — SPO

109D — DP.ASG.SP2- (172)

139C 20B 100C 120B — BP.NO.EXECUTE- (46)

-2701 74F374 U0703

DP.SH.T15.SEL2+ (471)
DP.R2.SRG- (263)
DP.R2.LSLN- (460)
DP.R2.LSL- (459)
DP.R2.SRG1.SP2- (463)
DP.R2.UP.CO+ (265)
DP.R2.SUBT+ (464)

109C — DP.SU.SP2+ (484)

DP.SU.SP0+ (483) — -1322 74S02 U0505

DP.SU- (482) — -1449 74S32 U0308

TBUS/UBUS -3040 825153 U0802 (PP) — DPL08 — 4-33

UBUS 15

-2701 74F374 U0902

DP.R1.ALU.EN- (430)
DP.R1.SH.EN- (439)
DP.R1.TXU.EN- (441)
DP.R1.HI.RU.EN- (434)
DP.R1.PG.RU.EN- (437)

DP.ACCR.SPO- (363)
DP.ACCL.SPO- (362)

-1150 74S51 U1504

29C 80E 139C 20B 60E 120E — DP.PULLUP+ (198) — CK.R.CPU4.DP+ (9)

129A — DP.R2.ACCR.STOU- (443)

137D — BP.ACCL.STOT- (327)

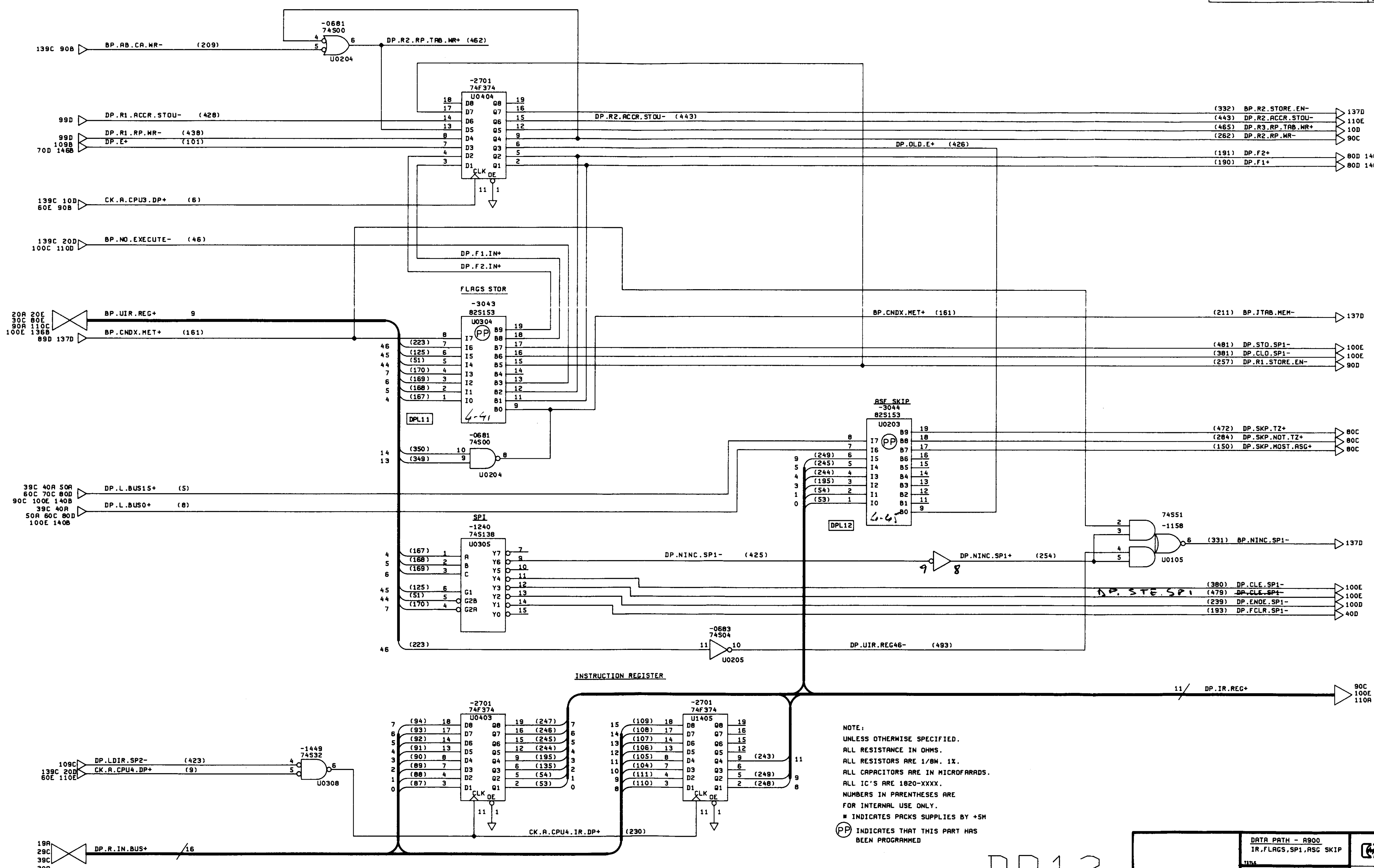
DP11

	DATA PATH - A900 SHIFT, T, U CONTROL	HEWLETT PACKARD
		12202-60001
		D-12202-60001-61

DP11

SYM	REVISIONS	APPROVALS	DATE
A	AS ISSUED	maf/ko	10/25/82
B	CORRECTED NOS.ON 74F374. CORRECTED G2A TO G2B & G2B TO G2A ON 74S138. CHGD. FAB P/Ns to PURCH. P/Ns per PRCR "A"	maf/ko	2/23/83

D-12202-60001-62



NOTE:
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ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED

DP12

DATA PATH - A900
IR,FLAGS,SP1,ASG SKIP

HEWLETT PACKARD

12202-60001

D-12202-60001-62

DP12

				D-12202-60001-63	
A	AS ISSUED	mcf/ko	10/25/82		

59C 79B
20A 30E
80A 143D
BP.T.BUS+

15	(12)	P1-16C	BP.T.BUS15+
14	(34)	P1-16B	
13	(33)	P1-15D	
12	(31)	P1-15C	
11	(30)	P1-15B	
10	(29)	P1-15A	
9	(14)	P1-14D	
8	(13)	P1-14C	
7	(40)	P1-14B	
6	(39)	P1-14A	
5	(38)	P1-13D	
4	(37)	P1-13C	
3	(36)	P1-13B	
2	(35)	P1-13A	
1	(28)	P1-11D	
0	(11)	P1-11C	BP.T.BUS0+

BP.S.BUS+ 30A

BP.S.BUS15+	(340)	P1-39B	15
	(339)	P1-38D	14
	(338)	P1-38C	13
	(337)	P1-38B	12
	(336)	P1-37D	11
	(335)	P1-37C	10
	(348)	P1-37B	9
	(347)	P1-37A	8
	(346)	P1-35D	7
	(345)	P1-35C	6
	(344)	P1-35B	5
	(343)	P1-35A	4
	(342)	P1-34D	3
	(341)	P1-34C	2
	(334)	P1-34B	1
BP.S.BUS0+	(333)	P1-34A	0

BP.UIR.REG+ 20A 20E 30C 80E 90A 100E 110C 120C
(BIT 12 IS UNCONNECTED)

BP.UIR.BUS45+	(223)	P1-30C	46
	(125)	P1-30B	45
	(51)	P1-30A	44
	(222)	P1-29D	43
	(221)	P1-29C	42
	(220)	P1-29B	41
	(100)	P1-29A	40
	(99)	P1-27D	39
	(98)	P1-27C	38
	(166)	P1-27B	37
	(165)	P1-27A	36
	(50)	P1-26D	35
	(49)	P1-26C	34
	(48)	P1-26B	33
	(47)	P1-26A	32
	(354)	P1-25D	31
	(353)	P1-25C	30
	(164)	P1-25B	29
	(163)	P1-25A	28
	(162)	P1-24D	27
	(124)	P1-24C	26
	(351)	P1-24B	25
	(218)	P1-23D	24
	(123)	P1-22C	19
	(122)	P1-22B	18
	(121)	P1-22A	17
	(120)	P1-21D	16
	(216)	P1-21C	15
	(350)	P1-21B	14
	(349)	P1-21A	13
	(215)	P1-19D	12
	(214)	P1-19C	11
	(225)	P1-19B	10
	(171)	P1-19A	9
	(170)	P1-18D	8
	(169)	P1-18C	7
	(168)	P1-18B	6
	(167)	P1-18A	5
	(219)	P1-17D	4
	(217)	P1-17C	3
	(213)	P1-17B	2
	(212)	P1-17A	1
BP.UIR.BUS0+		P1-16D	0

BP.R2.UIR.REG+ (UNCONNECTED)

P1-23C		23
P1-23B		22
P1-23A		21
P1-22D		20

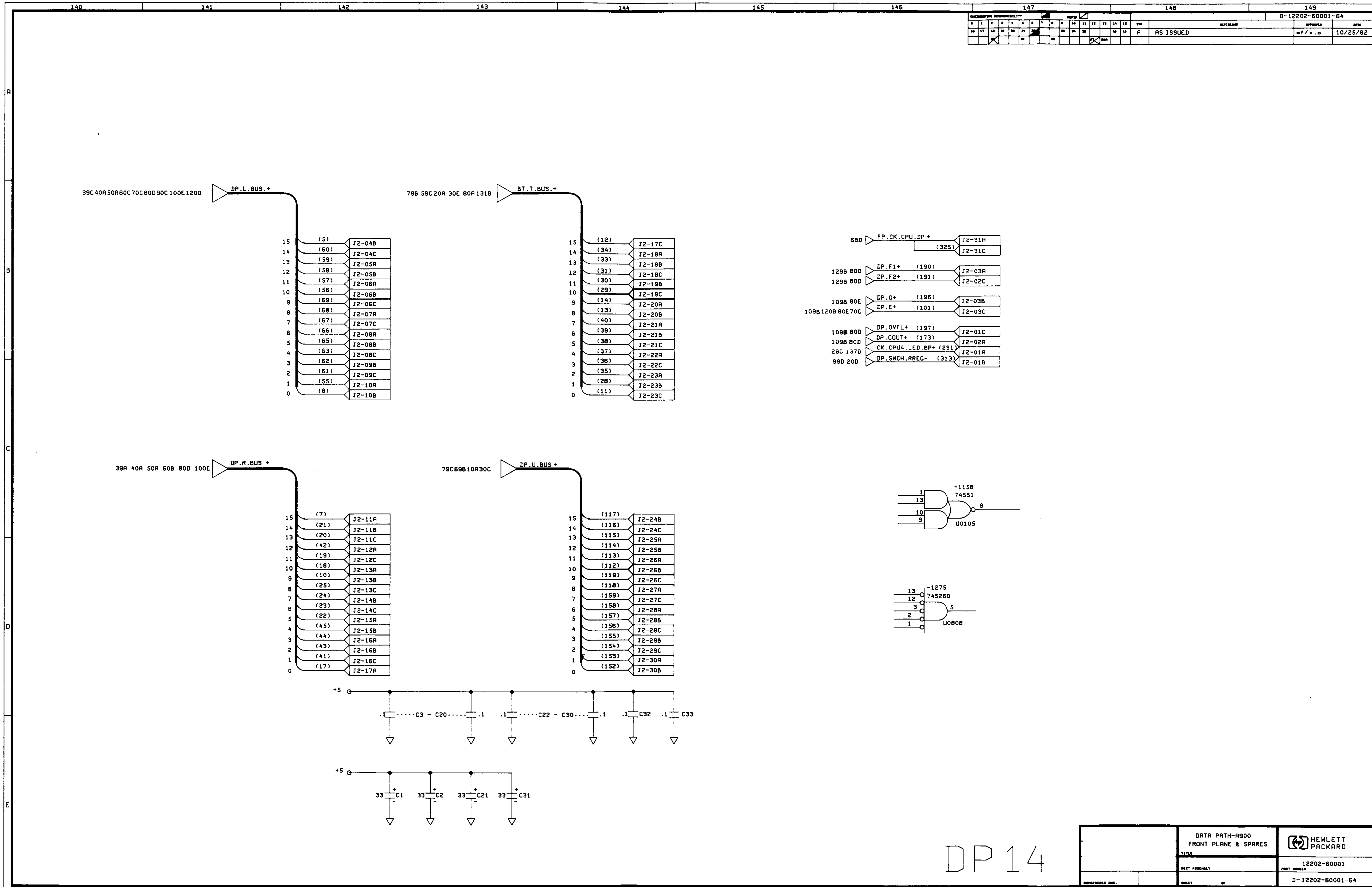
P1-11A	(328)	BP.B.CA.ADR+	90B
P1-10D	(209)	BP.AB.CA.WR-	90B 120A
P1-08A	(6)	CK.A.CPU3.DP+	10D 60E
P1-06B	(9)	CK.A.CPU4.DP+	90B 120B 11E 20D 60E 120E
P1-32C	(46)	BP.NO.EXECUTE-	20B 100C 110D 120B
P1-40D	(329)	BP.INTP+	80C
P1-09B	(330)	BP.LED.STOT-	20D
P1-31A	(495)	LBP.IORQ-	80C
P1-33B		LBP.PON+	(UNCONNECTED)

129A	BP.R2.STORE.EN-	(332)	P1-09C	
99C	BP.B.DP.ADR+	(210)	P1-33A	
89D 120C	BP.CNDX.MET+	(161)	P1-40B	
129C	BP.NINC.SPI-	(331)	P1-40C	
129D	BP.JTAB.MEM-	(211)	P1-30D	
110E	BP.ACCL.STOT-	(327)	P1-39C	
29C 146C	CK.CPU4.LED.BP+	(231)	P1-08D	
99C	BP.AB.DP.WR+	(326)	P1-10A	
29C	LBP.MCMOD-	(496)	P1-01B	
29C	LBP.ICMOD-	(494)	P1-01C	

DP13

	DATA PATH - A900 BACKPLANE	HEWLETT PACKARD
		12202-60001
		D-12202-60001-63

DP12



D-12202-60001-64
A AS ISSUED mf/k.o 10/25/82
39C 40A 50A 60C 70C 80D 90C 100E 120D
DP.L.BUS.+
15 (5) J2-04B
14 (60) J2-04C
13 (59) J2-05A
12 (58) J2-05B
11 (57) J2-06A
10 (56) J2-06B
9 (69) J2-06C
8 (68) J2-07A
7 (67) J2-07C
6 (66) J2-08A
5 (65) J2-08B
4 (63) J2-08C
3 (62) J2-09B
2 (61) J2-09C
1 (55) J2-10A
0 (8) J2-10B
79B 59C 20A 30E 80A 131B
BT.T.BUS.+
15 (12) J2-17C
14 (34) J2-18A
13 (33) J2-18B
12 (31) J2-18C
11 (30) J2-19B
10 (29) J2-19C
9 (14) J2-20A
8 (13) J2-20B
7 (40) J2-21A
6 (39) J2-21B
5 (38) J2-21C
4 (37) J2-22A
3 (36) J2-22C
2 (35) J2-23A
1 (28) J2-23B
0 (11) J2-23C
68D FP.CK.CPU.DP + J2-31A
(325) J2-31C
129B 80D DP.F1+ (190) J2-03A
129B 80D DP.F2+ (191) J2-02C
109B 80E DP.O+ (196) J2-03B
109B 120B 80E 70C DP.E+ (101) J2-03C
109B 80D DP.OVFL+ (197) J2-01C
109B 80D DP.COUT+ (173) J2-02A
29C 137D CK.CPU4.LED.BP+ (231) J2-01A
99D 20D DP.SWCH.RREG- (313) J2-01B
39A 40A 50A 60B 80D 100E
DP.R.BUS +
15 (7) J2-11A
14 (21) J2-11B
13 (20) J2-11C
12 (42) J2-12A
11 (19) J2-12C
10 (18) J2-13A
9 (10) J2-13B
8 (25) J2-13C
7 (24) J2-14B
6 (23) J2-14C
5 (22) J2-15A
4 (45) J2-15B
3 (44) J2-16A
2 (43) J2-16B
1 (41) J2-16C
0 (17) J2-17A
79C 69B 10A 30C
DP.U.BUS +
15 (117) J2-24B
14 (116) J2-24C
13 (115) J2-25A
12 (114) J2-25B
11 (113) J2-26A
10 (112) J2-26B
9 (119) J2-26C
8 (118) J2-27A
7 (159) J2-27C
6 (158) J2-28A
5 (157) J2-28B
4 (156) J2-28C
3 (155) J2-29B
2 (154) J2-29C
1 (153) J2-30A
0 (152) J2-30B
-1158
74S51
U0105
-1275
74S260
U0808
+5
.1 C3 - C20 .1
.1 C22 - C30 .1
.1 C32
.1 C33
+5
33 C1
33 C2
33 C21
33 C31
DP 14
DATA PATH-A900
FRONT PLANE & SPARES
HEWLETT PACKARD
12202-60001
D-12202-60001-64

DP14

Chapter 5
Memory Address Creation and Cache Control Card

5.1 Introduction

This chapter of the manual covers Memory Address Creation and the Cache (CA) Control card. The chapter is divided into two main parts: block diagram description and theory of operation.

To understand the operation of this microprogrammed computer, please refer to the HP 92049A RTE Microprogramming Package Reference Manual, Part No. 92049-90001.

5.2 Block Description

The circuitry for memory address creation logic circuitry is implemented on the cache control card which also contains the cache memory system. Figure 5-1 is a block diagram of the cache control card which is shown in Figure 5-2. The main functional blocks of this card are the following:

Data Store RAM with Cache, VCP, Boot, and Scratch Memory
TAG Store
Memory Address Data Path Registers
Map-Set Select Registers
Memory Address Adder
TAG Store and Modified Bit

A general description of operation is first given in the paragraphs under subheading 5.2 and their logical operations (theory of operation) are provided in the paragraphs under subheading 5.3.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

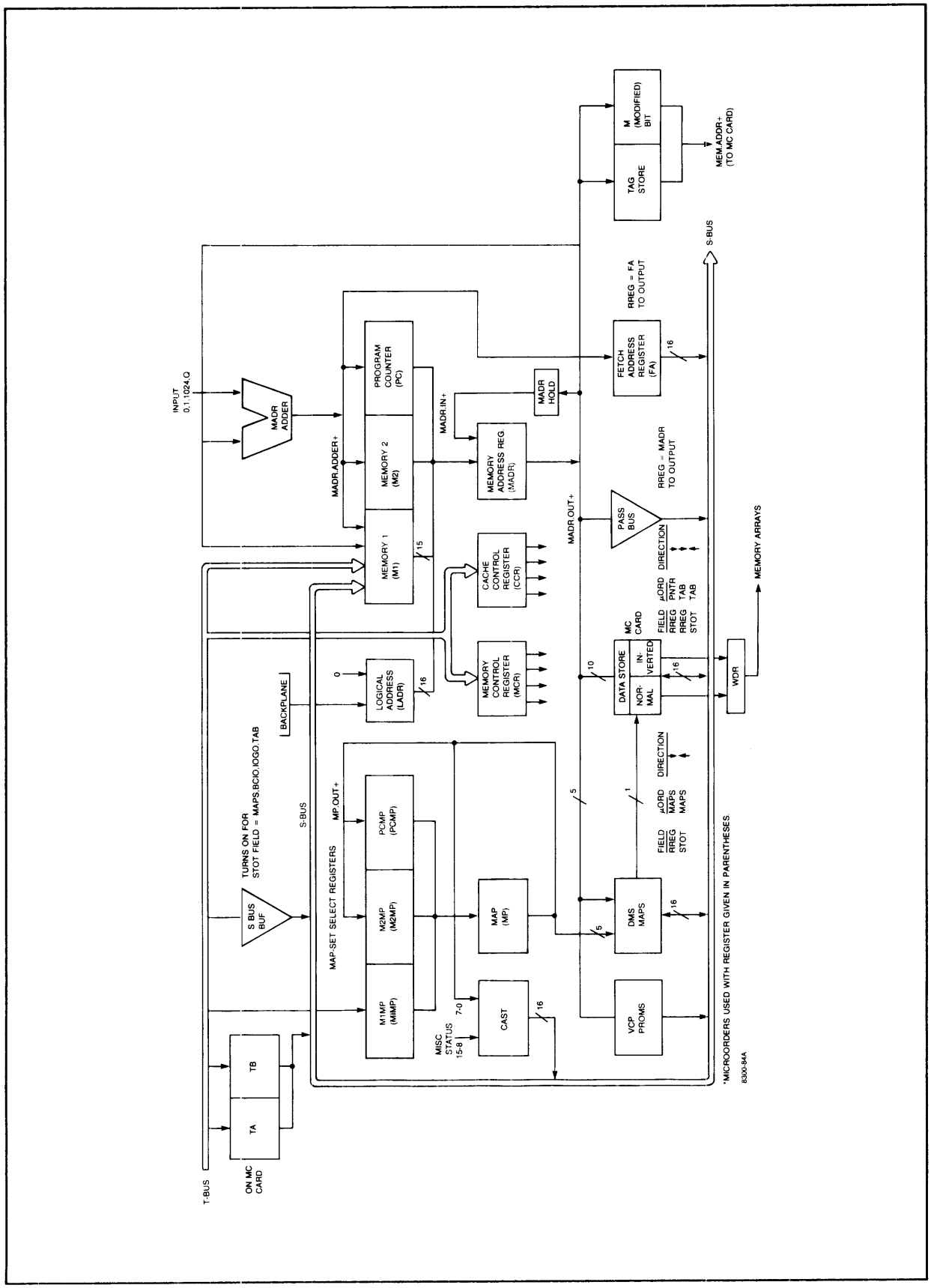


Figure 5-1. Cache Control Card Functional Block Diagram

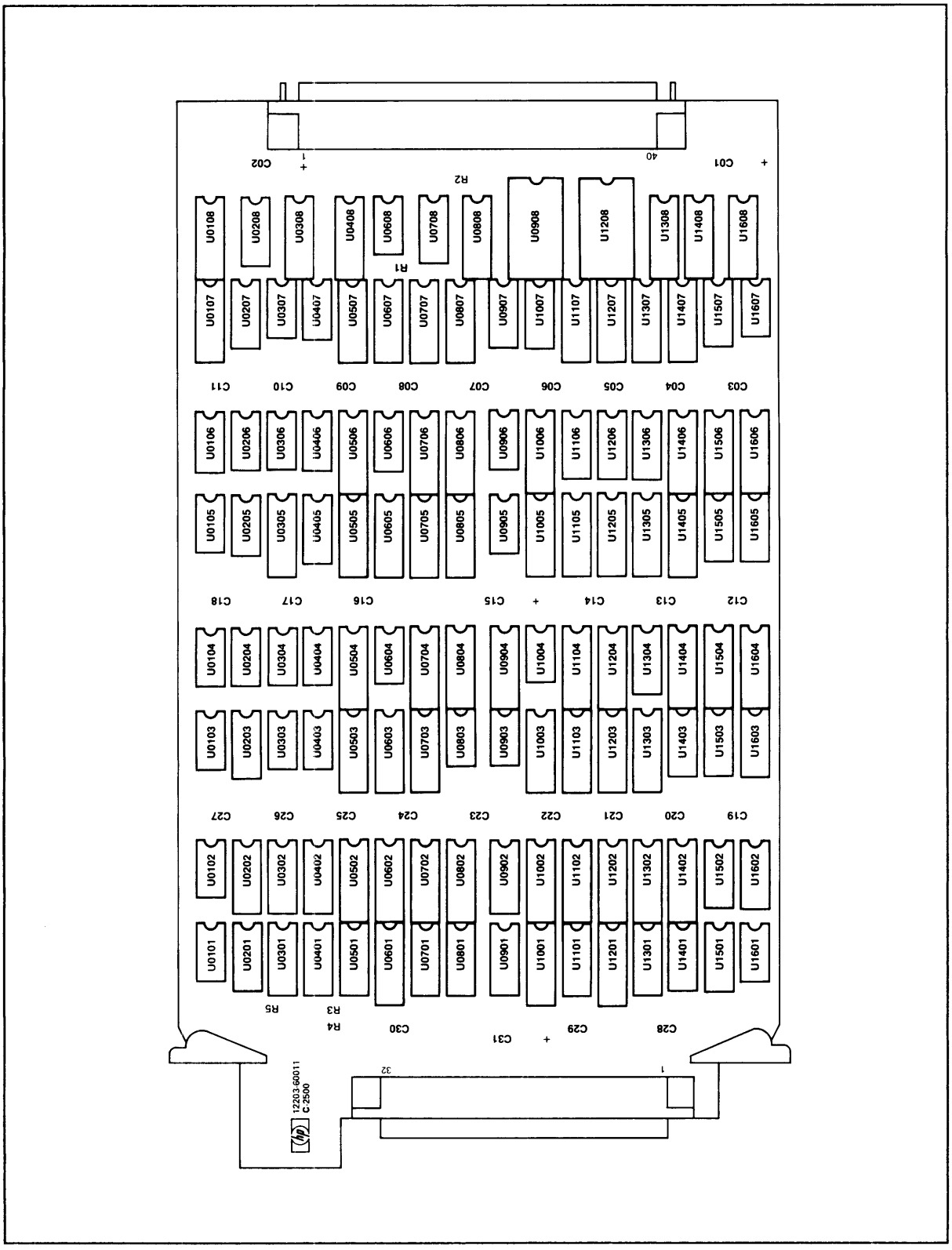


Figure 5-2. Cache Control Card (12203-60011)

5.2.1 Memory Address Creation

Address creation is quite important to the microprogrammer and is discussed from the microprogrammer's point of view in the HP92049A RTE Microprogramming Package Reference Manual. The following description supplements the microprogramming manual information.

5.2.1.1 Logical Address Registers

To the microprogrammer, it appears there are only three address sources: M1, M2, and PC. In reality, there are five sources. The two additional sources are the MADR HOLD buffer and the I/O Address from the backplane.

MADR HOLD (the first additional logical address source) is a buffer to keep the current MADR address while MADR is not updated for some reason; e.g., the address sources may not be correct. Because MADR is always clocked (gated clock signals are not permitted) the only way the present value can be saved is to reload it with a buffered version of its output from MADR HOLD.

The MADR HOLD buffer has several uses. One use is to keep the present address during cache fault processing. When it is determined that the cache has missed and that fault handling is going to be necessary, the logical address latches are already updated with their new values. Therefore, MADR HOLD keeps the old value for use in the next cycle.

A second use for the MADR HOLD buffer is for a JTAB operation that is A/B addressable. The A- or B-Register might still be updated from the previous macroinstruction. An example of this is LDB executed in the A-Register. The B-Register will be updated at the end of the cycle that is also reading the instruction from the B-Register. To get the correct answer, the fetch needs to be delayed one cycle, but the address latches might already be updated so the address comes from MADR HOLD.

A third use for the MADR HOLD buffer serves another function in transforming the cache from a 2k x 16 cache to a 1k x 32 cache for faster fault handling. This is covered in the Data Store paragraph in the block diagram description subsection and in the theory of operation subsection.

A fourth use for the MADR HOLD buffer is to hold the current address when the CPU freezes on a write request to the cache due to the following: the Write Data Register (WDR) is not free, and the addressed location is not in the cache (refer to the explanation of the WDR under the subsection Cache Fault Handling). To ensure proper execution of the write, the CPU remains frozen and MADR HOLD keeps the address until one of two conditions comes true: 1. The request hits the cache and thus WDR is not needed, or 2. The WDR becomes free.

The I/O address from the backplane (the second additional logical address source), is used for all DMA accesses and for reading the select code for IAK operations. The I/O address is the default value for the MEM field; i.e., when NOP is coded. This choice is invisible to the microcoder, but makes IAK operations easier.

Of the five logical address sources, only MADR HOLD and M1 are allowed to contain indirect addresses. By definition of the backplane, the address bus cannot be indirect since it does not have a bit 15. Both M2 and PC must have the address resolved before being loaded. This does not really present any problem since even M1 seldom has an indirect address in it. If an instruction has a DEF following it, then RREG/PNTR is used following MEM/PCPC to resolve to a direct address. When the CPU unfreezes, a fully resolved address exists in M1. If PNTR is not coded, then M1 is not loaded. M1 can only be loaded with a direct address from the data path (STOT/M1). The only way M1 can get an indirect address is through MRG address creation on the JTAB line. RREG/PNTR is used to resolve these to direct addresses before any TAB read or write can be done.

5.2.1.2 Map-Set Select Latches

Along with the three map-set select latches described in the microprogramming manual, there are also HOLD and LIO versions. The MP HOLD buffer has the same use as the MADR HOLD buffer. The LIO map set select latch is used to receive the Address Extension Bus (SC+ 5-0) (same as the L-Series). In the case of DMA self-configuration, this latch is forced to zero.

The format of the map-set select latch is as follows:

bit 7 - CDS enable (1 = Relocation allowed)
bit 6 - Boot Memory enable (1 = Access boot memory)
bit 5 - A/B Addressability enable (0 = A/B addressing allowed)
bits 4-0 - Map set select

Bit 0 may be forced to one if CDS (bit 7) is enabled. This is covered under Code and Data Separation.

5.2.1.3 Address Select

The decision for address selection is based not only upon the MEM field, but also upon DMA requests, cache misses, indirect addressing, and CDS relocations. Fault handling has the highest (first) priority since some faults are critical to processor operation. An example of this is a "write miss". Since the cache is written to before it is known whether or not it will hit, the Write Data Register (WDR) is first loaded with the old value of the cache location. If the cache does indeed miss, then this is the data to be written back to main memory. To do anything but handle that fault would mean loss of data. The specific loading of the WDR is covered in the paragraph on Fault Handling under the Cache Memory subsection.

The next highest (second) priority for address selection is a DMA request. Note that if DMA is selected, then the present MEM field is not used. If the present cycle in the cache were for the CPU and were to hit, then the CPU must not be frozen at the end of this microcycle. (Otherwise, it would not clock in the data read.) However, if the CPU gets a clock, then the MEM field gets updated. Because of this, in many cases an "old" copy of the MEM field must be kept.

The next highest (third) priority is CDS relocation. This is a higher priority than indirects so that an "indirect-address-to-base-page" is first relocated to the stack and then the indirection is followed. Naturally, indirection is the next highest (fourth) priority. In the indirect case, the next address comes from the M1 register since all indirects are resolved through M1. CDS relocation can occur through any address latch, but usually it will occur in M1 along with indirect resolution.

5.2.1.4 JTAB Address Creation and Selection

If JTAB is in the MEM field (or JTDI which is also a JTAB but temporarily disables macro-interrupts) and the present cycle in the cache is on behalf of the CPU (vs. DMA), then the access in the cache is assumed to be a macroinstruction fetch and a JTAB address creation is done with it. The address creation logic is mostly centered around creating MRG instruction operand addresses. The format of an MRG type instruction is:

bit 15 - indirect (1 = indirect address)
bits 14-11 - MRG opcode
bit 10 - base/current page (1 = current page)
bits 9-0 - page offset

On a JTAB, the MRG hardware always creates an MRG address into M1. Note that if the instruction were not an MRG type, then this is a completely incorrect address. However, if the macroinstruction was not an MRG, then M1 is not used as an address source and so it does not make any difference. The MRG address creation is done by taking bits 9-0 from the SBUS; i.e., from the macroinstruction to be read and bits 14-10 from the address of that macroinstruction; i.e., MADR. If the base/current page bit is zero, then bits 14-10 are forced to zero; i.e., base page.

The JTAB in the MEM field is also translated into either an M1M1 type request if the macroinstruction is of the MRG type or, otherwise, into a PCPC type request. If the macroinstruction does not have a DEF following it, then TAB or PNTR is not be coded in the RREG field of the first microinstruction since this causes cache control logic to chase the "indirects" with unknown results.

5.2.1.5 Address Latch Loading

The logical address latches are incremented by using a 15-bit adder with one of its inputs as MADR. Normally the value added is just a one, thus incrementing the present address. However, the NINC specials can stop this increment. SP0/PINC can also stop the "increment of one" and substitute an increment of "2exp10"; i.e., increment the page number. In an CDS relocation, the Q-Register can be substituted for either the "increment by one" or "2exp10" (refer to the paragraph on Code and Data Separation).

Both M2 and PC logical address latches can only be loaded from the MADR ADDER. M2 is loaded on M1M2 or M2M2 in the MEM field. PC is loaded when PCPC or M1PC is in the MEM field, but also when LDPC is in the SP0 field. This last case is used during macro JMP instructions. M1 is loaded from the M1 MUX which has four address sources:

a. MADR ADDER for M1M1 type stores or for CDS relocations.

b. TBUS for STOT/M1 stores into M1 (bit 15 is forced to zero).

c. SBUS for indirects and all RREG/PNTR operations.

d. A special combination of MADR and SBUS used for MRG address creation.

The page bits (14-10) can be forced to zero in the case of an MRG base-page address.

5.2.1.6 Indirect Addresses

The cache will automatically go to indirect addresses if RREG/PNTR is coded in the present microinstruction. A read is started from cache and if the data read has bit 15 = 0, a freeze or extra cycles will not occur. If bit 15 = 1 (indirect), then the value read is used as an address for another read. The CPU is frozen and the process continues until a direct (bit 15 = 0) address is read. RREG and M1 will both have the direct address when the process finishes.

5.2.1.7 Code and Data Separation (CDS)

If CDS is enabled (bit 7 of map set select) and if MADR bits 14-10 are zero, then the Q-Register is substituted for the normal increment through MADR ADDER, and M1 is loaded with the relocated value. This is higher priority than indirection. Normally, base page addresses are resolved in M1 and thus M2 and PC will seldom have base page addresses, whereas indirect addresses are only allowed in M1.

If the present access is an MRG created address in M1, then the map-set select bit 0 is forced to 1; i.e., to odd page sets. This is where code map sets are to reside in the CDS mode. After indirection or an CDS relocation this bit goes back to normal; (zero for the data map set). To allow operation of JMP indirects or JLY type instructions, SPO/CODE must be coded before the JTAB line. This forces the last access back into the code space.

5.2.1.8 DMA (Direct Memory Access)

DMA can take over whenever the cache is not in a HOLD cycle. A/B addressability and CDS are disabled for DMA. Thus, except for faults or writes when main memory is busy, DMA requests complete in just one cache cycle. DMA handshakes for the I/O bus are covered in the Backplane Chapter.

5.2.1.9 Boot Memory

To avoid having the VCP running instructions differently than normal macrocode, the VCP code is moved into part of the cache memory RAMs. This allows the VCP to run at maximum speed. Likewise, since the VCP needs a base page in which to have data to write to, this is also part of the cache memory RAMs. The actual cache memory takes up the last part of the cache.

The VCP data space can also be used in normal operation as a scratch memory space with use of the SPO/BOOT special. This special and the BOOT enable bit of the map set select register (MP) set the upper two bits that address the actual cache memory RAMs. This fixup is done just before the cache memory's version of MADR called CDADR (Cache Data ADdress Register). (Refer to the paragraph on Cache Memory for information about the addresses and uses of the parts of the data store RAMs.)

5.2.1.10 RREG/BPRM Addressing Function

The RREG/BPRM moves the VCP code from the PROMs into the VCP part of the cache data-store RAMs. Since the PROM has a 300 nanosecond access time, the same address needs to be fed to the PROM for three microcycles. Either a MEM/M1M2 function or MEM/M1M1 with SPO/NINC is useful for keeping the address constant. Additional addressing functions are covered in the microprogramming manual.

5.2.2 Cache Memory

The cache memory system consists of the DMS RAMs, the TAG store, and associated circuitry on the CA board plus the cache data store with all "in" and "out" buffers on the MC board.

Conceptually to the micromachine, a cache memory appears as a very fast main memory. The principle of cache memory operation is that it stores small pieces of main memory (called blocks which are always a power-of-2 words in size) in a local very high-speed RAM. To keep track of these blocks, the cache keeps an identifier for each called a "TAG". The TAGs are the main-memory address of each block.

This is a "set associative" cache; i.e., each cache main-memory block is stored in a separate "frame", and the frames are distinguished by their lower addresses. Thus, any two blocks can be in the cache as long as their lower addresses are not the same. Thus, the TAG does not need lower address bits due to the frame identification.

During a cache access, the cache uses the lower-address bits to select a cache frame. The TAG from this frame is compared to the upper-address bits to see if they match. If so, then the data in that frame is what is desired. If the TAG does not compare with the upper-address bits, then a "miss" has occurred. To keep the CPU from knowing something wrong has happened, the CPU is frozen. The cache then takes the TAG and the lower address bits and writes its present block back into main memory. It then uses the total address from the CPU to read a new block from main memory. This block is then stored in the cache with the TAG set to the new upper-address bits.

The A900 processor has the following features in its cache operation:

a. DMS mapping occurs at the same time that the frame is being read because only the lowest DMS bit (physical address 10 is used to select the cache frame.

b. Two frames are read at the same time using bit 10 to select between the two.

c. If a block is not changed in cache, the write-back is skipped due to a check bit that monitors for changes to the block.

d. Since the cache is the only user of main memory, the read for the next block is done before the write-back of the previous one. This allows the faulting operation to proceed immediately.

e. To avoid lost cycles, the requested cache read or write operation is done on the last fault processing cycle. Reads are handled normally. For writes the main memory data is merged with the CPU data (or DMA data for DMA cycles.)

f. There is only one possible frame for any given address. For read cycles the data from the present frame goes immediately to the CPU. If the cache misses, then the CPU is frozen before it could use the incorrect data. This gives the data to the CPU by mid-cycle. As a result, the IJT and AJT lookups can be done before the end of the microcycle.

g. The write operation is also done before hit/miss is known. The cache first reads out the data by mid-cycle, stores it in the Write Data Register (WDR) to main memory, and then does the write (refer to the Data Store paragraph.

h. To improve fault handling time, the cache changes from a 2k x 16 cache to a 1k x 32 cache (refer to the Data Store paragraph).

5.2.2.1 DMS (Dynamic Mapping System)

The DMS RAMs are 1k x 4 45-nanosecond RAMs except for the lowest bit which is in a 1k x 1 20-nanosecond RAM. This last RAM is faster since it is used as a "select bit" for selecting between even and odd physical pages of TAG stores and for selecting between the two parts of the data store.

The DMS RAMs are written from the CA version of the SBUS when STOT/MAPS is coded in the previous line of microcode. The DMS RAMs are read onto the CA version of the SBUS when RREG/MAPS is in this line of microcode.

5.2.2.2 Tag Store

The Tag store RAMs keep track of the physical-page address in main memory of each block in the cache data store. Since each block in the data store is two words, there is one tag for every two words. For speed reasons, the tag store is implemented as two sets of tag stores, one for even physical pages and one for odd physical pages. The tag store includes physical address bits 23-11 These bits are written during the second cycle of cache fault handling. The CPU has no control over when the tag store is written, just the cache state machine. The "select" bit is written with a logic "1" whenever a write cycle occurs and is written with the high-true "write" signal during the second cycle of a cache fault. The first case is used to record that the block in the data store has been written to, and the second case is used when a block is first being brought into the cache from main memory. Since write merging is done on a cache write fault, the data store block may get modified just as it is being loaded into the cache.

5.2.2.3 Tag Compare

The tag compare logic compares bits 23-11 from the DMS and tag store RAMs. If the physical address desired (DMS) matches the physical address in the cache (tag), then a "hit" has occurred and the operation (read or write) can continue. If the addresses do not match, then a "miss" has occurred and the block in the cache data store needs to be replaced with the block at the physical address desired. However, if the presently loaded block has not been modified, then it does not need to be written back since the main memory copy is the same. Thus, if "miss" and if "select" bit are set, then write block to tag store address. Then read block in from DMS address. Errors are discussed in the paragraphs on Fault Processing.

5.2.2.4 Data Store

The cache data store has several unusual features. First, only one fourth of the actual RAM space is used for the normal data store. Half of the space is for the VCP code and the other quarter can be used as VCP data space or as "scratch pad" space for the CPU when not in VCP mode. The cache data store is located on the Memory Controller Card. Refer to the subsection Cache Data Store in Chapter 6 for the theory of operation.

To improve fault handling time, the cache can change from a 2k x 16 cache to a 1k x 32 cache. This is done by storing data on one side "inverted" relative to the other side. The "normal" side has even addresses of even physical pages and odd addresses of odd physical pages. The "inverted" side has even addresses of odd physical pages and odd addresses of even physical pages.

During normal cache accesses, the lowest address bits of both parts of the cache are the same; i.e., the logical address being accessed. Selection between the two sides is based on physical address bit 10; thus the cache looks like a 2k x 16 cache. If a fault occurs, then the side which did not have the addressed word flips its lowest bit. That side will then access the other word of the block; thus the cache appears to be 32-bits wide. Since the side being addressed does not "move" during this change, no change needs to be made in the reading or writing logic to handle this switch. During the last cycle of a read fault, the desired data can be sent on to the CPU or to an I/O device. During the last cycle of a write fault, the write data can be merged with the data coming from main memory without losing a cycle.

CAUTION

Note that the words of odd physical pages are backwards from that of even physical pages. Since the cache is the only requestor of main memory, this is only of interest in logic analysis of the main memory data bus.

Cache write cycles are handled in an unusual manner to obtain a faster cache. Instead of using the "textbook" method of using the hit/miss signal to control the write strobes, the cache first reads the block, stores it in the Write Data Register (WDR) for main memory, and then writes to the cache; regardless of "hit" or "miss". If the cache hits, the operation is normal. However, if the cache misses, then the write was to an incorrect block. Since a copy of that word was made into the WDR, and in the event of a "miss", that block needed to be replaced anyway, no harm has been done. However, this does mean that writes cannot be allowed to proceed unless the WDR is free; i.e., the main memory is not busy.

5.2.2.5 TA and TB Registers

In order for the cache to chase indirects with the CPU frozen, it must have access to the A- and B-Registers. These are kept in TA and TB on the MC card. Accesses to memory addresses zero or one, with A/B addressability enabled, will go to TA and TB, respectively. All accesses to addresses "zero" or "one" stop the cache from faulting. This is to avoid the large conflicts that would occur between "A" and "B" and the first two words on even physical pages. On direct writes to "A" or "B", the cache also has to update the CPU versions of the A- and B-Registers. For this reason, no other write can be allowed to the primary register files in the same microinstruction line as a STOT/TAB.

Likewise, any store into the CPU versions of the A- and B-Registers is reflected in the cache versions. This store is pipelined like all CPU stores, but with one big difference: the cache "A" and "B" stores occur in the first CPU access to the cache in rank-two. For direct reads or writes to the cache, this is exactly as the CPU gets updated. For indirects, the store seems to happen after the first level of indirection; i.e., during rank-two. This difference is used to allow a LDB in "A" to be executed correctly by adding a fake cycle into the cache to allow "B" to be updated "before" the fetch occurs.

5.2.2.6 Fault Processing

Cache faults are handled with three additional states; i.e., a fault access takes four microcycle times versus one for a "hit". To improve the effective access time and because the cache is the only requestor to main memory, the main memory read cycle is done before the write.

Half of the block to be written back to main memory is read into the Write Data Register (WDR) during the first cache cycle (the one that faulted) and the other half is read into the WDR in the second cache cycle (first fault cycle). On the second fault cycle, the tag store is updated with the DMS value, and on the third fault cycle (fourth overall) the data from main memory is written into the cache data store. If main memory has a single-bit error, then the cache does not get data until another cycle later. However, the memory controller requests a freeze of the cache and I/O bus for this case and so neither sees the difference from a normal fault.

5.3 Theory of Operation

The A900 Cache Control card theory of operation is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 5-1 and the schematics at the end of this section of the manual. The schematic pages are referred to by a two letter card acronym followed by a page number; e.g., the schematics the cache memory card are CA1, CA2, etc.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U307 (CA118C) refers to part U0307 on the cache control card in row 3/column 7, which is shown on schematic page CA11 at horizontal location 8 and vertical location C.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

5.3.1 Memory Address Creation

Memory Address Creation consists of all the parts of the CA board which are involved in producing an address in the Memory ADdress Register (MADR/CDADR). This includes the DMA request arbitration, CPU address selection, address creation (MRG address), address incrementing, freeze logic, error checking, and main state flow.

5.3.1.1 Logical Address Latches

The three logical address sources for CPU are the M1, M2 and PC logical address latches:

M1 - U1404 (CA17A) and U1406 (CA17B)
M2 - U1504 (CA22B) and U1506 (CA22C)
PC - U1604 (CA22D) and U1606 (CA22E).

Along with the three CPU sources, there are two other sources for the CA.MADR.IN+ bus:

MADR HOLD - U1204 (CA24B) and U0108 (CA24C)
LADR - U1006 (CA36B) and U0808 (CA36C), I/O address of the type backplane.

The selection of which address will be used for the next cache cycle is described in the Address Select subsection which follows. The algorithm for deciding when and from where to load the address latches is described under Address Latch Loading, below.

The cache Memory ADdress Register (MADR) and the Cache Data store ADdress Register (CDADR) are loaded on every cache cycle. MADR is contained in chips U1104 (CA26B) and U0107 (CA26C). MADR is the source of address for chips on the CA board. This includes such chips of the cache as the DMS RAMs, TAG Store RAMs and the VCP PROMs. CDADR is the address source for the cache data store RAMs, which are contained on the MC card. All of these chips, except for the VCP PROMs, are described in the Cache Memory subsection, and the VCP PROMs are described under Boot Memory.

Both MADR and CDADR contain the same address, but are separated for load-speed reasons. Because the data store RAMs only need the lower ten bits of the logical address, CDADR does not contain addresses 15-10.

Since the cache data store RAMs are also used for keeping the VCP code and VCP data, two additional upper-address bits are needed: BP.EXT.ADDR1+ and BP.EXT.ADDR0+. These two bits are generated by the gates U0304 (CA24C), U0306 (CA25C), and U0306 (CA25C). The small figure to the right of CDADR (CA28D) shows what the extended addresses bits should be for various boot memory logical addresses.

The lowest address bit for the "normal" and "inverted" halves of the cache data store can be different. In non-HOLD mode, the lower two bits are always the same; i.e., logical address 0. In HOLD mode, the lower address bits come from the signals CA.DMS10+ and CA.PAGE.ODD-. This does the conversion of the cache from 2k x 16 into 1k x 32. The 2:1 MUX U0208 (CA24D) does this selection. In addition, it also selects and HOLDs the signal which determines whether a request is on behalf of the CPU or DMA -- CA.DMA.CYCLE+. The input CA.TRUE.DMA.REQ+ comes from the PLA U0305 (CA115C). CA.TRUE.DMA.REQ+ is a gated version of CA.DMA.REQ+ (a held version of LBP.MEMGO-) AND "not a DMA cycle". This fixes the problem caused by CA.DMA.REQ+ remaining asserted for too long.

5.3.1.2 Map Set Select Latches

Associated with each logical address latch, there is a map-set select latch:

1. M1MP U0706 (CA32B) for M1,
2. MP HOLD U0507 (CA32C) for MADR HOLD,
3. M2MP U0506 (CA32D) for M2,
4. PCMP U0807 (CA32D) for PC, and
5. LSC U0607 (CA34D) for the I/O address LADR.

MP HOLD, M2MP, and PCMP are "updated" whenever their respective logical address latch is updated. M1MP is loaded whenever M1MP is coded in the STOT field. LSC is updated with LBP.SC4-0+ masked by LBP.SC5+ (self-configure bit) in the five AND gates U0604 (CA34D) and U0608 (CA34D) whenever the I/O backplane is not BUSY; i.e., whenever a DMA request is not in process.

5.3.1.3 Address Select

The priority of address selection is: 1. HOLD, 2. DMA request, 3. CDS relocation, 4. Indirection, and 5. the MEM field.

The logic which implements address select is mostly contained on schematic sheet CA11. The signals that directly select address latches and their associated map-set select latches are the following:

CA.IO.EN- from U0105 (CA118B) selects LADR and LSC
CA.PC.EN- from U0307 (CA118C) selects PC and PCMP
CA.M2.EN- from U0105 (CA118C) selects M2 and M2MP
CA.M1.EN- from U0204 (CA118D) selects M1 and M1MP

HOLDs for fault handling are highest priority since the signal CA.NO.HOLDS+ must be true for any of the other latches to be selected.

CA.NO.HOLDS+ is only false in three situations:

a. The present true access to the cache missed (NOT CA.HIT+).

b. A CPU fetch was to the A- or B-Address Registers.

c. A write was requested, but the Write Data Register (WDR) to main memory was busy.

The first case causes a fault cycle to begin which consists of three states:

a. CA.F1+, CA.F2+, and CA.F3+. CA.HIT+ will also be false for the first two of these fault processing cycles.

b. Check for a possible pipelining side-effect. If a LDB macroinstruction is in the A-Register and if the program counter were pointing to "A", then the storing of "B" in the emulation code for LDB would happen in the same cycle as the fetch was occurring from "B". The data for the LDB instruction would not be what was fetched. To solve this problem, a fetch from "A" or "B" causes a one cycle pause (HOLD) to allow the pipeline to clear out.

c. The problem is caused by the cache doing a write before it has time to check for CA.HIT+.

In (c) above, since the half of the cache block which is about to be written to has been loaded into the WDR mid-cycle, the write can occur during the second half of the cycle. However, the WDR must either be free for this to occur or it must not be needed. After a cycle has checked the cache for a "hit" (CA.WRITE.HIT+ is asserted; i.e., the write did "hit"), then the next cycle can proceed with the write.

The cache holds and misses PLA U0504 (CA143D) generates the last two cases. Figure 5-3 shows the code for this PLA.

This PLA also generates the additional "misses" during fault processing (states F1 and F2) and forces the misses required to load up the cache during power up; i.e., for all states except for the final fault handling state, F3.

For the other priorities, refer to the code of the Address Selection PLA, U0305 (CA115C), which is shown in Figure 5-4.

```
*
*
*                C     C B                    C
*       C C C A        A P        B B        A
*       A A A . B      . .        P P      C .
*       . . . B P      H T        . .      A F
*       C M D O . C O R           U U      . O
*       P O M O M A L U           I I      W R
*       U D A T E . D E           R R    C R C
*       . E . . M A . .           . .    A T E
*       W . W C . B C W C C C R R        . . .
*       R L R Y B . Y R A A A E E        H H M
*       I O I C U H C I . . . G G        0 0 I
*       T A T L S I L T F F F 1 1        L L S
*       E D E E Y T E E 1 2 3 4 3        D D S
*       - + - + + - - + + + + + +        - + +
*
*       0 0 0 0 0 0 0 0 1 1 1 1 0        1 1 1
*PIN:   8 7 6 5 4 3 2 1 9 8 7 1 9        6 5 3
*
 SENSE:                                  L H H
*                           B B B B B    B B B
*ROW    7 6 5 4 3 2 1 0 9 8 7 1 0        6 5 3
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    L - - - - - - - L - - - - -      A A .   WDR BUSY & NEEDED
   1    - - L - - - - - L - - - - -      A A .     "    "       "
   2    - - - - - - - - - H - - - -      A . A   FAULT STATE 1
   3    - - - - - - - - - - H - - -      A . A   FAULT STATE 2
   4    - H - - - - - - - - - L - -      . . A   DON'T FAULT AGAIN
   5    - - - - - - L H - - - - H H      A . .   FETCH FROM A/B
  D3    - - - - - - - - - - - - - -              ^
  D5    - - - - - - - - - - - - - -        ^
  D6    - - - - - - - - - - - - - -      ^
*
```

Figure 5-3. Cache Holds and Misses PLA (U0504) Code

```
*                                                C
*                                                A           C
*                                      C C C     .           A
*       C   B B B     C A A A   T                .
*       A   P P P     A . . .   R                S C
*       . C . . .   C . D D D   U                . A
*       D A U U U   A P E E E   E C C C C B .
*       M . I I I   . N L L L   . A A A A U J
*       A R R R R   D T A A A   D . . . . S T
*       . R . . .   M R Y Y Y   M T T T T . A
*       C R R R R C A . . . .   A R R R R A B
*       Y . E E E A . R M M M   . Y Y Y Y L .
*       C H G G G . R R E E E   R . . . . L S
*       L I 1 1 1 F E E M M M   E I P M M O E
*       E T 4 3 2 3 Q G 2 1 0   Q O C 2 1 W L
*       - - + + + + + - + + +   + + + + - + -
*       0 0 0 0 0 0 0 0 1 1 1   1 1 1 1 1 1 0
*PIN:   8 7 6 5 4 3 2 1 9 8 7   6 5 4 3 2 1 9
 SENSE:                        H H H H L H L
*                         B B B   B B B B B B B
*ROW    7 6 5 4 3 2 1 0 9 8 7   6 5 4 3 2 1 0
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  0     H H L L L - L - - - -   . A . . . . .   MEM/NOP -> IO       no
  1     H H L L H - L - - - -   . . A . . . .   MEM/PCPC -> PC      DMA
  2     H H L H L - L - - - -   . . . A . . .   MEM/M2M2 -> M2      req.
  3     H H L H H - L - - - -   . . . . A . .   MEM/M1M1 -> M1       "
  4     H H H L - - L - - - -   . . . . A . .   MEM/M1XX -> M1       "
  5     H H H H - - L - - - -   . . A . . . A   MEM/JTAB -> PC       "
  6     L - - - - L - - L L L   . A . . . . .   DELAY/NOP -> IO     DMA
  7     L - - - - L - - L L H   . . A . . . .   DELAY/PCPC -> PC    req.
  8     L - - - - L - - L H L   . . . A . . .   DELAY/M2M2 -> M2    held
  9     L - - - - L - - L H H   . . . . A . .   DELAY/M1M1 -> M1    by
 10     L - - - - L - - H L -   . . . . A . .   DELAY/M1XX -> M1    DMA
 11     H L - - - - L - - - -   . . . . . . .   CDS -> M1 <DELETED>
 12     H - - - - - H - - - -   A A . . . . .   DMA.REQ -> IO
 13     H - - - - - L L - - -   . . . . . A .   PNTR INDIRECT
 14     L - - - - H H - - - -   A A . . . . .   DMA.REQ & F3 -> IO
 15     L - - - - - L - L L L   . A . . . . .   DELAY/NOP -> IO     no
 16     L - - - - - L - L L H   . . A . . . .   DELAY/PCPC -> PC    DMA
 17     L - - - - - L - L H L   . . . A . . .   DELAY/M2M2 -> M2    req.
 18     L - - - - - L - L H H   . . . . A . .   DELAY/M1M1 -> M1    but
 19     L - - - - - L - H L -   . . . . A . .   DELAY/M1MX -> M1    DMA
 20     H L - - - - L - - L H   . . A . . . .   DELAY dest PC -> PC RRR
 21     H L - - - - L - L H L   . . . A . . .   DELAY dest M2 -> M2 & no
 22     H L - - - - L - H L L   . . . A . . .   DELAY dest M2 -> M2 DMA
 23     H L - - - - L - L H H   . . . . A . .   DELAY dest M1 -> M1 REQ
 D0     - - - - - - - - - - -                 ^
 D1     - - - - - - - - - - -               ^
 D2     - - - - - - - - - - -             ^
 D3     - - - - - - - - - - -           ^
 D4     - - - - - - - - - - -         ^
 D5     - - - - - - - - - - -       ^
 D6     - - - - - - - - - - -     ^
```

Figure 5-4. Address Select PLA (U0305) Code

DMA requests are next the (second) highest priority as selected by terms 12 and 14 of the figure. These terms are also the source of the signal CA.TRUE.DMA.REQ+. As a side-effect of how the request is cleared from the DMA request logic term 12 masks the second DMA request in a row. Term 14 overrides 12 in the case of back-to-back DMA write requests in which the first one faulted. Only in this situation are DMA cycles allowed to be back-to-back in the cache. All other terms are held off by CA.DMA.REQ+ except for terms 6-10. These terms are for selecting the appropriate CPU address when a DMA request would be ignored anyway; i.e., if it is presently a DMA cycle in the cache and it isn't state F3. (Note that DMA cycles continue in the cache during a fault because the HOLD signal keeps the present request for the next cycle.) Thus, DMA is always the second highest priority in the cache.

CDS relocation is the next highest (third) priority. Terms 20-23 select the appropriate address source after an CDS relocation. This will be the destination address latch of the present access. That is, CDS causes the destination to be loaded with "source plus Q" and then another access is started with that same latch.

Indirect addresses are the next (fourth) selection priority. Indirects (RREG/PNTR) require testing bit 15 of the address coming back from the cache read. Since this is too far into the cycle to use a PLA to make the decision, the PLA only notes this case by asserting CA.SBUS15.ALLOW+. If it and bit 15 of the SBUS are both true, then the gate U1601 (CA116D) drives CA.PNTR.IND-. This selects the M1 latch and removes selection of the other latches.

If none of the above conditions is true, then the MEM field is the appropriate address source. Terms 0-5 decode the MEM field into the appropriate address latches. Two cases are significant:

1. MEM/NOP is decoded to the I/O address latch (LADR). This allows IAK operations to work easier since the trap cell select code is driven onto the I/O address bus (LBP.AB+) RREG/MADR will then read the select code.

2. JTAB or JTDI in the MEM field imply the read taking place is a macroinstruction fetch. This means either M1 or PC needs to be selected as the next address source.

Because address selection is done before the cycle in which the cache is accessed, DMA interference can cause bad side-effects. If the present cycle is for the CPU and if it hits, then the CPU should be allowed to go ahead at the end of this cycle; i.e., not freeze. This is because the clock is necessary to clock in the data from the cache. If a DMA request had just come in, then address creation must select the DMA address. However, this means the pipeline for address creation for the CPU has just been broken.

If the DMA cycle should hit the cache, then the next address selection should be for the CPU, even though the CPU will be frozen at the end of the cycle because of the DMA cycle. This allows the cache to "catch" up again with the CPU, but requires that the cache stores copies of the old MEM field. But certain MEM field values should not be kept. JTAB or JTDI has many side-effects relating to address creation. These imply that the "present" cycle also be on behalf of the CPU. This again will be explained in the next section, but the important part is that these two requests are turned into M1M1 or PCPC depending upon the macroinstruction read from the cache during the cycle in which JTAB or JTDI was first in the MEM field.

In the case where the previous cycle in the cache was for DMA, the address selection is taken from the delayed version of the MEM field. Terms 6-10 are for when the DMA cycle hit the cache and terms 15-19 are for when the DMA cycle missed the cache and is not followed by another DMA request. The delaying of the MEM field is done in the PLA U0505 (CA122B). Figure 5-5 shows the Delay Memory Field PLA code.

Terms 0-4 of the figure are for copying the present state of CA.DELAY.MEM+ if the present cycle is for DMA. If the present cycle is on behalf of the CPU (NOT CA.DMA.CYCLE-), and is not base relative (NOT CA.CDS.HIT-) and is not indirect (NOT CA.INDIRECT-), then the present MEM cycle is copied; except for JTAB or JTDI. JTAB or JTDI are handled by terms 12 and 13. Term 12 is for the case in which the macroinstruction read is an MRG macroinstruction. In this case, the effective MEM field becomes M1M1. If the macroinstruction is not of the MRG form (term 13), then the effective MEM field is PCPC. Terms 14-17 handle the CDS relocation case -- the effective MEM field becomes the destination of the present MEM field; e.g., M1M2 or M2M2 both become M2M2. Term 11 handles the indirect case. Again, the effective MEM field becomes M1M1.

```
*
*
*                                          C C C
*                                C C C     A A A
*       B B B   C        A A A   . . .
*       P P P   A C      . . .   D D D
*       . . . C . A      D D D   L L L
*       U U U A D .      E E E   Y Y Y
*       I I I . M I      L L L   . . .
*       R R R R A N      A A A   M M M
*       . . . R . D C    Y Y Y   E E E
*       R R R R C I A    . . .   M M M
*       E E E . Y R .    M M M   . . .
*       G G G H C E M    E E E   2 2 2
*       1 1 1 I L C R    M M M   B B B
*       4 3 2 T E T G    2 1 0   2 1 0
*       + + + - - - -    + + +   + + +
*
*       0 0 0 0 0 0 0    1 1 1   1 1 1
*PIN:   8 7 6 5 4 3 2    9 8 7   6 5 4
*
 SENSE:                                  H H H
*                                B B B   B B B
*ROW    7 6 5 4 3 2 1    9 8 7   6 5 4
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - L - -    L L H   . . A   IF DMA, STAY PUT
   1    - - - - L - -    L H L   . A .     "
   2    - - - - L - -    L H H   . A A     "
   3    - - - - L - -    H L L   A . .     "
   4    - - - - L - -    H L H   A . A     "
   5    L L H H H H -    - - -   . . A   IF NOT RRR OR INDIRECT,
   6    L H L H H H -    - - -   . A .     THEN TAKE NEW MEM
   7    L H H H H H -    - - -   . A A     VALUE.
   8    H L L H H H -    - - -   A . .     "
   9    H L H H H H -    - - -   A . A     "
  10    - - - L H - -    - - -   . . .   CDS -> M1M1
  11    - - - - H L -    - - -   . A A   INDIRECT -> M1M1
  12    H H - - H - L    - - -   . A A   JTAB & MRG -> M1M1
  13    H H - - H - H    - - -   . . A   JTAB & NOT MRG -> PCPC
  14    - - - L H - -    - L H   . . A   CDS PCPC/M1PC -> PCPC
  15    - - - L H - -    L H L   . A .   CDS M2M2 -> M2M2
  16    - - - L H - -    H L L   . A .   CDS M1M2 -> M2M2
  17    - - - L H - -    L H H   . A A   CDS M1M1 -> M1M1
  D4    - - - - - - -    - - -       ^
  D5    - - - - - - -    - - -     ^
  D6    - - - - - - -    - - -   ^
*
*
```

Figure 5-5. Delay Memory Field PLA (U0505) Code

5.3.1.4 JTAB Address Creation and Selection

If the present cycle in the cache is for the CPU and if the MEM field has JTAB or JTDI in it, then the cache performs an MRG address creation. The M1 input MUX is forced to the MRG input (0) which selects the page bits (14-10) from MADR and the lower ten bits (9-0) from the SBUS. This is done by the Address Store PLA U0904 (CA122A) (refer to address latch loading, below).

Note that this happens regardless of whether or not the macroinstruction was of the MRG type or not. The address select PLA, U0305 (CA115C) selects PC as the address source. If the macroinstruction turns out to be of the MRG type (CA.MRG-, from gate U1607 (CA112D)), then the PC selection is disabled and M1 is substituted. This happens if CA.JTAB.SEL- is asserted, which is gate U0404 (CA116D). Note that JTAB or JTDI are not allowed as delayed MEM field. Since JTAB and JTDI work on the address selection part of a cycle, they only make sense when the present cycle is a fetch for the CPU.

5.3.1.5 Address Latch Loading

The M1 input MUX selection is done by Address Store PLA U0904 (CA122A). The code for this and JTAB address creation and selection is listed in Figure 5-6. The first two terms are incremented versions of MADR going to M1, with JTAB not asserted. Term 4 is for CDS relocation, which also selects the MADR adder as the M1 input. Terms 5 and 6 select the TBUS as the input if not CDS, PNTR, JTAB or M1/STOT. Term 7 selects the SBUS for handling indirects if PNTR has been coded in the RREG field and no CDS relocation occurred. This gives the loading priority as:

```
CDS           -> ADDER
RREG/PNTR     -> SBUS
MEM/JTAB      -> MADR/SBUS
STOT/M1       -> TBUS
MEM/M1M1      -> ADDER
```

All but the last term are used for deciding when to load the various logical address latches. Since the latches need to be opened at mid-cycle, the PLA cannot be used to decide on certain later arriving signals. These are combined in the gates which follow the PLA. The PC load signal is gated by the signal BP.NO.EXECUTE- in gate U1601 (CA125A). This is because the Instruction Jump Table (IJT) entry for some macroinstructions is not correct (entry points are shared) and has to be stopped.

The only MEM field that is coded on the IJT line is PCPC (for resolving DEFs). BP.NO.EXECUTE- gives signals that the reloading should not occur. At the clock shaping gate U0606 (CA127A) PC also has another loading term added, CA.LDPC.SP0-. This term is asserted during a JMP macroinstruction so that PC gets loaded with an incremented version of the target address of the jump. Likewise, M1 has additional outside store terms of CA.R2.M1.STOT- and CA.PNTR.RREG-. M2 load signals goes directly to the clock shaping gate, U1004 (CA127A).

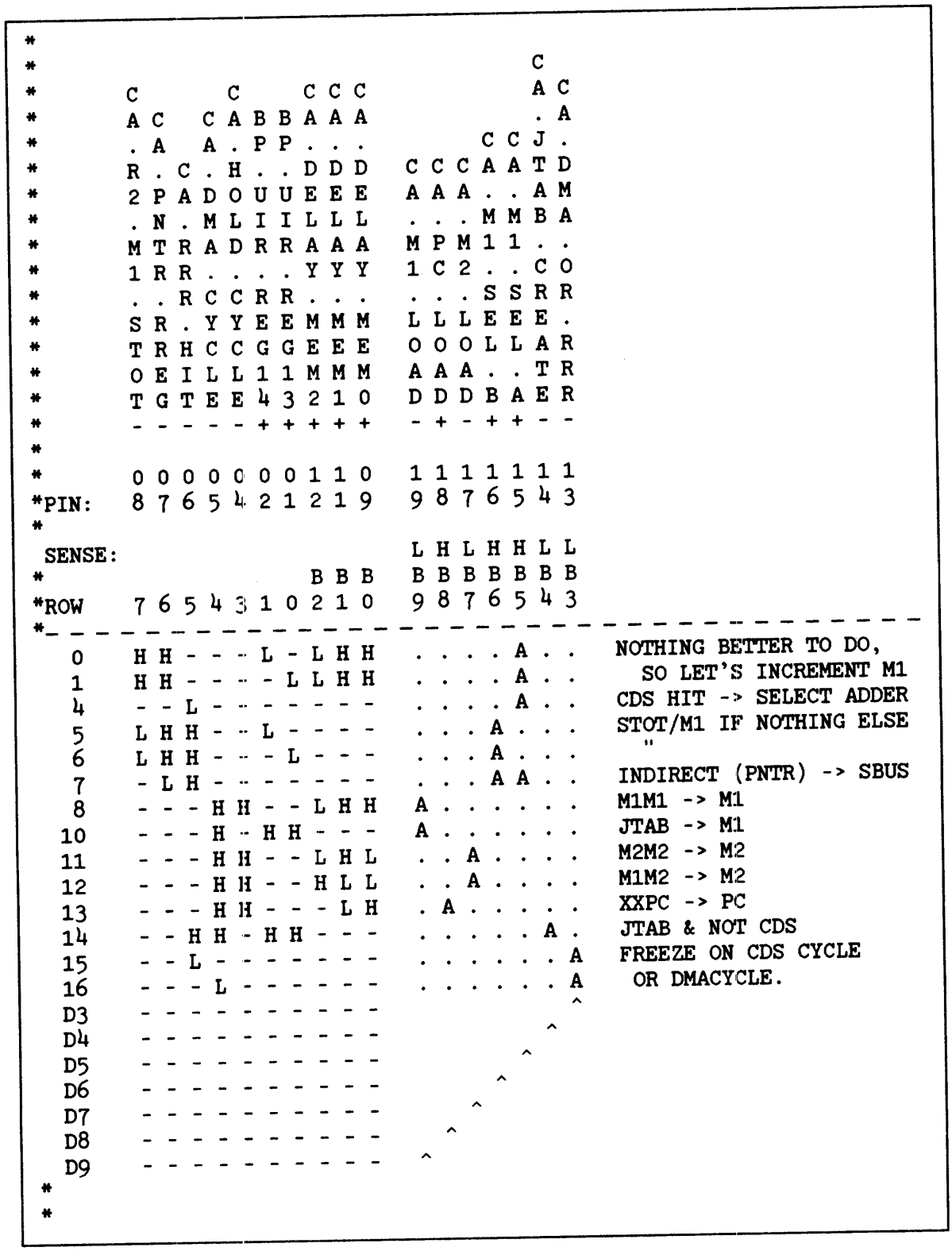


Figure 5-6. Address Store PLA (U0904) Code

CA 123 A

Term 14 in the PLA creates the signal CA.JTAB.CREATE- which is combined with CA.MRG- and BP.S.BUS10+ to produce CA.FORCE.PAGE0. This causes the page of the MRG address created to be forced to base page.

The incrementer for logical addresses, MADR ADDER, is contained in U1602, U1502, U1605, and U1505 (CA11B-D). It normally only adds "1" to the MADR value unless NINC is in SP0 or SP1 or if PINC is in SP0. These are combined in the gate U0205 (CA62A). PINC substitutes a page increment (2exp10) by inverter U0403 (CA62A).

5.3.1.6 Indirect Addressing

Indirection is signaled by RREG/PNTR and SBUS15 = 1. To avoid chasing indirects if the cache should stop, the signals BP.NO.EXECUTE- (ignore this microinstruction) and BP.IND.INT- are combined in U0307 (CA116D) to produce the signal CA.INDIRECT-. This signal causes the CPU to freeze and enables PLA U0705 (CA122E) to count indirects. The code listing for the Indirect Count PLA is given in Figure 5-7.

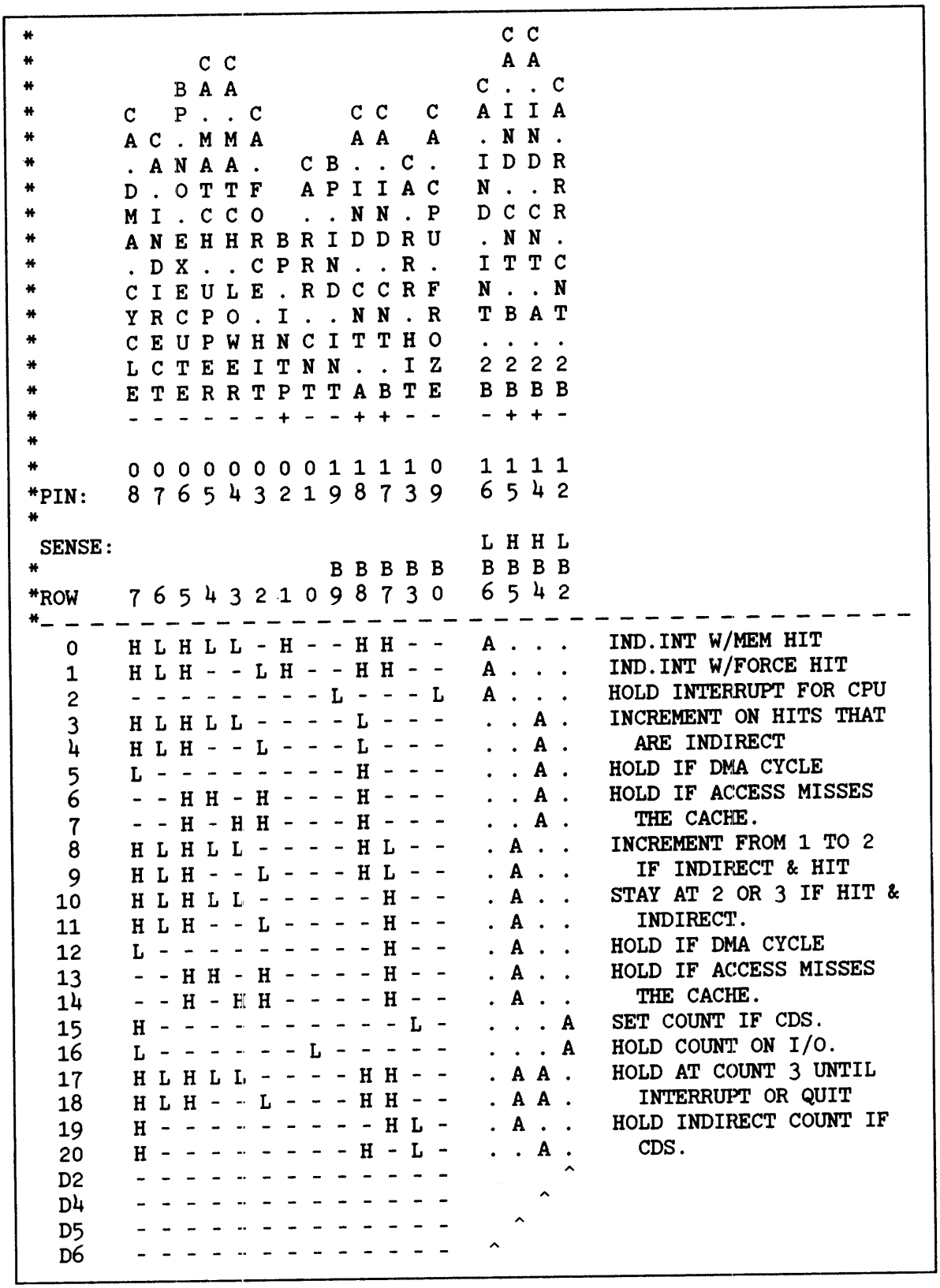
Indirects require the cache to hit (CA.MATCH.UPPER- and CA.MATCH.LOWER- or CA.FORCE.HIT-) and that the cycle be for the CPU. Any CPU cycle which does not indirect sets the count back to zero; except for CDS which leaves the count where it was as do DMA cycles and misses. At a count of three, the count is held. If a macro interrupt is asserted, BP.INTP+, then BP.IND.INT- is asserted and the cache stops chasing indirects.

5.3.1.7 Code and Data Separation (CDS)

The test for base page addresses is done with the same logic that checks for A/B addressability, U0102 and U1607 (CA112B). These are combined in gates U0104 and U0205 (CA113B) to produce CA.CDS.HIT+/- and CA.AB.HIT-. An access which is base relative (CDS) causes the Adder to be selected as the input to the M1 MUX, and M1 be selected as the next address for the CPU. Also, the Q-REG, U1302 (CA62B) and U1305 (CA62C) is substituted for the all zero buffer U1402 (CA64B) and U1405 (CA64C). This also stops any increments that might have been implied.

On the map-set select side, CDS requires non-MRG and non-code accesses to be made from the data map set. The code map is always the odd map of a map pair; data is the even map set. For example, if "2" is a data map then "3" would be the paired code map. PLA U0804 (CA132B) handles the CODE and BOOT specials. The code for the Code and Boot PLA is given in Figure 5-8.

The signal CA.CODE.REQ+ is asserted if CODE is in the SP0 field or if JTAB is in the MEM field (next access will either be a DEF or an MRG address -- both are in the code map set.) A copy of this is kept by CA.DLY.CODE.2B+ in case DMA holds off the CPU. These signals are all in terms 0-4 of the above PLA. The 4:1 MUX at U0207 (CA135A) is then used as a four input AND gate to AND in the terms: CA.MP.IN7+ (CDS enabled), not CA.INDIRECT-, and CA.NO.HOLDS- to produce the signal CA.FORCE.CODE+. This is then OR'd with the bottom bit of the map set select latches in the OR gate U0404 (CA35B).



```
*                                                    C C
*                                                    A A
*                 C C                              C . . C
*               B A A                              A I I A
*       C   P . . C       C C   C                  . N N .
*       A C . M M A       A A   A                  I D D R
*       . A N A A .   C B . . C .                  N . . R
*       D . O T T F   A P I I A C                  D C C R
*       M I . C C O   . . N N . P                  . N N .
*       A N E H H R B R I D D R U                  I T T C
*       . D X . . C P R N . . R .                  N . . N
*       C I E U L E . R D C C R F                  T B A T
*       Y R C P O . I . . N N . R                  . . . .
*       C E U P W H N C I T T H O                  2 2 2 2
*       L C T E E I T N N . . I Z                  B B B B
*       E T E R R T P T T A B T E                  - + + -
*       - - - - - - + - - + + - -
*
*       0 0 0 0 0 0 0 0 1 1 1 1 0                  1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 9 8 7 3 9                  6 5 4 2
*
 SENSE:                                            L H H L
*                           B B B B B              B B B B
*ROW    7 6 5 4 3 2 1 0 9 8 7 3 0                  6 5 4 2
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    H L H L L - H - - H H - -                  A . . .   IND.INT W/MEM HIT
   1    H L H - - L H - - H H - -                  A . . .   IND.INT W/FORCE HIT
   2    - - - - - - - - - L - - - L                A . . .   HOLD INTERRUPT FOR CPU
   3    H L H L L - - - - L - - -                  . . A .   INCREMENT ON HITS THAT
   4    H L H - - L - - - L - - -                  . . A .     ARE INDIRECT
   5    L - - - - - - - - H - - -                  . . A .   HOLD IF DMA CYCLE
   6    - - H H - H - - - H - - -                  . . A .   HOLD IF ACCESS MISSES
   7    - - H - H H - - - H - - -                  . . A .     THE CACHE.
   8    H L H L L - - - - H L - -                  . A . .   INCREMENT FROM 1 TO 2
   9    H L H - - L - - - H L - -                  . A . .     IF INDIRECT & HIT
  10    H L H L L - - - - - H - -                  . A . .   STAY AT 2 OR 3 IF HIT &
  11    H L H - - L - - - - H - -                  . A . .     INDIRECT.
  12    L - - - - - - - - - H - -                  . A . .   HOLD IF DMA CYCLE
  13    - - H H - H - - - - H - -                  . A . .   HOLD IF ACCESS MISSES
  14    - - H - H H - - - - H - -                  . A . .     THE CACHE.
  15    H - - - - - - - - - - L -                  . . . A   SET COUNT IF CDS.
  16    L - - - - - - L - - - - -                  . . . A   HOLD COUNT ON I/O.
  17    H L H L L - - - - H H - -                  . A A .   HOLD AT COUNT 3 UNTIL
  18    H L H - - L - - - H H - -                  . A A .     INTERRUPT OR QUIT
  19    H - - - - - - - - - H L -                  . A . .   HOLD INDIRECT COUNT IF
  20    H - - - - - - - - - H - L -                . . A .     CDS.
  D2    - - - - - - - - - - - - - -                        ^
  D4    - - - - - - - - - - - - - -                    ^
  D5    - - - - - - - - - - - - - -                  ^
  D6    - - - - - - - - - - - - - -                ^
```

Figure 5-7. Indirect Count PLA (U0705) Code

```
*
*                                                C C C C
*                          C   C                 A A A A
*            C               A   A B B             . . . .
*        C   A       C . C . P P   C D B D B
*        A C . C     A D A D . .   A L O L O
*        . A D A     . E . E U U   . Y O Y O
*        I . M .     C L B L I I   C . T . T
*        N R A D     O A O A R R   O C . B .
*        D R . M     D Y O Y . .   D O I O N
*        I R C A C E . T . R R     E D F O O
*        R . Y . A . C . B E E     . E . T .
*        E H C R . S O S O G G     R . I . I
*        C I L E F P D P O 1 1     E 2 N 2 N
*        T T E Q 3 0 E 0 T 4 3     Q B D B D
*        - - - + + - + - + + +     + + + + +
*
*        0 0 0 0 0 0 0 0 1 1 0     1 1 1 1 1
*PIN:    8 7 6 5 4 3 2 1 9 1 9     8 7 6 5 4
*
 SENSE:                           H H H H H
*                              B B B   B B B B B
*ROW     7 6 5 4 3 2 1 0 9 1 0     8 7 6 5 4
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0     - H H L - L - - - - -     A . . . .   CODE/SPO & NEW CYCLE
   1     - H H L - - - - - H H     A . . . .   JTAB & NEW CYCLE
   2     - - L - - - H - - - -     A A . . .   CODE DELAYED BY DMA
   3     H H H - - L - - - - -     . A . . .   CODE/SPO SELECT UNLESS DMA
   4     H H H - - - - - - H H     . A . . .   JTAB     SELECT UNLESS DMA
   5     - H H L - - - L - - -     . . . . A   BOOT & NEW CYCLE
   6     - - L L - - - - H - -     . . A . A   SELECT DELAY BOOT IF DMA,
   7     - L - L - - - - H - -     . . A . A     CDS, OR INDIRECT AND
   8     - - L - L - - - H - -     . . A . A     NO DMA REQUEST.
   9     - - - L - - - - H - -     . . A . .     ---
  10     H H H - - - - L - - -     . . . A .   DELAY BOOT GETS BOOT/SPO
  11     - - L - - - - - H - -     . . . A .     IF NEW CYCLE, ELSE HOLD
  12     - L - - - - - - H - -     . . . A .     IF DMA, CDS OR INDIRECT.
  13     L - - - - - - - H - -     . . . A .     ---
  D4     - - - - - - - - - - -                 ^
  D5     - - - - - - - - - - -               ^
  D6     - - - - - - - - - - -             ^
  D7     - - - - - - - - - - -           ^
  D8     - - - - - - - - - - -         ^
*
```

Figure 5-8. BOOT/SPO and CODE/SPO PLA (U0804) Coding

5.3.1.8 DMA

The selection of DMA was covered above in the address selection subsection. The handshaking of DMA requests on the I/O backplane will be covered in the backplane chapter (Chapter 9).

5.3.1.9 Boot Memory

Boot addressing refers to any access to the data store outside of the regular cache data store. The figure on schematic page CA2 (CA27D) shows the distribution of the cache data store RAM space. Since the VCP code expects to be at logical address 8k - 12k, and it expects to find a data space at logical address 0k - 1k, the data store addressing has to be modified during boot accesses.

A boot access can be made by either setting the boot memory bit in the map set select latches (bit 6) or by asserting SP0/BOOT in the microcycle before the access (same line as the MEM field). PLA U0804 does this OR'ing for the early signals and then uses the 4:1 MUX U0207 to do the AND'ing with not CA.INDIRECT- and CA.NO.HOLDS-. The signal CA.CODE.REQ+ is really a don't care. Two versions of the BOOT signal are generated and selected between by CA.INDIRECT-.

5.3.1.10 Miscellaneous Addressing Functions

The MADR read buffer U1202 (CA67C) and U1203 (CA67D) is used to drive the current MADR value to the CA.S.BUS.OUT+ and eventually to the BP.S.BUS+ if it is enabled by the RREG decoder.

The FA register is contained in U1303 (CA62D) and U1205 (CA62E). It is loaded from the CA.MADR.ADDER+ bus whenever JTAB (or JTDI) is coded in the MEM field. The FA clock enable signal comes from the DMS Checking PLA U0805 (CA122D). The code is given in Figure 5-9.

FA is enabled to clock whenever it is a CPU cycle (CA.DMA.CYCLE+), the cycle is not being aborted by the CPU (BP.NO.EXECUTE-), there is not an indirect interrupt pending (BP.IND.INT+), there is not a DMS violation pending (BP.MP.INT+), and JTAB or JTDI is in the MEM field (BP.UIR.REG14,13+ = 1). The MADR adder is used for loading FA instead of the CA.MADR.OUT+ bus because of hold-time problems. FA is on a gated clock and MADR is ungated.

The PLA U0805 (Figure 5-9) also generates the signal BP.MP.INT+. It ORs together the write violation signal (CA.WRT.VIOL+) with a read violation; i.e., a TAB or PNTR in RREG, the DMS system is enabled (CA.DMS.EN+), the page selected is read protected (CA.DMS.RP+), the cycle is not aborted (BP.NO.EXECUTE-), and the CPU is accessing the cache (NOT CA.DMA.CYCLE+).

A summary of how and when the various address selection decisions are made is shown in the assembly language sample program shown in Figure 5-10. The state of important cache decisions is shown in Figure 5-11.

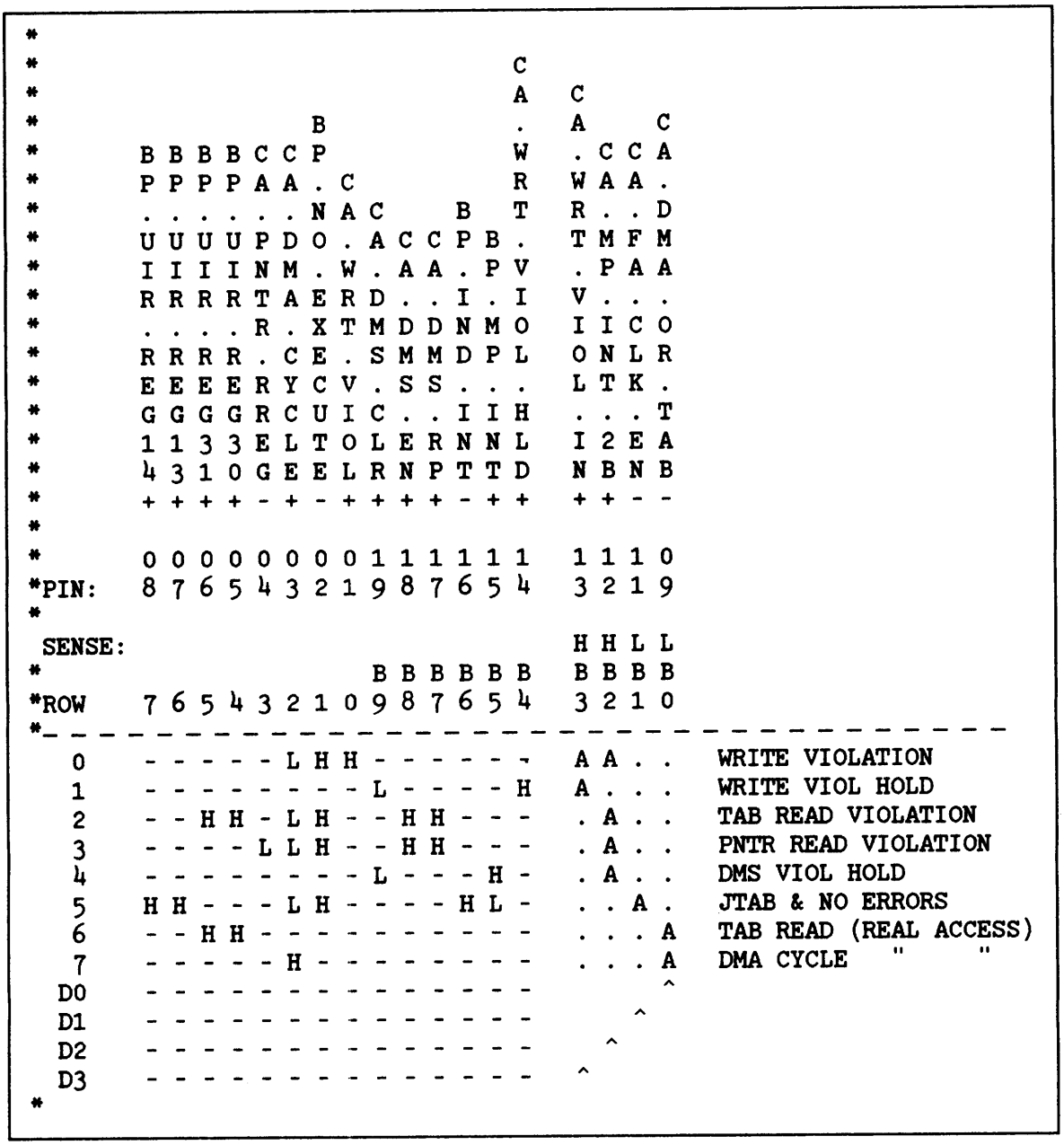


Figure 5-9. DMS Checking PLA (U0805) Code

```
 00000 ZERO:  LDB PARM1
.
.
.
000020 PARM1: DST
000021        DEF --


NOT PAGE ZERO:

              LDA FOO       * MRG direct
              LDA BAR,I     * MRG indirect
              DLD           * DLD direct
              DEF DAT2      *    (DMA gets in here)
              LDA PARM1     * MRG base relative
              LDA FOO       * MRG direct (DMA gets in and faults)
              STA DAT1      * Store that gets held up by WDR being busy
              DLD           * non-MRG CDS access
              DEF PARM1     *
              JMP ZERO      * jump to A to create fetch A/B and A/B
              .             *   updating problem.
              .
              .
       FOO    BSS
       BAR    DEF IND1
              .
              .
              .
       IND1   DEF IND2
              .
              .
              .
       IND2   DEF DAT1
              .
              .
              .
       DAT1   BSS
       DAT2   BSS
              BSS
```

Figure 5-10. Sample Program for Address Selection Decisions

	STOT	RREG	MEM	DELAY MEM	DELAY SOURCE	SELECT ADDR	SELECT WHY	PRESENT ADDR	INC DEST	SPECIAL DEST	SPECIAL WHY	FRZ	COMMENT
1	-	-	PCPC	-	-	PC	MEM	-	-	-	-	NO	
2	-	TAB	JTAB	PCPC	MEM	M1	JTAB	PC	PC	M1	JTAB	NO	FETCH LDA
3	-	TAB	PCPC	M1M1	JTAB	PC	MEM	M1	M1	-	-	NO	READ OPERAND
4	-	TAB	JTAB	PCPC	MEM	M1	JTAB	PC	PC	M1	JTAB	NO	FETCH LDA,I,C
5	-	PNTR	M1M1	M1M1	JTAB	M1	IND	M1	(M1)	M1	PNTR	YES	INDIRECT
6	"	"	"	M1M1	IND	M1	IND	M1	(M1)	M1	PNTR	YES	INDIRECT
7	"	"	"	M1M1	IND	M1	MEM	M1	(M1)	M1	PNTR	NO	DIRECT
8	-	TAB	PCPC	M1M1	MEM	PC	MEM	M1	M1	-	-	NO	READ OPERAND
9	-	TAB	JTAB	PCPC	MEM	PC	JTAB	PC	PC	M1	JTAB	NO	FETCH DLD
10	-	PNTR	M1M1	PCPC	JTAB	M1	MEM	PC	PC	M1	PNTR	NO	READ DEF
11	-	TAB	M1M1	M1M1	MEM	M1	MEM	M1	M1	-	-	NO	READ OPERAND 1
12	-	TAB	PCPC	M1M1	MEM	IO	DMA	M1	M1	-	-	NO	READ OPERAND 2
13	-	TAB	JTAB	PCPC	MEM	PC	DELAY	IO	-	-	-	YES	DMA HIT
14	"	"	"	PCPC	DELAY	M1	JTAB	PC	PC	M1	JTAB	NO	FETCH LDA,B
15	-	TAB	PCPC	M1M1	JTAB	M1	CDS	M1	(M1)	M1	CDS	YES	BASE PAGE REL.
16	"	"	"	M1M1	CDS	PC	MEM	M1	M1	-	-	NO	READ OPERAND
17	-	TAB	JTAB	PCPC	MEM	IO	DMA	PC	PC	M1	JTAB	NO	FETCH LDA
18	-	TAB	PCPC	M1M1	JTAB	HLD	MISS	IO	-	-	-	YES	DMA MISS
19	"	"	"	M1M1	DELAY	HLD	MISS	HLD	-	-	-	YES	STATE F1+
20	"	"	"	M1M1	DELAY	HLD	MISS	HLD	-	-	-	YES	STATE F2+
21	"	"	"	M1M1	DELAY	M1	DELAY	HLD	-	-	-	YES	STATE F3+
22	"	"	"	M1M1	DELAY	PC	MEM	M1	M1	-	-	NO	READ OPERAND
23	-	TAB	JTAB	PCPC	MEM	M1	JTAB	PC	PC	M1	JTAB	NO	FETCH STA
24	-	TAB	M1M1	M1M1	JTAB	M1	MEM	M1	M1	-	-	NO	READ OPERAND
25	TAB	-	PCPC	M1M1	MEM	HLD	BUSY	M1	M1	-	-	YES	WDR BUSY
26	"	"	"	PCPC	MEM	PC	MEM	HLD	-	-	-	NO	STORE OPERAND
27	-	TAB	JTAB	PCPC	MEM	PC	JTAB	PC	PC	M1	JTAB	NO	FETCH DLD,BASE
28	-	PNTR	M1M1	PCPC	JTAB	M1	MEM	PC	PC	M1	PNTR	NO	READ DEF
29	"	"	"	M1M1	CDS	M1	CDS	M1	(M1)	M1	CDS	YES	BASE PAGE REL.
30	-	TAB	M1M1	M1M1	MEM	M1	MEM	M1	M1	-	-	NO	READ OPERAND 1
31	-	TAB	PCPC	M1M1	MEM	PC	MEM	M1	M1	-	-	NO	READ OPERAND 2
32	-	TAB	JTAB	PCPC	MEM	M1	JTAB	PC	PC	-	-	NO	FETCH JMP
33	-	TAB	JTAB	M1M1	JTAB	M1	JTAB	M1	M1	PC	LDPC	NO	FETCH LDB
34	-	TAB	PCPC	M1M1	JTAB	PC	MEM	M1	M1	-	-	NO	READ OPERAND
35	-	TAB	JTAB	PCPC	MEM	HLD	A/B	PC	PC	-	-	YES	FETCH AT A/B
36	"	"	"	PCPC	JTAB	PC	JTAB	HLD	-	-	-	NO	WAIT ONE CLOCK
37								PC					

Figure 5-11. Cache Decision States

The fields of Figure 5-11 are:

STOT	- the current value of the STOT field
RREG	- " " " " " RREG "
MEM	- " " " " " MEM "
DELAY MEM	- the current value of the DELAY MEM bus.
DELAY SOURCE	- where the choice of DELAY MEM inputs came from.
SELECT ADDR	- next logical address for the cache
SELECT WHY	- reason for above choice.
PRESENT ADDR	- value of CA.MADR.OUT+ bus
INC DEST	- where the MADR ADDER output is stored caused by the MEM field. () means store was overridden.
SPECIAL DEST	- other stores of logical address
SPECIAL WHY	- reason for special store
FRZ	- is the CPU frozen at the end of this cycle?

5.3.2 Cache Memory

This detailed description of the cache memory supplements the information on the cache already covered in the preceding Address Creation chapter.

5.3.2.1 DMS (Dynamic Mapping System)

The DMS is contained on page CA4 of the schematics. The DMS RAMs are parts U1101, U1301, U0901, U0902 and U0201 (CA4). The read and write protect bits are stored as the most significant two bits. The least significant bit (physical address 10) is stored in the faster 1k x 1, 20 nanosecond RAM U0201 (CA46B). This is because this bit is necessary to select between the two parts of the data store ("normal" and "inverted") and the TAG store RAMs for even or odd physical pages. The other RAMs are 1k by 4 bits, 45 nanosecond chips. The format of the data is shown on page CA4 (CA46E).

The DMS RAMs can be read or written by the data path; i.e., through RREG and STOT fields. For RREG/MAPS, the RAMs are read by enabling them onto the CA.S.BUS.OUT+ with chips U1102 (CA44D) and U1003 (CA44E). These chips are controlled directly from the RREG decoder, U1007 (CA82C). The CA.S.BUS.OUT+ is enabled onto the backplane (BP.S.BUS+) by the buffers U1307 (CA65B) and U1207 (CA65C).

The DMS RAMs are written when STOT/MAPS is in rank-two. This is the output of the STOT decoder, U0907 (CA82D). The data from the CA.S.BUS.IN+ (which is always a copy of BP.S.BUS+) is enabled to the RAMs at the same time as the write pulse to the RAMs. This is shaped by chips U0403 and U0204 (CA41D) to be a "negative-true" signal occurring just before mid-cycle and running until just before end-of-cycle.

5.3.2.2 Tag Store

The tag store is contained on page CA5 of the schematics. The tag store consists of two pieces, the even physical page part and the odd physical page part. The odd physical page tag RAMs are chips U0301, U0202, U0401, and U0501. The even physical page tag RAMs are chips U0801, U0302, U0402 and U0701. Because there are 1k words in a page and there are two words per block, only 512 entries are needed for each half. For this reason, one address bit (A0) is not used.

The selection between the two halves is made by the least significant bit of the DMS RAMs (physical address 10). This is inverted to get the signal CA.PAGE.ODD-. The "modified" bit (M-Bit), (sometimes called the "dirty" bit) is stored in a 1k x 1 fast 20 nanosecond RAM U0203 (CA55D). Since it is much faster than the other RAMs, it is shared between the two pieces; CA.PAGE.ODD- is used as its lower address bit.

The M-bit needs to be updated whenever a block is written into or whenever a block replacement is done (cache fault). The write case is handled by input BP.TRUE.WRITE+ (to be described later) and the fault case by input CA.F3+ (last cycle of a replacement cycle) to gate U1004 (CA52E). This is then shaped by the OR gate U0404 (CA53E) to produce a second half write pulse to the M-bit RAM. The input to the RAM is naturally BP.TRUE.WRITE+. The output of the M-bit RAM, is sampled before the write cycle is begun by the flip-flop U1309 (CA57D).

The Tag Store RAMs are never read or written to directly by the CPU. They are only updated during the second cycle of a fault (state F2). Thus, the write pulse and data-in enable is generated from CA.F2+ and CK.MEM.A.D50+ by chip U0204 (CA51E). The data for writing the tag store comes from the physical address; i.e., the output of the DMS RAMs. This is done by chips U0802 (CA52D) and U0601 (CA53D).

5.3.2.3 Tag Compare

The circuit for "test for HIT" is on schematic page CA7. The physical address (DMS output) is compared to the physical address tag on the data (Tag Store output) by the 8-bit comparator U0702 (CA72B) and U0703 (CA74B). These outputs are combined by the AOI gate U0606 (CA76A). Under certain cases, no real access to the cache is intended. In these cases, it is desired not to have the cache either fault or freeze the CPU.

Gate U0306 (CA72A) forces a "HIT" when a cycle is being done for the CPU (NOT CA.DMA.CYCLE-) and the CPU is stopping the cycle (BP.NO.EXECUTE-). This case occurs whenever a new macroinstruction was started by the CPU but an interrupt was found to be waiting or if the first microinstruction line of a macroinstruction was incorrect. This is a side-effect of "guessing" on an IJT line, but in some macroinstructions the choice is wrong. Gate U0406 (CA72A) adds in four other cases as follows:

a. The access hit the macro A- or B-Registers (BP.AB.HIT+) -- do not fault, or else all lower two words of every page will have unacceptable hit ratios.

b. The access created a write violation (CA.WRT.VIOL+) -- stop the fault or during the block replacement the merge will write on a write protected page.

c. No real access was intended (CA.NO.CYCLE+) -- not a DMA cycle nor a CPU read or write.

d. No faults are desired for other reasons (CA.CDS.BOOT.HIT+).

The latter signal is generated by the gates U0206 (CA116B) and U0106 (CA117B). These OR together three more force-hit conditions:

a. CA.CDS.HIT- (CDS relocation; thus not a real access).

b. CA.BOOT.CYCLE- (access is to boot memory -- which is always present).

c. CA.ALWAYS.HIT- (a Cache Control Register (CCR) diagnostic bit).

The addresses for reading and writing blocks to main memory are latched whenever the main memory is busy. A fault cannot start unless the memory controller is free (NOT BP.MEM.BUSY+) and the memory controller becomes busy immediately upon such a fault. Thus BP.MEM.BUSY+ is used as the latching signal for both the read and write addresses. The read address is the physical address (DMS output) and is stored in U0602 (CA76C) and U0603 (CA76D).

The write address is the physical address (tag) of the data now in the cache; i.e., the block being replaced (Tag store output). This is stored in U0502 (CA74C) and U0503 (CA74D). The least significant bit (CA.MADR.OUT9+), comes directly from the address register (MADR) and is much faster than the other bits. The remaining eight bits of the main memory address come from the MC card as latched versions of the Cache Data ADdress Register (CDADR). This bus is called BP.LOG.ADDR8-1+ and is latched in U0401 (MC37D) on the MC card. Refer to Chapter 6 in the Cache Data Store subsection.

5.3.2.4 Write Generation

The write strobes for the cache RAMs originate on schematic CA9 and go to the memory controller schematic MC15 covering Cache Write Control. (refer to the Memory Controller Card, Chapter 6).

Gates U0407 (CA92A) , U0407 (CA93A) and 8:1 MUX U1501 (CA96B) generate the signals BP.NORMAL+ and BP.INVERT+. If CA.BOOT.CYCLE+ is false (regular operation), then the equation for BP.INVERT+ is:

```
BP.INVERT+ := CA.MADR.OUT0+ XOR CA.DMS10+
```

That is, XOR the lower physical address with the physical page number. If CA.BOOT.CYCLE+ is true (VCP operation), the equation for BP.INVERT+ is:

BP.INVERT+ := CA.MADR.OUT0+ XOR CA.MADR.OUT10+

Note that BP.NORMAL+ is just the complemented form of BP.INVERT+. (Refer to "normal" and "inverted" description above for an explanation of this.)

The signal BP.TRUE.WRITE+ is the signal that causes a write unless something is wrong with the cycle itself. To activate this signal, a number of events that must occur as follows:

a. The WDR must be available if a miss might occur, since writes are done before HIT is known. The gate U0303 (CA92B) generates the "no miss" cases:

   1. A BOOT (VCP) memory cycle (all memory is in cache).
   2. The last state of cache fault handling (F3+) has resumed.
   3. The last cycle is already checked and the block was in cache (CA.WRITE.HIT+). The top part of AND/OR/INVERT (AOI) U0103 (CA96C) ORs the "no miss" cases with the WDR being available (NOT BP.MEM.BUSY+). That is ANDed in the AOI with either a CPU write (pin 4) or a DMA write (pin 5). The DMA write is a DMA write cycle generated by gate U0204 (CA92C).

b. CPU write is:

   1. TAB in rank 2 of the STOT field.
   2. The address must not be base page if CDS is enabled (not CA.CDS.HIT-).
   3. The cycle must be a CPU cycle (not CA.DMA.CYCLE-).
   4. The access did not hit macro A- or B-Registers (not CA.AB.HIT-).
   5. The three levels of indirect with an interrupt must not have happened (not BP.IND.INT-). This is produced by gate U0205 (CA92C).

c. The DMA write is simply a DMA cycle which is a write, generated by gate U0204 (CA92C).

A write violation has occurred and the write must be stopped for the following conditions:

a. The write protect bit is true (CA.DMS.WP+)

b. The DMS system is enabled (CA.DMS.EN+),

c. The cycle is for the CPU (CA.DMA.CYCLE-),

d. This is not the last cycle of a cache fault (CA.F3-). This last term is necessary since even though a merge is not desired, the block should be written into the cache. Consequently, a write violation is allowed to create a cache fault.

Gate U0803 (CA94D) checks for DMS write protection. Gate U0106 (CA97D) generates a true-write violation from a CPU write and write protection.

The write-strobe generation circuit continues on the memory controller (refer to Cache Write Control in Chapter 6).

5.3.2.5 Fault Processing

Fault processing has been described in several of the sections above. The first cycle in a cache access has no state other than NOT CA.HOLD.CYCLE+. The next cycle is labeled CA.F1+ and is followed unconditionally by CA.F2+ and CA.F3+. The cache had to miss to cause the first fault cycle to occur (CA.F1+), it is forced to miss during CA.F2+ and CA.F3+ by the signal CA.FORCE.MISS+. Since the tag store is updated during state CA.F2+, the cache will always hit on cycle CA.F3+.

Note that the read of main memory data is done before the write-back of modified data in the cache. Since the cache is the only requestor of main memory, this presents no problems. The cache ignores the actual write-back operation. It only cares if the memory controller is busy or not.

5.4 Parts Locations

The parts locations for the cache control card are shown in Figure 5-12.

5.5 Replaceable Parts List

The replaceable parts list for the cache control card are listed in Table 5-1. The names and addresses of the manufacturers of the parts are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

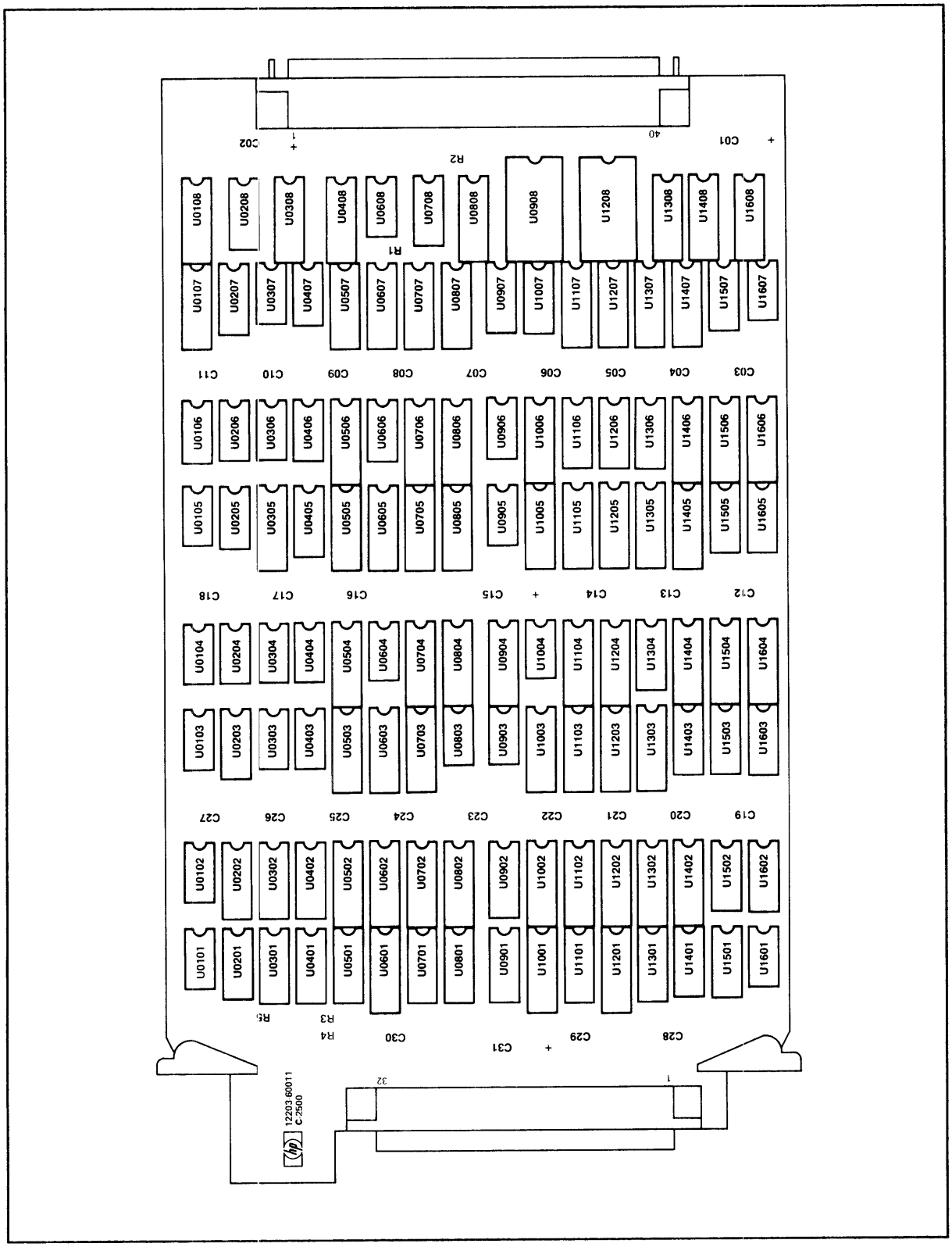


Figure 5-12. Cache Control Card Parts Location

Table 5-1. Cache Control Card Replaceable Parts (Sheet 1 of 3)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12203-60011	5	1	PCA-CACHE CNTRL	28480	12203-60011
C1	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-4835	7	27	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C31	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
R1	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R2	0757-0442	9	1	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-0084	9	3	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R4	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R5	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
U101	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U102	1820-1275	4	4	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U103	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U104	1820-0685	8	2	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U105	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U106	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U107	1820-2701	3	18	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U108	1820-2795	5	17	IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U201	1816-1583	8	2	IC TTL 1024 (1K) STAT RAM 20-NS 3-S	03797	AM93425SADC
U202	1818-3052	4	12	IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U203	1816-1583	8		IC TTL 1024 (1K) STAT RAM 20-NS 3-S	03797	AM93425SADC
U204	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U205	1820-0686	9	3	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U206	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U207	1820-2769	3	4	IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U208	1820-3227	0	1	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F257PC
U301	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U302	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U303	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U304	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74S04N
U305	1820-3272	5	1	IC PRGMBL-LGC TTL S	18324	PLS153N
U306	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U307	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U308	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U401	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052

Table 5-1. Cache Control Card Replaceable Parts (Sheet 2 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U402	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U403	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U404	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U405	1820-2693	2	2	IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U406	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U407	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U408	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U501	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U502	1820-2700	2	13	IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U503	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U504	1820-3056	3	1	IC PRGMBL-LGC TTL S PLA	18324	PLS153N PRGMD
U505	1820-3274	7	1	IC PRGMBL-LGC TTL S	18324	PLS153N PRGMD
U506	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U507	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U601	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U602	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U603	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U604	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U606	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U607	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U608	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U701	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U702	1820-2311	1	2	IC COMPTR TTL LS MAGTD 8-BIT	34335	AM25LS2521PC
U703	1820-2311	1		IC COMPTR TTL LS MAGTD 8-BIT	34335	AM25LS2521PC
U704	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U705	1820-3273	6	1	IC PRGMBL-LGC TTL S	18324	PLS153N PRGMD
U706	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U707	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U708	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U801	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U802	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U803	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U804	1820-3275	8	1	IC PRGMBL-LGC TTL S	18324	PLS153N PRGMD
U805	1820-3055	2	1	IC PRGMBL-LGC TTL S PLA	18324	PLS153N PRGMD
U806	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U807	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U808	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U901	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U902	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U903	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U904	1820-3054	1	1	IC PRGMBL-LGC TTL S PLA	18324	PLS153N PRGMD
U905	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U906	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U907	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1001	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1002	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1003	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1004	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U1005	1820-3023	4	1	IC PRGMBL-LGC TTL S PLA	18324	PLS153N PRGMD
U1006	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1007	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1101	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U1102	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1103	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1104	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1105	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1106	1820-3226	9	5	IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F253PC
U1107	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1201	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1202	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1203	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1204	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1205	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1206	1820-3226	9		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F253PC

Table 5-1. Cache Control Card Replaceable Parts (Sheet 3 of 3)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U1207	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1301	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U1302	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1303	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1304	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1305	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1306	1820-3226	9		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F253PC
U1307	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1308	1820-3862	9	1	IC PRGMBL-LGC TTL S PLA	18324	PLS153N PRGMD
U1401	1820-2693	2		IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U1402	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1403	1820-3226	9		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F253PC
U1404	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1405	1820-1871	6	4	IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1406	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1407	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1408	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1501	1820-3225	8	1	IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	07263	74F251PC
U1502	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1503	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1504	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1505	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	07263	74F244PC
U1506	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1507	1820-3226	9		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F253PC
U1601	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1602	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1603	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1604	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1605	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1606	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1607	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U1608	1820-3271	4	1	IC PRGMBL-LGC TTL S	18324	PLS153N PRGMD
	1200-0994	8	2	SOCKET-IC 28-CONT DIP PC	28480	1200-0994
	1251-7540	1	1	CONN-POST TYPE .100-PIN-SPCG 160-CONT	00779	532809-1
	1251-7974	5	1	CONN-POST TYPE .100-PIN-SPCG 96-CONT	28480	1251-7974
	1252-1461	5	2	KEY-POST CONN	00779	533874-1
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

A	AS ISSUED PCO 22-7407	JW	12-26-84

D-12203-80011-51

M1 MUX

MADR ADDER

M1

69A 40D 160B — CA.S.BUS.IN+ /16
30A 60A 140A 155A — BP.T.BUS+ /15
29A 40A 50B 60C 70E 90A 110A 183B — CA.MADR.OUT+ /16

-1071 74S283 U1602 — A4 A3 A2 A1 B4 B3 B2 B1 C4 S4 S3 S2 S1 CO
-1071 74S283 U1502 — A4 A3 A2 A1 B4 B3 B2 B1 C4 S4 S3 S2 S1 CO
-1071 74S283 U1605 — A4 A3 A2 A1 B4 B3 B2 B1 C4 S4 S3 S2 S1 CO
-1071 74S283 U1405 — A4 A3 A2 A1 B4 B3 B2 B1 C4 S4 S3 S2 S1 CO

CA.ADDER.CRY3+ (341)
CA.ADDER.CRY2+ (340)
CA.ADDER.CRY1+ (339)
7

69A — CA.A.CR.PINC+ /15

-2769 74F153 U1603 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G
-2769 74F153 U1304 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G
-2769 74F153 U1503 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G
-3226 74F253 U1403 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G

-3226 74F253 U1507 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G
-3226 74F253 U1206 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G
-3226 74F253 U1306 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G
-3226 74F253 U1106 — 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3 1Y 2Y A B 1G 2G

CA.M1.IN+

-2700 74F373 U1404 — D8 D7 D6 D5 D4 D3 D2 D1 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 G OE
-2700 74F373 U1406 — D8 D7 D6 D5 D4 D3 D2 D1 Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 G OE

15 CA.MADR.ADDER+ — 20A 60D
16 CA.MADR.IN+ — 20A 39B

119E — CA.FORCE.PAGE0+ (81)
129B — CA.M1.SEL.A+ (33)
129B — CA.M1.SEL.B+ (34)

129A — CK.A.CAC2.M1.LD+ (285)
119C 30B — CA.M1.EN- (195)
139D — CA.PDI-

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

M1 SELECT:

B	A	BIT15	BITS 14-10	BITS 9-0	USE
0	0	S.BUS	MADR	S.BUS	MGR address create
0	1	MADR	ADDER	ADDER	Address increment & RRR Q add
1	0	Ground	T.BUS	T.BUS	Loading M1 from Data Path
1	1	S.BUS	S.BUS	S.BUS	Indirection

CA1

CACHE CONTROLLER -A800 ADDRESS INCREMENTER &M1	HEWLETT PACKARD
12203A	12203-60011
SHEET OF	D-12203-60011-51

A	AS ISSUED PCO 22-7407	jw

MADR HOLD

M2
-2700
74F373
U1504

PC
-2700
74F373
U1604

-2700
74F373
U1508

-2700
74F373
U1608

-2795
74F244
U1204

-2795
74F244
U0108

MADR
-2701
74F374
U1104

-2701
74F374
U0107

CDADR
-2701
74F374
U0408

-2701
74F374
U0308

-0683
74S04
U0304

-1322
74S02
U0308

-3227
74F257
U0208

74S04
U0304
-0683

-0683
74S04
U0304

CA.A.CAC1.CA+ (35)
CA.NO.HOLDS+
CA.BOOT.2B-
CA.DMS10+
CA.PAGE.ODD- (71)
CA.MADR.IN+
CA.MADR.ADDER+
CA.MADR.OUT+
CK.A.CAC2.M2LD+
CA.M2.EN-
CK.A.CAC2.PC.LU+
CA.PC.EN-
CA.TRUE.DMA.REQ+ (452)
CK.A.CAC2.CA+ (29)
CA.PULLUP+ (21)
CA.PD1-
CA.PD2-
CA.MADR.IN 13- (419)
CA.EXT.IN1+ (372)
CA.EXT.IN0+ (371)
CA.LOG.ON+ (397)
CA.LOG.OI+ (398)
BP.DMA.CYCLE.2B+
CA.NO.HOLDS-
BP.LOG.ADDR+
BP.EXT.ADDR1+ (308)
BP.EXT.ADDR0+ (307)
BP.LOG.ADDR0N+ (313)
BP.LOG.ADDR0I+ (312)
CA.BOOT.CYCLE- (234)
CA.DMA.CYCLE+ (31)
BP.DMA.CYCLE+ (498)
CA.DMA.CYCLE- (27)
CA.BOOT.CYCLE+ (233)
CA.NO.HOLDS- (498)

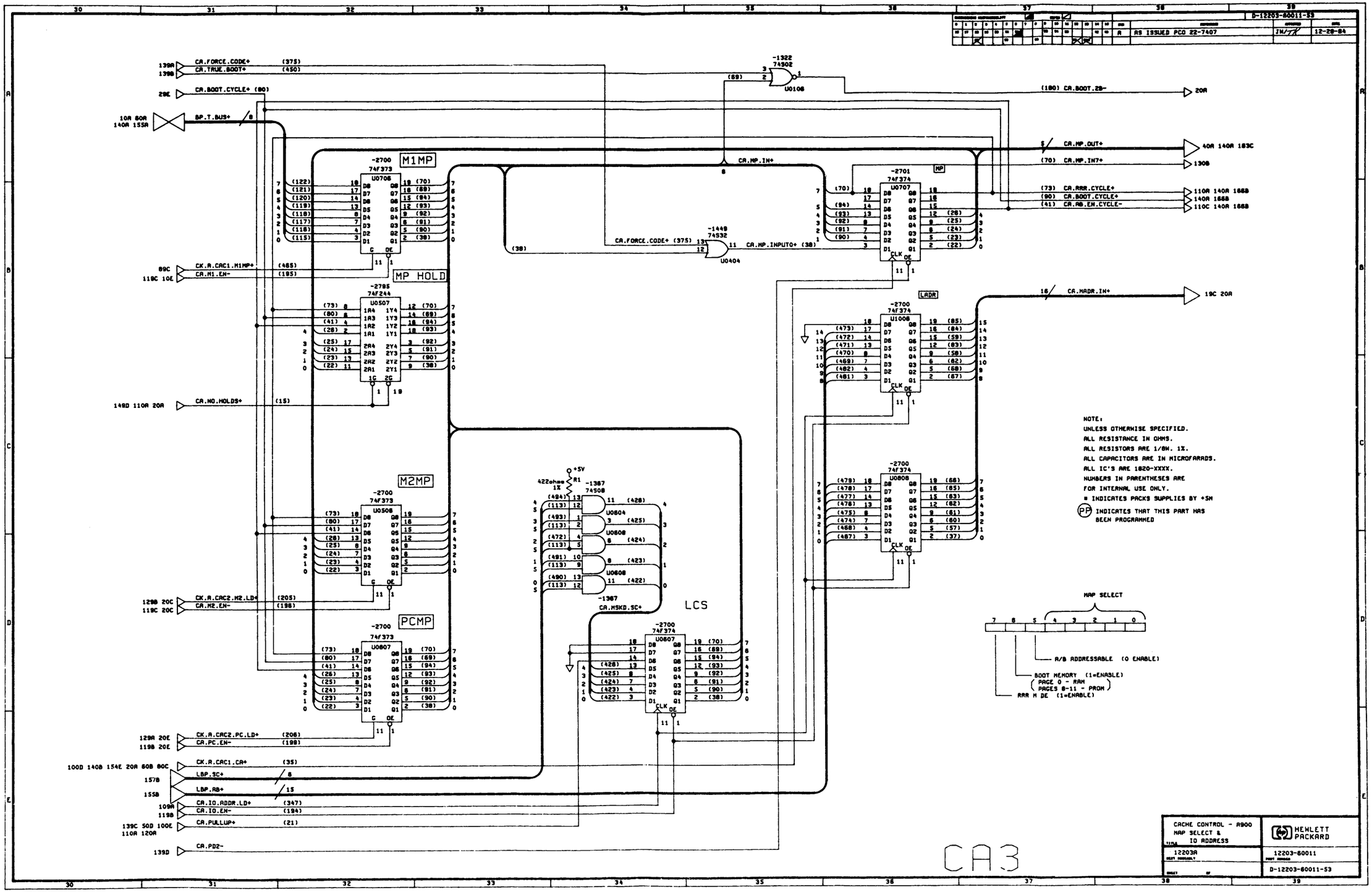
RAM Address — DATA STORE MEMORY MAP

0K	Cache Memory (Boot 2-3K)
2K	Boot 0-1K
4K	Boot 10-11K
6K	Boot 8-9K
8K	

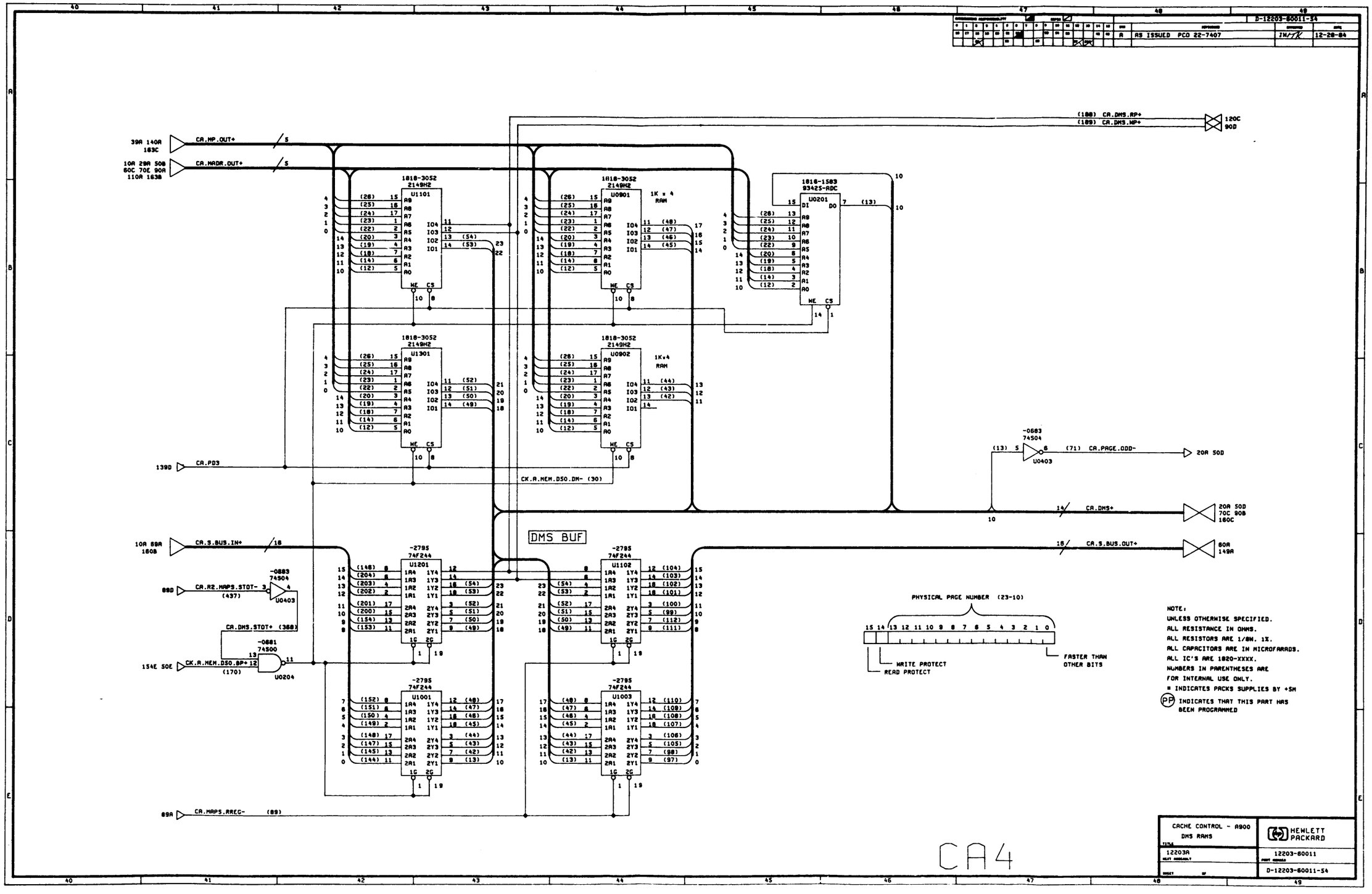
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
= INDICATES PA_KS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

CACHE CONTROLLER-A900 M2, PC & MADR	HEWLETT PACKARD
12203A	12203-80011
	D-12203-80011-52

CA2



Update 2 5-45/5-46


39A 140A 183C
CA.MP.OUT+ 5
10A 28A 50B 80C 70E 90A 110A 163B
CA.MADR.OUT+ 5
(188) CA.DMS.RP+
(189) CA.DMS.WP+
120C 90D
1818-3052 2149H2
U1101
U0901
1K x 4 RAM
1816-1583 93425-RDC
U0201
U1301
U0902
1K+4 RAM
U1001
U1003
139D CA.PD3
CK.A.MEM.D50.DM- (30)
-0883 74S04
U0403
(71) CA.PAGE.ODD-
20A 50D
20A 50D 70C 90B 180C
CA.DMS+
DMS BUF
-2795 74F244
U1201
U1102
10A 88A 180B
CA.S.BUS.IN+ 16
CA.S.BUS.OUT+
60A 149A
88D CA.R2.MAPS.STOT- 3
(437)
CA.DMS.STOT+ (388)
-0881 74S00
U0204
154E 50E CK.A.MEM.D50.BP+ 12
(170)
89A CA.MAPS.RREG- (89)
PHYSICAL PAGE NUMBER (23-10)
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
WRITE PROTECT
READ PROTECT
FASTER THAN OTHER BITS
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
CACHE CONTROL - A900
DMS RAMS
12203A
12203-60011
D-12203-60011-54
HEWLETT PACKARD
CA4
A RS ISSUED PCO 22-7407 12-28-84
D-12203-60011-54

D-12203-60011-55

A	AS ISSUED PC22-7407	JW/	12-28-84

29A 10A 40A 60C
70E 90A 110A 163B
CA.MADR.OUT+ / 9

1818-3052
2149H2
U0301

1818-3052
2149H2
U0401

1818-3052
2149H2
U0801

1818-3052
2149H2
U0402

1818-3052
2149H2
U0202

1818-3052
2149H2
U0501

1818-3052
2149H2
U0302

1818-3052
2149H2
U0701

(16) CK.MEM.DSO.TG-

49C 20A CA.PAGE.ODD- (71)

(13) TAG BUF

13 / CA.TAG+ 70C

49C 70C CA.DMS+ / 14

30E 100E CA.PULLUP+ (21) / 10
110A 120A 139C

-2795
74F244
U0802

-2795
74F244
U0601

1816-1583
93425-ADC
U0203

CA.DIRTY.DOUT+ (238)

DIRTY BIT

-2693
74F109
PR
U1401
CLK
CLR

(370) CA.DOUT.CLKD- 140C

-0681
74S00
U0204

149C 100B CA.F2+ (123)
154E 40D CK.MEM.DSO.BP+ (170)

(16) CK.MEM.DSO.TG-

99B 140A BP.TRUE.WRITE+ (40)
151E 166B

-1322
74S02
U1004

90B 109B CA.F3+ (36)
110C 130B 149C

CA.DIRTY.WRT- (354)

-1449
74S32
U0404

CK.CAC2.DB.CA+ (466)

109E 166B CK.CAC2.B.CA- (169)

-1158
74S51
U0103

(171) CK.SHAPED.CA- 120C

139D CA.PD3-

CACHE CONTROLLER-A900
TAG STORE

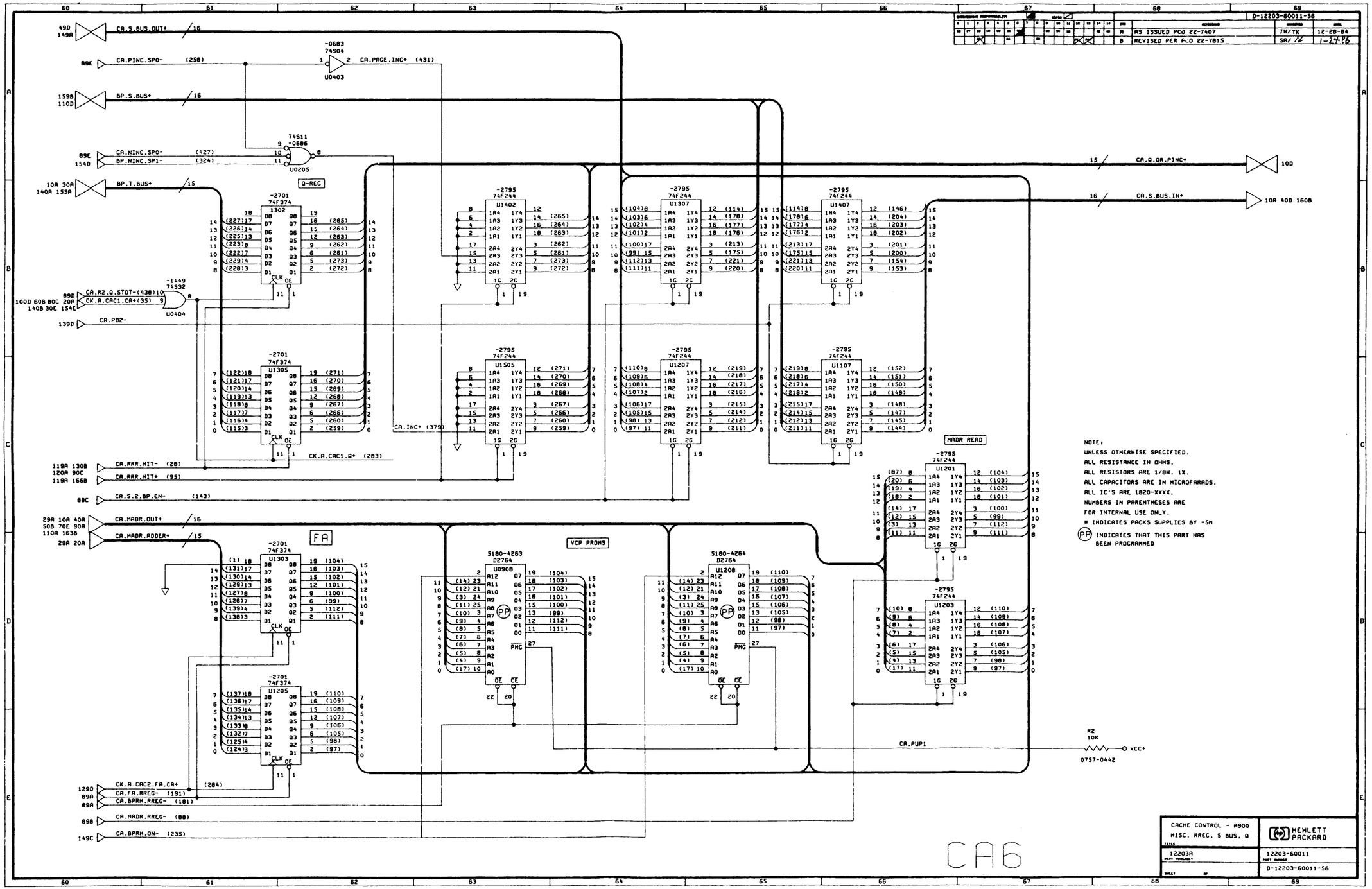
HEWLETT PACKARD

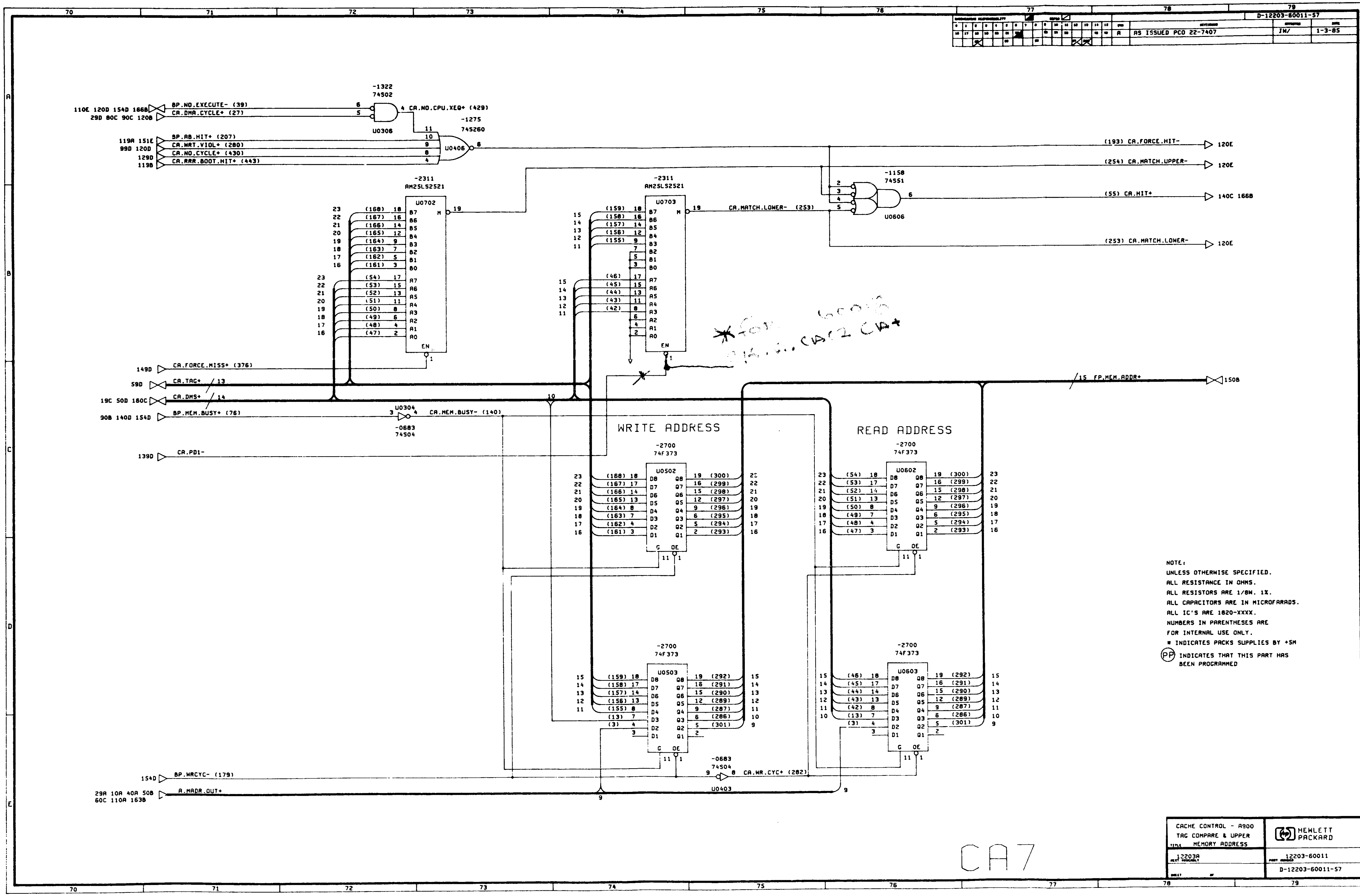
12203A

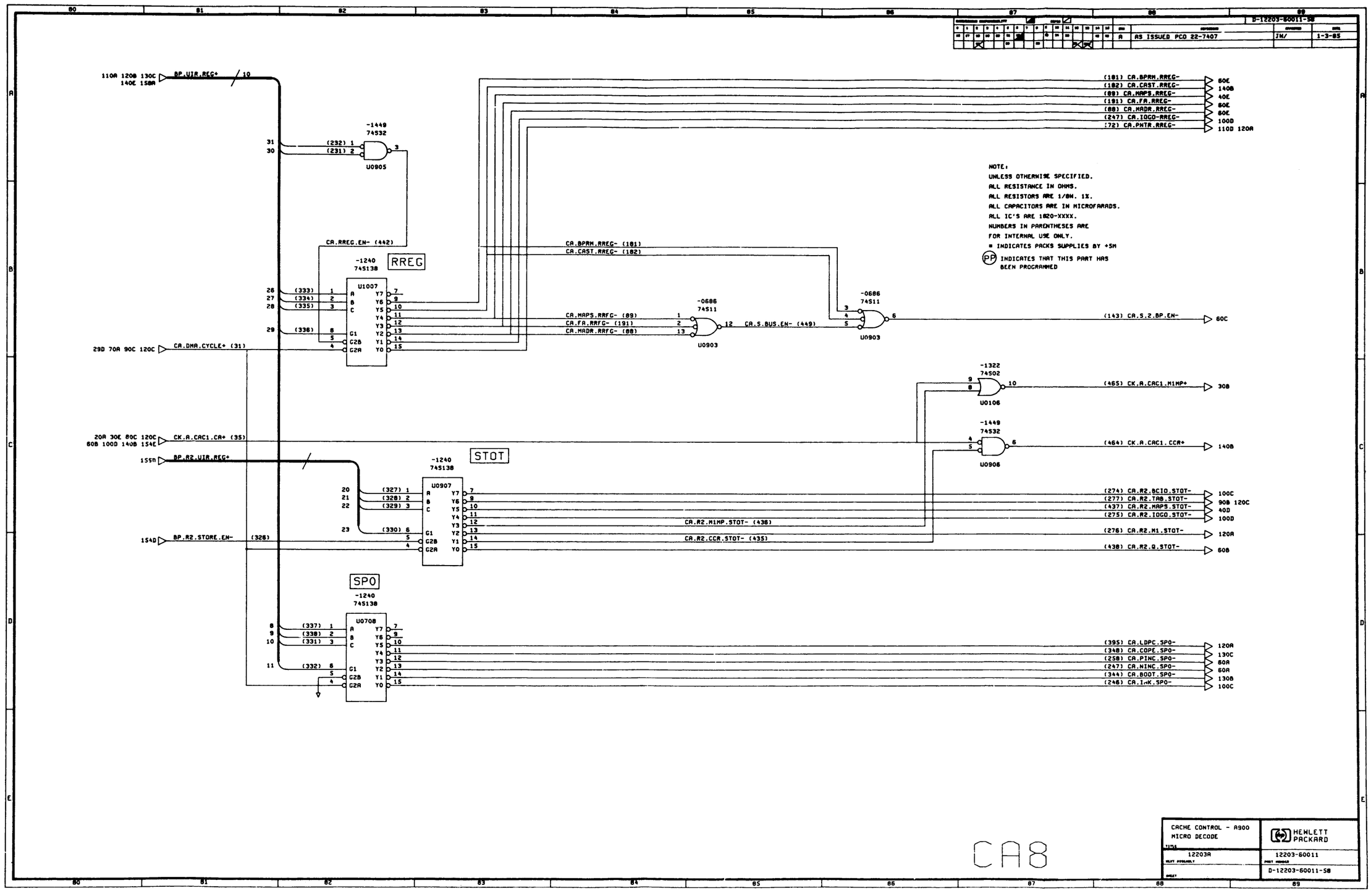
12203-60011

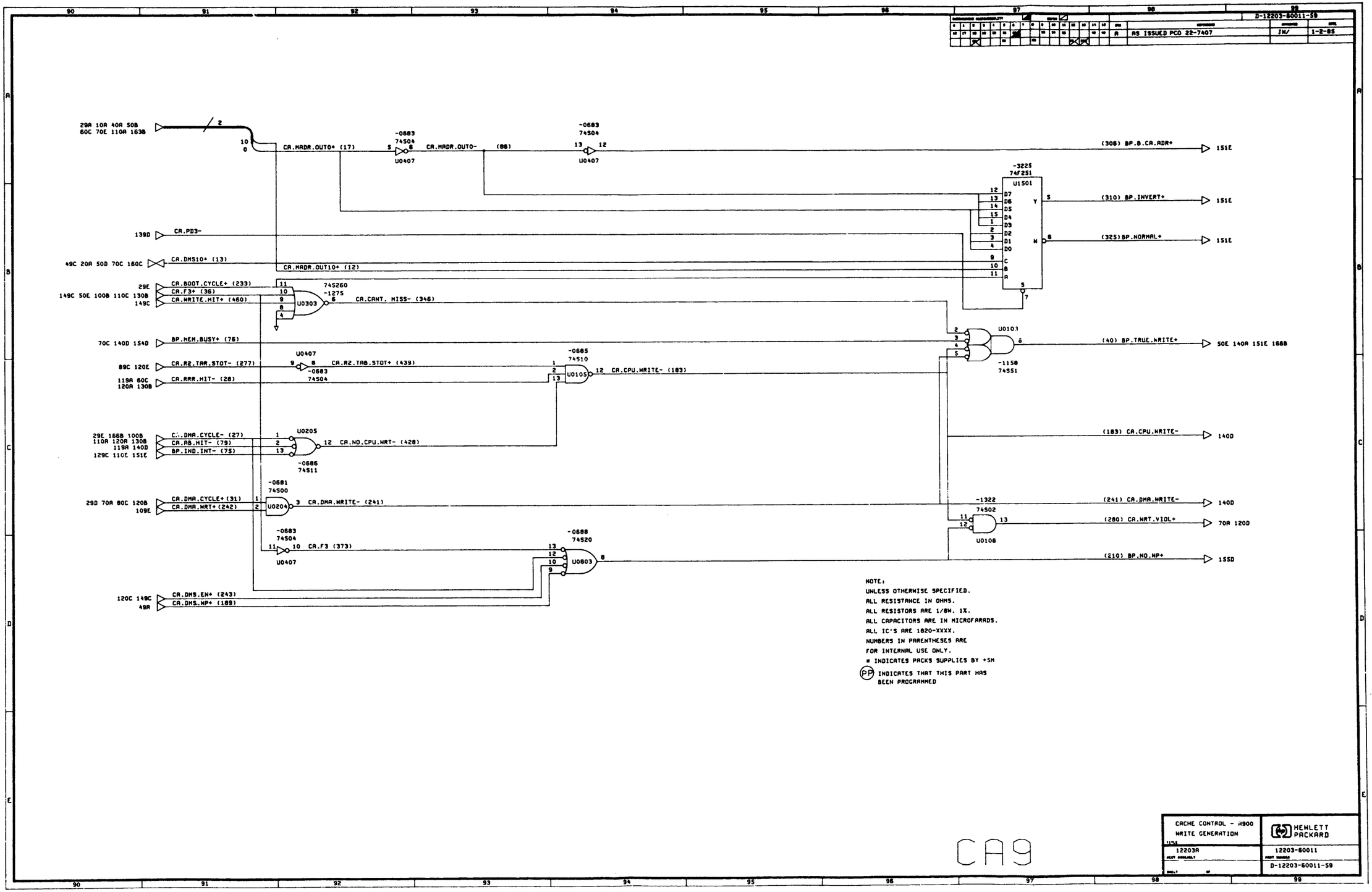
D-12203-60011-55

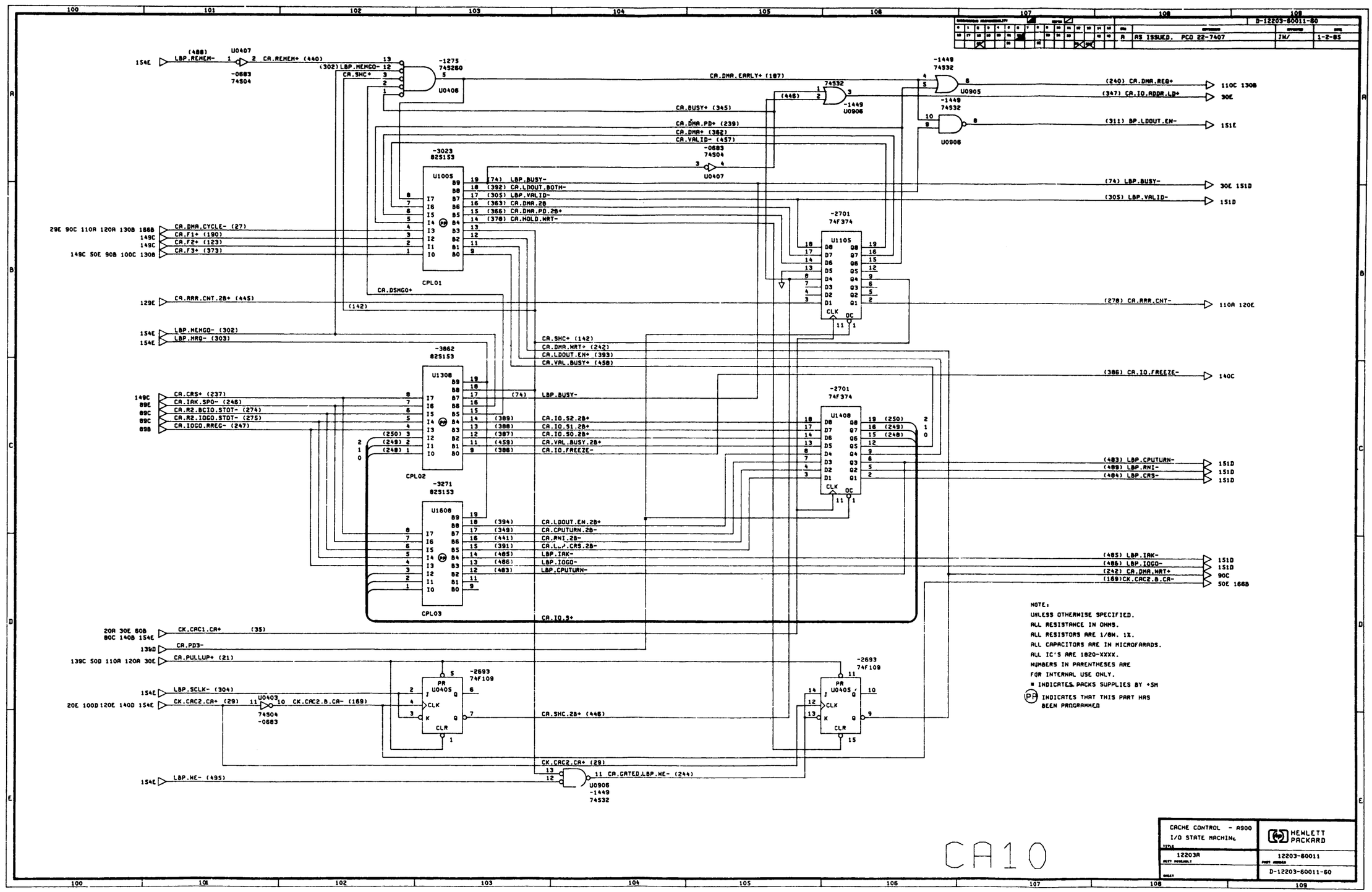
CA5


D-12203-60011-S6
A | AS ISSUED PCO 22-7407 | JW/TK | 12-28-84
B | REVISED PER ECO 22-7815 | SA/ | 1-24-86
49D 149A CA.S.BUS.OUT+ 16
89E CA.PINC.SPO- (258)
-0683 74S04 U0403
CA.PAGE.INC+ (431)
159B 110D BP.S.BUS+ 16
74S11 -0686 U0205
89E CA.NINC.SPO- (427)
154D BP.NINC.SP1- (324)
10A 30A 140A 155A BP.T.BUS+ 15
Q-REG
-2701 74F374 U1302
-2795 74F244 U1402
-2795 74F244 U1307
-2795 74F244 U1407
15 CA.Q.OR.PINC+
10D
16 CA.S.BUS.IN+
10A 40D 160B
-1449 74S32 U0404
89D CA.R2.Q.STOT-(438)10
100D 60B 80C 20A 140B 30E 154E CK.A.CAC1.CA+(35) 9
139D CA.PD2-
-2701 74F374 U1305
-2795 74F244 U1505
-2795 74F244 U1207
-2795 74F244 U1107
CA.INC+ (379)
CK.A.CAC1.Q+ (283)
MADR READ
-2795 74F244 U1201
-2795 74F244 U1203
119A 130B CA.RRR.HIT- (28)
120A 90C CA.RRR.HIT+ (95)
119A 156B
89C CA.S.2.BP.EN- (143)
29A 10A 40A 50B 70E 90A 110A 163B 29A 20A CA.MADR.OUT+ 16
CA.MADR.ADDER+ 15
FA
-2701 74F374 U1303
-2701 74F374 U1205
VCP PROMS
5180-4263 D2764 U0908
5180-4264 D2764 U1208
CA.PUP1
R2 10K 0757-0442 VCC+
129D CK.A.CAC2.FA.CA+ (284)
89A CA.FA.RREG- (191)
89A CA.BPRM.RREG- (181)
89B CA.MADR.RREG- (88)
149C CA.BPRM.ON- (235)
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
CACHE CONTROL - A900
MISC. RREG. S BUS, Q
12203A
12203-60011
D-12203-60011-S6
HEWLETT PACKARD
CA6


D-12203-60011-57
A AS ISSUED PCO 22-7407 JW/ 1-3-85
-1322
74S02
U0306
BP.NO.EXECUTE- (39)
CA.DMA.CYCLE+ (27)
110E 120D 154D 166B
29D 80C 90C 120B
CA.NO.CPU.XEQ+ (429)
-1275
74S260
U0406
BP.AB.HIT+ (207)
CA.WRT.VIOL+ (280)
CA.NO.CYCLE+ (430)
CA.RRR.BOOT.HIT+ (443)
119A 151E
99D 120D
129D
119B
(193) CA.FORCE.HIT- 120E
(254) CA.MATCH.UPPER- 120E
-1158
74S51
U0606
(55) CA.HIT+ 140C 166B
(253) CA.MATCH.LOWER- 120E
-2311
AM25LS2521
U0702
U0703
CA.MATCH.LOWER- (253)
149D CA.FORCE.MISS+ (376)
59D CA.TAG+ 13
19C 50D 160C CA.DMS+ 14
90B 140D 154D BP.MEM.BUSY+ (76)
U0304
-0683
74S04
CA.MEM.BUSY- (140)
139D CA.PD1-
15 FP.MEM.ADDR+ 150B
WRITE ADDRESS
READ ADDRESS
-2700
74F373
U0502
U0503
U0602
U0603
154D BP.WRCYC- (179)
U0403
CA.WR.CYC+ (282)
29A 10A 40A 50B
60C 110A 163B
A.MADR.OUT+
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
PP INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
CACHE CONTROL - A900
TAG COMPARE & UPPER
MEMORY ADDRESS
HEWLETT PACKARD
12203A
12203-60011
D-12203-60011-57
CA7


B-12203-60011-58
A AS ISSUED PCO 22-7407 JW/ 1-3-85
110A 120B 130C 140E 150A
BP.UIR.REG+ / 10
-1449 74532 U0905
(232) 1
(231) 2
31
30
3
CA.RREG.EN- (442)
-1240 74S138 RREG U1007
A B C G1 G2B G2A
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
26 (333) 1
27 (334) 2
28 (335) 3
29 (336) 8
5
4
7 9 10 11 12 13 14 15
29D 70A 90C 120C CA.DMA.CYCLE+ (31)
CA.BPRM.RREG- (181)
CA.CAST.RREG- (182)
CA.MAPS.RRFG- (89)
CA.FA.RRFG- (191)
CA.MADR.RRFG- (88)
-0686 74S11 U0903
1 2 13 12
CA.S.BUS.EN- (449)
3 4 5 6
(181) CA.BPRM.RREG- 60E
(182) CA.CAST.RREG- 140B
(89) CA.MAPS.RREG- 40E
(191) CA.FA.RREG- 80E
(88) CA.MADR.RREG- 80E
(247) CA.IOCO-RREG- 100D
(72) CA.PHTR.RREG- 110D 120A
(143) CA.S.2.BP.EN- 60C
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
PP INDICATES THAT THIS PART HAS BEEN PROGRAMMED
-1322 74502 U0106
9 8 10
(465) CK.A.CAC1.M1MP+ 30B
-1449 74532 U0906
4 5 6
(464) CK.A.CAC1.CCR+ 140B
20A 30E 80C 120C 60B 100D 140B 150E CK.A.CAC1.CA+ (35)
155D BP.R2.UIR.REG+
154D BP.R2.STORE.EN- (328)
STOT -1240 74S138 U0907
A B C G1 G2B G2A
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
20 (327) 1
21 (328) 2
22 (329) 3
23 (330) 6
5
4
7 9 10 11 12 13 14 15
CA.R2.M1MP.STOT- (438)
CA.R2.CCR.STOT- (435)
(274) CA.R2.BCIO.STOT- 100C
(277) CA.R2.TAB.STOT- 90B 120C
(437) CA.R2.MAPS.STOT- 40D
(275) CA.R2.IOCO.STOT- 100D
(276) CA.R2.M1.STOT- 120A
(438) CA.R2.B.STOT- 60B
SPO -1240 74S138 U0708
A B C G1 G2B G2A
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0
8 (337) 1
9 (338) 2
10 (331) 3
11 (332) 6
5
4
7 9 10 11 12 13 14 15
(395) CA.LDPC.SPO- 120A
(348) CA.COPE.SPO- 130C
(258) CA.PINC.SPO- 60A
(247) CA.NINC.SPO- 60A
(344) CA.BOOT.SPO- 130B
(248) CA.IWK.SPO- 100C
CA8
CACHE CONTROL - A900 MICRO DECODE
TITLE
12203A
WAFF ASSEMBLY
HEWLETT PACKARD
12203-60011
PART NUMBER
D-12203-60011-58
SHEET


29A 10A 40A 50B
60C 70E 110A 163B
CA.MADR.OUT0+ (17)
-0683
74504
U0407
CA.MADR.OUT0- (86)
(308) BP.B.CA.ADR+
151E
-3225
74F251
U1501
(310) BP.INVERT+
(325) BP.NORMAL+
139D
CA.PD3-
49C 20A 50D 70C 160C
CA.DMS10+ (13)
CA.MADR.OUT10+ (12)
29E
CA.BOOT.CYCLE+ (233)
149C 50E 100B 110C 130B
CA.F3+ (36)
149C
CA.WRITE.HIT+ (460)
74S260
-1275
U0303
CA.CANT. MISS- (346)
U0103
70C 140D 154D
BP.MEM.BUSY+ (76)
(40) BP.TRUE.WRITE+
50E 140A 151E 168B
-1150
74S51
89C 120E
CA.R2.TAR.STOT- (277)
CA.R2.TAB.STOT+ (439)
-0685
74S10
U0105
CA.CPU.WRITE- (183)
119A 60C
120A 130B
CA.RRR.HIT- (28)
29E 166B 100B
110A 120A 130B
119A 140D
129C 110E 151E
C..DMA.CYCLE- (27)
CA.AB.HIT- (79)
BP.IND.INT- (75)
U0205
CA.NO.CPU.WRT- (428)
-0686
74S11
(183) CA.CPU.WRITE-
140D
-0681
74S00
29D 70A 80C 120B
109E
CA.DMA.CYCLE+ (31)
CA.DMA.WRT+ (242)
U0204
CA.DMA.WRITE- (241)
-1322
74S02
(241) CA.DMA.WRITE-
(280) CA.WRT.VIOL+
70A 120D
U0108
-0688
74S20
U0803
(210) BP.NO.WP+
155D
120C 149C
49A
CA.DMS.EN+ (243)
CA.DMS.WP+ (189)
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
D-12203-80011-59
A
AS ISSUED PCO 22-7407
JW/
1-2-85
CACHE CONTROL - A900
WRITE GENERATION
12203A
12203-80011
D-12203-80011-59
HEWLETT PACKARD
CA9


D-12203-80011-80
A AS ISSUED. PCO 22-7407 JW/ 1-2-85
U0407
74S04
-0683
U0408
-1275
74S260
U1005
-3023
825153
CPL01
U1105
-2701
74F374
U1308
-3862
825153
CPL02
U1408
-2701
74F374
U1608
-3271
825153
CPL03
U0905
-1449
74S32
U0906
-1449
74S32
U0907
-1449
74S32
U0405
-2693
74F109
U0403
74S04
-0683
U0906
-1449
74S32
CA.DMA.EARLY+ (187)
CA.BUSY+ (345)
CA.DMA.PD+ (239)
CA.DMA+ (382)
CA.VALID- (457)
CA.DSMGO+
CA.SHC+ (142)
CA.DMA.WRT+ (242)
CA.LDOUT.EN+ (393)
CA.VAL.BUSY+ (458)
CA.IO.S+
(240) CA.DMA.REQ+
(347) CA.IO.ADDR.LD+
(311) BP.LDOUT.EN-
(74) LBP.BUSY-
(305) LBP.VALID-
(278) CA.RRR.CNT-
(386) CA.IO.FREEZE-
(483) LBP.CPUTURN-
(489) LBP.RNI-
(484) LBP.CRS-
(485) LBP.IAK-
(486) LBP.IOGO-
(242) CA.DMA.WRT+
(188)CK.CAC2.B.CA-
CA.DMA.CYCLE- (27)
CA.F1+ (190)
CA.F2+ (123)
CA.F3+ (373)
CA.RRR.CNT.28+ (445)
LBP.MEMGO- (302)
LBP.MRQ- (303)
CA.CRS+ (237)
CA.IAK.SPO- (248)
CA.R2.BCIO.STOT- (274)
CA.R2.IOGO.STOT- (275)
CA.IOGO.RREG- (247)
CA.IO.S2.28+ (389)
CA.IO.S1.28+ (388)
CA.IO.S0.28+ (387)
CA.VAL.BUSY.28+ (459)
CA.IO.FREEZE- (386)
CA.L.DOUT.EN.28+ (394)
CA.CPUTURN.28- (349)
CA.RNI.28- (441)
CA.L.D.CRS.28- (391)
LBP.IAK- (485)
LBP.IOGO- (486)
LBP.CPUTURN- (483)
CK.CAC1.CA+ (35)
CA.PD3-
CA.PULLUP+ (21)
LBP.SCLK- (304)
CK.CAC2.CA+ (29)
CK.CAC2.B.CA- (189)
CA.SHC.28+ (446)
CK.CAC2.CA+ (29)
LBP.WE- (495)
CA.GATED.LBP.WE- (244)
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
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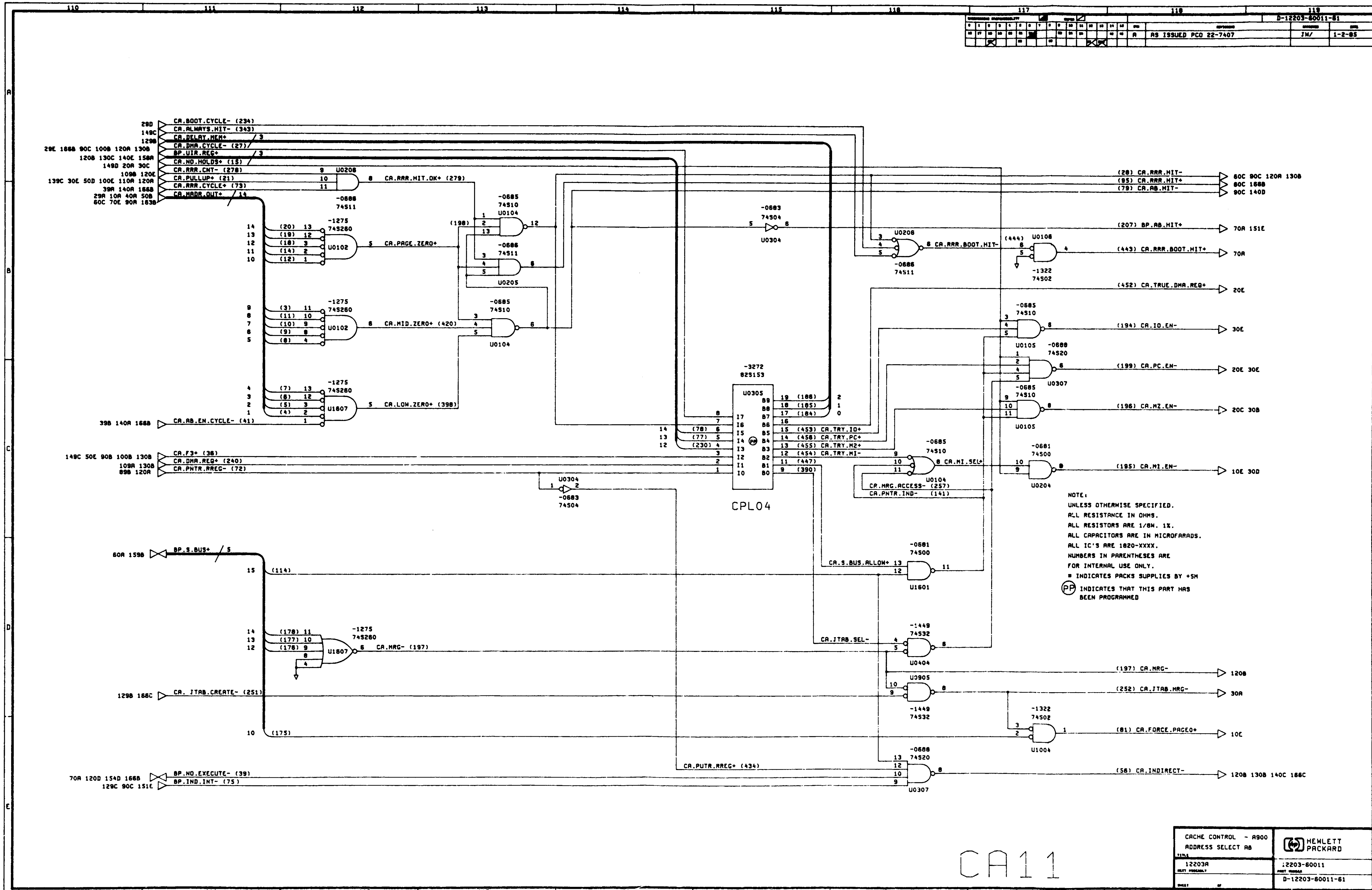
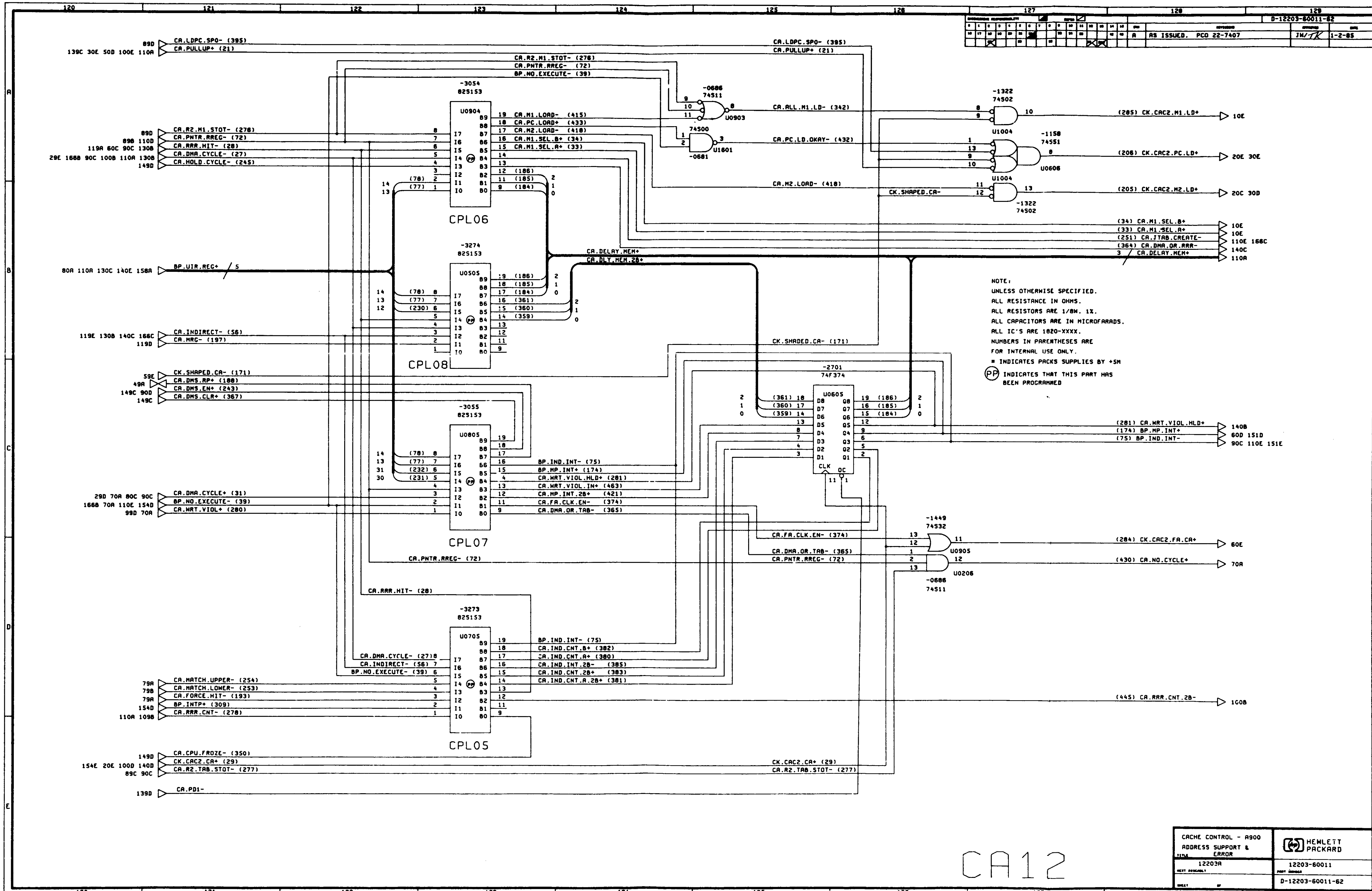
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PF) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
CACHE CONTROL - A900
I/O STATE MACHINE
12203A
HEWLETT PACKARD
12203-60011
D-12203-60011-60
CA10


CA.BOOT.CYCLE- (234)
CA.ALWAYS.HIT- (343)
CA.DELAY.MEM+
CA.DMA.CYCLE- (27)
BP.UIR.REG+
CA.NO.HOLDS+ (15)
CA.RRR.CNT- (278)
CA.PULLUP+ (21)
CA.RRR.CYCLE+ (73)
CA.MADR.OUT+
CA.RRR.HIT.OK+ (279)
CA.PAGE.ZERO+
CA.MID.ZERO+ (420)
CA.LOW.ZERO+ (398)
CA.AB.EN.CYCLE- (41)
CA.F3+ (38)
CA.DMA.REQ+ (240)
CA.PNTR.RREG- (72)
U0305
825153
CPL04
CA.TRY.IO+
CA.TRY.PC+
CA.TRY.M2+
CA.TRY.MI-
CA.MI.SEL+
CA.MRG.ACCESS- (257)
CA.PNTR.IND- (141)
BP.S.BUS+
CA.S.BUS.ALLOW+
CA.MRG- (197)
CA.JTAB.SEL-
CA. JTAB.CREATE- (251)
CA.PUTR.RREG+ (434)
BP.NO.EXECUTE- (39)
BP.IND.INT- (75)
(28) CA.RRR.HIT-
(95) CA.RRR.HIT+
(79) CA.AB.HIT-
(207) BP.AB.HIT+
CA.RRR.BOOT.HIT-
(443) CA.RRR.BOOT.HIT+
(452) CA.TRUE.DMA.REQ+
(194) CA.IO.EN-
(199) CA.PC.EN-
(196) CA.M2.EN-
(195) CA.MI.EN-
(197) CA.MRG-
(252) CA.JTAB.MRG-
(81) CA.FORCE.PAGE0+
(56) CA.INDIRECT-
A AS ISSUED PCO 22-7407 JW/ 1-2-85
D-12203-60011-61
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
PP INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
CA11
CACHE CONTROL - A900
ADDRESS SELECT AB
12203A
12203-60011
D-12203-60011-61
HEWLETT PACKARD


CA.LDPC.SPO- (395)
CA.PULLUP+ (21)
89D
139C 30E 50D 100E 110A
CA.R2.M1.STOT- (278)
CA.PNTR.RREG- (72)
BP.NO.EXECUTE- (39)
CA.R2.M1.STOT- (276)
CA.PNTR.RREG- (72)
CA.RRR.HIT- (28)
CA.DMA.CYCLE- (27)
CA.HOLD.CYCLE- (245)
89D
89B 110D
119A 60C 90C 130B
29E 166B 90C 100B 110A 130B
149D
-3054
82S153
U0904
CPL06
CA.M1.LOAD- (415)
CA.PC.LOAD+ (433)
CA.M2.LOAD- (418)
CA.M1.SEL.B+ (34)
CA.M1.SEL.A+ (33)
-0686
74S11
U0903
74S00
U1601
-0681
CA.ALL.M1.LD- (342)
CA.PC.LD.OKAY- (432)
CA.M2.LOAD- (418)
CK.SHAPED.CA-
-1322
74S02
U1004
-1158
74S51
U0606
(285) CK.CAC2.M1.LD+
10E
(206) CK.CAC2.PC.LD+
20E 30E
(205) CK.CAC2.M2.LD+
20C 30D
(34) CA.M1.SEL.B+
10E
(33) CA.M1.SEL.A+
10E
(251) CA.JTAB.CREATE-
110E 166C
(364) CA.DMA.OR.RRR-
140C
CA.DELAY.MEM+
110A
80A 110A 130C 140E 158A
BP.UIR.REG+
-3274
82S153
U0505
CPL08
CA.DELAY.MEM+
CA.DLY.MEM.2B+
119E 130B 140C 166C
119D
CA.INDIRECT- (56)
CA.MRG- (197)
CK.SHADED.CA- (171)
59E
49A
149C 90D
149C
CK.SHAPED.CA- (171)
CA.DMS.RP+ (188)
CA.DMS.EN+ (243)
CA.DMS.CLR+ (367)
-2701
74F374
U0605
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
PP INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
(281) CA.WRT.VIOL.HLD+
140B
(174) BP.MP.INT+
60D 151D
(75) BP.IND.INT-
90C 110E 151E
-3055
82S153
U0805
CPL07
BP.IND.INT- (75)
BP.MP.INT+ (174)
CA.WRT.VIOL.HLD+ (281)
CA.WRT.VIOL.IN+ (463)
CA.MP.INT.2B+ (421)
CA.FA.CLK.EN- (374)
CA.DMA.OR.TAB- (365)
29D 70A 80C 90C
166B 70A 110E 154D
99D 70A
CA.DMA.CYCLE+ (31)
BP.NO.EXECUTE- (39)
CA.WRT.VIOL+ (280)
CA.FA.CLK.EN- (374)
CA.DMA.OR.TAB- (365)
CA.PNTR.RREG- (72)
-1449
74S32
U0905
U0206
-0686
74S11
(284) CK.CAC2.FA.CA+
60E
(430) CA.NO.CYCLE+
70A
CA.RRR.HIT- (28)
-3273
82S153
U0705
CPL05
CA.DMA.CYCLE- (27)
CA.INDIRECT- (56)
BP.NO.EXECUTE- (39)
BP.IND.INT- (75)
CA.IND.CNT.B+ (382)
CA.IND.CNT.A+ (380)
CA.IND.INT.2B- (385)
CA.IND.CNT.2B+ (383)
CA.IND.CNT.A.2B+ (381)
79A
79B
79A
154D
110A 109B
CA.MATCH.UPPER- (254)
CA.MATCH.LOWER- (253)
CA.FORCE.HIT- (193)
BP.INTP+ (309)
CA.RRR.CNT- (278)
(445) CA.RRR.CNT.2B-
1C0B
149D
154E 20E 100D 140D
89C 90C
CA.CPU.FROZE- (350)
CK.CAC2.CA+ (29)
CA.R2.TAB.STOT- (277)
CK.CAC2.CA+ (29)
CA.R2.TAB.STOT- (277)
139D
CA.PD1-
A
AS ISSUED. PCO 22-7407
JW/TK
1-2-85
D-12203-60011-62
CA12
CACHE CONTROL - A900
ADDRESS SUPPORT &
ERROR
12203A
HEWLETT PACKARD
12203-60011
D-12203-60011-62

REVISION RECORD			
A	AS ISSUED PCO 22-7407	JH/	1-2-85

D-12203-60011-83

-2789
74F153
U0207

39A CA.MP.IN7+ (70)

(70)
(233)
(498)
(451)
(56)

1C0 1C1 1C3 1C4 1Y
2C0 2C1 2C2 2C3 2Y
A B
1G 2G
1 15

CA.FORCE.CODE+ (375) 30A
CA.TRUE.BOOT+ (450) 37A

29E CA.NO.HOLDS- (498)

149C CA.DELAY.BOOT+ (351)

-3275
825153
U0804

119E 120B 140C 168C CA.INDIRECT- (58) 0
119A 80C 90C 120A CA.RRR.HIT- (28) 7
29E 90C 100B 110A 120A 185B CA.DMA.CYCLE- (27) 6
109A 110C CA.DMA.REQ+ (240) 5
149C 50E 90B 100B 110C CA.F3+ (38) 4
89E CA.CODE.SPO (348) 3
149D CA.DELAY.CODE+ (353) 2
89E CA.BOOT.SFG- (344) 1

I7 I6 I5 I4 I3 I2 I1 I0
89 88 87 86 85 84 83 82 81 80

CA.CODE.REQ+
CA.BOOT.IF.IND+
CA.BOOT.NO.IND+
(78)
(77)

CA.DLY.CODE.28+ (258) 140D
CA.DLY.BOOT.28+ (357) 150D

CPLIO

80B 158A 120B 140E BP.UIR.REG+

-0683
74S04
U0403

13 12
CA.PULLUP+ (21) 30E 50D 100E 110A 120A

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

-0881
74S00
U1601

-2693
74F109
U1401

PR J Q K Q̄ CLR

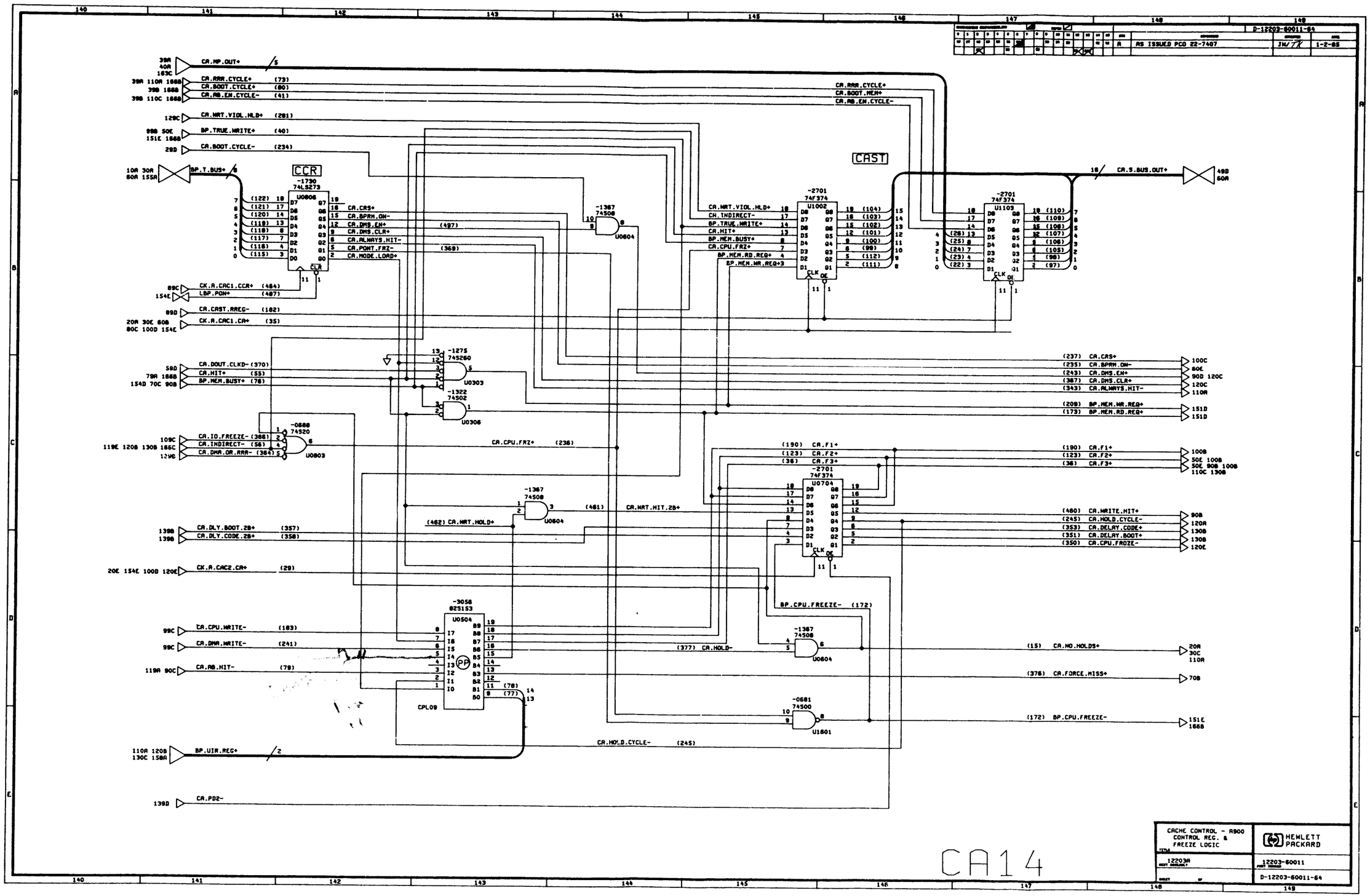
VCC+
0698-1184 R5 2.15K
0698-0084 R4 2.15K
0698-0084 R3 2.15K

CA.PD1-
CA.PD2-
CA.PD3-

U0101
74LS04
1820-1199

CA13

CACHE CONTROL - A900 SPO DELAY	HEWLETT PACKARD
12203A	12203-60011
	D-12203-60011-83


CA.MP.OUT+
CA.RRR.CYCLE+ (73)
CA.BOOT.CYCLE+ (80)
CA.RB.EN.CYCLE- (41)
CA.WRT.VIOL.HLD+ (281)
BP.TRUE.WRITE+ (40)
CA.BOOT.CYCLE- (234)
CCR
-1730
74LS273
U0606
CA.CRS+
CA.BPRM.ON-
CA.DMS.EN+ (497)
CA.DMS.CLR+
CA.ALWAYS.HIT-
CA.PONT.FRZ- (368)
CA.MODE.LOAD+
BP.T.BUS+
CK.A.CAC1.CCR+ (484)
LBP.PON+ (487)
CA.CAST.RREG- (182)
CK.A.CAC1.CA+ (35)
CAST
-2701
74F374
U1002
U1103
CA.WRT.VIOL.HLD+
CH.INDIRECT-
BP.TRUE.WRITE+
CA.HIT+
BP.MEM.BUSY+
CA.CPU.FRZ+
BP.MEM.RD.REQ+
BP.MEM.WR.REQ+3
CA.S.BUS.OUT+
-1367
74S08
U0604
-1275
74S260
U0303
-1322
74S02
U0306
-0688
74S20
U0803
CA.DOUT.CLKD- (370)
CA.HIT+ (55)
BP.MEM.BUSY+ (78)
CA.IO.FREEZE- (386)
CA.INDIRECT- (56)
CA.DMA.OR.RRR- (384)
CA.CPU.FRZ+ (236)
CA.DLY.BOOT.28+ (357)
CA.DLY.CODE.28+ (358)
CK.A.CAC2.CA+ (29)
-3056
82S153
U0504
CPL09
CA.CPU.WRITE- (183)
CA.DMA.WRITE- (241)
CA.RB.HIT- (79)
BP.UIR.REG+
CA.PD2-
CA.WRT.HIT.28+ (481)
(462) CA.WRT.HOLD+
-2701
74F374
U0704
-0681
74S00
U1601
BP.CPU.FREEZE- (172)
(377) CA.HOLD-
CA.HOLD.CYCLE- (245)
(237) CA.CRS+
(235) CA.BPRM.ON-
(243) CA.DMS.EN+
(387) CA.DMS.CLR+
(343) CA.ALWAYS.HIT-
(208) BP.MEM.WR.REQ+
(173) BP.MEM.RD.REQ+
(190) CA.F1+
(123) CA.F2+
(36) CA.F3+
(480) CA.WRITE.HIT+
(245) CA.HOLD.CYCLE-
(353) CA.DELAY.CODE+
(351) CA.DELAY.BOOT+
(350) CA.CPU.FROZE-
(15) CA.NO.HOLDS+
(376) CA.FORCE.MISS+
(172) BP.CPU.FREEZE-
CA14
CACHE CONTROL - A900
CONTROL REG. & FREEZE LOGIC
HEWLETT PACKARD
12203A
12203-60011
D-12203-60011-64
D-12203-60011-84
A AS ISSUED PCO 22-7407 JW 1-2-85

			D-12203-80011-65
A	AS ISSUED PCO 22-7407	JW/	1-3-85

29C BP.LOG.ADDR+

9	(323)	P1-05A	BP.LOG.ADDR9+
8	(322)	P1-03D	
7	(321)	P1-03C	
6	(310)	P1-03B	
5	(318)	P1-03A	
4	(317)	P1-02D	
3	(316)	P1-02C	
2	(315)	P1-02B	
1	(314)	P1-02A	BP.LOG.ADDR1+

79C FP.MEM.ADDR+

23	(300)	P1-09B	FP.MEM.ADDR23+
22	(299)	P1-09A	
21	(298)	P1-08D	
20	(297)	P1-08C	
19	(296)	P1-08B	
18	(295)	P1-07D	
17	(294)	P1-07C	
16	(293)	P1-07B	
15	(292)	P1-07A	
14	(291)	P1-06D	
13	(290)	P1-06C	
12	(289)	P1-06B	
11	(287)	P1-06A	
10	(286)	P1-05D	
9	(301)	P1-33C	FP.MEM.ADDR9+

BP.T.BUS+ 10A 30A 60A 140A

BP.T.BUS15+	P1-16C	(227)	15
	P1-16B	(226)	14
	P1-15D	(225)	13
	P1-15C	(223)	12
	P1-15B	(223)	11
	P1-15A	(222)	10
	P1-14D	(220)	9
	P1-14C	(228)	8
	P1-14B	(122)	7
	P1-14A	(121)	6
	P1-13D	(120)	5
	P1-13C	(119)	4
	P1-13B	(118)	3
	P1-13A	(117)	2
	P1-11D	(116)	1
BP.T.BUS0+	P1-11C	(115)	0

LBP.AB+ 30E

LBP.AB14+	P1-29C	(473)	14
	P1-29B	(472)	13
	P1-27D	(471)	12
	P1-27C	(470)	11
	P1-27B	(469)	10
	P1-27A	(482)	9
	P1-26D	(481)	8
	P1-26C	(479)	7
	P1-26B	(478)	6
	P1-26A	(477)	5
	P1-24B	(476)	4
	P1-23D	(475)	3
	P1-22C	(474)	2
	P1-22B	(468)	1
LBP.AB0+	P1-22A	(467)	0

BP.UIR.REG+ 80A 110A 120A 130C 140E

BP.UIR.REG31+	P1-25D	(232)	31
	P1-25C	(231)	30
	P1-25B	(336)	29
	P1-25A	(335)	28
	P1-24D	(334)	27
BP.UIR.REG28+	P1-24C	(333)	26
BP.UIR.REG14+	P1-21B	(78)	14
	P1-21A	(77)	13
	P1-19D	(230)	12
	P1-19C	(332)	11
	P1-19B	(331)	10
	P1-19A	(330)	9
BP.UIR.REG0+	P1-18D	(337)	8

LBP.SC+ 30E

LBP.SC5+	P1-21D	(113)	5
	P1-21C	(494)	4
	P1-32D	(493)	3
	P1-11B	(492)	2
	P1-10C	(491)	1
LBP.SC0+	P1-09D	(490)	0

BP.S.BUS+ 60A 110B

BP.S.BUS15+	P1-39B	(114)	15
	P1-38D	(178)	14
	P1-38C	(177)	13
	P1-38B	(176)	12
	P1-37D	(219)	11
	P1-37C	(175)	10
	P1-37B	(221)	9
	P1-37A	(220)	8
	P1-35D	(219)	7
	P1-35C	(218)	6
	P1-35B	(217)	5
	P1-35A	(216)	4
	P1-34D	(215)	3
	P1-34C	(214)	2
	P1-34B	(212)	1
BP.S.BUS0+	P1-34A	(211)	0

109B	LBP.BUSY-	(74)	P1-39A
109D	LBP.CPUTURN-	(483)	P1-30B
109D	LBP.CRS-	(484)	P1-38A
109D	LBP.IAK-	(485)	P1-31D
109D	LBP.IOGO-	(486)	P1-18C
109D	LBP.RNI-	(489)	P1-31A
109D	LBP.VALID-	(305)	P1-30D
109B			

29C	BP.EXT.ADDR0+	(307)	P1-05B
29C	BP.EXT.ADDR1+	(308)	P1-05C
29D	BP.LOG.ADDR0I+	(312)	P1-01D
29D	BP.LOG.ADDR0N+	(313)	P1-01C
149C	BP.MEM.RD.REQ+	(173)	P1-39C
149C	BP.MEM.WR.REQ+	(209)	P1-39D
60D 129C	BP.MP.INT+	(174)	P1-16D
99D	BP.NO.WP+	(210)	P1-16B
99B	BP.NORMAL+	(325)	P1-17C
50E 99B 140A 166B	BP.TRUE.WRITE+	(40)	P1-17A
70A 119A	BP.AB.MIT+	(207)	P1-17B
99A	BP.S.CM.ADR+	(308)	P1-11A
149E 166B	BP.CPU.FREEZE-	(172)	P1-10D
29D	BP.DMA.CYCLE+	(496)	P1-31C
90C 110E 129C	BP.IND.INT-	(75)	P1-33A
99B	BP.INVERT+	(310)	P1-17D
109A	BP.LDOUT.EN-	(311)	P1-18A

BP.R2.UIR.REG+ 80C

BP.R2.UIR.REG23+	P1-23C	(330)	23
	P1-23B	(329)	22
	P1-23A	(328)	21
BP.R2.UIR.REG20+	P1-22D	(327)	20

P1-40D	(309)	BP.INTP+	120E
P1-40C	(324)	BP.NINC.SP1-	60A
P1-40B	(78)	BP.MEM.BUSY+	70C 90B 140D
P1-32C	(38)	BP.NO.EXECUTE-	70A 110E 120D 166B
P1-09C	(326)	BP.R2.STORE.EN-	80D
P1-01B	(179)	BP.WR.CYC-	70E
P1-10A	(35)	CK.A.CAC1.CA+	20A 30E 60B 80C 100D 140B
P1-10B	(29)	CK.A.CAC2.CA+	100D 120E 140D 20E
P1-33D	(170)	CK.A.MEM.D50.BP+	40D 50E
P1-29D	(302)	LBP.MEMGO-	100C
P1-30C	(303)	LBP.MRQ-	100C
P1-33B	(487)	LBP.PON+	140B
P1-29A	(488)	LBP.REMEM-	100A
P1-22B	(304)	LBP.SCLK-	100E
P1-33A	(495)	LBP.WE-	100E

CA15

CACHE CONTROL-A900 BACKPLANE	HEWLETT PACKARD
12203A	12203-60011
	D-12203-60011-65

Update 2 5-69/5-70

			D-12203-80011-66
A	AS ISSUED PCO 22-7407	JM/JL	1-3-85

89A 10A 40D — CA.S.BUS.IN +

15	(148)	J2-11A
14	(204)	J2-11B
13	(203)	J2-11C
12	(202)	J2-12A
11	(201)	J2-12C
10	(200)	J2-13A
9	(154)	J2-13B
8	(153)	J2-13C
7	(152)	J2-14B
6	(151)	J2-14C
5	(150)	J2-15A
4	(149)	J2-15B
3	(148)	J2-16A
2	(147)	J2-16B
1	(145)	J2-16C
0	(144)	J2-17A

29A 90A 70E 110A — CA.MADR.OUT +

14	(20)	J2-08C
13	(19)	J2-09B
12	(18)	J2-09C
11	(14)	J2-10A
10	(12)	J2-10B
9	(3)	J2-26C
8	(11)	J2-27A
7	(10)	J2-27C
6	(9)	J2-28A
5	(8)	J2-28B
4	(7)	J2-28C
3	(6)	J2-29B
2	(5)	J2-29C
1	(4)	J2-30A
0	(17)	J2-30B

50E 109E	CK.A.CAC2.B.CA -	(169)	J2-31A J2-31C
14BE 151E 70A 110E 120D 154D 50E 99B 140A 151E	BP.CPU.FREEZE -	(172)	J2-20B
	BP.NO.EXECUTE -	(39)	J2-18C
	BP.TRUE.WRITE +	(40)	J2-18A
60C 119A 79A 140C	CA.RRR.HIT+	(95)	J2-19B
	CH.HIT+	(55)	J2-20A
39A 110A 140A 39B 110C 140A 29E 90C 100B 110A 120A 130B	CA.RRR.CYCLE +	(73)	J2-05B
	CA.AB.EN.CYCLE -	(41)	J2-06B
	CA.DMA.CYCLE -	(27)	J2-17C
110E 129B 39B 140A 119E 120B 130B 140C	CA.JTAB.CREATE -	(251)	J2-18B
	CA.BOOT. CYCLE +	(80)	J2-06A
	CA.INDRECT -	(58)	J2-19C

49D 50D 70C 90A — CA.DMS +

23	(54)	J2-21A
22	(53)	J2-21B
21	(52)	J2-21C
20	(51)	J2-22A
19	(50)	J2-22C
18	(49)	J2-23A
17	(48)	J2-23B
16	(47)	J2-23C
15	(46)	J2-24B
14	(45)	J2-24C
13	(44)	J2-25A
12	(43)	J2-25B
11	(42)	J2-26A
10	(13)	J2-26B

39A 40A 140A — CA.MP.OUT +

4	(26)	J2-06C
3	(25)	J2-07A
2	(24)	J2-07C
1	(23)	J2-08A
0	(22)	J2-08B

+5 — .1 C3-C14 .1 — .1 C16-C30 .1

+5 — 33 C1 — 33 C2 — 33 C15 — 33 C31

CA 16

CACHE CNTRL - A 300 FRONT PLANE	HEWLETT PACKARD
12203 A	12203-80011-66
	D-12203-80011-66

Chapter 6
Memory Controller

6.1 Introduction

This chapter describes the block diagram and theory of operation of the memory controller (MC) card. To understand fully the operation of this microprogrammed computer, please refer to the HP 92049A RTE Microprogramming Package Reference Manual, Part No. 92049-90001.

6.2 Block Description

The memory controller circuitry is implemented on the MC card. The cache data store and interrupt logic are also contained on this card (covered in subsections on Cache Data Store and Macrointerrupts, respectively). Figure 6-1 is a block diagram of the memory controller card which is shown in Figure 6-2.

The card is divided into the following functional blocks:

Refresh Counter and Address Driver
Memory Controller State Machine
Cache Interface
Array Control
Error Detection and Correction Section
Micromachine Interface
Registers for Memory Controller Status, Parity Violation, Memory Test, and Memory Control

Subheading 6.2 is a general description of these function blocks. Subheading 6.3 describes their logical operations (theory of operation).

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

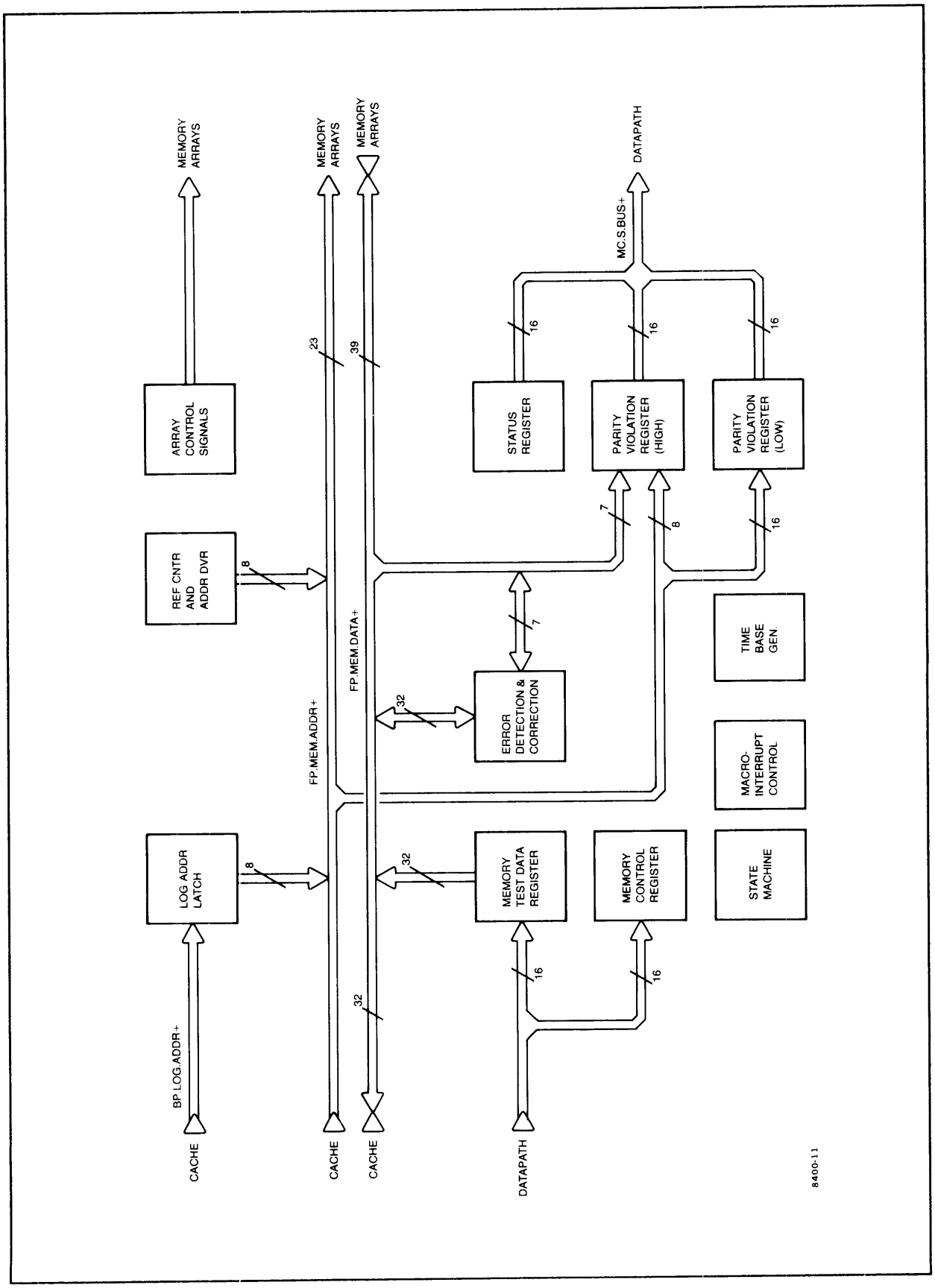


Figure 6-1. Memory Controller Card Functional Block Diagram

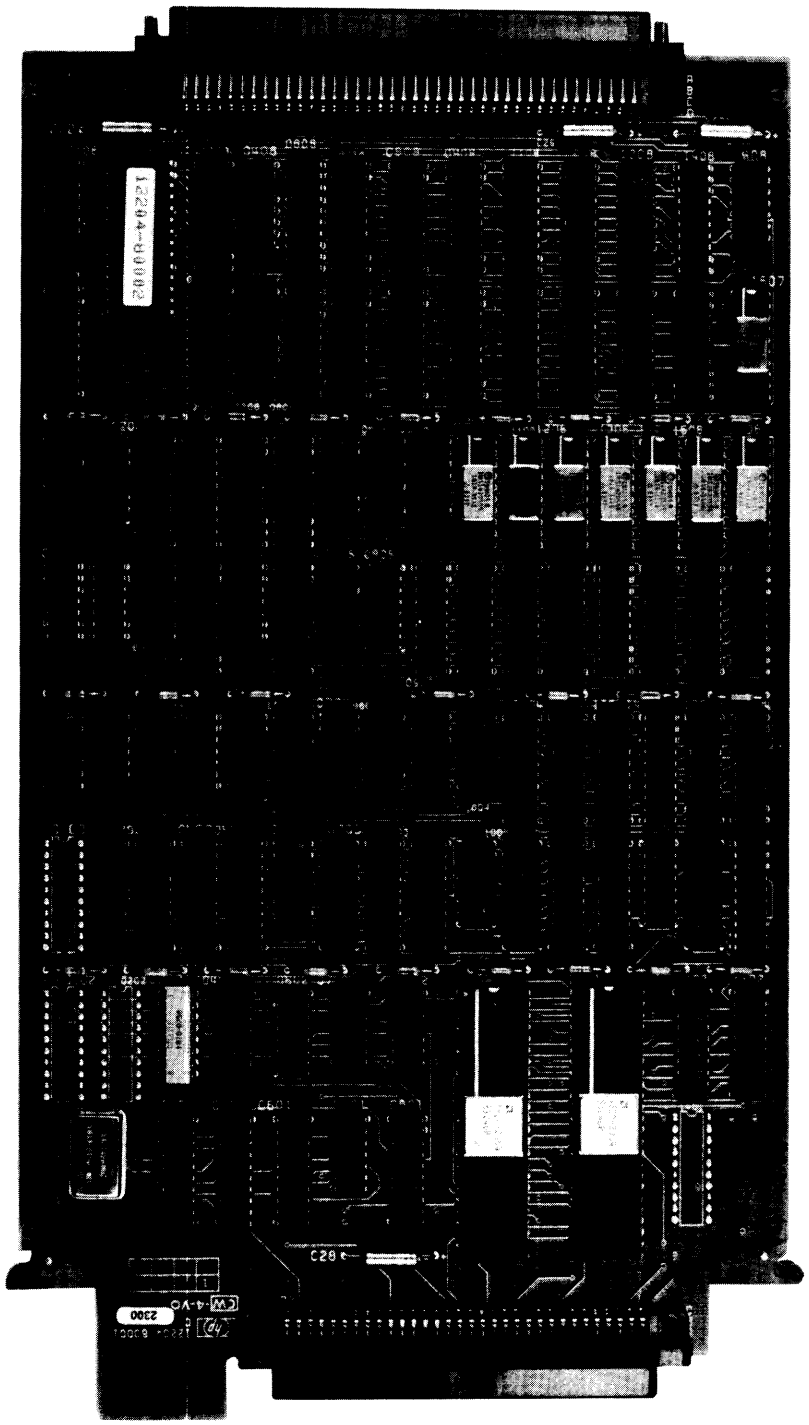


Figure 6-2. Memory Controller Card (12204-60001)

6.2.1 Initialization

To assure proper functioning of the memory controller when power first comes up, as well as when CPU power goes down (under battery backup), initialization of the memory controller must be exactly defined.

6.2.1.1 Power On

The memory controller uses the backplane signal LBP.PON+ to initialize the Memory Control Register (MCR). It is initialized to the proper value for operation while +5 CPU is down. This signal is also an input to the Memory Controller State Machine where it is used to inhibit the start of all memory reads and writes.

6.2.1.2 Memory Array Initialization

Initializing the Memory Array (AR) cards is accomplished in two phases. The first is to initialize the Bank Select RAMs (BSRs) that reside on each AR card. The second is to initialize memory itself to make sure that the checkbits match the data before attempting any memory reads.

BSRs are initialized under microcode control. The CA card drives bank addresses to the AR cards; the memory controller provides the write pulses and (indirectly) the data to write into the BSRs. The data that is written into the BSRs is passed from one AR card to the next through a chained frontplane signal that originates on the MC card. A more detailed description of the BSRs and their function may be found in the Memory Array section (Chapter 7). All of the signals necessary to initialize the BSRs are bits in the Memory Control Register (MCR). The exact microcode sequencing can be found in subsection 6.3.1.3 (Initialization Microcode).

Once the BSRs have been initialized, the dynamic RAMs are next. All physical memory locations must be initialized prior to normal memory accesses to ensure that the error correction checkbits match the data bits. If this is not done, a memory read on random data will quite probably result in a multiple-bit error. Consequently, during this initialization, multiple-bit error interrupts should be turned off. This is done by setting a bit in the MCR (refer to paragraph 6.2.7.1).

6.2.2 State Machine

The memory-controller state machine is a prime function of the control structure of the memory controller. It handles requests from the cache, makes sure that refresh cycles occur in a timely manner, and generally oversees the generation of the array control signals. Figure 6-3 shows the main features of the memory-controller state machine. Figure 6-4 is the state diagram showing the state flow.

5 state variables

MC.RD.CYC-	(MC0803 - 12, MC0903 - 5)
BP.WR.CYC-	(MC0803 - 9, MC0903 - 4)
MC.REF.CYC-	(MC0803 - 6, MC0903 - 3)
MC.STATE.CNTR1-	(MC0803 - 5, MC0903 - 2)
MC.STATE.CNTR0-	(MC0803 - 2, MC0903 - 1)

10 states

				CNTR		
name	RD-	WR-	REF-	1-	0-	
RD0	0	1	1	1	1	(IDLE state)
RD1	0	1	1	1	0	
RD2	0	1	1	0	0	
RD3	0	1	1	0	1	
WR0	1	0	1	1	1	
WR1	1	0	1	1	0	
WR2	1	0	1	0	0	
REF0	1	1	0	1	1	
REF1	1	1	0	1	0	
REF2	1	1	0	0	0	

5 inputs

MC.MEM.RD.REQ+	(RDRQ)	(MC0903 - 19)
MC.MEM.WR.REQ+	(WRRQ)	(MC0903 - 18)
MC.REF.REQ+	(RFRQ)	(MC0903 - 8)
MC.MEM.RD.ERR+	(ERR)	(MC0903 - 7)
LBP.PON+	(PON)	(MC0903 - 6)

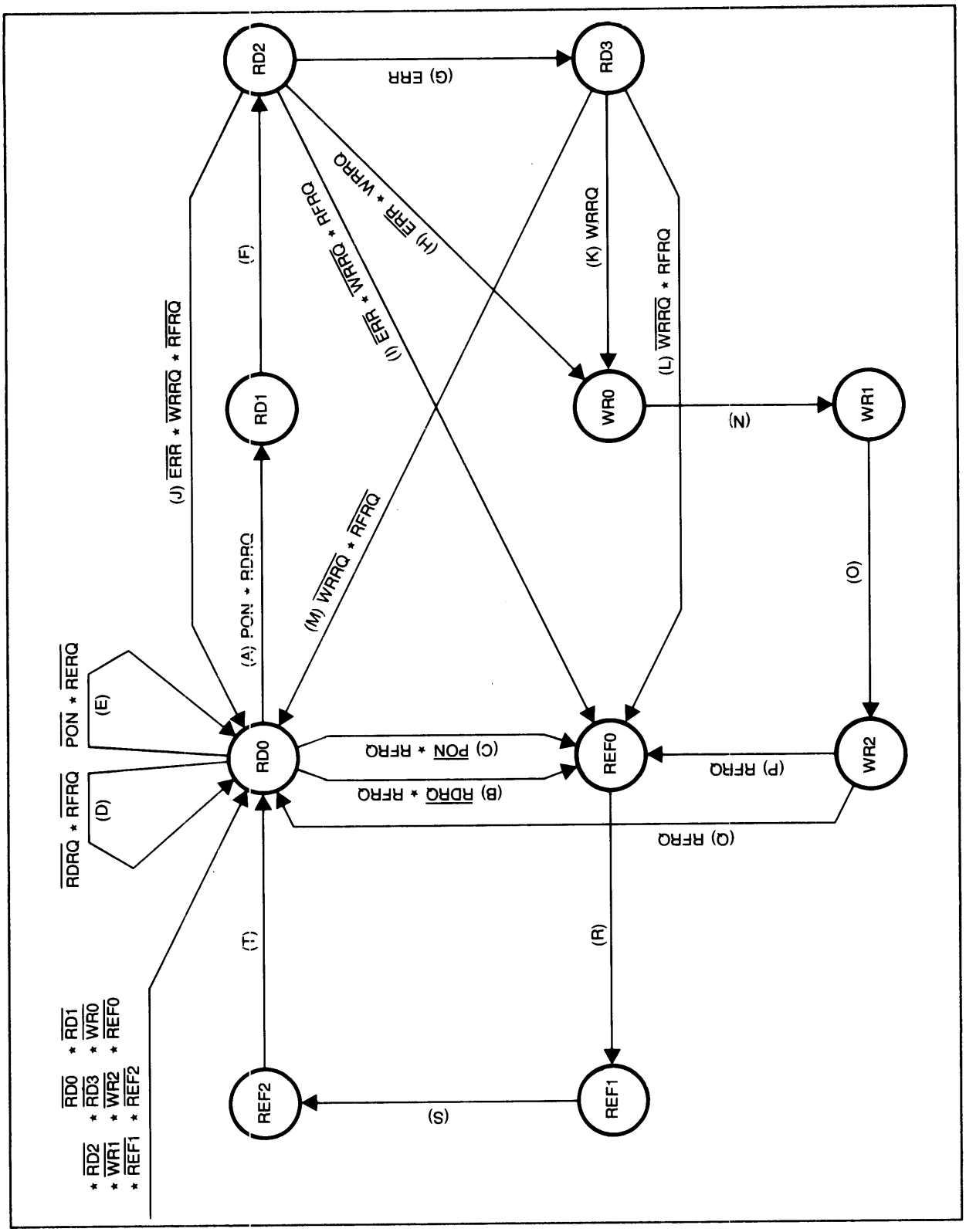
2 outputs

MC.CLR.MEM.BUSY-	(MC0803 - 19)
MC.DATA.LE-	(MC0803 - 16)

1 feedback:

MC.SELF.START+	(SS)	(MC0903 - 15)

Figure 6-3. Memory Controller State-Machine Parameters



8400-15

Figure 6-4. Memory Controller State Machine

The current state of the memory controller is defined by five state variables. The first three of these indicate which kind of operation the memory controller is currently involved in. The last two indicate which stage of this operation is in progress.

There are five input signals to the state machine. The first two are memory requests from the cache. The third is a signal from the refresh circuitry indicating that it is time for a refresh operation. The fourth is a signal from the error detection circuitry that indicates that an error has been detected on memory read data. The last signal indicates whether or not +5 CPU is up.

There are ten state machine states. The first four states deal with memory read operations, the next three deal with memory write operations, and the last three states deal with refresh operations.

The memory-controller state machine assumes that the first request will usually be a memory read request. Consequently, its "idle state" is state RD0. Another way of understanding the "idle state" is to look at it as a read operation that was aborted; anytime the state machine has nothing else to do, it begins a read operation, which is immediately aborted if a read request does not arrive by the end of that cycle.

A memory read is a four or five cycle operation; state RD3 is only executed if a read error is detected. The sequence is as follows: RD0 -> RD0 -> RD1 -> RD2 -> (RD3). The state RD3 is required to allow time to correct the error. A memory write request causes the execution of states WR0 -> WR1 -> WR2. A refresh operation causes the execution of states REF0 -> REF1 -> REF2.

In general, memory read requests have the highest priority, followed by memory writes, followed by refresh. If a refresh request occurs while a read or write request is in progress, it will be serviced before the next read request is accepted. The priority of operations are shown in the state machine flow diagram.

When PON is deasserted, only refresh requests are started. Any operation that is in progress when PON deasserts will be completed, so that the dynamic RAM contents will not be scrambled, but after that only refresh requests will be honored until PON is asserted again.

6.2.3 Cache Interface

All memory read and write requests come from the cache, as do the associated address bits, and all data is transacted solely with the cache. The memory-controller/cache interface is described in the following paragraphs.

6.2.3.1 Request Protocol

There are three signals involved in the request protocol: MEM.RD.REQ, MEM.WR.REQ, and MEM.BUSY.

MEM.BUSY changes on microcycle boundaries. It is asserted by the memory controller during all microcycles in which a request is being processed. The deassertion of MEM.BUSY means that the memory-controller state machine has entered its "idle state" (RD0), and is ready to accept new requests.

Shortly before a microcycle boundary, MEM.RD.REQ is asserted by the cache to place a memory read request. The cache understands that this request will not be processed until all previous requests have been serviced as indicated by the deassertion of MEM.BUSY. Therefore, it waits until MEM.BUSY is deasserted to place its memory read request. If MEM.RD.REQ is asserted in the same microcycle that MEM.BUSY was deasserted, that cycle is transformed from the "idle state" into the first state of a memory read operation - with no intervening dead cycles. (If you choose to look at the "idle state" as an aborted read, this simply means that the request arrived in time to avoid the abortion.)

MEM.WR.REQ only occurs in conjunction with a memory read request. This corresponds to a cache "replacement cycle" and reflects the fact that the only time the cache requests a write is when it wants to replace modified cache data with read data. Since the read data is more important to the cache than the outgoing write data, the memory read request is serviced first. The associated write request is placed simultaneously with the read request and is cleared when the write operation begins immediately following the read operation.

6.2.3.2 Address Sources

The cache generates a 24-bit physical address with each memory request. Address bits 1 through 8 are held in the logical address latch during read and write operations. Bits 9 through 23 are held in separate read address and write address latches on the cache card. When the memory controller is processing a read or write request it enables the logical address latch and the proper CA address latch (read or write) to drive the address across the frontplane to the AR cards. Memory address bits 1 through 8 are also sourced by the refresh address driver during refresh cycles.

6.2.3.3 Data Flow

The Cache Data Store RAMs are bidirectionally connected to a 32-bit cache data bus. Memory read data from the memory controller goes through drivers onto this bus, and memory write data from this bus is held in latches until the memory controller is ready for it. The memory controller to cache data drivers are under control of the cache and are separately controlled (upper and lower 16 bits) for use in cache writes that merge in 16 bits of CPU or I/O data. The cache-to-memory-controller data registers are loaded by the cache prior to placing a memory write request. The memory controller enables them onto its data bus during memory write operations.

6.2.4 Array Control

The memory array (AR) cards in the system are controlled solely by the memory controller. The assertion of the Row Address Strobe (RAS) starts a RAM access on the AR cards. The memory controller asserts RAS at the beginning of the second microcycle of all AR operations. (The first cycle of each operation allows the appropriate address to reach the AR cards.) A second signal, Write Enable (WE), indicates that the operation is a memory write, and occurs simultaneously with RAS during memory write cycles. The signal ReaD ENable (RD.EN) gives permission to the selected AR card to drive memory read data onto the frontplane data bus. The fourth signal, REFresh ENable (REF.EN), is asserted during refresh cycles to inhibit the generation of the Column Address Strobe (CAS) on the AR cards.

6.2.5 Error Detection and Correction

Error correcting memory is the standard type used in the A900. The necessary logic resides on the memory controller card. Two 16-bit Error Detection and Correction (EDC) chips form the basis of this circuitry. During memory write operations the 32 bits of data from the cache are sent through the EDC logic which generates seven checkbits. These are merged with the 32 data bits and sent across the frontplane data bus to be stored on an AR card. When a memory read operation occurs, these 39 bits are sent back across the frontplane data bus to the memory controller. All 39 bits are then sent through the EDC logic which internally regenerates what the seven checkbits should be and compares them to the checkbits that it actually got from the AR card. The result of this comparison is called the syndrome.

6.2.5.1 Single Bit Errors

The checkbits for each 32-bit pattern are chosen so that the syndrome reveals useful information about any errors that are detected. If the error is a single-bit error, the syndrome can be decoded to see which bit is wrong. The EDCs do this, and correct the error. Time is allowed for this by extending an "erring memory read" operation one additional microcycle - state RD3. All other system clocks are paused for this time; they need not be aware that an error ever occurred.

6.2.5.2 Multiple Bit Errors

Multiple bit errors are not correctable. The best that can be done is to detect their presence and interrupt the processor. The EDC chips are designed to detect all two-bit errors; if more than two bits are wrong, almost anything can happen.

If the error is a double-bit error, the syndrome indicates that an uncorrectable error has occurred. The read operation is extended an additional microcycle, but no data correction is attempted.

If more than two bits are wrong, the results are less predictable. Sometimes this type of error goes undetected, while some of them are properly detected as uncorrectable errors, and others imitate single-bit errors where attempted corrections introduce additional errors.

However, the probability of any error at all is actually quite low, with single-bit errors being many times more likely than any other type. Double-bit errors are next, commonly being the combination of a "hard" error (like a dead RAM) and a "soft" error (like a temporary error caused by an alpha particle). Errors of more than two bits are so rare that their unpredictable effect on the EDC circuitry can safely be ignored.

6.2.5.3 Preventive Maintenance

An important part of any error correcting system is regular Preventive Maintenance (PM). As an illustration, let's assume that one RAM in a system dies. The EDC circuitry can compensate for this problem, but if another single-bit error of any kind occurs in the same doubleword as the dead RAM and combines with it to create a double-bit error, the EDC circuitry can no longer correct the error. This is where a regular PM schedule is important so that a dead RAM will be found and replace before it can become part of an uncorrectable multiple bit error.

When any error is detected by the EDC circuitry, the memory read address (physical address) and the syndrome are latched into the Parity Violation Register (PVR). Reading and clearing this register on a regular basis will show the location of dead or dying RAMs that would be wisely replaced at the next PM. If the error is not correctable, further latching is disabled, and an interrrupt is sent to the interrupt logic. This interrupt is cleared by clearing the PVR.

6.2.6 Dynamic RAM Refresh Operation

Dynamic RAMs lose their information in a few milliseconds if the contents are not renewed. This renewal process, called refreshing, is provided by the memory controller.

The 64k-bit dynamic RAMs are compatible with 256k-bit dynamic RAMS in organization and refresh timing (2 milliseconds and 4 milliseconds, respectively). In operation, the memory controller keeps track of which row to refresh and when to refresh. One row of cells in each dynamic RAM in the system is refreshed during each refresh operation. After the proper number of microcycles, the refresh timer informs the memory-controller state machine that a refresh cycle needs to be performed. This operation will begin, in the worst case, eight microcycles later.

Regardless of when the refresh request is actually serviced, the refresh timer starts its count over again at two microcycles after the request was placed.

6.2.7 Micromachine Interface

Besides the cache and memory arrays, the memory controller occasionally needs to communicate with the rest of the processor. This is accomplished through four registers: the Memory Control Register (MCR), the Memory Test Data Register (MTDR), the Parity Violation Register (PVR), and the Memory Controller Status Register (MCST). The first two receive data from the TBUS, and the last two send data back across the SBUS.

6.2.7.1 Memory Control Register

The MCR is loaded by coding "MCR" in the STOT field of a microinstruction. It is a 16-bit register used for control and testing of the memory controller. The MCR bits are the following:

Bit	Application
0 - 7	Performs diagnostic testing of the memory controller circuitry (refer to paragraph 6.2.8).
8	Clears the top eight bits of the PVR. (These are the error syndrome and the multiple-bit error interrupt bit.)
9	Controls the clocking of the PVR.
10 - 12	Manipulates the memory array cards through microcode. This includes BSR initialization and turning the Parity Error LED on and off.
13	Controls the clocking of the MCST.
14	Generates the backplane signal SCHOD-.
15	Reserved for future use.

6.2.7.2 Memory Test Data Register

The MTDR is loaded by coding 'MTDR' in the STOT field of a microinstruction. It is a "double" 16-bit register used for driving known data patterns onto the 32-bit Memory Controller data bus for test purposes, and for driving all ones on non-existent memory reads during normal system operation.

The 16 bits of the MTDR are actually loaded into two 16-bit registers. One drives bits 31 through 16 of the MEM.DATA bus, and the other one drives bits 15 through 0. During testing, this data can be loaded into the EDC internal diagnostic latches. The other function of the MTDR is to drive all ones on a non-existent memory read. If there is ever a memory read request to an address that is beyond the end of physical memory, the memory controller, by convention, should drive a data pattern of all ones. This is done using the MTDR, which consequently should contain all ones during normal system operation.

6.2.7.3 Parity Violation Register

The PVR can be read by the micromachine by coding a "PVRL" or "PVRH" in the RREG field of a microinstruction. The PVR is a 32-bit register that holds address and syndrome data for memory errors. The upper 16 bits are PVRH and the lower 16 bits are PVRL.

When the memory controller is powered on, the PVR bits for the parity error syndrome are clear. Also MCR bits 8 and 9, which control the PVR, are clear, thus disabling PVR. Once the MCR bits 8 and 9 have been set to their normal operating state, the PVR can begin latching memory-read error information. PVRL and the lower eight bits of PVRH record the double-word

address where an error occurred. Bit "0" of the address is meaningless because the memory controller deals only with 32-bit double-words. Address bit "0" always returns a "0".

The syndrome, PVRH bits 8 through 14, can be decoded to reveal in which of the 32 bits the single-bit error occurred. If the error was more than one bit, the syndrome contains no useful information. Bit 15 of PVRH is the multiple bit error interrupt flag. When this bit is set, the state of the PVR is frozen. When this bit is clear, single-bit memory read errors overwrite each other in the PVR.

In addition to its normal use in recording the address of uncorrectable memory errors, one extended use of the PVR is the "logging" of single-bit errors. The PVR can be read and cleared on a regular basis, with its contents being stored to a disc file (and possibly the system console). This data can be reviewed to uncover hard errors before they cause uncorrectable errors that can seriously degrade system performance.

6.2.7.4 Memory Controller Status Register

The MCST can be read by the micromachine by coding "MCST" in the RREG field of a microinstruction. It gives the self-test access to the memory-controller state machine variables to verify that the state machine is operating as it should.

6.2.8 Memory Controller Self-Test

The MCR, PVR, MTDR, and MCST registers all have features that make the testing of the memory controller easy. The MCST is included specifically for self-test verification of the basic functions. The MTDR allows any 16-bit data pattern to be driven onto both halves of the FP.DATA.BUS. A CPU read that misses the cache will retrieve this data. The MCR has many diagnostic signals; e.g., MC.DIAG.LE.HI and MC.DIAG.LE.LO that allow latching data into the EDC (error detection and correction) internal diagnostic latches.

MC.DIAG.MODE transfers control of the EDCs to the MCR register. This allows many of the EDC functions and features to be tested. The syndrome and address can be accessed by the micromachine through the force-load feature of the PVR which is controlled by MCR bits (9-8): MC.FRC.PVR.CLK- and MC.PVR.CLR-.

6.3 Theory of Operation

The A900 Memory Controller (MC) card theory of operation is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 6-1 and the schematics at the end of this section of the manual. The schematic pages are referred to by a two letter card acronym followed by a page number; e.g., the schematics for the memory controller card are MC1, MC2, etc.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U0801 (MC65C) refers to part U0801 on the memory controller card in row 8/column 1, which is shown on schematic page MC6 at horizontal location 5 and vertical location C.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

6.3.1 Power On

The backplane signal LBP.PON+ initializes the Memory Control Register (MCR); it is also an input to the memory-controller state machine. The state that PON forces on MCR is one that will not interfere with the refresh operations during battery backup. Only read and write requests of the state machine are affected by a change in PON. Due to the PFW signal, the CPU places power-down routine read and write requests, finishing by the time when LBP.PON+ becomes deasserted (low). PON operations are not synchronized with the clock.

6.3.1.1 Memory Control Register

Initialization of the memory-array (AR) card Bank Select RAMs (BSR) is controlled by microcode through MCR bits 10, 11, and 12. The functions of these bits are the following:

a. Bit 12 of the MCR is MC.INIT.MODE+. Its source is pin 12 of U0703 (MC16C). It is inverted by U0402 (MC62B), creating MC.INIT.MODE- which asynchronously clears the MEM.BUSY flip-flop. This flip-flop prevents the cache logic from interfering with generation of bank addresses needed for BSR initialization. Also, MC.INIT.MODE+ is driven onto the frontplane through U0801 (MC65C) as FP.INIT.MODE+ to the AR cards where its deasserted sense clears the bank select shift register flip-flops.

b. Bit 11 of the MCR is MC.MEM.CH.IN- from U0703 (MC16C). While it is asserted low, it forces the assertion of MC.NEXT.AR.BD+ through U0305 (MC122C) for self-test verification of this signal. MC.MEM.CH.IN- is inverted by U0402 (MC17D) and is driven onto the frontplane through ~~U0801 (MC65C)~~ as ~~FP.MEM.CH.IN+~~ to the first AR card where it becomes the initial serial input to the bank-select shift register chain.

c. Bit 10 of the MCR is MC.MEM.INIT.CLK+. Its source is pin 6 of U0703 (MC16C). It is driven onto the frontplane through U0801 (MC65C) as FP.INIT.CLK+ to the AR cards where it is used to clock the bank-select shift register and write the BSRs.

6.3.1.2 Memory Array LED Control

Another use of the MCR initialization bits is turning "on" and "off" the memory error LED on the AR cards. This LED is lit on all of AR cards as a side effect of BSR initialization. When a multiple-bit error is encountered, part of the interrupt code includes a microcode sequence that turns "off" the LED on the AR card that had the error. This is done by toggling MC.INIT.MODE which clocks a type "D" flip-flop on the AR cards. When this flip-flop is set, the LED on that card is not lit. The data input to this flip-flop is AR.BD.SEL which indicates whether or not a particular card is being addressed. For this to occur, the address of the desired card must be present on the frontplane.

6.3.1.3 Initialization Microcode

When CPU power "comes up", one requirement is to initialize the BSRs on the AR cards. Three things are required: addresses, data, and write pulses.

The address inputs of the BSRs are connected to FP.MEM.ADDR[17:23]+. These signals are sourced by either of two address latches on the CA card. The read address latch (default) is used during BSR initialization. The write pulse is the deasserted level of MC.MEM.INIT.CLK+.

The data for the BSRs is provided by a multiple-card shift register that is implemented through a chained frontplane signal from one AR card to the next. This shift register is cleared by the deasserted level of MC.INIT.MODE+ and clocked by MC.MEM.INIT.CLK+. MC.MEM.CH.IN- provides a single pulse that is shifted through the shift register in sync with the address changes and write pulses.

As a part of this process, whenever the data pulse shifts from one AR card to another, it can be detected in the memory-controller status register (bit 15) through the open collector frontplane signal FP.NEXT.AR.BD-. This allows self-test to determine the exact memory configuration. Figure 6-5 shows the BSR initialization in a timing diagram form.

6.3.2 Memory Controller State Machine

The state machine that drives the processor's memory controller is implemented with a PLA U0903 (MC22C), and U0804 (MC26C). It involves five state variables, ten states, five inputs, two outputs, and one feedback signal that is internal to the PLA. This last signal has no external connections, but can be seen at U0903 - 15. Refer back to the diagram of Figure 6-4 that shows the relationships between the different states and how the five input signals control the state sequencing. The arrows show that there are 20 state-to-state transitions, and one special transition that assures that the state machine is self starting.

The U0903 has sufficient 'AND' terms (32) to allow the state equations to be implemented in a very straight-forward manner without being reduced. The first 20 'AND' terms each represent one of the 20 state-to-state transitions. Four more are added to allow generation of the feedback signal. These four, which represent states RD0, RD2, RD3, and WR2, along with the six 'AND' terms that represent states REF0, REF1, REF2, RD1, WR0, and WR1 are 'ORed' together using one of the 'OR' terms and fed back, inverted, to assist in self-startup. This feedback signal indicates that the state machine is not in any normal state, and that it goes to the idle state. This occurs only at power-up.

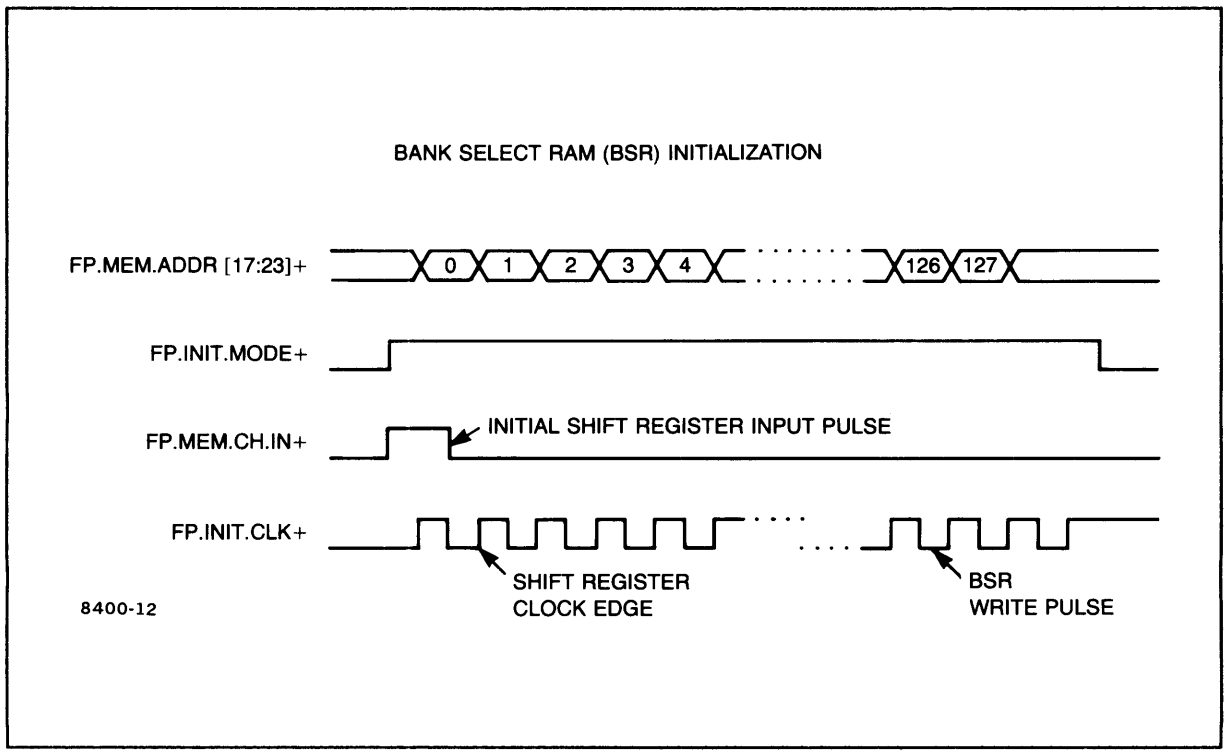


Figure 6-5. BSR Initialization Timing Diagram

In addition to the state variables, two additional signals are generated by the PLA. They are MC.NEXT.DATA.LE-, which controls the EDC chip data-latch enable, and MC.NEXT.CLR.M.B-, which controls the clearing of the MEM.BUSY flip-flop. Figure 6-6 shows the PLA coding.

Four of the states are explicitly decoded by U0504 (MC22B). The signals generated here are:

MC.RD0- (MC0504 - 7),
MC.RD1- (MC0504 - 6),
MC.RD2- (MC0504 - 4),
MC.RD3- (MC0504 - 5).

This section of the U0504 is enabled by MC.RD.CYC-, and the associated selects are driven by MC.STATE.CNTR1-, and MC.STATE.CNTR0-. Note that their order is reversed due to their "low true" nature. The other section of the U0504 is always enabled, and, having the same select input signals, decodes which state of an operation is currently underway. Even though this second set of signals do not indicate which operation is currently in progress, they prove to be useful nonetheless. A number of these signals are inverted by U0604 (MC23B). Similarly, some of the state variables are inverted by U0804 (MC26C).

6.3.3 Memory Request Signals

Memory read and write requests are transacted with the CA card through a simple protocol involving three signals: BP.MEM.RD.REQ+, BP.MEM.WR.REQ+, and BP.MEM.BUSY+. The request signals are received by the U1403 (MC125C). Both sections of this chip are clocked by CK.MEM.1.MC+, which is a version of CK.MEM.MC+ that is buffered by U1308 (MC127D).

BP.MEM.RD.REQ+ (U1403 - 2) becomes MC.MEM.RD.REQ+ (U1403 - 6) and is an input to the state machine. This memory read request is cleared by the occurrence of state RD1 as indicated by the assertion "low" of MC.RD1- at U1403-1. BP.MEM.RD.REQ+ is also connected to U1004 (MC64A) where it assists in directly generating MC.RAS. This is done to eliminate the dead cycle that can occur before a write or refresh operation. For write and refresh operations, MC.RD.CYC- and MC.STATE0+ are fed into U1004 (MC64B) to detect when the RAS flip-flop should be set.

```
symbols (FPLA inputs)

RD    = MC.RD.CYC-                      RDRQ = MC.MEM.RD.REQ+
WR    = BP.WR.CYC-                      WRRQ = MC.MEM.WR.REQ+
RF    = MC.REF.CYC-                     RFRQ = MC.REF.REQ+
S1    = MC.STATE.CNTR1-                 ERR  = MC.MEM.RD.ERR+
S0    = MC.STATE.CNTR0-                 PON  = LBP.PON+
                                        SS   = MC.SELF.START+
'AND' terms:

A = state RD0 *  PON  *  RDRQ
B = state RD0 * -RDRQ *  RFRQ
C = state RD0 * -PON  *  RFRQ
D = state RD0 * -RDRQ * -RFRQ
E = state RD0 * -PON  * -RFRQ
F = state RD1
G = state RD2 *  ERR
H = state RD2 * -ERR  *  WRRQ
I = state RD2 * -ERR  * -WRRQ *  RFRQ
J = state RD2 * -ERR  * -WRRQ * -RFRQ
K = state RD3 *  WRRQ
L = state RD3 * -WRRQ *  RFRQ
M = state RD3 * -WRRQ * -RFRQ
N = state WR0 *
O = state WR1 *
P = state WR2 *  RFRQ
Q = state WR2 * -RFRQ
R = state REF0
S = state REF1
T = state REF2
U = state RD0
V = state RD2
W = state RD3
X = state WR2
Y = -SS

'OR' terms (FPLA outputs):

MC.NEXT.RD.CYC  = A + D + E + F + G + J + M + Q + T + Y
MC.NEXT.WR.CYC  = H + K + N + O
MC.NEXT.REF.CYC = B + C + I + L + P + R + S
MC.NEXT.ST.CTR1 = F + G + O + S
MC.NEXT.ST.CTR0 = A + F + N + O + R + S
MC.NEXT.CLR.M.B = J + M + Q + T + Y
MC.NEXT.DATA.LE = A + H + K
MC.SELF.START   = F + N + O + R + S + T + U + V + W + X
```

Figure 6-6. State Machine U0903 PLA Code

mc 22c

BP.MEM.WR.REQ+ (MC1403 - 14) becomes MC.MEM.WR.REQ+ (MC1403 - 10) and is also an input to the state machine. This memory write request is cleared by the execution of a memory write operation as indicated by the assertion low of MC.WR.CYC- at U1403 - 15.

The signal MC.MEM.BUSY is generated by U0602 (MC65B). It is clocked by CK.MEM.1.MC+ at U0602 - 12. This flip-flop is set whenever the memory controller begins processing a request. For read and write operations it is set using the MC.SET.RAS signal; for refresh operations the signal MC.REF.REQ.PEND is used. These two signals are 'ORed' together by U0603 (MC64B) to create MC.SET.MEM.BUSY+. Note that for refresh operations, MEM.BUSY is actually set one cycle before the state machine moves to state REF0. This is necessary in case a read request occurs as the state machine in moving to state REF0.

The MEM BUSY flip-flop is cleared by a rising clock edge that occurs while MC.CLR.MEM.BUSY- at pin 13 of U0602 is asserted low. MC.CLR.MEM.BUSY is the 'AND' of MC.NEXT.CLR.M.B and not MC.SET.MEM.BUSY. MC.NEXT.CLR.M.B is generated by the state machine as the PLA-internal 'OR' of the AND terms that represent the six state transitions that return the state machine to the IDLE state (RD0).

6.3.4 Memory Address Sources

Addresses for memory read and write operations are generated on the CA card as 24-bit physical addresses. Because the memory deals strictly in 32-bit quantities, bit 0 of this address is not relevant to memory operations, and in fact, the AR cards never see this address bit.

The low-order address bits, FP.MEM.ADDR+ (bits (-1), are used as the row address for the RAMs. Since the row address is used first, they need to be fast. Fortunately, these bits do not need to go through the DMS maps. They are clocked into a register on the CA card, and sent directly onto the backplane as BP.LOG.ADDR+ (bits 8-1) to the MC card where they are latched into the logical address latch which is U0401 (MC37D).

The logical address latch drives frontplane signals FP.MEM.ADDR+ (bits 8-1). The latching occurs during state RD0. Since BP.LOG.ADDR (bits 8-1) is valid by the end of the cycle in which the read request arrives, using MC.RD0+ assures that the inputs to the logical address latch have been stable for a full cycle before the latch closes. Since write requests only occur following read requests as the second part of a cache replacement cycle, these lower address bits are valid for both the read and its associated write. The enable signal for this latch is MC.REF.CYC+. This signal enables the latch whenever the bus's only other source, the refresh address driver, is disabled.

The other source for the low-order address bits is the refresh counter, U0701 (MC35C). MC.REF.CNTR+ bits 7 - 0 are driven onto the frontplane as FP.MEM.ADDR+ (bits 8 - 1) through the refresh address driver, U0601 (MC37C). This driver is enabled by MC.REF.CYC- which only occurs during refresh operations.

The high-order address bits, FP.MEM.ADDR+ (bits 9 - 23), come from the the read address latch or the write address latch, both of which reside on the CA card. They are enabled onto the frontplane address bus by opposite senses of BP.WR.CYC- which is generated on the MC card. These upper address bits are routed out to the AR cards through the MC frontplane.

6.3.5 Memory Data Flow

Actual data transactions with the cache are performed through the Read Data Register (RDR) and the Write Data Register (WDR):

The RDR is separated into two words: data bits 31 - 16, and data bits 15 - 0. The upper RDR word is handled by U1305 (MC76B) and U1505 (MC76C). Similarly, the lower RDR word is also processed by U1404 (MC86B) and U1204 (MC86C). The two words are enabled separately to allow data merging with sixteen bits of CPU or I/O data. They are controlled by the cache.

The WDR is also separated into an upper word and a lower word. The upper WDR word is stored in U1205 (MC77B) and U1405 (MC77C). The lower WDR word is stored in U1504 (MC87B) and U1104 (MC87C). The loading of the WDR is controlled by the cache. Their contents are enabled onto the FP.MEM.DATA+ bus by MC.WR.CYC- during write operations.

The RDR and WDR connect the frontplane memory data bus with the two 16-bit buses that are connected directly to the cache data-store RAMs and the cache DIN and DOUT register sets.

6.3.6 Memory Array Control

The memory array cards are controlled by the memory controller. During normal operation (not initialization), this is accomplished through the use of four frontplane signals: FP.RAS-, FP.WE-, FP.RD.EN+, and FP.REF.EN-.

6.3.6.1 Signal FP.RAS-

The RAS flip-flop is U0602 (MC65A). It is clocked by a buffered version of the memory controller's copy of the microcycle clock: CK.MEM.1.MC+. It is used in the inverted configuration to accommodate the "low true" output of U1004 (MC64A) which is used to set it.

The RAS flip-flop is set at the beginning of the second microcycle of all memory operations. For write and refresh operations, this is done by ANDing MC.RD.CYC- (i.e., write or refresh cycle) with MC.STATE0+ in U1004 (MC64A). This causes MC.SET.RAS- to be asserted "low" at the K-bar input to the RAS flip-flop so that the next microcycle clock edge will assert MC.RAS- "low" at pin 6.

The other condition that asserts MC.SET.RAS- "low" is when BP.MEM.RD.REQ+ is asserted "high" at the end of a RD0 state while LBP.PON+ is asserted "high". LBP.PON+ is needed because when CPU power is down, the RAS flip-flop must be set during refresh operations, and BP.MEM.RD.REQ+ is not guaranteed while CPU power is questionable. U0904 (MC62A) ANDs MC.RD0+ with LBP.PON+ to generate MC.RD0.PON+. This signal is used to qualify BP.MEM.RD.REQ+ in U1004 (MC64A) in the generation of MC.SET.RAS-.

The RAS flip-flop is cleared by the second half of states RD2, WR2, and REF2. MC.STATE.CNTR1+ and CK.MEM.B.MC- are NANDed in U0603 (MC63A) to generate MC.CLR.RAS-. This signal pulses the preset input of the RAS flip-flop to clear it when in the inverted state. MC.RAS- is driven onto the frontplane as FP.RAS- through U0801 (MC65C).

6.3.6.2 Signal FP.WE-

FP.WE- is a gated copy of FP.RAS- that occurs only during memory write operations. MC.WE- is generated by ORing MC.RAS- with MC.WR.CYC- in U0702 (MC63C). It is then driven onto the frontplane through U0801 (MC65C) as FP.WE-.

6.3.6.3 Signal FP.RD.EN+

During error correction of memory read data it becomes necessary to inhibit the AR cards from driving the frontplane data bus so that the error correction chips can drive the corrected data. This is the reason for the signal FP.RD.EN+. The AR cards are allowed to drive data onto FP.MEM.DATA+ (bits 38-0) only while this signal is asserted high.

The RD.EN Latch is a cross-coupled pair of gates of U0104 (MC52B). It is set by the assertion "low" of MC.RD1- at pin 5. It is cleared by the assertion low of MC.CLR.RD.EN- at pin 1. This signal becomes asserted "low" whenever a new operation is started, as signalled by the assertion "high" of MC.STATE0+ at pin 6 of U0203 (MC51B), or when a memory read error is detected as signalled by the assertion "high" of MC.MEM.RD.ERR+.

U0203 (MC53C) generates MC.MEM.RD.ERR+ as the NOR of BP.PE.FREEZE- and CK.MEM.B.B.MC+. CK.MEM.B.B.MC+ is included because BP.PE.FREEZE- is not valid during the first half of state RD2. This logic implementation has been chosen to minimize the delay from the EDC error condition output to the clock pausing circuitry through BP.PE.FREEZE-. U0702 (MC51C) is used to assure that BP.PE.FREEZE- is only asserted during a state RD2 that has activated a memory array card; non-existent memory read requests will not cause a clock freeze.

6.3.6.4 Signal FP.REF.EN-

The memory array control signal FP.REF.EN- inhibits the column address strobe (CAS) during refresh operations It is generated as the OR of MC.REF.CYC and not LBP.PON in U0904 (MC63D). LBP.PON is included to force FP.REF.EN asserted while CPU power is down in order to minimize +5M powered parts on the AR cards. MC.REF.CYC- is driven onto the frontplane as FP.REF.EN- through U0801 (MC65C).

6.3.7 Error Detection and Correction

The error correction memory system for the A900 is implemented by a pair of LSI Error Detection and Correction chips (EDCs) that use a modified Hamming code.

6.3.7.1 EDC Chips

The EDCs chips are combinatorial in nature with internal latches and tri-state outputs. The chips are 48-pin DIPs with the following inputs and outputs:

a. 16 bidirectional data lines (latched in both directions and output enabled on a per byte basis).

b. Seven checkbit (CB) inputs (latched).

c. Seven syndrome/checkbit (SC) outputs (output enabled).

d. Six latching and output enable control signals.

e. Eight control and configuration inputs.

f. Two error condition outputs.

Each EDC handles one 16-bit data word so two chips process the 32-bits. The check bits are handled in a "parallel/feedback" fashion as follows:

a. The EDC-0/1 that deals with bytes 0 and 1 has its SC outputs permanently enabled; they drive the CB inputs of the EDC that deals with bytes 2 and 3 (EDC-2/3).

b. EDC-2/3 drives the generated checkbits to the memory arrays during write operations, and drives the syndrome to the parity violation register during error correction.

c. EDC-0/1 receives the returning checkbits from the memory arrays during read operations, and receives the feedback syndrome from EDC-2/3 during error correction. This feeding back of the syndrome is necessary so that EDC-0/1 can correct a wrong bit in byte 0 or 1.

The EDC input latch enable, pin 6, is driven on both EDCs by MC.EDC.DATA.LE+. The EDC diagnostic latch enable, pin 7, controls an internal EDC latch. This latch, containing substitute checkbits and control bits, is driven on EDC-0/1 by MC.DIAG.LE.LO+, and on EDC-2/3 by MC.DIAG.LE.HI+.

The output latch enable , pin 19, is tied "high" on both EDCs by MC.PULLUP+. The data output enables, pins 8 and 18, are driven on both EDCs by MC.EDC.DATA.OE-. The SC output enable, pin 31, is tied to ground on EDC-0/1, and driven by MC.EDC.SC.OE- on EDC-2/3. This signal is inverted by U0402 (MC41C); MC.EDC.SC.OE+ enables the Checkbit Receiver onto MC.SYNDROME+. Note that the two tri-state sources for this bus are enabled by opposite senses of the same signal to preclude prolonged contention.

The SC outputs of EDC-2/3 are driven onto FP.MEM.DATA[38:32]+ by the Checkbit/Syndrome Driver, U1402 (MC48C). This path serves two functions: checkbits are driven to the AR cards during memory write operations, and the error syndrome bits are driven to the PVR to be latched for error logging purposes. These two conditions are ORed in U0904 (MC48E).

The two "diagnostic mode" control inputs, pins 46 and 47, and the "pass through" control input, pin 48, are tied to ground on both EDCs. Similarly, the "correct" control input, pin 1 is tied "high" through MC.PULLUP+. The "generate" control input, pin 42, is driven, on both EDCs by MC.EDC.GEN-. The last three control inputs are the "code id" control inputs as follows:

a. For EDC-0/1 the CODE ID is "010" for processing bytes 0 and 1 in a 32-bit memory system.

b. For EDC-2/3 the CODE ID is "011" for processing bytes 2 and 3 for a 32-bit system.

For additional information on the EDCs, refer to the data sheet for the AM2960 (Advanced Micro Devices Inc., Sunnyvale Calif.).

The EDC Control MUX is U1003 (MC45E). This MUX selects the source of the four dynamic EDC control signals:

MC.EDC.GEN- (pin 12)
MC.EDC.DATA.OE- (pin 9)
MC.EDC.DATA.LE+ (pin 7)
MC.EDC.SC.OE- (pin 4)

The Memory Control Register (MCR) includes the signal MC.DIAG.MODE+ which drives the select input (pin 1) of the EDC Control MUX. In the diagnostic mode (MC.DIAG.MODE+ asserted "high"), these four EDC control signals are supplied by MCR bits 5 - 2 where normally they are controlled by the state machine.

6.3.7.2 Checkbit Generation

During memory write operations, the function of the EDCs is to generate the seven checkbits that accompany the 32 data bits out to the addressed memory array card for storage. The operation is as follows:

a. The Write Data Register (WDR) is enabled onto the frontplane data bus during states WR0, WR1, and WR2.

b. This WDR data is latched into the EDCs during state WR0.

c. The EDCs combinatorially compute the correct checkbits for this particular data pattern.

d. The SC outputs of EDC-2/3 pass these checkbits to the Checkbit/Syndrome Driver which drives them onto the frontplane checkbit bus, FP.MEM.DATA+ (bits 38 - 32).

e. FP.MEM.DATA+ (bits 38 - 0) is received by the data transceivers on the correct memory array card, and presented to the RAMs.

The WDR was loaded with the write data by the cache prior to its placing the memory write request. This register is a set of four chips (U1405, U1104, U1205, and U1504). They are enabled by the assertion of MC.WR.CYC- at pin 1. This signal remains asserted throughout the memory write operation which is defined by states WR0, WR1, and WR2.

For the duration of state WR0, the state machine asserts MC.DATA.LE- at pin 5 of the EDC Control MUX, which drives MC.EDC.DATA.LE+ to both EDCs. This opens the data input latch of the EDCs for this microcycle so that the WDR data can begin propagating through the EDCs. When the state machine moves to WR1, MC.DATA.LE- is deasserted, latching the data. MC.DATA.LE- also generates MC.EDC.SC.OE- at pin 4 of the EDC Control MUX.

During normal operation MC.EDC.DATA.LE+ and MC.EDC.SC.OE- are each asserted whenever the other is deasserted, but they can be controlled separately for testing purposes in the diagnostic mode. During WR1 and WR2, MC.EDC.SC.OE- is asserted to allow the final checkbits from EDC-2/3 to be driven through the Syndrome/Checkbit Driver across the frontplane to the memory arrays.

As for the actual computation of the checkbit pattern, each EDC first computes a partial checkbit pattern from the data bits that it receives. EDC-0/1 then drives its partial pattern to EDC-2/3 across MC.SC.CB[6:0]+ where it is combined with EDC-2/3's partial pattern to produce the final checkbits that appear on the SC outputs of EDC-2/3.

There are two other EDC control signals of concern: MC.EDC.DATA.OE-, which remains deasserted for the entire memory write operation, and MC.EDC.GEN-. This is the signal that tells the EDCs whether to generate checkbits for a write operation, or check the returning checkbits to see if they still match

the accompanying data bits. The state machine output MC.WR.CYC- is inverted by U0804 (MC26C) and sent through the EDC Control MUX to assert MC.EDC.GEN- throughout all three write operation microcycles.

6.3.7.3 Detecting and Correcting Errors

During memory read operations, the function of the EDCs is to detect, and correct if possible, any errors that may exist in the 39 bits that are returning from the memory arrays on the MEM.DATA bus. The operation is as follows:

a. The memory array is requested to send data. (39 bits)

b. The data is latched into the EDCs (All 39 bits) where error checking is commenced.

c. At the proper time, the EDC error signal is checked. If no error is detected, the cache takes the data.

d. If an error is detected, a number of things happen:
   - The clock circuitry pauses for one microcycle.
   - The selected AR card is disconnects from the frontplane data bus.
   - The EDCs, which are combinatorially computing the error syndrome and correcting the data, begin driving the frontplane data bus.

e. The correct data is received by the cache.

f. The frontplane address bus and error syndrome are clocked into the PVR along with the output of the multiple-bit error condition from EDC-2/3 that indicates an uncorrectable error. This last bit is the multiple-bit error interrupt flag that RTE knows as a parity error.

Read requests only occur during state RD0. This state is the idle state unless a read request is placed by the cache. The timing of the request is such that it occurs shortly before the end of the microcycle, just in time to generate the row address strobe for the memory array card that is being addressed. This begins the memory read operation; the assertion of FP.RAS- on the frontplane asks the selected AR card to send read data.

The read data from the AR card is latched into the EDCs by MC.EDC.DATA.LE+ which is valid for the duration of state RD1.

The error condition does not become valid until after EDC-2/3 has had time to combine its own partial syndrome pattern with partial pattern from EDC-0/1. MC.EDC.ERR- is valid beginning at the second half of state RD2. It is sourced by pin 32 of the EDC U0901 (MC46C).

U0702 (MC51C and MC53C) combines MC.RD2-, MC.AR.BD.SEL-, and MC.EDC.ERR- to generate BP.PE.FREEZE-. The clock circuitry uses the state of this signal at the end of state RD2 to pause other system clocks for one microcycle as needed. U0203 (MC53D) ANDs this clock freeze condition with an inverted microcycle clock to produce MC.MEM.RD.ERR+. The inverted microcycle clock is used to disable assertion of MC.MEM.RD.ERR+ until the BP.PE.FREEZE- signal is valid. MC.MEM.RD.ERR+ informs the state machine that state RD3 is needed, and is also used to clear the RD.EN Latch U0104 (MC53B) through U0203 (MC51B).

Clearing the RD.EN Latch tells the selected AR card to stop driving the frontplane data bus. It also causes the assertion of MC.DATA.OE+ through U0203 (MC55B). The other input to this gate is MC.WRITE.ANYWAY- (state RD2 or RD3) which defines the proper time window for the EDCs to drive the frontplane data bus. This signal is generated by U0204 (MC152B).

MC.DATA.OE+ passes through the EDC Control MUX U1003 (45E) to enable the EDCs to drive their corrected data onto the frontplane data bus. Similarly, U0904 (MC48E), the Checkbit/Syndrome Driver, is enabled onto the frontplane data bus to drive the seven-bit error syndrome to the PVR.

6.3.8 Memory Refresh

The memory controller refreshes the dynamic RAMs on the AR cards with a RAS-only access cycle. It provides the RAS pulse and row address for use by either 64k or 256k dynamic RAMs. 64k dynamic RAMs are organized as 128 rows of 512 bits each, and require each row to be refreshed at least once every 2 milliseconds. The 256k dynamic RAMs are organized as 256 rows of 1024 bits each, and require each row to be refreshed at least once every 4 milliseconds, which is compatible with the 64k dynamic RAMs.

The memory controller keeps track of which row to refresh next with an eight bit counter. Keeping track of when to refresh cycles is done by counting memory-controller clock cyles. This clock never pauses. Every dynamic RAM in the system is refreshed simultaneously, one row at a time.

6.3.8.1 Refresh Timer

The refresh timer is U0802 (MC31B) configured as an 8-bit binary counter. It is clocked by CK.MEM.B.MC- which is generated in U0804 (MC153C). When the refresh timer has counted 128 microcycles from the time its asynchronous clear was released, it asserts MC.SET.REF.REQ+. This signal causes the refresh request latch U0704 (MC33C) to set.

Signal MC.SET.REF.REQ+ also goes to U0803 (MC24C) where it is delayed one cycle to generate MC.CLR.PULSE which is ORed with MC.PULLDOWN- on the output control pin of U0803. This signal is a one cycle pulse that occurs one cycle after the refresh request latch is set. Its purpose is to asynchronously clear the refresh timer so that it can start over counting microcycles. Note that the time interval between successive refresh requests is not affected by the few cycles of delay that may occur before the refresh request is actually processed.

The REF.REQ flip-flop is cleared by the first clock edge following the assertion of MC.REF.CYC-. This is the start of the refresh operation that is satisfying the refresh request. It may occur any time from one-to-ten microcycles after the REF.REQ F/F is set.

6.3.8.2 Refresh Counter

The refresh counter is U0701 (MC35C) configured as an 8-bit binary counter for keeping track of the proper row address for refreshing the dynamic RAMs. It is clocked by MC.REF.REQ.PEND once each refresh operation and its outputs are driven onto the frontplane address bus through the refresh address driver U0601 (37C) during refresh operations.

6.3.9 Micromachine Interface

The memory controller logic includes four registers that are accessible to the micromachine: the Memory Control Register (MCR), the Memory Test Data Register (MTDR), the Parity Violation Register (PVR), and the Memory Controller Status Register (MCST). The micromachine can write to the MCR and MTDR, and it can read back the PVR and MCST.

6.3.9.1 STOT Decode

When MCR or MTDR is coded in the STOT field of a microinstruction, the current data on the TBUS is stored into the corresponding register. The proper UIR bits are decoded by U0607 (MC153D). Since the actual store occurs at the second rank of the micromachine pipeline, rank-two versions of the UIR bits are decoded: BP.R2.UIR.REG+ (bits 23 - 20). The signals resulting from this decode are MC.MCR.STOT- and MC.MTDR.STOT-; they are ORed with CK.MEM.MC+ by U0705 (MC15C and MC15D) to generate the gated clocks that the MCR and MTDR registers use to store the TBUS data.

6.3.9.2 RREG Decode

The PVR and MCST registers can be read by the micromachine by coding PVRL, PVRH, or MCST in the RREG field of a microinstruction. This microcode field is sensed by the U1607 (MC12C) that decodes BP.UIR.REG+ (bits 30 - 26) to generate MC.MCST.RREG-, MC.PVRL.RREG-, and MC.PVRH.RREG-. These signals directly enable the MCST and the two halves of the PVR onto the SBUS. The other input to the RREG decoder is BP.KIS.S.OFF-. This signal is asserted by the cache to keep the SBUS clear during clock freezes.

6.3.9.3 Memory Control Register

Table 6-1 shows the contents of the MCR. The lower eight bits reside in U1103 (MC42D):

Bit 0: MC.DIAG.MODE+, when asserted high, switches the EDC control MUX at U1003 (MC45E) so that the dynamic EDC control signals are driven by MCR bits 2 - 5 for testing purposes. It also forces the Code ID control inputs of both EDCs to "001" to utilize the EDC internal EDC diagnostic latches.

Bit 1: MC.TEST.DATA.EN+, forces the contents of the MTDR onto the frontplane data bus. This is useful for testing this bus and for providing the data to latch into the EDC diagnostic latches.

Bit 6: MC.DIAG.LE.HI+, drives the diagnostic latch enable input on EDC-2/3 for exactly this purpose; when this MCR bit is asserted "high" data flows into the latch, and deasserting it "low" latches the data in.

Bit 7: MC.DIAG.LE.LO+ provides the same function for EDC-0/1.

The top eight bits of the MCR reside in U0703 (MC16C):

Bit 8: MC.PVR.CLR-, clears the top eight bits (31 - 24) of the PVR. This clears the multiple-bit error interrupt flag (PVR bit 31) and the seven error syndrome bits. While MC.PVR.CLR- remains asserted low, multiple error interrupts are disabled.

Bit 9: MC.FRC.PVR.CLK- provides the capability to clock the PVR. A deasserted-to-asserted transition of this signal causes clocking of the PVR. A side effect of this capability is that if MC.FRC.PVR.CLK- is left asserted "low", all clocking of the PVR is disabled. Forced clocking of the PVR is useful for testing reasons because it gives the microprogrammer access to the frontplane address bus and the error syndrome bits.

Bits 10 - 12: Initializes the AR card BSRs and controls the AR card LED (refer to Memory Controller State Machine).

Bit 13: MC.MCST.CLK.EN- when asserted freezes the contents of the MCST for testing purposes.

Bit 14: MC.SCHOD- causes the assertion of SLAVE- on the I/O backplane via the I/O microcode.

6.3.9.4 Memory Test Data Register

Table 6-2 shows the format of MTDR. The MTDR is a "double" 16-bit register. BP.TBUS+ (bits 15 - 8) gets clocked into U1303 (MC16A) and U1304 (MC18A).

Table 6-1. Memory Control Register

Bit	Signal Name	Initial Value	Normal Operation
15	not used	0	?
14	MC.SCHOD-	0	1
13	MC.MCST.CLK.EN-	0	X
12	MC.INIT.MODE+	0	0
11	MC.MEM.CH.IN.-	0	0
10	MC.MEM.INIT.CLK+	0	0
9	MC.FRC.PVR.CLK-	0	1
8	MC.PVR.CLR-	0	1
7	MC.DIAG.LE.LO+	0	X
6	MC.DIAG.LE.HI+	0	X
5	MC.DIAG.GEN+	0	X
4	MC.DIAG.DATA.OE+	0	X
3	MC.DIAG.DATA.LE-	0	X
2	MC.DIAG.SC.OE+	0	X
1	MC.TEST.DATA.EN+	0	0
0	MC.DIAG.MODE+	0	0

Table 6-2. Memory Test Data Register

Bit	Signal Name	Initial Value*	Normal Operation
15	FP.MEM.DATA31, 15+	?	1
14	FP.MEM.DATA30, 14+	?	1
13	FP.MEM.DATA29, 13+	?	1
12	FP.MEM.DATA28, 12+	?	1
11	FP.MEM.DATA27, 11+	?	1
10	FP.MEM.DATA26, 10+	?	1
9	FP.MEM.DATA25, 9+	?	1
8	FP.MEM.DATA24, 8+	?	1
7	FP.MEM.DATA23, 7+	?	1
6	FP.MEM.DATA22, 6+	?	1
5	FP.MEM.DATA21, 5+	?	1
4	FP.MEM.DATA20, 4+	?	1
3	FP.MEM.DATA19, 3+	?	1
2	FP.MEM.DATA18, 2+	?	1
1	FP.MEM.DATA17, 1+	?	1
0	FP.MEM.DATA16, 0+	?	1

* Data varies according to when the test is run.

In the same way, BP.TBUS+ (bits 7 - 0) is clocked into U1105 (MC18A) and U1203 (MC18A). The MTDR needs to be 32-bits wide to be able to drive the 32 bits of the frontplane data bus. It is enabled onto this bus, FP.MEM.DATA+ (bits 31 - 0), by U1004 (MC13D) for one of two reasons: the assertion of MC.TEST.DATA.EN+ (MCR bit 1), or a nonexistent memory reference. The first case is for testing purposes, and the second case allows the memory controller to drive a known data pattern to the cache when no memory array card responds.

By convention, HP 1000 memory systems return all ones; the normal operating value of the MTDR should be all ones. The proper time to drive all ones is during states RD1 and RD2 whenever MC.AR.BD.SEL- is deasserted high. U0603 (MC11C) generates MC.RD1.OR.RD2+ which is combined with MC.AR.BD.SEL- to detect exactly this case.

6.3.9.5 Parity Violation Register (PVR)

Table 6-3 shows the format of the PVR. It is a 32-bit register that records information about memory system errors. It is split into two halves (PVRL and PVRH) for accessing by the micromachine:

a. PVRL (low) consists of U0503 (MC57A) and U0301 (MC57B).

b. PVRH (high) consists of U0605 (MC57C) and U1503 (MC55D) that is driven onto MC.S.BUS+ (bits 15 - 8) through U1603 (MC57D).

PVRL and PVRH are clocked by MC.ERR.CLK+ which is generated by U0603 (MC54E) as the NAND of MC.FRC.PRV.CLK- (MCR bit 9) and MC.NRML.ERR.CLK-. This signal is generated in U0404 (MC52E) as the NAND of three signals: MC.MULT.ERR.INT-, MC.POSSBL.ERR+, and MC.RD3.2ND.HALF+.

MC.MULT.ERR.INT- is generated by inverting PVR bit 31 in U0804 (MC52E). This signal disables further clocking of the PVR whenever a multiple bit error is encountered. MC.POSSBL.ERR+ is the NOR of MC.AR.BD.SEL- and MC.EDC.ERR- generated by U0304 (MC51D). The state of this is valid only during a particular time window; MC.RD3.2ND.HALF+ provides the correct timing for the PVR clock pulse.

Table 6-3. Parity Violation Register

Parity Violation Register (High)			
Bit	Signal Name	Initial Value*	Normal Operation
15	MC.MULT.ERR.INT+	0	0
14	MC.LCH.SYN6+	0	↑
13	MC.LCH.SYN5+	0	
12	MC.LCH.SYN4+	0	last single
11	MC.LCH.SYN3+	0	bit error
10	MC.LCH.SYN2+	0	syndrome.
9	MC.LCH.SYN1+	0	↓
8	MC.LCH.SYN0+	0	
7	FP.MEM.ADDR23+	?	↑
6	FP.MEM.ADDR22+	?	
5	FP.MEM.ADDR21+	?	address of
4	FP.MEM.ADDR20+	?	last single
3	FP.MEM.ADDR19+	?	bit error.
2	FP.MEM.ADDR18+	?	↓
1	FP.MEM.ADDR17	?	
0	FP.MEM.ADDR16	?	

Parity Violation Register (Low)			
Bit	Signal Name	Initial Value*	Normal Operation
15	FP.MEM.ADDR15+	?	↑
14	FP.MEM.ADDR14+	?	
13	FP.MEM.ADDR13+	?	
12	FP.MEM.ADDR12+	?	
11	FP.MEM.ADDR11+	?	
10	FP.MEM.ADDR10+	?	
9	FP.MEM.ADDR9+	?	
8	FP.MEM.ADDR8+	?	address of
7	FP.MEM.ADDR7+	?	last single
6	FP.MEM.ADDR6+	?	bit error.
5	FP.MEM.ADDR5+	?	↓
4	FP.MEM.ADDR4+	?	
3	FP.MEM.ADDR3+	?	
2	FP.MEM.ADDR2+	?	
1	FP.MEM.ADDR1+	?	
0	MC.GND-	0	0

* Data varies according to when the test is run.

The 16 bits of PVRL and the lower eight bits of PVRH record the address of the memory error. Their values come from the frontplane address bus, FP.MEM.ADDR+ (bits 23 - 1). Bits 8 - 14 of PVRH are the error syndrome for the detected memory error. For single-bit errors, this syndrome can be decoded to deduce which bit of the 32-bit memory doubleword had the failure. This is enough information to isolate the failure to the RAM level. Bit 15 of PVRH is the multiple error interrupt flag; it is the state of the multiple error output of EDC-2/3 at the time the PVR is clocked. Table 6-4 is a table of the error correction syndrome decoding. For single bit errors, this table will tell which bit was found to be in error. To find out which bank of RAMs is involved, look at the address in PVRH address bits 17 - 23.

6.3.9.6 MC Status Register

Table 6-5 shows the format of the Memory Controller Status Register (MCST). It is a 16-bit register that holds information about the current state of the memory controller. Its primary use is for microcode self-test. Bits 0 - 7 of the MCST are stored in in U0303 (MC124E), and bits 8 - 15 are stored in U0403 (MC124D). Both halves are clocked by a gated version of the memory system clock: CK.MEM.ST.MC+. This clocking can be halted by deasserting MCR bit 13: MC.MCST.CLK.EN-. The lower half is enabled onto the SBUS by coding MCST in the RREG field of a microinstruction. The upper half responds to either MCST or INTR in that field.

The the MCST bits have the following meanings:

Bits 0 - 4	Shows the state of the memory controller state machine in the cycle prior to the last enabled clock edge.
Bits 5 - 9	Shows the following state.
Bits 10-13	Shows the decoded versions of four possible states from the bottom five bits.
Bit 14	Stores the BP.MISSED.TICK used for testing the TBG logic.
Bit 15	Stores signal MC.NEXT.AR.BD to be read at BSR initialization.

Signal MC.NEXT.AR.BD is the OR of MC.MEM.CH.IN and FP.NEXT.AR.BD generated by U0305 (MC122C). It is read by the micromachine during BSR initialization after each FP.INIT.CLK edge to detect when the shift register pulse is passing from one card to another. It provides the capability to exactly determine the physical memory configuration - even when different sized array cards are introduced.

Table 6-4. Error Correction Syndrome Decoding

Bit In Error	Syndrome Octal	Hex	Bit In Error	Syndrome Octal	Hex
0	117	4F	20	026	16
1	112	4A	21	031	19
2	122	52	22	032	1A
3	124	54	23	034	1C
4	127	57	24	142	62
5	130	58	25	144	64
6	133	5B	26	147	67
7	135	5D	27	150	68
8	043	23	28	153	6B
9	045	25	29	155	6D
10	046	26	30	160	70
11	051	29	31	165	75
12	052	2A			
13	054	2C	32	001	01
14	061	31	33	002	02
15	064	34	34	004	04
16	016	0E	35	010	08
17	013	0B	36	020	10
18	023	13	37	040	20
19	025	15	38	100	40

Table 6-5. Memory Controller Status Register

Bit	Signal Name	Initial Value*	Normal Operation*
15	MC.NEXT.AR.BD+	?	?
14	BP.MISSED.TICK-	?	?
13	MC.RD3-	?	?
12	MC.RD2-	?	?
11	MC.RD1-	?	?
10	MC.RD0-	?	?
9	MC.NEXT.RD.CYC-	?	?
8	MC.NEXT.WR.CYC-	?	?
7	MC.NEXT.REF.CYC-	?	?
6	MC.NEXT.ST.CTR1-	?	?
5	MC.NEXT.ST.CTR0-	?	?
4	MC.RD.CYC-	?	?
3	MC.WR.CYC-	?	?
2	MC.REF.CYC-	?	?
1	MC.STATE.CNTR1-	?	?
0	MC.STATE.CNTR0-	?	?

* Data varies according to when the test is run.

6.3.10 Cache Data Store

The data store for the cache is located on the MC card and connects to the CA card via the frontplane. The cache address from the Cache Data Address Register on the MC card is transferred over the BP.LOG.ADDR8-1+ bus and is latched in U0401 (MC37D). Refer to Cache Memory and Tag Compare in the theory of operation subsection, and the Data Store subsection of the block diagram description in Chapter 5.

6.3.10.1 Data Store

To improve fault handling time, the cache can change from a 2k x 16 cache to a 1k x 32 cache. This is done by dividing the data store into two parts, the "normal" part and the "inverted" part. In the normal part, "even addresses" store data from even physical pages and "odd addresses" store data from odd physical pages. In the inverted part, "even addresses" store data from odd physical pages and "odd addresses" store data from even physical pages. This is shown in Figure 6-7.

The normal part of the data store consists of RAMs U1306, U1006, U1506 and U1406 on schematic MC7. The inverted part of data store consists of RAMs U1606, U1607, U1206, and U1106 on schematic MC8. 4k by 4-bit static RAMs are used. Only the normal case is described below since the inverted case is just mirrored with respect to physical address bit 10.

Only 1k of the 4k locations in the RAMs are used for the cache memory. Another one-quarter of the RAMs are used for Virtual Control Panel (VCP) base-page memory and general CPU scratch memory locations (2k words). The remaining half of the RAMs (4k words) are used for VCP code. This is read in from the PROMs on the CA board (RREG/BPRM) and stored in the cache data store RAMs. The reason for moving the data is to provide a more uniform access to memory from both a part and speed standpoint. Figure 6-8 shows a map of the Data Store RAMs.

The buffers U0905 (MC72D) and U1605 (MC74D) drive the MC.S.BUS+ in to the data store when doing either a CPU or DMA write operation. The buffers U1305 (MC76B) and U1505 (MC76C) are part of the Read Data Register (RDR) which brings the data in from main memory during a read replacement cycle. The registers U1205 (MC77B) and U1405 (MC77C) are part of the Write Data Register (WDR) which holds data from the cache for a write back cycle to main memory. The latches U1207 (MC76D) and U1208 (MC77D) are part of the Data OUT (DOUT) latch which drives data from the cache to the BP.S.BUS+ during a DMA or CPU read cycle.

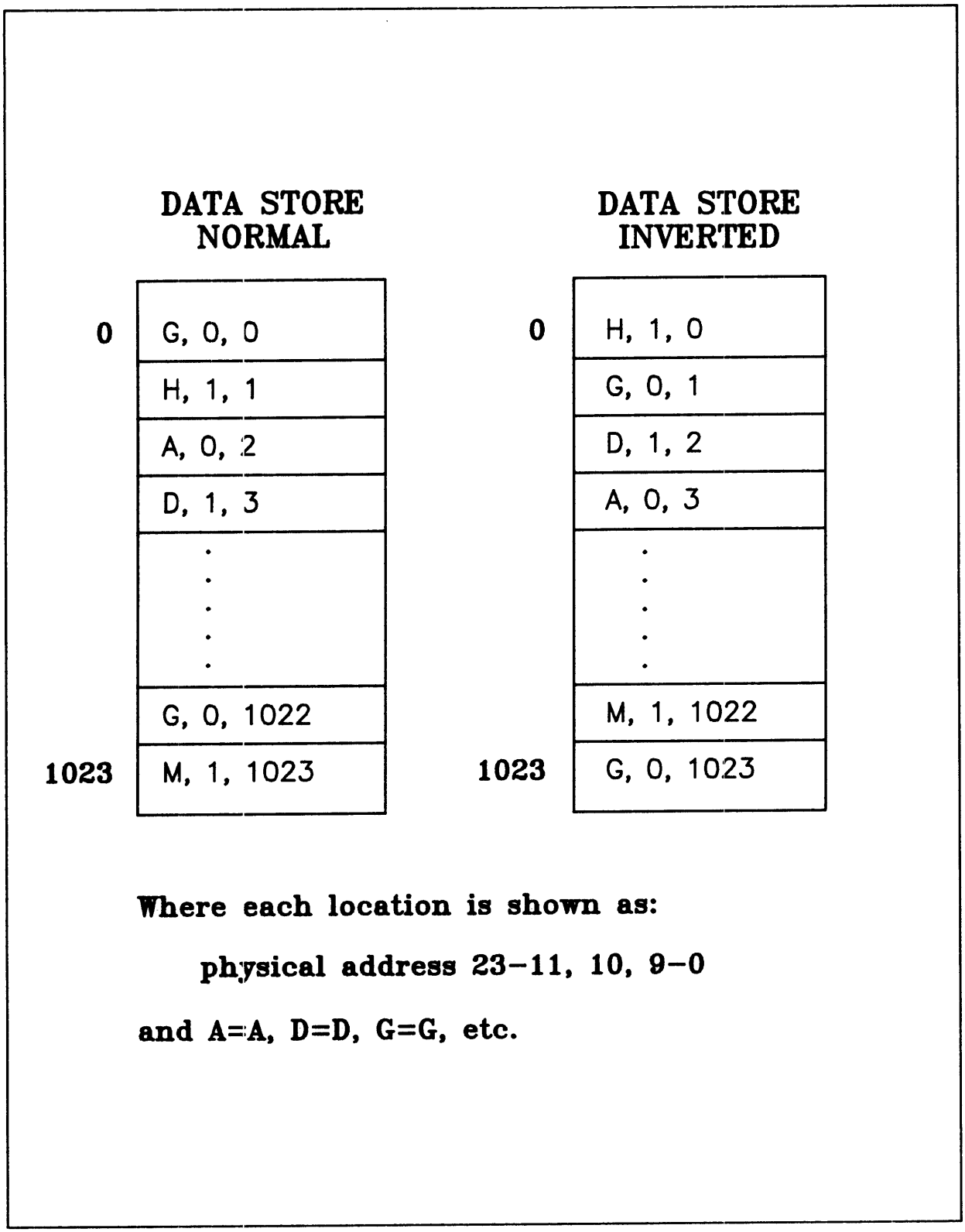


Figure 6-7. Normal Versus Inverted Data Store

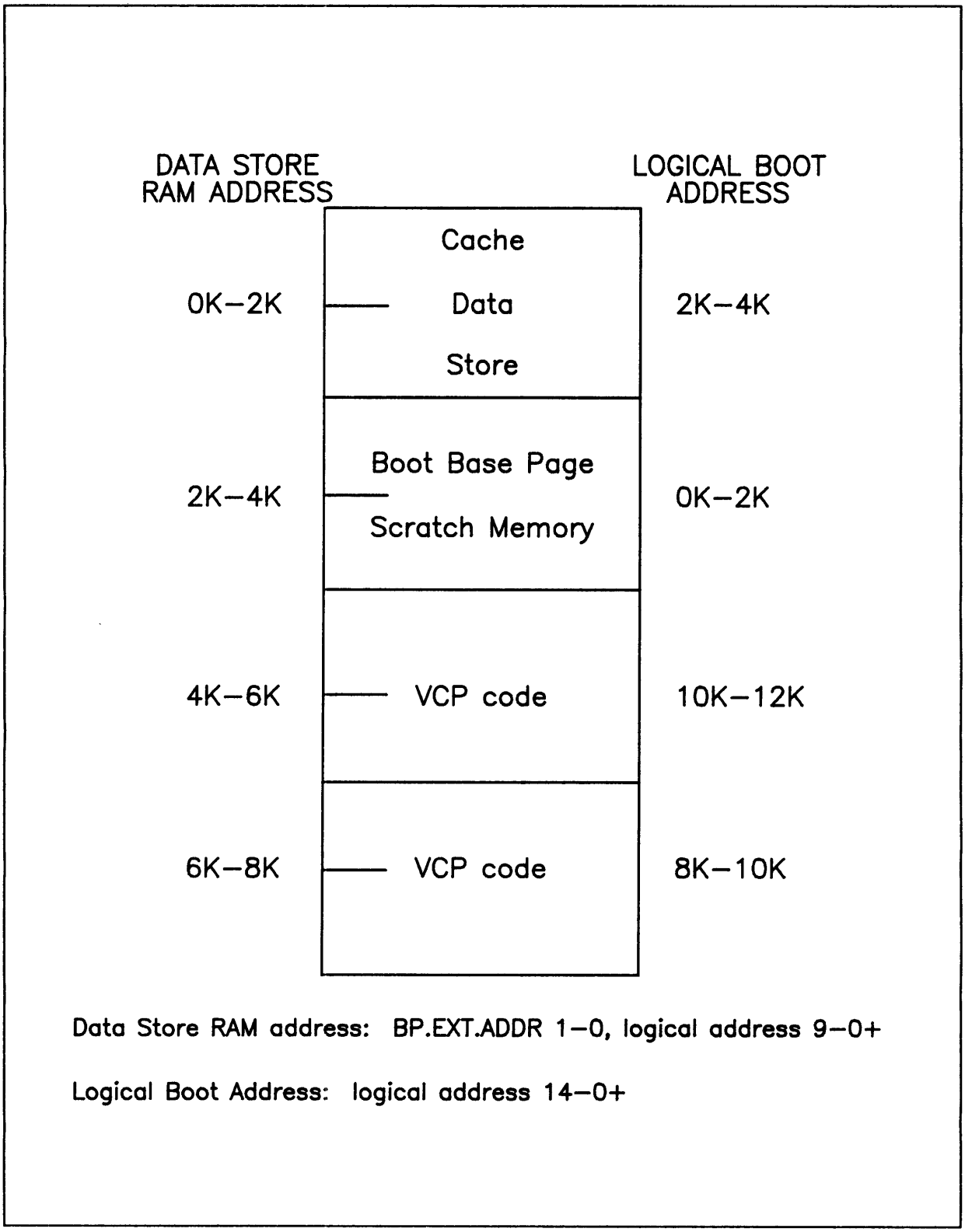


Figure 6-8. Data Store RAM Map

The write strobe generation continues on sheet MC15. The normal part of write generation circuit is shown near the top of the schematic, and the inverted write strobe generation circuit is in the middle of the schematic. Gate U0706 ANDs the write signal with BP.NORMAL+. In fault processing, both chips (normal and inverted) are written to. However, a single-bit error may have added state RD3 to the memory-controller state flow, both RD2 and RD3 must be used to force a write. This is done by gates U0204 (MC151B) and U0706 (MC152B).

The combined signal from RD2 and RD3 is then shaped with the regular and delayed versions of the clocks to produce a write strobe contained in the second half of a microcycle. Since write protection is checked so late, it comes in at the last moment to stop a write, if needed. This is done in gate U0806 (MC155B). The two gates U0906 (MC156B) decide on data merging for writes. For CPU or DMA writes to the cache, the data comes from the DIN buffer. The upper gate enables NDIN if a write was to happen to the normal side and a write strobe really occurs. This is the case when a merge of CPU or DMA occurs with the data coming back from main memory (RDR). The lower gate enables NRDR if a write strobe occurs, but no write was to be done by CPU or DMA.

During the fault handling for a read that misses, the data store RAMs are written by data from the RDR buffers. This same data is passed through the DOUT latches to the CPU or backplane. In order for the data to propagate through the IJT PLAs by the end of the microcycle, the write strobes must begin early during fault handling. This is done by the addition of MC.LAST.READ- to the clock which starts the write strobe in mid-cycle.

Near the end of the cycle, the write strobe stops and the RDR buffers are tri-stated. Until the RAMs start driving the bus again, the bus is garbaged. To avoid this garbage affecting the BP.S.BUS+, the DOUT latches are latched during this transition. Gate U0906 (MC152D) provides this narrow latch signal near the end of a cycle.

6.3.10.2 SBUS Enables

The decision as to which chip drives the SBUS during a read cycle is done on schematic MC16. The PLA U0608 (MC161A) decides when the MC board should drive the backplane SBUS (MC.DRIVE.S.BUS+). This signal is OR'd with MC.READ+ and BP.AB.HIT+ to generate MC.S.EN- in gate U0108 (MC166B) which drives the MC.S.BUS+ onto BP.S.BUS+.

PLA U0608 also decides which data-in source should be used for a write cycle (CPU DIN or LDIN.) The other signal it generates is MC.READ+, which means a memory read cycle is underway. MC.READ+ is ANDed by the gates U0505 (MC164B&C) and U0404 (MC164D) with BP.AB.HIT+ to decide whether the address was to the macro A- or B-Registers. These gates also select either "the lowest address bit (BP.B.CA.ADR+) for the TA or TB case" or "normal or inverted data store for DOUT selection". The PLA coding is shown in Figure 6-9.

```
*
*
*                                  B B B B
*                                  P P P P                 M
*                                  . . . .       M         C
*       B B B B B B B B            R R R R       C         .
*       P P P P P P P P            2 2 2 2       .     M   D
*       . . . . . . . .  M         . . . .       C M C   R
*       U U U U U U D C  U         U U U U       P C .   I
*       I I I I I I M .  I         I I I I  L    U . L   V
*       R R R R R R A L  R         R R R R  B    . L D   E M
*       . . . . . . . D  .         . . . .  P    D D O   . C
*       R R R R R R C I  R         R R R R  .    I I U   S .
*       E E E E E E Y N  E         E E E E  I    N N T   . R
*       G G G G G G C .  G         G G G G  O    . . .   B E
*       3 3 2 2 2 2 L L  2         2 2 2 2  G    E E L   U A
*       1 0 9 8 7 6 E D  3         2 1 0 0  O    N N D   S D
*       + + + + + + + +  +         + + + +  -    - - +   + +
*
*       0 0 0 0 0 0 0 0  1         1 1 1 0  1    1 1 1   1 1
*PIN:   8 7 6 5 4 3 2 1  9         8 7 6 9  5    4 3 2   2 1
*
 SENSE:                                      L    L L H   H H
*                                  B B B B B  B    B B B   B B
*ROW    7 6 5 4 3 2 1 0  9         8 7 6 0  5    4 3 2   2 1
*-------------------------------------------------------------------------------
   0    L L H H H H L -  H         H - - -  A    . . A   . CPU WRITE & RREG/SWCH
   1    L L L - H - L -  H         H - - -  A    . . A   . CPU WRITE & RREG/ONES&ZERO/PVR
   2    - H - - - - L -  H         H - - -  A    . . A   . CPU WRITE & RREG/ACCR&TAB
   3    H - - - - - L -  H         H - - -  A    . . A   . CPU WRITE & RREG/REG&TAB
   4    - - - - - - H -  -         - - - -  .    A A .   A DMA CYCLE
   5    L L H L L H L -  L         - - - -  .    A . A   . RREG/IOGO & NO WRITE
   6    L L H L L H L -  -         L - - -  .    A . A   . RREG/IOGO & NO WRITE
   7    - - - - - - L -  H         H L L L  .    . A .   . STOT/IOGO STARTED
   8    - - - - - - L L  H         H H H -  .    . . .   . STOT/BCIO STARTED (DEL)
   9    L L L L H - L -  -         - - - -  .    . . A   . RREG/PVRL OR PVRH(SEE 1)
  10    L L L H L - L -  -         - - - -  .    . . A   . RREG/INTR OR MCST
  11    H H - - - - L -  L         - - - -  .    . . .   A TAB READ & NO STORE
  12    H H - - - - L -  -         L - - -  .    . . .   A "
  13    L L H L L L L -  L         - - - -  .    . . .   A PNTR READ & NO STORE
  14    L L H L L L L -  -         L - - -  .    . . .   A "
  15    - - - - - - L H  H         H H H -  .    . A .   . STOT/BCIO STARTED
  D1    - - - - - - - -  -         - - - -  .    . . .   ^
  D2    - - - - - - - -  -         - - - -  .    . . ^
  D3    - - - - - - - -  -         - - - -  .    . ^
  D4    - - - - - - - -  -         - - - -  .    ^
  D5    - - - - - - - -  -         - - - -  ^
*
```

Figure 6-9. SBUS Enable U0608 PLA Coding

6.3.10.3 Write Data Register (WDR) Loading

The WDR is always loaded mid-cycle if the memory controller is not busy (BP.MEM.BUSY+). On the second cycle of a fault sequence (RD0) only the side not addressed will be loaded because the cache is treated like a 32-bit memory during fault processing. WDR loading is done by the gates on the bottom of schematic page MC16.

6.3.10.4 TA and TB

The enabling of TA or TB unto the S.BUS was covered in the last subsection. The loading of TA and TB is done by the PLA at U0607 (MC152D). Its coding is shown in Figure 6-10.

TA and TB are loaded on the first cycle done on behalf of the CPU. Thus a DMA cycle will not cause TA or TB to be loaded, but an indirect cycle will. Also, TA and TB can be loaded by both a CPU write to A or B or a memory write to locations "0" or "1" with A/B addressability enabled. TA is the two latches U0406 (MC92A) and U0306 (MC92B). TB is the two latches U0506 (MC94A) and U0405 (MC94B).

```
*
*
*                                  B
*       C                          P                          M M
*       K           B B B . B B    M M M     M C C
*       . B B B     P P P R P P    C C C M B . .
*       A P P P     . . . 2 . .    . . . C P T T
*       . . . . B D U U . U U      V I M . . A B
*       M A B B P M I I S I I      E M T M A . .
*       E B . . . A R R T R R      C S D C B L L
*       M . D C A . . . O . .      T K R R . O O
*       . D P A B C R R R R R      . . . . C A A
*       B P . . . Y E E E E E      S S S S A D D
*       . . A A H C G G . G G      T T T T . . .
*       M W D D I L 2 2 E 2 2      O O O O W E E
*       C R R R T E 3 2 N 0 1      T T T T R N N
*       - + + + + + + + - + +      - - - - - - -
*
*       0 0 0 0 0 0 0 0 1 1 0      1 1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 9 1 9      8 7 6 5 4 3 2
*
 SENSE:                            L L L L L L L
*                                  B B B B B B B
*ROW    7 6 5 4 3 2 1 0 9 1 0      8 7 6 5 4 3 2
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - - - L H L H L      . A . . . . .   IMSK STORE
   1    - - - - - - L H L L H      . . A . . . .   MTDR STORE
   2    - - - - - - L H L H H      . . . A . . .   MCR STORE
   3    - - - - H L H H L L H      . . . . A . .   MEMORY WRITE TO A OR B
   4    H - - L H L H H L L H      . . . . . A .   MEMORY WRITE TO A
   5    - H L - - L - - - - -      . . . . . A .   CPU WRITE TO A
   6    H - - H H L H H L L H      . . . . . . A   MEMORY WRITE TO B
   7    - H H - - L - - - - -      . . . . . . A   CPU WRITE TO B
   8    - - - - - - L L L H H      A . . . . . .   VECT STORE
  D2    - - - - - - - - - - -                  ^
  D3    - - - - - - - - - - -                ^
  D4    - - - - - - - - - - -              ^
  D5    - - - - - - - - - - -            ^
  D6    - - - - - - - - - - -          ^
  D7    - - - - - - - - - - -        ^
  D8    - - - - - - - - - - -      ^
*
```

Figure 6-10. STOT AND A/B PLA (U0607) Code

6.3.11 Macrointerrupt System

The macrointerrupt system is located on the MC board and appears mainly on schematic MC14. Its main part is the macrointerrupt PLA which is U0208 (MC145C). The coding for this PLA is listed in Figure 6-11. The meanings of the various PLA input signals are summarized in the following table:

#	Signal	Name	Comment
I15	BP.UINTP+	UINTP	Interrupt
I14	MC.R2.VECT.STOT-	TCF	Mask-For Trap Cell fetch
I13	MC.TBGT.INT+	TBGT	Interrupt-TBG Tick
I12	MC.SSTP.INT+	SSTP	Interrupt-Single Step
I11	MC.MULT.BIT.INT+	MULT	Interrupt-Multiple Bit Data Error
I10	BP.MP.INT+	MP	Interrupt-Memory Protect
I9	MC.R2.SLAVE-	SLAVE	Interrupt-Slave Request (LBP)
I8	MC.R2.PFW-	PFW	Interrupt-Power Fail Warning (LBP)
I7	MC.FLO.INT+	FLO	Interrupt-Floating Overflow
I6	MC.TBGF.INT+	TBGF	Interrupt-TBG Flag
I5	MC.R2.INTRQ-	INTRQ	Interrupt-I/O System (LBP)
I4	-	-	Unused
I3	MC.TBGM+	TBGM	Mask-For TBGF
I2	MC.TYPE3+	TYPE3	Mask-For INTRQ, TBGF, FLO
I1	MC.TYPE23+	TYPE23	Mask-For INTRQ, TBGF, FLO, PFW
I0	BP.UIR.REG12+	JTDI	Mask-Only valid during JTAB, JTDI

The interrupt inputs come from various places around the machine. Three of the interrupts are derived from I/O backplane (LBP) signals. LBP.SLAVE-, LBP.PFW-, and LBP.INTRQ- are synchronized to the unfrozen microcycle clock by two passes through the register U1108 (MC142D). The double synchronized signals are used by the PLA as the SLAVE, PFW, and INTRQ interrupts. Two interrupts (FLO and TBGF) and three masks (TBGM, TYPE3, and TYPE23) are produced by the IMSK register. This register U0307 (MC143B) also controls SSTPE and TBGE. It is loaded from BP.T.BUS[7:0]+ at the end of any cycle in which MC.IMSK.STOT- is low. Its clock is generated by gate U0705 (MC15B).

The Interrupt PLA drives BP.INTP+ "high" if there are unmasked pending interrupts. UINTP, SSTP, JTDI, or TCF are not included in this signal. BP.JTAB.INT- is similar, but includes SSTP, JTDI, and TCF. Since the bottom bit of the MEM field (BP.UIR.REG12+) is used as a "low true" version or TDI, this signal is only valid when the MEM field contains JTAB or JTDI.

```
*          M     M
*          C     C
*          .     .
*          R     M                                  B       M M M M M M
*          2 M M U   M     M M                      P   B   C C C C C C
*          . C C L   C   M C C                      .   P   . . . . . .
*          V . . T B . M C . .          M U         .     I I I I I I
*        B E T S . P R C . T R        M C I         J     N N N N N N
*        P C B S E . 2 . F B 2      M C . R         T B T T T T T T
*        . T G T R M . R L G .      C . T .         A P R R R R R R
*        U . T P R P S 2 O F I      . T Y R         B . . . . . . .
*        I S . . . . L . . . N S T Y P E          . I P P P P P P
*        N T I I I I A P I I T P B P E G          I N R R R R R R
*        T O N N N N V F N N R A G E 2 1          N T I I I I I I
*        P T T T T T E W T T Q R M 3 3 2          T P 5 4 3 2 1 0
*        + - + + + + - - + + - E + + + +          - + + + + + + +
*        2 2 2 2 2 2 2 2 0 0 0 0 0 0 0 0          1 1 1 1 1 1 1 1
*PIN:    0 1 2 3 4 5 6 7 2 3 4 5 6 7 8 9          0 1 2 3 5 6 7 8
 SENSE:                                          L H L H H H H H
*        I I I I I I I I I I I I I I I I
*        1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0          F F F F F F F F
*ROW     5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0          7 6 5 4 3 2 1 0
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0     H - - - - - - - - - - - - - - - -        . . . A . . A .   UINTP
   1     - - H - - - - - - - - - - - - - -        . A . A . . . .   TBGT
   2     - H H - - - - - - - - - - - - - H        A . . . . . . .   TBGT * TDI
   3     - H - H - - - - - - - - - - - - -        A . . . . . . .   SSTP
   4     - - - - H - - - - - - - - - - - -        . A . . . . . .   MULT
   5     - H - - H - - - - - - - - - - - -        A . . . . . . .   MULT
   6     - - - - - H - - - - - - - - - -          . A . . . . . .   MP
   7     - H - - - H - - - - - - - - - -          A . . . . . . .   MP
   8     - - - - - - L - - - - - - - - -          . A . . . . . .   SLAVE
   9     - H - - - - L - - - - - - - - -          A . . . . . . .   SLAVE
  10     - - - - - - - L - - - - - - H -          . A . . . . . .   PFW
  11     - H - - - - - L - - - - - - H H          A . . . . . . .   PFW * TDI
  12     - - - - - - - - H - - - - H H -          . A . . . . . .   FLO
  13     - H - - - - - - H - - - - H H -          A . . . . . . .   FLO
  14     - - - - - - - - - H - - H H H -          . A . . . . . .   TBGF
  15     - H - - - - - - - H - - H H H H          A . . . . . . .   TBGF * TDI
  16     - - - - - - - - - - L - - H H -          . A . . . . . .   INTRQ
  17     - H - - - - - - - - L - - H H H          A . . . . . . .   INTRQ * TDI
  18     L - L H - - - - - - - - - - - - -        . . . . A A A .   SSTP  HIGHEST
  19     L - L L H - - - - - - - - - - - -        . . . . A A . .   MULT  HIGHEST
  20     L - L L L H - - - - - - - - - - -        . . . . A . A .   MP    HIGHEST
  21     L - L L L L L - - - - - - - - - -        . . . . A . . .   SLAVE HIGHEST
  22     L - L L L L H L - - - - - - - H -        . . . . . A A .   PFW   HIGHEST
  23     L - L L L L H H H - - - - H H -          . . . . . A . .   FLO   HIGHEST
  24     L - L L L L H H L H - - H H H -          . . . . . . A .   TBGF  HIGHEST
  25     - - - - - - - - - - H - - - - -          . . . . . . . A   UNMASKED INTRQ
```

Figure 6-11. Macrointerrupt PLA (U0208) Code

Since the TCF condition is simply a rank-2 version of the signal which indicates that the VECT register is being written, care must be taken to avoid writing this register near the end of an instruction. To reliably assert the condition, the register must be loaded for two consecutive cycles. This is because the register which generates MC.R2.VECT.STOT- never freezes, but the logic which looks at BP.JTAB.INT- may freeze. If a freeze occurs just after VECT is written, the rank-2 signal disappears before the end of the frozen cycle.

The PLA also does a priority encoding of the highest priority pending interrupt which includes UINTP and SSTP but not JTDI or TCF. The four bit priority drives MC.INTR.PRI[4:1]+. The PLA forces MC.INTR.PRI5+ constantly high and drives MC.INTR.PRI0+ with a "high true" version of INTRQ.

The six priority lines along with MC.R2.PFW- and LBP.MLOST- are loaded into the INTR register at the end of each microcycle. This register, which is U0308 (MC147B), drives MC.S.BUS[7:0]+ whenever MC.INTR.RREG- is low. The top half of the MCST register is also enabled at this time to prevent MC.S.BUS[15:8] from floating.

6.3.12 Time Base Generator

The TBG appears on schematic MC13. At its heart is a chain of counters. The chain divides the 14.7456 Mhz communication clock (LBP.CCLK-) generated by U0201 (MC132A). The first two counters are U0205 (MC134B) and U0105 (MC135B). The first counter divides by 256 and the second divides by 64. Their output is sent to U0206 (MC137B) which acts as a divide by 9. This is done by having the counter loaded with all zeros at the end of its 1000 state. The combination of these three counters performs a divide by 147456. Therefore the output of the counter (MC.TBG.D5+) has a frequency of 0.1 Khz with a corresponding period of 10 milliseconds between "ticks".

The counter is reset to all zeros when MC.TBGE+ (from IMSK) is "low". This assures that when MC.TBGE+ returns "high" a full 10 milliseconds will elapse before a tick occurs. Since CCLK is asynchronous to the microcycle, the counters output is synchronized by register U1307 (MC136C) to produce MC.TBG.SYNC[3:1]+. The TBG/SSTP PLA U1107 (MC134C) searches for a falling edge in the counters output indicating that it has completed a cycle. The coding for this PLA is listed in Figure 6-12.

If MC.TBG.SYNC2+ is "low" and MC.TBG.SYNC3+ is still "high" (this will occur for exactly one cycle) the PLA will assert MC.TBGT.INT.D+ "high". At the end of the cycle this signal will be clocked into the register U1307 (MC136C) to become MC.TBGT.INT+ which is one of the inputs to the Interrupt PLA. It is also fed back to the TBG/SSTP PLA which latches it (TBGC bit set in IMSK). MC.TBG.INT.D+ will also be forced "low" if MC.TBGE+ is "low".

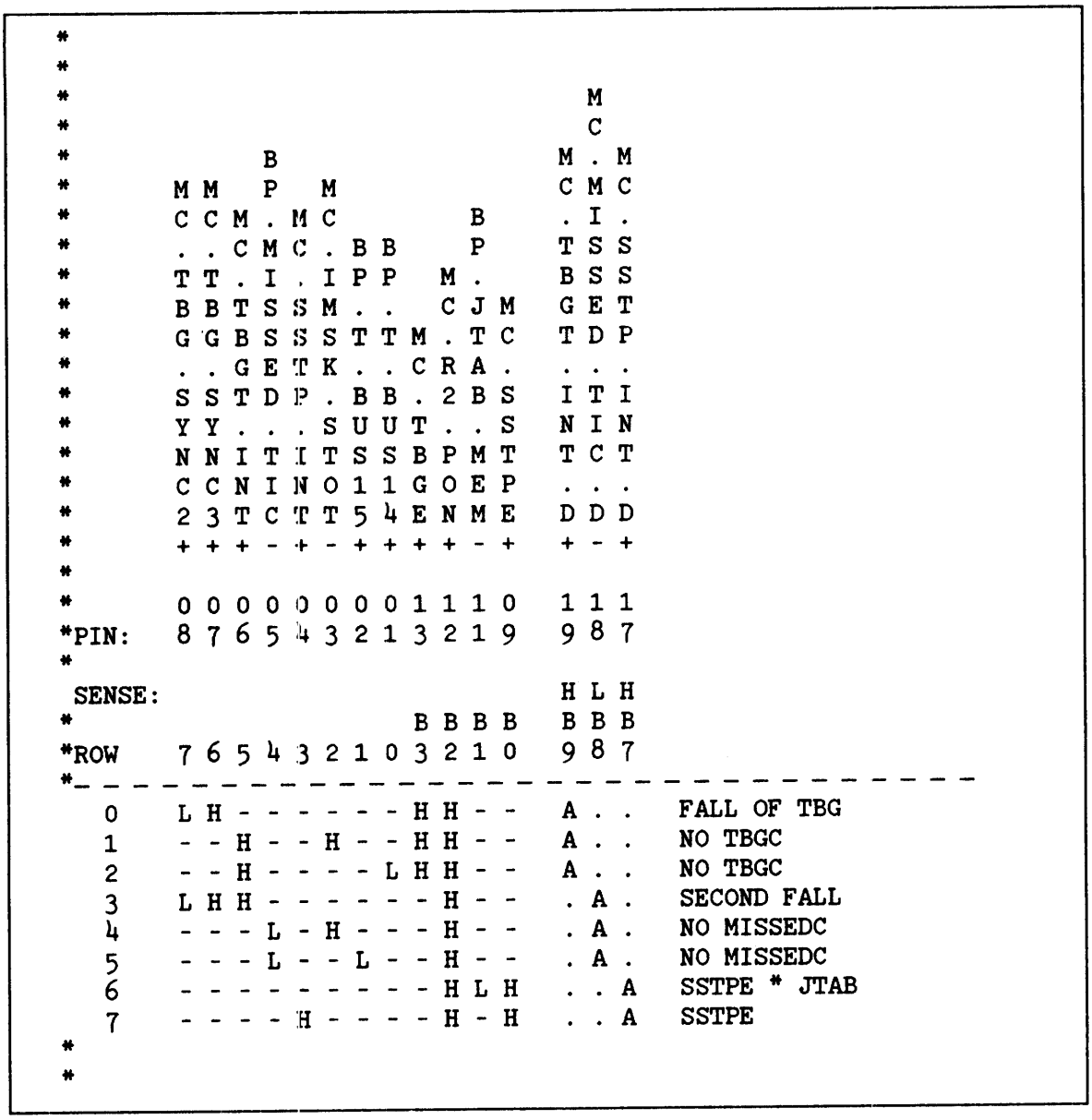
Note that since there are several cycles of delay through the synchronizing register, clearing TBGE and then immediately setting it again may cause TBGF to be set erroneously. TBGE must always be left cleared for at least four cycles to prevent this.

If the PLA detects a falling edge in the counter's output (MC.TBG.SYNC2+ "low", and MC.TBG.SYNC3+ "high") while MC.TBGT.INT+ is "high", it forces MC.MISSED.TIC.D- "low". This signal is clocked into the register U1307 (MC136C) to form BP.MISSED.TICK- which is sent to the microinterrupt system. It is also sent back to the TBG/SSTP PLA which latches it "high" until a cycle in which MC.IMSK.STOT- is "low" and BP.T.BUS15+ is "high" (MISSEDC set in IMSK) which again forces it "high".

A double-synchronized version of LBP.PON+ (MC.R2.PON+) forces MC.TBG.INT.D+ "low" and MC.MISSED.TIC.D- "high" whenever it is "low".

6.3.13 Single Step Interrupt

The SSTP interrupt is controlled by the TBG/SSTP PLA U1107 (MC134C), the TBG/SSTP PLA. The SSTP coding is included in the Figure 6-13 along with the TBG coding In a cycle in which MC.SSTPE+ is "high" and BP.JTAB.MEM- is "low", the PLA will assert MC.SSTP.INT.D+ "high". This signal is loaded into the register U1307 (MC136C) at the end of each cycle to become MC.SSTP.INT+ which is an input to the Interrupt PLA. It is also an input to the TBG/SSTP PLA which latches it "high" as long as MC.SSTPE+ remains "high". MC.SSTP.INT.D+ is forced "low" when MC.R2.PON+ is "low".



```
*
*
*                                                    M
*                                                    C
*                    B                             M . M
*       M M          P     M                       C M C
*       C C M . M C                      B          . I .
*       . . C M C . B B                  P          T S S
*       T T . I . I P P       M .                   B S S
*       B B T S S M . .       C J M                 G E T
*       G G B S S S T T M . T C                     T D P
*       . . G E T K . . C R A .                     . . .
*       S S T D P . B B . 2 B S                     I T I
*       Y Y . . . S U U T . . S                     N I N
*       N N I T I T S S B P M T                     T C T
*       C C N I N O 1 1 G O E P                     . . .
*       2 3 T C T T 5 4 E N M E                     D D D
*       + + + - + - + + + + - +                     + - +
*
*       0 0 0 0 0 0 0 0 1 1 1 0                     1 1 1
*PIN:   8 7 6 5 4 3 2 1 3 2 1 9                     9 8 7
*
 SENSE:                                             H L H
*                                 B B B B           B B B
*ROW    7 6 5 4 3 2 1 0 3 2 1 0                     9 8 7
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    L H - - - - - - H H - -                     A . .   FALL OF TBG
   1    - - H - - H - - H H - -                     A . .   NO TBGC
   2    - - H - - - - L H H - -                     A . .   NO TBGC
   3    L H H - - - - - - H - -                     . A .   SECOND FALL
   4    - - - L - H - - - H - -                     . A .   NO MISSEDC
   5    - - - L - - L - - H - -                     . A .   NO MISSEDC
   6    - - - - - - - - - H L H                     . . A   SSTPE * JTAB
   7    - - - - H - - - - H - H                     . . A   SSTPE
*
*
```

Figure 6-12. TBG/SSTP PLA (U1107) Code

anc 134c

6.4 Parts Locations

The parts locations for the memory controller card are shown in Figure 6-13.

6.5 Replaceable Parts List

The replaceable parts list for the memory controller cards are listed in Table 6-6. The names and addresses of the manufacturers of the parts are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

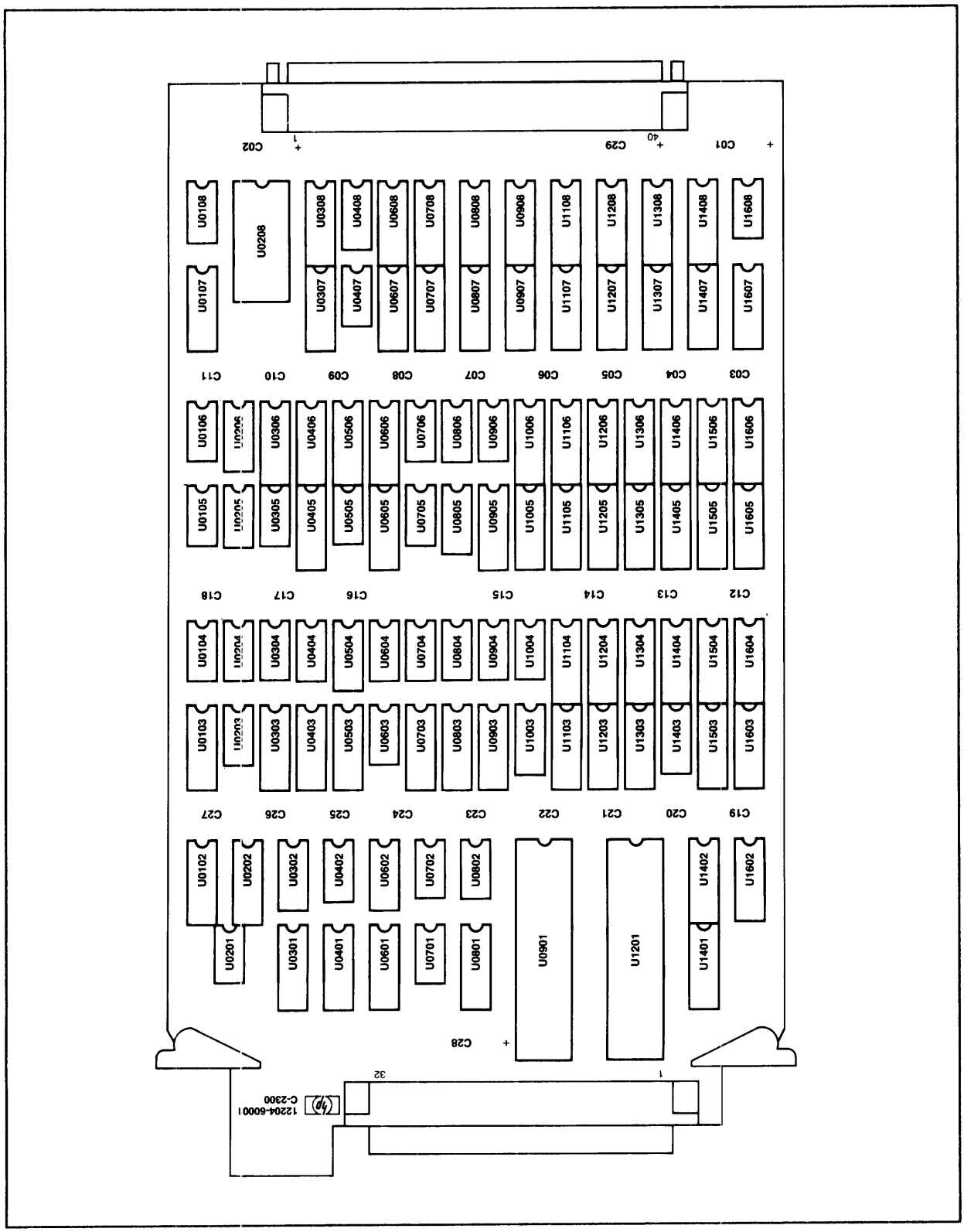


Figure 6-13. Memory Controller Card Parts Locations

Table 6-6. Memory Controller Card Replaceable Parts (Sheet 1 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12204-60001	4	1	PCA-MEM CNTRLR	28480	12204-60001
C1	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-4835	7	25	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C29	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
U104	1820-0681	4	4	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U105	1820-1989	7	4	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U106	1820-0683	6	4	IC INV TTL S HEX 1-INP	01295	SN74S04N
U107	1820-2795	5	17	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U108	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U201	1813-0196	1	1	XTAL-CLOCK-OSCILLATOR 14.7456-MHZ	28480	1813-0196
U203	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U204	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U205	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U206	1820-1876	1	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	34335	AM74S161N
U208	12204-80002	7	1	IC-INTERRUPT	28480	12204-80002
U301	1820-2701	3	22	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U302	1810-0256	8	1	NETWORK-RES 16-DIP1.0K OHM X 15	01121	316A102
U303	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U304	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U305	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U306	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U307	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U308	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U401	1820-2700	2	9	IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U402	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U403	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U404	1820-0685	8	2	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U405	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U406	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U407	1820-1449	4	4	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U408	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U503	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U504	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U505	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U506	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U601	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U602	1820-2693	2	3	IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U603	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U604	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U606	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U607	1820-3047	2	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3047
U608	1820-4557	1	1	IC PRGMBL-LGC TTL S PLA	28480	1820-4557
U701	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U702	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U703	1820-1730	6	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U704	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U705	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U706	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N

Table 6-6. Memory Controller Card Replaceable Parts (Sheet 2 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U707	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U708	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U801	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U802	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U803	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U804	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U805	1820-2693	2		IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U806	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U807	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U808	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U901	1820-2954	8	2	IC MISC TTL S 16-BIT	28480	1820-2954
U903	1820-3049	4	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3049
U904	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U905	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U906	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U907	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U908	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1003	1820-1015	0	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U1004	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U1005	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1006	1818-3118	3	8	IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1103	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U1104	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1105	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1106	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1107	1820-3048	3	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3048
U1108	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1201	1820-2954	8		IC MISC TTL S 16-BIT	28480	1820-2954
U1203	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1204	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1205	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1206	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1207	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1208	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1303	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1304	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1305	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1306	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1307	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1308	1820-2565	7	1	IC BFR TTL S LINE DRVR OCTL	34335	AM74S244N
U1402	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1403	1820-2693	2		IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U1404	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1405	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1406	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1407	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1408	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1503	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U1504	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1505	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1506	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1602	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1603	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1604	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1605	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1606	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1607	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U1608	1810-0182	9	1	NETWORK-RES 14-DIP MULTI-VALUE	28480	1810-0182

A	AS ISSUED	oo/ko	10/20/82
B	CORRECTED NUMBERS ON 74F374	mcf/ko	3/3/83
	CORRECTED G2A TO G2B & G2B TO G2A ON 745138		

D-12204-60001-51

MEMORY TEST DATA REGISTER (MTDR)

90A 105A 140B 40D 130D — BP.T.BUS+ / 16

130D 159D — MC.IMSK.STOT- (282)
159D — MC.MTDR.STOT- (385)
159D — MC.MCR.STOT- (389)

160A 105C — BP.UIR.REG+ / 5

169A 105E — BP.KIS.S.OFF- (210)

RREG.DECODE

-1240 74S138 U0408

(218) (219) (220) → A B C
(221) (222) → G1 G2A G2B
Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0

MC.MCST.RREG- (287)
MC.INTR.RREG- (374)
MC.PVRH.RREG- (196)
MC.PVRL.RREG- (299)

-1449 74S32 U0705

(282) (52) → 3 (332)
(332) CK.A.MEM.MSK.MC+ → 140B

-2241 74F374 U1303

(35)(39)(49)(48)(47)(46)(51)(50) → D8 D7 D6 D5 D4 D3 D2 D1
CLK OE (11, 1) (83)
19(111) 16(110) 15(109) 12(107) 9(106) 6(105) 5(104) 2(103) → Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1

-2241 74F374 U1304

(35)(39)(49)(48)(47)(46)(51)(50) → D8 D7 D6 D5 D4 D3 D2 D1
CLK OE (11, 1) (83)
19(92) 16(91) 15(90) 12(89) 9(88) 6(87) 5(117) 2(118) → Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1

-2241 74F374 U1105

(45)(44)(43)(42)(41)(40)(38)(37) → D8 D7 D6 D5 D4 D3 D2 D1
CLK OE (11, 1) (83)
19(102) 18(101) 15(100) 12(99) 9(97) 8(25) 5(94) 2(93) → Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1

-2241 74F374 U1203

(45)(44)(43)(42)(41)(40)(38)(37) → D8 D7 D6 D5 D4 D3 D2 D1
CLK OE (11, 1) (83)
19(115) 18(114) 15(113) 12(112) 9(109) 6(88) 5(86) 2(85) → Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1

-1449 74S32 U0705

10 9 → 8
CK.A.MEM.MTD.MC+ (155)

32 / FP.MEM.DATA+ → 40A 79A 89A 117B 50D

MC.MTDR.EN- (155)

MEMORY (ON MOD REG (MCR - HI)

-4736 74LS273 U0703

(35)(39)(49)(48)(47)(46)(51)(50) → D8 D7 D6 D5 D4 D3 D2 D1
CLR (11, 1)
19 16(306) 15(390) 12(283) 9 MC.MEM.CM.IN-(289) 6(465) 5(366) 2(407) → Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1

(306) MC.SCHOD- → 120A
(390) MC.MCST.CLK.EN- → 120E
(283) MC.INIT.MODE+ → 80C
(289) MC.MEM.CM.IN- → 120C
(465) MC.MEM.INIT.CLK+ → 80C
(366) MC.FRC.PVR.CLK- → 50E
(407) MC.PVR.CLR- → 50E

29B 150B 50C 120D — MC.RD2-)162)
29B 50B 120D — MC.RD1- (161)

-0681 74S00 U0603

MC.RDLOR.RD2+ (419)

-1158 74S51 U1004

49D 113D 50E 80E — MC.TEST.DATA.EN+ (317)
FP.AR.DBSEL- (84)

120D 102E 150E — CK.A.MEM.MC+ (52)

-1449 74S32 U0705

(389) (52) → (227)
(227) CK.A.MEM.MCR.MC+ → 40E

-0683 74S04 U0402

(335) FP.MEM.CH.IN+ → 112D

60A 20C 102D 130D 40E — LBP.PON+ (53)

(287) MC.MCST.RREG- → 120E
(374) MC.INTR.RREG- → 140C
(196) MC.PVRH.RREG- → 50A
(299) MC.PVRL.RREG- → 50A

-0681 74S00 U0305

MC.MCST.OR.INTR+ (467)

-0683 74S04 U0106

MC.MCST.OR.INTR- (466) → 120E

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC1

	MEMORY CONTROLLER-A900 MC UIR DECODE	HEWLETT PACKARD
	SIZE	12204-60001
	SHEET OF	D-12204-60001-51

MC 1

D-12204-60001-52			
A	AS ISSUED	co/ko	10/20/82
B	CORRECTED NUMBERS ON 74F374	maf/ko	3/3/83
C	CIRCUIT CHANGE PER PC22-6770	go/ko	3/9/83

STATE DECODER

-1022
74S139
U0504

(63) MC.STATE.CNTR1- (163) MC.STATE.CNTR0-

MC.RD.CYC- (61)

MC.RD.0- (302)
MC.RD1- (161)
MC.RD3- (197)
MC.RD2- (162)
MC.STATE0-

-0683
74S04
U0604

(159) MC.RD0+
(302) MC.RD0-
(161) MC.RD1-
(197) MC.RD3-
(162) MC.RD2-

60A 160D 30E
120D
50B 10D 120D
150B 120D 50E
150B 10C 50C 120D

(441)
(311) MC.STATE0+
50B 60B

(398) MC.NEXT.CLR.MB-
60B

129C MC.MEM.WR.REQ+ (393)
129B MC.MEM.RD.REQ+ (392)

MPL05

5180-4232
825153
U0903

MC.REF.REQ+ (431)
59C MC.MEM.RD.ERR+ (290)
60A 130A 10D 102D 40E LBP.PON+ (53)
MC.RD.CYC- (61)
BP.WR.CYC- (5)
MC.REF.CYC- (57)
MC.STATE.CNTR1- (63)
MC.STATE.CNTR0- (163)

MC.NEXT.CLR.MB-
MC.NEXT.DATA.LE- (399)
MC.NEXT.RD.CYC- (293)
MC.NEXT.WR.CYC- (297)
MC.NEXT.REF.CYC- (294)
MC.NEXT.ST.CTR1- (296)
MC.NEXT.ST.CTR0- (295)

MC.REF.REQ.PEND+

-2201
74F374
U0803

MC.REF.REQ+ (431)
MC.CLR.PULSE+ (354)
MC.RD.CYC- (61)
BP.WR.CYC- (5)
MC.REF.CYC- (57)
MC.STATE.CNTR1- (63)
MC.STATE.CNTR0- (163)

(273) MC.DATA.LE-
40E

-0683
74S04
U0804

(63)
(57)
(442) MC.STATE.CNTR1+
(304) MC.REF.CYC+
60A
30E

60B 128D 130D 150D CK.A.MEM.I.MC+ (31)
30C 69E MC.PULLDOWN- (158)
39A MC.SET.REF.REQ+ (309)

(354) MC.CLR.PULSE+
30B

-1449
74S32
U0702

(272) MC.LAST.READ-
150B

(163) MC.STATE.CNTR0-
(63) MC.STATE.CNTR1-
(57) MC.REF.CYC-
(5) BP.WR.CYC-
(61) MC.RD.CYC-
120E
151B 120E
30C 60D 120E
60C 70C 80C 120D 40E 107E
60B 40E 120E

39B MC.REF.REQ.PEND+ (305)

(293) MC.NEXT.RD.CYC-
(297) MC.NEXT.WR.CYC-
(294) MC.NEXT.REF.CYC-
(296) MC.NEXT.ST.CTR1-
(295) MC.NEXT.ST.CTR0-
120D
120D
120E
120E
120E

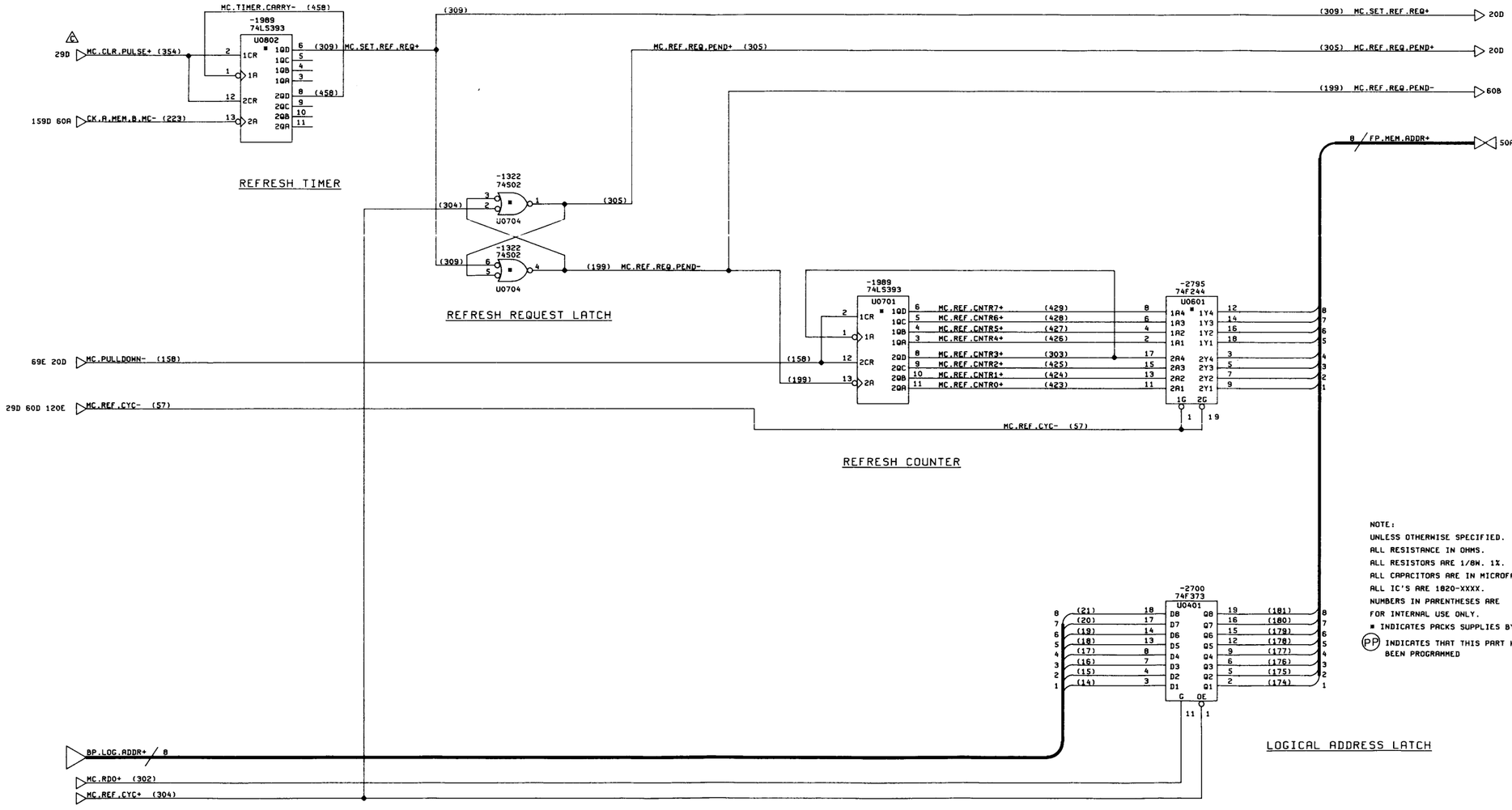
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC2

	MEMORY CONTROLLER-A900 STATE MACHINE	HEWLETT PACKARD
		12204-60001
		D-12204-60001-52

MC 2

ITR	REVISIONS	APPROVED	DATE
A	AS ISSUED	eaf/ko	10/20/82
B	CORRECTED NUMBERS ON 74F373	eaf/ko	3/3/83
C	CIRCUIT CHANGE PER PC22-6770	cd/ko	3/9/83



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC3

	MEMORY CONTROLLER- A900 REFRESH (TITLE)	HEWLETT PACKARD
	NEXT ASSEMBLY	12204-60001 (PART NUMBER)
SUPERSEDES ###.	SHEET OF	D-12204-60001-53

MC 3

D-12204-60001-54			
A	AS ISSUED	mof/ko	10/20/82

ERROR DETECTION AND CORRECTION

79A 89A 117B 19C 50D — FP.MEM.DATA+ 39

CHECKBIT RECEIVER

~2795 74F244 U1602

(4) 8 — 1A4 1Y4 — 12
38 (188) 6 — 1A3 1Y3 — 14 (207) 6
37 (187) 4 — 1A2 1Y2 — 16 (206) 5
36 (186) 2 — 1A1 1Y1 — 18 (205) 4
35 (185) 17 — 2A4 2Y4 — 3 (204) 3
34 (184) 15 — 2A3 2Y3 — 5 (203) 2
33 (183) 13 — 2A2 2Y2 — 7 (202) 1
32 (182) 11 — 2A1 2Y1 — 9 (201) 0
1G 2G
1 19

MC.EDC.SC.OE+ (279)

~0683 74S04 U0402: 9 → 8 (279)

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
(92) (91) (90) (89) (88) (87) (112) (116) (115) (114) (113) (112) (109) (98) (86) (85)

Am2960
GND = pin 13
VCC = pin 36

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16
(111) (110) (108) (107) (106) (105) (104) (103) (102) (101) (100) (99) (97) (95) (94) (93)

2 3 4 5 9 10 11 12 14 15 16 17 20 21 22 23

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 — DATA

U1201 EDC-0/1

(207) 41	CB6	SC6	25 (207) 6
(206) 39	CB5	SC5	29 (206) 5
(205) 38	CB4	SC4	26 (205) 4
(204) 37	CB3	SC3	28 (204) 3
(203) 35	CB2	SC2	27 (203) 2
(202) 34	CB1	SC1	24 (202) 1
(201) 40	CB0	SC0	30 (201) 0
(362) 7	LE DIAG	OE BYTE 1	8 (59)
(276) 6	LE IN	OE BYTE 0	18
19	LE OUT	OE SC	31

CODE ID 2 1 0 — GEN — COR — PAS — DIAG 1 0 — MER — ENB

-2954 Am2960

45 44 43 42 1 48 47 46 33 32

MC.SC.CB6+ (438) … MC.SC.CB0+ (432)

U0901 EDC-2/3

41	CB6	SC6	25 (207) 6
39	CB5	SC5	29 (206) 5
38	CB4	SC4	26 (205) 4
37	CB3	SC3	28 (204) 3
35	CB2	SC2	27 (203) 2
34	CB1	SC1	24 (202) 1
40	CB0	SC0	30 (201) 0
7	LE DIAG	OE BYTE 1	8 (59)
(276) 6	LE IN	OE BYTE 0	18
19	LE OUT	OE SC	21 (280)

CODE ID 2 1 0 — GEN — COR — PAS — DIAG 1 0 — MER — ENB

-2954 Am2960

45 44 43 42 1 48 47 46 33 32

MC.SYNDROME+

CHECKBIT/SYNDROME DRVR

~2795 74F244 U1402

8			12
(207) 6	1A4	1Y4	14 (188) 38
(206) 4	1A3	1Y3	16 (187) 37
(205) 2	1A2	1Y2	18 (186) 36
(204) 17	1A1	1Y1	3 (185) 35
(203) 15	2A4	2Y4	5 (184) 34
(202) 13	2A3	2Y3	7 (183) 33
(201) 11	2A2	2Y2	9 (182) 32
	2A1	2Y1	
	1G	2G	
	1	19	

69D 120C — MC.PULLUP+ (4)

MC.EDC.SC.OE- (280)

(276)

(280) — (277) MC.EDC.ERR- 50E

(59)

MC.MULT.ERR- (396) — 13 → 12 (364) MC.EDC.MULT.ERR+ 50D

U0804

MEMORY CONTROL REGISTER (LO)

~1730 74LS273 U1103

7 (45)	18 D8	Q8	19	MC.DIAG.LE.LO+ (362)
6 (44)	17 D7	Q7	16	MC.DIAG.LE.HI+ (361)
5 (43)	14 D6	Q6	15	MC.DIAG.GEN+ (360)
4 (42)	13 D5	Q5	12	MC.DIAG.DATA.OE+ (359)
3 (41)	8 D4	Q4	9	MC.DIAG.DATA.LE- (358)
2 (40)	7 D3	Q3	6	MC.DIAG.SC.OE+ (363)
1 (38)	4 D2	Q2	5	MC.TEST.DATA.EN+ (317)
0 (37)	3 D1	Q1	2	MC.DIAG.MODE+ (191)
		CLR	11	1

10A 90A 105A 140A 130D — BP.T.BUS+ /8

~0683 74S04 U0402: (191) 11 → 10 MC.DIAG.MODE- (274)

(317) MC.TEST.DATA.EN+ 10D

19D — CK.A.MEM.CMR.MC+ (227)

50A 20C 20D 102D 130D — LBP.PON+ (53)

29D 60B 120E — MC.RD.CYC- (61)

59B — MC.DATA.OE+ (357)

29C — MC.DATA.LE- (273)

EDC CONTROL MUX

~1015 74S158 U1003

(360) 13	4B	4Y	12 MC.EDC.GEN- (278)
(61) 14	4A		
(3) 10	3B	3Y	9 MC.EDC.DATA.OE- (59)
(357) 11	3A		
(358) 6	2B	2Y	7 MC.EDC.DATA.LE+
(273) 5	2A		
(363) 3	1B	1Y	4 MC.EDC.SC.OE- (280)
(273) 2	1A		
	G	S	

(59) — BP.MR.CYC- (5)

~1367 74S08 U0904: 4, 5 → 6 MC.CB.SYN.DR.EN- (270)

29D 60C 70C 80C 120D 107E — BP.MR.CYC- (5)

(191) MC.DIAG.MODE+

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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC4

	MEMORY CONTROLLER- A900 ERROR CORRECTION	HEWLETT PACKARD
	TITLE	12204-60001
	NEXT ASSEMBLY	PART NUMBER D-12204-60001-54
	SHEET OF	

MC 4

	D-12204-60001-55		
VMS	REVISIONS	APPROVED	DATE
A	AS ISSUED	mcf/ko	10/20/82
B	CORRECTED NUMBERS ON 74F374	mcf/ko	3/3/83

19D MC.PVRH.RREG- (196)
19D MC.PVRL.RREG- (299)
39B 102B 112D FP.MEM.ADDR+ 23

15B MC.WRITE.ANYWAY- (209)

29B 60B MC.STATE0+ (311) → U0203 (-1322 74S02) → (356)MC.CLR.RD.EN-
U0104 (-0681 74S00) → MC.RD.EN- (422)
29B 10D 120D MC.RD1- (161) → U0104 (-0681 74S00) → MC.RD.EN+ (198)

RD.EN LATCH

MC.MEM.RD.ERR+ (290)

151C 120D 140F 160E CK.A.MEM.2.MC+ (22)
29B 150B 10C 120D MC.RD2- (162) → U0702 (-1449 74S32) → MC.RD2.BD.SEL- (420)
U0203 (-1322 74S02) → MC.MEM.RD.ERR+ (290)

PARITY VIOLATION REGISTER

U0702 (-1449 74S32) → BP.PE.FREEZE-

49C MC.EDC.MULT.ERR+(364)
40A 79A 89A 117B 19C FP.MEM.DATA+ 7
U0804 (-0683 74S04) → MC.MULT.ERR.INT- (291)
10D 113D 60E FP.AR.BD.SEL- (84)
49C MC.EDC.ERR- (277)
U0304 (-1322 74S02) → MC.POSSBL.ERR+ (405)
29B 150B 120D MC.RD3- (197)
U0304 (-1322 74S02) → MC.RD3.2ND.HALF+ (421)
U0404 (-0685 74S10) → MC.NRML.ERR.CLK-(401)
19D MC.FRC.PVR.CLK- (366)
U0603 (-0681 74S00) → MC.ERR.CLK+ (152)
19D MC.PVR.CLR- (407)

U1503 (-1730 74LS273): MC.MULT.ERR.INT+ (194), MC.LCH.SYN6+ (387), MC.LCH.SYN5+ (386), MC.LCH.SYN4+ (385), MC.LCH.SYN3+ (383), MC.LCH.SYN2+ (382), MC.LCH.SYN1+ (381), MC.LCH.SYN0+ (380)

U0503 (-2701 74F374) PVRL
U0301 (-2701 74F374)
U0605 (-2701 74F374) PVRH
U1603 (-2795 74F244)

(357) MC.DATA.OE+ → 40E
(198) MC.RD.EN+ → 60E
(290) MC.MEM.RD.ERR+ → 20C
(214) BP.PE.FREEZE- → 107E
(194) MC.MULT.ERR.INT+ → 140D
16 MC.S.BUS+ → 129D 149B 90C 70E 80E
(291) MC.MULT.ERR.INT- → 120B

NOTE:
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ALL IC'S ARE 1820-XXXX.
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FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC5

	MEMORY CONTROLLER - A900 "PARITY" VIOLATION REGULATOR	HEWLETT PACKARD
		12204-60001
		D-12204-60001-55

MC 5

A	AS ISSUED	acf/ko	10/20/82

D-12204-60001-56

29C MC.STATE.CNTR1+ (442)
159D 30B CK.A.MEM.B.MC- (223)
-0681 74S00 U0603
MC.CLR.RAS- (355)

29B 160D 30E MC.RDQ+ (159)
20C 10D 102D 130D 40E LBP.PON+ (53)
-1367 74S08 U0904
MC.RDQ.PON+ (418)

120B 102E BP.MEM.RD.REQ+ (212)
29D 40E 120E MC.RD.CYC- (61)
29C 50B MC.STATE0+ (311)
-1158 74S51 U1004
MC.SET.RAS- (308)

-2693 74F109 U0602
MC.RAS- (301)
MC.RAS+ (417)
-0683 74S04 U0402
(463) FP.ADDR.CLK+ 112D

69E 120B MC.PULLUP.PR+ (60)
39B MC.REF.REQ.PEND- (199)

29C MC.NEXT.CLR.MB- (398)
-1322 74S02 U0704
13 MC.CLR.MEM.BUSY+(351)
-0683 74S04 U0604

MEM BUSY F/F

-0683 74S04 U0402
MC.INIT.MODE-

-0681 74S00 U0603
MC.SET.MEM.BUSY+ (307)
MC.CLR.MEM.BUSY- (353)

-2693 74F109 U0603
(353)
(391) MC.MEM.BUSY-
-0683 74S04 U0402
(169) BP.MEM.BUSY+ 107D 160E

20D 120D 130D 150D CK.A.MEM.1.MC+ (31)
(367)

19D MC.MEM.INIT.CLK+ (465)
19C MC.INIT.MODE+ (203)
59B MC.RD.EN+ (198)
29D 70C 80C 120E 40E 107E BP.WR.CYC- (5)
29D 30C 120E MC.REF.CYC- (57)

-2795 74F244 U0801
MC.MEM.INIT.CLK+ (465)
MC.RAS+ (417)
MC.REF.EN- (430)
(464) FP.CK.MEM.MC+ 112D
(333) FP.INIT.CLK+ 112D
(334) FP.INIT.MODE+ 112D
(339) FP.WE- 112D
(336) FP.RAS+ 112D
(337) FP.RD.EN+ 112D
(338) FP.REF.EN- 112D

-1367 74S08 U0904
-1449 74S32 U0702
MC.RAS- (301)

ARRAY CONTROL SIGNAL BUFFER

TERM
+5M
220
330
U1608 1810-0182

120D 140D LBP.INTRQ- (255)
102D LBP.IORQ- (340)
102D LBP.MCMODOC- (341)
160B 102D 91E LBP.MEMGO- (190)
140A 102D LBP.MLOST- (256)
102D LBP.MRQ- (342)
102D 140D LBP.PFN- (267)
102D LBP.REMEM- (344)
120D 140D LBP.SLAVE- (268)
102D LBP.WE- (347)
10D 113D 50E FP.AR.BD.SEL- (84)
120C 113E FP.NEXT.AR.BD- (246)

MC.TBG.PULLUP+ (469)
MC.PULLUP+ (4)
MC.PULLUP.PR+ (60)
MC.PULLUP.CLR+ (406)
-0683 74S04 U0604
(469) MC.TBG.PULLUP+ 130A
(4) MC.PULLUP+ 40C 120C
(60) MC.PULLUP.PR+ 60B 120B
(406) MC.PULLUP.CLR+ 120A
(158) MC.PULLDOWN- 30C 20D

BACKPLANE PULLUPS

RDIP IKx15 U0302 1810-0256
+5M

NOTE:
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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC6

MEMORY CONTROLLER - A900 MISCELLANEOUS CONTROL

HEWLETT PACKARD

12204-60001

D-12204-60001-56

MC 6

		D-12204-80001-57	
		REVISIONS	
A	AS ISSUED	maf/ko	10/20/82
B	CORRECTED NUMBERS ON 74F373 &	maf/ko	3/3/83
	74F374; CHANGED FABRICATED PART NUMBERS TO PURCHASED PART NUMBERS PER PRCR "A".		

DATA STORE(N)

80A 102A 30E — BP.LOG.ADDR+ / 9

80A 102E — BP.EXT.ADDR1+ (33)

80A 102E — BP.EXT.ADDR0+ (36)

102E — BP.LOG.ADDR0N+ (66)

CA 26 L

159B — MC.DSN.WE- (56)

159B — MC.NRDR.EN- (157)

169D — MC.NWDR.CLK+ (298)

60B 60C 29D 120D 40E 107E — BP.WR.CYC- (5)

MC.DSN.DATA+

159A — MC.NDIN.EN- (156)

169C — MC.NDOUT.EN- (292)

159D 80E — MC.DOUT.HLD- (54)

149B 129D 59E 90C 88E — MC.S.BUS.+ / 16

16 / FP.MEM.DATA+ — 89A 19C 40A 117B 50D

16 / BP.S.BUS+ — 109C 89E 90C

U1306, U1506, U1006, U1406 — 1818-3118 1420 — 4K x 4 RAM (A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0; D4, D3, D2, D1; WE, CS)

RDR(N)

U1305, U1505, U1207, U0905, U1605 — -2795 74F244 — 1A4 1A3 1A2 1A1 2A4 2A3 2A2 2A1; 1Y4 1Y3 1Y2 1Y1 2Y4 2Y3 2Y2 2Y1; 1G 2G

WDR(N)

U1205, U1405 — -2701 74F374 — D8 D7 D6 D5 D4 D3 D2 D1; Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1; CLK OE

U1208, U1308 — -2700 74F373 — D8 D7 D6 D5 D4 D3 D2 D1; Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1; G OE

DIN(N)

DOUT(N)

NOTE:
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ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC7

	MEMORY CONTROLLER - A900 MC DATA STORE NORMAL	HEWLETT PACKARD
	TITLE	12204-60001
	NEXT ASSEMBLY	PART NUMBER
	SHEET OF	D-12204-60001-57

DATA STORE (INVERTED)

REVISIONS	APPROVED	DATE
A	AS ISSUED	mcf/ko	10/20/82
B	CORRECTED NUMBERS ON 74F373 & 74F374 ; CHANGED FABRICATED PART NUMBERS PER PRCR 'A'.	mcf/ko	3/3/83

D-12204-60001-58

70A 102E BP.EXT.ADDR1+ (33)
70A 102E BP.EXT.ADDR0+ (36)
102E BP.LOGADDR01+ (65)
70A 102E 30E BP.LOG.ADDR+ / 9

159C MC.DSI.WE- (55)

1818-3118 1420 U1606
1818-3118 1420 U1607
1818-3118 1420 U1206
1818-3118 1420 U1106
4K x 4 RAM

159C MC.IRDR.EN- (154)
169E MC.INDR.CLK+ (284)
28D 80C 70C 120D 40E 107E BP.WR.CYC- (5)

MC.DSI.DATA+

-2795 74F244 U1604
-2795 74F244 U1005

159B MC.IDIN.EN- (153)
169D MC.IDOUT.EN- (281)
159D 80E MC.DOUT.HLD- (54)
149B 129D 59E 90C 70E MC.S.BUS+ / 16

DIN (I)

RDR(I)

-2795 74F244 U1404
-2795 74F244 U1204

WDR(I)

FP.MEM.DATA+ 79A 40A 117B 19C 50D

-2701 74F374 U1504
-2701 74F374 U1104

-2700 74F373 U0907
-2700 74F373 U0908

(281)
(54)

16 / BP.S.BUS+ 109C 90C 79E

DOUT (1)

NOTE:
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ALL RESISTORS ARE 1/8W. 1%.
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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC8

MEMORY CONTROLLER - A900 DATA STORE (INVERTED)

HEWLETT PACKARD

12204-60001

D-12204-60001-58

MC 8

		D-12204-60001-59	
A	AS ISSUED	mcf/ko	10/20/82
B	CORRECTED NUMBERS ON 74F373 & 74F374.	mcf/ko	3/3/83

TA

TB

CPU DIN

MC S BUS BUF

10A 105A 140A 40D 130D BP.T.BUS+ / 16

169B MC.S.EN- (184)

159E CK.A.MEM.TA.MC+ (229)
169C MC.TA.EN- (312)
159E CK.A.MEM.TB.MC+ (230)
MC.TB.EN- (316)
169B MC.CPU.DIN.EN- (118)
169B

149B 129D 59E 70E 80E MC.S.BUS+ / 16

109C 79E 89E BP.S.BUS+ / 16

169B MC.LDIN.EN- (285)

MC.LDIN.LD+ (286)

105D BP.LDOUT.EN- (211)
168C CK.MEM.DS0.LDOUT+ (226)

109B LBP.DB+ / 16

129B MC.SCLK+ (200)
161B 102D LBP.IOGO- (189)
60D 102D LBP.MEMGO- (190)

LDIN

LDOUT

(286) MC.LDIN.LD+ 160B

NOTE:
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FOR INTERNAL USE ONLY.
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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC9

	MEMORY CONTROLLER - A900 MC TA/TB/LBUS DATA	HEWLETT PACKARD
		12204-60001
		D-12204-60001-59

MC 9

		D-12204-60001-60	
A	AS ISSUED	mcf/ko	10/20/82

BP.LOG.ADDR+ → 70A 80A 30E

BP.LOG.ADDR9+ … BP.LOG.ADDR1+

P1-05A	(34)	9
P1-03D	(21)	8
P1-03C	(20)	7
P1-03B	(19)	6
P1-03A	(18)	5
P1-02D	(17)	4
P1-02C	(16)	3
P1-02B	(15)	2
P1-02A	(14)	1

BP.T.BUS+ → 10A 90A 140B 40 130D

BP.T.BUS15+ … BP.T.BUS0+

P1-16C	(35)	15
P1-16B	(39)	14
P1-15D	(49)	13
P1-15C	(48)	12
P1-15B	(47)	11
P1-15A	(46)	10
P1-14D	(51)	9
P1-14C	(50)	8
P1-14B	(45)	7
P1-14A	(44)	6
P1-13D	(43)	5
P1-13C	(42)	4
P1-13B	(41)	3
P1-13A	(40)	2
P1-11D	(38)	1
P1-11C	(37)	0

FP.MEM.ADDR+ → 50A 112B

CA 78C w/R HARRIS

FP.MEM.ADDR23+ … FP.MEM.ADDR9+

P1-09B	(244)	23
P1-09A	(243)	22
P1-08D	(242)	21
P1-08C	(241)	20
P1-08B	(240)	19
P1-07D	(239)	18
P1-07C	(238)	17
P1-07B	(237)	16
P1-07A	(236)	15
P1-06D	(235)	14
P1-06C	(234)	13
P1-06B	(233)	12
P1-06A	(232)	11
P1-05D	(231)	10
P1-33C	(245)	9

BP.UIR.REG+ → 160A 10B

BP.UIR.REG31+ … BP.UIR.REG12+

P1-25D	(330)	31
P1-25C	(222)	30
P1-25B	(221)	29
P1-25A	(220)	28
P1-24D	(219)	27
P1-24C	(218)	26
P1-19D	(329)	12

LBP.DB+ → 90E

LBP.DB15+ … LBP.DB0+

P1-27D	(255)	15
P1-27C	(254)	14
P1-27B	(253)	13
P1-27A	(252)	12
P1-26D	(251)	11
P1-26C	(250)	10
P1-26B	(264)	9
P1-26A	(263)	8
P1-24B	(262)	7
P1-23D	(261)	6
P1-22C	(260)	5
P1-22B	(259)	4
P1-22A	(258)	3
P1-21D	(257)	2
P1-21C	(249)	1
P1-21B	(248)	0

BP.S.BUS+ → 79E 89E 90C

BP.S.BUS15+ … BP.S.BUS0+

P1-39B	(74)	15
P1-38D	(73)	14
P1-38C	(72)	13
P1-38B	(71)	12
P1-37D	(70)	11
P1-37C	(69)	10
P1-37B	(82)	9
P1-37A	(81)	8
P1-35D	(80)	7
P1-35C	(79)	6
P1-35B	(78)	5
P1-35A	(77)	4
P1-34D	(76)	3
P1-34C	(75)	2
P1-34B	(68)	1
P1-34A	(67)	0

P1-18C	(189)	LBP.IOGO- 161B 90E
P1-10B	(266)	LBP.MLOST- 140A 60E
P1-19B	(341)	LBP.MCHODOC- 60D
P1-19C	(267)	LBP.PFW- 140D 60E
P1-29A	(344)	LBP.REMEM- 60E
P1-29B	(265)	LBP.INTRQ- 140C 60D
P1-29C	(1)	LBP.MP+ (GROUND) 140C
P1-29D	(190)	LBP.MEMGO- 60D 90E
P1-30A	(347)	LBP.WE- 60E
P1-30B	(268)	LBP.SLAVE- 140D 60E
P1-30C	(342)	LBP.MRQ- 60E
P1-31A	(340)	LBP.IORQ- 60D
P1-32B	(346)	LBP.SCLK- 120B
P1-32C	(247)	LBP.CCLK- 127D
P1-33B	(53)	LBP.PON+ 60A 20C 10D 130D 40E
P1-19A	(343)	LBP.PE- 129B
P1-21A	(345)	LBP.SCHOD- 129D
P1-05B	(36)	BP.EXT.ADDR0+ 70A 80A
P1-05C	(33)	BP.EXT.ADDR1+ 70A 80A
P1-39C	(212)	BP.MEM.RD.REQ+ 60A 120B
P1-39D	(325)	BP.MEM.WR.REQ+ 120C
P1-33D	(225)	CK.A.MEM.D50.BP+ 150C 161C
P1-31D	(52)	CK.A.MEM.MC+ 10D 121D 150E
P1-01D	(65)	BP.LOG.ADDR01+ 80A
P1-01C	(66)	BP.LOG.ADDR0N+ 70A
P1-31B	(331)	CK.A.MEM.D30.BP+ 151D

BP.R2.UIR.REG+ → 160A 150E

BP.R2.UIR.REG23+ … BP.R2.UIR.REG20+

P1-23C	(173)	23
P1-23B	(172)	22
P1-23A	(216)	21
P1-22D	(215)	20

P1-16D	(326)	BP.MP.INT+	140C
P1-17A	(217)	BP.TRUE.WRITE+	150B
P1-17B	(58)	BP.AB.HIT+	160C 150E
P1-17C	(171)	BP.NORMAL+	150B 160C
P1-17D	(168)	BP.INVERT+	150C 160C
P1-18A	(211)	BP.LDOUT.EN-	90E
P1-18B	(213)	BP.NO.WP+	150C
P1-10A	(319)	BP.AB.DP.WR+	150D
P1-11A	(166)	BP.B.CA.ADR+	160B 150D
P1-33A	(321)	BP.B.DP.ADR+	150D
P1-11B	(328)	BP.UINTP+	140D
P1-30D	(324)	BP.JTAB.MEM-	130D
P1-31C	(167)	BP.DMA.CYCLE+	160A 150E
P1-32D	(210)	BP.KIS.S.OFF	169A 10C
P1-09C	(327)	BP.R2.STORE.EN-	150D

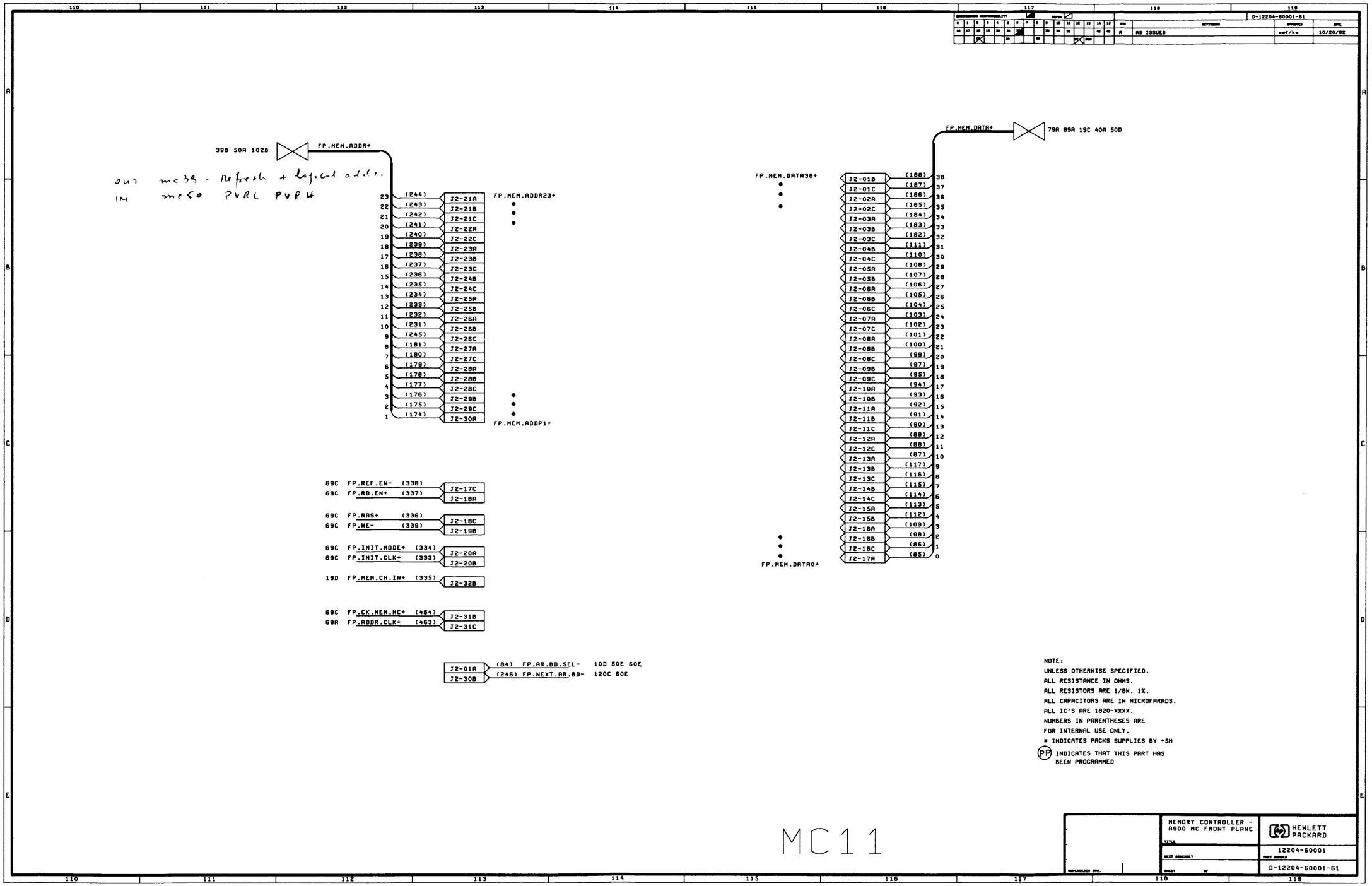
BP.MEM.BUSY+	(169)	P1-40B	69B 160E
BP.JTAB.INT-	(323)	P1-40C	149C
BP.INTP+	(322)	P1-40D	149C
BP.MISSED.TICK-	(170)	P1-09D	139D 120D
BP.PE.FREEZE-	(214)	P1-10C	59D
BP.AB.CA.WR-	(318)	P1-10D	159E
BP.WR.CYC-	(5)	P1-01B	29B 60B 70C 80C 120D 40E

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC10

TITLE	MEMORY CONTROLLER - BACKPLANE	HEWLETT PACKARD
NEXT ASSEMBLY		12204-60001
SHEET OF		D-12204-60001-60

MC 10


D-12204-80001-81
A5 ISSUED
mcf/ka
10/20/82
FP.MEM.ADDR+
39B 50A 102B
out mc39 - Refresh + logical addrs.
IN mc50 PURL PURH
FP.MEM.ADDR23+
FP.MEM.ADDP1+
J2-21A (244) 23
J2-21B (243) 22
J2-21C (242) 21
J2-22A (241) 20
J2-22C (240) 19
J2-23A (239) 18
J2-23B (238) 17
J2-23C (237) 16
J2-24B (236) 15
J2-24C (235) 14
J2-25A (234) 13
J2-25B (233) 12
J2-26A (232) 11
J2-26B (231) 10
J2-26C (245) 9
J2-27A (181) 8
J2-27C (180) 7
J2-28A (179) 6
J2-28B (178) 5
J2-28C (177) 4
J2-29B (176) 3
J2-29C (175) 2
J2-30A (174) 1
FP.MEM.DATA+
79A 89A 19C 40A 50D
FP.MEM.DATA38+
FP.MEM.DATA0+
J2-01B (188) 38
J2-01C (187) 37
J2-02A (186) 36
J2-02C (185) 35
J2-03A (184) 34
J2-03B (183) 33
J2-03C (182) 32
J2-04B (111) 31
J2-04C (110) 30
J2-05A (108) 29
J2-05B (107) 28
J2-06A (106) 27
J2-06B (105) 26
J2-06C (104) 25
J2-07A (103) 24
J2-07C (102) 23
J2-08A (101) 22
J2-08B (100) 21
J2-08C (99) 20
J2-09B (97) 19
J2-09C (95) 18
J2-10A (94) 17
J2-10B (93) 16
J2-11A (92) 15
J2-11B (91) 14
J2-11C (90) 13
J2-12A (89) 12
J2-12C (88) 11
J2-13A (87) 10
J2-13B (117) 9
J2-13C (116) 8
J2-14B (115) 7
J2-14C (114) 6
J2-15A (113) 5
J2-15B (112) 4
J2-16A (109) 3
J2-16B (98) 2
J2-16C (86) 1
J2-17A (85) 0
69C FP.REF.EN- (338)
69C FP.RD.EN+ (337)
J2-17C
J2-18A
69C FP.RAS+ (336)
69C FP.WE- (339)
J2-18C
J2-19B
69C FP.INIT.MODE+ (334)
69C FP.INIT.CLK+ (333)
J2-20A
J2-20B
19D FP.MEM.CH.IN+ (335)
J2-32B
69C FP.CK.MEM.MC+ (464)
69A FP.ADDR.CLK+ (463)
J2-31B
J2-31C
J2-01A (84) FP.AR.BD.SEL- 10D 50E 60E
J2-30B (246) FP.NEXT.AR.BD- 120C 60E
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
MC11
MEMORY CONTROLLER -
A900 MC FRONT PLANE
TITLE
HEWLETT PACKARD
12204-60001
D-12204-60001-61
SHEET OF

MC 11

REVISIONS			
ZONE	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	maf/ko	10/20/82
B	CORRECTED NUMBERS ON 74F374.	maf/ko	3/3/83
	CHANGED U1308 F244 TO S244 PER PRCR "B".		

D-12204-60001-62

19C MC.SCHOD- (306)
69D MC.PULLUP.CLR+ (406)
102D LBP.SCLK- (346)
59E MC.MULT.ERR.INT- (291)
69D 60B MC.PULLUP.PR+ (60)
60A 105D BP.MEM.RD.REQ+ (212)
69D 40C MC.PULLUP+ (4)
19D MC.MEM.CH.IN- (289)
60E 113E FP.NEXT.AR.BD- (246)
102E BP.MEM.WR.REQ+ (325)
29D 60C 70C 80C 40E 107E BP.WR.CYC- (5)
139D 107E BP.MISSED.TICK- (170)
29B 150B 50E MC.RD3- (197)
29B 150B 10C 50C MC.RD2- (162)
29B 50B 10D MC.RD1- (161)
29B MC.RD0- (302)
29D MC.NEXT.RD.CYC- (293)
29D MC.NEXT.WR.CYC- (297)
19C MC.MCST.CLK.EN- (390)
10D 102E 150E CK.A.MEM.MC+ (52)
29D MC.NEXT.REF.CYC- (294)
29D MC.NEXT.ST.CTR1- (296)
29D MC.NEXT.ST.CTR0- (295)
29D 60B 40E MC.RD.CYC- (61)
29D 30C 60D MC.REF.CYC- (57)
29D 151B MC.STATE.CNTR1- (63)
29D MC.STATE.CNTR0- (163)
19E MC.MCST.RREQ- (287)
19E MC.MCST.PR.INTR- (486)
139B MC.CCLK- (350)

-2693 74F109 U0805
-0683 74S04 U0804
-1449 74S32 U0407
-2693 74F109 U1403
-0681 74S00 U0305
-2693 74F109 U1403
-2701 74F374 U0403
-1449 74S32 U0705
-2701 74F374 U0303

MC.LCH.SCHOD- (379)
(200) MC.SCLK+ 90E
(343) LBP.PE- 102D
(392) MC.MEM.RD.REQ+ 20C
(393) MC.MEM.WR.REQ+ 20C
16 / MC.S.BUS+ 149B 59E 90C 70E 80E
MC.NEXT.AR.BD+ (397)
MC.SCLK+ (200)
CK.A.MEM.ST.MC+ (228)

MCST

BACKPLANE BUFFER

-2565 74S244 U1308

(350) MC.CCLK-
MC.LCH.SCHOD-
(52) CK.A.MEM.MC+
MC.PULLUP+
LBP.CCLK-
(247)

(247) LBP.CCLK- 102D
(345) LBP.SCHOD- 102D
(31) CK.MEM.1.MC+ 60B 20D 130D 150D
(22) CK.A.MEM.2.MC+ 50C 150C 140E 160E
(348) MC.BUF.CCLK- 130E

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MEMORY CONTROLLER - 8000 CACHE INTFC SIGNALS

HEWLETT PACKARD

12204-60001

D-12204-60001-62

MC12

MC 12

REVISIONS			
		D-12204-60001-83	
DESCRIPTION		APPROVED	DATE
A	AS ISSUED	mof/ko	10/20/82
B	CORRECTED NUMBERS ON 74F374, FABRICATED PART NUMBER CHANGED TO PURCHASED PART NUMBER PER PRCA "A".	mof/ko	3/3/83

69D MC.TBG.PULLUP+ (469)

128E MC.BUF.CCLK- (348)

DIPOSC
(14-PIN) OSC 14.7456 Mhz 25PPM
1813-0196
U0201

8 MC.CCLK- (350)

MC.TBG.D1+ (451)
/256
-1989
74LS393
U0205

MC.TBG.D2+ (452)

MC.TBG.D3+ (453)
/64
-1989
74LS393
U0105

-0683
74S04
U0106

(450) MC.TBG.B4-
/9
-1876
74S161
U0206

MC.TBG.B4+ (449)

149A MC.TBGE+ (208)

-0683
74S04
U0106

MC.TBGE- (165)

-0683
74S04
U0106

MC.TBG.D5- (454)

MC.TBG.D5+ (314)

(350) MC.CCLK- 121E

MC.SSTP.INT+ (310)

BP.MISSED.TICK- (170)

MC.TBGT.INT+ (313)

MC.TBG.SYNC3+ (456)

MC.TBG.SYNC2+ (315)

MC.TBG.SYNC1+ (455)

TBP/SSTP
-3048
82S153
U1107

MC.TBGT.INT.D+ (447)

MC.MISSED.TIC.D- (394)

MC.SSTF.INT.D+ (440)

-2701
74F374
U1307

159D 10B MC.IMSK.STOT- (282)

10A
90A
105A
40D
140B
BP.T.BUS+ / 2
149A MC.SSTPE+ (439)

MPL03

105E BP.JTAB.MEM- (324)

60B 20D
128D 150D CK.A.MEM.1.MC+ (31)

60A 20C
10D 102D 40E LBP.PON+ (53)

MC.R1.PON+ (410)

MC.R2.PON+ (413)

(313) MC.TBGT.INT+ 140C

(170) BP.MISSED.TICK- 120D 107E

(310) MC.SSTP.INT+ 140C

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC13

	MEMORY CONTROLLER - A900 TBG & SSTP	HEWLETT PACKARD
	NEXT ASSEMBLY	12204-60001
	SHEET OF	D-12204-60001-83

MC 13

	D-12204-60001-64		
A	AS ISSUED	mat/ko	10/20/82
B	CORRECTED NUMBERS ON 74F374	mat/ko	3/3/83

102D 60E LBP.MLOST- (266)

29D 10A 90A 105A 40D 130D BP.T.BUS+ / 9

IMSK -2701 74F374 U0307

19B CK.A.MEM.MSK.MC+ (332)

19E MC.INTR.MREG- (374)

160A 105C 10D BP.UIR.REG12+ (329)

105D BP.MP.INT+ (326)

139D MC.SSTP.INT+ (310)

139D MC.TBGT.INT+ (313)

105E BP.UINTP+ (328)

MC.TYPE23+ (459)

MC.TYPE3+ (460)

MC.TBGH+ (448)

MC.R2.INTRQ- (412)

MC.TBGF.INT+ (445)

MC.FLO.INT+ (365)

MC.R2.PFW- (300)

MC.R2.SLAVE- (414)

MC.R2.VECT.STOT- (415)

INTERRUPT -2247 825100 U0208 (PP)

MPL04

MC.R1.INTRQ- (408)

-2701 74F374 U1108

60D 102D LBP.INTRQ- (265)

159D MC.VECT.STOT- (461)

59D MC.MULT.ERR.INT+ (194)

102D 60E LBP.PFW- (267)

102D 60E LBP.SLAVE- (268)

50C 128D 160E CK.A.MEM.2.MC+ (22)

MC.R1.SLAVE- (411)

MC.R1.PFW- (409)

MC.MULT.BIT.INT+ (468)

MC.R2.PFW- (300)

MC.INTR.PRI+

INTR -2701 74F374 U0308

MC.SSTP+ (438)

MC.TBGE+ (208)

130D

130B

8 / MC.S.BUS+

129D 59E 90C 70E 80E

(322) BP.INTP+

(323) BP.JTAB.INT-

102D

102D

6-63

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M

(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

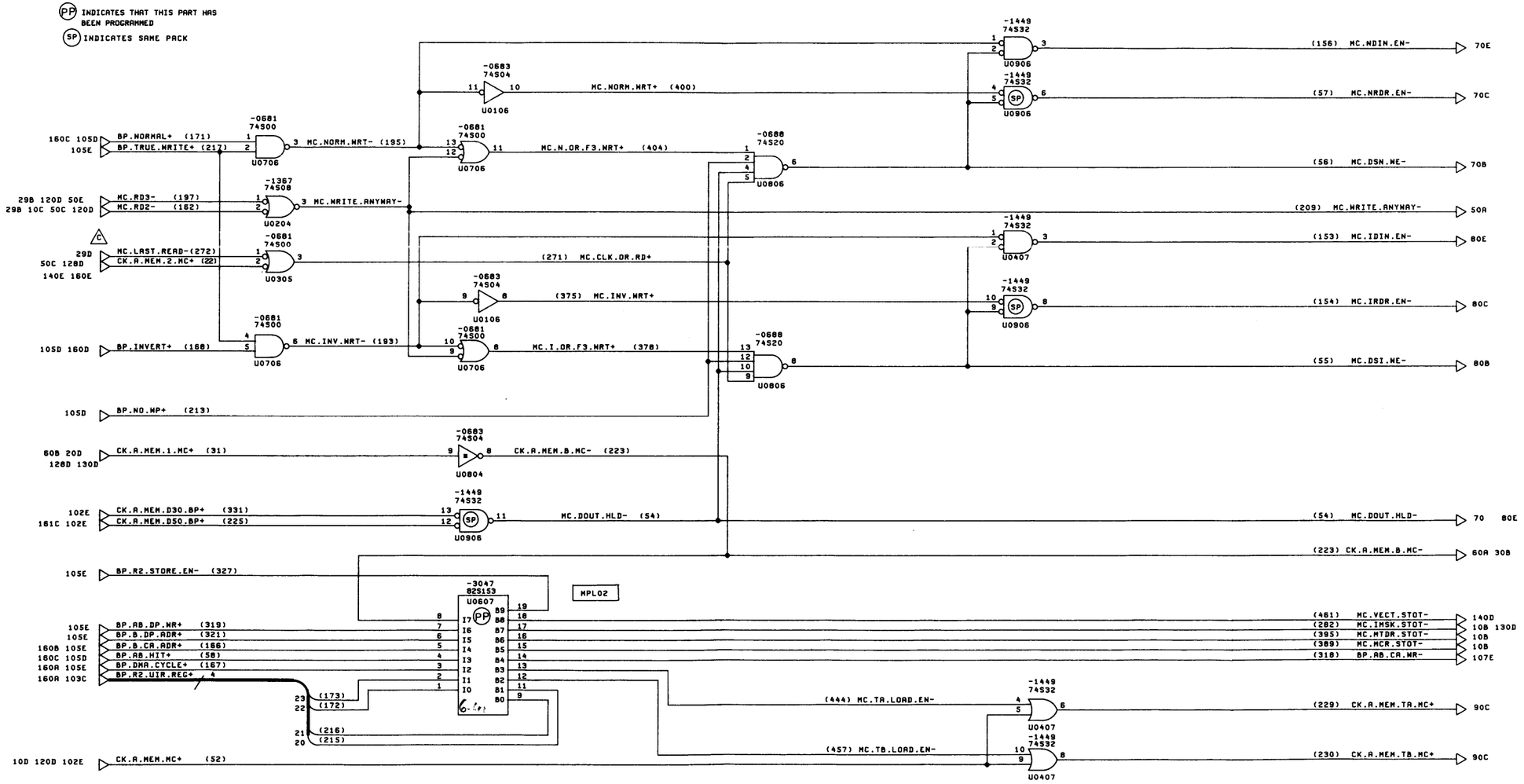
MC14

	MEMORY CONTROLLER - A900 INTERRUPTS	HEWLETT PACKARD
		12204-60001
		D-12204-60001-64

MC 14

	D-12204-60001-65		
	REVISIONS	APPROVED	DATE
A	AS ISSUED	maf/ko	10/20/83
B	CHANGED FABRICATED PART NUMBERS PER PRCR "A".	maf/ko	3/3/83
C	CIRCUIT CHANGE PER PC22-6770.	gd/ko	3/9/83

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
(SP) INDICATES SAME PACK



MC15

	MEMORY CONTROLLER - A900 CACHE WRITE CONTROL	HEWLETT PACKARD
	TITLE	12204-60001
	NEXT ASSEMBLY	PART NUMBER
	SHEET OF	D-12204-60001-65

MC 15

REVISIONS			
		D-12204-60001-66	
ECO	DESCRIPTION	ENGINEER	DATE
A	AS ISSUED	oo/ko	10/20/82
B	CHANGED FABRICATED PART NUMBER	mcf/ko	3/3/83
	TO PURCHASED PART NUMBER PER PRCR "A"		

105E 150E BP.DMA.CYCLE+ (167)

105E 150E BP.R2.UIR.REG+ /4

10B 105C BP.UIR.REG+ /6

MPL01

-3046 82S153 U0508

(330) 8 (222) 7 (221) 6 (220) 5 (219) 4 (218) 3

(173) (172) (216) (215)

99E MC.LDIN.LD+ (286)

102D 91E LBP.IPGO- (189)

105E 150D BP.B.CA.ADR+ (166)

-0683 74S04 U0604 MC.B.CA.ADR- (349)

105D 150E BP.AB.HIT+ (58)

150C 102E

-0683 74S04 U0604 MC.AB.HIT- (289)

150B 105D BP.NORMAL+ (171)

150C 105D BP.INVERT+ (168)

29B 60A 30E MC.RDO+ (159)

69B 107D BP.MEM.BUSY+ (169)

50C 128D 140E CK.A.MEM.2.MC+ (22)

-0681 74S00 U0104 MC.N.LD2- (403)

-0681 74S00 U0104 MC.I.LD2- (377)

-1367 74S08 U0904 MC.S.BUS.USED+ (443)

MC.LDOUT.LD+ (388)
MC.DRIVE.S.BUS+ (275)
MC.READ+ (62)

-0685 74S10 U0505

-1158 74S51 U0108

MC.READ+ (62)
BP.AB.HIT+ (58)

-1367 74S08 U0204

MC.LDOUT.LD+ (388)
CK.A.MEM.D50.BP+ (225)

-0685 74S10 U0505

-0685 74S10 U0505

-0685 74S10 U0404

-1367 74S08 U0204 MC.NWDR.LD- (402)

-1367 74S08 U0204 MC.IWDR.LD- (376)

-1322 74S02 U0704

-1322 74S02 U0304

-1322 74S02 U0304

(210) BP.KIS.S.OFF- → 10C 10E

(118) MC.CPU.DIN.EN- → 90C
(285) MC.LDIN.EN- → 90D

(164) MC.S.EN- → 90B

(316) MC.TB.EN- → 90C

(226) CK.A.MEM.D50.LDOUT+ → 90E

(312) MC.TA.EN- → 90C

(292) MC.NDOUT.EN- → 70E

(281) MC.IDOUT.EN- → 80E

(298) MC.NWDR.CLK+ → 70C

(284) MC.IWDR.CLK+ → 80D

SQ 110 A

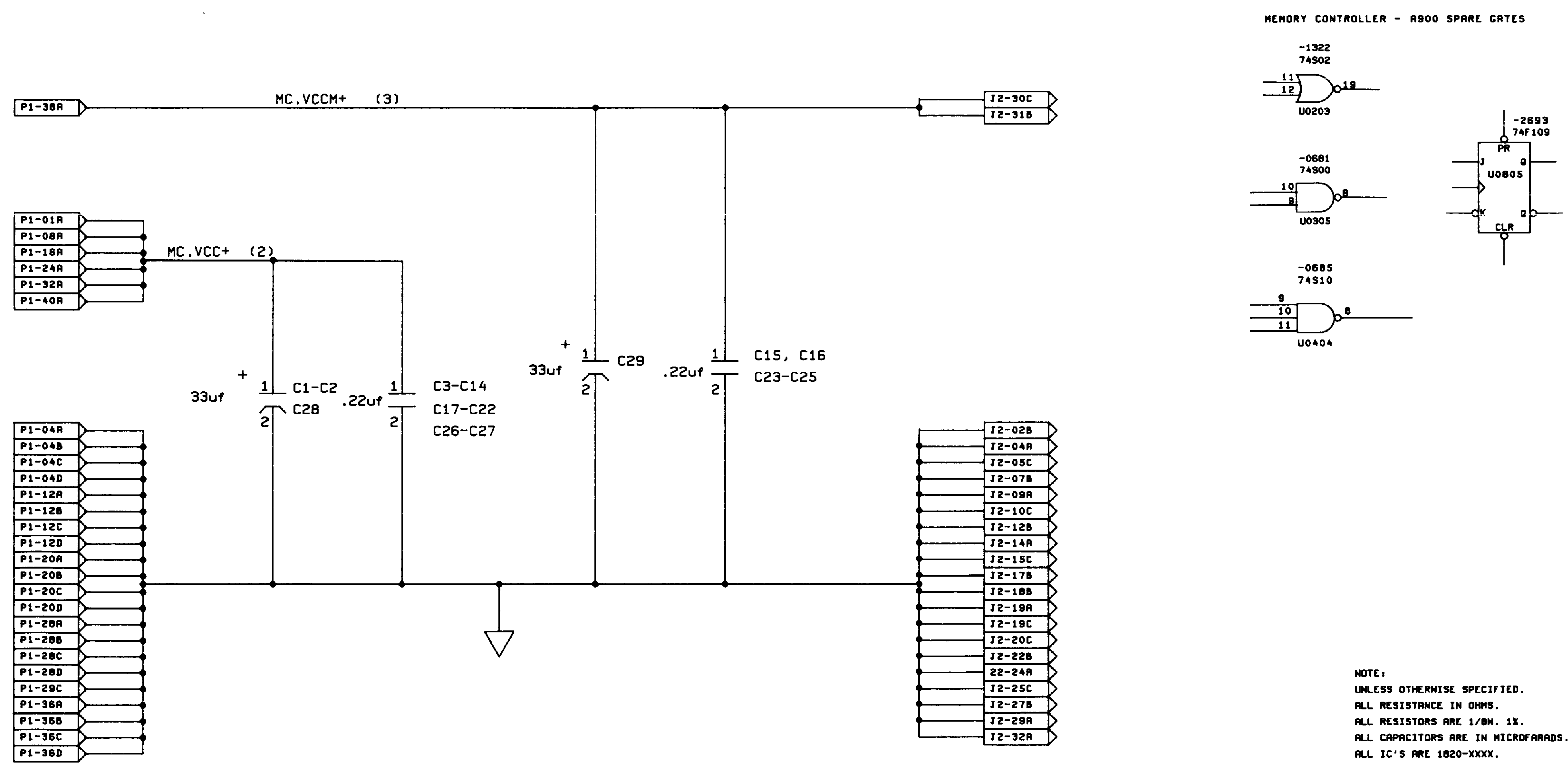
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

MC16

	MEMORY CONTROLLER - A900 CACHE SBUS CONTROLLER	HEWLETT PACKARD
	NEXT ASSEMBLY	12204-60001
	SHEET OF	D-12204-60001-66

MC 16

A AS ISSUED jaf/ko 10/20/82



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED

MC17 & MC18

MEMORY CONTROLLER - A900 VCC & GROUND

HEWLETT PACKARD

12204-60001

D-12204-60001-68

MC 17 . 18

Chapter 7
Memory Array

7.1 Introduction

This chapter describes the block diagram and the theory of operation of the memory array (AR) card. To understand fully the operation of this microprogrammed computer, please refer to the HP 92049A RTE Microprogramming Package Reference Manual, Part No. 92049-90001.

7.2 Block Description

The memory array circuitry is implemented on the Memory Array (AR) card. Figure 7-1 is a block diagram of the memory array card shown in Figure 7-2.

The card is divided into the following functional blocks:

Adder MUX and RAM Drivers
Initialization Logic
Bank Select RAMs
Control Logic
Data Transceivers
RAM Array

These functional blocks are described in general in the paragraphs under subheading 7.2 and their logical operations (theory of operation) are described in the paragraphs under subheading 7.3.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

The A900 memory system consists of Cache (CA), Memory Controller (MC) and Memory Array (AR) cards. The AR cards are where the actual data is stored in the memory system. A minimum system would include the CA, MC and one AR card with additional AR cards added for more memory, if desired. The AR card is exclusively controlled by the MC card. The address lines, data lines and control signals come from the MC card.

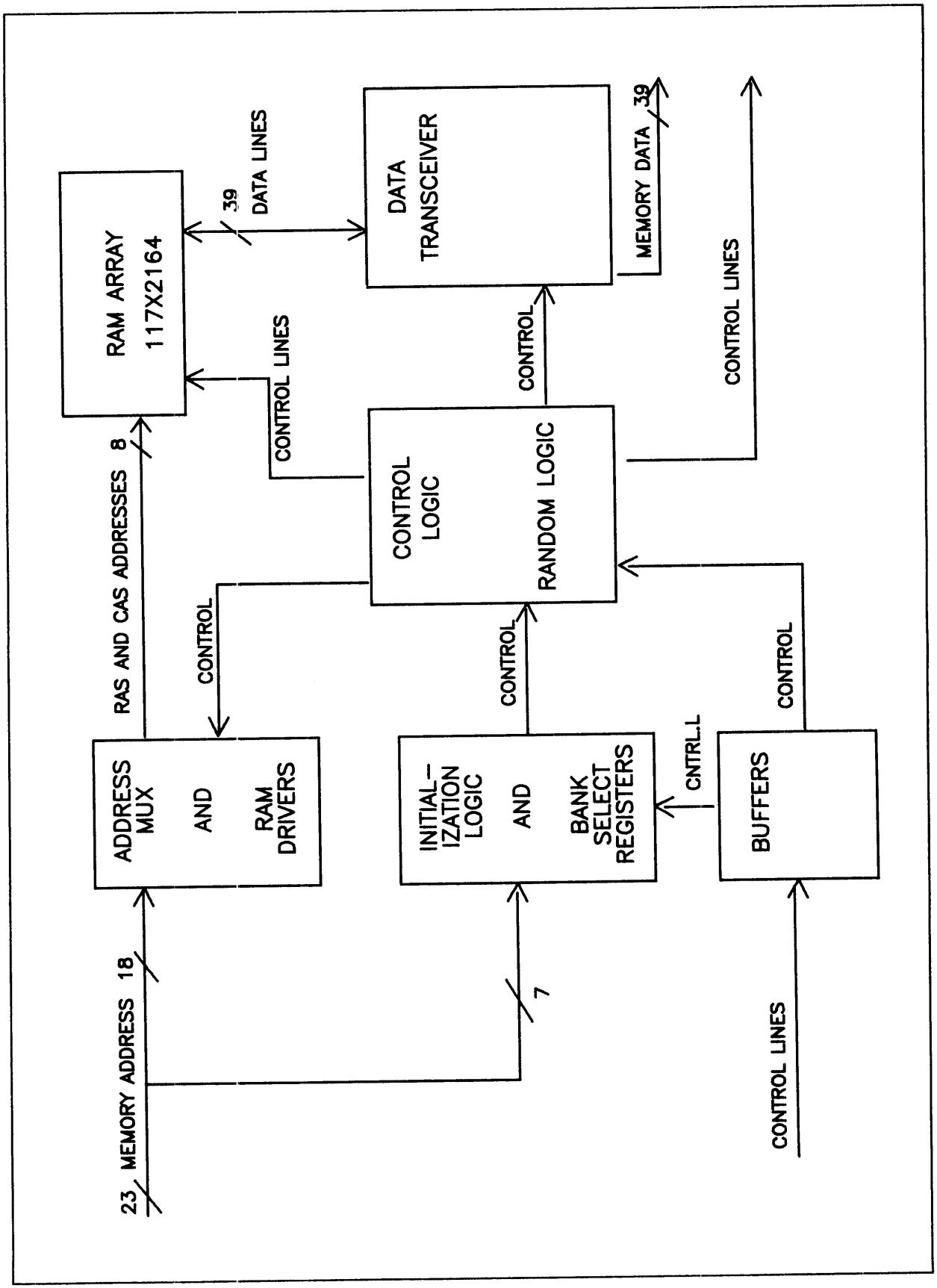


Figure 7-1. Memory Array Card Functional Block Diagram

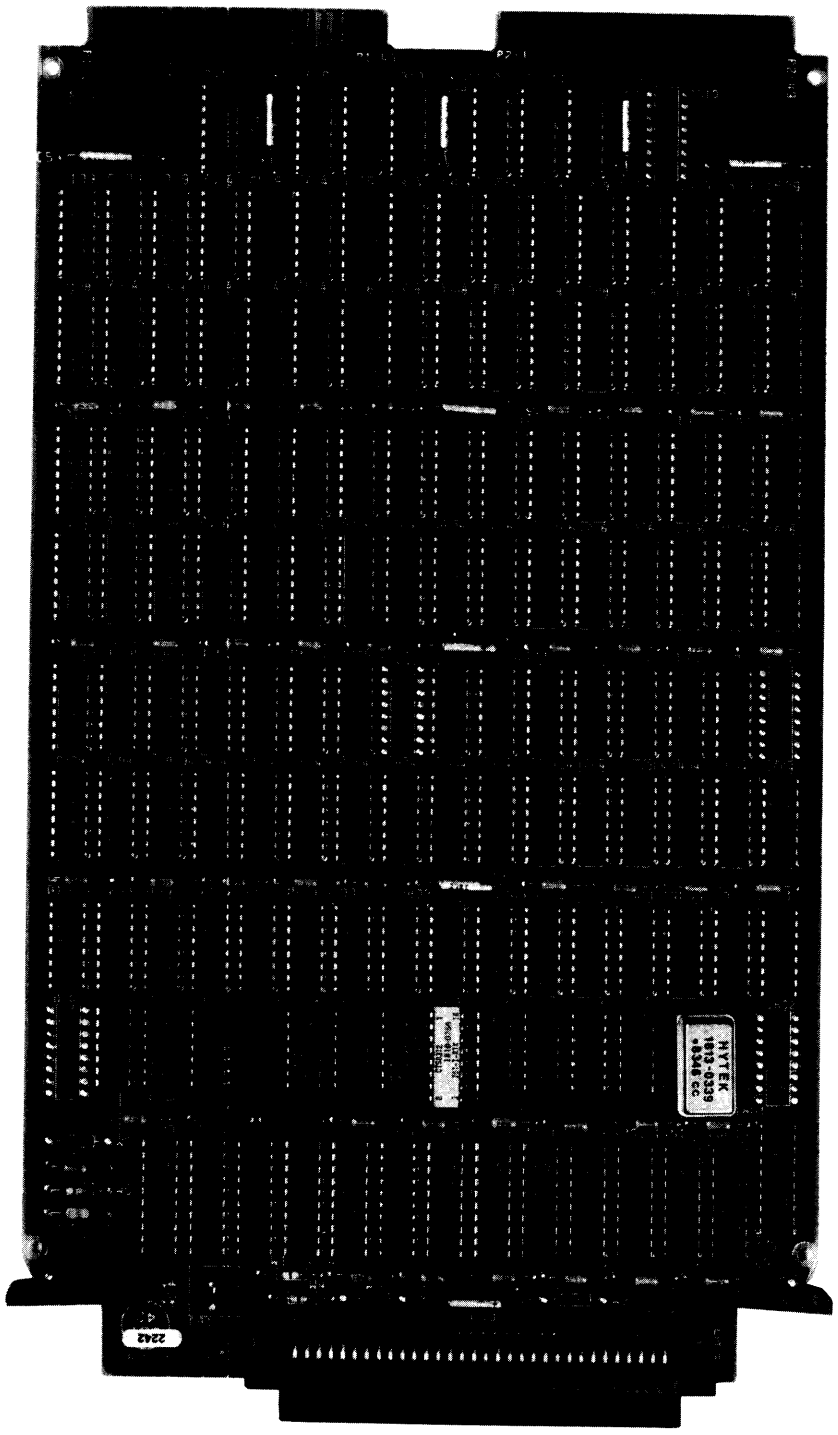


Figure 7-2. Memory Array Card (12220-60001)

As shown in the block diagram, the AR card has one 39-bit bidirectional data bus, FP.MEM.DATA+ (bits 38 - 0), and one 23-bit address bus, FP.MEM.ADDR+ (bits 23 - 1). The RAM Array is composed of three banks, and each bank includes 39 RAMs. The RAM Array receives its address from the RAM drivers and the memory data flows through the data transceivers. Each AR card is initialized to a unique address space so that the system can access it. This is accomplished in the INIT (initialization) block.

7.2.1 Data Format

The AR card has three banks of data. Data is stored in Main Memory as two 16-bit words with seven error correction bits to detect and correct errors. The data is transferred directly to frontplane from the AR cards. All data transfers occur 39 bits at a time (32 data bits + 7 error correction bits).

7.2.2 Data Capacity

The capacity of the Memory system depends on the number of address lines available. Since there are 24 address lines (on the frontplane to AR cards) 32 Mbyte of memory can be addressed. The amount of memory present in the system depends on the number of AR cards present in the system. There is a limit of eight AR cards per system. Provisions have been made on the AR card so that either 64k X 1 bit or 256k X 1 bit dynamic RAMs can be used. Three-quarters megabyte of memory can be obtained with the 64k-bit RAMs at 64k memory locations per bank, while 3M byte of memory can be obtained with 256k RAMs at 256k memory locations per bank.

7.2.3 Memory Array Operation

Operation of the AR card begins with initialization of the AR card to a unique section of memory. After initialization of all AR cards in the system and selection of one AR card, data can be written or read by proper issuance of the control signals generated by the MC card. There are two active "low" and two "high true" signals that drive the circuitry needed for read, write and refresh operations.

7.2.3.1 Read Operation

A read operation occurs when FP.WE- and FP.REF.EN- are deasserted. The address lines and control lines are stable before the issuance of FP.RAS+. In this way the signals are set up well in advance to actual operation. The data is driven out of data transceivers. A complete memory access to main memory for a read occurs in four microcycles at 130 nanoseconds (0.13μs) per microcycle assuming that no errors are detected. Therefore, the fastest data transfer rate for read is:

$$\text{access rate} = 2 \times 1/(0.130 \times 4) = 3.85 \text{ Mword/sec}$$

A read with error adds one more microcycle to the read operation.

7.2.3.2 Write Operation

The AR card does a write operation if FP.RAS+ and FP.WE- are asserted and FP.REF.EN- is deasserted. The incoming data lines, address lines and control lines should be stable well in advance. The data transceivers are only active during the assertion of FP.RAS+. To shut off these transceivers in the shortest possible time, the FP.RAS+ is actually fed through the driver that is gated by the FP.RAS+ line itself. In this way the actual shutdown of FP.RAS+ controls the disabling of the data transceivers. A complete memory access to main memory for a write occurs in three microcycles.

7.2.3.3 Refresh Operation

The characteristics of the dynamic RAMs require memory refreshing for maintaining data. This refreshing must be performed every two milliseconds for 64k RAMs (4 ms for 256k RAMs) and be interleaved between requested memory cycles. For refresh of the AR card, the MC card will assert the FP.REF.EN- line.

The MC card controls the actual time when the AR card will be refreshed, but the AR card does the actual refreshing. The AR card does a refresh for RAS. For this reason, the CAS line, data lines and write line are disabled. During a refresh, all three banks of RAMs are selected to refresh all banks. In this way all RAMs get an RAS and refresh the row that is specified on the address lines by the MC card. Since a refresh operation selects all three banks, a large current surge can occur. For this reason, 33 microfarad capacitors are installed, one per column.

7.2.4 Initialization

Each AR card, when installed, must have a unique address space so that the system can access it. The AR cards are automatically configured by the MC in an ascending address order. Thus, if two cards are interchanged, they are automatically reconfigured to form the ascending address sequence. The advantage of this scheme is that identical memory modules become unique in the address space of the computer without the aid of manually selected switch or jumper settings or dedicated backplane location.

7.2.4.1 Bank Select RAM

The function of decoding the high-order address bits and generating "bank select" and "card select" signals on the AR card is performed by the Bank Select RAM (BSR). The 64k-bit or 256k-bit dynamic RAMs on the AR card are divided into three banks.

Physical address bits 23 - 17 are the bank address bits that address the BSR on each AR card. The BSR is a 4-bit wide static RAM, three bits of which are the bank select signals for the three banks of dynamic RAMs. The fourth bit is unused. The contents of the BSR (which holds "low true" data) is "0" in the bit assigned to a given bank at that bank's address, and "1s" for all other bank addresses. The BSR replaces address jumpers and comparators that are commonly used to decode high-order address bits.

The BSRs are initialized by the memory controller under microcode control. The memory controller drives a bank address to the AR cards and provides a write pulse to write the correct data into the BSR. This is repeated 128 times using bank addresses 0 through 127 in ascending order.

7.2.4.2 Shift Register

The data to write into the BSRs is provided by 3-bit shift registers on each AR card that are linked together through a chained frontplane signal. Initialization begins by clearing the shift register. Then, while the memory controller is driving bank address "0" onto the frontplane, it sends a "1" to the first bit of the shift register on the first AR card where it is clocked in, and is written (inverted) into address "0" of the BSR for the bit assigned to the first bank of dynamic RAMs.

At the same time, all of the other BSRs are writing "1s" into address "0". Next the memory controller increments its bank address counter to "1", drives this bank address onto the frontplane, clocks the shift register, and sends a write pulse to the BSRs. This writes a "0" into the second bit on the first AR card at address "1", and "1s" into all other BSRs at address "1".

Clocking the shift register moved the data bit from the first bit on the first AR card to the second bit on the first AR card. Similarly, the fourth cycle of this process moves this data bit into the first bit of the shift register on the second AR card, and so on. After all 128 bank addresses have been driven across the frontplane, and 128 clock edges and write pulses have been sent, the BSRs are fully initialized.

7.2.4.3 Clock

AR cards loaded with 256k-bit RAMs have four times as much data storage as AR cards loaded with 64k-bit RAMs. Each bank of 256k-bit RAMs is the equivalent of four banks of 64k-bit RAMs. Consequently, the shift register on an AR card with 256k-bit RAMs is clocked four times more slowly, and each BSR bit holds "0s" at four consecutive "bank" addresses instead of only one. One restriction of this approach is that when both 64k-bit RAM AR cards and 256k-bit RAM AR cards are used in the same system, the 256k-bit RAM AR cards should be placed closest to the memory controller to prevent the shift register data bit from getting out of sync with the slower clock. Figure 7-3 shows the state of the BSRs in an initialized system:

	2.25 Mbyte System			4.5 Mbyte System		
	AR #1 (64k)	AR #2 (64k)	AR #3 (64k)	AR #1 (256k)	AR #2 (64k)	AR #3 (64k)
Bank	BSR	BSR	BSR	BSR	BSR	BSR
Addr	1 2 3	1 2 3	1 2 3	1 2 3	1 2 3	1 2 3
0	0 1 1	1 1 1	1 1 1	0 1 1	1 1 1	1 1 1
1	1 0 1	1 1 1	1 1 1	0 1 1	1 1 1	1 1 1
2	1 1 0	1 1 1	1 1 1	0 1 1	1 1 1	1 1 1
3	1 1 1	0 1 1	1 1 1	0 1 1	1 1 1	1 1 1
4	1 1 1	1 0 1	1 1 1	1 0 1	1 1 1	1 1 1
5	1 1 1	1 1 0	1 1 1	1 0 1	1 1 1	1 1 1
6	1 1 1	1 1 1	0 1 1	1 0 1	1 1 1	1 1 1
7	1 1 1	1 1 1	1 0 1	1 0 1	1 1 1	1 1 1
8	1 1 1	1 1 1	1 1 0	1 1 0	1 1 1	1 1 1
9	1 1 1	1 1 1	1 1 1	1 1 0	1 1 1	1 1 1
10	1 1 1	1 1 1	1 1 1	1 1 0	1 1 1	1 1 1
11	1 1 1	1 1 1	1 1 1	1 1 0	1 1 1	1 1 1
12	1 1 1	1 1 1	1 1 1	1 1 1	0 1 1	1 1 1
13	1 1 1	1 1 1	1 1 1	1 1 1	1 0 1	1 1 1
14	1 1 1	1 1 1	1 1 1	1 1 1	1 1 0	1 1 1
15	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	0 1 1
16	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 0 1
17	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 0
18	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1
.	. . .	. . .	. . .	. . .	. . .	. . .
.	. . .	. . .	. . .	. . .	. . .	. . .
.	. . .	. . .	. . .	. . .	. . .	. . .
126	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1
127	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1	1 1 1

Figure 7-3. System Examples of BSR Contents

All of the signals necessary to initialize the BSRs are bits in the memory control register (refer to Chapter 6).

7.2.5 Addressing

The memory system can address up to 32 Mbytes of memory with its 24-bit address bus. Bits 23 - 17 of memory address are used in selecting one of 128 banks in the case of 64k-bit RAMs. If the AR card contains 256k-bit RAMs then bits 23 - 19 are used in selection of the banks. If any of the three banks on a given card is selected then that card is selected. In the case of 64k-bit RAMs, bits 16 - 1 are used to address a unique location in a bank. For 256k-bit RAMs, bits 18 - 1 are used to address a unique location in a bank.

7.2.5.1 RAS and CAS

The RAM elements need two clock signals to allow access of the array. This is necessary since the RAM elements are organized into a 64k by 1 or 256k by 1 matrices and thus require a 16- or 18-bit address, respectively, to identify each memory cell. Since the RAM has a 16-pin DIP package, there are insufficient pins to allow direct addressing. Therefore, the 16- or 18-bit address is split into two groups of eight or nine, respectively. The low-order address is called ROW address and the upper-order address is called COLUMN address. The procedure for accessing a RAM cell is as follows:

1. Set up ROW address at RAM input
2. Apply RAS clock to RAM
3. Set up COLUMN address at RAM input
4. Apply CAS clock to RAM

The timing of these two clocks is critical to efficient memory timing. Therefore, a delay line is incorporated on each AR card to ensure a tightly controlled time spacing between the RAS and CAS pulses. Thus, when the RAS pulse arrives from the memory controller and is asserted at the RAMs, the CAS pulse occurs a precise time later at the RAMs.

7.2.5.2 Address MUX

Equally as critical as the timing of the RAS and CAS signals is the timing of the multiplexer switching of the ROW and COLUMN addresses. To ensure the correct timing between clocks and address switching, the same delay line is used to switch the multiplexer from row address to column address. This signal occurs from an intermediate tap on the delay line.

7.2.6 Data Transceivers

The data to be written into or read from the RAMs on AR cards is buffered by data transceivers. The direction of flow of data is determined by the write signal received from MC card. These data buffers are enabled when the AR card is selected and the AR is not in refresh mode.

7.2.7 +5M POWER

Whenever power is removed from memory, data present in memory will be lost. Under AC power failure with battery backup operation, +5M must be applied to the memory for retention of data. All the circuitry involved in refreshing the RAMs should be connected to +5M to maintain the refresh operation.

7.3 Theory of Operation

The A900 Computer Array Card theory of operation is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 7-1 and the schematics at the end of this section of the manual. The schematic pages are referred to by a two letter card mnemonic followed by a page number; e.g., the schematics for the array card are AR1, AR2, etc.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U0602 (AR23B) refers to part U0602 on the memory array card in row 6/column 2, which is shown on schematic page AR3 at horizontal location 3 and vertical location B.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

7.3.1 Data Format and RAM Array

Data is stored as two 16-bit words with seven error correction bits in main memory. The RAM array consists of 117 dynamic RAMs, arranged in three rows (banks) of 39 (32 data bits plus seven error correction bits) The RAMs in bank-1 are located on schematics AR3 and AR4. Sheet AR3 holds the RAMs for bits 19 - 0 and sheet AR4 contains the RAMs for bits 39 - 20 of bank-1.

Bank-2 and bank-3 are located on schematics AR5, AR6, AR7, and AR8. They are arranged in the same way as bank-1. During any access only one bank is activated, except for refresh which accesses all banks of all AR cards simultaneously. If an AR card is not selected, all RAMs on that card are in standby mode. This reduces power requirements on a system scale

7.3.2 Data Capacity and Addressing

The capacity of the Memory system depends on the number of address lines available. Since there are 24 address lines (on the frontplane to AR cards) 32 Mbyte of memory can be addressed. The amount of memory present in the system depends on the number of AR cards present in the system. There is a limit of eight AR cards per system.

To accomplish the addressing of either 64k-bit RAMs or 256k-bit RAMs, the address bits FP.MEM.ADDR+ (bit 9) and FP.MEM.ADDR+ (bit 18) are jumpered by J1 and J2 (AR12C), so that they can be used either as row or column address or bank select bits.

7.3.3 Memory Array Operations

Operation of the AR card begins with initialization of the AR card to a unique section of memory. After initialization of all AR cards in the system and selection of one AR card, data can be written or read by proper issuance of the control signals generated by the MC card. There are three active "low" and one "high true" signals that drive the circuitry needed for read, write and refresh operations. These four signals, FP.RAS+, FP.REF.EN-, and FP.WE- are received by buffer U0801 (AR13D), and FP.RD.EN+ is received by gate U1302 (AR113E). These frontplane signals are used indirectly to control the array through buffers and AND/OR gates. Refer to the subheading RAS and CAS under Addressing for the RAS and CAS control signals, and to Refresh for the FP.REF.EN- signal.

In Figures 7-4, 7-5, and 7-6, signal FP.RAS+ is represented by AR.BNKX.RAS.X-, FP.WE- is represented by AR.BNK.WE.X-, and the signal AR.BNKX.CAS.X- is generated from AR.REF.EN+ and board select: where for BNKX, "X" equals the bank number; where for RAS.X and CAS.X, "X" represents A or B; and where for WE.X, "X" represents A, B, C, or D. FP.RD.EN+ become AR.DATA.EN-.

7.3.3.1 Read Operation

A read operation occurs when FP.WE- and FP.REF.EN- are deasserted and FP.RAS+ and FP.RD.EN+ are asserted. Figure 7-4 shows the timing diagram for a read operation with no errors, which takes four microcycles.

As shown in the idle state the address is set by the MC. In RD0 the FP.RAS+ (AR.BNKX.RAS.X-) signal is asserted and 80 nanoseconds later the AR.CAS.EN+ (AR.BNKX.CAS.X-) signal is asserted. The data becomes valid in the middle of RD1 and FP.RD.EN+ (AR.DATA.EN-) enables the data transceivers causing the memory array to drive the FP.MEM.DATA[38:0]+ bus. If there is an error in the data just read from the AR card, the read cycle will be extended to five microcycles. Figure 7-5 shows the timing diagram for a read with error. The error will be detected in RDX and the corrected data is written to the Cache in the RDX microcycle.

7.3.3.2 Write Operation

The AR card does a write operation if FP.WE- (AR.BNK.WE.X+) is asserted and FP.REF.EN- is deasserted. Figure 7-6 shows the timing diagram for the write operation. As shown, the address should be stable before the FP.RAS+ (AR.BNKX.RAS.X-) signal is asserted in WRD1. The AR.CAS+ (AR.BNKX.CAS.X-) will be asserted 80 nanoseconds later and data will be written into the RAMs when the AR card data transceivers at U1601 (AR22D), U1501 (AR24D), U1401 (AR25D), U1301 (AR26D) and U1201 (AR27D), are enabled and AR.DATA.IN+ is asserted at U1002 (AR15E).

7.3.3.3 Refresh Operation

For refresh of the AR card, the MC card will assert the FP.REF.EN- line, which is buffered by U0402 (AR14E). Signals AR.RAS1.EN+, AR.RAS2.EN+ and AR.RAS3.EN+ are either driven by the upper-half of U0501 (AR15D) or by the lower-half of the same chip depending on the assertion of AR.REF.EN+. If this signal is asserted, then the AR card is in "refresh mode" and the upper-half of U0501 (AR15D) is disabled while the lower-half is enabled by the inverted version of AR.REF.EN+ U0402 (AR16E). U0402 (AR113C) is used to disable the CAS drivers, when AR.REF.EN+ is true. AR.WE- is buffered by the upper-half of U0301 (AR116A) to generate the write signals to the RAMs.

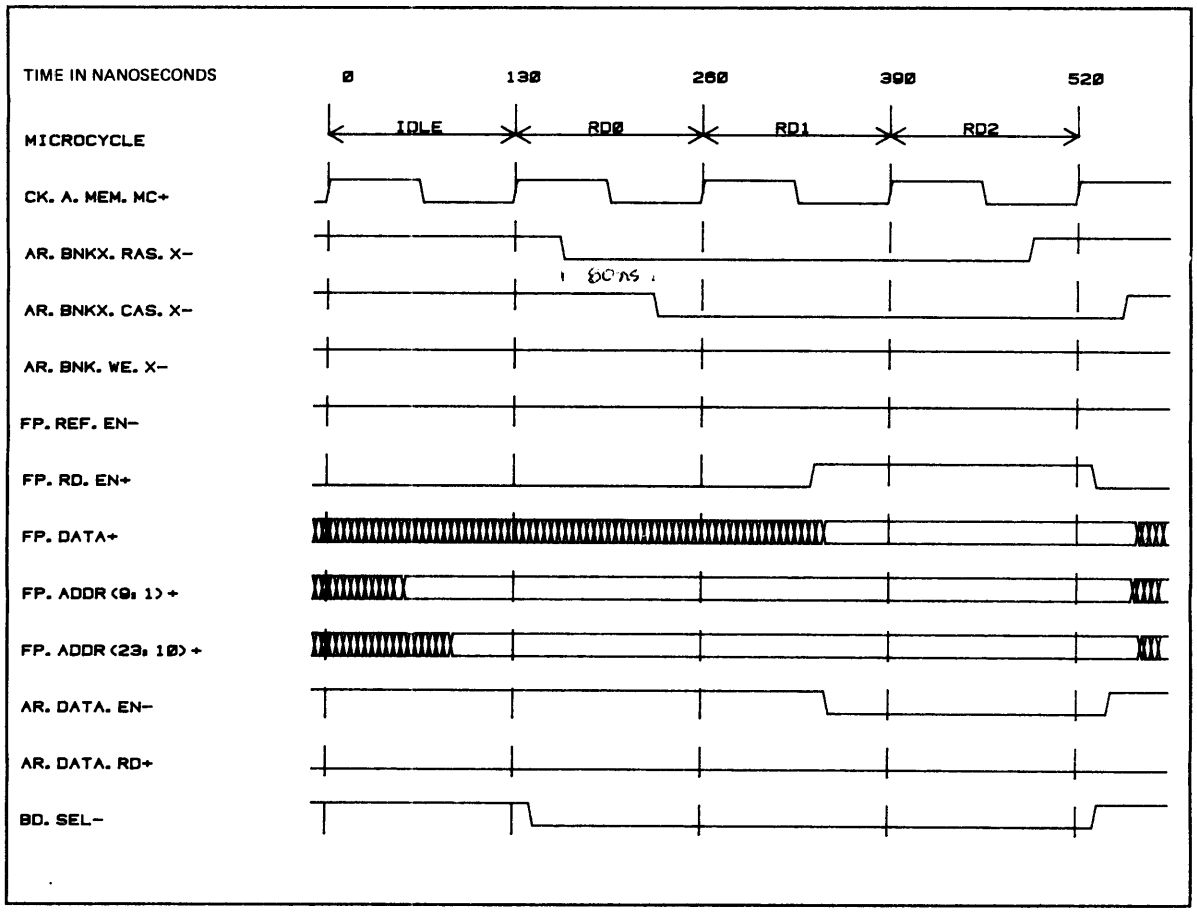


Figure 7-4. Signals For Memory Read With No Errors

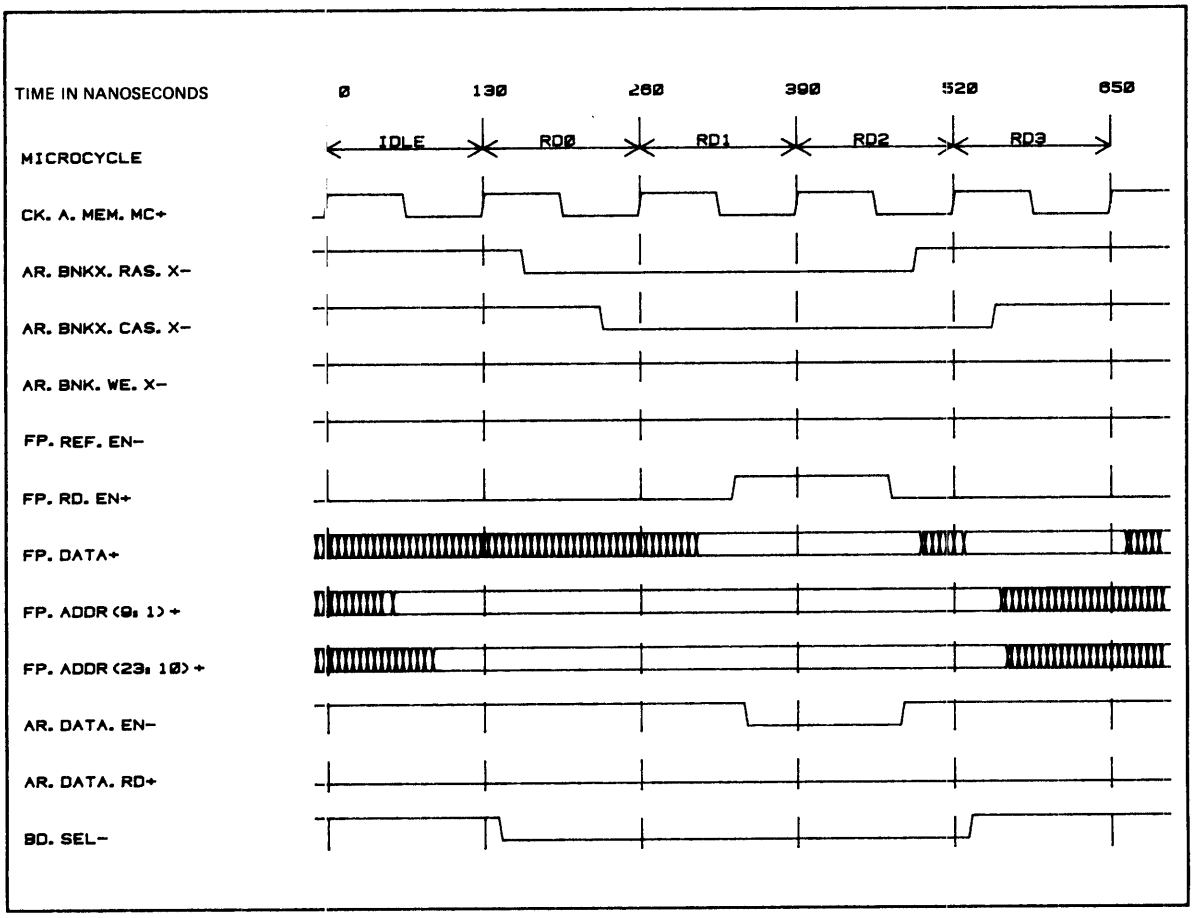


Figure 7-5. Signals For Memory Read With Errors

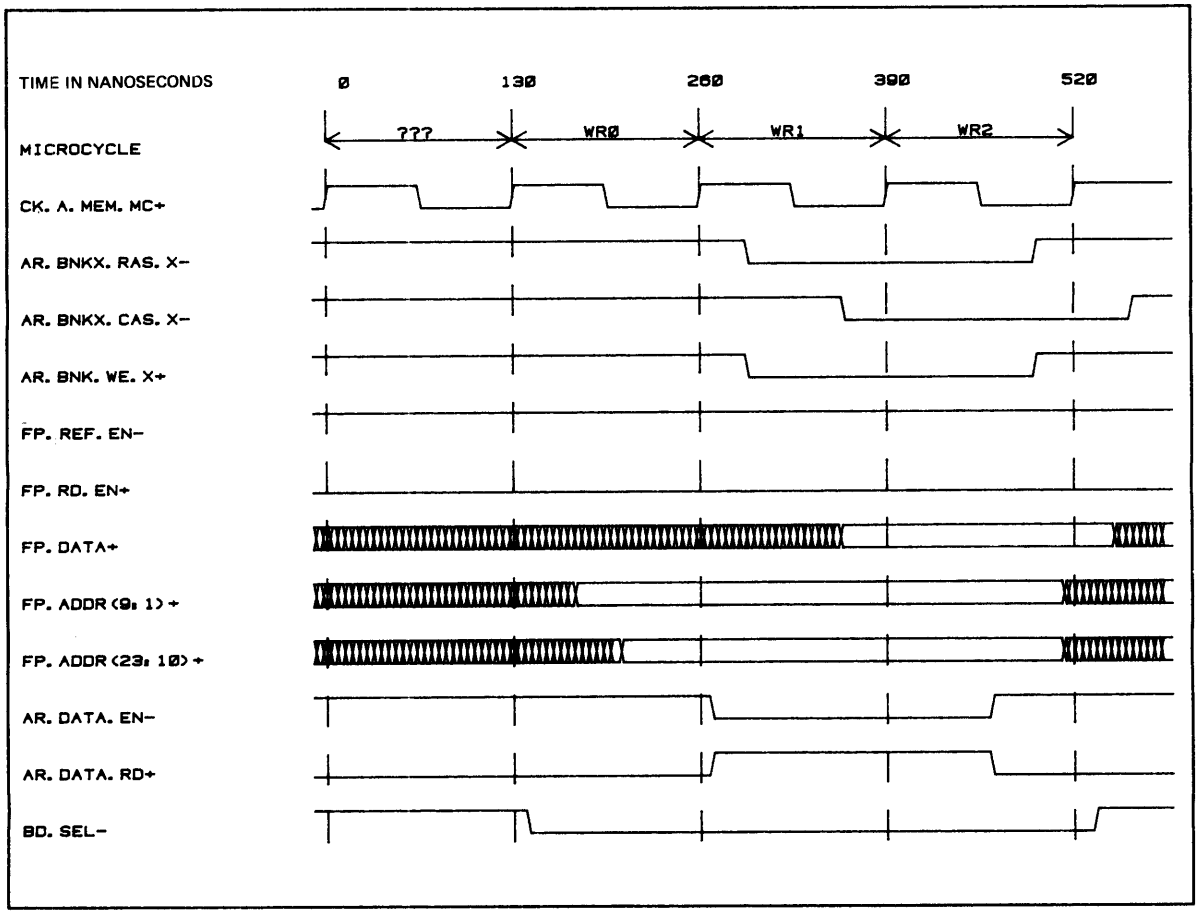


Figure 7-6. Signals For Memory Write

7.3.4 Initialization

Each AR card, when installed, must have a unique address space so that the system can access it. The AR cards are automatically configured by the MC in an ascending address order. Thus if two cards are interchanged, they are automatically reconfigured to form the ascending address sequence. The advantage of this scheme is that identical memory modules become unique in the address space of the computer without the aid of a manually selected switch, jumper settings, or dedicated backplane locations. The only restriction is that the AR cards containing 256k-bit RAMs should be closest to the MC.

7.3.4.1 Bank Select RAM (BSR)

The AR card has a BSR which is initialized to a certain portion of memory space by the MC card. The MC uses a counter to increment through all the bank addresses. When an AR card's addresses are passed by the MC, it signals the next AR card with a chained signal. The BSR is a 1k by 4 static RAM, but only 128 lower locations are used.

The AR card receives FP.MEM.ADDR+ (bits 23 - 17) signals as the address of the BSR, which then decodes them into bank select lines. Each AR card contains three physical banks. The bits are used as follows:

Least significant bit (LSB)	Not Used
Bit 1	Select signal of bank1
Bit 2	Select signal of bank2
Bit 3	Select signal of bank3

Figure 7-7 represents the contents of a BSR for the first 16 locations of a 64k RAM card. For example the 12th word in the BSR corresponds to the 3rd bank in the 4th AR card with the first AR card next to the MC. The locations corresponding to the banks not physically located on the card contain all ones.

MEM ADDR	23	22	21	20	19	18	17	BSR DATA			
BSR ADDR	A6	A5	A4	A3	A2	A1	A0	B3	B2	B1	B0
	0	0	0	0	0	0	0	1	1	1	X
	0	0	0	0	0	0	1	1	1	1	X
	0	0	0	0	0	1	0	1	1	1	X
	0	0	0	0	0	1	1	1	1	1	X
	0	0	0	0	1	0	0	1	1	1	X
	0	0	0	0	1	0	1	1	1	1	X
	0	0	0	0	1	1	0	1	1	1	X
	0	0	0	0	1	1	1	1	1	1	X
	0	0	0	1	0	0	0	1	1	1	X
	0	0	0	1	0	0	1	1	1	0	X
	0	0	0	1	0	1	0	1	0	1	X
	0	0	0	1	0	1	1	0	1	1	X
	0	0	0	1	1	0	0	1	1	1	X
	0	0	0	1	1	0	1	1	1	1	X
	0	0	0	1	1	1	0	1	1	1	X
	0	0	0	1	1	1	1	1	1	1	X

Figure 7-7. Contents of First 16 Locations for 64k BSR

The BSR CS- pin is connected to ground therefore the BSR is always enabled. FP.INIT.CLK+ is received by U0801 (AR13D) to generate AR.CLK+. This signal is used for both enabling the upper-half of U0801 (AR13D), which drives AR.BNK1.SEL-, AR.BNK2.SEL- and AR.BNK3.SEL- signals onto the BSR data bits 1, 2, and 3, respectively, and putting the BSR into the write mode.

7.3.4.2 Shift Register

The AR card uses a 4-bit shift register to write into its BSR. The shift register is implemented by flip/flops U0602 (AR23A), U0602 (AR24A), U0702 (AR25A), and U0702 (AR27A). The MC starts the initialization of BSR under microcode control by clearing the shift register. FP.INIT.MODE+ is received by U0801 (AR13D) to generate AR.INIT.MODE+. This signal, when deasserted, clears the shift register in U0602 (AR23A), U0702 (AR26A), and U0802 (AR23B).

The memory controller sends a "high true" pulse on FP.MEM.CH.IN+ to the first bit of the shift register U0602 (AR23A). The "Q" output of this flip-flop is connected to the "D" input of U0602 (AR25A), "Q" output of U0602 is connected to the "D" input of U0702 (AR26A) and "Q" output U0702 is connected to U0702 (AR27A). With the occurrence of AR.CLK1+ clock generated by the MC, the initialization pulse (FP.MEM.CH.IN+) ripples through the shift register. The "Q" output of the first three bits of shift register is written to the BSR at each bank address provided by the MC. Once the initialization pulse reaches bit 4 of the shift register U0702 (AR27A), the chain signal FP.MEM.CHOUT+ goes high causing FP.MEM.CHIN+ on the next AR card to go high. FP.MEM.CHIN+ and FP.MEM.CH.OUT are connected on the frontplane, which is a hard PC plane. The BSR on each AR card should be completely loaded through the shift register, such that addresses corresponding to banks not physically located on the card contain all ones.

7.3.4.3 Clock

To accommodate both 64k-bit and 256k-bit dynamic RAMs, the shift register must be clocked at two different frequencies where the 256k-bit RAMs must be clocked four times slower than the initialization clock used for the 64k chips. The BSR U0502 (AR12D) addresses are incremented at the same rate for both 64k-bit and 256k-bit RAMs. Figure 7-8 shows the differences between the two cases.

The divide circuitry to generate the slow clock for 256k RAMs is located on schematic AR2. U0802 (AR23B) divides AR.CLK1+ by two to generate AR.CLK2+, which is fed to CLK input pin of U0802 (AR25B) to divide AR.CLK2+ by two to generate AR.CLK4+, which is the desired clock for 256k RAMs. Either jumper J3 or J4 (AR25B) is installed depending on whether 256k or 64k RAMs reside on the card, respectively. To keep the AR cards with different RAMs in sync for initialization, the FP.MEM.CH.OUT+ should be sent to the next AR card at different times depending on the size of dynamic RAMs on the card.

Figure 7-9 and Figure 7-10 show the different initializing clocks for 64k-bit RAM and 256k-bit RAM, respectively, that clock the chain signal flip-flop U0702 (AR27A). In either case the chain signal should be asserted before (120 ns) the address is incremented to the next card's first bank address and should stay on for one clock period (240 ns). The clock for the chain signal, in the case of 256k RAMs, is generated by U1102 (AR27A) and is connected to pin 12 of U0702 (AR27A) by jumper J5 (AR26A). For 64k RAMs jumper J6 (AR27A) connects pin 6 of U0702 (AR26B) to pin 12 of U0702.

	ADDRESS									DATA					
MEM	23	22	21	20	19	18	17	BRD #		64k			256k		
BSR	A6	A5	A4	A3	A2	A1	A0	64k	256k	B3	B2	B1	B3	B2	B1
	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0
	0	0	0	0	0	0	1	1	1	1	0	1	1	1	0
	0	0	0	0	0	1	0	1	1	0	1	1	1	1	0
	0	0	0	0	0	1	1	2	1	1	1	0	1	1	0
	0	0	0	0	1	0	0	2	1	1	0	1	1	1	0
	0	0	0	0	1	0	1	2	1	0	1	1	1	1	0
	0	0	0	0	1	1	0	3	1	1	1	0	1	1	0
	0	0	0	0	1	1	1	3	1	1	0	1	1	1	0
	0	0	0	1	0	0	0	3	1	0	1	1	1	1	0
	0	0	0	1	0	0	1	4	1	1	1	0	1	1	0
	0	0	0	1	0	1	0	4	1	1	0	1	1	1	0
	0	0	0	1	0	1	1	4	1	0	1	1	1	1	0
	0	0	0	1	1	0	0	5	2	1	1	0	1	0	1
	0	0	0	1	1	0	1	5	2	1	0	1	1	0	1
	0	0	0	1	1	1	0	5	2	0	1	1	1	0	1
	0	0	0	1	1	1	1	6	2	1	1	0	1	0	1

Figure 7-8. Shift Register Clocking For 64K and 256k RAMs

7.3.5 Addressing

The 24-bit physical address goes on the frontplane from the memory controller to all the AR cards. Bits 18 - 1 identify a word in 256k RAM banks, and bits 16 - 1 identify a word in 64k RAM banks. The upper address bits (not used for word addressing) select one of banks.

7.3.5.1 RAS and CAS

The RAM elements use two clock signals for array access due to the different address requirements of 64k and 256k RAMs. The RAM packages have insufficient pins to allow direct addressing; therefore, the 16- or 18-bit address is split into two groups of eight or nine, respectively. The low-order address is called ROW address and the upper-order address is called COLUMN address. The procedure for accessing a RAM cell is as follows:

1. Set up ROW address at RAM input
2. Apply RAS clock to RAM
3. Set up COLUMN address at RAM input
4. Apply CAS clock to RAM

FP.RAS+ is buffered by U0801 (AR13E) to produce AR.RAS+, which is ANDed with AR.RAS1.EN+ to generate AR.RAS1- at U0202 (AR111B). AR.BNK1.RAS.A-, the buffered version of AR.RAS1- at U0301 (AR116B), is the strobe signal for the RAMs on schematic AR3. AR.BNK1.RAS.B- is logically identical to AR.BNK1.RAS.A-, and is used to strobe the ROW address to the RAMs on schematic AR4.

The strobe lines for banks two and three are generated in the same manner as bank-1. AR.RAS+ is also the input to the delay line at U1502 (AR112D). This delay line provides AR.CAS+ 80ns later which is ANDed with AR.CAS.EN+ at U0202 (AR114D) to generate the CAS signal, AR.CAS.ALL-. This signal is buffered at U0301 (AR116B) and U0401 (AR116C) to generate AR.BNK1.CAS.A-, AR.BNK1.CAS.B-, AR.BNK2.CAS.A-, AR.BNK2.CAS.B-, AR.BNK3.CAS.A-, and AR.BNK3.CAS.B-. These signals are all logically identical and they are separate signals for loading reasons. AR.CAS.EN+ is asserted at U0402 (AR113C) when the AR card is selected, and the card is not in refresh mode.

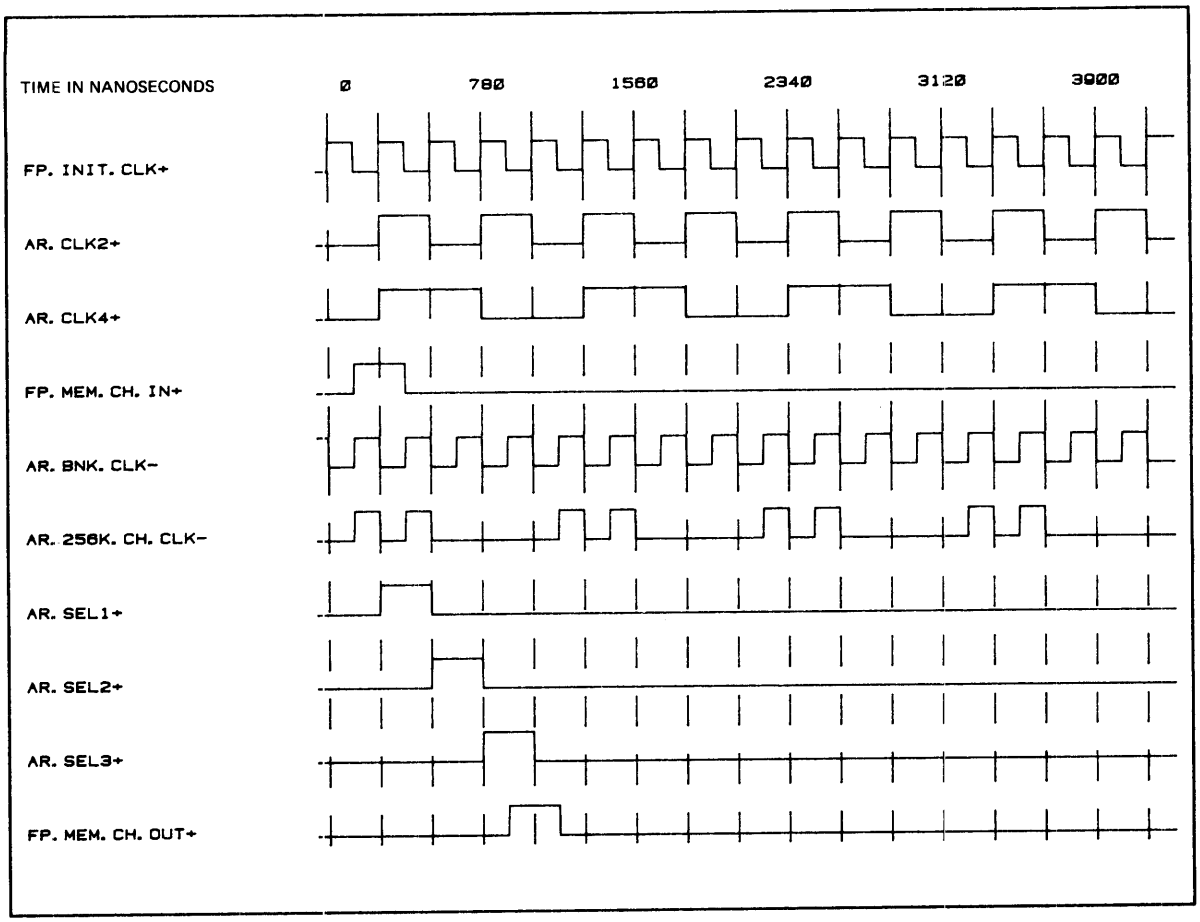


Figure 7-9. Initializing BSR For 64k-Bit RAMs

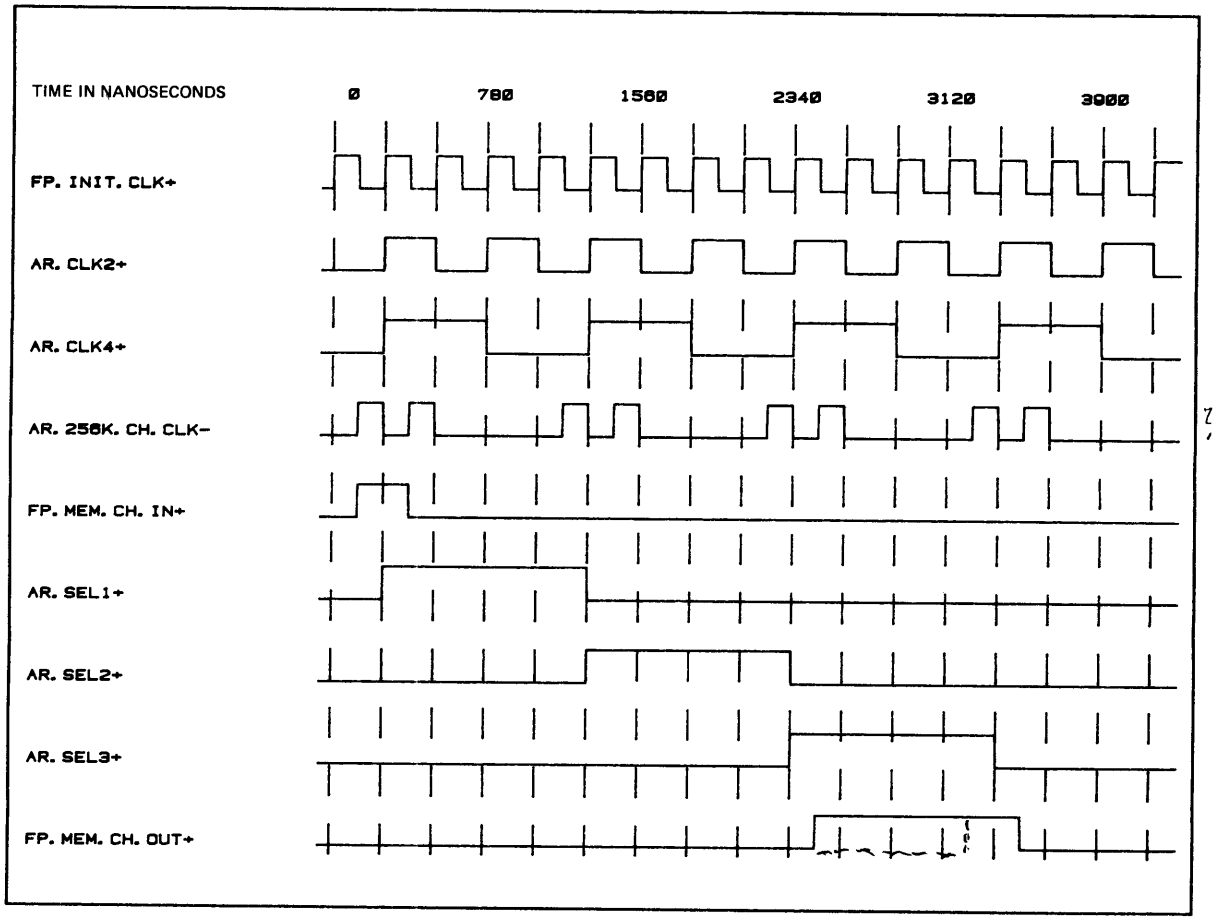


Figure 7-10. Initializing BSR For 256k-Bit RAMs

7.3.5.2 Address MUX

Equally as critical as the timing of the RAS and CAS signals is the timing of the multiplexer switching of the ROW and COLUMN addresses. FP.MEM.ADDR+ (bits 16 - 1) lines are received by four RAM drivers from the frontplane. Figure 7-11 shows the address bits used for ROW and COLUMN addressing. This combination is chosen to ensure all the ROW address bits come directly from MADR on the CA card and do not go through the DMS maps. That allows the ROW address to arrive 45 nanoseconds faster.

RAM ADDR	PIN	64k RAM ROW ADDR	256k RAM ROW ADDR	64k RAM COL ADDR	256k RAM COL ADDR
A8	1	+5V	9	+5V	17
A7	9	8	8	16	16
A6	13	7	7	15	15
A5	10	6	6	14	14
A4	11	5	5	13	13
A3	12	4	4	12	12
A2	6	3	3	11	11
A1	7	2	2	10	10
A0	5	1	1	9	18

Figure 7-11. Address Bits For Row and Column Addressing

Bits 8 - 1 are received by U0601 (AR12A) and U0701 (AR13B) to provide the ROW address. Bits 18, 16 - 9 are received by U0901 (AR12B) and U1001 (AR13B) to provide the COLUMN address for the dynamic RAMs. U1101 (AR12C) provides the proper address bit (bit 9 or 17) to pin 1 (A8) of the 256k dynamic RAMs.

The ROW address buffers are turned off 30 nanoseconds after the occurrence of AR.RAS+ by the delay line U1502 (AR112D), which generates AR.RAS.ADDR.DIS+. This signal is also inverted at U1002 (AR113D), to generate AR.CAS.ADDR.EN-, which enables the COLUMN address buffers. This allows sufficient time for the ROW address hold time, before switching to the COLUMN address.

The two sets of address buses, [AR.ADDR.A.BUS[I:A]+ and AR.ADDR.B.BUS[I:A]+], generated by the five RAM drivers U0601 (AR12A), U0701 (AR13A), U0901 (AR12B), U1001 (AR13B), and U1101 (AR12C)], are logically identical and are separate signals for loading reasons. AR.ADDR.A.BUS+ (I and A) provide the addresses for the RAMs located on schematics AR3, AR4, and AR5, while AR.ADDR.B.BUS+ (I and A) provide the addresses for the RAMs located on schematic AR6, AR7, and AR8.

7.3.5.3 Card Select

An AR card is selected if any of its banks are enabled. AR.BNK1.SEL.BUF- AR.BNK2.SEL.BUF- and AR.BNK3.SEL.BUF- are the enable lines for bank-1, bank-2 and bank-3, respectively. These signals are ORed together in U1202 (AR15D) to produce AR.BD.SEL-. In the deselected mode, the FP.AR.BD.SEL- which is the buffered version of AR.BD.SEL+ U1202 (AR17D) goes high. U1202 is an open collector part. The MC looks at this line to see if a valid memory location has been found.

7.3.6 Data Transceivers

The A-sides of data transceivers U1601 (AR22D), U1501 (AR24D), U1401 (AR25D), U1301 (AR26D) and U1201 (AR27D) are connected to FP.MEM.DATA+ (38 - 0) and B-sides are connected to AR.DATA.BUS+ (Bits 38 - 0). These transceivers are enabled when AR.RD.EN+ is asserted and the AR card is selected and not in refresh mode or the AR card is selected and not in refresh mode but it is in write mode.

Transceiver control is accomplished by U1302 (AR113E). These drivers are only active during a write or read operation . The direction of flow of data is determined by the AR.DATA.IN+, which is the inverted version of AR.WE-, U1002 (AR15E). When AR.DATA.IN+ is high and drivers are enabled data is being written into the RAMs.

7.4 Parts Locations

The parts locations for the array card are shown in Figure 7-12.

7.5 Replaceable Parts List

The replaceable parts for the 768 kb and 3 Mb cards are listed in Tables 7-1 and 7-2. The names and addresses of the manufacturers of the parts are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

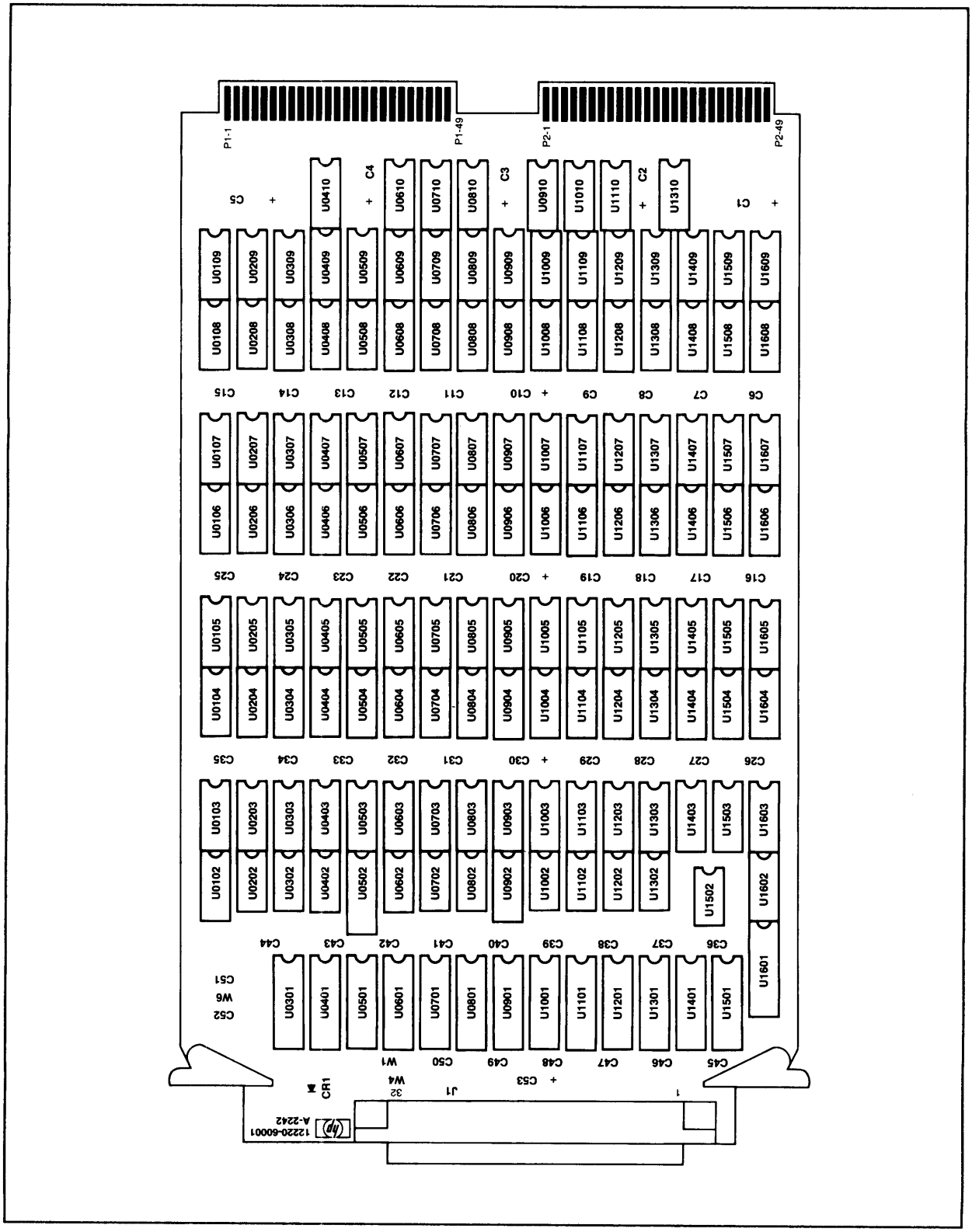


Figure 7-12. Array Card Parts Locations

Table 7-1. 768 Kb Array Card Replaceable Parts (Sheet 1 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12220-60001	4	1	PCA-3/4MB A900	28480	12220-60001
C1	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C4	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C5	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C6	0160-4835	7	37	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C31	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C32	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C33	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C34	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C35	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C36	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C37	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C38	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C39	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C40	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C41	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C42	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C43	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C44	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C52	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C53	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
CR1	1990-0598	1	1	LED-LAMP LUM-INT=800UCD IF=60MA-MAX	28480	5082-4190
U103	5180-0156	4	117	IC-RAM, 64K 75NS	28480	5180-0156
U104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U105	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U106	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U107	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U108	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U109	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U202	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U205	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U206	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U207	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U208	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U209	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U301	1820-2981	1	7	IC MEM-SPRT TTL S OCTL	28480	1820-2981
U302	1820-0693	8	4	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U307	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U401	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981

Table 7-1. 768 Kb Array Card Replaceable Parts (Sheet 2 of 3)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U402	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U407	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U410	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U501	1820-2698	7	1	IC DRVR TTL F LINE DRVR OCTL	07263	74F240PC
U502	1818-3052	4	1	IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U507	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U601	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U602	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U701	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U702	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U703	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U704	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U705	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U706	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U707	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U708	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U709	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U710	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U801	1820-2795	5	1	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U802	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U803	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U804	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U806	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U807	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U808	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U809	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U810	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U901	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U902	1810-0256	8	1	NETWORK-RES 16-DIP1.0K OHM X 15	01121	316A102
U903	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U904	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U905	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U906	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U907	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U908	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U909	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U910	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1001	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U1002	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U1003	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1004	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1005	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1006	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1007	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1008	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1009	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1010	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1101	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U1102	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U1103	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1105	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1106	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1107	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1108	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156

Table 7-1. 768 Kb Array Card Replaceable Parts (Sheet 3 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1109	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1110	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1201	1820-2075	4	5	IC MISC TTL LS	01295	SN74LS245N
U1202	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U1203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1205	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1206	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1207	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1208	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1209	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1301	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U1302	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U1303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1307	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1401	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U1403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1407	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1501	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U1502	1813-0339	4	1	IC DLY-LN HYBRID MULTI-TAP	28480	1813-0339
U1503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1507	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1601	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U1603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1607	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
W1	0811-3587	5	3	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W4	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W6	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587

Table 7-2. 3 Mb Array Card Replaceable Parts (Sheet 1 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12221-60001	5	1	PCA-3MB A900	28480	12221-60001
C1	0180-0229	7	8	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C4	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C6	0160-4835	7	44	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C31	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C32	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C33	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C34	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C35	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C36	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C37	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C38	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C39	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C40	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C41	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C42	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C43	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C44	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C45	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C46	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C47	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C48	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C49	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C50	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C51	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C52	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C53	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
CR1	1990-0598	1	1	LED-LAMP LUM INT=800UCD IF=60MA MAX	28480	5082-4190
U103	5180-4259	6	116	IC RAM 256K, TESTED	28480	5180-4259
U104	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U105	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U106	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U107	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U108	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U109	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U202	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U203	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U204	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U205	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U206	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U207	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U208	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U209	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U301	1820-2981	1	7	IC MEM-SPRT TTL S OCTL	28480	1820-2981
U302	1820-0693	8	4	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U303	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U304	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U305	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259

Table 7-2. 3 Mb Array Card Replaceable Parts (Sheet 2 of 3)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
U306	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U307	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U308	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U309	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U401	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U402	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U403	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U404	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U405	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U406	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U407	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U408	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U409	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U410	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U501	1820-2698	7	1	IC DRVR*TTL F LINE DRVR OCTL	07263	74F240PC
U502	1818-3052	4	1	IC NMOS 4096 (4K) STAT RAM 45 NS 3-S	28480	1818-3052
U503	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U504	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U505	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U506	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U507	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U508	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U509	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U601	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U602	1820-0693	8		IC FF TTL S D-TYPE POS EDGE-TRIG	01295	SN74S74N
U603	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U604	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U605	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U606	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U607	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U608	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U609	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U610	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U701	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U702	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U703	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U704	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U705	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U706	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U707	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U708	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U709	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U710	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U801	1820-2795	5	1	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U802	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U803	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U804	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U805	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U806	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U807	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U808	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U809	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U810	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U901	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U902	1810-0256	8	1	NETWORK*RES 16-DIP1.0K OHM X 15	01121	316A102
U903	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U904	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U905	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U906	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U907	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U908	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U909	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U910	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1001	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U1002	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U1003	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1004	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1005	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1006	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1007	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1008	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1009	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1010	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1101	1820-2981	1		IC MEM-SPRT TTL S OCTL	28480	1820-2981
U1102	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N

Table 7-2. 3 Mb Array Card Replaceable Parts (Sheet 3 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1103	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1104	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1105	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1106	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1107	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1108	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1109	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1110	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1201	1820-2075	4	5	IC TRANSCEIVER TTL LS BUS OCTL	28480	1820-2075
U1202	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U1203	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1204	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1205	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1206	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1207	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1208	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1209	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1301	1820-2075	4		IC TRANSCEIVER TTL LS BUS OCTL	28480	1820-2075
U1302	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U1303	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1304	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1305	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1306	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1307	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1308	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1309	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1401	1820-2075	4		IC TRANSCEIVER TTL LS BUS OCTL	28480	1820-2075
U1403	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1404	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1405	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1406	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1407	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1408	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1409	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1501	1820-2075	4		IC TRANSCEIVER TTL LS BUS OCTL	28480	1820-2075
U1502	1813-0339	4	1	IC DLY-LN HYBRID MULTI-TAP	28480	1813-0339
U1503	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1504	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1505	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1506	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1507	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1508	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1509	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1601	1820-2075	4		IC TRANSCEIVER TTL LS BUS OCTL	28480	1820-2075
U1603	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1604	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1606	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
U1609	5180-4259	6		IC RAM 256K, TESTED	28480	5180-4259
W2	0811-3587	5	3	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W3	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W5	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587

			D-5955-8642-51
A	AS ISSUED	JSF/VDS	1/31/84
B	U1102 COMPONENT LABEL ADDED	JW/	11/7/84

94B FP.MEM.ADDR+ / 23

9 / AR.ADDR.A.BUS+ → 30E 40E 50E

9 / AR.ADDR.B.BUS+ → 60E 70E 80E

119D AR.RAS.ADDR.DIS+ (84)

119D AR.CAS. ADDR. EN - (86)

+5V 16 1810-0256 U0902 7 (88)

(196) AR.PULLUPA+ 8 U0902 1810-0256 +5V 16

AR.PULLUPB+

-2981 AM2966 U0601 (116) (115) (114) (113) (112) (111) (110) (101) H (20) G (19) F (18) E (17) D (16) C (15) B (14) A (13)

-2981 AM2966 U0701 H G F E D C B A

-2981 AM2966 U0901 (108) (107) (106) (105) (104) (103) (102) H G F E D C B A I (21)

-2981 AM2966 U1001 H (11) G (10) F (9) E (8) D (7) C (6) B (5) A (4) I (12)

-2981 AM2966 U1101 (93) (109) (98) AR.RAM.ADDR1+ M1 M2

1818-3052 2149H-2 U0502 (92) (109) (133) (134) (135) (136) (137) A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 I/O0 I/O1 I/O2 I/O3 CS WE

AR.BNK1.SEL.BUF- (94)
AR.BNK2.SEL.BUF- (95)
AR.BNK3.SEL.BUF- (97)

-2795 74F244 U0801

-2898 74F240 U0501

-0685 74S10 U1102

-0683 74S04 U1002

-1451 74S38 U1202

-1322 74S02 U0402

93D (132) FP.INIT.MODE+
29A (185) AR.BNK1.SEL-
29A (186) AR.BNK2.SEL-
29A (118) AR.BNK3.SEL-
93D (131) FP.INIT.CLK+
93D (179) FP.RAS+
93D (181) FP.REF.EN-
93D (182) FP.WE-

(184) AR.BD.SEL- → 110C
(85) AR.BD.SEL+ → 20C 110E
(100) FP.AR.BD.SEL- → 95D
(125) AR.RAS1.EN+ → 110B
(127) AR.RAS2.EN+ → 110B
(130) AR.RAS3.EN+ → 110C
(39) AR.CLK1+ → 20B 110E
(89) AR.WE- → 110A
(41) AR.INIT.MODE+ → 20A
(91) AR.RAS+ → 110D
(99) AR.REF.EN+ → 110C
(40) AR.DATA.IN+ → 20E 110E

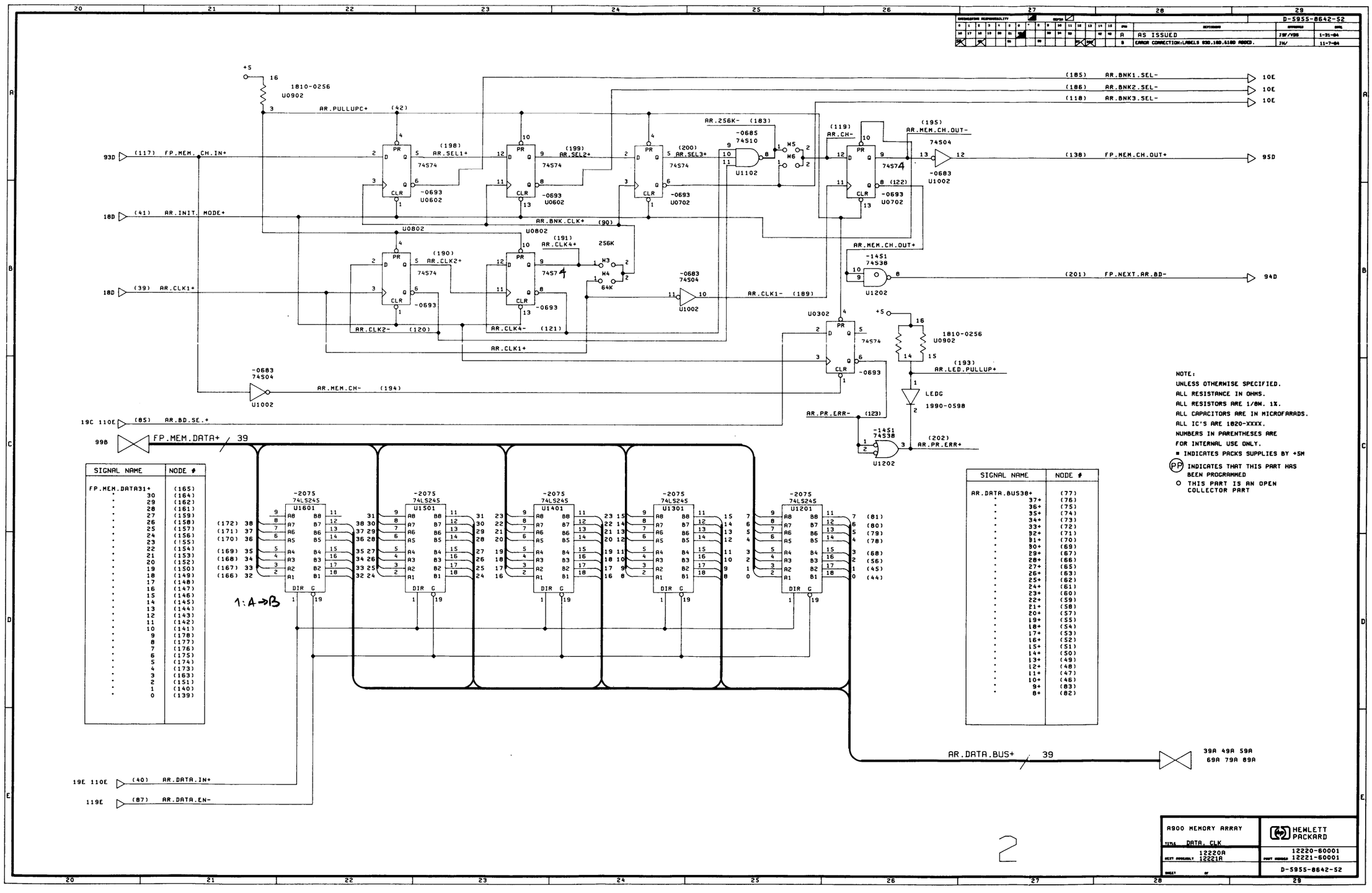
(197) AR.REF.EN-

JUMPER POSITION TABLE			
JUMPR #	64 RAM BOARD	256K RAM BOARD	JUMPR LOCATION
	12220-60001	12221-60001	
W1	IN	OUT	NEAR U0601
W2	OUT	IN	NEAR U1201
W3	OUT	IN	NEAR U0801
W4	IN	OUT	NEAR U0704
W5	OUT	IN	NEAR U0401
W6	IN	OUT	NEAR U0301

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
○ THIS PART IS AN OPEN COLLECTOR PART

A900 MEMORY ARRAY TITLE ADDR. CONTROL	HEWLETT PACKARD
NEXT ASSEMBLY 12220A 12221A	12220-60001 PART NUMBER 12221-60001
SHEET OF	D-5955-8642-51

1



SIGNAL NAME	NODE #
FP.MEM.DATA31+	(165)
" 30	(164)
" 29	(162)
" 28	(161)
" 27	(159)
" 26	(158)
" 25	(157)
" 24	(156)
" 23	(155)
" 22	(154)
" 21	(153)
" 20	(152)
" 19	(150)
" 18	(149)
" 17	(148)
" 16	(147)
" 15	(146)
" 14	(145)
" 13	(144)
" 12	(143)
" 11	(142)
" 10	(141)
" 9	(178)
" 8	(177)
" 7	(176)
" 6	(175)
" 5	(174)
" 4	(173)
" 3	(163)
" 2	(151)
" 1	(140)
" 0	(139)

SIGNAL NAME	NODE #
AR.DATA.BUS30+	(77)
" 37+	(76)
" 36+	(75)
" 35+	(74)
" 34+	(73)
" 33+	(72)
" 32+	(71)
" 31+	(70)
" 30+	(69)
" 29+	(67)
" 28+	(66)
" 27+	(65)
" 26+	(63)
" 25+	(62)
" 24+	(61)
" 23+	(60)
" 22+	(59)
" 21+	(58)
" 20+	(57)
" 19+	(55)
" 18+	(54)
" 17+	(53)
" 16+	(52)
" 15+	(51)
" 14+	(50)
" 13+	(49)
" 12+	(48)
" 11+	(47)
" 10+	(46)
" 9+	(83)
" 8+	(82)

REVISIONS			
ZONE	REVISION	APPROVED	DATE
A	AS ISSUED	[illegible]	1-31-82

AR.DATA.BUS+ / 20 — 49A 59A 69A 79A 89A 29E

U0108 (44) · U0208 (45) · U0308 (56) · U0408 (88) · U0508 (78) · U0608 (79) · U0708 (80)

U0808 (81) · U0908 (82) · U1008 (83) · U1108 (46) · U1208 (47) · U1308 (48) · U1408 (49)

U1508 (50) · U1608 (51) · U0109 (52) · U0209 (53) · U0309 (54) · U0409 (55)

119A 40C — AR.BNK.WE.A- (20)

119B — AR.BNK1.RAS.A- (23)

119B — AR.BNK1.CAS.A- (22)

19A 40E 50E — AR.ADDR.A.BUS+ / 9

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
** THIS PART POWERED BY +5M
THIS PART IS 5180-0156 ON THE 12220-60001 ASSEMBLY AND 1818-3310 ON THE 12221-60001 ASSEMBLY.

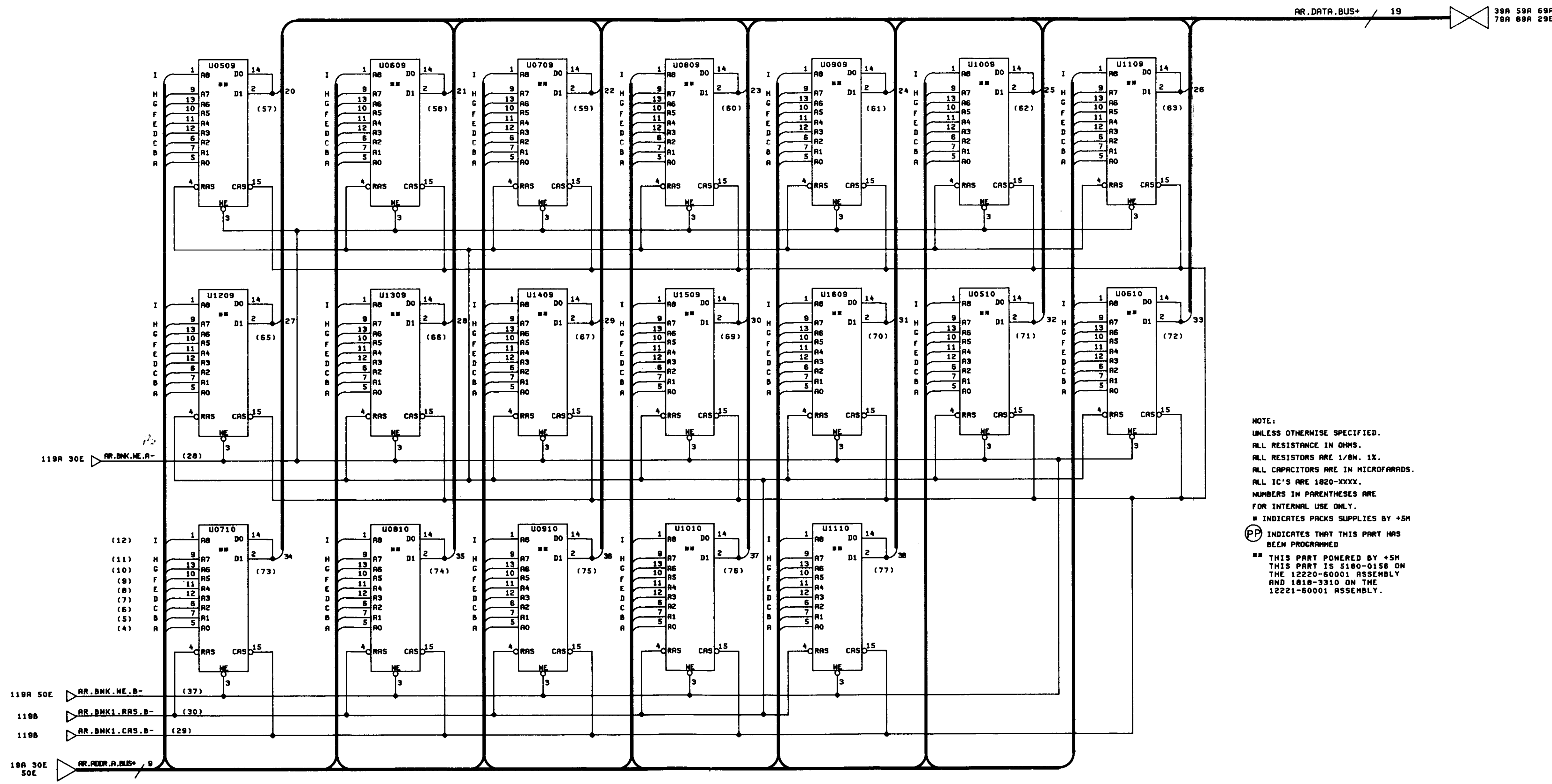
3

D-12220-60001-53 11-10-81	A900 MEMORY ARRAY TITLE RAM. ARRAY	HEWLETT PACKARD
	NEXT ASSEMBLY 12220A 12221A	PART NUMBER 12220-60001 12221-60001
	SHEET OF	D-5955-8642-53

40 41 42 43 44 45 46 47 48 49

D-5955-8642-54

REV	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	1-31-84



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED
** THIS PART POWERED BY +5M
THIS PART IS 5180-0156 ON
THE 12220-60001 ASSEMBLY
AND 1818-3310 ON THE
12221-60001 ASSEMBLY.

4

TITLE	A900 MEMORY ARRAY RAM. ARRAY	HEWLETT PACKARD
NEXT ASSEMBLY	12220A 12221A	PART NUMBER 12220-60001 12221-60001
SHEET OF		D-5955-8642-54

40 41 42 43 44 45 46 47 48 49

ZONE	REVISIONS	APPROVED	DATE
A	AS ISSUED	JDS	1-31-84

AR.DATA.BUS+ / 20 — 39A 49A 69A 79A 89A 29E

U0107 (44) · U0207 (45) · U0307 (56) · U0407 (68) · U0507 (78) · U0607 (79) · U0707 (80)

U0807 (81) · U0907 (82) · U1007 (83) · U1107 (46) · U1207 (47) · U1307 (48) · U1407 (49)

U1507 (50) · U1607 (51) · U0106 (52) · U0206 (53) · U0306 (54) · U0406 (55)

119A 40E AR.BNK.WE.B- (37)

119C AR.BNK2.RAS.A- (25)

119C AR.BNK2.CAS.A- (24)

19A 30E 40E AR.ADDR.A.BUS+ / 9

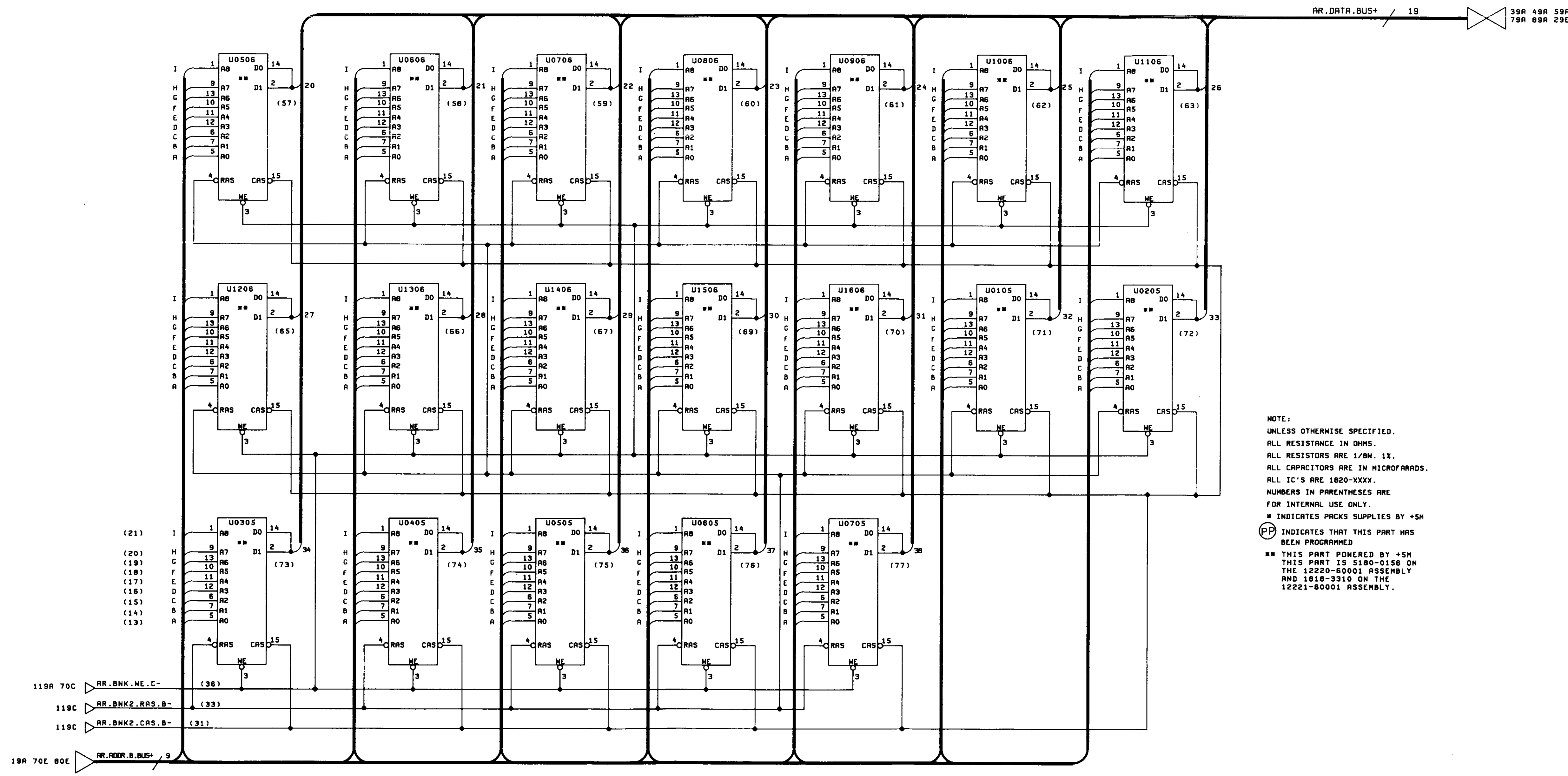
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5V
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
** THIS PART POWERED BY +5V
THIS PART IS 5180-0156 ON
THE 12220-60001 ASSEMBLY
AND 1818-3310 ON THE
12221-60001 ASSEMBLY.

5

	A900 MEMORY ARRAY TITLE RAM. ARRAY	HEWLETT PACKARD
	NEXT ASSEMBLY 12220A 12221A	PART NUMBER 12220-60001 12221-60001
	SHEET OF	D-5955-8642-55

REV	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	1-31-84

D-5955-8642-56



NOTE:

UNLESS OTHERWISE SPECIFIED.

ALL RESISTANCE IN OHMS.

ALL RESISTORS ARE 1/8W. 1%.

ALL CAPACITORS ARE IN MICROFARADS.

ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.

* INDICATES PACKS SUPPLIES BY +5M

(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

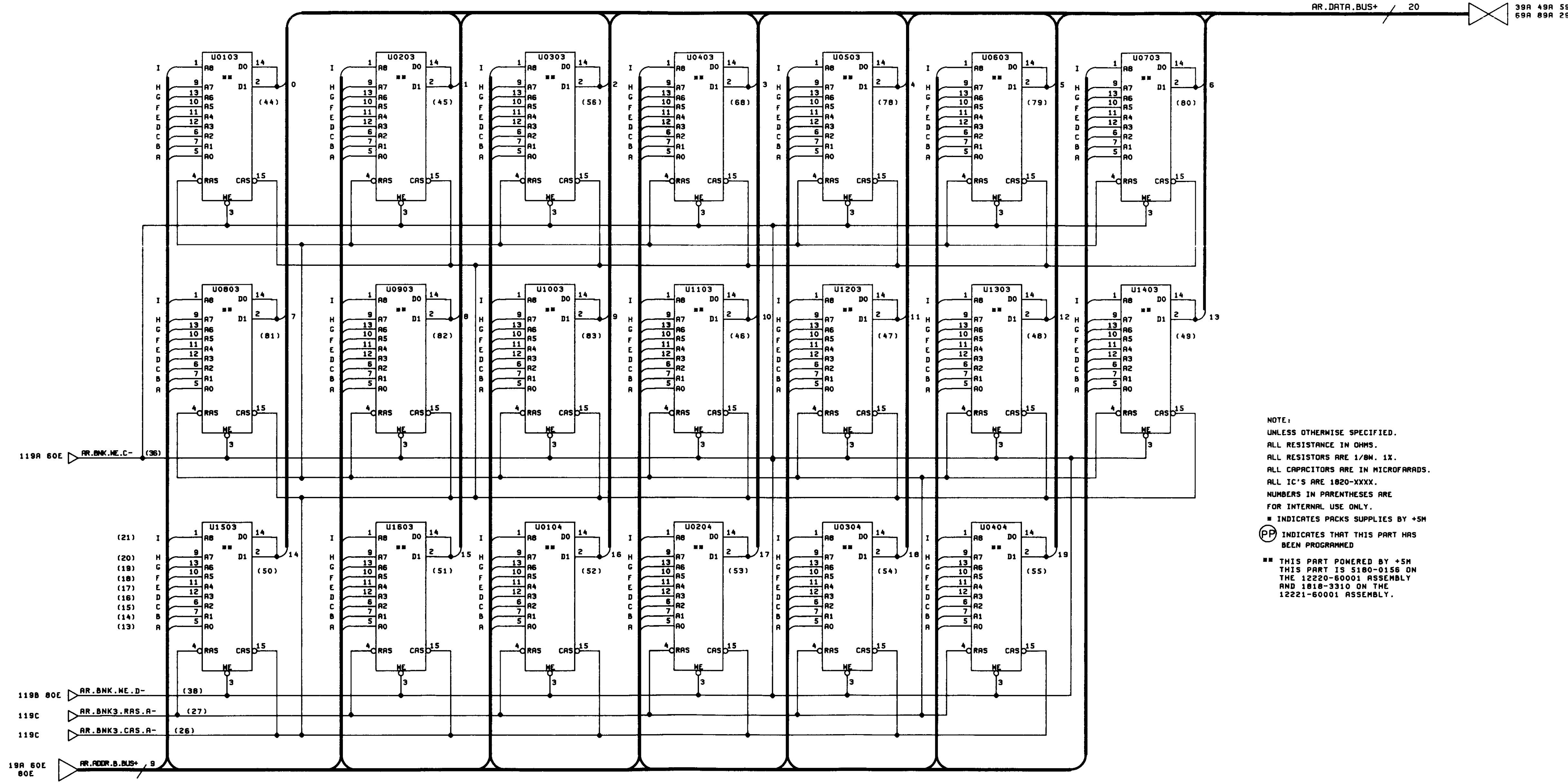
** THIS PART POWERED BY +5M THIS PART IS 5180-0156 ON THE 12220-60001 ASSEMBLY AND 1818-3310 ON THE 12221-60001 ASSEMBLY.

6

TITLE: A900 MEMORY ARRAY RAM. ARRAY	HEWLETT PACKARD
NEXT ASSEMBLY: 12220A 12221A	PART NUMBER: 12220-60001 12221-60001
SHEET OF	D-5955-8642-56

D-5955-8642-57

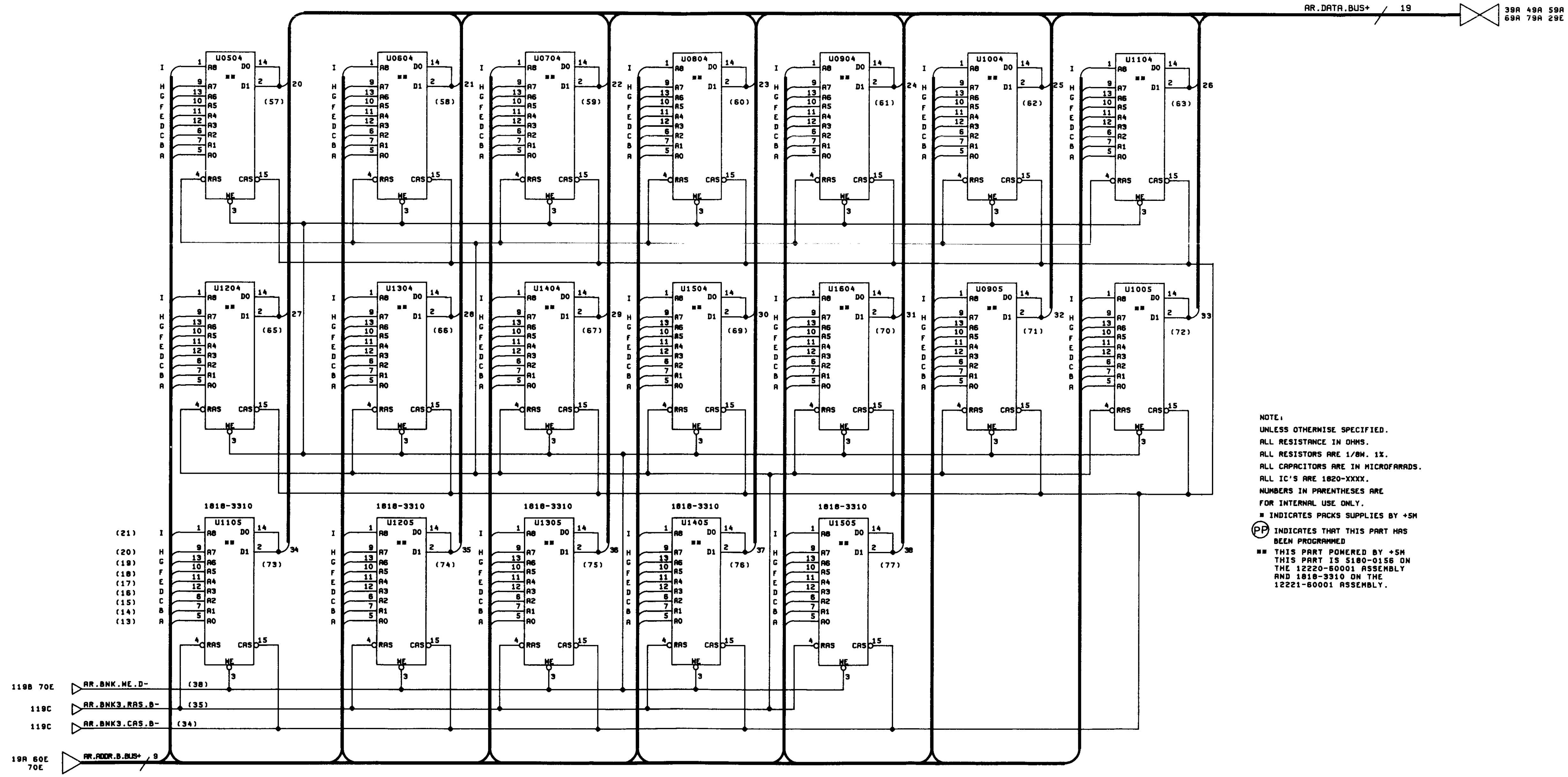
LTR	REVISIONS	APPROVED	DATE
A	AS ISSUED		1-31-84



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
** THIS PART POWERED BY +5M
THIS PART IS 5180-0156 ON
THE 12220-60001 ASSEMBLY
AND 1818-3310 ON THE
12221-60001 ASSEMBLY.

7

A900 MEMORY ARRAY	HEWLETT PACKARD
TITLE RAM. ARRAY	
NEXT ASSEMBLY 12220A 12221A	PART NUMBER 12220-60001 12221-60001
SHEET OF	D-5955-8642-57



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
** THIS PART POWERED BY +5M
THIS PART IS 5180-0156 ON THE 12220-60001 ASSEMBLY AND 1818-3310 ON THE 12221-60001 ASSEMBLY.

D-5955-8642-58

A AS ISSUED 1-31-84

A900 MEMORY ARRAY
TITLE RAM. ARRAY
NEXT ASSEMBLY 12220A 12221A
PART NUMBER 12220-60001 12221-60001
HEWLETT PACKARD
SUPERSEDES DWG. D-12220-60001-58 11-10-81
D-5955-8642-58

8

			D-5955-8642-59
A	AS ISSUED	WFW	1-31-84

FP.MEM.ADDR23+

FP.MEM.ADDR1+

FP.MEM.ADDR+ IN → 10A

OUT
mc 336 Network + buffers

J2-21A	(137)	23	
J2-21B	(136)	22	
J2-21C	(135)	21	
J2-22A	(134)	20	
J2-22C	(133)	19	
J2-23A	(109)	18	
J2-23B	(92)	17	
J2-23C	(108)	16	
J2-24B	(107)	15	
J2-24C	(106)	14	
J2-25A	(105)	13	
J2-25B	(104)	12	
J2-26A	(103)	11	
J2-26B	(102)	10	
J2-26C	(93)	9	
J2-27A	(116)	8	
J2-27C	(115)	7	
J2-28A	(114)	6	
J2-28B	(113)	5	
J2-28C	(112)	4	
J2-29B	(111)	3	
J2-29C	(110)	2	
J2-30A	(101)	1	

FP.MEM.DATA38+

FP.MEM.DATA+ → 20C

J2-01B	(172)	38
J2-01C	(171)	37
J2-02A	(170)	36
J2-02C	(169)	35
J2-03A	(168)	34
J2-03B	(167)	33
J2-03C	(166)	32
J2-04B	(165)	31
J2-04C	(164)	30
J2-05A	(162)	29
J2-05B	(161)	28
J2-06A	(159)	27
J2-06B	(158)	26
J2-06C	(157)	25
J2-07A	(156)	24
J2-07C	(155)	23
J2-08A	(154)	22
J2-08B	(153)	21
J2-08C	(152)	20
J2-09B	(150)	19
J2-09C	(149)	18
J2-10A	(148)	17
J2-10B	(147)	16
J2-11A	(146)	15
J2-11B	(145)	14
J2-11C	(144)	13
J2-12A	(143)	12
J2-12C	(142)	11
J2-13A	(141)	10
J2-13B	(178)	9
J2-13C	(177)	8
J2-14B	(176)	7
J2-14C	(175)	6
J2-15A	(174)	5
J2-15B	(173)	4
J2-16A	(163)	3
J2-16B	(151)	2
J2-16C	(140)	1
J2-17A	(139)	0

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

mc 68C	OUT	J2-30B	FP.NEXT.AR.BD- (201) 29B
	IN	J2-17C	FP.REF.EN- (181) 10E
	IN	J2-18A	FP.RD.EN+ (180) 11OE
	IN	J2-18C	FP.RAS+ (179) 10E
	IN	J2-19B	FP.WE- (182) 10E
	IN	J2-20A	FP.INIT.MODE+ (132) 10E
	IN	J2-20B	FP.INIT.CLK+ (131) 10E
mc 13D	IN	J2-32B	FP.MEM.CH.IN+ (117) 20A

29A FP.MEM.CH.OUT+ (138) J2-32C OUT

19D FP.AR.BD.SEL- (100) J2-01A OUT

FP.MEM.DATRO+

AR.BACKPLANE

P1-1	LBP.ICHID	LBP.ICHID	P1-2
P1-3	LBP.MCHID	LBP.MCHOD	P1-4
P2-11	LBP.SCHID	LBP.SCHOD	P2-12

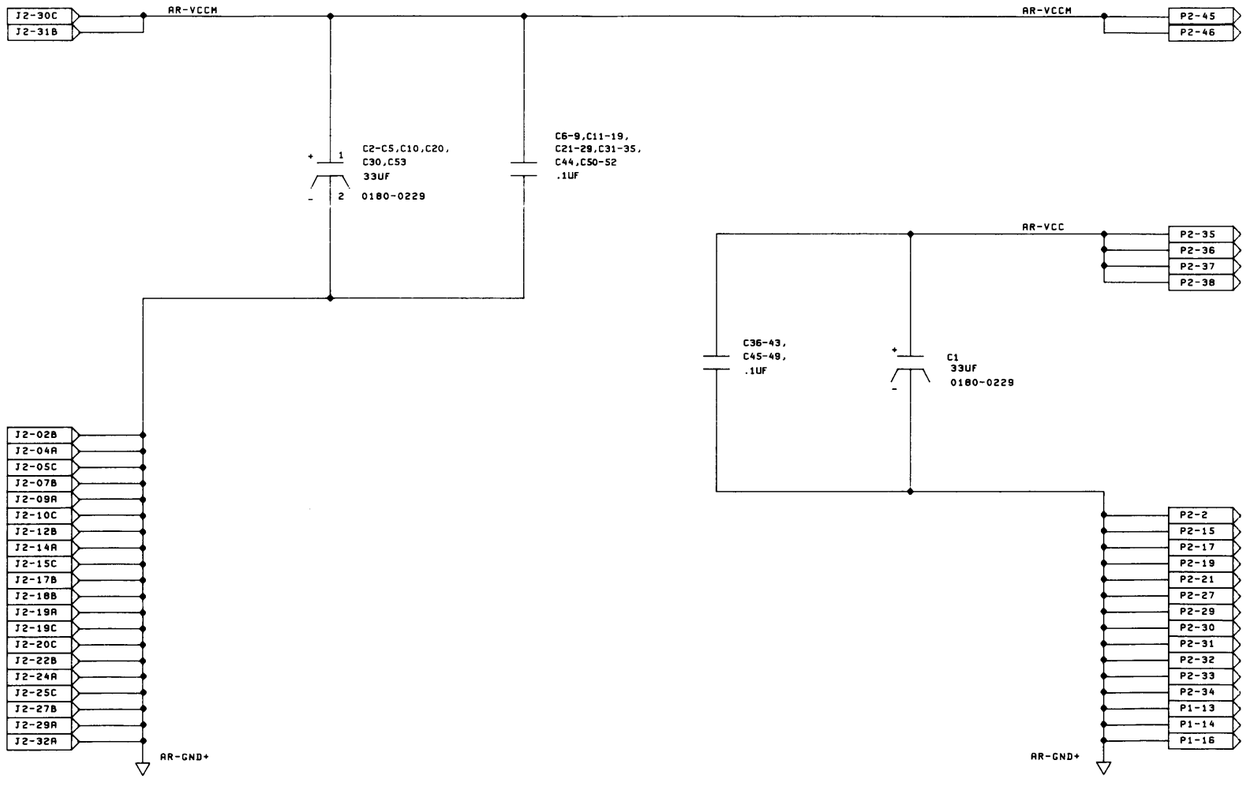
9

	A900 MEMORY ARRAY	HEWLETT PACKARD
	TITLE FP & BP	
	12220A	12220-60001
	NEXT ASSEMBLY 12221A	PART NUMBER 12221-60001
	SHEET OF	D-5955-8642-59

REVISIONS			D-5955-8642-60
ZONE	REVISIONS	REVISED	DATE
A	AS ISSUED	JSF/VDS	1-31-84
B	ERROR CORRECTED	JW/	11-7-84

FRONTPLANE
POWER AND GROUND
CONNECTIONS

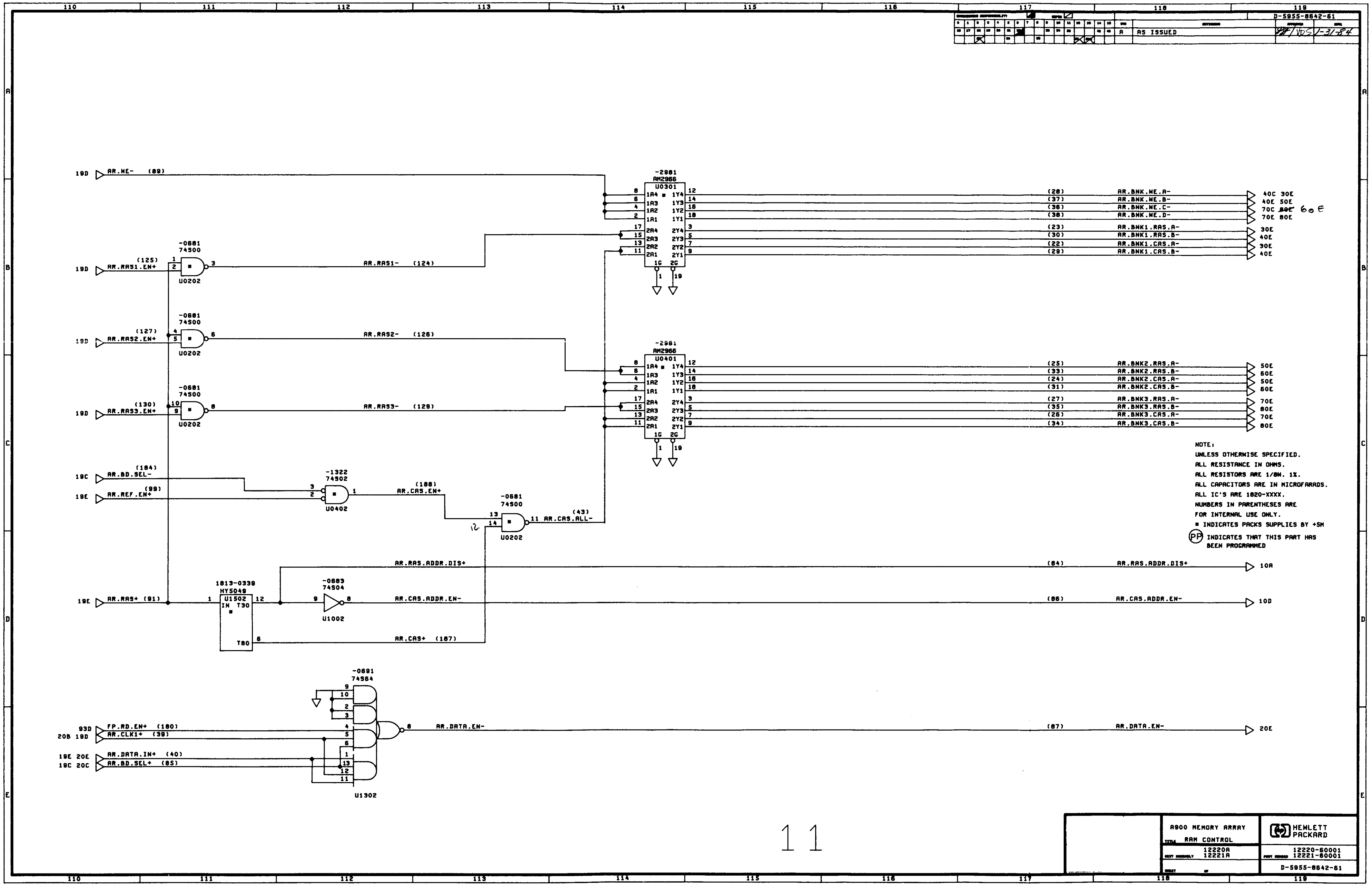
BACKPLANE
POWER AND GROUND
CONNECTIONS



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

10

A900 MEMORY ARRAY TITLE POWER & GND	HEWLETT PACKARD
ASSY PROGRAM 12220A 12221A	PART NUMBER 12220-60001 12221-60001
SHEET OF	D-5955-8642-60


D-5955-8642-61
A AS ISSUED
1-31-84
19D AR.WE- (89)
-2981
AM2966
U0301
19D AR.RAS1.EN+ (125)
-0681
74S00
U0202
AR.RAS1- (124)
19D AR.RAS2.EN+ (127)
AR.RAS2- (126)
19D AR.RAS3.EN+ (130)
AR.RAS3- (129)
U0401
(28) AR.BNK.WE.A- 40C 30E
(37) AR.BNK.WE.B- 40E 50E
(36) AR.BNK.WE.C- 70C 80E 60E
(38) AR.BNK.WE.D- 70E 80E
(23) AR.BNK1.RAS.A- 30E
(30) AR.BNK1.RAS.B- 40E
(22) AR.BNK1.CAS.A- 30E
(29) AR.BNK1.CAS.B- 40E
(25) AR.BNK2.RAS.A- 50E
(33) AR.BNK2.RAS.B- 60E
(24) AR.BNK2.CAS.A- 50E
(31) AR.BNK2.CAS.B- 60E
(27) AR.BNK3.RAS.A- 70E
(35) AR.BNK3.RAS.B- 80E
(26) AR.BNK3.CAS.A- 70E
(34) AR.BNK3.CAS.B- 80E
19C AR.BD.SEL- (184)
19E AR.REF.EN+ (99)
-1322
74S02
U0402
AR.CAS.EN+ (188)
AR.CAS.ALL- (43)
19E AR.RAS+ (91)
1813-0339
HY5049
U1502
IN T30
T80
AR.RAS.ADDR.DIS+
(84) AR.RAS.ADDR.DIS+ 10A
-0683
74S04
U1002
AR.CAS.ADDR.EN-
(86) AR.CAS.ADDR.EN- 10D
AR.CAS+ (187)
-0691
74S64
U1302
93D FP.RD.EN+ (180)
20B 19D AR.CLK1+ (39)
19E 20E AR.DATA.IN+ (40)
19C 20C AR.BD.SEL+ (85)
AR.DATA.EN-
(87) AR.DATA.EN- 20E
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
PP INDICATES THAT THIS PART HAS BEEN PROGRAMMED
11
A900 MEMORY ARRAY
RAM CONTROL
12220A
12221A
HEWLETT PACKARD
12220-60001
12221-60001
D-5955-8642-61

Chapter 8
Control Store

8.1 Introduction

This chapter describes the block diagram and includes the theory of operation of the Control Store (CS) card. To understand fully the operation of this microprogrammed computer, please refer to the HP 92049A RTE Microprogramming Package Reference Manual, part no. 92049-90001.

8.2 Block Description

The control store circuitry is implemented on the CS card. Figure 8-1 is a block diagram of the control store card shown in Figure 8-2.

The card is divided into the following functional blocks:

PROM Control Store Bank
Control Sore Bank Select
Writeable Control Store Bank
Frontplane and Backplane Interfaces

These functional blocks are described in general in the paragraphs under subheading 8.2 and their logical operations (theory of operation) are described in the paragraphs under subheading 8.3.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

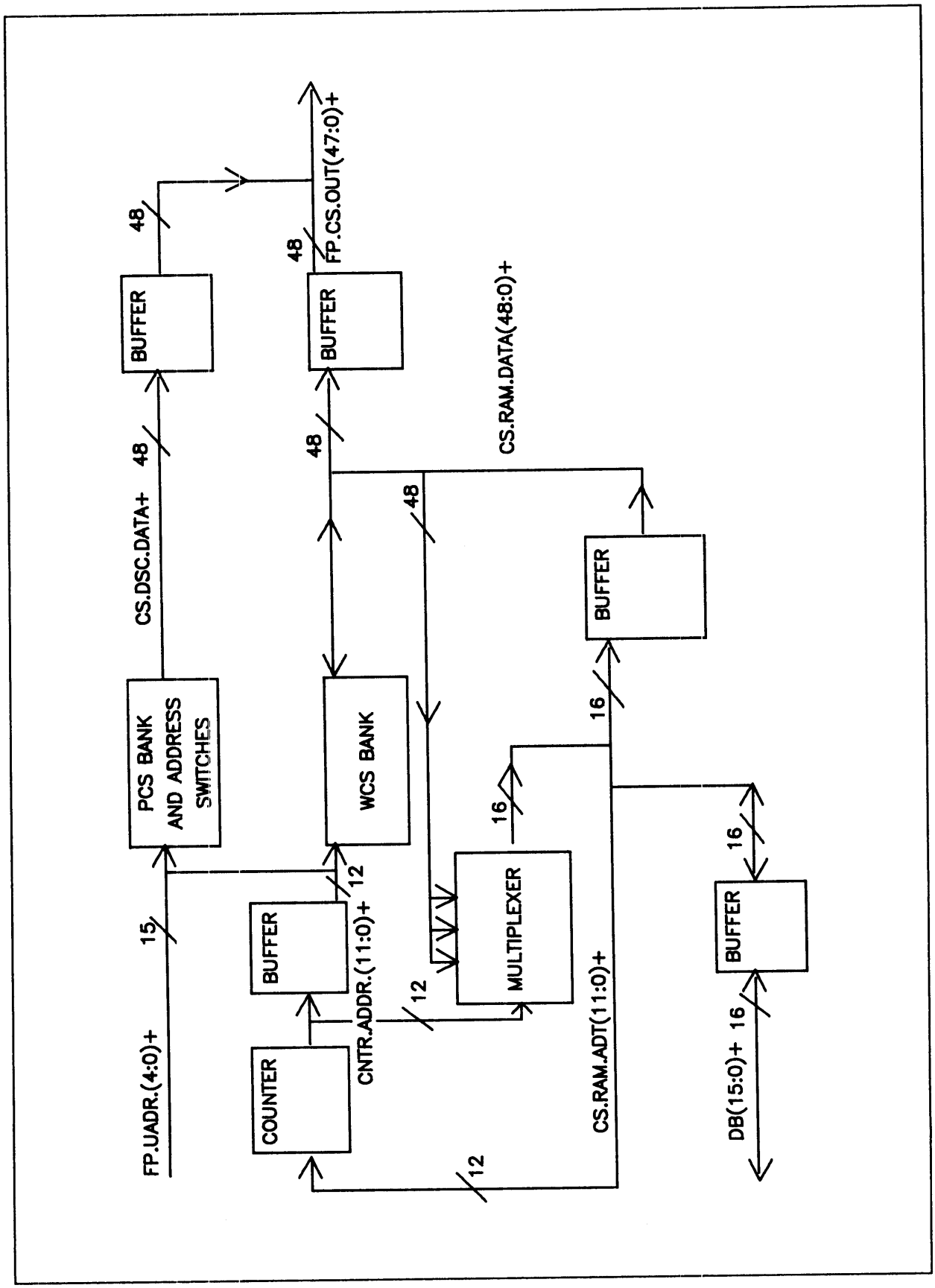


Figure 8-1. Control Store Card Functional Block Diagram

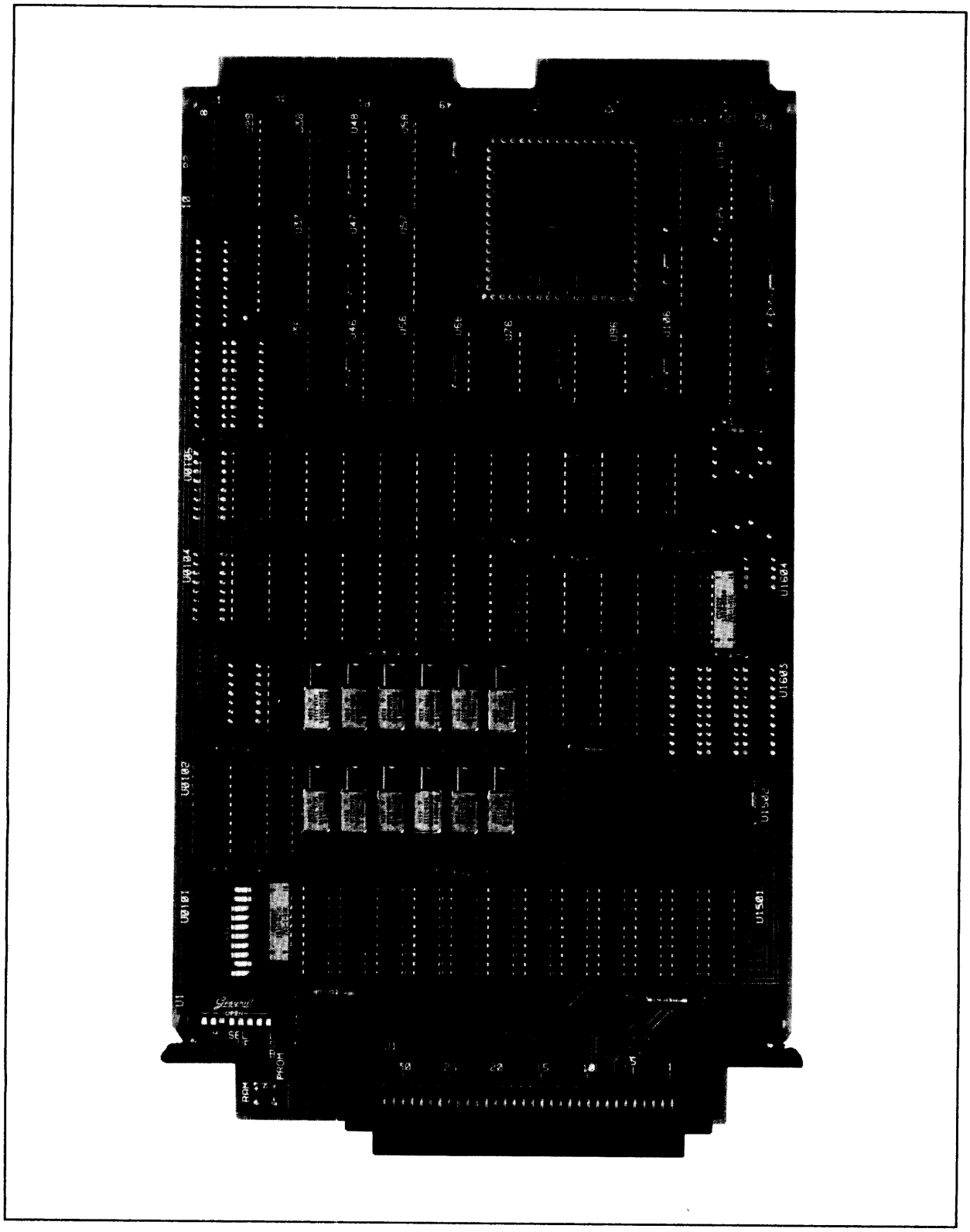


Figure 8-2. Control Store Card (12205-60001)

8.2.1 External Control Store

The CS card extends microprogramming capability to the user. This card will include one bank of PROM Control Store (PCS) and one bank of Writeable Control Store (WCS). The CS PCS bank will provide storage for 2k words of microcode at initial release and as larger PROMs become available the CS PCS can expand up to 8k. The WCS bank will provide storage for 4k words of microcode. The microword in the A900 is 48-bits wide. The CS card resides on the standard card size for the A900 card cage.

As shown, the banks of CS can be addressed by the FP.UADR+ bus through the frontplane. FP.CS.OUT+ is the 48-bit data bus through the frontplane. The WCS bank can also be accessed through the backplane by the I/O master which resides on the CS card. At power up the CS PCS bank is enabled and the WCS bank is disabled.

8.2.2 PROM Control Store

There is one bank of PCS on the CS card which can be addressed by the 15 bits of FP.UADR+ bus. The microaddress space is 32k and the CS PCS bank may be assigned to any 2k block. The CS PCS bank has priority over the main PCS which is located on the SQ card. This allows the base-set microcode to be overwritten by the microcode on the CS PCS bank.

8.2.2.1 CS PCS Bank Select

The CS PCS consists of switches and six sockets to be loaded with PROMs. The CS PCS can be filled with different sizes of PROMs. The card is designed to accommodate 2k by 8 , 4k by 8 or 8k by 8 PROMs. A comparator performs modular selection by comparing control store address bits [14:11] against the address set in the switches associated with the CS PCS bank. If they match, the CS card is enabled, and FP.IJT.EN+ is deasserted then the CS PCS bank's data buffers are enabled and drive the FP.CS.OUT[47:0]+ bus on the frontplane.

8.2.2.2 Frontplane and Backplane Interfaces

On the frontplane the CS PCS bank interfaces to the SQ card. When the SQ card drives an address onto the control store address bus, the CS PCS bank receives the address and if it is selected drives the data onto the frontplane. The CS PCS bank does not use the backplane except for power and ground connections.

8.2.3 Writeable Control Store Bank

There is one bank of WCS on the CS card that can be accessed either through the backplane or frontplane. The WCS bank is part of main control store and is also part of the I/O system. To the processor (frontplane) the WCS bank is indistinguishable from the processor's control store PROMs. To the backplane, the CS card is an I/O card. It allows DMA and programmed I/O, the same as any other I/O card. When WCS is enabled, it acts as main control store, receiving the microaddress from the control store address bus and determining if the address accesses a location on the WCS bank, if so, it disables the CS PCS bank and main control store on the SQ card and drives the microword onto the control store data bus (FP.CS.OUT[47:0]+).

8.2.3.1 Summary of CS I/O Instruction Usage

The WCS bank has a frontplane interface to the SQ card and a backplane interface through the I/O master. The WCS bank is designed such that the backplane protocol and interface requirements are met and the user's interface is entirely through software.

All I/O cards have an eight-position rocker DIP switch near the frontplane of the I/O card. The switches are numbered left to right. S3-S8 should be set to the select code of the card. S3 is the MSB and S8 is the LSB. An up (open) switch represents a logic "1". A down (closed) switch represents a logic "0". With exception of CLC 0 the WCS requires that the Global Register contain the select code of the CS card, and be enabled for the WCS bank to be accessed. The following table lists the I/O instructions executed by WCS.

```
   OT* 30  Writes into RAMs
   LI* 30  Reads RAMs
   OT* 31  Writes address in WCS
   LI* 31  Reads address in WCS (bits 11-0)

To turn WCS bank "ON":
   LD* 60000          Set bits 14 and 13
   OT* 31
   OT* 32

To turns WCS "OFF":
   LD* 0              Clear bits 14 and 13
   OT* 31
   OT* 32

   LI* 31  Reads status of CS (bits 15 and 14)
   STC 30  Handles address increment in programmed I/O
   CLC 30  Clears Flag 30

      * = A/B
```

8.2.3.2 Direct Memory Access (DMA)

The I/O interfacing guide (HP 1000 A/L-Series Computer Interfacing Guide, part no. 02103-90005) describes the control words which specify DMA operation. WCS puts the following restrictions on Control Word 1:

```
Bit 14 - DVCMD - must be set.
Bit 13 - WORD  - must be clear.
Bit 8  - AUTO  - must be clear for input, set for output transfers.
Bit 7  - IN    - must indicate direction of transfers.
```

The remaining bits in Control Word 1 and other Control Words may be set as specified by the I/O Interfacing guide. In four word self-configuration DMA, Control Word 2 is loaded into the address counter on the CS card and should contain the address in WCS of the first word of the data transfer.

8.2.3.3 Backplane Interface

Access to the WCS bank is possible only when CS is "off". On power up the WCS bank is "off" and the CS PCS is "on". The WCS bank must be turned "on" before the SQ card (frontplane) can access WCS.

Turning CS "on":

```
LIA 20000 ---- bit 13 of A should be 1
OTA 31    ---- set bit 13
OTA 32    ---- turn on the CS
```

Turning CS "off":

```
LDA 0     ---- bit 13 of A should be 0
OTA 31    ---- clear bit 13
OTA 32    ---- turn off the CS
```

Turning WCS "on":

```
LDA 60000 ---- bits 14 and 13 of A should be 1
OTA 31    ---- set bits 14 and 13
OTA 32    ---- turn on the WCS
```

Turning WCS "off":

```
LDA 0     ---- bits 14 and 13 of A should be 0
OTA 31    ---- clear bits 14 and 13
OTA 32    ---- turn off the WCS
```

To read status of WCS card:

LIA 31 ---- returns CS status in sign bit of A with "1" meaning "ON", and "0" meaning "OFF".
returns WCS status in bit 14 of A with "1" meaning WCS bank's buffers are enabled, and "0" meaning WCS bank's buffers are disabled.

Addressing the WCS bank:

OTA/B 31 ---- A/B must contain:
WCS bank address in bits [11:0]

Write data to the WCS bank RAMs:

OTA/B 30 ---- A/B contains 1/3 of microword (16 bits)

Read data from WCS bank RAMs:

LIA/B 30 --- 1/3 of microword returned in A/B (16 bits)

8.2.3.4 Examples of I/O Usage

```
LDA SELCD          *Load and enable the Global Register
OTA 2,C            *with select code of the CS card
.
.
LDA X2XXXXB        *Bit 13 should be 1
OTA 31             *Set bit 13
OTA 32B            *Turn CS "on"
.
.
LDA X0XXXXB        *Bit 13 should be 0
OTA 31             *Clear bit 13
OTA 32B            *Turn CS "off"
.
.
LDA X6XXXXB        *Bits 14 and 13 should be 1
OTA 31B            *Set bits 14 and 13 to 1
OTA 32             *Turn WCS "on"
.
.
LDA X0XXXXB        *Bits 14 and 13 should be 0
OTA 31B            *Clear bits 14 and 13
OTA 32             *Turn WCS "off"
.
.
LIA 31B            *Status in bits 15 and 14 of A
.
.
LDA XXXXXNB        *WCS Module address in the
OTA 31B            *lower three bits of A
                   *Set the WCS bank address
```

8.2.3.5 Frontplane Interface

On the frontplane, the WCS bank interfaces only with the SQ card. It appears to the SQ card as a ROM. When WCS is turned "on" and the SQ card puts an address on the FP.UADR[14:0]+ bus, The WCS takes this address and determines if it matches an address located on this bank. If so, it disables the CS PCS bank and the main control store on the SQ card and drives the microword onto the FP.CS.OUT[47:0]+ bus. The WCS bank is assigned to a 4k section of control store before is turned "on". This is accomplished by loading the address of the 4k section into the lower three bits of the address counter through the backplane.

8.3 Theory of Operation

The A900 Computer Control Store card theory of operation is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 8-1 and the schematics at the end of this chapter of the manual. The schematic pages are referred to by a two letter card acronym followed by a page number; e.g., the schematics the control store card are CS1, CS2, etc.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U1204 (CS17C) refers to part U1204 on the CS card in row 12/column 4, which is shown on schematic page CS1 at horizontal location 7 and vertical location C.

The mnemonics used in this engineering reference document relating to microinstructions and microorders are defined in the microprogramming reference manual.

8.3.1 External Control Store

The Control Store (CS) card is designed to become part of the main control store and extends the flexibility of the processor. The same logical address space could exist on the WCS bank and the PCS bank at the same time, with the WCS bank having priority over the CS PCS bank, and with both banks having priority over the main control store on the SQ card. When the CS card is loaded and enabled, it acts as the main control store, receiving the microaddress from the SQ card and determining if the address accesses a location on the card. If the address is on the card a signal is sent to the SQ card to disable the SQ control store.

8.3.2 Turning CS On and Off

The CS card is turned "on" (for access by the SQ card) or "off" (for access by the backplane), as control store. To turn the CS card "on" bit 13 of A/B register should be set to "1" and a OTA/B 31 instruction must be executed. This will set up the CS card for turn-on and the card will actually be "on" when a "OTA/B 32" is executed after the "OTA/B 31" instruction, with bit 13 of the A/B register set.

The logic to turn on the CS card for SQ access consists of U1205 (CS17D). The "D" input of U1205 is connected to CS.RAM.DATA13+ and it is clocked by CS.ADDR.VALID- (the AND of BCS2- and CKDAT- at U1105 (CS41D)). The "Q" output of U1205 connects to the "D" input of U1204 (CS17C). The U1204 flip-flop is clocked with the inverted version of BCS3- signal. Signal BCS3- is generated by an "OTA 32" instruction (BCS3- is preset by the RST- signal going "low" either at power up or by the execution of a "CLC 0" instruction).

Turning "off" the CS card is very similar to turning "on" the CS card, the only difference is that the bit 13 of the A/B register should be set to zero before the "OTA/B 31" instruction, followed by the "OTA/B 32" instruction.

The "Q" output of U1204 (CS17C) is buffered by U1203 (CS18C) to generate FP.CS.ON-, which is received by the SQ card and enables the SQ card to drive FP.UADR[14:0]+ bus. This signal also enables the address comparators for both the WCS and the CS PCS banks at U0101 (CS23B) and U0102 (CS31B). The noninverted version of this signal, CS.BD.ON+, disables the RAM address buffers located on the CS card, at U0302 (CS31C) and U0202 (CS31D), when CS is "on".

The status of the CS card can be read by an LIA 31. Bits 0 through 11 of the A register will contain the address of control store and bit 15 will contain the CS card's ON and OFF bit, bit 14 will contain The WCS bank status.

8.3.3 CS PCS Bank

The PROM Control Store Bank on the CS card is designed to accommodate either 2k by 8, 4k by 8 or 8k by 8 PROMs. This bank can be accessed by the SQ card through the frontplane. The CS PCS bank may be assigned to any 2k block within the 32k address space of control store.

8.3.3.1 CS PCS Bank Select

The comparator U0101 (CS23B) compares the upper bits of FP.UADR+ bus with the CS PCS bank's address, set on the card by switches. If FP.CS.ON- is true and FP.IJT.EN+ is deasserted and the CS PCS bank address matches, FP.XCS2- signal becomes valid and eventually enables the CS PCS bank output buffers. The output buffers of the CS PCS bank will drive the FP.CS.OUT[47:0]+ bus, if the CS PCS bank is selected, WCS is "on" and the WCS bank is not selected. CS.PRM.BUF.EN- is the enable signal for the CS PCS bank buffers U1101, U1001, U1201, U1401, U1501 and U1301 (CS20D-28D). This signal is asserted when FP.XCS2- is true and CS.RBNK.SEL+ is deasserted by U1104 (CS23C). The CS PCS bank can be disabled manually by turning off switch position 9 on U0201 (CS21A).

The PROMs on the CS PCS bank are always enabled to meet the timing constraints. These PROMs are U1102, U1002, U1202 (CS24A-28A), U1302, U1402 and U1502 (CS24B-CS28B). Their address pins are connected to the FP.UADR[14:0]+ bus. Pins 19 and 18 are chip selects for 2k by 8 PROMs. Pin 19 becomes address bit 11 for 4k by 8 PROMs and pin 18 remains as a chip select pin. For 8k by 8 PROMs, pins 19 and 18 become address bits 11 and 12, respectively. Switches 1 and 2 U1401 (CS21A), provide the desired signal to pins 19 and 18 of the PROMs. Switches 3 through 8 are used to set the CS PCS bank address on the card.

8.3.4 WCS Bank

There is one bank of WCS on the CS card that can be accessed either through the backplane or frontplane. The WCS bank must function as control store for the processor and allow backplane access as well as frontplane access. To prevent contention between the two paths, the WCS can be turned "on" for frontplane access and "off" for backplane access. When WCS is "on" it acts as control store for the processor. When addressed, it disables the PCS bank and main control store on the SQ card, and outputs data to the control store data bus. When WCS is "on" all attempted backplane accesses are ignored, except OTA 32. When WCS is "on" the I/O master signals will still be generated but CS.BD.ON+ will prevent any changes to the card except OTA 32. LIA 30 and 31 will appear to read from the card but the data will not be valid.

While WCS is "off", the user has access to WCS through the backplane and any frontplane accesses are ignored. If WCS is "off", it effectively does not exist as control store. Address and data must be multiplexed or otherwise separated between the frontplane and backplane. WCS supports DMA and programmed I/O. The address from the backplane is loaded into a counter which can be incremented.

8.3.4.1 Turning CS ON and OFF

The CS card is turned "on" (for access by the SQ card) or "off" (for access by the backplane), as control store, by "OTA 32" for "on" and "LIA 32" for "off". "OTA 32" generates a BCS3- in the I/O Master. BCS3- is ANDed with RST- by U1404 (CS11C) to generate CS.ON-, which presets the "D" type flip-flop U1204 (CS17D).

The command "LIA 32" generates a BCS7- in the I/O Master. This signal clears the "D" type flip-flop U1204 (CS17D). The "Q" output of this flip-flop is buffered by U1203 (CS18C) to generate FP.CS.ON-, which is received by the SQ card and enables the SQ card to drive FP.UADR[14:0]+ bus. This signal also enables the address comparators for both the WCS and the CS PCS banks at U0101 (CS23B) and U0102 (CS31B). The noninverted version of this signal, CS.BD.ON+, disables the RAM address buffers located on the CS card, at U0302 (CS31C) and U0202 (CS31D), when CS is "on".

The status of the CS card can be read by an "LIA 31" instruction. Bits 0 through 11 of the A-register will contain the address of control store and bit 15 will contain the CS card's "on" and "off" bit, bit 14 will contain The WCS bank status.

8.3.4.2 Backplane Transceivers

The backplane data bus (DB[15:0]) is received by transceiver buffers U0605 (CS12A) and U0705 (CS12C). During the assertion of BCS1- and BCS2-, which are generated by the I/O Master as a result of "OTA 30", and "OTA 31" instructions, respectively. The direction of data is from the backplane toward the card.

During the assertion of BCS5- and BCS6-, as a result of executing LIA 30 and LIA 31 instructions, the direction of data is from the card toward the backplane. This is accomplished by ORing BCS1-, and BCS2- at U1005 (CS11D) to generate CS.RDATA.OUT+. This signal is ORed with CS.RDATA.IN+ (the OR of BCS5- and BCS6- U1304 (CS11C)) by U1305 (CS12D) to generate the enable signal for the transceiver buffers, CS.DB.BUF.EN-.

8.3.4.3 Service Request (SRQ-) Signal

The I/O Master requires an SRQ- signal for each data transfer. In the CS card, SRQ- is the "Q-" output of U1504 (CS42E). This flip-flop is clocked by CS.DVCMD-, which is the AND of DVCMD- and SCLK+ U1105 (CS41E). The "D" input and PRESET of the flip-flop are pulled up and the flip-flop is cleared by SACK-. With this scheme the CS card generates an SRQ- signal each time there is a data transfer.

8.3.4.4 Address Counter

An address is sent to the CS card through the backplane with an "OTA 31" which generates the BCS2- signal in the I/O Master. The address is received by the 12-bit address counter U0204 (CS43B), U0303 (CS43C) and U0304 (CS43D) with the backplane data input to the data pins of the counter. For programmed I/O the address must be loaded for each data transfer or programmatically incremented. For DMA the address must be loaded for the first data transfer and is incremented for each succeeding transfer.

The counter is loaded with CS.LD.AD.CNTR-, which is asserted when CS.BD.ON+ is deasserted and CS.RAM.ON.CLK+ is asserted by U1104 (CS42D). CS.RAM.ON.CLK+ is the AND of BCS2- and CKDAT- at U1105 (CS42D). The address counter is enabled to count when CS.INC.ADD.CNTR- is asserted. Since DVCMD- is asserted on DMA IN start-up, CS.COUNT.EN+ is used to prevent incrementing the counter before the first data transfer occurs. This signal is generated by a flip-flop U1405 (CS52B), which is preset by BCS1- or BCS5- at U1404 (CS52A). The "D" input of the flip-flop is tied "low" and the flip-flop is clocked by LDCW1-.

The LDCW1- signal will clock the flip-flop "low" so that CS.COUNT.EN+ will be "low". Thus, CS.COUNT.EN+ will be "high" after the assertion of BCS1- or BCS5-. CS.BD.ON- is input to the clear of the flip-flop to guarantee power up with CS.COUNT.EN+ "low". CS.COUNT.EN+ is ANDed with CS.DVCMD+ and CS.LW.WRD+ at U1005 (CS54A) to generate the CS.INC.ADD.CNTR-.

Synchronous counting in the address is provided by SCLK+ which is input to the clock inputs of the address counter. The ripple-carry outputs of each 74LS191 are connected to the enable inputs of the upper 74LS191. The address counter will be enabled only when these three conditions are met at U1005 (CS54B):

1. The word counter must have counted to three (CS.LW.WRD+ U1303 CS55C)

2. CS.DVCMD+ is asserted U1203 (CS52B)

3. CS.COUNT.EN+ is asserted U1405 (CS52B)

8.3.4.5 Word Counter

Since the microword is 48-bits wide and the width of the data path through the backplane is 16, for every microword transfer there should be three data transfers through the backplane. U1303 (CS55C) is a counter to keep track of which third of the microword is being transferred. The U1303 counter acts as a shifter when its load/shift pin is high, and loads the values at the input pins when the signal to this pin is "low". The word counter resets to the value of the input pins every time there is an "OTA 30", which generates BCS2-, or when the address counter is being incremented at U1404 (CS55B).

The input pins are hardwired, the A-input pin is connected to +5V through a resistor and the B-, C-, D-input pins are grounded. When CS.WRD.CNTR.RST- is "low", the word counter is loaded with 0001 and when this signal goes "high" the word counter starts to shift left through 0010, 0100 and then it resets to 0001 and starts over again.

The clear pin of the word counter is connected to CS.BD.ON- to clear the counter when CS is "on" (frontplane access). The word counter is clocked by CS.IN.WRD.CNTR-, which is the AND of SCLK+ and CS.WRD.CEN- at U1105 (CS55A). Since the word counter is a synchronous part, it will only be loaded at the positive going edge of its clock (CS.INC.WRD.CNTR-). In order to synchronize the load and the clock signals, it is necessary to OR BCS2- and CS.CNT.EN- at U1404 (CS55B). CS.CNT.EN- is the AND of CS.COUNT.EN+ and CS.DVCMD+ at U1005 (CS54B).

8.3.4.6 WCS Bank RAMs

The size of the WCS bank on the CS card is 4k. The static RAMs are chosen for their "high" density and fast access time. They are located on schematic CS3 as follows: U0702, U0802, U0902, U0703, U0803, U0903, U0602, U0502, U0402, U0603, U0503 and U0403). The address pins of the RAMs are connected to FP.UADR[11:0]+ and the RAMs are always enabled due to timing constraints.

The WCS bank can be assigned to any 4k block within the 32k address space of control store. This is accomplished by loading the address of the desired section of control store to the lower three bits of the address counter U0304 (CS44D), when the WCS is "off". These three bits, CNTR.ADDR[2:0]+, are compared with FP.UADR[14:12]+ to see if the addressed microword is in the WCS bank.

If the addresssed microword is in the WCS bank and CS.RAM.BNK.ON+ is true, then FP.XCS1- at U0102 (CS31B) becomes asserted. CS.RAM.BNK.ON+ is generated by U1205 at CS52D. This signal is asserted by setting bit-14 of the A/B register, and then executing an "OTA 31", which will cause CS.RAM.ADT14+ to be clocked into U1205 at CS52D. FP.XCS1- is buffered by U0202 (CS31D) to generate CS.RBUF.OUT.EN-, which enables the RAMs' output buffers. The RAMs' output buffers drive the FP.CS.OUT[47:0]+ bus: U0601, U0701, U0501, U0801, U0401, and U0901 (CS15).

8.3.4.7 Data RAM Buffers

The 4k by 4 static RAMs (IMS1420) in the WCS bank have common data I/O pins. This requires buffering the input data to prevent contention between input and output data or shorts between the frontplane and backplane. The input buffers are U0604 (CS14A), U0704 (CS14B), U0504 (CS14C), U0804 (CS14D), U0404 (CS14D) and U0904 (CS14E). Their data input pins are connected to CS.RAM.ADT[15:0]+ and their data output pins are connected to CS.RAM.DATA[47:0]+. U0604 and U0704 are enabled by CS.INBUF.LW.EN-, which is the buffered version of CS.WE.LW-. U0504 and U0804 are enabled by CS.INBUF.MD.EN-, which is the buffered version of CS.WE.MD-. U0404 and U0904 are enabled by CS.INBUF.HI.EN-, which is the buffered version of CS.WE.HI- at U0202 (CS31D).

The circuitry for generating the write-enable signals to the RAMs is located on schematic CS5. CS.WR.DATA- indicates valid data on the backplane data bus at U1105 (CS51A) and when WCS is "off", CS.WR.VALID+ becomes asserted at U1305 (CS52A). CS.WR.VALID+ is ANDed individually with the following:

CS.LW.WRD+
CS.MD.WRD+
CS.HI.WRD+

by U1304 (CS58B/C) to generate CS.WE.LW-, CS.WE.MD-, and CS.WE.HI-, respectively. These three signals are the write enable signals to the RAMs.

8.3.4.8 Backplane Output Logic

The user has complete access to the CS card through the backplane. Eight multiplexer chips multiplex the CS address, CS data, or CS status onto the backplane. CS.RAM.DATA[47:0]+ are the inputs to the C0, C1 and C2 pins of the multipexers: U0505 (CS46A), U0405 (CS46B), U0305 (CS46C), U0205 (CS46D), U0905 (CS48A), U1004 (CS48B), U1003 (CS48C), and U0805 (CS48D). C0 pins of the multipexers are connected to CNTR.ADDR[11:0]+, except U1003 and U0805 and CS.RAM.BNK.ON+ is the input to the 1C0 pin of U0805.

CS.BD.ON+ is the input to the 2C0 pin of U1505. The multipexers output is chosen from one of the four inputs by the values of the "A" and "B" select pins of the multipexers. The following table shows the output select for each combination of "A" and "B".

A	B	output
0	1	C0 low RAM Bits
1	0	C1 Mid RAM Bits
1	1	C2 Hi RAM Bits
0	0	Address & Status

CS.MD.WRD+ from U1303 (CS55C) is ORed with CS.BCS6+ in U1103 (CS58C) to generate CS.MUX.SELA+, which is connected to the A-select pin of the multipexers. CS.LW.WRD+ at U1303 (CS55C) is ORed with CS.BCS6+ at U1103 (CS58D) to generate CS.MUX.SELB+, which is connected to B-select pin of the multiplexers. Due to timing requirements of the backplane during DMA input, the multiplexers enable must be decoded and input to the multiplexers before the actual DMA request is made. Bit 7 of control word 1 defines the direction of the DMA transfer, "1" means from CS to backplane, "0" from backplane to CS. DB7+ is connected to the "D" input of U1204 (CS41C), which is clocked by LDCW1- to generate CS.DMA.IN-. The value of the flip-flop is changed only on assertion of LDCW1-.

The multiplexers output must be disabled for DMA out at U1305 (CS42C) or the assertion of BCS1- or BCS2- at U1005 (CS11C). The multiplexers should be enabled for DMA by the assertion of BCS5- or BCS6- at U1304 (CS11C) going to U1305 (CS42C), which generates CS.MUX.EN- signal.

8.3.5 WCS and PCS LEDS

There are two LEDs on the CS card. LED1, labled RAM, at CS54E is "on" if the WCS bank is "on", which means CS.RAM.BNK.ON- and CS.BD.ON- are both asserted "low". This is acomplished by U1104 at CS54E. LED2, labled PROM, at CS54E is "on" if the CS card is "on" and the PCS bank is enabled by bit 9 of the switch U0201 at CS21A. CS.BD.ON- and CS.PCS.SW- are ORed by U1104 at CS54E.

8.4 Parts Locations

The parts locations for the control store are shown in Figure 8-3.

8.5 Replaceable Parts List

The replaceable parts list for the control store are listed in Table 8-1. The names and addresses of the manufacturers of the parts are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

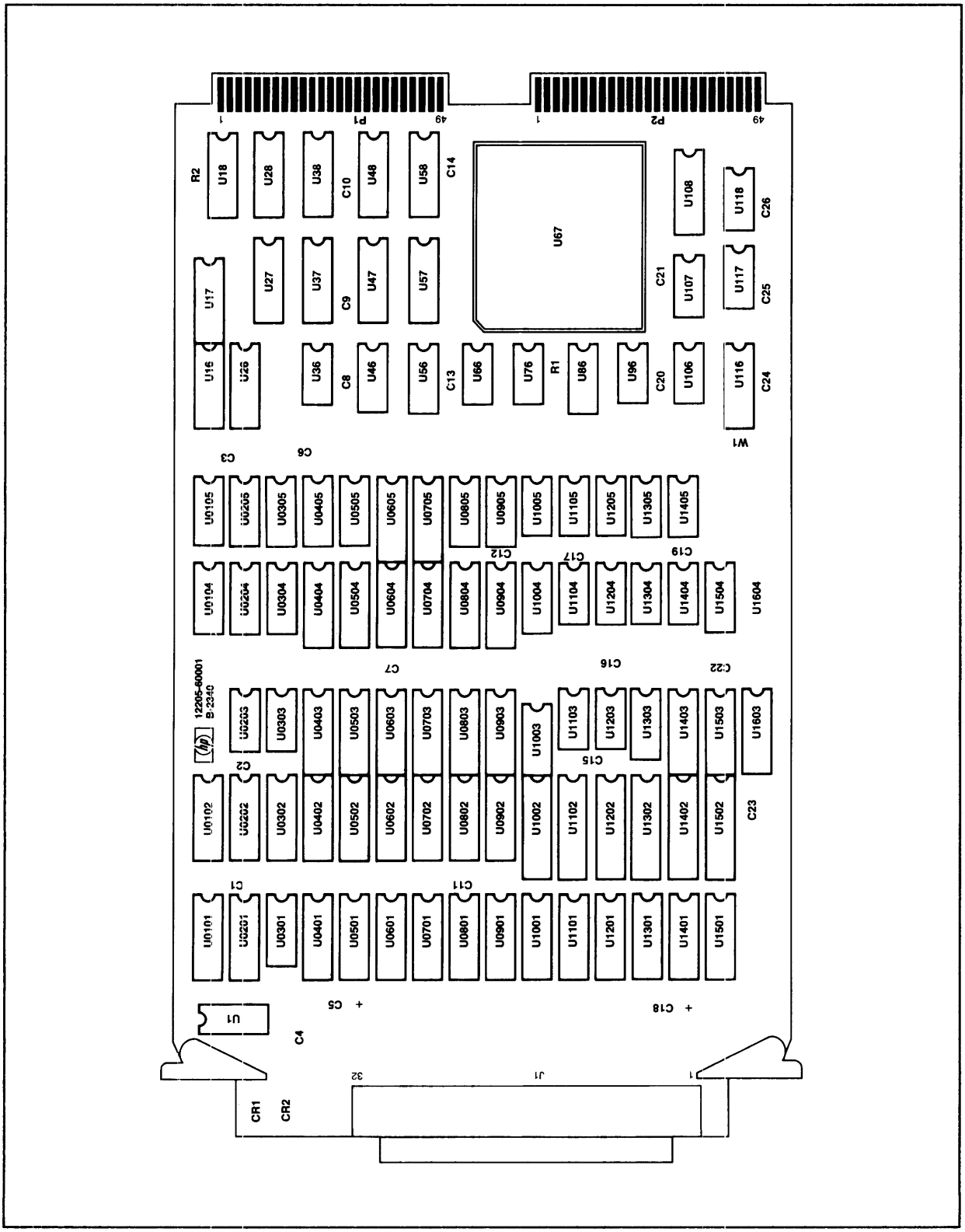


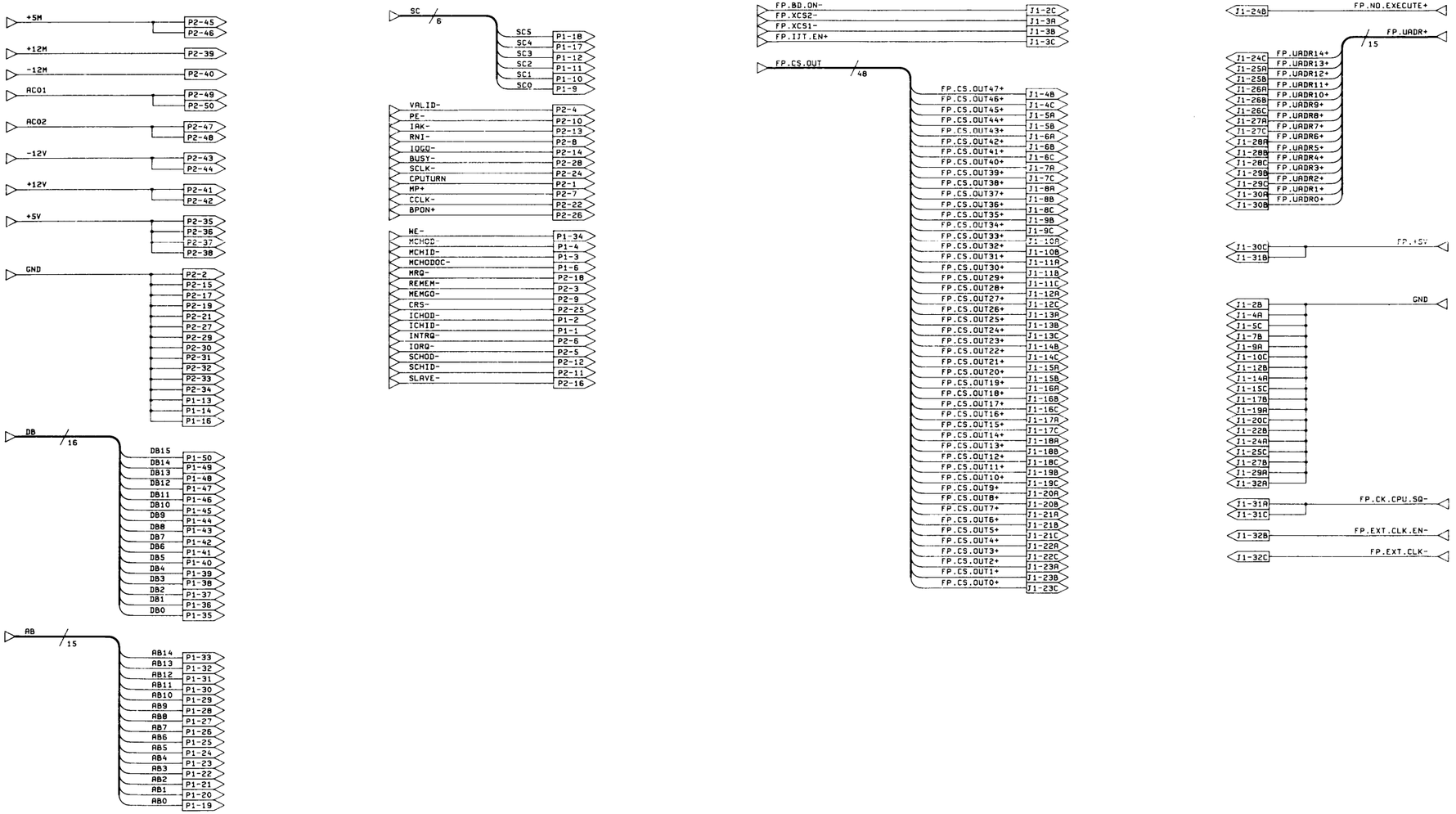
Figure 8-3. Control Store Card Parts Location

Table 8-1. Control Store Card Replaceable Parts (Sheet 1 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12265-60001	5	1	PCA-CONTRL STORE	28480	12265-60001
C1	0160-4835	7	24	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C2	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C5	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1990-0685	7	2	LED-LAMP LUM-INT=200UCD	28480	HLMP-6620
CR2	1990-0685	7		LED-LAMP LUM-INT=200UCD	28480	HLMP-6620
R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
U1	3101-2243	6	1	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U18	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U27	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U36	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U46	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U66	1820-1322	2	4	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U76	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U101	1820-2311	1	2	IC COMPTR TTL LS MAGTD 8-BIT	34335	AM25LS2521PC
U102	1820-2311	1		IC COMPTR TTL LS MAGTD 8-BIT	34335	AM25LS2521PC
U106	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U107	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U118	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U201	3101-0418	3	1	SWITCH-RKR DIP-RKR-ASSY 16-1A .1A 30VDC	28480	3101-0418
U202	1820-2795	5	20	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U204	1820-1278	7	3	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U205	1820-1238	9	8	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U301	1810-0256	8	2	NETWORK-RES 16-DIP1.0K OHM X 15	01121	316A102
U302	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U303	1820-1278	7		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U304	1820-1278	7		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U305	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U401	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U402	1818-3118	3	12	IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U403	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U404	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U405	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U501	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795

Table 8-1. Control Store Card Replaceable Parts (Sheet 2 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U502	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U503	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U504	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U505	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U601	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U602	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U603	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U604	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U605	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U701	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U702	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U703	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U704	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U705	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U801	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U802	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U803	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U804	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U805	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U901	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U902	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U903	1818-3118	3		IC NMOS 16384 (16K) STAT RAM 55-NS 3-S	28480	1818-3118
U904	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U905	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U1001	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1003	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U1004	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U1005	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U1101	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1103	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U1104	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1105	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1201	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1203	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U1204	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U1205	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U1301	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1303	1820-1300	6	1	IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
U1304	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1305	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U1401	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1404	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U1405	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U1501	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1504	1810-0256	8		NETWORK-RES 16-DIP1.0K OHM X 15	01121	316A102
W1	0811-3587	5	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587



D-12205-60001-56

REVISIONS			
DASH	REVISION	APPROVED	DATE
A	AS ISSUED	MKH / VDS	11/16/83

6

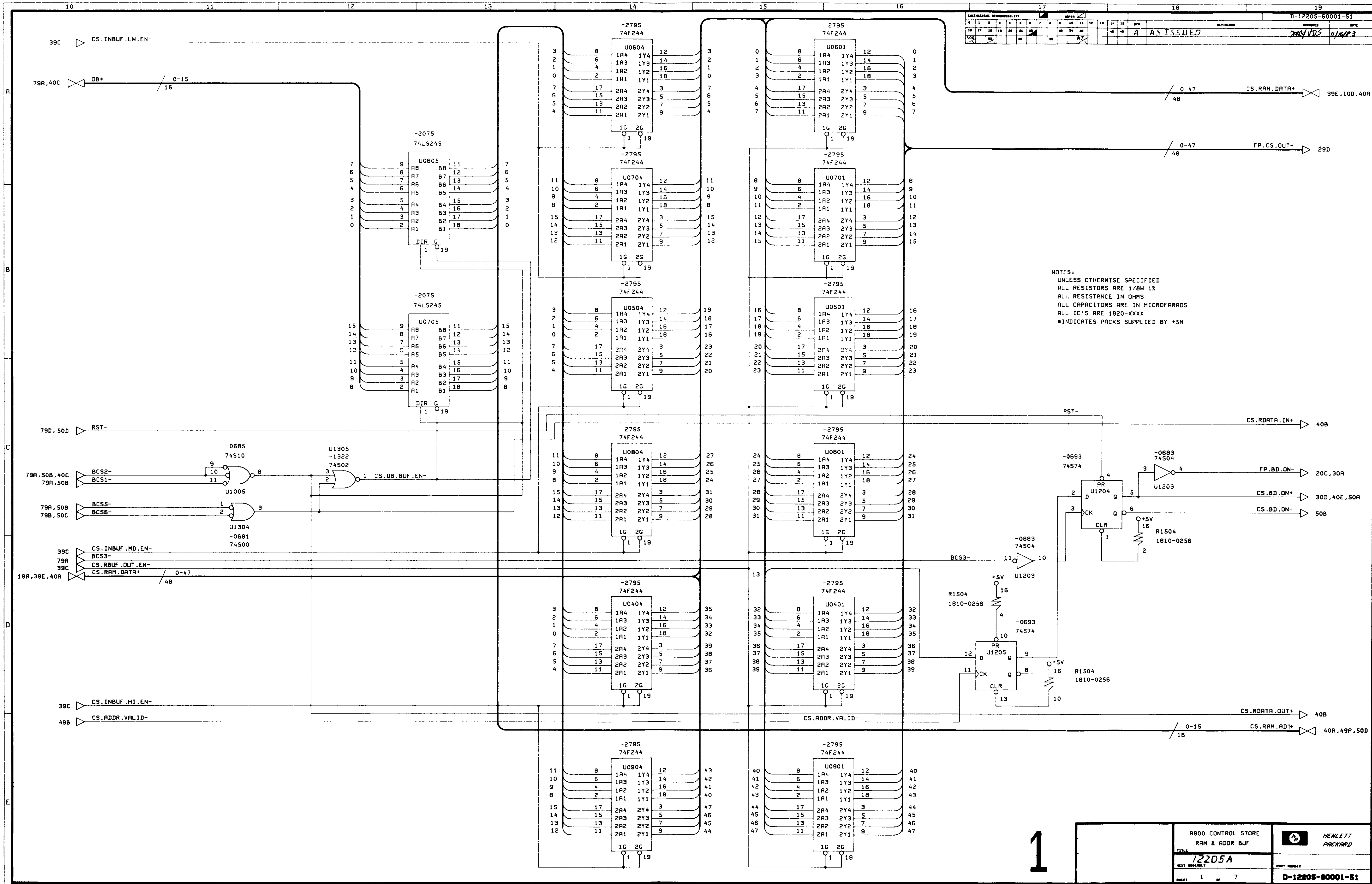
A900 CONTROL STORE
FRONT & BACKPLANE PINS

HEWLETT PACKARD

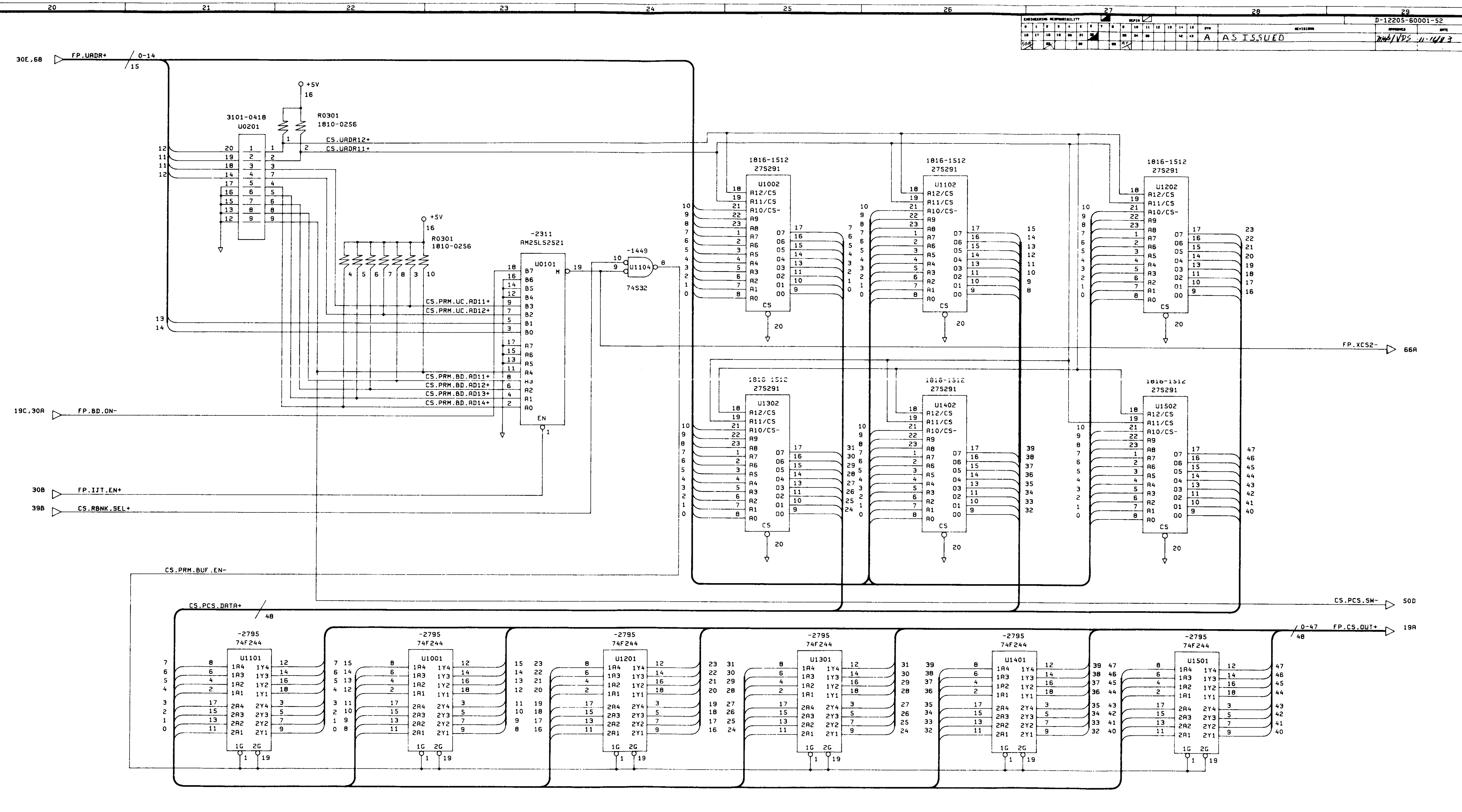
12205A

D-12205-60001-56

SHEET 6 OF 7



D-12205-60001-51
A AS ISSUED
39C CS.INBUF.LW.EN-
79A,40C DB+ 0-15 16
-2075 74LS245 U0605
-2075 74LS245 U0705
-2795 74F244 U0604
-2795 74F244 U0601
-2795 74F244 U0704
-2795 74F244 U0701
-2795 74F244 U0504
-2795 74F244 U0501
-2795 74F244 U0804
-2795 74F244 U0801
-2795 74F244 U0404
-2795 74F244 U0401
-2795 74F244 U0904
-2795 74F244 U0901
0-47 48 CS.RAM.DATA+ 39E,10D,40A
0-47 48 FP.CS.OUT+ 29D
NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
*INDICATES PACKS SUPPLIED BY +5M
79D, 50D RST-
79A,50B,40C BCS2-
79A,50B BCS1-
-0685 74S10 U1005
U1305 -1322 74S02
CS.DB.BUF.EN-
79A,50B BCS5-
79B,50C BCS6-
U1304 -0681 74S00
39C CS.INBUF.MD.EN-
79A BCS3-
39C CS.RBUF.OUT.EN-
19A,39E,40A CS.RAM.DATA+ 0-47 48
39C CS.INBUF.HI.EN-
49B CS.ADDR.VALID-
CS.RDATA.IN+ 40B
-0693 74S74 U1204
-0683 74S04 U1203
FP.BD.ON- 20C,30A
CS.BD.ON+ 30D,40E,50A
CS.BD.ON- 50B
R1504 1810-0256
-0693 74S74 U1205
CS.RDATA.OUT+ 40B
0-15 16 CS.RAM.ADT+ 40A,49A,50D
1
A900 CONTROL STORE
RAM & ADDR BUF
12205A
SHEET 1 OF 7
HEWLETT PACKARD
D-12205-60001-51



NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
*INDICATES PACKS SUPPLIED BY +5M

2

A900 CONTROL STORE
PCS BANK

NEXT ASSEMBLY 12205A

SHEET 2 OF 7

HEWLETT PACKARD

PART NUMBER D-12205-60001-52

CHANGE/ISSUE RESPONSIBILITY	REV/ISS	D-12205-60001-53
	A AS ISSUED	APPROVED DATE

59B CS.WE.LW-

19C,20C FP.BD.ON-

49A CS.CNTR.ADDR+ 0-11 / 12

59D,40A CS.RAM.BNK.ON+

20C,66B FP.IJT.EN+

59B CS.WE.MD-

19C,40E,50A CS.BD.ON+

59C CS.WE.HI-

20A,66B FP.UADR+ 0-14 / 15

1810-0256 -2311 AM2SLS2521 U0102 R0301 +5V

-2795 74F244 U0302

-2795 74F244 U0202

1818-3118 IMS1420 U0702 U0703 U0602 U0603 U0802 U0803 U0502 U0503 U0902 U0903 U0402 U0403

FP.XCS1- 65B

CS.RBNK.SEL+ 20C

U1203 -0683 74S04

CS.INBUF.HI.EN- 10D

CS.INBUF.MD.EN- 10D

CS.INBUF.LW.EN- 10R

CS.RBUF.OUT.EN- 10D

0-47 / 48 CS.RAM.DATA+ 19A,10D,40A

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
#INDICATES PACKS SUPPLIED BY +5M

3

A900 CONTROL STORE WCS.BANK

12205A

HEWLETT PACKARD

D-12205-60001-53

SHEET 3 OF 7

59D,30B
19A,39E,10D
19E,49A,50D
CS.RAM.BNK.ON+
CS.RAM.DATA+ / 48
CS.RAM.ADT+ / 16

CS.RAM.ADT+ / 12 CS.CNTR.ADDR+ → 19E,40A,50D 30B

59C CS.MUX.SELA+

59C CS.MUX.SELB+

59B CS.INC.ADD.CNTR-

19C CS.RDATA.IN+
19D CS.RDATA.OUT+

79A,10R DB7+
79A,50B LDCM1-

79A,10C,50B BCS2-
79A,50A CKDAT-

79B,50B DVCMD-
79C,50A SCLK+

79B SACK-

19C,30D,50A CS.BD.ON+

CS.ADDR.VALID- → 10E

CS.LD.AD.CNTR- → 50D

SRQ- → 79C

-1278 74LS191 U0204
-1278 74LS191 U0303
-1278 74LS191 U0304
D,QD C,QC B,QB A,QA CEN REM CLK M/M LD D/U

-1238 74LS253 U0505
-1238 74LS253 U0405
-1238 74LS253 U0305
-1238 74LS253 U0205
-1238 74LS253 U0905
-1238 74LS253 U1004
-1238 74LS253 U1003
-1238 74LS253 U0805
1C0 1C1 1C2 1C3 2C0 2C1 2C2 2C3 A B 1G 2G 1Y 2Y

-1322 74S02 U1305
-1322 74S02 U1305
-1449 74S32 U1105
-1449 74S32 U1104
-0693 74S74 U1505 PR D CK CLR Q
-0693 74S74 U1405 PR D CK CLR Q

+5V
R1504 1810-0256

CS.DMA.IN+
CS.DMA.IN-
CS.EN.AD.CNTR2-
CS.MUX.EN-
CS.EN.AD.CNTR1-
CS.LD.AD.CNTR-
CS.DVCMD-
CS.MUX.EN-

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
*INDICATES PACKS SUPPLIED BY +5M

4

A900 CONTROL STORE
ADDR CNTR & MUX
TITLE
12205A
NEXT ASSEMBLY
HEWLETT PACKARD
PART NUMBER
D-12205-80001-54
SHEET 4 OF 7

D-12205-60001-55
A AS ISSUED

79C,40E SCLK+
79A,40C CKDAT-
19C,30D,40E CS.BD.ON+
79A,10C BCS1-
79A,10C BCS5-
79A,40C LDCM1-
19C CS.BD.ON-
79B,40E DVCMD-
79A,10C,40C BCS2-
79B,10C BCS6-
19E,49A,40A CS.RAM.ADT14+
49C CS.LD.AD.CNTR-
79D,10C RST-
29D CS.PCS.SW-

-1449 74S32 U1105
-1322 74S02 U1305
-1367 74S00 U1404
-0693 74S74 U1405
-0685 74S10 U1005
-1367 74S08 U1404
-1449 74S32 U1105
-1367 74S08 U1404
-0685 74S10 U1005
-0683 74S04 U1203
1810-0256 R1504 +5V
-1300 74LS195 U1303
-0681 74S00 U1304
-0681 74S00 U1304
-1322 74S02 U1103
-1322 74S02 U1103
-0683 74S04 U1203
+5V R1504 1810-0256
-0693 74S74 U1205
+5V RAM LED 1990-0685
+5V PROM LED 1990-0685
-1449 74S32 U1104

CS.WR.DATA-
CS.WR.VALID+
CS.DATA-
CS.COUNT.EN+
CS.CNT.EN-
CS.WRD.CEN-
SCLK+
BCS2-
CS.INC.ADD.CNTR-
CS.INC.WRD.CNTR-
CS.BD.ON-
CS.WRD.CNTR.RST-
CS.HI.WRD+
CS.MD.WRD+
CS.LW.WRD+
CS.BCS6+
CS.LW.WRD+
CS.RAM.BNK.ON+
W1

CS.INC.ADD.CNTR- 40D
CS.WE.LW- 30A
CS.WE.MD- 30C
CS.WE.HI- 30D
CS.MUX.SELA+ 40A
CS.MUX.SELB+ 40D
CS.RAM.BNK.ON+ 30B,40A

SWITCH CONFIGURATION FOF PCB BANK

SW	2K	4K	8K	DISABLE PCB
1	OP	OP	CL	DON'T CARE
2	OP	CL	CL	"
3	CL	OP	OP	"
4	CL	CL	OP	"
5	B14	B14	B14	"
6	B13	B13	B13	"
7	B12	B12	OP	"
8	B11	OP	OP	"
9	CL	CL	CL	OP

NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
*INDICATES PACKS SUPPLIED BY +5M

5

A900 CONTROL STORE
WRD CNTR & CNTL
12205A
SHEET 5 OF 7
HEWLETT PACKARD
D-12205-60001-55

ENGINEERING RESPONSIBILITY	SCALE	SIZE
		A

SYM	REVISIONS	APPROVED	DATE
A	RS ISSUED		7/29/80
B	CPUTURN-ADD & FCLR-DELETE		
C	MEMGO & BPDH-((COMMENTS)DH #)		

L-SERIES BACKPLANE

DATA BUS

LMIP BUS TRI-STATE

DATA BUS TRI-STATE

BOARD ID CODE

SELECT CODE SWITCHES

U67 IAF5-6202 I/O PROCESSOR (IOP) CHIP

BUS CONTROL STATES

PERIPHERAL INTERFACE

SLAVE FF

SLACK FF

MEMGO FF

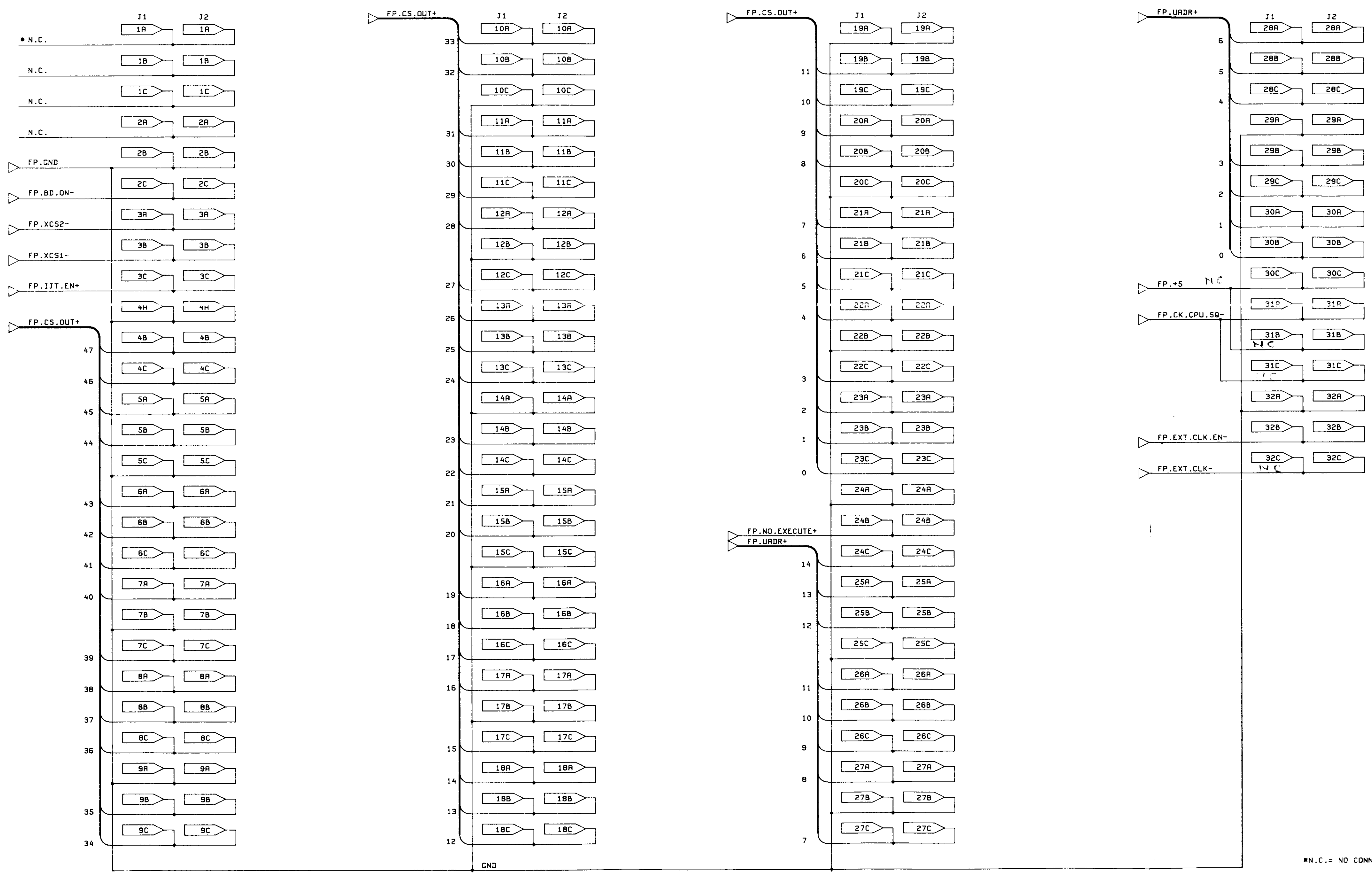
4.7K RESISTORS ARE 1810-0079
RESISTOR DIP +5 PIN 16
2K RESISTORS ARE 1810 0280
RESISTOR DIP +5 PIN 16

NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

DRAWN BY: Y.SUZUKI	DATE 8.30.83	A900 WCS CARD	HEWLETT PACKARD
ENGINEER: S.BOSCHMA		TITLE	
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG		SHEET 7 OF ?	E-12205-60001-57

D-12205-60002-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	11/29/83



*N.C.= NO CONNECTIONS

TITLE	A900 CONTROL STORE FRONTPLANE 2 CONN.
NEXT ASSEMBLY	12205A
SHEET	1 OF 1
PART NUMBER	12205-60002
	D-12205-60002-51

HEWLETT PACKARD

Chapter 9
Backplane

9.1 Introduction

This chapter describes the operational characteristics and the theory of operation for the I/O (input/output) interface.

The backplane provides a link between the A900 Computer System sequencer card, data path card, memory controller, memory array, control store, interface cards and the power supply. There are two backplane configurations covered: The HP 2139A 20-slot backplane (Part No. 12210-60002), and the HP 2439A 16-slot backplane (Part No. 02430-60004).

In this document the backplane is viewed from two aspects: physical and logical.

The backplane signal names that are basic to this I/O scheme may be prefaced with either BP.name or LBP.name. The LBP prefix indicates that it is used in I/O control and it is discussed in the I/O Interfacing Guide.

The I/O backplane of the A900 computer is the same as that of the HP 1000 L-Series Computer with the exception that CPU memory accesses do not use the backplane. In all discussions in this document concerning the "I/O backplane", the "A-Series/L-Series type backplane" is meant. The I/O reference material for this and all A-Series computers is the HP 1000 A-Series and L-Series Computer I/O Interfacing Guide, Part No. 02103-90005.

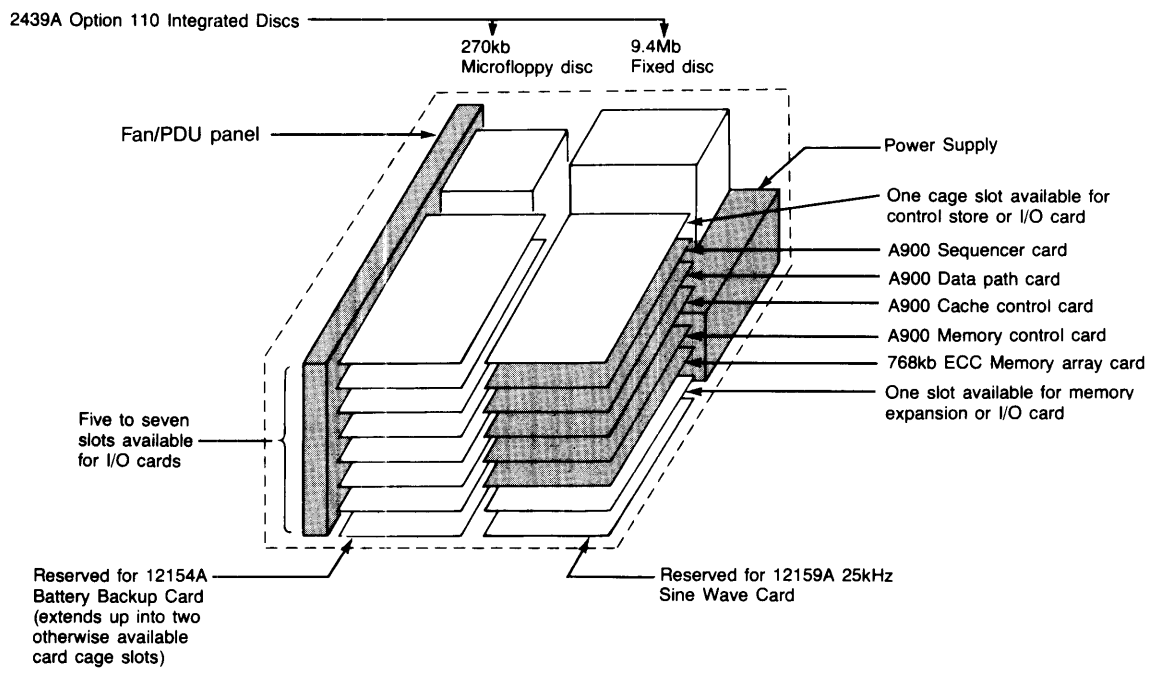
9.2 Backplane Physical Description

The backplane functions as a mother board for the processor, memory and interface cards. It is a printed circuit card on which the traces carry the power, ground and interconnecting signals between all the cards in the computer. Figure 9-1 shows the physical layout of the 16-slot and 20-slot backplanes. The connector pin listing for the processor is provided in Appendix A.

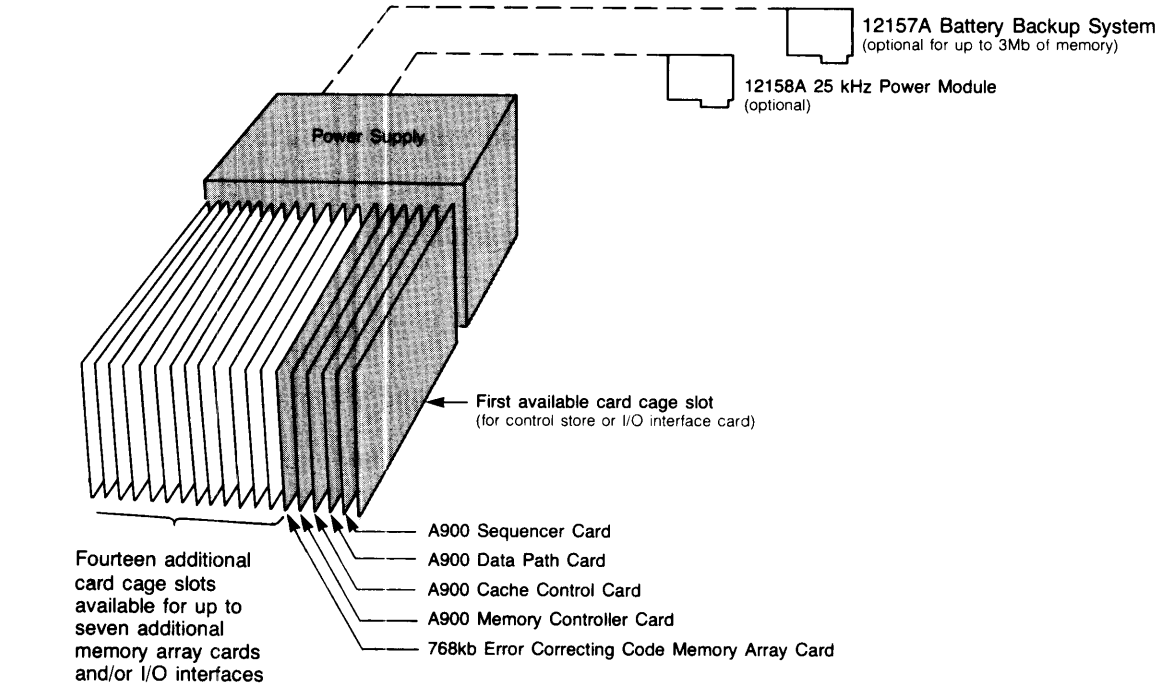
The logical backplane defines protocols for the communications between all cards in the system. The definition, function, and timing of the backplane signals, and the protocols for their interaction are all considered to be part of the logical backplane.

Thus, the physical backplane houses a set of communications channels, whereas the logical backplane defines protocols for that communication.

This chapter covers both aspects of the backplane, and is intended to provide all the information needed to design a hardware interface to the backplane and thereby successfully integrate a design of arbitrary functions into the A900 Computer.



16-Slot Backplane



** Additional memory array cards must plug into space immediately to the left of the Memory Controller card, moving all card positions to the left.*

20-Slot Backplane

Figure 9-1. HP 1000 A900 Backplanes

9.3 Overview

9.3.1 System Environment Overview

An backplane integrated into a system environment is shown in Chapter 1, Figure 1-2. The backplane holds two sets of connectors for card edge connections as follows:

A. POWER SUPPLY CONNECTOR SLOTS
Dc power is connected to the backplane directly from the power supply into the side opposite from the I/O and processor cards. For the 2139A, the connection is through 50-pin sockets, designated J1 and J2 (sockets XA21 and XA22). For the 2439A, the connection is through a single 35-pin socket designated J4.

B. A900 CARD CONNECTOR SLOTS
Each processor card plugs into a 160-pin socket (4 rows of 40 pins). A single set of dual 50-pin sockets above the processor cards is for the optional control store card or an I/O card. The 20-slot backplane has 15 additional dual sockets for I/O cards, and the 16-slot backplane has nine additional dual sockets for I/O cards. The 20-slot backplane is shown in Figure 9-2, and the 16-slot backplane is shown in Figure 9-3.

A900 cards can be plugged into any backplane card slot subject to the following constraints.

a. The optional control store must be in slot 1 or it must be filled with an I/O card.

b. Slot 2 is for the sequencer card and slot 3 is for the data path card.

c. The cache control card goes directly below the data path card.

d. The memory controller must go directly below the cache control card.

e. The first error correcting memory array must go directly below the memory controller followed by any additional memory arrays.

f. All I/O cards must go below the processor cards in the order of the desired card priority (slot 1 has the highest I/O priority if it is not used for the CS card).

g. Any unused slot between two I/O cards must be filled with a priority jumper card.

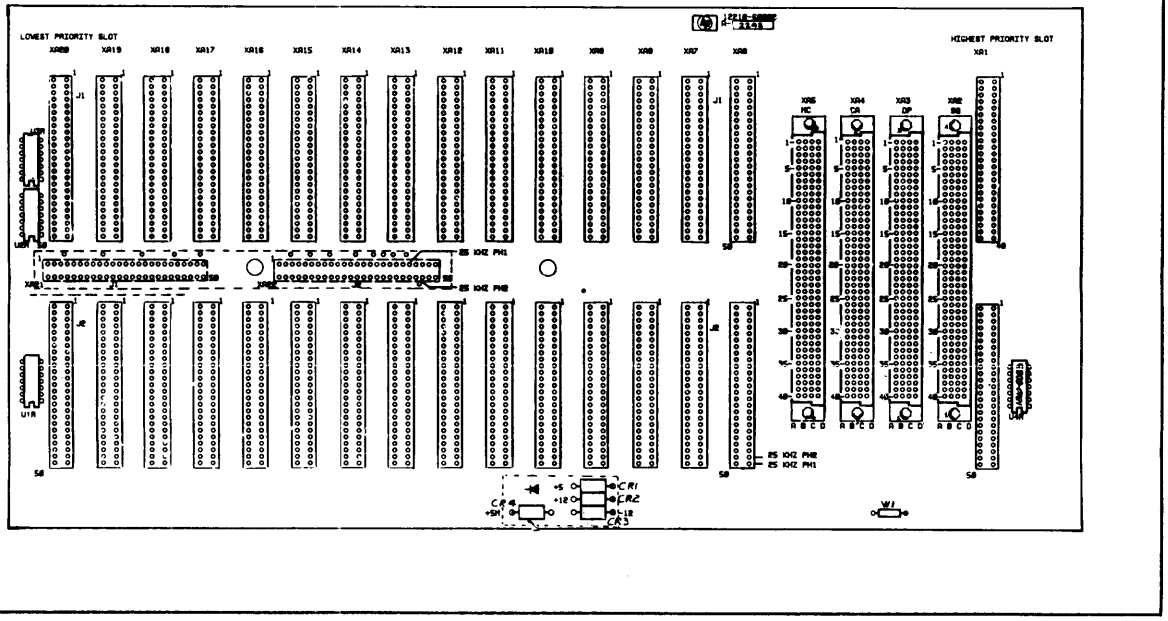


Figure 9-2. 20-Slot Backplane Configuration

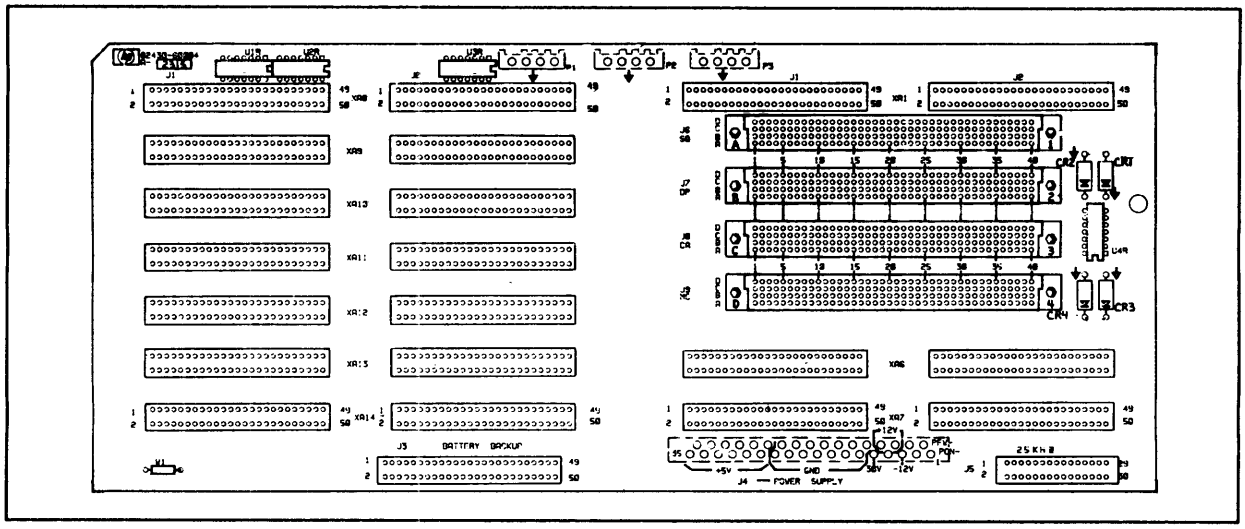


Figure 9-3. 16-Slot Backplane Configuration

The terms "above" and "below" are not to be taken literally. The term "above" refers to a higher priority slot and "below" refers to a lower priority slot where the physical orientation of the slots may be horizontal. The backplane slots are numbered from the highest priority slot XA1 in order down to XAn which is the nth highest priority slot in the card cage.

9.3.2 Internal Specifications Overview

The backplane parts location diagrams are Figures 9-2 and 9-3.

The four diodes on each backplane are on the +5V, +5M, +12V and -12V lines from the Power Supply. They are transient voltage suppressors, with a clamping action response of one picosecond, and the capability of handling a surge current of 50 amperes. They serve to protect the components on the cards plugged into the backplane from any power supply over-voltage or transient spike.

The physical backplane includes four different types of traces.

a. Bus line: This line is common to the same pin on each set of card sockets. Examples are WE- and CRS-.

b. Power Supply line: This line comes from the power supply and runs to the same pin on each set of card sockets. Examples are PFW and PON+.

c. Ground and Voltage lines: This line comes from the power supply and typically has two or more pin assignments on each set of card sockets. Grounds and voltages are typically carried on much wider traces than other signals. Examples are +5V and +12V.

d. Chained lines: This is a set of lines which connect every pair of adjacent card sockets. Each of these lines is common to exactly two sockets. Examples are ICHID-, ICHOD-, SCHID-, and SCHOD-.

The distinction between these four types of lines is important when determining backplane compatibility.

9.4 Specifications

9.4.1 General Hardware Specifications

The backplane uses a printed circuit card to provide all the required signal and power traces. One layer provides a +5V plane, and another is a ground plane to minimize signal crosstalk and permit the traces to maintain a consistent characteristic impedance throughout their length.

The remaining layers are mainly to carry signals and for voltage distribution. The layout provides a characteristic impedance of 47 to 51 ohms that provides a good match with the output impedances of the backplane drivers. The driver impedances are in the range of 25 to 100 ohms; i.e., all impedances are matched within a 2 to 1 ratio.

9.4.2 Power Supply Interconnect

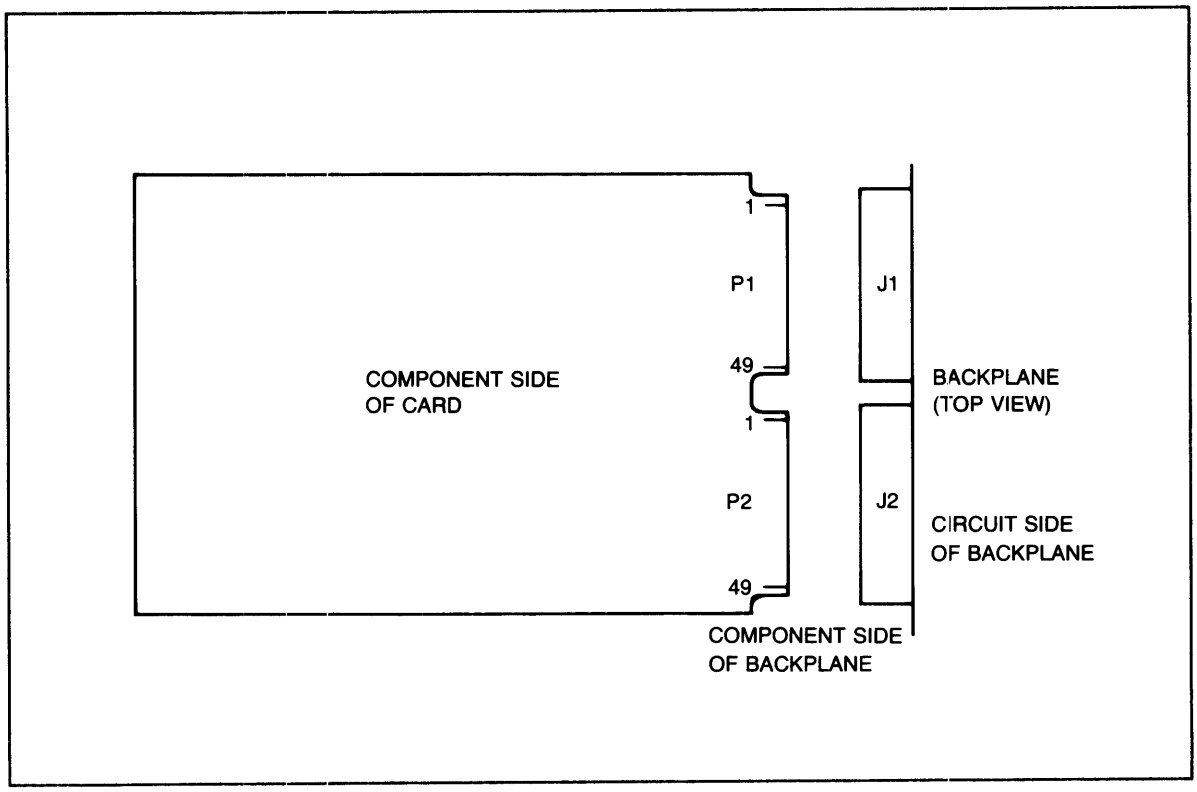
The dc output connectors for power supply connection are mounted on the opposite side from the processor and I/O connectors. The 20-slot backplane has dual 50-pin edge-type connectors, where XA21 is dedicated to +5V (36-pins) and ground (14-pins), and XA22 has the other dc voltages, power supply control signals, and the 25 kHz sine-wave supply. The 16-slot backplane has a single 35-pin female connector (J4) for the power supply in which 12 pins are used for ground and 12 pins are used for +5V. The 16-slot backplane has separate connectors (J3 and J5) for the battery backup board and the 25 kHz sine-wave board, respectively.

Refer to the power supply section (Chapter 11) of this manual for power supply details.

Ground and +5.1V lines carry the highest currents and are thus transferred over whole planes. Currents for other voltages are carried over multiple traces.

9.4.3 Card Socket Interconnects

Each I/O card has two 50-pin edge-connectors, P1 and P2, which plug into a matching set of 50 pin sockets, J1 and J2, on the backplane. The card cage is constructed with card guides, in such a manner that the cards will slide in and then snap into place in the backplane connectors. The cards must be inserted with the component sides of the cards facing the same way as shown in Figure 9-4 where the components face to the right (20-slot backplane) when looking into the front of the cage. (In 16-slot systems, the components face upward.) The pin assignments for these 100 connections are given in Table 9-1. For signal definitions, refer to Table 9-31.



8400-14

Figure 9-4. Card Socket Interconnects

Table 9-1. Pin Assignments for Backplane Sockets

PIN	P1 SIGNALS		PIN	PIN	P2 SIGNALS		PIN
1	ICHID-	ICHOD-	2	1	CPUTURN	ISOGND	2
3	MCHID-	MCHOD-	4	3	REMEM-	VALID-	4
5	MLOST-	MCHODOC-	6	5	IORQ-	INTRQ-	6
7	PFW-	SPARE	8	7	MP+	RNI-	8
9	AE0 (SC0)	AE1 (SC1)	10	9	MEMGO-	PE-	10
11	AE2 (SC2)	AE3 (SC3)	12	11	SCHID-	SCHOD-	12
13	GND	GND	14	13	IAK-	IOGO-	14
15	COTURN	GND	16	15	ISOGND	SLAVE-	1
17	AE4 (SC4)	SELFC-	18	17	ISOGND	MRQ-	18
19	AB0+	AB1+	20	19	ISOGND	SPARE	20
21	AB2+	AB3+	22	21	ISOGND	CCLK-	22
23	AB4+	AB5+	24	23	SPARE	SCLK-	24
25	AB6+	AB7+	26	25	CRS-	PON+	26
27	AB8+	AB9+	28	27	ISOGND	BUSY-	28
29	AB10+	AB11+	30	29	GND	GND	30
31	AB12+	AB13+	32	31	GND	GND	32
33	AB14+	WE-	34	33	GND	GND	34
35	DB0+	DB1+	36	35	+5V	+5V	36
37	DB2+	DB3+	38	37	+5V	+5V	38
39	DB4+	DB5+	40	39	+12M	-12M	40
41	DB6+	DB7+	42	41	+12V	+12V	42
43	DB8+	DB9+	44	43	-12V	-12V	44
45	DB10+	DB11+	46	45	+5M	+5M	46
47	DB12+	DB13+	48	47	25kHz Ph2	25kHz Ph2	48
49	DB14+	DB15+	50	49	25kHz Ph1	25kHz Ph1	50

9.4.4 Backplane Loading Rules

Backplane loading rules were established in order to provide guidelines for the selection of bus drivers and backplane signal drivers, and in order to insure that these drivers are not overloaded. These rules take into account the drive capabilities and loading of certain industry standard parts such as the S and LS 240 and 241. Because there may be a maximum of 15 I/O interface cards in any given A900 system, each card must adhere strictly to the rules in order to prevent possible overloading. These loading rules were established assuming a maximum of 20 cards in a system. Note that the I/O Master is designed such that all backplane lines except the data bus are buffered and cannot be used in the unbuffered form by I/O interface logic external to the I/O Master.

DC loading rules are made to ensure that a device driving any given backplane line can handle sufficient current to keep all the inputs connected to that line at the required voltage level. Low-state load on a given line is the sum of I_{IL} maximum for all receivers plus I_{OZL} for all tri-state drivers. High-state load is the sum of I_{IH} for all receivers plus I_{OZH} for all tri-state drivers.

9.4.4.1 AC Loading

Every connection made to any given line places a a capacitive load on that line due to PC board trace capacitance and due to the integrated circuit input or output capacitance. Care must be taken to ensure that any given line is not capacitively overloaded as this results in a slowing down of its switching speed to below an acceptable level. Typical delays/capacitive loads are in the range of 2-nanoseconds/50-picofarads for a line driven by an LS240/241 and 4-nonoseconds/50-picofarads for an LS373/374. Refer to the capacitance data in Table 9-2.

Table 9-2. Capacitance Data on 20-Slot System

PIN	SIGNAL	C IN pF L
J1 - 1,2	ICHID, ICHOD	40
J1 - 3,4	MCHID, MCHOD	25
J1 - 5	MLOST	200
J1 - 6	MCHODOC	850
J1 - 7	PFW	200
J1 - 9,10,11,12,17	AE0 - AE4 (SC0 - SC4)	400
J1 - 18	SELFC	900
J1 - 19,20,..,34	ADDRESS BUS	500
J1 - 35,36,..,50	DATA BUS	1300
J2 - 1	CPUTURN	400
J2 - 3	REMEM	600
J2 - 4	VALID	550
J2 - 5	IORQ	580
J2 - 6	INTRQ	650
J2 - 7	MP	500
J2 - 8	RNI	500
J2 - 9	MEMGO	550
J2 - 10	PE	500
J2 - 11,12	SCHID, SCHOD	30
J2 - 13	IAK	500
J2 - 14	IOGO	500
J2 - 16	SLAVE	740
J2 - 18	MRQ	550
J2 - 20	FCLK	500
J2 - 22	CCLK	620
J2 - 23	SPRQ	250
J2 - 24	SCLK	500
J2 - 25	CRS	500
J2 - 26	PON	550
J2 - 28	BUSY	400

NOTE: All capacitances shown are the estimated worst case figures.

9.5 Interface Protocols

The following paragraphs deal with the protocols for memory accesses and I/O card accesses. An important feature of A-Series computers is their distributed intelligence; i.e., every interface card has the capability of handling its own memory accesses (DMA), of decoding its own instructions, and of forcing the central processor into slave mode processing. Refer to the HP 1000 A/L-Series I/O Interfacing Guide for general backplane information and protocol diagrams.

9.5.1 Memory Access Protocol

Every card that accesses memory uses the same handshake protocol. This approach greatly simplifies the operation of multichannel DMA. The DMA feature of every A-Series I/O interface allows input or output operations to proceed without processor intervention thus significantly easing the processing requirements on the CPU. Unlike other A-Series processors, the A900 only uses the A-Series backplane for I/O related transactions. For DMA, the A900 will assert CPUTURN- upon being blocked by MRQ- so that it will not be locked out of the backplane by DMA of high bandwidth. This keeps all cards from re-asserting MRQ- after they finish their present request.

A priority scheme is used in the A-Series backplane to resolve contention between interfaces wanting memory cycles. An interface wanting a memory cycle will assert MRQ-, MCHOD-, and MCHODOC-. The first signal, MRQ-, will disable the processor from taking the next memory cycle. MCHOD- is part of a priority chain which will ripple down, disabling all lower-priority interfaces. MCHODOC- is a look-ahead on this chain. It is used as the top of the chain for the stack of lowest-priority slots. Although MRQ- may be asserted by one or more interfaces at any given time, MEMGO- may only be asserted by the one interface that gets the memory cycle.

An interface determines if it is entitled to a memory cycle (to assert MEMGO-) by monitoring certain backplane signals. It can initiate a memory cycle on any falling edge of SCLK- when BUSY- is high, its MCHID- is high, and its MRQ- has been asserted for at least one cycle. This stipulation means that contention among I/O cards for memory always has one cycle of SCLK in which to be resolved, namely, the cycle which occurs just before the assertion of MEMGO-.

The processor card begins its access to the A-Series backplane by asserting MEMGO- on the falling edge of SCLK-. If an I/O interface card desiring a DMA transfer asserts MRQ- on that same edge, the processor card must immediately relinquish its claim to accessing memory by releasing MEMGO- prior to the next rising edge of SCLK-. Therefore, contention between the

processor and any I/O interface for the A-Series backplane is resolved during the long half cycle between the falling and rising edges of SCLK-. MEMGO- will be asserted at the completion of all current DMA requests. Refer to Table 9-15 for the aborted MEMGO- timing specifications.

9.5.1.1 Remote Memory Access

All I/O interface cards have the capability of accessing a remote memory (i.e., a memory other than that plugged into the backplane directly above the processor card). In order to access the remote memory, an interface card must assert REMEM- with MEMGO-. The assertion of REMEM- will signal the local memory to ignore MEMGO-. Instead, a cycle with the remote memory will be initiated. This function is not currently used in the A900 and has not been tested.

9.5.1.2 Expanded Memory Access

To facilitate DMA access to expanded memory, each A-Series I/O card has been designed with a five bit Address Extension Bus AE0-AE4 (previously called SC0 - SC4) that is driven onto the backplane simultaneously with the address bus during a memory access.

9.5.2 I/O Transfer Protocol

The A-Series I/O structure is such that I/O instructions are not executed by the CPU; instead, they are decoded by the interface card to which they apply, then executed by that interface card in conjunction with the CPU. The instruction decoding and executing capability of the interface card is provided by an LSI I/O chip, located on each interface card. The I/O handshake uses the two signals IORQ- (I/O request by an interface card) and IOGO- (go ahead signal from the processor card).

The processor card's IOGO- may be preempted by concurrent DMA activity. Both IOGO- and MRQ- are asserted on the falling edge of SCLK- ; thus the processor may come into contention with an I/O interface card if both signals occur simultaneously. The DMA activity has higher priority than the processor so that IOGO- must be deasserted prior to the next rising edge of SCLK-. When all concurrent DMA has completed, then IOGO- may be asserted on the backplane to complete the I/O handshake.

The I/O instructions may be broken down into three groups in terms of their execution requirements, as follows:

A. Data Transfer I/O instructions - OTA/B, LIA/B, MIA/B

This group requires a double handshake (refer to the DMA subsection). In the first half of the handshake, a control word is transferred from the interface card to the processor card. In the second half of the handshake, the data is transferred either into or out of the A or B register, according to which of the six instructions above is being executed. I/O transfers over the backplane have lower priority than DMA transfers, and can be preempted. DMA transfers can occur while an I/O instruction is in the process of being executed (i.e., between the two halves of the handshake).

B. Status Sensing Instructions - SFS, SFC

This group requires, at most, a single handshake during which a control word from the interface card to the processor (signaling the program counter) is transferred. If no skip is required, no handshake occurs.

C. Status Altering Instructions - STC, CLC, STF, CLF

This group requires no interaction with the CPU. The interface card executes these instructions itself, and never needs to assert IORQ-.

9.6 Operational Characteristics

Most of the I/O interface is done on the CA board and all of the macrointerrupt logic is on the MC card. The slave acknowledge signal is also driven by the MC card. The macrointerrupt system is distributed across the SQ, CA, and MC cards, and the microinterrupt system is contained on the SQ card.

9.6.1 Direct Memory Access (DMA)

The DMA handshakes are shown in Figure 9-5. Note that the shortest DMA read cycle is three SCLK cycles long. DMA write cycles are always two SCLK cycles long since they are "pre-acknowledged"; i.e., the handshake happens as soon as the request is received. The BUSY signal may be asserted longer if the cache cannot handle the write request in time before another can come along. Remote memory (REMEM) is supported on the A900.

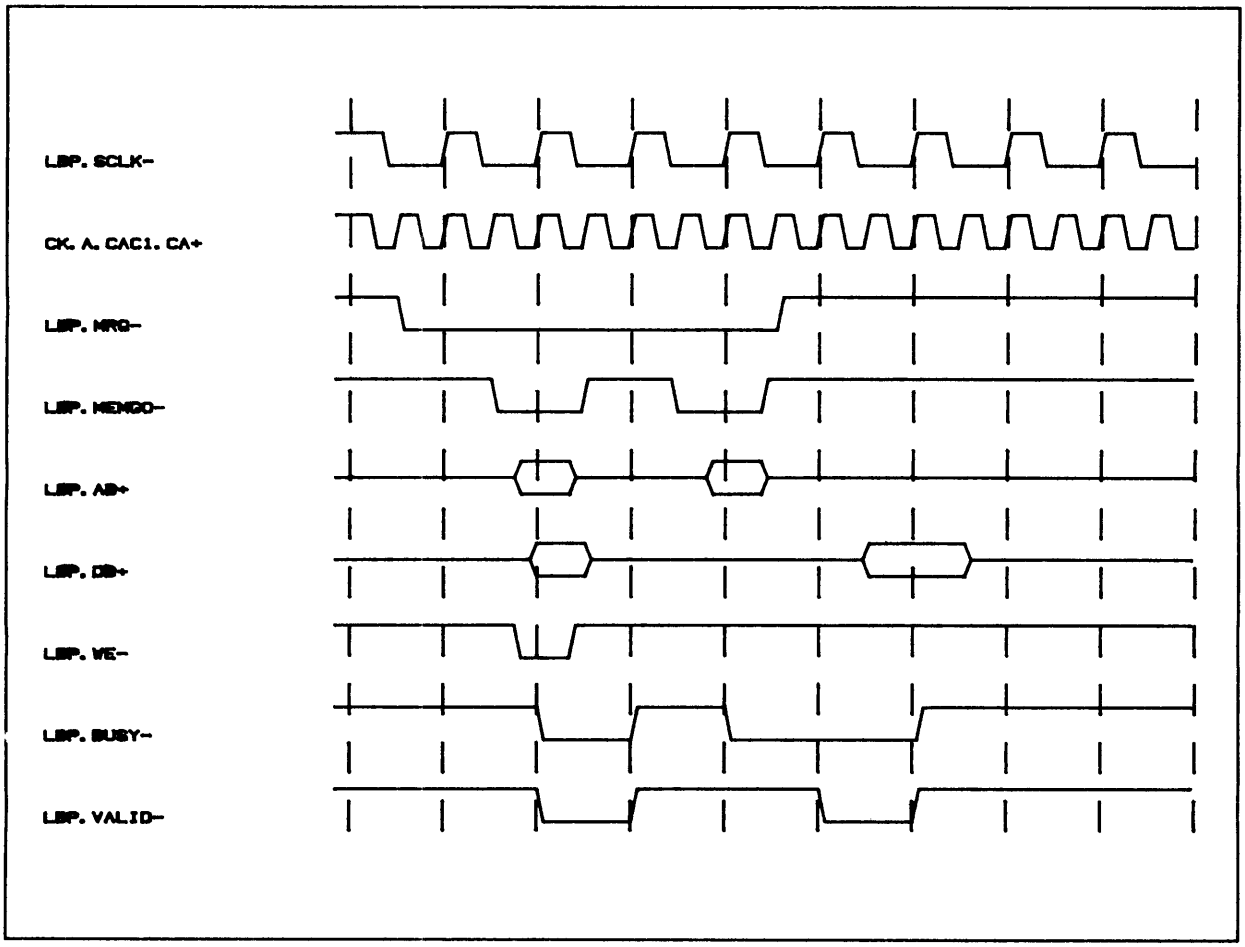


Figure 9-5. DMA Write Followed by DMA Read

9.6.2 Broadcast I/O (BCIO)

A BCIO cycle is shown in Figure 9-6. MEMGO is asserted by the cache to support an analysis interface (AI) card. A normal I/O card does not recognize MEMGO and the cache does not do a memory cycle for broadcast operations. The signal CPUTURN is asserted if the cache attempts a BCIO cycle and MRQ is asserted on the backplane. CPUTURN will remain on until the BCIO cycle can be completed. This is to avoid having the CPU come to a standstill during heavy DMA traffic.

The sequence of asserting signals is for the I/O master operation (the I/O master is the I/O interface logic circuit on each I/O card). The cache does not start a BCIO cycle until it has the data ready to send. The TBUS is used to drive the SBUS which drives the backplane.

9.6.3 IOGO Read

An IOGO read and write cycle is shown in Figure 9-7. The cache does not look at the IORQ line. It is expected that the CPU will not attempt an IOGO read unless IORQ is asserted. It is also expected that no device connnected to the backplane will require an IOGO cycle other than three SCLK periods long. To get the data to the CPU, the LDIN latch drives the MC version on the SBUS which, in turn, drives the BP version which goes to the R-register on the DP board.

9.6.4 IOGO Write

An IOGO write cycle is also shown in Figure 9-7. The data for an IOGO write comes from the TBUS, which is driven onto the MC SBUS, which is driven onto the BP SBUS, where the LDOUT latch drives it onto the backplane. For both IOGO read and IOGO write, CPUTURN is asserted if MRQ is asserted and will remain on until IOGO can be asserted onto the backplane. Just as for BCIO, this is to avoid the CPU being locked out during heavy DMA traffic.

9.6.5 Interrupt Acknowledge (IAK)

An IAK cycle is shown in Figure 9-8.

For an IAK, CPUTURN is also driven if MRQ prevents IAK from being asserted. After IAK is asserted, the cache then waits until MEMGO is asserted. The CPU gets the select code from the backplane because it is driven onto the address bus which is the default selection in the MEM field. This allows the CPU to read it by coding RREG/MADR in the same line as SPO/IAK.

Note that the slave chain (SCHID-, SCHOD-) operates differently from the other chains in that its quiescent state is low or disabled. It is enabled only for one cycle at a time, during which the highest priority interface card pulling on SLAVE- must assert IORQ-, thereby entering slave mode. SCHOD is deasserted to acknowledge a slave request. Since SCHOD can happen concurrent with DMA, the CPU first asserts the no freeze bit in the Cache Control Register (CCR) and then deasserts the SCHOD bit in the Memory Control Register (MCR) for two CPU cycles. This assures that SCHOD is asserted for exactly one SCLK period. Unlike all other I/O handshakes, this one will not freeze the CPU and CPUTURN need not be asserted to keep from locking up the processor.

9.6.6 Slave Mode Transfers

An interface card may force the processor card to enter an I/O handshake by pulling down the open-collector line SLAVE-. Once in slave mode, the interface has the capability of accessing the internal CPU registers, and does so with the use of the same handshake signals as in the I/O transfer protocol. See Figure 9-9 for slave mode operation.

Once the slave mode has been entered, an interface card may keep the processor in that mode as long as desired by setting a bit in the control word (transferred during the first half of the handshake) which signals that another double handshake will occur.

The control words which are sent to the CPU by an interface card during an I/O instruction (requiring a handshake), and during all slave mode processing are made up of five bits using bits 8 through 4 of the data bus.

Control words for slave mode processing are defined below:

	Data Bus Bit				
	8*	7	6	5	4
NOP	X	0	0	0	0
Load Program Counter	X	0	0	0	1
Load A	X	0	0	1	0
Load B	X	0	0	1	1
Clear O	X	0	1	0	0
Set O	X	0	1	0	1
OR into A/B	X	0	1	1	0
Increment Program Counter	X	0	1	1	1
Read E and O	X	1	0	0	0
Enable ROMs	X	1	0	0	1
Read A	X	1	0	1	0
Read B	X	1	0	1	1
Clear E	X	1	1	0	0
Set E	X	1	1	0	1
Read P	X	1	1	1	0
Read and Increment P	X	1	1	1	1

* Loop for next control word if X=1; last handshake if X=0.

9.6.7 Reset Signal

The I/O backplane reset signal (CRS) is shown in Figure 9-10. For CRS, CPUTURN needs to be asserted to stop DMA requests. Like most other I/O handshakes, the CPU is frozen if DMA activity gets in the way. As for all handshakes (except slave), the CPU is frozen until the correct operation has happened to the backplane. Thus, CRS should be set for only one microcycle. Leaving the CRS bit asserted in the CCR will not keep CRS asserted on the backplane.

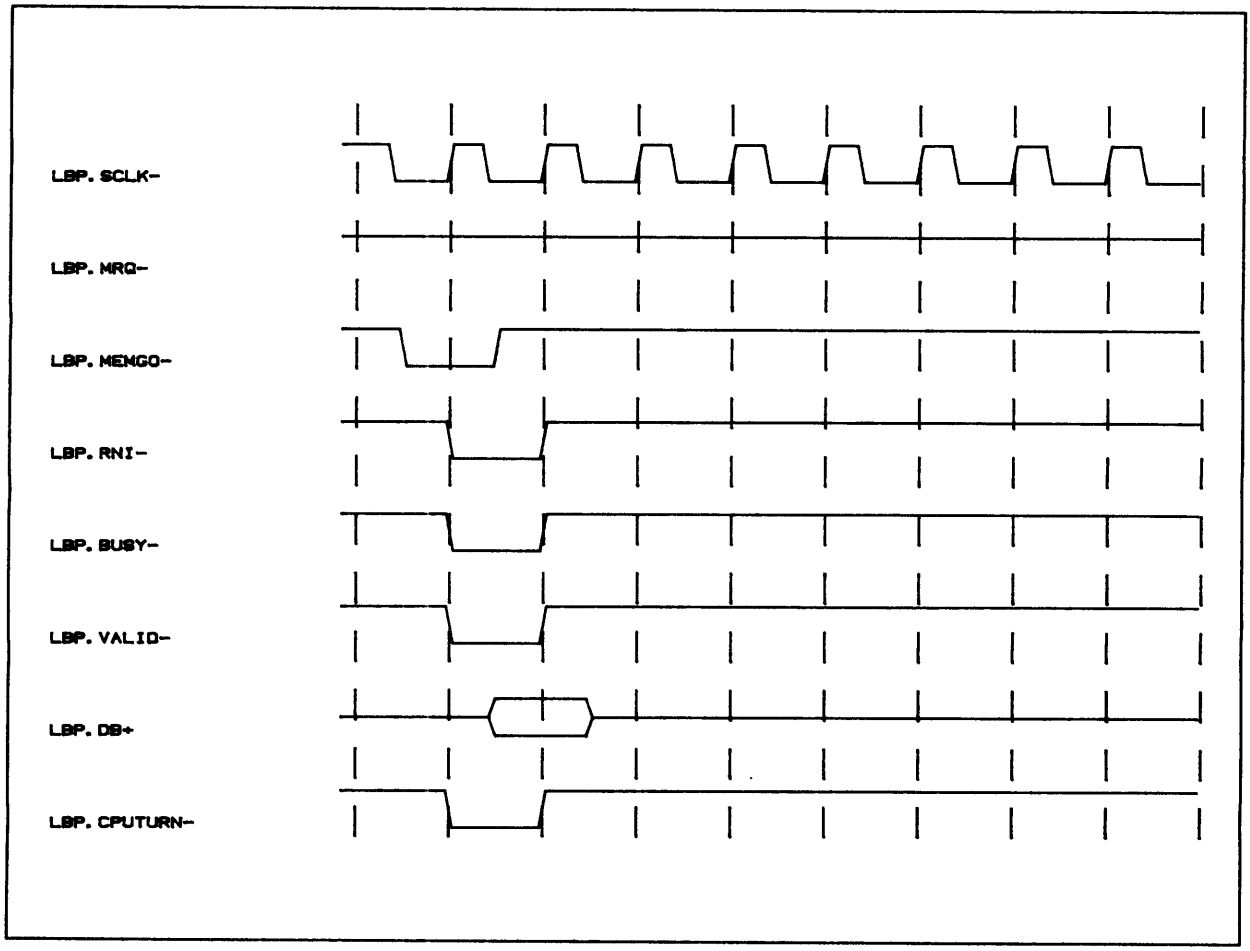


Figure 9-6. Broadcast I/O Cycle

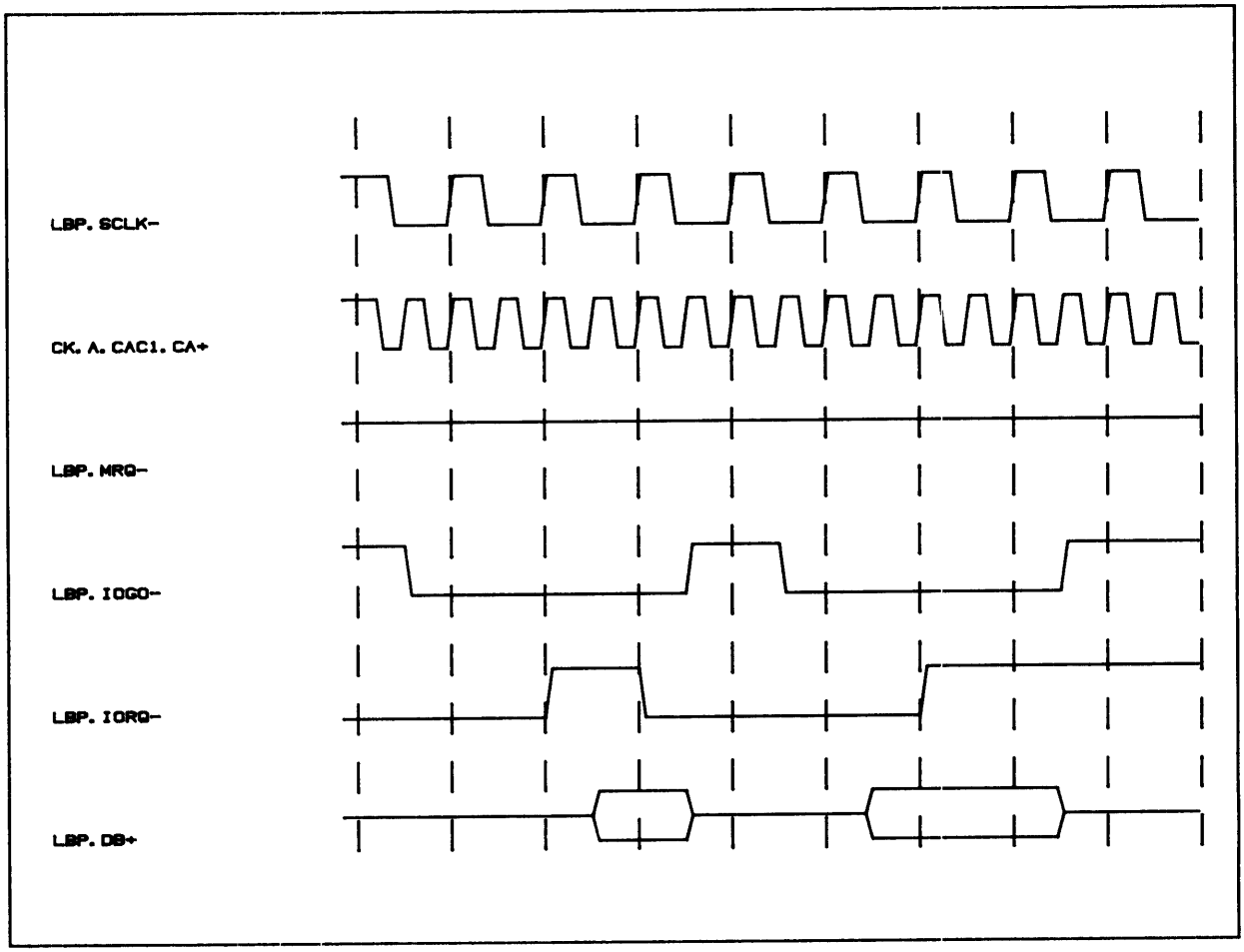


Figure 9-7. IOGO Read Followed by IOGO Write

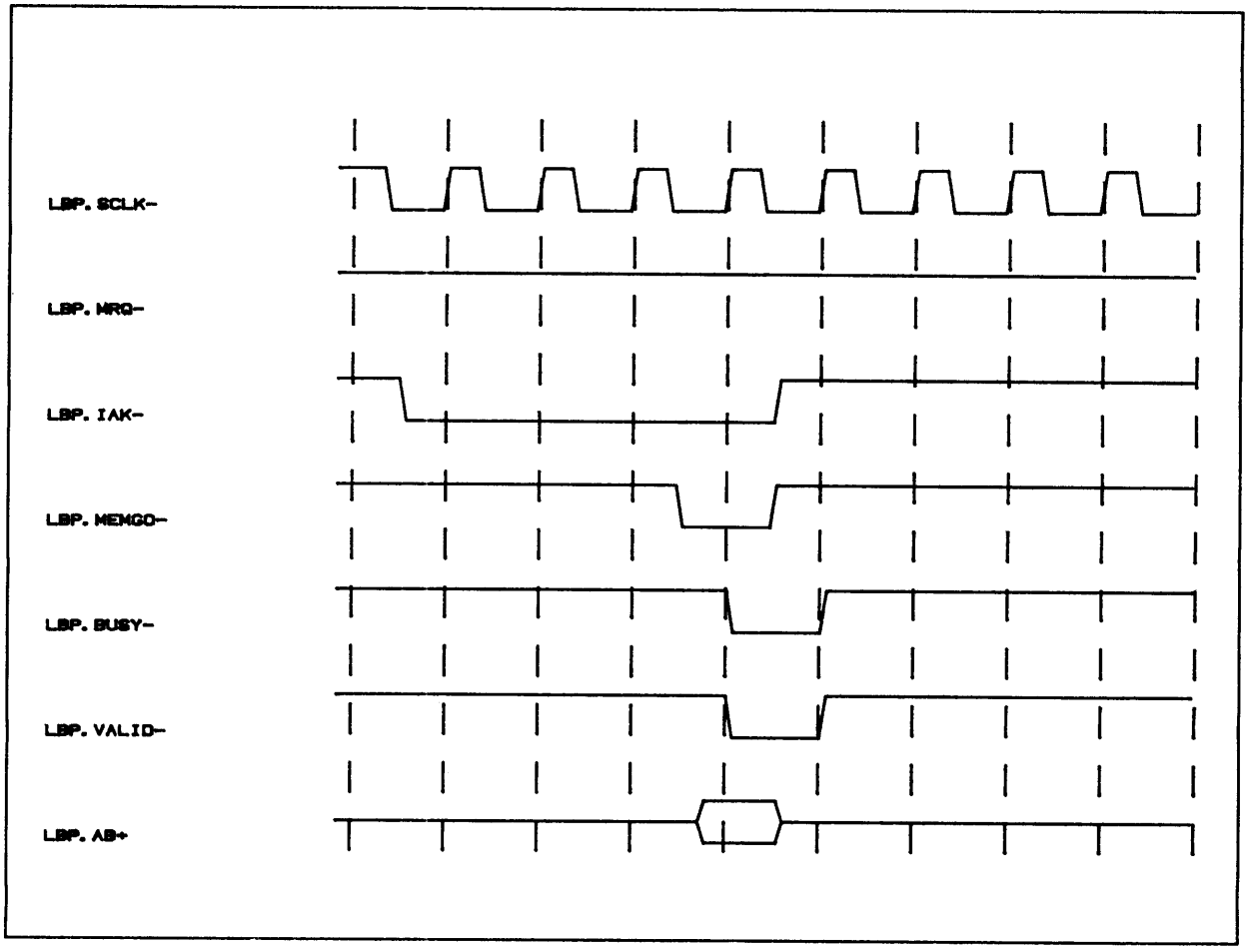


Figure 9-8. IAK Operation

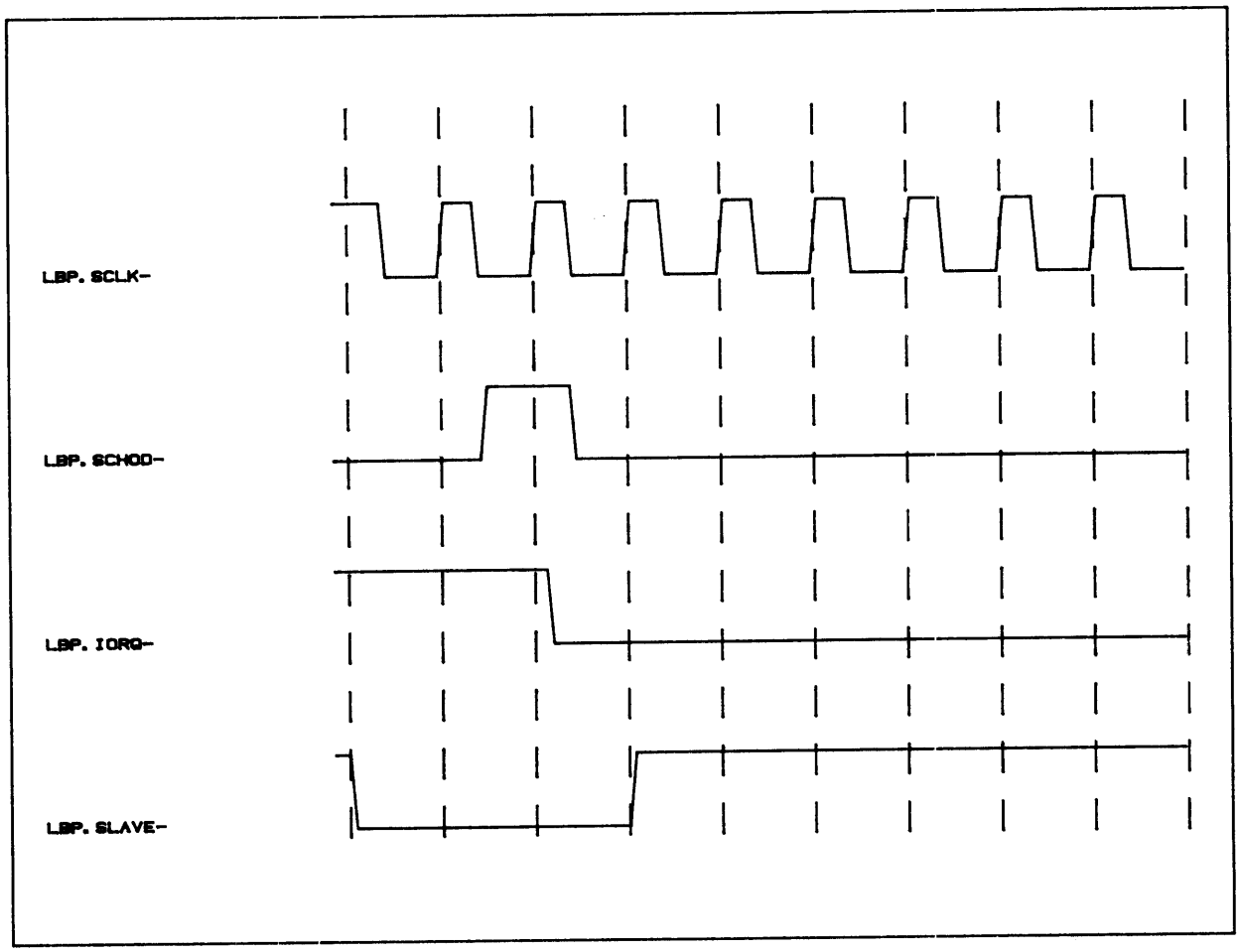


Figure 9-9. Slave Handshake

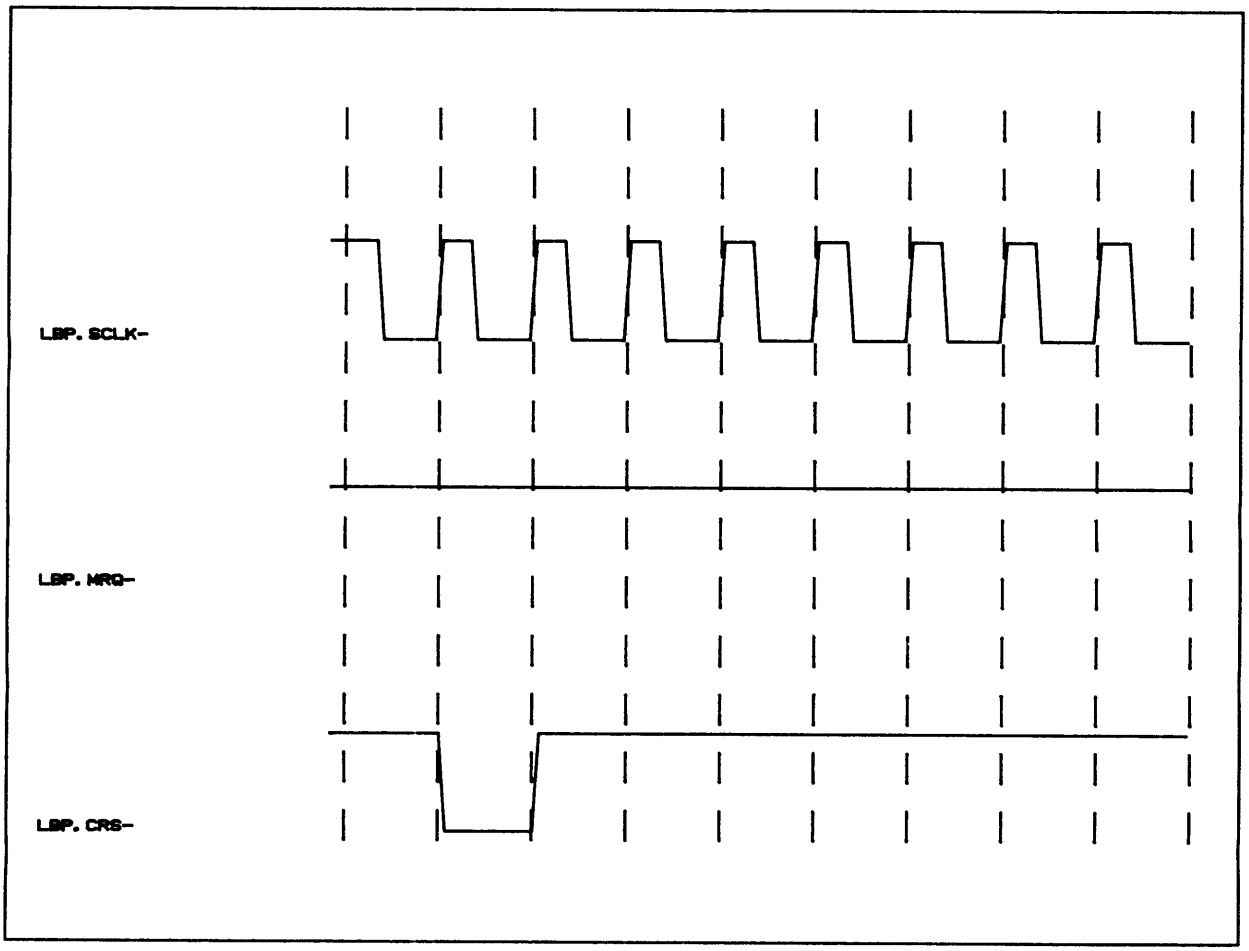


Figure 9-10. Reset Operation

9.7 Theory of Operation

The I/O Interface theory of operation is covered in the following paragraphs. The schematic to be used for the I/O Interface is CA10 located at the rear of Chapter 5. The theory of operation for the macrointerrupt system is covered in Chapter 6 under the MC card, and the microinterrupt system is covered in Chapter 3.

The IC packages (chips) are referenced by both U-numbers and schematic locations. For example U0406 (CA102A) refers to part U0406 on the cache card in row 4/column 6, which is shown on schematic page CA10 at horizontal location 2 and vertical location A.

9.7.1 I/O Interface

Except for the slave mode acknowledge signal (SCHOD), all of the I/O interface is shown on page CA10. The PLA U1005 (CA103B) does all of the DMA handshaking, U1308 (CA103C) generates timing signals for the other I/O handshakes, and U1608 (CA103D) drives most of the other I/O handshakes. The terms SHC and LHC refer to the Short Half Cycle (asserted SCLK-) and Long Half Cycle (deasserted SCLK-) respectively. The signal CA.SHC.2B+ (which causes CA.SHC+) is produced by the flip-flop U0405 (CA103E) which is clocked by an inverted form of the processor clock. This allows sampling of LBP.SCLK- where it is safe from setup or hold time problems due to backplane loading skews. The resulting signal, CA.SHC+, is used to decide when to assert signals.

All signals driven by the CA card are driven from processor clock edges; not LBP.SCLK- edges.

9.7.2 Direct Memory Access (DMA)

DMA covers not only true DMA accesses, but also any other coprocessor which makes memory requests across the I/O backplane without driving MRQ. Such a device must remove its MEMGO if CPUTURN was asserted. If there was such a device, it would be treated the same as I/O DMA.

The PLA equations for DMA are shown in Figure 9-11. Figure 9-12 shows two back-to-back DMA read cycles. The first read hits the cache and the second one misses. Note that in both cases the access is a so called three-cycle handshake. By the time the cache knows whether or not it had the correct data (hit), it is already too late to assert VALID for a two-cycle handshake.

```
*                                                                  B
*       C       C                                                  P     C
*       A       A                                      C C         .     A C
*       .       .                                      C A A       L       . A
*       D     C D                    L               A . .       D L C D .
*       M C   A M                  L B               . L V     L O B A M H
*       A A   . A                  B P               D D A     B U P . A O
*       . . C D .                  P . C             M O L     P T . D . L
*       E V A M C C C C . V A A U .                            . . V M P D
*       A A . A Y A A A B A . . T B                            B B A A D .
*       R L D . C . . . U L S W . U                            U O L . . W
*       L I M P L F F F S I H R E S                            S T I 2 2 R
*       Y D A D E 1 2 3 Y D C T N Y                            Y H D B B T
*       + - + + - + + + - - + + + +                            - - - + + -
*       0 0 0 0 0 0 0 0 1 1 1 1 1 0                            1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 9 7 3 2 1 9                            9 8 7 6 5 4
*
 SENSE:                                                        L L L H H L
*                                  B B B B B B                 B B B B B B
*ROW    7 6 5 4 3 2 1 0 9 7 3 2 1 0                            9 8 7 6 5 4
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - - - - - - - H H - -                            . . . . . A   HOLD DURING SHC
   1    - - - - - - - - L - - H - -                            . . . . . A   HOLD IF STILL BUSY
   2    - - - H - - - - - - - - - -                            A . . . . .   WAITING FOR CACHE
   3    - - H - - - - - - - - - - -                            A . . . . .   NOT DONE YET
   4    - - - - - - - - - - - - - H                            A . . . . .   OTHER IO HANDSHAKES
   5    - - - - L - L L - - - H - -                            A . . . . .   UNTIL WRITE DONE
   6    - L - - - - - - - - - L - -                            . A . . . .   DRIVE DMA READ DATA
   7    - - - - - - - - - - - - H -                            . A . . . .   OTHER IO HANDSHAKES
   8    - - - - - - - - - - - - - H                            . . A . . .   OTHER IO HANDSHAKES
   9    - - H - - - - - - - - H - -                            . . A . . .   WRITE HIT OR MISS
  10    - - H L H - - - - - H L - -                            . . A . . .   READ HIT
  11    - - - - L - H - - - H L - -                            . . A . . .   READ NORMAL
  12    - - - - L - - H - - H L - -                            . . A . . .   READ DELAYED CYCLE
  13    - - H - - - - - - L - - - -                            . . A . . .   GLITCH REMOVER
  14    - L H - - - - - - - - - - -                            . . A . . .   HOLD FOR 2ND HALF
  15    H - - - - - - - - - - - - -                            . . . A A .   NEW REQUEST
  16    - - - H H - - - - - - - - -                            . . . . A .   UNTIL CACHE STARTS
  17    - - H - - - - - - - H - - -                            . . . A . .   ALWAYS A FULL CYCLE
  18    - H H - - - - - - - - L - -                            . . . A . .   READ MISS
  19    - - H - L - - L - - - L - -                            . . . A . .   READ HIT
  20    - - - - L - - L - - - H - -                            . . . . . A   HOLD WRT FOR CACHE
  D4    - - - - - - - - - - - - - -                                      ^
  D5    - - - - - - - - - - - - - -                                    ^
  D6    - - - - - - - - - - - - - -                                  ^
  D7    - - - - - - - - - - - - - -                                ^
  D8    - - - - - - - - - - - - - -                              ^
  D9    - - - - - - - - - - - - - -                            ^
```

Figure 9-11. Coding for DMA Control PLA (CA Card)

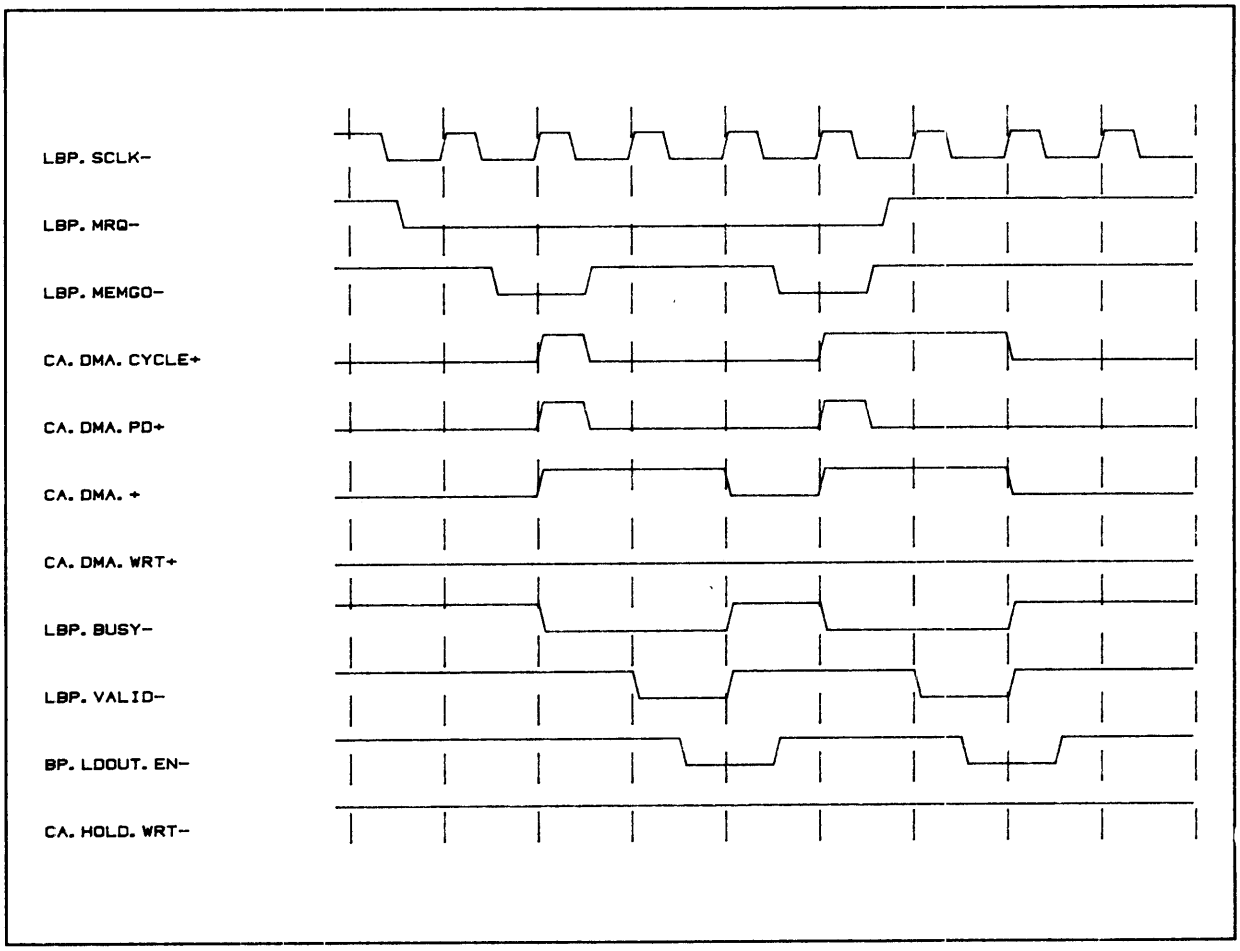


Figure 9-12. DMA Read Cycle

All DMA requests start by asserting the signal CA.DMA.EARLY+, which is produced by the gate U0406 (CA102A). This gate ANDs the following: MEMGO has been asserted, REMEM (remote memory) is not asserted, the MEMGO did not come from another I/O handshake (CA.DISABLE+), it occurs during the LHC of an SCLK (to avoid getting the request too early in a slow clock situation and violating hold times), and BUSY is not asserted (which turns CA.DMA.EARLY+ off so multiple cache cycles are not started). Signal CA.DMA.EARLY+ is fed through OR gate U0905 (CA107A) to produce the DMA cache request signal (CA.DMA.REQ+).

The other OR gate U0905 input is a pending DMA request; i.e., a DMA request that came earlier, but still has not been handled. This signal stays one cycle too long and so the cache arbitration logic has to ignore a DMA request if the present cycle is a DMA cycle and the cache hits. (Misses will allow enough time for the signal to be cleared.)

The signal CA.DMA.PD+ records that a DMA request has come in, but the cache has not serviced it yet. The signal CA.DMA.CYCLE- comes from the cache state machine when the present cache cycle is on behalf of DMA. The signal CA.DMA+ also starts with the assertion of CA.DMA.EARLY+ and stays around until LBP.VALID- has been asserted. LBP.VALID- is asserted immediately for writes and when the data is ready for reads.

Figure 9-13 shows back-to-back DMA write cycles. The first write cycle hits the cache and the second and third ones miss. In all three cases, the accesses are two cycle handshakes. This can be done for write requests since no data needs to be sent back to the IOCs (IO chips) and thus LBP.VALID- can be asserted immediately. If the cache is slow in handling the request, LBP.BUSY- is used to hold off more DMA requests. BUSY needs only to be released just before another LBP.MEMGO- is asserted (by a SHC.). The signal CA.HOLD.WRT- keeps the CA.DMA.WRT+ flip-flop, U0405 (CA105E) asserted until the present DMA request is finished. The PLA could not be used for generating the write signal because LBP.WE- comes too late relative to processor clocks.

Figure 9-14 shows the cases of both DMA read and write cycles which did not get started immediately. Note that in the write cycle case (the second request), VALID is asserted even before the cache has selected the DMA cycle. BUSY is important for holding off another request.

9.7.3 Broadcast I/O (BCIO)

Figure 9-15 shows an I/O instruction broadcast for the I/O backplane. Several signals are common in this and the other I/O handshakes. The signals CA.IO.S0-2+ are timing signals for the handshakes.

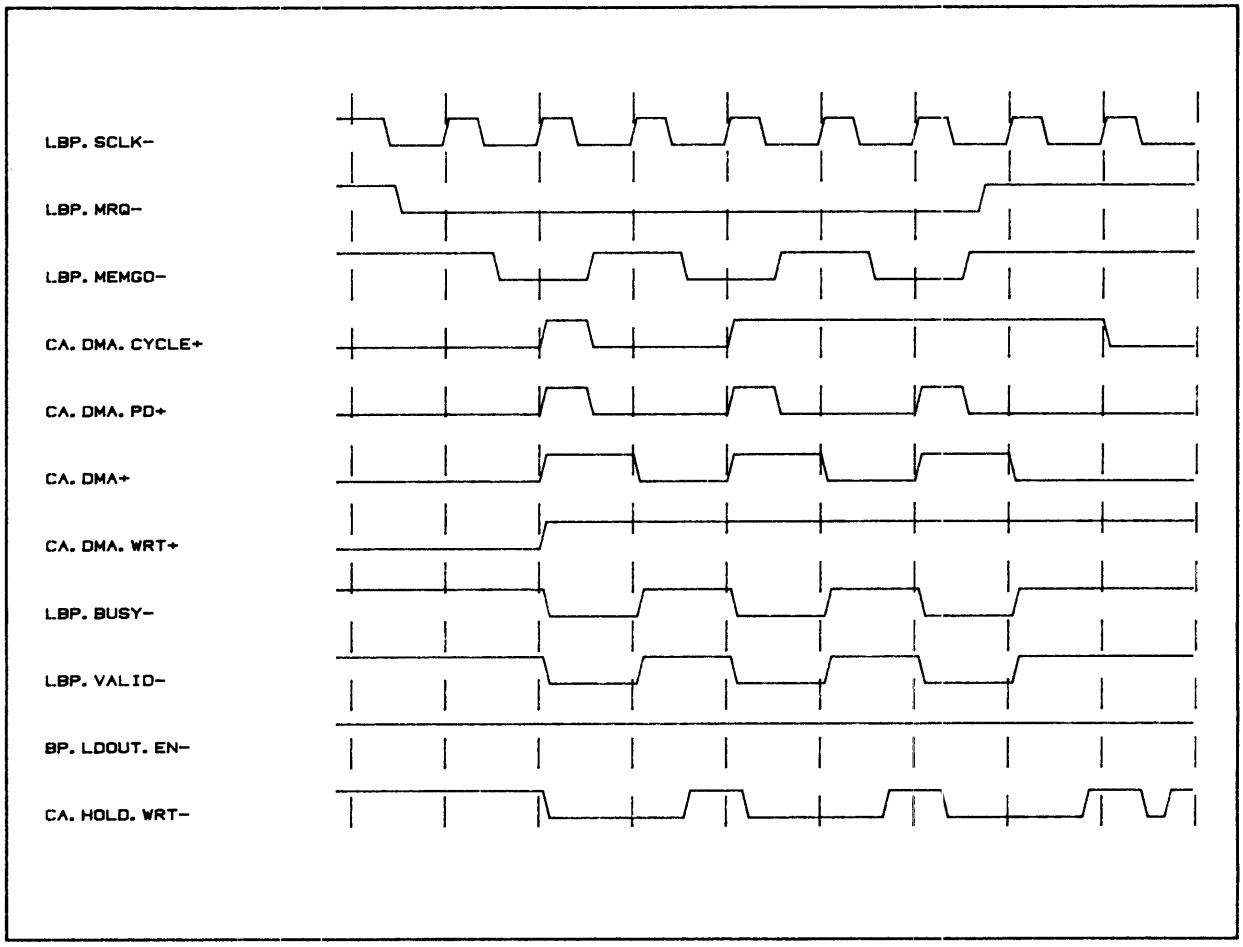


Figure 9-13. DMA Write Timing

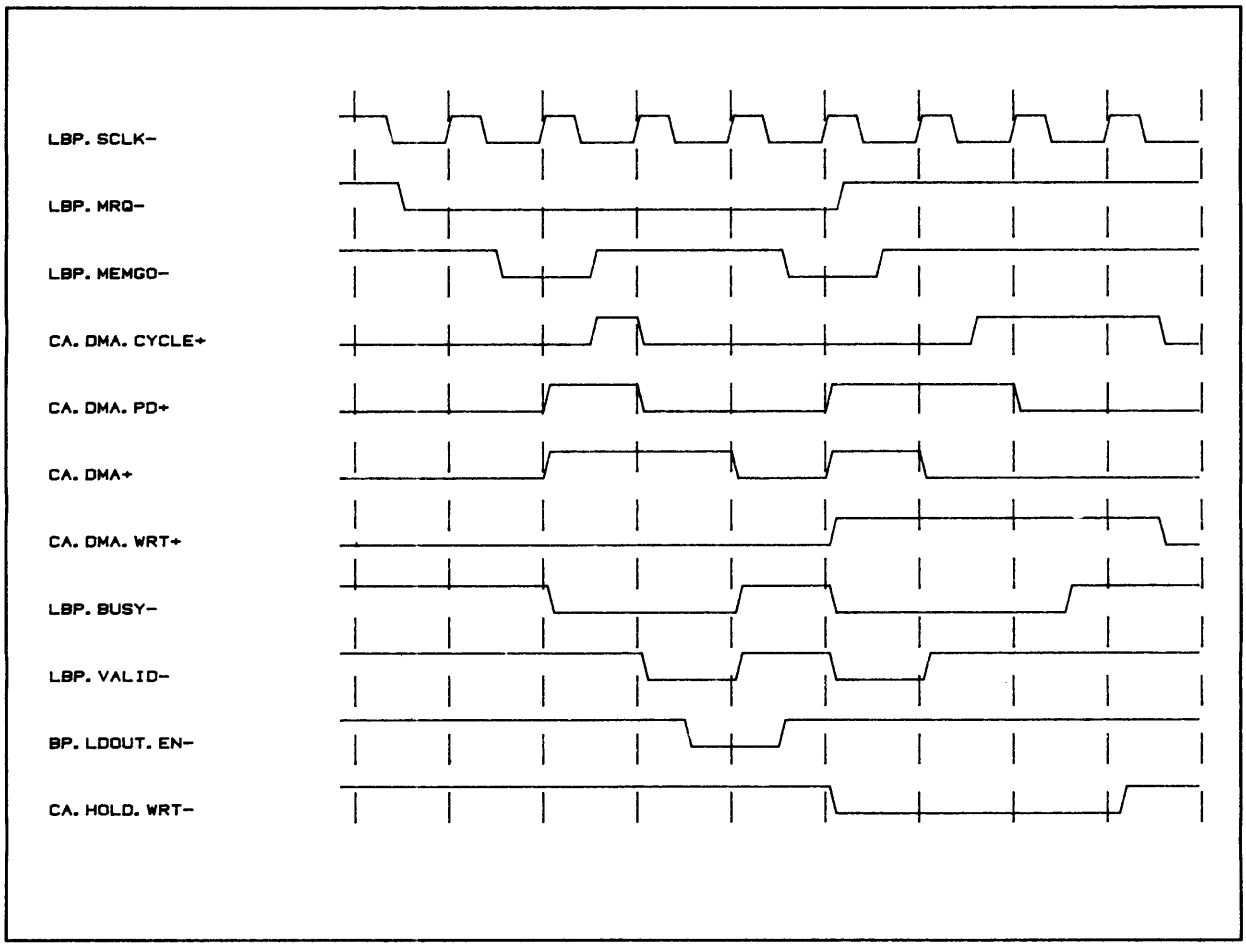


Figure 9-14. Delayed DMA Timing

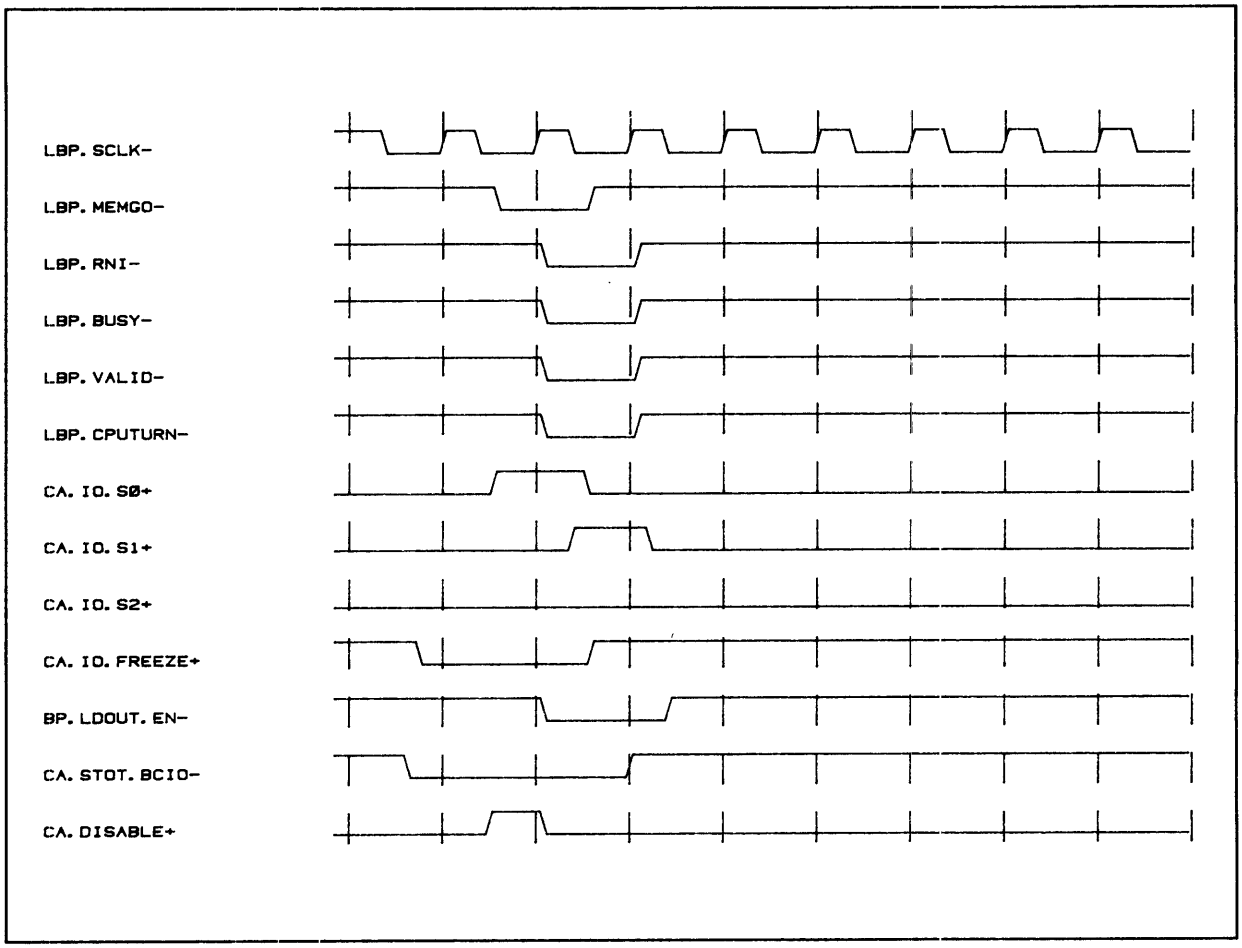


Figure 9-15. Broadcast I/O Handshake Timing

CA.IO.S0+ comes true during the LHC if a request has been posted by the CPU and no DMA is in process (LBP.BUSY- false.) If LBP.MRQ- is also not asserted during the LHC, then CA.IO.S0+ will remain true until the requested I/O handshake is completed. Likewise, timing signals CA.IO.S1+ and CA.IO.S2+ will follow if CA.IO.S0+ stays true. If LBP.MRQ- is asserted, then CA.IO.S0+ goes false and the I/O handshake waits until the DMA request is completed (but keeps trying).

The signal LBP.CPUTURN- is asserted whenever the CPU has posted an I/O handshake request and the request has been held off by DMA (BP.MRQ-); i.e., CA.IO.S0+ did not stay true. This is so that if the I/O backplane is saturated with DMA, the CPU will still continue to process and not halt when the first CPU I/O handshake request is placed. The signal CA.CPU.FREEZE+ is asserted when an I/O handshake request is posted and continues until the proper time for the CPU to continue.

The description in the above paragraph is true of all of the I/O handshake cycles. However, for Broadcast I/O, the I/O states S0, S1 and S2 are handled differently. The signal LBP.BUSY- stops the state machine and thus S0-S2 go away before the entire cycle has completed. These signals are not needed for the last part of the handshake and so this is not any real problem.

For the BCIO operation, LBP.CPUTURN- is kept asserted until the end of the operation. This makes sure the I/O masters are ready to look at the macroinstruction just "fetched". LBP.MEMGO- is asserted for when an analysis interface is used. CA.DISABLE+ is asserted just before LBP.MEMGO- in order to stop the DMA PLA from thinking it has a DMA request.

Figure 9-16 shows the coding of the I/O timing PLA that generates the timing signals and Figure 9-17 shows the coding of the I/O control PLA which generates most of the other signals. Signals which end in .2B+ are inputs to a "D" type flip-flop. In particular, LBP.BUSY- and LBP.VALID- are driven by the DMA PLA and so the signal CA.VAL.BUSY+ requests both to be asserted. Likewise, CA.LDOUT.EN.2B+ asks the DMA PLA to enable the LDOUT latch to be driven onto the I/O backplane.

9.7.4 IOGO Read

Figure 9-18 shows an IOGO read cycle followed by an IOGO write cycle. In both cases, the PLAs just count for three SCLK periods before releasing LBP.IOGO-. This means that no device can use other than a three cycle IOGO handshake. (It cannot be faster due to definition and to be any slower would degrade LIA/OTA times even more.) The CPU is unfrozen just in time to read the LBP.DB+ for the desired data or control information.

9.7.5 IOGO Write

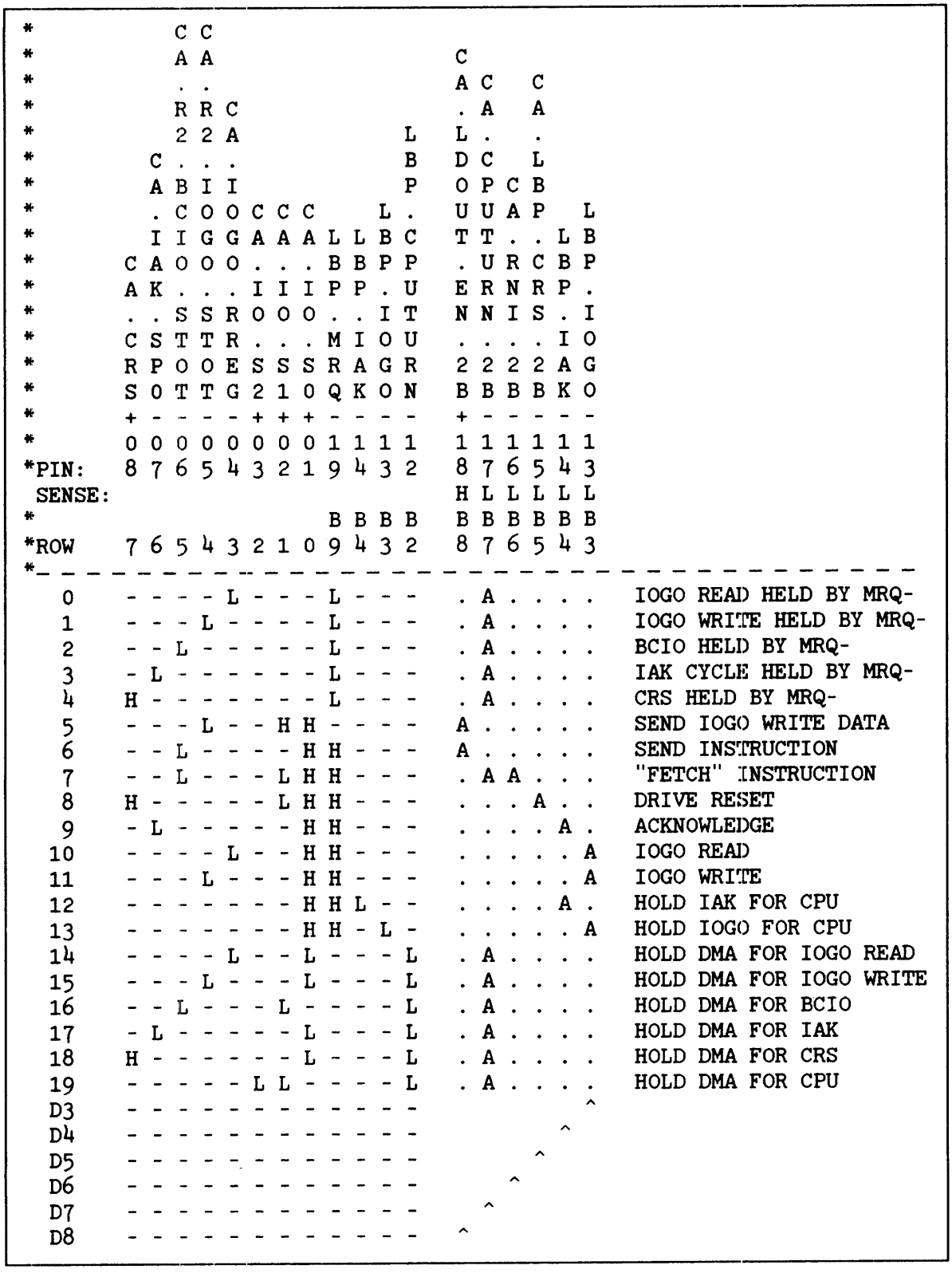
Figure 9-14 also shows an IOGO write operation. Data from the CPU's TBUS is driven onto the LBP.DB+ for the last two SCLKs of the IOGO operation. The CPU is frozen longer in an IOGO write operation in order to keep the LBP.DB+ valid longer.

```
*            C C
*            A A                              C
*            . .                          C   A
*            R R C                        A   . C
*            2 2 A                        . C C C V A
*          C . . .                        D A A A A .
*          A B I I               L      L I . . . L I
*          . C O O C C C       L B      B S I I I . O
*          I I G G A A A L     B P      P A O O O B .
*        C A O O O . . . B C P .        . B . . . U F
*        A K . . . I I I P A . M        M L S S S S R
*        . . S S R O O O . . B E        E E 2 1 0 Y E
*        C S T T R . . . M S U M        M . . . . . E
*        R P O O E S S S R H S G        G 2 2 2 2 2 Z
*        S O T T G 2 1 0 Q C Y O        O B B B B B E
*        + - - - - + + + - + - -        - + + + + + -
*        0 0 0 0 0 0 0 0 1 1 1 1        1 1 1 1 1 1 0
*PIN:    8 7 6 5 4 3 2 1 9 8 7 6        6 5 4 3 2 1 9
 SENSE:                                 L H H H H H L
*                        B B B B        B B B B B B B
*ROW     7 6 5 4 3 2 1 0 9 8 7 6        6 5 4 3 2 1 0
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
```

Figure 9-16. I/O Timing PLA Coding (CA Card) (Sheet 1 of 2)

```
*ROW    7 6 5 4 3 2 1 0 9 8 7 6   6 5 4 3 2 1 0
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
  0     - - - - L - - - - H H -   . . . . A . .   IOGO READ START S0
  1     - - - L - L - - - H H -   . . . . A . .   IOGO WRITE START S0
  2     - - L - - - - - - H H -   . . . . A . .   BROADCAST START S0
  3     - L - - - - - - - H H -   . . . . A . .   IAK START S0
  4     H - - - - - - - - H H -   . . . . A . .   LIO RESET START S0
  5     - - - - - - - H H L - -   . . . . A . .   HOLD S0
  6     - - - - - - - H - H - -   . . . A . . .   START S1
  7     - - - - - - H H - L - -   . . . A . . .   HOLD S1
  8     - - - - - - H - - H - -   . . A . . . .   START S2
  9     - - - - - H - H - L - -   . . A . . . .   HOLD S2
 10     - - - - L L - - - - - -   . . . . . . A   UNTIL DATA READY
 11     - - - L - L - - - - - -   . . . . . . A   KEEP IOGO SIGNAL
 12     - - - L - - - - - L - -   . . . . . . A   MAINTAIN TBUS DATA
 13     - - L - - - L - - - - -   . . . . . . A   KEEP CPUTURN ON
 14     - L - - - - L - - - - -   . . . . . . A   HOLD UNTIL IAK ON
 15     - L - - - - - - - - H -   . . . . . . A   WAIT FOR "DATA"
 16     H - - - - - L - - - - -   . . . . . . A   WAIT FOR RESET
 17     - - L - - - L H H - - -   . . . . . A .   BCIO VALID/BUSY
 18     - L - - - - H H - L - L   . . . . . A .   IAK VAL/BUSY & LHC
 19     - L - - - - H - - - - -   . A . . . . .   IGNORE IAK MEMGO
 20     - - L - - - - - H H H -   . A . . . . .   IGNORE BCIO MEMGO
 21     - - - - - - - - - - - -   A . . . . . .   ALWAYS TRUE
 22     L H H H H - - H H H L -   . . . . . A .   HOLD IAK VAL/BUSY
 D0     - - - - - - - - - - - -                 ^
 D1     - - - - - - - - - - - -                 ^
 D2     - - - - - - - - - - - -                 ^
 D3     - - - - - - - - - - - -                 ^
 D4     - - - - - - - - - - - -                 ^
 D5     - - - - - - - - - - - -                 ^
 D6     - - L - - - L H H - - -   ^                 BCIO MEMGO
*
```

Figure 9-16. I/O Timing PLA Coding (CA Card) (Sheet 2 of 2)



```
*           C C                                 C
*           A A                                 A C   C
*           . .                                 . A   A
*           R R C                               . A   A
*           2 2 A                           L   L .   .
*         C . . .                           B   D C   L
*         A B I I                           P   O P C B
*         . C O O C C C     L .             U U U A P   L
*         I I G G A A A L L B C             T T . . L B
*       C A O O O . . . B B P P             . U R C B P
*       A K . . . I I I P P . U             E R N R P .
*       . . S S R O O O . . I T             N N I S . I
*       C S T T R . . . M I O U             . . . . I O
*       R P O O E S S S R A G R             2 2 2 2 A G
*       S 0 T T G 2 1 0 Q K O N             B B B B K O
*       + - - - - + + + - - - -             + - - - - -
*       0 0 0 0 0 0 0 0 1 1 1 1             1 1 1 1 1 1
*PIN:   8 7 6 5 4 3 2 1 9 4 3 2             8 7 6 5 4 3
 SENSE:                                     H L L L L L
*                         B B B B           B B B B B B
*ROW    7 6 5 4 3 2 1 0 9 4 3 2             8 7 6 5 4 3
*- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   0    - - - - L - - - L - - -   . A . . . .   IOGO READ HELD BY MRQ-
   1    - - - L - - - - L - - -   . A . . . .   IOGO WRITE HELD BY MRQ-
   2    - - L - - - - - L - - -   . A . . . .   BCIO HELD BY MRQ-
   3    - L - - - - - - L - - -   . A . . . .   IAK CYCLE HELD BY MRQ-
   4    H - - - - - - - L - - -   . A . . . .   CRS HELD BY MRQ-
   5    - - - L - - H H - - - -   A . . . . .   SEND IOGO WRITE DATA
   6    - - L - - - - H H - - -   A . . . . .   SEND INSTRUCTION
   7    - - L - - - L H H - - -   . A A . . .   "FETCH" INSTRUCTION
   8    H - - - - - L H H - - -   . . . A . .   DRIVE RESET
   9    - L - - - - - H H - - -   . . . . A .   ACKNOWLEDGE
  10    - - - - L - - H H - - -   . . . . . A   IOGO READ
  11    - - - L - - - H H - - -   . . . . . A   IOGO WRITE
  12    - - - - - - - - H H L - -   . . . . A .   HOLD IAK FOR CPU
  13    - - - - - - - - H H - L -   . . . . . A   HOLD IOGO FOR CPU
  14    - - - - L - - L - - - L   . A . . . .   HOLD DMA FOR IOGO READ
  15    - - - L - - - L - - - L   . A . . . .   HOLD DMA FOR IOGO WRITE
  16    - - L - - - L - - - - L   . A . . . .   HOLD DMA FOR BCIO
  17    - L - - - - - L - - - L   . A . . . .   HOLD DMA FOR IAK
  18    H - - - - - - L - - - L   . A . . . .   HOLD DMA FOR CRS
  19    - - - - - L L - - - - L   . A . . . .   HOLD DMA FOR CPU
  D3    - - - - - - - - - - - -                 ^
  D4    - - - - - - - - - - - -               ^
  D5    - - - - - - - - - - - -             ^
  D6    - - - - - - - - - - - -           ^
  D7    - - - - - - - - - - - -         ^
  D8    - - - - - - - - - - - -       ^
```

Figure 9-17. I/O Control PLA Coding (CA Card)

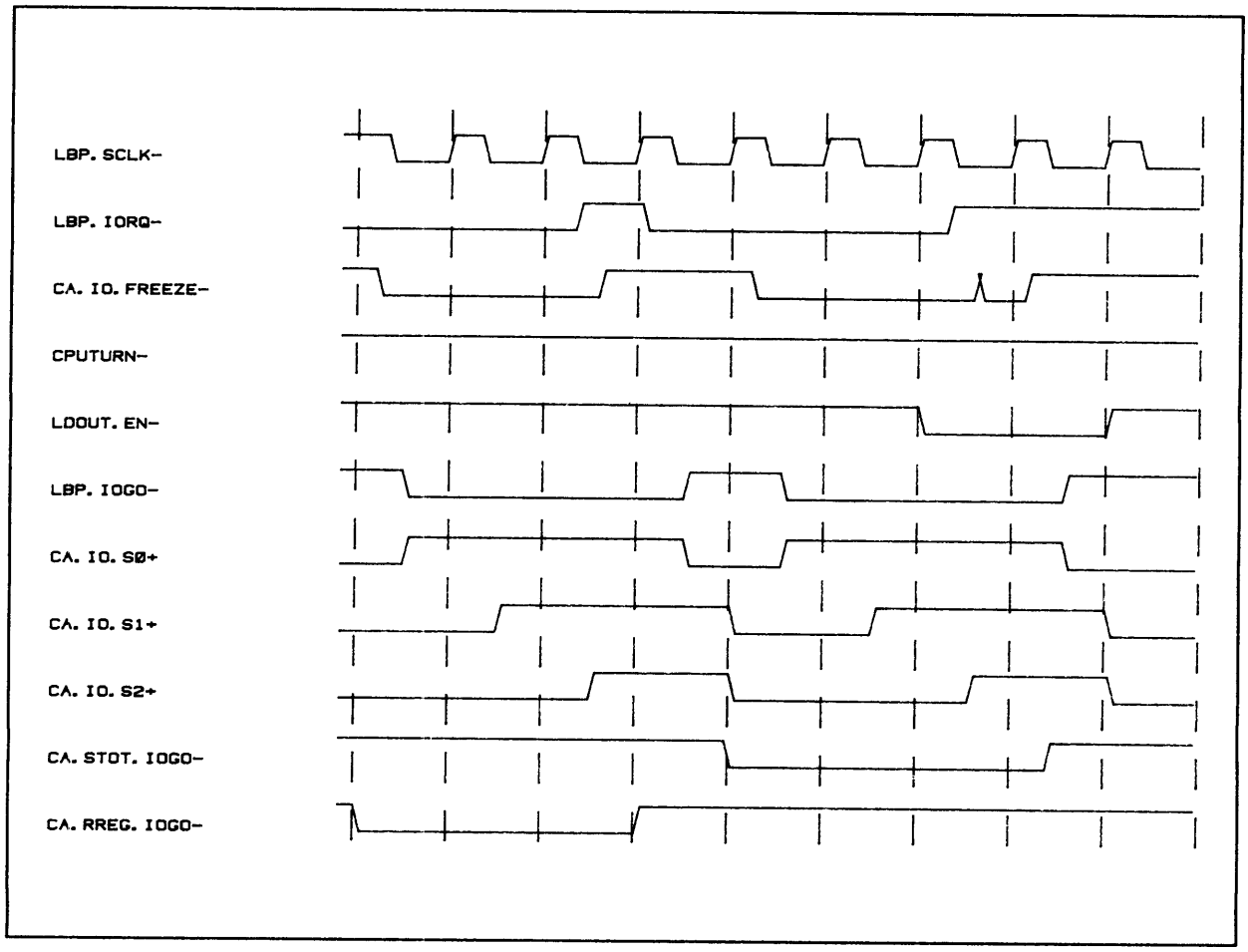


Figure 9-18. IOGO Handshake Timing

9.7.6 IAK

Figure 9-19 shows an interrupt acknowledge handshake. Once a LHC occurs without LBP.MRQ- being asserted, LBP.IAK- is asserted until some I/O master responds with LBP.MEMGO- (CPUTURN is also asserted). It is important that an IAK request not be made unless some card is requesting an interrupt, otherwise the processor will stop. Again, the CPU is unfrozen when the select code (BP.AB+) is in the cache address register (MADR). The CPU gets the select code from the backplane because it is driven onto the address bus, which is the default selection of the MEM field. This allows the CPU to read it by coding RREG/MADR in the same line as SP0/IAK. To read the select code, the MEM field should have NOP coded. NOP actually selects the I/O address latch.

9.7.7 Other Handshakes

Figure 9-20 shows a CRS reset for the I/O backplane. LBP.CRS- is only asserted for one SCLK- period. Keeping CA.CRS+ asserted in the Cache Control Register (CCR) will NOT cause BP.CRS- to be asserted for additional SCLK periods.

The slave acknowledge signal (LBP.SCHOD-) is deasserted to acknowledge a slave request by flip-flop U0805 (MC124A) on the MC board. Its input comes from the Memory Control Register (MCR.) Since slave acknowledge can be done independent of DMA, the CPU can directly drive the SCHOD signal by turn-off freezes in the cache (a CCR bit) and then deasserting SCHOD for two CPU cycles (one SCLK period.)

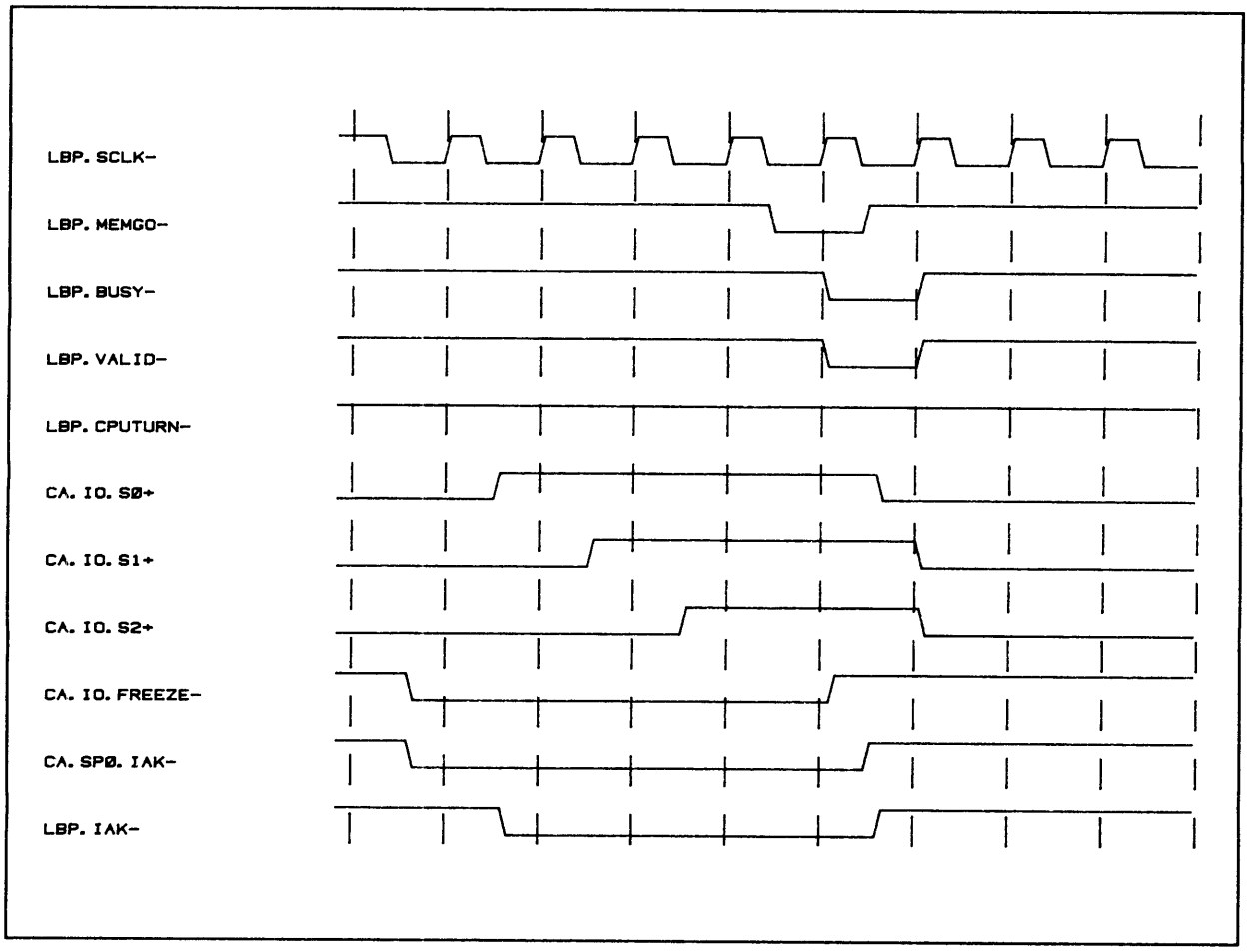


Figure 9-19. IAK Handshake Timing

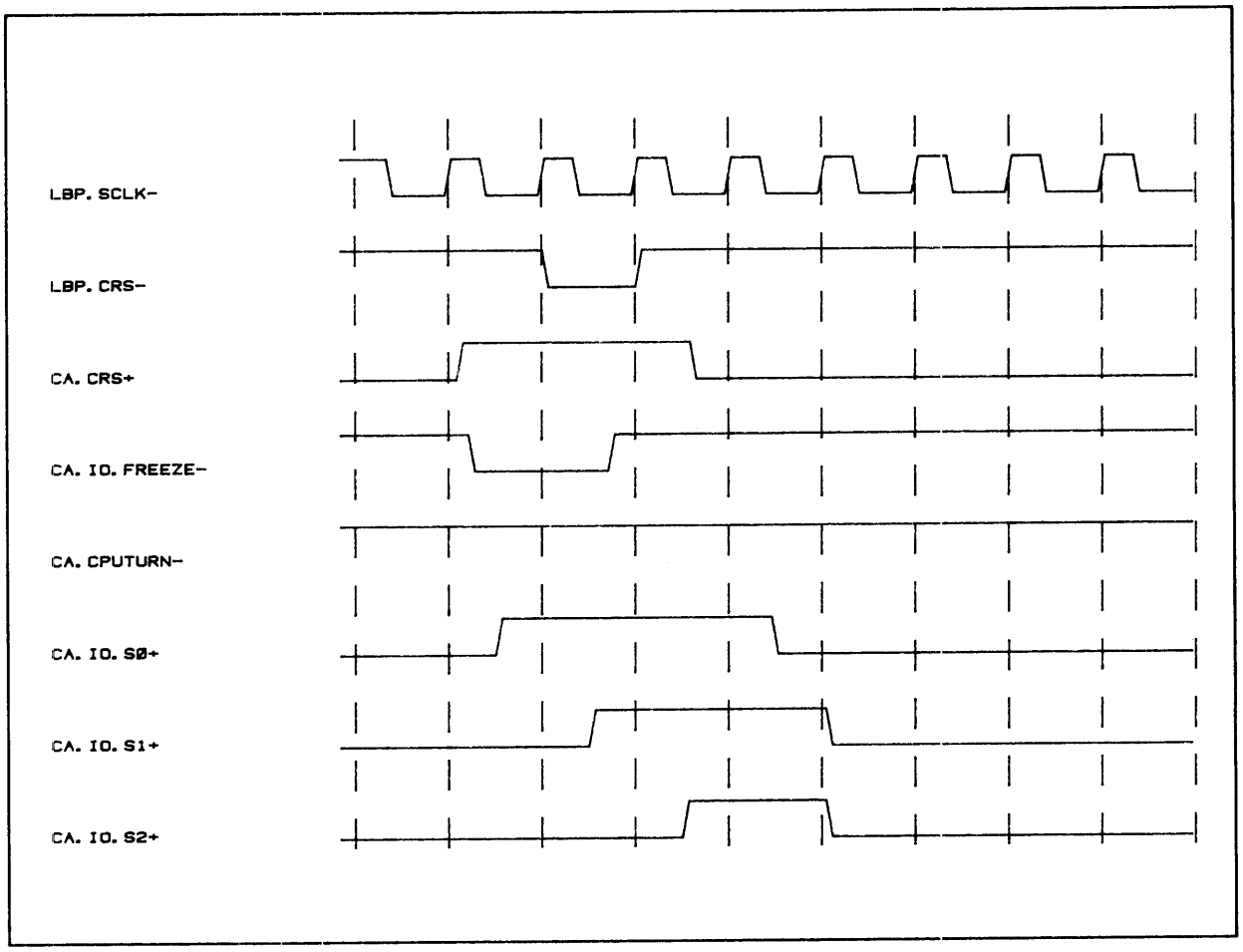
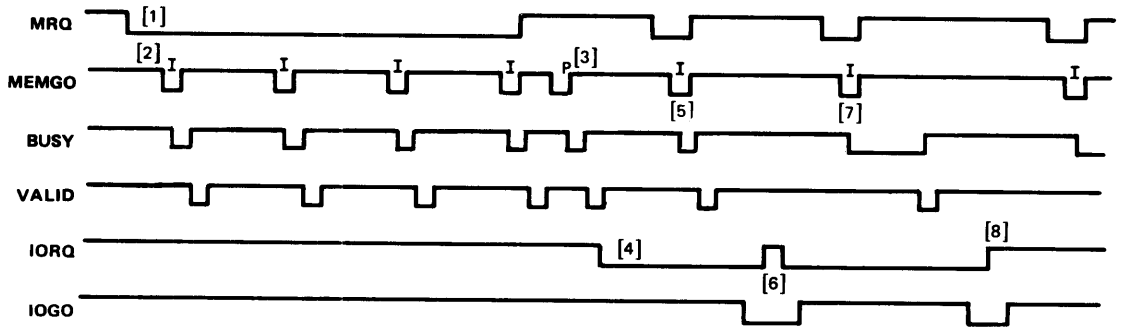


Figure 9-20. CRS Handshake Timing

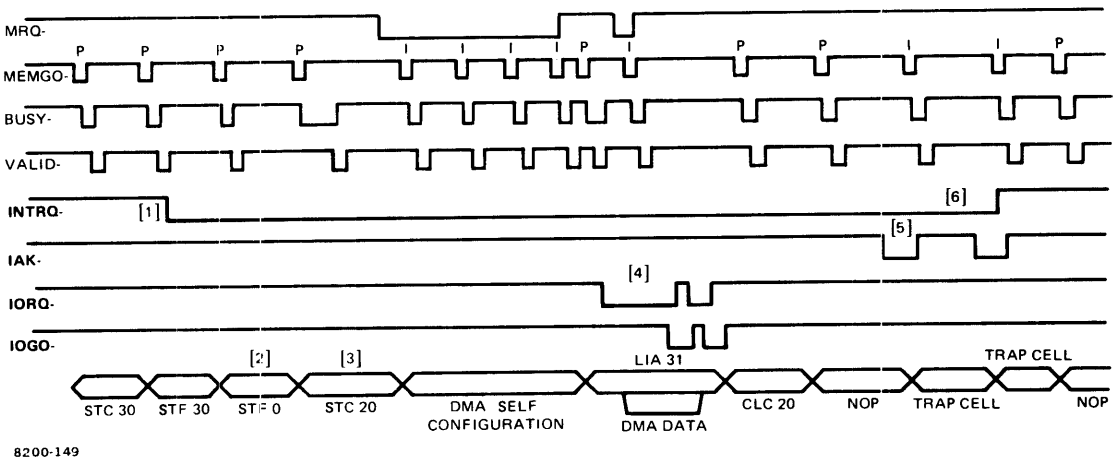
9.7.8 Interactive Timing Examples

Previous timing examples have shown handshakes or protocols by type of interaction. In actuality, however, transactions may start only to be preempted by other higher priority transactions and held off for an indefinite period of time. Figures 9-21 and 9-22 show various transactions over the backplane which begin, are preempted, and then later are allowed to complete.



1. MRQ- is held asserted for 21C during a four-word self-configuration.
2. All assertions of MEMGO- are labeled with their source; P for processor, I for I/O Master.
3. The processor fetches an LIA instruction.
4. The I/O Master asserts IORQ- upon recognition of the LIA, but the processor is held off from responding by [5].
5. The first actual DMA data transfer takes place.
6. The first half of the I/O instruction handshake can now complete.
7. The second DMA data transfer takes place. It happened when memory was refreshing, so BUSY- is asserted for 5C instead of the usual 2C in order that the refresh can complete.
8. Now that this DMA transfer is complete, the I/O handshake can complete.

Figure 9-21. Interactive DMA and I/O Instruction Timing



1. The Flag and Control flip-flops are set, so the I/O Master attempts to interrupt.

2. Interrupt system is turned on with an STF 0 but processor must not respond until after the next instruction if current is an I/O instruction.

3. Self-configurating DMA is started, set up for a one-word transfer.

4. An LIA is executed, interleaved with DMA as in Figure 9-21.

5. After the NOP instruction is fetched, the processor can respond to the interrupt caused by Flag 30.

6. The I/O Master does not release INTRQ, because it now also has a DMA completion interrupt pending.

Figure 9-22. Interactive DMA, I/O Instruction, and Interrupt Timing

9.8 Signal Timing Specifications

The A900 cards can be categorized into three types for backplane timing: memory, processor with memory, and I/O Master. Each type of card has its timing requirements for the signals it receives and its timing guarantees for the signals it generates. In order to insure the basic integrity of all backplane interactions, it is necessary only to ascertain that all requirements are satisfied by the guarantees. All timing guarantees take into account the signal propogation delay due to line length and loading.

In Tables 9-3 through 9-30, timing specifications are given in terms of both requirements and guarantees. All backplane signals are listed in alphabetical order.

The definition of terms used in the timing specifications are provided below. All times are given in nanoseconds unless otherwise indicated.

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS

C - Cycle
One cycle of Slow Clock (SCLK).

f - Frequency
The number of cycles per unit time of a given signal.

I/O - I/O Master
The A-Series I/O Master consists of an I/O chip and some TTL logic which together performs all the backplane I/O interfacing functions.

LHC - Long Half Cycle
The Long Half Cycle refers to the time period when SCLK- is low.

P - Processor
This could be the cache for DMA operations or special logic for all other operations.

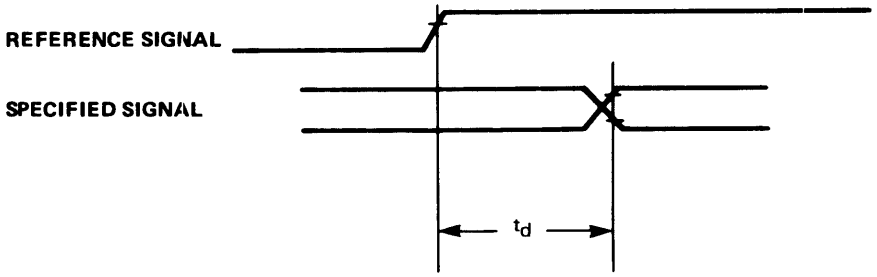
PS - Power Supply

SHC - Short Half Cycle
The Short Half Cycle is the time period when SCLK- is high.

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (Continued)

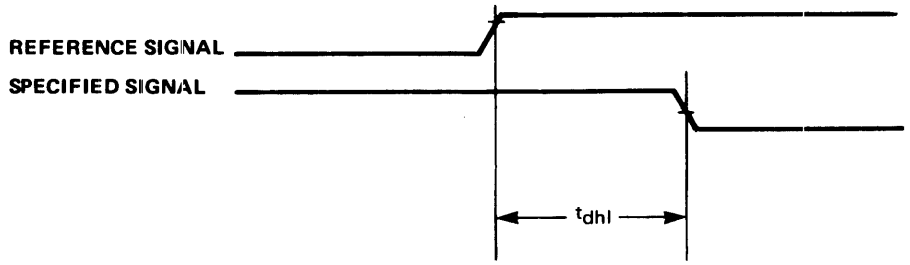
t_d - Delay time

The time interval from a signal edge used as a reference point to the point in time when the specified signal is guaranteed to be stable on the backplane.

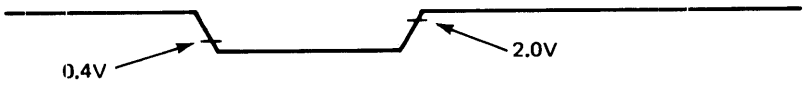


t_{dhl} - Delay time high to low

The time interval from a signal edge used as a reference point, to the point in time when the specified signal is guaranteed to be low if in fact it is going low.



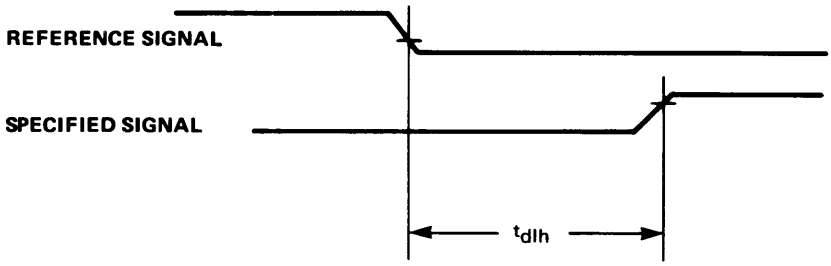
Note: In these timing diagrams, a high notch is 2.0 volts and a low notch is 0.4 volt as shown below.



DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (Continued)

t_{dlh} - Delay time low to high

The time interval from a signal edge used as a reference time to the point in time when the specified signal is guaranteed to be high if in fact it is going high.

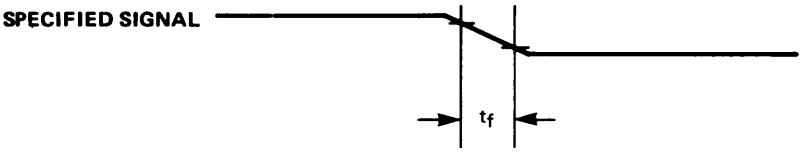


t_{dz} Delay time to high impedance

The time interval from a signal edge used as reference to the point in time when the specified signal will no longer be actively driven.

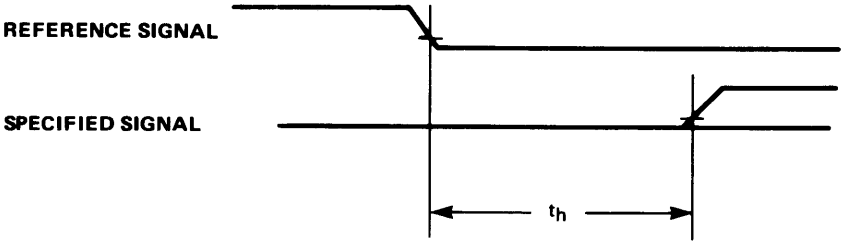
t_f - Fall time

The time interval during which a signal is in transition from high to low.



t_h - Hold time

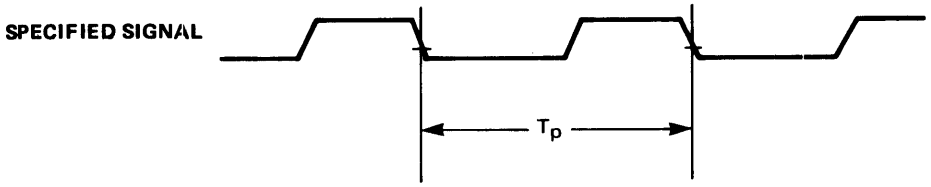
The period of time during which a specified signal must remain stable at its logic level after a certain reference edge.



DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (Continued)

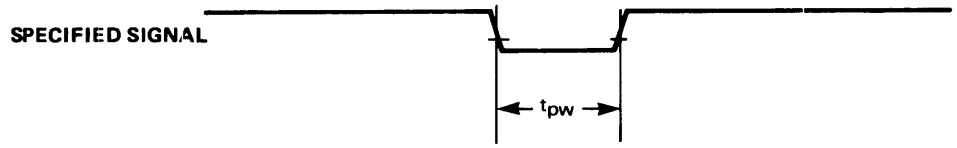
t_p - Period

The duration of one cycle of a periodic signal.



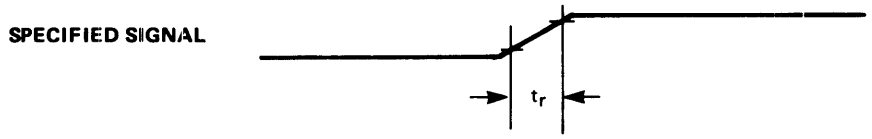
t_{pw} - Pulse width time

The time interval between the leading and trailing edge of a pulse. Specifically, for a normally high signal, tpw is the time when that signal is low. For a normally low signal, tpw is the time when that signal is high.



t_r - Rise time

The time interval during which a signal is in transition from low to high.



t_{su} - Set-up time

The time interval a specified signal must be at a stable logic level before a given edge of a reference signal.

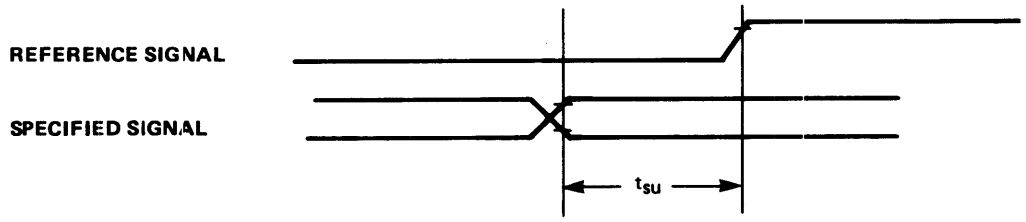


Table 9-3. Timing Specifications for AB0 - 14

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑	Edges that occur during MEMGO		M	85		
t_{h}	SCLK-↑	Edges that occur during MEMGO		M	-46		
t_{d}	SCLK-↓	Edge that causes MEMGO-↓	I/O				100
t_{h}	SCLK-↓	Edge that causes MEMGO-↑	I/O		0		

AE0 - AE4 ADDRESS EXTENSION BUS

This bus was previously called the select code bus SC0 - SC4. Refer to Table 9-24, Timing Specifications for SC0 - SC4.

Table 9-4. Timing Specifications for BUSY-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↑	Edge that occurs during MEMGO-	M		0		54
t_{dlh}	SCLK-↑		M		0		54
t_{su}	SCLK-↓	In order to hold off MEMGO-		I/O	5		
t_{h}	SCLK-↓			I/O	5		

Table 9-5. Timing Specifications for CCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
f	asynchronous	To all other backplane signals	P		14.7441 MHz	14.7456 MHz	14.7471 MHz
Duty cycle			P			50%	

Table 9-6. Timing Specifications for CPUTURN-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↑	That causes BUSY-↓	P				165
t_{dlh}	SCLK-↑		P				145
t_{su}	SCLK-↓	To inhibit MRQ-		I/O	25		
t_{h}	SCLK-↓	Same edge		I/O	-5		

Table 9-7. Timing Specifications for CRS-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{pw}				I/O	1C		
t_{su}	SCLK-↓			I/O	-30		
t_{dhl}	SCLK-↑	No concurrent DMA	P		5		20
t_{dhl}	SCLK-↑	End of DMA	P		5		20
t_{dlh}	Next SCLK-↑		P		5		20
t_{pw}			P		1C		

Table 9-8. Timing Specifications for DB0 - 15

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↓	Edge that causes MEMGO-↑ (DMA)		M	0		
t_{h}	SCLK-↓	Edge that causes MEMGO-↑		M	12		
t_{su}	SCLK-↑	That causes VALID-↑	M		50		
t_{h}	SCLK-↑	That causes VALID-↑	M		20		
t_{su}	VALID-↑	All cases	M		65		
t_{d}	SCLK-↓	Edge that causes MEMGO-↓ (DMA)	I/O				140
t_{h}	SCLK-↓	Edge that causes MEMGO-↑ (DMA)	I/O		35		
t_{d}	SCLK-↓	First SCLK-↓ after IOGO-↓* (I/O instruction)	I/O				315
t_{h}	SCLK-↑	Third SCLK-↑ during IOGO- (I/O instruction)	I/O		65		
t_{su}	VALID-↑	DMA read		I/O	50		
t_{h}	VALID-↑	DMA read		I/O	50		180
t_{su}	SCLK-↓	Second SCLK-↓* during IOGO- (I/O instr)		I/O	10		

Table 9-8. Timing Specifications for DB0 - 15 (Continued)

t_{su}	SCLK-↓	Second SCLK-↓ during IOGO- (I/O instruction*)	P	33	
t_h	SCLK-↑	Third SCLK-↑ during IOGO-	P	110	
t_{su}	SCLK-↑	That causes VALID-↑ (I/O instruction)	P	200	
t_h	SCLK-↓	after VALID-↑	P	11	
t_h	SCLK-↑	Third SCLK-↑* during IOGO- (I/O instruction)	I/O	40	250
*Provided IOGO-↓ met 10-ns set-up time to previous SCLK-↑.					

Table 9-9. Timing Specifications for IAK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑			I/O	10		
t_h	SCLK-↑	Same edge		I/O	25		
t_{pw}				I/O	2C		3C
t_{su}	SCLK-↓	To inhibit MRQ		I/O	25		
t_h	SCLK-↓	Same edge		I/O	0		
t_{su}	SCLK-↑	First after IAK-↓	p		71		
t_h	SCLK-↓	First after VALID-↓	P		27		

Table 9-10. Timing Specifications for ICHID-/ICHOD-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su} ICHID-	SCLK-↓	Second SCLK-↓* during IAK-		I/O	10		
t_{h} ICHID-	SCLK-↓	Third SCLK-↓* during IAK-		I/O	50		
t_{d}	Asynch-ronous	ICHID-↓ to ICHOD-↓	I/O			5	7.5
t_{dhl} ICHOD-	SCLK-↑	Edge that causes INTRQ-↓	I/O				200
t_{h} ICHOD-	IAK-↑	ICHOD- is held low during the entire assertion of IAK-	I/O		SHC		

Table 9-11. Timing Specifications for INTRQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↓		I/O				200
t_{dlh}	SCLK-↓	Third SCLK- after IAK-↓*	I/O				300
t_{su}	SCLK-↓			P	none (asynchronous)		

*Provided IAK- met 10-ns set-up time to previous SCLK-↑.

Table 9-12. Timing Specifications for IOGO-

PARAMETER	REFERENCE	NOTES	BY	BY	MIN	TYP	MAX
t_{su}	SCLK-↑	During IORQ-		I/O	10		
t_h	SCLK-↑	Same edge		I/O	25		
t_{pw}		3↑ of SCLK-		I/O	2C + LHC		
t_{su}	SCLK-↓	To inhibit MRQ		I/O	25		
t_h	SCLK-↓	Same edge		I/O	0		
t_{su}	SCLK-↑		P		65		
t_h	SCLK-↓	3rd SCLK-↓ after IOGO-↓	P		27		

Table 9-13. Timing Specifications for IORQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dh11}	Data bus valid during VALID-*	1 refers to first handshake request after RNI-↓	I/O				325
t_{dh12}	SCLK-↓	2 refers to second SCLK-↓ after** IOGO-↓ (double handshake only)	I/O				145
t_{dh13}	SCLK-↑	SCLK-↑ following SCHID-↑ (3 refers to initial IORQ-↓ on slave cycle)	I/O				45
t_{dlh}	SCLK-↓	First SCLK-↓ after IOGO-↓**	I/O				210

* During VALID-, there could be false assertions of IORQ- due to the data bus being in transition. This will not affect system operation, however, because the processor does not check IORQ- until two states after RNI-↑ when IORQ- is guaranteed to be valid.

** Provided IOGO-↓ met 10-ns set-up time to previous SCLK-↑.

Table 9-14. Timing Specifications for MCHID-/MCHOD-, MCHODOC-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su} MCHID-	SCLK-↓			I/O	5		
t_{h} MCHID-	SCLK-↓	Same edge		I/O	20		
t_{dhl}		MCHID-↓ to MCHOD-↓	I/O			5	7
t_{dhl} MCHOD-	SCLK-↓	Edge that causes MRQ-↓	I/O				30
t_{dhl} MCHODOC-	SCLK-↓	Edge that causes MRQ-↓	I/O				55
t_{dlh} MCHODOC-	SCLK-↓	Edge that causes MRQ-↑	I/O				165

Table 9-15. Timing Specifications for MEMGO-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑			M	50		
t_{h}	SCLK-↑	Same edge		M	-10		
t_{dhl}	SCLK-↓		I/O				45
t_{dlh}	SCLK-↓	Next edge	I/O		30		110

Table 9-16. Timing Specifications for MLOST-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME MIN	TYP	MAX
t_r, t_f			BB				50 ns
t_{su}	PON+↑		BB		500		us
t_h	PON+↑		BB		10 ms		1 s
t_h	PON+↑		SW*		5 ms		

* Processor does not latch MLOST-. During the pretest, the state of this line is used by the software to determine whether or not to initialize memory.

Table 9-17. Timing Specifications for MP+

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	VALID-↑			I/O	0		
t_h	SCLK-↑	Second SCLK-↑ after VALID-↑ (non-I/O instr). Second SCLK-↑ after last IOGO↑ (I/O instr)		I/O	0		

Table 9-18. Timing Specifications for MRQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↓		I/O				50
t_{dlh}	SCLK-↓	Edge that causes MEMGO-↑	I/O		30		110
t_{su}	SCLK-↑			P	100		
t_{h}	SCLK-↑	Edge that causes BUSY-↓		P	-10		

Table 9-19. Timing Specifications for PE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{pw}		Must occur during window		I/O	50		
t_{su}	Start window SCLK-↓	First edge after edge that causes RNI-↓ (instr fetch window)		I/O	0		
t_{h}	End window SCLK-↑	First edge after VALID-↑ (instr fetch window)		I/O	0		
t_{su}	Start window SCLK-↓	First edge after edge that causes VALID-↓ (DMA window)		I/O	0		
t_{h}	End window SCLK-↓	Second edge after edge that causes VALID-↑ (DMA window)		I/O	0		
t_{d}	SCLK-↑		M		20		
t_{pw}		Every SHC until double bit error cleared	M		100		

Table 9-20. Timing Specifications for PFW-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	PON+↓		PS		5 ms		
t_{su}	PON+↑		PS		10 ms		
t_r , t_f			PS				50
t_{su}	PON+↓	Software requires time for power down routine to execute		SW	5 ms		

Table 9-21. Timing Specifications for PON+

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME MIN	TYP	MAX
t_d		Supplies up and within regulation	PS		50	65	100 ms
t_r , t_f			PS				50 ms
t_{pw}		Time required to reset CPU		P	133		ns

Table 9-22. Timing Specifications for REMEM-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑	SCLK- that occurs during MEMGO-		M	55		
t_{h}	SCLK-↑	Same edge		M	-10		
t_{dhl}	SCLK-↓		I/O				45
t_{dlh}	SCLK-↓	Next edge	I/O		30		110

Table 9-23. Timing Specifications for RNI-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↓	That occurs during VALID-		I/O	25		
t_{h}	SCLK-↓	Same edge		I/O	30		
t_{dhl}	SCLK-↑	First edge after MEMGO-↓ from CPU	P				15
t_{dlh}	SCLK-↑	Edge that causes VALID-↑	P				15
t_{pw}			P			1C	
t_{pw}				I/O	1C-t_{su}	1C	

Table 9-24. Timing Specifications for SC0 - SC4 (AE0 - AE4)
Note: In A-Series Computers this bus is labeled AE0 - AE4.

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_d	SCLK-↓	Edge that causes MEMGO-↓	I/O				90
t_h	SCLK-↓	Edge that causes MEMGO↑	I/O		20		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-		M	90		
t_h	SCLK-↑	Edge that occurs during MEMGO-		M	-44		

Table 9-25. Timing Specifications for SCHID-/SCHOD-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_d		SCHID-↓ to SCHOD-↓	I/O			5	7.5
SCHOD- t_{dhl}*	SCLK-↑	Edge that caused SCHID-↑	I/O				25
SCHID- t_{su}	SCLK-↑			I/O	0		
SCHID- t_h	SCLK-↑	Same edge		I/O	15		
t_{dlh}	SCLK-↑		P				50
t_{dhl}	SCLK-↑	Next edge	P				50

* If a low priority interface asserts SLAVE-, a higher priority interface can get the slave cycle if the higher priority interface lowers SCHOD- at any time up until 1C-169 ns after the SCLK- which caused SCHID-.

Table 9-26. Timing Specifications for SCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
f			P		-0.005%	3.75 MHz	+0.005%
t_p				I/O	227		
t_{pw}		LHC		I/O	135		
t_{pw}		SHC		I/O	90		
t_p			P		267*		
t_{pw}		LHC	P		167*		
t_{pw}		SHC	P		95		
t_d	Processor clock (e.g., CK.A.CAC1. CK+)	to SCLK-↑	P		0		26
t_d	..	to SCLK-↓	P		100		120
t_d	SCLK-↓	to processor clock	P		13		33
t_d	SCLK-↑	..	P		107		133

* A memory error correction cycle will add 133 ns to this value.

Table 9-27. Timing Specifications for SELFC

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↓	Edge that causes MEMGO-↓	I/O				80
t_{h}	SCLK-↓	Edge that causes MEMGO↑	I/O		40		180
t_{su}	SCLK-↑	Edge that occurs during MEMGO-		M	90		
t_{h}	SCLK-↑	Edge that occurs during MEMGO-		M	-44		

Table 9-28. Timing Specifications for SLAVE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↑		I/O				45
t_{dlh}	SCLK-↑	First edge after SCHID-↓	I/O				130
t_{su}	SCLK-↓			P	asynchronous		

Table 9-29. Timing Specifications for VALID-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{dhl}	SCLK-↑		M		50		70
t_{dlh}	SCLK-↑		M		-10		55
t_{su}	SCLK-↓			I/O	10		
t_{h}	SCLK-↓	Same edge		I/O	30		

Table 9-30. Timing Specifications for WE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑	That occurs during MEMGO		M	33		
t_{h}	SCLK-↑	Same edge		M	0		
t_{d}	SCLK-↓	That causes MEMGO-↓	I/O				100
t_{h}	SCLK-↓	That causes MEMGO-↑	I/O		20		

9.9 Signal Definitions

Table 9-31 lists all backplane signals. The signals are listed in alphabetical order, along with their definitions, where they originated, where they go, functions, and general timing specifications. Timing values, when given, are nominal. For specific timing values, see Tables 9-3 through 9-30.

Table 9-31. Backplane Signal Definitions

(AB0+)-(AB14+)

FULL NAME: Address Bus 0-14 (Tri-state, high true)

DRIVEN BY: The I/O Master during a DMA transfer or while receiving interrupt service. (In the case of interrupt service, the card drives AB0 - AB5 with its select code and AB6 - AB14 with zeros.)

RECEIVED BY: Memory and processor card.

FUNCTION: The address bus is used to transfer a 15-bit absolute address to the memory, of which AB0 is the least significant bit. The processor will latch the address in case a parity error or memory protect violation occurs. (Will not check for these during DMA.)

TIMING: The address bus is driven with the assertion of MEMGO- during a DMA transfer and during an interrupt cycle.

(AE0 - AE4)

FULL NAME: Address Extension Bus. This bus was previously called the SC (Select Code) Bus. Refer to (SC0 - SC4) for signal definition.

Table 9-31. Backplane Signal Definitions (Continued)

BUSY-

FULL NAME: Memory Busy (low true)

DRIVEN BY: Memory cards

RECEIVED BY: Interface cards

FUNCTION: BUSY- is asserted by the memory to indicate that it is unable to begin a new cycle.

TIMING: BUSY- is asserted after the rising edge of SCLK-, following the assertion of MEMGO-. BUSY- is released following the rising edge of SCLK- that precedes the next possible memory cycle by one cycle of SCLK-.

CCLK-

FULL NAME: Communications Clock (low true)

DRIVEN BY: Processor card

RECEIVED BY: Interface cards

FUNCTION: This clock provides a fixed frequency which may be used to drive a state machine, or which may be divided down for baud rate generation.

TIMING: 14.7456 MHz clock with a 50-percent duty cycle.

CPUTURN-

FULL NAME: Processor Turn (low true)

DRIVEN BY: Processor Card

RECEIVED BY: All interface cards

FUNCTION: Asserted during RNI- and in addition, in order to signal that the processor card requests backplane priority. The assertion of CPUTURN- inhibits all interface cards from reasserting MRQ- once all current requests are satisfied.

TIMING: When the processor wants to get out on the backplane for any one of three reasons (broadcasting an I/O instruction, acknowledging an interrupt, or participating in an I/O handshake) but is held off by DMA, the CPU will assert CPUTURN. CPUTURN stays asserted until the processor starts its transaction on the backplane.

Table 9-31. Backplane Signal Definitions (Continued)

CRS-

FULL NAME: Control Reset (low true)

DRIVEN BY: Processor Card

RECEIVED BY: All cards

FUNCTION: The assertion of CRS- completely resets the I/O system. All of the following will occur:

1. All interface control flip-flops will be cleared.
2. All interface flag flip-flops will be cleared.
3. All pending I/O interrupts will be cleared except power fail.
4. The global register will be disabled.
5. Parity valid LED on memory card will be turned on.

In addition, each interface card interprets CRS- to perform its own various test functions.

TIMING: CRS- is asserted for one cycle of SCLK- when a CLC 0 instruction is executed.

(DB0+)-(DB15+)

FULL NAME: Data Bus 0-15 (Tri-state, high true)

DRIVEN BY: Any memory or interface card or the processor card.

RECEIVED BY: Any memory or interface card or the processor card.

FUNCTION: DB0 to 15, of which DB0+ is the least significant bit, are used for all system data transfers.

TIMING: An interface card will drive the data bus during the assertion of MEMGO- on a DMA write. The RAM card drives the data bus on a read cycle for one cycle, during the assertion of VALID-. The processor card drives the data bus with the assertion of MEMGO- on a memory write (STA), with IOGO- on an I/O write (OTA), and with VALID- clocked by start of long half-cycle on A or B fetch or Boot Read.

Table 9-31. Backplane Signal Definitions (Continued)

IAK-

FULL NAME: Interrupt Acknowledge (low true)

DRIVEN BY: Processor card

RECEIVED BY: Any interrupting card

FUNCTION: Asserted to signal that an interrupt request is about to be serviced and to freeze the interrupt priority chain.

TIMING: IAK- is asserted by the processor card following the start of the short half cycle of SCLK-. It is held until after the trap cell instruction has commenced. (MEMGO-↓ causes IAK-↑.)

ICHID-

FULL NAME: Interrupt Chain In Disable (low true)

DRIVEN BY: The next higher priority card, to whom this signal is ICHOD-.

RECEIVED BY: All interface cards

FUNCTION: See ICHOD-

TIMING: See ICHOD-

ICHOD-

FULL NAME: Interrupt Chain Out Disable (low true)

DRIVEN BY: All interface cards, and the processor card (which is the top of the chain).

RECEIVED BY: The next lower priority card, to whom this signal is ICHID-.

FUNCTION: Asserted to disable lower priority cards from interrupting. A high on this line keeps interrupt generation enabled. ICHOD- is part of the ICHID-/ICHOD- daisy chain, used to determine interrupt priority.

TIMING: Asserted by an interface card when its ICHID line goes low, or when its FLAG and CONTROL flip-flops get set. De-asserted when ICHID- goes high, and on either a CLF, CLC or PON+.

Table 9-31. Backplane Signal Definitions (Continued)

INTRQ-

FULL NAME: Interrupt Request (open-collector, low true)

DRIVEN BY: All interface cards

RECEIVED BY: Processor card

FUNCTION: Asserted to signal an interrupt request, and held low until the interrupt gets service, until PON+ goes low, or until a CLC 0 is executed.

TIMING: Asserted by an interface card when both its CONTROL and FLAG flip-flops are set and its ICHID- signal is high. De-asserted when the CONTROL or FLAG flip-flop is cleared, or 2 cycles after the assertion of IAK- while ICHID- is high.

IOGO-

FULL NAME: I/O Handshake Request Acknowledge (low true)

DRIVEN BY: Processor card

RECEIVED BY: All interface cards

FUNCTION: Asserted to signal that the processor card is ready to receive a command or send or receive an operand from an interface card. De-asserted when the transfer has been completed.

TIMING: Pulled low when the data bus is available for transfers and released as soon as the data has been clocked off the backplane.

NOTE: For some types of I/O transfers, this signal will participate in a double handshake.

Table 9-31. Backplane Signal Definitions (Continued)

IORQ-

FULL NAME:	I/O Handshake Request (open collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Processor card
FUNCTION:	Asserted to signal that an interface requires processor service, and de-asserted when being serviced.
TIMING:	Asserted within 2 cycles after the rising edge of RNI-, or in slave mode on the next rising edge of SCLK- after SCHID- goes high. De-asserted to signal that data will be valid on the second rising edge of SCLK-, or during an input, to signal that data has just been latched.
NOTE:	For some types of I/O transfers, this signal will participate in a double handshake.

MCHID-

FULL NAME:	Memory Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is MCHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	Asserted to disable initiation of a memory cycle.
TIMING:	MCHID- is asserted a maximum of one cycle after MRQ- goes low. Released as soon as memory cycle of higher priority device is complete.

Table 9-31. Backplane Signal Definitions (Continued)

MCHOD-

FULL NAME: Memory Chain Out Disable (low true)

DRIVEN BY: All interface cards and processor card.

RECEIVED BY: The next lower priority card, to whom this signal is MCHID-.

FUNCTION: Asserted to disable all lower priority cards from initiating a memory cycle.

TIMING: An interface card wanting a DMA cycle asserts MCHOD- at the end of the short half cycle of SCLK-. MCHOD- is de-asserted at the end of the short half cycle, following the assertion of BUSY-. The processor card is the top of this priority chain. MCHOD- is tied high on the processor card.

NOTE: All cards not using the memory priority chain must connect MCHOD- to MCHID-.

MCHODOC-

FULL NAME: Memory Chain Out Disable Open Collector (open collector, low true)

DRIVEN BY: All interface cards

RECEIVED BY: Head of priority chain on lower priority stack.

FUNCTION: Used as look-ahead for the memory priority chain. If any interface card in the higher priority stack asserts MCHODOC-, all interface cards in the lower priority stack will become disabled from initiating a memory cycle.

TIMING: An interface card wanting a DMA cycle asserts MCHODOC- at the end of the short half cycle of SCLK-. MCHODOC- is released at the end of the short half cycle, following the assertion of BUSY-.

NOTE: As far as the output of any given interface card is concerned, MCHODOC- is logically identical to MCHOD-.

The pull-up resistor on this line is located on the backplane.

Table 9-31. Backplane Signal Definitions (Continued)

MEMGO-

FULL NAME: Memory Cycle Initiation (open collector, low true)

DRIVEN BY: Interface cards.

RECEIVED BY: Memory, processor, and interface cards.

FUNCTION: Pulled low to signal a memory request and released once service begins.

TIMING: MEMGO- may be asserted by the card wishing to initiate a memory cycle after the falling edge of SCLK- that follows the release of BUSY-. MEMGO- is released by an interface card after being held low for one cycle of SCLK-.

MLOST-

FULL NAME; Memory Lost (open collector, low true)

DRIVEN BY: Processor, memory, and battery option in the power supply (or battery back-up card in a Micro/1000 system).

RECEIVED BY: Processor card, memory controller

FUNCTION: MLOST- is asserted by the optional battery in the power supply (or battery back-up card in a Micro/1000 system, to indicate that memory power was lost when system power last went down. Memory will then be cleared on the next power up. Where there is no back-up supply for the memory, MLOST- can be grounded. Do this by setting a switch on the processor card which grounds MLOST-, or by jumper settings on the memory card which shorts +5V to +5M and grounds MLOST-.

TIMING: Asserted as soon as memory power fails. Released 10 ms after the rising edge of PON+.

Table 9-31. Backplane Signal Definitions (Continued)

MP+

FULL NAME: Memory Protect (open collector, high true)

DRIVEN BY: Processor card

RECEIVED BY: All interface cards, memory controller

FUNCTION: When MP+ is high, all I/O interface cards are inhibited from recognizing I/O instructions. DMA is not affected.

TIMING: MP+ is always false in the A900. The CPU will not broadcast an I/O instruction unless it is in the privileged mode.

MRQ-

FULL NAME: Memory Request (open collector, low true)

DRIVEN BY: All interface cards

RECEIVED BY: Processor card, memory controller

FUNCTION: Asserted to indicate that an interface card performing DMA has requested a memory cycle. When MRQ- is low, the processor card is inhibited from requesting a memory cycle.

TIMING: An interface card wanting a DMA cycle asserts MRQ- at the start of the long half cycle of SCLK-. MRQ- is de-asserted on the falling edge of SCLK- after the assertion of BUSY-.

PE-

FULL NAME: Parity Error (low true)

DRIVEN BY: Memory controller.

RECEIVED BY: Interface cards.

FUNCTION: Asserted if last memory read produced a parity error.

TIMING: PE- asserted for one short-half-cycle after release of VALID-.

Table 9-31. Backplane Signal Definitions (Continued)

PFW-

FULL NAME:	Power Fail Warning (open collector, low true)
DRIVEN BY:	Power supply
RECEIVED BY:	Processor card
FUNCTION:	Asserted to signal an ac line voltage failure.
TIMING:	Asserted at least 5 ms before the fall of PON+. Released before the rise of PON+.
NOTE:	The pull-up resistor on this open collector line is located on the processor card.

PON+

FULL NAME:	Power On (open collector, high true)
DRIVEN BY:	Power supply and processor.
RECEIVED BY:	All cards in system.
FUNCTION:	PON+ is asserted by the power supply shortly after all power supply voltages are stable, to allow time for initialization on individual system cards. It is also pulsed low by a momentary switch located on the processor card in order to reset the computer.
TIMING:	Asserted 1 ms after all power supplies are stable. De-asserted if any supply falls below a tolerable level.

REMEM-

FULL NAME:	Remote Memory (open collector, low true)
DRIVEN BY:	Interface cards
RECEIVED BY:	Memory
FUNCTION:	REMEM- is asserted to indicate that the simultaneous MEMGO- which occurs should initiate a memory cycle with the remote memory. Any memory card in the system should ignore MEMGO- if it occurs with REMEM-.
TIMING:	REMEM- is asserted and released with MEMGO-.

Table 9-31. Backplane Signal Definitions (Continued)

RNI-

FULL NAME: Read Next Instruction (low true)

DRIVEN BY: Processor card.

RECEIVED BY: All interface cards.

FUNCTION: RNI- is asserted to indicate that the current memory cycle is a fetch and that an instruction will be on the data bus.

TIMING: RNI- is asserted on the rising edge of SCLK- after MEMGO-, and it is deasserted one SCLK later.

NOTE: The instruction is to be latched on the trailing (rising) edge of RNI-.

(SC0+) - (SC4+) or (AE0+) - (AE4+)

FULL NAME: Address Extension Bus 0 - 4 (tri-state function, high true)

DRIVEN BY: Interface Cards

RECEIVED BY: Memory Controller

FUNCTION: The SC bus is used to select one of 32 map sets.

TIMING: The Address Extension Bus is driven simultaneously with AB0 - AB14.

SCHID-

FULL NAME: Slave Chain In Disable (low true)

DRIVEN BY: The next higher priority card, to whom this signal is SCHOD- (except the highest priority card which is driven by the processor).

RECEIVED BY: All interface cards

FUNCTION: See SCHOD-

TIMING: See SCHOD-

Table 9-31. Backplane Signal Definitions (Continued)

SCHOD-

FULL NAME: Slave Chain Out Disable (low true)

DRIVEN BY: All interface cards

RECEIVED BY: The next lower priority card, to whom this signal is SCHID-.

FUNCTION: SCHOD- is asserted to disable lower priority cards from entering slave mode. SCHOD- is part of the SCHID-/SCHOD- priority chain, used to settle conflicts for slave mode processing.

TIMING: SCHOD- is asserted with SLAVE-, or if a higher priority card pulls on SCHID-, and is held as long thereafter as it takes the daisy chain to ripple down. Likewise, SCHOD- is released with SLAVE- or SCHID-.

NOTE: The top of the priority chain is the processor card. Whenever SLAVE- is asserted, and the processor card has completed executing the current instruction, SCHOD- goes high for one cycle of SCLK-.

There must be exactly one non-inverting Schottky gate on each card between SCHID- and SCHOD-. Example:

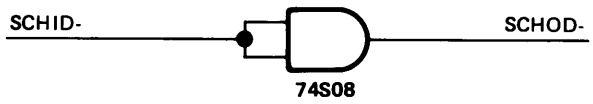


Table 9-31. Backplane Signal Definitions (Continued)

SCLK-

FULL NAME: Slow clock

DRIVEN BY: Processor card

RECEIVED BY: All system cards

FUNCTION: SCLK- is used to synchronize many diverse system signal interactions.

TIMING: SCLK- is a derivative of processor clocks. It is generated with a divide-by-8 circuit which produces a signal with a minimum of a 267-nanosecond period and a 37-percent duty cycle.

NOTE: In all timing descriptions, the term "short half-cycle" refers to the time (3/8 period) when SCLK- is high. The "long half-cycle" refers to the 5/8 period when SCLK- is low.

So as to minimize clock skew, all cards are required to receive SCLK- into an S240.

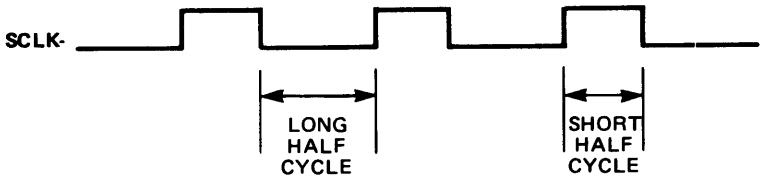


Table 9-31. Backplane Signal Definitions (Continued)

SELFC-

FULL NAME: Self Configure (Open collector, low true)

DRIVEN BY: Interface Cards

RECEIVED BY: Memory Controller

FUNCTION: SELFC- is asserted to indicate that DMA self-configuration is occurring. The memory controller enables MAP 0 to use during DMA self configuration.

TIMING: SELFC- is driven simultaneously with AB0 - AB14.

SLAVE-

FULL NAME: Slave Request (open collector, low true)

DRIVEN BY: Interface cards

RECEIVED BY: Processor card

FUNCTION: SLAVE- is asserted to request the processor to enter slave mode, i.e., to force the processor to enter an I/O handshake.

TIMING: SLAVE- is held asserted until the start of the long half cycle of SCLK- following the release of SCHID-.

VALID-

FULL NAME: Data Valid (Tri-state, low true)

DRIVEN BY: Memory controller

RECEIVED BY: Interface cards

FUNCTION: VALID- is asserted to signal that the data on the data bus is about to become valid during a memory read cycle.

TIMING: On a read cycle, the memory will assert VALID- after the rising edge of SCLK- that precedes the appearance of valid data on the backplane by one cycle. VALID- will be held low for one cycle and then released after the rising edge of SCLK- right after data becomes valid. VALID- is asserted during write.

Table 9-31. Backplane Signal Definitions (Continued)

WE-

FULL NAME:	Write Enable (Tri-state, low true)
DRIVEN BY:	Any card accessing memory
RECEIVED BY:	Memory controller
FUNCTION:	WE- is asserted to signal a memory write, and held high to signal a memory read.
TIMING:	WE- is asserted and released with (AB0+)-(AB14+).

9.10 Parts Locations

Parts locations for the 20-slot and 16-slot backplanes are shown in Figure 9-2 and 9-3.

9.11 Parts List

The parts list for the 20-slot backplane is provided in Table 9-32 and the parts list for the 16-slot backplane is provided in Table 9-33.

Table 9-32. 20-Slot Backplane Replaceable Parts

REF. DESIG.	HP PART NUMBER	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
CR1	1902-0939	2	DIODE-ZENER 5.0V	03287	1N5908
CR2	1902-0941	2	DIODE TRANSIENT SUP, 12.0V	03287	GS ICTE-12
CR3	1902-0941		DIODE TRANSIENT SUP, 12.0V	03287	GS ICTE-12
CR4	1902-0939		DIODE-ZENER 5.0V	03287	1N5908
U1R	1810-0182	1	RES NETWORK 220/1330 X 12	04200	1810-0271
U2R-U4R	1810-0083	1	RES NETWORK 1K X 13	04200	1810-0272
W1	1811-3587	1	RESISTOR - FXD 0 OHM	03123	104
	1251-8053	34	CONNECTOR - AC EDGE	28480	1251-8053

Table 9-33. 16-Slot Backplane Replaceable Parts

REF. DESIG.	HP PART NUMBER	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
CR1	1902-0939	2	DIODE-ZENER 5.0V	03287	1N5908
CR2	1902-0941	2	DIODE TRANSIENT SUP, 12.0V	03287	GS ICTE-12
CR3	1902-0941		DIODE TRANSIENT SUP, 12.0V	03287	GS ICTE-12
CR4	1902-0939		DIODE-ZENER 5.0V	03287	1N5908
U1R	1810-0083	3	RES NETWORK 1K X 13	04200	1810-0083
U2R	1810-0083		RES NETWORK 1K X 13	04200	1810-0083
U3R	1810-0182	1	RES NETWORK 220/330 X 12	04200	1810-0182
U4R	1810-0083		RES NETWORK 1K X 13	04200	1810-0083
W1	1811-3587	1	RESISTOR - FXD 0 OHM	03123	104

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
03123	Micro Ohm	El Monte, CA	91734
03287	General Semiconductor	Tempe, AZ	85282
04200	Sprague Electric	North Adams, MA	01247
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304

9.12 Dimensions

The dimensions for the A900 CPU cards are as follows:

Length	304mm (11.950 inches)
Width	172mm (6.75 inches)
Thickness	2.49mm (0.098 inch)
Parts Clearance:	
Top-of-card	10.2mm (0.4 inch)
Beneath card	5.1mm (0.2 inch)

The backplane and card cage dimensions are the following:

20-Slot Backplane	
Length	419mm (16.5 inches)
Width	203mm (8.0 inches)
16-Slot Backplane	
Length	375mm (14.75 inches)
Width	140mm (5.50 inches)
12030A Card Cage (Power Module excluded)	
Width	362mm (14.25 inches)
Height	117mm (4.63 inches)
Depth	313mm (12.3 inches)
2139A (20-Slot Rack Mounted Box)	
Width	483mm (19 inches)
Height	266 (10.5 inches)
Depth	6120mm (24 inches)
2439A, 2489A (16-Slot Rack Mounted Box)	
Width	483mm (19 inches)
Height	178mm (7 inches)
Depth	648mm (25.5 inches)

Figures 9-23 and 9-24 show the assembly of the rack-mounted boxes used for the 20-slot and 16-slot backplanes, respectively.

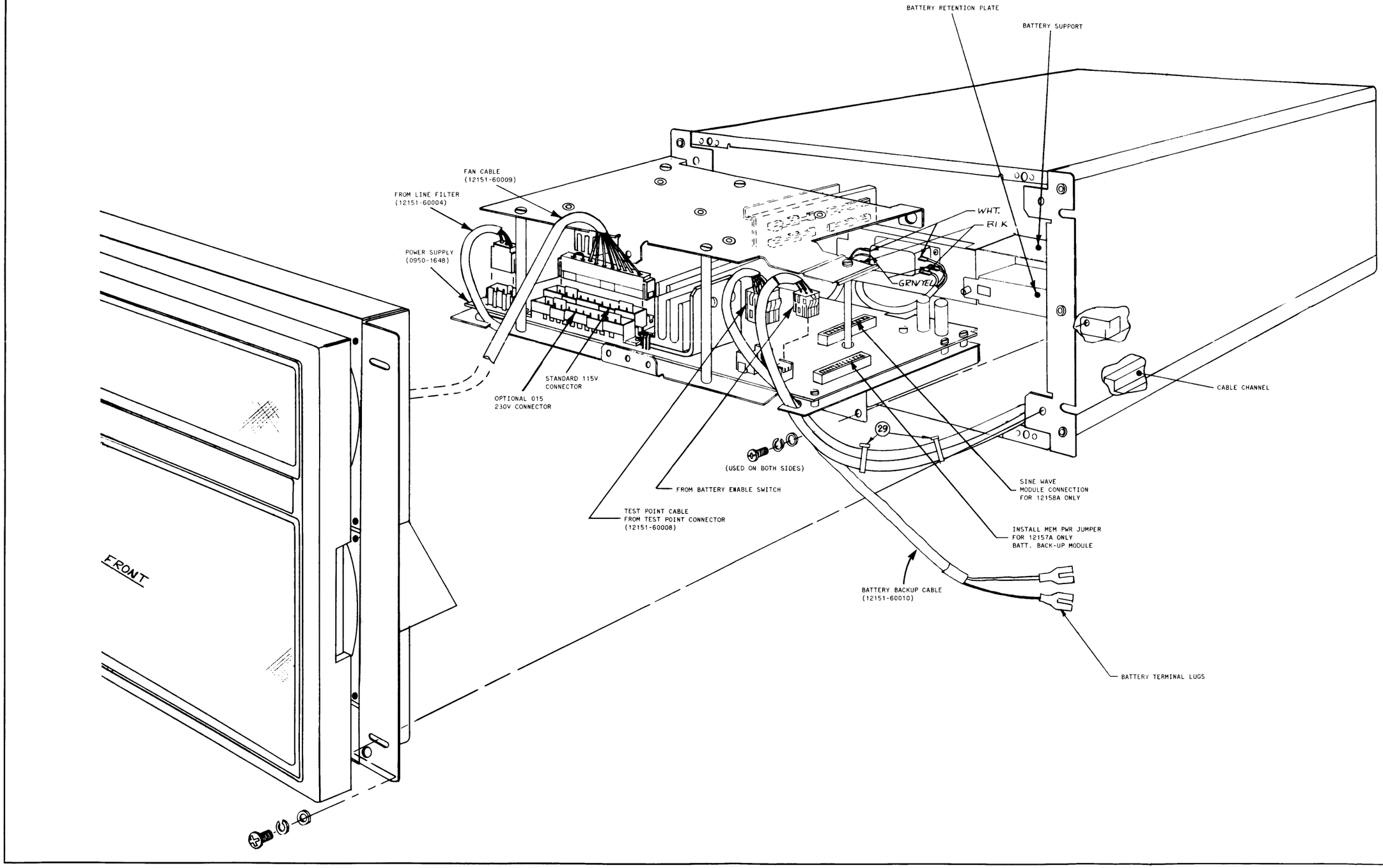
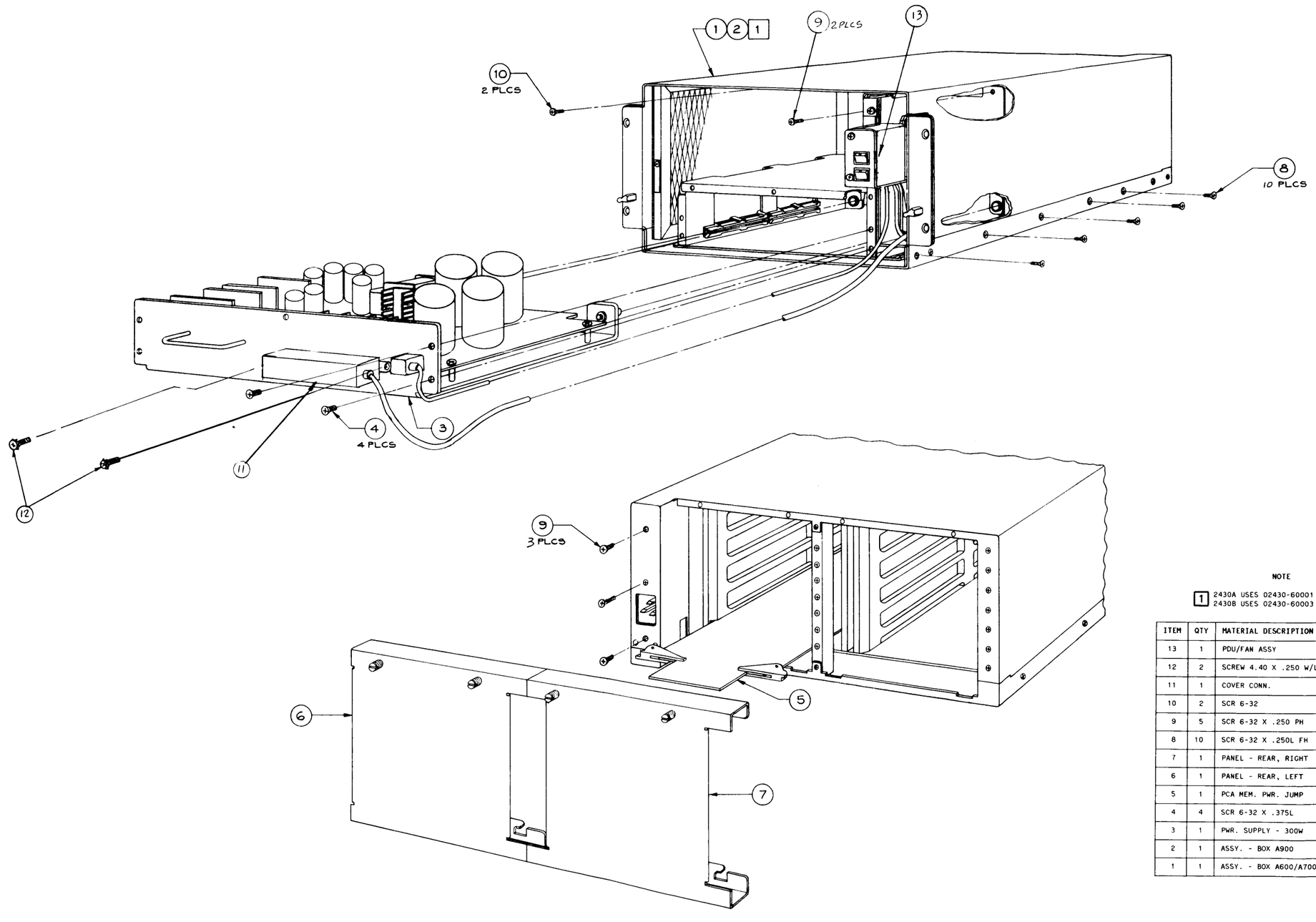


Figure 9-23. 20-Slot Box Assembly Diagram

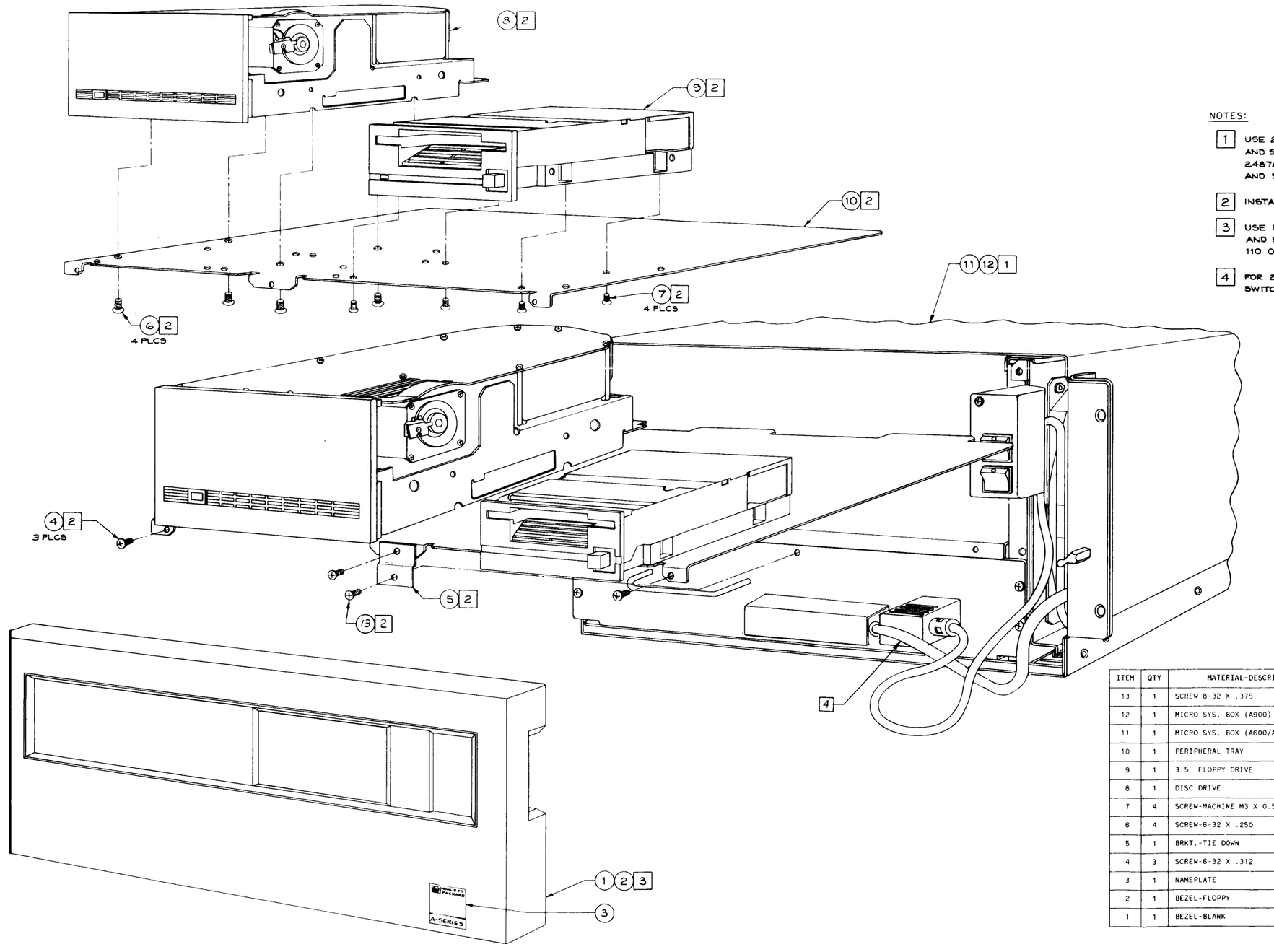


NOTE

[1] 2430A USES 02430-60001 BOX ASSY.
2430B USES 02430-60003 BOX ASSY.

ITEM	QTY	MATERIAL DESCRIPTION	PART NUMBER
13	1	PDU/FAN ASSY	02430-60005
12	2	SCREW 4.40 X .250 W/LK	2200-0103
11	1	COVER CONN.	02430-00028
10	2	SCR 6-32	2360-0429
9	5	SCR 6-32 X .250 PH	2360-0113
8	10	SCR 6-32 X .250L FH	2360-0192
7	1	PANEL - REAR, RIGHT	02430-00021 REF.
6	1	PANEL - REAR, LEFT	02430-00012 REF.
5	1	PCA MEM. PWR. JUMP	02430-60009
4	4	SCR 6-32 X .375L	2360-0117
3	1	PWR. SUPPLY - 300W	0950-1646
2	1	ASSY. - BOX A900	02430-60003
1	1	ASSY. - BOX A600/A700	02430-60001

Figure 9-24. 16-Slot Box Assembly Diagram (Sheet 1 of 4)



NOTES:

1. USE 2430A (11) FOR A600/A700 COMPU AND SYSTEMS - 2436A/E, 2437A, 248 2487A. USE 2430B (12) FOR A900 C AND SYSTEM - 2439A AND 2489A.
2. INSTALL FOR OPTION 110 ONLY.
3. USE ITEM (1) FOR STANDARD COMPU AND SYSTEM. USE ITEM (2) FOR OP 110 OF COMPUTER AND SYSTEM.
4. FOR 230V AC OPERATION, (OPTION 01 SWITCH CABLE INSTALLATION.

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO.
13	1	SCREW 8-32 X .375	2510-0045
12	1	MICRO SYS. BOX (A900)	2430B
11	1	MICRO SYS. BOX (A600/A700)	2430A
10	1	PERIPHERAL TRAY	02430-00013
9	1	3.5" FLOPPY DRIVE	88121DT
8	1	DISC DRIVE	88234DT 015
7	4	SCREW-MACHINE M3 X 0.5	0515-0076
6	4	SCREW-6-32 X .250	2360-0192
5	1	BRKT.-TIE DOWN	02430-00025
4	3	SCREW-6-32 X .312	2360-0115
3	1	NAMEPLATE	5180-4242
2	1	BEZEL-FLOPPY	02430-40002
1	1	BEZEL-BLANK	02430-40001

Figure 9-24. 16-Slot Box Assembly Diagram (Sheet 2 of 4)

ITEM	QTY	MATERIAL-DESCRIPTION	MATL'-PART NO.
11	3	CLAMP-CABLE	1400-1157
10	1	MICRO SYS. BOX (A600/A700)	2430A
9	1	MICRO SYS. BOX (A900)	2430B
8	1	FIXED DISC DRIVE	88234DT 015
7	1	3.5" FLOPPY DISC DRIVE	88121DT
6	1	CABLE-POWER, FIXED DISC	12022-60004
5	1	CABLE-POWER, MICROFLOPPY	12022-60006
4	1	DISCINTERFACE CARD	12022-60001
3	1	CABLE-CONTROL, FIXED DISC	12022-60002
2	1	CABLE-DATA, FIXED DISC	12022-60003
1	1	CABLE-SIGNAL, MICROFLOPPY	12022-60005

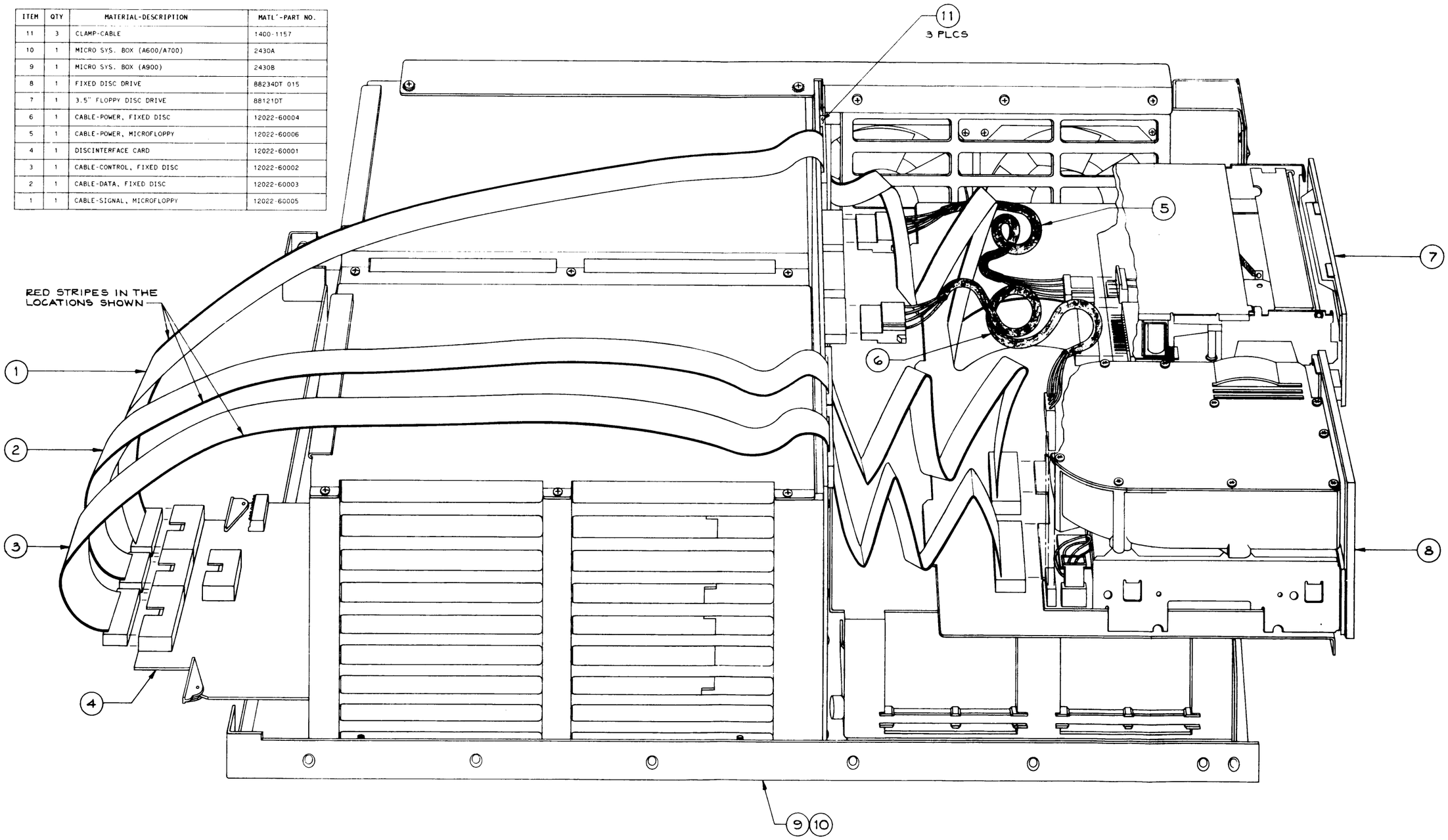
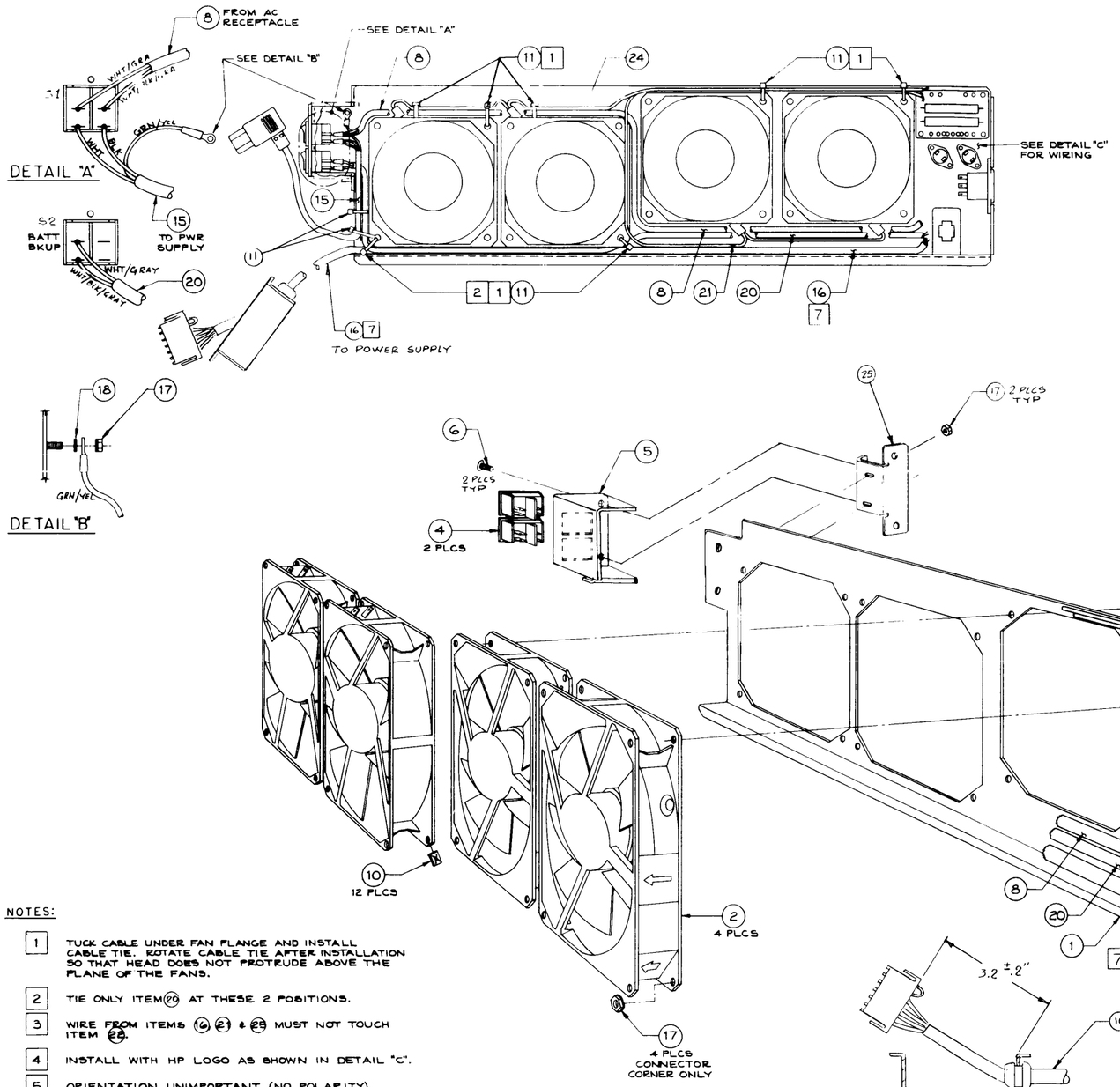


Figure 9-24. 16-Slot Box Assembly Diagram (Sheet 3 of 4)



NOTES:

1. TUCK CABLE UNDER FAN FLANGE AND INSTALL CABLE TIE. ROTATE CABLE TIE AFTER INSTALLATION SO THAT HEAD DOES NOT PROTRUDE ABOVE THE PLANE OF THE FANS.
2. TIE ONLY ITEM (20) AT THESE 2 POSITIONS.
3. WIRE FROM ITEMS (16) (21) & (23) MUST NOT TOUCH ITEM (23).
4. INSTALL WITH HP LOGO AS SHOWN IN DETAIL "C".
5. ORIENTATION UNIMPORTANT (NO POLARITY).
6. INSTALL CONNECTOR WITH #1 UP.
7. INSTALL ITEMS (26) (27) BEFORE SOLDERING ITEM (16) TO ITEM (19). SEE DETAIL "E"

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO.
27	1	STRAIN RELIEF GROMMET	0400-0155
26	1	COVER	02430-00028
25	1	SWITCH BRACKET	02430-00027
24	1	FAN CABLE-SHORT	8120-4271
23	4	SCREW-4-40 X .438	2200-0145
22	2	RESISTORS 200 Ω	0811-3643
21	1	FAN CABLE-LONG	8120-4272
20	1	CA. ASSY. BATT. BKUP. - SW.	02430-60011
19	1	PCB-FAN RESISTOR	02430-80010
18	2	LOCK WASHER, EXT. #6	2190-0008
17	8	NUT 6-32 W/LOCK	2420-0001
16	1	CABLE-PCA TO P.S.	02430-60008
15	1	CABLE-A.C. SW. TO P.S.	02430-60007
14	2	SCREW-4-40 X .375 F.H.	2200-0144
13	6	WASHER-FLAT #4	3050-0229
12	10	WASHER-LOCK #4	2190-0108
11	9	CABLE TIE	1400-0249
10	12	CLIP	0590-1516
9	6	NUT #4	2260-0002
8	1	A.C. POWER CABLE	02430-60006
7	16	SCREW #6 F.H. .375	2360-0196
6	2	SCREW #6 F.H. .312	3260-0194
5	1	SWITCH PLATE	02430-00009
4	2	SWITCH-RKR. DPST	3101-0402
3	2	THERMAL SWITCH	3103-0113
2	4	FAN-4.125"	3160-0420
1	1	FAN PANEL	02430-00008

Figure 9-24. 16-Slot Box Assembly Diagram (Sheet 4 of 4)

Update 1 **9-87/9-88**

ENGINEERING RESPONSIBILITY — SEPIA

D-12210-60002-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	11/16/82

CONNECTORS: XA1 XA6 XA7 THROUGH XA20

28D LBP.ICHID- J1-1 J1-1 J1-1 ... J1-1 (J1-1 IS ICHID-)
J1-2 J1-2 J1-2 ... J1-2 (J1-2 IS ICHOD-)

J1-3,4: SEE MEMORY ENABLE/DISABLE CHAIN BELOW

34A 26C LBP.MLOBT- J1-5 J1-5 J1-5 ... J1-5

J1-6: SEE MEMORY ENABLE/DISABLE CHAIN BELOW

33A 26A LBP.PFW- J1-7 J1-7 J1-7 ... J1-7
SPARE 1 J1-8 J1-8 J1-8 ... J1-8
26D LBP.SC0+ J1-9 J1-9 J1-9 ... J1-9
26C LBP.SC1+ J1-10 J1-10 J1-10 ... J1-10
26C LBP.SC2+ J1-11 J1-11 J1-11 ... J1-11
22B LBP.SC3+ J1-12 J1-12 J1-12 ... J1-12
28C 33B BP.GND J1-13 J1-13 J1-13 ... J1-13
J1-14 J1-14 J1-14 J1-14
LBP.COUTURN- J1-15 J1-15 J1-15 ... J1-15
J1-16 J1-16 J1-16 ... J1-16
25B LBP.SC4+ J1-17 J1-17 J1-17 ... J1-17
25B LBP.SC5+ J1-18 J1-18 J1-18 ... J1-18
J1-19 J1-19 J1-19 ... J1-19
J1-20 J1-20 J1-20 ... J1-20
J1-21 J1-21 J1-21 ... J1-21
J1-22 J1-22 J1-22 ... J1-22
J1-23 J1-23 J1-23 ... J1-23
J1-24 J1-24 J1-24 ... J1-24
J1-25 J1-25 J1-25 ... J1-25
J1-26 J1-26 J1-26 ... J1-26
25B LBP.AB+/15 J1-27 J1-27 J1-27 ... J1-27
J1-28 J1-28 J1-28 ... J1-28
J1-29 J1-29 J1-29 ... J1-29
J1-30 J1-30 J1-30 ... J1-30
J1-31 J1-31 J1-31 ... J1-31
J1-32 J1-32 J1-32 ... J1-32
J1-33 J1-33 J1-33 ... J1-33
22C LBP.WE- J1-34 J1-34 J1-34 ... J1-34

CONNECTORS: XA1 XA6 XA7 THROUGH XA20

25B 35C LBP.DB+/16
0 J1-35 J1-35 J1-35 ... J1-35
1 J1-34 J1-34 J1-34 ... J1-34
2 J1-37 J1-37 J1-37 ... J1-37
3 J1-36 J1-36 J1-36 ... J1-36
4 J1-39 J1-39 J1-39 ... J1-39
5 J1-40 J1-40 J1-40 ... J1-40
6 J1-41 J1-41 J1-41 ... J1-41
7 J1-42 J1-42 J1-42 ... J1-42
8 J1-43 J1-43 J1-43 ... J1-43
9 J1-44 J1-44 J1-44 ... J1-44
10 J1-45 J1-45 J1-45 ... J1-45
11 J1-46 J1-46 J1-46 ... J1-46
12 J1-47 J1-47 J1-47 ... J1-47
13 J1-48 J1-48 J1-48 ... J1-48
14 J1-49 J1-49 J1-49 ... J1-49
15 J1-50 J1-50 J1-50 ... J1-50

CONNECTORS: XA1 XA6 XA7 THROUGH XA20

22C LBP.CPUTURN- J2-1 J2-1 J2-1 ... J2-1
BP.GND J2-2 J2-2 J2-2 ... J2-2
22D LBP.REMEM- J2-3 J2-3 J2-3 ... J2-3
22C LBP.VALID- J2-4 J2-4 J2-4 ... J2-4
22C LBP.IORQ- J2-5 J2-5 J2-5 ... J2-5
22D LBP.INTRQ- J2-6 J2-6 J2-6 ... J2-6
22D LBP.MP+ J2-7 J2-7 J2-7 ... J2-7
22C LBP.RNI- J2-8 J2-8 J2-8 ... J2-8
22D LBP.MEMGO- J2-9 J2-9 J2-9 ... J2-9
26A LBP.PE- J2-10 J2-10 J2-10 ... J2-10
25B LBP.SCHOD- J2-11 J2-11 J2-11 ... J2-11 (J2-11 IS SCHID-)
J2-12 J2-12 J2-12 ... J2-12 (J2-12 IS SCHOD-)

CONNECTORS: XA1 XA6 XA7 THROUGH XA20

22C LBP.IAK- J2-13 J2-13 J2-13 ... J2-13
26A LBP.IOGO J2-14 J2-14 J2-14 ... J2-14
J2-15 J2-15 J2-15 ... J2-15
22C LBP.SLAVE- J2-16 J2-16 J2-16 ... J2-16
J2-17 J2-17 J2-17 ... J2-17
22C LBP.MRQ- J2-18 J2-18 J2-18 ... J2-18
J2-19 J2-19 J2-19 ... J2-19
32D LBP.FCLK- J2-20 J2-20 J2-20 ... J2-20
J2-21 J2-21 J2-21 ... J2-21
22B 32D LBP.CCLK- J2-22 J2-22 J2-22 ... J2-22
LBP.SPRQ- J2-23 J2-23 J2-23 ... J2-23
22B 32D LBP.SCLK- J2-24 J2-24 J2-24 ... J2-24
38D LBP.CRS- J2-25 J2-25 J2-25 ... J2-25
22B 34A LBP.PON+ J2-26 J2-26 J2-26 ... J2-26
J2-27 J2-27 J2-27 ... J2-27
38D LBP.BUSY- J2-28 J2-28 J2-28 ... J2-28
J2-29 J2-29 J2-29 J2-29
J2-30 J2-30 J2-30 J2-30
J2-31 J2-31 J2-31 J2-31
J2-32 J2-32 J2-32 J2-32
J2-33 J2-33 J2-33 J2-33
J2-34 J2-34 J2-34 J2-34
BP.GND
28D 35B BP.+5V J2-35 J2-35 J2-35 ... J2-35
LBP.+12M J2-36 J2-36 J2-36 J2-36
LBP.-12M J2-37 J2-37 J2-37 ... J2-37
LBP.+12V J2-38 J2-38 J2-38 J2-38
33B LBP.-12V J2-39 J2-39 J2-39 ... J2-39
28D 33A LBP.+5M J2-40 J2-40 J2-40 J2-40
34A LBP.25KHZ.02 J2-41 J2-41 J2-41 ... J2-41
J2-42 J2-42 J2-42 J2-42
34A LBP.25KHZ.01 J2-43 J2-43 J2-43 ... J2-43
J2-44 J2-44 J2-44 J2-44

CONNECTORS: XA1 XA6 XA7 THROUGH XA9 XA10 XA11 XA12 THROUGH XA20

28D LBP.MCHID- J1-3 J1-3 J1-3 ... J1-3 J1-3 J1-3 J1-3 ... J1-3 (J1-3 IS MCHID-)
J1-4 J1-4 J1-4 ... J1-4 J1-4 J1-4 J1-4 ... J1-4 (J1-4 IS MCHOD-)
26A 38D LBP.MCHODOC- J1-6 J1-6 J1-6 ... J1-6 J1-6 J1-6 J1-6 ... J1-6 BIT BUCKET

Memory Enable/Disable Chain

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L DWG. NO.	MAT'L SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE: A900 BACKPLANE MEMORY/IO CONNECTOR

NEXT ASSEMBLY

FINISH SCALE

HEWLETT PACKARD

PART NUMBER D-12210-60002-51

SHEET OF

STOCK NO. 8280-0004

28
27
26
25
24
23
22
21
D-12210-60002-52
SYM
REVISIONS
APPROVED
DATE
A
AS ISSUED
CONNECTORS: XA2 XA3 XA4 XA5
BP.+5V
BP.WR.CYC-
LBP.ICHID-
LBP.MCHID-
BP.LOG.ADDR0N+
BP.LOG.ADDR0I+
LBP.+5M
BP.LOG.ADDR
BP.GND+
BP.EXT.ADDR0+
BP.EXT.ADDR1+
CK.A.CPU3.DP+
CK.A.CPU4.DP+
FP.MEM.ADDR+
SQ.DP.SPARE+
CK.A.CPU4.LED.BP+
BP.LED.STOT-
BP.R2.SBRE.GN-
BP.MISSED.TICK-
LBP.SC0+
BP.AB.DP.WR+
CK.A.CAC1.CA+
CK.A.CAC2.CA+
LBP.MLOST-
LBP.SC1+
BP.RE.FREEZE-
BP.CPU.FREEZE-
BP.AB.CA.WR-
BP.B.CA.ADR+
LBP.SC2+
BP.UIUTP+
BP.GND+
BP.T.BUS+
BP.+5V
BP.MP.INT+
BP.TRUE.WRITE+
BP.AB.HIT+
BP.NORMAL+
BP.INVERT+
BP.LDOUT.EN-
BP.NO.WP+
LBP.IOGO-
LBP.AE-
LBP.MCHODOC-
LBP.PFW-
BP.UIR.REG7+
BP.R2.UIR.REG20+
BP.R2.UIR.REG21+
BP.R2.UIR.REG22+
BP.R2.UIR.REG23+
BP.+5V
LBP.SCHOD-
LBP.SC4+
LBP.SC5+
LBP.DB+
LBP.AB+
BP.UIR.REG+
BP.+5V
BP.GND+
BP.GND+
LBP.REMEM-
LBP.INTRQ-
LBP.MP+
LBP.AB13+
LBP.AB14+
LBP.MEMGO-
LBP.WE-
LBP.CPUTURN-
LBP.SLAVE-
LBP.MRQ-
LBP.VALID-
BP.JTAB.MEM-
LBP.IORQ-
LBP.RNI-
CK.A.MEM.D32.BP+
BP.DMA.CYCLE+
LBP.IAK-
CK.A.MEM.MC+
BP.+5V
LBP.SCLK-
BP.NO.EXECUTE-
LBP.CCLK-
BP.KEYS.OFF-
LBP.SC3+
BP.IND.INT-
BP.B.DP.APR+
LBP.PWN+
FP.MEM.ADDR3+
CK.A.MEM.D24.BP+
CK.A.MEM.D56.BP+
BP.S.BUS+
BP.GND+
XA2 = SQ
XA3 = DP
XA4 = CA
XA5 = MC
ITEM
QTY.
MATERIAL-DESCRIPTION
MAT'L-PART NO.
MAT'L-DWG. NO.
MAT'L-SPEC.
DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 608
A900 BACKPLANE
PROCESSOR CONN (1A-36D)
TITLE
HEWLETT PACKARD
NEXT ASSEMBLY
PART NUMBER
D-12210-60002-52
SUPERSEDES DWG.
FINISH
SCALE
SHEET OF
STOCK NO 8280-0004

D-12210-60002-53

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	11/18/82

ENGINEERING RESPONSIBILITY | SEPIA

DIP RESISTOR PACKS

U4R: 1K x 13, 1810-0083
U3R: 1K x 13, 1810-0083
U2R: 1K x 13, 1810-0083
U1R: 220/330 x 12, 1810-0182

CONNECTOR: XA2 XA3 XA4 XA5

22A BP.S.BUS+
LBP.+5M
13C LBP.CRS-
13C LBP.BUSY-
BP.S.BUS+
BP.GND+
BP.+5V
LBP.MCHODOC- 18A 26A
LBP.DB+ 26B 11C
LBP.FCLR- 13C
LBP.CCLR- 22B 13C
LBP.SCLR- 22B 13C
LBP.+5M

BP.ACCL.STOT-
BP.MEM.RD.REQ+
BP.MEM.WR.REQ+
LBP.+12V
BP.+5V
BP.CNDX.MET+
BP.MEM.BUSY+
BP.JTAB.INT-
BP.NINC.SPI-
BP.INT P+

PROCESSOR CONNECTORS (PINS 37A - 40D)

CONNECTOR: XA21

BP.+5V → 13B 28D
BP.GND+ → 13B

CONNECTOR: XA22

BP.GND+ → 18C 28C
LBP.+12V → 13B
LBP.-12V → 13B
BP.+5M → 13B 28D
LBP.25KHZ.01 → 13B
LBP.2KHZ.02 → 13A
LBP.PON+ → 13C 22B
LBP.PFW- → 26A 18C
LBP.MLOST- → 26C 18C
BP.+5M (SENSE)

POWER SUPPLY CONNECTORS

LBP.+5M
LBP.+12V
LBP.-12V
BP.+5V
BP.GND+

CR1 (5V) 1902-0939
CR4 (5V) 1902-0939
CR2 (12V) 1902-0941
CR3 (12V) 1928-0941

TRANSIENT PROTECTION DIODES

W1 0Ω 0811-3587 (CHASSIS GROUND)

NOTES

1. XA22 PIN 50 IS A +5M SENSE LINE THAT IS CONNECTED TO A SPECIAL FEEDTHROUGH NEAR XA9 BETWEEN J1 AND J2.
2. THE 2.5 kHz PHASES ARE ROUTED STRANGELY TO REMAIN COMPATIBLE WITH THE A700 20-SLOT BOX, XA22 01 IS ROUTED TO XA1,5-10 02 AND VICE-VERSA.
3. ALL OPEN AREAS ON BOTH SURFACE LAYERS HAVE BEEN CROSS-HATCHED WITH GROUND.
4. ALL UNLISTED PROCESSOR CONNECTOR PINS (XA2- XA5) ARE UNUSED.
5. PIN 7 OF U2R, U3R, & U4R IS TIED TO GROUND SO THAT UP/DOWN TERMINATING RESISTOR PACKS CAN BE SUBSTITUTED EASILY.

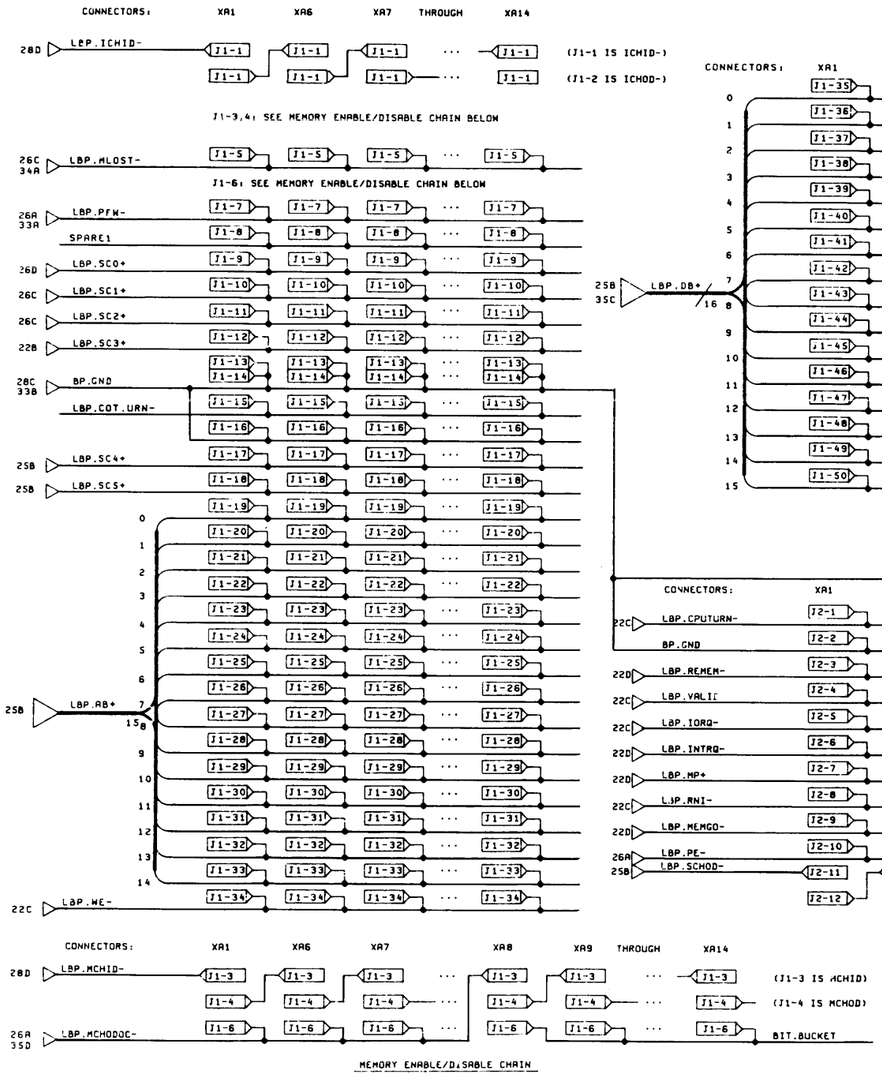
* THIS PART POWERED BY +5M

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING
UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.
TOLERANCES .XX ± .02 .XXX ± .005
SEE CORP. STD. 608

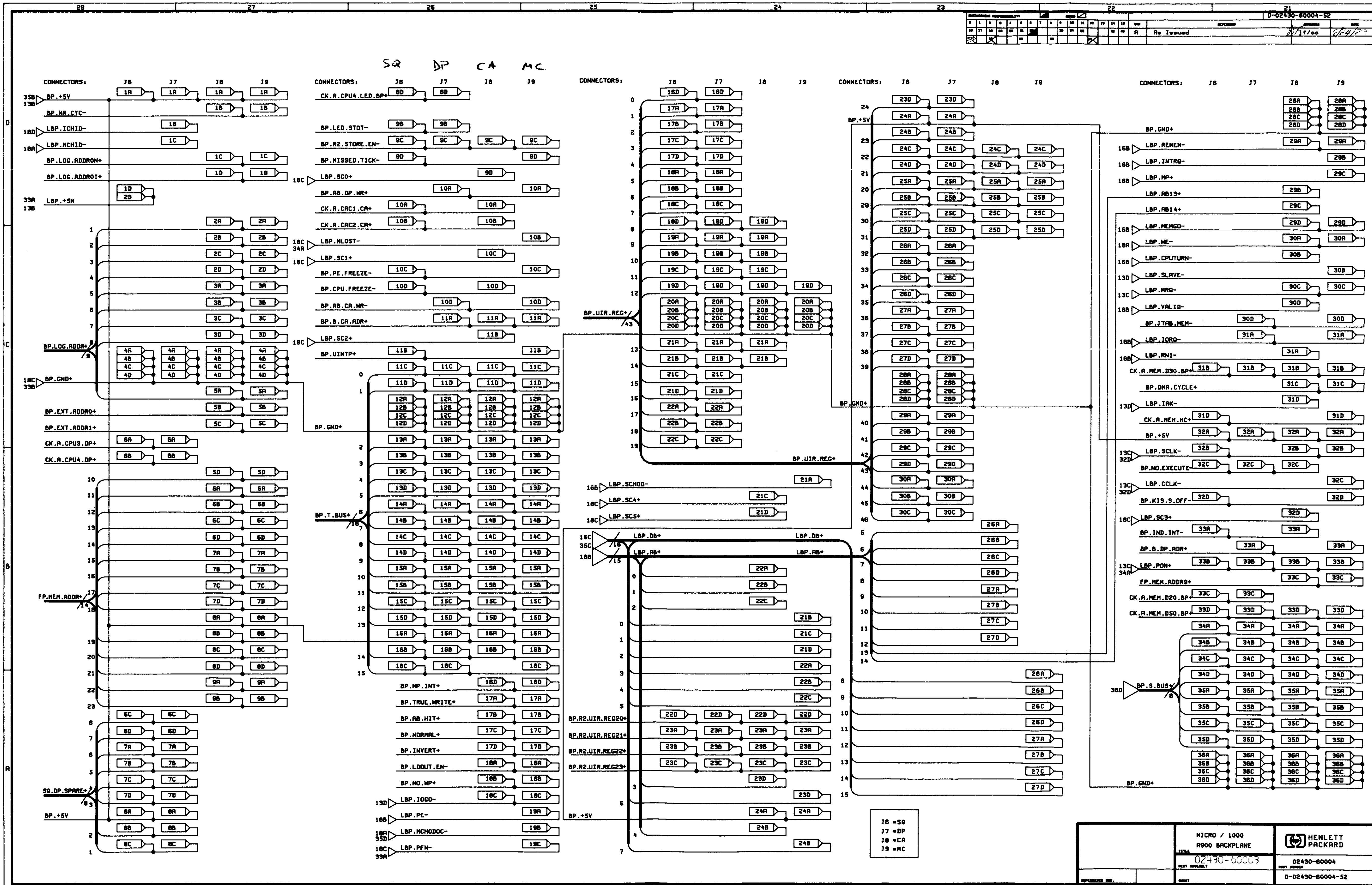
TITLE: A900 BACKPLANE MISCELLANEOUS
NEXT ASSEMBLY
FINISH | SCALE
SUPERSEDES DWG.
HEWLETT PACKARD
PART NUMBER D-12210-60002-53
SHEET OF

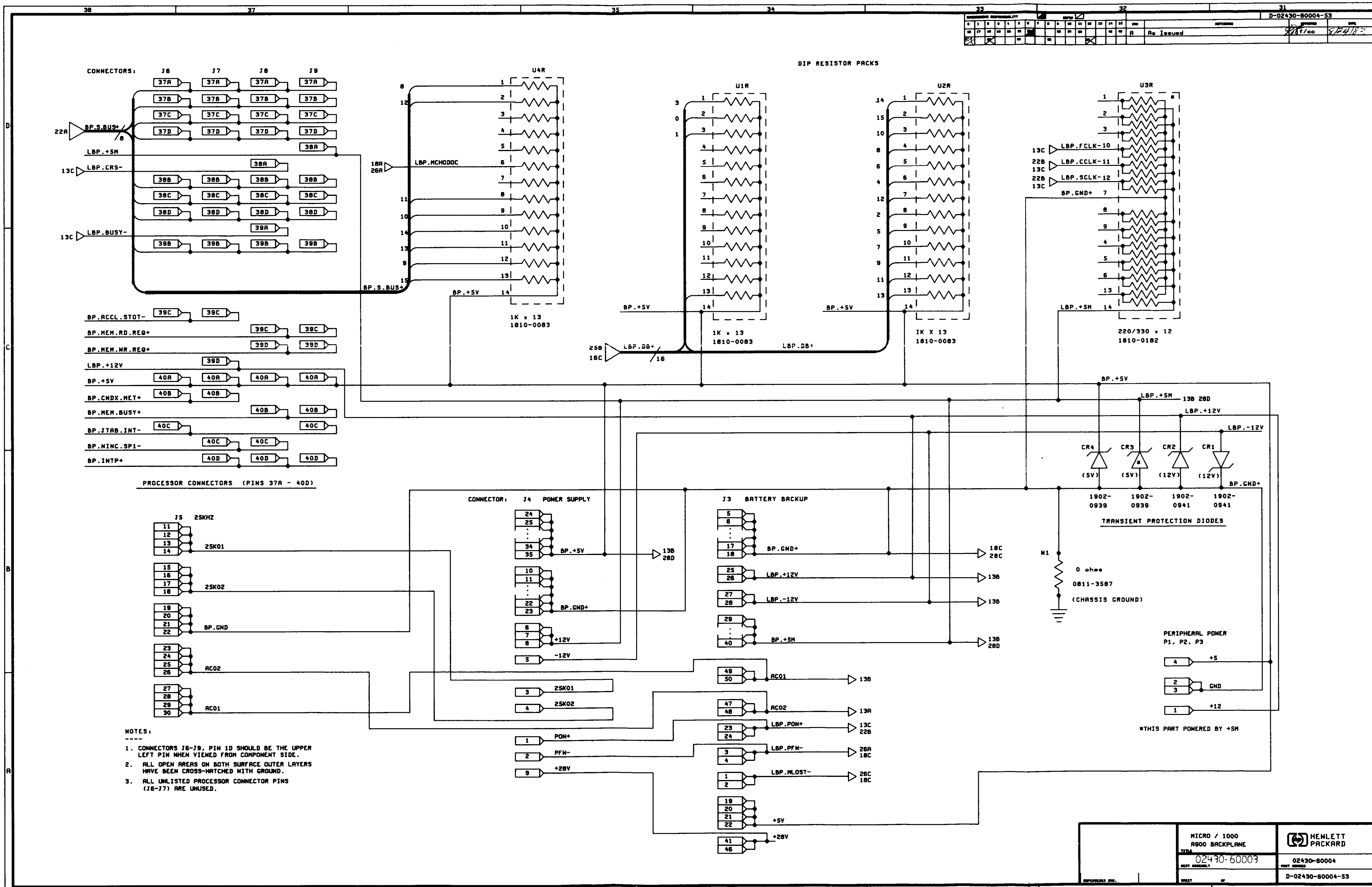
STOCK NO. 8280-0004



MEMORY ENABLE/DISABLE CHAIN

	MICRO / 1000 A900 BACKPLANE	HEWLETT PACKARD
	02430-60003	02430-60004
		D-02430-60004-51


SQ DP CA MC
CONNECTORS: J6 J7 J8 J9
BP.+5V
BP.WR.CYC-
LBP.ICHID-
LBP.MCHID-
BP.LOG.ADDRON+
BP.LOG.ADDROI+
LBP.+5M
BP.LOG.ADDR+
BP.GND+
BP.EXT.ADDRO+
BP.EXT.ADDR1+
CK.A.CPU3.DP+
CK.A.CPU4.DP+
FP.MEM.ADDR+
SQ.DP.SPARE+
CK.A.CPU4.LED.BP+
BP.LED.STOT-
BP.R2.STORE.EN-
BP.MISSED.TICK-
LBP.SC0+
BP.AB.DP.WR+
CK.A.CAC1.CA+
CK.A.CAC2.CA+
LBP.MLOST-
LBP.SC1+
BP.PE.FREEZE-
BP.CPU.FREEZE-
BP.AB.CA.WR-
BP.B.CA.ADR+
LBP.SC2+
BP.UINTP+
BP.T.BUS+
BP.MP.INT+
BP.TRUE.WRITE+
BP.AB.HIT+
BP.NORMAL+
BP.INVERT+
BP.LDOUT.EN-
BP.NO.WP+
LBP.IOGO-
LBP.PE-
LBP.MCHODOC-
LBP.PFW-
BP.UIR.REG+
LBP.SCHOD-
LBP.SC4+
LBP.SC5+
LBP.DB+
LBP.AB+
BP.R2.UIR.REG20+
BP.R2.UIR.REG21+
BP.R2.UIR.REG22+
BP.R2.UIR.REG23+
BP.+5V
J6 =SQ
J7 =DP
J8 =CA
J9 =MC
LBP.REMEM-
LBP.INTRQ-
LBP.MP+
LBP.AB13+
LBP.AB14+
LBP.MEMGO-
LBP.WE-
LBP.CPUTURN-
LBP.SLAVE-
LBP.MRQ-
LBP.VALID-
BP.JTAB.MEM-
LBP.IORQ-
LBP.RNI-
CK.A.MEM.D30.BP+
BP.DMA.CYCLE+
LBP.IAK-
CK.A.MEM.MC+
LBP.SCLK-
BP.NO.EXECUTE-
LBP.CCLK-
BP.KIS.S.OFF-
LBP.SC3+
BP.IND.INT-
BP.B.DP.ADR+
LBP.PON+
FP.MEM.ADDR9+
CK.A.MEM.D20.BP+
CK.A.MEM.D50.BP+
BP.S.BUS+
D-02430-60004-52
A As Issued
MICRO / 1000
A900 BACKPLANE
02430-60003
HEWLETT PACKARD
02430-60004
D-02430-60004-52



NOTES:
----

1. CONNECTORS J6-J9, PIN 1D SHOULD BE THE UPPER LEFT PIN WHEN VIEWED FROM COMPONENT SIDE.
2. ALL OPEN AREAS ON BOTH SURFACE OUTER LAYERS HAVE BEEN CROSS-HATCHED WITH GROUND.
3. ALL UNLISTED PROCESSOR CONNECTOR PINS (J6-J7) ARE UNUSED.

MICRO / 1000
A900 BACKPLANE

NEXT ASSEMBLY: 02430-60003

HEWLETT PACKARD

PART NUMBER: 02430-60004

D-02430-60004-53

Chapter 10
Frontplanes

10.1 Description

There are two frontplanes used with the A900 processor, one standard and the other optional. The standard frontplane connects the address and data buses from the memory controller to the memory array card or cards, and the other frontplane is included with the optional HP 12205A control store card to connect this card to the sequencer card.

Both frontplanes consist of printed circuit cards with circuit traces between the connectors (there are no active components). The same memory frontplane is used regardless of the array size of the memory card (i.e., the 768 kB and 3 Mb cards use the same frontplane). The control store frontplane has two connectors. The schematics are shown on the following pages. The processor frontplane schematics for the sequencer and data path cards are shown in the last schematic of the sets in Chapters 3 and 4.

The processor frontplane pins are identified in Appendix B. The control store frontplane signals are identified in the 12205-60002 schematic which is the last schematic in the set of Chapter 8.

10.2 Product and Part Identification

The memory array frontplane is available in eight versions for from one-to-eight error-checking memory array cards. The product numbers and part numbers are listed in Table 10-1. All connectors of the memory array and control store frontplanes are identical 96-pin male connectors consisting of three rows of 32 pins each, Part No. 1251-7972.

The HP 12222A and 12222B frontplanes include a protective polyurethane foam pad (date code 2421 and later). The foam pad is applied so that when the frontplanes are used in a HP Micro/1000 system the ribbon cable is protected from possible damage when the front door is closed against it. The part numbers of the pads for the two frontplanes are:

HP 12222A (P/N 12222-60001) ..... Pad P/N 4208-0344
HP 12222B (P/N 12222-60002) ..... Pad P/N 4208-0345

Only Hewlett-Packard replacement foam pads should be used because the material is selected for high temperature operation and fire resistance.

Table 10-1. Frontplane Part Numbers

PRODUCT	DESCRIPTION	PART NO.	NO. CONNECTORS (P/N 1251-7972)
12205A*	CS card to SQ card	12205-60002	2
12222A	One array card	12222-60001	2
12222B	Two array cards	12222-60002	3
12222C	Three array cards	12222-60003	4
12222D	Four array cards	12222-60004	5
12222E	Five array cards	12222-60005	6
12222F	Six array cards	12222-60006	7
12222G	Seven array cards	12222-60007	8
12222H	Eight array cards	12222-60008	9
* Accessory to the 12205A card.			

D-5955-8873-51

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 16	
16 17 19 21 22 23 26 29 30 32 33 38 43	
46 48 61 63	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	4/4/82

CONNECTORS: J1 J2 J3 J4 J5 J6 J7 J8 J9

H G F E D C B A

FP. AR. BD. SEL −

FP. MEM. DATA +

FP. GND

FP. GND

FP. GND

FP. GND

FP. GND

FP. GND

FP. GND

FP. MEM. DATA +

FP. GND

FP. GND

FP. REF. EN −

FP. RD. EN +

FP. ISOGND1

FP. RAS +

FP. CAS

FP. WE −

FP. ISOGND2

FP. INIT. MODE +

FP. INIT. CLK +

FP. GND

FP. MEM. ADDR +

FP. GND

FP. GND

FP. GND

FP. GND

FP. GND

FP. GND

FP. GND

CONNECTORS: J1 J2 J3 J4 J5 J6 J7 J8 J9

FP. GND

FP. MEM. ADDR +

FP. NEXT. AR. BD −

FP. +5M

FP. CK. MEM. MC +

FP. ADDR. CLK +

FP. GND

FP. MEM. CH. IN +

FP. MEM. CH. OUT +

THIS SCHEMATIC COVERS EIGHT DISTINCT FRONTPLANE BOARDS: 12222A (J1 AND J2 ONLY) THROUGH 12222H (J1 THROUGH J9)

CONNECTOR J1 ATTACHES TO THE A900 MEMORY CONTROLLER BOARD; CONNECTORS J2 THROUGH J9 ATTACH TO A900 MEMORY ARRAY BOARDS.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DO NOT SCALE THIS DRAWING

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES.

TOLERANCES .XX ± .02 .XXX ± .005

SEE CORP. STD. 608

SUPERSEDES DWG.

TITLE: A900 Memory Frontplanes 12222A (2 conn.) through 12222H (9 conn.)

NEXT ASSEMBLY

FINISH

SCALE

HEWLETT PACKARD

PART NUMBER D-5955-8873-51

SHEET 1 OF 1

STOCK NO. 5280-0004

Chapter 11
Power Supply

11.1 Introduction

There are two power supplies used with the A900. A 440-watt supply is for the 20-slot backplane and a 300-watt supply is for the 16-slot backplane. Both supplies are modules that plug into the back (circuit trace side) of the appropriate backplane. The A-Series supplies are considered non-repairable in the field and, in case of failure, the entire unit should be replaced with an exchange unit from Hewlett-Packard and the original unit returned for repair.

This chapter of the manual provides information required to evaluate the supply's performance. Included are an overall operating description, control signal descriptions, mechanical and electrical specifications. Located at the back of this chapter are parts location diagrams (assembly drawings), parts lists, and schematics.

This chapter is divided into several main parts. The paragraphs under subheading 11.2 cover the 440-watt supply, Part No. 0950-1671; the paragraphs under subheading 11.3 cover the Micro/1000 300-watt supply, Part No. 0950-1646, the paragraphs under subheading 11.4 cover the HP 12154A battery backup module for Micro/1000 systems, and paragraphs under subheading 11.5 cover the HP 12159A 25-kHz module for Micro/1000 systems.

11.2 440-Watt Supply

The 440-watt supply, Part No. 0950-1671, is used with the 20-slot backplane. The supply operates from either 115 Vac or 230 Vac. There are four fans for cooling the power supply and the computer. The fans plug into either connector P7 for 115 Vac operation or into P8 for 230 Vac operation

The supply has four dc outputs at +5V, +5V memory backup (+5M), +12V, and -12V. It also provides 25 kHz ac power that is used as a power source for certain I/O cards. The +5M battery backup (BB) and the 25 kHz ac outputs are optional and are provided by separate cards that plug into the supply. If the battery backup is not installed, a jumper card must be placed in the BB connector of the supply. A block diagram of the 440-Watt supply is shown in Figure 11-1.

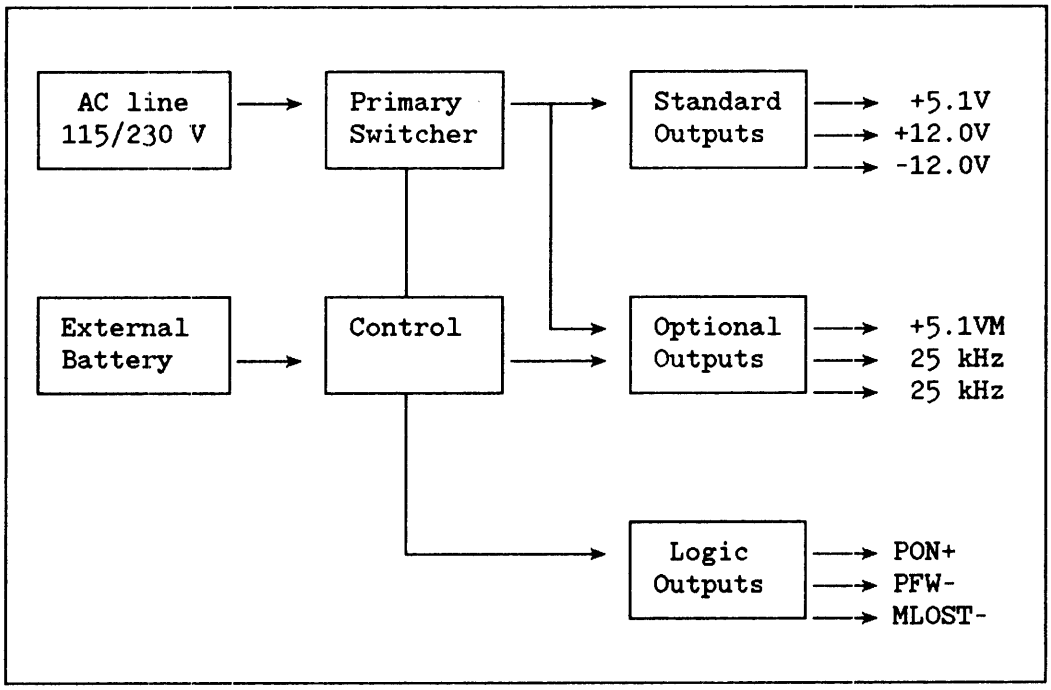


Figure 11-1. 440-Watt Power Supply Block Diagram

11.2.1 Logical Signals

The power supply provides logical control signals to the computer to indicate power availability so that appropriate action can be taken.

11.2.1.1 PON+

PON+ is a signal that indicates the condition of the dc outputs. When the outputs are within specification, PON+ will be 2.4V to 5.2V. When the outputs are outside of specification, PON+ will be 0.2V plus or minus 0.2V. This definition includes the time when ac power is not applied (i.e., when ac power is down, the PON+ signal should be the out-of-specification condition.)

11.2.1.2 PFW-

The PFW- signal indicates the condition of ac power into the supply. When the input line voltage is above the "power fail trip point", PFW- is 2.4V to 5.2V. When the input line voltage is below the "power fail trip point", PFW- is 0.2V plus or minus 0.2V.

11.2.1.3 MLOST-

The MLOST- indicates the condition of the memory backup voltage as the main supply is being powered up. At all other times this signal is of no importance to the system. MLOST- is a pulse that is valid for 1 millisecond before and 5 millisecond after the rising edge of PON+. The MLOST- pulse during power up will be 2.4V to 5.2V if the memory supplies were within specification during the last power down. If the memory supplies are not within specification, MLOST- will be 0.2V plus or minus 0.2V.

11.2.2 Mechanical Specifications (440W Supply)

The overall mechanical dimensions and connector locations of the 0950-1671 supply are shown in Figure 11-2. The connector specifications are given in Table 11-1.

The cooling air flow should be a minimum of 70 CFM of air flowing across the power board in the direction indicated in Figure 11-2. Power supply assembly diagrams are provided at the rear of this section of the manual.

Table 11-1. Connector Specifications (440W Supply)

CONNECTOR	AMP PART NO.	AMP MATING NO.
P1/P3	Edge Card	
P2/P4	Edge Card	
P5	9-350255-2	350240
P6	9-350264-2	350243
P7	207584-1	207396-1
P8	207584-1	207396-1
P9	207365-1	207360-1

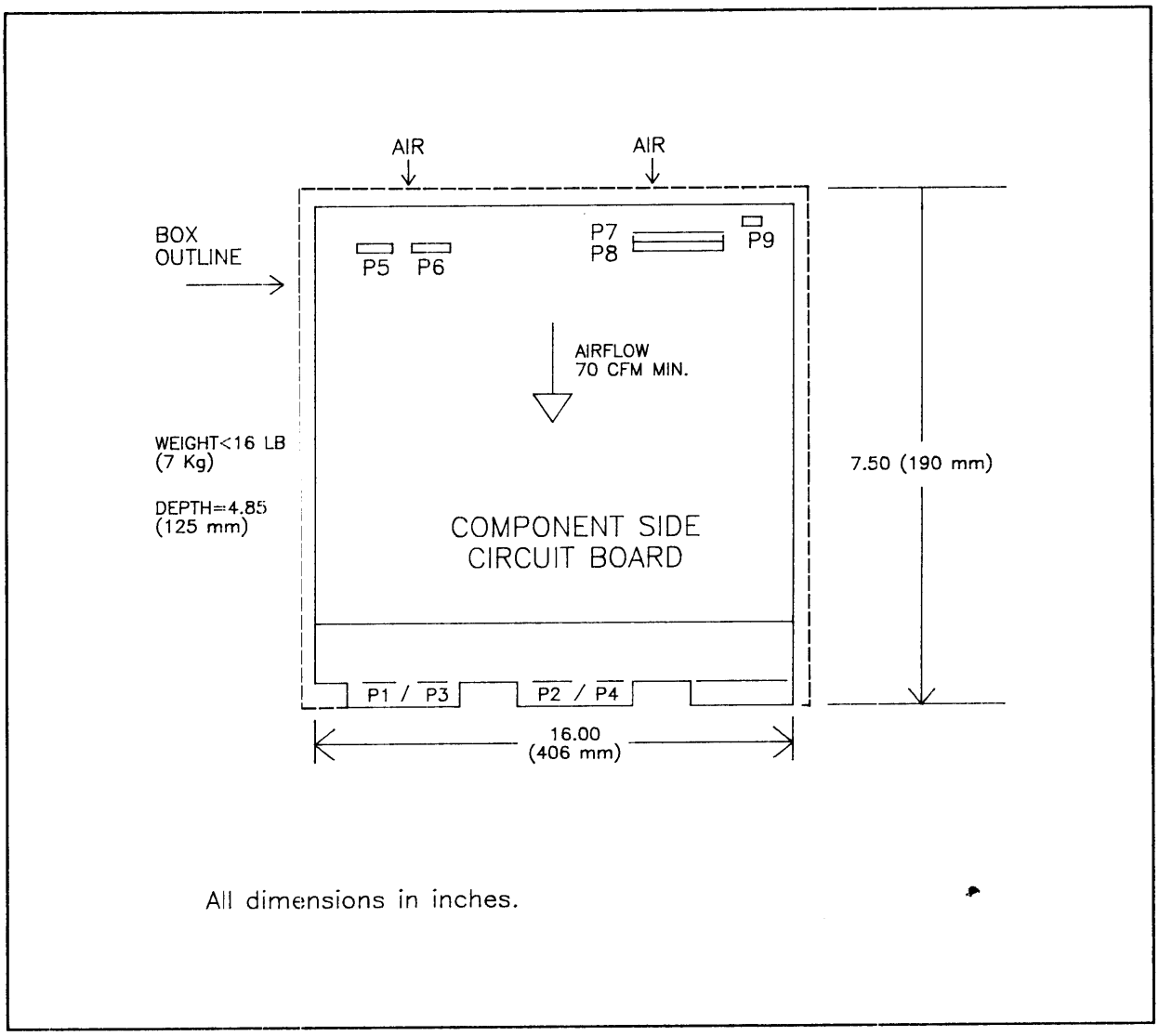


Figure 11-2. Dimensions and Connector Locations (440W Supply)

11.2.3 Electrical Connections (440W Supply)

The electrical contacts for the 440 watt power supply are provided by nine connectors. Two of these are edge-card connectors that plug into the backplane. A power supply connector diagram is shown in Figure 11-3, and the electrical connector pin definitions are given in Table 11-2.

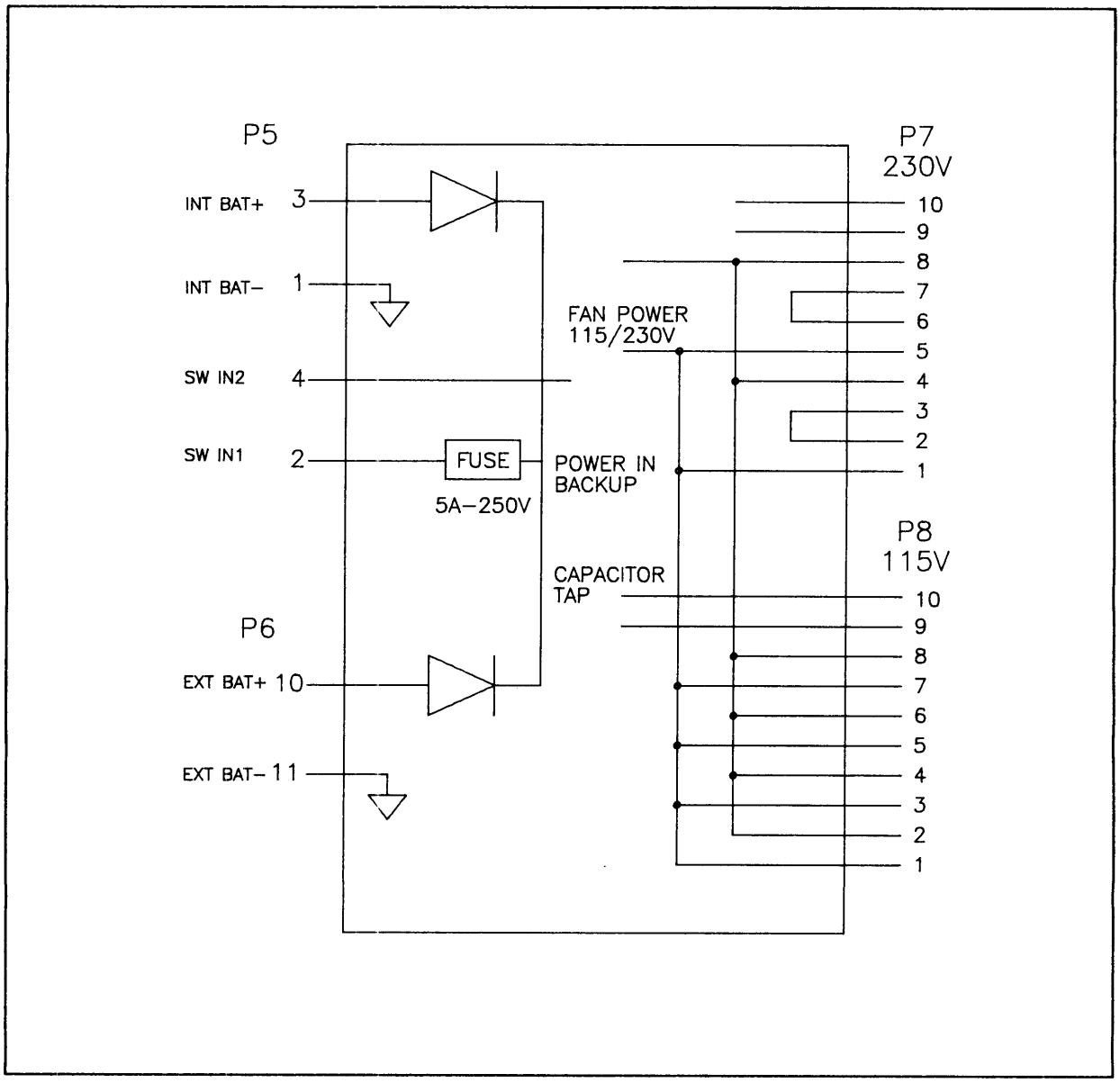


Figure 11-3. 440 Watt Power Supply Connector Diagram

Table 11-2. Electrical Connections (440W Supply)

P1 DC OUTPUT CONNECTOR (PC EDGE BOARD)	
Pin Number	**Signal Name**
1 thru 36	+5.1 Volts
37 thru 50	Common
P2 DC OUTPUT CONNECTOR (PC EDGE BOARD)	
Pin Number	**Signal Name**
1 thru 28	Common
29 thru 32	+12 Volts
33, 34	-12 Volts
35 thru 38	+5.1 Volts Memory Backup
39 thru 42	25 kHz Phase 1
43 thru 46	25 kHz Phase 2
47	PON+
48	PFW-
49	MLOST-
50	+5.1 Volts Memory Sense
P5 BATTERY SWITCH CONNECTOR	
Pin Number	**Signal Name**
2	Switch in 1
4	Switch in 2
1	Internal Battery -
3	Internal Battery +
P9 AC LINE INPUT	
Pin Number	**Signal Name**
1	AC Line
2	No Connection
3	AC Neutral

Table 11-2. Electrical Connections (440W Supply) (Continued)

P7/P8 AC LINE CONFIGURATION / FANS	
Pin Number	**Signal Name**
1	Fan #1
2	Fan #1
3	Fan #2
4	Fan #2
5	Fan #3
6	Fan #3
7	Fan #4
8	Fan #4
9	230v / 115v
10	230v / 115v
P6 TEST POINTS / EXTERNAL BATTERY	
Pin Number	**Signal Name**
1	+5V Test
2	+12V Test
3	-12V Test
4	+5VM Test
5	PON
6	PFW
7	MLOST
8	25 kHz Test
9	25 kHz Test
10	Battery +
11	Battery -
12	Common

11.2.4 Electrical Specifications (440W Supply)

The electrical specifications of the 440 watt supply are provided below in several tables. Ac line input specifications are given in Table 11-3, battery input specifications are given in Table 11-4, and supply output specifications are given in Table 11-5.

Table 11-3. Input Electrical Specifications (440W Supply)

AC LINE SPECIFICATIONS

These specifications do not include the power required for the fans.

	Min	Nominal	Max	
Range 1				
Voltage	84	120	140	Volts RMS
RNS Current (Max)	9.4	7.2	6.2	Amps
Inrush	-	-	136	Amps
Range 2				
Voltage	176	230	278	Volts RMS
RMS Current (Max)	4.7	3.7	3.1	Amps
Inrush	-	-	262	Amps
Carry Over	10.6	-	-	mSec
PFW Trip Point				
Range 1	-	-	84	Volts RMS
Range 2	-	-	176	Volts RMS
Line Frequency	47	60	67	Hz
Line Fuse	-	-	10	Amps
Input Power	-	-	700	Watts

Note: Power supply input operation permits input transients of up to 3000V for periods of not less than 10 μs.

Table 11-4. Battery Input Specification (440W Supply)

	MINIMUM	NOMINAL	MAXIMUM	
Battery Voltage	10.0	12.0	14.4	Volts
Discharge, Continuous	-	-	40.0	Amps
Internal Resistance	-	10.0	-	mohms

Note: 10.0V is the approximate input disconnect voltage. Disconnect occurs when Output #1 (5.1V) drops to 4.9V, as measured at the battery backup board (coincident with the assertion of MLOST-.

Table 11-5. Output Electrical Specifications (440W Supply)

Maximum Dynamic Load: **10% over 10 microseconds**

Output Stress Conditions Allowed:

a. Supply will recover from a shorted regulated output and excessive ambient temperature.

b. Over rated operated temperature.

Output Regulation (Note 4):

Output # 1	Nominal Voltage	5.1	Volts	
	Maximum Current	70	Amps	(1) (5)
Regulation	0.0 to 3.0 Amps	+10%	-10%	
	3.0 to 6.2 Amps	+5%	-5%	
	6.2 to 70.0 Amps	+2%	-2%	
Output # 2	Nominal Voltage	12.0	Volts	
	Maximum Current	5.6	Amps	
Regulation	0.0 to .03 Amps	+10%	-10%	
	.03 to 5.6 Amps	+6%	-3%	
Output # 3	Nominal Voltage	-12.0	Volts	
	Maximum Current	3.5	Amps	
Regulation	0.0 to .10 Amps	+12%	-12%	
	.10 to 3.5 Amps	+6%	-6%	

Table 11-5. Output Electrical Specifications (440W Supply) (Continued)

Output # 4 (opt.)	Nominal Voltage	5.1	Volts
	Maximum Current	10.0	Amps (2)
Regulation	0.0 to .10 Amps	+10%	-10%
	.10 to 10.0 Amps	+2%	-2%
Output # 5 (opt.)	Nominal Voltage	39	Volts RMS (5)
	Split Phase	19.5	Volts RMS
	Maximum Current	1.5	Amps
Regulation	0.0 to .02 Amps	+10%	-12%
	.02 to 1.5 Amps	+8%	-8%
Output # 6 (opt.)	Battery Charger		
	Minimum Current less than	.050	Amps (3)
	Maximum Current	.200	Amps
	Maximum Voltage	14.4	Volts
Output # 7	Fan Power		
	Nominal Voltage	115	Volts RMS
	Maximum Current	1.25	Amps

NOTES: (1) When no battery backup module is installed, the Output #4 current is supplied by Output #1. The total current drawn from Output #1 will not exceed 70 Amp.

(2) Output #4 shall be limited to 7 Amps when the 0950-1666 battery backup module is installed.

(3) When the battery is fully charged.

(4) Although the sum of the maximums listed above exceeds the 440 Watt specification of the power supply front end, not all of the outputs will be at maximum load at the same time and the actual maximum load will never exceed 440 Watts (not including fan power).

(5) When the maximum load is applied to Output #5 the load on Output #1 will not exceed 64 Amps.

11.2.5 Environmental Specifications (440W Supply)

The environmental specifications of the 0950-1671 440-watt power supply are provided in Table 11-6.

Table 11-6. Environmental Specifications (440W Supply)

Non Operating Temperature:
-40 deg C to 75 deg C

Operating Temperature:
0 deg C to 55 deg C
Type Tested
-5 deg C to 60 deg C (to insure margins)

Operating Survival Temperature:
-20 deg C to 65 deg C

Operating Humidity:
5% to 95% at 40 deg C wet bulb temperature

Vibration:

Sweep
From 5 to 55 Hz and back at a rate of one octave per minute, with an excursion of .015", for 15 minutes

Resonance
At each resonant point, not to exceed 4 points, dwell for 10 minutes at the following excursions:

5 - 10 Hz	.125"
11 - 25 Hz	.060"
25 - 55 Hz	.015"

Shock:

30g peak force applied as an 11 millisecond sine pulse. To be tested in each direction of each axis (6 tests).

Altitude:

Full operating temperature, at 440 Watts output power (not including fan power), at altitudes up to 10,000 feet, at 15,000 feet a derating of up to 10 deg C, of operating temperature, is allowed.

11.2.6 Replaceable Parts (440W Supply)

Replaceable parts lists for the 440W power supply are provided at the back of this chapter. Tables 11-15 and 16 cover the supply, Table 11-17 covers the battery backup board, and Table 11-18 covers the 25 kHz sinewave card. The parts can be located in Figures 11-11 through 11-14. These tables and figures are located at the back of this chapter in front of the schematics.

11.3 300-Watt Supply

The 300-watt supply, Part No. 0950-1646 is used with the 16-slot backplane for the Micro/1000 computers. The supply operates from either 115 Vac or 230 Vac. There are four fans for cooling (two fans blow across the supply and two fans blow through the I/O card cage). The fans plug into either connector J3 for 115 Vac operation or into J2 for 230 Vac operation

The supply has four dc outputs at +5V, +12V, -12V and +28V (backup battery source). The power supplies for the battery backup (BB) 5M voltage and the 25 kHz ac outputs are provided by separate optional cards that plug into the backplane. The main supply generates a 25 kHz square wave that is input to the 25 kHz sine-wave card as the source for its sine wave output. The 25 kHz sine wave is used as a power source for certain I/O cards. A block diagram of the 300-Watt supply is shown in Figure 11-4.

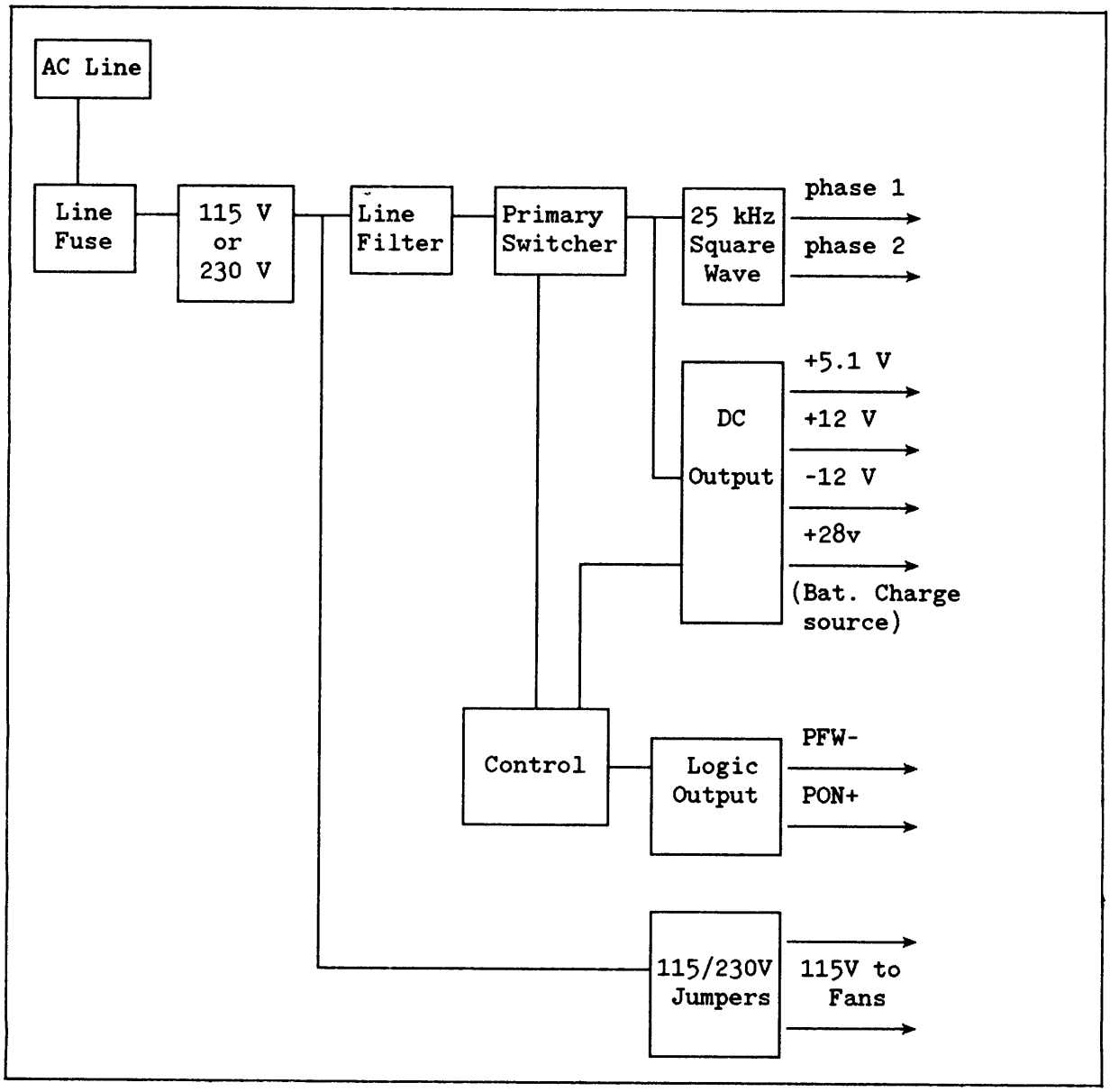


Figure 11-4. 300-Watt Power Supply Block Diagram

11.3.1 Logical Signals

The power supply logical control signals to the computer are the same as for the 440 watt supply described in the previous subsection, except that the MLOST- signal goes directly from the battery backup card to the backplane rather than through the power supply as in case of the 440 watt supply.

11.3.2 Mechanical Specifications (300W Supply)

The overall mechanical dimensions and connector locations of the 0950-1646 supply are shown in Figure 11-5. The power supply connectors are shown schematically in Figure 11-6. The connector specifications are given in Table 11-7.

The cooling air flow should be a minimum of 40 CFM of air flowing across the power board in the direction indicated in Figure 11-5. Power supply assemble diagrams are provided at the rear of this section of the manual.

Table 11-7. Connector Specifications (300W Supply)

CONNECTOR	PART NO.
P1	4-582390-4 (AMP)
J2	207378-1 (AMP)
J3	207378-1 (AMP)
J4	EAC-303 (SWITCHCRAFT)

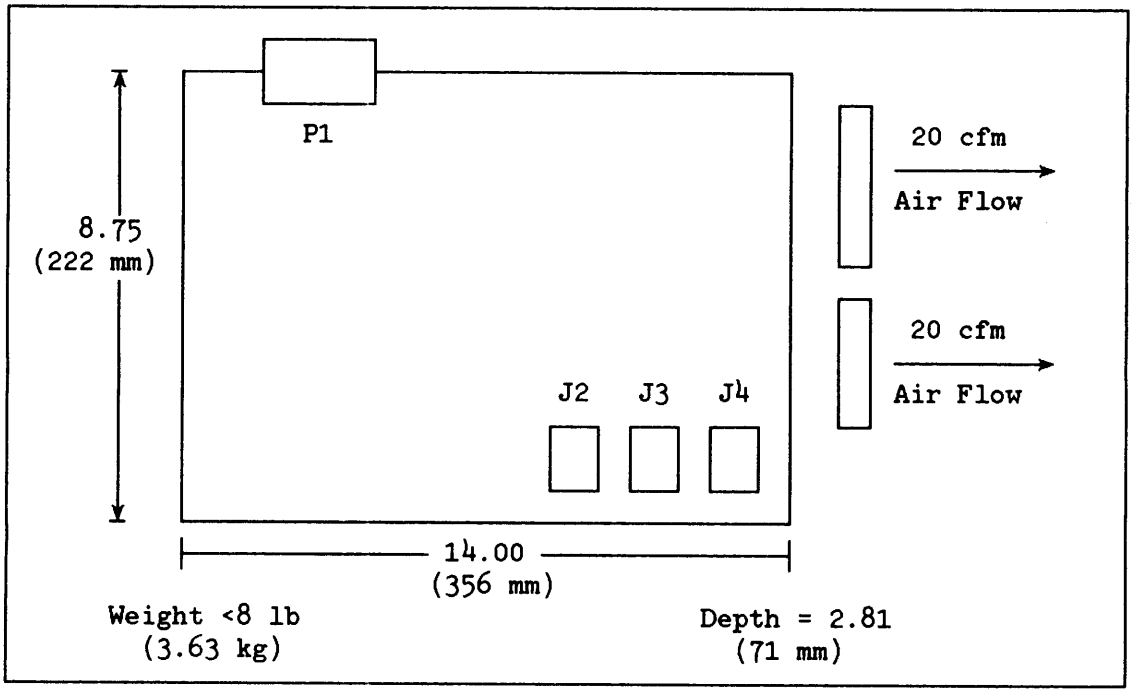


Figure 11-5. Dimensions and Connector Locations (300W Supply)

11.3.3 Electrical Connections (300W Supply)

The electrical contacts for the 300 watt power supply are provided by a plug and three jacks. The plug inserts into a jack on the backplane and the jacks are for the fans and ac input. A power supply connector diagram is shown in Figure 11-6. The electrical connector definitions are given in Table 11-8.

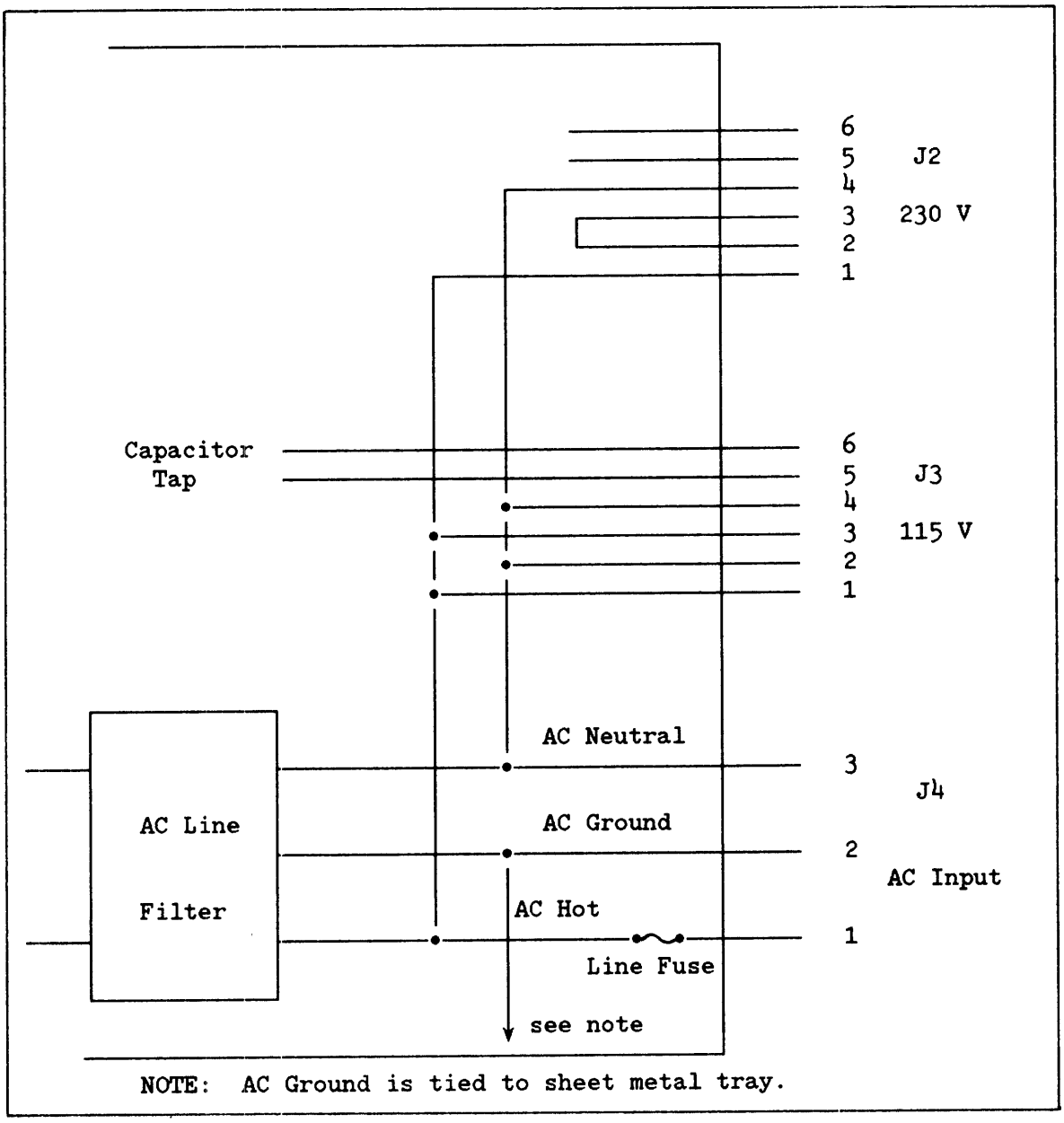


Figure 11-6. 300-Watt Power Supply Connector Diagram

Table 11-8. Electrical Connections (300W Supply)

ELECTRICAL CONNECTOR PIN DEFINITIONS	
P1 DC OUTPUT CONNECTOR	
Pin Number	**Signal Name**
24 thru 35	+5.1 Volts
10 thru 23	Common
6 thru 8	+12 Volts
5	-12 Volts
9	+28 Volts
3	25 KHz Phase 1
4	25 KHz Phase 2
1	PON+
2	PFW-
J4 AC LINE INPUT	
Pin Number	**Signal Name**
1	AC Line
2	AC Ground
3	AC Neutral
Pin 2 of this input connector must be tied to the sheet metal base.	
J2/J3 AC LINE CONFIGURATION / FANS	
Pin Number	**Signal Name**
1	Fan #1
2	Fan #1
3	Fan #2
4	Fan #2
5	230V / 115V
6	230V / 115V

11.3.4 Electrical Specifications (300W Supply)

The electrical specifications of the 300 watt supply are provided in the tables below. Ac line input specifications are given in Table 11-9, and supply output specifications are given in Table 11-10.

Table 11-9. Input Electrical Specifications (300W Supply)

AC LINE SPECIFICATIONS

These specifications do not include the power required for the fans.

	Min	Nominal	Max	
Range 1				
Voltage	84	115	140	Volts RMS
RNS Current (Max)	5.7	4.5	4.3	Amps
Inrush	-	-	102	Amps
Range 2				
Voltage	168	230	280	Volts RMS
RMS Current (Max)	2.8	2.3	2.1	Amps
Inrush	-	-	204	Amps
Carry Over	16.0	-	-	mSec
PFW Trip Point				
Range 1	-	-	84	Volts RMS
Range 2	-	-	168	Volts RMS
Line Frequency	47	60	67	Hz
Line Fuse	-	-	10.0	Amps
Input Power (Not including fans)	-	-	400	Watts

Notes:

1. The line filter reduces conducted noise to 2 dBuV below the VDE 0871 Level B conducted emission specification. Conducted noise is measured with the power supply configured for 230 Vac operation and its output loaded for 300W by a resistive load. For 115 Vac operation of the supply, conducted noise must be 2 dBV below the FCC Level B conducted emission specification.

2. Power supply operation permits input transients of up to 3000V for periods of not less than 10 s.

Table 11-10. Output Electrical Specifications (300W Supply)

Maximum Dynamic Load Change: 10% over 10 microseconds

Output Stress Conditions Allowed:

a. Supply will recover from a short to ground or to another regulated output and excessive ambient temperature.

b. Over rated operated temperature.

Output Regulation:

Note: For the following specifications to be valid Output #1 will have at least a 3.0 amp load. With a load less than 3.0 amps on Output #1, the maximum ripple on outputs #1, 2, 3, 4, and 6 must not exceed 1.5 volts peak to peak.

Output # 1	Nominal Voltage	5.1	Volts
	Maximum Current	50	Amps
Regulation	0.0 to 3.0 Amps	+10%	-10%
	3.0 to 6.2 Amps	+5%	-5%
	6.2 to 50.0 Amps	+2%	-2%
Ripple	Maximum Ripple	0.10	Volt
Output # 2	Nominal Voltage	12.0	Volts
	Maximum Current	7.0	Amps
Regulation	0.0 to .03 Amps	+10%	-10%
	.03 to 7.0 Amps	+6%	-3%
Turn-on Surge	9.0 Amps (for 10 sec. max.)	+6%	-30%
Ripple	Maximum Ripple	0.12	Volt
Output # 3	Nominal Voltage	-12.0	Volts
	Maximum Current	3.0	Amps
Regulation	0.0 to .10 Amps	+12%	-12%
	.10 to 3.0 Amps	+6%	-6%
Ripple	Maximum Ripple	0.12	Volt
Output # 4	Square Wave		

The Square Wave outputs must be in regulation when the load on +5.1 Volts is greater than 6.2 Amps.

	Min	Nominal	Max	
Phase to Phase	11.20	11.87	12.54	Volts RMS
Phase to Ground	5.60	5.94	6.27	Volts RMS
RMS Current	0.00	-	3.30	Amps/Phase
Frequency	24k	28k	32k	Hertz
Output Power	-	-	36	Watts

Table 11-10. Output Electrical Specifications (300W Supply) (Continued)

Output # 5	Fan Power		
	Nominal Voltage	115	Volts RMS
	Maximum Current	1.25	Amps
Output # 6	Nominal Voltage	+28.0	Volts
	Maximum Current	2.50	Amps
Regulation	0.0 to 2.5 Amps	+20%	-20%
Ripple	Maximum Ripple	0.30	Volt

Note:
Although the sum of the maximums listed above exceeds the 300 Watt specification of the power supply front end, not all of the outputs will be at maximum load at the same time and the actual power is 325 watts for a maximum of 10 seconds.

11.3.5 Environmental Specification (300W Supply)

The environmental specifications of the 0950-1671 300-watt supply are the same as for the 440-watt supply described in the subsection 11.2 above.

11.3.6 Replaceable Parts (300W Supply)

Replaceable parts lists for the 300W power supply are provided in Table 11-19 and they may be located in Figure 11-15. The table and figures are located in the back of this chapter in front of the schematics.

11.4 HP 12154A Battery Backup Module

The HP 12154A battery backup module for the Micro/1000 computers is designed to provide current that will retain the current status of the system in memory if ac power is interrupted. The Hewlett-Packard part number for this card is 12154-60001. The schematic for this card is shown in Figure 11-7.

11.4.1 Configuration

The battery backup module is installed in the 16-slot backplane of the Micro/1000 A-series computers. The sixth, seventh, and eighth physical slots down from the top of the left side of the card cage are dedicated to the battery backup module. There are three slots reserved to account for the height of the batteries and the space necessary for component heat sinks.

11.4.2 Physical Description

The module (or card) dimensions are the following:

Width: 6.75 inches (171 mm) Standard card width

Depth: 12.75 inches (324 mm) Attaches to bulkhead connector panel

Max. Component Height: 2.0 inches (51mm) for D-size battery packs

11.4.3 Electrical Specification

The module is comprised of the battery charging circuit, enable/disable circuit, D-size battery pack, and a control circuit. When power is present, the module will charge the 9.6V Nicad (nickel/cadmium) batteries. When power fails, the 9.6V battery voltage is reduced to 5.1V through the regulator, and supplies the +5M power line to sustain memory.

The module derives its power from the 12V dc output of the system power supply. When the voltage of the batteries drops below 8.0V, the module will inhibit the +5.1V memory regulator circuit.

11.4.4 Replaceable Parts

Replaceable parts for the HP 12154A are listed in Table 11-11 and a parts location diagram for it is shown in Figure 11-8. The parts manufacturer's names and addresss are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03508	GE Co Semiconductor Prod Dept	Auburn, NY	13201
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
12969	Unitrode Corp	Watertown, MA	02172
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
3L585	RCA Corp Solid State Div	Somerville, NJ	
56289	Sprague Electric Co.	North Adams, MA	01247
75915	Littlefuse Inc	Des Plaines, IL	60016

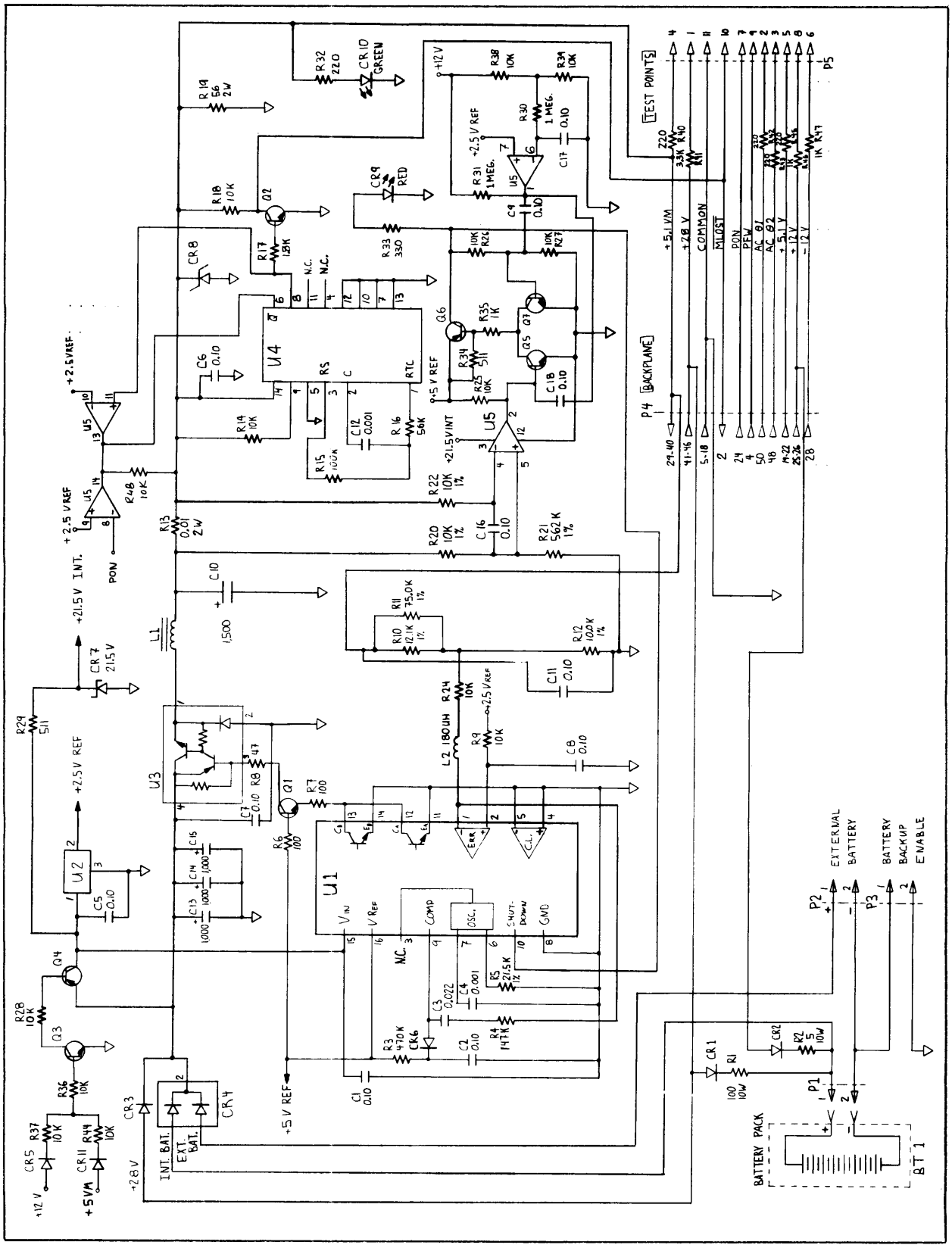


Figure 11-7. HP 12154A Battery Backup Module Schematic

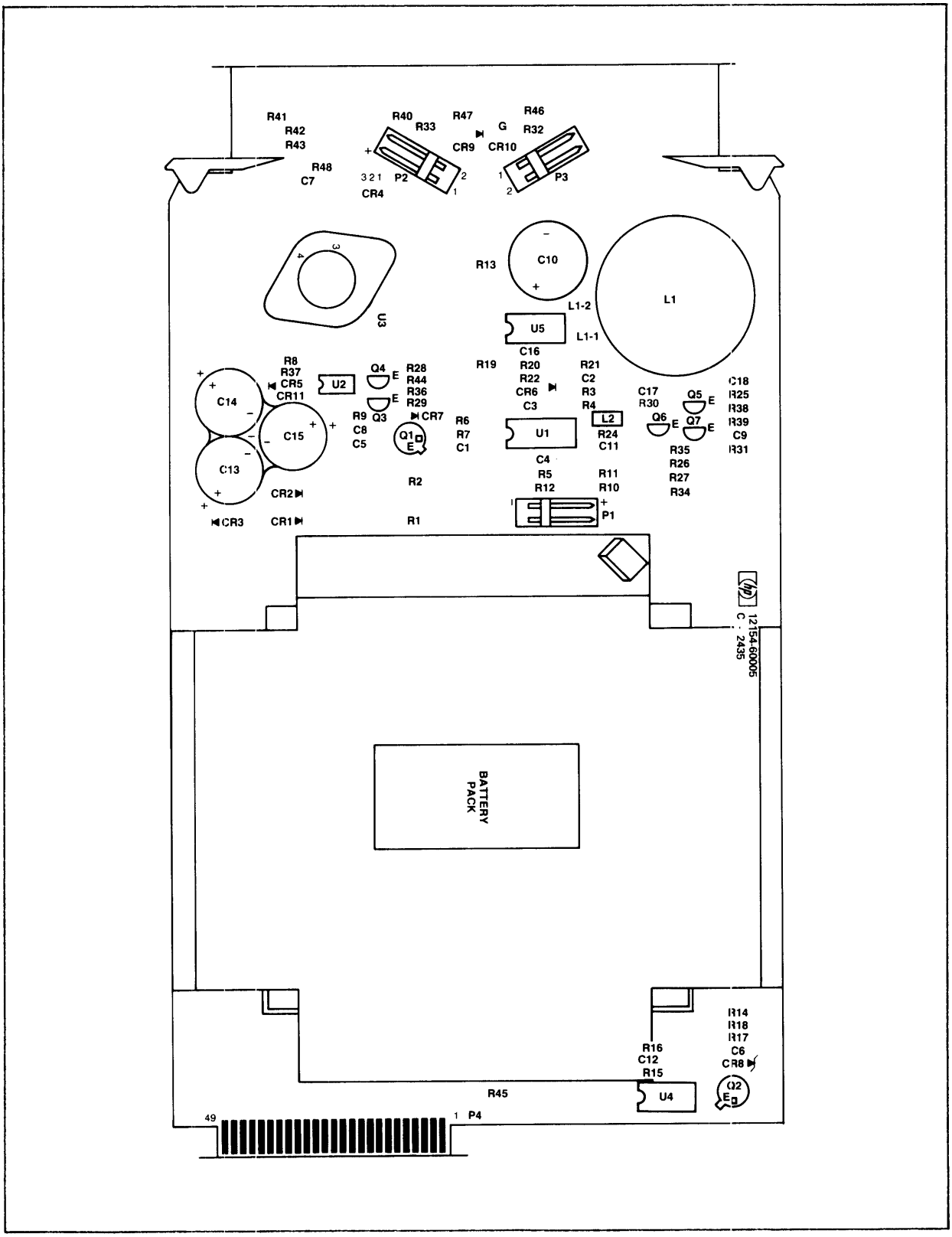


Figure 11-8. HP 12154A Replaceable Parts Location Diagram

Table 11-11. HP 12154A Replaceable Parts (Sheet 1 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12154-60005	3	1	PCA-BACKUP	28480	12154-60001
B1	1420-0321	1	1	BATTERY ASSEMBLY 9.6V NOM; RECHARGEABLE	28480	1420-0321
C1	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C2	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0160-4833	5		CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
C4	0160-4847	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0180-2997	0	1	CAPACITOR-FXD 1500UF+100-10% 25VDC AL	56289	674D158H025HJ5A
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4847	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C13	0180-3019	9	3	CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C14	0180-3019	9		CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C15	0180-3019	9		CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1901-0673	6	3	DIODE-PWR RECT 100V 5A SOS	03508	A15A
CR2	1901-0673	6		DIODE-PWR RECT 100V 5A SOS	03508	A15A
CR3	1901-0673	6		DIODE-PWR RECT 100V 5A SOS	03508	A15A
CR4	1906-0265	2	1	DIODE-RECT.	28480	1906-0265
CR5	1901-0050	3	4	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1902-3245	6	1	DIODE-ZNR 21.5V 5% DO-35 PD=.4W	28480	1902-3245
CR8	1902-0939	9	1	DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA	11961	1N5908
CR9	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
CR10	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
CR11	1901-0460	9	2	DIODE-STABISTOR 30V 150MA DO-7	28480	1901-0460
L1	9140-0811	8	1	INDUCTOR 356UH 10% 1.7DX1.2LG	28480	9140-0811
L2	9100-2279	2		INDUCTOR RF-CH-MLD 180UH 10% .105DX.26LG	28480	9100-2279
Q1	1854-0013	7	2	TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW	04713	2N2218A
Q2	1854-0013	7		TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW	04713	2N2218A
Q3	1854-0467	5	3	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q4	1853-0036	2	2	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
Q5	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q6	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
Q7	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
R1	0811-3644	5	1	RESISTOR 100 10% 10W PW TC=0+-300	28480	0811-3644
R2	0811-3656	9	1	RESISTOR 5 10% 10W PW TC=0+-300	28480	0811-3656
R3	0683-4745	6	2	RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
R4	0698-3452	1	2	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
R5	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R6	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R7	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R8	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R9	0683-1035	1	26	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R10	0757-0444	1		RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
R11	0757-0462	3	2	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
R12	0757-0442	9	8	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R13	0811-3511	5	1	RESISTOR .01 1% 2W PWW TC=0+-150	28480	0811-3511
R14	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R15	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R16	0683-5635	5		RESISTOR 56K 5% .25W FC TC=-400/+800	01121	CB5635
R17	0683-1825	7		RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
R18	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R19	0764-0013	5	1	RESISTOR 56 5% 2W MO TC=0+-200	28480	0764-0013
R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R21	0698-8824	1		RESISTOR 562K 1% .125W F TC=0+-100	28480	0698-8824
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R25	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R26	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R27	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R28	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R29	0757-0416	7	4	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R30	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R31	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055

Table 11-11. HP 12154A Replaceable Parts (Sheet 2 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R32	0683-2215	1	10	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R33	0683-3315	4		RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
R34	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R35	0683-1025	9	6	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R36	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R37	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R38	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R39	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R40	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R41	0683-3325	6	2	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
R42	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R43	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R44	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R45	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R46	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R47	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R48	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
U1	1826-1050	5	1	IC V RGLTR-SWG 4.9/5.1V 16-DIP-P PKG	28480	1826-1050
U2	1826-0544	0	1	V REF 8-DIP-C	04713	MC1403U
U3	1813-0114	3	1	IC V RGLTR TO-3	12969	PIC645
U4	1820-3516	0	1	IC TIMER CMOS	28480	1820-3516
U5	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N

11.5 HP 12159A 25 kHz Power Module

The HP 12159A is a module that takes the 25 kHz square-wave power from the 300W power supply and provides 25 kHz sine-wave power to the 16-slot backplane of a Micro-1000 computer for distribution to certain I/O cards having on-card power supplies. The module plugs into slot 8 of the backplane, and does not need forced air flow for cooling.

The Hewlett-Packard part number for this module is 12159-60001.

11.5.1 HP 12159A Specifications

The HP 12159A electrical specifications are provided in Table 11-12, and the connector pin definitions are listed in Table 11-13.

Table 11-12. HP 12159A 25-kHz Module Electrical Specifications

Input Specifications:

	Min	Nominal	Max	
Phase to Phase	11.28	12.00	12.72	Volts rms
RMS Current (max)	0.00	-	3.20	Amps
Frequency	24	25	32	kHz
Input Power	-	-	36	Watts

Output Specifications:

Maximum output power	30 Watts
Maximum distortion	10% total harmonic distortion
Maximum dynamic load change	10% of load over 10 microseconds

Output Stress Conditions:

The module shall recover, with no permanent damage from a shorted regulated output (it may be necessary to replace the fuse to resume normal operation)

Output Loading:

The load on the 25 kHz module can be applied from phase-to-phase (39 Vrms) or from phase-to-common (19.5 Vrms). Up to one half of the maximum rated power can be drawn from each phase (phase-to-common) or up to all of the rated power can be drawn phase-to-phase as long as the total power does not exceed the maximum rated power. The phase to common load need not be balanced between between the two phases.

Regulated Output Specification:

Nominal Voltage	39	Volts rms
Split Phase	19.5	Volts rms
Maximum Current	0.84	Amps

Regulation:

0.0 to 0.02 Amps	+10%	-12%
0.02 to 0.84 Amps	+8%	-8%

Table 11-13. HP 12159A Electrical Connector (P1) Pin Definitions

PIN	SIGNAL NAME
11-14	25 kHz1
15-18	25 kHz2
19-22	GND
23-26	AC02 (phase 2)
27-30	AC01 (phase 1)

11.5.2 HP 12159A Theory of Operation

For this theory of operation, refer to the schematic shown in Figure 11-9. The input transformer T1 steps the input 24 Volt peak-to-peak square wave up to 114 Volts peak-to-peak across 3-6. The winding 5-6 regulates the output as described below.

L1, L2, C1, and C2 are the main harmonic filters of the square wave. The regulator coil L3 also contributes to filtering.

Components R1, R2, C3, and C4 attenuate the noise generated by the switching diodes CR1 and CR2.

The regulator limits the amplitude of the output sine wave to less than 59 Volts and imposes no minimum value. The output of CR1, CR2, and C5 is the peak of the output sine wave. If this voltage exceeds 26 volts (zener diode CR3 voltage) plus the B-E drops across Q1 and Q2, then a current flows into the base of Q1, causing current flow through CR4 and Q2. This current adds to the main circuit current through L3, causing a voltage drop across L3. This voltage drop is a strong function of excessive output voltage which has the effect of providing regulation.

The regulator clamps the output to be less than or equal to the sum of the zener voltage plus the B-E drops of the transistors.

11.5.3 Replaceable Parts

Replaceable parts for the 12159A are listed in Table 11-14 and the names and addresses of the parts manufacturers are listed in the Manufacturer's Codes List below. The parts locations are shown in Figure 11-10.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

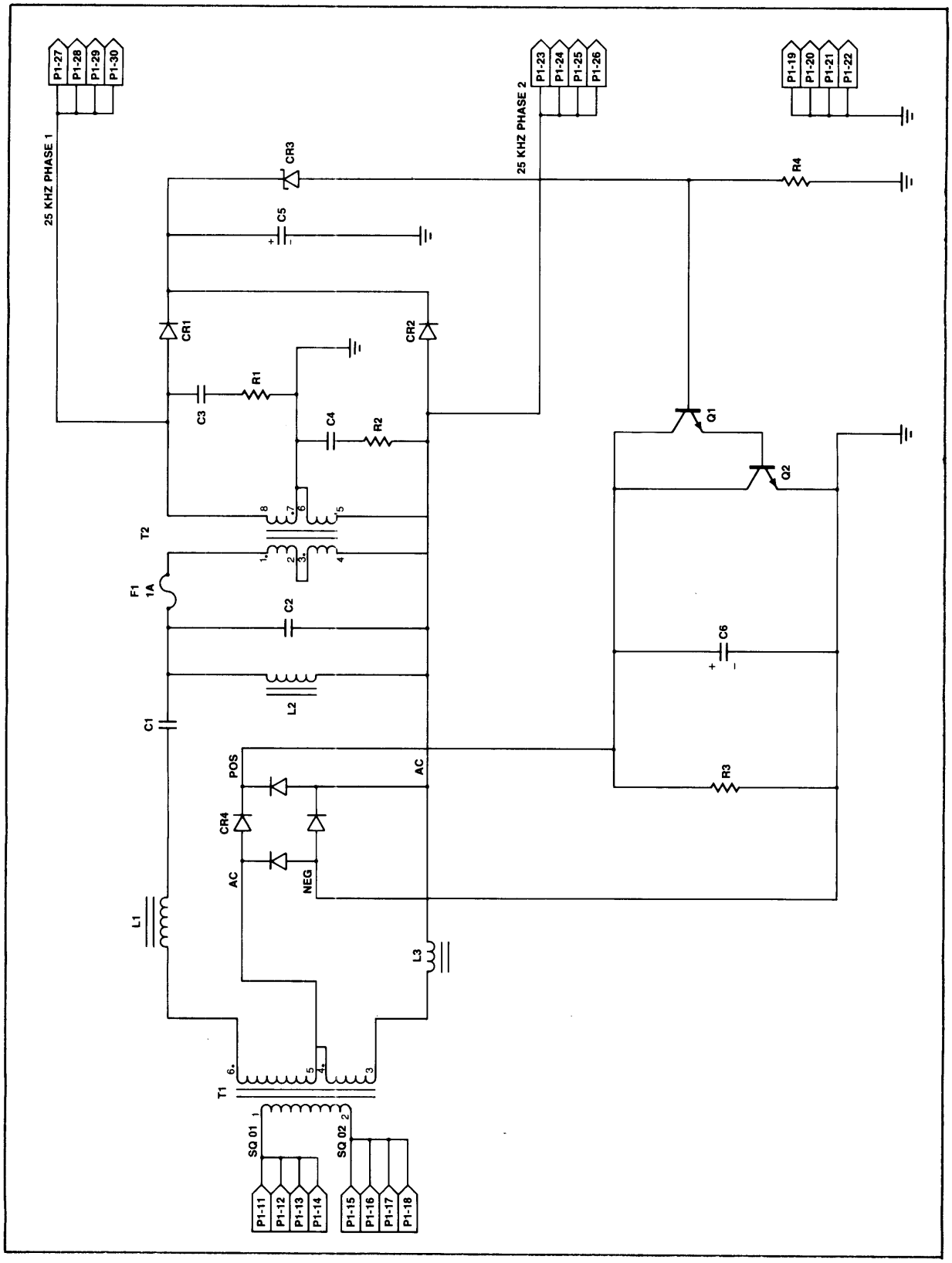


Figure 11-9. HP 12159A 25 kHz Power Module Schematic

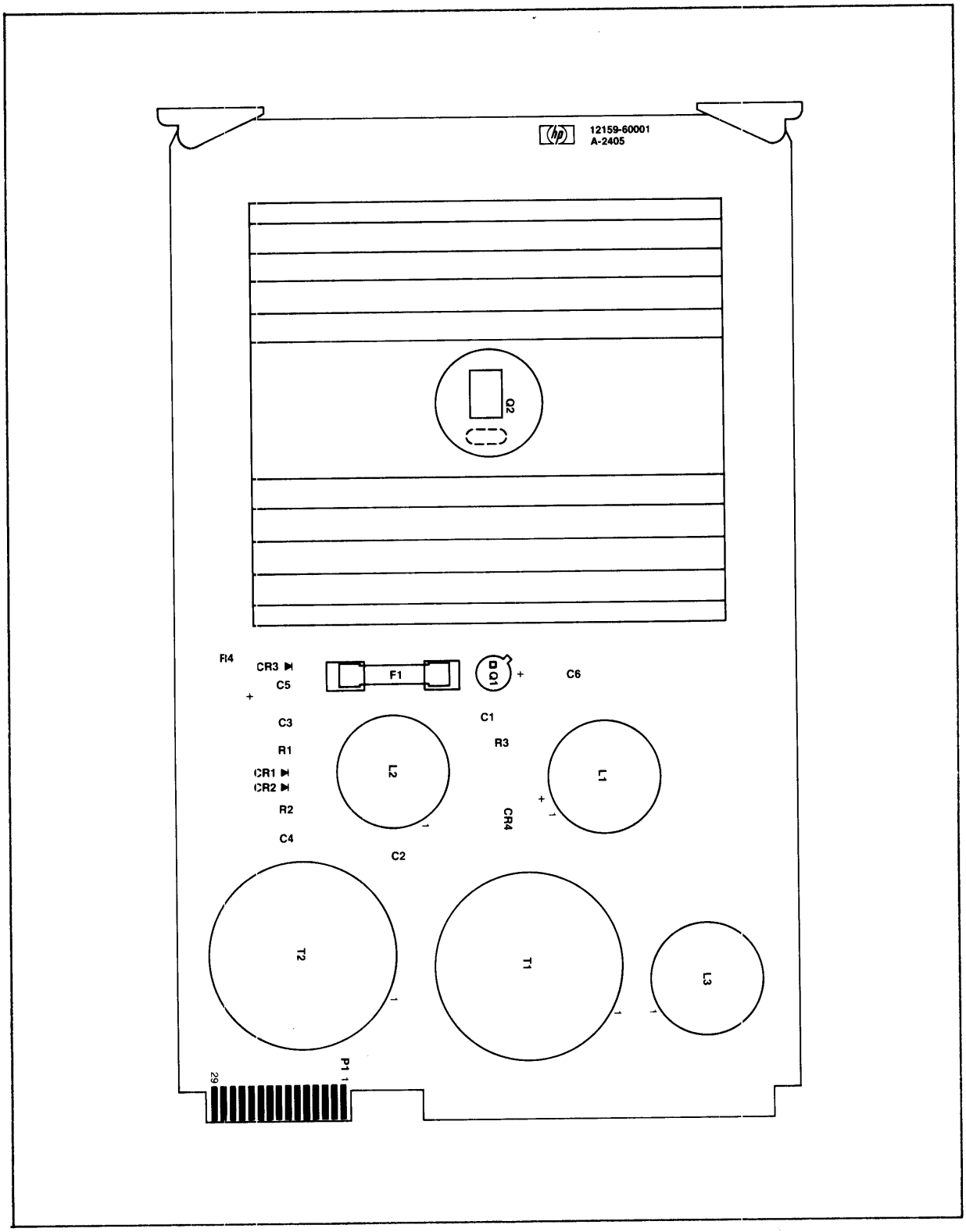


Figure 11-10. HP 12159A Replaceable Parts Locations

Table 11-14. HP 12159A Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12159-60001	8	1	PCA-25KHZ	28480	12159-60001
C1	0160-6040	0	2	CAP 0.1 UF	28480	0160-6040
C2	0160-6040	0		CAP 0.1 UF	28480	0160-6040
C3	0160-0161	4	2	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C4	0160-0161	4		CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C5	0180-0269	5	1	CAPACITOR-FXD 1UF+50-10% 150VDC AL	56289	30D105G150BA2
C6	0180-0141	2	1	CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
CR1	1901-0096	7	2	DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0096
CR2	1901-0096	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0096
CR3	1902-3269	4	1	DIODE-ZNR 26.1V 2% DO-35 PD=.4W	28480	1902-3269
CR4	1906-0077	4	1	DIODE-FW BRDG 400V 5A	28480	1906-0077
F1	2110-0001	8	1	FUSE 1A 250V NTD 1.25X.25 UL	75915	312001
L1	9140-0863	0	1	IND-FXD 240UH	28480	9140-0863
L2	9140-0861	8	1	IND-FXD 335 UH	28480	9140-0861
L3	9140-0862	9	1	IND-FXD 95UH	28480	9140-0862
Q1	1854-0079	5	1	TRANSISTOR NPN 2N3439 SI TO-5 PD=1W	3L585	2N3439
Q2	1854-0727	0	1	TRANSISTOR NPN 2N6474 SI TO-220AB PD=40W	3L585	2N6474
R1	0698-3620	5	2	RESISTOR 100 5% 2W MO TC=0+-200	28480	0698-3620
R2	0698-3620	5		RESISTOR 100 5% 2W MO TC=0+-200	28480	0698-3620
R3	0683-2735	0	1	RESISTOR 27K 5% .25W FC TC=-400/+800	01121	CB2735
R4	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
T1	9140-0859	4	1	XFMR	28480	9140-0859
T2	9140-0860	7	1	XFMR	28480	9140-0860

22K

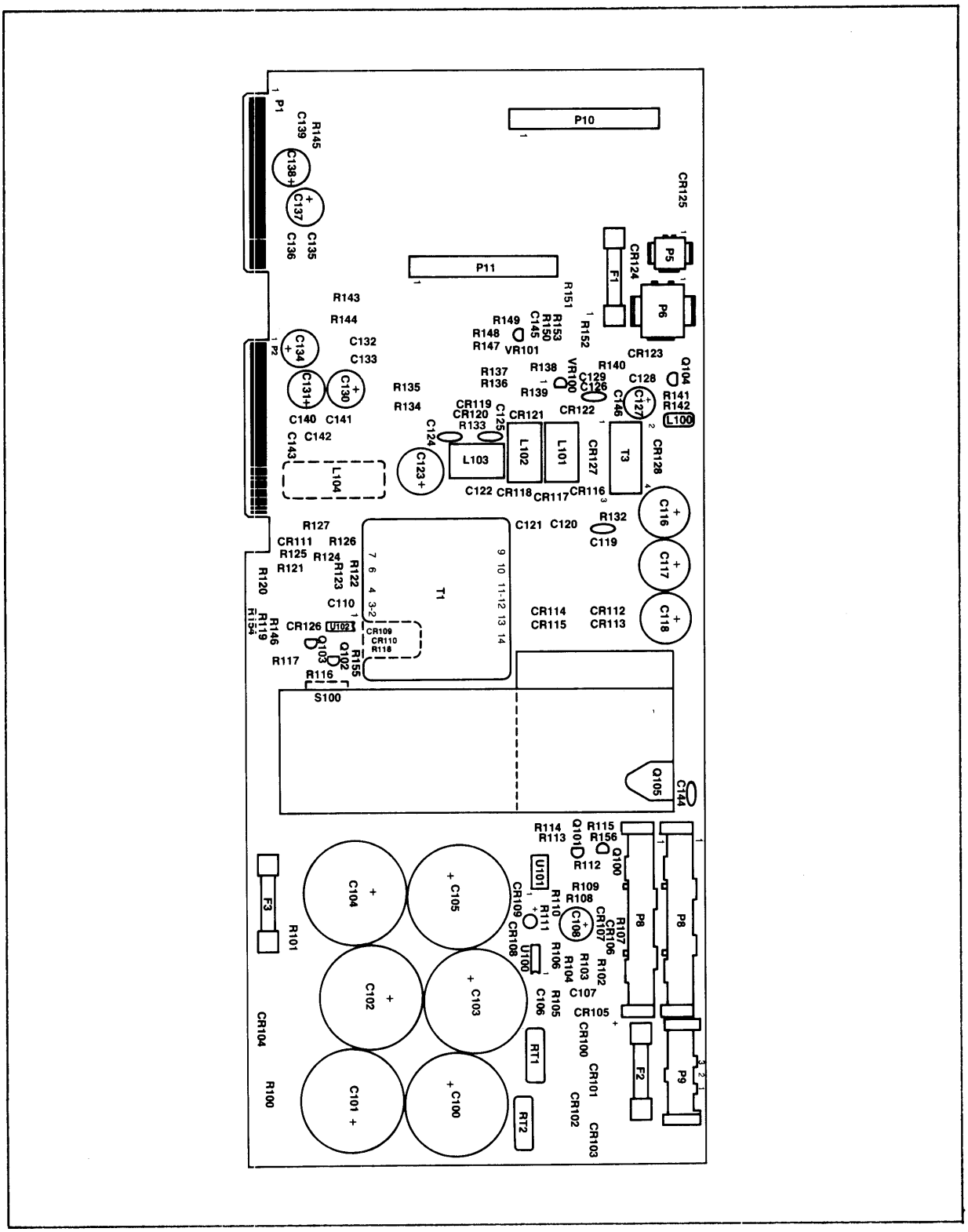


Figure 11-11. Parts Locations for Board 1, 440W Supply

Table 11-15. 440W Supply Board 1 Replaceable Parts (Sheet 1 of 3)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13713	P C B XL400-5411R	
002			
003	13825	SUB ASSY XFMR WIRING HARNESS BD	T1, (REF)
004	13824	SUB ASSY DIODE HEATSINK XL400-3411	R128, R129, R130, R131, C111, C112, C113, C114, CR112, CR113, CR114, CR115, (REF)
005	13835	BUS BAR RETURN	
006	13836	HEATSINK DIODE	
007			
008			
009			
010	13536	CAP ELECT 1000UF-200V SNAP-IN TERM	C100, C101, C102, C103, C104, C105
011	11659-02	CAP ELECT RAD LDS 3.3UF-250V DC	C108
012	10520-04	OBSOLETE(CAP ELECT 3.3UF-50V)	C109
013	10765-18	CAP ELECT 330UF 63V RD LDS VB	C123
014	11106-01	CAP ELECT R LDS 470UF-25VDC LO ESR	C130, C131
015	11110-01	CAP ELECT 1000UF 10V	C134, C137, C138
016	12951	CAP ELECT 10UF-100VDC LD ESR R LDS	C127
017	2032	CAP CERM .001UF 10% 1000VDC	C119
018	2060	CAP CERM 470PF-1KV	C124, C125, C126
019	10765-06	CAP ELECT 3.3UF 63V RD LDS VB	C109, REPLACES ITEM #012
020	12685-07	CAP MET POLY .47UF 5% 63/100V	C107
021	13594-02	CAP MET POLY .047UF 250V 5% .4"LS	C106, C128
022	12328-05	CAP MET POLY 0.33UF 63VDC 5%	C110, C133, C135
023	12657-07	CAP MET POLY RLD .10UF 10% 250VDC	C122, C139
024	12328-04	CAP MET POLY 0.22UF 63VDC 5%	C120, C121, C129, C132, C136, C140, C141, C142, C143, C146
025	13723-01	CAP ELECT 2200UF-16V RLD LOZ HI RIP	C116, C117, C118
026	13593-07	CAP MET POLY .01UF 630/1000V 5%	C145
027			
028	2105	CAP CERM 100PF-1KV	C144
029			
030	1021	DIODE HI CUR. AX LDS. 400V,6A MR754	CR100, CR101, CR102, CR103
031	10056-01	OBSOLETE(DIODE FAST RECV)	CR117, CR118
032	11380-04	DIODE FULL WAVE BRDG PREP/10868-04	CR105
033	1038	DIODE GEN PUR 1A IN4004 400VDC	CR106
034	12594	DIODE SILICON CASE DO-35,IN4448	CR107, CR109, CR110, CR126
035			
036	1043	DIODE GEN PUR AX LDS 3A 400V MR504	CR123, CR124, CR125
037	12577-02	DIODE RECT FAST RECV.16A 100V	CR116
038	14461-01	DIODE FST RECV 2A 100V AX LDS	CR119, CR120
039	1014	DIODE ZENER 500 MW 5.6V 5% IN5994B	CR104
040	1008	DIODE ZENER 400MW 15V 5% IN965A	CR108
041	11356-15	DIODE ZENER 500MW 8.2V 5% IN5998B	CR111
042	1042	DIODE FST RCV 200V 3A AX LDS MR852	CR121, CR122, CR127, CR128
043	10056-03	DIODE FAST RECV BYW 29-150	CR117, CR118, REPLACES ITEM #031
044			
045			
046	10180-01	FUSE 5A-250V NORMAL-BLOW	F1, F3
047	10865	FUSE 10 AMP 250V (BUSS ABC10)	F2
048	13799	HARNESS 2 PIN CONN	J14
049	13800	HARNESS 3 PIN CONN	J13
050	13801	HARNESS 4 PIN CONN	J12

Table 11-15. 440W Supply Board 1 Replaceable Parts (Sheet 2 of 3)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
051			
052	7421	WIRE RED 18 AWG 5" (1/4 X 1/4) UL10	JP7
053	10009-07	WIRE YEL 18 AWG 2.75 LG 1/4 X 1/4	JP3
054	7949	WIRE RED 18 AWG 3 5/8" (1/4 X 1/4)	JP8
055	10372-11	WIRE WHT 22 AWG 3.75" 1/4 X 1/4	JP4
056	10236-04	WIRE BLK 22 AWG 4.25" (1/4 X 1/4)	JP5
057	10008-06	WIRE ORN 18 AWG 3.75" 1/4 X 1/4	JP6
058			
059	14364	INDUCTOR OUTPUT 70A XL400-5411R	L104
060	10799	INDUCTOR 18 UH	L100
061	10899	INDUCTOR 14.4 UH	L101, L102, L103
062	13332	PCB PIN HEADER 4 CKT GOLD PIN	P5
063	13331	PCB PIN HEADER 12 CKT GOLD PIN	P6
064	13333-02	CONN PCB 10 CKT INLINE PIN HEADER	P7, P8
065	13333-01	CONN PCB 3 CKT INLINE PIN HEADER	P9
066	14565-04	CONN PCB 15/30 CONT PRS .125 CTR	P10, P11
067			
068			
069			
070	1016	TRANS PNP CASE TO-92 2N4126	Q104
071	12592	TRANS PNP CASE TO-92,MPS 2907A	Q102
072	12593	TRANS NPN TO-92 CASE MPS2222A	Q100, Q103
073	12591	TRANS NPN CASE TO 92 2N4124	Q101
074	14263-01	TRANS NPN POWER DARLING 10A TIP 140	Q105
075	3124	OBSOLETE(RES 150K OHM 1/4W)	R156
076	3077	OBSOLETE(RES 1.6K OHM 1/4W)	R146
077	3062	OBSOLETE(RES 390 OHM 1/4)	R141
078	3324	RES CF 150K OHM 5% 1/2W	R102
079	3091	OBSOLETE(RES 6.2K OHM 1/4W)	R104
080	3120	OBSOLETE(RES 100K OHM 1/4W)	R105, R119
081	3096	OBSOLETE(RES 10K OHM 1/4W)	R108, R112, R118, R125
082	3078	OBSOLETE(RES 1.8K OHM 1/4W)	R106
083	3122	OBSOLETE(RES 120K OHM 1/4W)	R111
084	3082	OBSOLETE(RES 2.7K OHM 1/4W)	R110
085	3072	RES CF 1K OHM 5% 1/4W	R109, R148, R154
086	3100	OBSOLETE(RES 15K OHM 1/4W)	R113
087	3088	OBSOLETE(RES 4.7K OHM 1/4W)	R115, R120, R121
088			
089	3093	OBSOLETE(RES 7.5K OHM 1/4W)	R126
090	3112	OBSOLETE(RES 47K OHM 1/4W)	R122
091	3108	OBSOLETE(RES 33K OHM 1/4W)	R124
092	10318-76	OBSOLETE(RES 3K OHM 1/4W)	R149
093	3084	OBSOLETE(RES 3.3K OHM 1/4W)	R155, R150
094	3256	RES CF 220 OHM 5% 1/2W	R133
095	10304-41	RES CF 100 OHMS 5% 1/2W	R132
096	3115	OBSOLETE(RES 62K OHM 1/4W)	R151
097	10318-102	OBSOLETE(RES 1.2 OHM 1/4W)	R142
098	3060	OBSOLETE(RES 330 OHM 1/4)	R136, R140
099	3064	OBSOLETE(RES 470 OHM 1/4W)	R138
100	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R153, R147
101	10233-84	RES MET OXIDE 27K OHM 5% 2W	R100, R101
102	10233-48	RES MET OXIDE 820 OHM 5% 2W	R127

Table 11-15. 440W Supply Board 1 Replaceable Parts (Sheet 3 of 3)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBEI	DESCRIPTION	REFERENCE DESIGNATORS
103	11313-51	RES MF 3.32K OHMS 1% 1/8W	R137
104	10232-57	RES MET OXIDE 1K OHM 5% 1 W	R117
105	10232-65	RES MET OXIDE 2.2K OHM 5% 1W	R116
106	3080	OBSOLETE(RES 2.2K OHM 1/4W)	R114
107			
108			
109	10522-29	RES WW 12K OHMS 5% 5W	R107
110	3820	RES WW 120 OHM 5% 2W BWH	R134, R135
111	3903	RES WW 10 OHM 5% 5W	R143, R144
112	10966-49	RES WW 1K OHM 10% 2W BWH	R145
113	3943	RES POT 5K VADJ MTURN .5W CERMET	R139
114	10519-16	RES POT 50K OHM VADJ STURN .5W CERM	R103
115	10519-10	RES POT 2K OHM VADJ STURN .5W CERM	R123, R152
116			
117			
118			
119			
120	3938	RES THERMISTOR DISC 5 OHM 15% ST LD	RT1, RT2
121	3911	THERMOSTAT SNAP-ACTING AUTO RESET	S100
122			
123	14159	TRANSFORMER T3 BIFILAR	T3
124			
125			
126			
127	10505	I C LOW POWER DUAL VOLT COMP LM393N	U100, U102
128	11498	I C OPTO-ISOLATOR OP1-1264B	U101
129	1071	I C SHUNT REG TL430	VR100, VR101
130	14381	TIE WRAP PUSH MOUNT	(REF), L104
131	11661-01	SPACER GLASS .225 OD .067 ID .185TH	(REF), R107, RT1, RT2
132	7501	TIE WRAP MEDIUM	(REF), L104
133	7500	TIE WRAP SMALL	
134	13887	INSULATOR	
135	13831	TRANSFORMER SUPPORT	(REF), T1
136	7015	FUSE CLIP PCB TYPE FOR 3AG FUSE	XF1, XF2, XF3
137	10006-12	WIRE BLU 18AWG 3.75"(1/4 X 1/4)	T3(REF)
138	10004-13	WIRE BLK 18 AWG 3.75"(1/4 X 1/4)	T3(REF)
139	10002-04	WIRE RED 18 AWG 5.50 (1/4 X 1/4)	(REF), S100
140	7578	SCREW P H 4-40 X 1/4	(REF), S100
141	7511	SCREW P H 6-32 X 1/2	(REF), H/S, T1
142			
143	7576	SCREW P H 6-32 X 1/4	Q105(REF)
144	7577	WASHER SPLIT LOCK #4	(REF), S100
145	7588	WASHER SPLIT RING LOCK #6	(REF), H/S, T1
146	7506	WASHER FLAT #6	(REF), H/S, T1
147	11828	WASHER METAL	(REF), Q105
148	12560	MTG HDW TO-220 NON CNDCT #4	(REF), CR116, CR117, CR118
149	10726-01	SPACER INSULATED #6 .250 DIA .125LG	
150	13979	STIFFENER 3.00 X 4.50	(REF), C100, C101, C102, C103, C104, C105
151	13980	STIFFENER .75 X 2.20	(REF), C116, C117, C118
152	13981	STIFFENER .50 X 1.00	(REF), C137, C138
153			
154			
155	12459	LABEL FUSE WARNING	(REF), C104
156	12569	LABEL,CSA MARK	
157	7740	LABEL DANGER HIGH VOLTAGE	(REF), C101

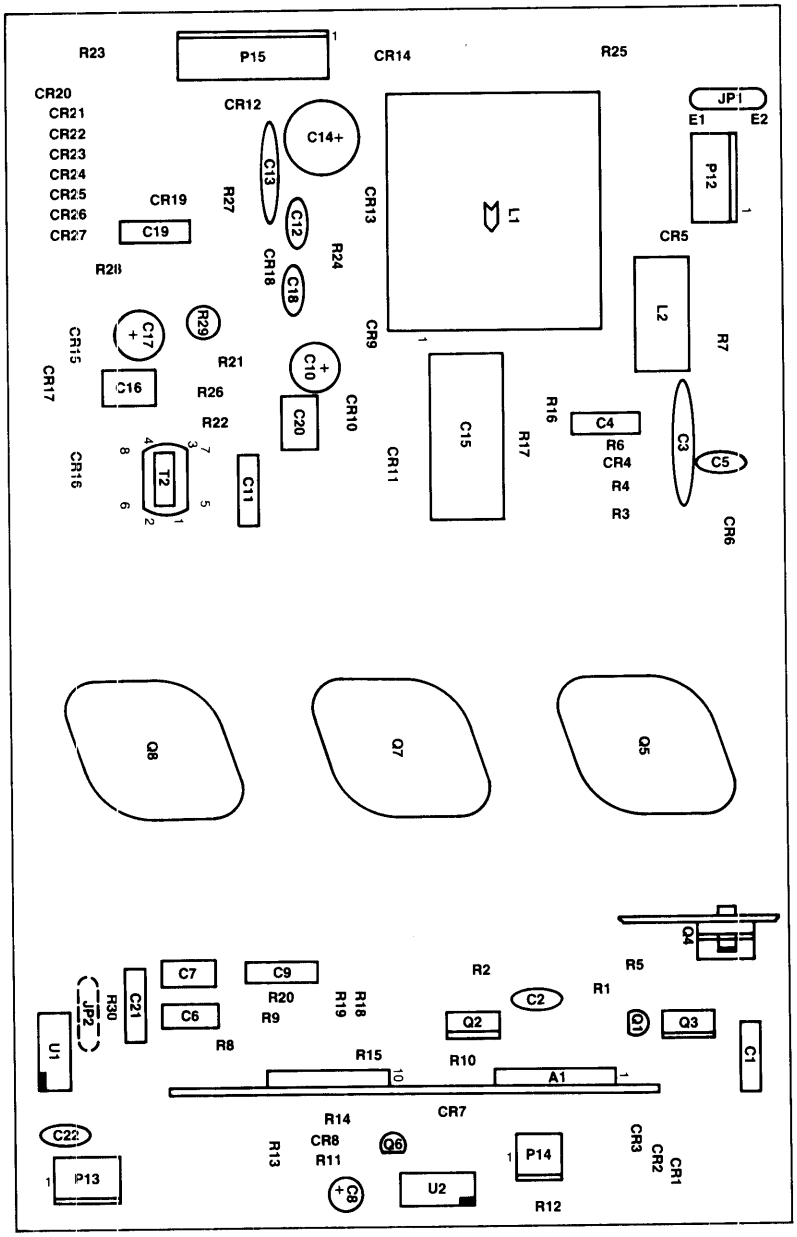


Figure 11-12. Parts Locations for Board 2, 440W Supply

Table 11-16. 440W Supply Board 2 Replaceable Parts (Sheet 1 of 2)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13619	TRANS NPN POWER 400V 15A 2N6678	Q5, Q7, Q8
002	1118	TRANS NPN POWER MJE13007	Q4
003			
004			
005			
006			
007	3098	OBSOLETE(RES 12K OHM 1/4W)	R30
008	3080	OBSOLETE(RES 2.2K OHM 1/4W)	R8
009	3046	OBSOLETE(RES 82 OHM 1/4W)	R9
010	3096	OBSOLETE(RES 10K OHM 1/4W)	R11
011	3104	OBSOLETE(RES 22K OHM 1/4W)	R10, R20
012	3064	OBSOLETE(RES 470 OHM 1/4W)	R1
013	10318-22	OBSOLETE(RES 16 OHM 1/4W)	R14
014	3048	OBSOLETE(RES 100 OHM 1/4W)	R13
015	3056	OBSOLETE(RES 220 OHM 1/4W)	R12
016	3135	OBSOLETE(RES 430K OHM 1/4W)	R19
017	3040	OBSOLETE(RES 47 OHM 1/4W)	R26
018	3024	OBSOLETE(RES 10 OHM 1/4W)	R6
019	10233-78	RES MET OXIDE 15K OHM 5% 2W	R2, R23
020	13598-08	RES MF UNCUT LDS 365K 1% 1/8W	R18
021	10232-95	RES MET OXIDE 47K OHM 5% 1 W	R21, R22
022	10233-30	RES MET OXIDE 150 OHM 5% 2W	R24, R27
023	10232-16	RES MET OXIDE 20 OHM 5% 1 W	R29
024			
025	3811	RES WW 10 OHM 10% 1W BW20F	R15, R3, R4
026	3816	RES WW .2 OHM 5% 2W BWH	R16, R17
027	12261-13	RES WW 10 OHM 10% 10W	R25
028	3812	RES WW 82 OHM 10% 1W BW20F	R5
029	3918	RES WW 5 OHM 5% 5W	R7
030	10048-65	RES WW 47 OHM 5% 2W BWH	R28
031			
032			
033			
034	12872-01	TRANSFORMER DRIVE,PC MT TWO CORE 4T	T2
035	11498	I C OPTO-ISOLATOR OP1-1264B	U2
036	12975-15	OPTO ISOLATOR SORTED VDE 390 ORN	U1
037	12854	CONN JACK CLOSED ENTRY P C SWAGE MT	E1, E2, E3, E4
038	11661-01	SPACER GLASS .225 OD .067 ID .185TH	(REF), R25
039	11399	ASSY MTG HDW TO-3 CNDCT PEM STUD	(REF), Q5, Q7, Q8
040	7509	SCREW P H 4-40 X 1/2	(REF), Q4, CR6
041	7503	NUT HEX 4-40	(REF), Q4, CR6
042	7602	WASHER INT TOOTH LOCK #4	(REF), Q4, CR6
043	7010	INSULATOR ALUM TO-220	(REF), Q4, CR6
044	11572	INSULATOR TO-220	(REF), Q4, CR6
045	7930	WIRE RED 22 AWG 1 1/2" (1/4, 1/4)T	(REF), T2
046	7202	ORTV 108 CLEAR	
047			
048			
049			
050			
051			
052			

Table 11-16. 440W Supply Board 2 Replaceable Parts (Sheet 2 of 2)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053	13730	P C B	
054	12983	CONTROL BOARD 723	A1
055			
056			
057			
058			
059			
060			
061	13834	HEATSINK TRANSISTOR	(REF), Q5, Q7, Q8
062	10346-01	CAP ELECT 10UF-16V RAD LDS	C8
063	12288	CAP ELECT 4.7UF 20% 100V LO ESR RLD	C10, C17
064	2071	CAP ELECT RAD.LEADS 10UF-250V	C14
065	2105	CAP CERM 100PF-1KV	C2
066	2003	CAP CERM .1UF +80%-20% 500VDC	C3
067	2073	CAP CERM DISC .001UF-3KV 20%	C12, C18
068	2062	CAP CERM 270PF-1KV	C5
069	2032	CAP CERM .001UF 10% 1000VDC	C22
070	2005	CAP CERM DISC .01UF 1KVDC 20% Z5U	C13
071	12328-04	CAP MET POLY 0.22UF 63VDC 5%	C6
072	12328-06	CAP MET POLY 0.47 63VDC 5%	C7
073	13593-05	CAP MET POLY .0047UF 630/1000V 5%	C9, C11, C21
074	12328-08	CAP MET POLY 1.0UF 63VDC 5%	C16, C20
075	13450-01	CAP MET POLY .1UF 100VDC 5% R LDS	C1, C4, C19
076	2080	CAP MET POLY 2UF-200VDC 10%	C15
077			
078			
079			
080			
081	14461-01	DIODE FST RECV 2A 100V AX LDS	CR20, CR21, CR22, CR23, CR24, CR25, CR26, CR27
082	13734	DIODE GEN PUR FST FWD REC IN4004	CR1, CR2, CR3, CR12, CR13, CR18, CR19
083	12594	DIODE SILICON CASE DO-35,IN4448	CR4, CR8
084	1045	DIODE FST RCV 100V 3A AX LDS MR854	CR5, CR14
085	11196	DIODE FAST RECV MR2404F	CR6
086	1028	OBSOLETE(DIODE RECTIFIER)	CR17, CR9
087	12260-04	DIODE HI CUR AX LDS. 30V,6A SR3773	CR10, CR11, CR15, CR16
088	11356-15	DIODE ZENER 500MW 8.2V 5% IN5998B	CR7
089	1155	DIODE FST RCV 1A 600V AX LD IN4937	CR17, CR9, REPLACES ITEM #034
090	10024-02	TERM PLUG .400	JP1
091			
092	13733	INDUCTOR 4MH	L1
093	11625	INDUCTOR 010467-01/02	L2
094			
095			
096	13195-01	CONN FRICTION LOCK 4 POS .156 CTR	P12
097	13195-04	CONN FRICTION LOCK 2 POS .156 CTR	P14
098	13195-05	CONN FRICTION LOCK 3 POS .156 CTR	P13
	13195-06	CONN FRICTION LOCK 7 POS .156 CTR	P15
	12592	TRANS PNP CASE TO-92,MPS 2907A	Q1, Q6
	12675	TRANS PNP HI VOLT 400V TO-126 CASE	Q3
	1005	TRANS NPN POWER TIP-50	Q2

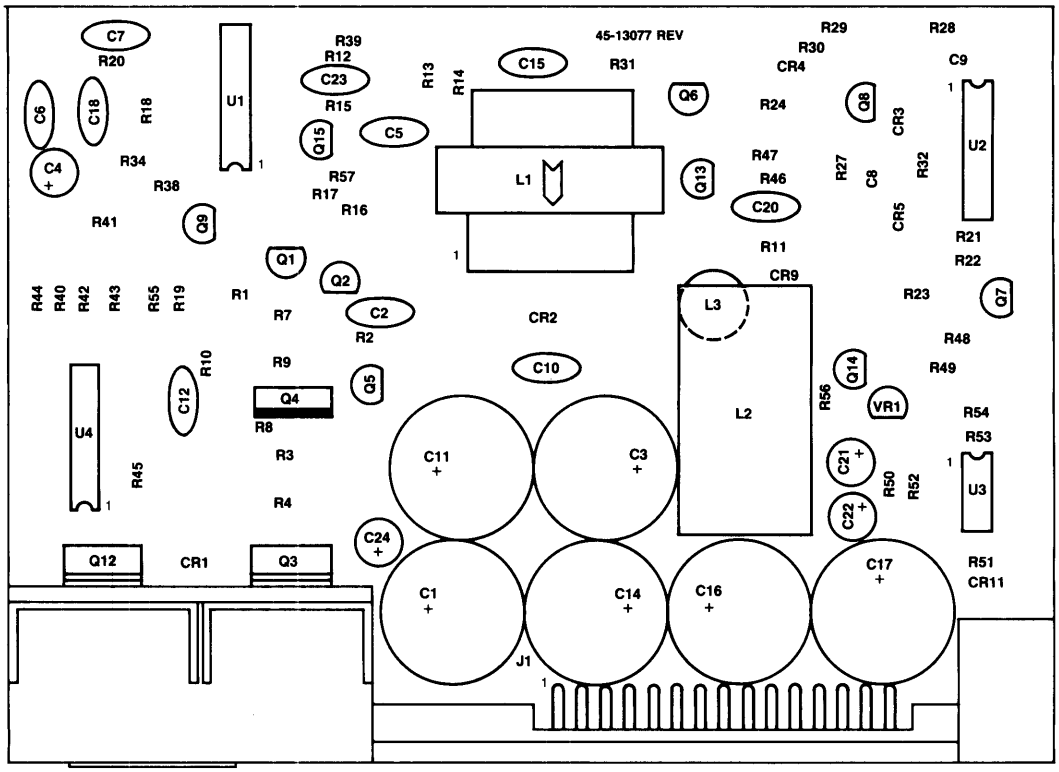


Figure 11-13. Parts Locations for Battery Backup Card (BB500)

Table 11-17. Battery Backup Card Option Replaceable Parts (Sheet 1 of 3)
(Boschert BB500 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13093	P C B	
002			
003			
004	2032	CAP CERM .001UF 10% 1000VDC	C2, C18
005	2008	CAP CERM .1UF-100V	C5, C10, C23
006	2120	CAP CERM .0022UF-1KV	C6, C12
007			
008			
009	2060	CAP CERM 470PF-1KV	C7
010	2062	CAP CERM 270PF-1KV	C15
011	2059	CAP CERM .01UF-100V	C20
012			
013			
014	10520-13	CAP ELECT 470UF 50V RD LDS VB	C1, C3, C11, C14, C16, C17
015	10520-05	OBSOLETE(CAP ELECT 4.7UF-50V)	C4
016	10520-02	OBSOLETED(CAP ELECT 1.0UF-50V)	C21
017	10346-01	CAP ELECT 10UF-16V RAD LDS	C22
018	10520-04	OBSOLETE(CAP ELECT 3.3UF-50V)	C24
019	10765-07	CAP ELECT 4.7UF 63V RD LDS VB	C4, REPLACES ITEM #015
020	13593-01	CAP MET POLY .001UF 630/1000V 5%	C8, C9
021	10765-06	CAP ELECT 3.3UF 63V RD LDS VB	C24, REPLACES ITEM #018
022	10541-03	CAP ALUM ELECT 1.0UF 100W VDC	C21, REPLACES ITEM #016
023	1038	DIODE GEN PUR 1A IN4004 400VDC	CR1
024	12594	DIODE SILICON CASE DO-35,IN4448	CR3, CR4, CR5, CR9, CR11
025			
026	11730-20	HEATSINK SUB ASSY TO-220	CR2, (REF)
027			
028	12540	I C ADJ PREC SHUNT REG TO 92	VR1
029			
030			
031			
032			
033			
034	11969	INDUCTOR 3 TERM REG	L1
035	11762	INDUCTOR 011749	L2
036	12209	INDUCTOR AIR CORE	L3
037			
038			
039	11463	TRANS MPS-A56	Q1, Q2, Q5, Q9
040	11689	TRANS PNP HIGH VOLT D45C11	Q4
041	13530	TRANS NPN POWER 45V 15A D44VH4	Q3
042			
043			
044	11464	TRANS NPN MPS-A06	Q6, Q7, Q15
045	1017	TRANS NPN GEN PUR MPS-5172	Q8
046	1144	TRANS NPN POWER SIL TIP-31 TO-220	Q12
047			
048			
049	12593	TRANS NPN TO-92 CASE MPS2222A	Q13, Q14
050			
051			
052			

Table 11-17. Battery Backup Card Option Replaceable Parts (Sheet 2 of 3)
(Boschert BB500 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053			
054			
055	3074	OBSOLETE(RES 1.2K OHM 1/4W)	R1, R7, R40
056	3067	OBSOLETE(RES 620 OHM 1/4W)	R2
057	3048	OBSOLETE(RES 100 OHM 1/4W)	R8
058			
059			
060	3064	OBSOLETE(RES 470 OHM 1/4W)	R10
061			
062	3113	OBSOLETE(RES 51K OHM 1/4W)	R15
063			
064			
065	3120	OBSOLETE(RES 100K OHM 1/4W)	R17, R28
066	3103	OBSOLETE(RES 20K OHM 1/4W)	R55
067	3116	OBSOLETE(RES 68K OHM 1/4W)	R20
068	3110	OBSOLETE(RES 39K OHM 1/4W)	R53
069			
070	3096	OBSOLETE(RES 10K OHM 1/4W)	R21, R22, R45, R57, R47
071	3072	RES CF 1K OHM 5% 1/4W	R23, R29, R42
072	3091	OBSOLETE(RES 6.2K OHM 1/4W)	R24
073	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R46
074			
075	3090	OBSOLETE(RES 5.6K OHM 1/4W)	R27, R50
076	3108	OBSOLETE(RES 33K OHM 1/4W)	R30
077	3134	OBSOLETE(RES 390K OHM 1/4W)	R32, R34
078			
079			
080	3087	OBSOLETE(RES 4.3K OHM 1/4W)	R38
081			
082			
083	3040	OBSOLETE(RES 47 OHM 1/4W)	R39
084	10318-05	OBSOLETE(RES 3.3 OHM 1/4W)	R44
085	3068	OBSOLETE(RES 680 OHM 1/4W)	R52
086			
087			
088	3088	OBSOLETE(RES 4.7K OHM 1/4W)	R54, R56
089	3084	OBSOLETE(RES 3.3K OHM 1/4W)	R51
090			
091	10329-91	RES MF 43K 2% 1/4W	R12
092	10329-61	RES MF 2.4K 2% 1/4W	R16
093	10329-03	RES MF 270K 2% 1/4W	R31
094	10329-74	RES MF 8.2K 2% 1/4W	R14
095			
096			
097	3094	OBSOLETE(RES 8.2K OHM 1/4W)	R43, R19
098	3102	OBSOLETE(RES 18K OHM 1/4W)	R48
099			
100			
101			
102			
103			
104	3800	RES WW .1 OHM 5% 2W BWH	R3, R4

Table 11-17. Battery Backup Card Option Replaceable Parts (Sheet 3 of 3)
(Boschert BB500 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
105	3811	RES WW 10 OHM 10% 1W BW20F	R9
106	10966-49	RES WW 1K OHM 10% 2W BWH	R11
107			
108	10660-10	RES POT 2K OHMS VERT ADJ .5W CERM	R13
109	3902	RES POT 5K OHM HORZ ADJ 10% .75W	R41, R49
110	10519-10	RES POT 2K OHM VADJ STURN .5W CERM	R18
111			
112			
113	1000	I C VOLT REG 723	U1, U4
114	10379-01	I C NOR GATE DUAL IN CMOS CD4001BE	U2
115	10505	I C LOW POWER DUAL VOLT COMP LM393N	U3
116			
117	13495	BRACKET BATT BACK-UP XL400-3502	
118	7577	WASHER SPLIT LOCK #4	
119	7506	WASHER FLAT #6	
120	7588	WASHER SPLIT RING LOCK #6	
121	11092-01	STANDOFF HEX 4-40 .250LG	
122	13744	MTG HDW TO-220 NON CNDCT #4	
123	14578	LABEL SMALL BOSCHERT MODEL/SER NO	
124	13570	HEATSINK TO-220 NO MTG TABS	
125	15178	LABEL CUSTOMER ID	L1(REF)
126	7863	0.0400TAPE 2 SIDED 1/16	L2, (REF)
127			
128	12891-03	PEM STUD 4-40 THREAD .625 LG	
129	13618-01	SCREW CAPTIVE PANEL .625" LG 6-32	

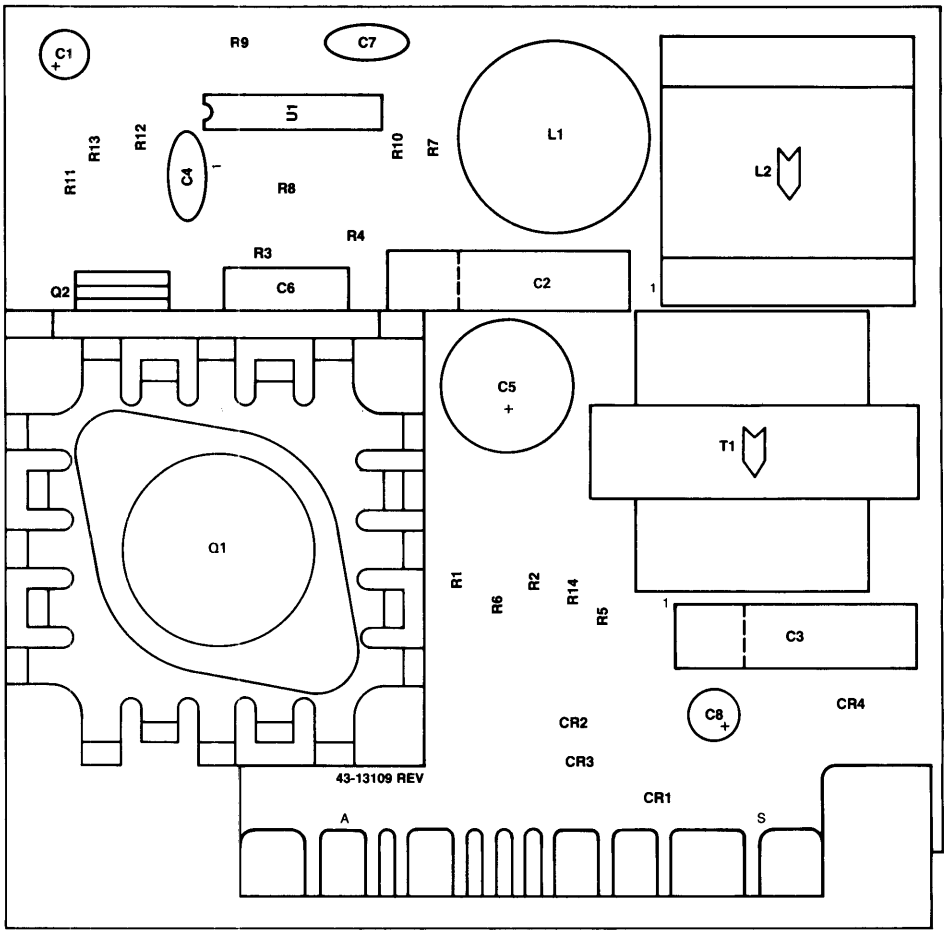


Figure 11-14. Parts Locations for 25 kHz Card (SW100)

Table 11-18. 25 kHz Card Option Replaceable Parts (Sheet 1 of 2)
(Boschert SW100 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13137	P C B SW100	
002	13527	HEATSINK TO-3	
003	13494	BRACKET SINE WAVE,SW100	
004			
005	2059	CAP CERM .01UF-100V	C4
006	11133-01	CAP MET POLY .1UF 100V 10% RLDS	C6
007			
008			
009			
010	13249-01	OBSOLETE(CAP ELECT 100UF-50V)	C5
011	14297-04	CAP ELECT 100UF 50V LO ESR RLDS RX	C5, REPLACES ITEM #010
012	10765-06	CAP ELECT 3.3UF 63V RD LDS VB	C1, C8
013	2032	CAP CERM .001UF 10% 1000VDC	C7
014			
015			
016	14580-01	CAP MET POLYP 0.22UF 250V 5% RLD	C2
017	14580-02	CAP MET POLYP 0.33UF 250V 5% RLD	C3
018			
019			
020	1088	OBSOLETE(DIODE FST RCV 100V-3A)	CR1, CR2
021	1026	OBSOLETE(DIODE 200V-1A)	CR3, CR4
022	1155	DIODE FST RCV 1A 600V AX LD IN4937	CR3, CR4, REPLACES ITEM #021
023	1042	DIODE FST RCV 200V 3A AX LDS MR852	CR1, CR2, REPLACES ITEM #020
024			
025	13163	INDUCTOR ASSY 140UH @ 1.75 ADC	L1
026	13164	INDUCTOR 100 UH @ 1.25A PQ26/25	L2
027			
028			
029	1094	TRANS NPN POWER 2N5885	Q1
030	1144	TRANS NPN POWER SIL TIP-31 TO-220	Q2
031			
032			
033			
034	3040	OBSOLETE(RES 47 OHM 1/4W)	R3
035	3082	OBSOLETE(RES 2.7K OHM 1/4W)	R9, R5
036	3068	OBSOLETE(RES 680 OHM 1/4W)	R4
037			
038			
039	3087	OBSOLETE(RES 4.3K OHM 1/4W)	R14
040	3100	OBSOLETE(RES 15K OHM 1/4W)	R13
041	3104	OBSOLETE(RES 22K OHM 1/4W)	R8
042			
043			
044	3113	OBSOLETE(RES 51K OHM 1/4W)	R11
045	3052	OBSOLETE(RES 150 OHM 1/4W)	R6
046	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R10
047	3272	RES CF 1K OHM 5% 1/2W	R7
048			
049			
050	10048-02	RES WW .36 OHM 5% 2W BWH	R1, R2
051			
052	3902	RES POT 5K OHM HORZ ADJ 10% .75W	R12

Table 11-18. 25 kHz Card Option Replaceable Parts (Sheet 2 of 2)
(Boschert SW100 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053			
054	14578	LABEL SMALL BOSCHERT MODEL/SER NO	
055			
056	13162	TRANSFORMER DRIVE XL400	T1
057			
058	13618-01	SCREW CAPTIVE PANEL .625" LG 6-32	
059			
060	1000	I C VOLT REG 723	U1
061	11247-19	SCREW P H 6-32 X 1.5 LG	L1, (REF)
062	7504	NUT HEX 6-32	L1, (REF)
063	7506	WASHER FLAT #6	
064	7549	WASHER FENDER	L1, (REF)
065			
066	7580	INSULATOR MICA TO-3	Q1, (REF)
067			
068	7588	WASHER SPLIT RING LOCK #6	
069	11828	WASHER METAL	Q2, (REF)
070	12298	INSULATOR TO-220	Q1, Q2, (REF)
071	7505	WASHER FLAT #4	Q1, Q2, (REF)
072	7577	WASHER SPLIT LOCK #4	
073	7584	SCREW F H 4-40 X 1/2	Q2, (REF)
074	11092-01	STANDOFF HEX 4-40 .250LG	
075	11837	INSULATOR CHOMERICS	Q2, (REF)

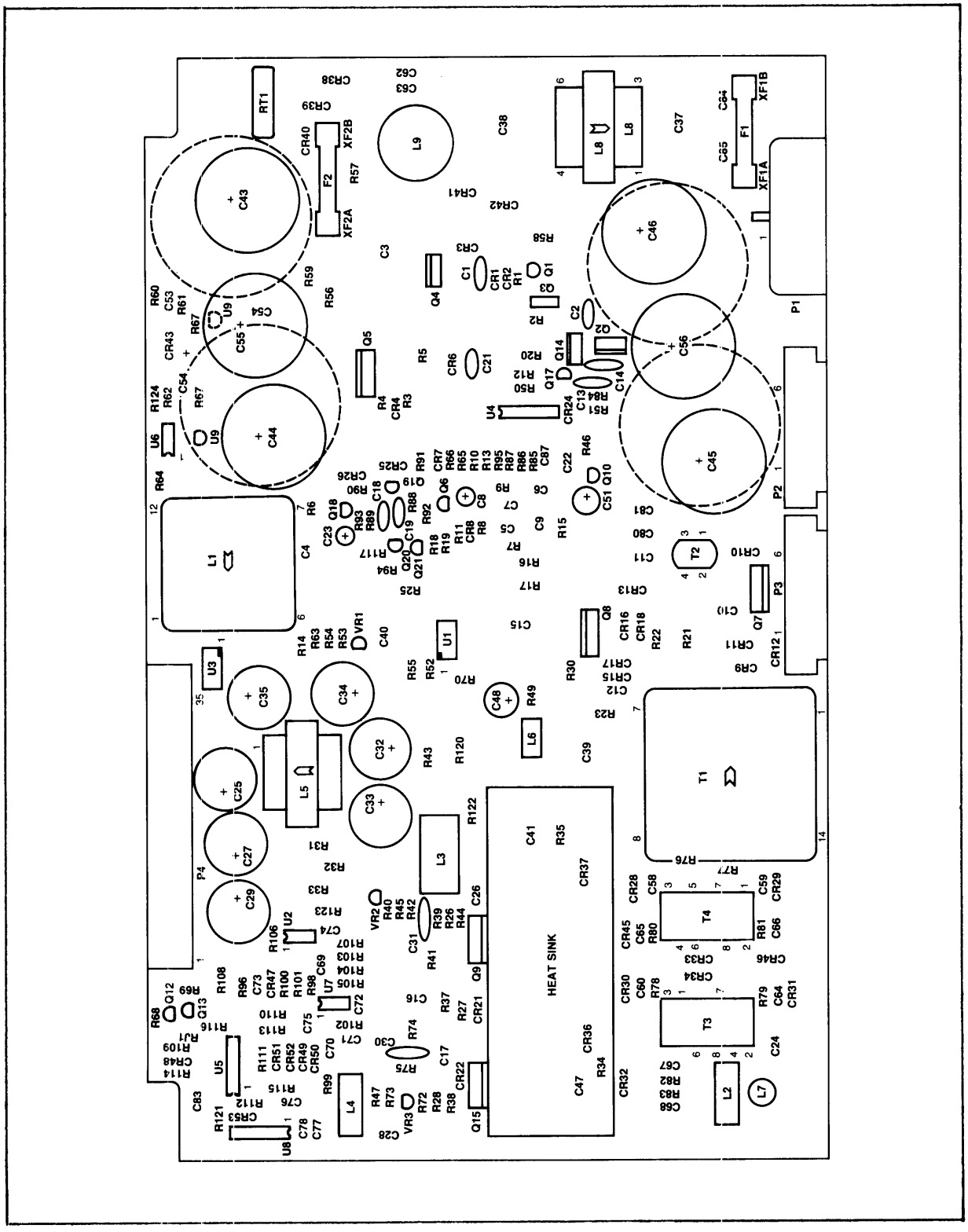


Figure 11-15. Parts Locations for 300W Supply

Table 11-19. 300W Supply Replaceable Parts (Sheet 1 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	14645	P C B XL301-5612	
002	14718	BRACKET L 300 WATT	
003	15009	STUD,LOCATING	
004	14732	HEATSINK XL301-5612	
005	15632-01	HEATSINK	Q5, S1, (REF)
006	15632-02	HEATSINK	Q7, Q8, (REF)
007	12012	HEATSINK TO-220	CR6, Q4, (REF)
008	14995	PLATE COVER	
009	2105	CAP CERM 100PF-1KV	C2
010	2000	CAP CERM .0047UF-1KV	C13, C14
011	2059	CAP CERM .01UF-100V	C18
012	2006	CAP CERM 150PF-1KV	C19
013	2008	CAP CERM .1UF-100V	C1, C41, C47
014	2062	CAP CERM 270PF-1KV	C21
015	2004	CAP CERM .1UF-16V	C30, C31
016			
017	15111-01	CAP SOLID ELECT 6.8uf 20% 25V RLDS	C11, C80, C81
018			
019	10346-05	CAP ELECT 47UF-16V RAD LDS	C51
020	10346-01	CAP ELECT 10UF-16V RAD LDS	C8
021	14992-01	CAP ELEC 1600UF 15V COMP GRLDS	C35
022	14993-01	CAP ELEC 570UF 40V COMP GRLDS	C27, C29, C32, C33, C34
023	15869-05	CAP ELEC 200V 1200UF 85deg C SNP IN	C43, C44, C45, C46, C55, C56
024	12939	CAP ELECT LO LEAK R LDS 100UF 10VDC	C23
025	14994-01	CAP ELEC 350UF 60V COMP GRLDS	C25
026			
027			
028	12951	CAP ELECT 10UF-100VDC LD ESR R LDS	C48
029			
030	15032-10	CAP F&F POLYC 0.68UF 400V 10% RLDS	C3
031	13593-07	CAP MET POLY .01UF 630/1000V 5%	C10
032	12685-03	CAP MET POLY 0.1UF 5% 63/100V	C4, C6, C69, C70, C71, C72, C73, C74, C75, C76
033	13279-07	CAP POLY RLD BOX .10UF 10% 250V	C5, C24, C39
034	12328-04	CAP MET POLY 0.22UF 63VDC 5%	C16, C17, C26, C28, C40
035	12685-07	CAP MET POLY .47UF 5% 63/100V	C7
036	13593-03	CAP MET POLY .0022UF 630/1000V 5%	C9, C87
037			
038	12328-08	CAP MET POLY 1.0UF 63VDC 5%	C83
039	11133-01	CAP MET POLY .1UF 100V 10% RLDS	C12, C53
040	2080	CAP MET POLY 2UF-200VDC 10%	C15
041			
042	15016-07	CAP F&F POLYC 1000PF 160VDC/100VAC	C58, C59, C60, C64, C65, C66, C67, C68
043	11133-03	CAP MET POLY .22UF 100V 10% RLDS	C22
044	12685-10	CAP MET POLY .022UF 5% 63/100V	C77, C78
045	13932-03	CAP MET EMI SUP X-CAP 1.00UF 250VAC	C37, C38
046			
047			
048			
049			
050	2021	CAP TANT 47UF-6V	C54
051	11414-02	CAP MET PAPER .0022UF 250VAC VDE AP	C62, C63, C84, C85
052	1038	DIODE GEN PUR 1A IN4004 400VDC	CR1, CR2, CR3, CR9, CR10, CR11, CR12

Table 11-19. 300W Supply Replaceable Parts (Sheet 2 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053	12594	DIODE SILICON CASE DO-35,IN4448	CR8, CR25, CR26, CR49, CR50, CR51, CR52, CR53
054	14990-01	DIODE FST RCV 9A 400V BYV29-400	CR6
055	10056-03	DIODE FAST RECV BYW 29-150	CR28, CR29
056			
057	10672	DIODE SCHOT STD POL 45V 60A SD-51	CR36, CR37
058	14482	DIODE DUAL SCHOT 20A 45V TO-220	CR32
059	12260-04	DIODE HI CUR AX LDS. 30V,6A SR3773	CR13
060	1021	DIODE HI CUR. AX LDS. 400V,6A MR754	CR38, CR39, CR41, CR42
061			
062			
063			
064	15088-01	DIODE FST RCV 3.5A 150V AXLD	CR33, CR34
065	14461-01	DIODE FST RECV 2A 100V AX LDS	CR4, CR15, CR16, CR17, CR18, CR30, CR31, CR45, CR46
066			
067	11356-15	DIODE ZENER 500MW 8.2V 5% IN5998B	CR7
068	1014	DIODE ZENER 500 MW 5.6V 5% IN5994B	CR40
069	10879	DIODE ZENER 400MW 68V 5% IN5266B	CR21, CR22
070	1008	DIODE ZENER 400MW 15V 5% IN965A	CR24
071	1056	DIODE ZENER 500MW 5.1V 5% IN5993B	CR43, CR47, CR48
072			
073			
074	7015	FUSE CLIP PCB TYPE FOR 3AG FUSE	XF1A, XF1B, XF2A, XF2B
075	10180-01	FUSE 5A-250V NORMAL-BLOW	F2
076	10865	FUSE 10 AMP 250V (BUSS ABC10)	F1
077			
078	12472	RECEPTACLE AC RT ANGLE 6A 250V	P1
079	15001-01	CONN IN LINE RT ANG PIN HDR 6 POS	P2, P3
080	14987-01	CONN RT ANG PCB 35 POS	P4
081			
082	13733	INDUCTOR 4MH	L1
083	14033	INDUCTOR PWDR IRON 3.4UH @ 6A	L4
084	14034	INDUCTOR PWDR IRON 5UH 10A	L3
085	15115	INDUCTOR 5V	L5
086	10799	INDUCTOR 18 UH	L6
087	14850	BALUN SUPER E-375 XL301	L8
088	15012	BALUN TOROIDAL 2x1mh XL301	L9
089	12209	INDUCTOR AIR CORE	L7
090	11944	INDUCTOR 18UH MIN.	L2
091			
092	12592	TRANS PNP CASE TO-92,MPS 2907A	Q1, Q6, Q18
093	1005	TRANS NPN POWER TIP-50	Q2, Q14
094	12675	TRANS PNP HI VOLT 400V TO-126 CASE	Q3
095			
096	1118	TRANS NPN POWER MJE13007	Q4
097			
098	1016	TRANS PNP CASE TO-92 2N4126	Q17
099	14988-02	TRANS NPN POWER 15A 1000V BUW 13A	Q5, Q7, Q8
100	14263-01	TRANS NPN POWER DARLING 10A TIP 140	Q9, Q15
101	13595	TRANS N-CHANNEL POWER FET VN10KM	Q12, Q13
102	12591	TRANS NPN CASE TO 92 2N4124	Q10, Q19, Q20, Q21
103			
104			

Table 11-19. 300W Supply Replaceable Parts (Sheet 3 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
105			
106	3081	OBSOLETE(RES 2.4K OHM 1/4W)	R14, R54
107	3124	OBSOLETE(RES 150K OHM 1/4W)	R50, R51
108	3108	OBSOLETE(RES 33K OHM 1/4W)	R65, R88, R90
109	3099	OBSOLETE(RES 13K OHM 1/4W)	R66
110	3088	OBSOLETE(RES 4.7K OHM 1/4W)	R85
111	3072	RES CF 1K OHM 5% 1/4W	R86, R87
112	3110	OBSOLETE(RES 39K OHM 1/4W)	R84
113			
114			
115	10318-47	OBSOLETE(RES 180 OHM 1/4W)	R27, R28
116	3064	OBSOLETE(RES 470 OHM 1/4W)	R1, R53
117	3024	OBSOLETE(RES 10 OHM 1/4W)	R6, R34, R35, R76, R77, R78, R79, R80, R81, R82, R83
118	3098	OBSOLETE(RES 12K OHM 1/4W)	R7, R117
119	3080	OBSOLETE(RES 2.2K OHM 1/4W)	R8, R30, R67, R60
120			
121	3046	OBSOLETE(RES 82 OHM 1/4W)	R9
122	3104	OBSOLETE(RES 22K OHM 1/4W)	R10
123	3096	OBSOLETE(RES 10K OHM 1/4W)	R11, R45, R47, R63, R68, R69, R93, R100, R101, R116, R124
124			
125	3048	OBSOLETE(RES 100 OHM 1/4W)	R13
126	3020	OBSOLETE(RES 6.8 OHM 1/4W)	R95
127	3135	OBSOLETE(RES 430K OHM 1/4W)	R19
128			
129			
130	3128	OBSOLETE(RES 220K OHM 1/4W)	R62
131	3069	OBSOLETE(RES 750 OHM 1/4W)	R64
132			
133			
134	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R40, R75
135	3089	OBSOLETE(RES 5.1K OHM 1/4W)	R109, R114
136	10318-102	OBSOLETE(RES 1.2 OHM 1/4W)	R49
137	3084	OBSOLETE(RES 3.3K OHM 1/4W)	R39, R73
138			
139	3106	OBSOLETE(RES 27K OHM 1/4W)	R37, R42
140	3100	OBSOLETE(RES 15K OHM 1/4W)	R46
141	3079	OBSOLETE(RES 2.0K OHM 1/4WO	R103, R104, R112
142			
143			
144	3060	OBSOLETE(RES 330 OHM 1/4)	R26, R38, R52
145	3120	OBSOLETE(RES 100K OHM 1/4W)	R89, R111
146	3130	OBSOLETE(RES 270K OHM 1/4W)	R92
147	3122	OBSOLETE(RES 120K OHM 1/4W)	R91
148			
149	10328-34	OBSOLETE(RES 680K OHM 1/4W)	R102, R105
150	10328-36	OBSOLETE(RES 820K 1/4W)	R110
151	10328-45	OBSOLETE(RES 2M OHM 1/4W)	R121
152			
153	10232-17	RES MET OXIDE 22 OHM 5% 1 W	R23
154	3336	RES CF 470K OHM 5% 1/2W	R12
155	10304-71	RES CF 1.8K 5% 1/2W	R44, R72

Table 11-19. 300W Supply Replaceable Parts (Sheet 4 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
156			
157			
158	11313-01	RES MF 1.0K OHMS 1% 1/8W	R94
159	11891-6491	RES MF 6.49K OHMS 1% 1/4W	R61
160	13598-08	RES MF UNCUT LDS 365K 1% 1/8W	R18
161	11891-4873	RES MF 487K OHMS 1% 1/4W	R59
162	10318-88	OBSOLETE(RES 9.1K OHM 1/4W)	R98
163			
164			
165	10966-49	RES WW 1K OHM 10% 2W BWH	R31
166	10232-95	RES MET OXIDE 47K OHM 5% 1 W	R20
167			
168	3825	RES WW 470 OHM 5% 2W BWH	R96
169	10233-78	RES MET OXIDE 15K OHM 5% 2W	R2, R22
170	10233-84	RES MET OXIDE 27K OHM 5% 2W	R21, R57, R58
171	11313-40	RES MF 2.55K OHMS 1% 1/8W	R99, R107
172	11313-35	RES MF 2.26K OHMS 1% 1/8W	R106
173	10232-60	RES MET OXIDE 1.3K OHM 5% 1W	R108
174	11306-51	RES MF 332K OHMS 1% 1/8W	R113
175	11306-93	RES MF 909K OHMS 1% 1/8W	R115
176			
177			
178	3828	RES WW .30 OHM 5% 2W BWH	R17
179	3809	RES WW .33 OHM 5% 2W BWH	R16
180	10967-41	RES WW 47K OHM 5% 5W	R56
181	3811	RES WW 10 OHM 10% 1W BW20F	R3, R4
182	3820	RES WW 120 OHM 5% 2W BWH	R32, R33, R122, R123
183	3812	RES WW 82 OHM 10% 1W BW20F	R5
184	3208	RES CF 2.2 OHM 5% 1/2W	R15
185	3903	RES WW 10 OHM 5% 5W	R25, R43, R120
186			
187			
188			
189	10519-12	RES POT 5K OHM VADJ STURN .5W CERM	R55
190	10519-10	RES POT 2K OHM VADJ STURN .5W CERM	R41, R74
191			
192	3938	RES THERMISTOR DISC 5 OHM 15% ST LD	RT1, RT2
193	13462	RES WIRE WW ZEROHM JUMPER WIRE 25A	RJ1
194			
195	3911	THERMOSTAT SNAP-ACTING AUTO RESET	S1
196	10422-11	WIRE RED 22 AWG 5"LG 1/4 X 1/4	S1, (REF)
197	7480	WIRE RED 18 AWG 1.50" (1/4 X 1/4)	T2, (REF)
198			
199	14729	TRANSFORMER XL301 VDE/RFI	T1
200	12871-02	TRANSFORMER PC MT SINGLE CORE 5T	T2
201	14923	TRANSFORMER TOROIDAL XL301	T3, T4
202			
203	12977	OPTO-RESISTOR MATCHED VDE	R70, U1
204			
205	13363	I C CMOS D PREC MONO MULTI CD4538BE	U8
206	11498	I C OPTO-ISOLATOR OP1-1264B	U3
207	14984-01	I C VOLT REF PREC 2.5V 1% MDIP	U2

Table 11-19. 300W Supply Replaceable Parts (Sheet 5 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
208	14985-01	I C VOLT REF 2.5V 2% TO-92	U9
209	10505	I C LOW POWER DUAL VOLT COMP LM393N	U7
210	12219	I C OP AMP VCOMP 8 PIN MDIP LM392N	U6
211	13437	I C QUAD 2 IN SCHMITT TRIG CD4093BE	U5
212	1000	I C VOLT REG 723	U4
213	7500	TIE WRAP SMALL	S1, (REF)
214	12540	I C ADJ PREC SHUNT REG TO 92	VR1, VR2, VR3
215	7694-2	NUT KEPS CONICAL 1/4-28	CR36, CR37, (REF)
216	6009	PIN MALE BEAD .65 LG .095 DIA	E1, E2, E5
217	14957-03	JUMPER TERMINAL FEMALE	JP4
218	15696	SPRING CLIP HDWR CNDCT 12012 HTSINK	Q4, (REF)
219	11092-01	STANDOFF HEX 4-40 .250LG	P1, (REF)
220	15695	SPRING CLIP HDWR NCNDCT 12012 H/S	CR6, (REF)
221	10915	STD MTG HDW PC BD SUPPORT NYLON	
222	7501	TIE WRAP MEDIUM	
223	15451-01	STIFFENER 1.25 X 4.25" LG	C43, C44, C45, C46, C55, C56, (REF)
224	11319	RETAINING RING EXTERNAL	CR36, CR37, (REF)
225	12569	LABEL,CSA MARK	L-BRKT, (REF)
226			
227	15081-01	HANDLE .25DIA 3.0LG 1.0H 6/32THD	
228	12459	LABEL FUSE WARNING	C46, (REF)
229	14996	LABEL 115 VAC / 230 VAC	L-BRKT, (REF)
230	7740	LABEL DANGER HIGH VOLTAGE	C43, (REF)
231	7881	LABEL SERIAL NO.	T1, (REF)
232			
233	15640	SPRING CLIP HDWR (NCNDCT) TO218/220	CR32, Q7, Q8, Q9, Q15, (REF)
234	7578	SCREW P H 4-40 X 1/4	S1, (REF)
235	7511	SCREW P H 6-32 X 1/2	
236	7506	WASHER FLAT #6	
237	7588	WASHER SPLIT RING LOCK #6	
238	7577	WASHER SPLIT LOCK #4	P1, S1, L-BRKT, (REF)
239	7505	WASHER FLAT #4	P1, L-BRKT, (REF)
240	10366-01	WIRE RED 16 AWG 8" (1/4 X 1/4)	JP2, JP3
241	15633	SPRING CLIP HDWR CNDCT TO-218/220	Q5, (REF)
242	11661-01	SPACER GLASS .225 OD .067 ID .185TH	RT1, RT2, R21, R57, R58, (REF)
243	7202	0.0040RTV 108 CLEAR	L6, L7, C15, C43, C44, C45, C46, C55, C56, (REF)
244	15239	LABEL WARNING	L-BRKT, (REF)
245	15240	LABEL INFORMATION (WARNING)	L-BRKT, (REF)
246	15742	LABEL CUSTOMER I D	L-BRKT, (REF)
247	7737	0.0010LOCKTITE	
248	12891-03	PEM STUD 4-40 THREAD .625 LG	P.C. B.D., (REF)
249	7508	SCREW P H 4-40 X 3/8	L-BRKT, (REF)

REV	DESCRIPTION	ECO	DATE	APPROVED
X	SEE SH 2			

BD2 P12 J12 RED E21 F3 WHT 5A,250V E22 E23 BRN
110/220V HOT P9 F2 10A 250V
110/220V HOT/NEUT
220V OP FAN 1 FAN 2 FAN 3 FAN 4 P7
110V OP FAN 1 FAN 2 FAN 3 FAN 4 P8
SHORT FOR 110V OP
CR100 MR754 CR101 MR754 RT1 5
CR102 MR754 CR103 MR754 RT2 5
C105 1000 200V C100 1000 200V C103 1000 200V C104 1000 200V C102 1000 200V C101 1000 200V
CR104 IN 5994B 5.6V
R100 27K 2W R101 27K 2W
CR105 KBP04 AC AC + -
R102 150K ½W R104 6.2K
CR106 IN4004 CR107
C107 0.47 63V R103 50K 3CW R105 100K C106 .047 250V
C108 3.3 250V R107 12K 5W R108 10K R106 1.8K
U100 LM393N R111 120K R109 1K R110 2.7K
U101 OPI-1264B C109 3.3 50V CR108 IN 965A 15V
R114 2.2K R112 10K Q100 MPS 2222A R113 15K R156 150K Q101 2N 4124 R115 4.7K
R121 4.7K R123 2K 3CW R126 7.5K U102A LM393N C110 0.33 63V CR109 R122 47K
R124 3.3K R120 4.7K R125 10K R146 1.6K R118 10K R119 100K U102B LM393N CR126 Q103 MPS2222A R154 1K CR110
CR111 IN 5998B 8.2V R127 820 2W
30V CR124 MR502 F1 5A-250V CR123 MR502
P5 2 SW IN 1 / 3 INT BATT + / 4 SW IN 2 / 1 INT BATT −
P6 1 +5.1V / 2 +12V / 3 −12V / 4 +5.1V MEM. / 5 PON + / 6 PFW − / 7 M LOST / 8 25 KHZ Ø1 / 9 25 KHZ Ø2 / 10 BATT + / 11 BATT − / 12 RET
P2 1 28 COM / 29 32 +12V / 33 34 −12V / 35 38 +5.1V MEM. / 39 42 Ø1 / 43 46 Ø2 / 47 PON / 48 PFW / 49 M LOST / 50 +5 MMRY SENSE
P1 1 36 +5.1V / 37 50 RET
C134 1000 10V C133 0.33 63V C132 0.22 63V C131 470 25V R135 120 2W BWH C130 470 25V R134 120 2W BWH
C140 0.22 63V C143 0.22 63V C142 0.22 63V C141 0.22 63V
C139 .1 250V R145 1K 2W BWH-10%
SEE SHT 2 C D E
T1 80-13732 (43-13825) PC BD ON T1 J15 BRN RED GRN WHT BLK
T3 80-14159 2T 2T BLU E31 CR128 MR850 C146 0.22 63V
CR127 MR850 A SEE SHT 2
C125 470 pf - 1KV CR121 MR851 CR122 MR851 C126 470 pf - 1KV
CR120 BYV27-100 CR119 BYV27-100
L103 80-10899 L104 80-14364 L100 80-10799 L101 80-10899 L102 80-10899
A2 (P10 REF) BB500 (13077) OPTIONAL
A3 (P11 REF SW100 (13109) OPTIONAL
CR116 SES5402C CR117 BYW 29-50 CR118 BYW 29-50
C122 0.1 250V C123 330 50V CR125 MR 502 C119 .001 1KV C120 0.22 63V C121 0.22 63V
R132 100 1/2W R133 220 1/2W C124 470PF 1KV
VR100 TL430 2.75V REF R139 5K 3CW R140 330 R141 390 Q104 2N4126 C128 .047 250V C129 0.22 63V R136 330 R137 3.32K 1%, 1/8W R138 470 C127 10 100V
JP3 YEL JP6 GRN JP8 RED JP4 WHT JP5 BLK
BUSS BAR
C111 0.1 100V C112 0.1 100V C113 0.1 100V C114 0.1 100V
R128 10 R129 10 R130 10 R131 10
CR112 SD51 CR113 SD51 CR114 SD51 CR115 SD51
FL1 RED FL2 RED FL5 WHT FL4 WHT
C118 2200 16V C117 2200 16V C116 2200 16V
R142 1.2 R143 10 5W R144 10 5W R117 1K 1W
C137 1000 10V C138 1000 10V
Q102 MPS2907A R155 3.3K R116 2.2K 1W C135 0.33 63V C136 0.22 63V
S100 E28 E27
P14 BD2 J14 BLK E12 RED E24
P13 BD2 J13 E25 RED E26 BLK

BD. NO. 1 (BOTTOM)
REFERENCE DESIGNATIONS 3

LAST USED	NOT USED
A3	A1
C146	C115
CR128	
E36	E1, 2
F3	
JP8	JP1, JP2
L103	
Q105	
R156	
S100	
T3	
U102	

NOTES ARE ON SH 2.

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
DECIMALS (.XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES °

NEXT ASSY	MOD NO.
45-13596-01	XL400-5411R

DO NOT SCALE DRAWING

BOSCHERT ASSOCIATES SUNNYVALE, CALIFORNIA

SCHEMATIC, MODEL: XL400-5411R

SIZE	DWG NO.	REV
D	90-13709	C
SCALE NONE	SHEET 1 OF 2	

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-1478

REV	DESCRIPTION	ECO	DATE	APPROVED
1	PRE REL			
2	PRE REL			
3	PRE REL			
4	PRE REL			
A	REL TO PROD.			
B	INCORP.	7910		
C	INCORPORATED	8664		

80-13733
L1

P12
1
2
4

C3 0.1 500V
CR1 IN4004
CR2 IN4004
C1 0.1 100V
CR3 IN4004
R1 470
Q1 MPS 2907A
C2 100pF 1KV
R2 15K 2W
Q3 25A1156
Q2 TIP50
MJE13007
Q4
R3 10-1W BW20F-10%
CR4
R4 10-1W BW20F 10%
R5 82-1W BW20F 10%
R6 10
C4 0.1, 100V
L2 80-11625
CR5 MR854
R7 5-5W 10%
C5 270pf 1KV
CR6 MR 2404F

A1
43-12983
N/C
CR7 IN5998B 8.2V
JP2
E3
E4
R30 12K
R10 22K
R8 2.2K
R9 82
CR8
Q6 MPS 2907A
C8 10 16V
C7 0.47 63V
R11 10K
C6 0.22 63V
C21 .0047 400V
SELECTED OPTO 15-12975-15 TO MATCH R14
P13
C22 .001 1KV
U1
P14
R12 220
U2 OPI1264B 115-11498
R13 100
R14 16
R15 10, 1W BW20F 10%
R16 0.2, 2W BWH
R17 0.2, 2W BWH
R18 365K 1% 1/8W
R19 430K
C9 .0047 400V
R20 22K

80-12872-01
T2

E2
JP1
E1
1
P15
CR9 10-1028
R22 47K 1W
R21 47K 1W
R23 15K 2W
CR10 SR3773
CR11 SR3773
C10 4.7, 100V
C20 1, 63V
Q7 2N6678
C11 .0047 400V
R24 150 2W
CR12 IN 4004
R25 10 10W-10%
CR14 MR854
CR13 IN 4004
C12 .001 3KV
C13 .01 1KV
C14 10 250V
C15 2 250V
R26 47
C16 1, 63V
C17 4.7, 100V
Q8 2N6678
CR15 SR3773
CR16 SR3773
CR17 10-1028
C18 .001 3KV
CR18 IN 4004
CR19 IN 4004
R27 150 2W
CR26 CR20
CR22
CR23
CR24
CR25
CR27 CR21
R28 47, 2W BWH
R29 20, 1W
C19 0.1, 100V

SEE SHT1 A (T3-2,3)
C144 100pf-1KV
Q105 150 10K TIP140
RED JP7
E35 E36
C SEE SHT1 (30V)
R147 6.8K
R149 3K
R148 1K
C145 .01-400V
R150 3.3K
VR101 2.75V REF TL430
R152 2K CW
R153 6.8K
SEE SHT1 D (12V)
R151 62K
(RET)
B SEE SHT1
E (-12V) SEE SHT1
BD1 (BOTTOM)

4 TO ISOLATE REGULATOR CONNECTION TO INVERTER, REMOVE JP1 & INSTALL IT TO JP2 POSITION TO KEEP REGULATOR VOLTAGE FROM RISING EXCESSIVELY.

3 DES. NOS. ON BOARD 1 (BOT) ARE ASSIGNED 100 ON, BOARD 2 (TOP) ARE ASSIGNED NO'S. 1-99, EXCEPT FOR A,E,F, JP, P, S, AND T DES. WILL CON'T.

2. SHEET 1 AND PART OF SHT. 2 OF SCHEMATIC ARE BD1 (BOTTOM) SHEET 2 OF SCHEMATIC IS BD 2 (TOP)

1. UNLESS OTHERWISE SPECIFIED:
RESISTORS ARE IN OHMS, ±5%, 1/4W
CAPACITORS ARE IN MICROFARADS (UF)
DIODES ARE IN4448
VOLTAGE RATINGS ARE DC

NOTES:

BRD. NO. 2 (TOP)

REFERENCE DESIGNATORS LAST USED	NOT USED
A1	
C22	
CR27	
E4	
JP2	
L2	
P15	P1 - P11
Q8	
R30	
T2	T1
U2	

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS (.XX) FRACTIONS
DECIMALS (.XXX) ANGLES

NEXT ASSY	MOD NO.
45-13729	XL400-5411R

DO NOT SCALE DRAWING

APPROVALS: DATE
DRAWN
CHECKED
ENG
ENG MGR
MFG MGR
QA MGR
RELEASED

boschert BOSCHERT ASSOCIATES SUNNYVALE, CALIFORNIA

SCHEMATIC
MODEL XL400-5411R

SIZE D | DWG NO. 90-13709 | REV C
SCALE NONE | SHEET 2 OF 2

REV	DESCRIPTION	ECO	DATE	APPROVED
	PRE-REL			
2	PRE-REL			
3	PRE-REL		2-23-83	
4	PRE REL			
A	PRE-REL			
B	INCORPORATED	7825	11/14/83	
C	INCORPORATED	8342A		

REV
PC NO. 90-13076

+ INPUT

J1 1

C1 470 50V
C11 470 50V
R2 620
C2 .001 1KV
R3 0.1,2W BWH
R4 0.1,2W BWH
Q1 MPS-A56
Q2 MPS A56
Q3 D44VH4
Q4 D45C11
R9 10,1W BW20F 10%
R8 100
Q5 MPS-A56
R10 470
R1 1.2K
R19 8.2K
R55 20K
Q9 MPS-A56
C4 4.7-50V
C5 0.1 100V
R34 390K
R7 1.2K
C12 .0022-1KV
Q6 MPS-A06
Q8 MPS 5172
R27 5.6K
C8 .001 100V
R24 6.2K
R32 390K
R14 8.2K 2%
R39 47
U1 723
CW R13 2K
R12 43K 2%
C23 0.1 100V
R15 51K 2%
R16 2.4K 2%
Q15 MPS-A06
R57 10K
R18 2K CW
R38 4.3K
C18 .001 1KV
R20 68K
C7 470pF 1KV
R17 100K
C6 .0022 1KV
CR5
CR3
R21 10K
R22 10K
U2(C) 4001B
U2(D) 4001B
Q7 MPS-A06
R23 1K
U2(A) 40018
U2(B) 40018
CR4
R28 100K
R29 1K
R30 33K
C9 .001 100V

L1 80-11969
C10 0.1 100V
CR2 USD840 143-11730-20
C3 470 50V
R11 1K 2W BWH 10%
C14 470 50V
C15 270pF 1KV
L3 80-12209
L2 80-11762
C16 470 50V
C17 470 50V

J1 11 12 OUTPUT +
14 RETURN -
15
M-LOST 9
CR11
R56 4.7K
R31 270K 2%
R52 680
R51 3.3K
R50 5.6K
U3(A) LM393N
C21 1 50V
R53 39K
R54 4.7K
U3(B) LM393N
Q14 MPS2222A
C22 10 16V
R49 5K CW
R48 18K
VR1 TL430
7 ENABLE
CR9

CHG. SOURCE 3
TO BATT 5

C24 3.3 50V
U4 723
R40 1.2K
R41 5K CW
R42 1K
R43 8.2K
CR1 IN4004
Q12 TIP31
R45 10K
R44 3.3
Q13 MPS2222 A
R47 10K
R46 6.8K
C20 .01 100V

REFERENCE DESIGNATORS	
LAST USED	NOT USED
C24	C19,13
CR11	CR6,7,8,10
J1	
L3	
Q15	Q10,11
R57	R5,6,25,26,35-37, 33
U4	
VR1	

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
CAPACITORS ARE IN MICROFARADS.
RESISTORS ARE IN OHMS, 1/4 WATT. C.F., 5%
DIODES ARE IN4448.
RATINGS ARE IN D.C.

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS (XX) — FRACTIONS —
DECIMALS (XXX) — ANGLES —

NEXT ASSY	MOD NO.
	BB500

DO NOT SCALE DRAWING

boschert BOSCHERT ASSOCIATES SUNNYVALE CALIFORNIA

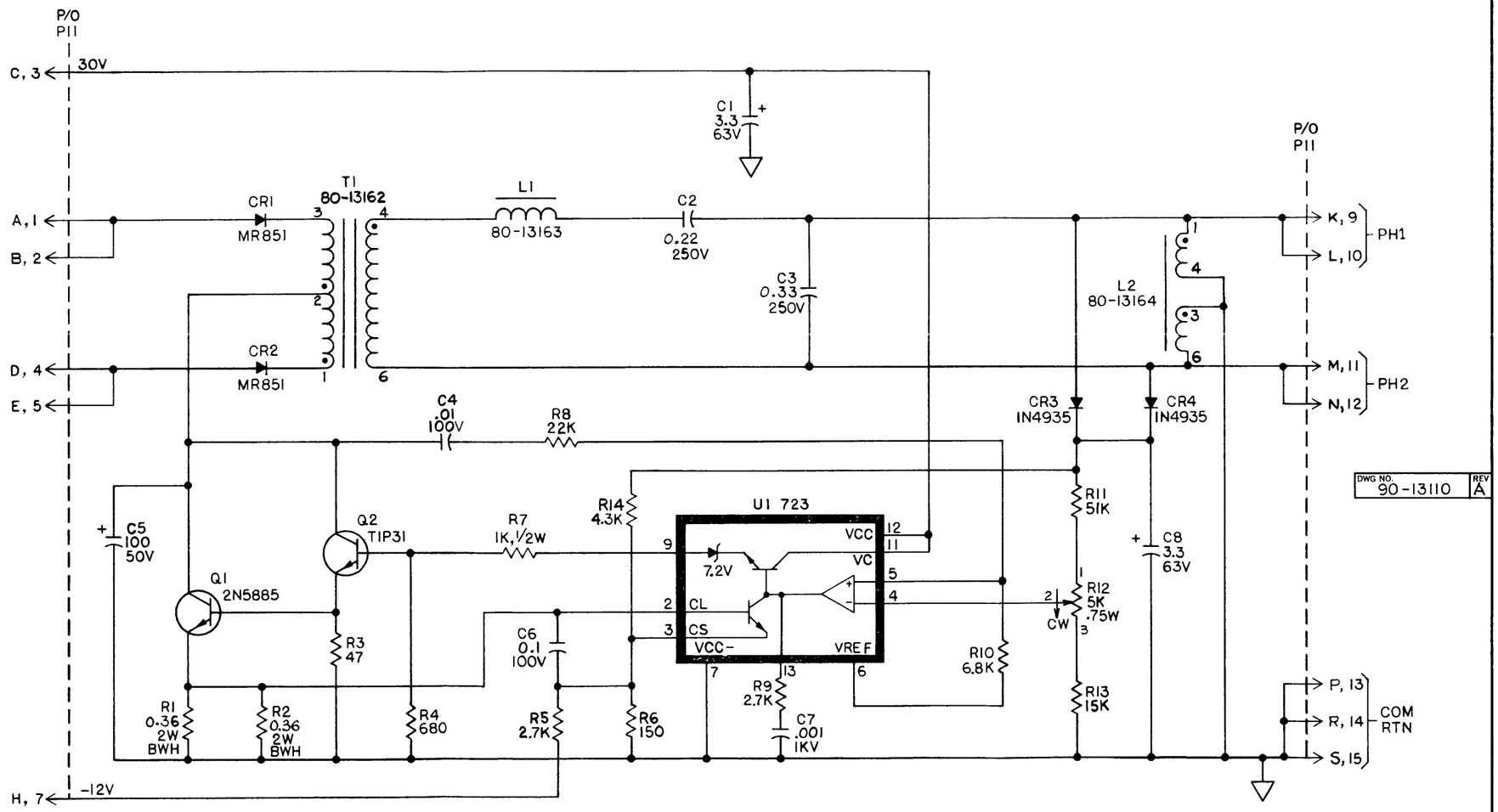
SCHEMATIC
+5.1V BATTERY BACK-UP SUPPLY
MODEL: BB500

SIZE	DWG NO	REV
D	90-13076	C

SCALE NONE SHEET 1 OF 1

90-13076-jp

REV	DESCRIPTION	ECO	DATE	APPROVED
4	PRE REL FOR PROD		10/14/82	DD MC
5	PRE REL		12/1/82	MC DD
A	REL FOR PROD		1/20/83	MC DD



DWG NO.	REV
90-13110	A

LAST USED	UNUSED
CR4	
Q2	
U1	
C8	
R14	
T1	
L2	

1. ALL VOLTAGES ARE "DC".
   ALL CAPACITORS ARE IN MICROFARADS
   ALL RESISTORS ARE IN OHMS, ± 5%, 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED;

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES:
TOLERANCES:
DECIMALS (.XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES ±

NEXT ASSY	MOD NO.
43-13728	XL400-5411

DO NOT SCALE DRAWING

BOSCHERT INCORPORATED
SUNNYVALE, CALIFORNIA

SCHEMATIC
SINE WAVE SUPPLY
SW100

SIZE	DWG NO.	REV
C	90-13110	A

SCALE N/A SHEET 1 OF 1

REV	DESCRIPTION	ECO	DATE	APPROVED
A	PRE REL			
	REL FOR PROD			

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
DECIMALS (XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES ±

NEXT ASSY	MOD NO.
45 - 14418	

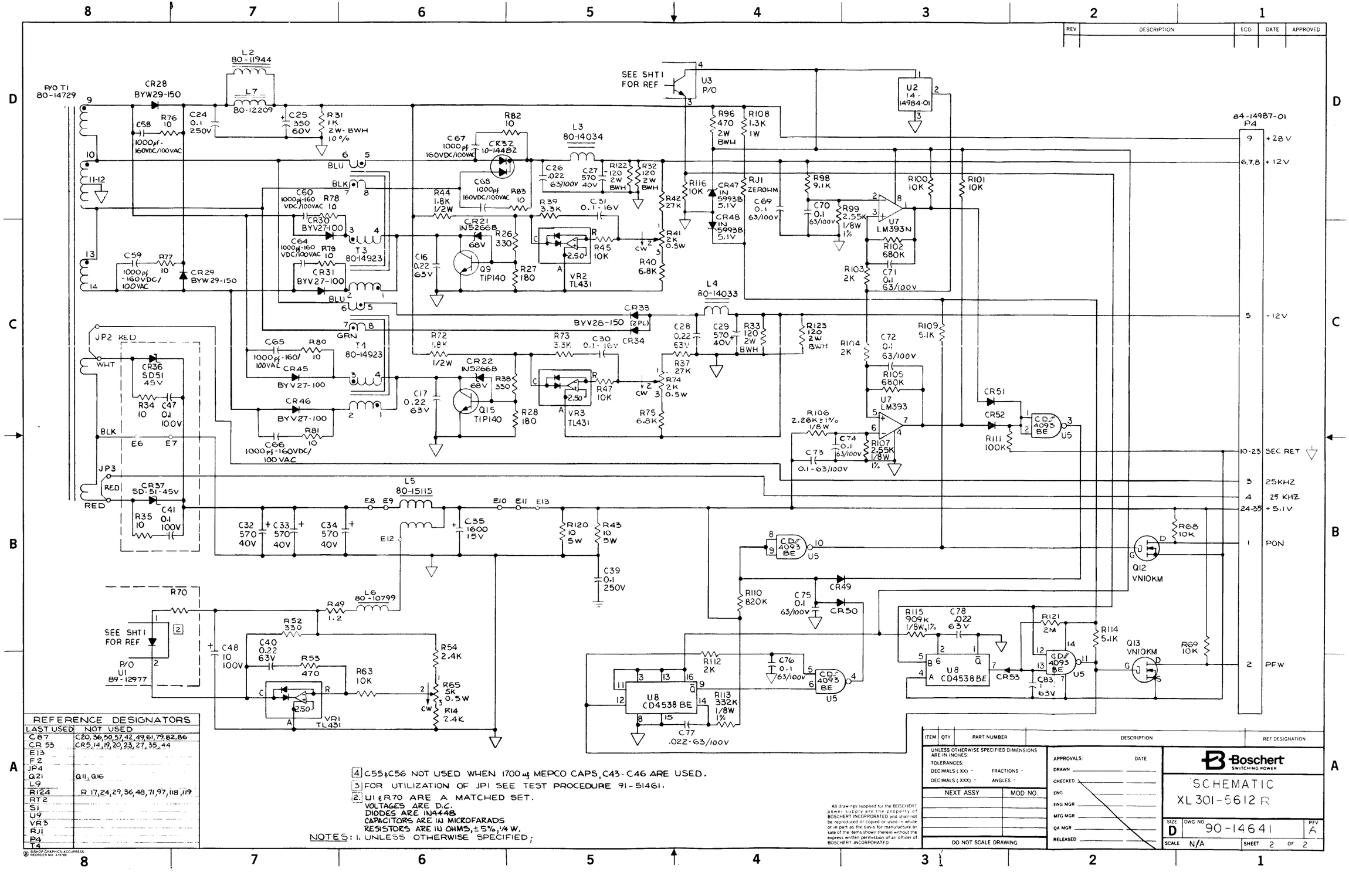
DO NOT SCALE DRAWING

Boschert SWITCHING POWER

SCHEMATIC
MODEL: XL301-5612 R

SIZE	DWG NO.	REV
D	90-14641	A
SCALE NA	SHEET 1 OF 2	

REV	DESCRIPTION	ECO	DATE	APPROVED



REFERENCE DESIGNATORS	
LAST USED	NOT USED
C87	C20,36,50,57,42,49,61,79,82,86
CR 53	CR5,14,19,20,23,27,35,44
E13	
F2	
JP4	
Q21	Q11,Q16
L9	
R124	R17,24,29,36,48,71,97,118,119
RT2	
S1	
U9	
VR3	
RJ1	
P4	
T4	

4 C55&C56 NOT USED WHEN 1700 μf MEPCO CAPS, C43-C46 ARE USED.

3 FOR UTILIZATION OF JP1 SEE TEST PROCEDURE 91-51461.

2 U1 & R70 ARE A MATCHED SET.

NOTES: 1. UNLESS OTHERWISE SPECIFIED;
VOLTAGES ARE D.C.
DIODES ARE IN4448
CAPACITORS ARE IN MICROFARADS
RESISTORS ARE IN OHMS, ±5%, ¼ W.

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS (.XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES ±

NEXT ASSY	MOD NO.

DO NOT SCALE DRAWING

APPROVALS:	DATE
DRAWN	
CHECKED	
ENG	
ENG MGR	
MFG MGR	
QA MGR	
RELEASED	

Boschert SWITCHING POWER

SCHEMATIC
XL 301-5612 R

SIZE	DWG NO.	REV
D	90-14641	A

SCALE N/A SHEET 2 OF 2

Appendix A
Backplane Signals

BACKPLANE SIGNALS				
PIN	SQ	DP	CA	MC
01A	BP.+5V	BP.+5V	BP.+5V	BP.+5V
01B			BP.WR.CYC-	BP.WR.CYC-
01C			BP.LOG.ADDR0N+	BP.LOG.ADDR0N+
01D			BP.LOG.ADDR0I+	BP.LOG.ADDR0I+
02A			BP.LOG.ADDR1+	BP.LOG.ADDR1+
02B			BP.LOG.ADDR2+	BP.LOG.ADDR2+
02C			BP.LOG.ADDR3+	BP.LOG.ADDR3+
02D			BP.LOG.ADDR4+	BP.LOG.ADDR4+
03A			BP.LOG.ADDR5+	BP.LOG.ADDR5+
03B			BP.LOG.ADDR6+	BP.LOG.ADDR6+
03C			BP.LOG.ADDR7+	BP.LOG.ADDR7+
03D			BP.LOG.ADDR8+	BP.LOG.ADDR8+
04A	BP.GND	BP.GND	BP.GND	BP.GND
04B	BP.GND	BP.GND	BP.GND	BP.GND
04C	BP.GND	BP.GND	BP.GND	BP.GND
04D	BP.GND	BP.GND	BP.GND	BP.GND
05A			BP.LOG.ADDR9+	BP.LOG.ADDR9+
05B			BP.EXT.ADDR0+	BP.EXT.ADDR0+
05C			BP.EXT.ADDR1+	BP.EXT.ADDR1+
05D			FP.MEM.ADDR10+	FP.MEM.ADDR10+
06A	CK.A.CPU3.DP+	CK.A.CPU3.DP+	FP.MEM.ADDR11+	FP.MEM.ADDR11+
06B	CK.A.CPU4.DP+	CK.A.CPU4.DP+	FP.MEM.ADDR12+	FP.MEM.ADDR12+
06C			FP.MEM.ADDR13+	FP.MEM.ADDR13+
06D			FP.MEM.ADDR14+	FP.MEM.ADDR14+
07A			FP.MEM.ADDR15+	FP.MEM.ADDR15+
07B			FP.MEM.ADDR16+	FP.MEM.ADDR16+
07C			FP.MEM.ADDR17+	FP.MEM.ADDR17+
07D			FP.MEM.ADDR18+	FP.MEM.ADDR18+
08A	BP.+5V	BP.+5V	BP.+5V	BP.+5V
08B			FP.MEM.ADDR19+	FP.MEM.ADDR19+
08C	SQ.DP.SPARE1+	SQ.DP.SPARE1+	FP.MEM.ADDR20+	FP.MEM.ADDR20+
08D	CK.A.CPU4.LED.BP+	CK.A.CPU4.LED.BP+	FP.MEM.ADDR21+	FP.MEM.ADDR21+
09A			FP.MEM.ADDR22+	FP.MEM.ADDR22+
09B	BP.LED.STOT-	BP.LED.STOT-	FP.MEM.ADDR23+	FP.MEM.ADDR23+
09C	BP.R2.STORE.EN-	BP.R2.STORE.EN-	BP.R2.STORE.EN-	BP.R2.STORE.EN-
09D	BP.MISSED.TICK-		LBP.SC0+	BP.MISSED.TICK-
10A	CK.A.CAC1.CA+	BP.AB.DP.WR+	CK.A.CAC1.CA+	BP.AB.DP.WR+
10B	CK.A.CAC2.CA+		CK.A.CAC2.CA+	LBP.MLOST-

BACKPLANE SIGNALS				
PIN	SQ	DP	CA	MC
10C	BP.PE.FREEZE-		LBP.SC1+	BP.PE.FREEZE-
10D	BP.CPU.FREEZE-	BP.AB.CA.WR-	BP.CPU.FREEZE-	BP.AB.CA.WR-
11A		BP.B.CA.ADR+	BP.B.CA.ADR+	BP.B.CA.ADR+
11B	BP.UINTP+		LBP.SC2+	BP.UINTP+
11C	BP.T.BUS0+	BP.T.BUS0+	BP.T.BUS0+	BP.T.BUS0+
11D	BP.T.BUS1+	BP.T.BUS1+	BP.T.BUS1+	BP.T.BUS1+
12A	BP.GND	BP.GND	BP.GND	BP.GND
12B	BP.GND	BP.GND	BP.GND	BP.GND
12C	BP.GND	BP.GND	BP.GND	BP.GND
12D	BP.GND	BP.GND	BP.GND	BP.GND
13A	BP.T.BUS2+	BP.T.BUS2+	BP.T.BUS2+	BP.T.BUS2+
13B	BP.T.BUS3+	BP.T.BUS3+	BP.T.BUS3+	BP.T.BUS3+
13C	BP.T.BUS4+	BP.T.BUS4+	BP.T.BUS4+	BP.T.BUS4+
13D	BP.T.BUS5+	BP.T.BUS5+	BP.T.BUS5+	BP.T.BUS5+
14A	BP.T.BUS6+	BP.T.BUS6+	BP.T.BUS6+	BP.T.BUS6+
14B	BP.T.BUS7+	BP.T.BUS7+	BP.T.BUS7+	BP.T.BUS7+
14C	BP.T.BUS8+	BP.T.BUS8+	BP.T.BUS8+	BP.T.BUS8+
14D	BP.T.BUS9+	BP.T.BUS9+	BP.T.BUS9+	BP.T.BUS9+
15A	BP.T.BUS10+	BP.T.BUS10+	BP.T.BUS10+	BP.T.BUS10+
15B	BP.T.BUS11+	BP.T.BUS11+	BP.T.BUS11+	BP.T.BUS11+
15C	BP.T.BUS12+	BP.T.BUS12+	BP.T.BUS12+	BP.T.BUS12+
15D	BP.T.BUS13+	BP.T.BUS13+	BP.T.BUS13+	BP.T.BUS13+
16A	BP.+5V	BP.+5V	BP.+5V	BP.+5V
16B	BP.T.BUS14+	BP.T.BUS14+	BP.T.BUS14+	BP.T.BUS14+
16C	BP.T.BUS15+	BP.T.BUS15+	BP.T.BUS15+	BP.T.BUS15+
16D	BP.UIR.REG0+	BP.UIR.REG0+	BP.MP.INT+	BP.MP.INT+
17A	BP.UIR.REG1+	BP.UIR.REG1+	BP.TRUE.WRITE+	BP.TRUE.WRITE+
17B	BP.UIR.REG2+	BP.UIR.REG2+	BP.AB.HIT+	BP.AB.HIT+
17C	BP.UIR.REG3+	BP.UIR.REG3+	BP.NORMAL+	BP.NORMAL+
17D	BP.UIR.REG4+	BP.UIR.REG4+	BP.INVERT+	BP.INVERT+
18A	BP.UIR.REG5+	BP.UIR.REG5+	BP.LDOUT.EN-	BP.LDOUT.EN-
18B	BP.UIR.REG6+	BP.UIR.REG6+	BP.NO.WP+	BP.NO.WP+
18C	BP.UIR.REG7+	BP.UIR.REG7+	LBP.IOGO-	LBP.IOGO-
18D	BP.UIR.REG8+	BP.UIR.REG8+	BP.UIR.REG8+	
19A	BP.UIR.REG9+	BP.UIR.REG9+	BP.UIR.REG9+	LBP.PE-
19B	BP.UIR.REG10+	BP.UIR.REG10+	BP.UIR.REG10+	LBP.MCHODOC-
19C	BP.UIR.REG11+	BP.UIR.REG11+	BP.UIR.REG11+	LBP.PFW-
19D	BP.UIR.REG12+	BP.UIR.REG12+	BP.UIR.REG12+	BP.UIR.REG12+
20A	BP.GND	BP.GND	BP.GND	BP.GND
20B	BP.GND	BP.GND	BP.GND	BP.GND
20C	BP.GND	BP.GND	BP.GND	BP.GND
20D	BP.GND	BP.GND	BP.GND	BP.GND
21A	BP.UIR.REG13+	BP.UIR.REG13+	BP.UIR.REG13+	LBP.SCHOD-
21B	BP.UIR.REG14+	BP.UIR.REG14+	BP.UIR.REG14+	LBP.DB0+

BACKPLANE SIGNALS				
PIN	SQ	DP	CA	MC
21C	BP.UIR.REG15+	BP.UIR.REG15+	LBP.SC4+	LBP.DB1+
21D	BP.UIR.REG16+	BP.UIR.REG16+	LBP.SC5+	LBP.DB2+
22A	BP.UIR.REG17+	BP.UIR.REG17+	LBP.AB0+	LBP.DB3+
22B	BP.UIR.REG18+	BP.UIR.REG18+	LBP.AB1+	LBP.DB4+
22C	BP.UIR.REG19+	BP.UIR.REG19+	LBP.AB2+	LBP.DB5+
22D	BP.R2.UIR.REG20+	BP.R2.UIR.REG20+	BP.R2.UIR.REG20+	BP.R2.UIR.REG20+
23A	BP.R2.UIR.REG21+	BP.R2.UIR.REG21+	BP.R2.UIR.REG21+	BP.R2.UIR.REG21+
23B	BP.R2.UIR.REG22+	BP.R2.UIR.REG22+	BP.R2.UIR.REG22+	BP.R2.UIR.REG22+
23C	BP.R2.UIR.REG23+	BP.R2.UIR.REG23+	BP.R2.UIR.REG23+	BP.R2.UIR.REG23+
23D	BP.UIR.REG24+	BP.UIR.REG24+	LBP.AB3+	LBP.DB6+
24A	BP.+5V	BP.+5V	BP.+5V	BP.+5V
24B	BP.UIR.REG25+	BP.UIR.REG25+	LBP.AB4+	LBP.DB7+
24C	BP.UIR.REG26+	BP.UIR.REG26+	BP.UIR.REG26+	BP.UIR.REG26+
24D	BP.UIR.REG27+	BP.UIR.REG27+	BP.UIR.REG27+	BP.UIR.REG27+
25A	BP.UIR.REG28+	BP.UIR.REG28+	BP.UIR.REG28+	BP.UIR.REG28+
25B	BP.UIR.REG29+	BP.UIR.REG29+	BP.UIR.REG29+	BP.UIR.REG29+
25C	BP.UIR.REG30+	BP.UIR.REG30+	BP.UIR.REG30+	BP.UIR.REG30+
25D	BP.UIR.REG31+	BP.UIR.REG31+	BP.UIR.REG31+	BP.UIR.REG31+
26A	BP.UIR.REG32+	BP.UIR.REG32+	LBP.AB5+	LBP.DB8+
26B	BP.UIR.REG33+	BP.UIR.REG33+	LBP.AB6+	LBP.DB9+
26C	BP.UIR.REG34+	BP.UIR.REG34+	LBP.AB7+	LBP.DB10+
26D	BP.UIR.REG35+	BP.UIR.REG35+	LBP.AB8+	LBP.DB11+
27A	BP.UIR.REG36+	BP.UIR.REG36+	LBP.AB9+	LBP.DB12+
27B	BP.UIR.REG37+	BP.UIR.REG37+	LBP.AB10+	LBP.DB13+
27C	BP.UIR.REG38+	BP.UIR.REG38+	LBP.AB11+	LBP.DB14+
27D	BP.UIR.REG39+	BP.UIR.REG39+	LBP.AB12+	LBP.DB15+
28A	BP.GND	BP.GND	BP.GND	BP.GND
28B	BP.GND	BP.GND	BP.GND	BP.GND
28C	BP.GND	BP.GND	BP.GND	BP.GND
28D	BP.GND	BP.GND	BP.GND	BP.GND
29A	BP.UIR.REG40+	BP.UIR.REG40+	LBP.REMEM-	LBP.REMEM-
29B	BP.UIR.REG41+	BP.UIR.REG41+	LBP.AB13+	LBP.INTRQ-
29C	BP.UIR.REG42+	BP.UIR.REG42+	LBP.AB14+	LBP.MP+
29D	BP.UIR.REG43+	BP.UIR.REG43+	LBP.MEMGO-	LBP.MEMGO-
30A	BP.UIR.REG44+	BP.UIR.REG44+	LBP.WE-	LBP.WE-
30B	BP.UIR.REG45+	BP.UIR.REG45+	LBP.CPUTURN-	LBP.SLAVE-
30C	BP.UIR.REG46+	BP.UIR.REG46+	LBP.MRQ-	LBP.MRQ-
30D		BP.JTAB.MEM-	LBP.VALID-	BP.JTAB.MEM-
31A		LBP.IORQ-	LBP.RNI-	LBP.IORQ-
31B	MAGIC.SPARE1+	MAGIC.SPARE1+	MAGIC.SPARE1+	MAGIC.SPARE1+
31C			BP.DMA.CYCLE.2B+	BP.DMA.CYCLE.2B+
31D	CK.A.MEM.MC+		LBP.IAK-	CK.A.MEM.MC+
32A	BP.+5V	BP.+5V	BP.+5V	BP.+5V
32B	LBP.SCLK-		LBP.SCLK-	LBP.SCLK-
32C	BP.NO.EXECUTE-	BP.NO.EXECUTE-	BP.NO.EXECUTE-	LBP.CCLK-
32D	BP.KIS.S.OFF-		LBP.SC3+	BP.KIS.S.OFF-

BACKPLANE SIGNALS				
PIN	SQ	DP	CA	MC
33A	BP.IND.INT-	BP.B.DP.ADR+	BP.IND.INT-	BP.B.DP.ADR+
33B	LBP.PON+	LBP.PON+	LBP.PON+	LBP.PON+
33C	CK.A.MEM.D10.BP+	CK.A.MEM.D10.BP+	FP.MEM.ADDR9+	FP.MEM.ADDR9+
33D	CK.A.MEM.D50.BP+	CK.A.MEM.D50.BP+	CK.A.MEM.D50.BP+	CK.A.MEM.D50.BP+
34A	BP.S.BUS0+	BP.S.BUS0+	BP.S.BUS0+	BP.S.BUS0+
34B	BP.S.BUS1+	BP.S.BUS1+	BP.S.BUS1+	BP.S.BUS1+
34C	BP.S.BUS2+	BP.S.BUS2+	BP.S.BUS2+	BP.S.BUS2+
34D	BP.S.BUS3+	BP.S.BUS3+	BP.S.BUS3+	BP.S.BUS3+
35A	BP.S.BUS4+	BP.S.BUS4+	BP.S.BUS4+	BP.S.BUS4+
35B	BP.S.BUS5+	BP.S.BUS5+	BP.S.BUS5+	BP.S.BUS5+
35C	BP.S.BUS6+	BP.S.BUS6+	BP.S.BUS6+	BP.S.BUS6+
35D	BP.S.BUS7+	BP.S.BUS7+	BP.S.BUS7+	BP.S.BUS7+
36A	BP.GND	BP.GND	BP.GND	BP.GND
36B	BP.GND	BP.GND	BP.GND	BP.GND
36C	BP.GND	BP.GND	BP.GND	BP.GND
36D	BP.GND	BP.GND	BP.GND	BP.GND
37A	BP.S.BUS8+	BP.S.BUS8+	BP.S.BUS8+	BP.S.BUS8+
37B	BP.S.BUS9+	BP.S.BUS9+	BP.S.BUS9+	BP.S.BUS9+
37C	BP.S.BUS10+	BP.S.BUS10+	BP.S.BUS10+	BP.S.BUS10+
37D	BP.S.BUS11+	BP.S.BUS11+	BP.S.BUS11+	BP.S.BUS11+
38A	LBP.+5M		LBP.CRS-	LBP.+5M
38B	BP.S.BUS12+	BP.S.BUS12+	BP.S.BUS12+	BP.S.BUS12+
38C	BP.S.BUS13+	BP.S.BUS13+	BP.S.BUS13+	BP.S.BUS13+
38D	BP.S.BUS14+	BP.S.BUS14+	BP.S.BUS14+	BP.S.BUS14+
39A			LBP.BUSY-	LBP.BUSY-
39B	BP.S.BUS15+	BP.S.BUS15+	BP.S.BUS15+	BP.S.BUS15+
39C	BP.ACCL.STOT-	BP.ACCL.STOT-	BP.MEM.RD.REQ+	BP.MEM.RD.REQ+
39D		LBP.+12V	BP.MEM.WR.REQ+	BP.MEM.WR.REQ+
40A	BP.+5V	BP.+5V	BP.+5V	BP.+5V
40B	BP.CNDX.MET+	BP.CNDX.MET+	BP.MEM.BUSY+	BP.MEM.BUSY+
40C	BP.JTAB.INT-	BP.NINC.SP1-	BP.NINC.SP1-	BP.JTAB.INT-
40D		BP.INTP+	BP.INTP+	BP.INTP+

Appendix B
Processor Frontplane Signals

FRONTPLANE SIGNALS				
	MC AND AR	CS AND SQ	CA	DP
01A	FP.AR.BD.SEL-			
01B	FP.MEM.DATA38+			
01C	FP.MEM.DATA37+			DP.OVFL+
02A	FP.MEM.DATA36+			DP.COUT+
02B	FP.GND	FP.GND	FP.GND	FP.GND
02C	FP.MEM.DATA35+	FP.BD.ON-		DP.F2+
03A	FP.MEM.DATA34+	FP.XCS2-		DP.F1+
03B	FP.MEM.DATA33+	FP.XCS1-		DP.O+
03C	FP.MEM.DATA32+	FP.IJT.EN+		DP.E+
04A	FP.GND	FP.GND	FP.GND	FP.GND
04B	FP.MEM.DATA31+	FP.CS.OUT47+		DP.L.BUS15+
04C	FP.MEM.DATA30+	FP.CS.OUT46+		DP.L.BUS14+
05A	FP.MEM.DATA29+	FP.CS.OUT45+		DP.L.BUS13+
05B	FP.MEM.DATA28+	FP.CS.OUT44+	CA.RRR.CYCLE+	DP.L.BUS12+
05C	FP.GND	FP.GND	FP.GND	FP.GND
06A	FP.MEM.DATA27+	FP.CS.OUT43+	CA.BOOT.MEM+	DP.L.BUS11+
06B	FP.MEM.DATA26+	FP.CS.OUT42+	CA.AB.EN.CYCLE-	DP.L.BUS10+
06C	FP.MEM.DATA25+	FP.CS.OUT41+	CA.MP.OUT4+	DP.L.BUS9+
07A	FP.MEM.DATA24+	FP.CS.OUT40+	CA.MP.OUT3+	DP.L.BUS8+
07B	FP.GND	FP.GND	FP.GND	FP.GND
07C	FP.MEM.DATA23+	FP.CS.OUT39+	CA.MP.OUT2+	DP.L.BUS7+
08A	FP.MEM.DATA22+	FP.CS.OUT38+	CA.MP.OUT1+	DP.L.BUS6+
08B	FP.MEM.DATA21+	FP.CS.OUT37+	CA.MP.OUT0+	DP.L.BUS5+
08C	FP.MEM.DATA20+	FP.CS.OUT36+	CA.MADR.OUT14+	DP.L.BUS4+
09A	FP.GND	FP.GND	FP.GND	FP.GND
09B	FP.MEM.DATA19+	FP.CS.OUT35+	CA.MADR.OUT13+	DP.L.BUS3+
09C	FP.MEM.DATA18+	FP.CS.OUT34+	CA.MADR.OUT12+	DP.L.BUS2+
10A	FP.MEM.DATA17+	FP.CS.OUT33+	CA.MADR.OUT11+	DP.L.BUS1+
10B	FP.MEM.DATA16+	FP.CS.OUT32+	CA.MADR.OUT10+	DP.L.BUS0+
10C	FP.GND	FP.GND	FP.GND	FP.GND
11A	FP.MEM.DATA15+	FP.CS.OUT31+	CA.S.BUS.IN15+	DP.R.BUS15+
11B	FP.MEM.DATA14+	FP.CS.OUT30+	CA.S.BUS.IN14+	DP.R.BUS14+
11C	FP.MEM.DATA13+	FP.CS.OUT29+	CA.S.BUS.IN13+	DP.R.BUS13+
12A	FP.MEM.DATA12+	FP.CS.OUT28+	CA.S.BUS.IN12+	DP.R.BUS12+
12B	FP.GND	FP.GND	FP.GND	FP.GND
12C	FP.MEM.DATA11+	FP.CS.OUT27+	CA.S.BUS.IN11+	DP.R.BUS11+
13A	FP.MEM.DATA10+	FP.CS.OUT26+	CA.S.BUS.IN10+	DP.R.BUS10+
13B	FP.MEM.DATA9+	FP.CS.OUT25+	CA.S.BUS.IN9+	DP.R.BUS9+
13C	FP.MEM.DATA8+	FP.CS.OUT24+	CA.S.BUS.IN8+	DP.R.BUS8+

FRONTPLANE SIGNALS				
	MC AND AR	CS AND SQ	CA	DP
14A	FP.GND	FP.GND	FP.GND	FP.GND
14B	FP.MEM.DATA7+	FP.CS.OUT23+	CA.S.BUS.IN7+	DP.R.BUS7+
14C	FP.MEM.DATA6+	FP.CS.OUT22+	CA.S.BUS.IN6+	DP.R.BUS6+
15A	FP.MEM.DATA5+	FP.CS.OUT21+	CA.S.BUS.IN5+	DP.R.BUS5+
15B	FP.MEM.DATA4+	FP.CS.OUT20+	CA.S.BUS.IN4+	DP.R.BUS4+
15C	FP.GND	FP.GND	FP.GND	FP.GND
16A	FP.MEM.DATA3+	FP.CS.OUT19+	CA.S.BUS.IN3+	DP.R.BUS3+
16B	FP.MEM.DATA2+	FP.CS.OUT18+	CA.S.BUS.IN2+	DP.R.BUS2+
16C	FP.MEM.DATA1+	FP.CS.OUT17+	CA.S.BUS.IN1+	DP.R.BUS1+
17A	FP.MEM.DATA0+	FP.CS.OUT16+	CA.S.BUS.IN0+	DP.R.BUS0+
17B	FP.GND	FP.GND	FP.GND	FP.GND
17C	FP.REF.EN-	FP.CS.OUT15+	CA.DMA.CYCLE-	BP.T.BUS15+
18A	FP.RD.EN+	FP.CS.OUT14+	BP.TRUE.WRITE+	BP.T.BUS14+
18B	FP.GND	FP.CS.OUT13+	CA.JTAB.CREATE-	BP.T.BUS13+
18C	FP.RAS+	FP.CS.OUT12+	BP.NO.EXECUTE-	BP.T.BUS12+
19A	FP.GND	FP.GND	FP.GND	FP.GND
19B	FP.WE-	FP.CS.OUT11+	CA.RRR.HIT+	BP.T.BUS11+
19C	FP.GND	FP.CS.OUT10+	CA.INDIRECT-	BP.T.BUS10+
20A	FP.INIT.MODE+	FP.CS.OUT9+	CA.HIT+	BP.T.BUS9+
20B	FP.INIT.CLK+	FP.CS.OUT8+	BP.CPU.FREEZE-	BP.T.BUS8+
20C	FP.GND	FP.GND	FP.GND	FP.GND
21A	FP.MEM.ADDR23+	FP.CS.OUT7+	CA.DMS23+	BP.T.BUS7+
21B	FP.MEM.ADDR22+	FP.CS.OUT6+	CA.DMS22+	BP.T.BUS6+
21C	FP.MEM.ADDR21+	FP.CS.OUT5+	CA.DMS21+	BP.T.BUS5+
22A	FP.MEM.ADDR20+	FP.CS.OUT4+	CA.DMS20+	BP.T.BUS4+
22B	FP.GND	FP.GND	FP.GND	FP.GND
22C	FP.MEM.ADDR19+	FP.CS.OUT3+	CA.DMS19+	BP.T.BUS3+
23A	FP.MEM.ADDR18+	FP.CS.OUT2+	CA.DMS18+	BP.T.BUS2+
23B	FP.MEM.ADDR17+	FP.CS.OUT1+	CA.DMS17+	BP.T.BUS1+
23C	FP.MEM.ADDR16+	FP.CS.OUT0+	CA.DMS16+	BP.T.BUS0+
24A	FP.GND	FP.GND	FP.GND	FP.GND
24B	FP.MEM.ADDR15+	FP.NO.EXECUTE+	CA.DMS15+	DP.U.BUS15+
24C	FP.MEM.ADDR14+	FP.UADR14+	CA.DMS14+	DP.U.BUS14+
25A	FP.MEM.ADDR13+	FP.UADR13+	CA.DMS13+	DP.U.BUS13+
25B	FP.MEM.ADDR12+	FP.UADR12+	CA.DMS12+	DP.U.BUS12+
25C	FP.GND	FP.GND	FP.GND	FP.GND
26A	FP.MEM.ADDR11+	FP.UADR11+	CA.DMS11+	DP.U.BUS11+
26B	FP.MEM.ADDR10+	FP.UADR10+	CA.DMS10+	DP.U.BUS10+
26C	FP.MEM.ADDR9+	FP.UADR9+	CA.MADR.OUT9+	DP.U.BUS9+
27A	FP.MEM.ADDR8+	FP.UADR8+	CA.MADR.OUT8+	DP.U.BUS8+
27B	FP.GND	FP.GND	FP.GND	FP.GND
27C	FP.MEM.ADDR7+	FP.UADR7+	CA.MADR.OUT7+	DP.U.BUS7+
28A	FP.MEM.ADDR6+	FP.UADR6+	CA.MADR.OUT6+	DP.U.BUS6+
28B	FP.MEM.ADDR5+	FP.UADR5+	CA.MADR.OUT5+	DP.U.BUS5+
28C	FP.MEM.ADDR4+	FP.UADR4+	CA.MADR.OUT4+	DP.U.BUS4+

FRONTPLANE SIGNALS				
	MC AND AR	CS AND SQ	CA	DP
29A	FP.GND	FP.GND	FP.GND	FP.GND
29B	FP.MEM.ADDR3+	FP.UADR3+	CA.MADR.OUT3+	DP.U.BUS3+
29C	FP.MEM.ADDR2+	FP.UADR2+	CA.MADR.OUT2+	DP.U.BUS2+
30A	FP.MEM.ADDR1+	FP.UADR1+	CA.MADR.OUT1+	DP.U.BUS1+
30B	FP.NEXT.AR.BD-	FP.UADR0+	CA.MADR.OUT0+	DP.U.BUS0+
30C	FP.+5VM	FP.+5V	FP.+5V	FP.+5V
31A	FP.CK.MEM.MC+	FP.CK.CPU.SQ-	CK.A.CAC2.B.CA-	FP.CK.CPU.DP-
31B	FP.+5VM	FP.+5V	FP.+5V	FP.+5V
31C	FP.ADDR.CLK+	FP.CK.CPU.SQ-	CK.A.CAC2.B.CA-	FP.CK.CPU.DP-
32A	FP.GND	FP.GND	FP.GND	FP.GND
32B	FP.MEM.CH.IN+	FP.EXT.CLK.EN-		
32C	FP.MEM.CH.OUT+	FP.EXT.CLK-		

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HEWLETT PACKARD

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The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

First Edition	May 1984	
Update 1	Jan 1985	
Reprint	Jan 1985	Update 1 Incorporated

Figure 5-2. Cache Control Card (12203-60004)

5.2.1 Memory Address Creation

Address creation is quite important to the microprogrammer and is discussed from the microprogrammer's point of view in the HP92049A RTE Microprogramming Package Reference Manual. The following description supplements the microprogramming manual information.

5.2.1.1 Logical Address Registers

To the microprogrammer, it appears there are only three address sources: M1, M2, and PC. In reality, there are five sources. The two additional sources are the MADR HOLD buffer and the I/O Address from the backplane.

MADR HOLD (the first additional logical address source) is a buffer to keep the current MADR address while MADR is not updated for some reason; e.g., the address sources may not be correct. Because MADR is always clocked (gated clock signals are not permitted) the only way the present value can be saved is to reload it with a buffered version of its output from MADR HOLD.

The MADR HOLD buffer has several uses. One use is to keep the present address during cache fault processing. When it is determined that the cache has missed and that fault handling is going to be necessary, the logical address latches are already updated with their new values. Therefore, MADR HOLD keeps the old value for use in the next cycle.

A second use for the MADR HOLD buffer is for a JTAB operation that is A/B addressable. The A- or B-Register might still be updated from the previous macroinstruction. An example of this is LDB executed in the A-Register. The B-Register will be updated at the end of the cycle that is also reading the instruction from the B-Register. To get the correct answer, the fetch needs to be delayed one cycle, but the address latches might already be updated so the address comes from MADR HOLD.

A third use for the MADR HOLD buffer serves another function in transforming the cache from a 2k x 16 cache to a 1k x 32 cache for faster fault handling. This is covered in the Data Store paragraph in the block diagram description subsection and in the theory of operation subsection.

A fourth use for the MADR HOLD buffer is to hold the current address when the CPU freezes on a write request to the cache due to the following: the Write Data Register (WDR) is not free, and the addressed location is not in the cache (refer to the explanation of the WDR under the subsection Cache Fault Handling). To ensure proper execution of the write, the CPU remains frozen and MADR HOLD keeps the address until one of two conditions comes true: 1. The request hits the cache and thus WDR is not needed, or 2. The WDR becomes free.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	95051
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

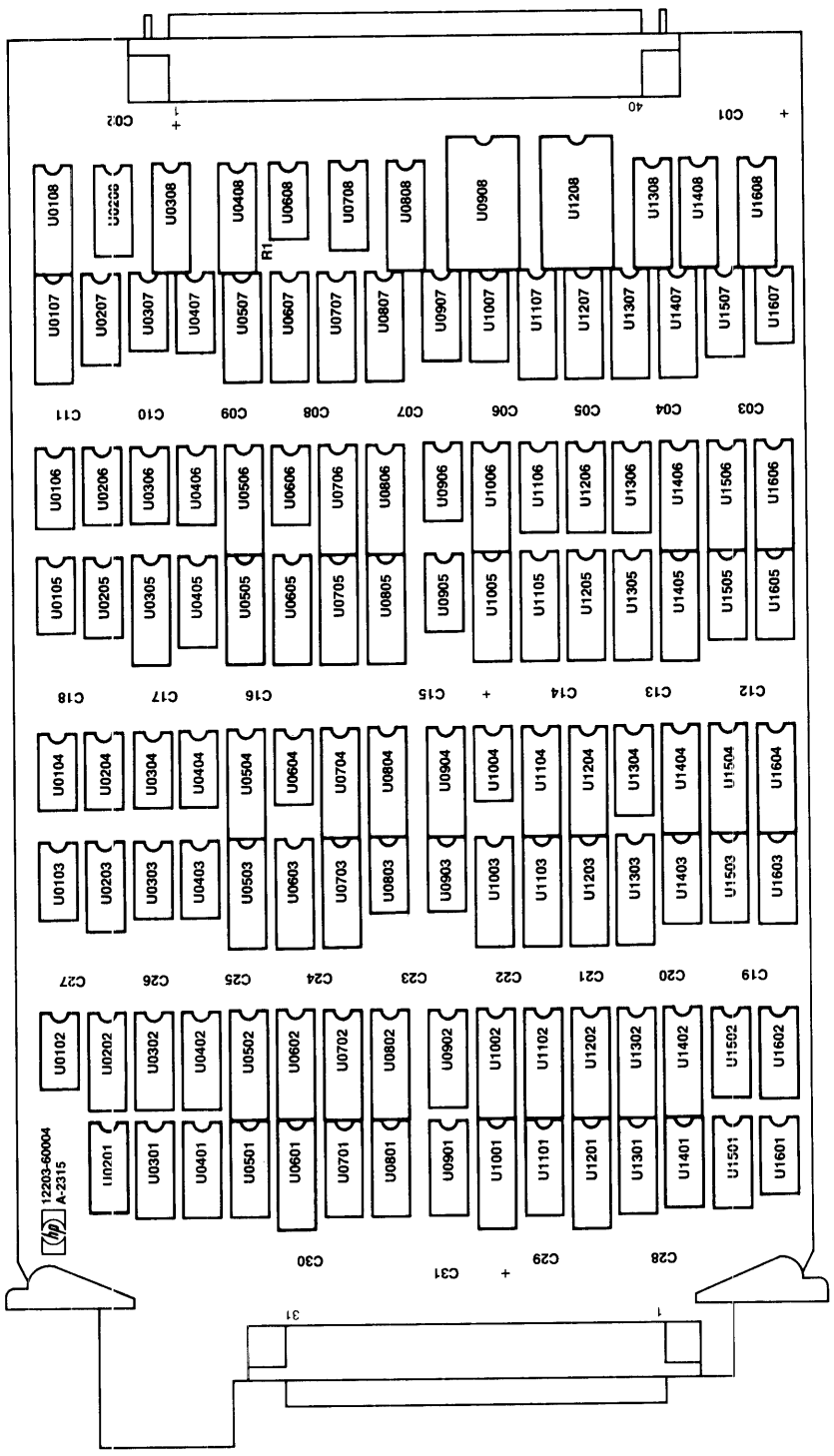


Figure 5-12. Cache Control Card Parts Locations

Table 5-1. Cache Control Card Replaceable Parts (Sheet 1 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12203-60004	6	1	PCA-CACHE CNTRL	28480	12203-60004
C1	0180-0229	7	4	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-4835	7	27	CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C4	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C13	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C14	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C15	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C29	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C30	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C31	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
R1	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
U102	1820-1275	4	4	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U103	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U104	1820-0605	8	2	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U105	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U106	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U107	1820-2701	3	18	IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U108	1820-2795	5	17	IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U201	1816-1583	8	2	IC TTL 1024 (1K) STAT RAM 20-NS 3-S	28480	1816-1583
U202	1818-3052	4	12	IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U203	1816-1583	8		IC TTL 1024 (1K) STAT RAM 20-NS 3-S	28480	1816-1583
U204	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U205	1820-0686	9	3	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U206	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U207	1820-2769	3	9	IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U208	1820-2654	5	1	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U301	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U302	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U303	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U304	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74S04N
U305	1820-3272	5	1	IC PRGMBL-LGC TTL S	28480	1820-3272
U306	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U307	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U308	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U401	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U402	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U403	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U404	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U405	1820-2693	2	2	IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U406	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U407	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U408	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U501	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U502	1820-2700	2	13	IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U503	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U504	1820-3056	3	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3056
U505	1820-3274	7	1	IC PRGMBL-LGC TTL S	28480	1820-3274
U506	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U507	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U601	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U602	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC

Table 5-1. Cache Control Card Replaceable Parts (Sheet 2 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U603	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U604	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U605	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U606	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U607	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U608	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U701	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U702	1820-2311	1	2	IC COMPTR TTL LS MAGTD 8-BIT	34335	AM25LS2521PC
U703	1820-2311	1		IC COMPTR TTL LS MAGTD 8-BIT	34335	AM25LS2521PC
U704	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U705	1820-3273	6	1	IC PRGMBL-LGC TTL S	28480	1820-3273
U706	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U707	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U708	1820-1240	3	3	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U801	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U802	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U803	1820-0680	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U804	1820-3275	8	1	IC PRGMBL-LGC TTL S	28480	1820-3275
U805	1820-3055	2	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3055
U806	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U807	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U808	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U901	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U902	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U903	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U904	1820-3054	1	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3054
U905	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U906	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U907	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1001	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1002	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1003	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1004	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U1005	1820-3023	4	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3023
U1006	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1007	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1101	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U1102	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1103	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1104	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1105	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1106	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1107	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1201	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1202	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1203	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1204	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1205	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1206	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1207	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1301	1818-3052	4		IC NMOS 4096 (4K) STAT RAM 45-NS 3-S	28480	1818-3052
U1302	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1303	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1304	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1305	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1306	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1307	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1308	1820-3050	7	1	IC PRGMBL-LGC TTL S PLA	28480	1820-3050
U1401	1820-2693	2		IC FF TTL F J-K BAR POS-EDGE-TRIG	07263	74F109PC
U1402	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1403	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1404	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1405	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1406	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1407	1820-2795	5		IC DRVR TTL F LINE DRVR OCTL	28480	1820-2795
U1408	1820-2701	3		IC FF TTL F D-TYPE POS-EDGE-TRIG COM	07263	74F374PC
U1501	1820-2936	6	1	IC MUXR/DATA-SEL TTL F 8-TO-1-LINE	28480	1820-2936
U1502	1820-1871	6	4	IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1503	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1504	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1505	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1506	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1507	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1601	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1602	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N

Table 5-1. Cache Control Card Replaceable Parts (Sheet 3 of 3)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1603	1820-2769	3		IC MUXR/DATA-SEL TTL F 4-TO-1-LINE DUAL	07263	74F153PC
U1604	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1605	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U1606	1820-2700	2		IC LCH TTL F D-TYPE OCTL	07263	74F373PC
U1607	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U1608	1820-3271	4	1	IC PRGMBL-LGC TTL S	28480	1820-3271

			D-12203-60004-51
A	AS ISSUED	maf/ko	5/5/83

M1 MUX

M1

MADR ADDER

69A 40D 160B — CA.S.BUS.IN+ /16
30A 60A 140A 155A — BP.T.BUS+ /15
29A 40A 50B 60C 70E 90A 110A 163B — CA.MADR.OUT+ /16

15 / CA.MADR.ADDER+ → 20A 60D

CA.M1.IN+

16 / CA.MADR.IN+ → 20A 39B

-1871 74S283 U1602
(20) (19) (18) (265) (264) (263) → A4 A3 A2 A1 B4 B3 B2 B1
S4 S3 S2 S1 → (131) (130) (129)
CO → 7 CA.ADDER.CRY3+

-1871 74S283 U1502
(14) (12) (3) (11) (262) (261) (273) (272) → A4 A3 A2 A1 B4 B3 B2 B1
C4 → (341)
S4 S3 S2 S1 → (127) (126) (139) (138)
CO → 7 CA.ADDER.CRY2+

-1871 74S283 U1605
(10) (9) (8) (7) (271) (270) (269) (268) → A4 A3 A2 A1 B4 B3 B2 B1
C4 → (340)
S4 S3 S2 S1 → (137) (136) (135) (134)
CO → 7 CA.ADDER.CRY1+

-1871 74S283 U1505
(6) (5) (4) (17) (267) (266) (280) (259) → A4 A3 A2 A1 B4 B3 B2 B1
C4 → (339)
S4 S3 S2 S1 → (133) (132) (125) (124)
CO → 7

69A CA.B.CA.PINC+ /15

-2769 74F153 U1803
(146) (87) (146) (20) (131) (227) (204) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (406)
2Y → 9 (405)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1304
(19) (130) (226) (203) (18) (129) (225) (202) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (404)
2Y → 9 (403)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1503
(14) (127) (223) (201) (12) (126) (222) (200) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (402)
2Y → 9 (401)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1403
(154) (139) (229) (154) (153) (138) (228) (153) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (414)
2Y → 9 (413)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1507
(152) (137) (122) (152) (151) (136) (121) (151) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (412)
2Y → 9 (411)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1206
(150) (135) (120) (150) (149) (134) (119) (149) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (410)
2Y → 9 (409)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1306
(148) (133) (118) (148) (147) (132) (117) (147) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (408)
2Y → 9 (407)
A B → 14 2
1G 2G → 1 15

-2769 74F153 U1106
(145) (125) (116) (145) (144) (124) (115) (144) → 1C0 1C1 1C3 1C4 2C0 2C1 2C2 2C3
1Y → 7 (400)
2Y → 9 (399)
A B → 14 2
1G 2G → 1 15

-2700 74F373 U1404
(406) (405) (404) (403) (402) (401) (414) (413) → D8 D7 D6 D5 D4 D3 D2 D1
Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 → (85) (84) (59) (83) (58) (82) (68) (67)
G OE → 11 1

-2700 74F373 U1406
(412) (411) (410) (409) (408) (407) (400) (399) → D8 D7 D6 D5 D4 D3 D2 D1
Q8 Q7 Q6 Q5 Q4 Q3 Q2 Q1 → (66) (65) (63) (62) (61) (60) (57) (37)
G OE → 11 1

119E CA.FORCE.PAGE0+ (81)
129B CA.M1.SEL.A+ (33)
129B CA.M1.SEL.B+ (34)

129A CK.A.CAC2.M1.LD+ (285)
119C 30B CA.M1.EN- (195)

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

M1 SELECT:

B	A	BIT15	BITS 14-10	BITS 9-0	USE
0	0	S.BUS	MADR	S.BUS	MGR address create
0	1	MADR	ADDER	ADDER	Address increment & RRR Q add
1	0	Ground	T.BUS	T.BUS	Loading M1 from Data Path
1	1	S.BUS	S.BUS	S.BUS	Indirection

CA1

	CACHE CONTROLLER -A900 ADDRESS INCREMENTER &M1	HEWLETT PACKARD
	12203A	12203-60004
		D-12203-60004-51

D-12203-80004-52

A	AS ISSUED	ko	5-5-83

MADR HOLD

M2
-2700
74F373
U1504

PC
-2700
74F373
U1604

-2700
74F373
U1506

-2700
74F373
U1606

-2795
74F244
U1204

-2785
74F244
U0108

MADR
-2701
74F374
U1104

-2701
74F374
U0107

CDADR
-2701
74F374
U0408

74F374
U0308

-0683
74S04
U0304

-1322
74S02
U0306

-2654
74F157
U0208

149D 30C 110A (15) CA.NO.HOLDS+
39A (180) CA.BOOT.2B-
49C 50D 70C 90B 160C (13) CA.DMS10+
49C 50D CA.PAGE.ODD-
19C 39B CA.MADR.IN+ 16
19A 50D CA.MADR.ADDER+ 15
129B 30D (205) CK.A.CAC2.M2LD+
119C 30D (196) CA.M2.EN-
129A 30E (206) CK.A.CAC2.PC.LD+
119B 30E (199) CA.PC.EN-
119B CA.TRUE.DMA.REQ+ (452)
154E 60B 80C 30E CK.A.CAC1.CA+ (35)
139C CA.PULLUP+ (21)
13 (59) 9 CA.MADR.IN 13- (419) 11
11 (58)
CA.EXT.IN1+ (372)
CA.EXT.IN0+ (371)
0 (37) CA.LOG.ON+ (397)
0 (37) CA.LOG.01+ (398)
(208)
(1) BP.DMA.CYCLE.2B+
CA.NO.HOLDS-
A/B
16 CA.MADR.OUT+ 10A 40A 50A 80C 70E 90A 110A 163B

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

9 BP.LOG.ADDR+ 151A
(308) BP.EXT.ADDR1+ 151D
(307) BP.EXT.ADDR0+ 151D

RAM Address | DATA STORE MEMORY MAP
0K Cache Memory (Boot 2-3K)
2K Boot 0-1K
4K Boot 10-11K
6K Boot 8-9K
8K

(313) BP.LOG.ADDR0N+ 151D
(312) BP.LOG.ADDR0I+ 151D
(234) CA.BOOT.CYCLE- 110A 140A
(31) CA.DMA.CYCLE+ 70A 80C 90C 120B
(496) BP.DMA.CYCLE+ 151E
(27) CA.DMA.CYCLE- 90C 100B 110A 120A 130B 165B
(233) CA.BOOT.CYCLE+ 30A 90B
(498) CA.NO.HOLDS- 130B

CA2

CACHE CONTROLLER-A900 M2, PC & MADR		HEWLETT PACKARD
12203A		12203-80004
		D-12203-80004-52

CA2

A	AS ISSUED PC22-6791	ko	5-5-83
B	DELETED ONE GATE ON U707 TO MATCH BOARD	gd/bmc/ko	9-7-83

D-12203-60004-53

139A CA.FORCE.CODE+ (375)
139B CA.TRUE.BOOT+ (450)
29E CA.BOOT.CYCLE+ (80)
10A 60A 140A 155A BP.T.BUS+ 8

-1322 74S02 U0106: (89) → (180) CA.BOOT.2B- → 20A

M1MP
-2700 74F373 U0706: (122)(121)(120)(119)(118)(117)(116)(115) → (70)(69)(94)(93)(92)(91)(90)(38)
CA.MP.IN+ 6
5/ CA.MP.OUT+ → 40A 140A 163C
(70) CA.MP.IN7+ → 130B
(73) CA.RRR.CYCLE+ → 110A 140A 166B
(90) CA.BOOT.CYCLE+ → 140A 166B
(41) CA.AB.EN.CYCLE- → 110C 140A 166B

-1448 74S32 U0404: CA.FORCE.CODE+ (375), (38) → CA.MP.INPUT0+ (38)

-2701 74F374 U0707 MP: (70)(94)(93)(92)(91)(90) → (26)(25)(24)(23)(22)

89C CK.A.CAC1.M1MP+ (485)
119C 10E CA.M1.EN- (195)

MP HOLD
-2795 74F244 U0507: (73)(80)(41)(26)(25)(24)(23)(22) → (70)(69)(94)(93)(92)(91)(90)(38)
149D 20A 110A CA.NO.HOLDS+ (15)

LADR
-2700 74F374 U1006: (473)(472)(471)(470)(469)(482)(481) → (85)(84)(59)(83)(82)(58)(68)(67)
16/ CA.MADR.IN+ → 19C 20A

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

M2MP
-2700 74F373 U0506: (73)(80)(41)(26)(25)(24)(23)(22) → (70)(69)(94)(93)(92)(91)(90)(38)
129B 20C CK.A.CAC2.M2.LD+ (205)
119C 20C CA.M2.EN- (196)

+5V 422ohms 1% R1
-1367 74S08 U0604 U0605 U0606 U0608: (494)(113)(493)(113)(472)(113)(491)(113)(490)(113) → (426)(425)(424)(423)(422)
-1367 CA.MSKD.SC+

LCS
-2700 74F374 U0807: (428)(425)(424)(423)(422) → (70)(69)(94)(93)(92)(91)(90)(38)

-2700 74F374 U0808: (479)(478)(477)(476)(475)(474)(468)(467) → (66)(65)(63)(62)(61)(60)(57)(37)

MAP SELECT
7 6 5 4 3 2 1 0
A/B ADDRESSABLE (0=ENABLE)
BOOT MEMORY (1=ENABLE)
(PAGE 0 - RAM
(PAGES 8-11 - PROM
RRH MODE (1=ENABLE)

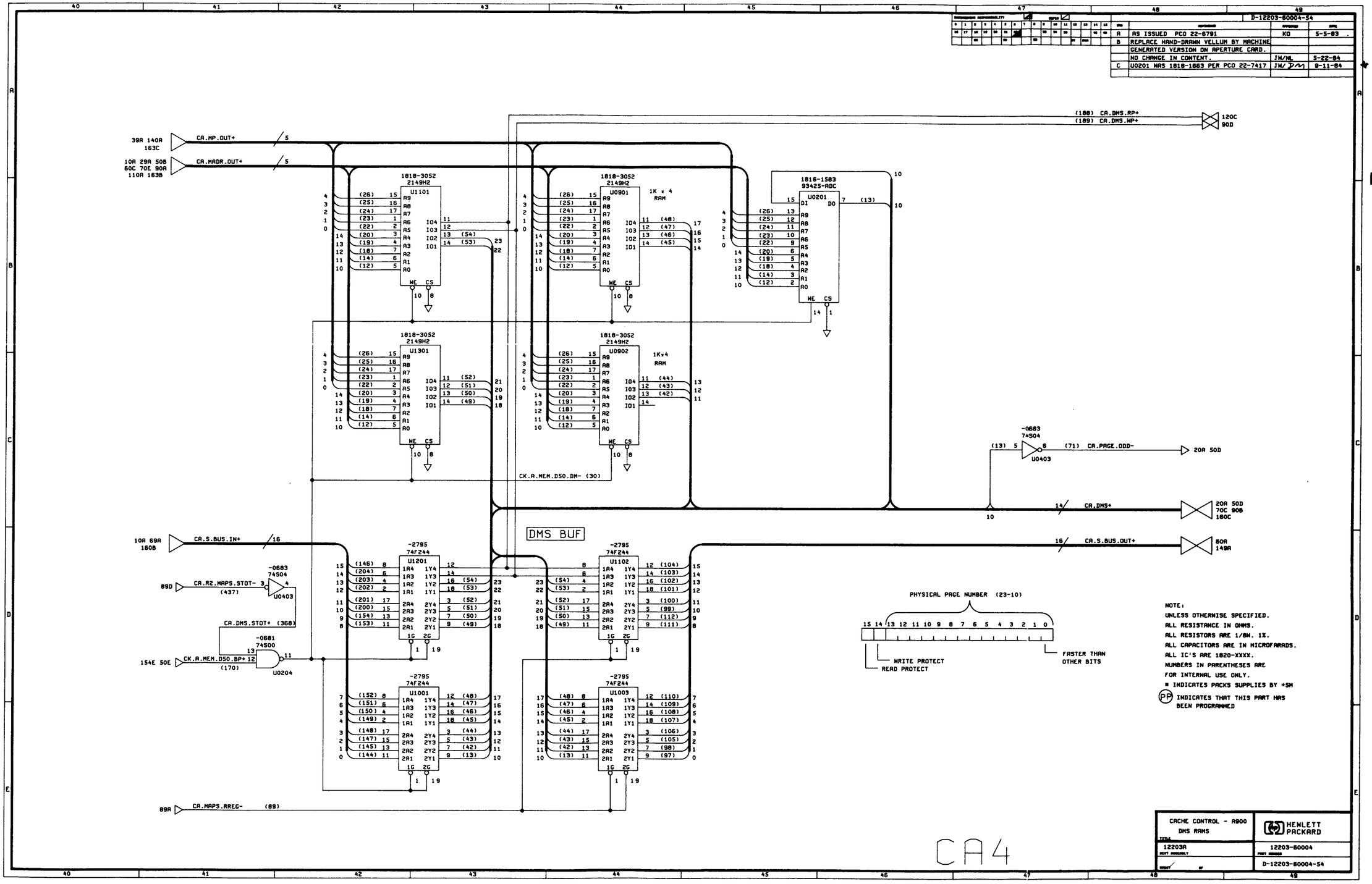
PCMP
-2700 74F373 U0807: (73)(80)(41)(26)(25)(24)(23)(22) → (70)(69)(94)(93)(92)(91)(90)(38)
129A 20E CK.A.CAC2.PC.LD+ (208)
119B 20E CA.PC.EN- (199)

20E 80B 80C 154E CK.A.CAC1.CA+ (35)
157B LBP.SC+ 5/
155B LBP.A8+ 15/
109A CA.IO.ADDR.LD+ (347)
119B CA.IO.EN- (194)
50D 100E 110A 120A 139C CA.PULLUP+ (21)

CA3

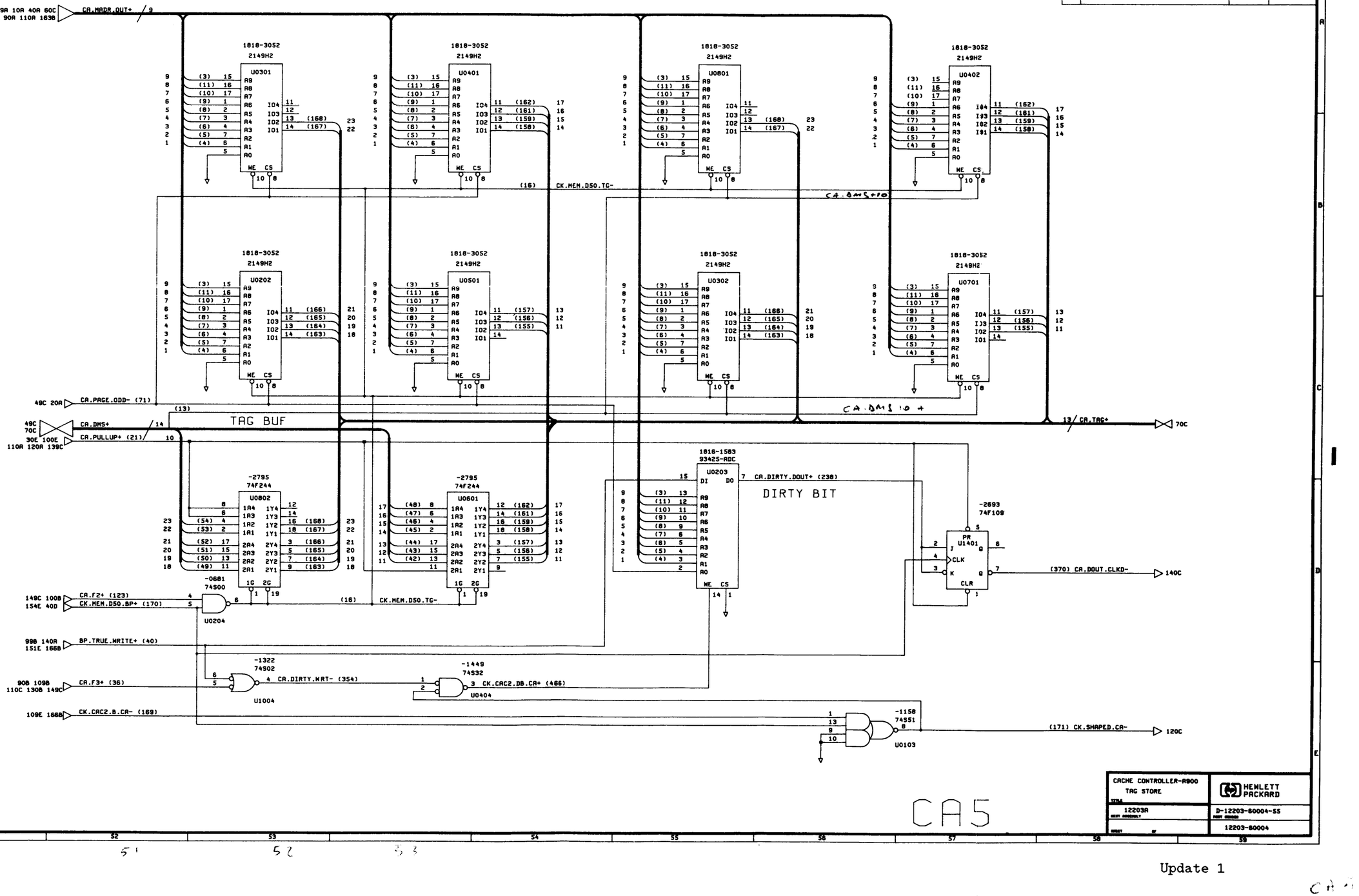
	CACHE CONTROL - A900 MAP SELECT & IO ADDRESS	HEWLETT PACKARD
	12203A	12203-60004
		D-12203-60004-53

CA3


D-12203-80004-54
A AS ISSUED PCO 22-6781 KO 5-5-83
B REPLACE HAND-DRAWN VELLUM BY MACHINE GENERATED VERSION ON APERTURE CARD. NO CHANGE IN CONTENT. JW/ML 5-22-84
C U0201 WAS 1818-1863 PER PCO 22-7417 JW/ 9-11-84
39A 140A 163C
10A 29A 50B 60C 70E 90A 110A 163B
CA.MP.OUT+ 5
CA.MADR.OUT+ 5
(188) CA.DMS.MP+
(189) CA.DMS.MP+
120C 90D
1818-3052 2149H2
U1101
U0901
U1301
U0902
1K x 4 RAM
1816-1583 93425-ADC
U0201
-0683 74S04
U0403
(71) CA.PAGE.ODD-
20A 50D
CK.A.MEM.DS0.DM- (30)
DMS BUF
-2795 74F244
U1201
U1102
U1001
U1003
CA.S.BUS.IN+ 16
CA.S.BUS.OUT+ 16
50A 149A
CA.R2.MAPS.STOT- (437)
CA.DMS.STOT+ (368)
-0681 74S00
U0204
CK.A.MEM.DS0.BP+ (170)
CA.MAPS.RREG- (89)
20A 50D
70C 90B 150C
CA.DMS+
PHYSICAL PAGE NUMBER (23-10)
WRITE PROTECT
READ PROTECT
FASTER THAN OTHER BITS
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
CACHE CONTROL - A900
DMS RAMS
HEWLETT PACKARD
12203A
12203-60004
D-12203-60004-54
CA4

CA4

		D-12203-80004-55	
A	AS ISSUED PC22-6791	maf/ko	5-5-83
B	REPLACE HAND-DRAWN VELLUM BY MACHINE GENERATED VERSION ON APERTURE CARD. NO CHANGE IN CONTENT.	JM/NL	5-15-84
C	U0203 WAS 1818-1663 PER PCO 22-7417	JM/DM	8-11-84



Update 1

		D-12203-60004-56	
		APPROVED	DATE
A	RS ISSUED PCO 22-6791	KO	5-5-83
B	PCO 22-6930;U0908,U1208 WERE 1818-1633 (2732)	GD/KO	8-3-83
C	PCO 22-7109; U0908 WAS 12203-80007; U1208 WAS 12203-80008.	GD/DM	1-5-84

NOTE:
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ALL RESISTORS ARE 1/8W. 1%.
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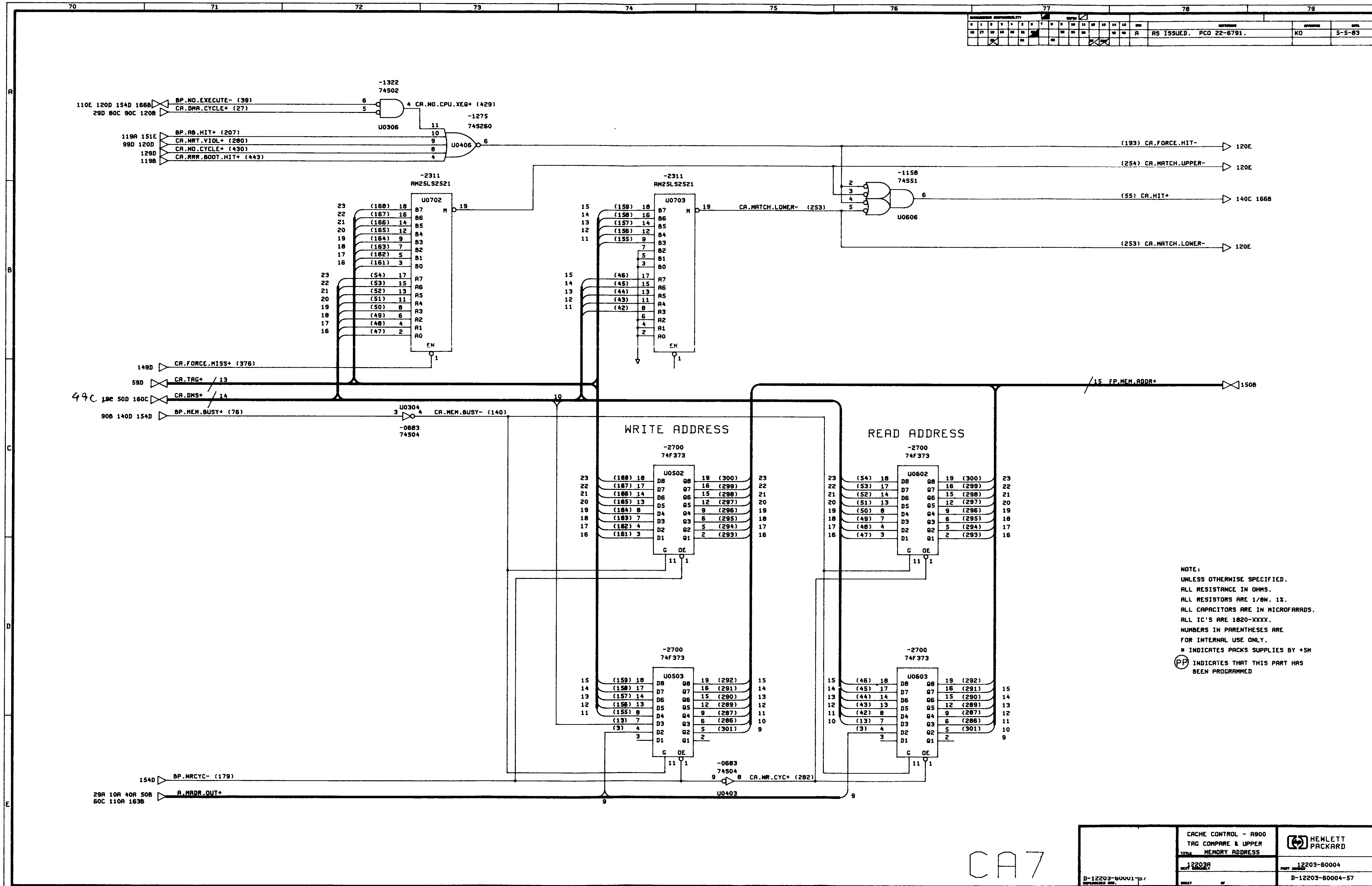
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

D-12203-60001-56	CACHE CONTROL - A900 MISC. RREG. S BUS, Q	HEWLETT PACKARD
	TITLE 12203A	12203-60004
	NEXT ASSEMBLY	PART NUMBER
	SHEET OF	D-12203-60004-56

CA6



NOTE:
UNLESS OTHERWISE SPECIFIED.
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ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
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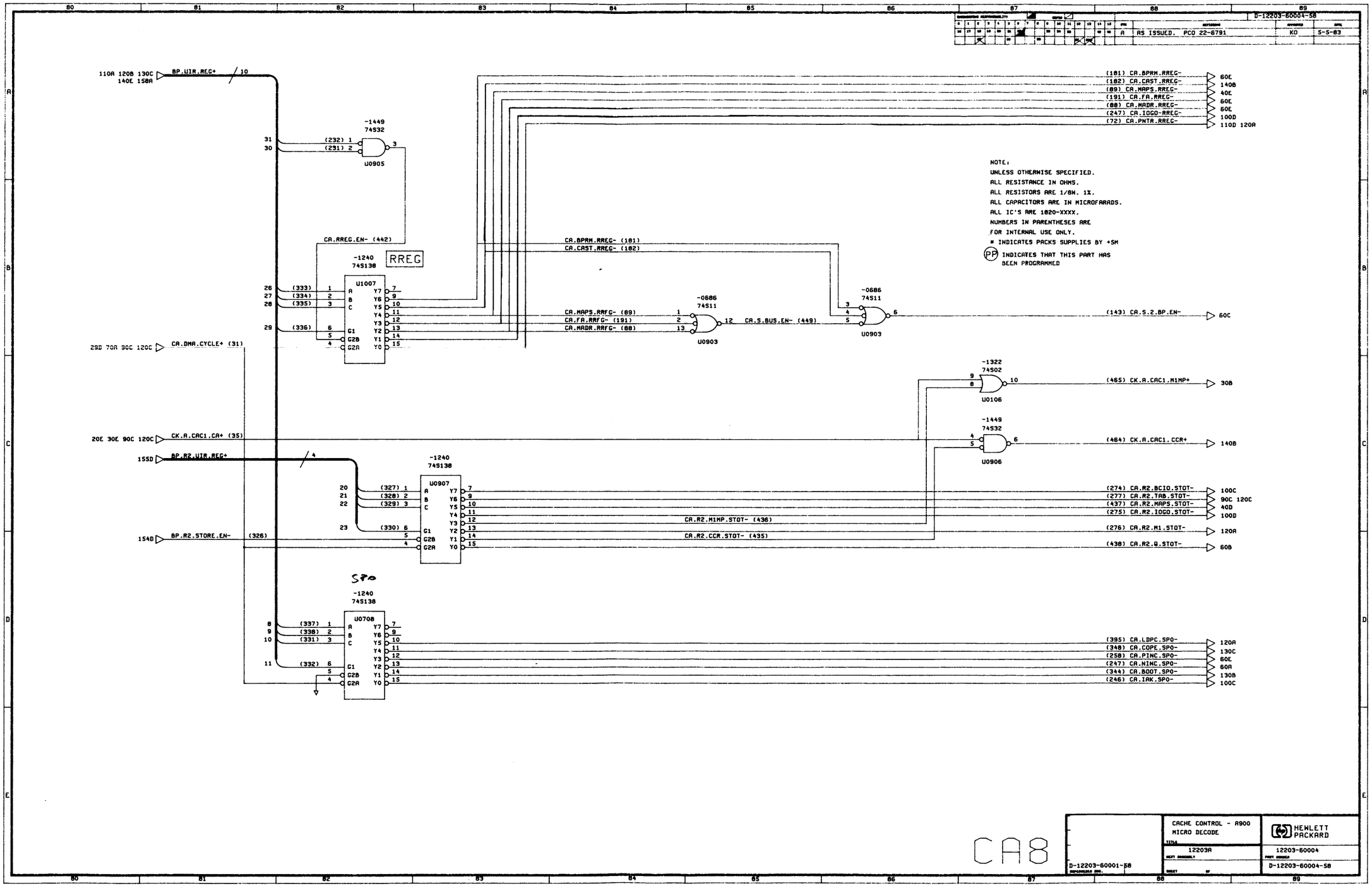
FOR INTERNAL USE ONLY.
■ INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS
BEEN PROGRAMMED

LTR	DESCRIPTION	APPROVED	DATE
A	AS ISSUED. PCO 22-6791.	KO	5-5-83

CACHE CONTROL - A900
TAG COMPARE & UPPER
MEMORY ADDRESS

HEWLETT PACKARD

NEXT ASSEMBLY: 12203A
PART NUMBER: 12203-60004
D-12203-60004-57
SUPERSEDES DWG. D-12203-60001-57


D-12203-60004-58
A RS ISSUED. PCO 22-6791 KO 5-5-83
110A 120B 130C 140E 158A BP.UIR.REG+ 10
-1449 74S32 U0905
(232) 1
(231) 2
3
31
30
CA.RREG.EN- (442)
-1240 74S138 RREG U1007
26 (333) 1 A
27 (334) 2 B
28 (335) 3 C
29 (336) 6 G1
5 G2B
4 G2A
Y7 7
Y6 9
Y5 10
Y4 11
Y3 12
Y2 13
Y1 14
Y0 15
CA.BPRM.RREG- (181)
CA.CAST.RREG- (182)
CA.MAPS.RRFG- (89)
CA.FA.RRFG- (191)
CA.MADR.RRFG- (88)
-0686 74S11 U0903
CA.S.BUS.EN- (448)
(181) CA.BPRM.RREG- 60E
(182) CA.CAST.RREG- 140B
(89) CA.MAPS.RREG- 40E
(191) CA.FA.RREG- 60E
(88) CA.MADR.RREG- 60E
(247) CA.IOGO-RREG- 100D
(72) CA.PNTR.RREG- 110D 120A
NOTE:
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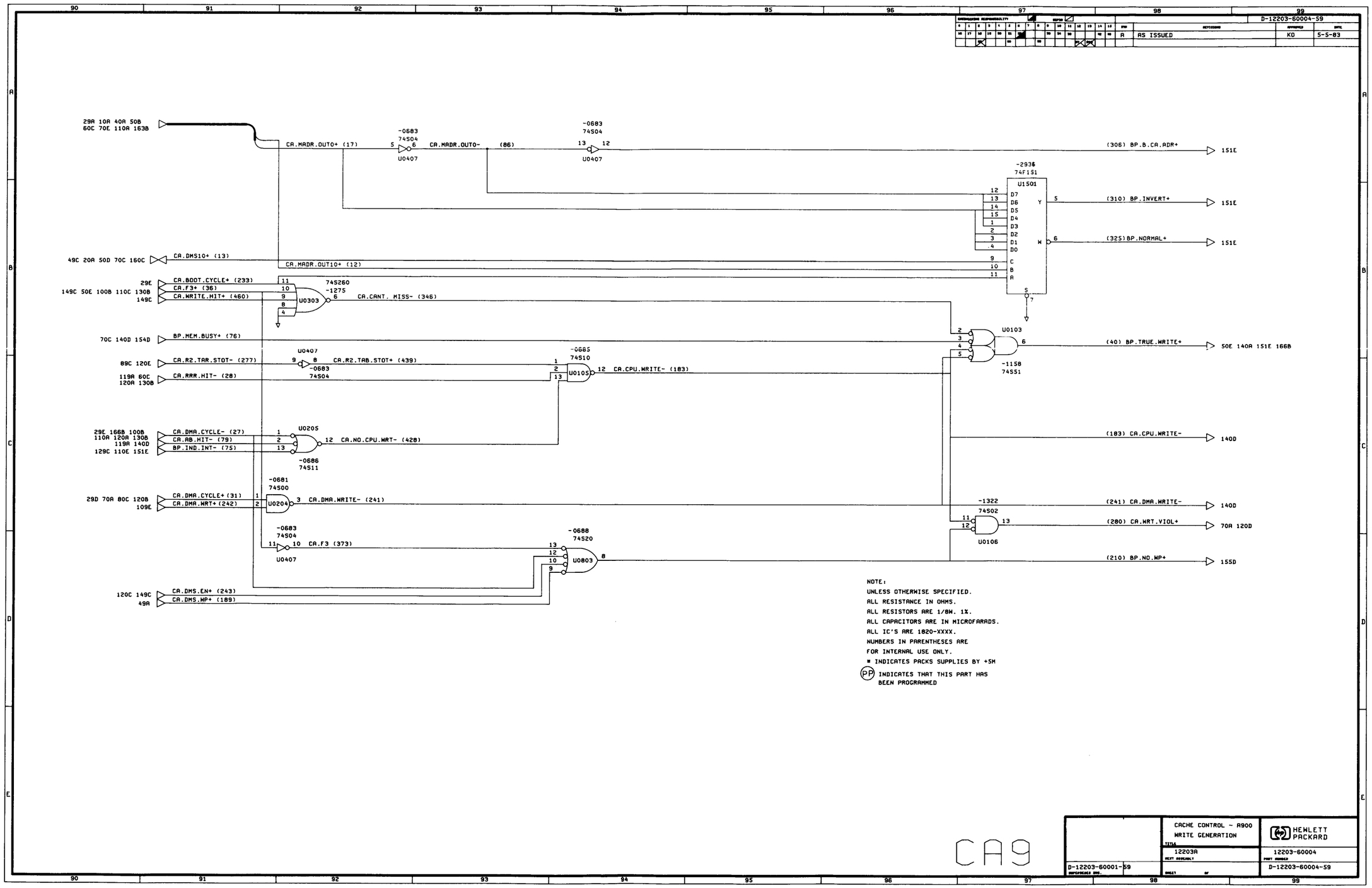
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED
(143) CA.S.2.BP.EN- 60C
29D 70A 90C 120C CA.DMA.CYCLE+ (31)
-1322 74S02 U0106
(465) CK.A.CAC1.M1MP+ 30B
20E 30E 90C 120C CK.A.CAC1.CA+ (35)
-1449 74S32 U0906
(464) CK.A.CAC1.CCR+ 140B
155D BP.R2.UIR.REG+ 4
-1240 74S138 U0907
20 (327) 1 A
21 (328) 2 B
22 (329) 3 C
23 (330) 6 G1
5 G2B
4 G2A
CA.R2.M1MP.STOT- (436)
CA.R2.CCR.STOT- (435)
(274) CA.R2.BCIO.STOT- 100C
(277) CA.R2.TAB.STOT- 90C 120C
(437) CA.R2.MAPS.STOT- 40D
(275) CA.R2.IOGO.STOT- 100D
(276) CA.R2.M1.STOT- 120A
(438) CA.R2.Q.STOT- 60B
154D BP.R2.STORE.EN- (326)
S70
-1240 74S138 U0708
8 (337) 1 A
9 (338) 2 B
10 (331) 3 C
11 (332) 6 G1
5 G2B
4 G2A
(395) CA.LDPC.SPO- 120A
(348) CA.COPE.SPO- 130C
(258) CA.PINC.SPO- 60E
(247) CA.NINC.SPO- 60A
(344) CA.BOOT.SPO- 130B
(246) CA.IAK.SPO- 100C
CA8
D-12203-60001-58
CACHE CONTROL - A900 MICRO DECODE
12203A
HEWLETT PACKARD
12203-60004
D-12203-60004-58

CA8



NOTE:
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ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

	CACHE CONTROL - A900 WRITE GENERATION	HEWLETT PACKARD
	12203A	12203-60004
D-12203-60001-59		D-12203-60004-59

D-12203-60004-59			
A	AS ISSUED	KO	5-5-83

CA9

CA9

REVISIONS			
REV	REVISIONS	APPROVED	DATE
A	RS ISSUED. PCO 22-6791.	KO	5-5-83
B	U1608 WAS -3051 IN ERROR	GD/KO	6-8-83

D-12203-60004-60

154E (488) LBP.REMEM- 1 — U0407 -0683 74S04 — 2 CA.REMEM+ (440)

(302) LBP.MEMGO- 12

CA.SHC+ 3

-1275 74S260 U0406

CA.DMA.EARLY+ (187)

-1449 74S32 U0905

(240) CA.DMA.REQ+ → 110C 130B

(347) CA.IO.ADDR.LD+ → 30E

CA.BUSY+ (345)

CA.DISABLE+ (355)

CA.DMA.PD+ (239)

CA.DMA+ (362)

CA.VALID- (457)

(446) 74S32 -1449 U0906

-1449 74S32 U0906

(311) BP.LDOUT.EN- → 151E

-3023 825153 U1005

-0683 74S04 U0407

(74) LBP.BUSY- → 30E 151D

(392) CA.LDOUT.BOTH-

(305) LBP.VALID- → 151D

(363) CA.DMA.2B

(366) CA.DMA.PD.2B+

(378) CA.HOLD.WRT-

29E 90C 110A 120A 130B 166B CA.DMA.CYCLE- (27)

149C CA.F1+ (190)

149C CA.F2+ (123)

149C 50E 90B 100C 130B CA.F3+ (373)

CPL01 (HP-N/A)

-2701 74F374 U1105

129E CA.RRR.CNT.2B+ (445) → (278) CA.RRR.CNT- → 110A 120E

(142)

154E LBP.MEMGO- (302)

154E LBP.MRQ- (303)

CA.SHC+ (142)

CA.DMA.WRT+ (242)

CA.LDOUT.EN+ (393)

CA.VAL.BUSY+ (458)

-3050 825153 U1308

(386) CA.IO.FREEZE- → 140C

149C CA.CRS+ (237)

89E CA.IAK.SPO- (246)

89C CA.R2.BCIO.STOT- (274)

89C CA.R2.IOGO.STOT- (275)

89B CA.IOGO.RREG- (247)

(74) LBP.BUSY-

(356) CA.DISABLE.2B+

(389) CA.IO.S2.2B+

(388) CA.IO.S1.2B+

(387) CA.IO.S0.2B+

(459) CA.VAL.BUSY.2B+

(386) CA.IO.FREEZE-

CPL02 (HP-N/A)

-2701 74F374 U1408

(250) (249) (248) → (483) LBP.CPUTURN- → 151D; (489) LBP.RNI- → 151D; (484) LBP.CRS- → 151D

-3271 825153 U1608

(394) CA.LDOUT.EN.2B+

(349) CA.CPUTURN.2B-

(441) CA.RNI.2B-

(391) CA.LBP.CRS.2B-

(485) LBP.IAK-

(486) LBP.IOGO-

(483) LBP.CPUTURN-

(485) LBP.IAK- → 151D

(486) LBP.IOGO- → 151D

(242) CA.DMA.WRT+ → 90D

(169)CK.CAC2.B.CA- → 50E 166B

CPL03

CA.IO.S+

CA.PULLUP+ (21)

-2693 74F109 U0405

154E LBP.SCLK- (304)

120E 140D 154E CK.CAC2.CA+ (29) — U0403 74S04 -0683 — CK.CAC2.B.CA- (169)

CA.SHC.2B+ (446)

CK.CAC2.CA+ (29)

154E LBP.WE- (495)

U0906 -1449 74S32 — CA.GATED.LBP.WE- (244)

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(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

CA10

D-12203-60001-60	CACHE CONTROL - A900 I/O STATE MACHINE	HEWLETT PACKARD
	12203A	12203-60004
		D-12203-60004-60

CA10

REVISIONS			
REV	DESCRIPTION	APPROVED	DATE
A	AS ISSUED. PCO 22-8791.	KO	5-5-83
B	U0305WAS -3052 IN ERROR	GD/KO	6-6-83

D-12203-60004-61

29D CA.BOOT.CYCLE- (234)
149C CA.ALWAYS.HIT- (343)
129B CA.DELAY.MEM+ /3
29E 166B 90C 100B 120A 130B CA.DMA.CYCLE- (27)
120B 130C 140E 158A BP.UIR.REG+ /3
149D 20A 30C CA.NO.HOLDS+ (15)
109B 120E CA.RRR.CNT- (278)
139C 30E 50D 100E 110A 120A CA.PULLUP+ (21)
39A 140A 166B CA.RRR.CYCLE+ (73)
29A 10A 40A 50B 60C 70E 90A 163B CA.MADR.OUT+ /14

U0206 -0686 74S11 — CA.RRR.HIT.OK+ (279)

-0685 74S10 U0104 — (198)
-0686 74S11 U0205

-1275 74S260 U0102 — CA.PAGE.ZERO+
-1275 74S260 U0102 — CA.MID.ZERO+ (420)
-1275 74S260 U1607 — CA.LOW.ZERO+ (398)

39B 140A 166B CA.AB.EN.CYCLE- (41)

149C 50E 90B 100B 130B CA.F3+ (36)
109A 130B CA.DMA.REQ+ (240)
89B 120A CA.PNTR.RREG- (72)

-0683 74S04 U0304

-3272 82S153 U0305 — CPL04 (HP-N/A) — 5-17

-0683 74S04 U0304

U0206 -0686 74S11 — CA.RRR.BOOT.HIT-

(444) U0106 -1322 74S02

-0685 74S10 U0104 — CA.MRG.ACCESS- (257), CA.PNTR.IND- (141)

-0685 74S10 U0104 — CA.MI.SEL+

-0681 74S00 U0204

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ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
# INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

60A 159B BP.S.BUS+ /5

-0681 74S00 U1601 — CA.S.BUS.ALLOW+ — (114)

-1275 74S260 U1607 — (178), (177), (176) — CA.MRG- (197)

-1449 74S32 U0404 — CA.JTAB.SEL~

129B 166C CA. JTAB.CREATE- (251)

U0905 -1449 74S32

-1322 74S02 U1004 — (175) — (81) CA.FORCE.PAGE0+

-0688 74S20 U0307 — CA.PUTR.RREG+ (434)

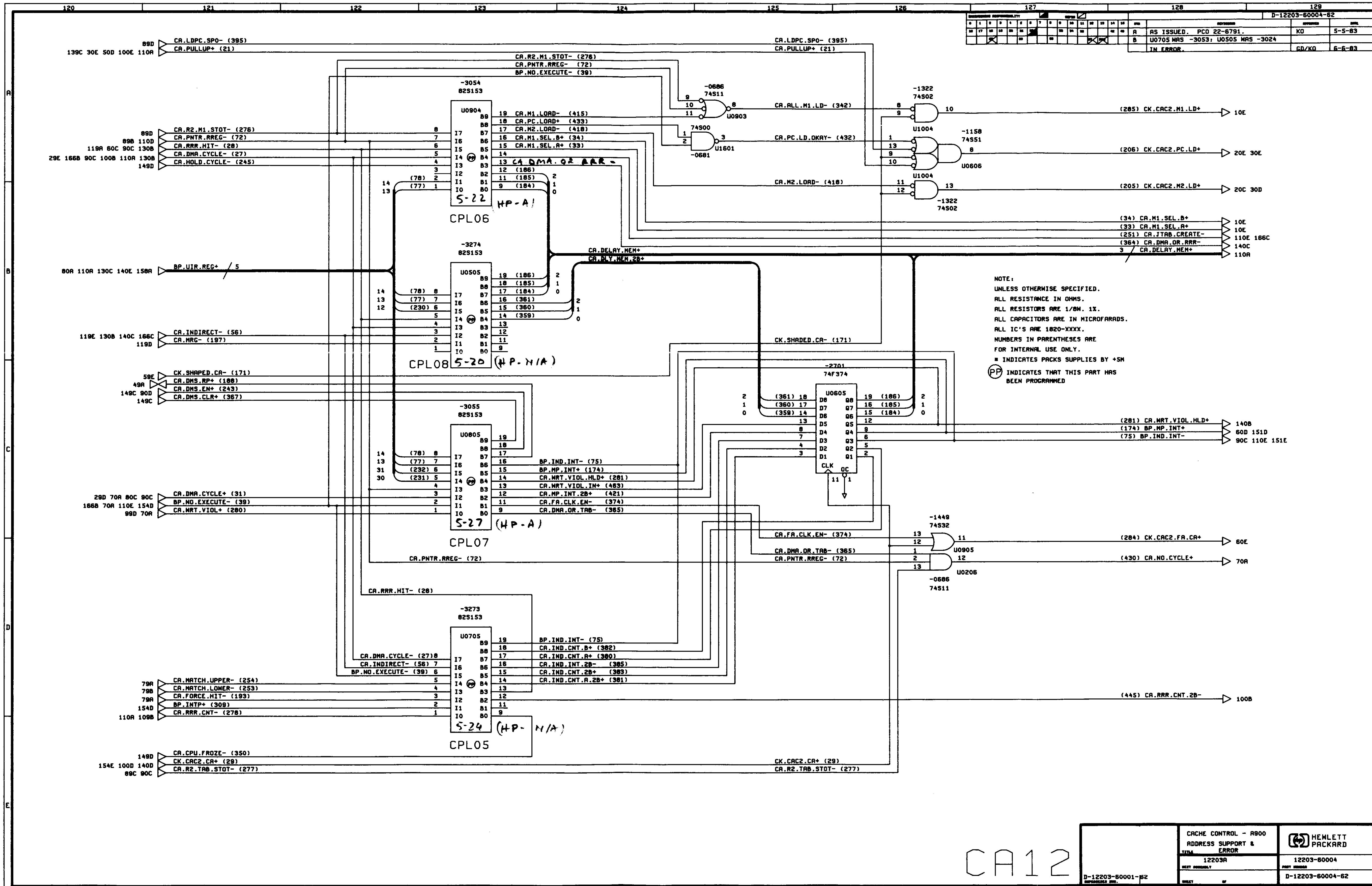
70A 120D 154D 166B BP.NO.EXECUTE- (39)
129C 90C 151E BP.IND.INT- (75)

(28) CA.RRR.HIT- 60C 90C 120A 130B
(95) CA.RRR.HIT+ 60C 166B
(79) CA.AB.HIT- 90C 140D
(207) BP.AB.HIT+ 70A 151E
(443) CA.RRR.BOOT.HIT+ 70A
(452) CA.TRUE.DMA.REQ+ 20E
(194) CA.IO.EN- 30E
(199) CA.PC.EN- 20E 30E
(196) CA.MZ.EN- 20C 30D
(195) CA.MI.EN- 10E 30D
(197) CA.MRG- 120B
(252) CA.JTAB.MRG- 30A
(56) CA.INDIRECT- 120B 130B 140C 166C

505-3 803-4
105-7 1002-17
804-8
207-7

CA11

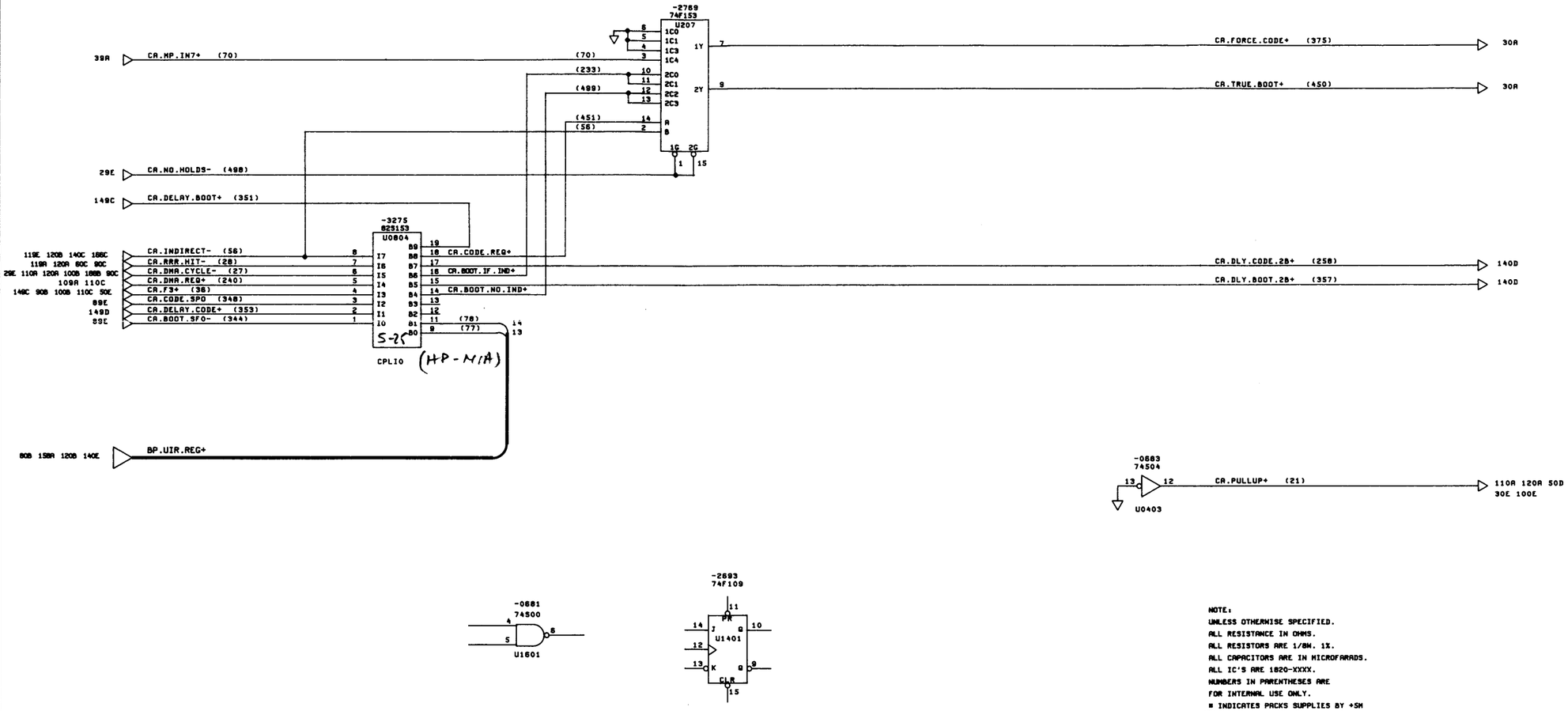
	CACHE CONTROL - A900 ADDRESS SELECT AB	HEWLETT PACKARD
D=12203-60001-61	12203A	12203-60004
		D-12203-60004-61



D-12203-60004-62
A AS ISSUED. PCO 22-6791. KO 5-5-83
B U0705 WAS -3053; U0505 WAS -3024 IN ERROR. GD/KO 6-6-83
89D CA.LDPC.SPO- (395)
139C 30E 50D 100E 110A CA.PULLUP+ (21)
CA.R2.M1.STOT- (276)
CA.PNTR.RREG- (72)
BP.NO.EXECUTE- (39)
89D CA.R2.M1.STOT- (276)
89B 110D CA.PNTR.RREG- (72)
119A 60C 90C 130B CA.RRR.HIT- (28)
29E 166B 90C 100B 110A 130B CA.DMA.CYCLE- (27)
149D CA.HOLD.CYCLE- (245)
-3054 82S153 U0904
CA.M1.LOAD- (415)
CA.PC.LOAD+ (433)
CA.M2.LOAD- (418)
CA.M1.SEL.B+ (34)
CA.M1.SEL.A+ (33)
CA DMA.OR RRR-
5-22 (HP-A)
CPL06
-0686 74S11 U0903
74S00 -0681 U1601
CA.ALL.M1.LD- (342)
CA.PC.LD.OKAY- (432)
CA.M2.LOAD- (418)
-1322 74S02 U1004
-1158 74S51 U0606
(285) CK.CAC2.M1.LD+ 10E
(206) CK.CAC2.PC.LD+ 20E 30E
(205) CK.CAC2.M2.LD+ 20C 30D
(34) CA.M1.SEL.B+ 10E
(33) CA.M1.SEL.A+ 10E
(251) CA.JTAB.CREATE- 110E 166C
(364) CA.DMA.OR.RRR- 140C
3 CA.DELAY.MEM+ 110A
80A 110A 130C 140E 158A BP.UIR.REG+ 5
CA.DELAY.MEM+
CA.DLY.MEM.2B+
-3274 82S153 U0505
5-20 (HP-N/A)
CPL08
119E 130B 140C 166C CA.INDIRECT- (56)
119D CA.MRG- (197)
CK.SHADED.CA- (171)
59E CK.SHAPED.CA- (171)
49A CA.DMS.RP+ (188)
149C 90D CA.DMS.EN+ (243)
149C CA.DMS.CLR+ (367)
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIES BY +5M
PP INDICATES THAT THIS PART HAS BEEN PROGRAMMED
-2701 74F374 U0605
(281) CA.WRT.VIOL.HLD+ 140B
(174) BP.MP.INT+ 60D 151D
(75) BP.IND.INT- 90C 110E 151E
-3055 82S153 U0805
BP.IND.INT- (75)
BP.MP.INT+ (174)
CA.WRT.VIOL.HLD+ (281)
CA.WRT.VIOL.IN+ (463)
CA.MP.INT.2B+ (421)
CA.FA.CLK.EN- (374)
CA.DMA.OR.TAB- (365)
29D 70A 80C 90C CA.DMA.CYCLE+ (31)
166B 70A 110E 154D BP.NO.EXECUTE- (39)
99D 70A CA.WRT.VIOL+ (280)
5-27 (HP-A)
CPL07
CA.PNTR.RREG- (72)
CA.FA.CLK.EN- (374)
CA.DMA.OR.TAB- (365)
CA.PNTR.RREG- (72)
-1449 74S32 U0905
(284) CK.CAC2.FA.CA+ 60E
U0206 -0686 74S11
(430) CA.NO.CYCLE+ 70A
CA.RRR.HIT- (28)
-3273 82S153 U0705
CA.DMA.CYCLE- (27)
CA.INDIRECT- (56)
BP.NO.EXECUTE- (39)
BP.IND.INT- (75)
CA.IND.CNT.B+ (382)
CA.IND.CNT.A+ (380)
CA.IND.INT.2B- (385)
CA.IND.CNT.2B+ (383)
CA.IND.CNT.A.2B+ (381)
79A CA.MATCH.UPPER- (254)
79B CA.MATCH.LOWER- (253)
79A CA.FORCE.HIT- (193)
154D BP.INTP+ (309)
110A 109B CA.RRR.CNT- (278)
(445) CA.RRR.CNT.2B- 100B
5-24 (HP-N/A)
CPL05
149D CA.CPU.FROZE- (350)
154E 100D 140D CK.CAC2.CA+ (29)
89C 90C CA.R2.TAB.STOT- (277)
CK.CAC2.CA+ (29)
CA.R2.TAB.STOT- (277)
CA12
D-12203-60001-62
CACHE CONTROL - A900 ADDRESS SUPPORT & ERROR
12203A
HEWLETT PACKARD
12203-60004
D-12203-60004-62

CA12

REVISIONS			
		D-12203-60004-63	
REV	DESCRIPTION	APPROVED	DATE
A	AS ISSUED PC022-8791	ko	5-5-83
B	UBD4 WAS -3057 IN ERROR	gd/ko	6-6-83



NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.
= INDICATES PACKS SUPPLIES BY +5M
(PP) INDICATES THAT THIS PART HAS BEEN PROGRAMMED

CA13

D-12203-60001-63	CACHE CONTROL-A900 SPO DELAY	HEWLETT PACKARD
	SIZE	12203-60004
	NEXT ASSEMBLY	PART NUMBER
	SHEET OF	D-12203-60004-63

CA13

D-12203-60004-64

REVISIONS																ZONE	DESCRIPTION	APPROVED	DATE
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	A	AS ISSUED	ko	5-5-83
16	17	18	19	20	21	22		23		24		25		26					

39A 40A 163C — CA.MP.OUT+ /5

39A 110A 166B — CA.RRR.CYCLE+ (73)

39B 166B — CA.BOOT.CYCLE+ (80)

39B 110C 166B — CA.AB.EN.CYCLE- (41)

129C — CA.WRT.VIOL.HLD+ (281)

99B 50E 151E 166B — BP.TRUE.WRITE+ (40)

29D — CA.BOOT.CYCLE- (234)

10A 30A 60A 155A — BP.T.BUS+ /8

CCR

-1730 74LS273 U0806

(122) 18 D7 Q7 19 — CA.CRS+ 16

(121) 17 D6 Q6 — CA.BPRM.ON- 15

(120) 14 D5 Q5 — CA.DMS.EN+ 12 (497)

(119) 13 D4 Q4 — CA.DMS.CLR+ 9

(118) 8 D3 Q3 — CA.ALWAYS.HIT- 6

(117) 7 D2 Q2 — CA.PONT.FRZ- 5 (369)

(116) 4 D1 Q1 — CA.MODE.LOAD+ 2

(115) 3 D0 Q0

CLR 11 1

89C — CK.A.CAC1.CCR+ (484)

154E — LBP.PON+ (487)

89D — CA.CAST.RREG- (182)

-1387 74S08 U0604

CA.WRT.VIOL.HLD+ 18

CA.INDIRECT- 17

BP.TRUE.WRITE+ 14

CA.HIT+ 13

BP.MEM.BUSY+ 8

CA.CPU.FRZ+ 7

BP.MEM.RD.REQ+ 4

BP.MEM.WR.REQ+3

-2701 74F374 U1002

D8 Q8 19 (104) 15

D7 Q7 16 (103) 14

D6 Q6 15 (102) 13

D5 Q5 12 (101) 12

D4 Q4 9 (100) 11

D3 Q3 6 (99) 10

D2 Q2 5 (112) 9

D1 Q1 2 (111) 8

CLK OE 11 1

CAST

-2701 74F374 U1103

18 D8 Q8 19 (110) 7

17 D7 Q7 16 (109) 6

14 D6 Q6 15 (108) 5

(26) 13 D5 Q5 12 (107) 4

(25) 8 D4 Q4 9 (106) 3

(24) 7 D3 Q3 6 (105) 2

(23) 4 D2 Q2 5 (98) 1

(22) 3 D1 Q1 2 (97) 0

CLK OE 11 1

16 CA.S.BUS.OUT+ — 49D 60A

59D — CA.DOUT.CLKD- (370)

79A 168B — CA.HIT+ (55)

154D 70C 90B — BP.MEM.BUSY+ (76)

-1275 74S260 U0303

-1322 74S02 U0306

(237) CA.CRS+ — 100C

(235) CA.BPRM.ON- — 60E

(243) CA.DMS.EN+ — 90D 120C

(367) CA.DMS.CLR+ — 120C

(343) CA.ALWAYS.HIT- — 110A

(209) BP.MEM.WR.REQ+ — 151D

(173) BP.MEM.RD.REQ+ — 151D

109C — CA.IO.FREEZE- (386)

119E 120B 130B 166C — CS.INDIRECT- (56)

129B — CA.DMA.OR.RRR- (364)

-0688 74S20 U0803

CA.CPU.FRZ+ (236)

(190) CA.F1+ — (190) CA.F1+ — 100B

(123) CA.F2+ — (123) CA.F2+ — 50E 100B

(36) CA.F3+ — (36) CA.F3+ — 50E 90B 100B 110C 130B

-2701 74F374 U0704

-1367 74S08 U0604

(461) CA.WRT.HIT.2B+

(462) CA.WRT.HOLD+

(460) CA.WRITE.HIT+ — 90B

(245) CA.HOLD.CYCLE- — 120A

(353) CA.DELAY.CODE+ — 130B

(351) CA.DELAY.BOOT+ — 130B

(350) CA.CPU.FROZE- — 120E

139B — CA.DLY.BOOT.2B+ (357)

139B — CA.DLY.CODE.2B+ (358)

154E 100E 120E — CK.A.CAC2.CA+ (29)

-3056 82S153 U0504

BP.CPU.FREEZE- (172)

99C — CA.CPU.WRITE- (183)

99C — CA.DMA.WRITE- (241)

119A 90C — CA.AB.HIT- (79)

(377) CA.HOLD-

-1367 74S08 U0604

(15) CA.NO.HOLDS+ — 20A 30C 110A

(376) CA.FORCE.MISS+ — 70B

-0681 74S00 U1601

(172) BP.CPU.FREEZE- — 151 166B

CPL09

5-16

(HP-MIA)

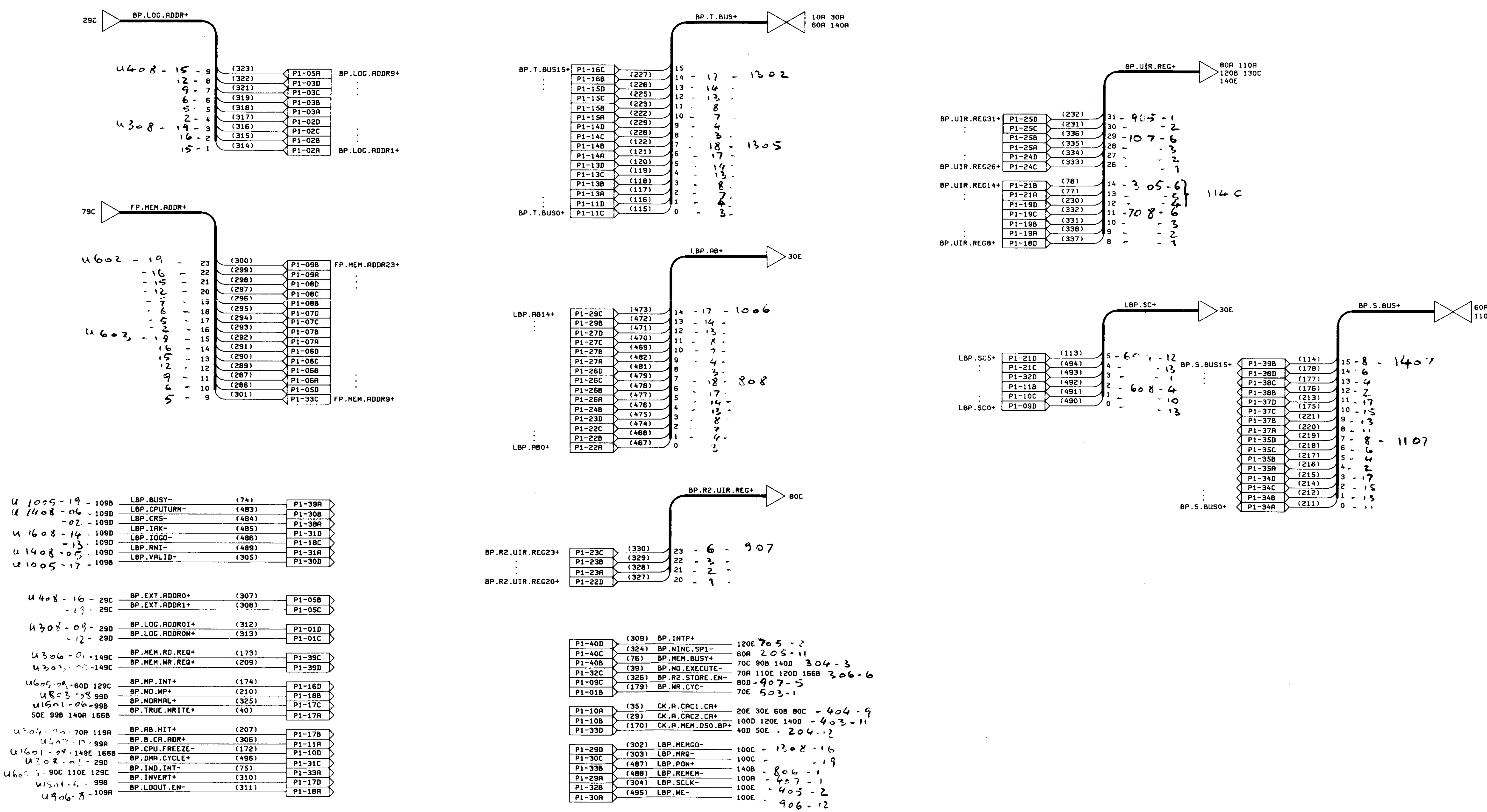
CA.HOLD.CYCLE- (245)

110A 120B 130C 158A — BP.UIR.REG+ /2

CA14

	CACHE CONTROL - A900 CONTROL REG. & FREEZE LOGIC	HEWLETT PACKARD
	12203A	12203-60004
		D-12203-60004-64

CA 14



A	AS ISSUED per PC22-6791	ko 5-5-83

CA15

CACHE CONTROL-A900
BACKPLANE

12203A

HEWLETT PACKARD

12203-60004

D-12203-60004-65

	D-12203-60004-66		
A	AS ISSUED PCO-22-6791	K.0	5-5-83

69A 10A 40D — CA.S.BUS.IN +

1407 - 12 - 15	(146)	J2-11A
14 - 14	(204)	J2-11B
16 - 13	(203)	J2-11C
18 - 12	(202)	J2-12A
3 - 11	(201)	J2-12C
5 - 10	(200)	J2-13A
7 - 9	(154)	J2-13B
9 - 8	(153)	J2-13C
1107 - 12 - 7	(152)	J2-14B
14 - 6	(151)	J2-14C
16 - 5	(150)	J2-15A
18 - 4	(149)	J2-15B
3 - 3	(148)	J2-16A
5 - 2	(147)	J2-16B
7 - 1	(145)	J2-16C
9 - 0	(144)	J2-17A

29A 90A 70E 110A — CA.MADR.OUT +

1104 - 16 - 14	(20)	J2-08C
15 - 13	(18)	J2-09B
12 - 12	(19)	J2-09C
9 - 11	(14)	J2-10A
6 - 10	(12)	J2-10B
5 - 9	(3)	J2-26C
2 - 8	(11)	J2-27A
107 - 19 - 7	(10)	J2-27C
16 - 6	(9)	J2-28A
15 - 5	(8)	J2-28B
12 - 4	(7)	J2-28C
9 - 3	(6)	J2-29B
6 - 2	(5)	J2-29C
5 - 1	(4)	J2-30A
2 - 0	(17)	J2-30B

103 - 1 - 50E 109E	CK.A.CAC2.B.CA -	(169)	J2-31A J2-31C
1601 - 8	BP.CPU.FREEZE -	(172)	J2-20B
306 - 6 70A 110E 120D 154D	BP.NO.EXECUTE -	(39)	J2-18C
1004 - 6 50E 99B 140A 151E	BP.TRUE.WRITE +	(40)	J2-18A
1405 - 1 50C 119A	CA.RRR.HIT +	(95)	J2-19B
606 - 6 79A 140C	CA.HIT +	(55)	J2-20A
707 - 19 - 39A 110A 140A	CA.RRR.CYCLE +	(73)	J2-05B
- 15 39B 110C 140A	CA.RB.EN.CYCLE -	(41)	J2-06B
304 - 10 29E 90C 100B 110A 120A 130B	CA.DMA.CYCLE -	(27)	J2-17C
905 - 9 110E 129B	CA.JTAB.CREATE -	(251)	J2-18B
304 - 12 - 29E 39B 140A	CA.BOOT.CYCLE +	(80)	J2-06A
307 - 8 119E 120B 130B 140C	CA.INDIRECT -	(56)	J2-19C

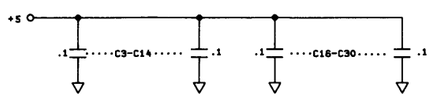
50 19D

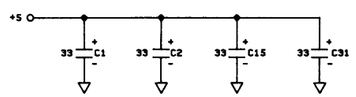
49D 50D 70C 90A — CA.DMS +

1201 - 16 - 23	(54)	J2-21A
18 - 22	(53)	J2-21B
3 - 21	(52)	J2-21C
5 - 20	(51)	J2-22A
7 - 19	(50)	J2-22C
9 - 18	(49)	J2-23A
1001 - 12 - 17	(48)	J2-23B
14 - 16	(47)	J2-23C
16 - 15	(46)	J2-24B
18 - 14	(45)	J2-24C
3 - 13	(44)	J2-25A
5 - 12	(43)	J2-25B
7 - 11	(42)	J2-26A
9 - 10	(13)	J2-26B

39A 40A 140A — CA.MP.OUT +

707 - 12 - 4	(26)	J2-06C
9 - 3	(25)	J2-07A
6 - 2	(24)	J2-07C
5 - 1	(23)	J2-08A
2 - 0	(22)	J2-08B



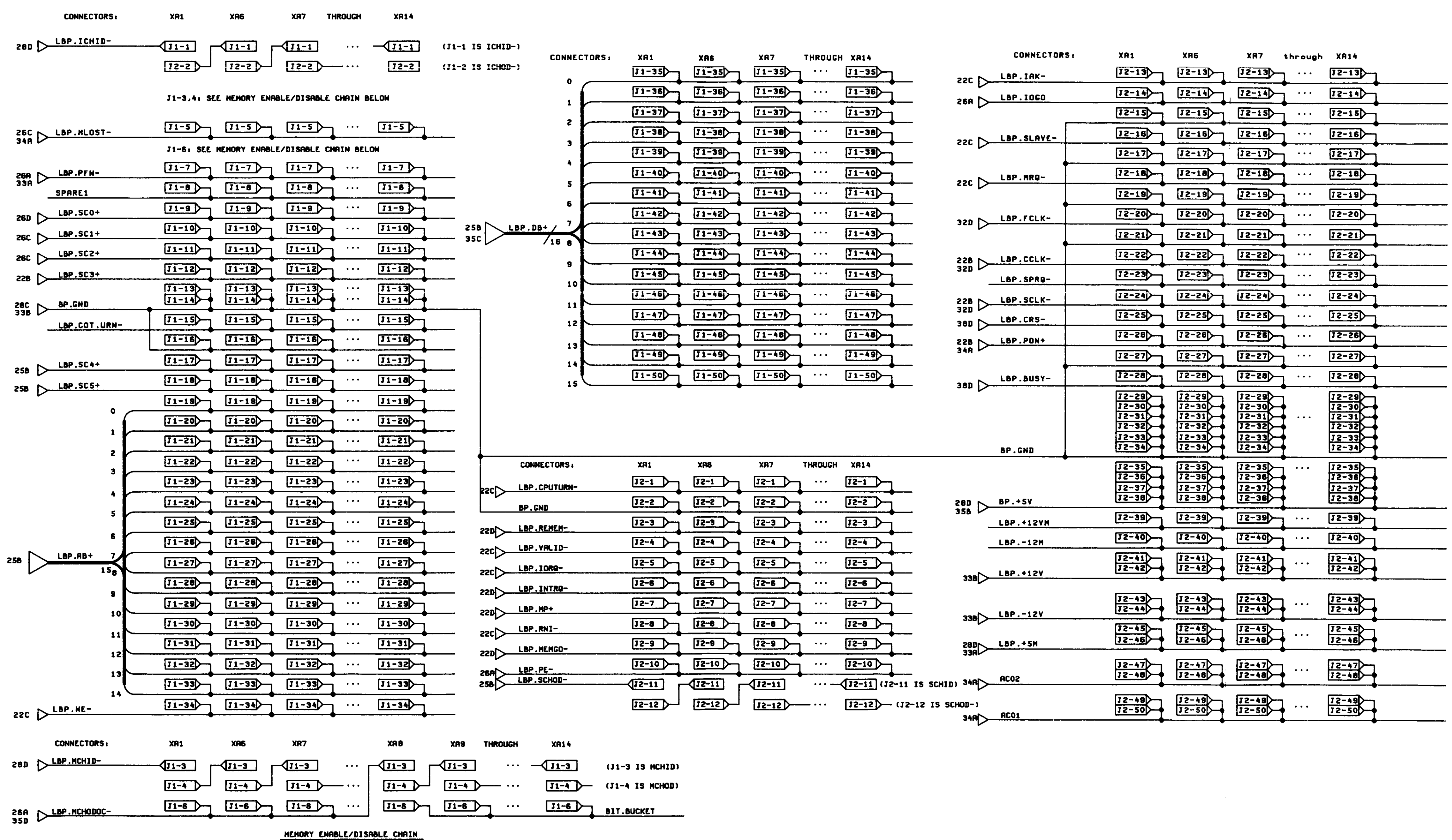


CA 16

	CACHE CNTRL - A900 FRONT PLANE	HEWLETT PACKARD
	12203 A	
D-12203-60001-66		D-12203-60004-66

D- 02430-60004-51

REV	DESCRIPTION	APPROVED	DATE
A	AS ISSUED	JT/cc	8/24/83



MICRO / 1000
A900 BACKPLANE

02430-60003

HEWLETT PACKARD

02430-60004

D- 02430-60004-51

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HP 1000 Computers

HP 1000 A900 Computer
Engineering and Reference Documentation

02139-90003 April, 1986

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