HEWLETT hp PACKARD

OPERATING AND SERVICE MANUAL

12565A

DISC INTERFACE KIT

(FOR 2100, 2114, 2115, AND 2116 COMPUTERS)

Card Assemblies
12565-60001, Rev 1030
12565-60002, Rev 1030

12565-90003

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This operating and service manual covers general information, installation, programming, theory of operation, maintenance, and replaceable parts for the HP 12565A Disc Interface Kit. (See figure 1-1).

1-3. GENERAL DESCRIPTION.

1-4. The HP 12565A Disc Interface Kit interfaces the Hewlett-Packard 2100, 2114, 2115, and 2116 Computers equipped with DMA to the HP 2883A/2884A/2885A Disc Files. The HP 2883A Disc File consists of a disc controller and one disc drive unit. (The disc controller can control a maximum of two disc drive units.) The HP 2884A Disc File consists only of one disc drive unit, and the HP 2885A Disc File consists only of a power sequencer. (The power sequencer can handle up to six disc controllers.) One interface kit consisting of two printed-circuit cards is required for each disc controller. The two interface cards are electrically identical except for the positions of the jumper wires on each card. The signal outputs to the disc controller are inverted to make the signals compatible with the disc controller logic.

1-5. One interface card, used as the data channel, transfers data, status, and addressing information. The other interface card, used as the command channel, transfers commands and drive selection signals. Commands, addressing, and status words are transferred under program control: data words are transferred under direct memory access (DMA) control.

1-6. KIT CONTENTS.

1-7. The HP 12565A Disc Interface Kit contains the following:

a. 12565-60001 Data Channel Card.
b. 12565-60002 Command Channel Card.
c. 12565-60003 Cable Assembly.
d. 12849-60003 48-Pin Test Connector.
e. 12849-60004 48-Pin Test Connector.
f. 12565-90003 Operating and Service Manual.

1-8. IDENTIFICATION.

1-9. Printed-circuit card revisions are identified by a letter, a revision code, and a division code stamped on the card (e.g. A-1030-22). The letter code identifies the version of the etched trace pattern on the unloaded card. The revision code (four middle digits) refers to the electrical characteristics of the loaded card. The division code (last two digits) identifies the Hewlett-Packard division that manufactured the card. If the revision codes stamped on the printed-circuit cards do not agree with the revision codes shown on the title page of this manual, there are differences between your cards and the cards described in this manual. These differences are described in manual supplements available at the nearest HP Sales and Service Office.

1-10. SPECIFICATIONS.

1-11. Specifications for the data channel card and the command channel card are given in table 1-1.

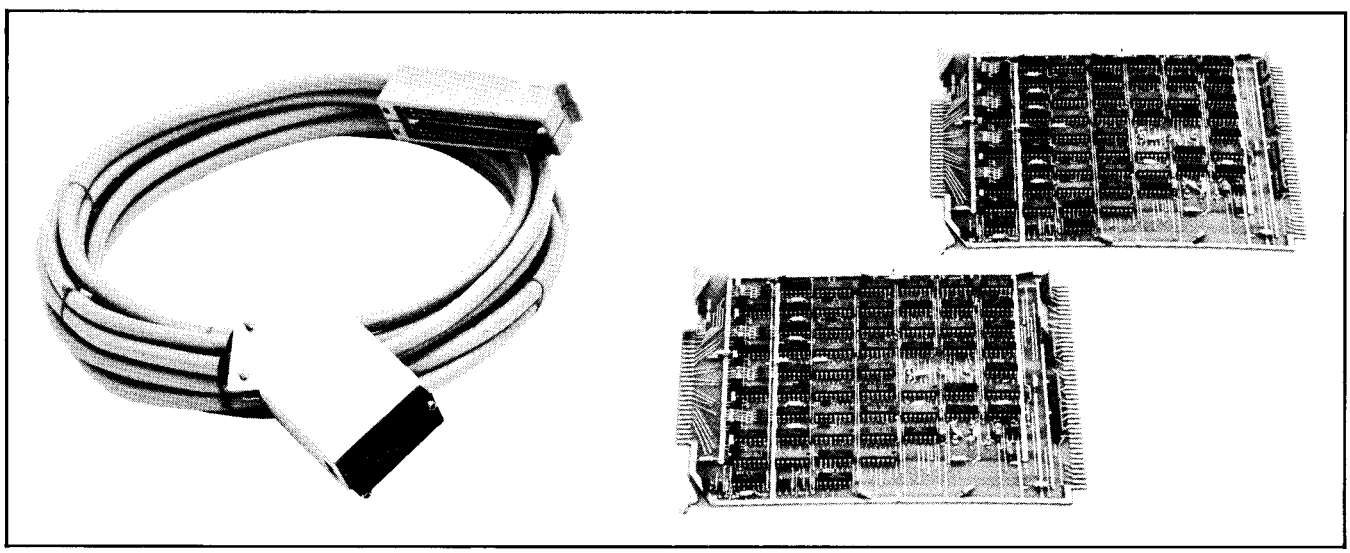

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Figure 1-1. HP 12565A Disc Interface Kit

Table 1-1. Interface Kit Specifications

POWER REQUIREMENTS		VOLTAGE	CURRENTS
		-2V dc +4.5V dc	0.17 amperes 3.5 amperes
SIGNAL REQUIREMENTS		**"0" LEVEL**	**"1" LEVEL**
DATA AND FLAG INPUTS	Voltage	+2.4 to +5V dc (1)	0 to +0.5V dc
	Open Circuit Voltage and Impedance	+3V dc, Z_{in} = 122 ohms	
	Current Required	–	0.025 amperes
	Minimum Pulse Width	300 nanoseconds	
DATA AND COMMAND OUTPUTS	Voltage	+2.4 to +5V dc (2)	0 to +0.5V dc
	Impedance	1K (to +5V dc)	–
	Current Sink (maximum)	–	0.031 amperes

NOTES:
(1) Or open circuit capable of withstanding +5V dc.
(2) +5V dc maximum; impedance determined by external circuit.
(3) Maximum interface cable length is 15 feet.

SECTION II

INSTALLATION AND PROGRAMMING

2-1. INTRODUCTION.

2-2. This section provides information on unpacking, inspection, installation, and programming for the HP 12565A Disc Interface Kit.

2-3. UNPACKING AND INSPECTION.

2-4. If the shipping container is damaged upon receipt, request that the carrier's agent be present when the kit is unpacked. Inspect the kit for contents and damage (cracks in printed-circuit card, broken parts, etc.). If the kit is damaged and fails to meet specifications, notify the carrier and the nearest HP Sales and Service Office immediately. (Sales and Service Offices are listed at the back of this manual.) Retain the shipping container and packing material for the carrier's inspection. The HP Sales and Service Office will arrange for the repair or replacement of the damaged part without waiting for any claims against the carrier to be settled.

2-5. INSTALLATION.

2-6. JUMPER WIRES.

2-7. Table 2-1 lists the jumper wires and their appropriate positions for each interface card. Inspect each card and verify that the jumper wires are in the required positions. See the parts location diagrams in figures 4-1 and 4-2 to determine the physical location of the jumpers.

Table 2-1. Interface Card Jumper Wire Positions

JUMPER WIRE	POSITION	
	COMMAND CHANNEL	DATA CHANNEL
W1	A	A
W2	B	B
W3	B	B
W4	B	B
W5	In	In
W6 thru W8	In	In
W9	A	B
W10	B	B

2-8. CARD INSTALLATION.

CAUTION

Calculate the current drain from the computer power supplies for the interface cards. (Refer to the computer documentation.) The computer may be damaged if the power supplies are overloaded. Also make certain that power is off at the computer and at the disc controller before installing the interface kit, or damage to the computer or disc controller may result.

2-9. Install the interface cards and the interconnecting cable as follows:

a. Turn computer power and disc file power off. Open the computer for access to the I/O card slots

b. Plug the interface cards into the I/O card slots assigned for the particular computer system. (Ensure that the data channel interface card is in the higher priority position.)

c. Pass the interface card connectors of the 12565-60003 Cable Assembly through the opening at the rear of the computer. Slide the connectors onto the corresponding cards and close the computer.

d. Pass the disc controller connector of the cable assembly through the opening below the rear door of the disc file cabinet. Secure the connector to the disc controller with the metal lock tabs located above and below the connector receptacle. Secure the ground lug of the cable assembly under one of the lock tab screws.

2-10. Table 2-2 contains a list of cable assembly pin assignments for both interface card connectors and the disc controller connector. The cable assembly contains 72 twisted-pair conductors. Each twisted pair consists of a signal conductor and a signal-ground conductor. The entries in table 2-2 are organized with the signal conductor of a twisted pair listed first and the corresponding signal-ground conductor immediately following. The table also provides a cross-reference of signal names between the disc controller and the interface cards. The minus signs (-) in the SIGNAL NAME column for the disc controller indicate ground-true, positive-false signal levels. The plus (+) signs indicate positive-true, ground-false signal levels.

2-11. PROGRAMMING.

2-12. The following programming information includes disc drive unit characteristics, addressing information, an explanation of command words and format, content of the disc status word, data transfer timing considerations, sample programs, and programming recommendations.

Table 2-2. Interconnecting-Cable Connector-Pin Functions

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
28	A		Bit 0	CPU Data In 0 Bit
29	BB, 24		Sig Gnd	
30	B		Bit 1	CPU Data In 1 Bit
29	BB, 24		Sig Gnd	
31	C		Bit 2	CPU Data In 2 Bit
32	BB, 24		Sig Gnd	
33	D		Bit 3	CPU Data In 3 Bit
32	BB, 24		Sig Gnd	
34	E		Bit 4	CPU Data In 4 Bit
35	BB, 24		Sig Gnd	
36	F		Bit 5	CPU Data In 5 Bit
35	BB, 24		Sig Gnd	
37	H		Bit 6	CPU Data In 6 Bit
38	BB, 24		Sig Gnd	
39	J		Bit 7	CPU Data In 7 Bit
38	BB, 24		Sig Gnd	
40	K		Bit 8	CPU Data In 8 Bit
41	BB, 24		Sig Gnd	
42	L		Bit 9	CPU Data In 9 Bit
41	BB, 24		Sig Gnd	
43	M		Bit 10	CPU Data In 10 Bit
44	BB, 24		Sig Gnd	
45	N		Bit 11	CPU Data In 11 Bit
44	BB, 24		Sig Gnd	
46	P		Bit 12	CPU Data In 12 Bit
47	BB, 24		Sig Gnd	
48	R		Bit 13	CPU Data In 13 Bit
47	BB, 24		Sig Gnd	
49	S		Bit 14	CPU Data In 14 Bit
50	BB, 24		Sig Gnd	
51	T		Bit 15	CPU Data In 15 Bit
50	BB, 24		Sig Gnd	
1	1		Bit 0	CPU Data Out 0 Bit
2	BB, 24		Sig Gnd	
3	2		Bit 1	CPU Data Out 1 Bit
2	BB, 24		Sig Gnd	
4	3		Bit 2	CPU Data Out 2 Bit
5	BB, 24		Sig Gnd	
7	4		Bit 3	CPU Data Out 3 Bit
5	BB, 24		Sig Gnd	

Table 2-2. Interconnecting-Cable Connector-Pin Functions (Continued)

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
8 10	5 BB, 24		Bit 4 Sig Gnd	CPU Data Out 4 Bit
11 10	6 BB, 24		Bit 5 Sig Gnd	CPU Data Out 5 Bit
12 13	7 BB, 24		Bit 6 Sig Gnd	CPU Data Out 6 Bit
14 13	8 BB, 24		Bit 7 Sig Gnd	CPU Data Out 7 Bit
15 16	9 BB, 24		Bit 8 Sig Gnd	CPU Data Out 8 Bit
17 16	10 BB, 24		Bit 9 Sig Gnd	CPU Data Out 9 Bit
18 20	11 BB, 24		Bit 10 Sig Gnd	CPU Data Out 10 Bit
21 20	12 BB, 24		Bit 11 Sig Gnd	CPU Data Out 11 Bit
22 23	13 BB, 24		Bit 12 Sig Gnd	CPU Data Out 12 Bit
24 23	14 BB, 24		Bit 13 Sig Gnd	CPU Data Out 13 Bit
25 26	15 BB, 24		Bit 14 Sig Gnd	CPU Data Out 14 Bit
27 26	16 BB, 24		Bit 15 Sig Gnd	CPU Data Out 15 Bit
52 53	22 BB, 24		Device Command Sig Gnd	Data Channel Device Command
54 53	23 BB, 24 All Others		Device Flag Sig Gnd Not Used	Data Channel Device Flag
55 56		A BB, 24	Bit 0 Sig Gnd	Command Channel 0 Bit
57 56		B BB, 24	Bit 1 Sig Gnd	Spare (1 Bit)
58 59		C BB, 24	Bit 2 Sig Gnd	Spare (2 Bit)
60 59		D BB, 24	Bit 3 Sig Gnd	Spare (3 Bit)
62 63		E BB, 24	Bit 4 Sig Gnd	Spare (4 Bit)

Table 2-2. Interconnecting-Cable Connector-Pin Functions (Continued)

DISC CONTROLLER CONNECTOR PIN	DATA CHANNEL CARD CONNECTOR PIN	COMMAND CHANNEL CARD CONNECTOR PIN	SIGNAL NAME	
			INTERFACE CARD	DISC CONTROLLER
64 63		K BB, 24	Bit 8 Sig Gnd	Spare (8 Bit)
65 66		P BB, 24	Bit 12 Sig Gnd	Command Channel 12 Bit
67 66		R BB, 24	Bit 13 Sig Gnd	Command Channel 13 Bit
70 71		S BB, 24	Bit 14 Sig Gnd	Command Channel 14 Bit
72 71		T BB, 24	Bit 15 Sig Gnd	Command Channel 15 Bit
73 74		W BB, 24	Power On Normal Sig Gnd	PON
76 74		19 BB, 24	POPIO(B) Sig Gnd	POPIO
77 78		22 BB, 24	Device Command Sig Gnd	Command Channel Device Command
79 78		23 BB, 24 All Others	Device Flag Sig Gnd Not Used	Command Channel Device Flag Not Used

2-13. DISC DRIVE UNIT CHARACTERISTICS.

2-14. The disc drive unit contains 11 discs and 20 read/write heads. (See figure 2-1.) There are 203 cylinders available for information storage. The cylinder address numbers range from zero to 202. Each cylinder consists of 20 tracks, one on each disc surface except for the top of the upper disc and the bottom of the lower disc. Also, each track is divided into 23 sectors. Within a cylinder, sectors are addressed by specifying a read/write head number and a sector number. The head numbers range from zero to 19 and sector numbers range from zero to 22.

2-15. The smallest addressable data storage area in the disc drive unit is a sector. Addressing is accomplished by specifying the cylinder number (0 to 202), read/write head number (0 to 19), and sector number (0 to 22). More information on addressing is contained in paragraph 2-30.

Note

Although there are 203 cylinders for storage, three cylinders are reserved as alternates to replace defective tracks. With 20 tracks per cylinder, a total of 60 tracks are available for alternate use.

2-16. Each sector contains a sector address field and a data field. The sector address field contains the cylinder, head, and sector numbers of the sector, as well as indicators for defective and protected track. The data field stores 128 16-bit words of data. Only the data field is transferred to and from the computer; the sector address field is generated and checked in the disc controller. Both fields are cyclic checked by the disc controller.

2-17. The disc file contains up to two disc drive units, and the disc drive units are numbered zero and one for addressing commands to a particular disc drive unit. Disc drive unit one is addressed if bit 0 equals a logic 0 and disc drive unit two is addressed if bit 0 equals a logic 1. Use of the disc drive unit number bits is explained further in the remainder of this section.

2-18. CHANNEL ADDRESSES.

2-19. The disc file has a data channel and a command channel, each of which can be addressed by the computer program. The data channel is associated with the data channel card and is addressed by using the I/O select code for that card. The command channel is associated with the command channel card and is addressed by using the I/O select code for the command channel interface card.

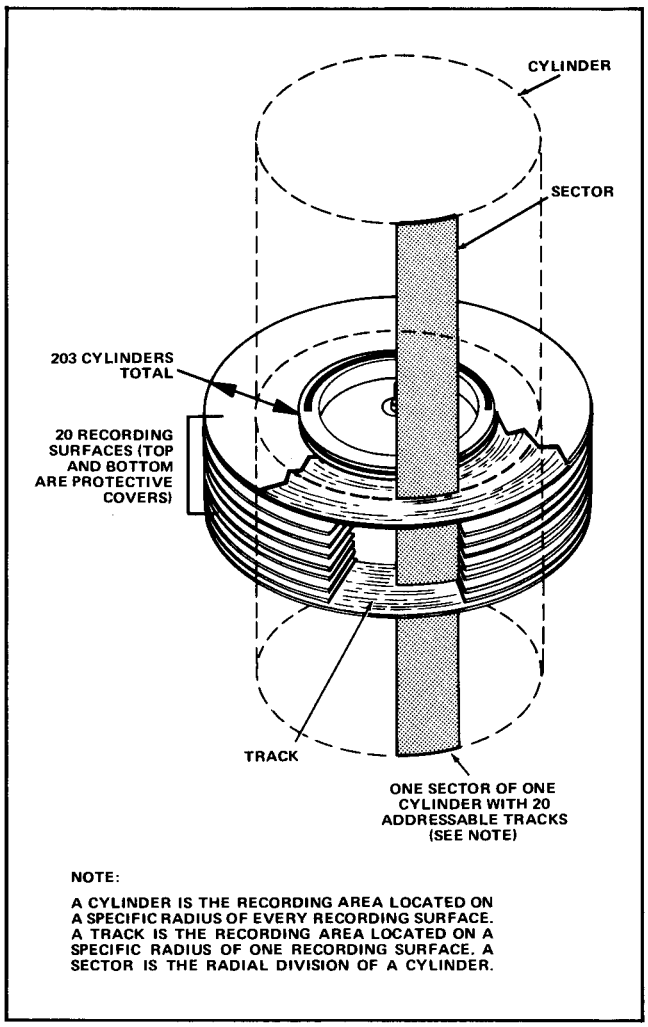

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Figure 2-1. Disc Pack Nomenclature

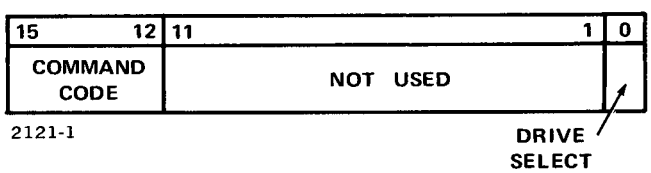
2-20. COMMAND CHANNEL I/O SELECT CODE. The command channel I/O select code can be used with OTA/B, STF, CLF, STC, CLC, SFS, and SFC instructions. The OTA/B instruction sends a command word to the disc controller which specifies the operation to be performed. A STF instruction can be used to force an interrupt to a service subroutine for transferring data or checking status of a drive. The STC and CLF instructions are usually used together to initiate the operation specified in the command word and to ensure that the command channel Flag FF is cleared. The SFS and SFC instructions are used to check command completion (if the Flag FF is set, the command has been executed).

2-21. DATA CHANNEL I/O SELECT CODE. The data channel I/O select code can be used with OTA/B, LIA/B, MIA/B, CLF, STC, CLC, SFS, and SFC instructions. An OTA/B instruction is used to transfer cylinder and head/sector numbers for specifying the location for reading and writing data. The OTA/B instruction also transfers sector count words which are used in data recoverability checks. Either an LIA/B or MIA/B instruction can be used for transferring the disc status word to the computer. The STC and CLF instructions are used together to cause the disc controller to accept the cylinder, head/sector, or sector count number and to ensure that the data channel Flag FF is cleared. The CLC instruction may be used to prevent an interrupt, if the interrupt system is enabled, during cylinder, head/sector, and sector count word transfers. The SFS and SFC instructions are used to check if a word transferred over the data channel by the computer program has been accepted by the disc controller, or if a word has been issued by the disc controller. (If a word has been accepted or issued, the Flag FF is set.)

2-22. COMMAND WORDS.

2-23. To initiate a disc operation, the computer places a command word in the output register of the command channel card and issues an STC instruction. The disc controller decodes the command word and initiates the operation specified on the drive selected. When a Position or Recalibrate command is issued, the disc controller will be free to accept another command as soon as the required address transfer through the data channel has been completed. For all other commands, the command word must remain unchanged on the command channel card until the disc controller sets the Flag FF on the command channel card.

2-24. The command word consists of four bits of command information and one bit of disc drive select information. The format is shown in figure 2-2. The one-bit disc drive select field contains the number of the disc drive unit which is to execute the command. The four-bit command field contains the binary code of the command to be executed. The command codes are shown in table 2-3. An explanation of each command word is discussed in the following paragraphs.



2121-1

Figure 2-2. Command Word Format

2-25. STATUS CHECK. The Status Check command is used to transfer a word of status information from the disc controller to the computer. When the command is issued, the disc controller selects the disc drive unit specified, assembles the status word, and transfers the word to the computer via the data channel interface card. The word details status of the selected disc drive unit as well as conditions detected by the disc controller during data operations with the disc drive unit. Status word bit definitions are given in paragraph 2-42. Command execution is completed when the disc controller sends the status word to the data channel card and sets the Flag FF on the data channel card. The Flag FF is not set on the command channel card.

Table 2-3. Command Codes

CODE BITS				COMMAND
15	14	13	12	
0	0	0	1	Status Check
0	0	1	0	Recalibrate
0	0	1	1	Position
0	1	0	0	Read Data
0	1	0	1	Write Data
0	1	1	0	Read Address
0	1	1	1	Write Address
1	0	0	0	Cyclic Check
1	0	1	1	Load Address
1	1	0	0	Address Skip

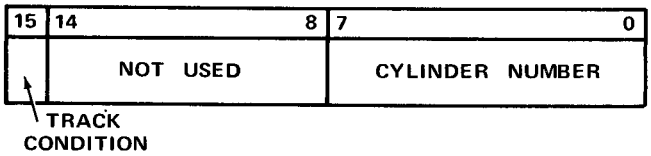
2-26. WRITE DATA. Write data is the normal command used for writing after the disc has been addressed. When the command is issued, the disc controller selects the disc drive unit specified and waits for the addressed sector to come into position. In all cases, the addressed sector is that sector specified by the contents of the disc controller record address register (RAR). When the addressed sector comes into position, the disc controller examines the track condition indicator and addresses information in the address field. If the address compares properly and the track is not protected or defective, the disc controller initiates data transfer from the data channel card. The controller always writes 128 data words in a sector; if the computer sends less than 128 words, the controller fills the remainder of the sector with "0's" before setting the Flag FF on the command channel card. If the computer has more than 128 words to write, the controller adds one to the contents of the record address register and continues writing in the next sector. The maximum number of words that can be written before a new head positioning command is required is 58,880. The maximum number can be written only if the writing starts at sector zero, head zero, of a particular cylinder. In other words, the disc controller will write data in a maximum of 460 sectors before a new Position command or Load Address command is required. Data transfer is suspended as the controller assembles and writes the sector address field. The address information is taken from the record address register; the track indicator information is written as it was read from the first sector. Data transfer resumes with the first data word of the sector. Writing continues until the computer has no more data to transfer, or the disc controller detects an End of Cylinder signal or other error condition. In either case, the Flag FF is set on the command channel card to signal completion.

2-27. If, during the address checking phase of the command, the address does not compare with the contents of the record address register, the Flag FF is set on the command channel card and no writing or data transfer occurs. A Status Check command, which should be issued after every operation, will initiate a status check to determine the cause for termination. If the track is flagged, a Status Check after a Write Data operation indicates Any Error (bit 0), No Record Found (bit 4), and Flagged Track (bit 3). If the track is write protected and the FORMAT switch is not set to FORMAT, the Status Check indicates Any Error and Flagged Track.

2-28. READ DATA. Read Data is the normal command used for reading. When the command is issued, the disc controller compares the contents of the record address register with the sector in position. With the sector in position, the controller initiates data transfer to the data channel card. The controller always reads 128 data words from the data field of the sector. If the computer accepts less than 128 words, the controller continues to the end of the sector to complete the cyclic check before signaling completion by setting the Flag FF on the command channel card. If the computer tries to accept more than 128 data words, the controller adds one to the contents of the record address register and continues reading in the next sector. The maximum number of words that can be read before a new head positioning command is required is 58,880. The maximum number can be read only if the reading starts at sector zero and head zero of a particular cylinder. In other words, the disc controller will read data in a maximum of 460 sectors before a new Position command or Load Address command is required. Data transfer is suspended while the controller examines the address field; data transfer resumes with the first data word of the sector. Reading continues until the computer stops accepting data or the controller detects an End of Cylinder signal or other error condition. In either case, the Flag FF is set on the command channel card to signal completion.

2-29. If the address written in the sector address field does not compare with the contents of the record address register or if the defective track indicator is on, the disc controller halts data transfer and sets the Flag FF on the command channel card. At this point, the disc controller halts data transfer and sets the Flag FF on the command channel card. If the protected track indicator is encountered, the Read Data operation proceeds normally. Issuing a Status Check command after the Read Data operation will indicate the presence of a protected track indicator or the status detailing the cause for early termination. If the track is flagged, the Any Error (bit 0), No Record Found (bit 4), and Flagged Track (bit 3) indicators will be logic 1's. If the track is write protected, the Any Error and Flagged Track indicators will be logic 1's.

2-30. POSITION. Position is the command used to initiate a head positioning operation in the disc drive unit. A Position command must precede all commands except Recalibrate and Load Address commands. When the command is issued, the disc controller selects the disc drive unit specified and accepts two words of address information from the data channel card. The first word contains the cylinder number to which the head is to move; the second word contains the head/sector number. (See figure 2-3 for word formats.)



15 13	12 8	7 5	4 0
NOT USED	HEAD NUMBER	NOT USED	SECTOR NUMBER

2121-2

Figure 2-3. Address Word Formats

2-31. As the disc controller accepts each of these words, it assembles a new record address in the record address register (previous contents of the register are lost), transfers cylinder and head/sector numbers to the selected disc drive unit, and initiates the head positioning operation in the disc drive unit. The Flag FF on the command channel card is not set until the head positioning operation is complete. However, the disc controller is free to perform other operations as soon as the second word of address information has been accepted. Other operations may include commands for this or another disc drive unit.

2-32. If the selected disc drive unit has a head positioning operation already in progress when the Position command is issued, the disc controller will accept the new command and address words normally, but the new head positioning operation will not be initiated. The position-incomplete error condition is set in the disc drive unit. To make maximum use of the computer time and disc drive units of the disc system, two Position commands may be issued before issuing the command to read or write data on a particular disc drive unit. When the Device Flag signal from the disc controller sets the Flag FF on the command channel card, the status word must be examined to determine which disc drive unit set the Flag FF and is ready for data transfer. A method for issuing multiple Position commands is given in table 2-4. If another command is issued to a disc drive unit (write, read, etc.), the Device Flag signal from the other disc drive unit is inhibited until the command has been executed.

2-33. If the command addresses a cylinder number greater than 202, the disc controller accepts the Position command and address words normally. The selected disc drive unit will detect an invalid seek, initiate a restore operation, and remove the File Ready signal. This causes the Any Error and Positioner Busy status bits to be set.

2-34. RECALIBRATE. The Recalibrate command is a special variation of the Position command; however, only the command channel card is involved. In other words, the positioner is directed to an address, but that address is not a result of the two-word cylinder, head/sector address normally transferred to the disc controller by the data channel card. When a Recalibrate command is transferred by the command channel card, the record address register is set to head zero, cylinder zero, and sector zero, and the positioner moves to that location. No transfer of file data occurs between the computer and disc controller. The disc controller generates a Device Flag signal that sets the command channel card Flag FF. The Device Flag signal indicates the completion of the positioner operation. This command can be used to reinstate File Ready if the drive can execute this command.

2-35. ADDRESS SKIP. Address Skip is a special recovery command that the disc controller performs on a sector when the address field is not intact. The command should be used only after retry procedures have failed to recover data. (Error recovery procedures are given in paragraph 2-60). When the command is issued, the disc controller forces a reading of the data field in a sector immediately after the address contained in the record address register. The Flag FF is set on the command channel card to signal completion.

2-36. CYCLIC CHECK. The Cyclic Check command performs a cyclic check of file data to verify recoverability of the data. (A Position command normally precedes the Cyclic Check command to specify the starting address.) The disc controller executes the command in the same manner as the Read Data command; however, no transfer of file data occurs between the computer and the disc controller. When the command is issued, the disc controller accepts a single word of count information from the data channel card. The word contains the positive count of sectors to be checked in the format shown in figure 2-4. The maximum number of sectors that can be checked is 460.

15 9	8 0
NOT USED	SECTOR COUNT

2121-3

Figure 2-4. Sector Count Word Format

2-37. The controller selects the disc drive unit specified and waits for the addressed sector to come into position. With the sector in position, the disc controller examines the track indicators and address information and cyclic checks the entire sector. The disc controller subtracts one from the sector count. If the count is not zero, the checking operation is repeated in the next sector. This process continues until the sector count reaches zero or the disc controller detects an End of Cylinder signal or other error condition. At this point, the Flag FF is set on the command channel card to signal completion.

2-38. If the address written in the sector address field does not compare with the contents of the record address register or the defective track indicator is on during examination of the sector address field, the disc controller halts the checking operation at the end of the current sector and sets the Flag FF on the command channel card. A Status Check command to the disc drive unit in operation will detail the cause for early termination. If the protected track indicator is encountered, the Cyclic Check operation proceeds normally. Issuing a Status Check command after the Cyclic Check operation is complete will indicate the presence of a protected track indicator.

Table 2-4. Sample Program for a Multiple Position Operation

```
0001                    ASMB,A,B,L,T
0002  02000                   ORG 2000B
0003*
0004* THIS PROGRAM PERFORMS OVERLAPPING POSITIONING ON TWO
0005* DISC DRIVES
0006*
0007  02000 002400  INIT  CLA
0008  02001 072174        STA CNTR     SET OPERATION COUNTER TO ZERO
0009  02002 072175        STA UNIT     SET DRIVE UNIT DESIGNATOR TO ZERO
0010  02003 062203        LDA POSN     DEFINE 'RARCH' PROGRAM
0011  02004 072204        STA CMND          TO BE A POSITION COMMAND
0012  02005 062205        LDA CYL0     DESIGNATE CYLINDER AND HEAD AND
0013  02006 066206        LDB HDST0         SECTOR NUMBERS FOR UNIT 0
0014*                                     POSITION
0015  02007 016101        JSB RARCH    GO TO RAR CHANGE PROGRAM AND
0016*                                  POSITION
0017  02010 036175        ISZ UNIT     SET DRIVE UNIT DESIGNATOR TO ONE
0018  02011 062207        LDA CYL1     DESIGNATE CYLINDER AND HEAD AND
0019  02012 066210        LDB HDST1         SECTOR NUMBERS FOR UNIT 1
0020*                                     POSITION
0021  02013 016101        JSB RARCH    GO TO RAR CHANGE PROGRAM AND
0022*                                  POSITION
0023  02014 102320        SFS CC       IS EITHER OF THE POSITIONINGS
0024*                                  COMPLETE?
0025  02015 026014        JMP *-1           NO, KEEP WAITING
0026  02016 016064        JSB STAT          YES, CHECK STATUS ON UNIT 1
0027  02017 012211        AND PBBIT    STATUS IN A-REG, CHECK POSITIONER
0028*                                  BUSY BIT
0029  02020 002002        SZA               IS UNIT 1 BUSY POSITIONING?
0030  02021 026060        JMP SS4                YES, UNIT 0 SET FLAG
0031  02022 062176  SS2   LDA DRST                NO, UNIT 1 SET FLAG
0032  02023 000010        SLA          IS DRIVE STATUS WORD ERROR
0033*                                  BIT SET?
0034  02024 102011        HLT 11B           YES, ERROR HALT
0035  02025 062202        LDA LDADR    DEFINE 'RARCH' PROGRAM TO BE A
0036  02026 072204        STA CMND          LOAD ADDRESS COMMAND
0037  02027 062175        LDA UNIT     DETERMINE WHICH UNIT IS TO
0038*                                  BE READ
0039  02030 002003        SZA,RSS           FROM AND SET RAR PROPERLY
0040  02031 026035        JMP SS7      GO TO SET UP READ FROM UNIT 0
0041  02032 062207        LDA CYL1     DESIGNATE CYLINDER AND HEAD AND
0042  02033 066210        LDB HDST1         SECTOR NUMBERS FOR UNIT 1
0043*                                     LOAD ADDRESS COMMAND
0044  02034 026037        JMP SS6
0045  02035 062205  SS7   LDA CYL0     DESIGNATE CYLINDER AND HEAD AND
0046  02036 066206        LDB HDST0         SECTOR NUMBERS FOR UNIT 0
0047*                                     LOAD ADDRESS COMMAND
0048  02037 016101  SS6   JSB RARCH    GO TO RAR CHANGE PROGRAM
0049  02040 016120        JSB READ     GO READ DATA
0050  02041 016064        JSB STAT     MAKE STATUS CHECK
0051  02042 000010        SLA               IS STATUS WORD ERROR BIT SET
0052  02043 102022        HLT 22B                YES, HALT
0053  02044 062175        LDA UNIT               NO
0054  02045 022212        XOR D1       CHANGE UNIT NUMBER FROM 0 TO 1,
0055  02046 072175        STA UNIT          OR 1 TO 0, AND SAVE
0056  02047 036174        ISZ CNTR     INCREMENT OPERATION COUNTER
0057  02050 062174        LDA CNTR     HAVE BOTH UNITS POSITIONED
0058  02051 052213        CPA D2            AND READ DATA?
0059  02052 102033        HLT 33B                YES, HALT--FINISHED
0060  02053 016064  SS5   JSB STAT               NO, GO GET STATUS
0061  02054 012211        AND PBBIT    STATUS IN A-REG, CHECK POSITIONER
0062*                                  BUSY BIT
0063  02055 002002        SZA               IS THIS UNIT BUSY
0064*                                     POSITIONING?
0065  02056 026053        JMP SS5                YES, KEEP WAITING
0066  02057 026022        JMP SS2                NO, GO SET UP FOR READ
0067*                                               OPERATION
```

Table 2-4. Sample Program for a Multiple Position Operation (Continued)

```
0068  02060 002400  SS4   CLA          UNIT 0 WAS FIRST POSITIONED, SET
0069  02061 072175        STA UNIT     UNIT DESIGNATOR
0070*                                  APPROPRIATELY
0071  02062 016064        JSB STAT     MAKE STATUS CHECK ON UNIT 0
0072  02063 026022        JMP SS2      GO SET UP FOR UNIT 0 READ
0073*                                  OPERATION
0074*
0075* PROGRAM GETS STATUS WORD FOR SPECIFIED UNIT
0076*
0077  02064 000000  STAT  NOP          ENTRY
0078  02065 062201        LDA STCMD    LOAD STATUS COMMAND AND
0079  02066 032175        IOR UNIT          INCLUDE UNIT NUMBER
0080  02067 103717        STC DC,C     PREPARE DATA CHANNEL TO RECEIVE
0081*                                  STATUS
0082  02070 102620        OTA CC       OUTPUT STATUS COMMAND
0083  02071 106720        CLC CC       ENSURE CONTROLLER WILL RESPOND TO
0084*                                  STC
0085  02072 103720        STC CC,C     SIGNAL CONTROLLER
0086  02073 102317        SFS DC       HAS STATUS BEEN LOADED INTO DATA
0087*                                  CHANNEL?
0088  02074 026073        JMP *-1           NO, WAIT
0089  02075 102517        LIA DC            YES, LOAD STATUS INTO
0090*                                       A-REGISTER
0091  02076 106717        CLC DC       CLEAR DATA CHANNEL
0092  02077 072176        STA DRST     STORE STATUS IN DRIVE STATUS WORD
0093  02100 126064        JMP STAT,I   RETURN TO CALLING PROGRAM
0094*
0095* PROGRAM TO POSITION OR LOAD ADDRESS, DEPENDING UPON WHAT
0096* IS STORED INTO CMND--EITHER RESULTS IN RAR CHANGE
0097*
0098  02101 000000  RARCH NOP          ENTRY
0099  02102 102617        OTA DC       OUTPUT CYLINDER NUMBER TO DATA
0100*                                  CHANNEL
0101  02103 103717        STC DC,C     SIGNAL CONTROLLER
0102  02104 062204        LDA CMND     PICK UP COMMAND (POSITION OR LOAD
0103  02105 032175        IOR UNIT          ADDRESS), INCLUDE UNIT
0104  02106 102620        OTA CC            NUMBER, AND OUTPUT TO
0105*                                       CONTROLLER THROUGH
0106*                                       COMMAND CHANNEL
0107  02107 106720        CLC CC       ENSURE CONTROLLER WILL RESPOND TO
0108*                                  STC
0109  02110 103720        STC CC,C     SIGNAL CONTROLLER
0110  02111 102317        SFS DC       HAS CONTROLLER ACCEPTED CYLINDER
0111*                                  NUMBER?
0112  02112 026111        JMP *-1           NO, WAIT
0113  02113 106617        OTB DC       OUTPUT HEAD/SECTOR TO CONTROLLER
0114  02114 103717        STC DC,C     SIGNAL CONTROLLER
0115  02115 102317        SFS DC       HAS CONTROLLER ACCEPTED
0116*                                  HEAD/SECTOR NUMBER?
0117  02116 026115        JMP *-1           NO, WAIT
0118  02117 126101        JMP RARCH,I       YES, RETURN TO CALLING
0119*                                       PROGRAM
0120*
0121* PROGRAM TO READ DATA FROM THE DISC--CORRECT
0122* POSITIONING AND RAR IS ASSUMED
0123*
0124  02120 000000  READ  NOP          ENTRY
0125  02121 062215        LDA CW1      INITIALIZE
0126  02122 102606        OTA 6           DMA
0127  02123 106702        CLC 2            OPERATION
0128  02124 062216        LDA CW2RD          NORMALLY
0129  02125 066175        LDB UNIT           (MODIFY DMA CW2
0130  02126 006002        SZB                ADDRESS PER
0131  02127 042214        ADA B500           UNIT NUMBER)
0132  02130 102602        OTA 2                WITH
0133  02131 102702        STC 2                THREE
0134  02132 062220        LDA CW3                CONTROL
0135  02133 102602        OTA 2                    WORDS
```

Table 2-4. Sample Program for a Multiple Position Operation (Continued)

```
0136  02134 062200         LDA RDCMD    LOAD READ COMMAND WORD,
0137  02135 032175         IOR UNIT          INCLUDE UNIT NUMBER, AND
0138  02136 102620         OTA CC            OUTPUT TO COMMAND CHANNEL
0139  02137 106720         CLC CC       ENSURE CONTROLLER WILL RESPOND TO
0140*                                   STC
0141  02140 103717         STC DC,C     INSURE NO SPURIOUS DATA WILL BE
0142*                                   RECEIVED
0143  02141 103706         STC 6,C      START DMA
0144  02142 103720         STC CC,C     START READ OPERATION
0145  02143 102320         SFS CC       IS READ OPERATION COMPLETE?
0146  02144 026143         JMP *-1           NO, WAIT
0147  02145 126120         JMP READ,I        YES, RETURN
0148*
0149* PROGRAM TO WRITE DATA ONTO DISC--CORRECT
0150* POSITIONING AND RAR IS ASSUMED
0151*
0152  02146 000000  WRITE NOP           ENTRY
0153  02147 062215         LDA CW1      INITIALIZE
0154  02150 102606         OTA 6           DMA
0155  02151 106702         CLC 2            OPERATION
0156  02152 062217         LDA CW2WR          NORMALLY
0157  02153 066175         LDB UNIT           (MODIFY DMA CW2
0158  02154 006002         SZB                ADDRESS PER
0159  02155 042214         ADA B500           UNIT NUMBER)
0160  02156 102602         OTA 2                WITH
0161  02157 102702         STC 2                THREE
0162  02160 062220         LDA CW3                CONTROL
0163  02161 102602         OTA 2                     WORDS
0164  02162 062177         LDA WRCMD    LOAD WRITE COMMAND WORD,
0165  02163 032175         IOR UNIT          INCLUDE UNIT NUMBER, AND
0166  02164 102620         OTA CC            OUTPUT TO COMMAND CHANNEL
0167  02165 106720         CLC CC       ENSURE CONTROLLER WILL RESPOND TO
0168*                                   STC
0169  02166 102117         STF DC       ENSURE NO SPURIOUS DATA IS
0170*                                   WRITTEN
0171  02167 103706         STC 6,C      START DMA
0172  02170 103720         STC CC,C     START WRITE OPERATION
0173  02171 102320         SFS CC       IS WRITE OPERATION COMPLETE?
0174  02172 026171         JMP *-1           NO, WAIT
0175  02173 126146         JMP WRITE,I       YES, RETURN TO CALLING
0176*                                   PROGRAM
0177*
0178* PARAMETERS, CONTROL WORDS, CONSTANTS, ETC.
0179*
0180  00017          DC     EQU 17B      DATA CHANNEL TO/FROM CONTROLLER
0181  00020          CC     EQU 20B      COMMAND CHANNEL TO CONTROLLER
0182  02174 000000  CNTR   BSS 1        OPERATION COUNTER
0183  02175 000000  UNIT   BSS 1        UNIT NUMBER--0 OR 1
0184  02176 000000  DRST   BSS 1        STORAGE FOR DRIVE STATUS WORD
0185  02177 050000  WRCMD  OCT 50000    WRITE COMMAND WORD
0186  02200 040000  RDCMD  OCT 40000    READ COMMAND WORD
0187  02201 010000  STCMD  OCT 10000    STATUS COMMAND WORD
0188  02202 130000  LDADR  OCT 130000   LOAD ADDRESS COMMAND WORD
0189  02203 030000  POSN   OCT 30000    POSITION COMMAND WORD
0190  02204 000000  CMND   BSS 1        WILL CONTAIN POSITION OR LOAD
0191*                                   ADDRESS COMMAND
0192  02205 000003  CYL0   OCT 3        CYLINDER NUMBER FOR DRIVE UNIT 0
0193*                                   POSITION
0194  02206 006021  HDST0  OCT 6021     HEAD/SECTOR FOR DRIVE UNIT 0
0195*                                   POSITION
0196  02207 000100  CYL1   OCT 100      CYLINDER NUMBER FOR DRIVE UNIT 1
0197*                                   POSITION
0198  02210 003003  HDST1  OCT 3003     HEAD/SECTOR FOR DRIVE UNIT 1
0199*                                   POSITION
0200  02211 000004  PBBIT  OCT 4        DRIVE BUSY POSITIONING BIT
0201  02212 000001  D1     DEC 1        CONSTANT--FOR MASKING STATUS WORD
```

Table 2-4. Sample Program for a Multiple Position Operation (Continued)

```
0202*                                    ERROR BIT
0203  02213 000002  D2     DEC 2         CONSTANT--OPERATION COUNTER LIMIT
0204  02214 000500  B500   OCT 500       INCREMENT USED TO MODIFY
0205*                                    CW2RD/CW2WR
0206  02215 120017  CW1    OCT 120017    DMA CONTROL WORD 1
0207  02216 104000  CW2RD  OCT 104000    DMA CONTROL WORD 2 FOR READ
0208  02217 006000  CW2WR  OCT 6000      DMA CONTROL WORD 2 FOR WRITE
0209  02220 177470  CW3    DEC -200      DMA WORD COUNT AND CONTROL WORD 3
0210                       END
** NO ERRORS*
```

2-39. WRITE ADDRESS. Write address is the command used to initialize unwritten tracks and to generate the defective track indicator or protected track indicator. (A Position command must precede the Write Address command to specify the starting address.) This command is accepted only when the FORMAT switch on the disc file is set to FORMAT. If the FORMAT switch is set to OFF, the command channel card Flag FF is set and the disc controller makes no attempt to execute the command. The disc controller executes the command in the same manner as the Write Data command, except that the controller does not check the first sector for address and track indicator information. When the command is issued, the disc controller selects the disc drive unit specified and waits for the starting address sector to come into position. With the sector in position, the disc controller assembles and writes the address field. The address information is written from the computer via DMA. The track condition information is written according to the state of bit 15 of the address word. (See figure 2-3.) If bit 15 is a "1," the Flag bit in the address field is set and the Flag FF on the command card is set.

2-40. READ ADDRESS. The Read Address command determines the address of an alternate track when a flagged defective track is called by the record address register. (All sectors of a defective track should contain the address of the alternate track.) After a Position command and Read Address command are issued, the disc controller waits for the next sector to come into position, then reads the address field. The resulting two-word address is transferred to a computer via the data channel card. The Device Flag from the disc controller sets the command channel card Flag FF when the operation is complete. If a Status Check command after a Read Address command indicates a data error, the Read Address command should be repeated because the first Read Address operation may have occurred at the defective sector of the flagged track. After a satisfactory address is stored in memory, a Position command starts the selected head toward the alternate track.

Note

At the time a track is flagged as defective and an alternate address assigned, a Read Address command should be issued to verify a successful address transfer.

2-41. LOAD ADDRESS. The Load Address command is used to alter the contents of the record address register in the disc controller. The command is executed in the same manner as the Position command, except that no operation is initiated on the disc drive unit specified. When the command is issued, the disc controller accepts two words of address information from the data channel card. The format of the address words is that described in paragraph 2-30. As the disc controller accepts each of these words, it assembles a new record address in the record address register (previous contents of the register are lost). When the second address word has been accepted, command execution terminates, and the Flag FF is set on the command channel card.

Note

The Load Address command is useful to ensure that the correct disc drive unit is selected for servicing during a multiple position operation.

2-42. STATUS WORD.

2-43. The disc status word is an 8-bit word that lists the condition of the disc file. A Status Check command issued by the computer program causes the disc controller to generate the status word. The status word then can be transferred to the computer by an LIA/B instruction to the data channel I/O select code. The portion of the program shown in table 2-4 labeled STAT obtains a disc status word. The format and content of the disc status word are given in table 2-5.

2-44. DATA TRANSFER TIMING CONSIDERATIONS.

Note

The restrictions in paragraphs 2-45 and 2-46 apply only to transfer of file data and not to transfers involving address, count, or status information.

2-45. During data transfer to and from the disc controller, the computer must transfer data at an average rate equal to the data rate of the disc drive unit. (The data rate of the disc drive unit is 156,000 words per second.) This transfer rate

Table 2-5. Disc Status Word

BIT	DESCRIPTION
0	ANY ERROR. A "1" indicates that "PL0 unsafe" condition has been detected or that one or more of the remaining 7 bits is a "1".
1	DATA ERROR. A "1" indicates an error has been detected in the data transfer between the disc controller and the disc drive unit during a read operation.
2	POSITIONER BUSY. A "1" indicates the selected drive is busy executing a Position command.
3	FLAGGED TRACK. A "1" indicates the track being processed is write-protected or defective. If the track is defective, the ANY ERROR, NO RECORD FOUND, and FLAGGED TRACK bits will be "1's." If a Write Data or Write Address command is issued without the FORMAT switch set to FORMAT, the ANY ERROR and FLAGGED TRACK bits will be "1's."
4	NO RECORD FOUND. A "1" indicates the address read from the track does not compare with contents of the record address register in the disc controller. When bit 3 (FLAGGED TRACK) also is a "1," the track being processed is defective.
5	END OF CYLINDER. A "1" indicates the computer has attempted to extend a data command across a cylinder boundary. This occurs when the computer has more data to write or read and the end of sector 22, head 19 has been reached.
6	NOT READY. A "1" indicates that the selected disc drive unit is not connected to the disc controller, or is not sequenced up with disc spinning and heads loaded, or is in an unsafe condition. Normally, manual intervention is required to bring a disc drive unit from the not-ready to the ready stage.
7	DRIVE ID. A "1" indicates disc drive unit one; a "0" indicates disc drive unit zero.

is maintained by the request/response nature of the computer/disc controller communication on the data channel card. The disc controller transfers a word of data and sets the Flag FF on the data channel card to request service. The computer, in turn, accepts the data through DMA and sends a Device Command signal (STC and CLF instructions) to the disc controller to input another data word.

2-46. In order to maintain data transfers with the disc drive unit, the computer must respond to the request for service within a certain length of time, termed the data transfer window time. (The data transfer window time of the disc drive unit is from 19.2 microseconds to 25.6 microseconds.) If the computer fails to respond within the data transfer window time, the disc controller terminates the data transfer with the computer. No further communications occur on the data channel card. The disc controller completes processing of the current sector before setting the Flag FF on the command channel card. If a write operation is in process, "0's" are written in the remainder of the field; if a read operation is in process, the remainder of the field is cyclic checked. If the computer responds with a STC instruction to the data channel card after the termination of data transfer but before the setting of the Flag FF on the command channel card, the disc controller sets a data overrun error latch. This is to warn the program that the computer may have failed to transfer as much data as intended.

2-47. SAMPLE PROGRAMS.

2-48. Sample programs are integrated with the multiple position program. (Refer to table 2-4.) They consist of a status check labeled STAT, a record address register change labeled RARCH, a read operation labeled READ, and a write operation labeled WRITE. Table 2-6 gives a summary of device flag responses to aid in varying a program to suit a particular need.

Note

In the RARCH section of the multiple position program, either a Position command or Load Address command is used to change the record address register, depending on which command word the calling program stores in variable CMND. Although both commands change the record address register, only the Position command results in head movement.

2-49. PROGRAMMING RECOMMENDATIONS.

2-50. DESIGN CONSIDERATIONS. The disc file has been designed to function with an interrupt driven program. In most cases, the best level of system performance will be achieved when the program issues one or more disc storage commands and then goes on to other tasks,

Table 2-6. Device Flag Responses to Command Words

COMMAND	RESPONSE
STATUS CHECK	Device Flag is issued to data channel card after the status word is transferred. (See note 1.)
WRITE DATA	Device Flag is issued to data channel card after each data word is transferred. Device Flag is issued to command channel card after completion.
READ DATA	Device Flag is issued to data channel card after each data word is transferred. Device Flag is issued to command channel card after completion.
POSITION	Device Flag is issued to data channel card after each of the two address words is transferred. Device Flag is issued to command channel card after head positioning is complete. (See note 1.)
ADDRESS SKIP	Device Flag is issued to data channel card after each data word is transferred. Device Flag is issued to command channel card after completion of the command.
CYCLIC CHECK	Device Flag is issued to data channel card after sector count word is transferred. Device Flag is issued to command channel card after completion.
WRITE ADDRESS	Device Flag is issued to data channel card after each address word is transferred. Device Flag is issued to command channel card after completion.
LOAD ADDRESS	Device Flag is issued to data channel card after each of the two address words is transferred. Device Flag is issued to command channel card after completion.
READ ADDRESS	Device Flag is issued to data channel card after each of the two address words is transferred. Device Flag is issued to command channel card after completion.
RECALIBRATE	Device Flag is issued to command channel card after completion.

NOTE: 1. When the last data channel Device Flag has been issued for a Status Check or a Position command, the disc controller is free to process other commands. To issue another command, a CLC is first issued to the command channel. Any command may then be issued normally. If no command is issued after the last data channel Device Flag for a Position command, the disc controller will issue a command channel Device Flag when any positioner operation completes.

relying upon the disc controller to generate a command channel interrupt whenever a command is completed. Following each interrupt, the program must issue a Status Check command to the disc drive unit that executed the storage command and verify that the Any Error bit (bit 0) is not a "1" in the disc status word. A new command can then be issued to either disc drive unit in the system. Although the disc controller has no capability to queue or execute more than one read or write command at a time, provisions have been made to allow overlap of Position commands. (Refer to paragraph 2-32.) In applications where more than one disc drive unit is active, such overlap should be used to minimize the effects of accessing delays.

2-51. DISC CONTROLLER RECORD ADDRESS REGISTER. The record address register controls the location of the positioner. As an operation starts, the present cylinder, head, and sector information is read from the disc address

field. The address is compared with the contents of the record address register. As the disc turns, the comparing function continues until an equal is obtained between the record address register and the present address field. When an equal compare is found, the disc controller initiates the data handling operation. If a comparison is not achieved, the Any Error (bit 0) and No Record Found (bit 4) indicators will be a "1" during the following Status Check command.

Note

To initialize the disc, a Recalibrate command should be issued to start initializing at cylinder, head, and sector zero.

2-52. Use can be made of the fact that the RAR address is updated by the disc controller when multiple sectors are processed (such as reading or writing more than 128 words of data). If the program needs to read sectors 2 and 3 into one core memory block and sectors 4 and 5 into another, two Read Data commands are used. The RAR sector address must be at 2 when the first Read Data command is issued (and a DMA word count of 256). When the command is completed, the program executes a Status Check command to test for errors, modifies the core memory starting address, and issues a second Read Data command. Similar techniques may be used for writing successive sectors from several different core memory locations.

2-53. WRITE CHECKING. When records are written on a disc drive unit, some form of program check should be executed to ensure that the record was written exactly as it existed in core memory and that the record can be recovered without error from the disc. Where data integrity is crucial, each record written should be read back from the disc into core memory and compared word-for-word with the original record transferred during the write operation. This provides a check, not only on the serial data transfer between the disc controller and the disc drive unit, but also on the parallel transfer between the disc controller and the computer. The latter is important since the system provides no hardware check of data transfer from computer to the file during write operations.

2-54. Where data integrity is less crucial, issuing a Cyclic Check command to the address of each record that is written on the disc is sufficient. (Refer to paragraph 2-36.) This provides a check on the serial data transfer between the disc controller and the disc. Write checking should be eliminated from the program in those situations where data integrity is not crucial.

2-55. DISC INITIALIZATION. All discs have been analyzed for defects by the disc manufacturer according to accepted industry standards. Prior to use in a system, new (unwritten) discs should be processed by a disc initialization program. The program should initialize all sectors to generate the sector address fields and provide for flagging any tracks found defective. (Refer to paragraph 2-39.) Also, the program should execute additional data testing to help isolate defects which may have developed after the manufacturing process. The additional data testing should include the following routine executed six times on each track:

a. Write a fixed pattern in all data fields of the track.

b. Execute the Cyclic Check command 10 times to all sectors of the track.

2-56. On each of the six passes, a different data pattern should be used. Below, in octal, are the six words recommended:

a. 000000
b. 101421
c. 125252
d. 052525
e. 162745
f. 170360

2-57. If a data error occurs more than once in executing the routine on a track, the track should be flagged defective.

2-58. TRACK FLAGGING AND DEFECTIVE TRACK PROCESSING. As discussed earlier, the disc controller provides the program with the ability to flag tracks as either write-protected or defective. (One flag bit indicates both conditions. Software is required to differentiate between the two conditions.) In either case, the entire track (all 23 sectors) must be so flagged to avoid erroneous responses from the disc controller during subsequent operations on the track. The Write Address command should be used for the flagging operation.

2-59. There are several workable schemes for handling defective tracks. Regardless of the method employed, the following recommendations should be considered:

a. The system should allow up to three cylinders per disc as alternates to replace flagged tracks (leaving 200 cylinders for active data storage).

b. If the system relies on reading an alternate track address from the defective track, the address should be written in several different (preferably in all) sectors of the defective track.

2-60. ERROR RECOVERY PROCEDURES. Certain errors which are detected in the disc status word (see table 2-5) during data storage operations are often correctable through retry procedures. User programs should include provisions for retry to reduce the frequency of errors which impact on the application. Listed below are the correctable error conditions and the recommended retry procedures for each:

a. Data Error During Read Data Operation. Read the same record 16 times. If the error persists after 16 retries, issue a Recalibrate command. Issue a Position command to the failing record address, and reread up to 16 times. If error persists, terminate retry.

b. Data Error During Write Data or Write Address Operations. Retry the write operation once. If error persists, terminate retry.

c. Data Error During Write Check Routine. If data error occurs during the Read Data or Cyclic Check operations used in a write check routine (refer to paragraph 2-53), the complete Write Data operation and write check routine should be retried three times or more. If the error persists, the track should be either flagged immediately or logged for future checking and possible flagging. If an error is detected during the word-for-word comparison, the Write Data operation and write check routine should be retried once.

d. No Record Found. Issue a Recalibrate command then a Position command to the failing cylinder. If error persists, terminate retry.

2-61. RECORD LENGTH. The maximum number of sectors that can be written or read before a new Position command or Address Load command must be issued is 460. This can occur only if the Read Data or Write Data operation starts at head 0, sector 0. When the end of sector 22 is reached the disc controller will automatically switch from head 0 to head 1 or from head 2 to head 3, etc.

SECTION III

THEORY OF OPERATION

3-1. INTRODUCTION.

3-2. This section contains a brief functional description of the disc interface kit followed by a detailed circuit description. An overall block diagram of the disc interface is shown in figure 3-1. Signal timing diagrams are given in figures 3-2 and 3-3. Functional flow diagrams for each command operation are provided in figures 3-4 through 3-10. Schematic diagrams of the two interface cards are provided in figures 4-1 and 4-2.

3-3. FUNCTIONAL DESCRIPTION.

3-4. COMPUTER POWER ON.

3-5. When power is initially applied by the POWER switch of the computer, the POPIO (B) and CRS signals are received simultaneously from the I/O control card. These signals establish initial conditions for operation of the command channel and data channel cards. The POPIO (B) signal sets the Flag Buffer FFs on each card and resets the output data and command bit lines from each card to logic 0 (+4.5 volts dc). The POPIO(B) signal from the command channel card is buffered and sent to the disc controller to establish initial conditions for the disc system. The CRS signal resets the Control FF and Device Command FF on each interface card.

3-6. When the dc power supplies in the computer have settled to the proper output voltages, the Power On Normal (PON) signal is applied to the interface cards for buffering. Only the buffered PON signal from the command channel card is applied to the disc controller to indicate that the computer dc power supplies are operating properly.

3-7. DATA OUTPUT OPERATIONS.

3-8. To output data to the disc memory system, address words are sent through the data channel card and command words are sent through the command channel card to prepare the system for a write operation. Data to be written is then sent through the data channel card under DMA control.

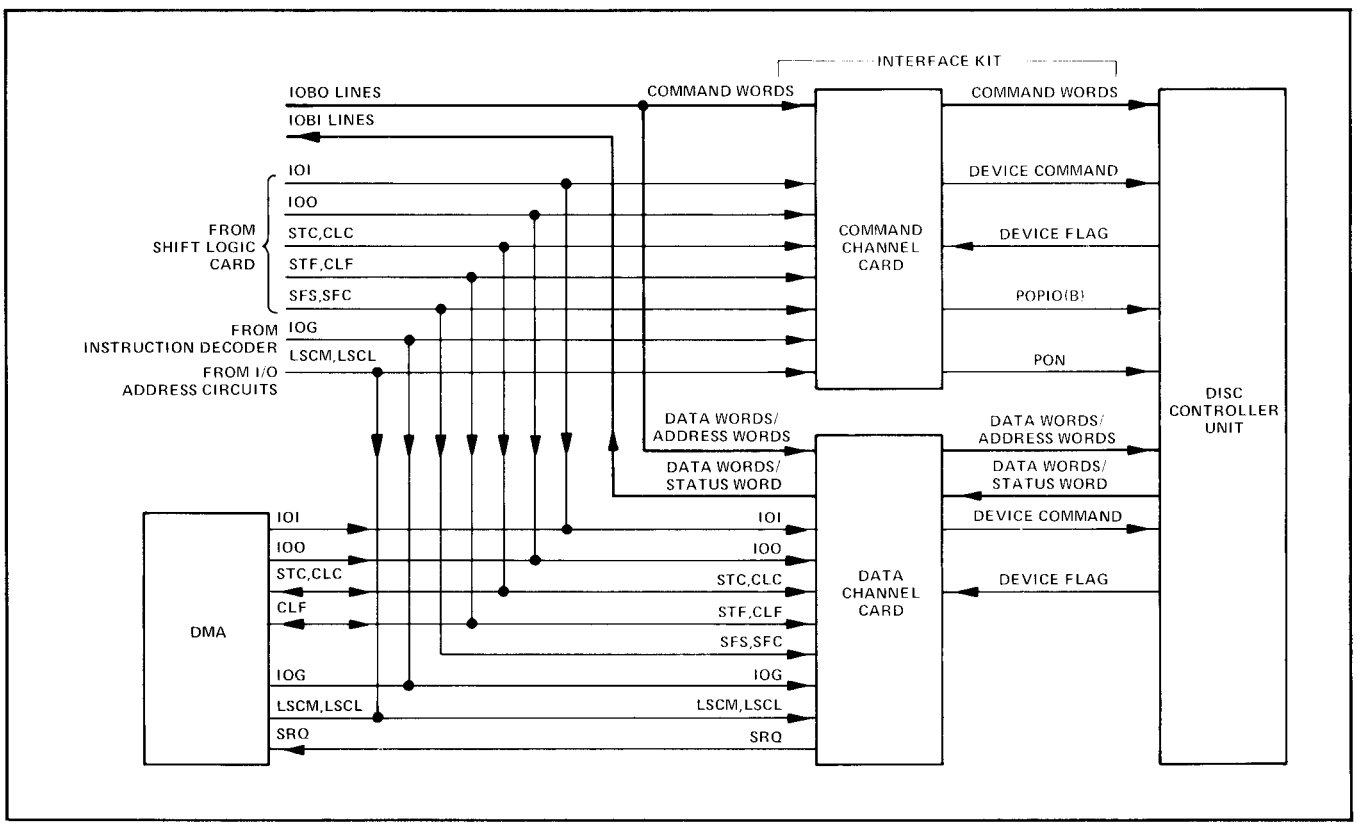


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Figure 3-1. Disc Interface Overall Block Diagram

3-9. CYLINDER NUMBER TRANSFER. The cylinder number is placed in the A- or B-register by a LDA/B instruction. An OTA/B instruction with the data channel card select code places the cylinder number (bits 0 through 7) on the IOBO lines to the output buffer register on the data channel card. The IOO signal from the computer, as a result of the OTA/B instruction, clocks the cylinder number into the output buffer register. The cylinder number is now present on the data channel lines to the disc controller. The output buffer register still contains the cylinder number until the IOBO lines change state and another IOO signal to the data channel card is received. The voltage levels of the bits are inverted by the gates at the output of the buffer register to make the buffer register logic compatible with the disc controller logic. An STC,C instruction with the data channel card select code sets the Device Command FF and clears the Flag Buffer FF and Flag FF. The set output from the Device Command FF is inverted and sent to the disc controller data channel as a ground-true Device Command signal. The Device Command signal indicates that information is available on the data channel lines to the disc controller.

3-10. POSITION COMMAND TRANSFER. The Position command word is placed in the A- or B-register by a LDA/B instruction. An OTA/B instruction with the command channel card select code places the command word on the IOBO lines to the output buffer register on the command channel card. The IOO signal from the computer, as a result of the OTA/B instruction, clocks the Position command word into the output buffer register. The Position command word is now present on the command channel lines to the disc controller. The voltage levels of the command word bits are inverted by the gates at the output of the buffer register to make the buffer register logic compatible with the disc controller logic. An STC,C instruction with the command channel select code sets the Device Command FF and clears the Flag Buffer FF and Flag FF. The set output from the Device Command FF is inverted and sent to the disc controller command channel as a ground-true Device Command signal. This signal causes the disc controller to decode the command word and initiate write/read head positioning on the selected drive. The disc controller issues a Device Flag signal to the data channel interface card to set the Flag Buffer FF and Flag FF when the cylinder number (first word of the two word address) has been accepted.

3-11. HEAD/SECTOR NUMBER TRANSFER. The head/sector number bits (see figure 2-3) are transferred to the disc controller by the same instructions and in the same manner as the cylinder number. After the head positioning operation is complete, the disc controller issues a Device Flag signal to clear the Device Command FF and to set the Flag Buffer FF and Flag FF on the command channel card.

3-12. WRITE DATA COMMAND TRANSFER. Before the Write Data command is issued, DMA is initialized to prepare DMA to respond with the proper data and assume control of the data transfer when the Write Data Command is accepted by the disc controller. During initialization, the starting address in memory that contains the data is specified along with the number of data words to be transferred.

3-13. The Write Data command word bits (see figure 2-2) are transferred to the disc controller by the same instructions and in the same manner as the Position command. (Refer to paragraph 3-10.) Next, the program issues a STF instruction to the data channel card. The resulting STF signal sets the Flag Buffer FF and Flag FF. The set output from the Flag FF is sent to DMA as a Service Request (SRQ) signal. The disc controller will issue a Device Flag signal to the command channel card when all the data has been transferred and the write operation is complete.

3-14. DATA TRANSFER. When DMA receives the SRQ signal from the data channel card, phase 5 is set on the next machine cycle and DMA provides SCL, SCM, IOG, and IOO signals to transfer data to the disc. The SCL, SCM, and IOG signals enable the IOO signal to clock the first data word into the output buffer register and onto the data channel lines to the disc controller. Also, DMA issues a STC instruction to the data channel interface card which generates the Device Command signal to indicate that a data word is present on the data lines to the disc controller. When the data word is accepted, the disc controller issues Device Flag to clear the Device Command FF and set the Flag Buffer FF and Flag FF. The set output from the Flag FF (SRQ signal) is sent to DMA and the process is repeated for each word until all the data words are transferred.

3-15. DATA INPUT OPERATIONS.

3-16. Data is transferred from the disc system to the computer by sending address and read command words through the data and command channels, and receiving data words, under DMA control, through the data channel.

3-17. ADDRESSING. Addressing the disc system to locate the data to be read consists of sending the cylinder number, the Position command, and the head/sector number to the disc controller in the same manner as described in paragraphs 3-9 through 3-11.

3-18. READ DATA COMMAND TRANSFER. Before the Read Data command is issued, DMA is initialized to prepare DMA to assume control of the data transfer when the Read Data command word is accepted by the disc controller. During initialization, the starting address in memory where the first data word will be stored and the number of data words to be transferred are specified. The last step in the initialization process sends a STC,C instruction to the data channel interface card to set the Device Command FF and clear the Flag Buffer FF and Flag FF.

3-19. The Read Data command word bits (see figure 2-2) are transferred to the disc controller by the same instructions and in the same manner as the Position command. (Refer to paragraph 3-10.) When the disc controller has accepted the Read Data command word and has applied the first data word to the input buffer register on the data channel card,

it issues a Device Flag signal to the data channel card. This clears the Device Command FF and sets the Flag Buffer FF and Flag FF. The set output from the Flag FF (SRQ signal) is sent to DMA to start the data transfer. Also, the Device Flag signal clocks the data word into the input buffer register.

3-20. DATA TRANSFER. When DMA receives the SRQ signal from the data channel card, phase 5 is set on the next machine cycle and DMA provides LSCL, LSCM, IOG, STC, CLF, and IOI signals to transfer data to the computer. The IOI signal gates the data out of the input buffer register onto the IOBI lines for storage in memory.

3-21. Next, DMA issues STC and CLF signals to the data channel card. The STC signal sets the Device Command FF which in turn sends a Device Command signal to the disc controller. The CLF signal clears the Flag Buffer FF and Flag FF to enable the Device Flag signal to generate another data word to the input buffer register and a Device Flag signal to clock the data into the input buffer register. The Device Flag signal also clears the Device Command FF and sets the Flag Buffer FF and Flag FF. The set output from the Flag FF sends another SRQ signal to DMA which sets the computer in another phase 5 mode on the next machine cycle. The above process is repeated for each data word until the number of data words specified during initialization of DMA have been transferred.

3-22. On the last phase 5 of the data transfer, the STC signal is not sent to the data channel card and this prevents the disc controller from inputing another data word beyond the number specified. A CLC signal from DMA is sent during the last phase 5 to clear the Control FF on the data channel card.

3-23. DETAILED CIRCUIT DESCRIPTION.

3-24. COMPUTER POWER ON.

3-25. When power is initially applied, POPIO(B) and CRS signals are applied simultaneously to both interface cards. The POPIO(B) signal sets the Flag Buffer FF, provides a ground-true POPIO(B) signal to the disc controller from the command channel card (the POPIO(B) from the data channel card is not used), and provides a clock input to the output buffer register FF. The true clock input clears the flip-flops since all IOBO lines are false at power turn on. The output gates from the buffer register invert the positive-true/ground-false signal levels to ground-true/positive-false levels to be compatible with the disc controller logic. The Control Reset (CRS) signal resets the Control FF and Device Command FF. The CRS signal buffered through U101B is not used.

3-26. At time T2, the ENF signal from the I/O control card resets the Interrupt Request (IRQ) FF. The set output from the Flag Buffer FF and the ENF signal set the Flag FF.

3-27. The Power Or Norma (PON) signal is buffered and inverted and connected to pin W. Only the command channel card PON signal is routed to the disc controller. The ground-true PON signal indicates that the computer power supplies are operating normally, and a positive-false signal indicates a computer power fail.

3-28. OUTPUT OPERATIONS.

3-29. COMMAND CHANNEL CARD. Command words are placed on the IOBO lines to the output buffer register FFs by an OTA/B instruction with the command channel card select code. The select code (LSCM, LSCL) from the I/O address circuits, along with the IOG(B) signal from the I/O control card starting at time T3, enables the instruction logic gates. The IOO signal resulting from the OTA/B instruction is applied to gate U35C at time T3T4. The false output from U35C during T4 is inverted by U75A to clock the command word into the output buffer register FFs. The gates in the output lines from the output buffer register are constantly enabled by jumper wire W4 in position B. The command word is now present on the command channel lines to the disc controller. The false output from U35C is also applied to the ORL (Output Register Loaded) FF; however, this curcuit is not used.

3-30. Next, an STC,C instruction is issued to the command channel card select code from the computer program. Again, the instruction logic gates are enabled by LSCM, LSCL, and IOG(B) signals starting at time T3. The STC and CLF signals are applied simultaneously during time T4. The STC signal sets the Control FF and Device Command FF. The true set-side output from the Control FF is applied to gate U36B to enable the disc controller Device Flag signal to cause an interrupt after the command has been executed. The buffered CTL signal from gate U94B is not used. The true set-side output of the Device Command FF provides the ground-true Device Command signal to the disc controller command channel.

3-31. The CLF signal clears the Flag Buffer FF and the Flag FF. The true clear-side output from the Flag FF provides flag status information for the SFC instruction and allows the Flag Buffer FF to be set when a Device Flag signal is received from the disc controller command channel.

3-32. The Device Flag signal is applied to the command channel card when the addressed disc drive has executed the command. The negative-going Device Flag signal is inverted by gate U77A and delayed 100 nanoseconds by R61 and C3. The leading edge of the signal is shaped by schmitt trigger U77C, U77D, R62, R63, and R64. The positive-going output from U77D is applied to the command reset pulse-shaping network (U76A, U76C, R66, and C5) and to the flag pulse-shaping network (U76B, U76D, R65, and C4). The output from each pulse-shaping network is a negative-going 300-nanosecond pulse. The pulse from U76D is inverted and applied to gate U77B which is enabled by the clear condition of the Flag FF. The resulting false output sets the Flag Buffer FF. The output from U75B also clocks the Bit 0 through Bit 15 FFs of the input buffer register; however, these bits are not used in this application.

3-33. The Flag Buffer FF set-side output sets the Flag FF at time T2 (ENF true). The set output from the Flag FF provides flag status information for the SFS instruction. The SRQ and FLG signals generated by the set-side output of the Flag FF are not used in command channel operation. If the interrupt method is used with the command channel, the Flag FF set-side output is also "anded" with the Interrupt Enable (IEN) signal from the I/O control card and with the Control FF set-side output to prevent I/O devices of lower priority from requesting interrupt (PRL false). At time T5 (SIR true) the IRQ FF is set, providing an I/O device of higher priority has not requested interrupt (PRH false). The true set-side output from the IRQ FF generates the FLGL and IRQL signals which are applied to the computer I/O address circuits to request an interrupt during the next available machine cycle and to specify the service request address (the memory location corresponding to the address, or select code, of the command channel card). Generally, the memory location will contain a JSB instruction.

3-34. When the computer responds to the interrupt, the IAK signal becomes true. The IAK signal and the true set-side output from the IRQ FF reset the Flag Buffer FF. Another command word may now be transferred by an OTA/B instruction followed by an STC,C instruction.

3-35. DATA CHANNEL CARD. Address words (cylinder and head/sector numbers) are transferred to the disc controller in the same manner and by the same instructions as the command words through the command channel card. (Refer to paragraphs 3-29 through 3-34). However, the interrupt method is not used in data channel card operation.

3-36. Data words are transferred by control signals provided by DMA during phase 5. After DMA has been initialized, the program sends a STF signal to the data channel interface card. The LSCM and LSCL signals from the I/O address card and the IOG(B) signal from the I/O control card enable the instruction logic gates at time T3 of the fetch phase (phase 1). The STF signal, during time T3, sets the Flag Buffer FF which, in turn, sets the Flag FF at time T2 of the next machine cycle.

3-37. The true set-side output from the Flag FF generates a ground-true FLG signal to the disc controller which is not used. The positive-true SRQ signal is sent to DMA to set phase 5 on the next machine cycle. With phase 5 set, LSCM, LSCL, and IOG(B) signals are true during the entire machine cycle. The IOO and STC signals are applied simultaneously during T3T4. The STC signal sets the Device Command FF; the true set-side output is inverted to provide a ground-true Device Command signal to the disc controller data channel. The IOO signal causes a true clock signal to the output buffer register FF to be generated during T4. The data word is gated onto the IOBO lines to the output buffer register at time T4T5 by DMA, and is present on the data channel lines to the disc controller starting at T4. The gates in the output lines from the output buffer register are constantly enabled. The output from U35C is also applied to the Output Register Loaded (ORL) FF; however, this circuit is not used.

3-38. The Clear Flag (CLF) signal is sent to the data channel card by DMA during time T4T5 of phase 5 to clear the Flag Buffer FF and the Flag FF. The SRQ signal is false when the Flag FF is cleared at the beginning of T4, which prevents another phase 5 from being set on the next machine cycle.

3-39. When the disc memory system has accepted the data word, the disc controller issues a negative-going Device Flag signal to the data channel card. The positive-going leading edge from U77A is shaped by the schmitt trigger circuit and applied to the pulse-shaping networks in the same manner as described in paragraph 3-32. The false 300-nanosecond pulse from gate U76C resets the Device Command FF. The negative-going pulse output from gate U76D is inverted and "anded" with the true clear-side output from the Flag FF to set the Flag Buffer FF. At time T2, the true set output from the Flag Buffer FF is "anded" with the ENF signal to set the Flag FF. The set output from the Flag FF generates another SRQ signal to set phase 5 on the next machine cycle.

3-40. The process described in paragraphs 3-37 through 3-39 is repeated for each data word transferred.

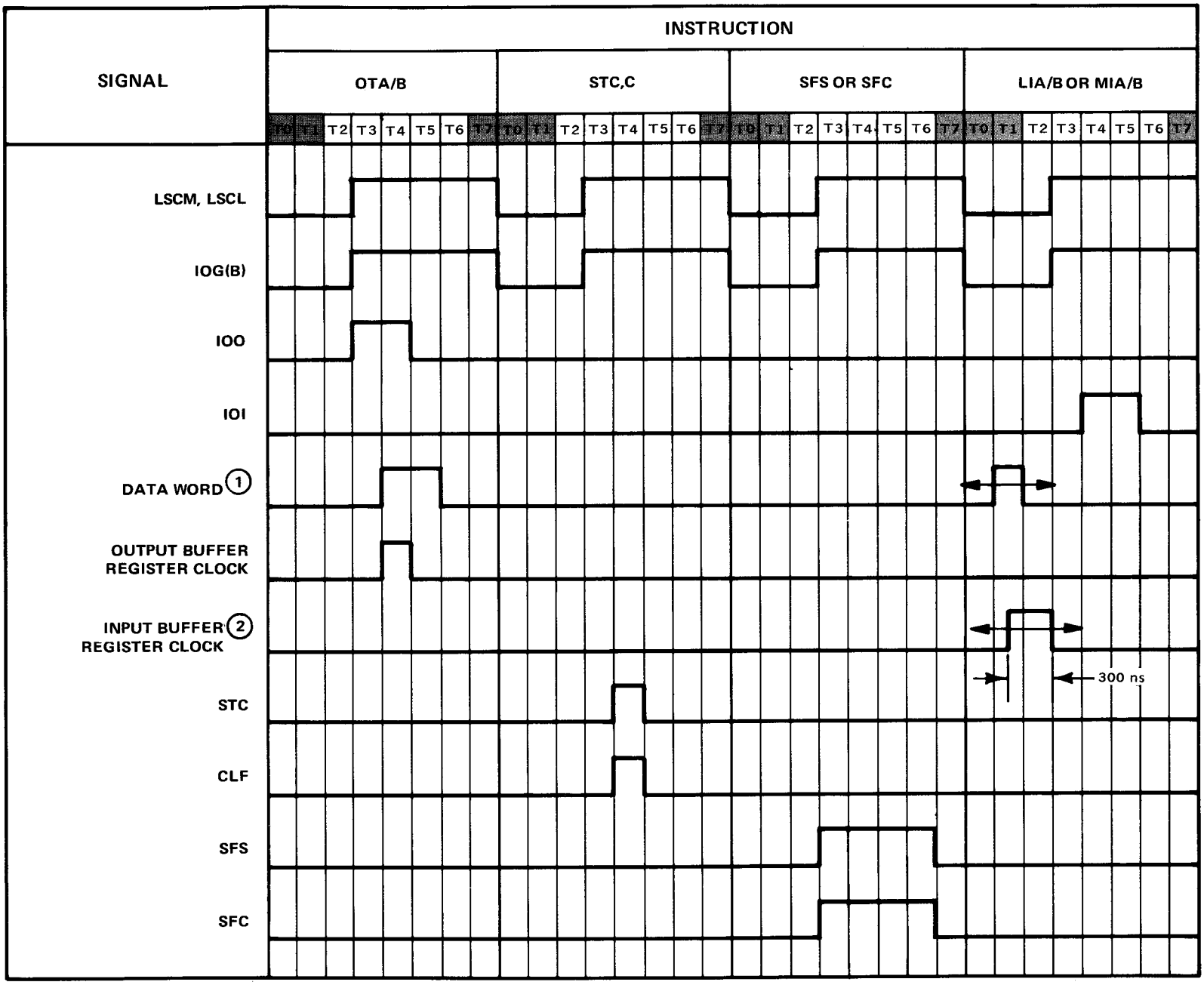
3-41. INPUT OPERATIONS.

3-42. COMMAND CHANNEL CARD. When the disc memory system consists of two disc drive units and multiple Position command operations are used, the first disc drive unit to complete the execution will cause the disc controller to send a Device Flag signal to the command channel card.

3-43. When the Device Flag signal is received, the Device Command FF is cleared and the Flag Buffer FF is set. At time T2, the Flag FF is set, and the true set-side output is "anded" with the SFS signal when the SFS instruction is issued by the computer program. The resulting SKF signal at T4 causes the computer to skip the next instruction which may be a JMP *-1. (Refer to table 2-4.) On the next machine cycle, an LIA instruction with the command channel select code will generate a true IOI signal at T4T5. The true IOI signal and the true output from U46B enable the gates in the input lines from the input buffer register during T4T5. The status of the first disc drive unit to complete the Position command is then put on the IOBI lines to the computer.

3-44. DATA CHANNEL CARD. The control signals required to transfer the data words to the computer are provided by DMA during phase 5; status words are transferred by control signals resulting from instructions in the computer program.

3-45. When the first data word is placed on the input lines to the input buffer register, a negative-going Device Flag signal is applied to the card. The positive-going leading edge from U77A is shaped by the schmitt trigger circuit and applied to the pulse-shaping networks. The negative-going 300-nanosecond pulse from U76C clears the Device Command FF. The output from U76D provides a true clock signal for storing the data word in the input buffer register. The true output from U85B is also "anded" with the true clear-side



NOTES:

(1) DATA WORD MEANS COMMAND WORD, ADDRESS WORD, OR STATUS WORD. THE STATUS WORD OR ATTENTION BITS WILL BE LOADED ONTO THE DATA LINES FROM THE DISC CONTROLLER SIMULTANEOUSLY WITH THE DEVICE FLAG SIGNAL.

(2) LEADING EDGE TIME OCCURS 100 NANOSECONDS AFTER THE DEVICE FLAG SIGNAL.

■ SHADED TIME PERIODS USED IN 2114, 2115, AND 2116 COMPUTERS ONLY.

Figure 3-2. Signal Timing During Program Control

output from the Flag FF to set the Flag Buffer FF. At time T2 (ENF true), the set output from the Flag Buffer FF sets the Flag FF.

3-46. The true set-side output from the Flag FF generates a true SRQ signal. The SRQ signal is sent to DMA to set phase 5 on the next machine cycle. With phase 5 set, LSCM, LSCL, and IOG(B) signals are true during the entire machine cycle. The IOI signal, which is true during T2 of phase 5, is "anded" with the true output from U46B. The resulting true output from U15B gates the data word onto the IOBI lines for storage in computer memory.

3-47. During T3T4 of phase 5 the STC signal is true, which sets the Device Command FF. The true set-side output provides the ground-true Device Command signal to the disc controller. The Device Command signal causes the disc controller to input another data word.

3-48. During T4T5 of phase 5, the CLF signal is true, which clears the Flag Buffer FF and the Flag FF. The SRQ signal is false when the Flag FF is cleared at the beginning of T4, which prevents another phase 5 on the next machine cycle.

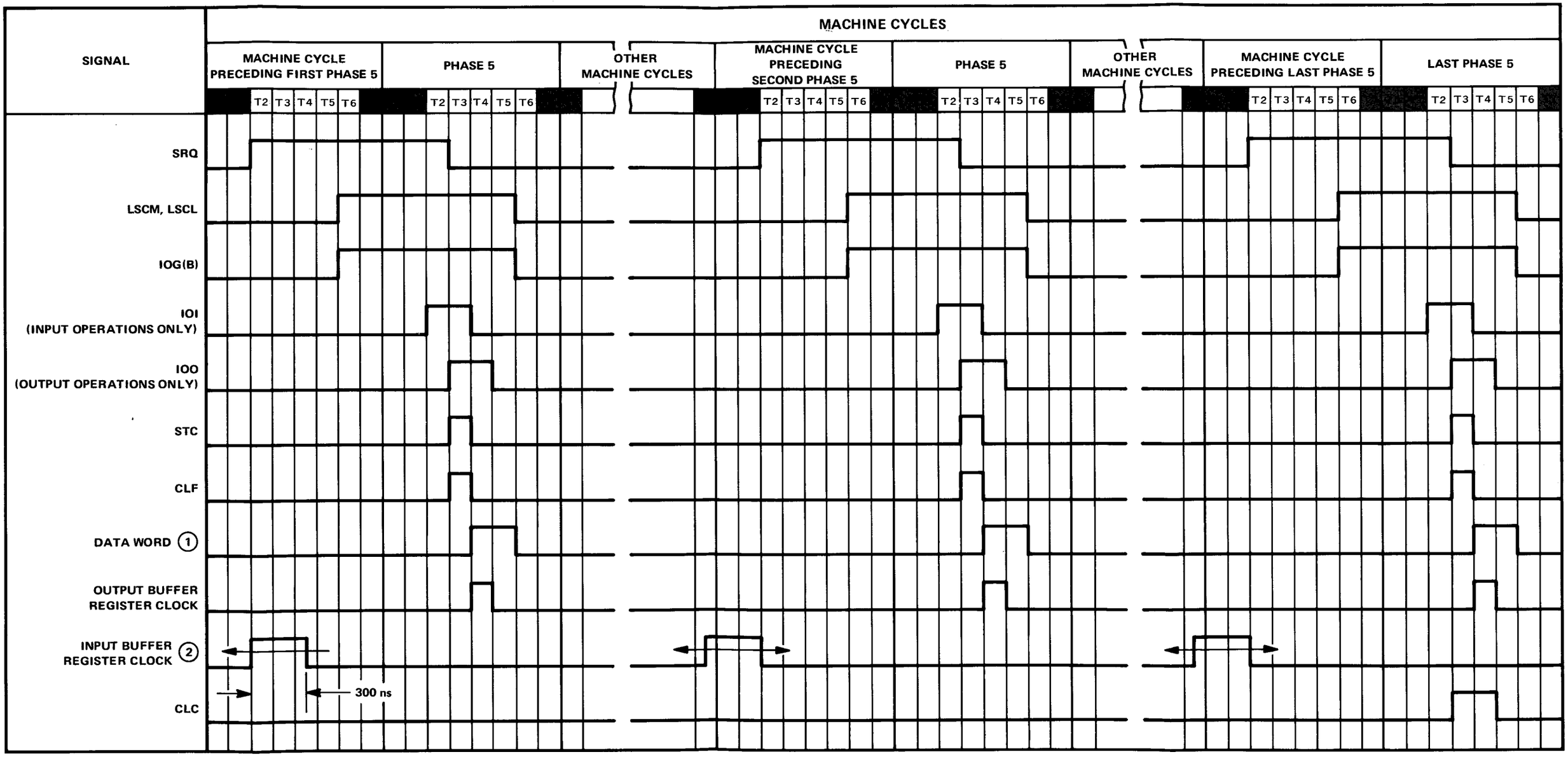
3-49. The process described in paragraphs 3-45 through 3-48 is repeated for each data word until all the data words are transferred.

3-50. When the disc status word is placed on the input lines to the input buffer register, a Device Flag signal is sent to the data channel card. The Device Flag signal clears the Device Command FF, clocks the disc status word into the input buffer register, and sets the Flag Buffer FF. At time T2, the Flag FF is set.

3-51. If the skip flag method is used by the computer program, an SFS instruction will be issued by the program. The resulting SFS signal, which is true during T3, is "anded" with the true set output from the Flag FF to generate the SKF signal. The computer will skip the next instruction in the program and execute the following instruction. The following instruction may be an LIA/B with the data channel card select code to input the disc status word into the A- or B-register. The IOI signal, resulting from the instruction, is true during time T4T5 and enables the gates in the input lines from the input buffer register. The disc status word is now present on the IOBI lines for storage in the A- or B-register.

3-52. If the interrupt method is used, the true set output from the Flag FF is "anded" with the true IEN signal from the I/O control card and with the true set-side output from the Control FF, which prevents I/O devices of lower priority from requesting an interrupt (PRL false). At time T5 (SIR true) the IRQ FF is set by gate U25A, providing that an I/O device of higher priority has not requested interrupt (PRH false). The true set-side output from the IRQ FF generates the FLGL and IRQL signals which are applied to the computer I/O address circuits to request the computer for an interrupt on the next available machine cycle and to specify the service request address (the memory location corresponding to the address, or select code, of the data channel interface card). Generally, the memory location will contain a JSB instruction. The subroutine will contain an LIA/B or MIA/B instruction to gate the disc status word onto the IOBI lines.

3-53. When the computer responds to the interrupt, the IAK signal and the true set-side output of the IRQ FF clear the Flag Buffer FF.



2090-3A

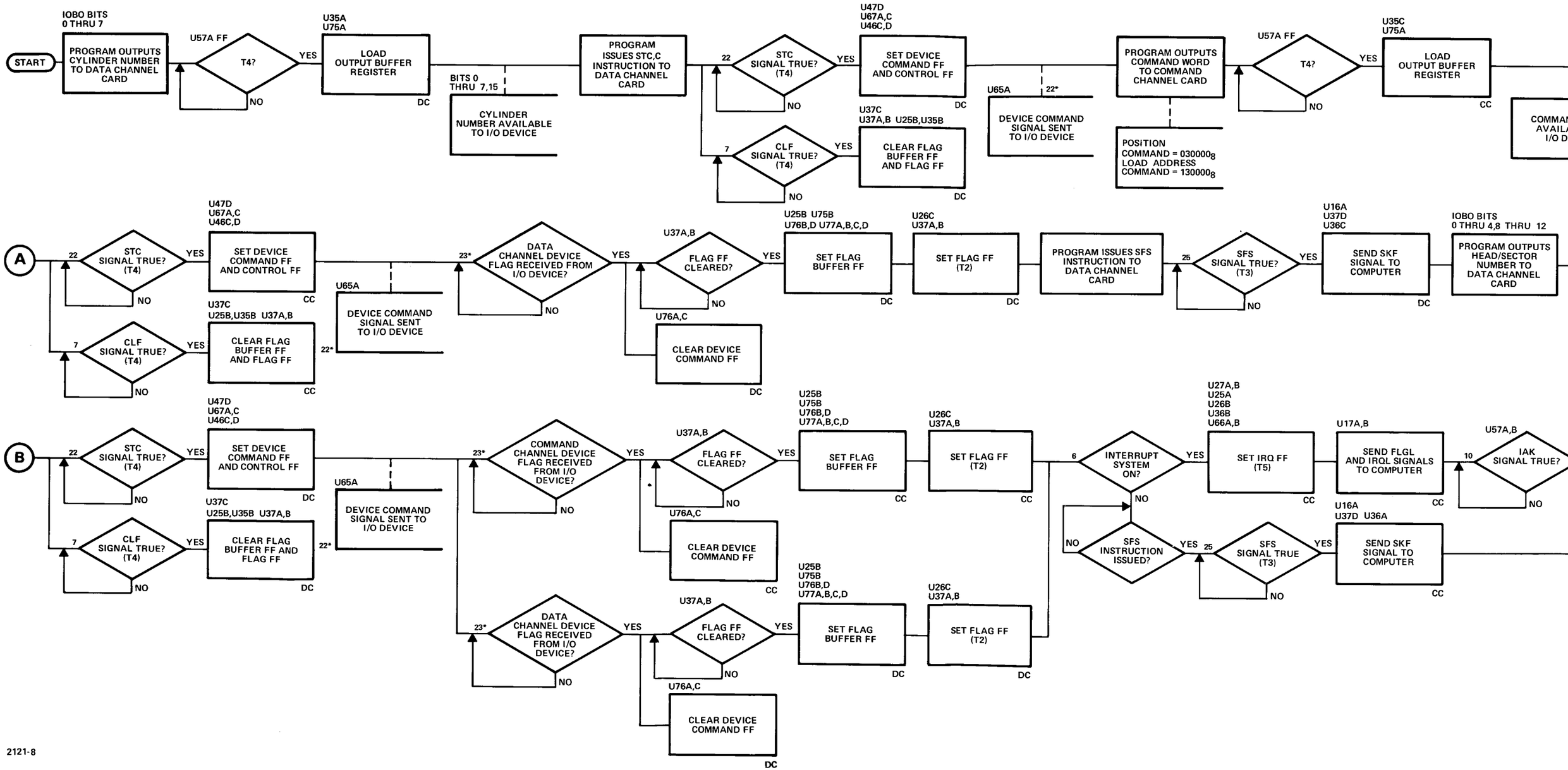
NOTES:

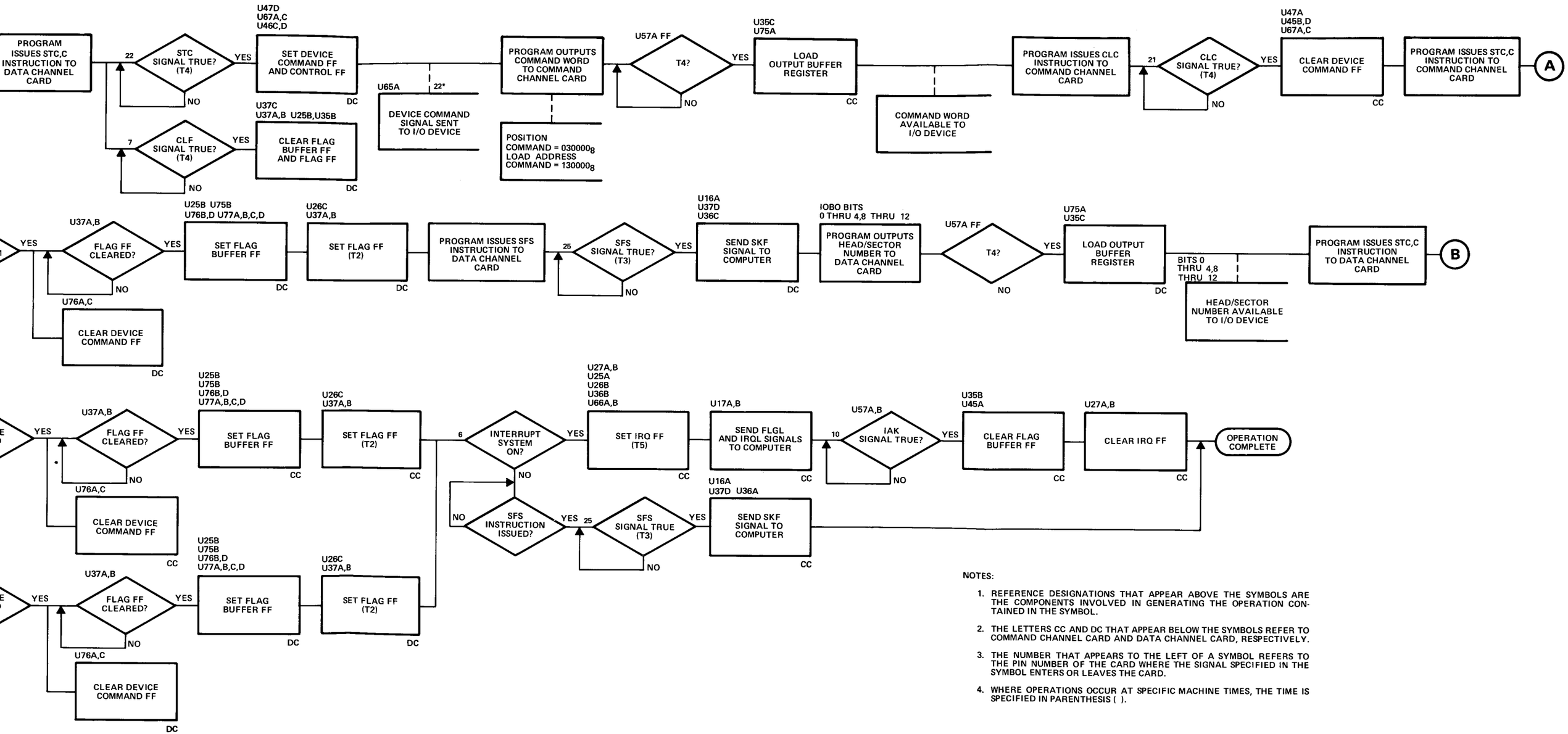
(1) OUTPUT DATA WORD TIMING IS SHOWN. INPUT WORD WILL BE LOADED ONTO THE DATA LINES FROM THE DISC CONTROLLER SIMULTANEOUSLY WITH DEVICE FLAG SIGNAL.

(2) LEADING EDGE TIME OCCURS 100 NANOSECONDS AFTER THE DEVICE FLAG SIGNAL.

■ SHADED TIME PERIODS USED IN 2114, 2115, AND 2116 COMPUTERS ONLY.

Figure 3-3. Signal Timing During DMA Control

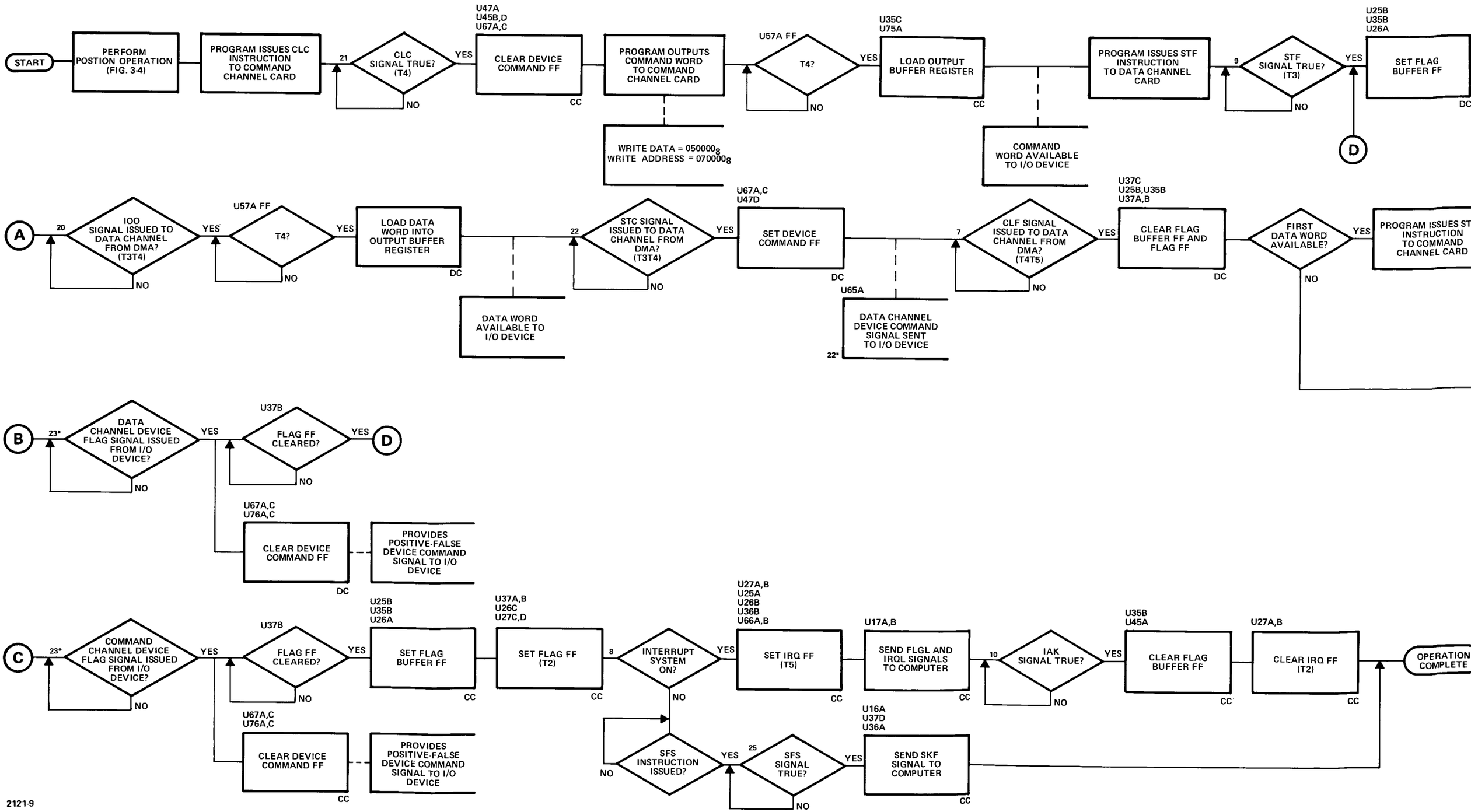

START
IOBO BITS 0 THRU 7
PROGRAM OUTPUTS CYLINDER NUMBER TO DATA CHANNEL CARD
U57A FF
T4?
YES
NO
U35A U75A
LOAD OUTPUT BUFFER REGISTER
DC
BITS 0 THRU 7,15
CYLINDER NUMBER AVAILABLE TO I/O DEVICE
PROGRAM ISSUES STC,C INSTRUCTION TO DATA CHANNEL CARD
22
STC SIGNAL TRUE? (T4)
U47D U67A,C U46C,D
SET DEVICE COMMAND FF AND CONTROL FF
7
CLF SIGNAL TRUE? (T4)
U37C U37A,B U25B,U35B
CLEAR FLAG BUFFER FF AND FLAG FF
U65A
22*
DEVICE COMMAND SIGNAL SENT TO I/O DEVICE
PROGRAM OUTPUTS COMMAND WORD TO COMMAND CHANNEL CARD
POSITION COMMAND = 030000$_8$ LOAD ADDRESS COMMAND = 130000$_8$
U35C U75A
LOAD OUTPUT BUFFER REGISTER
CC
A
U37C U25B,U35B U37A,B
CLEAR FLAG BUFFER FF AND FLAG FF
23*
DATA CHANNEL DEVICE FLAG RECEIVED FROM I/O DEVICE?
U37A,B
FLAG FF CLEARED?
U76A,C
CLEAR DEVICE COMMAND FF
U25B U75B U76B,D U77A,B,C,D
SET FLAG BUFFER FF
U26C U37A,B
SET FLAG FF (T2)
PROGRAM ISSUES SFS INSTRUCTION TO DATA CHANNEL CARD
25
SFS SIGNAL TRUE? (T3)
U16A U37D U36C
SEND SKF SIGNAL TO COMPUTER
IOBO BITS 0 THRU 4,8 THRU 12
PROGRAM OUTPUTS HEAD/SECTOR NUMBER TO DATA CHANNEL CARD
B
U27A,B U25A U26B U36B U66A,B
SET IRQ FF (T5)
U17A,B
SEND FLGL AND IRQL SIGNALS TO COMPUTER
U57A,B
IAK SIGNAL TRUE?
6
INTERRUPT SYSTEM ON?
SFS INSTRUCTION ISSUED?
U16A U37D U36A
SEND SKF SIGNAL TO COMPUTER
2121-8

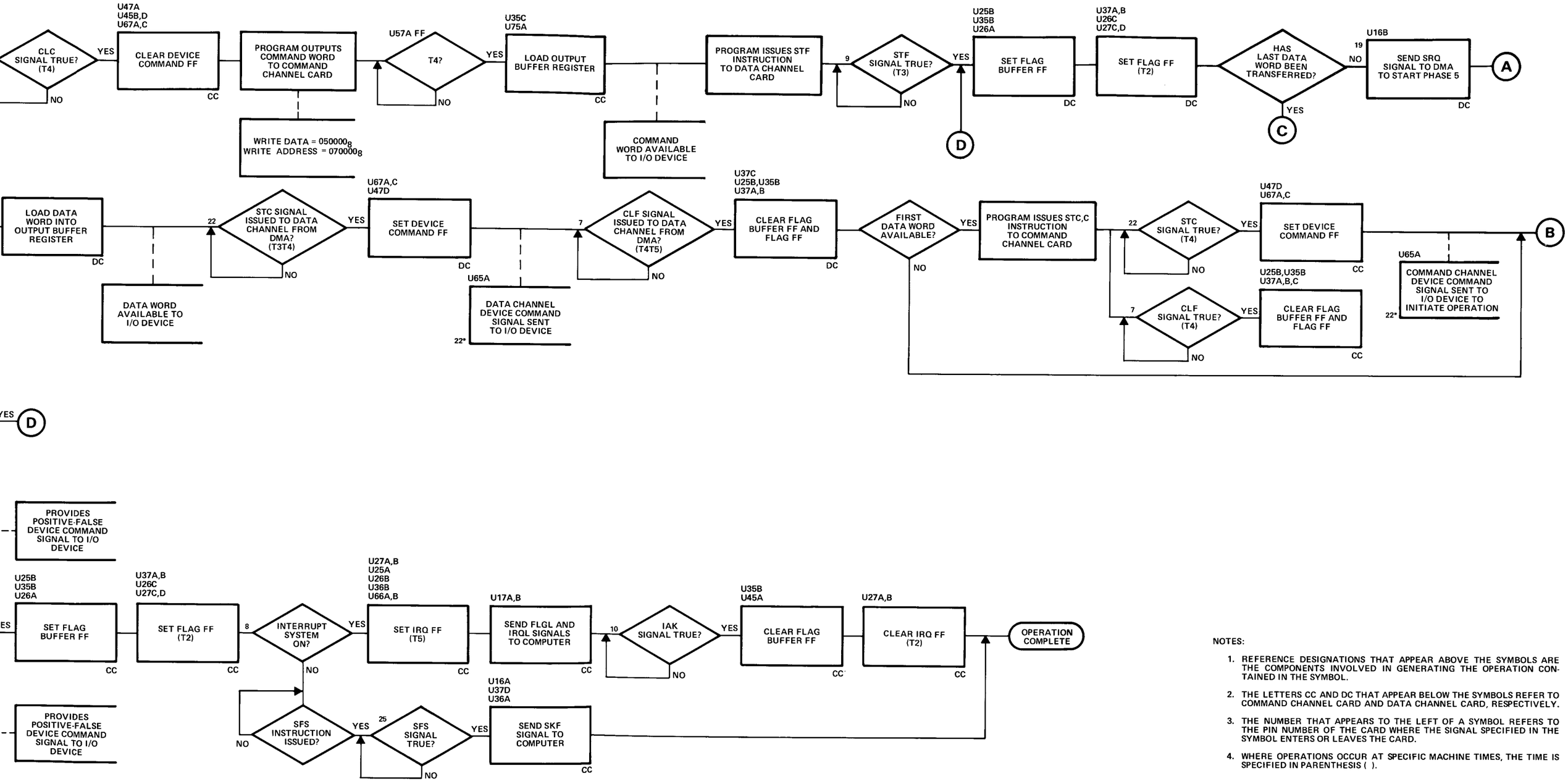


NOTES:

1. REFERENCE DESIGNATIONS THAT APPEAR ABOVE THE SYMBOLS ARE THE COMPONENTS INVOLVED IN GENERATING THE OPERATION CONTAINED IN THE SYMBOL.
2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY.
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-4. Position and Load Address Operations, Flow Diagram


START
PERFORM POSTION OPERATION (FIG. 3-4)
PROGRAM ISSUES CLC INSTRUCTION TO COMMAND CHANNEL CARD
21
CLC SIGNAL TRUE? (T4)
YES
NO
U47A
U45B,D
U67A,C
CLEAR DEVICE COMMAND FF
CC
PROGRAM OUTPUTS COMMAND WORD TO COMMAND CHANNEL CARD
WRITE DATA = 050000₈
WRITE ADDRESS = 070000₈
U57A FF
T4?
YES
NO
U35C
U75A
LOAD OUTPUT BUFFER REGISTER
CC
COMMAND WORD AVAILABLE TO I/O DEVICE
PROGRAM ISSUES STF INSTRUCTION TO DATA CHANNEL CARD
9
STF SIGNAL TRUE? (T3)
YES
NO
U25B
U35B
U26A
SET FLAG BUFFER FF
DC
D
A
20
IOO SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T3T4)
YES
NO
U57A FF
T4?
YES
NO
LOAD DATA WORD INTO OUTPUT BUFFER REGISTER
DC
DATA WORD AVAILABLE TO I/O DEVICE
22
STC SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T3T4)
YES
NO
U67A,C
U47D
SET DEVICE COMMAND FF
DC
U65A
DATA CHANNEL DEVICE COMMAND SIGNAL SENT TO I/O DEVICE
22*
7
CLF SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T4T5)
YES
NO
U37C
U25B,U35B
U37A,B
CLEAR FLAG BUFFER FF AND FLAG FF
DC
FIRST DATA WORD AVAILABLE?
YES
NO
PROGRAM ISSUES ST INSTRUCTION TO COMMAND CHANNEL CARD
B
23*
DATA CHANNEL DEVICE FLAG SIGNAL ISSUED FROM I/O DEVICE?
YES
NO
U37B
FLAG FF CLEARED?
YES
NO
D
U67A,C
U76A,C
CLEAR DEVICE COMMAND FF
DC
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
C
23*
COMMAND CHANNEL DEVICE FLAG SIGNAL ISSUED FROM I/O DEVICE?
YES
NO
U37B
FLAG FF CLEARED?
YES
NO
U25B
U35B
U26A
SET FLAG BUFFER FF
CC
U67A,C
U76A,C
CLEAR DEVICE COMMAND FF
CC
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
U37A,B
U26C
U27C,D
SET FLAG FF (T2)
CC
8
INTERRUPT SYSTEM ON?
YES
NO
SFS INSTRUCTION ISSUED?
YES
NO
25
SFS SIGNAL TRUE?
YES
NO
U27A,B
U25A
U26B
U36B
U66A,B
SET IRQ FF (T5)
CC
U16A
U37D
U36A
SEND SKF SIGNAL TO COMPUTER
CC
U17A,B
SEND FLGL AND IRQL SIGNALS TO COMPUTER
CC
10
IAK SIGNAL TRUE?
YES
NO
U35B
U45A
CLEAR FLAG BUFFER FF
CC
U27A,B
CLEAR IRQ FF (T2)
CC
OPERATION COMPLETE
2121-9



NOTES:

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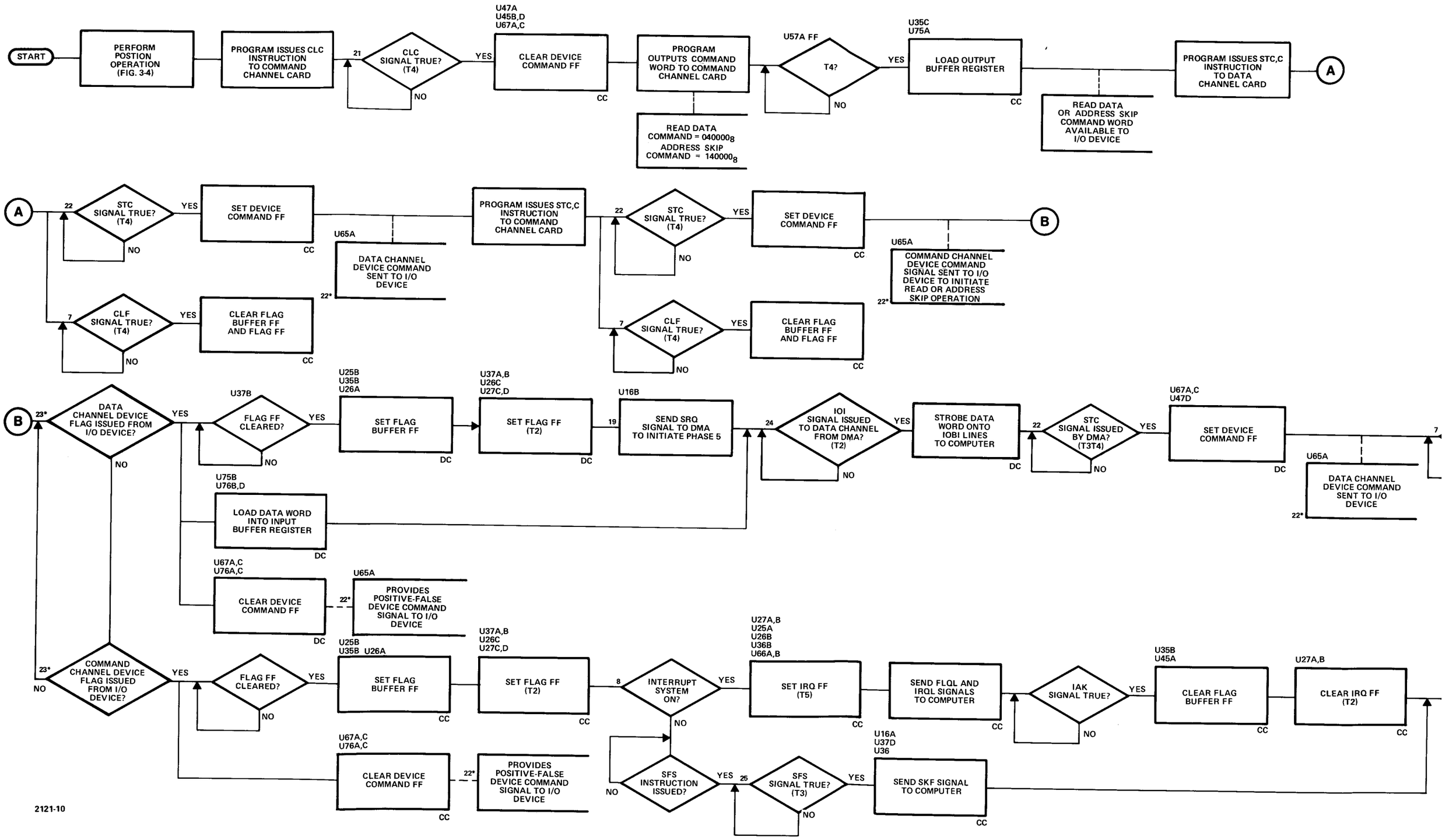
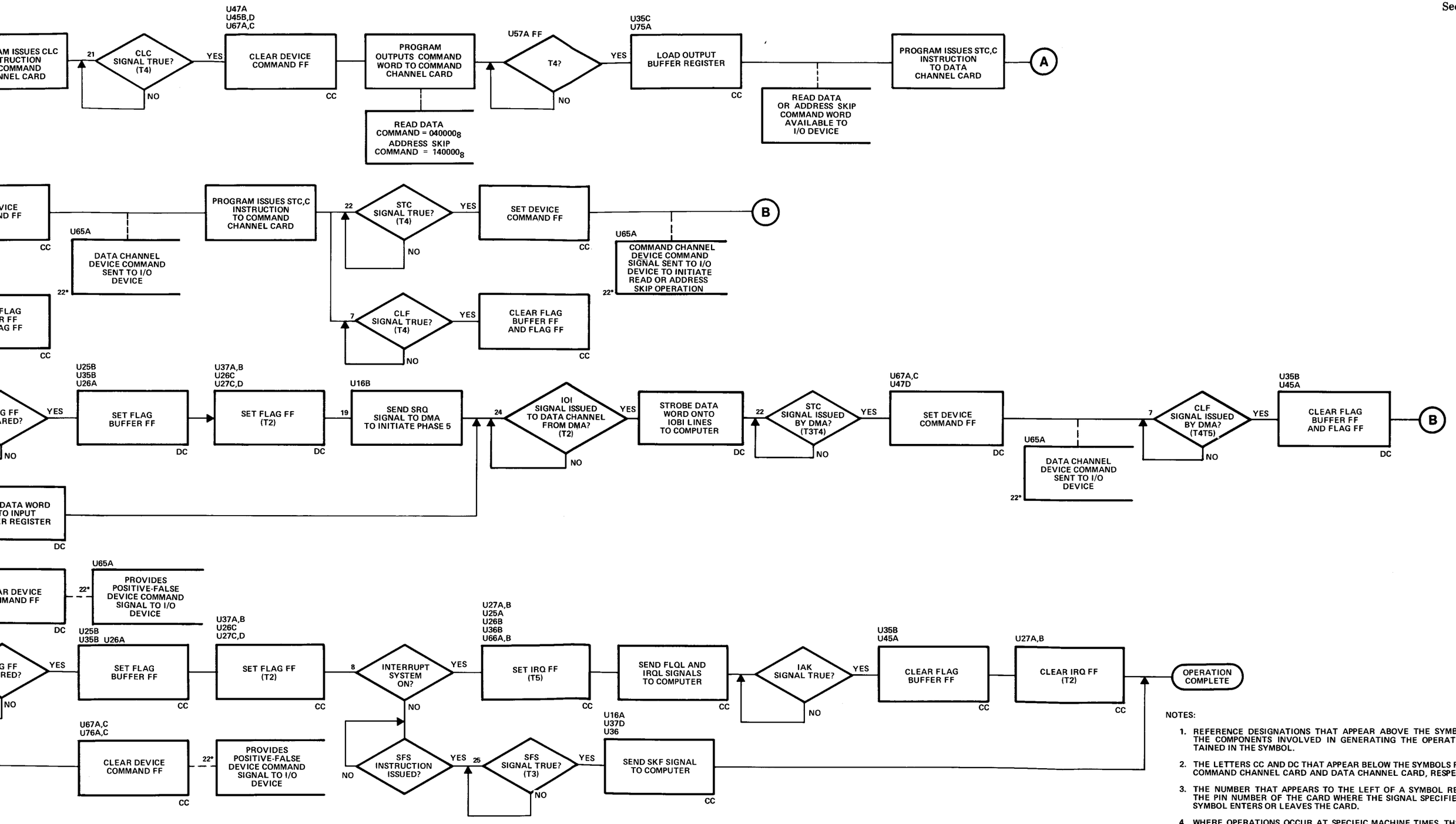
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-5. Write Data and Write Address Operations, Flow Diagram

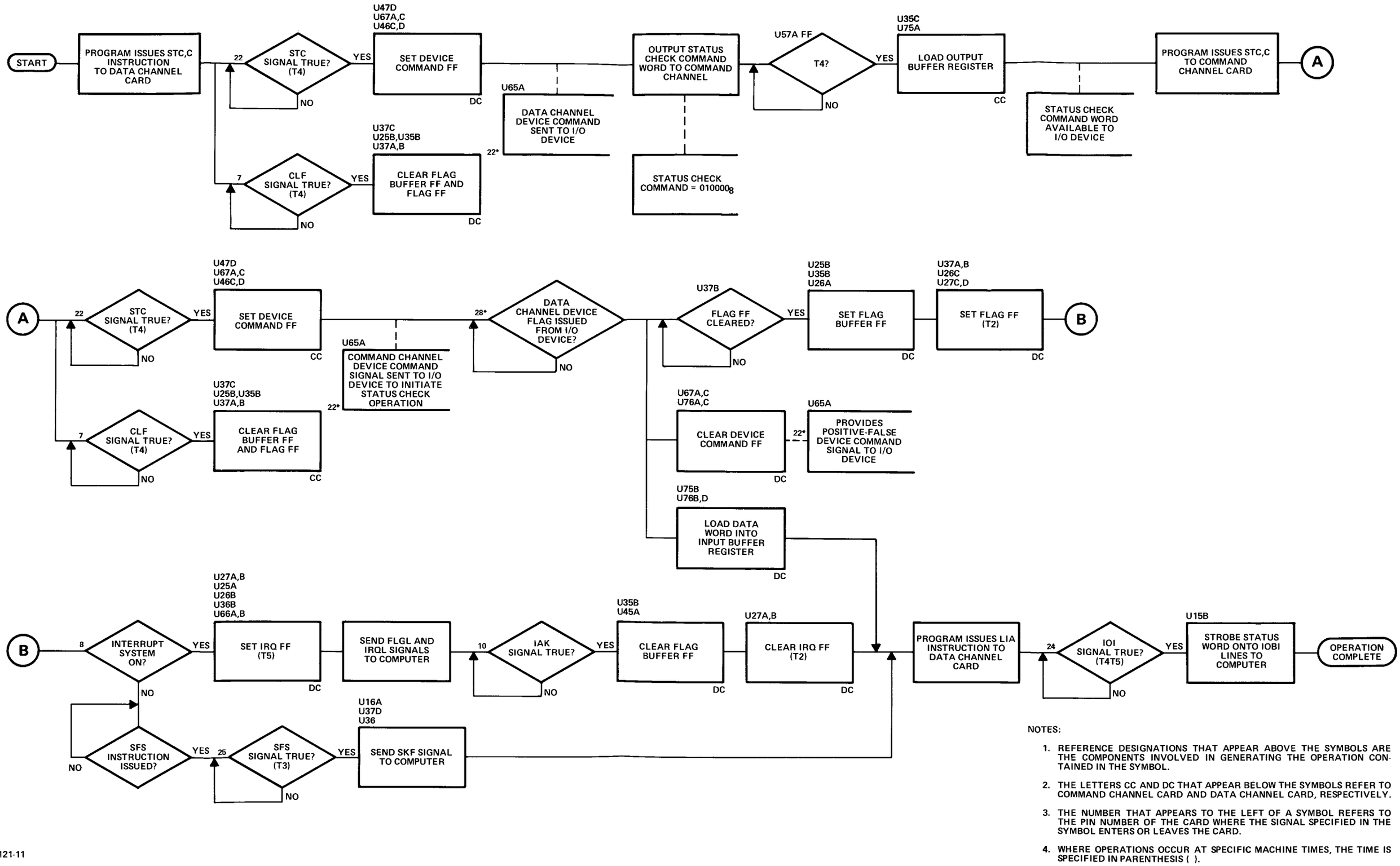

START
PERFORM POSTION OPERATION (FIG. 3-4)
PROGRAM ISSUES CLC INSTRUCTION TO COMMAND CHANNEL CARD
21
CLC SIGNAL TRUE? (T4)
NO
YES
U47A U45B,D U67A,C
CLEAR DEVICE COMMAND FF
CC
PROGRAM OUTPUTS COMMAND WORD TO COMMAND CHANNEL CARD
READ DATA COMMAND = 040000₈ ADDRESS SKIP COMMAND = 140000₈
U57A FF
T4?
NO
YES
U35C U75A
LOAD OUTPUT BUFFER REGISTER
CC
READ DATA OR ADDRESS SKIP COMMAND WORD AVAILABLE TO I/O DEVICE
PROGRAM ISSUES STC,C INSTRUCTION TO DATA CHANNEL CARD
A
A
22
STC SIGNAL TRUE? (T4)
NO
YES
SET DEVICE COMMAND FF
CC
U65A
DATA CHANNEL DEVICE COMMAND SENT TO I/O DEVICE
22*
PROGRAM ISSUES STC,C INSTRUCTION TO COMMAND CHANNEL CARD
22
STC SIGNAL TRUE? (T4)
NO
YES
SET DEVICE COMMAND FF
CC
U65A
COMMAND CHANNEL DEVICE COMMAND SIGNAL SENT TO I/O DEVICE TO INITIATE READ OR ADDRESS SKIP OPERATION
22*
B
7
CLF SIGNAL TRUE? (T4)
NO
YES
CLEAR FLAG BUFFER FF AND FLAG FF
CC
7
CLF SIGNAL TRUE? (T4)
NO
YES
CLEAR FLAG BUFFER FF AND FLAG FF
CC
B
23*
DATA CHANNEL DEVICE FLAG ISSUED FROM I/O DEVICE?
NO
YES
U37B
FLAG FF CLEARED?
NO
YES
U25B U35B U26A
SET FLAG BUFFER FF
DC
U37A,B U26C U27C,D
SET FLAG FF (T2)
DC
U16B
19
SEND SRQ SIGNAL TO DMA TO INITIATE PHASE 5
24
IOI SIGNAL ISSUED TO DATA CHANNEL FROM DMA? (T2)
NO
YES
STROBE DATA WORD ONTO IOBI LINES TO COMPUTER
DC
22
STC SIGNAL ISSUED BY DMA? (T3T4)
NO
YES
U67A,C U47D
SET DEVICE COMMAND FF
DC
U65A
DATA CHANNEL DEVICE COMMAND SENT TO I/O DEVICE
22*
7
U75B U76B,D
LOAD DATA WORD INTO INPUT BUFFER REGISTER
DC
U67A,C U76A,C
CLEAR DEVICE COMMAND FF
DC
22*
U65A
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
23*
COMMAND CHANNEL DEVICE FLAG ISSUED FROM I/O DEVICE?
NO
YES
FLAG FF CLEARED?
NO
YES
U25B U35B U26A
SET FLAG BUFFER FF
CC
U37A,B U26C U27C,D
SET FLAG FF (T2)
CC
8
INTERRUPT SYSTEM ON?
NO
YES
U27A,B U25A U26B U36B U66A,B
SET IRQ FF (T5)
CC
SEND FLQL AND IRQL SIGNALS TO COMPUTER
CC
IAK SIGNAL TRUE?
NO
YES
U35B U45A
CLEAR FLAG BUFFER FF
CC
U27A,B
CLEAR IRQ FF (T2)
CC
U67A,C U76A,C
CLEAR DEVICE COMMAND FF
CC
22*
PROVIDES POSITIVE-FALSE DEVICE COMMAND SIGNAL TO I/O DEVICE
SFS INSTRUCTION ISSUED?
NO
YES
25
SFS SIGNAL TRUE? (T3)
NO
YES
U16A U37D U36
SEND SKF SIGNAL TO COMPUTER
CC
2121-10



NOTES:

1. REFERENCE DESIGNATIONS THAT APPEAR ABOVE THE SYMBOLS ARE THE COMPONENTS INVOLVED IN GENERATING THE OPERATION CONTAINED IN THE SYMBOL.
2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY.
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-6. Read Data and Address Skip Operations, Flow Diagram



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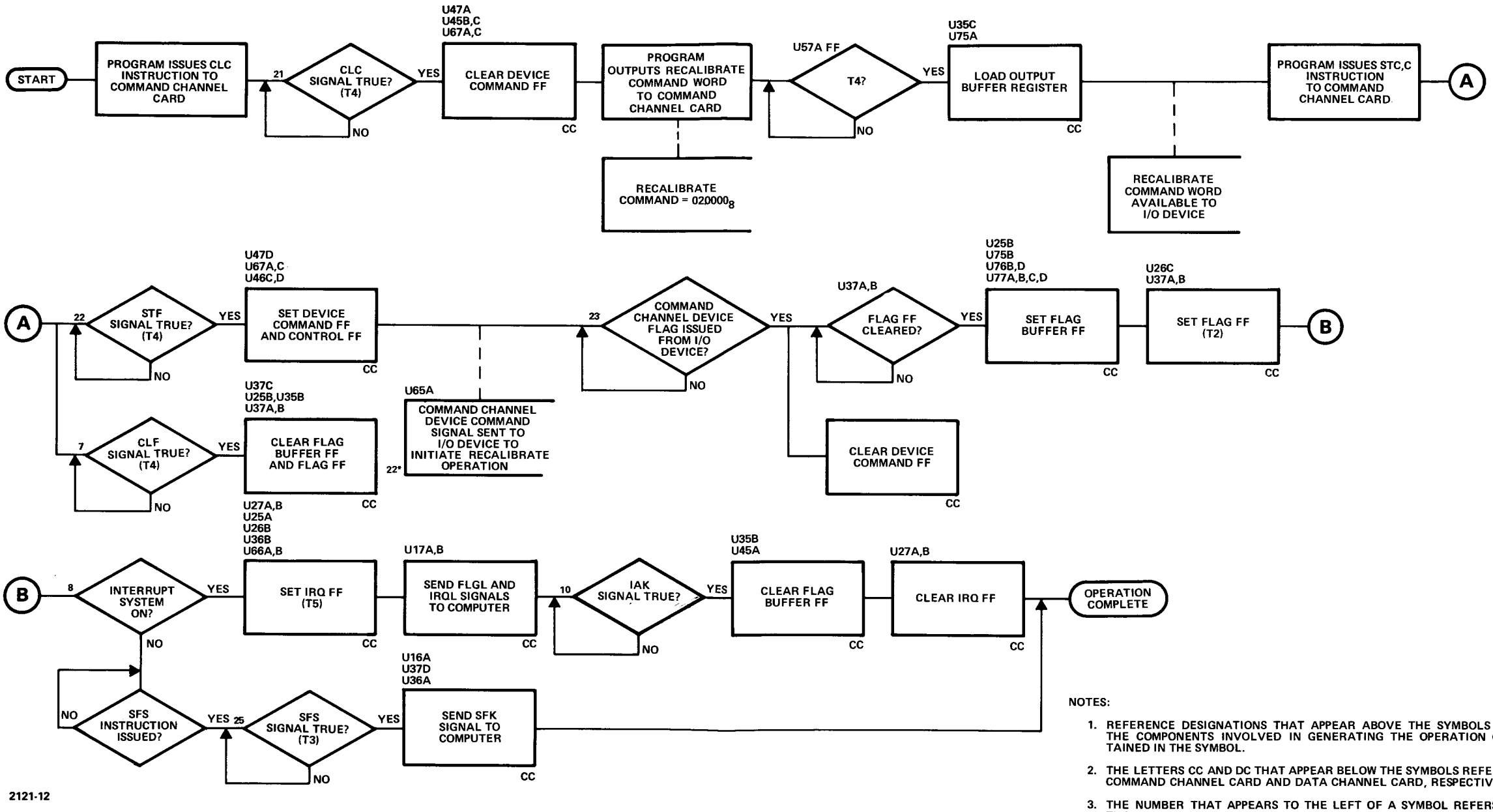
NOTES:

1. REFERENCE DESIGNATIONS THAT APPEAR ABOVE THE SYMBOLS ARE THE COMPONENTS INVOLVED IN GENERATING THE OPERATION CONTAINED IN THE SYMBOL.
2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY.
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

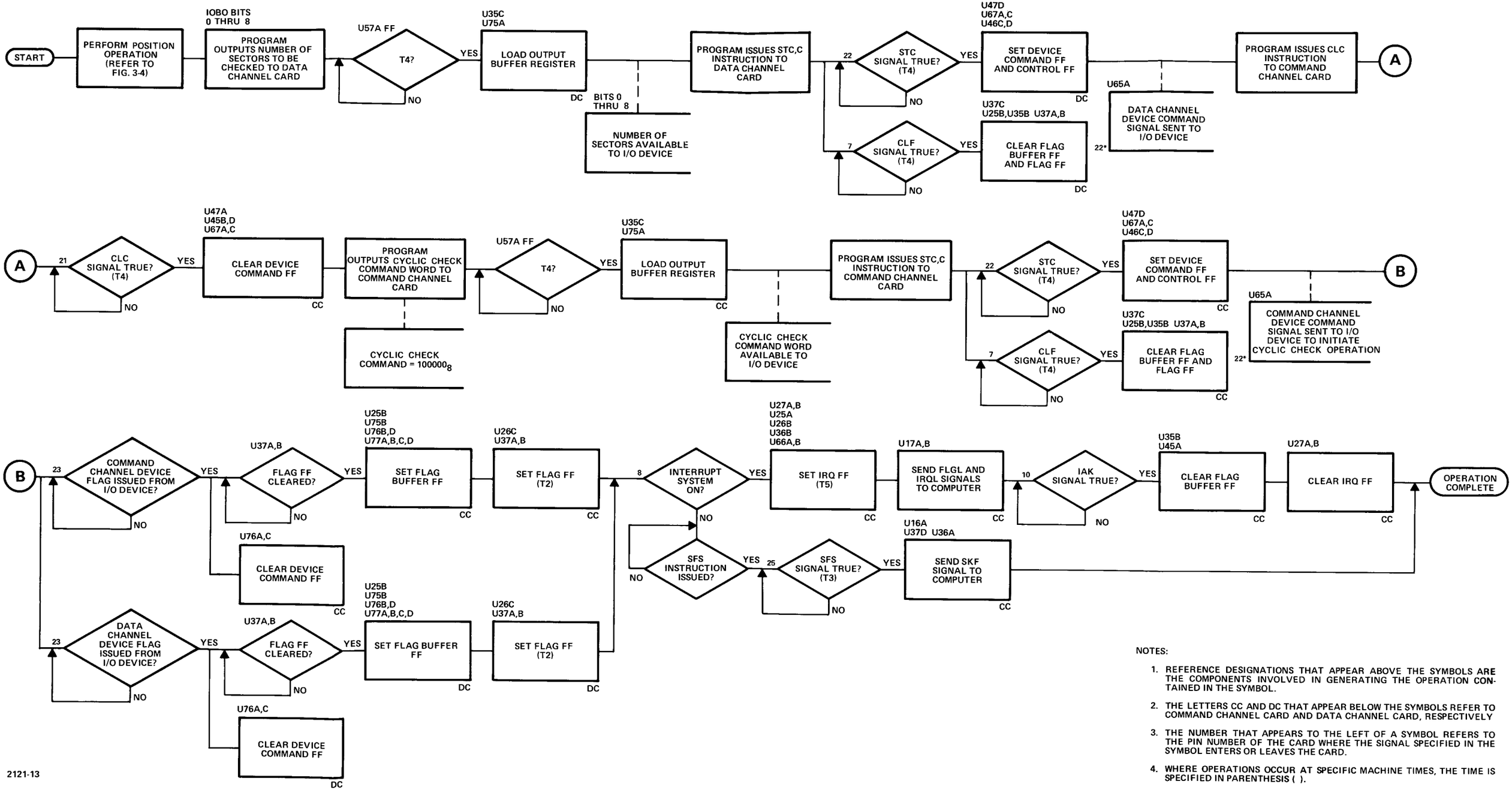
Figure 3-7. Status Check Operation, Flow Diagram



NOTES:

1. REFERENCE DESIGNATIONS THAT APPEAR ABOVE THE SYMBOLS ARE THE COMPONENTS INVOLVED IN GENERATING THE OPERATION CONTAINED IN THE SYMBOL.
2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY.
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.

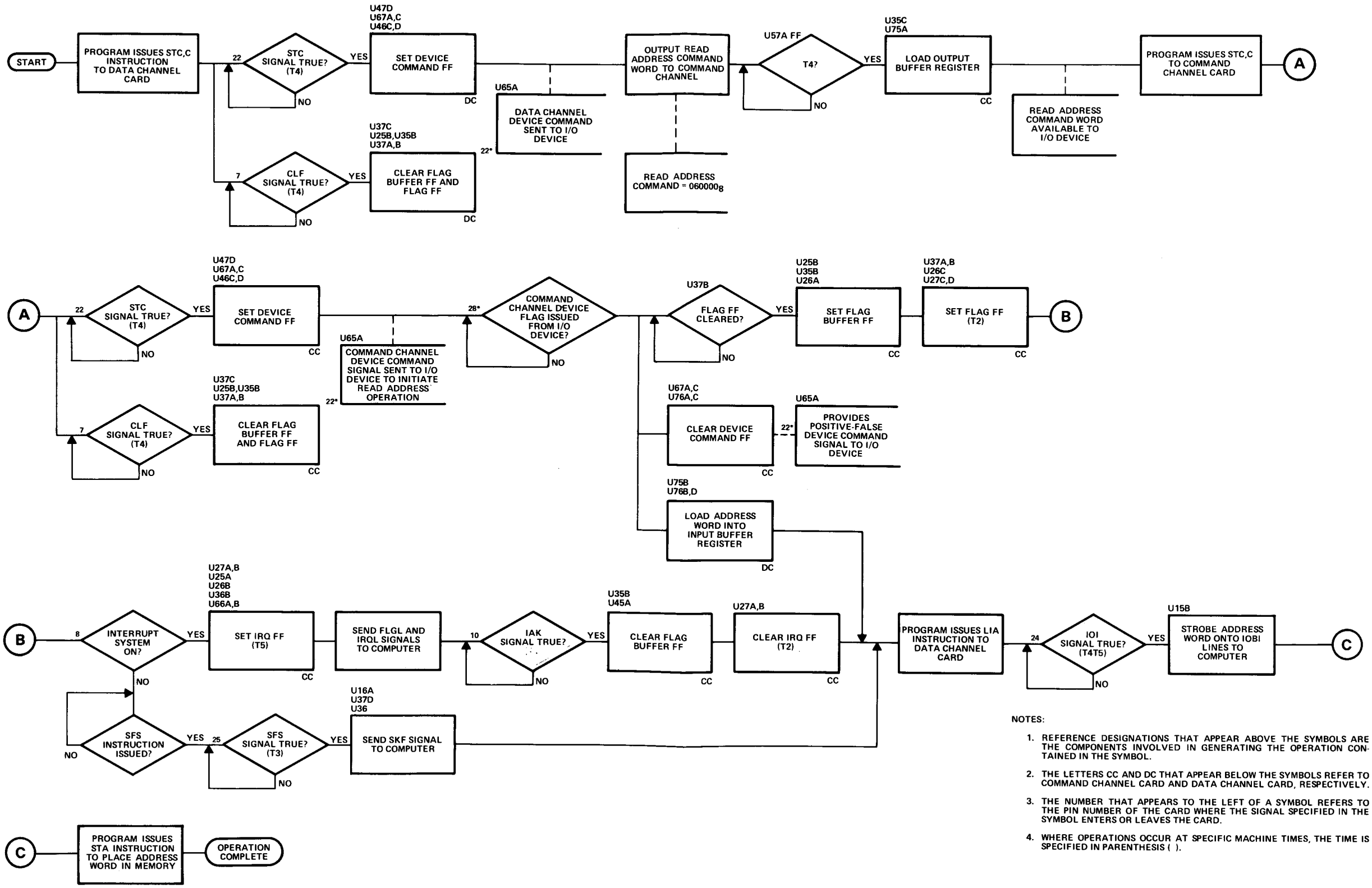
Figure 3-8. Recalibrate Operation, Flow Diagram



NOTES:

1. REFERENCE DESIGNATIONS THAT APPEAR ABOVE THE SYMBOLS ARE THE COMPONENTS INVOLVED IN GENERATING THE OPERATION CONTAINED IN THE SYMBOL.
2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

Figure 3-9. Cyclic Check Operation, Flow Diagram



NOTES:

1. REFERENCE DESIGNATIONS THAT APPEAR ABOVE THE SYMBOLS ARE THE COMPONENTS INVOLVED IN GENERATING THE OPERATION CONTAINED IN THE SYMBOL.
2. THE LETTERS CC AND DC THAT APPEAR BELOW THE SYMBOLS REFER TO COMMAND CHANNEL CARD AND DATA CHANNEL CARD, RESPECTIVELY.
3. THE NUMBER THAT APPEARS TO THE LEFT OF A SYMBOL REFERS TO THE PIN NUMBER OF THE CARD WHERE THE SIGNAL SPECIFIED IN THE SYMBOL ENTERS OR LEAVES THE CARD.
4. WHERE OPERATIONS OCCUR AT SPECIFIC MACHINE TIMES, THE TIME IS SPECIFIED IN PARENTHESIS ( ).

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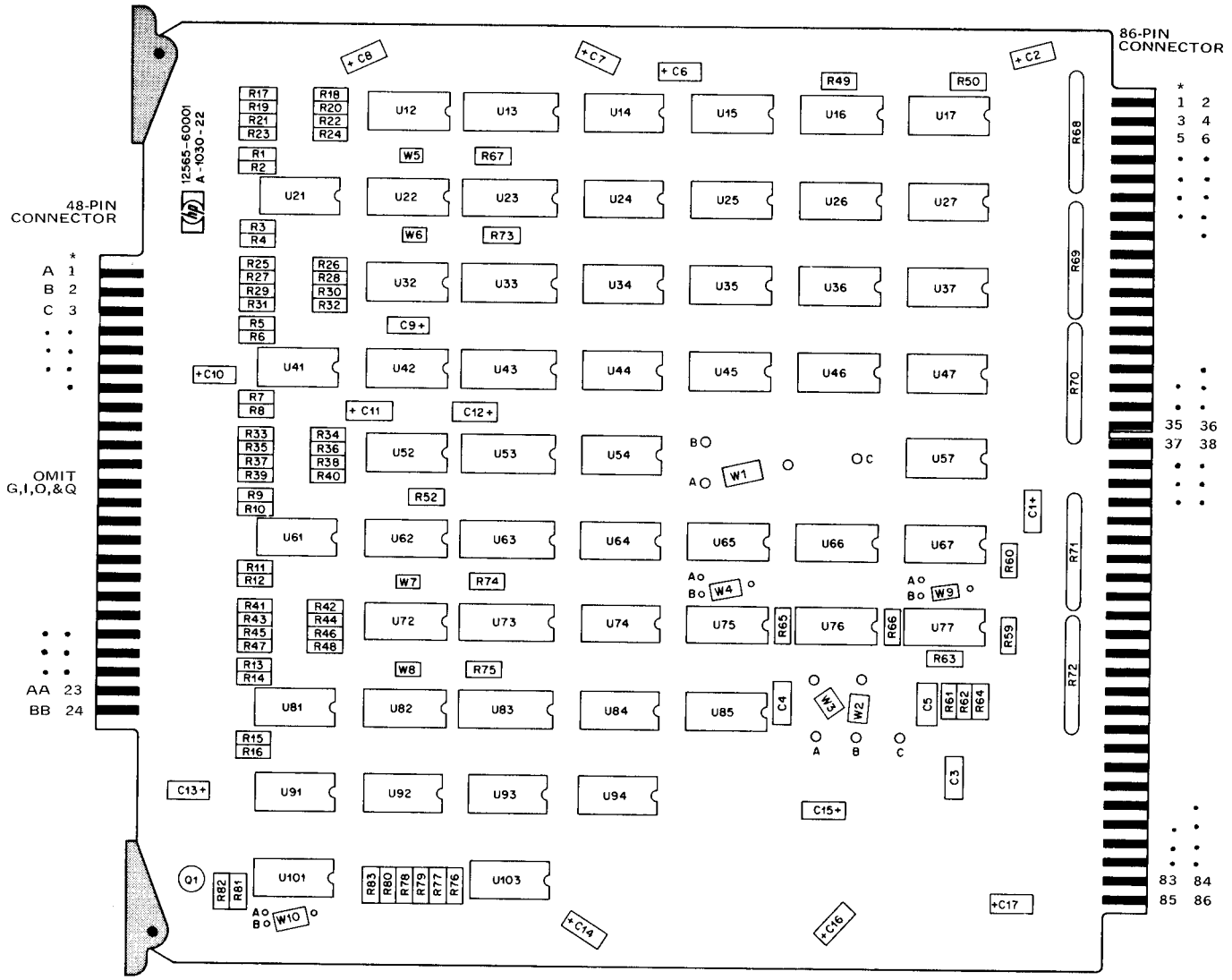
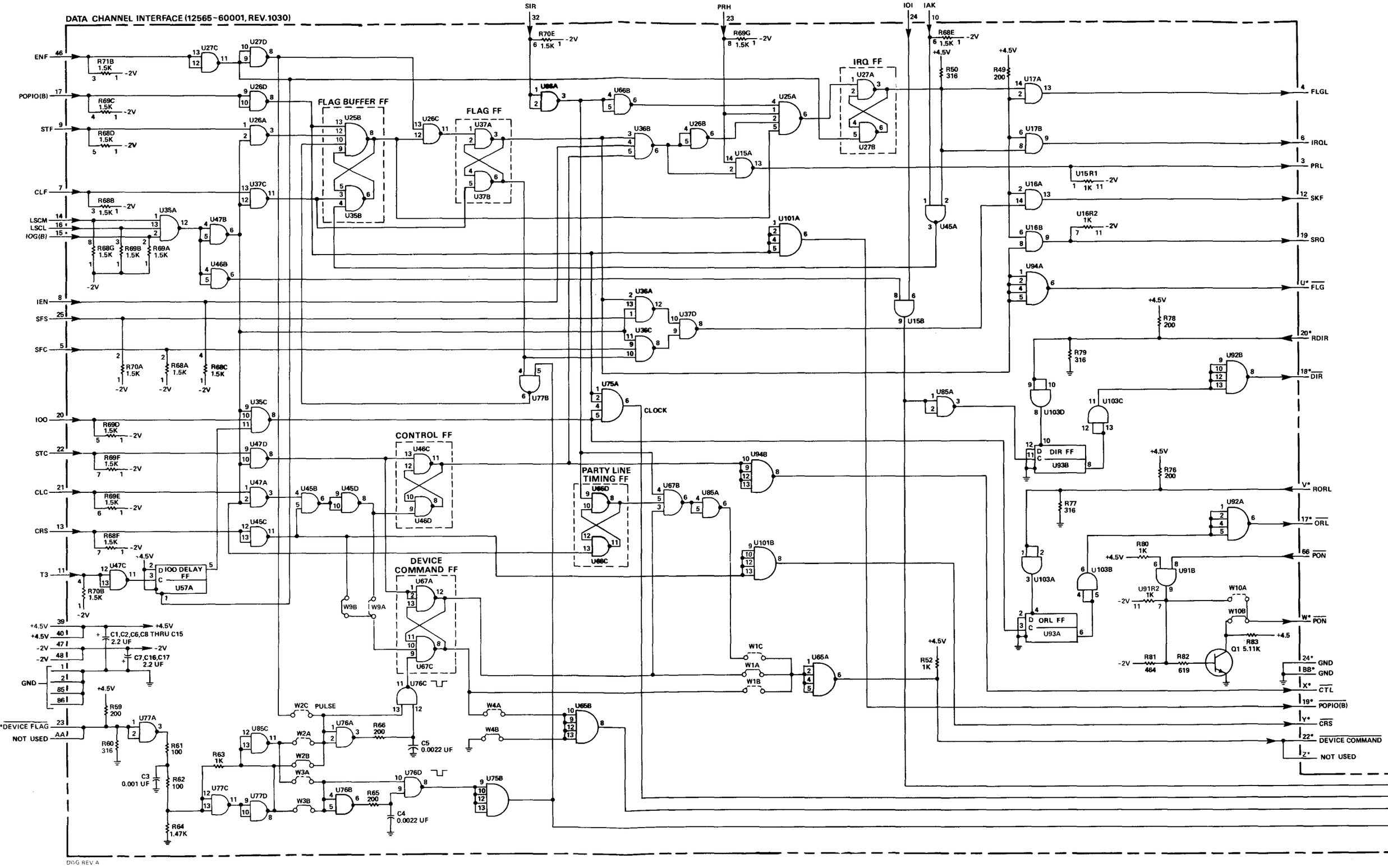
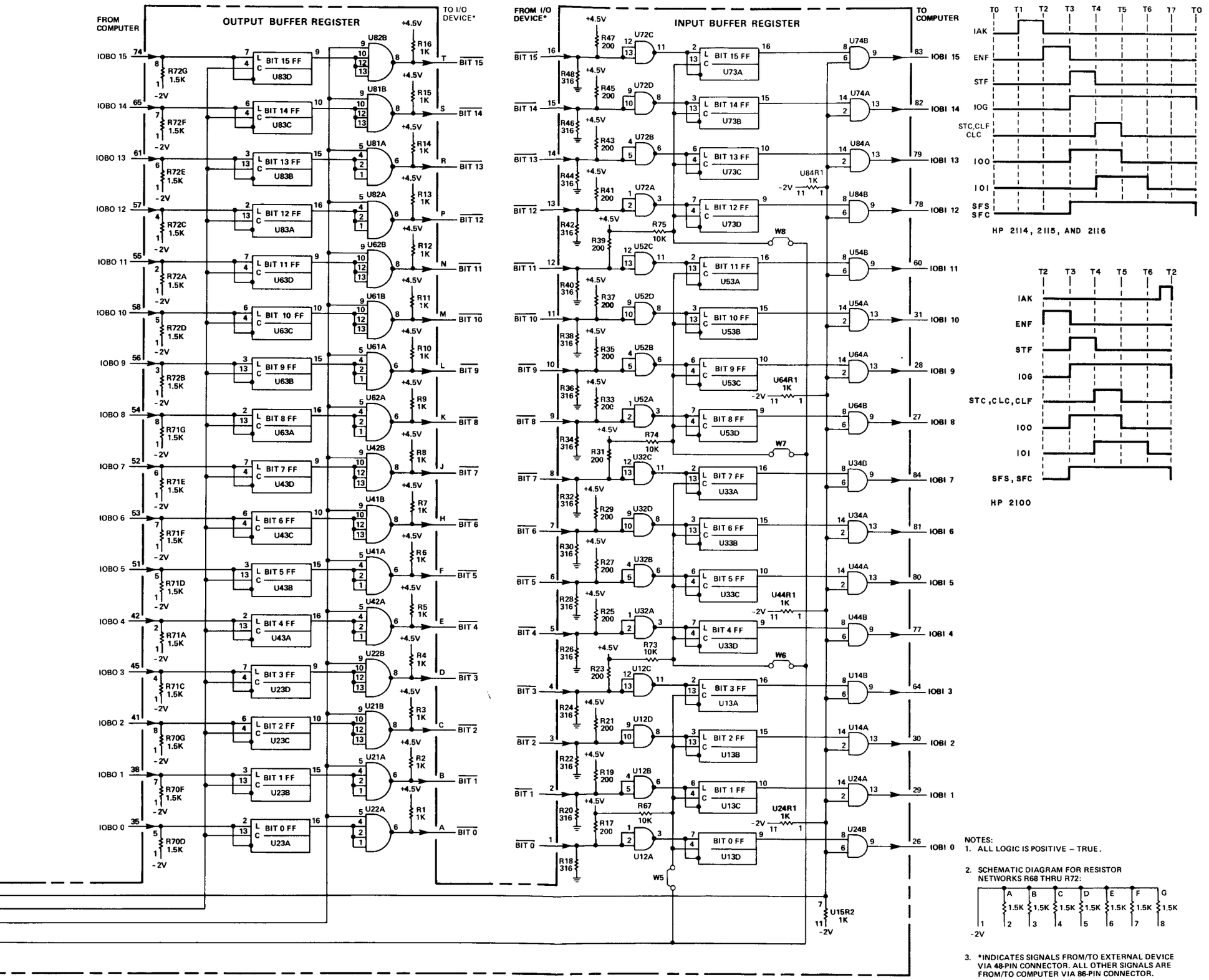
Figure 3-10. Read Address Operation, Flow Diagram



*DENOTES COMPONENT SIDE OF CARD FOR 48- AND 86-PIN CONNECTOR DESIGNATIONS.


DATA CHANNEL INTERFACE (12565-60001, REV. 1030)
SIR
PRH
IOI
IAK
ENF
POPIO(B)
STF
CLF
LSCM
LSCL
IOG(B)
IEN
SFS
SFC
IOO
STC
CLC
CRS
T3
*DEVICE FLAG
NOT USED
GND
FLAG BUFFER FF
FLAG FF
IRQ FF
CONTROL FF
PARTY LINE TIMING FF
DEVICE COMMAND FF
IOO DELAY FF
DIR FF
ORL FF
CLOCK
PULSE
C1,C2,C6,C8 THRU C15 2.2 UF
C7,C16,C17 2.2 UF
C3 0.001 UF
C4 0.0022 UF
C5 0.0022 UF
+4.5V
-2V
FLGL
IRQL
PRL
SKF
SRQ
U* FLG
RDIR
DIR
V* RORL
17* ORL
66 PON
W* PON
24* GND
BB* GND
X* CTL
19* POPIO(B)
Y* CRS
22* DEVICE COMMAND
Z* NOT USED
DWG REV A



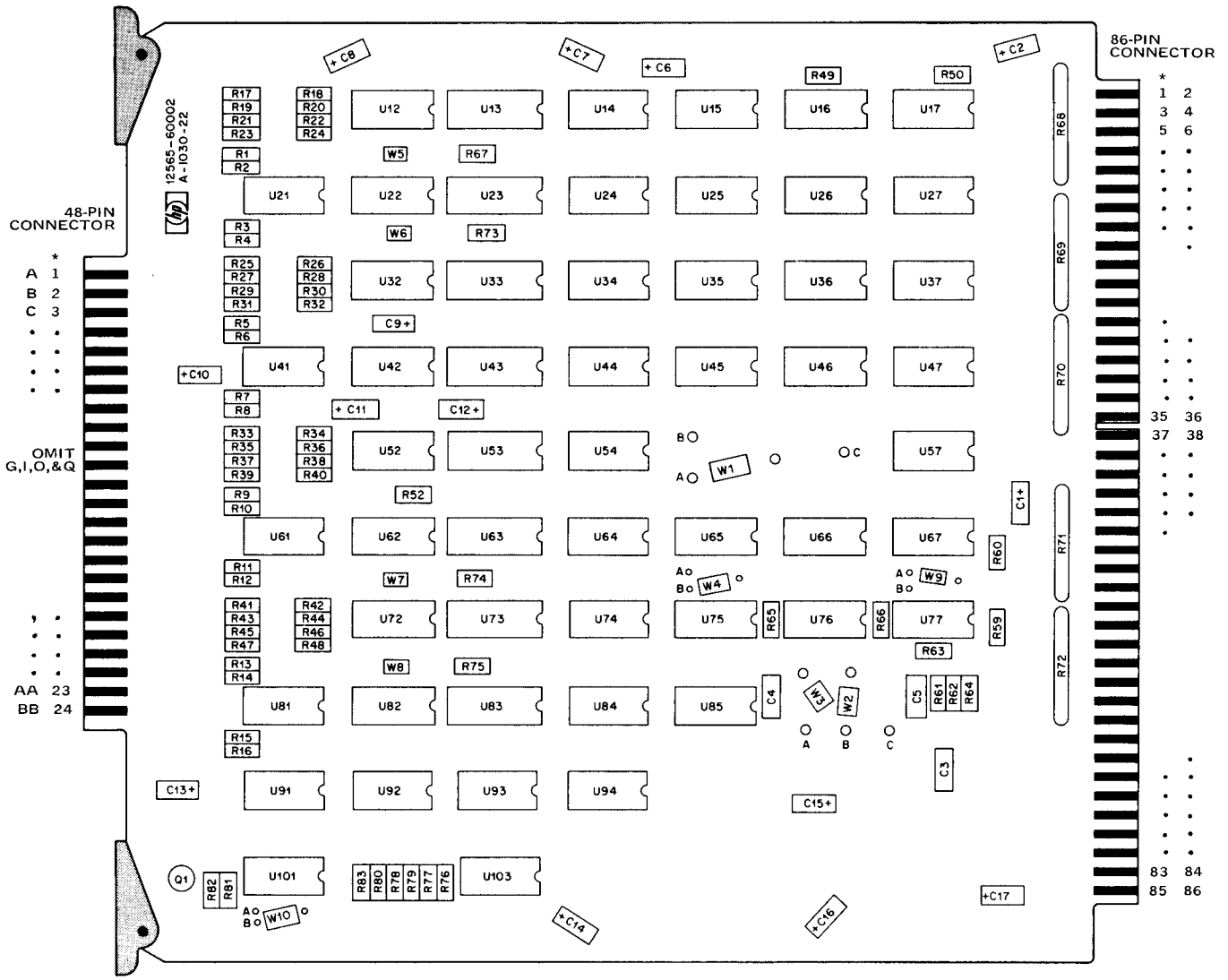
NOTES:
1. ALL LOGIC IS POSITIVE – TRUE.
2. SCHEMATIC DIAGRAM FOR RESISTOR NETWORKS R68 THRU R72:

3. *INDICATES SIGNALS FROM/TO EXTERNAL DEVICE VIA 48-PIN CONNECTOR. ALL OTHER SIGNALS ARE FROM/TO COMPUTER VIA 86-PIN CONNECTOR.

Figure 4-1. Data Channel Card (12565-60001), Schematic and Parts Location Diagrams

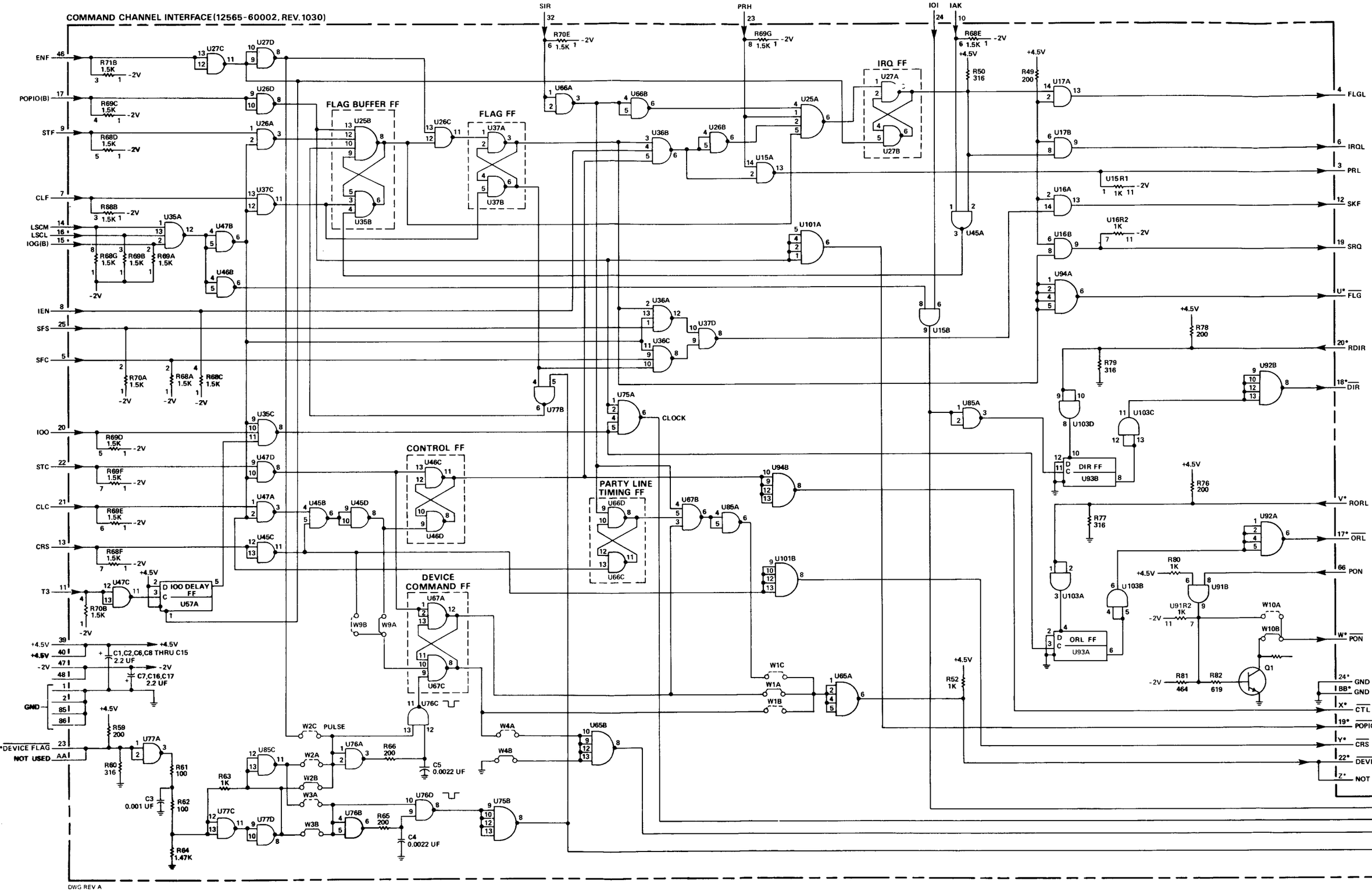
Table 4-4. Command Channel Card (12565-60002), Replaceable Parts

REFERENCE DESIGNATION	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.
C1,2,C6 thru C17	0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	28480	0180-0197
C3	0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153
C4,5	0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154
Q1	1854-0094	Transistor, Si, NPN	07263	2N3646
R1 thru R16,52,63,80	0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F
R17,19,21,23,25,27,29,31,33,35, 37,39,41,43,45,47,49,59,65, 66,67,78	0757-0407	Resistor, Fxd, Flm, 200 ohms, 1%, 1/8W	14674	MF4CD2000F
R18,20,22,24,26,28,30,32,34,36, 38,40,42,44,46,48,50,60, 77,79	0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F
R61,62	0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	14674	MF4CD1000F
R64	0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	28480	0757-1094
R67,R73 thru R75	0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	14674	MF4CD1002F
R68 thru R72	1810-0020	Resistor Network, (7 fxd flm resistors)	28480	1810-0020
R81	0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	19701	MF4CD4640F
R82	0757-0418	Resistor, Fxd, Flm, 619 ohms, 1%, 1/8W	14674	MF4CD6190F
R83	0757-0438	Resistor, Fxd, Flm, 5.11k, 1%, 1/8W	14674	MF4CD5111F
U12,26,27,32,37,U45 thru U47, 52,66,72,76,77,85	1820-0054	Integrated Circuit, TTL	01295	SN4343
U13,23,33,43,53,63,73,83	1820-0301	Integrated Circuit, TTL	01295	SN4463
U14 thru U17,34,44,54,64,74, 84,91	1820-0956	Integrated Circuit, CTL	07263	SL3459
U21,22,41,42,61,62,81,82	1820-0348	Integrated Circuit, DTL	01295	SN4506
U25	1820-0069	Integrated Circuit, TTL	56289	USN7420A
U35,36,67	1820-0068	Integrated Circuit, TTL	01295	SN4343
U57,93	1820-0077	Integrated Circuit, TTL	56289	USN7474A
U65,75,92,94	1820-0071	Integrated Circuit, TTL	56289	USN7440A
U101	1820-0140	Integrated Circuit, TTL	04713	SC7513PK
U103	1820-0141	Integrated Circuit, TTL	04713	SC7514PK
W1 thru W10	8159-0005	Jumper Wire	28480	8159-0005



*DENOTES COMPONENT SIDE OF CARD FOR 48- AND 86-PIN CONNECTOR DESIGNATIONS.

COMMAND CHANNEL INTERFACE (12565-60002, REV. 1030)



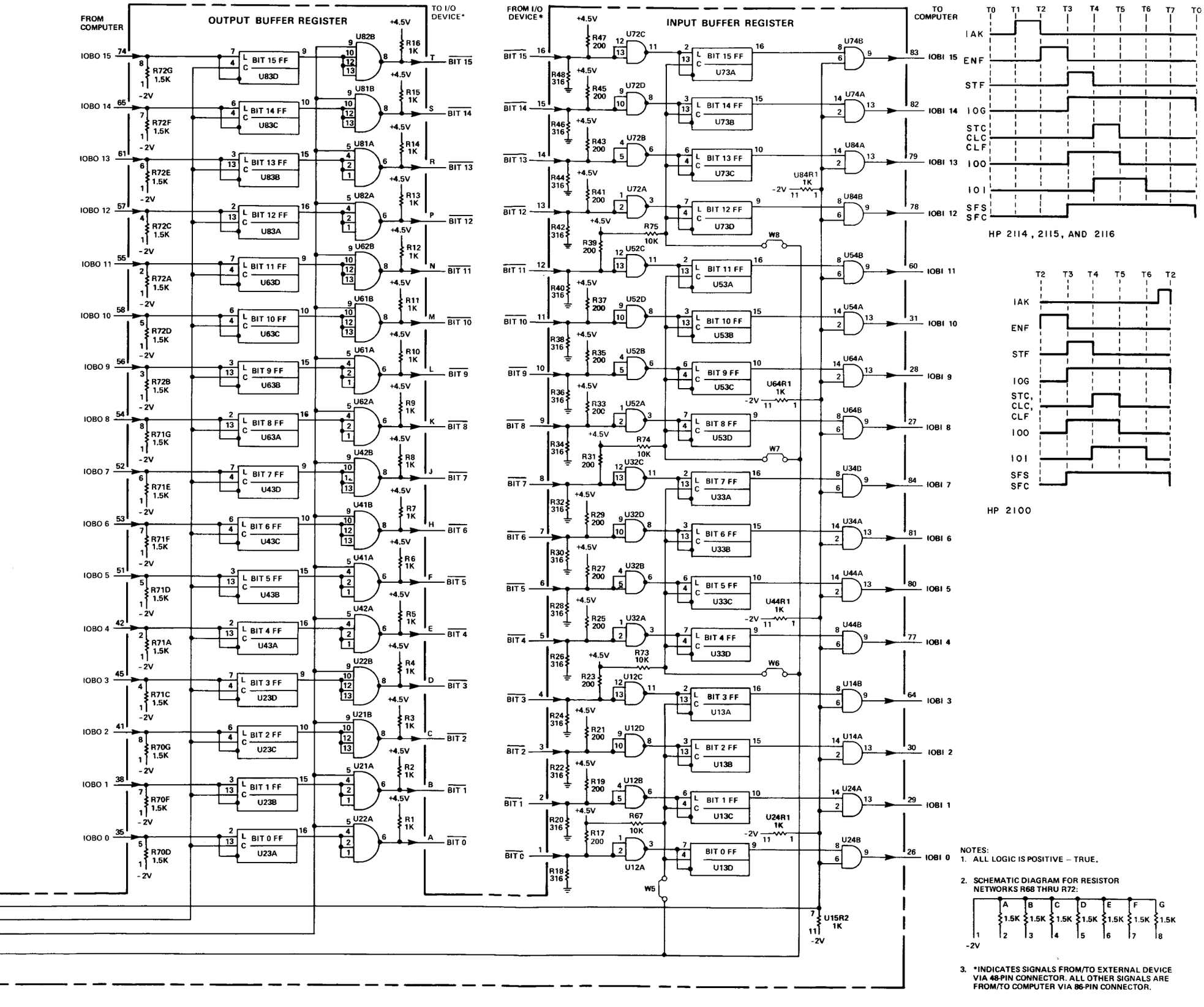


Figure 4-2. Command Channel Card (12565-60002), Schematic and Parts Location Diagrams

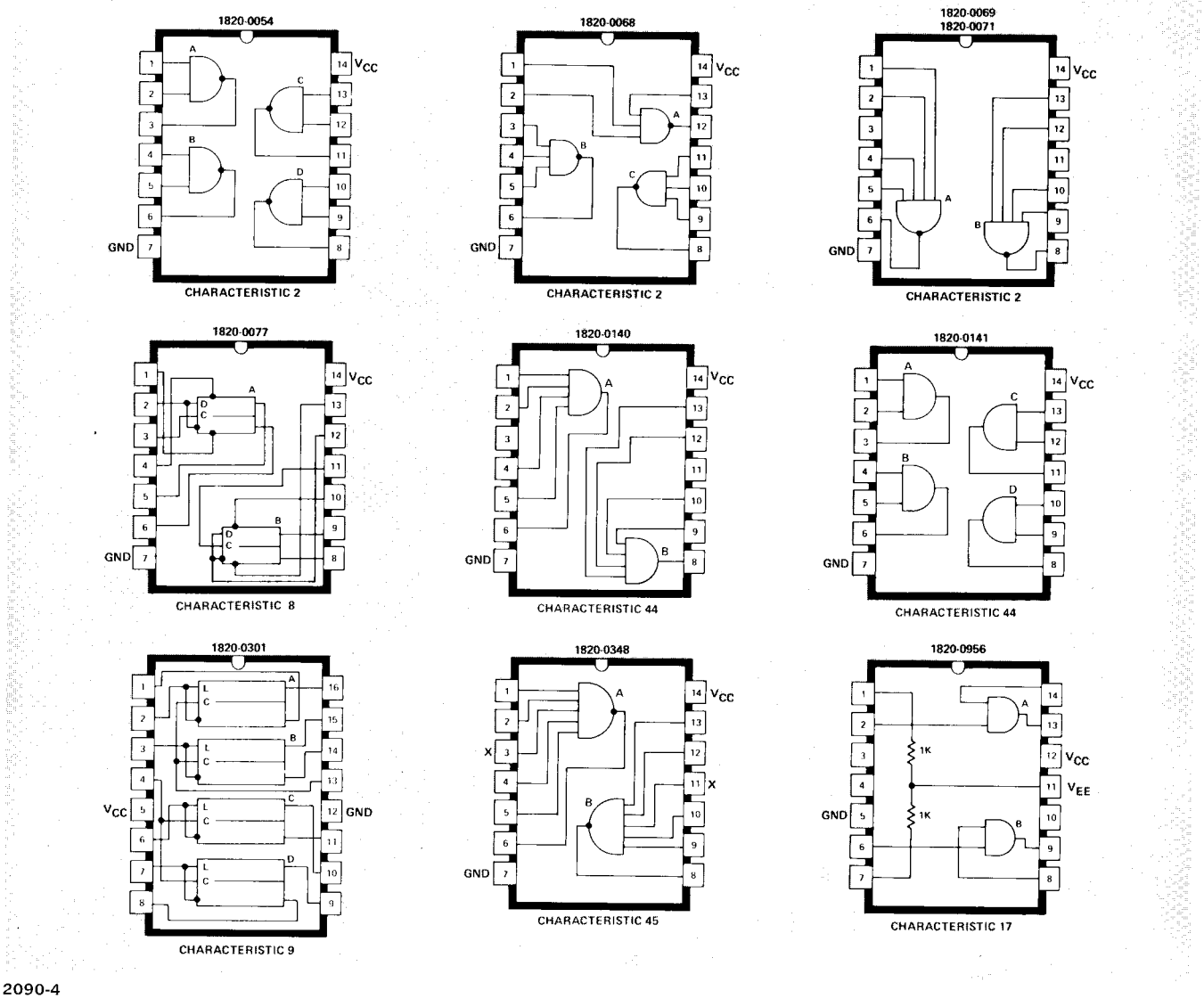


Figure 4-3. Integrated Circuit Diagrams

Table 4-5. Integrated Circuit Characteristics

CHARACTERISTIC	INPUT LEVEL		OUTPUT LEVEL		OPEN INPUT ACTS AS:	PROPAGATION DELAY (MAX)	
	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)	LOGIC 1 (VOLTS, MIN)	LOGIC 0 (VOLTS, MAX)		TO LOGIC 1 (NANOSECONDS)	TO LOGIC 0 (NANOSECONDS)
2	+2.0	+0.8	+2.4	+0.4	Logic 1	29	15
8	+2.0	+0.8	+2.4	+0.4	Logic 1	35	50
9	+2.0	+0.8	+2.4	+0.4	Logic 1	40	25
17	+1.25	+0.5	+2.25	-0.36	Logic 0	18	18
44	+1.8	+1.1	+2.5	+0.4	Logic 1	15	15
45	+2.0	+1.1	Note 1	+0.5	Logic 1	50	35

NOTE:

1. Depends on load.

SECTION V

REPLACEABLE PARTS

5-1. INTRODUCTION.

5-2. This section contains information for ordering replacement parts for the disc interface kit. Table 5-1 lists the parts of the cable assembly called out in figure 5-1. Table 5-2 is a total quantity listing of all replaceable parts in the interface kit, and the parts are listed in numerical order by HP part number. Tables 5-1 and 5-2 list the following information for each part:

a. Description of the part. (Refer to table 5-4 for an explanation of abbreviations and reference designations used in the DESCRIPTION column.)

b. Typical manufacturer of the part in a five-digit code; refer to list of manufacturers in table 5-3.

c. Manufacturer's part number.

d. Total quantity of each part used in the interface kit.

5-3. A separate parts list is provided along with the parts location diagram for each disc interface card in section IV of this manual. These parts lists present the parts in alphanumeric order by reference designation.

5-4. ORDERING INFORMATION.

5-5. To order replacement parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office. (Refer to the list at the end of this manual for addresses.) Specify the following information for each part ordered:

a. Instrument model and serial number.

b. Hewlett-Packard stock number for each part.

c. Description of each part.

d. Circuit reference designation.

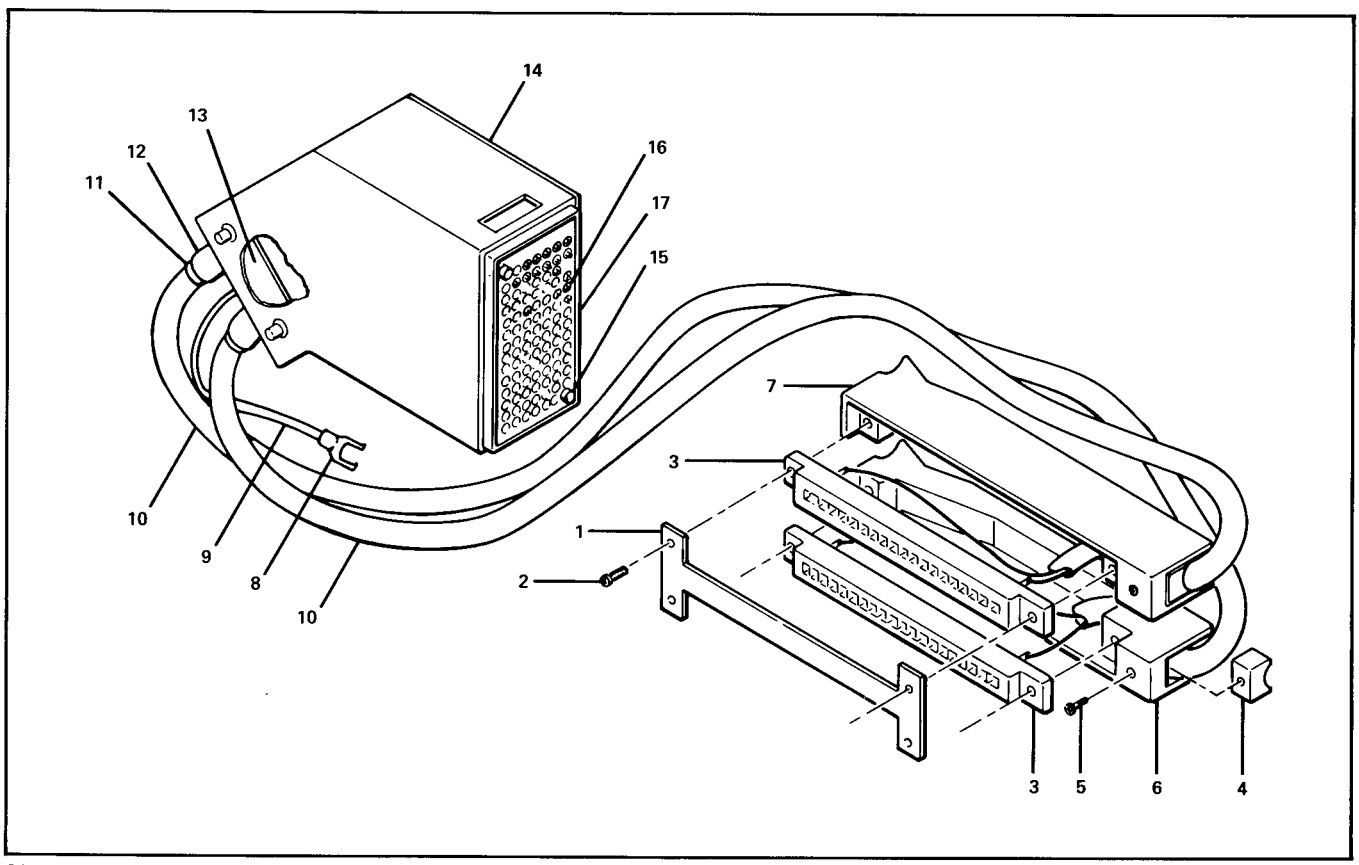


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Figure 5-1. Cable Assembly, Exploded View

Table 5-1. Cable Assembly Replaceable Parts

FIG. & INDEX NO.	HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	UNITS PER ASSY
5-1-	12565-60003	Cable Assembly	28480	12565-60003	1
1	02116-0081	* Brace, Double Connector	28480	02116-0081	1
		(Attaching Parts)			
2	0624-0098	* Screw, Machine, pozi, No. 4-40, 7/16 in.	00000	OBD	4
		– – – x – – –			
3	1251-0335	* Connector, Receptacle, PC, 48 pin	95238	K600-13-PCGD-24	2
4	5040-6003	* Cable Clamp	28480	5040-6003	2
		(Attaching Parts)			
5	3030-0143	* Setscrew, No. 6-32, 1/2 in.	00000	OBD	2
		– – – x – – –			
6	5020-7331	* Hood, Dual, Right	28480	5020-7331	1
7	5020-7332	* Hood, Dual, Left	28480	5020-7332	1
8	0362-0127	* Terminal Lug, 12-10 AWG	00000	OBD	1
9	8150-1899	* Wire, 12 AWG	00000	OBD	7-½ in.
10	8120-1416	* Cable, 36 twisted pair	28480	8120-1416	30-ft.
11	1251-0171	* Bushing, No. 8	98825	18220-1	2
12	1251-0170	* Bushing, No. 10	98825	18220-10	2
13	12565-00001	* Cable Clamp	28480	12565-00001	1
		(Attaching Parts)			
	2680-0107	* Screw, Machine, PH, No. 10-32, 3/4 in.	00000	OBD	2
14	1600-0205	* Strain Relief	28480	1600-0205	1
15	1251-2523	* Guide Pin, Female	28480	1251-2523	2
16	1251-2625	* Socket	28480	1251-2625	48
17	1251-1690	* Connector Block	28480	1251-1690	1

Table 5-2. Disc Interface Kit Replaceable Parts

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
0160-0153	Capacitor, Fxd, My, 1000 pF, 10%, 200 VDCW	28480	0160-0153	2
0160-0154	Capacitor, Fxd, My, 2200 pF, 10%, 200 VDCW	28480	0160-0154	4
0180-0197	Capacitor, Fxd, Elect, 2.2 uF, 10%, 20 VDCW	28480	0180-0197	28
0362-0127	Terminal Lug, 12-10 AWG	00000	OBD	1
0624-0098	Screw, Machine, pozi, No. 4-40, 7/16 in.	00000	OBD	4
0698-0082	Resistor, Fxd, Flm, 464 ohms, 1%, 1/8W	19701	MF4CD4640F	2
0698-3444	Resistor, Fxd, Flm, 316 ohms, 1%, 1/8W	19701	MF4CD3160F	40
0757-0280	Resistor, Fxd, Flm, 1k, 1%, 1/8W	14674	MF4CD1001F	38
0757-0401	Resistor, Fxd, Flm, 100 ohms, 1%, 1/8W	14674	MF4CD1000F	4
0757-0407	Resistor, Fxd, Flm, 200 ohms, 1%, 1/8W	14674	MF4CD2000F	44
0757-0418	Resistor, Fxd, Flm, 619 ohms, 1%, 1/8W	14674	MF4CD6190F	2
0757-0438	Resistor, Fxd, Flm, 5.1k, 1%, 1/8W	14674	MF4CD5111F	2
0757-0442	Resistor, Fxd, Flm, 10.0k, 1%, 1/8W	14674	MF4CD1002F	8
0757-1094	Resistor, Fxd, Flm, 1.47k, 1%, 1/8W	14674	MF4CD1471F	2
1251-0170	Bushing, rubber, No. 10	98825	18220-10	2
1251-0171	Bushing, rubber, No. 8	98825	18220-1	2
1251-0335	Connector, Receptacle, PC, 48 pin	95238	K600-13-PCGD-24	2
1251-1690	Connector Block	28480	1251-1690	1
1251-2523	Guide Pin, Female	00779	201047-4	2
1251-2524	Guide Pin, Male	00779	201046-4	2
1251-2525	Block, Pin	00779	202799-2	1
1251-2625	Socket	28480	1251-2625	48
1480-0116	Extractor, Pin, PC Card	28480	1480-0116	4
1600-0205	Strain Relief	28480	1600-0205	1
1810-0020	Resistor Network (7 fxd flm resistors)	28480	1810-0020	10
1820-0054	Integrated Circuit, TTL	01295	SN4342	28
1820-0068	Integrated Circuit, TTL	01295	SN4343	6
1820-0069	Integrated Circuit, TTL	56289	USN7420A	2
1820-0071	Integrated Circuit, TTL	56289	USN7440A	8
1820-0077	Integrated Circuit, TTL	56289	USN7474A	4
1820-0140	Integrated Circuit, TTL	04713	SC7513PK	2
1820-0141	Integrated Circuit, TTL	04713	SC7514PK	2
1820-0301	Integrated Circuit, TTL	01295	SN4463	16
1820-0348	Integrated Circuit, DTL	01295	SN4506	16
1820-0956	Integrated Circuit, CTL	07263	SL3459	24
1854-0094	Transistor, Si, NPN	07263	2N3646	2
2680-0107	Screw, Machine, PH, No. 10-32, 3/4 in.	00000	OBD	2
3030-0143	Setscrew, No. 6-32, 1/2 in.	00000	OBD	2
5040-6065	Extractor, PC Card	28480	5040-6065	4
8120-1416	Cable, 36 twisted pair	28480	8120-1416	30 ft.
8150-1899	Wire, 12 AWG	00000	OBD	7-1/2 in.
8159-0005	Jumper Wire	28480	8159-0005	20
02116-0081	Brace, Double Connector	28480	02116-0081	1
5020-7331	Hood, Dual, Right	28480	5020-7331	1
5020-7332	Hood, Dual, Left	28480	5020-7332	1

Table 5-2. Disc Interface Kit Replaceable Parts (Continued)

HP PART NO.	DESCRIPTION	MFR CODE	MFR PART NO.	TQ
5040-6003	Cable Clamp	28480	5040-6003	2
12565-00001	Cable Clamp	28480	12565-00001	1
12565-60001	Circuit Card, Data Channel	28480	12565-60001	1
12565-60002	Circuit Card, Command Channel	28480	12565-60002	1
12565-60003	Cable Assembly	28480	12565-60003	1
12565-90003	12565A Operating and Service Manual	28480	12565-90003	1
12849-60003	PC Connector, Test	28480	12849-60003	1
12849-60004	PC Connector, Test	28480	12849-60004	1

Table 5-3. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their latest supplements.

Code No.	Manufacturer	Address
00779	Amp. Inc.	Harrisburg, Pa.
01295	Texas Instruments, Inc., Transistor Products Div.	Dallas, Texas
04713	Motorola Inc. Semiconductor Products Div.	Phoenix, Arizona
07263	Fairchild Camera & Inst. Corp., Semiconductor Div.	Mountain View, Cal.
14674	Corning Glass Works	Corning, N.Y.
19701	Electra Mfg. Co.	Independence, Kansas
28480	Hewlett-Packard Co.	Palo Alto, Cal.
56289	Sprague Electric Co.	North Adams, Mass.
95238	Continental Connector Corp.	Woodside, N.Y.
98825	Canoga Electronics Corp.	Chatsworth, Cal.

MANUAL PART NO. 12565-90003
MICROFICHE PART NO. 12565-90006

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