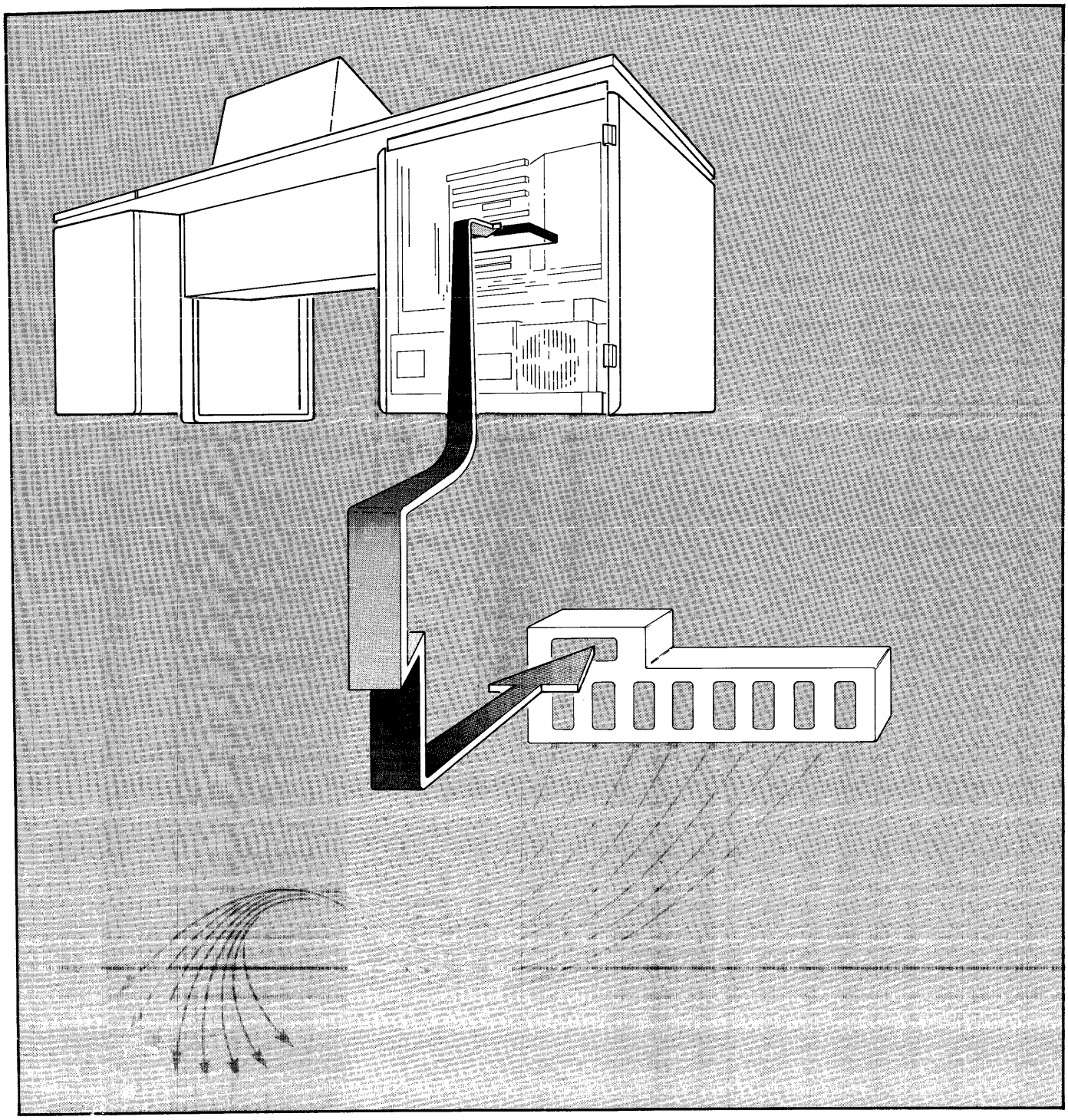
HEWLETT PACKARD

HP 12792A

8-Channel Asynchronous Multiplexer Subsystem Installation and Reference Manual

for HP 1000 M/E/F-Series Computers



HP 12792A
8-Channel Asynchronous Multiplexer Subsystem
installation and reference manual

For HP 1000 M/E/F-Series Computers

Card Assembly: 5061-3415
Date Code: 2026

HEWLETT PACKARD

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PRINTING HISTORY

New editions are complete revisions of the manual. Update packages contain replacement pages or write-in instructions to be merged into the manual by the customer. Manuals will be reprinted as necessary to incorporate all prior updates. A reprinted manual is identical in content (but not in appearance) to the previous edition with all updates incorporated. No information is incorporated into a reprinting unless it appears as a prior update. The edition does not change.

First Edition ..... Sept 1980

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

Preface

Hewlett-Packard introduces the first in this series of intelligent interfaces, the HP 12792A Eight Channel Asynchronous Multiplexer Subsystem.

The introduction of a new series of microprocessor based interfaces represents new versatility and intelligence in HP 1000 I/O processing. These products enable Hewlett-Packard to offer fresh new concepts in the areas of application program development and execution. This type of innovation provides welcome relief from the burgeoning and increasingly complicated I/O software overhead incurred by present operating system structures. The intelligent based I/O interface off-loads most of the data and control protocol that is necessary for communications to and from asynchronous or synchronous worlds.

Thus, a means is now provided in which users can interface their own particular "black boxes" (especially microprocessor based) as well as the standard HP terminals to the HP 1000 System.

Throughout this installation and reference manual, the HP 12792A Multiplexer Subsystem, which includes both hardware and software in one complete package, is referred to as the MUX Subsystem. References made to any particular portion of the total Subsystem will be called out specifically (i.e., MUX hardware, MUX interface, or MUX software). The purpose of the manual is to provide a source of information regarding the MUX Subsystem with concentration on the hardware. Portions of the manual will also refer to the HP 12828A RS-232-C Multiplexer Panel, a MUX Subsystem accessory, which provides an easy method for connecting terminals or your specific devices to the MUX hardware.

The information and concepts provided here are in areas such as general reference, installation, principles of operation, custom cabling, and diagnostics as well as servicing information and diagrams.

Three aids to "finding your way around" this manual are provided and listed below:

* Definition of Terms ..... page vii

* Table of Contents ..... page ix

There may be terms in this manual which are unfamiliar to you. If this is the case, please consult the "Definition of Terms" before reviewing the manual.

Unlike the conventional "List of Illustrations" and the "List of Tables", both lists include some Illustrations (Figures) and Tables that are not called out by specific Table or Figure numbers. This is because those particular Tables or Figures are called out and referenced in nearby text. A Figure or Table that is divorced from the same text which references it will contain the number and title, making it easier to identify.

Definition of Terms

ASCII - American Standard Code for Information Interchange.

asynchronous transmission - No timing signals are sent with the data. Start and stop bits serve to define transmitted words.

block - A contiguous stream of data words.

buffer - A segment of contiguous random-access memory (RAM) locations used for temporary storage of input/output messages.

card - The interface printed circuit assembly (PCA).

DIP (Dual In-line Package) - A type of integrated circuit package.

driver - In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

firmware - Z-80A software code packaged in read-only memory (ROM) or erasable programable read-only memory (EPROM).

full-duplex - Communications system or equipment capable of simultaneous two-way data communication.

half-duplex - Communications systems or equipment capable of transmission in either direction, but not both directions simultaneously.

handshaking - The alternating exchange of predetermined signals between two communicating devices for purposes of control.

hardwired full-duplex modem - A modem which is controlled by the connecting the necessary EIA status and control lines to various voltage or ground references thereby enabling the modem to operate in an unattended mode. Thus, the HP 12792A Multiplexer Subsystem views a hardwired full-duplex modem the same manner as it would the device cable.

host - The HP 1000 M/E/F-Series computer housing the MUX interface and software.

interface - A device providing electrical and mechanical compatibility between two communicating devices. The HP 12792A also provides other

control features for the associated communication link.

LED (Light Emitting Diode) - A component used on many printed circuit assemblies to provide a visible indication of desired information.

link - Communication interfaces, lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

modem (modulator-demodulator) - Equipment capable of digital-to-analog and analog-to-digital signal conversion for transmission and reception via common carrier telephone lines.

MUX - Multiplexer (The HP 12792A 8-Channel Asynchronous Multiplexer Subsystem product)

MUX interface - The eight-channel Z-80A based printed circuit assembly that resides in the I/O backplane of an HP 1000 M/E/F-Series Computer host.

MUX hardware - All hardware necessary to connect a terminal, printer, or user device to the I/O backplane of an HP 1000 M/E/F-Series Computer. This includes the MUX interface and cabling (including the MUX Panel if used).

MUX Panel - The RS-232-C distibution device that accepts one RS-423 cable input from the MUX interface and provides up to eight separate ports for the connection of terminals, printers, or user devices.

MUX Subsystem - The HP 12792A product as a whole. This includes the MUX interface, cabling, software, and diagnostic software. It may also loosely define the HP 12828A RS-232-C Multiplexer Panel when used in conjunction with the HP 12792A.

MUX software - All software necessary to enable an M/E/F-Series Computer to communicate with up to eight terminals or user devices. This includes the MUX interface and device drivers as well as the predriver and device driver address table.

PCA (Printed Circuit Assembly) - Interface cards are sometimes referred to as PCAs.

receiver - Any device capable of reception of electrically transmitted signals.

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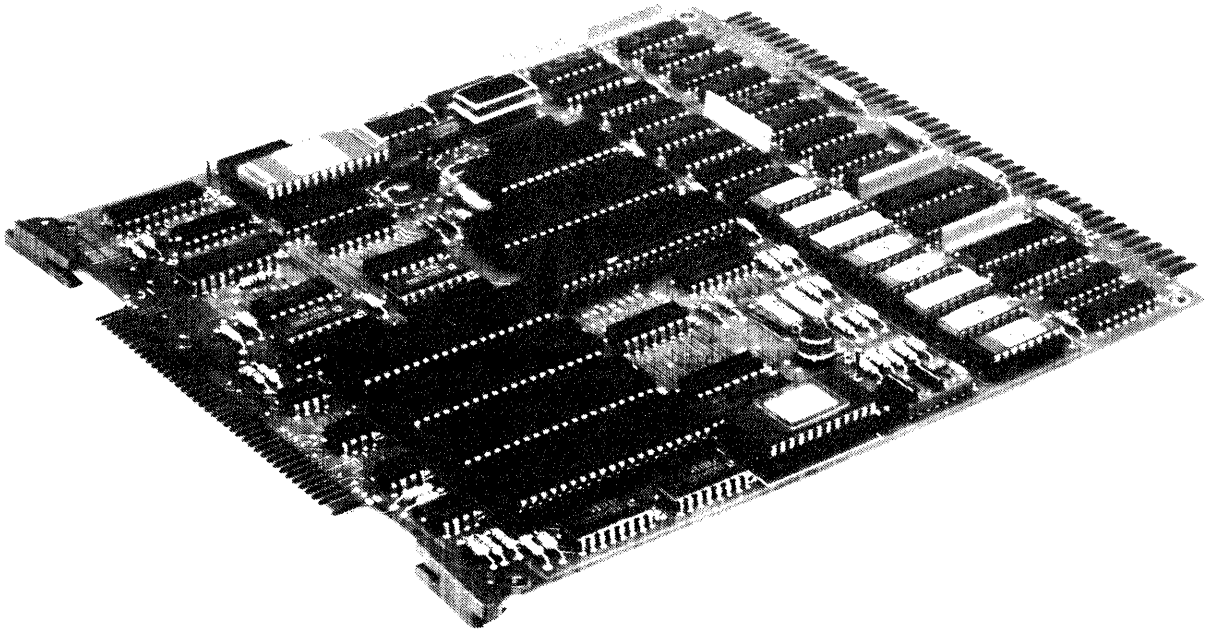


HP 12792A Multiplexer Interface

Chapter 1
General Information

Introduction

Chapter one contains the following descriptions and specifications related to the HP 12792A Eight Channel Asynchronous Multiplexer (MUX) product:

* HP 12792A Product Overview
* Detailed Description of the MUX
* HP 12828A Multiplexer Panel and Custom Cabling
* Equipment and Documentation Supplied with the Standard Product
* MUX Product Identification
* MUX Subsystem Specifications

Multiplexer Subsystem Overview

Hewlett-Packard's 12792A 8-Channel Asynchronous Multiplexer Subsystem and its accessory, the HP 12828A RS-232-C Multiplexer Panel (ordered separately) combine to provide a complete HP 1000 hardware/software package for multiplexed terminal/device applications. These applications include communications to and from all currently supported HP terminals (2621A/P, 2626A, 2631A+040, 2635A, 2640A/B, 2645A, 2647A, 2648A, 2649A and 2675A) as well as line printer support for the 2631A, 2635A, and 7310A. Other HP or non-HP devices may be used in conjunction with the multiplexer subsystem, however, it may be necessary for the user to write simple device drivers to supply the necessary control for certain devices. Consult the Multiplexer Subsystem User's Manual, part number 12792-90002, for detailed information regarding the user written device driver. This guide is supplied as part of the HP 12792A Multiplexer product.

Detailed Description

Hardware Operation

The HP 12792A 8-Channel Asynchronous Multiplexer Subsystem provides an efficient, high performance method for interfacing HP 1000 M/E/F-Series Computers to any RS-423 or RS-232-C compatible device connected in a hardwired or hardwire full-duplex modem point-to-point environment.

Device communication to and from the HP 1000 Computer is provided through a microprocessor based interface which significantly off-loads the overhead normally associated with routine communication management, thus freeing the computer for application program execution or development tasks of HP 1000 terminal users. The on-board Z-80A microprocessor, in conjunction with EPROM, RAM, DMA, and SIO support, manages the asynchronous TTY-like protocol of connected devices. Each of the eight channels is separately buffered (input and output) and most communications to/from the interface memory to the Host CPU backplane are accomplished under DMA, thus I/O processing time is significantly reduced. Up to 128 requests per second to the host from the interface are possible across the I/O backplane of the host.

Each interface provides two on-board programmable baud rate generators which control channel transmission speeds from 50 to 19.2K Baud. The total aggregate throughput capability of the interface is 76.8K bits per second.

MUX Software Driver

The HP 12792A Multiplexer Subsystem (hardware and software) operates in HP 1000 M/E/F-Series Processors/Systems in conjunction with RTE-IVB or RTE-MIII Operating Systems. Program development and program execution are supported on RTE-IVB. Application program execution is supported on RTE-MIII.

The software supplied with the HP 12792A product consists of an interface driver and two standard device drivers. The interface driver manages the communications across the CPU backplane to and from the multiplexer interface PCA. The device drivers perform the formatting of control and data, specifically the inclusion of control characters for device requirements.

Additional flexibility is built into the RTE compatible software in that I/O requests will be handled under DCPC control if a DCPC channel is currently available and deemed more efficient by the software driver. Otherwise, the request will be handled on a word-by-word basis. This dynamic allocation feature reduces the typical CPU overhead to approximately 3% per channel at 9600 baud for long block transfers on a continuous basis.

Flexibilty is a key feature in the interface and device software area in that customers may write their own device drivers to interface to other devices such as terminals, "black boxes", and plotters, so long as the devices meet RS-423-A or RS-232-C requirements.

MUX Panel and Custom Cabling

Nominally, up to eight terminals or devices can be connected to a single multiplexer interface through a MUX accessory, the HP 12828A RS-232-C Multiplexer Panel, or through the use of custom cabling constructed by the user.

Virtually any number of interfaces will be supported in the operating system, up to the maximum available I/O slots. The maximum number of physical devices which will be supported is 62. Future expansion can be built in at system generation time by allowing reserved slots for devices to be added as the need arises.

Since the interface supports the standard RS-423-A electrical interface specifications (also compatible with RS-232-C), the HP 12828A MUX Panel may be located at the CPU or up to 300 feet away from the main CPU (supported at channel speeds of 9600 baud). Devices may then be connected to the panel through standard EIA 25-pin connectors on the panel. This remote locatability of the panel overcomes the typical 50-foot limitation imposed by RS-232-C specifications. Additionally, hardwired full-duplex modems may be employed on a channel-by-channel basis, however no active modem controls to or from the MUX interface are possible.

Equipment and Documentation Supplied

The HP 12792A 8-Channel Asychronous Multiplexer Subsystem consists of the following:

Hardware

* 5061-3415 Multiplexer Interface PCA
* 12792-80001 Multiplexer Firmware
* 5061-3467 80 pin connector kit

Software

* 12792-13301 Mini-cartridge, including the following software:

%PVM00 Multiplexer Predriver (12792-16001)
%DVM00 Multiplexer Interface Driver (12792-16002)
%DDV05 26XX Screen Device Driver (12792-16003)
%DDV12 7310 Device Driver (12792-16004)
%$DVTB Device Driver Address Table (12792-16005)

* 12792-13302 Mini-cartridge, including the following software:

%MUXST RTE-IVB On-line downloadable diagnostic
!MUXST RTE-MIII Off-line downloadable diagnostic

Documentation

* 12792-90001 Multiplexer Subsystem Installation & Reference Manual
* 12792-90002 Multiplexer Subsystem User's manual
* 12792-90003 Multiplexer Subsystem Configuration Guide
* 12792-18999 Multiplexer Subsystem Numbering Catalog

Identification

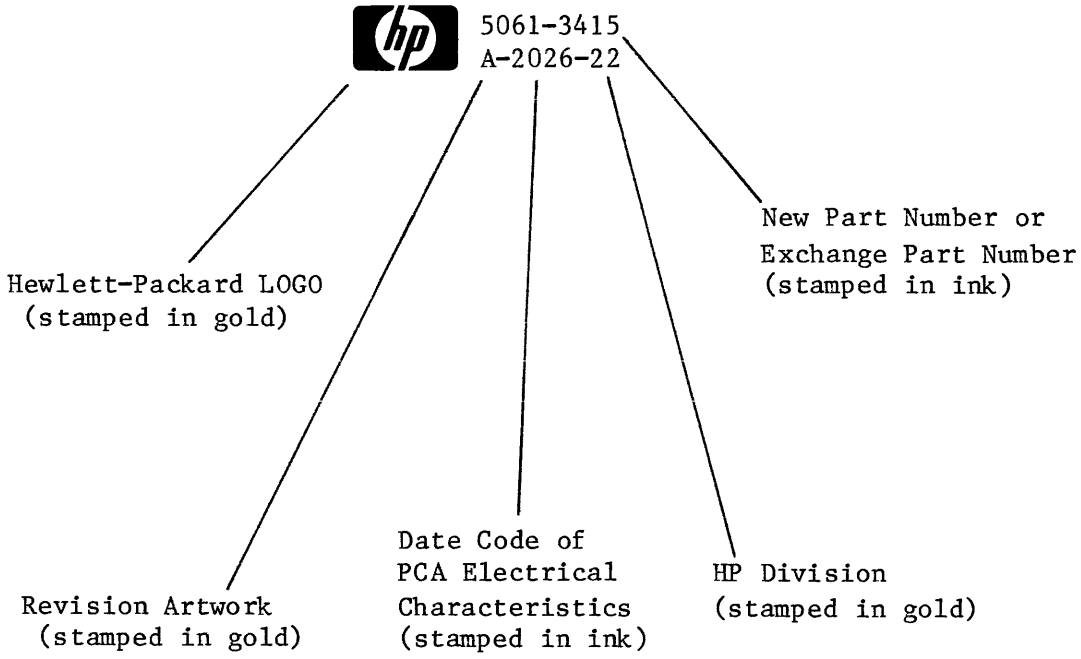
Product

Five digits and a letter (12972A) are used to identify the Asynchronous Multiplexer Subsystem. As in most Hewlett-Packard products used with Hewlett-Packard Computers, these five digits are used to identify the product number, and the suffix letter represents the revision level of that product.

Interface

The interface supplied with the Subsystem is identified by an eight digit part number (5061-3415) which is stamped in black ink, on the PCA near the HP logo. You should not confuse this number with a similar number which is stamped in gold (5090-1608), also near the HP logo, which is the manufacturing assembly number used to identify the unloaded PCA (without components). It is of no use to the user.

PCA revisions are identified by a letter, a date code, and a division code (e.g., A-2026-22). This series of characters is stamped on the PCA near the Hewlett-Packard logo and under the part number. The letter (UPPER CASE ONLY) identifies the revision of the etched trace pattern on the unloaded PCA. The four digit date code refers to the electrical characteristics of the loaded (with components) PCA. The division code (last two digits) identifies the Hewlett-Packard manufacturing division from which the PCA originates. An example of PCA identification is shown below:



If the revision letter and date code stamped on your Multiplxer interface does not agree with the revision and date code printed on the title page of this manual, there are differences between your interface and the interface decribed in this manual. If a discrepancy should occur, please contact your nearest Hewlett-Packard Sales and Service Office (listed at the back of this manual) for manual update information.

Documentation

All manuals supplied with the HP 12792A Multiplexer Subsystem are identified by their respective name, part numbers, and date codes. These identifiers are located on the front page of each manual along with the respective publication date. If a manual should change or be updated, a supplement that includes these changes is shipped with each manual. When the manual stock is depleted, all previous updates will be incorporated into a new printing of the manual and the print date will reflect the last supplement date. Consult the "Print History" page ii of this manual for further details.

MUX Subsystem Specifications

Physical

The HP 12792A is a standard size M/E/F-Series I/O interface occupying one slot in the HP 1000 I/O backplane:

* SIZE: 19.70 by 22.10 by 1.27 centimeters, 7.75 by 8.70 by 0.50 inches

* BACKPLANE INTERCONNECTS: One 86-pin edge connector plugs into the M/E/F-Series I/O backplane.

* DEVICE INTERCONNECTS: One 80-pin edge connector on which a cable hood or connector may be placed for connection to any one or all of eight I/O devices.

Electrical

* TRANSMISSION MODE: Bit serial, Asynchronous.

* CAPACITY: Eight full-duplex (transmit and receive) communication channels with two 254-byte transmit buffers and two 254-byte receive buffers per channel.

* PROGRAMMABLE FEATURES: Echo on or off; break key detection; record termination processing (CR, DC2, RS, control-D, end on count); buffer overflow detection; baud rates from 50 to 19.2K; on board editing (back space, line delete); block mode format.

* INTERFACE LEVEL: Conforms to EIA Standards (RS-423-A/RS-232-C or CCITT V.24).

* DATA TRANSFER LENGTH: Programmable character at 5, 6, 7, or 8 bits per character with programmable (1, 1-1/2, or 2) stop bits.

* DATA TRANSFER RATES: Two baud rate generators programmable from 50 to 19,200 baud.

* AGGREGATE THROUGHPUT CAPACITY: 7,680 characters/second (8 channels at 960 characters/second).

* ERROR DETECTION: Parity (even/odd/none), overrun, and framing error detection.

* POWER REQUIREMENTS: + 5 VOLTS 2.0 AMPS
+12 VOLTS 0.3 AMPS
-12 VOLTS 0.04 AMPS
Total Power Dissipation = 14.1 WATTS.

Chapter 2
Installation

Introduction

The following topics provide fundamental information which is necessary for successful installation of the HP 12792A Multiplexer Hardware.

* Unpacking and Inspection
* Calculation of Available Current vs Required Current
* Preparation Before Installation and Use
* Installation and Check-out of the Interface and Cable
* Reshipment for Repairs or Damage

Unpacking and Inspection

CAUTION

Static Sensitive Devices

Many components on the MUX interface are susceptible to damage by static discharge. These components can be identified readily, as they are the ICs that are inserted into sockets. Refer to the safety considerations information at the front of this manual before handling, removing, or replacing these parts.

Upon receipt of your HP 12792A Multiplexer Subsystem, immediately inspect the shipping container for signs of any physical damage. If damage is detected, request that the carrier's agent be present when the equipment is unpackaged. Inspect the interface, connector, and mini-cartridges for damage (scratches, cracks, loose components, etc.) and ensure that all the contents of the Multiplexer Subsystem are present (refer to Chapter One, specifically the Section entitled "Equipment and Documentation Supplied"). If you find damaged, incorrect or missing parts, notify the carrier and the nearest Hewlett-Packard Sales and Service Office immediately. Retain the shipping container and the packing material for the carrier's inspection.

The Hewlett-Packard Sales and Service Office will arrange for the repair or replacement of the damaged equipment without waiting for any claims against the carrier to be settled.

Available Current vs. Required Current

The HP 12792A MUX interface obtains its operating voltages from the host computer power supply. The power supply feeds a crossover assembly located on top of the I/O and memory card cages of the host computer. This, in turn, distributes the various voltages to both I/O and memory backplanes. The MUX interface is designed to be inserted into the I/O card cage and backplane (rear of the computer) where it receives operating voltages and also becomes part of the I/O data and control bus structure. Since all items installed in the computer derive their operating power from the computer power supply, a calculation should be performed to determine if the MUX interface, when installed in your present system, will cause a current overload.

CAUTION

These calculations should be made before installing the MUX interface!

To accomplish this task, you must obtain and add all of the current requirements for each interface/product installed in the computer. The +5 volt CPU and +5 volt memory current drains (amps) are the most critical. The total current requirements should then be compared with the available current for each supplied voltage. The electrical specifications for each product are listed in the "Specifications" section of the respective Operating & Reference or Installation & Service manuals. The current HP 1000 Hardware Data Book also contains this information for all computer related products in a section entitled "Power Specifications and Applicability Summary". The MUX Interface power/current requirements are as follows:

+ 5V @ 2.00 amps

+12V @ .30 amps

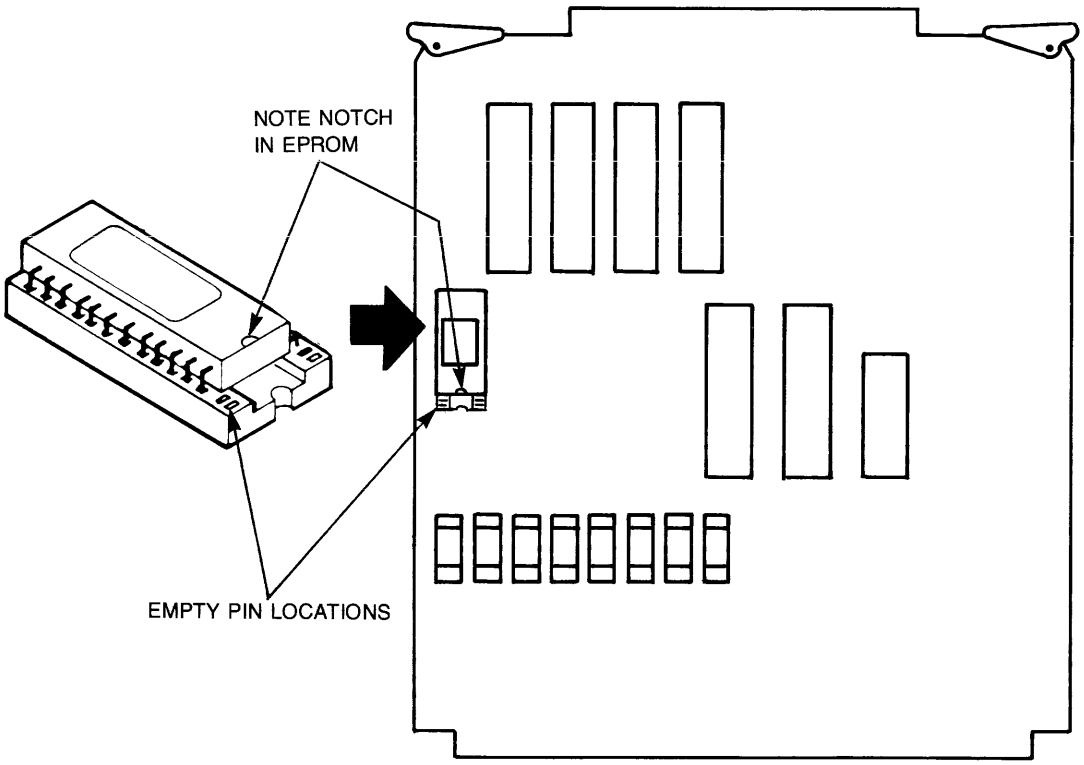
-12V @ .04 amps

If the additional Multiplexer current overloads the host computer power supply, it should not be installed until alternate arrangements have been made to off load the required current.

Preparation for Use

Proper Firmware (ROM) Installation

The firmware ROM is installed in a socket provided on the MUX interface as shown below:

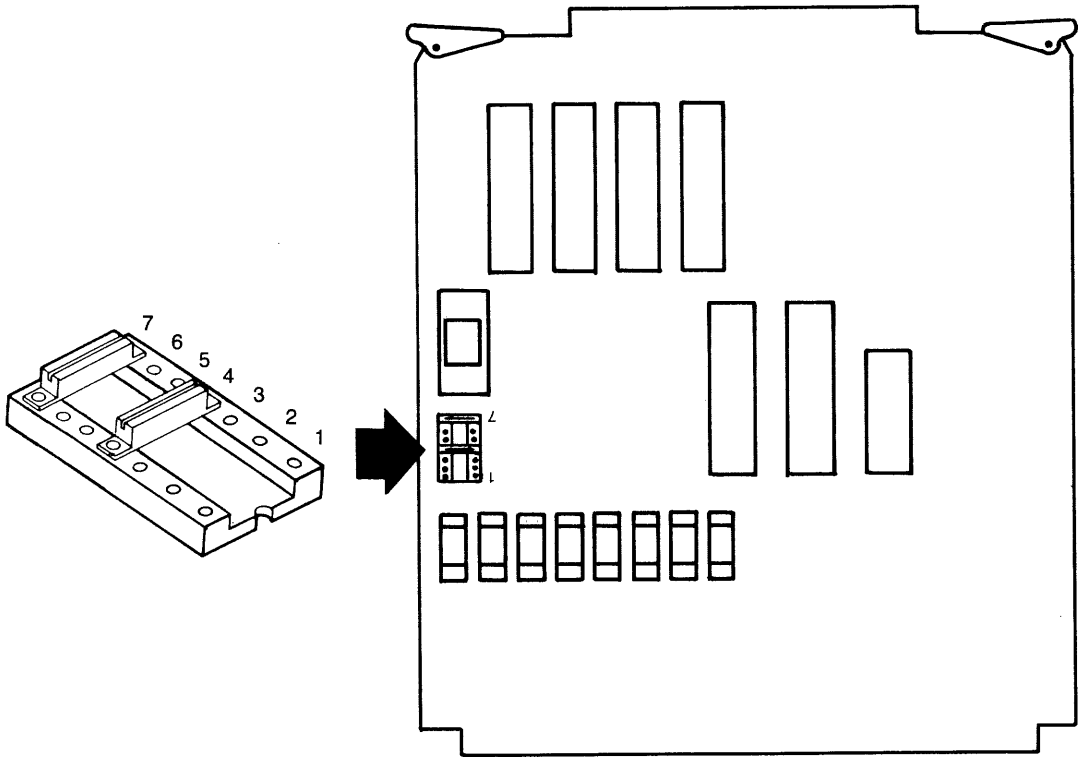


Ensure that the ROM is properly installed as shown above and that it has not been damaged or loosened from its socket during shipping.

Additionally, it is advisable to guard against bending or breaking during the process of installing or re-installing the ROM itself. These pins may also become folded between the ROM I/C and the I/C socket resulting in intermittent operation of the MUX Subsystem. In most cases, a bent or damaged pin can be straightened with careful use of needle-nose pliers.

EPROM/ROM Jumper Configurations

As previously noted, the EPROM or ROM that resides on the MUX interface is referred to as "firmware". Inspect the MUX Interface to ensure proper configuration and installation of the firmware jumpers. The following figure illustrates the location of this jumper block and shows the proper jumper configuration for the firmware on the MUX interface.



Note that the positions on the block are labled 1 through 7. A combination of two or more jumpers is required to be installed in the block for proper operation. The versatility of the MUX interface design provides the capability to accept several types of EPROM or ROMS. The following table provides the jumper configurations for some common ROMs and EPROMs. This is not an exhaustive list by any means, however the scheduled availability of these parts may necessitate shipping the interface with different ROMs or EPROMs from time to time.

Manufacturers Part Number	Install Jumpers	Size (bytes)
TI 4732, 2532	W2, W5	4K
MOT MCM68A332, MCM68764	W2, W5	4K
Intel 2716, TI 2516	W2, W6	2K
MK36000, AMI 54264	W3, W5	8K
MOT MCM68A364, MCM68764	W3, W5	8K
Intel 2732, 2332	W4, W7	4K
Intel 2364, 2764	W4, W7	8K
MK37000, MK2764	W4, W6	8K

Cabling

The HP 12792A Multiplexer Subsystem is designed to be used in a variety of applications. To facilitate this versatility, the connection from the MUX Interface to the terminals or user devices becomes the your responsibility. Further discussion will help you better understand this responsibility.

You have purchased the HP 12972A Multiplexer Subsystem, but may or may not have purchased the HP 12828A RS-232-C Multiplexer Panel. Thus, one of the following three areas may parallel your particular application:

* The separate, 8-junction RS-232-C Multiplexer Panel (HP product number 12828A), when used, provides convenient connection to the MUX Subsystem via a ten foot cable. The Panel then provides the capability for the connection of up to eight RS-232-C devices. The RS-232-C restrictions impose a 50-foot maximum line length from the Panel to any device.

* In addition to the MUX Panel, you can also construct cables that may be used to extend the Panel distance from the MUX Interface to 91 metres (300 ft). The added length from the MUX interface to the Panel is made possible by the RS-423 circuits that are resident on the interface.

* You can completely bypass the use of HP's RS-232-C MUX Panel by fabricating a panel and cables specific to your own lengths and requirements. If RS-423 standards are observed in both panel and cabling, you can indeed implement a 300 foot length between the host computer and your device.

Connector kits have been provided in both the HP 12792A MUX Subsystem and the HP 12828A RS-232-C Multiplexer Panel to facilitate implementation of the last two categories called out above. Although there are numerous cabling configurations which could be employed, the major cable fabrication and connection applications are further discussed in Chapter Four of this manual.

Cable and Interface Installation

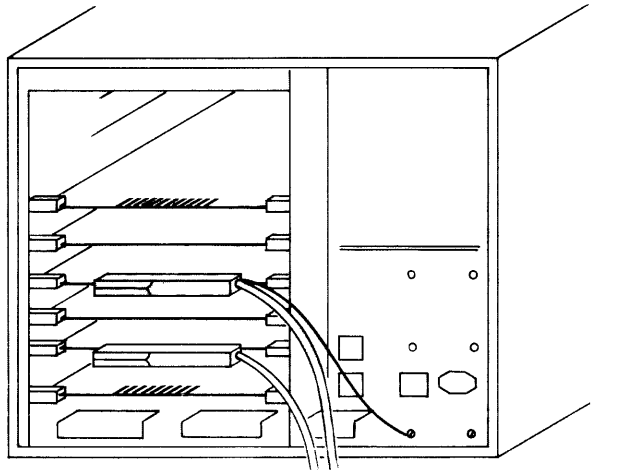
Before continuing with the actual installation of the interface, make sure that you have reviewed and completed the preparation tasks that have been previously outlined in this chapter.

CAUTION

Always ensure that the power to the computer is off before inserting or removing the MUX interface and associated cabling. Failure to do so may result in damage to the interface or the attached I/O device.

Gain access to the I/O card cage of the host computer and install the MUX interface into the desired backplane slot, ensuring that the component side of the interface is up. Press the interface firmly into place and note the number of this slot (select code number) as you will be required to reference this number when executing the MUX diagnostics and generating the MUX software into an operating system.

Next, connect the proper cable to the MUX interface. Ensure that 80-pin connector of the cable is properly attached to the interface such that the cable exits to the right of the backplane (toward the center of the host computer) as shown below:



ATTACH GROUND WIRE TO HOST FRAME USING AVAILABLE SCREWS AT REAR OF HOST

After connecting the RS-232-C Multiplexer Panel or user fabricated cabling to the desired I/O devices, the power may be restored to the computer system.

For installation and configuration of the MUX Panel and custom cabling examples refer to Chapter Four of this manual.

Multiplexer Check-out

Proper operation of the MUX interface and cabling can be assured by performing the tests and diagnostics described in Chapter Five of this manual.

Reshipment

If any part of the HP 12792A Multiplexer Subsystem is to be re-shipped for any reason, the items should be packaged in the original factory (or similar) material. The proper identification needs to accompany the items on the inside of the shipping container as well as addressing on the outside. When the standard factory packaging is not used, wrap the items in Air Cap TH-240 cushioning (or equivalent) manufactured by Sealed Air Corporation, Hawthorn, N.J. and place in a corrugated carton (200 pound test material). Seal the shipping carton securely and mark it "FRAGILE" to assure careful handling.

Chapter 3
Principles of Operation

Introduction

This section contains the following information relating to the Multiplexer Interface:

* A description of the host computer I/O backplane interface.
* A brief description of the Z-80A CPU and support chips.
* Descriptions of the principle command and status words.
* A functional-level description of the interface operation.

Hardware Description

The MUX interface, HP part number 5061-3415, includes the following major functional areas:

* HP 1000 M/E/F-Series Computer I/O backplane interface
* Z-80A Microprocessor family subsystem (CPU, SIO, DMA and CTC)
* Read-Only Memory (ROM)
* Random-Access Memory (RAM)
* Communication line interface

A block diagram illustrating the major functional areas of the MUX interface is presented in Figure 3-1.

Host Computer I/O Backplane Interface

The MUX interface communicates with the HP 1000 host computer through the computer I/O backplane. The backplane interface circuitry on the MUX interface can be logically divided into two major sections: the I/O data latches and the control circuitry section.

The I/O data latches consist of two 8-bit input latches and two 8-bit output latches. The input latches hold 16-bit data or command words that are output from the host computer until the MUX interface is ready to process them. Likewise, the output latches on the MUX interface hold 16-bit status or data words which are to be input to the computer.

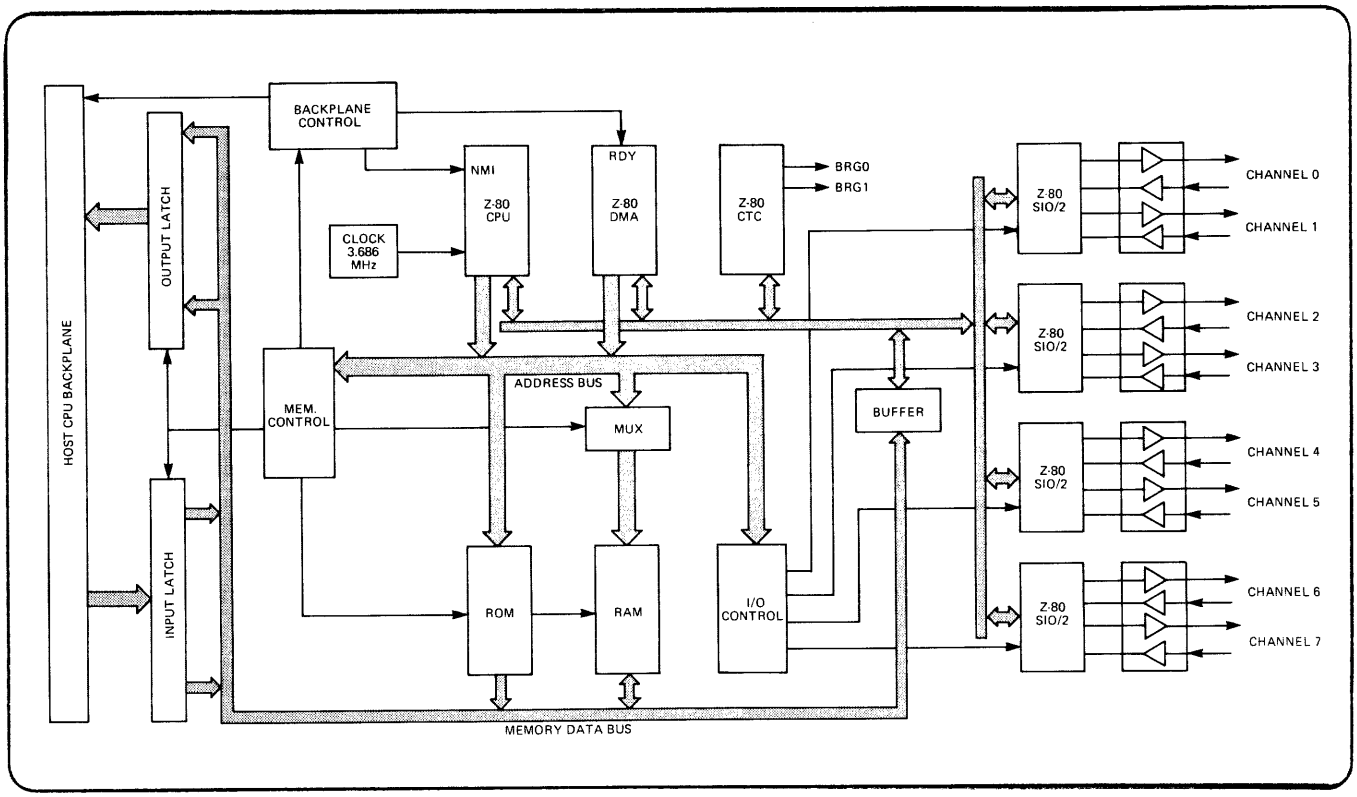


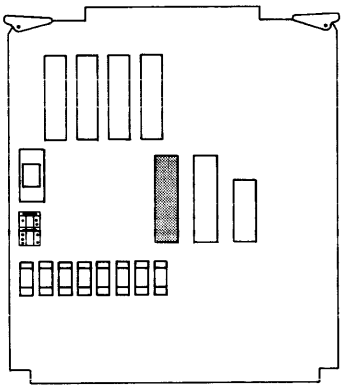
Figure 3-1. Multiplexer Interface Functional Block Diagram.

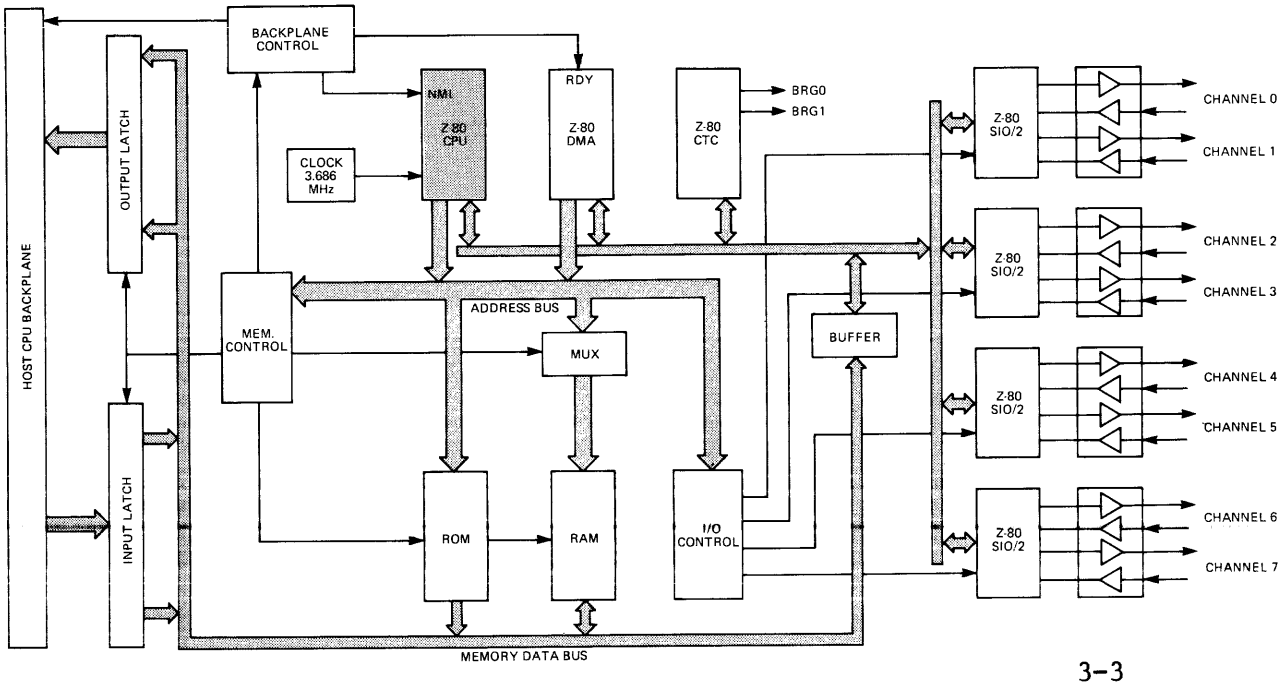
The control circuitry is made up of seven flip-flops (Flag, Flag Buffer, Control, LIA Instruction, Backplane Ready, DMA Ready, and Reset) and various other support logic elements. The primary function of this circuitry is to handle the control signals to and from the I/O backplane. These signals are used to generate and acknowledge interrupts, to handshake data between the host and the interface, and to conform to the standard HP 1000 computer I/O backplane signal conventions. For a more detailed discussion of the HP 1000 backplane signals, refer to the HP 1000 I/O Interfacing Guide, HP part number 02109-90006.

Z-80A Microprocessor Subsystem

Central Processing Unit (CPU)

The heart of the interface is the Z-80A CPU (Central Processing Unit). The CPU's location on the interface and its relationship to buses and other devices on the card are shown below.





This metal oxide semiconductor large scale integration microprocessor (MOS LSI) operates from a single +5 volt supply, uses a single-phase clock and has a typical instruction execution time of 1.0 microsecond. The Z-80A employs a data bus width of eight bits and an address bus width of 16 bits. All Z-80A CPU inputs and outputs are TTL compatible.

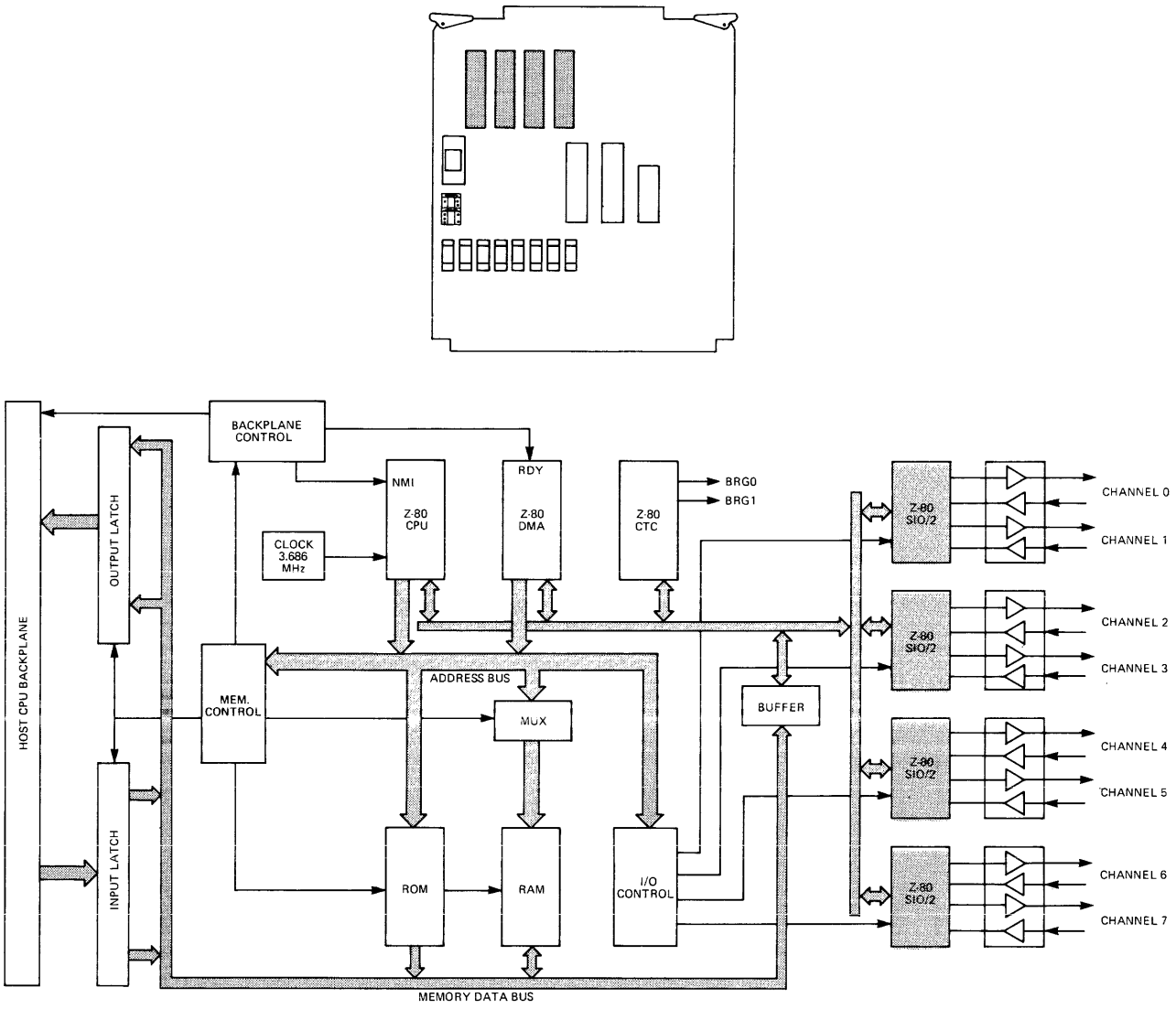
The Z-80A CPU employs a register-based architecture that includes two sets of six general-purpose registers which can be used as 8-bit registers or 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the MUX interface to function as a preprocessor to relieve the host computer of a majority of the protocol processing.

An important input function on the Z-80A as far as the MUX interface is concerned is the NMI (Non-Maskable Interrupt) input pin. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A. An NMI is the highest priority interrupt to the Z-80A and forces it to start fetching and executing instructions from a predetermined location in the firmware. The MUX interface software driver (DVM00) executed out of the host uses this feature to inform the interface that it requires service.

Various support chips are used in conjunction with the Z-80A CPU to facilitate interface operation as an intelligent communication multiplexer interface. These chips are discussed in the paragraphs that follow.

Two-Channel Serial Input/Output (SIO/2)

Four Z-80A SIO/2 chips are used on the interface to provide eight serial data communications channels as shown below.



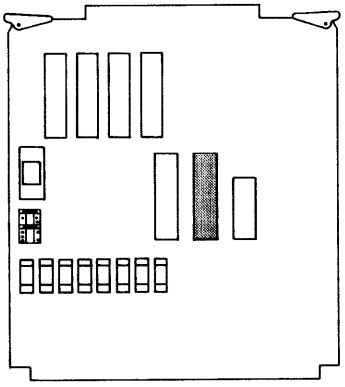
Each SIO/2 chip contains two Universal Synchronous-Asynchronous Receiver Transmitters (USART). The major function performed by the SIO/2 chips are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data. In addition, break, parity, overrun and framing error detection are also provided by the SIO/2 chip.

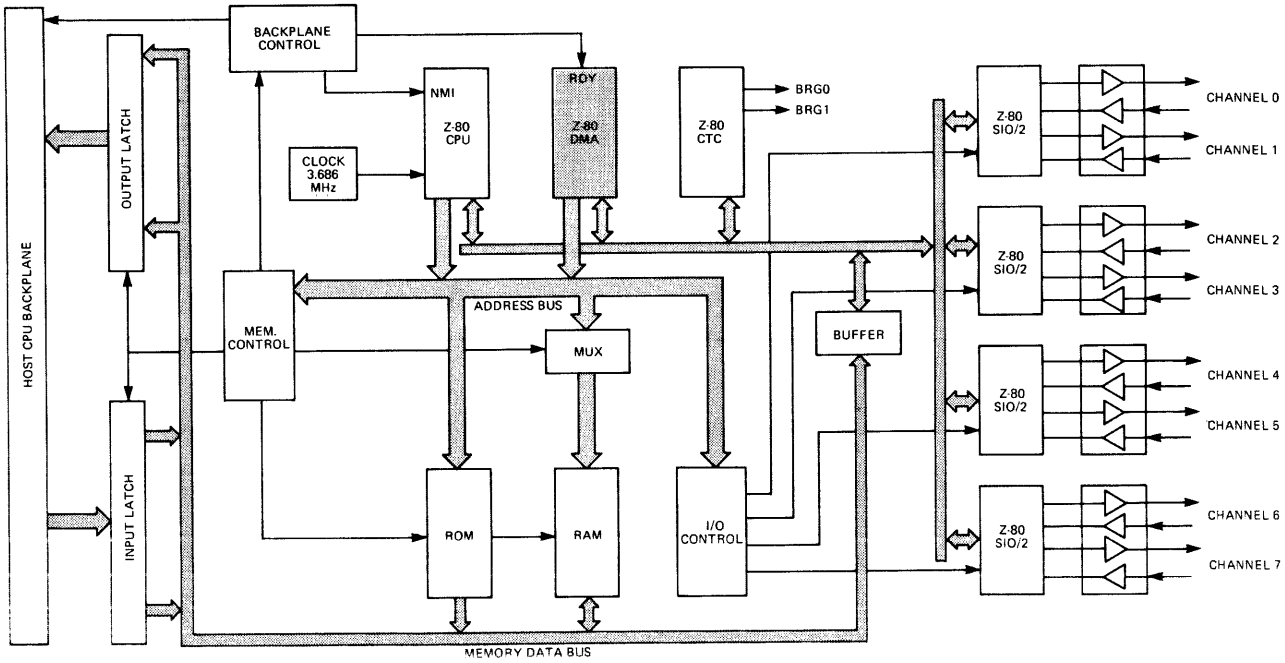
As shown in the illustration, the SIO/2 chips share the Z-80A data bus with other Z-80A devices. The data bus allows the Z-80A CPU to transfer data to and from the SIO/2 chips. In addition, the CPU can read status from the SIO/2 status registers and configure the SIO/2 chips for a particular operation by writing to their control registers using the data bus.

The SIO/2 chip interrupts the Z-80A CPU on an interrupt-per-character basis when transferring data to and from the communication line. In the transmit mode, the SIO/2 interrupts the CPU for the next character to be transmitted after the preceding character has been sent. In the receive mode, the CPU is interrupted each time the SIO/2 converts serial data into an 8-bit parallel data character and is ready to send it to a RAM buffer. Three 1-byte buffer registers are implemented on the SIO/2 chip to prevent the CPU from missing data characters when it responds to interrupts by the SIO/2 in the receive mode.

Direct Memory Access (DMA)

The interface uses a Z-80A DMA chip which is a LSI Direct Memory Access controller. The sole task of the DMA logic is to transfer data directly between the MUX interface memory and the host computer via the data latches of the backplane interface circuitry. The DMA logic accomplishes this task by creating signal sequences that enable data transfers to and from the host. The Z-80A CPU is free to execute other code while the data transfer is taking place. This increases the throughput rate of the interface.



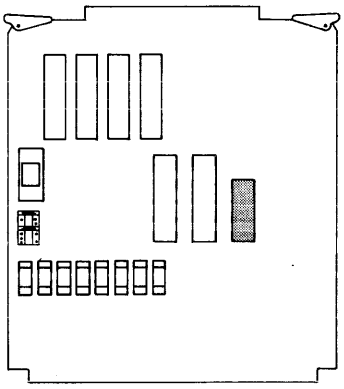


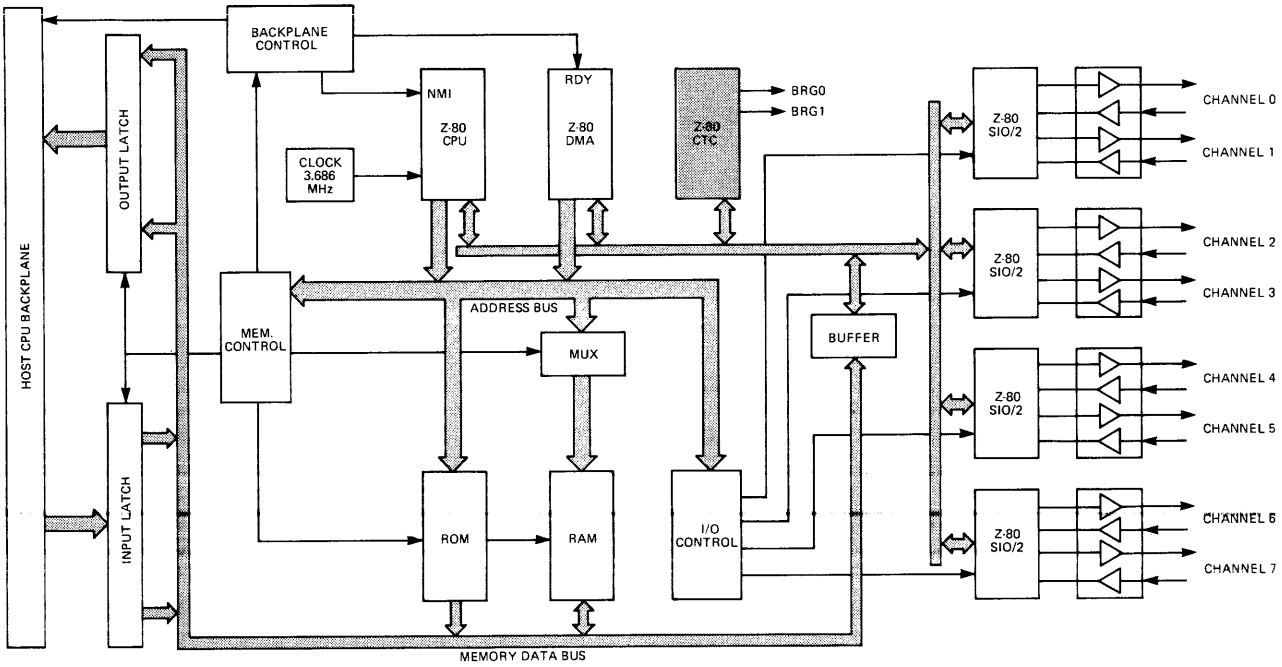
As is evident from the illustation, the DMA chip is capable of taking control of the data and address buses to accomplish its data transfer tasks. Since the Z-80A CPU and the DMA cannot take control of the buses at the same time, the CPU is locked out (from using either bus) during DMA data transfers. The DMA chip is prevented from taking control of the buses for extended periods of time by a counter called a DMA pacer so that the CPU has a chance to monitor all events taking place on the interface. In this manner, data is not lost on the interface while a DMA transfer is in progress.

The backplane control logic monitors the state of the host backplane and controls the operation and transfer rate of DMA transfers through manipulation of the Ready (RDY) input of the Z-80A DMA chip.

Counter-Timer Circuit (CTC)

The MUX interface uses one Z-80A Counter Timer Circuit which provides four independent counter/timers. Two of the counter/timers are used as serial baud rate generators (BRG0 and BRG1). Another is used to maximize the effective throughput of the interface by controlling the frequency of DMA cycle stealing (this is called a DMA pacer) and the fourth counter/timer is used as a system timer to control the processing of certain events within the Z-80A subsystem.



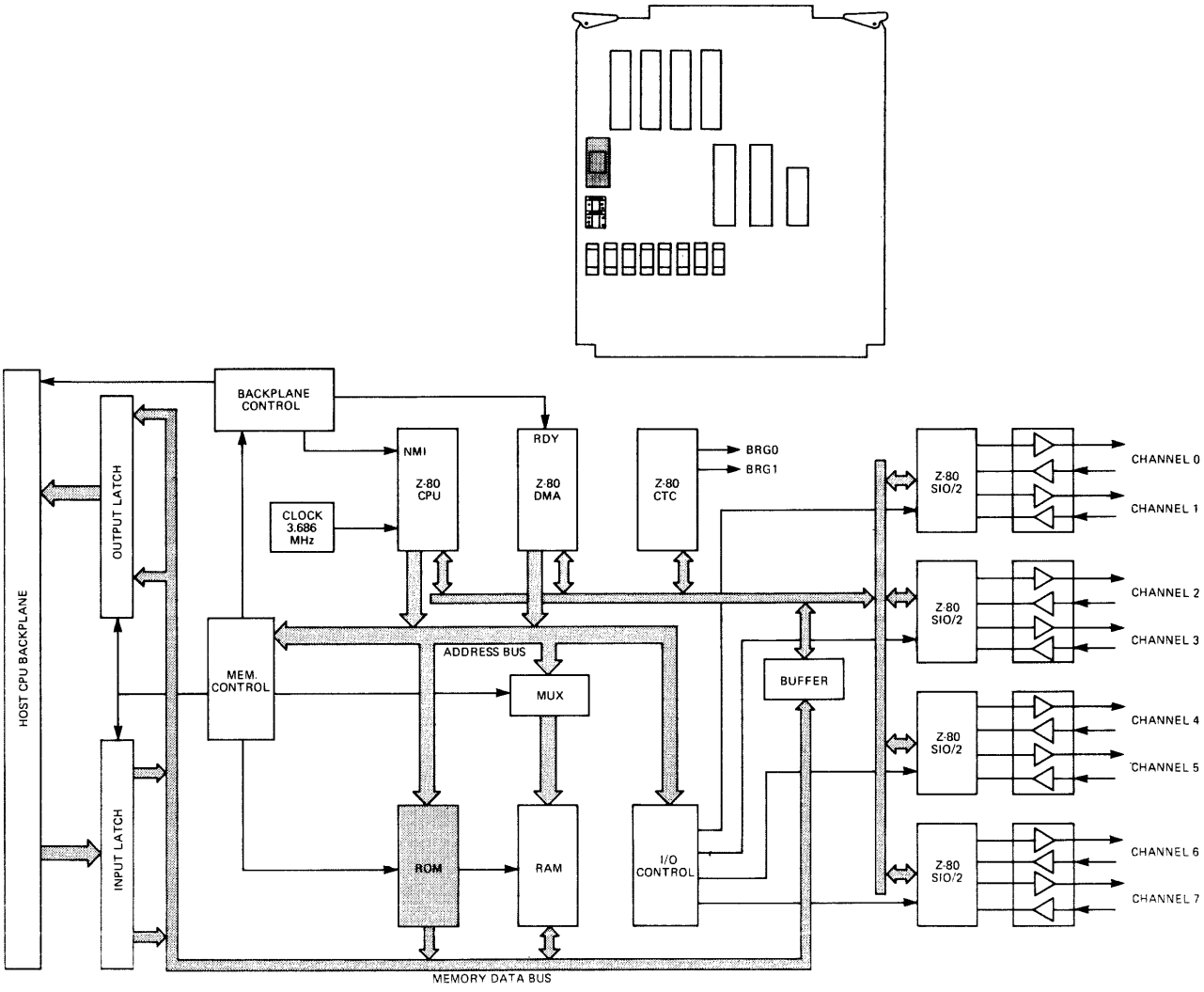


The CTC interfaces to the Z-80A data bus to allow the CPU to send configuration control words to the CTC and to read the status of four counter/timers when the need arises.

Each of the two channels of the CTC, acting as baud rate generators, can be programmed to produce many possible baud rates. Twelve baud rates have been selected from 50 baud to 19.2 kilobaud. This is accomplished through the issuance of a particular command word to the interface by the host software driver. The two resulting signals, BRG0 and BRG1, are then routed to the eight SIO/2 devices through wire jumpers on the communications cable connector. Some of the SIO/2 devices can be wired to operate at one baud rate, while the rest can be wired for another. For example, a system of seven terminals and one line printer can be wired so that the terminals operate at 9600 baud and the printer at 300 baud. Although the two rates are user programmable, only two DIFFERENT rates are available to all eight devices. Refer to Section 4, Cable Fabrication, for a more detailed discussion of baud rate selection.

Read-Only Memory (ROM)

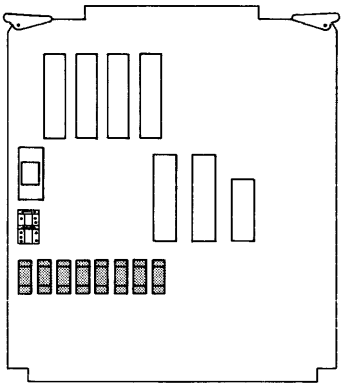
The MUX interface employs 4k bytes of ROM on one chip. All of the Z-80A software required to implement the backplane control and interaction functions for eight serial data communications channels is contained in this ROM and is referred to as firmware. The power fail recovery and initialization routines are also contained in ROM.

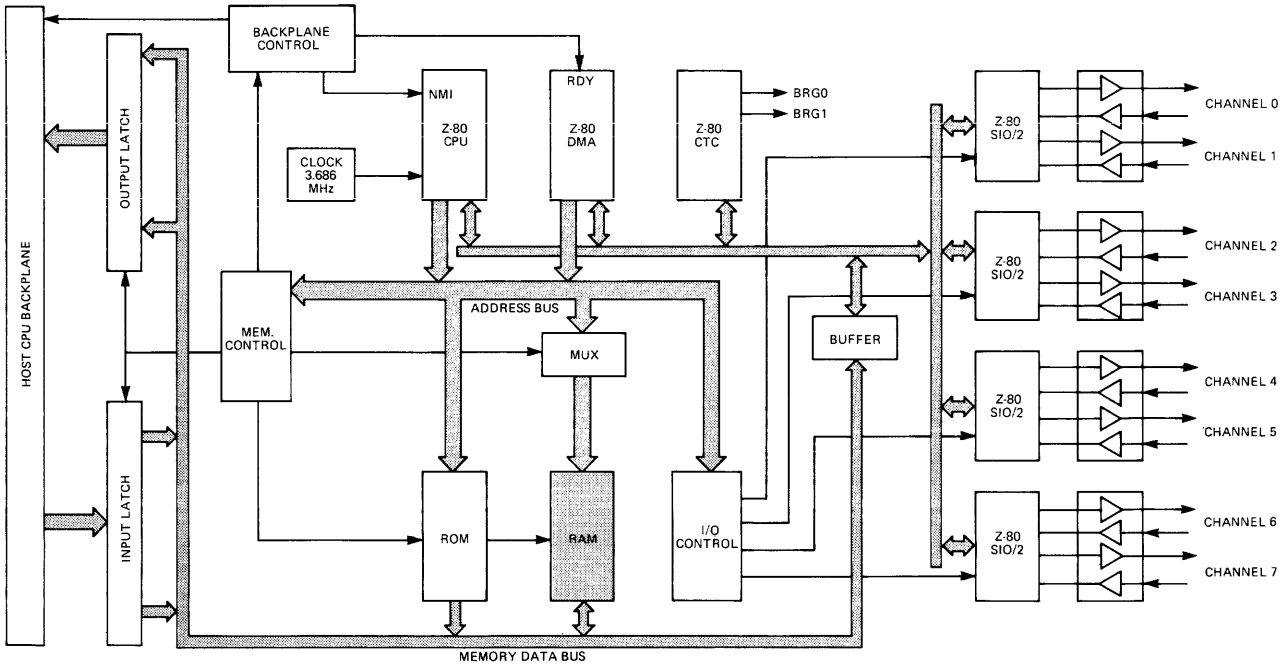


A set of removeable jumpers on the MUX interface is provided to allow the use of different ROM devices. Refer to Section 2, Installation, for the proper ROM jumper configuration. The HP 12792A product is shipped from the factory with the ROM jumpers properly configured for the type of ROM chip installed.

Random-Access Memory (RAM)

The MUX interface employs 16k bytes of dynamic RAM in the location illustrated below.





This memory is used for data buffers (two 254-byte buffers for transmit and

two 254-byte buffers for receive per channel) and the storage of firmware variables. The appropriate refresh signals are provided to the dynamic RAM devices by a combination of the refresh capability of the Z-80A CPU and a Field Programmable Logic Array (FPLA) on the MUX interface. The FPLA operates as a state machine and also invokes WAIT states in reads from ROM and in interrupt cycles, among others.

Additional technical information concerning the Z-80A CPU and support chips is available in the following technical manuals provided by the Zilog Corporation:

* Z-80A CPU Technical Manual (Zilog part number 03-0029-01)
* Z-80A SIO Technical Manual (Zilog part number 03-3033-01)
* Zilog Data Book (Zilog part number 03-8032-01)

Communication Line Interface

The communication line circuitry refers to the receivers and drivers on the MUX interface that accepts and sends data to and from a terminal or user device over the communication line. The MUX interface communication line circuitry is capable of supporting the EIA RS-232-C, CCITT V.24 and EIA RS-423-A serial I/O standards. For the purposes of this discussion, the various communications circuits are referred to by their RS-423-A names. A comparison of EIA RS-232-C, CCITT V.24 and EIA RS-423-A circuits and their respective signal connector pin assignments are given in Chapter Four of this manual.

Chapter Four of this manual addresses the subject of serial interface standards and their relationship to various cabling options for the HP 12792A Multiplexer interface and Subsystem.

Command and Status Words

In addition to data words, command and status words are also exchanged between the host computer and the MUX interface. These additional words are transferred across the data bus and the data latches to aid in the process of communication between the host and the interface. Command words are issued by the host to the interface and status words are sent by the interface to the host.

A brief description of the principle command and status words will prove helpful in understanding the functional level description given later in this section.

Command Words

Command words are initiated by the host driver. Some examples of command words are as follows:

SET KEY - Intializes certain parameters for a particular channel such as baud rate, parity, number of stop bits, and the number of bits per character.

RESET - Causes a branch to the power-up routine within the interface firmware.

ENABLE UNSOLICITED INPUTS - Enables the MUX interface to send status inputs to the host without the host asking for them. This command must be issued to enable the MUX interface to interrupt the host.

DISABLE UNSOLICITED INPUTS - Disables status inputs from the MUX

interface so that the host can initiate a transfer.

ACKNOWLEDGE - Host acknowledges an unsolicited status input from the MUX interface and requests any further information regarding the status input.

CANCEL ALL - Cancel all active receive buffers on an individual channel.

REQUEST WRITE - The host wishes to send data to a particular channel and requires information concerning the availability of transmit buffer space.

WRITE - The host is ready to send data to an individual channel.

SET CHARACTER COUNT - The host specifies that a line of text will be terminated on a predetermined character count as opposed to an end-of-text (EOT) character.

SET READ CONFIGURATION - The host sets the read configuration parameters such as echo, edit (backspace) and record terminators (CR, RS, DC2, control-D or character count).

READ - The host is ready to receive data from an individual channel.

Status Words

Status words are generated by the MUX interface to inform the host of events that have occurred or are occurring on the interface or communications line. Examples of these status words are as follows:

BREAK RECEIVED - The break key has been pressed on this particular channel.

BUFFER AVAILABLE - A transmit buffer is available for transmitting data to the terminal.

TEXT AVAILABLE - The MUX interface has received a line of text from an individual channel.

The MUX interface can send status inputs to the host only after the host has enabled unsolicited inputs. The host can, of course, ask for status from the card. This constitues a solicited status input.

Functional-Level Description

The description that follows typifies the transmit and receive operations of the MUX interface. The command and status words used in the description below were explained in the previous section and the various data paths and hardware groups referenced below are presented in the block diagram in Figure 3-1.

Initially, the HP 1000 has been powered up and the communications line is not yet operational. The process of powering up the host resets the logic on the MUX interface.

Before either a transmit or a receive operation can take place between the host and the MUX interface, certain setup parameters for each channel are sent to the interface via a command word from the host. These parameters include baud rate, parity type, number of stop bits, number of bits per character and ENQ-ACK handshake enable/disable. Once these parameters are set for each operational channel, the transmit and receive operations may proceed.

Transactions initiated by the host driver begin with a DISABLE UNSOLICITED INPUTS command followed by a series of other commands which vary from task-to-task. This command sequence is terminated by an ENABLE UNSOLICITED INPUTS command. The MUX Interface initiates transactions by sending an unsolicited status input to the host. The host driver takes over at this point and sends an ACKNOWLEDGE and a series of commands. These transactions are terminated by the host sending an ENABLE UNSOLICITED INPUTS command.

The host sends a command to the MUX interface by writing data to the select code of the interface and executing an STC instruction. The STC instruction causes a Z-80A Non-Maskable Interrupt which then informs the interface to treat the data in its input latch as a command instead of data.

Receive Mode

The steps involved in a "receive transfer" (i.e., a transfer from a terminal to the host computer) are as follows:

1. The host computer issues DISABLE UNSOLICITED INPUTS, SET KEY, and SET CHARACTER COUNT commands (if need be) to configure a particular channel for the request.

2. The host computer issues an ENABLE UNSOLICITED INPUTS command to the MUX interface.

3. Characters are transmitted one at a time from the terminal to the RAM buffer on the MUX interface allocated to this particular channel. The SIO/2 chip converts the serial data characters it receives from the communications line to parallel data for processing on the MUX interface and the host computer.

4. When the MUX interface has received an end-of-text character (or a predetermined number of characters) from the terminal, it informs the host of this event by writing a TEXT AVAILABLE status input message to the data latches and interrupting the host by setting the Flag flip-flop. This status input also contains end-of-text character information for the host.

5. The host returns with a READ command and the line of text is transferred from the RAM buffer on the MUX interface to a output data latches.

It should be noted that the Z-80A CPU is controlling all of the processing on the MUX interface by executing instructions that it fetches from ROM. This allows the host computer to communicate with eight separate devices in a multiplexed fashion.

Transmit Mode

The steps involved in a "transmit transfer" (i.e., a transfer from the host computer to a terminal are as follows:

1. The host software driver issues a REQUEST WRITE command to the MUX interface to find out if buffer space is available for the transmission of data.

2. When a transmit buffer becomes available, the MUX interface sends a BUFFER AVAILABLE status word to the host.

3. The host sends a WRITE command to the MUX interface.

4. The text block is transferred from the host to a RAM buffer on the MUX interface allocated to this particular channel via the DMA chip on the interface. The interface firmware appends carriage-return/line-feed characters to the text (if enabled to do so).

5. The transmit buffer on the MUX interface is transferred to the terminal a-character-at-a-time after all previous data transmissions to that terminal have completed. The transfer of the text to the terminal involves the RAM and the SIO/2 chips on the interface. The SIO/2 chip requests each character by interrupting the Z-80A CPU.

Chapter 4
Cable Fabrication

Introduction

The purpose of this chapter is to aid you in purchasing and fabricating cables for use with the HP 12792A Mulitplexer Subsystem. The information provided in this chapter is as follows:

* A brief description of the RS-232-C and RS-423 Serial Interface standards.
* A cabling overview.
* RS-232-C Panel-to-device cabling.
* MUX Interface-to-RS-232-C Panel custom cabling.
* MUX Interface-to-device custom cabling.
* Data transmission rate wiring.

Serial Interface Standards

The most widely used standard for interfacing data communications equipment to data terminal equipment is the RS-232-C standard issued in its original form by the Electronic Industries Association in 1969. This standard defines a single-ended, bipolar (+/- 25 volts, maximum), unterminated circuit for serial data transmission rates of up to 20 kilobauds with a maximum line length of 15 metres (50 ft). Only one signal line is required per circuit. However, the simplicity of the RS-232-C interface has its drawbacks. The line length and bandwidth restrictions result from the fact that considerable crosstalk and radiated emissions are generated by this interface.

The EIA issued the RS-423 standard in 1976 to allow higher data signalling rates and longer line lengths than the RS-232-C standard. This interface standard is single-ended, bipolar (+/- 6 volts, maximum) and unterminated for backward compatibility with RS-232-C. Signalling rates vary from 3 kilobauds at a 1219 metre (4000 ft) line length to 300 kilobauds at 12 metres (40 ft). RS-423 differs from RS-232-C in that a balanced receiver is used which references the driver's ground, thus permitting a ground potential difference between the local environments in which the driver and the receiver reside. In addition, the Signal Ground, Send Common and Receive Common circuits of the RS-423 equipment are connected to the AB circuit of the RS-232-C equipment. The end result of these measures is a reduction in noise interference.

Satisfactory operation and backward compatability of RS-232-C circuits with the RS-423 circuits is possible if certain electrical, functional, and mechanical provisions are made. These provisions include the following:

* The RS-423 receivers must withstand the maximum RS-232-C driver voltages of +/- 25 volts.

* The RS-423 driver waveshape must be compatible with the RS-232 risetime.

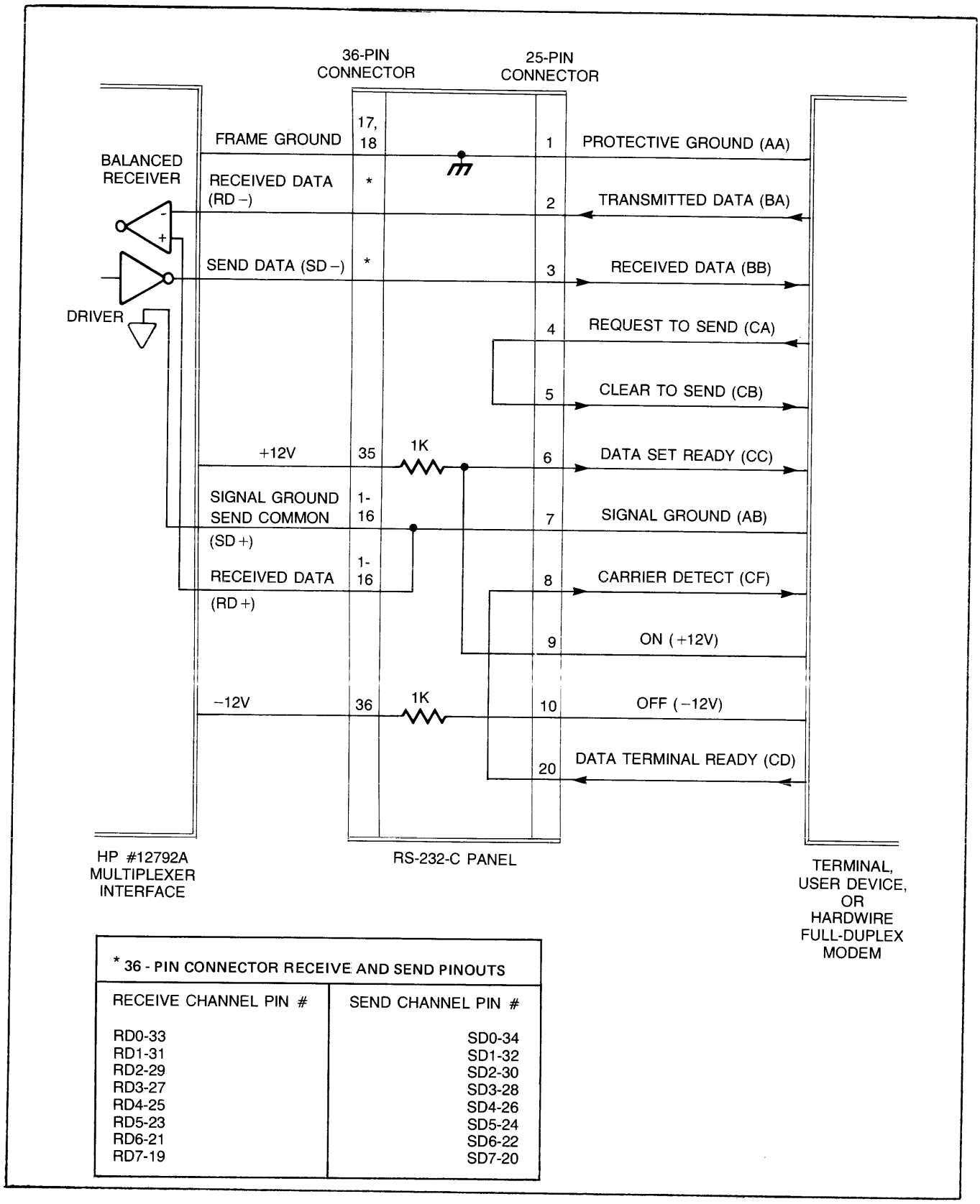
* The RS-423 load resistance should be equal to or greater than 3K ohms.

* All common returns should be connected together.

* There are three RS-232-C circuits that do not have equivalents in RS-423. Conversely, there are eight RS-423 circuits that do not have RS-232-C equivalents.

* RS-232-C devices typically use a 25-pin connector; RS-423 devices use a 37-pin connector.

Figure 4-1 illustrates the RS-423-to-RS-232-C conversion. The balanced receiver for each channel on the MUX interface is fed from a twisted pair containing a data transmission line, Receive Data (RD-), and a Receive Data common (RD+). The fact that the RD- line carries the actual data signal may be confusing, however the MUX interface design inverts this signal as it enters the interface for use with the Z-80A SIO subsystem. The non-differential signal drivers, Send Data (SD-) and a respective Send Data Common line (SD+) make up the transmit data twisted pair.



* 36 - PIN CONNECTOR RECEIVE AND SEND PINOUTS

RECEIVE CHANNEL PIN #	SEND CHANNEL PIN #
RD0-33	SD0-34
RD1-31	SD1-32
RD2-29	SD2-30
RD3-27	SD3-28
RD4-25	SD4-26
RD5-23	SD5-24
RD6-21	SD6-22
RD7-19	SD7-20

Figure 4-1 MUX interface-to-MUX Panel-to-device diagram

Since the MUX interface is designed to meet RS-423 standards, the aforementioned electrical and functional considerations are provided. The mechanical provisions such as connector compatibility and circuit wiring are your responsibility. This Chapter provides the information necessary to build or purchase custom cables (if need be) for proper MUX interface operation with either RS-232-C or RS-423 devices.

Cabling Overview

The HP 12792A Multiplexer Subsystem is designed to be versatile and adaptable to a wide range of system configurations. Let's examine the various hardware components that may be required to connect your I/O devices to the Multiplexer Subsystem. The first component is the MUX interface itself. Since the interface is capable of communicating with up to eight devices, the next consideration is one of the location and distribution of these devices. This becomes your responsibility. Hewlett-Packard provides the means for this communication distribution through the use of HP 12828A RS-232-C Multiplexer Panel. This Panel is designed to convert the RS-423 standard, that originates at the MUX interface, to the RS-232-C standard, thus providing the backward compatibility needed for existing terminals and user I/O devices. Figure 4-1 illustrates the Panel-to-RS-232-C device connections. The Panel provides the necessary EIA RS-232-C Modem signal simulation (CA, CB, CC, CD, and CF) to be used if your terminals or devices require it. A device not requiring the extra protocol lines to operate can operate sufficiently using the Transmitted Data (BA) and Received Data (BB) lines.

In an attempt to keep confusion to a minimum, the discussion that follows separates the MUX-to-device connection and cabling process into three recommended areas, each of which is designed to accomodate the requirements that are most likely to parallel your own requirements:

Case 1

Consider a configuration in which the devices you wish to connect to the MUX are required to be in the local vicinity of the host CPU. "Local" is defined as a 60 foot maximum radius from the host. The use of the HP 12828A RS-232-C Multiplexer Panel, mounted within 10 feet of the CPU, provides a central distribution point to which your I/O devices may be connected within 50 feet.

Thus, this configuration includes the following components: The HP 12792A Multiplexer interface, an HP 12828A RS-232-C Multiplexer Panel, a 10-foot cable (provided with the HP 12828A) between the the MUX and the Panel, your device, and the cable between the Panel and the device. Your responsibility in this configuration includes supplying, of course, the device and the Panel-to-device cable.

Case 2

Now, consider the same configuration as described in Case 1 with the exception that your I/O devices are required to be placed in a remote "cluster" in which the distance to the "cluster" from the host exceeds the 60-foot limitation. "Cluster" or "clustered" refers to the placement or installation of I/O devices (such as terminals and printers) all within a 50-foot radius of the central distribution point such as a HP 12828A RS-232-C Multiplexer Panel. The distribution point or Panel itself may be extended up to 300 feet from the host thus providing a maximum distance of 350 feet. The 50 foot radius restriction (Panel-to-device) is imposed by the RS-232-C standards by which the HP 12828A Multiplexer Panel is designed. There could be up to 100 feet separating any two devices connected to the same Panel.

Six components, therefore, make up this configuration: The five from Case 1 and an additional component, an extension cable, which provides up to 290 feet of extra length inserted between the existing 10 foot MUX-to-Panel cable and the Panel. A connector for each end of this extension is provided with the HP 12828A. Thus, it becomes your added responsibility to fabricate this extension cable.

Case 3

Consider a third type of configuration which involves the elimination of the HP 12828A RS-232-C Multiplexer Panel. Two possible types of connections are suggested: a direct connection from your device to the MUX interface or a connection that would involve a central distribution panel of your own design. One might consider a panel which does not impose the RS-232-C restriction but would implement and pass the RS-423 circuit standards, which are originally observed on the interface, to your I/O devices.

Thus, in Case 3, all components, except the MUX interface and the 80-pin connector provided with it, would be designed and fabricated by you.

Several of the possible Multiplexer system configurations mentioned above involve the fabrication or purchase of cables. The only case in which cable purchase or fabrication is not necessary is through the use of the HP 12828A RS-232-C Panel and the included 3-metre cable.

The following Sections in this chapter will describe in detail the purchases and responsibilities involved in the three configuration cases outlined above.

RS-232-C Panel-to-RS-232-C Device (Case 1)

The HP 12828A RS-232-C Panel is designed to connect eight RS-232-C compatible devices such as terminals, printers and modems to the Multiplexer Interface. Figure 4-2 illustrates the connection of several Hewlett-Packard terminals and line printers to the RS-232-C Panel. The HP cables that can be purchased separately for use with these products are also presented.

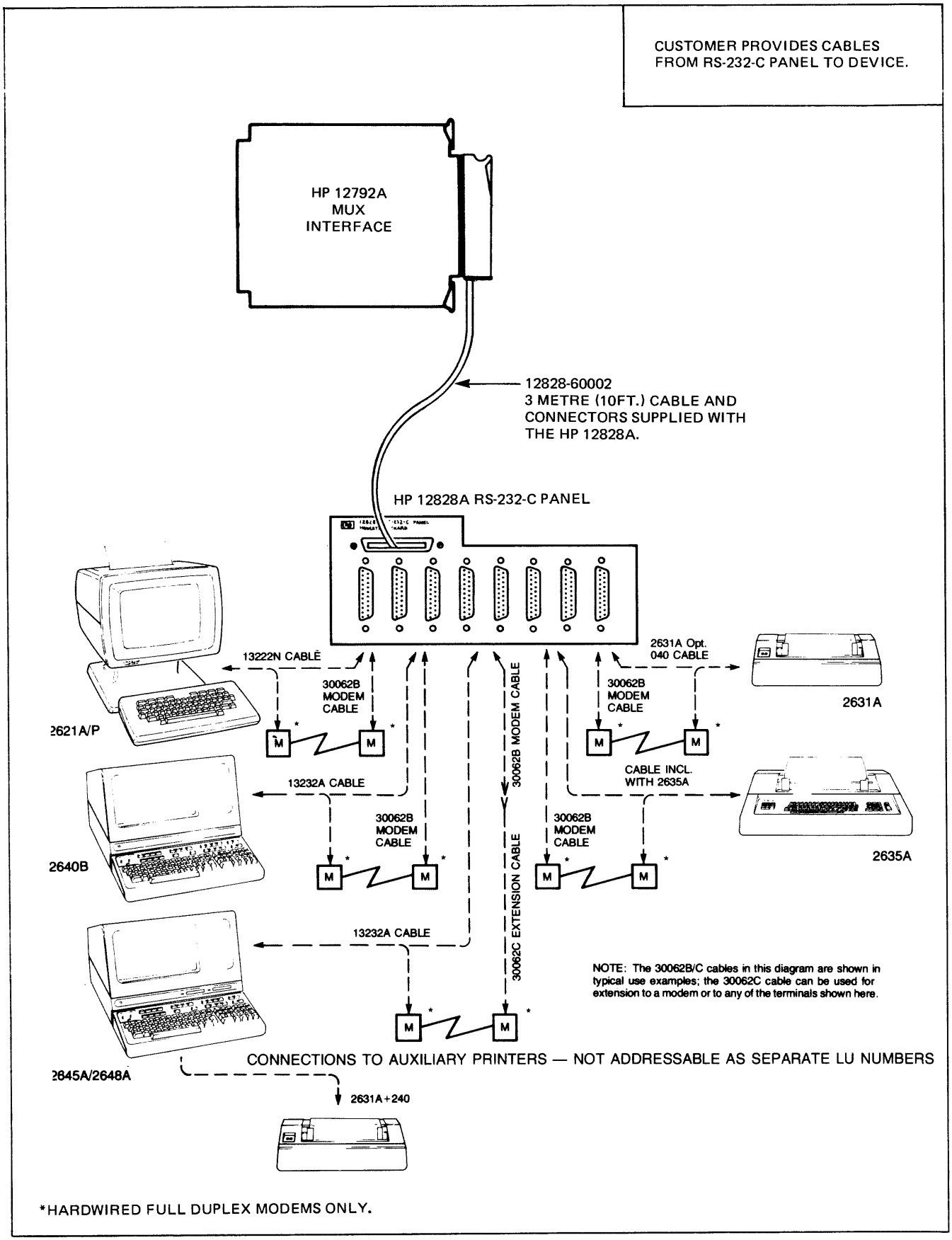


Figure 4-2. Case 1 Configuration Diagram.

Hewlett-Packard manufactures various lengths and types of device cables, some of which are suggested in Figure 4-2. The 13222N cable is a 5 metre (17 ft) cable for connection of a terminal to the HP 12828A RS-232-C Panel. The 13232A cable is a 4.5 metre (15 ft) cable used for the same purpose. They differ only with respect to the type of connectors used on the terminal end of the cable.

For connection of hardwired full-duplex modems to the HP 12828A, the 7.5 metre (25 ft) 30062B cables or the 15.2 metre (50 ft) 30062B, Option 001 cables can be used.

The 30062C RS-232-C Extention cable can be used to extend the distance of the point-to-point or modem cables suggested above.

In the case that you are using an HP 1000 Computer and the Multiplexer Interface with RS-232-C compatible terminals, printers or hardwired full-duplex modems that are not Hewlett-Packard products, or if you wish to use non-standard cable lengths not provided by Hewlett-Packard, you must purchase or fabricate your own RS-232-C Panel-to-device cables.

Figure 4-3 illustrates the RS-232-C Panel device connector pin assignments that are representative of each port, J0 through J7. Note that in keeping with EIA RS-232-C standards when referring to the terminal or I/O device, Received Data (BB) and Transmitted Data (BA) should be referenced with respect to the terminal or device. In other words the Transmitted Data (BA) at the device end is actually the Receive Data (RD-) with respect to the MUX interface. By the same convention, Received Data (BB) at the device is actually Send Data (SD-) at the MUX interface. A standard 25-pin male connector (shown in Figure 4-3) must be attached to the RS-232-C Panel end of the cable and your device compatible connector at the other. It is recommended that such a cable not exceed 15 metres (50 ft) in length by the RS-232-C standard. Figure 4-3 gives the pin-to-signal relationships for the 25-pin connector at the RS-232-C Panel end of the fabricated cable.

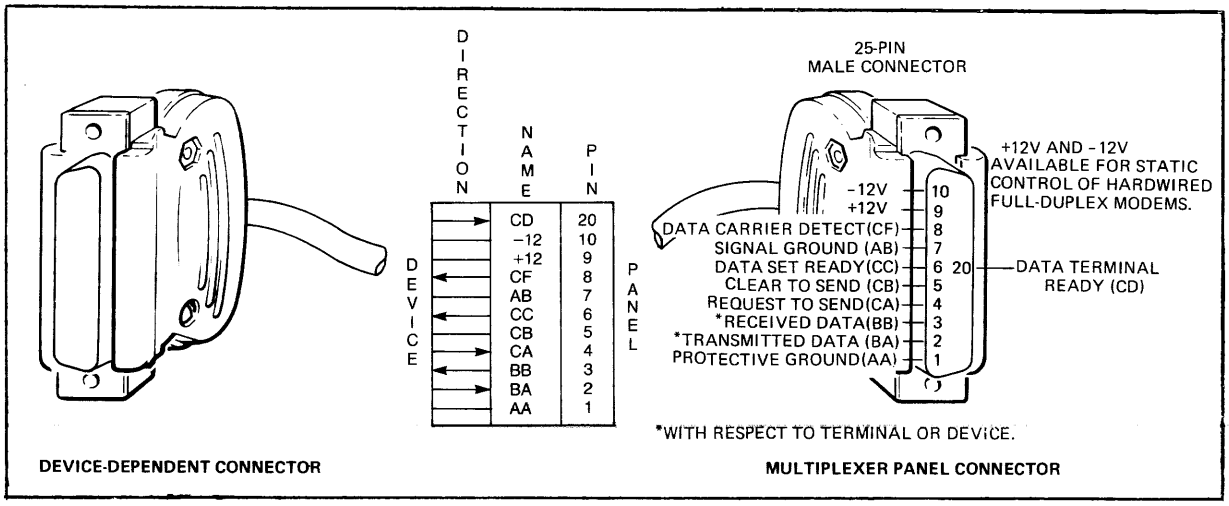


Figure 4-3. RS-232-C Panel-to-Device Cable Wiring Diagram.

A +12 volt line is provided on pin 9 of each RS-232-C Panel connector as well as a -12 volt line on pin 10. These lines are intended for use in providing static control levels to hardwired full-duplex modems. These voltages can be used in situations where a device handshake or control line needs to be permanently tied high or low. The current available at each connector is +/- 0.05 amps. This current is sufficient to drive three control lines.

Extending the MUX Interface-to-Panel Cable (Case 2)

The use of the RS-423 drivers and receivers on the MUX Interface allows the Interface-to-RS-232-C Panel cable to be extended to a maximum total length of 91 metres (300 ft). This extended cable is made up of the 3-metre (10 ft) cable (HP part number 12828-60002) supplied with the HP 12828A RS-232-C Panel and a custom-made 88 metre (290 ft) cable. Your are responsible for fabricating or purchasing this custom 88 metre cable. This extension makes possible a more remote operation of the terminals, printers or hardwired full-duplex modems being used with the interface. Figure 4-4 illustrates this configuration.

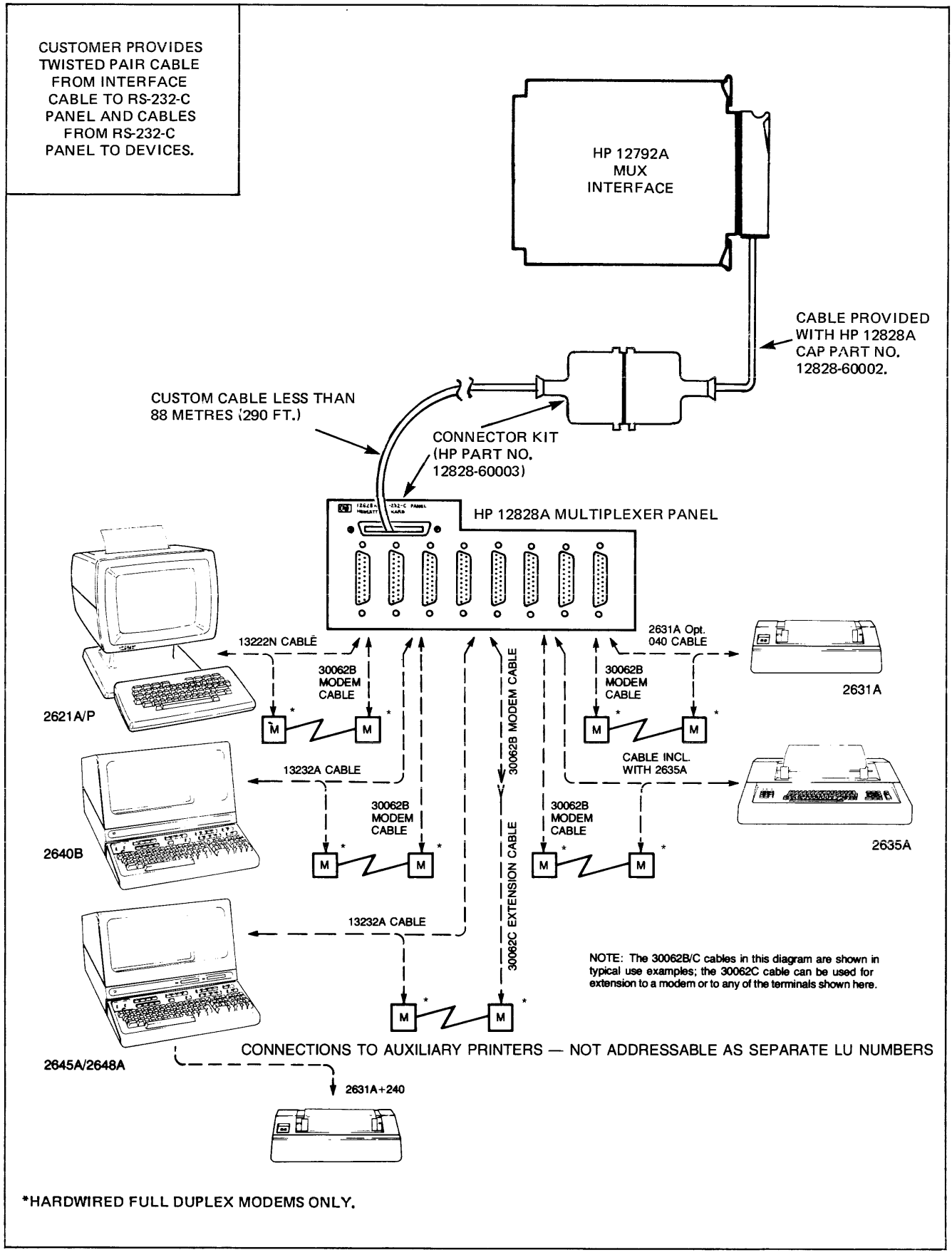


Figure 4-4. Case 2 Configuration Diagram.

Note that the cables connecting the individual devices to the RS-232-C Panel must (as in Case 1) be less than 15 metres (50 ft) in length.

The physical cable should be fabricated from an 18 or 19 twisted-pair conductor, 28 AWG cable (HP part number 8120-3072 or Belden part number 9519), 88 metres (290 ft) or less in length. The connectors used are those provided with the HP 12828A RS-232-C Panel as a kit (HP part number 12828-60003). The kit contains one female connector and one male connector as well as an insertion tool that alleviates the need to solder cable wires to the connectors. Figure 4-4 gives a wiring diagram for use in the construction of the extension cable.

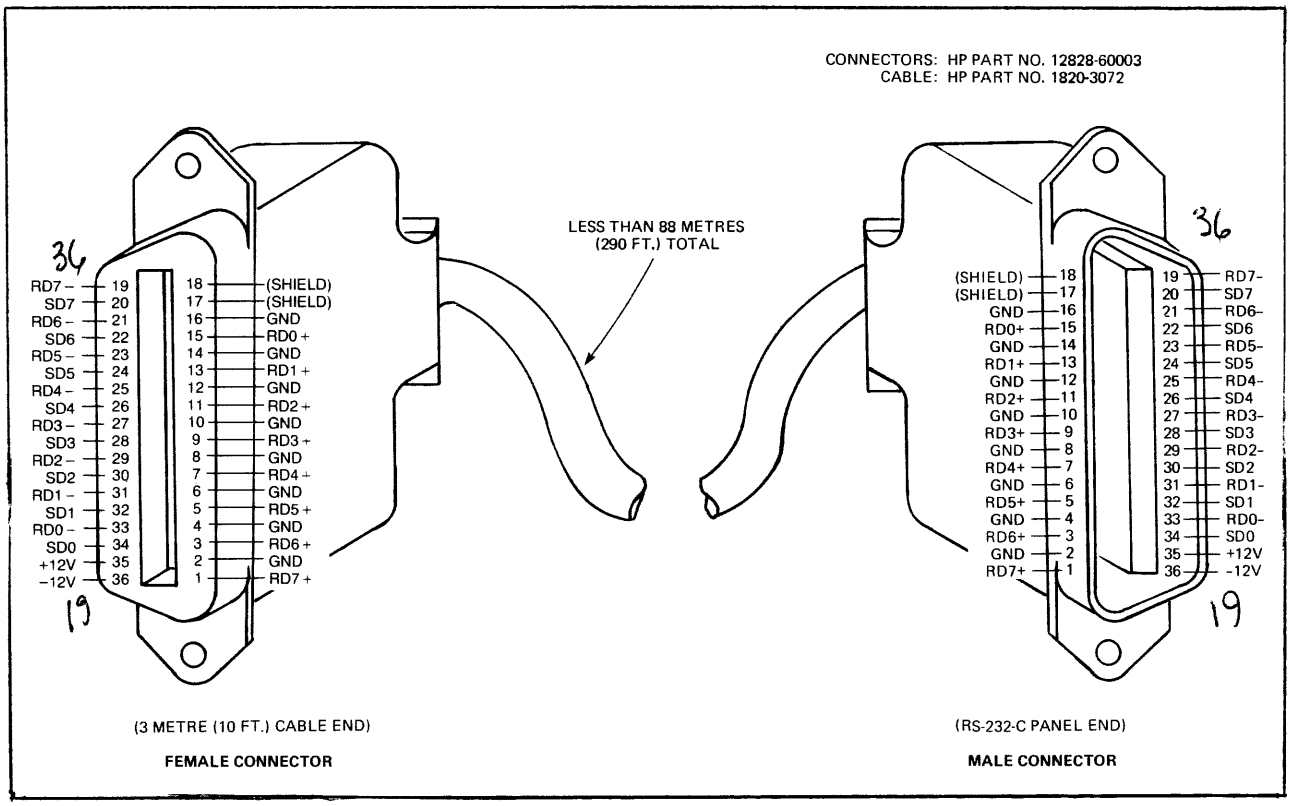


Figure 4-5. Multiplexer Cable Extension Wiring Diagram.

It is recommended that the signal-to-wire color convention implemented in the 3-metre (10 ft) cable be observed for when fabricating the 88-metre extention cable. Each twisted pair of wires contained in the HP and Belden cables observes the following convention:

Each Receive Data pair (receive with respect to the MUX interface) contains a

solid color wire that carries the Receive Data (RD-) signal. The Receive Data common or carrier is a white wire.

Each Send Data (transmit with respect to the MUX interface) contains a striped (solid color and white) wire that carries the Send Data (SD-) signal. The Send Data common or ground (SD+ or GND) carrier is a white wire.

Note that the common/ground wires of both receive and send pairs are white in color. In the standard twisted pair configuration for each channel (one twisted for Receive Data and one twisted pair for Send Data), the white (common) wires from both pairs are connected together once inside the MUX Panel. This wiring convention uses the standard resistor color code in assigning the wire colors to the eight individual channels. The color per channel assignments for the Send and Receive Data wires are as follows:

Channel Number	Receive Data (RD-) color	Send Data (SD-) color
Channel 0	Black	Black-White
Channel 1	Brown	Brown-White
Channel 2	Red	Red-White
Channel 3	Orange	Orange-White
Channel 4	Yellow	Yellow-White
Channel 5	Green	Green-White
Channel 6	Blue	Blue-White
Channel 7	Violet	Violet-White

The two static control lines are carried from the MUX interface with a striped gray-white (+12V) wire and a gray (-12V) wire.

This convention, if followed, should aid in the fabrication and connection process as well as the troubleshooting of the cable.

Direct Connection to RS-232-C Device (Case 3)

The HP 12792A Multiplexer may be directly connected to terminals, printers, hardwired full-duplex modems or user-supplied termination panels, thereby removing the need for the HP 12828A RS-232-C Panel. The backward compatible nature of the RS-423 drivers and receivers with RS-232-C devices makes this possible. The direct connection involves the fabrication of a cable less than 91 metres (300 ft) in length with the 80-pin card connector supplied with the HP 12792A product at one end and up to eight device dependent connectors or a termination panel at the other. This configuration is illustrated in Figure 4-6.

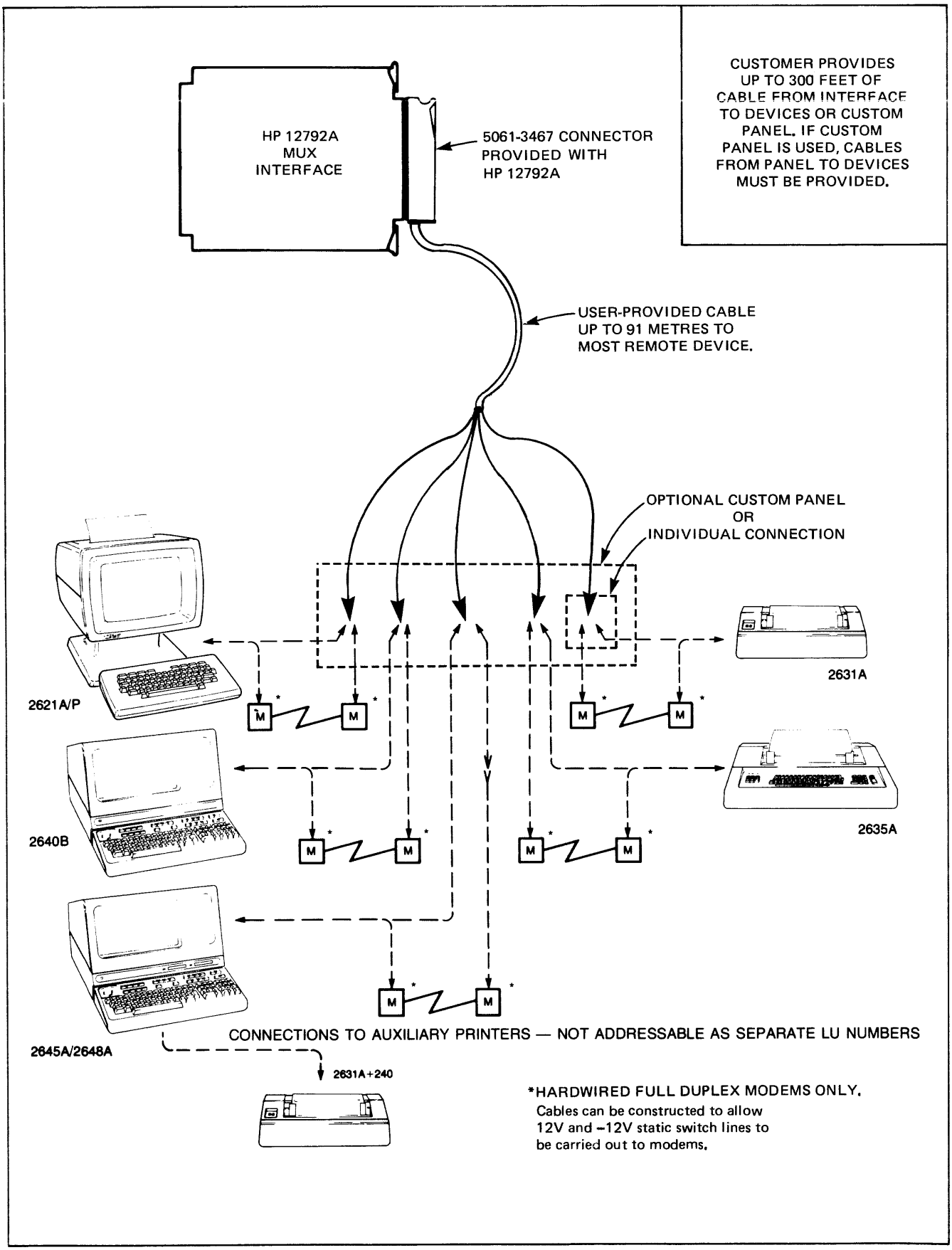


Figure 4-6. Case 3 Configuration Diagram.

Figure 4-7 details the actual fabrication of the cable. Terminals require connection of the Send Data (SD-) signal for data reception, the Receive Data (RD-) signal for data transmission and a signal ground. The Send Data (SD-) and ground signals (SD+) are all that are needed to connect a line printer. Remember that these signal names are referenced in respect to the terminal, printer, or I/O device.

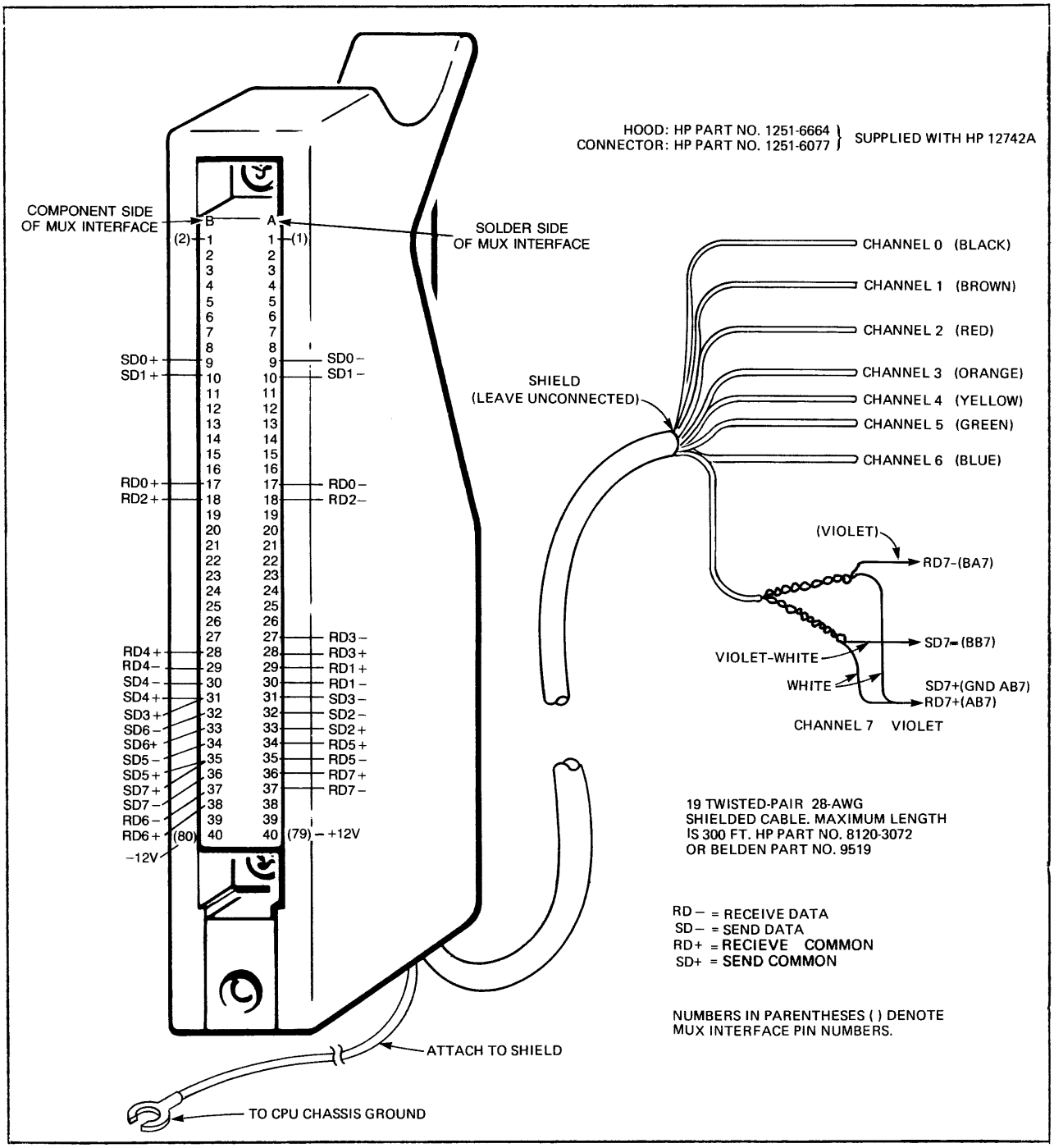


Figure 4-7. Multiplexer Direct Connection Cable.

Physically, this cable is an 18 or 19 twisted-pair conductor, 28 AWG cable (HP part number 8120-3072 or Belden part number 9519), less than 91 metres (300 ft) in length. The MUX interface connector is an eighty-pin hooded connector (supplied with the HP 12972A Multiplexer). This connector contains a

different pin numbering scheme than the MUX interface it connects to. The even-numbered (component) side of the MUX interface corresponds with the side labeled "B" of the connector. The odd-numbered (solder) side of the MUX interface corresponds with the side of the connector labeled "A".

The device connectors will, of course, depend upon the devices being interfaced. Hewlett-Packard terminals require a 30-pin hooded card connector (HP 2640A/B, HP 2645A, HP 2647A, HP 2648A and 2675A), a 50-pin connector (HP 2621A/P) or a standard 25-pin connector (HP 2635A). Hewlett-Packard printers require a 25-pin connector (HP 2631A, 2635A and HP 7310A).

Figure 4-8 illustrates the fabrication of the hooded card connector end the custom cable.

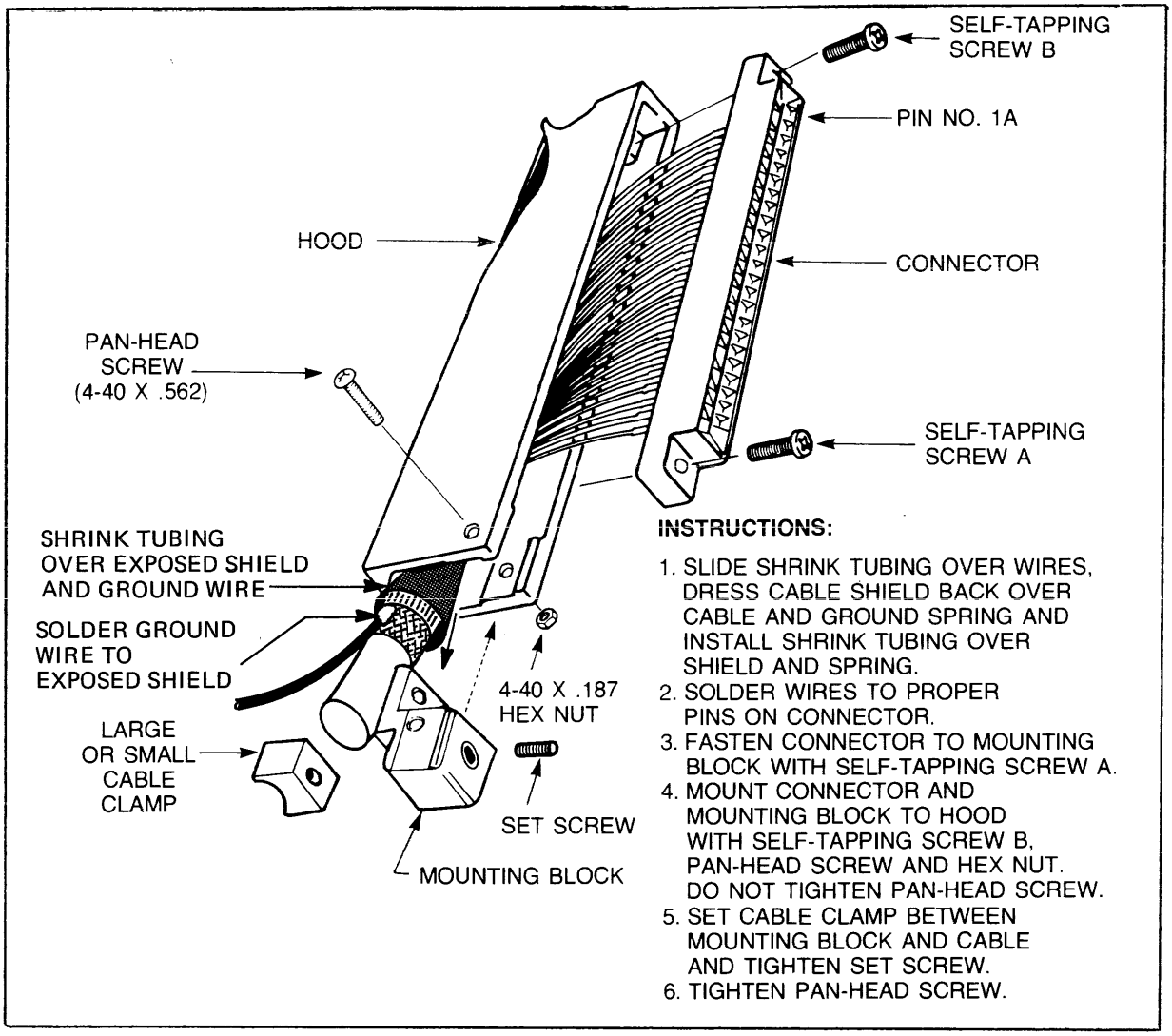


Figure 4-8. 80-Pin Hooded Card Connector Assembly

The same wiring convention explained in Case 2 should be followed in the fabrication of the custom cable. According to the RS-423 standard, the MUX interface Send Data common signals are simply ground connection pins on the edge connector. For instance, the channel 0 Send Data common (SDO+) signal is actually a ground pin on the MUX interface edge connector. This pin is numbered 18 on the interface and 9B on the connector. Note that there are two cases in which one ground pin serves as the Send Data common line for two channels. Pin 31B (62 on the MUX interface) is the Send Data common for channels 3 and 4; pin 35B (70 on the MUX interface) is the Send Data common for channels 5 and 7.

In making the RS-423-to-RS-232-C conversion for your terminal or device, the two common lines, Send Data common and Receive Data common (the white wire in each of the twisted pairs), can be tied together at the terminal or device end.

Static control-level lines for hardwired full-duplex modems are provided. In this case, the +12 volt line is on pin 40A (pin 79 of the MUX interface) and the -12 volt line is on pin 40B (pin 80 of the MUX interface). Because of the length of this cable, the available current at the end of each of the static control lines may be as small as +/- 0.04 amps.

Custom Panel

If the RS-423 (subset of RS-449) standards are observed and followed you can design and construct a RS-423 distribution panel. This may prevent the removal of your existing wiring when the device is in excess of fifty feet from the host or if your the placement and installation of your devices cannot be "clustered".

The RS-423 panel would have to implement the use of twisted pair for both send and receive lines between the panel and the device as well as from the MUX interface to the panel. The common (white) wires for each function would not be permitted to be tied together at the panel but instead passed through to the device, thus providing the needed differential operation between the host and the device. Good shielding and grounding practices should also be followed.

Data Transmission Rate Wiring

There are two hardware baud-rate generators on the Multiplexer Interface. The outputs of these two baud rate generators are distributed to the eight asynchronous communications channels in a manner such that some of the channels will operate at one baud rate and the rest at another. This distribution is hardwired through the use of jumpers in the Multiplexer Interface hooded card connector. You can rearrange the jumpers at any time (that the Multiplexer Interface is not in use) to suit your needs.

The host software interface driver allows you to programmatically set the rate of each of the two baud rate generators. The combination of the software selectable rate and the hardwired distribution of the baud rate generator outputs gives you great flexibilty. But remember, only two DIFFERENT baud rates can be distributed to the eight communications channels.

For example, consider a typical system configuration in which seven terminals and one line printer are used with the Multiplexer. The terminals assigned to Channels 1 through 7, are connected to one baud rate generator producing a data transmission rate of 9600 baud and the line printer, assigned to Channel 0, is connected to the other baud rate generator resulting in a data transmission rate of 300 baud. This configuration is physically brought about by connecting wire jumpers on the Multiplexer card connector as illustrated in Wiring Option 1 in Figure 4-9. (The Multiplexer card connector is wired at the factory in this configuration.) The actual baud rates of 300 and 9600 are set by the user through the interface software driver. The process of setting the baud rates through the interface driver is covered in depth in the HP 12792A Multiplexer Subsystem User's Manual, HP part number 12792-90002. The rest of the essential internal timing wiring remains constant as shown in Option 1 diagram of Figure 4-9.

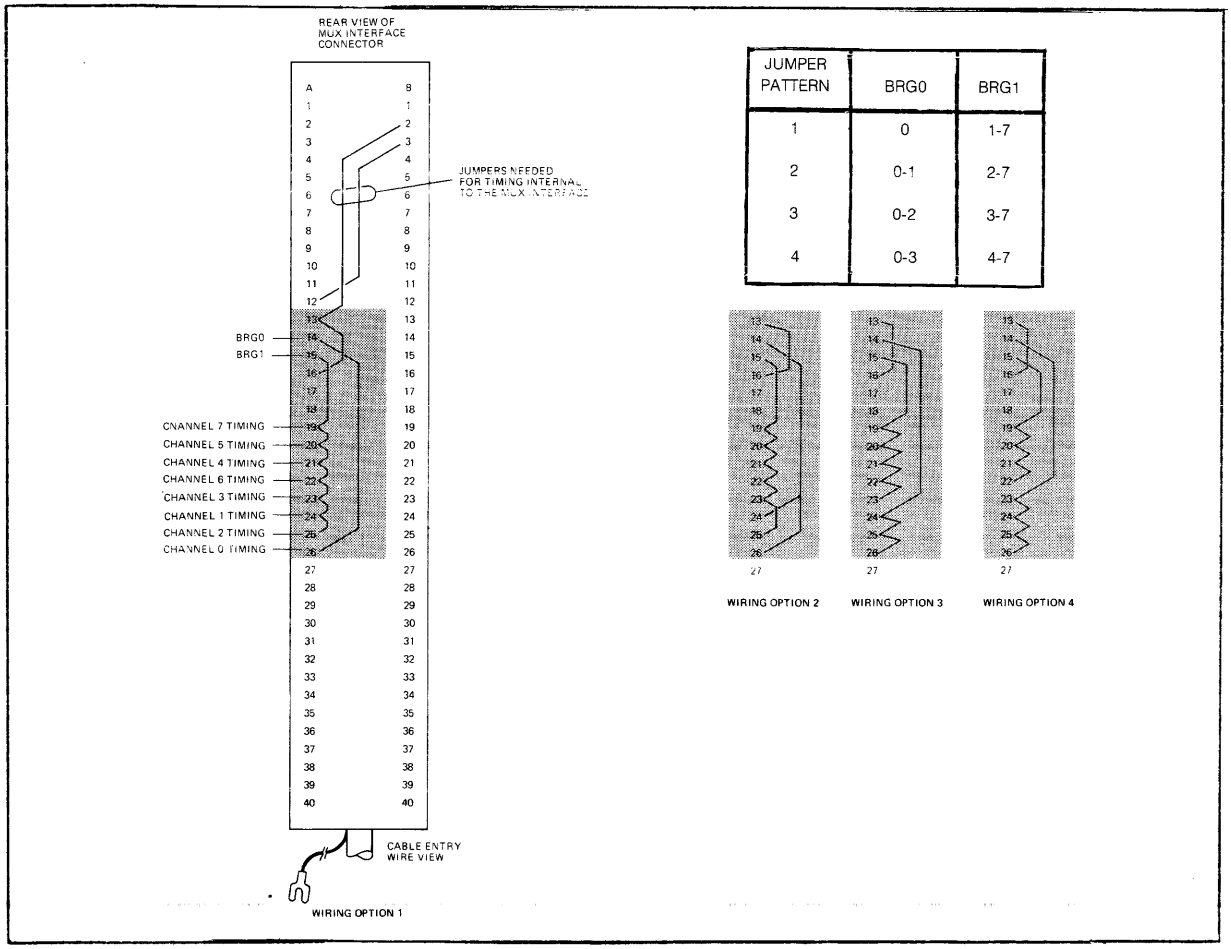


Figure 4-9. Data Rate Generator Wiring.

Wiring Option 2 illustrates the wiring of the connector for the configuration in which two devices operate at one baud rate and six devices at another. Wiring Option 3 distributes one baud rate to three devices and the other baud rate to the remaining five devices. Wiring Option 4 distributes the baud rates evenly, four and four.

Software vs. Hardware Handshaking

The HP 12792A MUX Subsystem implements the host-to-device and device-to-host communication handshaking through MUX software/firmware only. Devices requiring hardware handshaking may have to be modified. One way to acheive this is to construct a serial logic control circuit that sends and receives the needed software handshake words. The circuit would be connected to the device's hardware handshake logic and have access to the send and receive data lines used by the device.

Chapter 5
Maintenance/Diagnostics

Introduction

This chapter should be consulted for reference regarding the following topics:

* Maintenance Procedures
* Testing/Diagnostic Procedures
* Basic Troubleshooting Techniques

Preventive Maintenance

There is no preventive maintenance (PM) required for the HP 12792A Multiplexer Subsystem other than a routine inspection of interface, cables, etc. This should be performed as part of the entire HP 1000 system PM. At that time, the interface and cables should be visually inspected for loose or broken components, or the presence of foreign objects. The following MUX Interface Tests/Diagnostics should only be performed when a failure is suspected in the MUX hardware.

Two methods exist to verify proper operation of the Multiplexer hardware subsystem:

* The Echoplex Verification Test
* The Off/On-line Functional Diagnostics

More information regarding these tests is provided in the following paragraphs.

Echoplex Verification Test

The purpose of the Echoplex Verification Test is to confirm the basic integrity of the MUX interface. When performing power-up or PRESET, the MUX interface enters an echoplex mode. This enables the Z-80 subsystem, resident on the interface, to accept typed characters from terminals connected to any of its eight ports. The interface then processes the character(s) and echoes the character(s) back to the initiating terminal. As a result of this echo feature, any cables, panels, or terminals attached to the MUX interface are also tested as they provide the essential path by which the echo is accomplished.

This test is capable of testing the Z-80A CPU and subsystem (ROM, RAM, SIO, and CTC and all associated support circuitry), however, it is not capable of confirming the integrity of the communication path between the host computer and the MUX interface, i.e., the input and output data/control/status latches and the DMA circuitry.

The term "test" refers to a Go/No Go test that, when executed, provides 75% assurance or confidence that the hardware operates correctly as specified. This percentage figure is only an approximation and relates to the amount, as well as the importance, of the circuitry that is tested. The Echoplex test, though providing limited confidence, is quick and easy to perform and requires a minimal amount of additional equipment and set-up effort. It should be performed only as an initial check for the interface and associated hardware.

Preparation and Required Hardware

Before the test can be performed, one to eight terminals (HP 2645's, 2621's, etc.) must be connected to the MUX interface with a cable of your own design or the HP 12828A RS-232-C MUX Panel/cable and the appropriate RS-232-C compatible terminal cable(s). Consult chapter four of this manual if detailed cabling or baud rate configuration information is needed.

Reviewing chapter three, recall that two programmable baud rate generators (BRGs), resident on the MUX interface, are responsible for controlling the data transmission speed of all eight channels (ports). The physical connection between the BRGs and each of the eight ports is made in the cable connector (at the MUX interface end of the cable).

Both BRGs are initialized upon powering-up or after pressing PRESET. That is, BRG0 (baud rate generator number 0) will default to 2400 baud and BRG1 will default to 9600 baud. Thus, depending upon the BRG connections made inside the connector, each of the eight ports can be configured for either 2400 or 9600 baud. Note that the cable and connector supplied with the HP 12828A MUX Panel is wired so that channel 0 is connected to BRG0 while channels 1 through 7 are wired to BRG1. As previously stated, you can simply rewire this connector to obtain the desired baud rate/channel distribution.

Ensure that each terminal's baud rate setting is the same as that of the MUX interface port it is connected to. Also, the terminal(s) must be in the REMOTE mode.

Execution

After the desired number of terminals have been connected to the interface to be tested, you must either press PRESET or cycle the AC power on the host computer. This will initialize the echo mode as previously discussed. The following default conditions exist on the MUX interface as a function of power-up or PRESET:

* All ports are initialized to - Edit and Echo modes.
  - 8 bits/character.
  - 1 stop bit/character.
  - No parity.

* Baud rate generators default - BRG0 = 2400 baud
  - BRG1 = 9600 baud

The rest is up to you! As you type on any of the terminal keyboards, characters are sent to the MUX interface, processed by the Z-80 subsystem, then immediately sent back to the intiating terminal for your inspection. Characters should appear exactly as they are typed. You may wish to type in several ASCII combinations as well as perform the edit features (line delete and backspace) available in this mode.

Troubleshooting

Note that if the terminal is configured for LOCAL mode it may appear to pass this test, however this does not test the MUX interface and supporting hardware in this configuration.

If characters are not echoed back properly, a quick check of the following items may save troubleshooting time:

* Are MUX interface and supporting hardware correctly installed?

  Is the interface inserted all the way into the backplane of the host?

  Are the cabling connections (BRG-to-ports and input/output data lines) wired correctly for the ports you are using?

  Is there power supplied to the interface from the host CPU?

Did you intialize the echo test by pressing PRESET or by cycling the host computer power?

* Is the terminal correctly connected and configured?

  Is the cable properly connected to the terminal?

  Is the terminal set to the REMOTE mode and the baud rate correctly configured?

  Is there cause to suspect a failure in the terminal? Does the terminal operate correctly in other applications including connection to an HP 1000 computer under RTE?

MUX Status After Testing

The MUX interface will remain in the initialized (uninitialized from an operating system point of view) after power-up or PRESET until the driver software or system "welcome" commands are executed as a function of the RTE operating system. Thus the MUX hardware/firmware subsystem will not respond to operating software without first performing the proper control requests to the interface from the driver or an assembly language program. Consult the Multiplexer User's Guide for further details regarding MUX interface initialization from a driver.

Off-Line/On-Line Functional Diagnostic (MUXST)

If you require more than a minimum of functional assurance for MUX interface operation, a high level interface diagnostic may be performed as a function of the on-line RTE-IVB operating system or the off-line RTE-MIII system.

The term "diagnostic", with regard to the MUX Subsystem, is defined as a series of high level Go/No Go Z-80A assembly language tests which are performed by the Z-80A CPU and its subsystem. A total of 13 tests are performed on the following individual circuits and fuctional areas: Z-80A CPU, EPROM, RAM, Z-80A DMA, Z-80A CTC, and Z-80A SIO (ports 0-7).

The Z-80 object code for these individual tests are downloaded into the MUX RAM from the host CPU as a function of the diagnostic and its host operating system. This is achieved after the diagnostic program sends a download command to the MUX firmware.

The mini-cartridge tape (HP part number 12792-13302) included as part of the HP 12792A product contains two forms of this diagnostic, %MUXST and !MUXST, for use with RTE-IVB and RTE-MIII operating systems, respectively. Both versions are identical in the manner with which the MUX hardware subsystem is tested and you are provided with the flexibility of "on-line" or "off-line"

testing. In other words, if you need to test the MUX hardware while operating under the disc based RTE-IVB system, the relocatable file %MUXST can be loaded and exececuted. If your operating system is memory based (RTE-MIII) or if your RTE-IVB system is not up and running, the binary absolute file, !MUXST, can be loaded and executed.

The basic MUXST diagnostic can be broken up into two parts:

(1) "SLFTT", the series of tests which are downloaded into and executed out of MUX interface RAM.

(2) "DIAG", the HP-1000 assembly language program which provides the method to download the Z-80 code from the host and the conversational mode with which you can interact with the diagnostic.

The MUX firmware (ROM), in conjunction with the downloaded Z-80 object code in the MUX RAM, provides the necessary intelligence to execute the series of tests. The MUX then passes the results of these tests back to the calling program, DIAG, in the host computer.

The loading and executing of both %MUXST and !MUXST are further discussed in following paragraphs.

On-line Diagnostic (%MUXST)

Required Hardware

The On-line diagnostic (%MUXST) is supplied on mini-cartridge (HP part number 12792-13302) as part of the HP 12792A. An HP 1000 M, E, or F-Series computer system generated with a RTE-IVB operating system must be used to load and execute %MUXST. The next step is to identify a proper input device for your HP 1000 system. An HP 2645 or equivalent terminal with cartridge tape unit (CTU) must be used. Most terminals of this nature require an HP 12966A (the Buffered Asynchronous Communications Interface) to serve as the host interface. DVR05 (software driver for the HP 12966) should already be generated into your RTE-IVB operating system.

No reconfiguration to the interface is necessary, however, all channels(ports) on the interface are required to be wired to one or both of the baud rate generators. Refer to 'Preparation and Required Hardware' for the "Echoplex Verification Test" in this chapter, if needed, for details regarding the connection of the ports to BRGs. Since the MUXST diagnostic configures both BRGs to a 9600 baud rate, the method of distribution of the ports-to-BRGs is not important as long as all ports are connected to one BRG the other.

Loading %MUXST

Once the input device and the LU number of the CTU is selected, you are ready to store %MUXST onto an available private, group, or system disc cartridge. Make sure that the session switch table (SST), identified with your log-on account, contains the proper LU and EQT entries for the CTU you intend to use.

The first file of this cartridge contains a directory list. Obtain the file number of %MUXST by inspecting this directory, then position the tape to the beginning of that file. After the tape is in position, you are ready to store %MUXST into the system. To accomplish this, use the following RTE-IVB File Manager command:

```
:ST,LU#,%MUXST::CR#,BR
```

where LU# represents the LU of the CTU and CR# is the disc cartridge on which you wish to store %MUXST.

Once stored onto a disc cartridge in your computer system, %MUXST can be loaded by executing the following command:

```
:RU,LOADR,,%MUXST

        or

:RU,LOADR
  /LOADR:    RE,%MUXST
```

Further information regarding LOADR can be obtained by reviewing the RTE-IVB System Manager's Manual.

Executing %MUXST (DIAG)

After a successful load, you will now be able to run the diagnostic. The name of the program set up on the system cartridge by the LOADR is called DIAG. DIAG can be run from a MUX terminal or any other terminal including the the system console.

NOTE: IMPORTANT!!

CURRENTLY ACTIVE SESSIONS ON ALL TERMINALS OR DEVICES CONNECTED TO THE MUX INTERFACE UNDER TEST SHOULD BE TERMINATED BEFORE RUNNING DIAG!!!!!

To run DIAG, simply type: RU,DIAG.

DIAG begins execution by entering an interactive mode. It will ask you for the select code of the multiplexer card you intend to test. After you type in a satisfactory response, the series of Z-80 tests are downloaded from the host to the interface under the supervision of DIAG. The host interrupt system is turned off during the download and the MUX control flip flop is cleared, thus keeping the MUX software driver from recognizing any activity associated with the interface. DIAG now allows approximately 4 seconds for the MUX to complete the series of downloaded tests, at which time it looks at the status of the MUX flag. If the flag is not set, DIAG concludes that the self test has failed. If the flag is set, the result of the tests is read from the backplane latches on the MUX in the form of a number. DIAG interprets this number and responds by displaying any one of 4 different messages to the console from which the test is run:

1. 'MUX TEST PASSED'

2. 'NO RESPONSE FROM THE MUX'

   This message will indicate that DIAG cannot communicate with the MUX board. You should first check to see that you have entered the correct select code for the board under test. If you have, you must assume the board failed.

3. 'MUX TEST NUMBER #N FAILED'

   This message indicates failure of at least one of the components on the MUX interface. A test failure may occur because of an LSI chip or support circuit for that chip that has failed. #N indicates failures as follows:

#N	TEST FAILED
1	Z-80A CPU
2	EPROM
3	RAM
4	Z-80A DMA
5	Z-80A CTC
6	Z-80A SIO Port 7
7	Z-80A SIO Port 6
8	Z-80A SIO Port 5
9	Z-80A SIO Port 4
10	Z-80A SIO Port 3
11	Z-80A SIO Port 2
12	Z-80A SIO Port 1
13	Z-80A SIO Port 0
14	MUX-to-host latch circuitry

Note that if the Z-80A CPU, EPROM, or RAM has failed, a 'NO RESPONSE FROM MUX' message is likely since the intelligence to execute these tests originates from these same circuits.

4. 'MUX LOOPING IN TEST NUMBER #N'

   A failure of the test #N is indicated where #N has the same meaning as above.

   This failure may occur under certain failures of the SIO chips or if the cable hood is not attached to the board.

   An attempt to restart DIAG immediately after receiving this error message may result in the erroneous error message, 'NO REPONSE FROM MUX'. This is because the MUX is still looping as a result of the last attempt to test it, however, an additional attempt to run DIAG should result in the proper error message. This is the only condition in which this error will result.

MUX Status After Execution

The execution of DIAG leaves all eight MUX ports initialized to their default configuration by the MUX firmware after the tests have completed. If DIAG is initiated from one of the MUX ports under test, that port will be active after the completion of DIAG. The remaining ports will still remain in their default states. Reinitialization for all ports takes place after the RTE-IVB software driver resets the IDs for each port. This can be achieved by performing a file manager control request ('CT') using a function code of 30B to the inactive ports.

Even though it is possible to initiate DIAG from one of the MUX ports under test, it is suggested that you use another terminal not connected to that MUX.

Off-line Diagnostic (!MUXST) Loading/Execution

If you do not have the RTE-IVB operating system or wish to test the MUX in a stand alone fashion, !MUXST (included on mini-cartridge tape (HP part number 12792-13302) may be loaded and executed.

If not already familiar with MUXST and the on-line version, %MUXST, it is suggested that you review the preceding paragraphs before proceeding.

The body of the stand-alone diagnostic !MUXST and its on-line counterpart %MUXST, is identical in function, but the two differ slightly in configuration within their respective operating systems. The stand-alone diagnostic (called DIAG) is hosted by an RTE-MIII operating system and both are included in the

!MUXST file. This binary absolute file is loaded into the computer using an absolute binary loading device; in this case, a mini-cartridge tape unit.

Required Hardware

The required hardware includes an HP 1000 M, E, or F-Series Computer equipped with at least 32K bytes of memory, the Memory Protect and DCPC options, HP 12966A interface, and an HP 12992A mini-cartridge loader ROM (HP part number 1816-0587). The loader ROM should be installed in one of the available loader ROM sockets on the HP 1000 CPU board. A system console, which doubles as the diagnostic input device, should be a terminal equipped with a cartridge tape unit (CTU) for loading the mini-cartridge tape file !MUXST.

Loading !MUXST

Power-up both the host CPU and the system console. Referencing the index (first file) on tape (HP part number 12792-13302), obtain the file number for !MUXST, then position the tape to that file by using the softkey or off-line control functions for the CTU.

On the front panel of the host CPU, set the S-register as follows: bits 15 and 14 (either 00, 01, 10, or 11) for the correct address of the HP 12992C loader ROM, bits 11 thru 6 to the select code of the system console, and bits 13, 12, and 5-0 to zero. Be sure to press the STORE button after these bits are set.

Now Press PRESET, then IBL, then RUN.

The !MUXST file will be read into the host memory. A successful load is indicated by a halt code of 102077B in the display register. This may take several minutes. Any other halt code indicates an unsuccessful load.

Executing !MUXST (DIAG)

After !MUXST has been successfully loaded, you are required to store the select code of the console in bits 5-0 of the S-register. All other bits in the S-register must be set to zero.

Reset the program pointer by storing an octal 2 into the P-register, then press PRESET and RUN. DIAG will begin execution and again, like its on-line counterpart, is completely interactive. DIAG asks for the select code of the MUX interface you intend to test. After a correct reply, DIAG will download the Z-80 object code into the MUX RAM for execution. The tests and the messages which result from the tests are identical to the on-line version (%MUXST) described earlier in this chapter. Refer to these sections for a description of the possible messages and meanings. After DIAG has completed, it may be restarted by typing: RU,DIAG.

Should DIAG, for any reason, seem to hang up or not respond, you can abort it

by typing, "OF,DIAG,1". You can then attempt to restart it by typing: RU,DIAG.

Chapter 6
Servicing Diagrams and Information

Introduction

This Chapter contains the following information tables and servicing diagrams:

* M/E/F-Series/MUX interface backplane connections (P1 connector)
* MUX interface device communication lines connections (J1 connector)
* RS-232-C MUX Panel 36-pin (J8) and 25-pin connections (J0 through J7)
* Serial I/O Circuits and Equivalents
* Integrated Circuit Base Diagrams for the MUX interface components
* MUX interface Parts Location Diagram
* MUX interface Schematic Diagrams
* RS-232-C MUX Panel Schematic Diagram

Table 6-1. Host Backplane (MUX I/F connector P1) Pin Assignments

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME
1	GND	Ground
2	GND	Ground
3	PRL	Priority Low
4	FLAGL	Flag Signal, Lower Select Code
5	SFC	Skip if Flag is Clear
6	IRQL	Interrupt Request, Lower Select Code
7	CLF	Clear Flag
8	IEN	Interrupt Enable
9	STF	Set Flag
10	IAK	Interrupt Acknowledge
11	T3	I/O Time Period 3
12	SKF	Skip on Flag

Table 6-1. Host Backplane (MUX I/F connector P1) Pin Assignments (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME
13	CRS	Control Reset
14	LSCM	Select Code Most Significant Digit (Lower Address)
15	IOG	I/O Group
16	LSCL	Select Code Least Significant Digit (Lower Address)
17	POPIO	Power On Preset to I/O
18	BIOS	"Not" Block I/O Strobe (E-series only)
19	SRQ	Service Request
20	IOO	I/O Data Output Signal
21	CLC	Clear Control
22	STC	Set Control
23	PRH	Priority High
24	IOI	I/O Data Input Signal
25	SFS	Skip if Flag is Set
26	IOBI 0	I/O Bus Input, bit 0
27	IOBI 8	I/O Bus Input, bit 8
28	IOBI 9	I/O Bus Input, bit 9
29	IOBI 1	I/O Bus Input, bit 1
30	IOBI 2	I/O Bus Input, bit 2
31	IOBI 10	I/O Bus Input, bit 10
32	SIR	Set Interrupt Request
33	IRQH	Interrupt Request (Higher Select Code)
34	HSCL	Select Code Least Significant Digit (Higher Address)
35	IOBO 0	I/O Bus Output, bit 0
36	+28 Volts	
37	HSCM	Select Code Most Significant Digit (Higher Address)
38	IOBO 1	I/O Output Bus, bit 1
39	+5V	
40	+5v	
41	IOBO 2	I/O Bus Output, bit 2
42	IOBO 4	I/O Bus Output, bit 4
43	+12V	
44	+12V	
45	IOBO 3	I/O Bus Output, bit 3
46	ENF	Enable Flag
47	-2V	
48	-2V	
49	FLGH	Interrupt Flag Signal (Higher Select Code)
50	RUN	Run
51	IOBO 5	I/O Bus Output, bit 5

Table 6-1. Host Backplane (MUX I/F connector P1) Pin Assignments (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME
52	IOBO 7	I/O Bus Output, bit 7
53	IOBO 6	I/O Bus Output, bit 6
54	IOBO 8	I/O Bus Output, bit 8
55	IOBO 11	I/O Bus Output, bit 11
56	IOBO 9	I/O Bus Output, bit 9
57	IOBO 12	I/O Bus Output, bit 12
58	IOBO 10	I/O Bus Output, bit 10
59	NOT USED	
60	IOBI 11	I/O Bus Input, bit 11
61	IOBO 13	I/O Bus Output, bit 13
62	EDT	End Data Transfer (DCPC)
63	NOT USED	
64	IOBI 3	I/O Bus Input, bit 3
65	IOBO 14	I/O Bus Output, bit 14
66	PON	Power On Normal
67	BIOO	"Not" Block I/O Output (E-Series Only)
68	NOT USED	
69	-12V	
70	-12V	
71	NOT USED	
72	NOT USED	
73	BIOI	"Not" Block I/O Input (E-Series Only)
74	IOBO 15	I/O Bus Output, bit 15
75	NOT USED	
76	NOT USED	
77	IOBI 4	I/O Bus Input, bit 4
78	IOBI 12	I/O Bus Input, bit 12
79	IOBI 13	I/O Bus Input, bit 13
80	IOBI 5	I/O Bus Input, bit 5
81	IOBI 6	I/O Bus Input, bit 6
82	IOBI 14	I/O Bus Input, bit 14
83	IOBI 15	I/O Bus Input, bit 15
84	IOBI 7	I/O Bus Input, bit 7
85	GND	Ground
86	GND	Ground

Table 6-2. MUX interface device communication lines connector (J1)

LEGEND: > = OUTPUT FROM MUX INTERFACE
< = INPUT TO MUX INTERFACE
( ) = MUX INTERFACE CABLE CONNECTOR PIN NUMBER
EIA = DENOTES EIA RS-423 SIGNAL

MUX INTERFACE AND CABLE CONNECTOR PINOUTS BOTH GIVEN

TTL IS IMPLIED WHEN NO LOGIC LEVEL IS GIVEN

MUX INTERFACE CIRCUIT SIDE				MUX INTERFACE COMPONENT SIDE			
PIN		LABEL	NOTE	PIN		LABEL	NOTE
1	(1A)	+5V		2	(1B)	GND	
3	(2A)	+5V		4	(2B)	SCLK	1.843 MHz >
5	(3A)	+5V		6	(3B)	FCLK	7.373 MHz >
7	(4A)	+5V		8	(4B)	PNLIN	TTL <
9	(5A)	BLANK		10	(5B)	PNLIN	GND
11	(6A)	PNLOUT	TTL >	12	(6B)	PNLOUT	GND
13	(7A)	CLK'	3.686MHz >	14	(7B)	GND	GND
15	(8A)	ENABL	LED DRIVER >	16	(8B)	GND	GND
17	(9A)	SDO	EIA >	18	(9B)	GND	GND
19	(10A)	SD1	EIA >	20	(10B)	GND	GND
21	(11A)			22	(11B)	SDO+	GND
23	(12A)	TIMSTRB	TTL <	24	(12B)	SD1+	GND
25	(13A)	CLK1	CTC1 IN <	26	(13B)	GND	GND
27	(14A)	BRGO	CTCO OUT >	28	(14B)	GND	GND
29	(15A)	BRG1	CTC1 OUT >	30	(15B)	GND	GND
31	(16A)	CLKO	CTCO IN <	32	(16B)	GND	GND
33	(17A)	RDO-	EIA <	34	(17B)	RDO+	EIA <
35	(18A)	RD2-	EIA <	36	(18B)	RD2+	EIA <
37	(19A)	T7	TTL <	38	(19B)	T7	GND
39	(20A)	T6	TTL <	40	(20B)	T6	GND
41	(21A)	T5	TTL <	42	(21B)	T5	GND
43	(22A)	T4	TTL <	44	(22B)	T4	GND
45	(23A)	T3	TTL <	46	(23B)	T3	GND
47	(24A)	T2	TTL <	48	(24B)	T2	GND
49	(25A)	T1	TTL <	50	(25B)	T1	GND
51	(26A)	TO	TTL <	52	(26B)	TO	GND
53	(27A)	RD3-	EIA <	54	(27B)	GND	GND
55	(28A)	RD3+	EIA <	56	(28B)	RD4+	EIA <
57	(29A)	RD1+	EIA <	58	(29B)	RD4-	EIA <
59	(30A)	RD1-	EIA <	60	(30B)	SD4-	EIA >
61	(31A)	SD3-	EIA >	62	(31B)	SD3+,4+	GND
63	(32A)	SD2-	EIA >	64	(32B)	SD6-	EIA >
65	(33A)	SD2+	GND	66	(33B)	SD6+	GND

Table 6-2. MUX interface device communication lines connector (J1)(CONTIUED)

MUX INTERFACE CIRCUIT SIDE				MUX INTERFACE COMPONENT SIDE			
PIN		LABEL	NOTE	PIN		LABEL	NOTE
67	(34A)	RD5+	EIA <	68	(34B)	SD5-	EIA >
69	(35A)	RD5-	EIA <	70	(35B)	SD5+,7+	GND
71	(36A)	RD7+	EIA <	72	(36B)	SD7-	EIA >
73	(37A)	RD7-	EIA <	74	(37B)	RD6-	EIA <
75	(38A)	BLANK		76	(38B)	RD6+	EIA <
77	(39A)	+12V		78	(39B)	BLANK	
79	(40A)	+12V		80	(40B)	-12V	

Table 6-3. RS-232-C MUX Panel Connector Pinouts

36-PIN J8 CONNECTOR	SIGNAL MNEMONIC	SIGNAL FUNCTION
(MUX interface port)	(with respect to MUX interface)	
PIN NUMBER		
1	RD7+	RECEIVE DATA COMMON
2	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
3	RD6+	RECEIVE DATA COMMON
4	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
5	RD5+	RECEIVE DATA COMMON
6	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
7	RD4+	RECEIVE DATA COMMON
8	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
9	RD3+	RECEIVE DATA COMMON
10	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
11	RD2+	RECEIVE DATA COMMON
12	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
13	RD1+	RECEIVE DATA COMMON
14	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
15	RD0+	RECEIVE DATA COMMON
16	GND (SD+)	SIGNAL GROUND (SEND DATA COMMON)
17	GND*	FRAME GROUND (CABLE SHIELD)
18	GND*	FRAME GROUND (CABLE SHIELD)
19	RD7-	RECEIVE DATA
20	SD7-	SEND DATA

Table 6-3. RS-232-C MUX Panel Connector Pinouts

36-PIN J8 CONNECTOR	SIGNAL MNEMONIC	SIGNAL FUNCTION
(MUX interface port)	(with respect to MUX interface)	
PIN NUMBER		
21	RD6-	RECEIVE DATA
22	SD6-	SEND DATA
23	RD5-	RECEIVE DATA
24	SD5-	SEND DATA
25	RD4-	RECEIVE DATA
26	SD4-	SEND DATA
27	RD3-	RECEIVE DATA
28	SD3-	SEND DATA
29	RD2-	RECEIVE DATA
30	SD2-	SEND DATA
31	RD1-	RECEIVE DATA
32	SD1-	SEND DATA
33	RD0-	RECEIVE DATA
34	SD0-	SEND DATA
35	+12V	STATIC CONTROL VOLTAGE
36	-12V	STATIC CONTROL VOLTAGE

25-PIN CONNECTOR	SIGNAL MNEMONIC	SIGNAL FUNCTION
(Device ports J0-J7)	(with respect to Terminal or I/O Device)	
PIN NUMBER		
1	AA	PROTECTIVE GROUND
2	BA	TRANSMITTED DATA
3	BB	RECEIVED DATA
4	CA	REQUEST TO SEND
5	CB	CLEAR TO SEND
6	CC	DATA SET READY
7	AB	SIGNAL GROUND
8	CF	DATA CARRIER DETECT
9	ON	+12V STATIC LEVEL CONTROL
10	OFF	-12V STATIC LEVEL CONTROL

Table 6-3. RS-232-C MUX Panel Connector Pinouts

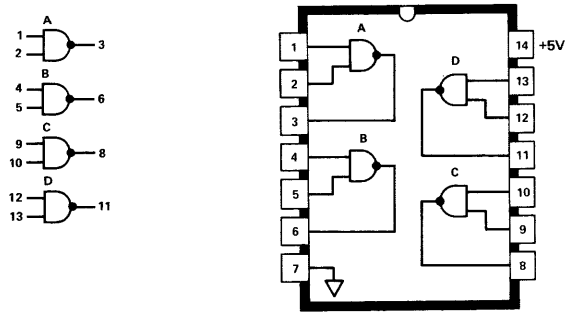
25-PIN CONNECTOR	SIGNAL MNEMONIC	SIGNAL FUNCTION
(Device ports J0-J7)	(with respect to Terminal or I/O Device)	
PIN NUMBER		
11	NC	NO CONNECTION
12	NC	NO CONNECTION
13	NC	NO CONNECTION
14	NC	NO CONNECTION
15	NC	NO CONNECTION
16	NC	NO CONNECTION
17	NC	NO CONNECTION
18	NC	NO CONNECTION
19	NC	NO CONNECTION
20	CD	DATA TERMINAL READY
21	NC	NO CONNECTION
22	NC	NO CONNECTION
23	NC	NO CONNECTION
24	NC	NO CONNECTION
25	NC	NO CONNECTION

Table 6-4. Serial I/O Circuits

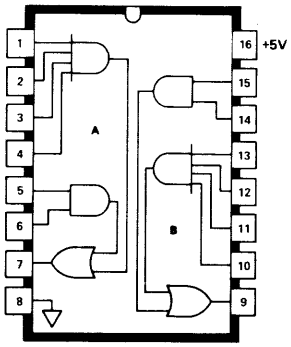
SIGNAL RS-232-C	CCITT V.24	FUNCTION	SIGNAL RS-449	FUNCTION	DIRECTION WITH RESPECT TO TERMINAL
AA	101	PROTECTIVE GROUND	--		
AB	102	SIGNAL GROUND	SG	SIGNAL GROUND	
--	---		SC	SEND COMMON	
--	---		RC	RECEIVE COMMON	
BA	103	TRANSMITTED DATA	* SD	SEND DATA	OUT
BB	104	RECEIVED DATA	* RD	RECEIVE DATA	IN
CA	105	REQUEST TO SEND	RS	REQUEST TO SEND	OUT
CB	106	CLEAR TO SEND	CS	CLEAR TO SEND	IN
CC	107	DATA SET READY	DM	DATA MODE	IN
CD	108.2	DATA TERMINAL READY	TR	TERMINAL READY	OUT
CF	109	CARRIER DETECT	RR	RECEIVER READY	IN

*SD (terminal) = RD- (MUX interface)
*RD (termianl) = RD+ (MUX interface)

1820-0681

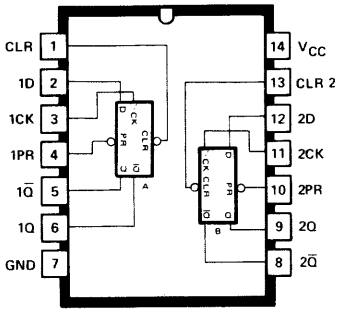


1820-1060



1820-1112

Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear

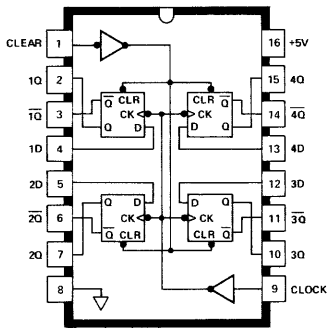


FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

*Non-stable condition exists only while both preset and clear inputs are low.

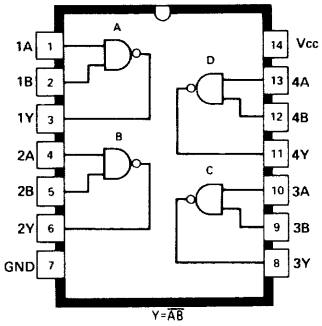
1820-1191



QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

1820-1197

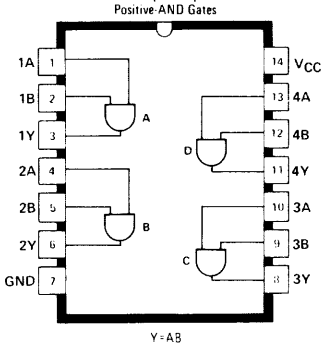
Quadruple 2-Input Positive-NAND Gates



$Y=\overline{AB}$

1820-1201

Quadruple 2-Input Positive-AND Gates



Y=AB

1820-1202

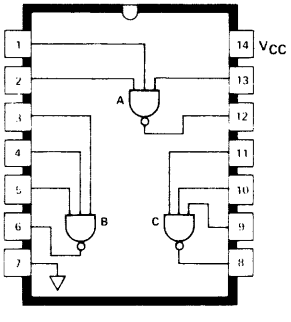
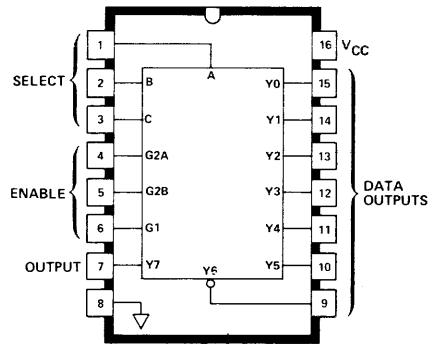
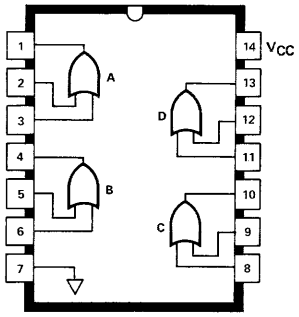


Figure 6-1. Integrated Circuit Base Diagrams (Sheet 1 of 5)

1820-1216

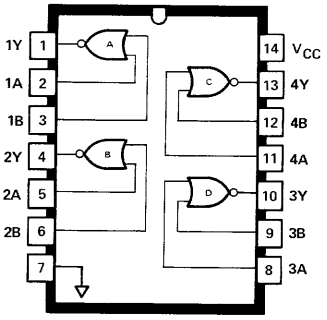


1820-1273



1820-1322

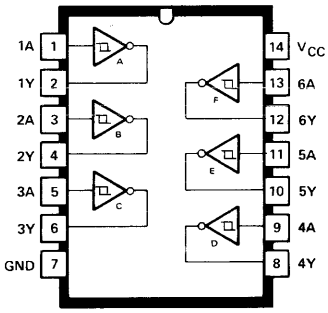
Dual 4-Input Positive-NOR Gates



$Y=\overline{A+B}$

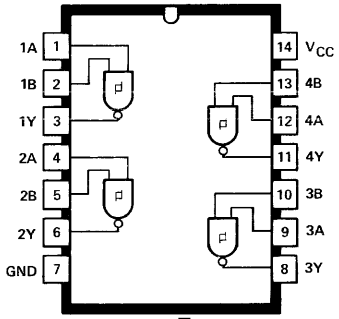
1820-1416

Description: Hex Inverters.



1820-1425

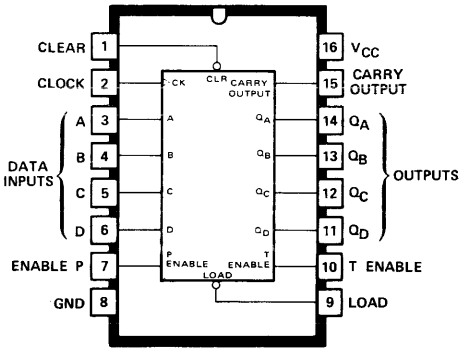
Quadruple 2-Input Positive-NAND Schmitt Triggers



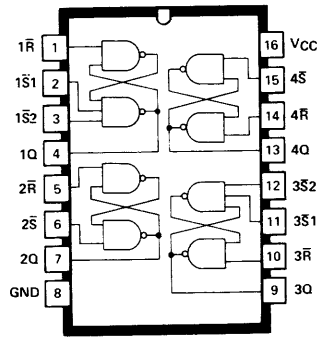
$Y=\overline{AB}$

1820-1430

Description: Synchronous 4-Bit Counter with Direct Clear.



1820-1440



FUNCTION TABLE
(EACH LATCH)

INPUTS $\bar{S}^\dagger$	INPUTS $\bar{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established
*This output level is pseudo stable; that is, it may not persist when the $\bar{S}$ and $\bar{R}$ inputs return to their inactive (high) level
†For latches with double $\bar{S}$ inputs
H = both $\bar{S}$ inputs high
L = one or both $\bar{S}$ inputs low

1820-1470

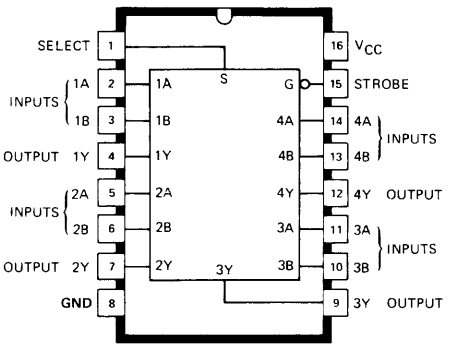
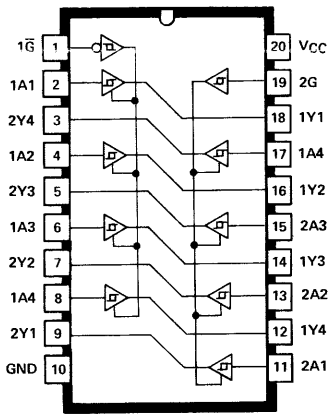


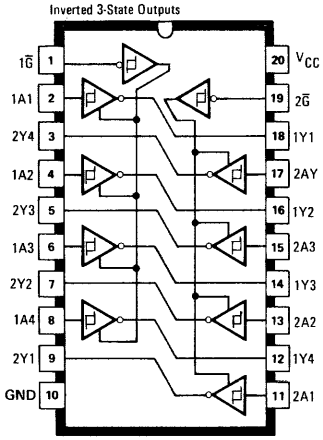
Figure 6-1. Integrated Circuit Base Diagrams (Sheet 2 of 5)

1820-1624



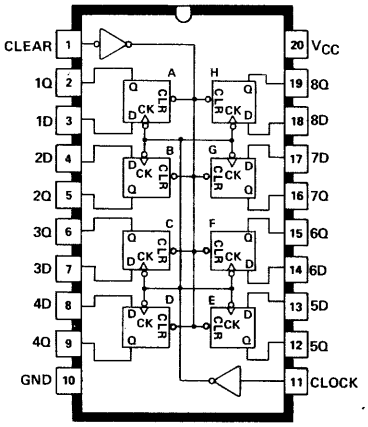
1820-1633

Octal Buffers/Line Drivers/Line Receivers
Inverted 3-State Outputs



1820-1730

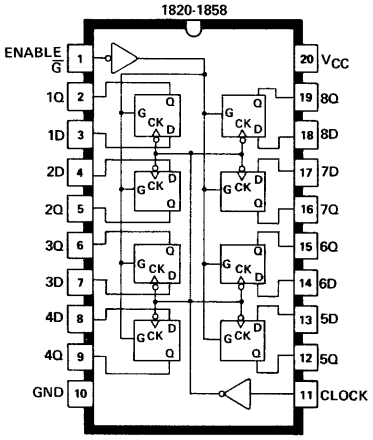
Octal D-Type Flip-Flops
Common Clock
Single-Rail Outputs



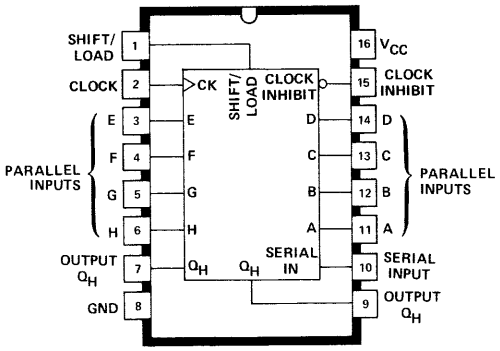
FUNCTION TABLE
(Each Flip-Flop)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

1820-1858



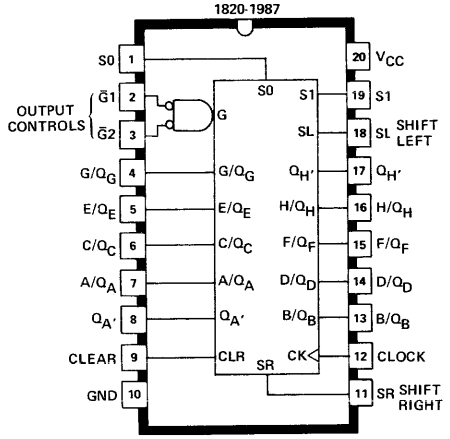
1820-1975



INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

Figure 6-1. Integrated Circuit Base Diagrams (Sheet 3 of 5)

1820-1987

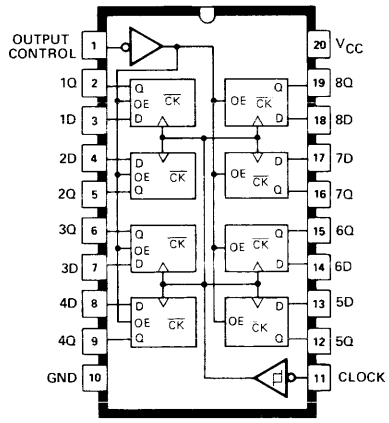


MODE	INPUTS							INPUTS/OUTPUTS								OUTPUTS	
	CLEAR	FUNCTION SELECT		OUTPUT CONTROL		CLOCK	SERIAL	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A	Q_H
		S1	S0	$\overline{G1}$↑	$\overline{G2}$↑		SL SR										
Clear	L L	X L	L X	L L	L L	X X	X X X X	L L	L L	L L	L L	L L	L L	L L	L L	L L	L L
Hold	H H	L X	L X	L L	L L	X L	X X X X	Q_{A0} Q_{A0}	Q_{B0} Q_{B0}	Q_{C0} Q_{C0}	Q_{D0} Q_{D0}	Q_{E0} Q_{E0}	Q_{F0} Q_{F0}	Q_{G0} Q_{G0}	Q_{H0} Q_{H0}	Q_{A0} Q_{A0}	Q_{H0} Q_{H0}
Shift Right	H H	L L	H H	L L	L L	↑ ↑	X H X L	H L	Q_{An} Q_{An}	Q_{Bn} Q_{Bn}	Q_{Cn} Q_{Cn}	Q_{Dn} Q_{Dn}	Q_{En} Q_{En}	Q_{Fn} Q_{Fn}	Q_{Gn} Q_{Gn}	H L	Q_{Gn} Q_{Gn}
Shift Left	H H	H H	L L	L L	L L	↑ ↑	H X L X	Q_{Bn} Q_{Bn}	Q_{Cn} Q_{Cn}	Q_{Dn} Q_{Dn}	Q_{En} Q_{En}	Q_{Fn} Q_{Fn}	Q_{Gn} Q_{Gn}	Q_{Hn} Q_{Hn}	H L	Q_{Bn} Q_{Bn}	H L
Load	H	H	H	X	X	↑	X X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input-output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

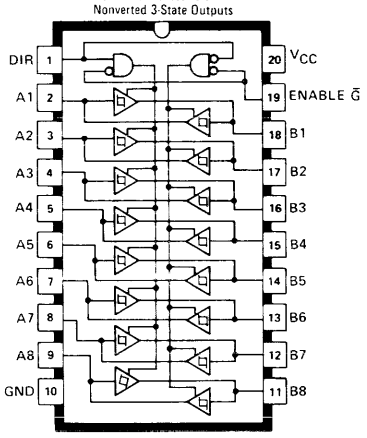
1820-1997

Octal D-Type Flip-Flops
Common Output Control
Common Clock



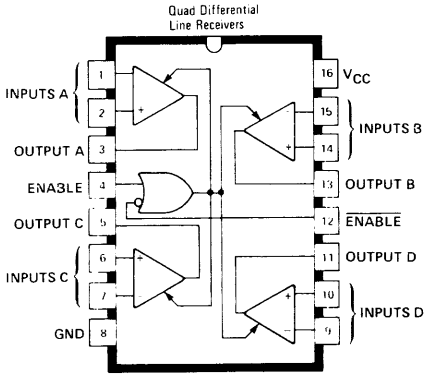
1820-2075

Octal Bus Transceivers
Nonverted 3-State Outputs



1820-2203

Quad Differential
Line Receivers



1820-2117

Dual Single-Ended Line Driver

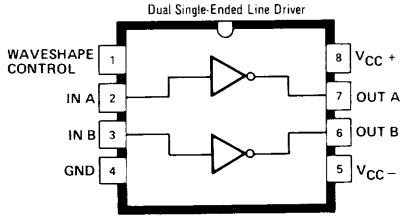


Figure 6-1. Integrated Circuit Base Diagrams (Sheet 4 of 5)

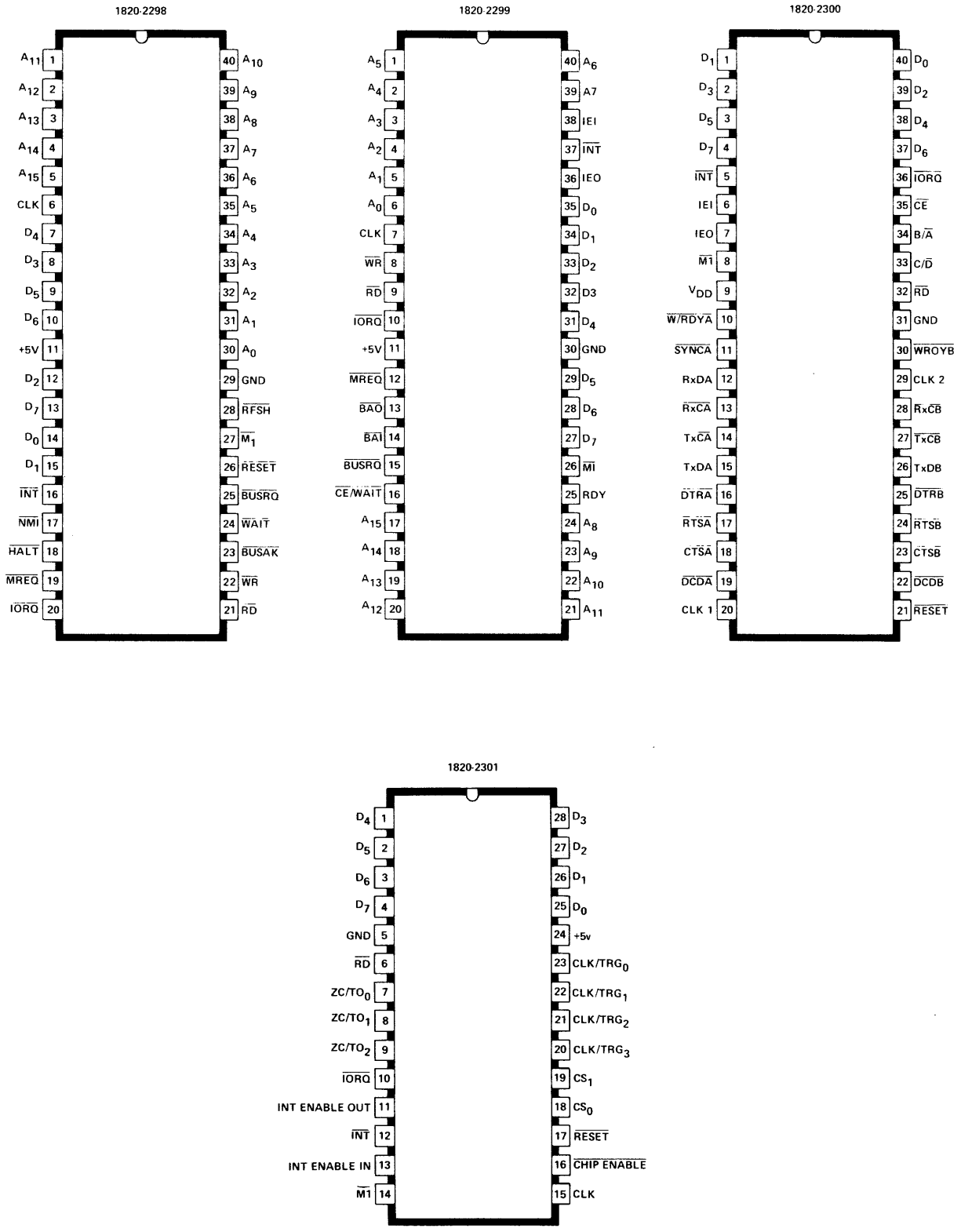


Figure 6-1. Integrated Circuit Base Diagrams (Sheet 5 of 5)

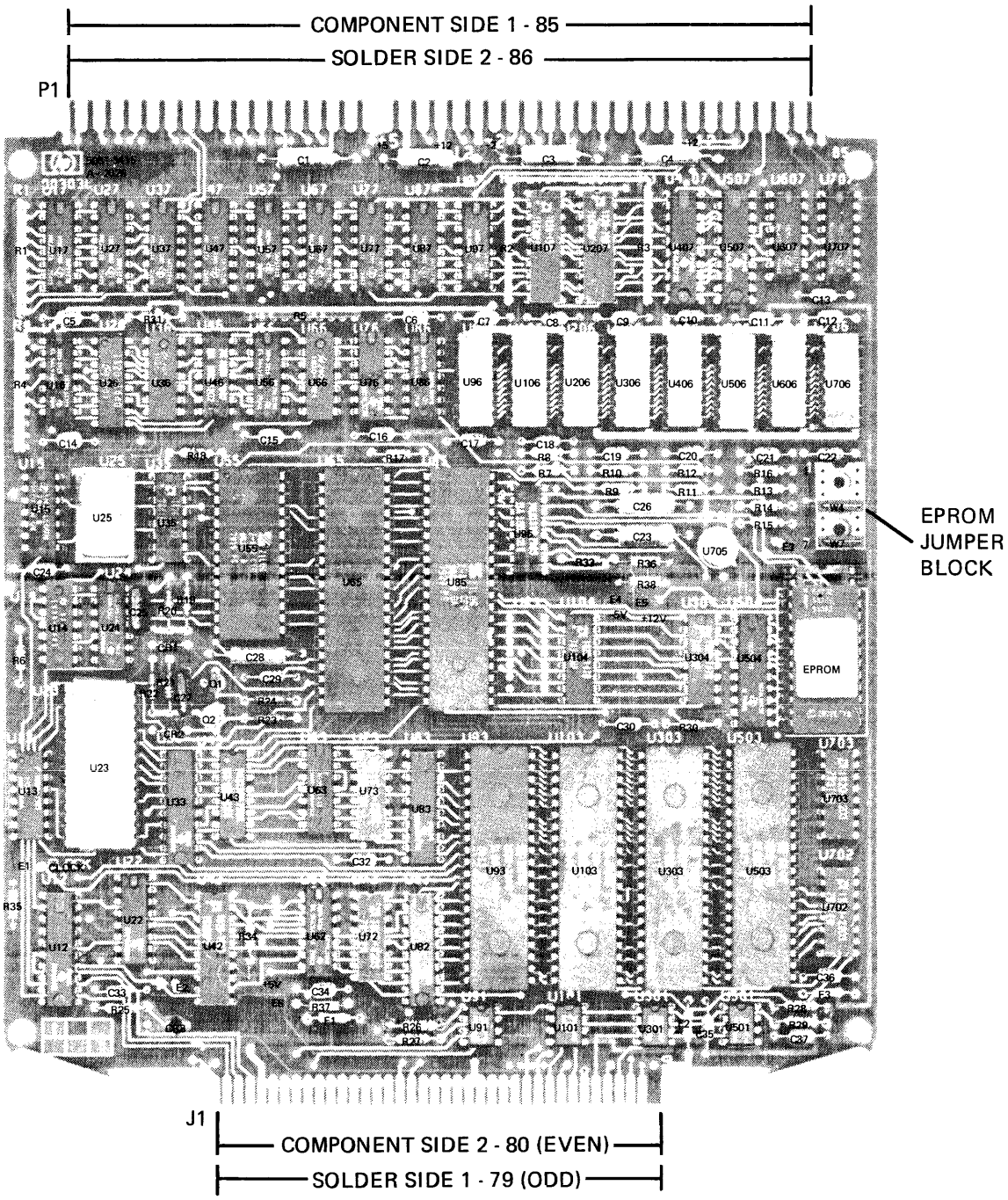


Figure 6-2 MUX Interface Parts Location Diagram

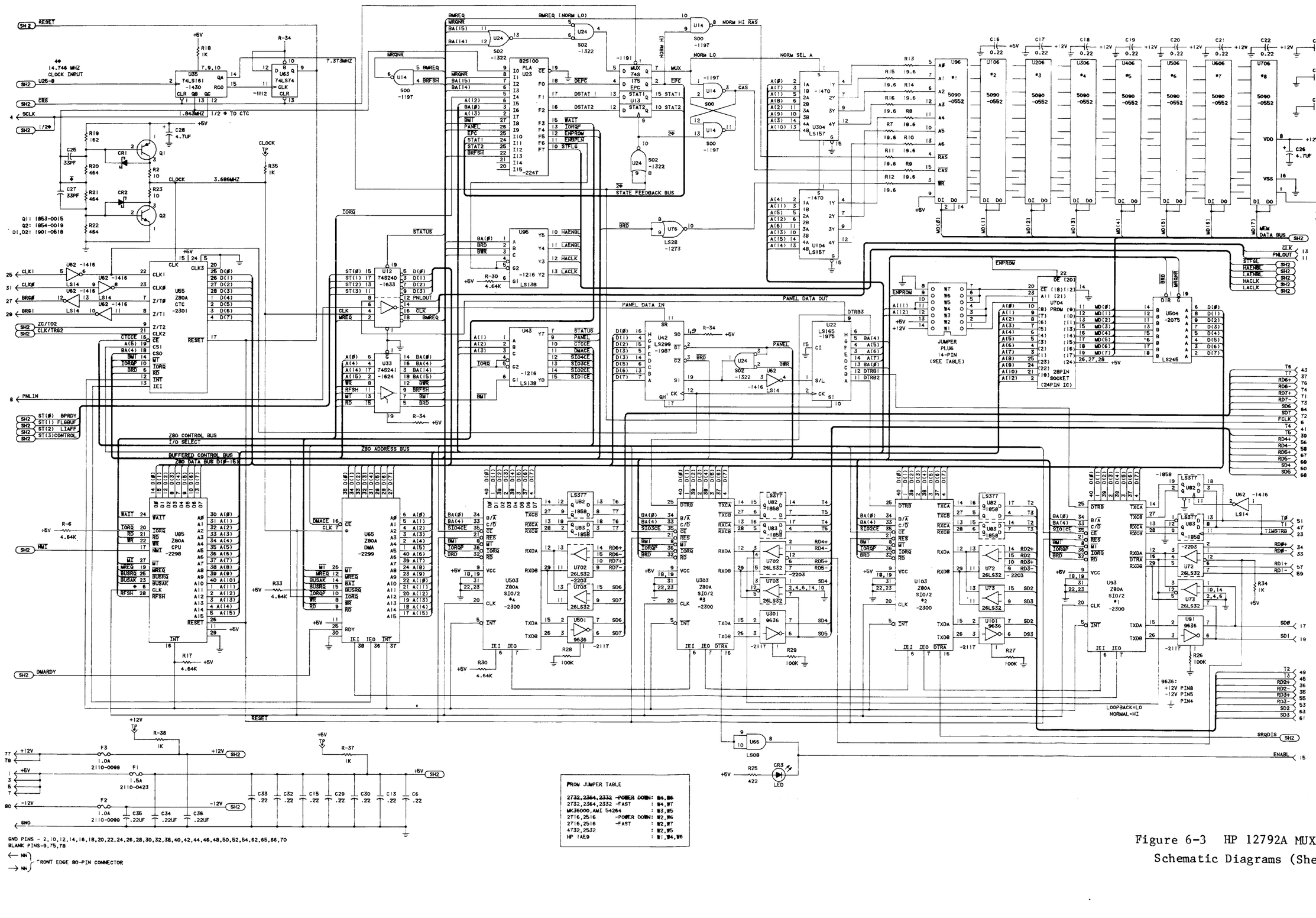


Figure 6-3 HP 12792A MUX Interface Schematic Diagrams (Sheet 1 of 2)

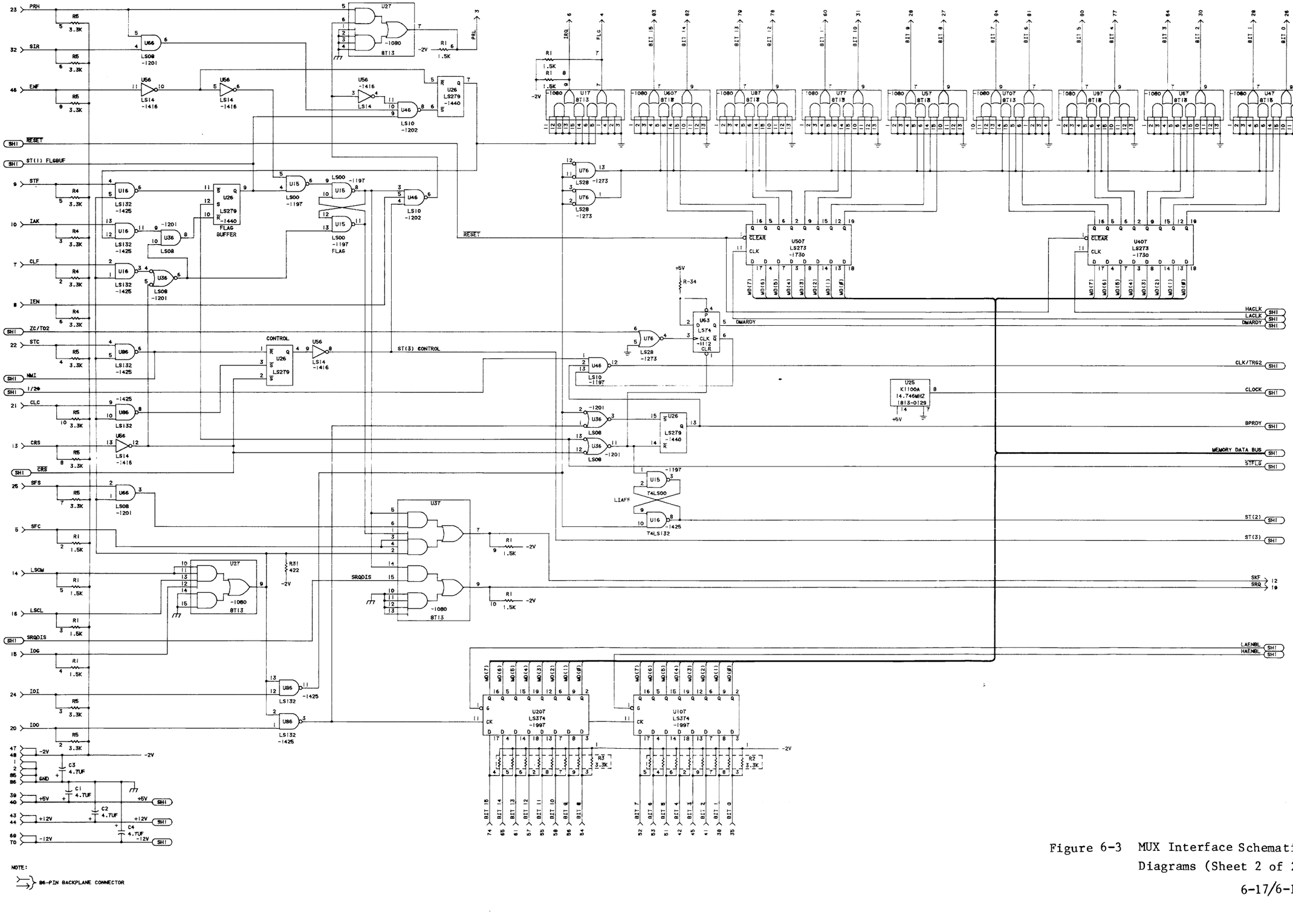
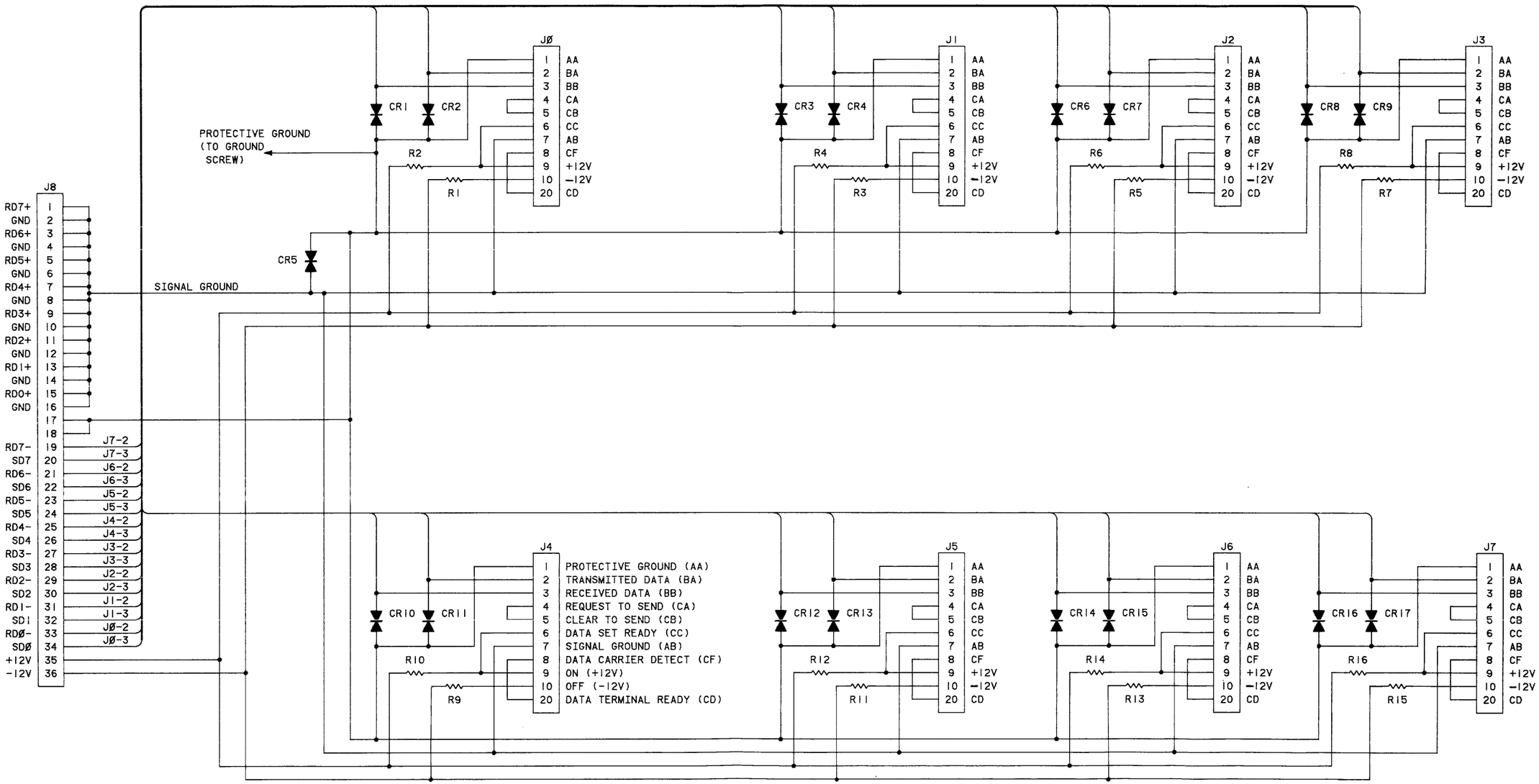


Figure 6-3 MUX Interface Schematic Diagrams (Sheet 2 of 2)



COMPONENTS:

R1-R16	1K, 1/4W (0683-1025)
CR1-CR17	TRANZORBS
JØ-J7	F RS-232 25 PIN CONNECTORS (NO HP PART#)
J8	F-36 PIN RECEPTACLE (1251-3661)

Figure 6-4. HP 12828A RS-232-C MUX Panel Schematic Diagram

Chapter 7
Replaceable Parts

Introduction

This Chapter contains the following information that will aid you when ordering replaceable parts for the HP 12792A MUX Interface:

* How to order listed and non-listed parts for the MUX
* Replaceable Parts tables and information for the MUX
* Code List of Manufacturers for the replaceable parts

Replaceable Parts

Table 7-1 gives you a list of the replaceable parts in alphanumeric order of the reference designations used on the MUX Interface Parts Location Diagram (Figure 6-2) and the MUX Interface Schematic Diagrams (Figure 6-3) in Chapter Six. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY) of each part used in the interface.
5. Description of the part.
6. A five-digit code number that corresponds to the manufacturer of the part.
7. The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information on the parts used in the MUX interface, address the order or inquiry to your local Hewlett-Packard Sales and Service Office (Sales and Service Office are listed in the back of this manual).

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity you require. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the MUX interface or part.
2. Description and function of the part.
3. Quantity required.

Table 7-1. HP 12792A MUX Interface Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A1	5061-3415	2	1	21 MX MULTIPLEXER	28480	5061-3415
C1	0180-0100	3	7	CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C2	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C3	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C4	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C5	0160-4842	6	27	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-2150	5	2	CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
C26	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C27	0160-2150	5		CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
C28	0180-0100	3		CAPACITOR-FXD 4.7UF+-10% 35VDC TA	56289	150D475X9035B2
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
CR1	1901-0518	8	2	DIODE-SCHOTTKY	28480	1901-0518
CR2	1901-0518	8		DIODE-SCHOTTKY	28480	1901-0518
CR3	1990-0486	6	1	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4684
F1	2110-0423	8	1	FUSE 1.5A 125V .281X.093	28480	2110-0423
F2	2110-0099	4	2	FUSE 1A 125V .281X.093	28480	2110-0099
F3	2110-0099	4		FUSE 1A 125V .281X.093	28480	2110-0099
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	1810-0276	2	1	NETWORK-RES 10-SIP1.5K OHM X 9	01121	210A152
R2	1810-0278	4	4	NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R3	1810-0278	4		NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R4	1810-0278	4		NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R5	1810-0278	4		NETWORK-RES 10-SIP3.3K OHM X 9	01121	210A332
R6	0698-3155	1	4	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R7	0698-3429	2	10	RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R8	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R9	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R10	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R11	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R12	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R13	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R14	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R15	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R16	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R17	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R18	0757-0280	3	6	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R19	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R20	0698-0082	7	3	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R21	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R22	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R23	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R24	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R25	0698-3447	4	2	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R26	0757-0465	6	4	RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R27	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R28	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R29	0757-0465	6		RESISTOR 100K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1003-F
R30	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F

Table 7-1. HP 12792A MUX Interface Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R31	0698-3447	4		RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R33	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R35	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R36	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R37	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R38	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
U12	1820-1633	8	1	IC BFR TTL 8 INV OCTL 1-INP	01295	SN748240N
U13	1820-1191	3	1	IC FF TTL 8 D-TYPE POS-EDGE-TRIG COM	01295	SN748175N
U14	1820-0681	8	1	IC GATE TTL 8 NAND QUAD 2-INP	01295	SN74800N
U15	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U16	1820-1425	6	2	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U17	1820-1080	9	11	IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U22	1820-1975	1	1	IC SHF-RGTR TTL LS NEG-EDGE-TRIG PRL-IN	01295	SN74LS165N
U23	1820-2544	2	1		28480	1820-2544
U24	1820-1322	2	1	IC GATE TTL 8 NOR QUAD 2-INP	01295	SN74802N
U25	1813-0129	0	1	IC OSC HYBRID	34344	K1100A
U26	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
U27	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U33	1820-1624	7	1	IC BFR TTL 8 OCTL 1-INP	01295	SN748241N
U35	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U36	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U37	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U42	1820-1987	5	1	IC SHF-RGTR TTL LS COM CLEAR STOR 8-BIT	01295	SN74LS299N
U43	1820-1216	3	2	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U46	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U47	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U55	1820-2301	9	1		28480	1820-2301
U56	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U57	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U62	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U63	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U65	1820-2299	4	1		28480	1820-2299
U66	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U67	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U72	1820-2203	0	4	IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U73	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U76	1820-1273	2	1	IC BFR TTL LS NOR QUAD 2-INP	01295	SN74LS28N
U77	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U82	1820-1658	9	2	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U83	1820-1658	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U85	1820-2298	3	1		28480	1820-2298
U86	1820-1425	6		IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U87	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U91	1820-2117	5	4	IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U93	1820-2300	8	4		28480	1820-2300
U95	1820-1216	3		IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U96	1818-0341	8	8	IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U97	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U101	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U103	1820-2300	8			28480	1820-2300
U104	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U106	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U107	1820-1997	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U206	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U207	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U301	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U303	1820-2300	8			28480	1820-2300
U304	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U306	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U406	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U407	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U501	1820-2117	5		IC DRVR TTL LINE DRVR DUAL	07263	9636ATC
U503	1820-2300	8			28480	1820-2300
U504	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U506	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U507	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U606	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U607	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N
U702	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U703	1820-2203	0		IC RCVR TTL LS LINE RCVR QUAD	34335	AM26LS32PC
U705	1826-0220	9	1	IC V REGLTR TO-39	27014	LM320H-05
U706	1818-0341	8		IC NMOS 16384-BIT RAM DYN 200-NS 3-S	0003J	UPD416D-2
U707	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	18324	N8T13N

Table 7-1. HP 12792A MUX Interface Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XW1	1258-0124	7	2	PIN-PROGRAMING DUMPER .30 CONTACT	91506	8136-4756-1
				MISCELLANEOUS PARTS		
	1200-0483	0	2	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0483
	1200-0567	1	1	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
	1200-0607	0	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0654	7	6	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654

Table 7-2. Code List of Manufacturers

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.

CODE NO.	MANUFACTURER	ADDRESS	CODE NO.	MANUFACTURER	ADDRESS
0003J	Nippon Electric Co.		27014	Natl. Semicond. Corp.	Santa Clara, CA 95051
01121	Allen-Bradley Co.	Milwaukee, WI 53204	28480	Hewlett-Packard Co. Corporate Hq.	Palo Alto, CA 94304
01295	Texas Instr Inc. Semicond. Compnt. Div.	Dallas, TX 75222	34335	Advanced Micro Devices Inc.	Sunnyvale, CA 94086
03888	KDI Pyrofilm Corp.	Whippany, NJ 07981	34344	Motorola Inc.	Franklin Park, IL 60131
07263	Fairchild Semicond. Div.	Mt. View, CA 94042	56289	Sprague Electric Co.	North Adams, MA 01247
18324	Signetics Corp.	Sunnyvale, CA 94086	91506	Augat Inc.	Attleboro, MA 02703
24546	Corning Glass Works (Bradford)	Bradford, PA 16701			

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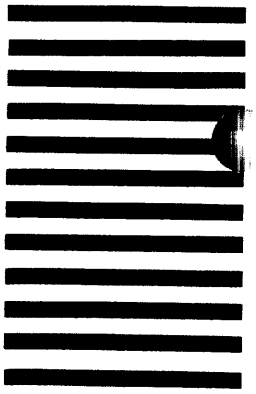

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