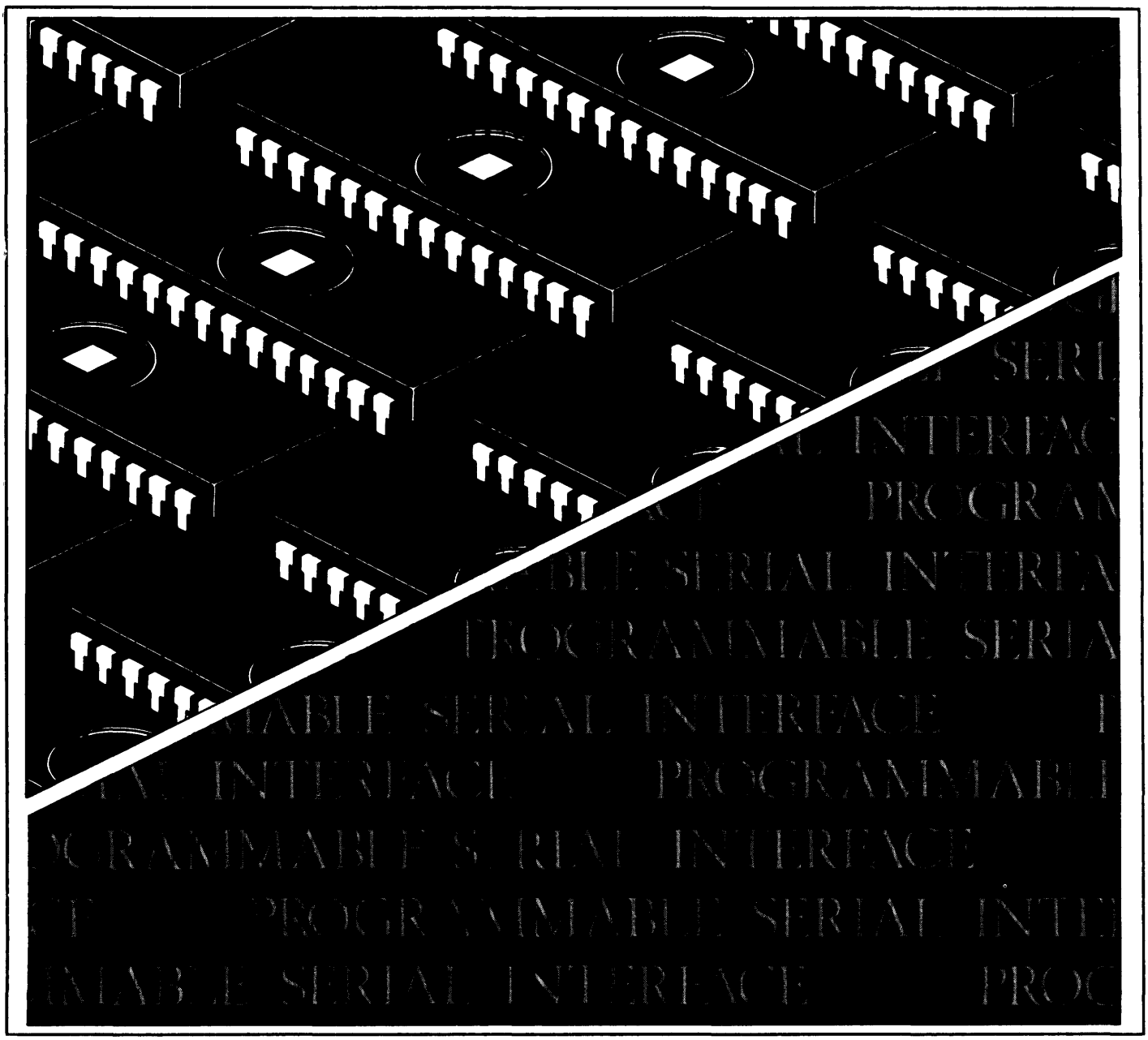
HP 1000 Computer Systems

HEWLETT PACKARD

PROGRAMMABLE SERIAL INTERFACE

for modem connection from M/E/F-series computers

Installation and Service Manual



HP 1000 M/E/F-Series Computer Systems

Programmable Serial Interface (PSI) for MODEM Connections

Installation and Service Manual

Card Assemblies: 12250-60001
12260-60001
12793-60002
12794-60002
12826-60001

Date Code: B-2410

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Printing History

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past updates; however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with the user-inserted update information. New editions of this manual will contain new information, as well as updates.

12826-91001

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Update 1 . . . . . November 1983
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SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

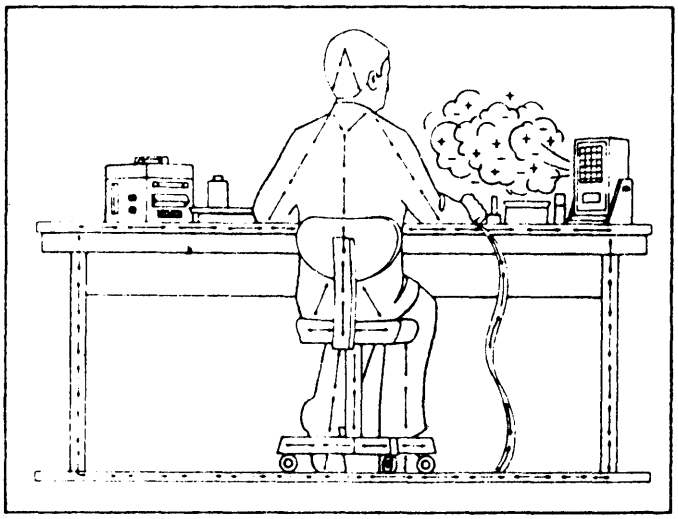
Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and *ultimate use.* Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by *3M Company.* Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in these shielding bags during storage or in transit.

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top, wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

Glossary of Terms

The following terms are defined as they are used in Hewlett-Packard computer products manuals. Some of the terms defined below may not be used in this manual.

Asynchronous transmission - No timing signals are sent with the data. Start and stop bits serve to delimit transmitted words.

Binary Synchronous Protocol - Bisync - BSC - These terms are synonymous, and stand for a character-oriented, half-duplex protocol.

Buffer - A segment of contiguous random-access memory locations used for temporary storage of input/output messages.

Card - The Printed Circuit Assembly (PCA).

CCITT - International Telephone and Telegraph Consultive Committee.

CRC-16 - Cyclic Redundancy Check - An error detection scheme used in data communications.

CRC-CCITT - Cyclic Redundancy Check - An error detection scheme defined by the International Telephone and Telegraph Consultive Committee.

DCE - Data Circuit-terminating Equipment - In most references, an entry node of the network.

DCPC - Dual Channel Port Controller.

DIP - Dual In-line Package - A type of integrated circuit package.

DMA - Direct Memory Access - The transfer of data directly to or from memory.

Driver - In a hardware sense, a driver refers to a circuit which is capable of supplying specific current and voltage requirements. In a software sense, a driver is a program that is capable of controlling a specific input/output device.

DS - Distributed System - A term used to refer to networks using Hewlett-Packard Distributed Systems hardware and software products.

DTE - Data Terminal Equipment - In most references, the local node which resides outside the network and communicates with the DCE.

EIA - Electronics Industries Association.

Firmware - Software code packaged in read-only memory (EPROM/ROM).

FCS - Frame Checking Sequence - A 16-bit sequence derived from an algorithm common to DCE and DTE. The sequence is appended to each frame and used as a verification of data transmission.

Flag - The LAP-B and HDLC synchronization character with a binary representation of "01111110". Because LAP-B and HDLC require zero insertion after a string of five "1" bits, the flag bit string is unique and cannot be misinterpreted.

Frame - A LAP-B and HDLC unit of information exchange, bounded by flags, consisting of an address field, control field, optional data field, and an FCS field.

Full-duplex - Communications systems or equipment capable of simultaneous two-way data communication.

Half-duplex - Communications system or equipment capable of transmission in either direction, but not both directions simultaneously.

Handshaking - The alternating exchange of predetermined signals between two communicating devices for purposes of control.

HDLC - High-Level Data Link Control. Types of protocols which eliminate much of the handshaking (and resultant time-consuming line turnarounds).

Host - The computer housing the circuit card.

HP-DLC-II - Hewlett-Packard Data Link Control II - A Hewlett-Packard HDLC standard defining the elements and procedures for a balanced, bit-oriented, Level-II protocol. HP-DLC-II is compatible with CCITT X.25 LAP-B, and LAP-B implementations by TELENET and TRANSPAC packet-switching networks.

I-Frame - A LAP-B and HDLC unit of information exchange containing a data field.

Interface - A device providing electrical and mechanical compatibility between two communicating devices.

ISO - International Standardization Organization.

k - Maximum number of outstanding I-frames: a system parameter (less than eight) defining the most unacknowledged information frames permissible at any given time.

LAP-B - Link Access Protocol -Balanced - A CCITT Recommendation X.25 Level II protocol. LAP-B, a bit-oriented protocol, uses the principles and terminology of ISO's HDLC.

LED - Light Emitting Diode - A component used on many printed circuit assemblies to provide a visual indication of desired information.

Link - Communication lines, modems, and other equipment which permit the transmission of information in data format between two or more devices.

Modem - Modulator-Demodulator - Equipment capable of digital-to-analog and analog-to-digital signal conversion for transmission and reception via common carrier telephone lines.

Modulus - Used by LAP-B and HDLC in the sequential numbering of I-frames; modulus equals eight.

N1 - Maximum number of bits in an I-frame; N1 is a system parameter used by LAP-B and HDLC.

N2 - Maximum (re)transmission; a LAP-B and HDLC system parameter specifying the number of times the local node will transmit and retransmit a frame before some recovery procedure is begun.

N(R) - Receive sequence number - Found in LAP-B and HDLC information, receiver ready, receiver not ready, and reject frames. N(R) denotes the expected sequence number of the next received I-frame.

N(S) - Send sequence number - Found in LAP-B and HDLC information frames, it denotes the sequence number of the transmitted I-frame.

Octet - A sequence of eight bits, i.e., a byte.

PCA - Printed Circuit Assembly - Circuit cards are commonly referred to as PCAs.

Primary - In LAP-B and HDLC, that logical portion of a DCE or DTE responsible for sending commands and receiving/processing the resulting responses. In Bisync, a primary is the node which initiated the call.

Primary System - A preconfigured operating system included with all HP 1000 Computer systems. It can be reconfigured to meet specific system I/O and memory requirements.

Receiver - Any device capable of reception of electrically transmitted signals.

SDLC - Synchronous Data Link Control - An IBM High-Level Data Link Control protocol.
Secondary - In LAP-B and HDLC, that logical portion of a DCE or DTE responsible for receiving commands from the remote DTE/DCE, processing these commands, and generating the correct responses. (Each LAP-B or HDLC DCE/DTE is a combined station, composed of both logical primary and secondary functions.) In Bisync, a secondary is the node which receives a call.

Synchronous transmission - Timing signals are transmitted with the data. No start and stop bits are used. Defined protocol characters must be used to delimit message blocks or frames.

System Parameter - As used in HP manuals, a parameter necessary for DCE/DTE communication; its value is agreed upon before network communication is attempted.

T1 - Timer T1 - In LAP-B and HDLC, the period of time that elapses while awaiting acknowledgement of an outstanding frame.

T2 - Timer T2 - In LAP-B and HDLC, the maximum period of time a node will allow without an exchange of frames while the link is logically connected. (T1 excludes T2.)

TELENET - A packet-switching network owned and operated by GTE.

TRANSPAC - The French packet-switching network.

V(R) - Receive state variable - In LAP-B and HDLC, V(R) denotes the sequence number of the next in-sequence information the node expects to receive.

V(S) - Send state variable - In LAP-B and HDLC, V(S) denotes the sequence number of the next in-sequence information frame to be transmitted by the node.

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Preface

The Programmable Serial Interface is a multiusage hardware interface which must be complemented by Hewlett-Packard, or user-designed firmware installed directly on the board.

This manual documents the uncharacterized PSI card (that is, without firmware installed). If you purchased the card with firmware installed, you should have received another manual, providing information specific to the firmware.

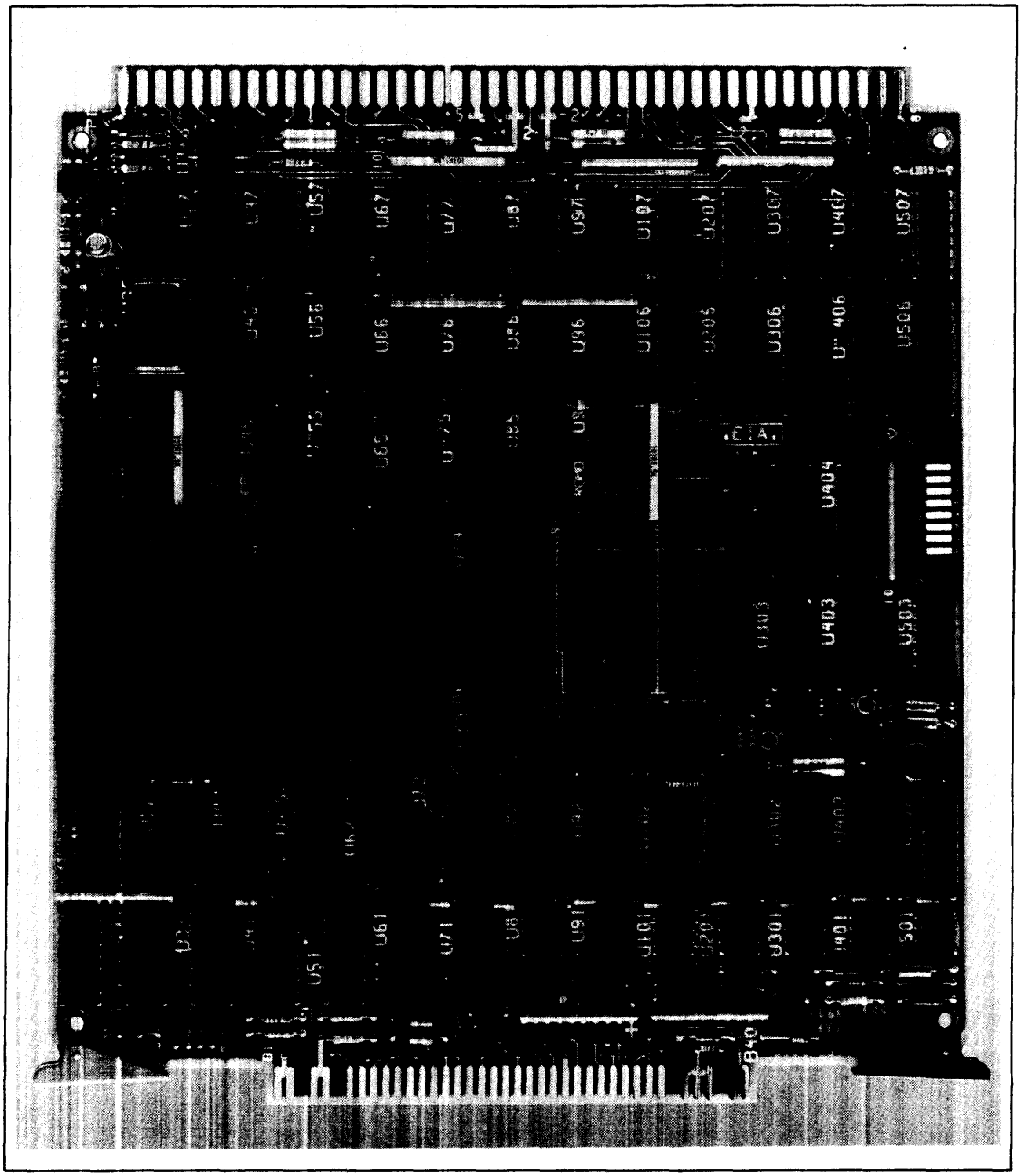


Figure 1-1. M/E/F-Series PSI

General Information
Chapter 1

This manual provides general information, installation procedures, principles of operation, maintenance instructions, replaceable parts information, and servicing diagrams for the M/E/F-Series Programmable Serial Interface (PSI) Card. This chapter contains general information concerning the PSI, and includes a description and specifications.

Physical Description

The PSI circuit card is shown in figure 1-1. One 86-pin edge connector connects the card to an HP 1000 M-, E-, or F-Series Computer backplane, and one 80-pin edge connector connects the card, via an interface cable, to a modem.

The PSI card provides an HP 1000 M/E/F-Series Computer with the capability to support a modem communications link in accordance with various communications protocols. These protocols are defined by such specifications as Electronics Industries Association Standards RS-449, RS-232-C, etc.; and the International Telegraph and Telephone Consultive Committee Recommendations V.24, V.28, X.25, etc.

Up to two ROMs/EPROMs are used to program the card for different applications. The ROM firmware is explained in separate manuals, depending on the application. Thus, a product of which the PSI is a part will consist of:

The PSI Printed Circuit Assembly (also referred to as a card in this manual).

One or two ROMs or EPROMs (mounted on the card).

Up to nine jumper plugs (mounted on the card).

An EIA RS-232-C interface cable (standard), or an optional RS-449 interface cable.

This manual, part number 12826-91001.

A firmware manual (the part number will depend on the product).

Functional Description

A simplified block diagram of the PSI is shown in figure 1-2. The PSI is an intelligent interface, and, in addition to supporting many different communications protocols, is capable of relieving a large amount of host CPU overhead.

A Z-80A Counter/Timer Circuit (CTC) and a Z-80A Serial Input/Output (SIO) are used to handle interface to the modem; the two Z-80A Direct Memory Access (DMA) controllers are used, one to control DMA between the card and the host CPU, and one to control access between the card memory and the SIO Channel A.

A Z-80A CPU controls the SIO, CTC, and DMAs.

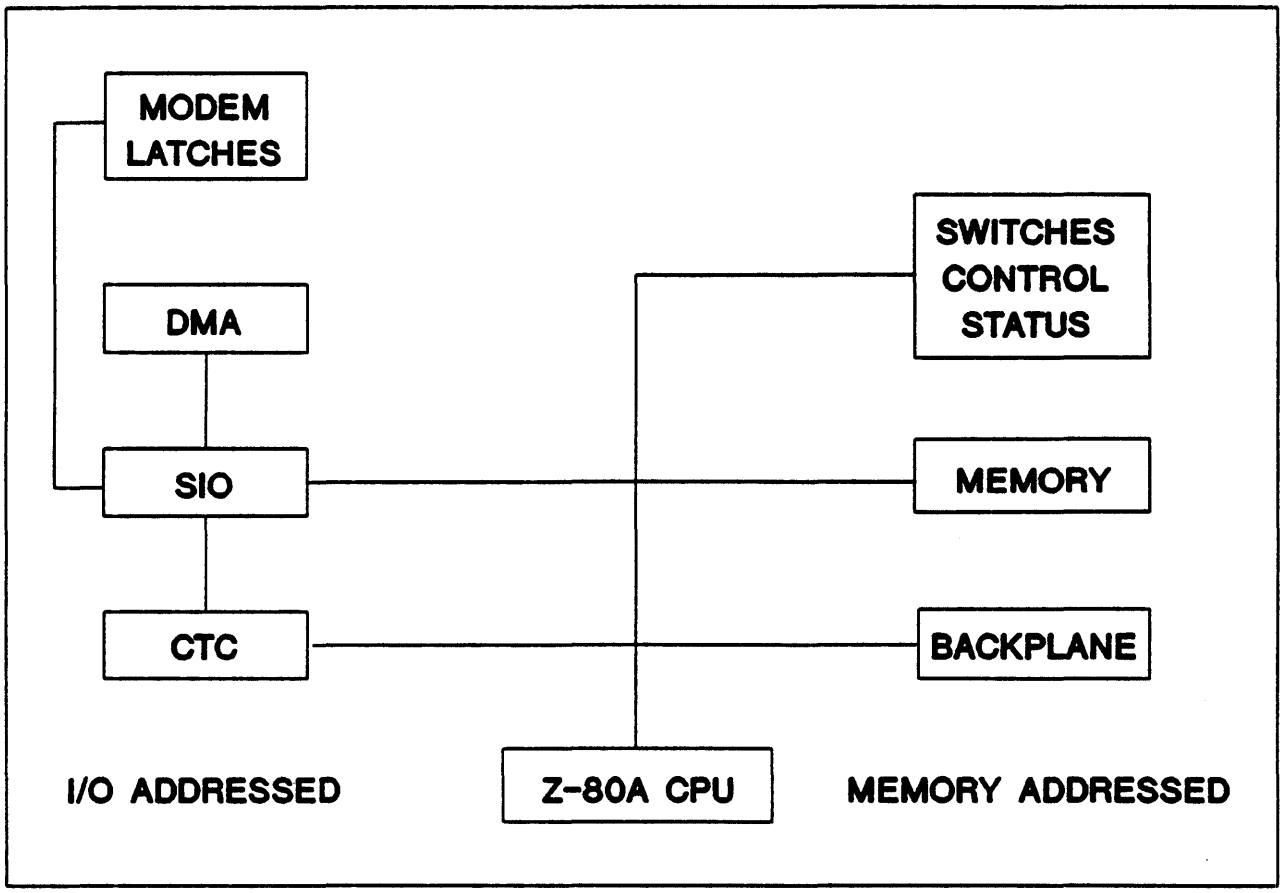


Figure 1-2. PSI Simplified Block Diagram

Identification

The Product

Five digits and a letter (e.g., 12250A) are used to identify HP products used with HP computers. The five digits identify the product, and the letter indicates the revision level. Note that the PSI card is not a product by itself, it is merely one part of an HP 1000 Computer System interface product (other parts of the product are the manuals, ROMs (or EPROMs), an interface cable, etc.). The complete product is described in the firmware manual.

The PSI Card

The PSI card is identified by a part number marked on the card. In addition to the part number, the card is further identified by a letter and a four-digit date code (e.g., B-2410). This designation is placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (the four digits following the letter) identifies the electrical characteristics of the card with components mounted. Thus, the complete part number of the PSI card will be one of the following parts:

12250-60001	12260-60001	12793-60002	12794-60002	12826-60001
B-2410	B-2410	B-2410	B-2410	B-2410

If the date code on the card does not agree with one above, there are differences between your card and the card described herein. These differences are described in Appendix A.

Installation and Service Manual

The manual supplied with the PSI card is identified by its name and part number. The part number (12826-91001) and publication date are printed on the title page. If the manual is revised, the publication date is changed. The Print History page (page ii) records the reprint dates.

Modem Compatibility

There are many modems that can be used with the PSI card. All modem control lines for EIA RS-232-C, EIA RS-449, CCITT V.10, V.11, etc., are made available by the hardware. Compatibility with specific modems is determined by the firmware.

Specifications

Table 1-1 lists the specifications of the PSI card. Note that these specifications are for the PSI card hardware only; they do not reflect the characteristics of a complete product with ROMs/EPROMs mounted. Product specifications are contained in the firmware manual which describes that particular product.

Table 1-1. Specifications

HARDWARE CHARACTERISTICS

Z-80A CPU based microprocessor control

4 mHz Z-80A-family microprocessor components

One Z-80A SIO/2 dual Serial I/O channel controller:

Two independent full duplex channels

Data rates

Asynchronous

57K bits per second maximum
50 bits per second minimum

Synchronous

460K bits per second maximum

50 bits per second minimum

Maximum speed with external clock: 810K bps
(the firmware will determine the actual speed)

Asynchronous features

5, 6, 7 or 8 bits per character

1, 1 1/2 or 2 stop bits
Even, odd, or no parity

X1, X16, X32, or X64 clock modes

Break generation and detection

Parity, overrun, and framing error
detection.

Table 1-1. Specifications (Continued)

Character-oriented protocol (BISYNC) features
One or two sync characters
Automatic sync character insertion and deletion
CRC generation and checking
Bit-oriented protocol (HDLC, SDLC, LAP-B) features
Abort sequence generation and checking
Automatic zero insertion and deletion
Address field recognition
Support for one to eight bits per character
Valid receive messages protected from overrun
CRC generation and checking
CRC-16 or CRC CCITT block frame check
Two modem control inputs and two modem control outputs per channel.

Table 1-1. Specifications (Continued)

The option of generating a vectored interrupt per channel: When the state of an SIO modem control input changes, When the transmit buffer becomes empty, When a receive character is available, When Special Receive Conditions occur: Parity error Receiver overrun error CRC/Framing error End of frame (SDLC, HDLC, LAP-B)
Two Z-80A DMA Direct Memory Access Controllers, Between memory and channel A of the SIO Between memory and the backplane I/O data latches
16K Bytes of Dynamic Ram, for tables, buffers, and/or firmware.
Two EPROM/ROM sockets (max 8K bytes per socket, 16K bytes max total), capable of using almost any combination of: 2716s, 2732s, 2764s, 2516s, 2532s, and other similar devices.
EIA RS-422 and EIA RS-423 Line Drivers and Receivers. 6 input lines (pairs) with balanced receivers 4 output lines (pairs) with balanced drivers, with duplicate unbalanced drivers. 8 output lines with unbalanced drivers 8 input lines with unbalanced receivers

Table 1-1. Specifications (Continued)

The drivers and receivers are capable of implementing:

A single EIA RS-449 compatible link

Two EIA RS-232-C compatible links which can control Bell 201(B,C), 208(A,B), or 209(A,B) modems.

A single fully supported EIA RS-232-C compatible link

A CCITT V.24/V.28 compatible link

Self-test Mode. Via firmware control, the PSI card's line interface can be placed into a self-test mode where:

The output of the Send Data line driver is looped back to the receive data input of the SIO on both channels A and B.

The CTC generated data clocks are routed back into the transmit and receive clock inputs of their respective SIO channels.

Multi-Drop Capability:

The EIA RS-422 line drivers for Terminal Timing and Request-to-Send can be placed in a high impedance state under firmware control. The Terminal Ready and Send Data line drivers can individually be placed into a high impedance state under firmware control.

Four programmable indicator lights (LEDs).

Eight switches, accessible as a single byte.

POWER REQUIREMENTS: (Assumes two 2732 EPROMs)

VOLTAGE	CURRENT	POWER DISSIPATION
+ 5 V	1.923 A	9.615 W
+12 V	0.315 A	3.780 W
-12 V	0.175 A	2.100 W
	Total:	15.495 W

Table 1-1. Specifications (Continued)

PHYSICAL CHARACTERISTICS:	
Size:	19.69 by 21.27 centimeters (7.750 by 8.374 inches)
Weight:	300 grams (10.6 ounces)
Backplane Interconnects:	One 86-pin edge connector (P1) plugs into the socket mounted on the backplane.
Device Interconnects:	One 80-pin edge connector (J1) on which a cable hood may be connected.

Installation
Chapter 2

This chapter provides information on unpacking, inspecting, installing, and checking the operation of the PSI Card.

Unpacking and Inspection

Inspect the shipping package immediately upon receipt to detect any evidence of mishandling during transit. If the package is damaged, ask that the carrier's agent be present when the product is unpacked. Carefully unpack the card and accessories and inspect for damage (scratches, broken components, etc.). If damage is noticed, notify the carrier and the nearest Hewlett-Packard Sales and Service Office listed at the back of this manual. Return the carton and packing material for the carrier's inspection.

After inspecting all components, refer to the equipment supplied information in the product manual to ensure that the product is complete. Also check the part numbers listed in that manual against the part numbers on the product components. If the product is incomplete, or if an incorrect component has been furnished, notify the nearest Hewlett-Packard Sales and Service Office.

After unpacking, inspecting, and checking part numbers of all parts of the product, follow installation and checkout procedures as defined in this chapter.

Computation of Current Requirements

The PSI card obtains its operating voltages from the computer power supply through the backplane. Before installing the card, it is necessary to determine whether the added current will overload the power supply. The current requirements of the PSI card are listed in the power requirements entry of table 1-1. Current specifications for all other interfaces can be found in the appropriate Reference or Installation and Service Manuals.

Firmware Installation

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS/EPROMS, RAMS, AND Z-80A COMPONENTS USED BY THE PSI CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Refer to figure 2-1 for correct installation positioning of the firmware ROMs/EPROMs. Note that when 24-pin ROMs/EPROMs are installed, socket pins 1, 2, 27, and 28 are left empty.

ROM/EPROM Configuration Jumpers

A set of jumpers on the PSI card provides the option of using different ROM/EPROM parts. The set consists of a 14-pin socket containing seven removable jumpers (XW1A through XW1G), and one hardwired jumper (W5). Check to see that XW1A through XW1G are configured as described in tables 2-1 and 2-2 for the specific ROM/EPROMs that are installed. (The hardwired jumper, W5, is configured at the factory.) Refer to figure 2-1 for the physical locations of the jumpers on the card. Functional locations of the jumpers are shown on the schematic logic diagram (figure 6-2, sheet 2, in Chapter 6).

Two additional jumpers, W1 and W6 (see figure 2-1 for the physical locations and figure 6-2, sheet 3, for the functional locations), are configured according to the function for which the card is to be used. Jumper W1 must be placed in position A during normal operation and when testing with a diagnostic or loop-back hood installed. This configuration releases the Terminal Ready line (TR) to firmware control. Jumper W6 is normally in the A position also. Refer to the applicable firmware manual for applications requiring different configurations of jumpers W1 and W6.

Table 2-1. ROM/EPROM Categories According to Part Type

CATEGORY	HP PART NO.	PART TYPE
A	1818-0762	TI 2532
B	1818-0498	TI 2516 Intel 2716
C	1818-0850 1818-1633 (No HP P/N) 1818-1747	Intel 2732 Intel 2732A Intel 2332 Intel 2764

Table 2-2. Jumper Requirements for all ROM/EPROM Combinations (X denotes a required jumper)

EPROM/ROM CATEGORY		X W 1	X W 1	X W 1	X W 1	X W 1	X W 1	X W 1
U93	U203	A	B	C	D	E	F	G
C	C					X		
A	A				X	X	X	X
C	A			X		X	X	
B	A			X		X	X	X
B	B			X	X	X	X	X
A	C	X				X		X
C	B	X			X	X	X	
A	B	X		X	X	X	X	X
B	C	X		X		X		X

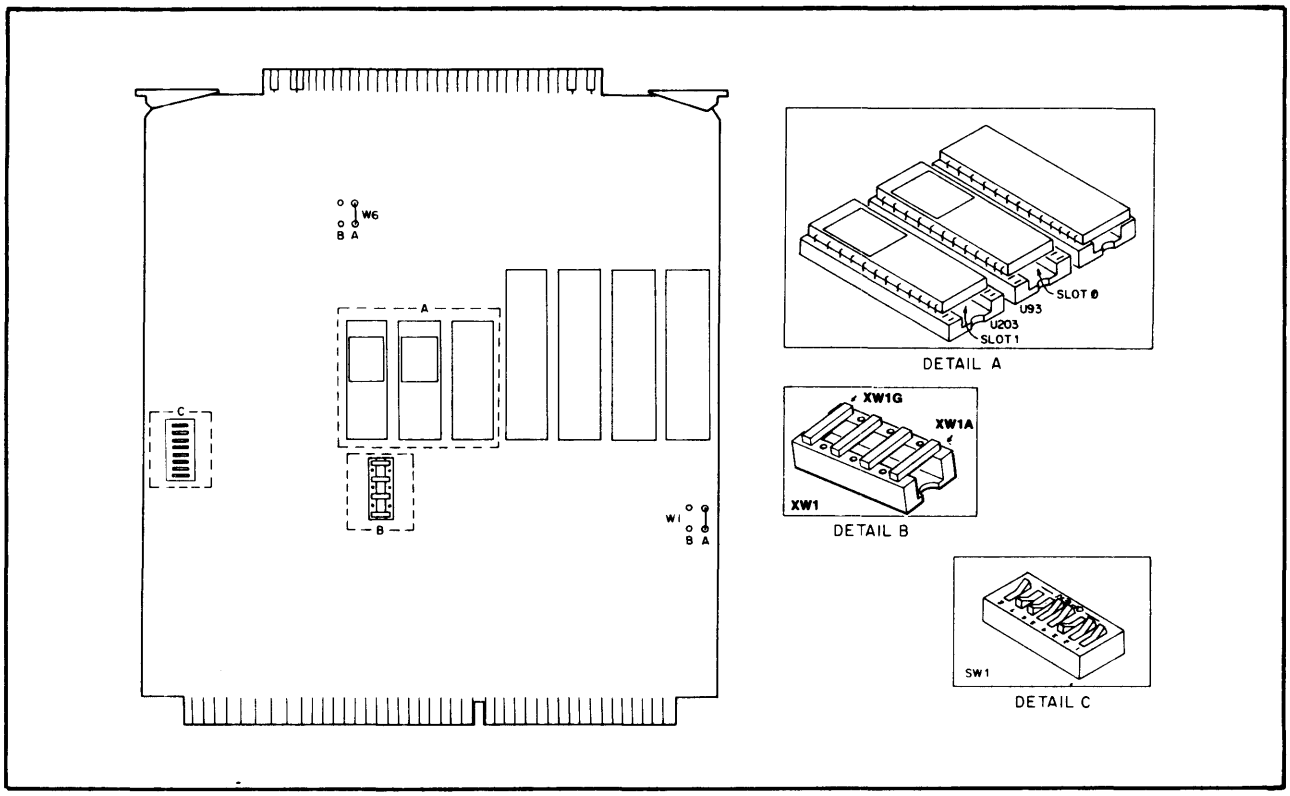


Figure 2-1. ROM/EPROM, Jumper, and DIP Switch Locations

DIP Switch Configuration

The card provides a Dual In-line Package (DIP) containing eight switches which may be sensed by the firmware. This set of switches can be used to determine the information field size, the transmit clock rate, and associated time-out values depending on the firmware implementation. The transmit clock rate should be set to indicate the clock rate that is supplied by the modem being used. Switch position number 1 (Bit 0) is both a firmware read switch, and a hardware function. When this switch is open, the forced cold load capability of the PSI card is physically disabled. Refer to figure 2-1 for switch position on the card, and to the firmware (product) manual for switch settings.

Backplane Interface

All interface between the PSI card and the M-, E-, or F-Series computer occurs on the computer backplane. The backplane connector (P1) is an 86-pin connector. Connections to P1 are listed in table 2-3.

Datacomm Interface

The front edge (datacomm) connector is an 80-pin connector which allows the PSI card to be connected to a modem. Connections from this connector (J1) are listed in table 2-4.

A comparison of EIA RS-232-C, CCITT V.24, and EIA RS-449 circuits and their respective signal connector pin assignments is presented in table 2-5.

Installing the PSI Card

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

After ensuring that the computer power supply can handle the added load, that the EPROMs are properly installed, and that the DIP switches and jumpers are configured properly (see the firmware manual), perform the following steps:

1. Turn off power at the computer and the modem. Install the interface card in the desired slot in the computer card cage, noting the select code. The card should be oriented the same as all other cards in the computer: components on the top side of the card. Press the card firmly into place.

2. Connect the cable supplied with the product to the interface card and modem. Ensure that the cable is connected using the same orientation as the cables connected to other cards in the computer.

3. Restore power to the computer and the modem.

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS/EPROMS, RAMS, AND Z-80A COMPONENTS USED BY THE PSI CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Checkout Procedure

Checkout procedure for the PSI card depends on the firmware and whether or not a self-test is programmed into the ROM/EPROMs. Refer to the firmware manual for your particular product for PSI card checkout.

Interface Card LEDS

There are four LEDs on the interface card. Located on the left side of the card next to the front edge connector, the LEDs are visible when the card is installed in the computer and are referenced as 0 through 3 with 0 being the LED on the right. These LEDs may be used as firmware-controlled self-test indicators. Refer to the applicable firmware manual for details.

Reshipment

If the PSI card is to be shipped to Hewlett-Packard for any reason, attach a tag identifying the owner and indicating the reason for shipment. Include the part number of the PSI card.

Remove the ROM/EPROMS from the card. Pack the card in the original factory material. If the original material is not available, good commercial packing material should be used. Reliable commercial packing and shipping companies have the facilities and materials to adequately repack the item.

Table 2-3. Backplane Connector P1

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
1	GND	Ground
2	GND	Ground
3	PRL	Priority Low
4	FLAGL	Flag Signal, Lower Select Code
5	SFC	Skip if Flag is Clear
6	IRQL	Interrupt Request, Lower Select Code
7	CLF	Clear Flag
8	IEN	Interrupt Enable
9	STF	Set Flag
10	IAK	Interrupt Acknowledge
12	SKF	Skip on Flag
13	CRS	Control Reset
14	LSCM	Select Code Most Significant Digit (Lower Address)
15	IOG	I/O Group
16	LSCL	Select Code Least Significant Digit (Lower Address)
17	POPIO	Power On Preset to I/O
18	BIOS	"Not" Block I/O Strobe (E-Series)
19	SRQ	Service Request
20	IOO	I/O Data Output Signal
21	CLC	Clear Control
22	STC	Set Control
23	PRH	Priority High
24	IOI	I/O Data Input Signal
25	SFS	Skip if Flag is Set
26	IOB0	I/O Bus Input, bit 0
27	IOB8	I/O Bus Input, bit 8
28	IOB9	I/O Bus Input, bit 9
29	IOB1	I/O Bus Input, bit 1
30	IOB2	I/O Bus Input, bit 2
31	IOB10	I/O Bus Input, bit 10
32	SIR	Set Interrupt Request
35	IOBO0	I/O Bus Output, bit 0
38	IOBO1	I/O Bus Output, bit 1

Table 2-3. Backplane Connector P1 (Continued)

PIN NO.	SIGNAL MNEMONIC	SIGNAL DEFINITION
39	+5V	
40	+5V	
41	IOBO2	I/O Bus Output, bit 2
42	IOBO4	I/O Bus Output, bit 4
43	+12V	
44	+12V	
45	IOBO3	I/O Bus Output, bit 3
46	ENF	Enable Flag
47	-2V	
48	-2V	
50	RUN	Run
51	IOBO5	I/O Bus Output, bit 5
52	IOBO7	I/O Bus Output, bit 7
53	IOBO6	I/O Bus Output, bit 6
54	IOBO8	I/O Bus Output, bit 8
55	IOBO11	I/O Bus Output, bit 11
56	IOBO9	I/O Bus Output, bit 9
57	IOBO12	I/O Bus Output, bit 12
58	IOBO10	I/O Bus Output, bit 10
60	IOB11	I/O Bus Input, bit 11
61	IOBO13	I/O Bus Output, bit 13
64	IOB3	I/O Bus Input, bit 3
65	IOBO14	I/O Bus Output, bit 14
69	-12V	
70	-12V	
74	IOBO15	I/O Bus Output, bit 15
77	IOB4	I/O Bus Input, bit 4
78	IOB12	I/O Bus Input, bit 12
79	IOB13	I/O Bus Input, bit 13
80	IOB5	I/O Bus Input, bit 5
81	IOB6	I/O Bus Input, bit 6
82	IOB14	I/O Bus Input, bit 14
83	IOB15	I/O Bus Input, bit 15
84	IOB7	I/O Bus Input, bit 7
85	GND	Ground
86	GND	Ground

Table 2-4. Datacomm Connector J1

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
1A	---	No Connection
1B	+12V	+12 Volts Power
2A	---	No Connection
2B	+12V	+12 Volts Power
3A	SSD	Secondary Send Data
3B	---	No Connection
4A	---	No Connection
4B	-12V	-12 Volts Power
5A	---	No Connection
5B	-12V	-12 Volts Power
6A	---	No Connection
6B	---	No Connection
7A	SRS	Secondary Request to Send
7B	TR(A)	Terminal Ready
8A	SD(U)	Send Data
8B	TT(B)	Terminal Timing
9A	RS(U)	Request to Send
9B	TT(U)	Terminal Timing
10A	TR(B)	Terminal Ready
10B	DAMPRT(B)	
11A	RS(A)	Request to Send
11B	TR(U)	Terminal Ready
12A	TT(A)	Terminal Timing
12B	---	No Connection
13A	SD(B)	Send Data
13B	SD(A)	Send Data
14A	---	No Connection
14B	RS(B)	Request to Send
15A	DAMPST(B)	
15B	RT(B)	Receive Timing
16A	CS(B)	Clear To Send
16B	DAMPRD(B)	
17A	CS(A)	Clear to Send
17B	---	No Connection
18A	SQ	Signal Quality
18B	RC	Receive Common
19A	ST(B)	Send Timing
19B	---	No Connection
20A	RD(B)	Receive Data
20B	ST(A)	Send Timing
21A	---	No Connection
21B	**BX16IN	
22A	SRR	Secondary Receiver Ready
22B	DM	Data Mode (RS-423, RS-449)

Table 2-4. Datacomm Connector J1 (Continued)

PIN NO.	SIGNAL MNEMONIC*	SIGNAL DEFINITION
23A	RD(A)	Receive Data
23B	TM	Test Mode
24A	RR(B)	Receiver Ready
24B	IC	Incoming Call
25A	SG	Signal Ground
25B	SC	Signal Common
26A	RR(A)	Receiver Ready
26B	**BDATACLK+	
27A	DM(A)	Data Mode (RS-232-C)
27B	DM(B)	Data Mode (RS-232-C)
28A	SF/SR	Select Frequency/Signaling Rate
28B	DD	Receive Timing
29A	**ASYNCCLK+	
29B	DA	Terminal Timing
30A	**X16IN	
30B	RT(A)	Receive Timing
31A	SCS	Secondary Clear to Send
31B	DB	Send Timing
32A	SRD	Secondary Receive Data
32B	RL	Remote Loopback
33A	LL	Local Loopback
33B	NS	New Signal
34A	IS	Terminal In Service
34B	---	No Connection
35A	---	No Connection
35B	GND	Power Ground
36A	---	No Connection
36B	GND	Power Ground
37A	---	No Connection
37B	GND	Power Ground
38A	(SHIELD)	
38B	---	No Connection
39A	---	No Connection
39B	+5V	+5 Volts Power
40A	---	No Connection
40B	+5V	+5 Volts Power

* The (A) or (B) after a mnemonic indicates portions of a differential input or output.
The (U) after a mnemonic indicates a single ended version of a signal that appears elsewhere as differential.

** These are TTL level signals for compatibility, they should be used only to loop back for proper firmware operation.

Table 2-5. Serial I/O Circuits and Equivalents

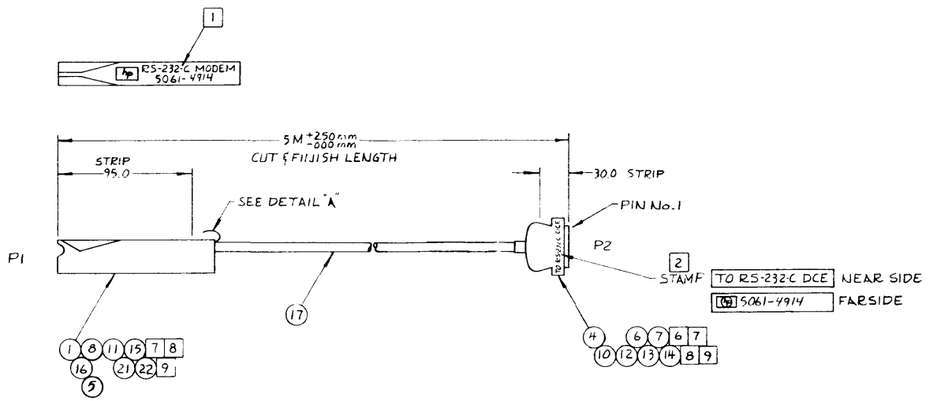
SIGNAL DESIGNATION			FUNCTION
RS-449	RS-232-C	CCITT V.24/V.28	
RD	BB	104	RECEIVE DATA
SD	BA	103	SEND DATA
CS	CB	106	CLEAR TO SEND
RS	CA	105	REQUEST TO SEND
TR	CD	108.2	TERMINAL READY
RR	CF	109	RECEIVER READY
ST	DB	114	SEND TIMING
RT	DD	115	RECEIVE TIMING
TT	DA	113	TERMINAL TIMING
IC	CE	125	INCOMING CALL
DM	CC	107	DATA MODE
TM	--	142	TEST MODE
LL	--	141	LOCAL LOOPBACK
RL	--	140	REMOTE LOOPBACK
SQ	CG	110	SIGNAL QUALITY
SF	CH	126	SELECT FREQUENCY
SR	CH	111	SELECT SIGNALING RATE
IS	--	---	TERMINAL IN SERVICE
NS	--	---	NEW SIGNAL
SRD	SBB	119	SEC. RECEIVE DATA
SSD	SBA	118	SEC. SEND DATA
SRS	SCA	120	SEC. REQUEST TO SEND
SCS	SCB	121	SEC. CLEAR TO SEND
SRR	SCF	122	SEC. RECEIVER READY
SG	AB	102	SIGNAL GROUND
SC	--	102a	SEND COMMON
RC	--	102b	RECEIVE COMMON
--	AA	101	PROTECTIVE GROUND

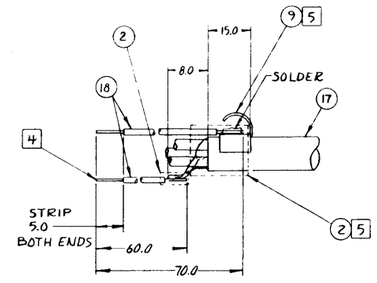
NOTES:

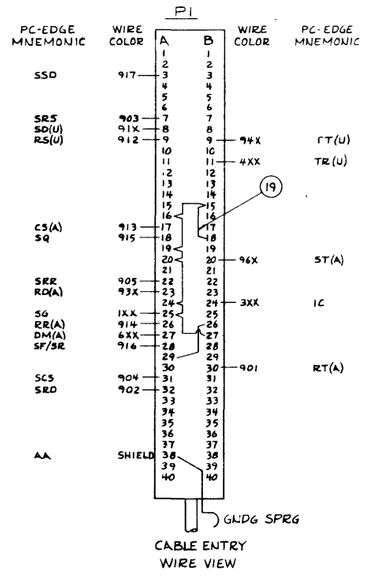
1. STAMP P1 HOOD AS SHOWN, REF DWG A-5950-5669-1.
2. STAMP P2 SHELL HALVES AS SHOWN, REF DWG A-5951-3021-1.
3. STRIPPING TABLE

CONNECTOR	JACKET	SHIELD	WIRE
P1	95.0	87.0	6.0
P2	30.0	30.0	4.0

4. FABRICATE SHIELD P1 (SEE DETAIL A) TWIST 8.0 OF SHIELD, CUT A 60.0 PIECE OF WIRE (ITEM 18), STRIP BOTH ENDS 5.0, SOLDER ONE END OF WIRE ONTO TWISTED SHIELD, SLIDE A 10.0 PIECE OF SHRINK TUBING (ITEM 3) OVER SOLDERED AREA AND SHRINK.
5. FABRICATE GROUNDING SPRING (ITEM 9) - SEE DETAIL "A", CUT A 70.0 PIECE OF WIRE (ITEM 18), STRIP BOTH ENDS 5.0 AND SOLDER ONE END ONTO GNDG SPR. PLACE GNDG SPR ON CABLE, SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) OVER GNDG SPR AND SHRINK.
6. SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) COVERING 10.0-15.0 OVER THE END OF THE OUTER JACKET.
7. CAPTURE UNUSED WIRE WITH A 15.0 PIECE OF SHRINK TUBING (ITEM 3).
8. SLIDE A 8.0 PIECE OF SHRINK TUBING (ITEM 3) TO INSULATE ADJACENT CONNECTION.
9. ASSEMBLE P1 PER B-5951-5613-1, P2 PER B-5951-7369-1
10. TEST FINISHED CABLE ASSY. ON BSD CABLE TESTER







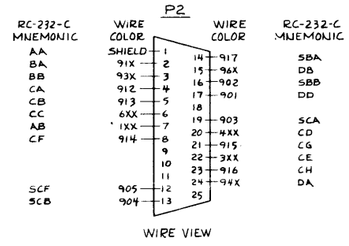


Figure 2-2. RS-232-C Modem Interface Cable Schematic Diagram

NOTES:

1. STAMP P1 HOOD AS SHOWN, REF DWG A-5950-5669-1.
2. STAMP P2 SHELL HALVES AS SHOWN.
3. STRIPPING TABLE

CONNECTOR	JACKET	SHIELD	WIRE
P1	95.0	87.0	6.0
P2	30.0	30.0	4.0

4. FABRICATE SHIELD, P1 (SEE DETAIL A) TWIST 8.0 OF SHIELD, CUT A 60.0 PIECE OF WIRE (ITEM 6), STRIP BOTH ENDS 5.0, SOLDER ONE END OF WIRE ONTO TWISTED SHIELD, SLIDE A 10.0 PIECE OF SHRINK TUBING (ITEM 2) OVER SOLDERED AREA AND SHRINK.
5. FABRICATE GROUNDING SPRING (ITEM 9) - SEE DETAIL "A", CUT A 70.0 PIECE OF WIRE (ITEM 18), STRIP BOTH ENDS 5.0 AND SOLDER ONE END ONTO GNDG SPR. PLACE GNDG SPR ON CABLE, SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) OVER GNDG SPR AND SHRINK.
6. SLIDE A 25.0 PIECE OF SHRINK TUBING (ITEM 2) COVERING 10.0-15.0 OVER THE END OF THE OUTER JACKET.
7. CAPTURE UNUSED WIRE WITH A 15.0 PIECE OF SHRINK TUBING (ITEM 3).
8. SLIDE A 8.0 PIECE OF SHRINK TUBING (ITEM 3) TO INSULATE ADJACENT CONNECTION.
9. ASSEMBLE P1 PER B-5951-5613-1, P2 PER DETAIL "B".
10. TEST PER A-5950-[illegible]5-1 "CABLE TESTER" USE ET-4530-018 AND ET-4530-007.

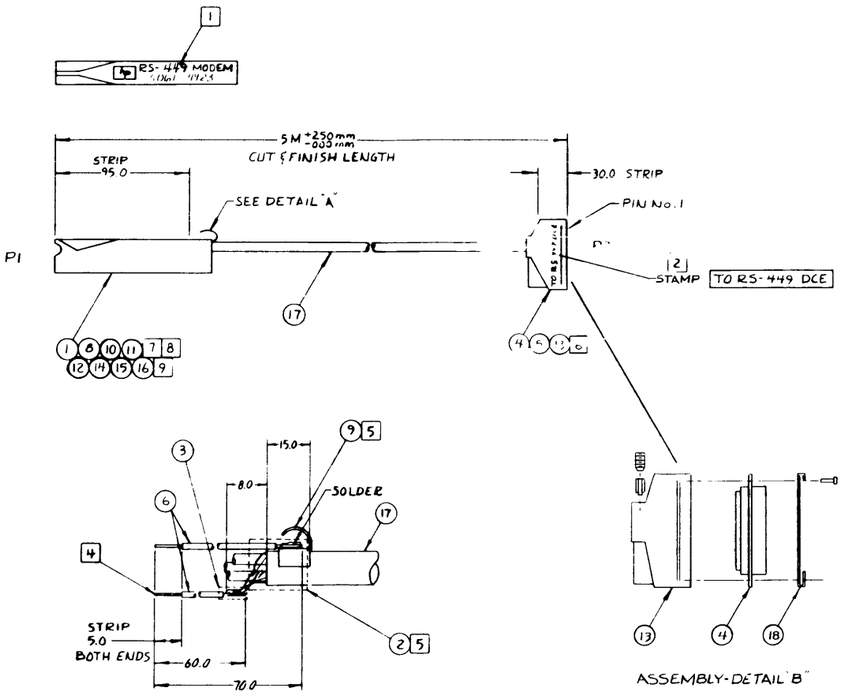


Figure 2-3. RS-449 Modem Interface Cable Schematic Diagram (Opt. 002)

Principles of Operation
Chapter 3

This chapter contains a description of the operation of the PSI card. The card consists of the following major functional areas:

HP 1000 M/E/F-Series Computer I/O backplane interface

Z-80A Microprocessor subsystem (CPU, SIO/2, DMA, and CTC)

Read-Only Memory (EPROM/ROM)

Random-Access Memory (RAM)

Communication line interface

A block diagram illustrating the major functional areas of the card is shown in figure 3-1. Each area is explained in detail in the following paragraphs.

Host Computer I/O Backplane Interface

The card communicates with the HP 1000 host computer over the I/O backplane. The backplane interface circuitry can be logically divided into two major sections: the I/O data latches and the control circuitry section.

The I/O data latches consist of two 8-bit input latches and two 8-bit output latches. The input latches hold 16-bit data or command words from the host computer until the card is ready to accept them. Similarly, the output latches hold 16-bit data or status words output from the card to the host computer.

The control circuitry consists of five flip-flops and other gate-level logic elements. The primary function of this section is to handle the control signals to and from the I/O backplane. These signals are used to generate and acknowledge interrupts, to handshake data between the host and the card and to conform to the standard HP 1000 computer I/O backplane signal conventions. For a more detailed discussion of these signals, refer to the HP 1000 I/O Interfacing Guide, HP part number 02109-90006.

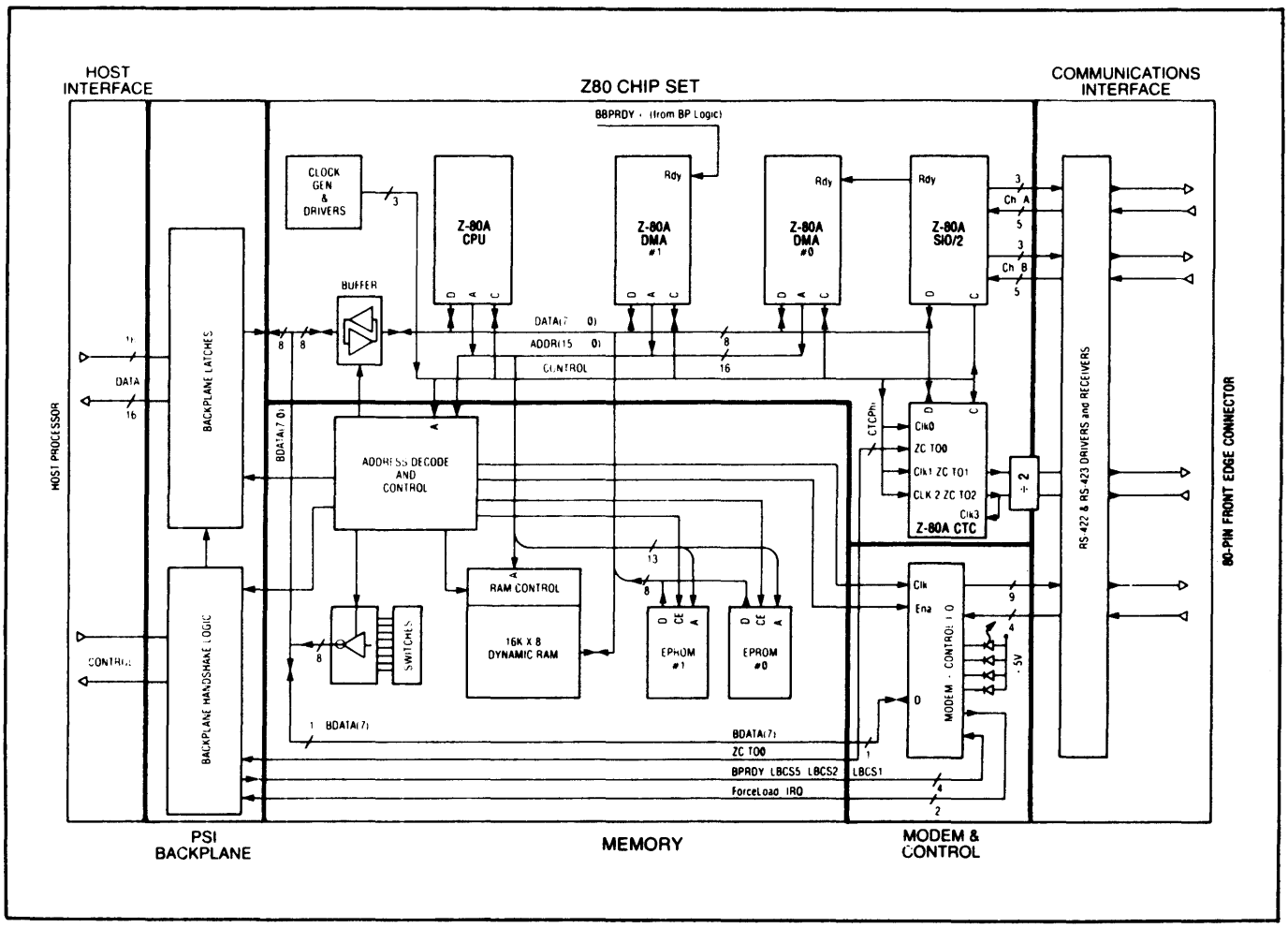


Figure 3-1. PSI Card Functional Block Diagram

Z-80A Microprocessor Subsystem

The heart of the PSI card is the Z-80A CPU (Central Processing Unit). This MOS LSI microprocessor operates from a single 5-volt supply, uses a single-phase clock and has a typical instruction execution time of 1 microsecond. The data bus is eight bits wide, and the address bus is 16 bits wide. All CPU pins are TTL compatible.

The Z-80A CPU employs a register-based architecture which includes two sets of six general-purpose registers which can be used as individual 8-bit registers or as 16-bit register pairs. Additional 8-bit registers include two sets of accumulator and flag registers, and the interrupt vector and memory refresh registers. Additional 16-bit registers include the stack pointer, program counter and two index registers. The Z-80A CPU provides the intelligence for the card to function as a preprocessor to relieve the host computer of a majority of the protocol processing.

An important pin on the Z-80A CPU as far as the PSI is concerned is the NMI (Non-Maskable Interrupt) input pin. By pulling this input low with an STC instruction, the host computer can "get the attention of" the Z-80A CPU. An NMI is the highest priority interrupt to the Z-80A CPU and forces it to start fetching and executing instructions from a predetermined location in the firmware. The host software driver uses this feature to issue commands to the card (commands from the host cannot be ignored).

Various support circuits are used in conjunction with the Z-80A CPU to facilitate the card's operation as an intelligent serial interface. These circuits are discussed in the following paragraphs.

Serial Input/Output (SIO)

A Z-80A SIO is used on the card to provide the serial data communications channel. The major functions performed by the SIO are serial-to-parallel conversion of input data and parallel-to-serial conversion of output data.

Direct Memory Access (DMA)

Two Z-80A LSI DMA controllers are used by the PSI card. One of the DMAs is used to transfer data between the SIO Channel A and the card memory; the other is used to transfer data between the host computer and the card memory. The function of the DMA logic is to transfer bytes of data in a manner that will be transparent to the Z-80A CPU. This enables the card to achieve higher throughput rates.

Counter Timer Circuit (CTC)

One Z-80A CTC is used to provide four independent counter/timers. One of the counter/timers may be used as a baud rate generator for SIO channel A. Another may be used as a baud rate generator for SIO channel B. Either of these could be used as timers by the firmware if they are not needed as baud rate generators. A third timer is available to the firmware. The fourth is used to maximize the effective throughput of the card by controlling the frequency of DMA cycle stealing.

Read-Only Memory (EPROM/ROM)

Two 28-pin sockets are provided for ROMs/EPROMs. All of the software required for the Z-80A CPU to implement the functions of protocol generation, modem control and backplane interaction control is contained in these ROMs/EPROMs and is referred to as firmware.

Random-Access Memory (RAM)

The card has 16K bytes of dynamic RAM. This memory is used for data buffers, program storage, and the storage of firmware variables. The refresh capability of the Z-80A CPU is used to provide the appropriate refresh signals to the dynamic RAMs.

Communication Line Interface

The communication line interface is the point at which the various signals are received onto the card or driven onto the communications line. The card is capable of supporting the EIA RS-232-C, CCITT V.28, and EIA RS-449, CCITT V.24 serial I/O standards. For the purposes of this discussion, the various interface circuits are referred to by their EIA RS-449 mnemonics. A comparison of EIA RS-232-C, EIA RS-449 and CCITT V.24/V.28 circuits and their respective signal connector pin assignments is given in table 2-5.

The EIA RS-449 standard consists of a combination of single-ended (EIA RS-423) and differential (EIA RS-422) drivers and receivers. The card uses both single-ended and differential drivers on some lines and only single-ended drivers on others. All of the receivers on the card are differential, although some are connected in such a way that they can only receive single-ended signals. The manner in which each signal is driven or received is illustrated in figure 3-2.

A single-ended driver produces one inverted output whereas its differential counterpart drives both the inverted and non-inverted signals. It is important to note that the mark and space conventions of the protocol are preserved in both cases. The advantage of differential drivers and receivers is that they offer higher noise immunity, thus allowing longer cable lengths and higher data signaling rates.

When a differential receiver is connected to a single-ended driver, the remaining input is either connected to ground (EIA RS-232-C or CCITT V.24/V.28) or to the Receiver Common (RC) circuit of the driving device (EIA RS-449). The various driver/receiver combinations are illustrated in figure 3-2. The combination used depends on the requirements of the modem. The receivers on the card can survive an input voltage range of +/- 25 volts and can operate with a maximum common mode input voltage of +/- 7 volts.

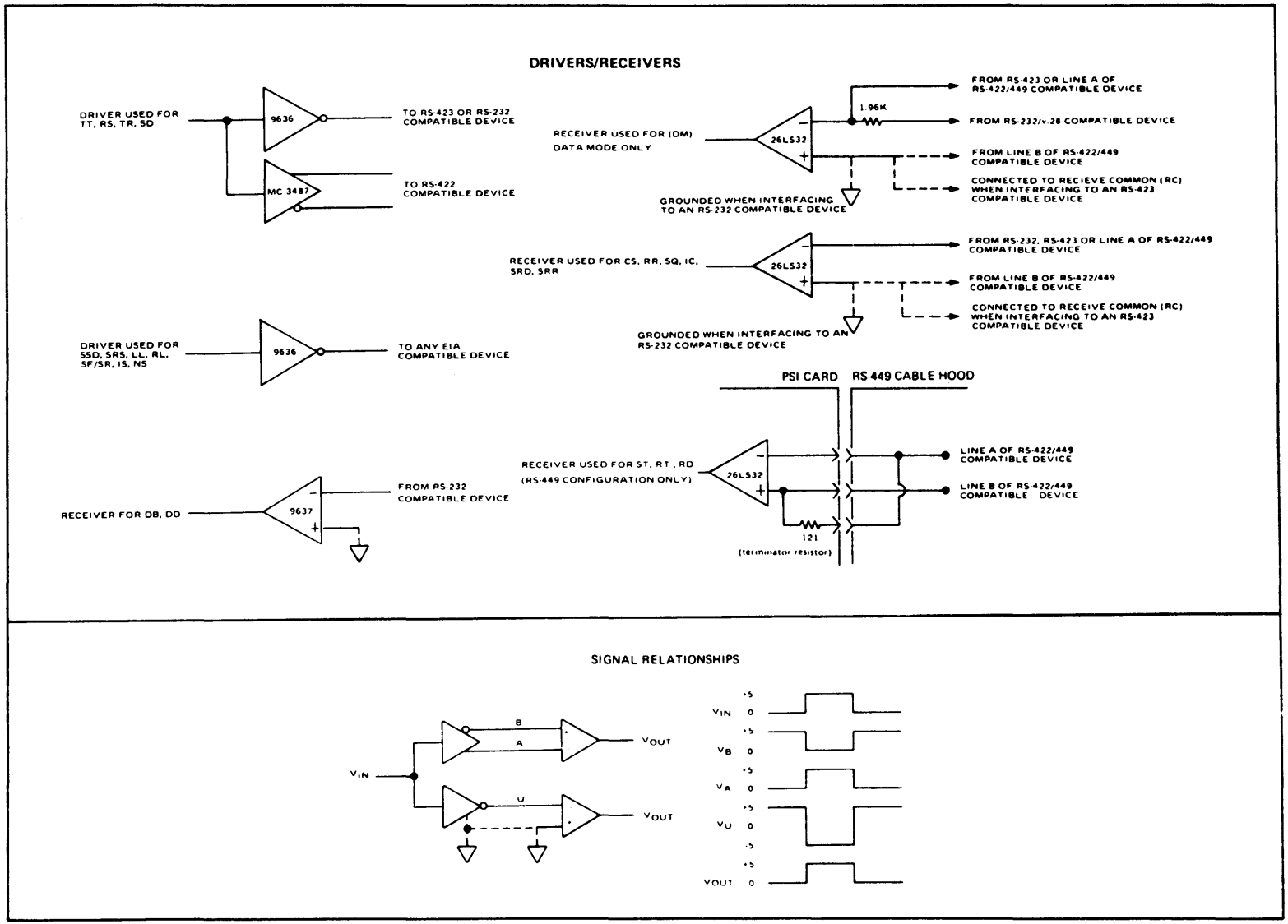


Figure 3-2. Driver/Receiver Combinations.

Maintenance
Chapter 4

This chapter provides maintenance information, including preventive maintenance instructions, for the M/E/F-Series PSI card.

Preventive Maintenance

There is no preventive maintenance (PM) necessary for the PSI card other than a routine inspection of the equipment which can be performed at the same time that PM is done for the entire system. The card should be checked for broken components, or the presence of foreign objects.

If installed, a self-test (residing in the firmware) is executed each time that power is applied to the card or the card is reset. In this manner the card is checked automatically, and only requires more thorough testing when specific failures occur.

Troubleshooting Techniques

CAUTION

ALWAYS TURN POWER OFF TO THE COMPUTER AND OTHER ASSOCIATED EQUIPMENT WHEN INSERTING OR REMOVING INTERFACE CARDS OR CABLES. FAILURE TO DO SO COULD RESULT IN DAMAGE TO THE EQUIPMENT.

CAUTION

STATIC SENSITIVE DEVICES

THE ROMS/EPROMS, RAMS, AND Z-80A COMPONENTS USED ON THIS CARD ARE SUSCEPTIBLE TO DAMAGE BY STATIC DISCHARGE. REFER TO THE SAFETY CONSIDERATIONS INFORMATION AT THE FRONT OF THIS MANUAL BEFORE REPLACING.

Once it has been determined that the PSI card is failing, proceed as follows to localize the failure to the specific component:

1. Check the card configuration as outlined in Chapter 2 of this manual.

2. If the card is being used with a Hewlett-Packard firmware product, a self-test (included in the firmware ROM/EPROM) will execute each time the power is turned on. This test examines Z-80A CPU operation, on-board DMA operation (channels 0 and 1), counter/timer performance, RAM and ROM/EPROM memory, and some parts of the driver/receiver circuits and Z-80A SIO. Refer to the firmware manual for any additional diagnostic tests.

3. If a failure is found using the above described tests, replace the failing card or firmware ROM/EPROM, and rerun the test that failed to ensure that the problem has been corrected. For information on repair or replacement of the failing components, contact the nearest Hewlett-Packard Sales and Service Office. (Sales and Service offices are listed at the back of this manual.) Each component (card or firmware ROM/EPROM) is handled separately by the HP service organization. Return only the failed part under the HP Assembly Exchange or Repair Program (if the card is defective, return it without the ROM/EPROM configuration jumpers or firmware EPROM/ROM).

4. If desired, further isolation to a defective part (other than the firmware ROM/EPROMs) may be performed. Such work is at the descretion of and under the responsibility of the customer. Refer to the servicing diagram information given in Chapter 6 of this manual and replaceable parts information given in Chapter 5.

Replaceable Parts
Chapter 5

This chapter contains information for ordering replaceable parts for the PSI card. Table 5-1 gives a list of replaceable parts, and table 5-2 contains the names and addresses of the manufacturers indexed by the code numbers used in table 5-1.

Replaceable Parts

Table 5-1 contains a list of replaceable parts in reference designation order. The following information is listed for each part:

1. Reference designation of the part.
2. The Hewlett-Packard part number.
3. Part number check digit (CD).
4. Total quantity (QTY).
5. Description of the part.
6. A five-digit manufacturer's code number of a typical manufacturer of the part. Refer to table 5-2 for a cross-reference of the manufacturers.
7. The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information on parts, address the order or inquiry to the local Hewlett-Packard Sales and Service Office (Sales and Support Offices are listed at the back of this manual).

To order a part, quote the Hewlett-Packard part number (with the check digit), and indicate the quantity required. The check digit will insure accurate and timely processing of your order.

Table 5-1. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
C1	0160-4832	4	1	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0180-0100	3	5	CAPACITOR-FXD 4.7UF +-10% 35VDC TA	56289	150D475X9035B2
C3	0180-0197	8	3	CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X9020A2
C4	0180-0100	3		CAPACITOR-FXD 4.7UF +-10% 35VDC TA	56289	150D475X9035B2
C5	0180-0100	3		CAPACITOR-FXD 4.7UF +-10% 35VDC TA	56289	150D475X9035B2
C6	0180-0100	3		CAPACITOR-FXD 4.7UF +-10% 35VDC TA	56289	150D475X9035B2
C7	0160-4835	7	18	CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C10	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C11	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C12	0180-0100	3		CAPACITOR-FXD 4.7UF +-10% 35VDC TA	56289	150D105X9035B2
C13	0180-0197	8		CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X9020A2
C14	0180-0197	8		CAPACITOR-FXD 2.2UF +-10% 20VDC TA	56289	150D225X9020A2
C15	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C16	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C19	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C20	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C21	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C22	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C23	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C24	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C25	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C26	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C27	0160-4835	7		CAPACITOR-FXD 0.1UF +-10% 50VDC CER	28480	0160-4835
C28	0160-4807	3	2	CAPACITOR-FXD 33PF +-5% 100FDC CER 0+-30	28480	0160-4807
C29	0160-4807	3		CAPACITOR-FXD 33PF +-5% 100FDC CER 0+-30	28480	0160-4807
CR1	1901-0518	8	2	DIODE-SM SIG SCHOTTKY	28480	1902-0518
CR2	1901-0518	8		DIODE-SM SIG SCHOTTKY	28480	1902-0518
CR3	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR4	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
CR5	1990-0662	0	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0662
CR6	1902-3002	3	1	DIODE=ZNR 2.37V 5% DO-7 PD=.4W TC=-.074%	28480	1902-3002
E1	0360-1682	0	3	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
F1	2110-0671	8	1	FUSE .125A 125V .281X.093	28480	2110-0671
F2	2110-0665	0	1	FUSE 1A 125V .281X.093	28480	2110-0665
F3	2110-0679	6	1	FUSE 1.5A 125V NTD .281X.093	28480	2110-0679
Q1	1853-0015	7	1	TRANSISTOR PNP SI PD=200MW FT=50MHZ	28480	1853-0015
Q2	1854-0019	3	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	0698-0082	7	4	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R2	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
R3	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-10000	24546	C4-1/8-T0-4640-F
R4	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-10000	24546	C4-1/8-T0-4640-F
R5	1810-0702	9	1	NETWORK-RES 10-SIP MULTI-VALUE	01120	110A2850/152
R6	1810-0279	5	4	NETWORK-RES 10-SIP 4.7K OHM X 9	01121	210A472
R7	1810-0279	5		NETWORK-RES 10-SIP 4.7K OHM X 9	01121	210A472
R8	0757-1094	9	6	RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R9	0757-0346	2	2	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0698-0082	7		RESISTOR 464 1% .125W F TC=0+-10000	24546	C4-1/8-T0-4640-F
R12	1810-0279	5		NETWORK-RES 10-SIP 4.7K OHM X 9	01121	210A472
R13	1810-0279	5		NETWORK-RES 10-SIP 4.7K OHM X 9	01121	210A472
R14	1810-0276	2	2	NETWORK-RES 10-SIP 1.5K OHM X 9	01121	210A152
R15	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R16	1810-0276	2		NETWORK-RES 10-SIP 1.5K OHM X 9	01121	210A152
R17	0698-3429	2	12	RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R18	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R19	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R20	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F

Table 5-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R21	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R22	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R23	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R24	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R25	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R26	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R27	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R28	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R29	0698-3429	2		RESISTOR 19.6 1% .125W F TC=04-100	03888	PME35-1/8-T0-19R6-F
R32	1810-0517	4	3	NETWORK-RES 10=SIP6.0K OHM X 9	28480	1810-0517
R33	1810-0517	4		NETWORK-RES 10=SIP6.0K OHM X 9	28480	1810-0517
R34	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R35	0757-0403	2	3	RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R36	0698-4590	0	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R37	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R38	0757-0403	2		RESISTOR 121 1% .125W F TC=0+-100	24546	C4-1/8-T0-121R-F
R39	1810-0517	4		NETWORK-RES 10=SIP6.0K OHM X 9	28480	1810-0517
R40	0757-0199	3	6	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R41	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R42	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R43	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R44	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R45	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R46	0757-0442	9	6	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R47	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R48	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R49	0757-0442	9	6	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R50	0757-0442	9	6	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R51	0757-1094	9		RESISTOR 1.47K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1471-F
R52	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R53	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R54	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R55	0698-0083	8	1	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
S1	3101-1983	9	1	SWITCH-RWR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-1983
U11	1820-2594	2	4	IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U12	1820-1729	3	2	IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U13	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U14	1200-0654	7	4	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654SELECTED
U15	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U21	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U22	1820-1298	1	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS251N
U25	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U26	1813-0129	0	1	IC DSC HYBRID	34344	SP6235B
	1200-0638	7	1	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
U27	1820-2096	9	1	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
U31	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U33	1820-2299	4	2	IC-Z80A DMA	28480	1820-2299
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U35	1816-1371	2	1	IC TTL S 2048 (2K) PROM 70-NS	01295	TBP18S22J (PER HP DWG)
U36	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U37	1820-1080	9	11	IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U38	1820-0799	5	1	IC DRVR TTL NAND DUAL 2-INP	01295	SN75452BP
U41	1820-2594	2		IC RCVR TTL LS LINE RCVR QUAD 2-INP	28480	1820-2594
U42	1820-1112	8	1	IC FF TTL LS D-TYPE PDS-EDGE-TRIG	01295	SN74LS74AN
U43	1820-2299	4		IC-Z80A DMA	28480	1820-2299
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U45	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U46	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U47	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U51	1820-2145	9	1	IC DRVR TTL LINE DRVR QUAD	04713	MC3487P
U52	1820-2024	3	1	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U55	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U56	1820-1440	5	1	IC LCH TTL I.S QUAD	01295	SN74LS279N
U57	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U61	1820-1244	7	2	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U62	1820-1729	3		IC LCH TTL LS COM CLEAR 8-BIT	01295	SN74LS259N
U63	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298

Table 5-1. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
U65	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U66	1820-1416	5	1	IC SCHMITT-TRIG LS INV HEX 1-INP	01295	SN74LS14N
U67	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U71	1820-1244	7		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
U72	1818-1396	5	8	IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0	8	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U74	1820-2301	9	1	IC-Z80A CTC	28480	1820-2301
	1200-0567	1	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U75	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U76	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U77	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U81	1820-2953	7	1	IC RCVR TTL S LINE RCVR DUAL	01295	UA9637ACP SELECTED
U82	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U85	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U86	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U87	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U91	1820-3778	6	6	IC DRVR TTL COMM EIA RS-423 DUAL	07263	9636ATC
U92	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0567	1	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U95	1820-0916	9	1	IC TTL S 256-BIT PROM 50-NS 3-S	18324	N82S123F
U96	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U97	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U101	1820-3778	6		IC DRVR TTL COMM EIA RS-423 DUAL	07263	9636ATC
U102	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U106	1820-1184	4	1	IC BFR TTL NOR QUAD 2-INP	01295	SN7428N
U107	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U201	1820-3778	6		IC DRVR TTL COMM EIA RS-423 DUAL	07263	9636ATC
U202	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
	1200-0567	1	3	SOCKET-IC 28-CONT DIP DIP-SLDR	28480	1200-0567
U206	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS74N
U207	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U301	1820-3778	6		IC DRVR TTL COMM EIA RS-423 DUAL	07263	9636ATC
U302	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U303	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U304	1820-2075	4	1	IC MISC TTL LS	01295	SN74LS245N
U306	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS74N
U307	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U401	1820-3778	6		IC DRVR TTL COMM EIA RS-423 DUAL	07263	9636ATC
U402	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U403	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
U404	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U406	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS74N
U407	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
U501	1820-3778	6		IC DRVR TTL COMM EIA RS-423 DUAL	07263	9636ATC
U502	1818-1396	5		IC NMOS 16384 (16K) DYN RAM 100-NS	S0545	UP416C-2 (SELECTED)
	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
U503	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
U504	1826-0220	9	1	IC V RGLTR TO-39	27014	LM320H-05
	1200-0185	9	1	INSULATOR-XSTR NYLON	28480	1200-0185
U506	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS74N
U507	1820-1080	9		IC DRVR TTL LINE DRVR DUAL 6-INP	01295	SN75121N SELECTED
W6	8159-0005	0	1	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XW1	1200-0483	0	1	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0483
	1251-1556	7	8	CONNECTOR-SGL CONT SKT .018-IN-BSC-SZ	28480	1251-1556
	1258-0124	7	2	PIN-PROGRAMING DUMPER .30 CONTACT	91506	8136-475G1
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	5040-6001	4	1	EXTRACTOR-PC	28480	5040-6001
	5040-6065	0	1	EXTRACTOR-RED	28480	5040-6065

Table 6-4. Code List of Manufacturers

Mfr Code	Manufacturer Name	Address		Zip Code
S0545	NIPPON ELECTRIC CO	TOKYO	JP	
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND COMPNT DIV	DALLAS	TX	75222
03888	K D I PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMINONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
18324	SIGNETICS CORP	SUNNYVALE	CA	94042
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34344	MOTOROLA INC	FRANKLIN PARK	IL	60131
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
91506	AUGAT INC	ATTLEBORO	MA	02703

Servicing Diagrams
Chapter 6

This chapter contains a parts location diagram and schematic logic diagram for the PSI card.

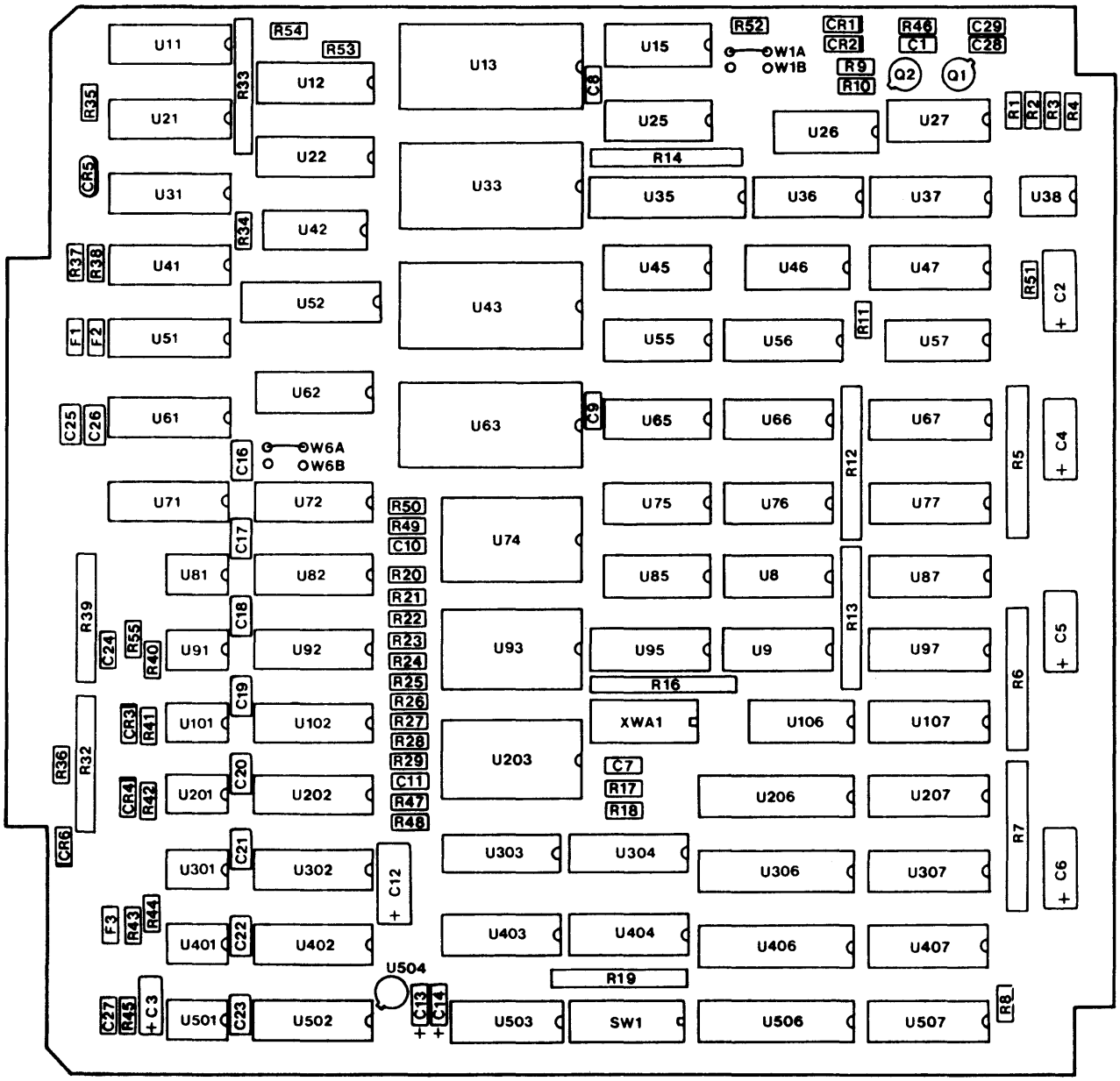


Figure 6-1. M/E/F-Series PSI Parts Location Diagram

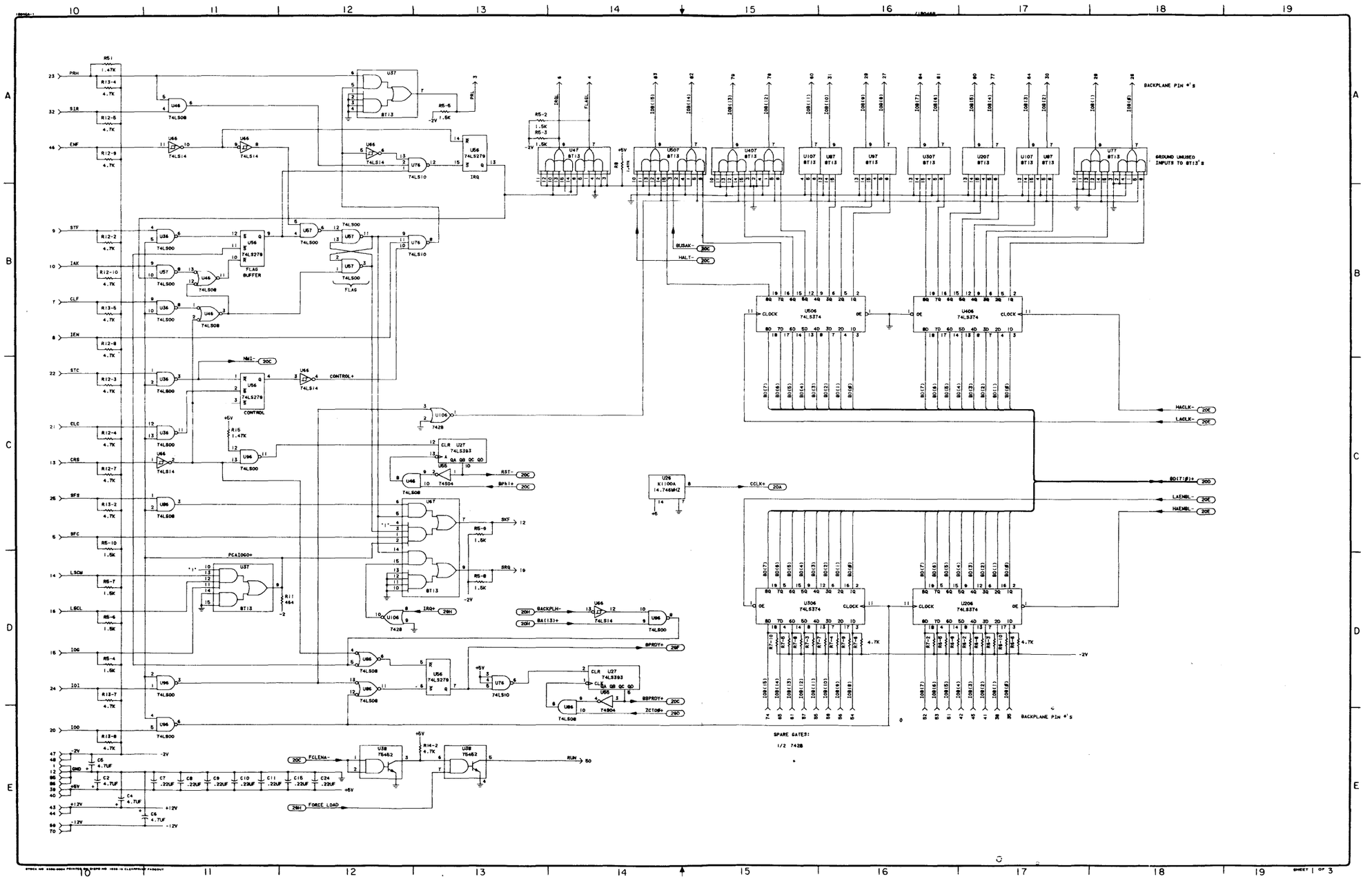


Figure 6-2. M/E/F-Series PSI Schematic Logic Diagram (Sheet 1 of 3)

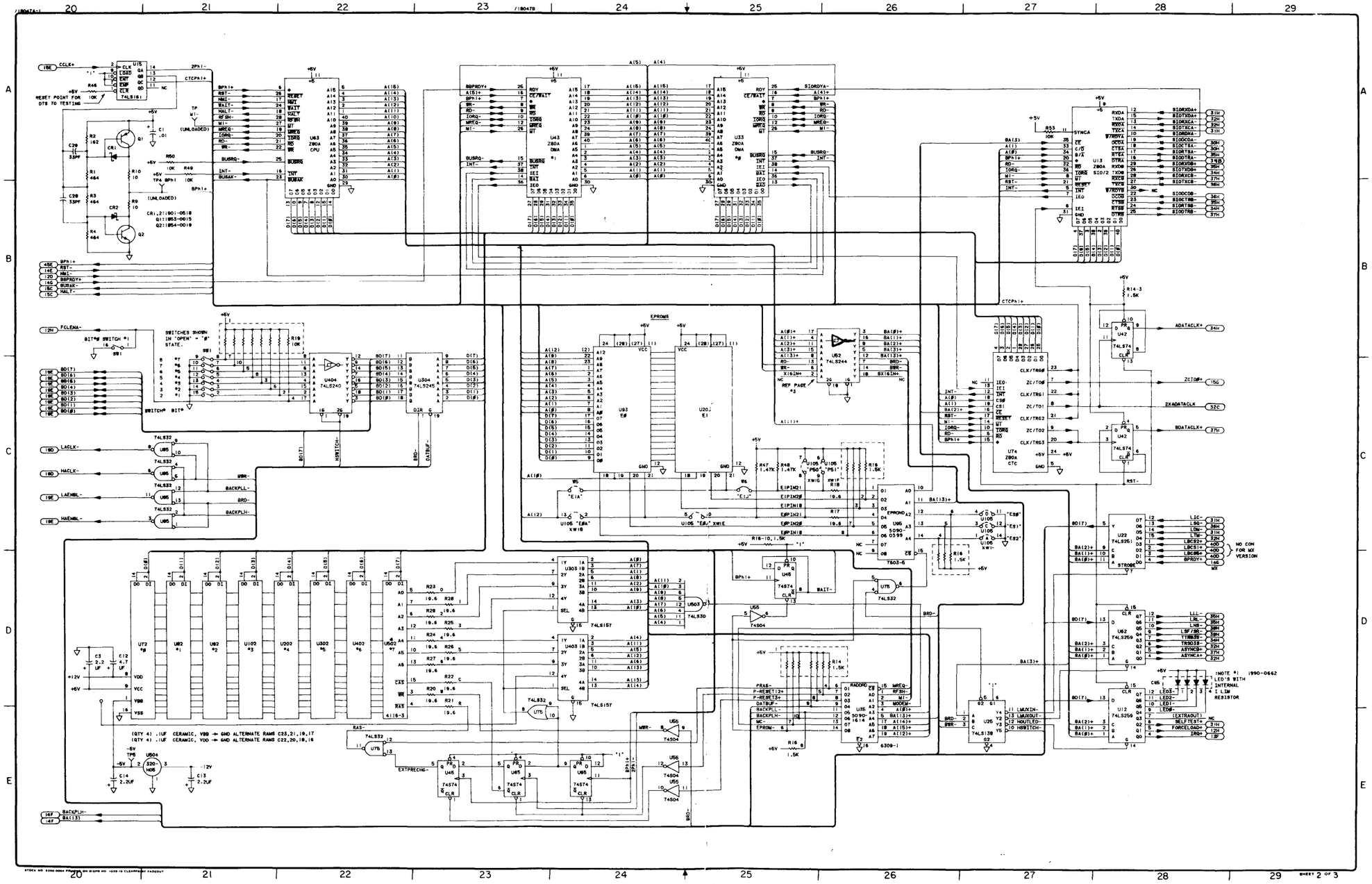


Figure 6-2. M/E/F-Series PSI
Schematic Logic Diagram
(Sheet 2 of 3)
6-5/6-6

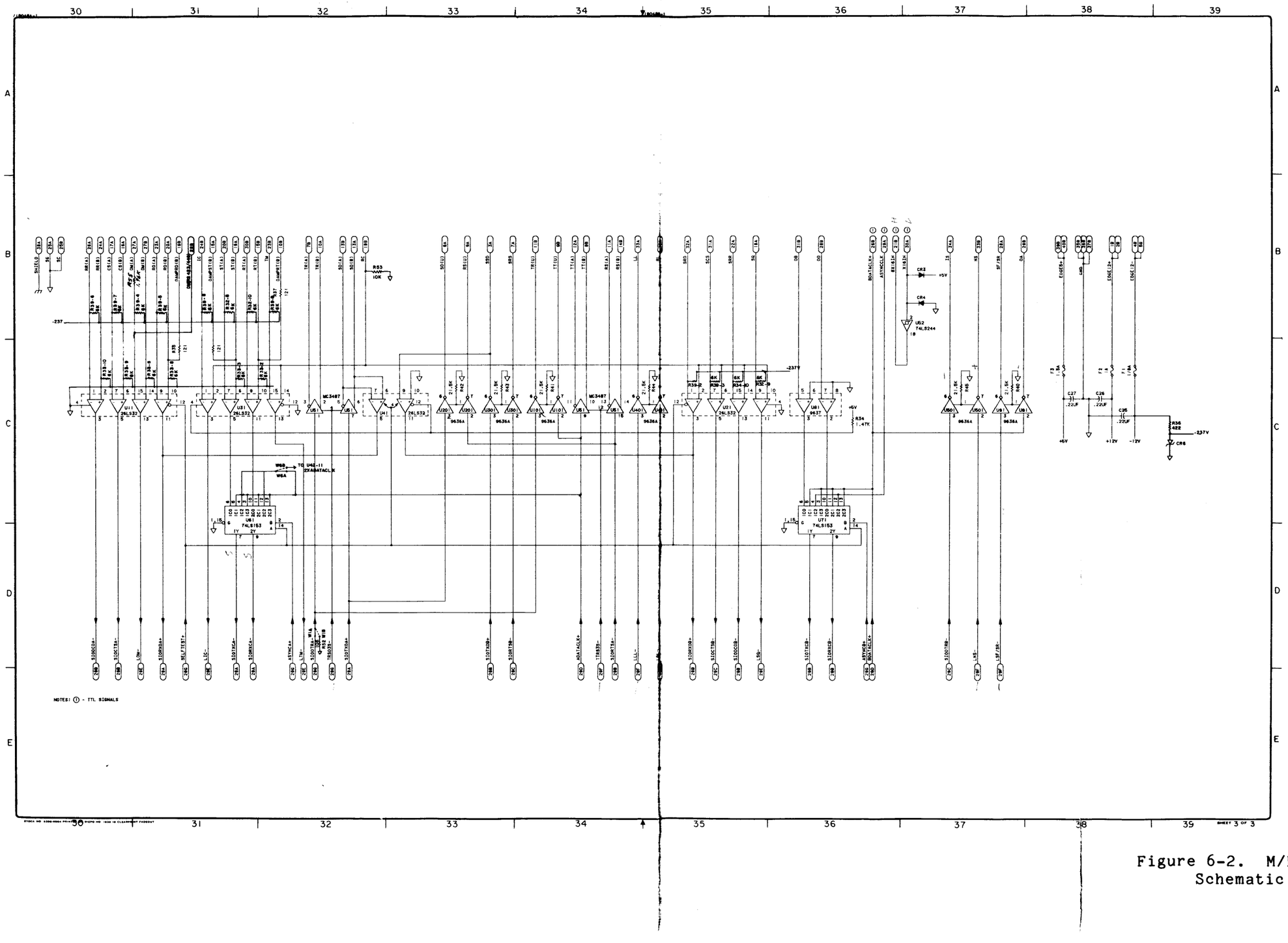


Figure 6-2. M/E/F-Series PSI Schematic Logic Diagram (Sheet 3 of 3) 6-7/6-8

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